UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Dell Inc., and Cisco
Petitioners

v.

Corrigent

Case No. IPR2023-00464

U.S. Patent No. 6,957,369

Declaration of Nader F. Mir, Ph.D.
In Support of Petitioners in the
Petition for *Inter Partes* Review of U.S. Patent No. 6,957,369

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I. INTRODUCTION

1. I, Nader F. Mir, have been retained by Gibson, Dunn & Crutcher LLP on behalf of Petitioners Dell Technologies Inc., Dell Inc., and Cisco, as an independent expert in this Petition for *inter partes* review by the U.S. Patent and Trademark Office. As part of my engagement, I have been asked to provide analysis and expert opinions on the following topics: (1) the disclosure of the U.S. Patent No. 6,957,369 ("the '369 patent"); and (2) the invalidity of claims 1–26.

II. BASIS FOR OPINIONS

A. Qualifications

2. I am a tenured professor in the Electrical Engineering Department of San Jose State University, California, where I also held the position of Associate Chair from 2006 through 2008. I have been a faculty member at San Jose State University since 2001.

3. In 1995, I received a Ph.D. in electrical engineering from Washington University, St. Louis. I received an M.Sc. degree in electrical engineering in 1990, also from Washington University. In 1985, I received a B.Sc. in electrical engineering from Polytechnic University.

4. I have over 30 years of experience with computer networks and communication systems, including both industry and academic experience. Before my current position at San Jose State University, I was an Assistant Professor in the

Department of Electrical and Computer Engineering at the University of Kentucky. I joined San Jose State University in 2001 as an Associate Professor. Since 2005, I have been a Full Professor in the Electrical Engineering Department at San Jose State University, where I perform research and teach in the areas of computer networks, networking devices, switches, routers, virtualization, virtual switches, cloud computing, software-defined networking in clouds, and cloud data centers.

5. I hold several technical editorial positions for various journals, including *IEEE Communications Magazine*. As a Technical Editor of *IEEE Communications Standards Magazine* for Cloud and Edge Computing, I am responsible for accepting or rejecting scientific articles submitted to the journal in the areas of computer networking focusing on cloud systems. From 2005 through 2020, I held the technical editorial position for *IEEE Communications Magazine*. I am a senior member of the IEEE and have served as a member of the technical program committees and the steering committees for a number of major IEEE communications and networking conferences.

6. For more than 30 years, I have conducted research in the areas of computer and communication networks; networking devices; protocols including (but not limited to) packet-switched networks, cloud and edge computing, software-defined networking in cloud systems, integrated voice, video, data center networks, TCP/IP, client/server operations, content delivery networks, multimedia and

streaming, client/server, networking traffic flow analysis, wireless/mobile networks, networking devices, network security, and network virtualization, among others.

7. I have received a number of university awards as well as national and international awards. In particular, I have received a number of research grants from private, state, and governmental funding agencies for conducting research in the fields of computers and communication networks. I am also the recipient of several university teaching recognition awards from San Jose State University; several research excellence awards; and the school's published book award for the year.

8. Before my positions in academia, I worked in various positions in the telecommunication and computer network industries. From 1985 to 1988, I was a Telecomm R&D Engineer at the Telecommunication Research & Development Center (TRDC) in Surrey, England. In particular, I headed engineering projects in the area of telecommunication engineering. I also participated in the design of a high-speed switch for digital Private Branch Exchange (PBX) and SS7 networks. In 1991, I worked as an Electrical Engineering Consultant for Bussmann Company, where I instructed engineers on electrical engineering topics and prepared them for the National Principles and Practice of Engineering (PE) exam. From 1989 to 1995, I worked as a Computer/Communications Chip-Design Engineer at the Computer & Communications Research Center in St. Louis, Missouri. In that position, I designed a VLSI gigabit switch control plane chip for a high-speed computer network using

CMOS technology. From 1995 to 1996, I was a Research Scientist Engineer at Advanced Telecommunications Institute, Stevens Institute of Technology in Hoboken, New Jersey. There I headed analyzing communications and high-speed computer networking projects.

9. Since obtaining my Ph.D., I have served in various consulting positions in the area of computer networking technology and communication engineering, including for CITS Inc. in San Jose, California (2012–2013), Morrison & Foerster LLP in San Francisco, California (2015–2016), and Butler and Snow in Jackson, Mississippi (2017–2018).

10. I have authored or co-authored over 100 articles in peer-reviewed journals, conference proceedings, texts, and monographs in the aforementioned areas of computer networking, communications, and related fields. I have published two textbooks, one of which is entitled "*Computer Communication Networks*." This textbook has been adopted by numerous universities worldwide.

11. I am a named inventor on one U.S. patent, which relates to a packet-switching network and method of routing packets.

12. I have served as an expert witness and technical consultant in litigation and *inter partes* review matters concerning computer networks, wireless networks at both the protocol and hardware levels, and telecommunications.

13. I attach as Exhibit 1004 my curriculum vitae ("CV"), which includes a more detailed list of my qualifications. My CV also contains a list of all other cases in which, during the previous four years, I testified as an expert at trial or by deposition.

B. Preparation for This Declaration

14. All of the opinions that I state in this declaration are based upon my own personal knowledge and professional judgment. If called upon to testify as a witness during any proceeding, I am willing and able to competently testify as to anything contained in this declaration.

15. In forming my opinions, in addition to my own knowledge, experience, and expertise, I have reviewed and relied upon: (1) the '369 patent; (2) the file history of the '369 patent; and (3) the prior art references cited in this declaration.

16. I am being compensated for my work on this declaration at my standard consulting rate and I am being reimbursed for any expenses I may incur. My compensation is not contingent upon the results of my analysis, the substance of my testimony, or the outcome of this petition.

C. Level of Ordinary Skill in the Art

17. In my opinion, as it relates to the '369 patent, a person of ordinary skill in May 2002 would have had at least a bachelor's degree in computer science, computer engineering, or electrical engineering and two to three years of work

experience related to administering distributed computing environments. This experience might have included, for example, experience in cloud networks design and analysis, client-server, cloud controller communication analysis and evaluation, load balancing, virtualization, latencies optimization, and managing physical and virtual computing environments in clouds. A master's degree or higher would have been acceptable in place of the work experience described above.

18. I meet the criteria described above and believe myself to be a person with at least ordinary skill in the art pertaining to the '369 patent. I would have qualified as such a person by at least May 30, 2002, which I understand is the earliest priority date of the '369 patent.

III. Legal Understandings

19. In this section, I describe my understanding of certain legal standards that I may have relied upon in forming my opinions set forth in this declaration. I have been informed of these legal standards by Petitioners' attorneys. Although I am not an attorney and have not researched the law on patent invalidity, I have formed the following understanding about the legal standards through Petitioners' attorneys.

A. A Person of Ordinary Skill in the Art

20. It is my understanding that a person of ordinary skill in the art ("POSITA") is a hypothetical person who is used to analyze the prior art without the

benefit of hindsight. A person of ordinary skill in the art is presumed to be one who uses conventional wisdom in the art, but does not undertake to innovate, either by extraordinary insights or by systematic research.

21. I further understand that the hypothetical POSITA is presumed to have knowledge of all references that are sufficiently related to one another and to the pertinent art, and to have knowledge of all arts reasonably pertinent to the particular problem that the claimed invention purports to address.

B. Legal Standard for Prior Art

22. It is my understanding that a patent, published patent application, or other publication, must first qualify as prior art before it can be used to invalidate a patent claim.

23. I further understand that a U.S. or foreign patent qualifies as prior art to a patent claim if the date of application, issuance, and/or publication of the prior art patent is prior to the purported date of invention of the patent claim.

24. I understand that a printed publication, such as a technical publication, a magazine article, or newsgroup post, qualifies as prior art to a patent claim so long as the date of publication is prior to the purported date of invention of the patent claim.

25. It is my understanding, moreover, that a U.S. patent qualifies as prior art to a patent claim if the application for the prior art patent was filed in the United States before the purported date of invention of the patent claim.

C. Claim Construction

26. I understand that the USPTO recently issued a new final rule addressing the claim construction standard applied during *inter partes* review ("IPR"). The new rule replaces the "broadest reasonable interpretation" standard with the same standard that is used during claim construction in district court civil actions, with which I am familiar. I understand that this new rule applies to the IPR petition filed concurrently herewith, which means that claim construction in this IPR will be governed by the same claim construction standards utilized in district court.

27. I understand that, in the district court context and in this IPR, the words of a claim are generally given their ordinary and customary meaning. This is the meaning the term would have to a person of ordinary skill in the art in question at the time of the invention, which generally means the time the application was filed.

28. I further understand that the specification informs the proper interpretation of a claim. This is because a POSITA is deemed to have read the claim term not only in the context of the particular claim in which the disputed term appears, but also in the context of the entire patent, including the specification. I understand that the prosecution history and extrinsic evidence concerning relevant

scientific principles, the meaning of technical terms, and the state of the art are also considered in ascertaining the meaning of claim terms.

D. Legal Standard for Anticipation

29. I understand that, once the claims of a patent have been construed, the second step in determining anticipation of a patent claim requires a comparison of the construed claim language to the prior art on a limitation-by-limitation basis.

30. It is my understanding that a prior art reference anticipates a claim, and thus renders the claim invalid, if all elements of the claim are disclosed in the prior art reference, either explicitly or inherently.

31. I further understand that, under Section 102 of the Patent Act, claims of a patent are invalid for lack of novelty if they are anticipated by a single prior art reference. I have been informed by counsel that a claimed invention is invalid as anticipated and hence lacks novelty if all of the limitations of the claim as construed by the Court are present in a prior art reference. It is my understanding, however, that a limitation of the claim need not be shown directly in a reference so long as a POSITA would have understood the limitation to be inherent or necessarily present in the reference.

E. Legal Standard for Obviousness

32. I understand that an invention may also be obvious, even though the invention is not identically disclosed or described in a single prior art reference,

which is required for anticipation. This is true if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the relevant art.

33. I understand the Supreme Court has urged caution in granting a patent based on the combination of elements found in the prior art. This is because a patent for a combination that only unites old elements with no change in their respective functions withdraws what already is known from the public, giving it exclusively to the patentee. The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

34. I further understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, the invention is likely obvious. For the same reason, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Put another way, a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions. I understand that this is a flexible standard and it is not confined to any particular formalistic conception.

35. I understand that, when conducting an obviousness inquiry, the analysis should consider the scope and content of the prior art, differences between the prior art and the claims of the challenged patent claims, and the level of ordinary skill in the art. Secondary considerations of nonobviousness can also be considered. Secondary considerations include commercial success enjoyed by devices practicing the patented invention, industry praise for the patented invention, copying by others, and the existence of a long-felt but unsatisfied need for the invention. I understand that there must be a nexus between these factors and the claims themselves for these secondary considerations to impact the analysis of obviousness.

36. I understand that there generally must be a motivation to combine the references in order to find obviousness. This motivation or reason to combine can arise from the references themselves, changing market dynamics, or from simple common sense.

37. I understand that a single reference can render a patent claim obvious, even if that reference does not fully anticipate the claim. To determine whether there was an apparent reason to combine the known elements in the way a patent claims, it will often be necessary to look to interrelated teachings of multiple patents; to the effects of demands known to the design community or present in the marketplace; and to the background knowledge possessed by a person having ordinary skill in the art.

IV. TECHNOLOGY BACKGROUND

38. To put in context my opinions on the validity of the claims of the '369 patent, in this section I provide a brief discussion of the relevant technological background, which relates to testing electronic systems on failure, network switches, and device backplanes.

39. Network switches in May 2002 were broadly available for a wide range of communication services including for use in self-testing systems. With switches, data units known as "packets" can be forwarded from an input port to an output port of a switch so that the associated links attached to physical ports can exchange data. A packet consists of a "payload" containing an application's information being carried by the packet and a "header" consisting of routing and control information. A switch can then be deployed for any application included in its payload. One can forward, for example, test packets to various parts of an electronic system and receive a response packet containing the information that detects a failing or idle equipment during.

40. The process of switching and forwarding of a test packet by a switch is essentially identical to the switching and forwarding process of any other types of packets such as email packets. The process of packet switching requires performing a lookup table operation for each incoming packet to find a matching output port number for the packet. This operation was well known in the priority date for the

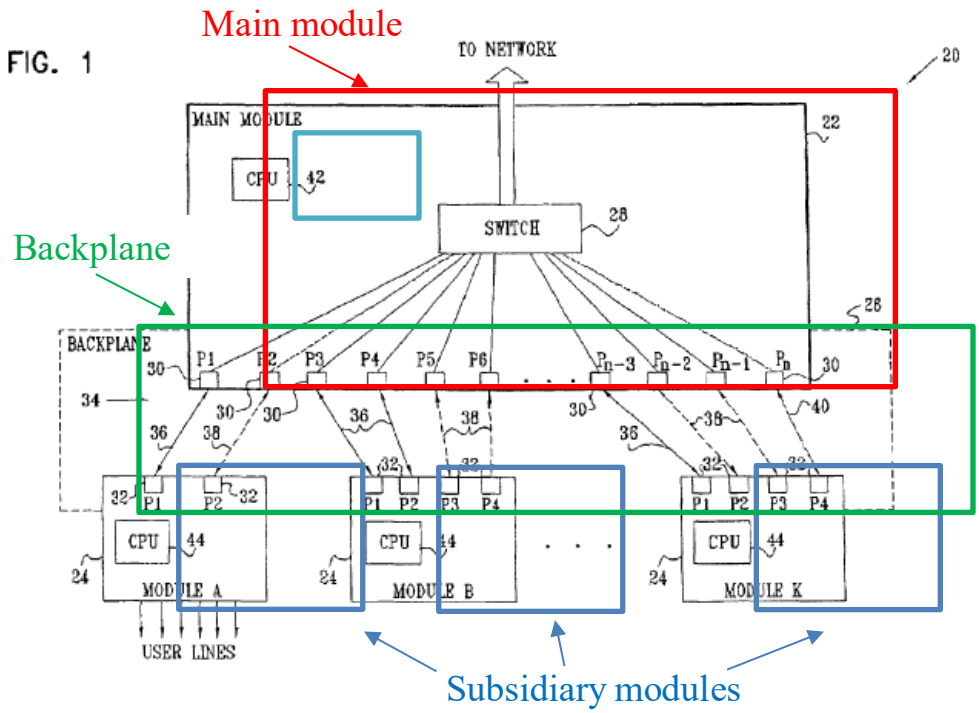
’369 patent and the process was independent of the application carried by a packet whether the purpose of the packet switching was for testing electronic components or a typical known Internet application such as email.

41. Systems with backplane configurations were also well known in May 2002. During this time frame, it arose from the demand by computer and communication manufacturing companies for better system maintenance that led to a backplane-based structure. In a backplane-based structure, a main module called backplane is interconnected by a core network to several other modules (boards) making the system maintenance and fault detection more convenient. A line card-based internal organization of an Internet router that was widely available in May 2002 can be a good example of such system structure. U.S. Patent No. 5,841,788 (“Ke”), filed in 1996 is another exemplary prior art disclosing methods for backplane interconnect to various modules. *See* Ex. 1008. Ke describes that a system structured with a backplane may be dynamically configurable, “the position of boards on the backplane can change and boards can be removed or added.” Ex. 1008, 1:37–39.

42. All of the concepts discussed in this section were well known and widely used well prior to the May 30, 2002 priority date for the ’369 patent. For example, I taught these concepts to undergraduate electrical engineering and computer science majors for several years prior to May 30, 2002.

V. The '369 PATENT

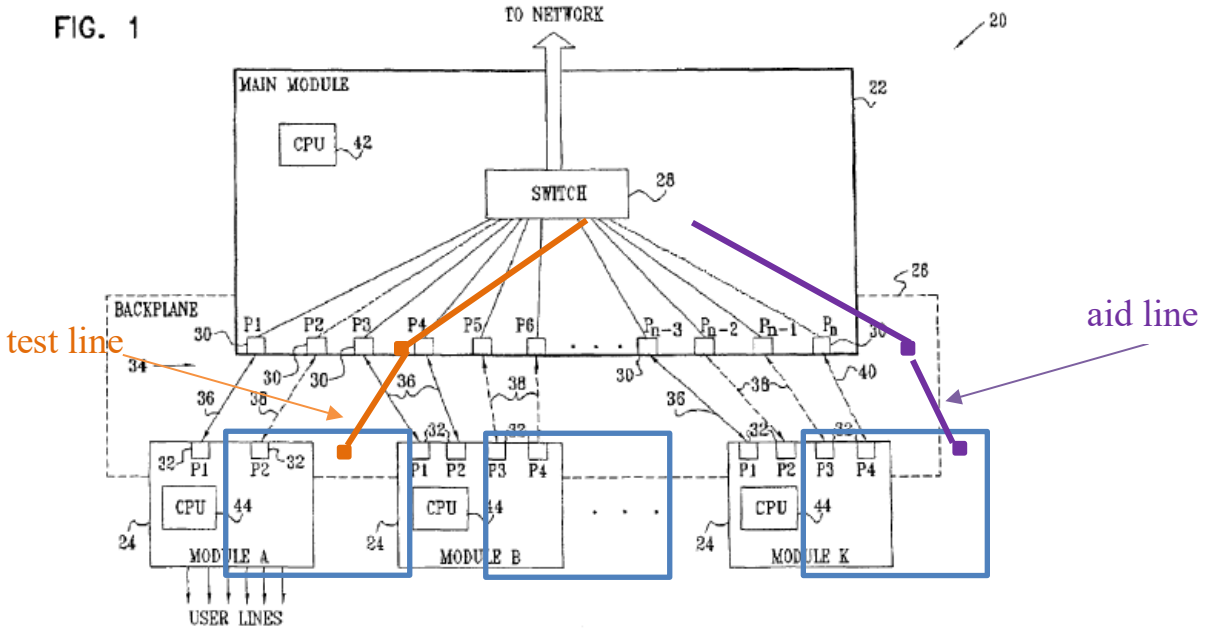
43. The '369 patent describes an electronic system which comprises of a "main module" and two or more "subsidiary modules." Ex. 1001, 4:54–67. Each subsidiary module is connected via a backplane to the main module. Ex. 1001, 4:54–67. The main module contains a switch, multiple ports, and a system control processor. Ex. 1001, 4:54–67; 5:41–45. Figure 1 (annotated below) depicts this arrangement:



44. The patent describes a method (and apparatus) to test the electronic system's idle lines. Ex. 1001, 5:55–6:39. The patent explains that testing idle lines is important because failures in these idle lines will go undetected until the line is needed. Ex. 1001, 1:11–24. The patent also explains that testing idle lines is ideal

because the test will not interrupt normal operation of the active components. Ex. 1001, 1:11–24.

45. The ’369 patent discloses a six-step method. First, the system control processor of the main module selects an idle line that connects a subsidiary module to a port of the switch of the main module in order to loop the test traffic through. Ex. 1001, 5:61–67. This line is called an “aid line” 40. Ex. 1001, 5:61–67. Next, the system control processor instructs the subsidiary module to loop back all traffic via the aid line. Ex. 1001, 5:63–6:9. Then, the system control processor selects another idle line connected to a different subsidiary module to be the test line 38. Ex. 1001, 6:10–13. Then, the system control processor configures the switch to connect the aid line and the test line. Ex. 1001, 6:14–17. Next, the system control processor tells the second subsidiary module to send test traffic. Ex. 1001, 6:18–22. Finally, it is reported if the test traffic did not return in a timely manner or intact. Ex. 1001, 6:23–39. This loop is demonstrated below:



A. Summary of the Prosecution History of the '369 Patent

46. The '369 patent's application was filed on May 30, 2002. Ex. 1001, [22]. The examiner rejected claims 1–20 under 35 U.S.C. §112 for failing to distinctly claim the subject matter. Ex. 1002, 67. The Examiner also rejected claims 1 and 8 for "omitting essential steps" and claims 1 and 15 for the being "unclear on whether the limitations following the phrase [were] part of the claimed invention." Ex. 1002, 67–68. The Examiner also rejected claims 1–4, 6–9, and 11–14 as anticipated by U.S. Patent No. 6,028,845 ("Serikawa") and over Serikawa in view of U.S. Patent No, 5,541,862 ("Bright"). Ex. 1002, 68.

47. The Applicant requested in an interview and it was discussed that an amendment of "wherein the test traffic is conveyed via the switch to the aid line

connecting to the first subsidiary module" would overcome the prior art challenge. In addition, the Applicant argued the prior art did not disclose a loopback test via a switch. Ex. 1002, 98–99. In the Applicant's remarks, the Applicant argued that the invention was innovative because it allowed to test subsidiary modules of different types and different formats. The Applicant also removed the "may be" and "adapted" language to overcome §112 objections. Ex. 1002, 87–95. The Examiner allowed the claims, and the patent issued on October 18, 2005. Ex. 1002, 111; Ex. 1001, [45].

B. Overview of the Challenged Claims

48. There are four independent claims in the '369 patent: claims 1, 8, 15, and 21. Claims 1 and 8 are system claims and claims 15 and 21 are apparatus claims.

49. I understand that Petitioners are challenging all of the claims in the '369 patent (the "Challenged Claims"). I have analyzed each of these claims.

1[pre]	In an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least 5 some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system, comprising:
1[a]	selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line;
1[b]	instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line

1[c]	selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module;
1[d]	configuring the switch to link the first and second ports;
1[e]	transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein 20 the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module; and
1[f]	reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.
2	A method according to claim 1, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.
3	A method according to claim 2, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.
4[a]	A method according to claim 1, further comprising: selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and
4[b]	repeating the configuring the switch, transmitting the test traffic, and reporting that the failure has occurred with respect to the further idle lines until all the idle lines have been tested.
5	A method according to claim 1, wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.
6	A method according to claim 1, wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic.

7	A method according to claim 6, wherein transmitting the test traffic comprises testing the second idle line while continuing to use the lines that are not idle for carrying the data to the network communication trunk.
8[pre]	In an electronic system that includes a main module and multiple subsidiary modules, each of said multiple subsidiary modules being connected to the main module by one or more lines for carrying data, a method for self-testing the system, comprising:
8[a]	selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats;
8[b]	instructing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module;
8[c]	configuring the main module to connect the first and second subsidiary modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module; and
8[d]	testing the system by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.
9	A method according to claim 8, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.
10	A method according to claim 8, wherein the main module and subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.
11	A method according to claim 8, wherein the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module.

12	A method according to claim 11, wherein testing the system comprises testing one or more of the lines of the second subsidiary module while continuing to use at least some of the lines that are not under test for carrying the data from the subsidiary modules to the network communication trunk
13	A method according to claim 8, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.
14	A method according to claim 13, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.
15[pre]	Modular electronic apparatus, comprising:
15[a]	a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;
15[b]	a main module, plugged into the backplane, the main module comprising a switch having ports for connection to the traces of the backplane;
15[c]	at least first and second subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces, at least some of which traces are sometimes idle; and
15[d]	a system control processor, which is operative to select a first idle trace among idle traces connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace, to instruct the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid trace, to select for testing a second idle trace among the idle traces connecting the second subsidiary module to a second port of the switch on the main module, and to configure the switch to link the first and second ports, the system control processor being further operative to cause test traffic to be transmitted over the second idle trace from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid trace connecting to the first subsidiary module, and to report that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

16	Apparatus according to claim 15, wherein the first subsidiary module is configured, under control of the system control processor, to loop back the traffic on the aid trace to the main module substantially without processing data comprised in the test traffic.
17	Apparatus according to claim 16, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.
18	Apparatus according to claim 15, wherein the system control processor is operative to select one or more further idle traces for testing among the idle traces in the system, wherein the further idle traces connect to further ports of the switch on the main module, and to repeatedly configure the switch, cause the test traffic to be transmitted, and report the failure when it occurs with respect to the further idle traces until all the idle lines have been tested.
19	Apparatus according to claim 15, wherein the switch is configured to connect the traces to a network communication trunk, and wherein the traffic comprises communication traffic.
20	Apparatus according to claim 19, wherein the test traffic is transmitted over the second idle trace while continuing to use the trace that are not idle for carrying the data to the network communication trunk.
21[pre]	Modular electronic apparatus, comprising:
21[a]	a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;
21[b]	a main module, plugged into the backplane;
21[c]	a plurality of subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces; and

21[d]	a system control processor, which is operative to select first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats, and which is further operative to test the modules by causing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module, by configuring the main module to connect the first and second subsidiary modules, so that a traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module, and by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.
22	Apparatus according to claim 21, wherein the first subsidiary module is configured to loop back the traffic to the main module substantially without processing the data comprised in the test traffic.
23	Apparatus according to claim 21, wherein the main module comprises a switch, which is coupled to connect the traces to a network communication trunk, and wherein the system control processor is operative to configure switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module during the test.
24	Apparatus according to claim 23, wherein the system control processor is operative to test one or more of the traces connected to the second subsidiary module while at least some of the traces that are not under test continue to be used for carrying the data from the subsidiary modules to the network communication trunk.
25	Apparatus according to claim 21, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.
26	Apparatus according to claim 25, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

50. For the reasons I detail below, it is my opinion that each of these claims is unpatentable over the prior art discussed below.

VI. Prior Art Considered

51. In this declaration, I provide four prior art references (among others) with exemplary citations identifying the relevant features related to the claim language of the Challenged Claims. I have also described combinations of these prior art references that, when combined, render the Challenged Claims obvious. It is my opinion that the Challenged Claims are anticipated and/or rendered obvious in light of the prior art specifically discussed in this declaration.

52. The citations presented in the body of this declaration correspond to the teachings disclosed in exemplary items of prior art that identify: (1) the problem(s) confronted by one of ordinary skill in the art; (2) an express suggestion to make one or more of the combinations; (3) an implicit suggestion to make one or more of the combinations; or (4) the knowledge of those skilled in the art as to the applicable field of technology.

A. Identification of the Primary Prior Art References

53. It is my opinion that a person of ordinary skill would consider at least the prior art references below:

Prior Art Reference	Qualifying Date	Exhibit No.
U.S. Patent No. 5,841,788 ("Ke")	11/24/1998	1008

U.S. Patent No. 4,685,102 ("Lewis")	8/4/1987	1009
U.S. Patent No. 4,074,352 ("Cook")	2/14/1978	1010
U.S. Patent Pub. No. 2003/0101426 ("Sarkinen")	11/27/2001	1011

54. Other references and knowledge described earlier in this declaration are relevant to show the state of the art – i.e., what a person of ordinary skill would have known when using the references identified above, or to use in combination with the references above to render the Challenged Claims invalid. The references include, but are not limited to:

- Braden, R., Ed., "Requirements for Internet Hosts - Communication Layers" STD 3, RFC 1122, DOI 10.17487/RFC1122, October 1989, <https://www.rfc-editor.org/info/rfc1122>. ("RFC 1122") (Ex. 1012).
- William Stallings, Data & Computer Communications 236 (6th ed. 2000) (Ex. 1013)

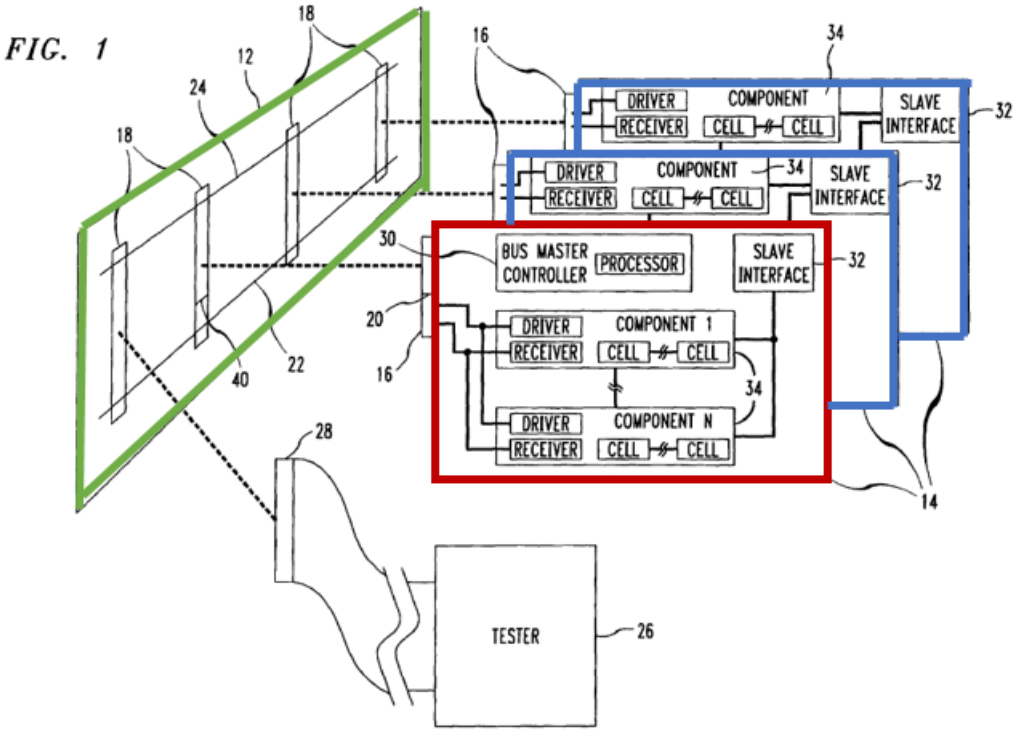
B. General Overview of the Primary Prior Art References

55. The following sections provide a brief description of the anticipating prior art systems and software that invalidate the '369 patent. This discussion is not meant to be exhaustive, and my full element-by-element analysis is provided in more detail below in the analysis section. I have personally reviewed the references cited

in this declaration. It is my opinion that Ke, Lewis, Cook, and Sarkinen each disclose or suggest the features of the Challenged Claims.

1. Ke

56. Ke involves a method for testing traces in a backplane. Ex. 1008, Abstract. The electronic system in Ke has a master board with bus master controller 30, and other boards with slave interfaces 32 which are all plugged into a backplane. Ex. 1008, 3:24–36. The bus master controller 30 performs a test of the backplane by driving the other boards through their slave interfaces. Ex. 1008, 3:24–36.

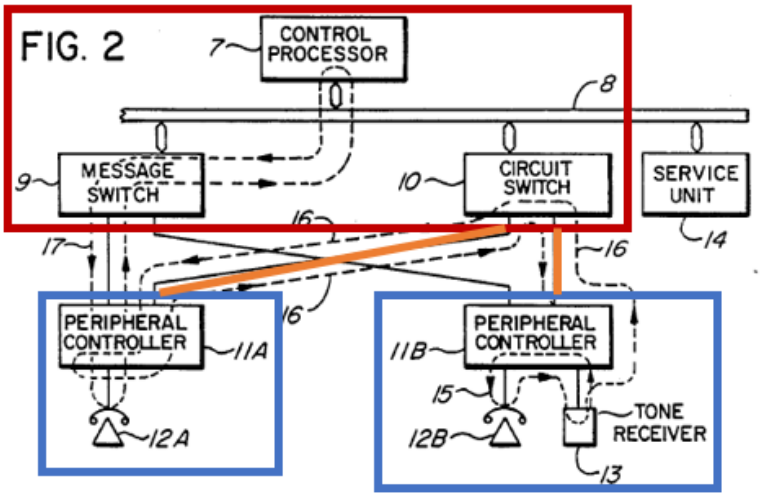


57. Ke states that there are different ways to test backplanes. Ex. 1008, 1:30–2:18. However, Ke discloses a new way a connection is tested one way at a

time by toggling the connections on and off to test one connection at a time. Ex. 1008, 3:61–4:40. After an error is detected, it is reported. Ex. 1008, 4:1–12.

2. Lewis

58. Lewis discloses switching system testing which utilizes a circuit loop to test switches, loops, and links. Ex. 1009, Abstract, 1:25–35. Lewis discloses a test in which circuit switch 10, which is able to communicate with a control processor 7 and message switch 9, sets up a loop to test peripherals 12A and 13. Ex. 1009, 3:47–53, 4:23–25. For example, the circuit switch sets up a loop 16 that connects peripheral 12A with peripheral 13 through the circuit switch 10.

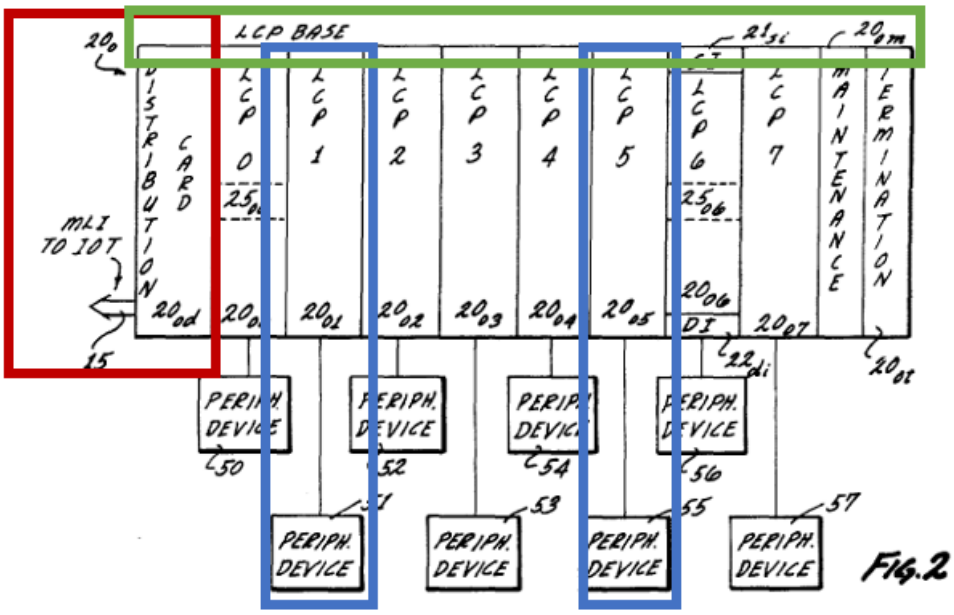


59. The control processor sends a message to peripheral 12A. This triggers a loopback test, which then travels via loop 16 to circuit switch 10 to peripheral 13. Peripheral 13 is configured to loop back the message to circuit switch 10 and then back to peripheral 12A. Ex. 1009, 4:42–54. The results are then reported back to the message switch. Ex. 1009, 4:34–41. Further, Lewis explains that it is optimal

to perform the loopback test when the links are idle as to not impede on the normal traffic. Ex. 1009, 2:19–20, 13:30–35.

3. <u>Cook</u>

60. Cook discloses a "digital data processing system" which contains several "line control processors" ("LCPs"). Ex. 1010, 4:39–45. The LCPs are connected to each other via a "backplane." Ex. 1010, 28:62–29:7. In the digital data processing system there are one or more LCP Base Modules consisting of eight LCPs. Ex. 1010, 4:39–52. The LCP Base Module contains a "distribution card unit" ("DCU"). Ex. 1010, 5:5–10. The DCU sends and receives data with the I/O Translator ("IOT") including data from the peripheral devices to the LCPs. Ex. 1010, 5:20–31. Figure 2 depicts this structure.



61. Each LCPs, and their corresponding peripheral device, are connected to each other and the distribution card unit through a backplane. Ex. 1010, 28:62–29:7. Figure 6 provides the same structure from a different view point:

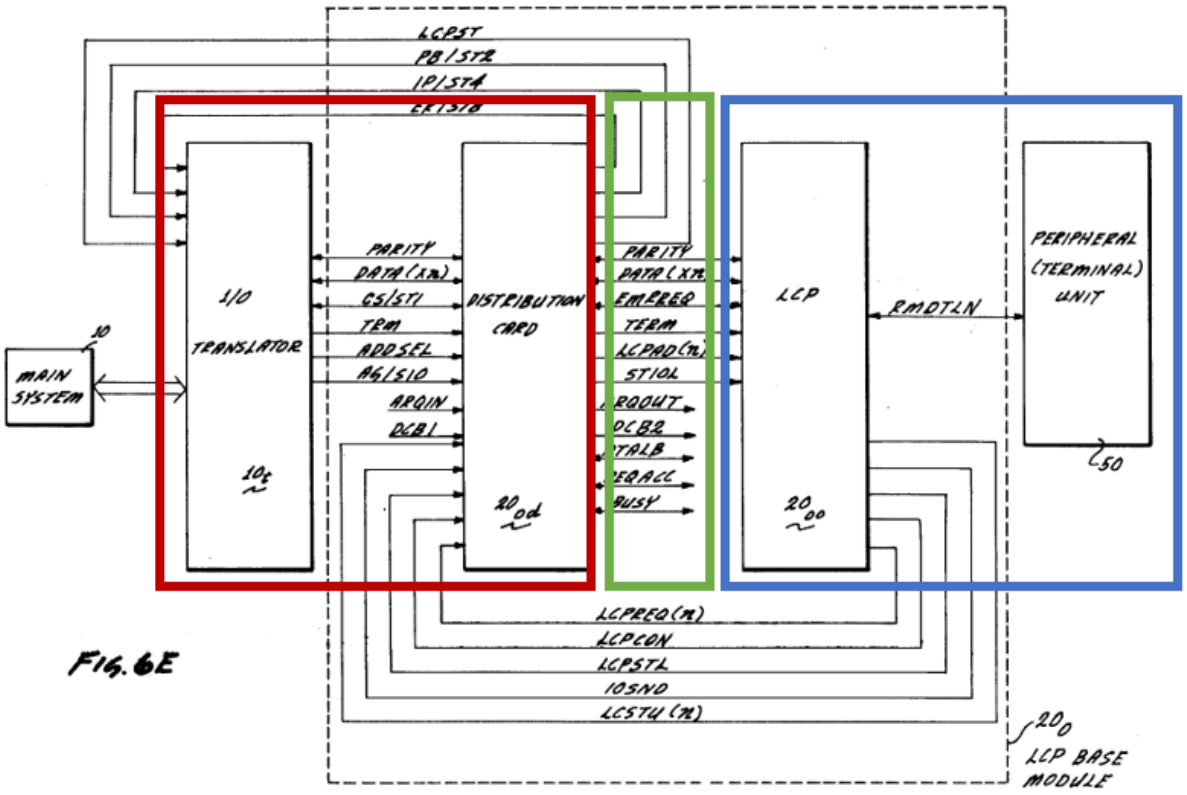


FIG. 6E

62. The DCU and IOT work together to act as a switch between the LCPs. Ex. 1010, 31:63–32:47. Cook discusses testing the connections between the DCU and the LCPs to identify errors. Ex. 1010, 23:43–24:27.

4. <u>Sarkinen</u>

63. Sarkinen discloses a system and method with a network switch or router which utilizes a midplane. Ex. 1011, ¶12. The midplane has mutliple lines and is able to be connected to mutliple fabric cards. Ex. 1011, ¶12. This is demonstrated

in Figure 3 which discloses a fabric interface (308), multiple line cards (304, 306), and fabric cards (312, 316) plugged into a midplane 314. Ex. 1011, ¶55.

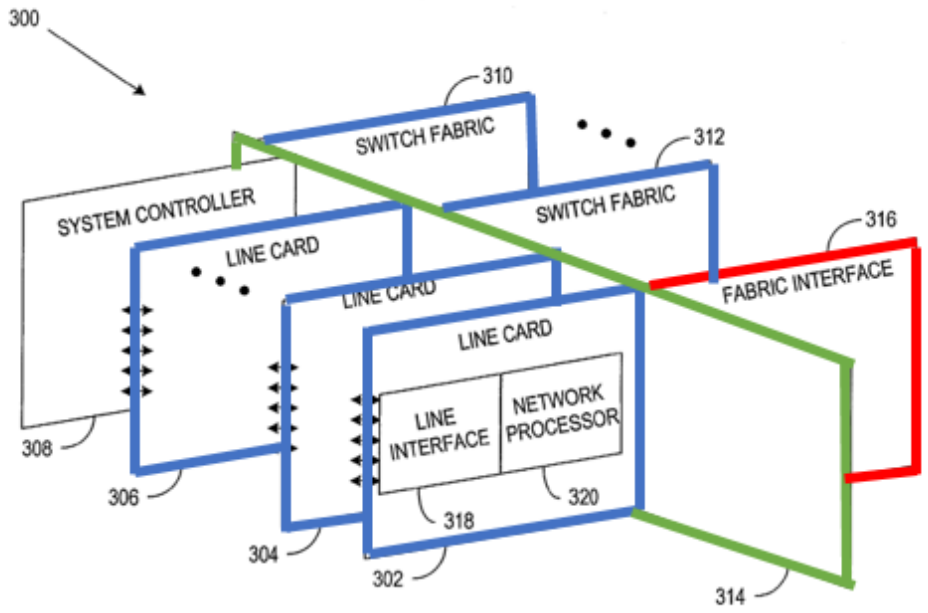


FIG. 3

64. Sarkinen discloses that the midplane depicted in the diagrams can also be a backplane. Ex. 1011, ¶¶12, 54. In fact, the claims of Sarkinen disclose a backplane. *See, e.g.*, Ex. 1011, cl. 1.

VII. ANALYSIS OF THE CHALLENGED CLAIMS AGAINST THE PRIOR ART

A. Claim Construction

65. Unless specifically noted otherwise below, I have accorded claim terms their ordinary and customary meaning as understood by a POSITA and in light of the patent specification and prosecution history.

66. I have been informed by counsel and understand that claim terms need not be construed when there is no dispute as to the meaning of a term that could affect the outcome of the proceeding. It is my opinion that none of the claims of the '369 patent require construction to determine their validity in view of the prior art I have analyzed in this declaration. Thus, for purposes of this proceeding, it is my opinion that no formal claim construction is necessary.

67. I understand that the parties have briefed claim construction in the co-pending district court litigation. I further understand that this briefing has covered four terms recited in the Challenged claims, namely "idle line" (claims 1, 3, 7); "subsidiary module" (claims 1–3, 5, 8–12, 15–17, 21–24); "backplane" (claims 5, 10, 15, 21); and the order of steps for claims (1, 8, 15, 21). As I explain below, because the prior art teaches and/or renders obvious these limitations under both parties' proposed constructions in the district court litigation, these constructions have no impact on the patentability of the Challenged Claims.

B. <u>Application of the Prior Art to the Claims</u>

68. Based upon my review of the prior art, particularly the references detailed in this declaration, it is my opinion that the subject matter of each of the Challenged Claims would have been obvious to one of ordinary skills in the art in view of the known prior art references.

69. It is my understanding that each of the prior art references analyzed in this declaration meets the legal requirements for prior art to the ’369 patent. I have performed my analysis with this understanding.

70. Based upon my analysis, it is my opinion that the Challenged Claims of the ’369 patent are rendered obvious by the following prior art grounds:

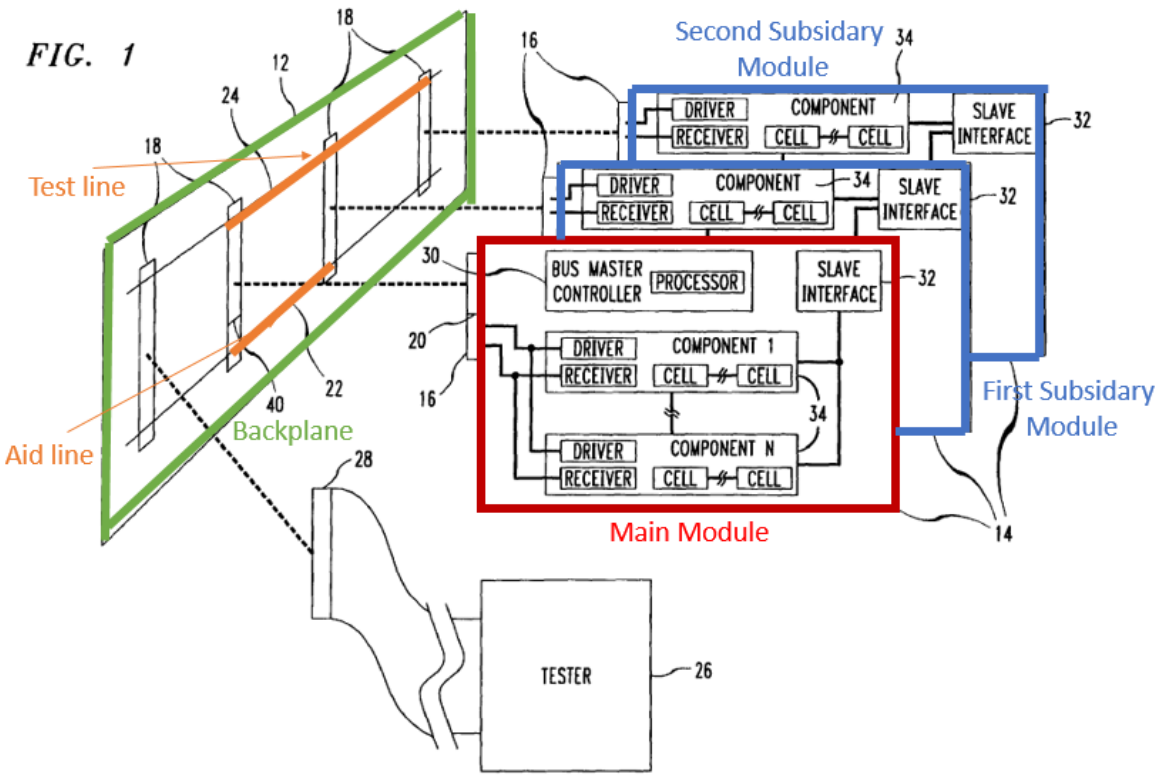
Ground	’369 Patent Claims	Basis for Rejection[1]
1	1–26	Obvious over Ke and Lewis
2	3, 6, 8, 13, 14, 17, 21, 25, and 26	Obvious over Ke, Lewis, and Sarkinen
3	1–26	Obvious over Cook and Lewis
4	3, 6, 8, 13, 14, 17, 21, 25, and 26	Obvious over Cook, Lewis, and Sarkinen

C. <u>Ground 1</u>

71. In my opinion, claims 1–26 of the ’369 patent would have been obvious over Ke in view of Lewis.

72. In my opinion, a POSITA would have been motivated to combine Ke’s backplane testing with Lewis’s loopback.

[1] All obviousness grounds include the knowledge of a POSITA.



73. In the above diagram, it is my opinion that a POSITA would be motivated to test the Ke system with the Lewis test. As depicted above, this could be accomplished by setting up an aid line on Ke's backplane which connects the first subsidiary module and a test line on Ke's backplane which connects the second subsidiary module to the main module, as disclosed in Lewis. The modules would then be able to route the test packet through the aid and test lines to perform Lewis's loopback test. Ex. 1009, 4:42–54.

74. In my opinion, a POSITA would be motivated to combine Ke and Lewis because both references discuss testing connections in a system which contains multiple components. Specifically, Ke discusses a master controller that

directs testing in other boards plugged into a backplane, while Lewis discusses testing peripheral controllers via a control processor/circuit. Ex. 1008, 3:24–37; Ex. 1009, 3:47–53. In my opinion, a POSITA would have understood the benefits of a loopback test in the context of a backplane with a master controller and thus would have been motivated to combine the testing protocol in Lewis in the structure disclosed in Ke.

75. Further, Ke states:

> If a system is dynamically configurable, the position of boards on the backplane can change and boards can be removed or added . . . Individual circuit boards can be tested using a multi-drop test bus configuration, in which multiple boards are connected to a common test bus. Each board is provided with a slave interface that monitors communications from a bus master. With this configuration, boards can be individually addressed for testing. However, multi-drop configurations have not been used for testing backplanes. . . Further, most backplanes are dynamically reconfigurable. Various board types (e.g., memory, input/output, etc.) may be inserted into the backplane. The total number of boards may vary, and the boards may be inserted into the backplane in different orders. Because the type, number, and order of the boards in the backplane are not fixed, thousands or millions of different system configurations may be possible.

Ex. 1008, 1:36–2:4. Based on this disclosure, a POSITA would have been motivated to look at other testing configurations, like the one disclosed in Lewis. A POSITA would know that a backplane could be tested by a loopback test. A POSITA would

also know that a loopback test would be ideal to test a backplane-based system because a loopback test could test the connections between the different boards connected to the backplane. In my opinion, a POSITA would also have known that testing between peripheral units would be essential because sometimes data needs to be transferred to and from different boards on the backplane. A POSITA therefore would have been motivated to apply the loopback testing between two peripherals in Lewis to the structure in Ke to test the connection between two boards in the backplane.

76. Lewis further discloses "[b]oth message and circuit switches are connected via serial links to one or more peripheral controllers 11A and 11B, the peripheral controllers being connected to peripherals 12A, 12B, 13 etc. via peripheral interface units." Ex. 1009, 3:53–60. Specifically, a POSITA would have been motivated to apply the loopback testing between two peripheral interfaces in Lewis to the input/outputs structure of board-pins in Ke since the input/outputs structure consist of bidirectional input/outputs acting as interfaces and participating in testing the connection between two boards in the backplane.

77. Additionally, a POSITA would have been motivated to test the lines of the backplane in Ke while they were idle as disclosed in Lewis. Ex. 1009, 2:19–20. Ke discusses testing the backplane traces by disabling certain parts of the system to avoid damage to circuit components. Ex. 1008, 2:29–35. A POSITA would

understand that waiting until those lines are idle would be the ideal time to test as that would avoid disrupting traffic when the lines were in use.

78. Finally, in my opinion, a POSITA would have known there was a reasonable expectation of success to implement the testing in Lewis in the structure in Ke because, as explained above, Ke acknowledged that there were multiple possible techniques for testing backplanes. Ex. 1008, 1:30–2:18. A POSITA would therefore have a reasonable expectation of success of the testing from Lewis. Specifically, Ke states:

> Boards 14 each have a slave interface 32 driven by tester 26 or bus master 30. Boundary scan test data is loaded into a scan chain that passes serially through each of the components 34 on a given board. To load a test vector into the boundary scan cells in the scan chain on a particular board, the slave 32 for that board is addressed using protocols communicated in test bus 24. Test vector data is then loaded via test bus 24.

Ex. 1008, 3:28–35. A POSITA would understand that this disclosure implies that the bus master could have been used to control the test.

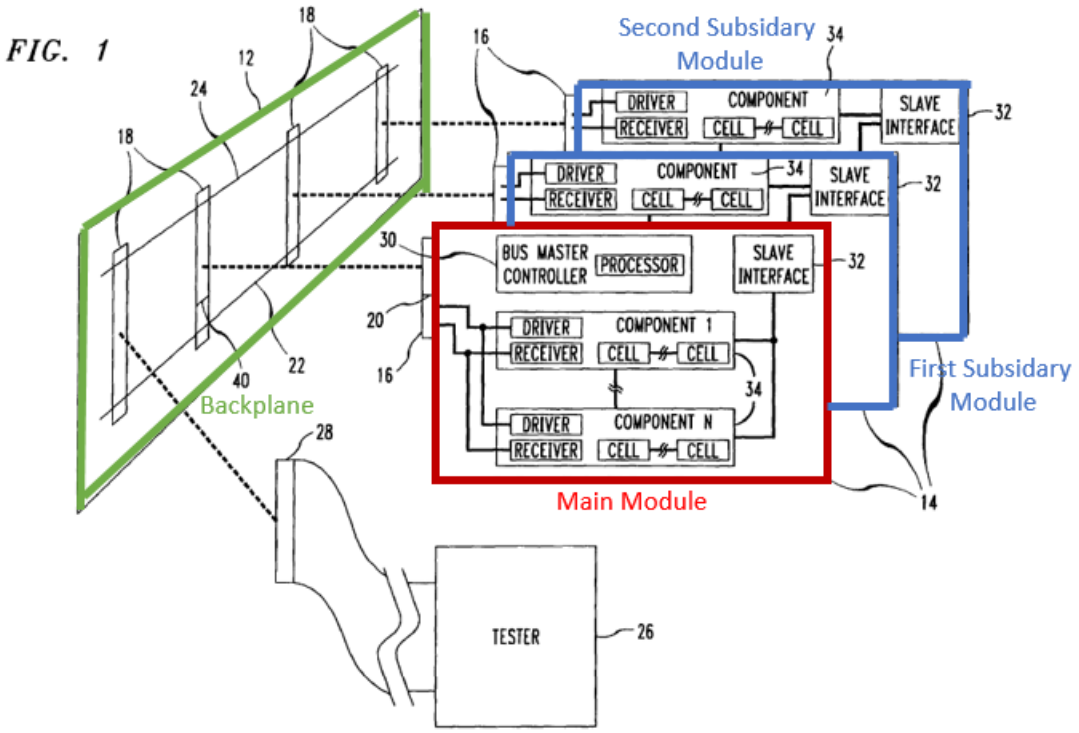
79. Therefore, it is my opinion that a POSITA would have therefore understood that the loopback testing between specific peripherals in Lewis could be employed in Ke by using the master bus controller to control testing between specific boards.

a) 1[pre]: In an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system, comprising:

80. In my opinion, to the extent the preamble is limiting, Ke in view of Lewis discloses 1[pre]. Ke discloses:

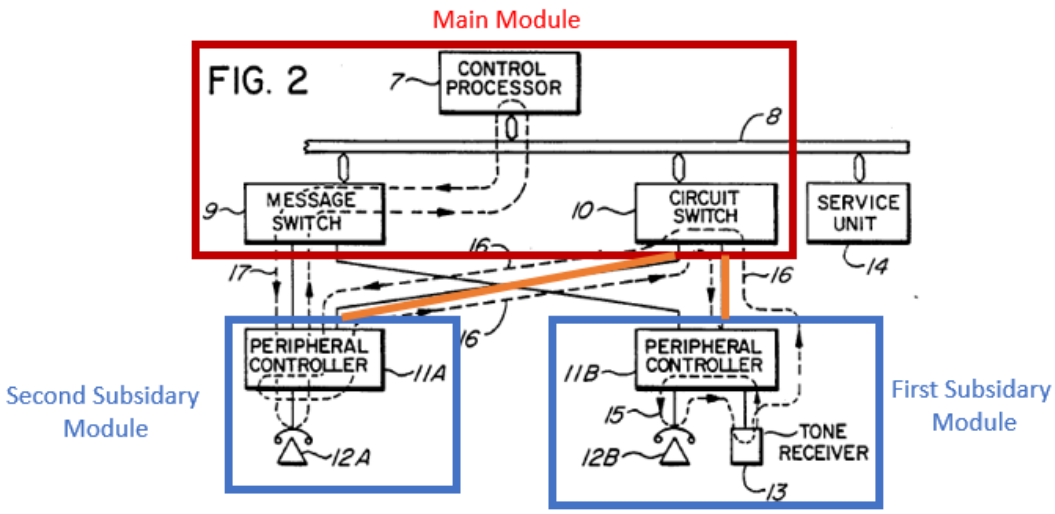
> Electrical system 10 is formed from backplane 12 and circuit boards 14, as shown in FIG. 1. In operation, boards 14 are mounted on backplane 12 by inserting edge connectors 16 into slot connectors 18. Pins on edge connectors 16, such as pin 20, are electrically connected to interconnect traces (interconnects) 22 on backplane 12 via slot connectors 18. Interconnects 22 provide communication pathways for data and control signals between boards 14.

Ex. 1008, 3:15–23. Each of these circuit boards have "a slave interface 32 driven by a tester 26 or a bus master 30." 1008, 3:28–29. In my opinion, a POSITA, would understand that the card which has the bus master controller 30, is akin to the main module. Similarly, a POSITA would understand at least two other cards would be akin to the subsidiary modules. This depiction is demonstrated below.



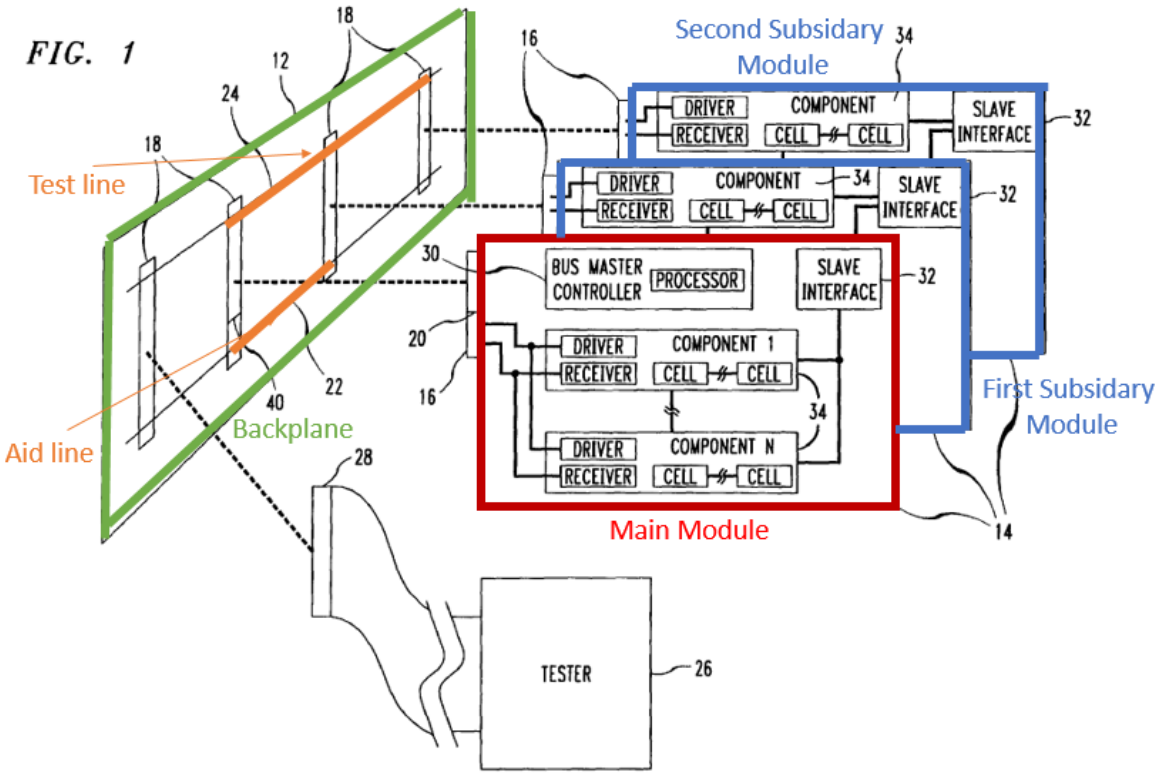
Ex. 1008, Fig.1.

81. Similarly, Lewis also has a circuit switch, a control processor 7, and message switch 9. Ex. 1009, 3:47–60. It would be obvious to a POSITA to view one or more switching units together with the control processor as akin to the main module in the '369 patent. The system in Lewis also describes as having multiple peripheral controllers (11A, 11B) which are connected to peripherals (12A, 12B, 13). Ex. 1009, 3:47–60. It would be obvious to a POSITA to view these peripherals as subsidiary modules.



Ex. 1009, Fig. 2.

82. Due to their similarities, it is my opinion that Lewis would have been obvious to a POSITA to combine with Ke. The below figure demonstrates Lewis on top of Ke. Specifically, the module in Ke with the bus master controller would be the main module, while the other two modules are subsidiary modules. The lines connecting the modules would be the test and aid lines. Ex. 1009, 4:32–54.



In regards to idle lines, Ke discloses:

> In accordance with the present invention, a group of primitive vectors (disable, enable 0, and enable 1 vectors) are precomputed prior to testing for each board 14. The enable 0 and enable 1 vectors allow drivers in system 10 to be individually toggled. Individual drivers on a board 14 are toggled while the circuitry on other boards 14 is disabled, which avoids contentions between drivers.

Ex. 1008, 3:61–67. In my opinion, a POSITA would understand that based on this disclosure lines in the backplane would sometimes be idle or not in use. Lewis also discloses that "[t]esting is also preferred to be performed during times when the switches or links are idle." Ex. 1009, 2:19–20. Due to this similarity, it would be obvious to a POSITA to combine Ke and Lewis.

83. Ke also discloses that the main module acts as a switch when it discloses:

> In accordance with the present invention, a group of primitive vectors (disable, enable 0, and enable 1 vectors) are precomputed prior to testing for each board 14. The enable 0 and enable 1 vectors allow drivers in system 10 to be individually toggled. Individual drivers on a board 14 are toggled while the circuitry on other boards 14 is disabled, which avoids contention between drivers.

Ex. 1008, 3:61–67. Here, the main module is driving the test and setting vectors to be individually toggled. A POSITA would understand this to be a switch. Ke also discloses:

> Electrical system 10 is formed from backplane 12 and circuit boards 14, as shown in FIG. 1. In operation, boards 14 are mounted on backplane 12 by inserting edge connectors 16 into slot connectors 18. Pins on edge connectors 16, such as pin 20, are electrically connected to interconnect traces (interconnects) 22 on backplane 12 via slot connectors 18. Interconnects 22 provide communication pathways for data and control signals between boards 14.

Ex. 1008, 3:15–22. A POSITA would understood that this was the same as a backplane interconnecting to other boards.

84. Finally, Ke discloses that the main module tests the connections of the backplane when it states:

> Backplanes have slot connectors into which the edge connectors of circuit boards are inserted and have interconnects for providing

> communication pathways between boards. Backplane testing involves testing the interconnects to ensure that the assembled backplane is functioning properly. Faults can arise due to misplugged boards, bent, broken or shorted board pins, or interconnect traces on the backplane that are open or shorted. Testing while the boards are inserted into the backplane is required to detect these various faults.

Ex. 1008, 1:23–32.

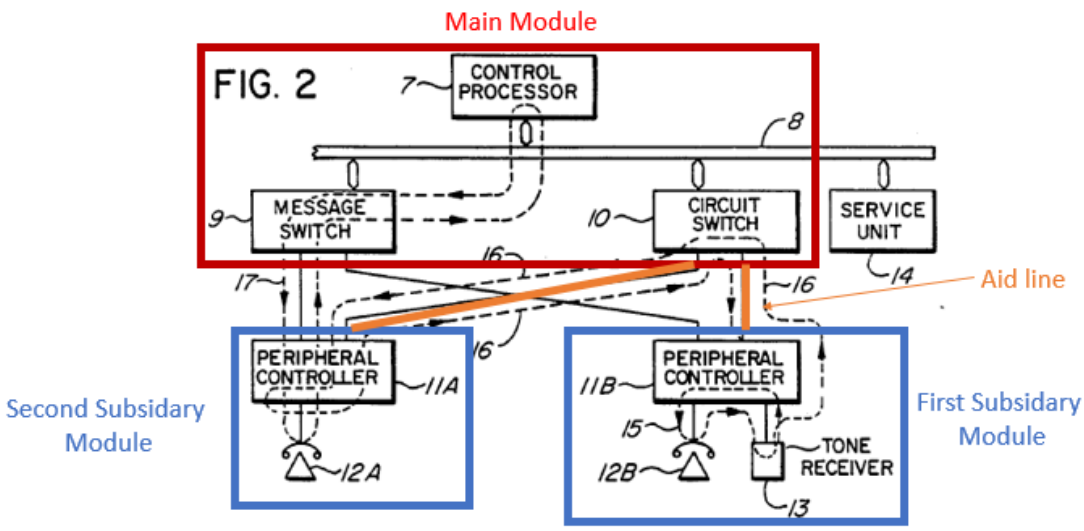
85. Therefore, it is my opinion that Ke in view of Lewis discloses "an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system."

b) 1[a]: selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line;

86. In my opinion, Ke in view of Lewis discloses 1[a]. Lewis discloses "a looparound arrangement in a switching system whereby transmission paths of the system can be tested." Ex. 1009, 1:4–7. Further, Lewis discloses that "[t]esting is also preferred to be performed during times when the switches or links are idle." Ex. 1009 2:19–20. Lewis states that:

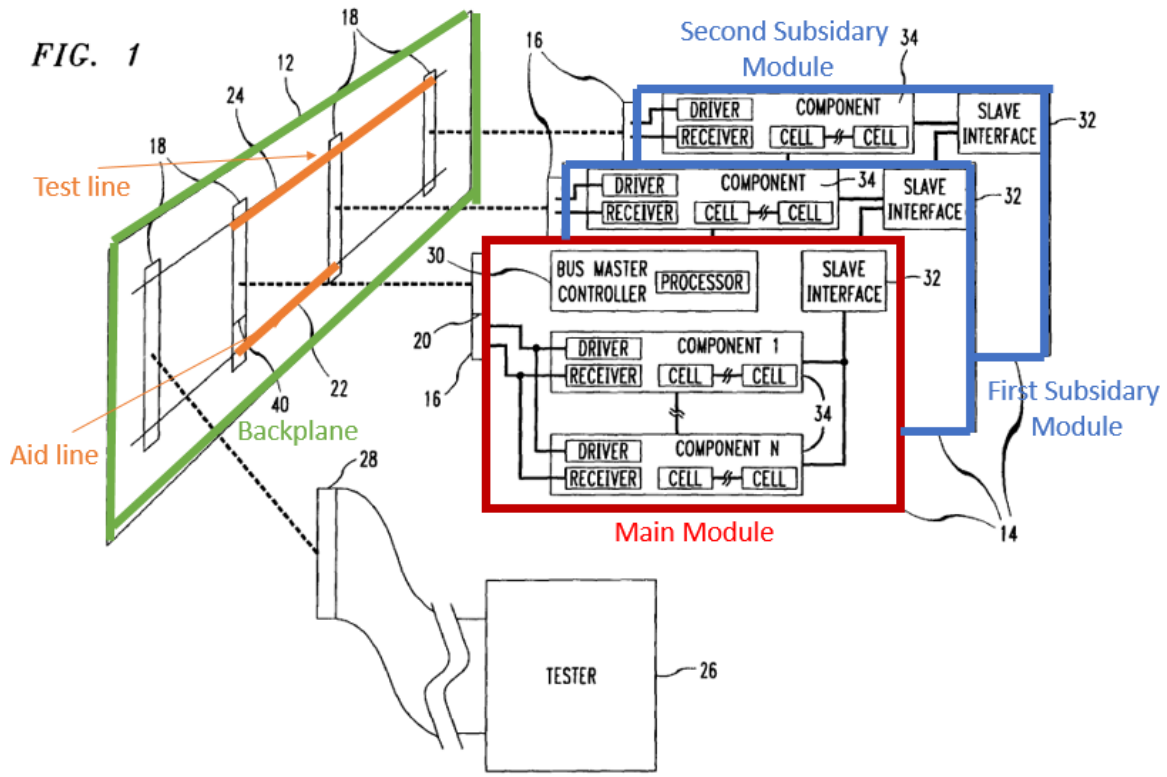
87. According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

88. Ex. 1009, 4:23–41. This system is demonstrated on the diagram below:



Ex. 1009, Fig. 2.

89. As per above, the modules in Ke are connected via a port on the backplane. Ex. 1008, 1:15–23. It would be obvious to a POSITA that the modules in Lewis could be connected to the main module via a port on backplane as they are in Ke. A POSITA would also know that the modules in Lewis could be connected to the main module via a port on a backplane. Such a combination is depicted, below.



90. Therefore, it is my opinion that Ke in view of Lewis discloses "selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line."

c) 1[b]: instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line;

91. In my opinion, Ke in view of Lewis discloses 1[b]. Lewis discloses "instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line." Specifically, Lewis states:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set

> 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.
>
> In a similar manner other forms of loops can be set up and tested. For example the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface. A test tone signal is injected into the loop by service unit 14 and the return signal received via the message links as described earlier with reference to local loop 15. In this manner a complete or long loop between peripheral interfaces can be set up and tested.

Ex. 1009, 4:23–54. A POSITA would have understood this disclosure as requiring instructing a first subsidiary module to loop back traffic it receives back to the circuit switch in the main module. Alternatively, it would have been obvious to a POSITA

that the main module would instruct the subsidiary module to loop back traffic. Ex. 1009 4:23–54.

92. Therefore, it is my opinion that Ke in view of Lewis disclose "instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line."

d) 1[c]: selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module;

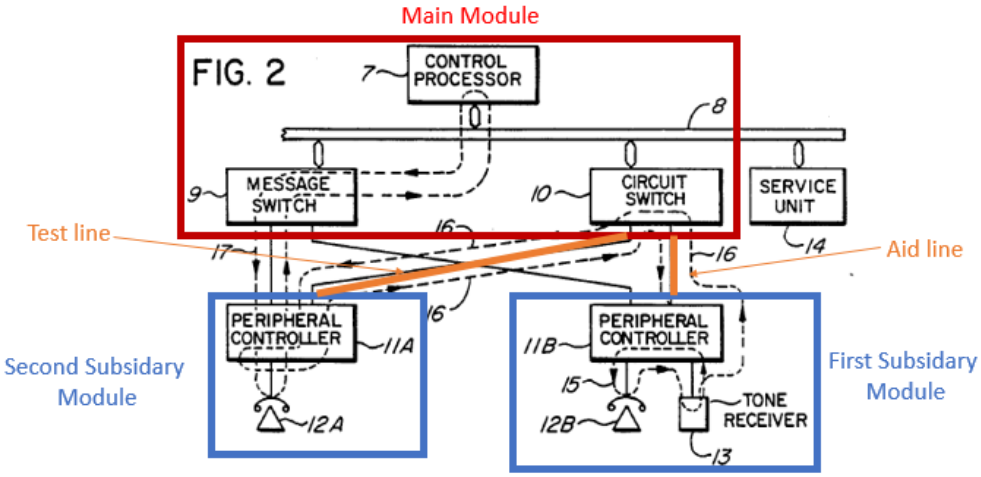
93. In my opinion, Ke in view of Lewis discloses 1[c]. Lewis discloses "selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module." Specifically, Lewis states:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes

back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

In a similar manner other forms of loops can be set up and tested. For example the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface. A test tone signal is injected into the loop by service unit 14 and the return signal received via the message links as described earlier with reference to local loop 15. In this manner a complete or long loop between peripheral interfaces can be set up and tested.

Ex. 1009, 4:23–54. As described above, the system selects a line between the second subsidiary module and the circuit switch ("test line") for testing.



94. As I stated in 1[a], a POSITA would have understood or found it obvious that the second subsidiary module is connected via a port to the circuit switch.

95. Therefore, it is my opinion that Ke in view of Lewis disclose "selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module."

e) 1[d]: configuring the switch to link the first and second ports;

96. In my opinion, Ke in view of Lewis discloses 1[d]. It would have been obvious to a POSITA that when the loopback is set up as described in 1[a] and 1[c], it is done by configuring a link between the first and second ports to form the loopback circuit. In view of Ke, it would have been obvious to a POSITA that the main module would link the first and second ports to close the loop between the subsidiary modules. *Id.*

97. Therefore, it is my opinion that Ke in view of Lewis discloses "configuring the switch to link the first and second ports."

f) 1[e]: transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module; and

98. In my opinion, Ke in view of Lewis discloses 1[e]. Lewis discloses:

According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

In a similar manner other forms of loops can be set up and tested. For example the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface. A test tone signal is injected into the loop by service unit 14 and the return signal received via the message links as described earlier with reference to local loop 15. In this manner a complete or long loop between peripheral interfaces can be set up and tested.

Ex. 1009, 4:23–54. A POSITA would understand that this discloses transmitting test data to the subsidiary modules. Similarly, Ke discloses:

> In accordance with the present invention, a group of primitive vectors (disable, enable 0, and enable 1 vectors) are precomputed prior to testing for each board 14. The enable 0 and enable 1 vectors allow drivers in system 10 to be individually toggled. Individual drivers on a board 14 are toggled while the circuitry on other boards 14 is disabled, which avoids contention between drivers.
>
> Further, because the vectors are precomputed, it is not necessary to process boundary scan description language and hierarchical description language files defining the board level characteristics of the boundary scan cells before testing. The precomputed primitives also simplify the process of managing dynamically reconfigurable boards 14, because the primitive vectors for boards 14 do not depend on the locations of boards 14 in backplane 12. Primitive vectors are provided to a given board 14 by addressing the appropriate slave interface 32. The capability to individually toggle the drivers of system 10 improves the fault detection and classification capabilities of system 10.
>
> The drivers (di) in system 10 are portions of components 34 that drive pins on edge connectors 16, such as pin 20. The receivers (ri) are portions of components 34 that receive the signals generated by drivers di. Drivers di are connected to receivers ri by interconnects 22. For example, in FIG. 3, driver d1 is connected to receiver r2 via interconnect 36. In a system with sufficient boundary scan cells, all drivers di are controllable and all receivers ri are observable.

> In order to perform boundary scan testing of backplane 12, each board 14 that does not contain the driver being toggled is temporarily disabled by applying a disable vector to its scan chain. FIGS. 3-6 are network representations of the disable states of various interconnect structures. In the simple net interconnect structure of FIG. 3, an output signal from driver d1 is provided directly to receiver r2. In the wired-AND network structure of FIG. 5, the path between drivers d1 (e.g., on a first board 14) and d2 (e.g., on a second board 14) and receiver r (e.g., on a third board 14) subjects the signals from d1 and d2 to a logical AND function. For the disable state, the drivers of wired and simple nets are set to noncontrolling values: 0 for wired-OR nets as shown in FIG. 6, 1 for wired-AND nets as shown in FIG. 5, and either 0 or 1 for simple nets as shown in FIG. 3. Three-state drivers are deactivated (i.e., tri-stated or not driving), as indicated by the letter Z in FIG. 4. Bidirectional pins are configured as receivers. When boards 14 are disabled, toggling one of the drivers in system 10 by applying the enable 0 and enable 1 primitive vectors will not create a signal conflict on interconnects 22.

Ex. 1008, 3:61–4:40. A POSITA would have recognized this disclosure in Ke as transmitting test traffic to the subsidiary modules.

99. Therefore, it is my opinion that Ke in view of Lewis discloses "transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module."

g) 1[f]: reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

100. In my opinion, Ke in view of Lewis discloses 1[f]. Lewis discloses:

> The main controller, **having received a message signal via the system described above of the returned test signal, formulates a message and** transmits it to the service unit 214, of the test signal, and also formulates a message signal to be returned to the peripheral acknowledging that it has received the message. This signal is downloaded via parallel bus 212 into COMRAM BUFFER 214, which operates in the reverse direction in the same way as described earlier.

Ex. 1009, 14:3–11. In my opinion, a POSITA would have understood that this discloses "reporting a failure has occurred." Further, a POSITA would understand that a failure constitutes the main module not receiving a test message from the second subsidiary module within a predetermined period of time. This sort of "time out" result is common and well understood. For example, Internet Control Message Protocol ("ICMP") messages, or ping, which have been commonplace in the field since at least 1989, sends a timeout message if the ICMP message was not returned in a reasonable amount of time. Ex. 1012 (RFC 1122), 57–58.

101. As another example, Stallings discloses the ICMP messages and shows two examples of such messages, echo messages and timestamp messages, that carry out the timeout function:

> The echo and echo-reply messages provide a mechanism for testing that communication is possible between entities. The recipient of an echo message is obligated to return the message in an echo-reply message. An identifier and sequence number are associated with the echo message to be matched in the echo-reply message. The identifier might be used like a service access point to identify a particular session, and the sequence number might be incremented on each echo request sent . . .
>
> The timestamp and timestamp reply messages provide a mechanism for sampling the delay characteristics of the internet. The sender of a timestamp message may include an identifier and sequence number in the parameters field and include the time that the message is sent (originate timestamp). The receiver records the time it received the message and the time that it transmits the reply message in the timestamp-reply message. If the timestamp message is sent using strict source routing, then the delay characteristics of a particular route can be measured.

See Ex. 1013, 549.

102. Therefore, it is my opinion that Ke in view of Lewis discloses "reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time," as it would have been obvious to a POSITA.

h) Claim 2: A method according to claim 1, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back

the traffic to the main module substantially without processing data comprised in the test traffic.

103. In my opinion, Ke in view of Lewis discloses claim 2 for the same reasons discussed in claim 1[b]. Specifically, Lewis discloses:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal **having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14**. In this manner a small, isolated transmission loop is established and tested.

Ex. 1009, 4:23–41 (emphasis added). In my opinion, a POSITA would have understood that this disclosure represents the idea that test traffic goes through the first subsidiary module without substantial processing.

104. Therefore, in my opinion, Ke in view of Lewis discloses "instructing the first subsidiary module comprises configuring the first subsidiary module to loop

back the traffic to the main module substantially without processing data comprised in the test traffic."

i) Claim 3: A method according to claim 2, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.

105. In my opinion, Ke in view of Lewis discloses claim 3 for the same reasons discussed in claim 2. Additionally, Ke discloses:

> Boundary scan test data is loaded into a scan chain that passes serially through each of the components 34 on a given board. To load a test vector into the boundary scan cells in the scan chain on a particular board, the slave 32 for that board is addressed using protocols communicated in test bus 24. Test vector data is then loaded via test bus 24. Preferably, system 10 supports the Test Access Port (TAP) and Boundary Scan Architecture defined in IEEE Std. 1149.1.

Ex. 1008, 3:30–37. This explains that test traffic is sent via protocols communicated over the bus and that test vector data is specifically loaded into the message for test traffic transmitted to the subsidiary modules (second format). Ex. 1008, 3:30–37. In my opinion, it would be obvious to a POSITA that a different format of message (without the test vector data) would have been used for normal messages (first format).

106. Alternatively, it would have been obvious to a POSITA that the subsidiary modules could send and receive data in multiple formats because different messages passed between the modules may require different formats and would have been organized differently.

107. Therefore, it is my opinion that Ke in view of Lewis discloses "wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format."

j) Claim 4: A method according to claim 1, further comprising: selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and repeating the configuring the switch, transmitting the test traffic, and reporting that the failure has occurred with respect to the further idle lines until all the idle lines have been tested.

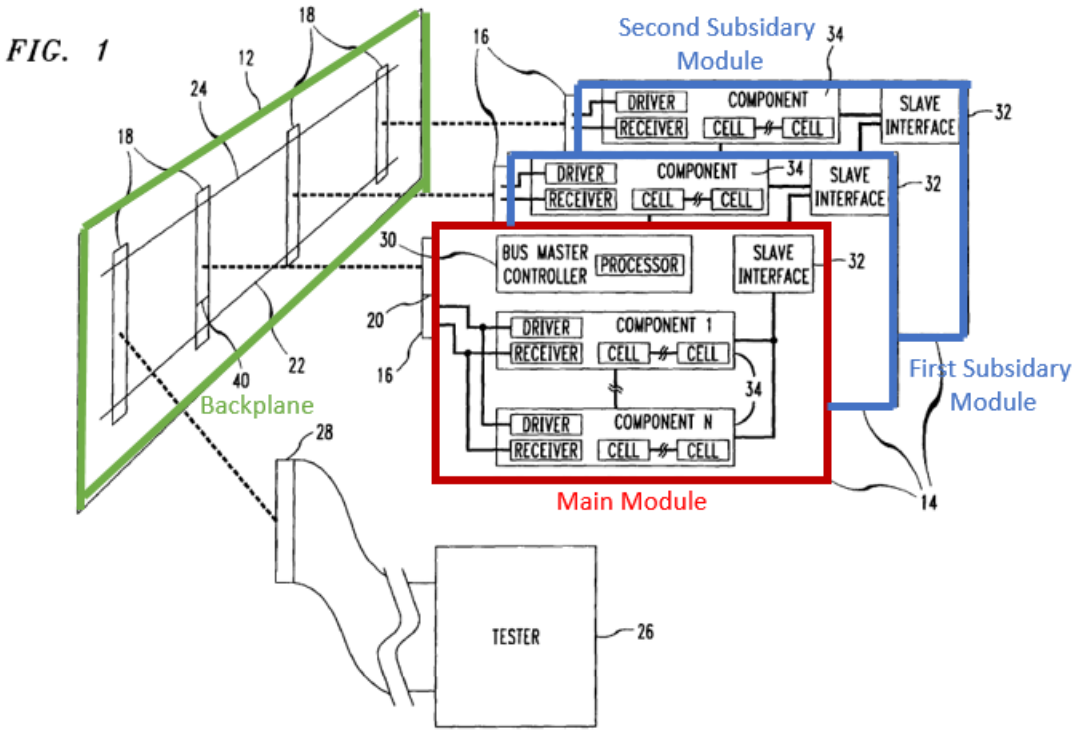
108. In my opinion, Ke in view of Lewis discloses claim 4, for the same reasons as claims 1[a] and 1[c]. Specifically, Lewis discloses selecting multiple idle lines that connect to ports on the circuit switch in the main module. *See* VII.C.b and VII.C. Lewis also discloses that "local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system." Ex. 1009, 4:23–25. In my opinion, a POSITA would have understood that any and all of the idle lines could

be added to the same loop for testing. Further, it would have been obvious to a POSITA that the same process for choosing idle lines could be repeated until all the idle lines have been tested. In fact, it would have been obvious to a POSITA to run the test repeatedly until all the idle lines were tested. A POSITA would also have been motivated to repeat the test in order to make sure that all potential hidden failures were discovered.

109. Therefore, it is my opinion that Ke in view of Lewis discloses "selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and repeating the configuring the switch, transmitting the test traffic, and reporting that the failure has occurred with respect to the further idle lines until all the idle lines have been tested."

k) Claim 5: A method according to claim 1, wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

110. In my opinion, Ke in view of Lewis discloses claim 5 for the same reasons as discussed for 1[pre]. As I explained above, Ke describes a card with the bus master controller 30 (main module) and two or more other cards (first and second subsidiary modules), and a backplane 24 with traces.



111. Ex. 1008, Fig. 1. It would be clear to a POSITA that the modules in Ke are plugged into the backplane, as is commonly practiced. Ke also refers to the modules being plugged in when it says cards can be misplugged. Ex. 1008, 1:23–32. It would be obvious to a POSITA that something that can be misplugged, can also be plugged.

112. Therefore, it is my opinion that Ke in view of Lewis discloses "wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane."

l) Claim 6: A method according to claim 1, wherein the switch is configured to connect the lines to a network

communication trunk, and wherein the traffic comprises communication traffic.

113. In my opinion, claim 6 would have been obvious to a POSITA over Ke in view of Lewis. A POSITA would know that an electrical system which utilizes a backplane could have a network switch or another type of network device. A POSITA would also have understood one of the modules inserted into the backplane could be connected to the internet through that network trunk.

114. Therefore, it is my opinion that Ke in view of Lewis discloses "wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic."

m) Claim 7: A method according to claim 6, wherein transmitting the test traffic comprises testing the second idle line while continuing to use the lines that are not idle for carrying the data to the network communication trunk.

115. In my opinion, Ke in view of Lewis discloses claim 7. Specifically, Lewis refers to idle lines when it says:

> Assuming that the location of an idle path has been determined, the main controller sends a message signal to the peripheral controllers, and to the circuit switch processor 218 to set up the circuit path.

Ex. 1009, 14:30–34. Lewis also states that "[t]esting is preferred to be performed during times when the switches or links are idle." Ex. 1009, 2:19–20. A POSITA would have known that these disclosures mean that the test could occur on idle lines, while the non-idle lines continue carrying normal traffic.

116. In my opinion, Ke suggests temporarily disabling boards that are not currently being tested. For example:

> In accordance with the present invention, a group of primitive vectors (disable, enable 0, and enable 1 vectors) are precomputed prior to testing for each board 14. The enable 0 and enable 1 vectors allow drivers in system 10 to be individually toggled. Individual drivers on a board 14 are toggled while the circuitry on other boards 14 is disabled, which avoids contentions between drivers.

Ex. 1008, 3:61–67. However, a POSITA would know that the loopback test from Lewis does not require disabling the other boards because the loopback would be narrowly targeted.

117. Therefore, it is my opinion that Ke in view of Lewis discloses "transmitting the test traffic comprises testing the second idle line while continuing to use the lines that are not idle for carrying the data to the network communication trunk."

n) 8[pre]: In an electronic system that includes a main module and multiple subsidiary modules, each of said multiple subsidiary modules being connected to the main module by one or more lines for carrying data, a method for self-testing the system, comprising:

118. It is my opinion that Ke in view of Lewis discloses 8[pre] for the same reasons as 1[pre].

o) 8[a]: selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary

modules being configured to transmit and receive the data in different, respective first and second formats;

119. It is my opinion that Ke in view of Lewis discloses 8[a] for the same reasons as 1[a], 1[c], and claim 3. In addition, Ke also states that "most backplanes are dynamically reconfigurable. Various board types (e.g., memory, input/output, etc.) may be inserted into the backplane." Ex. 1008, 1:65–67. A POSITA would understand that this was disclosing that the first and second subsidiary modules could be different types. Similarly, Lewis states:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

Ex. 1009, 4:23–41, Fig. 2. A POSITA would have understood that this disclosure means that the first and second modules could be different.

120. Therefore, it is my opinion that Ke in view of Lewis discloses "selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats."

p) 8[b]: instructing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module;

121. In my opinion, Ke in view of Lewis discloses 8[b] for the same reasons as 1[b].

q) 8[c]: configuring the main module to connect the first and second subsidiary modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module; and

122. In my opinion, Ke in view of Lewis discloses 8[c] for the same reasons as 1[c].

r) 8[d]: testing the system by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.

123. In my opinion, Ke in view of Lewis discloses 8[d] for the same reasons as 1[f] and claim 3. Specifically, Lewis states:

> The main controller, **having received a message signal via the system described above of the returned test signal, formulates a message and** transmits it to the service unit 214, of the test signal, and also formulates a message signal to be returned to the peripheral acknowledging that it has received the message. This signal is downloaded via parallel bus 212 into COMRAM BUFFER 214, which operates in the reverse direction in the same way as described earlier.

Ex. 1009, 14:3–11. This passage describes the main module acknowledging to have received the return signal if the test message was returned successfully. Ex. 1009, 14:3–11. A POSITA would understand that the main module confirm that the test message returned intact before it acknowledged receipt because the test would fail if the message did not return intact or did not return.

124. Therefore, it is my opinion that Ke in view of Lewis discloses "testing the system by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module."

s) Claim 9: A method according to claim 8, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.

125. In my opinion, Ke in view of Lewis discloses claim 9 for the same reasons as claim 2.

t) Claim 10: A method according to claim 8, wherein the main module and subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

126. In my opinion, Ke in view of Lewis discloses claim 10 for the same reasons as claim 5.

u) Claim 11: A method according to claim 8, wherein the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module.

127. In my opinion, Ke in view of Lewis discloses claim 11 for the same reasons as claim 6 and 1[d]. Further, a POSITA would know that linking the first and second ports is equivalent to the switch connecting lines of the first and second subsidiary modules. Alternatively, it would have been obvious to a POSITA that the switch could connect lines of the first and second subsidiary modules so they can send the test traffic to each other.

128. Therefore, it is my opinion that Ke in view of Lewis discloses "A method according to claim 8, wherein the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module."

v) Claim 12: A method according to claim 11, wherein testing the system comprises testing one or more of the lines of the second subsidiary module while continuing to use at least some of the lines that are not under test for carrying the data from the subsidiary modules to the network communication trunk.

129. In my opinion, Ke in view of Lewis discloses claim 12 for the same reasons as claim 7.

w) Claim 13: A method according to claim 8, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.

130. In my opinion, Ke in view of Lewis discloses claim 13 for the same reasons as claim 3. Further, it would have been obvious to a POSITA that the test traffic in the subsidiary modules could have a different protocol. A POSITA would have been motivated to use a different protocol so the module would know how to handle the test traffic because the test traffic is handled by the modules differently than normal traffic.

131. Therefore, it is my opinion that Ke in view of Lewis discloses "traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols."

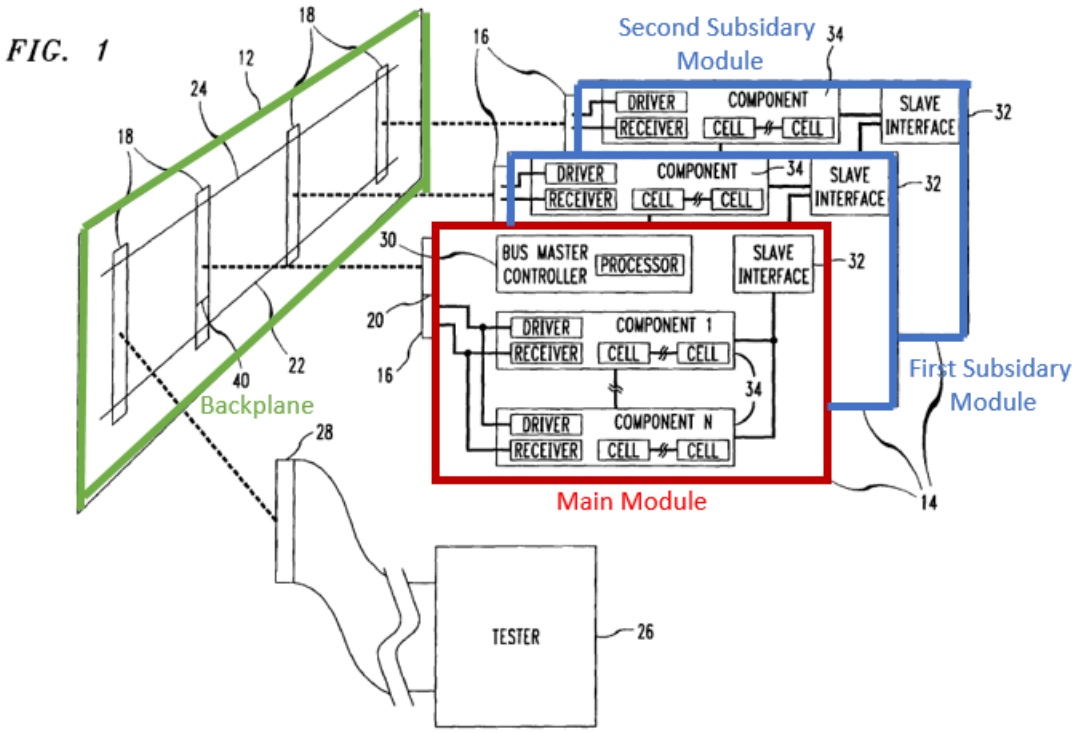
x) Claim 14: A method according to claim 13, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

132. In my opinion, Ke in view of Lewis discloses claim 14. In my opinion, it would have been obvious to a POSITA that the modules could utilize different protocols, including TDM protocols and packet data protocols, because the type of signal does not matter. Additionally, a POSITA would know that a TDM protocol is used for communications with other modules, while a packet data protocol is used to communicate with other devices over an IP-based network. For example, a textbook which predates the patents states that "two common forms of multiplexing are frequency-division multiplexing (FDM) and time division multiplexing (TDM)." *See* Ex. 1013, 236. The textbook also discusses packet switching which utilizes the packet data protocol. *See* Ex. 1013, 10.

133. Therefore, it is my opinion that Ke in view of Lewis discloses "a method according to claim 13, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol."

y) 15[pre]: Modular electronic apparatus, comprising:

134. In my opinion, and to the extent the preamble is limiting, Ke and Lewis render 15[pre] obvious for the same reasons as 1[pre]. Specifically, Ke discloses "a multiboard electronic system having a backplane to be tested." Ex. 1008, 2:55–56, Fig.1. A POSITA would have understood that cards, or modules, could be inserted or removed, making the disclosure in Ke a modular electronic apparatus.



135. Therefore, it is my opinion that Ke in view of Lewis renders obvious a "modular electronic apparatus."

z) 15[a]: a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;

136. In my opinion, Ke in view of Lewis discloses 15[a] for the same reasons as claim 5.

aa) 15[b]: a main module, plugged into the backplane, the main module comprising a switch having ports for connection to the traces of the backplane;

137. In my opinion, Ke in view of Lewis discloses 15[b] for the same reasons as 1[pre] and claim 5.

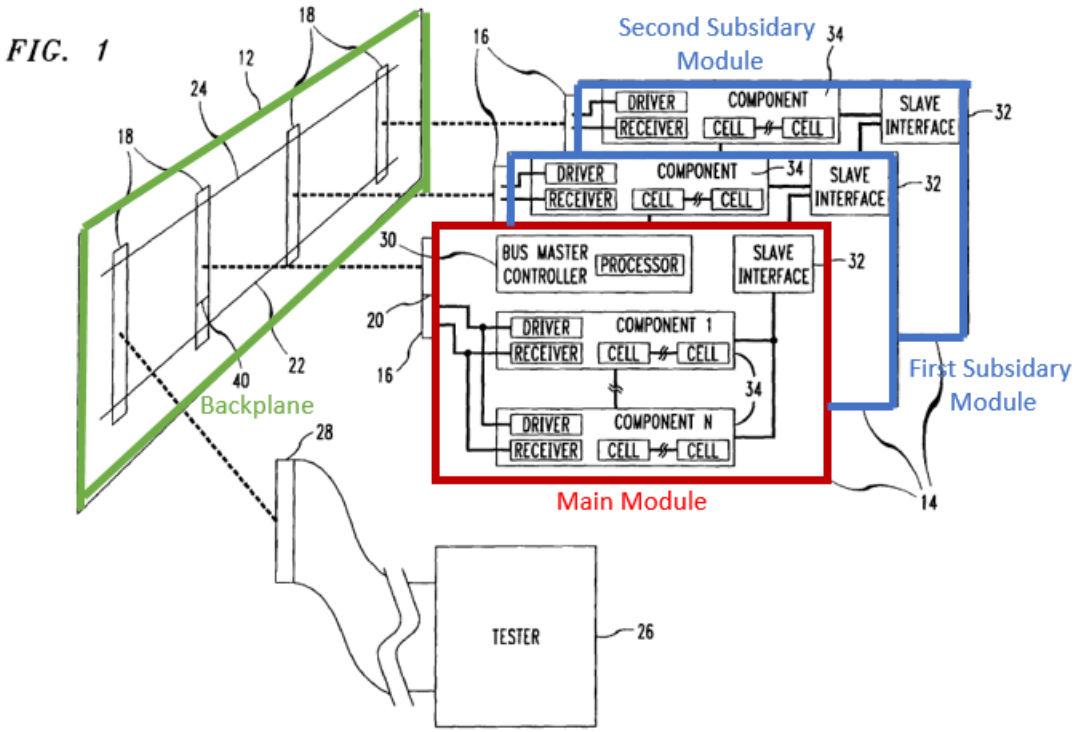
bb) 15[c]: at least first and second subsidiary modules, plugged into the backplane so as to be connected to

the main module by the traces, at least some of which traces are sometimes idle; and

138. In my opinion, Ke in view of Lewis discloses 15[c] for the same reasons as 1[pre] and claim 5.

cc) 15[d]: a system control processor, which is operative to select a first idle trace among idle traces connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace,

139. In my opinion, Ke in view of Lewis discloses 15[d] for the same reasons as 1[a]. Additionally, Ke also discloses a processor in the master controller of the main module which is operable to control the testing. Ex. 1009, Fig.1.



140. Therefore, it is my opinion that Ke in view of Lewis discloses "a system control processor, which is operative to select a first idle trace among idle traces

connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace."

dd) 15[e]to instruct the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid trace,

141. In my opinion, Ke in view of Lewis discloses 15[e] for the same reasons as 1[b].

ee) 15[f]to select for testing a second idle trace among the idle traces connecting the second subsidiary module to a second port of the switch on the main module, and

142. In my opinion, Ke in view of Lewis discloses 15[f] for the same reasons as 1[c].

ff) 15[g]to configure the switch to link the first and second ports,

143. In my opinion, Ke in view of Lewis discloses 15[g] for the same reasons as 1[d].

gg) 15[h]the system control processor being further operative to cause test traffic to be transmitted over the second idle trace from the second subsidiary module to the main module,

144. In my opinion, Ke in view of Lewis discloses 15[h] for the same reasons as 1[e].

hh) 15[i]wherein the test traffic is conveyed via the switch to the aid trace connecting to the first subsidiary module, and to report that a failure has occurred if the test traffic does not return to the second

subsidiary module within a predetermined period of time.

145. In my opinion, Ke in view of Lewis discloses 15[i] for the same reasons as 1[f].

ii) Claim 16: Apparatus according to claim 15, wherein the first subsidiary module is configured, under control of the system control processor, to loop back the traffic on the aid trace to the main module substantially without processing data comprised in the test traffic.

146. In my opinion, Ke in view of Lewis discloses claim 16 for the same reasons as claim 2.

jj) Claim 17: Apparatus according to claim 16, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.

147. In my opinion, Ke in view of Lewis discloses claim 17 for the same reasons as claim 3.

kk) Claim 18: Apparatus according to claim 15, wherein the system control processor is operative to select one or more further idle traces for testing among the idle traces in the system, wherein the further idle traces connect to further ports of the switch on the main module, and to repeatedly configure the switch, cause the test traffic to be transmitted, and report the failure when it occurs with respect to the further idle traces until all the idle lines have been tested.

148. In my opinion, Ke in view of Lewis discloses claim 18 for the same reasons as claim 4.

ll) Claim 19: Apparatus according to claim 15, wherein the switch is configured to connect the traces to a network communication trunk, and wherein the traffic comprises communication traffic.

149. In my opinion, Ke in view of Lewis discloses claim 19 for the same reasons as claim 6.

mm) Claim 20: Apparatus according to claim 19, wherein the test traffic is transmitted over the second idle trace while continuing to use the trace that are not idle for carrying the data to the network communication trunk.

150. In my opinion, Ke in view of Lewis discloses claim 20 for the same reasons as claim 7.

nn) 21[pre]: Modular electronic apparatus, comprising:

151. In my opinion, Ke in view of Lewis discloses 21[pre] for the same reasons as 15[pre].

oo) 21[a]: a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;

152. In my opinion, Ke in view of Lewis discloses 21[a] for the same reasons as 15[a].

pp) 21[b]: a main module, plugged into the backplane;

153. In my opinion, Ke in view of Lewis discloses 21[b] for the same reasons as 15[b].

qq) 21[c]: a plurality of subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces; and

154. In my opinion, Ke in view of Lewis discloses 21[c] for the same reasons as 15[c].

rr) 21[d]: a system control processor, which is operative to select first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats, and which is further operative to test the modules by causing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module, by configuring the main module to connect the first and second subsidiary modules, so that a traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module, and by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.

155. In my opinion, Ke in view of Lewis discloses 21[d] for the same reasons as 15[d]–15[i].

ss) Claim 22: Apparatus according to claim 21, wherein the first subsidiary module is configured to loop back the traffic to the main module substantially without processing the data comprised in the test traffic.

156. In my opinion, Ke in view of Lewis discloses claim 22 for the same reasons as claim 2.

tt) Claim 23: Apparatus according to claim 21, wherein the main module comprises a switch, which is coupled to connect the traces to a network communication trunk, and wherein the system control processor is operative to configure switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module during the test.

157. In my opinion, Ke in view of Lewis discloses claim 23 for the same reasons as claim 11.

uu) Claim 24: Apparatus according to claim 23, wherein the system control processor is operative to test one or more of the traces connected to the second subsidiary module while at least some of the traces that are not under test continue to be used for carrying the data from the subsidiary modules to the network communication trunk.

158. In my opinion, Ke in view of Lewis discloses claim 24 for the same reasons as claim 12.

vv) Claim 25: Apparatus according to claim 21, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.

159. In my opinion, Ke in view of Lewis discloses claim 25 for the same reasons as claim 13.

ww) Claim 26: Apparatus according to claim 25, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

160. In my opinion, Ke in view of Lewis discloses claim 26 for the same reasons as claim 14.

D. <u>Ground 2</u>

161. To the extent that the limitations of claims 3, 6, 8, 13, 14, 17, 21, 25 and 26 are not rendered obvious by Ke and Lewis, it is my opinion that they would have been obvious by Ke, Lewis and Sarkinen.

a) Claim 6

162. To the extent that claim 6 is not rendered obvious by Ke and Lewis, it is my opinion that it is rendered obvious by Ke, Lewis and Sarkinen.

163. Sarkinen discloses:

> Network line interface circuitry and switch fabric circuitry is located on one or more printed circuit boards (PCB). For example, the network line interface circuitry may be located on one or more line cards, and the switch fabric circuitry may be located on one or more switch cards. A fabric interface circuit which interfaces the network line interface circuitry to the switch fabric circuitry, is separately located on a fabric interface board that is distinct and isolated from the PCBs associated with the network line interface and switch fabric circuits.

Ex. 1011, ¶13. A POSITA would recognize that the backplane in the '369 patent was a (or, the same as the) printed circuit board. The line cards and fabric cards

were the same as the subsidiary modules, and the fabric interface board was the main module. Sarkinen also makes clear that the traffic transmitted over the line and fabric cards is communication traffic when it states:

> The PCBS are connected to the fabric interface board, and information is communicated between the network line interface circuitry and the switch fabric circuitry via the distinct fabric interface board.

Ex. 10011, ¶13.

164. A POSITA would have been motivated to combine Ke, Lewis and Sarkinen because it would be essential to test the connections between the line cards when idle. As stated above, testing the connections when idle would be optimal as the test would detect hidden failures and prevent any interference with the normal traffic. Finally, as seen in Fig. 4 below, it would be obvious to a POSITA that the fabric interface would act as a switch between the two line cards and be able to set up paths between them.

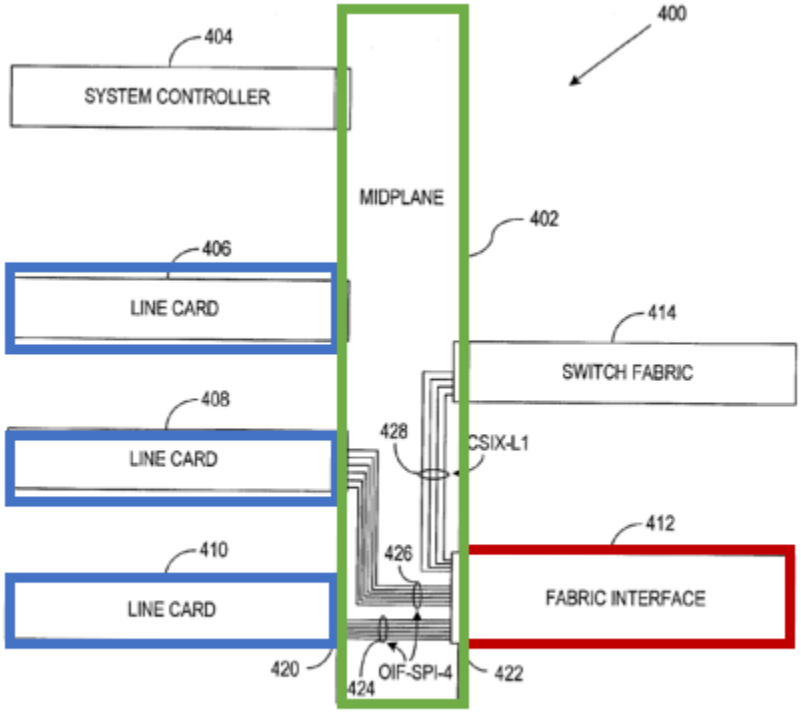


FIG. 4

Ex. 1011, Fig. 4.

165. Therefore, it is my opinion that Ke in view of Lewis and Sarkinen discloses "a method according to claim 1, wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic."

b) Claims 3, 8, 13, 14, 17, 21, 25, and 26

166. To the extent that claims 3, 8, 13, 14, 17, 21, 25, and 26 are not rendered obvious by Ke and Lewis, it is my opinion that they are rendered obvious by Ke, Lewis and Sarkinen.

167. It would be obvious to a POSITA to combine Ke, Lewis and Sarkinen because Sarkinen utilizes a network switch with a backplane, such as that discussed in Ke. Sarkinen also states that "[t]he isolated fabric interface circuit board 316 is designed as an intelligent interface to manage various types of switch fabrics, line cards, protocols, etc." Ex. 1011, ¶58. A POSITA would know that the second subsidiary module would have had to have chosen a data format to communicate a test message and it would have been obvious to choose one of the data formats already in use by the line card. *Id.*

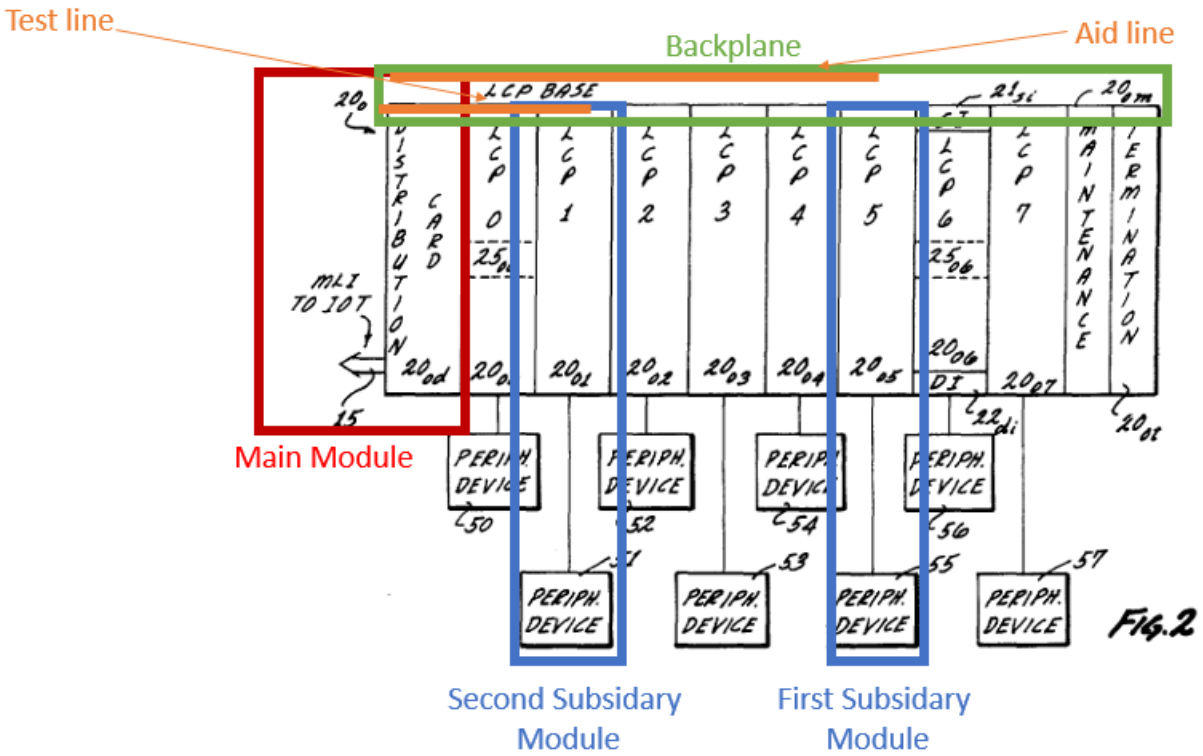
168. Claims 13 and 25 also recite that different formats are associated with a different protocol. As stated above, Sarkinen states that "[t]he isolated fabric interface circuit board 316 is designed as an intelligent interface to manage various types of switch fabrics, line cards, protocols, etc." Ex. 1011, ¶58. In addition, it would have been obvious to a POSITA that different formats of data traffic received by the line cards are associated with different modules.

169. Claims 14 and 26 recite that one protocol is a TDM protocol and the other is a packet data protocol. It would have been obvious to a POSITA that the protocols could be TDM and/or packet data protocols as they are common data protocols. TDM is a common audio-related protocol, while packet data protocol is a common internet and IP protocol. It would also be obvious to a POSITA that the two protocols could be utilized in the same system.

170. Therefore, it is my opinion that Ke in view of Lewis and Sarkinen render obvious claims 3, 8, 13, 14, 17, 21, 25, and 26.

E. <u>Ground 3</u>

171. In my opinion, claims 1–26 of the '369 patent would have been obvious over Cook and Lewis.



172. In the above diagram, it is my opinion that a POSITA would be motivated to test the Ke system with the Lewis loopback test. As depicted above, this could be accomplished by setting up an aid line on Cook's backplane which connects the first subsidiary module and a test line on Cook's backplane which connects the second subsidiary module to the main module, as disclosed in Lewis.

The modules would then be able to route the test packet through the aid and test lines to perform Lewis's loopback test. Ex. 1009, 4:42–54.

173. In my opinion, a POSITA would be motivated to combine Cook and Lewis because both references discuss testing connections in a system which contains multiple components. Specifically, Cook recites a DCU coupled to the IOT that directs traffic to the LCPs on a backplane, while Lewis discusses testing peripheral controllers via a control processor/circuit. Ex. 1010, 28:62–29:7; Ex. 1009, 3:47–53. In my opinion, a POSITA would have understood the benefits of a loopback test in the context of a backplane with a DCU and thus would have been motivated to combine the testing protocol in Lewis with the structure disclosed in Ke.

174. Cook explains that the system in which it discloses can have many different types of peripheral devices added to the LCPs. Specifically, Cook lists:

> The general configuration of a data processing system typically comprises a processor or processors, a main memory, and a plurality of various types of peripheral devices or terminals (sometimes called I/O units), which more specifically may be card readers, magnetic tape units, card punches, printers, disk files, supervisory terminals, and so on.

Ex. 1010, 1:43–49. Based on this disclosure, a POSITA would have been motivated to look at other testing configurations, like the one disclosed in Lewis. A POSITA would know that a backplane could be tested by a loopback test. A POSITA would

also know that a loopback test would be useful in a backplane-based system because a loopback test could test the connections between the different boards connected to the backplane. In my opinion, a POSITA would also have known that testing between the different boards would be essential because sometimes data needs to be transferred to and from different boards on the backplane. Further, Cook states that it would be beneficial to "tak[e] the load off of the processing unit and distributing it among a variety of Intelligent I/O Interface units which can work independently of the central processor in handling data transfer operations." Ex. 1010, 1:27–31. A POSITA therefore would have been motivated to apply the loopback testing between two peripherals in Lewis to the structure in Cook to test the connection between two boards in the backplane.

175. Lewis further discloses "[b]oth message and circuit switches are connected via serial links to one or more peripheral controllers llA and llB, the peripheral controllers being connected to peripherals 12A, 12B, 13 etc. via peripheral interface units." Ex. 1009, 3:53–57. Specifically, a POSITA would have been motivated to apply the loopback testing between two peripheral interfaces in Lewis to the input/outputs structure of board-pins in Cook since the input/outputs structure consist of bidirectional input/outputs acting as interfaces and participating in testing the connection between two boards in the backplane.

176. Additionally, a POSITA would have been motivated to test the backplane lines in Cook while they were idle as disclosed in Lewis. Ex. 1009, 2:19–2. Cook states that connections may not be made to LCPs when they are busy. Ex. 1010, 23:61–24:27. A POSITA would understand that the ideal time to test the lines is when the lines are idle because the test would not disrupt traffic.

177. Finally, in my opinion, a POSITA would have known there was a reasonable expectation of success to implement the testing in Lewis with the structure in Cook because Cook discusses a "poll test" as one of many possible ways for testing backplanes. Ex. 1008, 1:30–2:18. Cook acknowledged that there were multiple possible techniques for testing backplanes. Ex. 1008, 1:30–2:18. Further, Cook explains that the DCU and IOT work together to control the communications and testing of individual LCPs, which would indicate to a POSITA that a test like that described in Lewis could be implemented. Ex. 1010, 31:63–32:41. Thus, a POSITA would therefore have a reasonable expectation of success of the testing from Lewis.

178. Specifically, a POSITA would have found in the I/0 Subsystem of Cook using LCP, "the Main System (of Processor and Main Memory) is also provided with a unit called an Input-Output Translator unit (IOT) which becomes part of the Main System and provides an interface …" Ex. 1010, 4:64–67. Lewis similarly discloses a line interconnected interface when it states "[b]oth message and circuit

switches are connected via serial links to one or more peripheral controllers 11A and llB, the peripheral controllers being connected to peripherals 12A, 12B, 13 etc. via peripheral interface units." Ex. 1009, 3:53–57.

179. Therefore, it is my opinion that a POSITA would have understood that the loopback testing between specific peripherals in Lewis could be employed in Cook by the DCU to control testing between specific LCPs, including two LCPs within a single LCP Base Module.

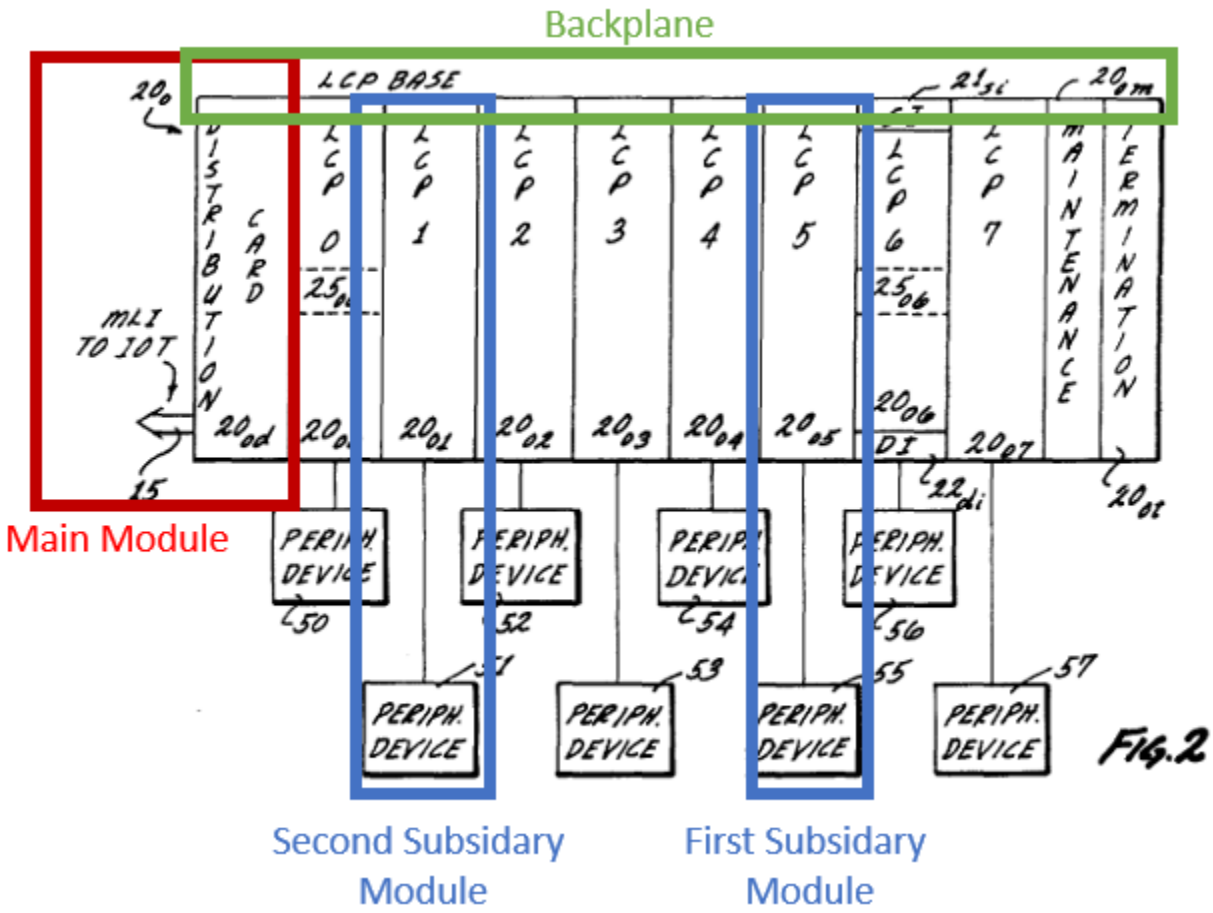
a) 1[pre]: In an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system, comprising:

180. In my opinion, to the extent the preamble is limiting, Cook in view of Lewis discloses 1[pre]. Cook discloses a digital computing and processing system. Cook's system which contains an LCP Base Module, LCPs, a DCU and an IOT. Ex. 1010, 5:5–19.

> The Line Control Processor's (LCP's) are organized in groups of eight called the LCP Base Module each of which has a single "Distribution Card Unit" which provides the interface between the Input-Output Translator, IOT, of the Main System and the eight LCP of any given Base Module. Each Base Module also carries a Maintenance Card unit which can provide all maintenance and checking functions for the

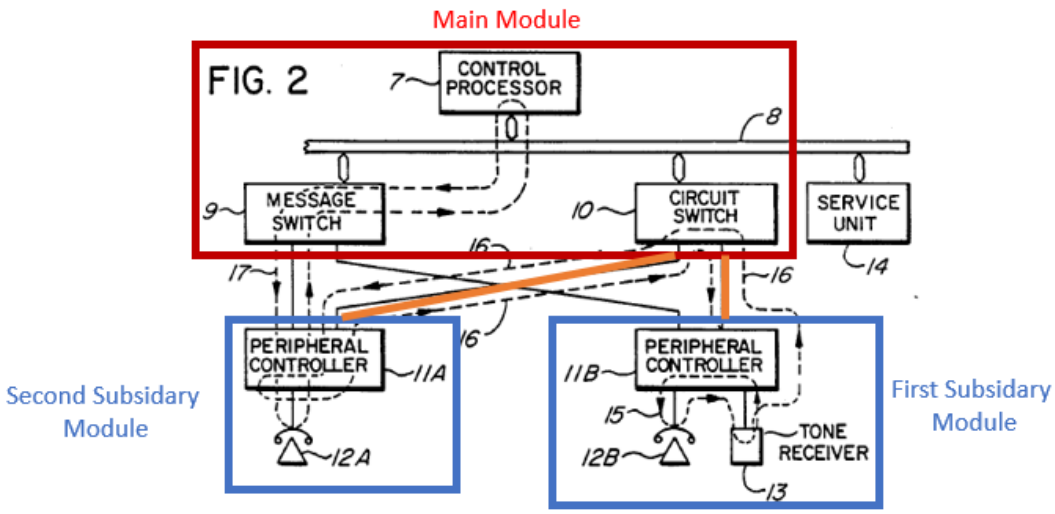
> group of eight LCP's of the Base Module. Each Base Module is also provided with one common "Termination Card Unit" which provides common clocking functions for all the LCP's of the group and also provides proper terminations for the transmission lines which connect the various LCP's, the Distribution Card, and the Maintenance Card of that particular Base Module.

Ex. 1010, 5:5–19. A POSITA would understand that the LCPs are akin to the subsidiary modules, and the DCU (along with the IOT) is akin to the main module. Ex. 1010, 5:5–19. Further, the LCP Base Modules contain a backplane which connects the LCPs to the DCU. Ex. 1010, 28:62–64. The configuration is detailed in Fig. 2, below.



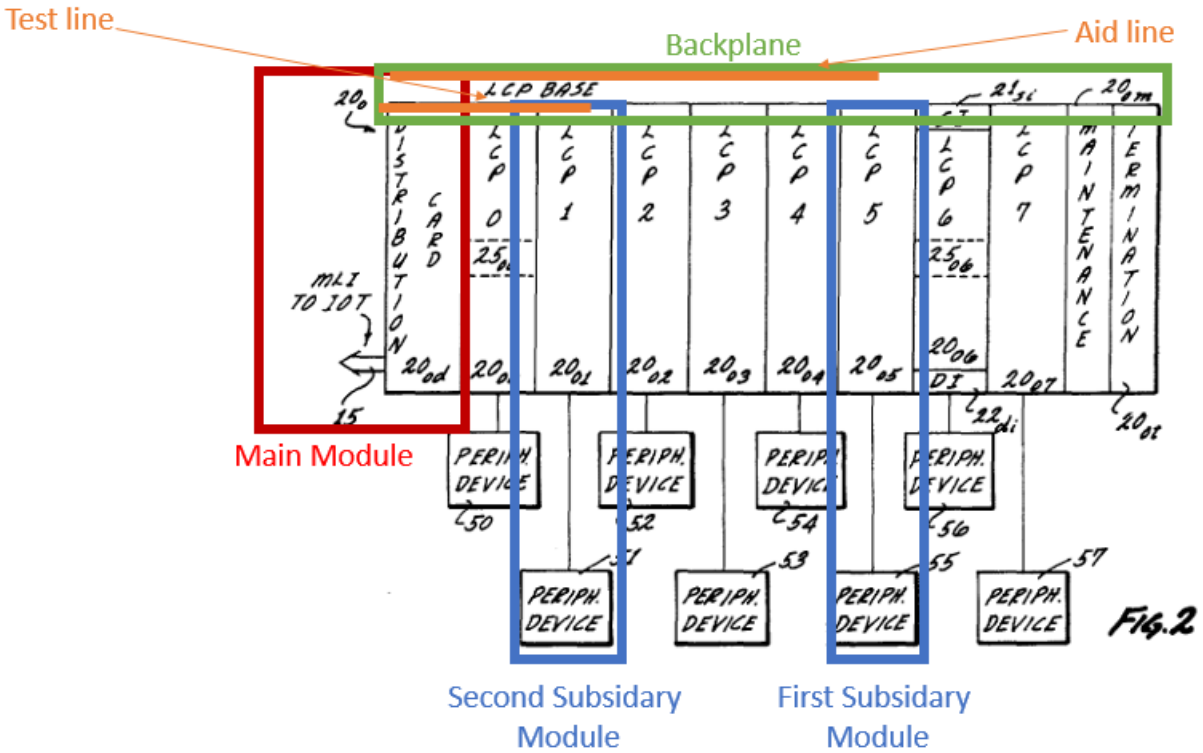
Ex. 1010, Fig.2.

181. Similarly, Lewis also has a circuit switch, a control processor 7, and message switch 9. Ex. 1010, 3:47–60. It would be obvious to a POSITA to view these units together as akin to the main module in the '369 patent. The system in Lewis also describes having multiple peripheral controllers (11A, 11B) which are connected to peripherals (12A, 12B, 13). Ex. 1010, 3:47–60. It would be obvious to a POSITA to view these peripherals as subsidiary modules.



Ex. 1010, Fig. 2.

182. Due to their similarities, it is my opinion that Lewis would have been obvious to a POSITA to combine with Cook. Specifically, as depicted below, it would be obvious to a POSITA that the backplane in Cook would perform the loopback test from Lewis with connections between the main module and subsidiary modules.



183. Cook discloses that the backplane may be inactive or idle. Specifically, Cook discloses that:

> An IOSF (I/O Send Flip-Flop) is used and put in a reset state at this time to enable the bidirectional data lines for transfer of data from the System 10 over to the LCP. There are provided multiplexor control levels SLAIN (Select A Input Multiplexor) and SLBIN (Select B Input Multiplexor). These are both inactive, connecting the data lines to the input multiplexor network 24xl of FIGS. 6B and 6D. There are other multiplexor control levels SLARAM (Select A Level Terminal Bus Multiplexor) and SLBRAM (Terminal Bus Multiplexor Select B Level). These also are both inactive, connecting the input multiplexor

> network 24xl to the input of the Terminal Bus Multiplexor Network 24x2.

Ex. 1010, 52:48–61. A POSITA would have understood based on this disclosure that the lines could be idle at time. Alternatively, it would have been obvious to a POSITA that the lines in the backplane would sometimes be idle or not in use. In addition, Lewis explains that it is optimal to perform the loopback test when the lines are idle as to not impede on the normal traffic. Ex. 1009, 2:19–20, 13:31–34. Based on this, it would have been obvious to a POSITA to combine Cook with Lewis.

184. Cook discloses a way to test the system called a Poll Test. Ex. 1010, 23:41–55; 31:63–32:41.

> The "Poll Test" is an algorithm used by the LCP Base Module to establish connection between the Base Module and a particular LCP; the Poll Test algorithm is a connection which is initiated by the IOT (as contrasted with an algorithm called "poll request" which is a connection initiated by the LCP). Once the connection between the LCP Base Module and the specific LCP is established, the Base Module, such as 200 of FIGS. 1A and 2, becomes transparent to data transfers between the LCP and the IOT. The "Poll Test" algorithm also checks for priority, transmission errors, and busy conditions, any one of which, if detected, could abort the connection attempt.

Ex. 1010, 23:43–55. Cook further discloses:

> [T]he Processor 10p starts the chain of input-output operations by the execution of an Initiate I/O Instruction. In this situation, the Processor passes certain information, including the channel number of the desired

LCP over to the IOT Initiation Module 10ta of FIG. 5C. The channel number is decoded to determine the Base Module number and the address of the LCP, which are then passed over to the Connection Module 10tb. The Connection Module then selects the proper LCP Base Module and sends a signal (channel select) to the appropriate Distribution Card, as 20od, for that Base Module, as 200, requesting that a connection attempt be made. The above described operation is called a "Poll Test" and is a means for the Main System to seek connection to an LCP; it is, further, a method by which the Distribution Card 20od, in response to the connection request, also attempts to connect to a specific LCP.

Following the transmission of a "Channel Select", the IOT 10t sends the address of the desired LCP to the Distribution Card in the selected Base Module. At the same time, the IOT sends "Address Select" to all Base Modules in the system. The Distribution Card that receives both the Address Select and Channel Select begins a "Poll Test" and responds to the IOT with an "LCP Strobe"; the Distribution Cards that received the Address Select only, consider it as a "busy" signal, and they are inhibited from communication with the IOT. When the IOT 10t receives the LCP Strobe, it drops the Channel Select.

When the Distribution Card receives an "Address Select" and "Channel Select", a signal is generated which enables the LCP address to be placed into an LCP address register in the Distribution Card. The BCD (Binary Coded Decimal) output of the LCP address register is decoded to enable one of eight lines. Each line represents one LCP in the Base Module. When an LCP detects that its address line is active, then that LCP responds to the Distribution Card with the signal LCPCON

> meaning "LCP connected". When this connected signal is received in the Distribution Card, a connect flip-flop (CONF) is set. Then depending on the state of the I/O send line (IOSND/FIG. 6C) from the connected LCP, this will cause an activation of control lines for either receiving data or sending data as between the LCP and the IOT (FIG. 6C).

Ex. 1010, 31:63–32:41. A POSITA would understand that the DCU and IOT (the main module) are akin to the switch in the '369 patent as it directs traffic to each of the different LCPs. Cook also discloses that the LCPs and DCU are connected to ports of the backplane. Ex. 1010, 28:62–29:7. Specifically, Cook states:

> A local common backplane is provided in each of the LCP Base Modules 200, 201, 202, etc. Each backplane connects to all the eight LCP's in the Base Module. The backplane is constructed so that all signal lines are bussed the length of the backplane, thus making each line available to all LCPs in that Base Module. From the individual position of a single LCP, these backplane lines fall into two general types: (a) those going to the Distribution Card and on to the IOT; and (b) those going to the Maintenance and Termination Cards. With the exception of the various clock and voltage lines, those lines going to the Maintenance Card, (such as for example, 20om of FIG. 2) are used for local or off-line maintenance functions.

Ex. 1010, 28:62–29:7. It is my opinion that a POSITA would have understood that the connections with the backplane act as the ports between the LCPs and the backplane.

185. Therefore, it is my opinion that Cook in view of Lewis discloses "an electronic system that includes a main module and at least first and second subsidiary modules, each of said at least first and second subsidiary modules connected to the main module by one or more lines for carrying data, at least some of which lines are sometimes idle, the main module including a switch having ports connected to the lines, a method for self-testing the system."

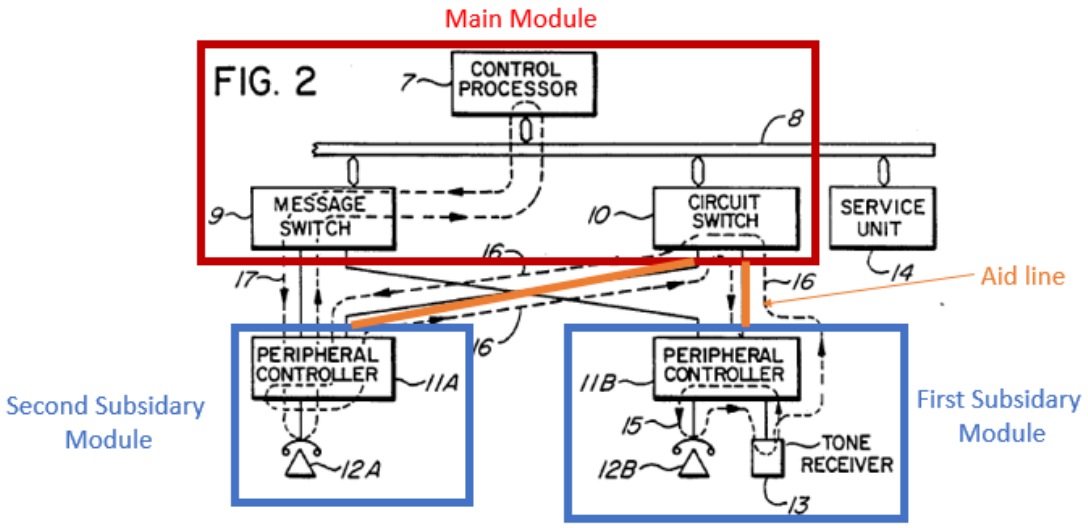
b) 1[a]: selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line;

186. In my opinion, Cook in view of Lewis discloses 1[a]. Lewis discloses a "a loop around arrangement in a switching system whereby transmission paths of the system can be tested." Ex. 1009, 1:4–6. Further, Lewis discloses that "[t]esting is also preferred to be performed during times when the switches or links are idle." Ex. 1009 2:19–20. Lewis states that:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit

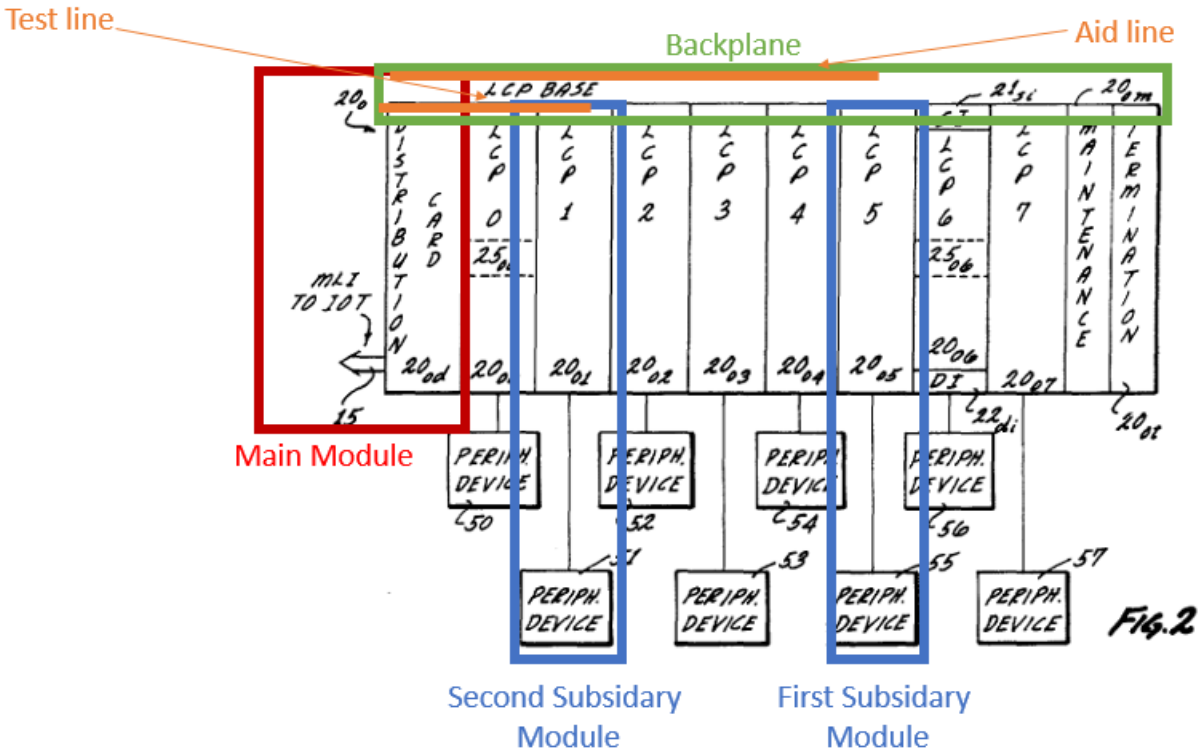
switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

Ex. 1009, 4:23–41. This system is demonstrated on the diagram below:



Ex. 1009, Fig. 2.

187. As per above, the modules in Cook are connected via a port on the backplane. Ex. 1008, 1:15–23. It would be obvious to a POSITA that the modules in Lewis could be connected to the main module via a port on backplane as they are in Cook. A POSITA would also know that the modules in Lewis could be connected to the main module via a port on a backplane.



188. Therefore, it is my opinion that Cook in view of Lewis discloses "selecting a first idle line among idle lines connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid line."

c) 1[b]: instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line;

189. In my opinion, Cook in view of Lewis discloses 1[b]. Lewis discloses "instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line." Specifically, Lewis states:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system.

> For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.
>
> In a similar manner other forms of loops can be set up and tested. For example the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface. A test tone signal is injected into the loop by service unit 14 and the return signal received via the message links as described earlier with reference to local loop 15. In this manner a complete or long loop between peripheral interfaces can be set up and tested.

Ex. 1009, 4:23–54. A POSITA would have understood this disclosure as requiring instructing the first subsidiary module to loop back traffic it receives back at the circuit switch. Alternatively, it would have been obvious to a POSITA that the main

module would instruct the subsidiary module to loop back traffic. Ex. 1009, 4:23–41.

190. Therefore, it is my opinion that Cook in view of Lewis discloses "instructing the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid line."

d) 1[c]: selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module;

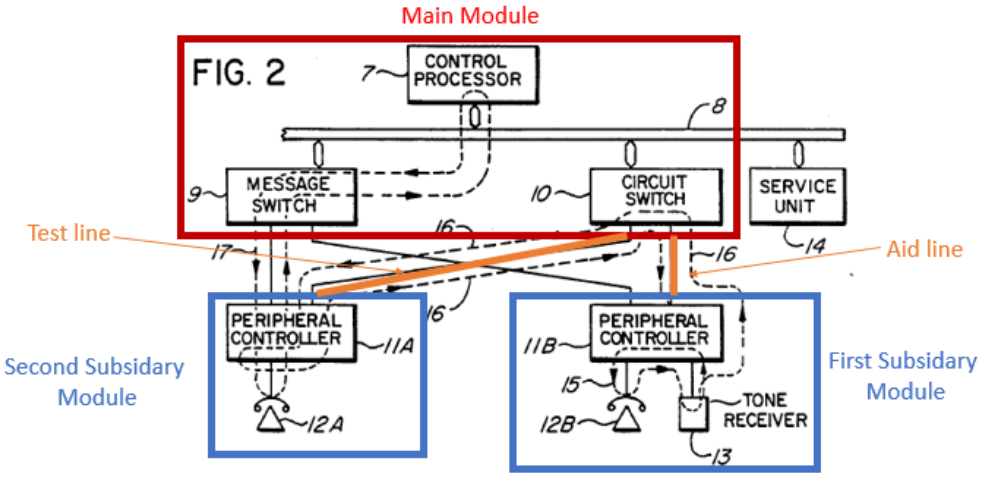
191. In my opinion, Cook in view of Lewis discloses 1[c]. Lewis discloses "selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module." Specifically, Lewis states:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes

back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

In a similar manner other forms of loops can be set up and tested. For example the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface. A test tone signal is injected into the loop by service unit 14 and the return signal received via the message links as described earlier with reference to local loop 15. In this manner a complete or long loop between peripheral interfaces can be set up and tested.

Ex. 1009, 4:23–54. As described above, the system selects a line between the second subsidiary module and the circuit switch ("test line") for testing.



192. As I stated in 1[a], a POSITA would have understood or found it obvious that the second subsidiary module is connected via a port to the circuit switch.

193. Therefore, it is my opinion that Cook in view of Lewis discloses "selecting for testing a second idle line among the idle lines connecting the second subsidiary module to a second port of the switch on the main module."

e) 1[d]: configuring the switch to link the first and second ports;

194. In my opinion, Cook in view of Lewis discloses 1[d]. Specifically, in view of Cook, it would have been obvious to a POSITA that the main module would link the first and second ports to close the loop between the subsidiary modules. It also would have been obvious to a POSITA that when the loopback is set up as described in 1[a] and 1[c], it is done by configuring the switch to link the first and second ports to form the loopback circuit.

195. Therefore, it is my opinion that Cook in view of Lewis discloses "configuring the switch to link the first and second ports."

f) 1[e]: transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module; and

196. In my opinion, Cook in view of Lewis discloses 1[e]. Lewis discloses:

According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal having passed through the loop passes back through the message switch link system just described for receipt by the service unit 14. In this manner a small, isolated transmission loop is established and tested.

In a similar manner other forms of loops can be set up and tested. For example the control processor 7 can send messages through bus 8 via the message switch 9 to the peripheral controller 11A, and to circuit switch 10 to set up a circuit switch loop 16 from a peripheral telephone 12A interface, through peripheral controller 11A, circuit switch 10, peripheral controller 11B to the tone receiver 13 interface. A test tone signal is injected into the loop by service unit 14 and the return signal received via the message links as described earlier with reference to local loop 15. In this manner a complete or long loop between peripheral interfaces can be set up and tested.

Ex. 1009, 4:23–54. A POSITA would understand that this discloses transmitting test data to the subsidiary modules.

197. Therefore, it is my opinion that Lewis discloses "transmitting test traffic over the second idle line from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid line connecting to the first subsidiary module."

g) 1[f]: reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

198. In my opinion, Cook in view of Lewis discloses 1[f]. Lewis discloses:

> The main controller, **having received a message signal via the system described above of the returned test signal, formulates a message and** transmits it to the service unit 214, of the test signal, and also formulates a message signal to be returned to the peripheral acknowledging that it has received the message. This signal is downloaded via parallel bus 212 into COMRAM BUFFER 214, which operates in the reverse direction in the same way as described earlier.

Ex. 1009, 14:3–11 (emphasis added). In my opinion, a POSITA would have understood that this discloses "reporting a failure has occurred." Further, a POSITA would understand that a failure constitutes the main module not receiving a test message from the second subsidiary module within a predetermined period of time. This sort of "time out" result is common and well understood. For example, ICMP messages, which have been commonplace in the field since at least 1989, send a

timeout message if the ICMP message was not returned in a reasonable amount of time. Ex. 1012 (RFC 1122), 57–58.

199. Therefore, it is my opinion that Cook in view of Lewis discloses "reporting that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time" or it would have been obvious to a POSITA.

h) Claim 2: A method according to claim 1, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.

200. In my opinion, Cook in view of Lewis discloses claim 2 for the same reasons discussed in claim 1[b]. Specifically, Lewis discloses:

> According to the present invention local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system. For example, to test a short transmission path between a telephone set 12B interface and the tone receiver 13 through peripheral controller 11B, the control processor 7 sends control messages via bus 8 and message switch 9 to peripheral controller 11B to set up a communication loop between the telephone set interface and tone receiver 13 through the switching matrix (e.g. time division switching matrix) in peripheral controller 11B, but excluding links to the circuit switch 10, in this case. In addition, a test message is sent from service unit 14 via bus 8, message switch 9 and peripheral controller 11B into the loop, and the resulting signal **having passed through the loop**

> **passes back through the message switch link system just described for receipt by the service unit 14**. In this manner a small, isolated transmission loop is established and tested.

Ex. 1009, 4:23–41 (emphasis added). In my opinion, a POSITA would have understood that this disclosure represents the idea that test traffic goes through the first subsidiary module without substantial processing.

201. Therefore, it is my opinion that Cook in view of Lewis discloses "instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic."

i) Claim 3: A method according to claim 2, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.

202. In my opinion, Cook in view of Lewis discloses claim 3 for the same reasons discussed in claim 2. Additionally, Cook discloses multiple formats including those described in Fig. 5A:

1A DESCRIPTORS USED TO GENERATE LCP COMMAND MESSAGES (IM)

DESCRIPTION	OP	VARIANT	A ADDRESS	B ADDRESS	C ADDRESS
READ, FORWARD	40	SLLL	AAAAAA	BBBBBB	
READ, FORWARD	50	SLLL	AAAAAA	BBBBBB	CCCCCC
READ, BACKWARD	41	SLLL	AAAAAA	BBBBBB	
READ, BACKWARD	51	SLLL	AAAAAA	BBBBBB	CCCCCC
WRITE, FORWARD	42	SLLL	AAAAAA	BBBBBB	
WRITE, FORWARD	52	SLLL	AAAAAA	BBBBBB	CCCCCC
WRITE, BACKWARD	43	SLLL	AAAAAA	BBBBBB	
WRITE, BACKWARD	53	SLLL	AAAAAA	BBBBBB	CCCCCC
TEST	44	SLLL			
TEST	54	SLLL	AAAAAA	BBBBBB	CCCCCC
ECHO	48	SLLL	AAAAAA	BBBBBB	
ECHO	58	SLLL	AAAAAA	BBBBBB	CCCCCC

↑↑↑↑
ABCD
DIGITS

NOTES:
S = VARIANTS USED BY THE IOT
- 8 = INHIBIT DATA TRANSFER TO MEMORY
- 4 = RESERVED
- 2 = ASCII TRANSLATION
- 1 = RESERVED

L = LCP VARIANTS WHICH ARE SENT UNMODIFIED TO LCP

1B DESCRIPTORS USED BY IOT

EXTENDED RD STORE	70 XX CC	AAAAAA	BBBBBB
CONDITIONAL CANCEL	71 XX CC	(CONVERTS TO TEST OP FOR LCP)	
UNCONDITIONAL CANCEL	72 XX CC	(CLEARS THE LCP)	

CC = CHANNEL DESIGNATION (00-77)

FIG. 5A

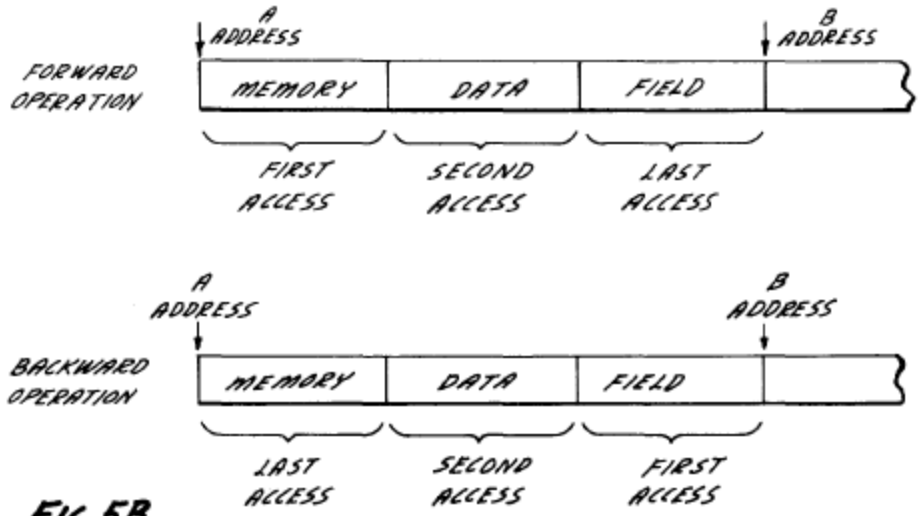


FIG. 5B

DATA FIELD BOUNDARIES

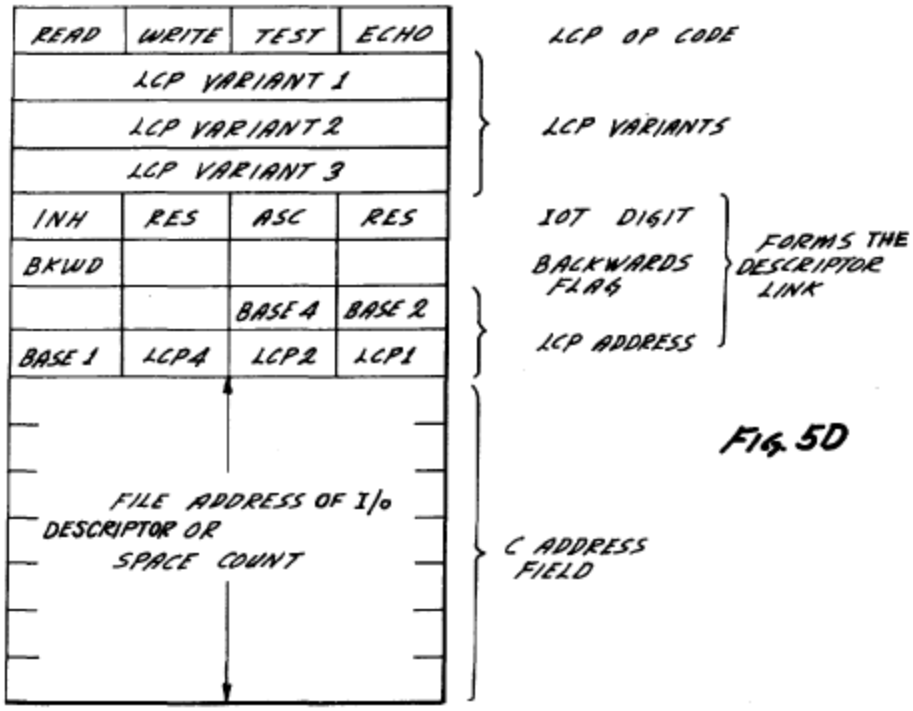


FIG. 5D

IOT DESCRIPTOR REGISTER INFORMATION

Ex. 1010, Figs. 5A, 5B, 5D. "FIG. 5A [] shows the four types of standard operational messages used for controlling the LCP's: these are 1. Read 2. Write 3. Test 4. Echo" Ex. 1010, 21:36–42. "FIG. 5B shows the data field boundaries of operations going in the forward direction and in the backward direction. (Forward = System to LCP)." Ex. 1010, 21:33–35.

203. A POSITA would have understood that the format for the loopback test traffic disclosed in Lewis could be in a different or second format from those described in Cook.

204. Alternatively, it would have been obvious to a POSITA that the subsidiary modules could send and receive data in multiple formats because different messages passed between the modules may require different formats and would have been organized differently.

205. Therefore, it is my opinion that Cook in view of Lewis discloses "a method according to claim 2, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format."

j) Claim 4: A method according to claim 1, further comprising: selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and repeating the configuring the switch, transmitting the test traffic,

and reporting that the failure has occurred with respect to the further idle lines until all the idle lines have been tested.

206. In my opinion, Cook in view of Lewis discloses claim 4, for the same reasons as claims 1[a] and 1[c]. Specifically, Lewis discloses selecting multiple idle lines that connect to ports on the circuit switch in the main module. *See* VII.E.b and VII.E.d. Lewis also discloses that "local supervisory loops of virtually any length can be set up to test virtually any switch or link in the system." Ex. 1009, 4:23–25. In my opinion, a POSITA would have understood that any and all of the idle lines could be added to the same loop for testing. Further, it would have been obvious to a POSITA that the same process for choosing idle lines could be repeated until all the idle lines have been tested. In fact, it would have been obvious to a POSITA to run the test repeatedly until all the idle lines were tested. A POSITA would also have been motivated to repeat the test in order to make sure that all potential hidden failures were discovered.

207. Therefore, it is my opinion that Cook in view of Lewis discloses "selecting one or more further idle lines for testing among the idle lines in the system, wherein the further idle lines connect to further ports of the switch on the main module; and repeating the configuring the switch, transmitting the test traffic, and reporting that the failure has occurred with respect to the further idle lines until all the idle lines have been tested."

k) Claim 5: A method according to claim 1, wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

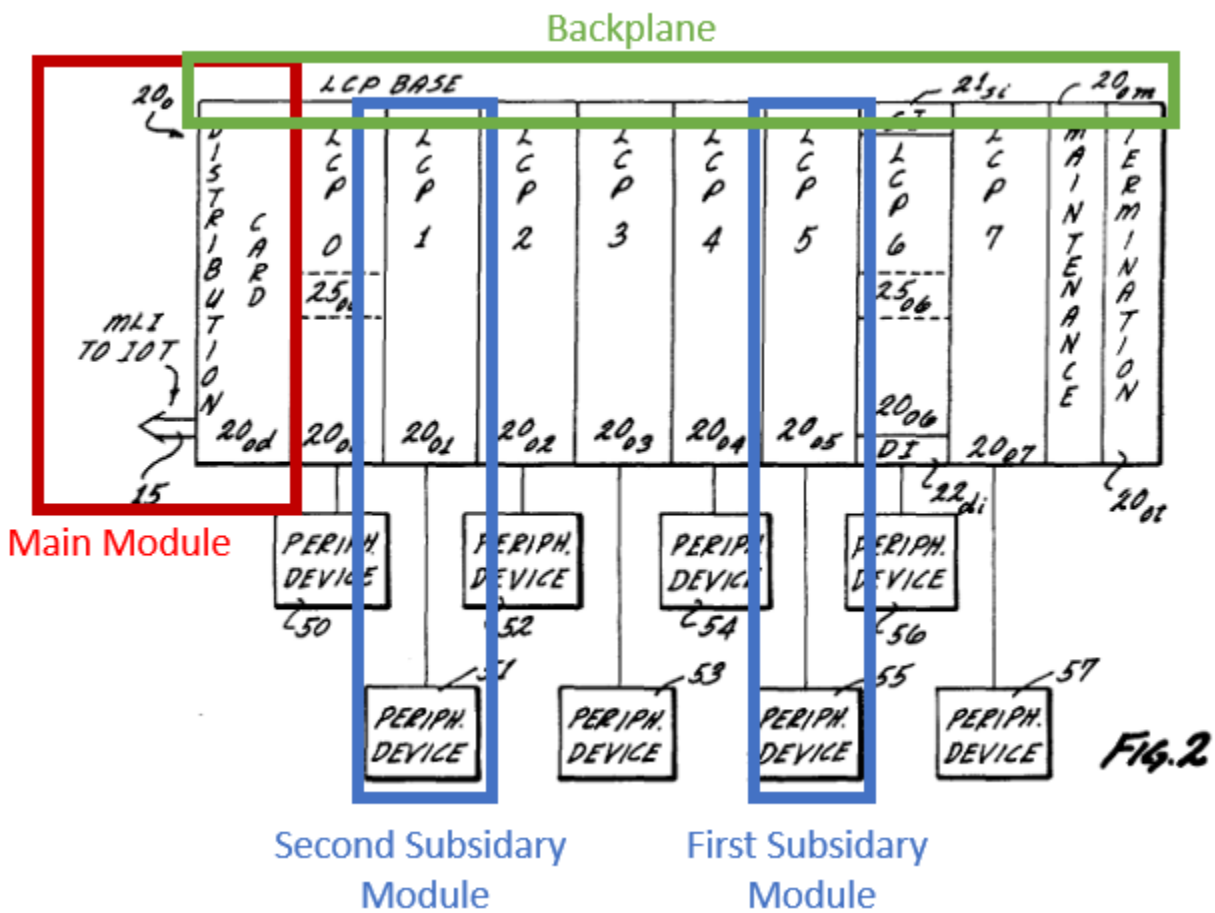
208. In my opinion, Cook in view of Lewis discloses Claim 5. Cook discloses a digital computing and processing system. Cook's system which contains an LCP Base Modules, LCPs, a DCU and an IOT. Ex. 1010, 5:5–19.

> The Line Control Processor's (LCP's) are organized in groups of eight called the LCP Base Module each of which has a single "Distribution Card Unit" which provides the interface between the Input-Output Translator, IOT, of the Main System and the eight LCP's of any given Base Module. Each Base Module also carries a Maintenance Card unit which can provide all maintenance and checking functions for the group of eight LCP's of the Base Module. Each Base Module is also provided with one common "Termination Card Unit" which provides common clocking functions for all the LCP's of the group and also provides proper terminations for the transmission lines which connect the various LCP's, the Distribution Card, and the Maintenance Card of that particular Base Module.

Ex. 1010, 5:5–19. A POSITA would understand that the LCPs are akin to the subsidiary modules, the DCU (along with the IOT) is akin to the main module. Ex. 1010, 5:5–19. Further, the LCP Base Modules contains a backplane which connects the LCPs to the DCU. Specifically, Cook discloses that:

A local common backplane is provided in each of the LCP Base Modules 200, 201, 202, etc. Each backplane connects to all the eight LCP's in the Base Module. The backplane is constructed so that all signal lines are bussed the length of the backplane, thus making each line available to all LCPs in that Base Module. From the individual position of a single LCP, these backplane lines fall into two general types: (a) those going to the Distribution Card and on to the IOT; and (b) those going to the Maintenance and Termination Cards.

Ex. 1010, 28:62–29:3. The configuration is detailed in Fig. 2, below.



Ex. 1010, Fig. 2.

209. It would be obvious to a POSITA that the LCPs and DCU are plugged into the backplane because that is how backplanes operate. Alternatively, it would have been obvious to a POSITA that the DCU and LCPs plug into the backplane. *Id.*

210. Therefore, it is my opinion that Cook in view of Lewis discloses "a method according to claim 1, wherein the main module and said at least first and second subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane."

l) Claim 6: A method according to claim 1, wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic.

211. In my opinion, claim 6 would have been obvious to a POSITA over Cook in view of Lewis. A POSITA would know that an electrical system which utilizes a backplane could have a network switch or another type of network device. A POSITA would also have understood one of the modules inserted into the backplane could be connected to the internet through that network trunk.

212. Therefore, it is my opinion that Cook in view of Lewis would render obvious "wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic."

m) Claim 7: A method according to claim 6, wherein transmitting the test traffic comprises testing the second idle line while continuing to use the lines that

are not idle for carrying the data to the network communication trunk.

213. In my opinion, Cook in view of Lewis disclose claim 7. Specifically, Lewis refers to idle lines when it says:

> Assuming that the location of an idle path has been determined, the main controller sends a message signal to the peripheral controllers, and to the circuit switch processor 218 to set up the circuit path.

Ex. 1009, 14:30–34. Lewis also states that "[t]esting is preferred to be performed during times when the switches or links are idle." Ex. 1009, 2:19–20. A POSITA would have known that these disclosures mean that the test could occur on idle lines, while the non-idle lines continue carrying normal traffic.

214. Therefore, it is my opinion that Cook in view of Lewis discloses "transmitting the test traffic comprises testing the second idle line while continuing to use the lines that are not idle for carrying the data to the network communication trunk."

n) 8[pre]: In an electronic system that includes a main module and multiple subsidiary modules, each of said multiple subsidiary modules being connected to the main module by one or more lines for carrying data, a method for self-testing the system, comprising:

215. In my opinion, Cook in view of Lewis discloses 8[pre] for the same reasons as 1[pre].

o) 8[a]: selecting first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary

modules being configured to transmit and receive the data in different, respective first and second formats;

216. In my opinion, Cook in view of Lewis discloses 8[a] for the same reasons as 1[a], 1[c], and claim 3. Both Cook and Lewis disclose that the peripherals in their respective systems could be different types. Ex. 1010, 1:47–49; Ex. 1009, 4:23–41. It is my opinion that a POSITA would have understood that the first and second subsidiary modules could be different types.

p) 8[b]: instructing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module;

217. In my opinion, Cook in view of Lewis discloses 8[b] for the same reasons as 1[b].

q) 8[c]: configuring the main module to connect the first and second subsidiary modules, so that the traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module; and

218. In my opinion, Cook in view of Lewis discloses 8[c] for the same reasons as 1[c].

r) 8[d]: testing the system by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.

219. In my opinion, Cook in view of Lewis discloses 8[d] for the same reasons as 1[f] and claim 3. Specifically, Lewis states:

> The main controller, **having received a message signal via the system described above of the returned test signal, formulates a message and** transmits it to the service unit 214, of the test signal, and also formulates a message signal to be returned to the peripheral acknowledging that it has received the message. This signal is downloaded via parallel bus 212 into COMRAM BUFFER 214, which operates in the reverse direction in the same way as described earlier.

Ex. 1009, 14:3–11 (emphasis added). This passage describes the main module acknowledging to have received the return signal if the test message was returned successfully. Ex. 1009, 14:3–11. A POSITA would understand that the main module confirms that the test message must be returned intact before it can send an acknowledged receipt because the test would be deemed a failure if the message did not return intact or did not return.

220. Therefore, it is my opinion that Cook in view of Lewis discloses "testing the system by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module."

s) Claim 9: A method according to claim 8, wherein instructing the first subsidiary module comprises configuring the first subsidiary module to loop back the traffic to the main module substantially without processing data comprised in the test traffic.

221. In my opinion, Cook in view of Lewis discloses claim 9 for the same reasons as claim 2.

t) Claim 10: A method according to claim 8, wherein the main module and subsidiary modules comprise cards, which are plugged into a backplane, and wherein the lines comprise traces on the backplane.

222. In my opinion, Cook in view of Lewis discloses claim 10 for the same reasons as claim 5.

u) Claim 11: A method according to claim 8, wherein the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module.

223. In my opinion, Cook in view of Lewis discloses claim 11 for the same reasons as claim 6 and 1[d]. Further, a POSITA would know that linking the first and second ports is equivalent to the switch connecting lines of the first and second subsidiary modules. Alternatively, it would have been obvious to a POSITA that the switch could connect lines of the first and second subsidiary modules so they can send the test traffic to each other.

224. Therefore, it is my opinion that Cook in view of Lewis discloses "the main module comprises a switch, which is coupled to connect the lines to a network communication trunk, and wherein configuring the main module comprises

configuring the switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module."

v) Claim 12: A method according to claim 11, wherein testing the system comprises testing one or more of the lines of the second subsidiary module while continuing to use at least some of the lines that are not under test for carrying the data from the subsidiary modules to the network communication trunk.

225. In my opinion, Cook in view of Lewis discloses claim 12 for the same reasons as claim 7.

w) Claim 13: A method according to claim 8, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.

226. In my opinion, Cook in view of Lewis discloses claim 13 for the same reasons as claim 3. Further, it would have been obvious to a POSITA that the test traffic in the subsidiary modules could have a different protocol. A POSITA would have been motivated to use a method which does not require the same protocol to be used by the modules, because the modules may use different protocols.

227. Therefore, it is my opinion that Cook in view of Lewis discloses "traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols."

x) Claim 14: A method according to claim 13, wherein one of the first and second protocols is a time domain

multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

228. In my opinion, Cook in view of Lewis discloses claim 14. In my opinion, it would have been obvious to a POSITA that the modules could utilize different protocols, including TDM protocols and packet data protocols, because the type of signal does not matter. Additionally, a POSITA would know that a TDM protocol is used for communications with other modules, while a packet data protocol is used to communicate with other devices over an IP-based network. For example, a textbook which predates the patents states that "two common forms of multiplexing are frequency-division multiplexing (FDM) and time division multiplexing (TDM)". *See* Ex. 1013, 236. The textbook also discusses packet switching which utilizes the packet data protocol. *See* Ex. 1013, 10.

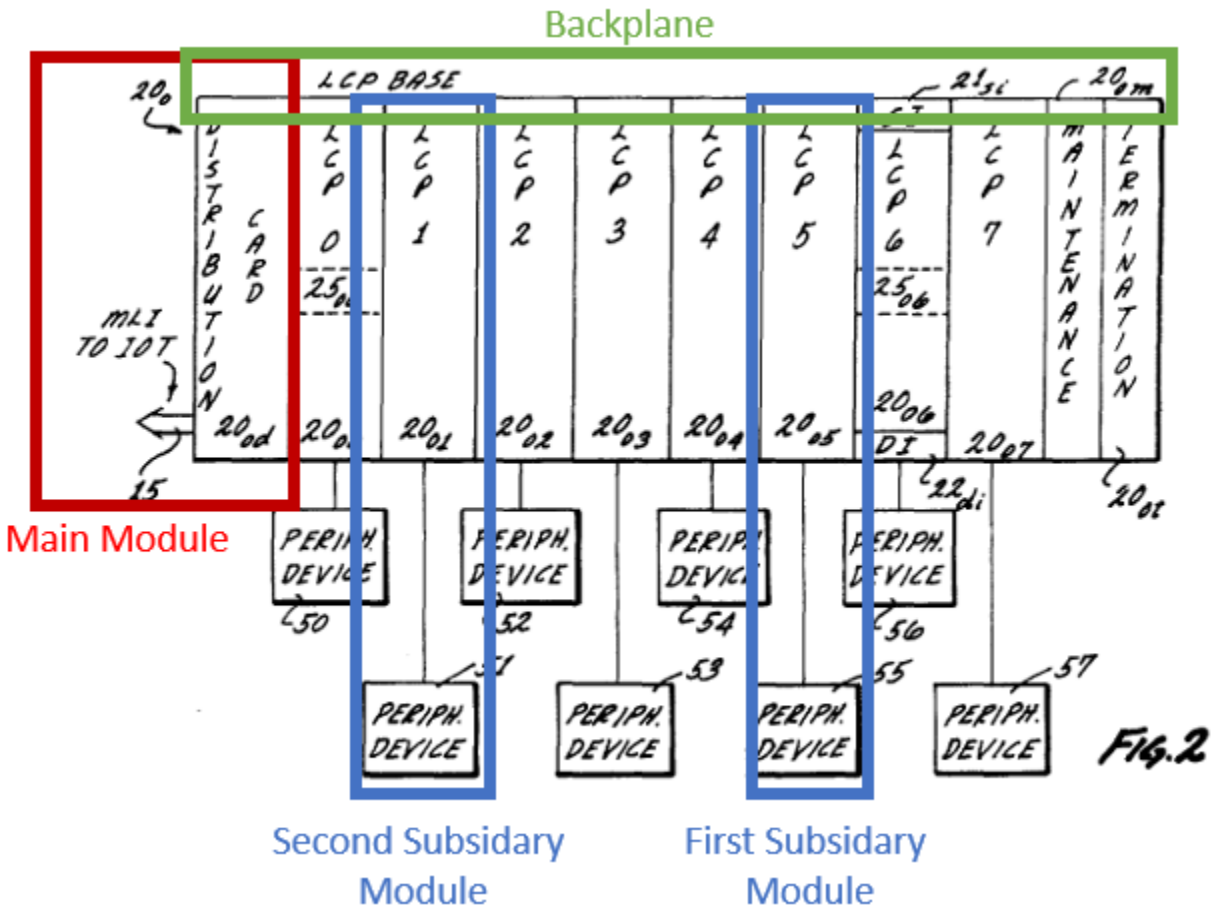
229. Therefore, it is my opinion that Cook in view of Lewis discloses "wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol."

y) 15[pre]: Modular electronic apparatus, comprising:

230. In my opinion, to the extent the preamble is limiting, Cook in view of Lewis discloses 15[pre]. Cook discloses a digital computing and processing system. Cook's system contains an LCP Base Module, LCPs, a DCU and an IOT. Ex. 1010, 5:5–19.

> The Line Control Processor's (LCP's) are organized in groups of eight called the LCP Base Module each of which has a single "Distribution Card Unit" which provides the interface between the Input-Output Translator, IOT, of the Main System and the eight LCP's of any given Base Module. Each Base Module also carries a Maintenance Card unit which can provide all maintenance and checking functions for the group of eight LCP's of the Base Module. Each Base Module is also provided with one common "Termination Card Unit" which provides common clocking functions for all the LCP's of the group and also provides proper terminations for the transmission lines which connect the various LCP's, the Distribution Card, and the Maintenance Card of that particular Base Module.

Ex. 1010, 5:5–19. A POSITA would understand that the LCPs are akin to the subsidiary modules, and the DCU (along with the IOT) is akin to the main module. Ex. 1010, 5:5–19. The configuration is detailed in Fig. 2, below.



Ex. 1010, Fig.2. A POSITA would know that the LCPs can be inserted and changed, like a modular system. In fact, the title of Cook is "Modular block unit for input-output subsystem." Ex. 1010, [19].

231. It is my opinion that a POSITA would have understood that the connections with the backplane act as the ports between the LCPs and the backplane.

232. Therefore, it is my opinion that Cook in view of Lewis discloses "modular electronic apparatus."

z) 15[a]: a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;

233. In my opinion, Cook in view of Lewis discloses 15[a] for the same reasons as claim 5.

aa) 15[b]: a main module, plugged into the backplane, the main module comprising a switch having ports for connection to the traces of the backplane;

234. In my opinion, Cook in view of Lewis discloses 15[b] for the same reasons as 1[pre] and claim 5.

bb) 15[c]: at least first and second subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces, at least some of which traces are sometimes idle; and

235. In my opinion, Cook in view of Lewis discloses 15[c] for the same reasons as 1[pre] and claim 5.

cc) 15[d]: a system control processor, which is operative to select a first idle trace among idle traces connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace,

236. In my opinion, Cook discloses 15[d] for the same reasons as 1[a]. A POSITA would have understood that the DCU has a processor so that it can process data sent to it and route the data to the correct LCP, or to the IOT.

237. Therefore, it is my opinion that Cook in view of Lewis discloses "a system control processor, which is operative to select a first idle trace among idle traces connecting the first subsidiary module to a first port of the switch on the main module to serve as an aid trace."

dd) 15[e] to instruct the first subsidiary module to loop back traffic reaching the first subsidiary module via the aid trace,

238. In my opinion, Cook in view of Lewis discloses 15[e] for the same reasons as 1[b].

ee) 15[f] to select for testing a second idle trace among the idle traces connecting the second subsidiary module to a second port of the switch on the main module, and

239. In my opinion, Cook in view of Lewis discloses 15[f] for the same reasons as 1[c].

ff) 15[g]to configure the switch to link the first and second ports,

240. In my opinion, Cook in view of Lewis discloses 15[g] for the same reasons as 1[d].

gg) 15[h]the system control processor being further operative to cause test traffic to be transmitted over the second idle trace from the second subsidiary module to the main module, wherein the test traffic is conveyed via the switch to the aid trace connecting to the first subsidiary module, and

241. In my opinion, Cook in view of Lewis discloses 15[h] for the same reasons as 1[e].

hh) 15[i] to report that a failure has occurred if the test traffic does not return to the second subsidiary module within a predetermined period of time.

242. In my opinion, Cook in view of Lewis discloses 15[i] for the same reasons as 1[f].

ii) Claim 16: Apparatus according to claim 15, wherein the first subsidiary module is configured, under control of the system control processor, to loop back the traffic on the aid trace to the main module substantially without processing data comprised in the test traffic.

243. In my opinion, Cook in view of Lewis discloses claim 16 for the same reasons as claim 2.

jj) Claim 17: Apparatus according to claim 16, wherein the first and second subsidiary modules are configured to transmit and receive data in different, respective first and second formats, and wherein the test traffic transmitted from the second subsidiary module and looped back by the first subsidiary module is in the second format.

244. In my opinion, Cook in view of Lewis discloses claim 17 for the same reasons as claim 3.

kk) Claim 18: Apparatus according to claim 15, wherein the system control processor is operative to select one or more further idle traces for testing among the idle traces in the system, wherein the further idle traces connect to further ports of the switch on the main module, and to repeatedly configure the switch, cause the test traffic to be transmitted, and report the failure when it occurs with respect to the further idle traces until all the idle lines have been tested.

245. In my opinion, Cook in view of Lewis discloses claim 18 for the same reasons as claim 4.

ll) Claim 19: Apparatus according to claim 15, wherein the switch is configured to connect the traces to a network communication trunk, and wherein the traffic comprises communication traffic.

246. In my opinion, Cook in view of Lewis discloses claim 19 for the same reasons as claim 6.

mm) Claim 20: Apparatus according to claim 19, wherein the test traffic is transmitted over the second idle trace while continuing to use the trace that are not idle for carrying the data to the network communication trunk.

247. In my opinion, Cook in view of Lewis discloses claim 20 for the same reasons as claim 7.

nn) 21[pre]: Modular electronic apparatus, comprising:

248. In my opinion, Cook in view of Lewis discloses 21[pre] for the same reasons as 15[pre].

oo) 21[a]: a backplane, which comprises traces for carrying data between modules that are plugged into the backplane;

249. In my opinion, Cook in view of Lewis discloses 21[a] for the same reasons as 15[a].

pp) 21[b]: a main module, plugged into the backplane;

250. In my opinion, Cook in view of Lewis discloses 21[b] for the same reasons as 15[b].

qq) 21[c]: a plurality of subsidiary modules, plugged into the backplane so as to be connected to the main module by the traces; and

251. In my opinion, Cook in view of Lewis discloses 21[c] for the same reasons as 15[c].

rr) 21[d]: a system control processor, which is operative to select first and second subsidiary modules of different types for testing among the multiple subsidiary modules, the first and second subsidiary modules being configured to transmit and receive the data in different, respective first and second formats, and which is further operative to test the modules by causing the first subsidiary module to loop back traffic reaching the first subsidiary module from the main module, by configuring the main module to connect the first and second subsidiary modules, so that a traffic transmitted by the second subsidiary module is conveyed to the first subsidiary module via the main module and is then looped back via the main module to the second subsidiary module, and by causing the second subsidiary module to transmit test traffic in the second format to the main module, and assessing whether the test traffic is returned intact from the first module.

252. In my opinion, Cook in view of Lewis discloses 21[d] for the same reasons as 15[d]–15[i].

ss) Claim 22: Apparatus according to claim 21, wherein the first subsidiary module is configured to loop back the traffic to the main module substantially without processing the data comprised in the test traffic.

253. In my opinion, Cook in view of Lewis discloses claim 22 for the same reasons as claim 2.

tt) Claim 23: Apparatus according to claim 21, wherein the main module comprises a switch, which is coupled to connect the traces to a network communication trunk, and wherein the system control processor is operative to configure switch to connect at least one of the lines of the first subsidiary module to at least one of the lines of the second subsidiary module during the test.

254. In my opinion, Cook in view of Lewis discloses claim 23 for the same reasons as claim 11.

uu) Claim 24: Apparatus according to claim 23, wherein the system control processor is operative to test one or more of the traces connected to the second subsidiary module while at least some of the traces that are not under test continue to be used for carrying the data from the subsidiary modules to the network communication trunk.

255. In my opinion, Cook in view of Lewis discloses claim 24 for the same reasons as claim 12.

vv) Claim 25: Apparatus according to claim 21, wherein the traffic comprises communication traffic, and wherein the first and second formats are determined respectively by different first and second communication protocols.

256. In my opinion, Cook in view of Lewis discloses claim 25 for the same reasons as claim 13.

ww) Claim 26: Apparatus according to claim 25, wherein one of the first and second protocols is a time domain multiplexing (TDM) protocol, while the other of the first and second protocols is a packet data protocol.

257. In my opinion, Cook in view of Lewis discloses claim 26 for the same reasons as claim 14.

F. Ground 4

258. To the extent claims 3, 6, 8, 13, 14, 17, 21, 25, and 26 are not rendered obvious by Cook and Lewis, it would have been obvious to combine Cook and Lewis with Sarkinen.

a) Claim 6

259. To the extent that claim 6 is not rendered obvious by Cook and Lewis, it is my opinion that it is rendered obvious by Cook, Lewis, and Sarkinen.

Sarkinen discloses:

> Network line interface circuitry and switch fabric circuitry is located on one or more printed circuit boards (PCB). For example, the network line interface circuitry may be located on one or more line cards, and the switch fabric circuitry may be located on one or more switch cards. A fabric interface circuit which interfaces the network line interface circuitry to the switch fabric circuitry, is separately located on a fabric interface board that is distinct and isolated from the PCBs associated with the network line interface and switch fabric circuits.

Ex. 1011, ¶13. A POSITA would recognize that the backplane in the '369 patent was a (or, the same as the) printed circuit board, as the line cards and fabric cards were the same as the subsidiary modules and the fabric interface board was the main

module. Sarkinen also makes clear that the traffic transmitted over the line and fabric cards is communication traffic for routing over the network when it states that:

> The PCBS are connected to the fabric interface board, and information is communicated between the network line interface circuitry and the switch fabric circuitry via the distinct fabric interface board.

Ex. 1011, ¶13.

260. A POSITA would have been motivated to combine Cook, Lewis and Sarkinen because it would be essential to test the connections between the line cards when idle. As stated above, testing the connections when idle would be optimal as the test would detect hidden failures and prevent any interference with the normal traffic. Finally, as seen in Fig. 4 below, it would be obvious to a POSITA that the fabric interface would act as a switch between the two line cards and be able to set up paths between them.

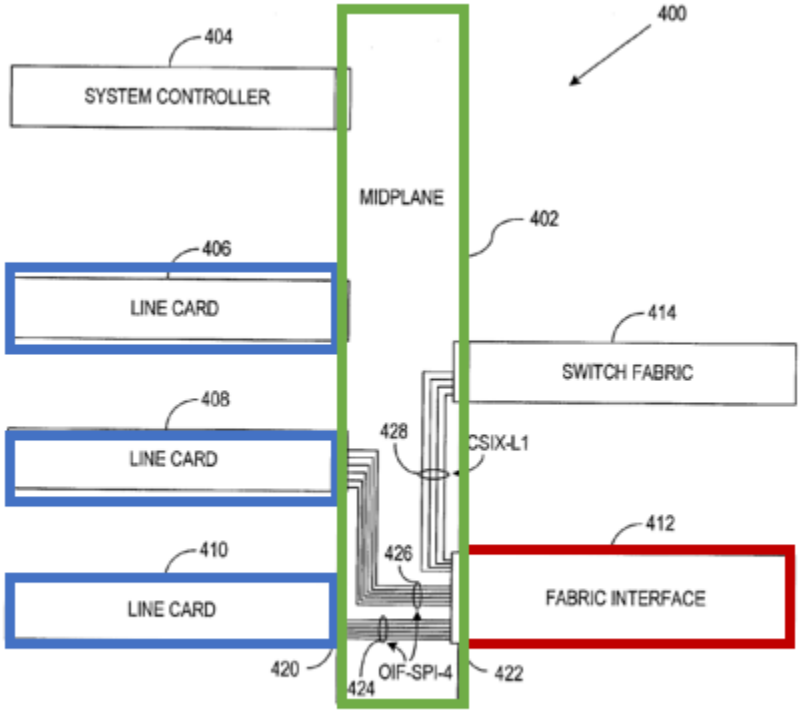


FIG. 4

Ex. 1011, Fig. 4.

261. Therefore, it is my opinion that Cook in view of Lewis and Sarkinen discloses "wherein the switch is configured to connect the lines to a network communication trunk, and wherein the traffic comprises communication traffic."

b) Claims 3, 8, 13, 14, 17, 21, 25, and 26

262. To the extent that claims 3, 8, 13, 14, 17, 21, 25, and 26 are not rendered obvious by Cook and Lewis, it is my opinion that they are rendered obvious by Cook, Lewis and Sarkinen.

263. It would be obvious to a POSITA to combine Cook, Lewis and Sarkinen because Sarkinen utilizes a network switch with a backplane, such as that discussed

in Cook. Sarkinen also states that "[t]he isolated fabric interface circuit board 316 is designed as an intelligent interface to manage various types of switch fabrics, line cards, protocols, etc." Ex. 1011, ¶58. A POSITA would know that the various line cards in the network may support different protocols and formats, which are set by a standard organization. A POSITA would also know that the second subsidiary module would have had to have chosen a data format to communicate a test message and it would have been obvious to choose one of the data formats already in use by the line card. *Id.*

264. Claims 13 and 25 also recite that different formats are associated with different protocols. As stated above, Sarkinen states that "[t]he isolated fabric interface circuit board 316 is designed as an intelligent interface to manage various types of switch fabrics, line cards, protocols, etc." Ex. 1011, ¶58. In addition, it would have been obvious to a POSITA that different formats of data traffic received by the line cards are associated with different modules.

265. Claims 14 and 26 recite that one protocol is a TDM protocol and the other is a packet data protocol. It would have been obvious to a POSITA that the protocols could be TDM and/or packet data protocols as they are common data protocols. TDM is a common audio-related protocol, while packet data protocol is a common internet and IP protocol. It would also be obvious to a POSITA that the two protocols could be utilized in the same system.

266. Therefore, it is my opinion that Cook in view of Lewis and Sarkinen renders obvious claims 3, 8, 13, 14, 17, 21, 25, and 26.

VIII. SECONDARY CONSIDERATIONS

267. I am not aware of any evidence of secondary considerations of nonobviousness relied upon by Patent Owner. To the extent Patent Owner is permitted to provide any evidence of secondary considerations to rebut my opinions expressed herein, I reserve the right to respond by supplementing and/or amending this declaration or submitting a reply declaration to consider the alleged secondary considerations of nonobviousness.

IX. RIGHT TO SUPPLEMENT

268. I reserve the right to supplement this declaration, if appropriate, should additional information come to light that is relevant to my opinions in this declaration. I also reserve the right to consider and comment on additional evidence, e.g., objective evidence of nonobviousness, that may be presented by Patent Owner or its experts.

269. At any trial or hearing at which I may testify in this matter, I may provide demonstrative aids, such as computer animations, excerpts, and figures from relevant exhibits and prior art references, and physical examples to assist in explaining the subject matter in my report.

270. I will continue my study and evaluation of relevant prior art as these proceedings continue, at least up until the end of the period prescribed by the relevant rules and regulations. In the event further issues arise that concern the subject matter in my declaration, I expressly reserve the right to supplement, modify, or amend my opinions as stated in this declaration as well as the bases supporting my opinions. I specifically reserve the right to supplement and/or amend this declaration at such time that the Board defines the disputed terms in the Challenged Claims, particularly if the Board adopts alternate instructions not advanced by Petitioners. I further reserve the right to supplement and/or amend this declaration to submit a reply declaration based on any information or contentions expressed by Patent Owner or its experts attempting to rebut my opinions in this declaration. In addition, I reserve the right to use demonstratives or other exhibits at trial in support of my opinions in any of my expert declarations and/or supplements thereto.

X. CONCLUSION

271. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like are so made punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the Petition for *inter partes* review.

For the reasons set forth above, it is my opinion that the Challenged Claims of the '369 patent are invalid.

Executed on January 18, 2023
San Jose, California

By: Nader F. Mir
Dr. Nader F. Mir