

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Chongqing HKC Optoelectronics Technology Co., Ltd.,

Petitioner

v.

138 East LCD Advancements Limited,

Patent Owner

Patent No. 7,116,390
Case No. IPR2023-00475

PETITION FOR *INTER PARTES* REVIEW

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LIST OF EXHIBITS

Exhibit	Description
Ex. 1001	U.S. Patent No. 7,116,390, issued to <i>Murade</i> , filed May 25, 2004, issued Oct. 3, 2006 (“’390 patent”)
Ex. 1002	Declaration of Carl Sechen, Ph.D. (“Sechen”)
Ex. 1003	Curriculum Vitae of Carl Sechen, Ph.D.
Ex. 1004	Excerpts of the Prosecution History for U.S. Patent No. 7,116,390 (“’390 FW”)
Ex. 1005	JP2002049052A to <i>Muraide</i> , published February 15, 2002 (“ <i>Muraide</i> ”)
Ex. 1006	JP2002196311A to <i>Sunao</i> , filed December 22, 2000, published July 12, 2002 (“ <i>Sunao</i> ”)
Ex. 1007	U.S. Patent No. 6,862,071 to <i>Fujikawa</i> , filed January 27, 2003, published September 18, 2003 as US20030174271A1, March 1, 2005 (“ <i>Fujikawa</i> ”)
Ex. 1008	U.S. Patent No. 6,262,702 to <i>Murade</i> , filed October 23, 1998, issued July 17, 2001 (“ <i>Murade II</i> ”)
Ex. 1009	U.S. Pub. Patent Application No. 20030063248A to <i>Komeno</i> , filed September 6, 2002, published April 3, 2003 (“ <i>Komeno</i> ”)
Ex. 1010	U.S. Patent No. 6,433,767 to <i>Murade</i> , filed February 1, 1999, issued August 13, 2002 (“ <i>Murade III</i> ”)
Ex. 1011	Declaration of Wenye Tan (“Tan”)

I. PRELIMINARY STATEMENT

Petitioner requests IPR and cancellation of claims 1-13 of the '390 patent (Ex. 1001).

The '390 patent describes a standard electro-optical device, such as an LCD, in which driving circuits are mounted in a peripheral region on a substrate. Sechen, ¶¶17-19. The patent describes a particular arrangement of the peripheral driving circuits and standard wiring lines used in such devices which purportedly reduces the mutual interference among the lines and thereby allows the device to be smaller in size. Sechen, ¶¶19-29.

The patent claims recite the basic, well-known configuration of an electro-optical device, such as an LCD, that has a plurality of pixel portions provided in an image display region on an element substrate. The claimed device includes a region peripheral to the image display region that has a plurality of external circuit connection terminals, which are coupled by a plurality of main wiring lines to the peripheral driving circuits. In addition, the claimed device has a counter electrode provided in a peripheral region on a counter substrate that is arranged to face the element substrate, and a counter electrode potential line that supplies counter electrode potential to the counter electrode. The device must also include upper and lower conduction terminals in the peripheral region on the element substrate that are connected to the counter electrode potential line. The plurality of main

wiring lines must be made of the same conductive film and be planarly laid out so as not to intersect each other in the peripheral region. Finally, the counter electrode potential line must be closest to the edges of the element substrate, among the plurality of main wiring lines. Sechen, ¶29.

While lengthy, the '390 patent's claimed structures were well-known in the prior art. Tellingly, to overcome prior art rejections during examination, claim 1 was amended to add "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Sechen, ¶¶30-37. However, this limitation not only was a common design choice, but also was well-known in the prior art. For example, *Sunao*, *Fujikawa* and *Komeno* all disclose a counter electrode potential line being closest to the edges of an element substrate.

For the reasons set forth below, the Board should institute IPR and cancel claims 1-13 of the '390 patent under pre-AIA 35 U.S.C. §102 and/or §103.

II. THE '390 PATENT

A. Overview

The '390 patent relates an electro-optical device, such as a driving circuit built-in liquid crystal device, obtained by mounting peripheral driving circuits on an element substrate. Sechen, ¶19; '390 patent, col. 1:8-10. The '390 patent itself describes prior art devices as having a plurality of pixel portions for displaying images arranged in a matrix in an image display region. The pixels are driven and

controlled by pixel electrodes and thin film transistors (TFT), which are arranged within the pixel portions and wiring lines, such as scanning lines, data lines, and capacitance lines. The patent recognizes the prior art describes scanning line driving circuits and a data line driving circuit for driving the scanning lines are mounted in a peripheral region on the same element substrate. Therefore, in general, various wiring lines, such as power source signal lines, clock signal lines, image signal lines, and control signal lines are planarly laid out in the peripheral region, which connect a plurality of external circuit connection terminals arranged along one side of the element substrate to the peripheral driving circuits. Sechen, ¶19; '390 patent, col. 1:14-32.

The '390 patent describes a particular arrangement of these well-known components that supposedly reduces the interference between the components so that a smaller device can be made. Sechen, ¶20; '390 patent, col. 1:33-40. As shown in Figure 1 of the '390 patent (below), the patent describes a TFT array substrate 10, and a counter electrode potential line LCCOM, which is one of the main wiring lines 108. Sechen, ¶¶20-24; '390 patent, col. 12:61-13:5.

Fig. 1

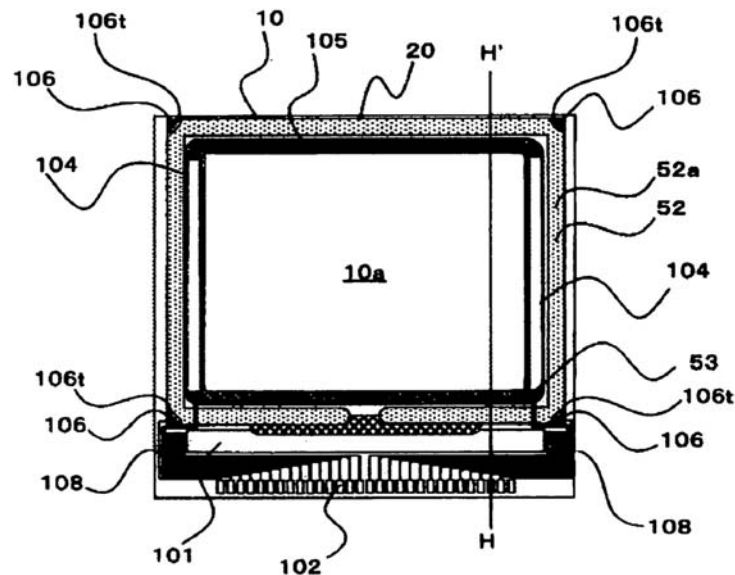
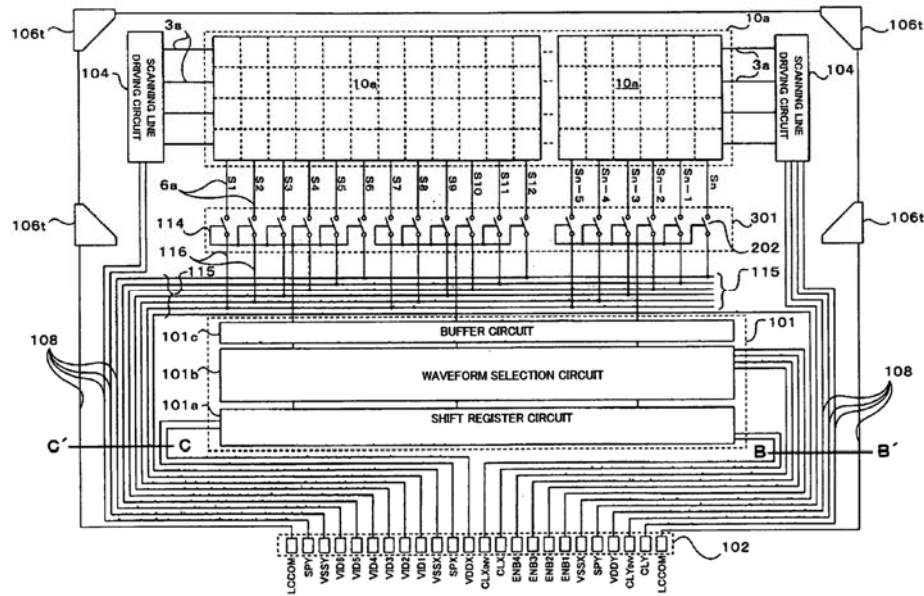


Figure 4 of the '390 patent (below), further illustrates the arrangement of the counter electrode potential lines LCCOM in relation to the scanning line driving circuits 104. As shown, the scanning line driving circuits 104 are arranged to be closer to the center of the TFT array substrate 10 than the counter electrode potential lines LCCOM provided along the edges of the TFT array substrate 10. Counter electrode potential line LCCOM passes through the four corners of the TFT array substrate 10 while being connected to the upper and lower conduction terminals 106t and surrounds the image display region 10a and various driving circuits. Sechen, ¶¶25-27; '390 patent, col. 13:6-19; Figs. 1, 4.



At the bottom of the figure, the outside most line is marked “LCCOM,” which is depicted as running outside of the other lines and connecting to the conduction terminals 106t. Sechen, ¶¶25-27.

B. Prosecution History

During examination, the pending claims were rejected over *Muraide* or *Muraide* in combination with *Yamazaki* (U.S Patent No. 6,011,607). Sechen, ¶¶30-34; '390 FW-0110. For example, in relation to original claim 1, the examiner found:

Muraide discloses an electro-optical device, comprising: a plurality of pixel portions provided in an image display region (10a) on an element substrate (10); in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals (102), a plurality of main wiring lines (400) each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits (101 or 104) coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on

electric signals supplied from the external circuit connection terminals through the main wiring lines, the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region, [see figs. 4 & 11].

'390 FW-0107-08; see Sechen, ¶¶32-34. In addition, in regard to then pending claims 4 and 5, the examiner found:

Muraide discloses the electro-optical device according to claim 1, further comprising a counter electrode provided in the peripheral region on a counter substrate (20) that is arranged to face the element substrate (10); and upper and lower conduction terminals (106) that are provide in the peripheral region on the element substrate, in order to connect a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is a at least one of the plurality of main wiring lines, [see figs. 3 & 4].

'390 FW-0110-11. In other words, *Muraide* disclosed essentially all limitations of the original claims. The examiner noted that: "Muraide lacks disclosure of the counter electrode potential line to the plurality of main wiring lines being positioned near edges of the element substrate in the peripheral region, and the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower connection terminals and the counter electrode potential line in the peripheral region." '390 FW-0110; see Sechen, ¶¶32-34.

In response, applicant amended independent claim 1 to add, *inter alia*, "the counter electrode potential line being closest to edges of the element substrate,

among the plurality of main wiring lines.” ’390 FW-0039; Sechen, ¶¶35-36. Based on this amendment, the examiner allowed the claims. ’390 FW-0006-0008.

III. STATEMENT OF PRECISE RELIEF REQUESTED

The challenged claims are unpatentable under Pre-AIA 35 U.S.C. §§102 or 103, and should be cancelled in view of the following prior art based on the grounds articulated herein.

Prior Art References	
Ref. 1	<i>Muraide</i> (Ex. 1005): filed on August 3, 2000, published on February 15, 2002 as JP2002049052A, and issued on December 13, 2006 as JP3858572B2; prior art under at least pre-AIA 35 U.S.C. §102(a) or (b).
Ref. 2	<i>Sunao</i> (Ex. 1006): filed on December 22, 2000, and published on July 12, 2002 as JP2002196311A; prior art under at least pre-AIA 35 U.S.C. §102(a) or (b).
Ref. 3	<i>Fujikawa</i> (Ex. 1007): filed on January 27, 2003, published on September 18, 2003 as US20030174271A1, and issued as U.S. Patent No. 6,862,071 on March 1, 2005; prior art under at least pre-AIA 35 U.S.C. §102(a) or (e).
Ref. 4	<i>Murade II</i> (Ex. 1008): filed on October 23, 1998, and issued as U.S. Patent No. 6,262,702 on July 17, 2001; prior art under at least pre-AIA 35 U.S.C. §102(a) or (b).
Ref. 5	<i>Komeno</i> (Ex. 1009): filed on Sept. 6, 2002, published as U.S. Pub. Patent Application No. 20030063248A on April 3, 2003; prior art under at least pre-AIA 35 U.S.C. §102(a) or (b).
Ref. 6	<i>Murade III</i> (Ex. 1010): filed on February 1, 1999, and issued as U.S. Patent No. 6,433,767 on August 13, 2002; prior art under at least pre-AIA 35 U.S.C. §102(a) or (b).

Specific Grounds	
Ground 1	<i>Muraide</i> in Combination with <i>Sunao</i> or <i>Komeno</i> Renders Obvious Claims 1-11 and 13.
Ground 2	<i>Muraide</i> in Combination with <i>Sunao</i> or <i>Komeno</i> and in Further Combination with <i>Murade III</i> Renders Obvious Claims 2-3 and 12.
Ground 3	<i>Fujikawa</i> Anticipates Claims 1-5, 7-8, 11 and 13.
Ground 4	<i>Murade II</i> in Combination with <i>Sunao</i> or <i>Komeno</i> Renders Obvious Claims 1, 4-11 and 13.
Ground 5	<i>Murade II</i> in Combination with <i>Sunao</i> or <i>Komeno</i> and in Further Combination with <i>Murade III</i> Renders Obvious Claims 2-3 and 12.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’390 patent would have either a bachelor’s degree in electrical or computer engineering with three years of experience in the field of display technology or a master’s degree with one year of experience in the field of display technology. Sechen, ¶¶38-41.

V. CLAIM CONSTRUCTION

In general, the claim terms should be given their plain and ordinary meaning. *Riverwood Int’l. Corp. v. R.A. Jones & Co.*, 324 F.3d 1346, 1357 (Fed.

Cir. 2003) (holding there is a heavy presumption that terms have the ordinary meaning that would be attributed to it by persons skilled in the relevant art).

In the related litigation, the parties have not exchanged proposed constructions for the terms yet. As such, Petitioner does not know what, if any, particular constructions Patent Owner may propose for any terms. Nonetheless, Petitioner currently contends that the Board need not provide a specific construction for any particular term as the prior art renders the claims unpatentable under any reasonable interpretation of the terms. Sechen, ¶¶42-43.

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Overview of the Prior Art

1. *Muraide*

Muraide describes an electro-optical device, such as an LCD, in which “data lines are driven in accordance with image signals, clock signals, and the like by peripheral circuits such as data line driving circuits and sampling circuits provided in peripheral regions on a TFT array substrate.” Sechen, ¶44; *Muraide*, ¶[0001]. *Muraide* discloses a device with a pixel electrode (9a), a TFT(thin film transistor 30) connected to the pixel electrode (9a) and a capacitive line (300) on a picture display region of a TFT array substrate (10) and is further provided with a data line (6a) and a scanning line (3a) connected to the TFT. Sechen, ¶44; *Muraide*, abstract. In the peripheral region, a peripheral circuit including a circuit related to data line driving, a signal line (400) connected to the peripheral circuit and made of

a same film as the capacitive line, and a shield (401a) electrically screening the signal line (400) from at least one direction and formed from a same film as the data line are provided. Sechen, ¶44; *Muraide*, abstract.

Notably, the figures of the '390 patent and *Muraide* are almost identical in many instances, and as such clearly disclose virtually the same electro-optical device. Sechen, ¶45 (comparing '390 Figs. 1, 2, 3, 6, 7, & 4 with *Muraide* Figs. 11, 12, 1, 2, 3, & 4).

2. Sunao

Sunao discloses a liquid crystal display device having a structure in which a liquid crystal layer is sandwiched between a matrix array substrate 2 and a counter substrate 3. A counter electrode 7 is formed on a whole surface of the counter substrate 3 and a metal cover frame 6 is arranged at an outer periphery of the liquid crystal display device. Sechen, ¶46; *Sunao*, abstract.

3. Fujikawa

Fujikawa discloses an electrooptic device in which a region that does not directly contribute to the display can be narrowed by improving the layout of peripheral circuits. Sechen, ¶47; *Fujikawa*, abstract. *Fujikawa* discloses an active matrix liquid crystal device using a thin-film transistor (TFT) as a pixel switching element, and a TFT array substrate 10 having pixel electrodes and pixel-switching TFTs formed on a transparent substrate. *Fujikawa* discloses a counter substrate 20

having counter electrodes formed on a transparent substrate that are bonded with a sealing material 107 with a predetermined space therebetween, and liquid crystal serving as an electrooptic substance being held between the substrates. Sechen, ¶47; *Fujikawa*, ¶¶[0004], [0046].

4. *Murade II*

Murade II discloses a liquid crystal apparatus, which includes a liquid crystal layer disposed between two substrates, pixel electrodes formed in a matrix fashion on a substrate, and TFTs serving for switching and controlling the pixel electrodes for suppressing the intrusion of high-frequency clock noise into an image signal. Image signal lines extend on the substrate at both sides of a data line driving circuit. The image signal lines are electrically shielded from clock signal lines, for example, by shielding lines formed on the substrate, and maintained at a constant voltage. Sechen, ¶48; *Murade II*, abstract.

5. *Komeno*

Komeno discloses a liquid crystal display device referred to as a TN type, in which a display region is formed by sealing liquid crystal in a gap defined by laminating a first substrate and a second substrate which constitute a pair of substrates. Sechen, ¶49; *Komeno*, ¶[0004]. *Komeno* discloses that on the display region of the first substrate is a matrix consisting of a large number of data lines which are crossed at a right angle by scanning lines, and a pixel is formed in a

region surrounded by a pair of data lines and a pair of scanning lines. Sechen, ¶49; *Komeno*, ¶[0004]. *Komeno* further discloses a second substrate that includes counter electrodes which face opposite the pixel electrodes and are used to apply an electric field to the liquid crystal of the pixel. Sechen, ¶49; *Komeno*, ¶[0005]. *Komeno* further discloses that each pixel is formed of the liquid crystal which is sandwiched between the pixel electrode provided to the first substrate and the counter electrode provided to the second substrate. *Id.*

6. *Murade III*

Murade III discloses an electro-optical apparatus, such as a liquid crystal apparatus, that has a built-in-peripheral circuit in which the resistance of input/output wirings in the peripheral circuit is reduced by effectively using thin films forming pixels. The liquid crystal apparatus includes a liquid crystal layer disposed between a pair of substrates and pixel electrodes formed in a matrix fashion on a TFT array substrate. Sechen, ¶50; *Murade III* (abstract). *Murade III* discloses a “conventional liquid crystal apparatus having built-in peripheral circuits, peripheral circuits such as a data line driving circuit, a scanning line driving circuit, and a sampling circuit are formed on a TFT array substrate, which is one of two substrates between which a liquid crystal is disposed.” Sechen, ¶50; *Murade III*, col. 1:21-26.

B. Ground 1: *Muraide* in Combination with *Sunao* or *Komeno* Renders Obvious Claims 1-11 and 13.

As explained in the Prosecution History Section, *Muraide* was cited by the Patent Office during prosecution as a §102 reference, but the combination of *Muraide* with *Sunao* or *Komeno* was never applied during prosecution.

During prosecution, to overcome the *Muraide* reference, the applicant amended independent claim 1 to add, *inter alia*, “the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.” ’390 FW-0039. However, this added limitation merely changes the location of “the counter electrode potential line”, which is an obvious matter of design choice. *In re Kuhle*, 526 F.2d 553, 188 (CCPA 1975) (particular placement of a contact in a conductivity measuring device was an obvious matter of design choice).

Moreover, as illustrated below, multiple prior art references teach this added limitation.

1. Claim 1

An electro-optical device, comprising:

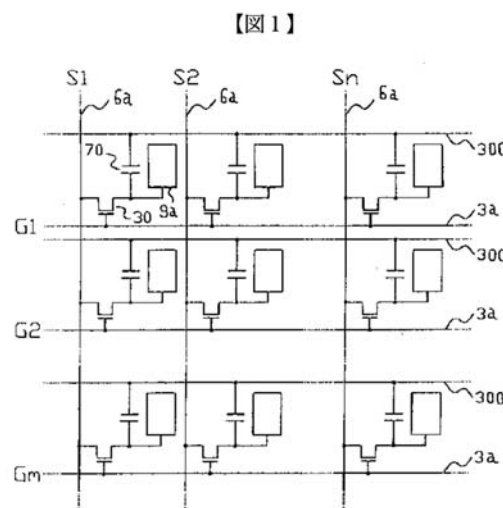
To the extent the preamble is limiting, *Muraide* discloses it. Sechen, ¶¶51-52.

Muraide specifically identifies its invention as relating to “electro-optical devices such as liquid crystal devices.” Sechen, ¶¶51-52; *Muraide*, ¶[0001].

**a plurality of pixel portions provided in an image display
region on an element substrate:**

Muraide discloses this limitation. Sechen, ¶¶53-55.

Muraide describes well-known LCD displays that consist of pixel portions on an element substrate as shown in Figure 1 of *Muraide* (shown below). Sechen, ¶¶53-55.



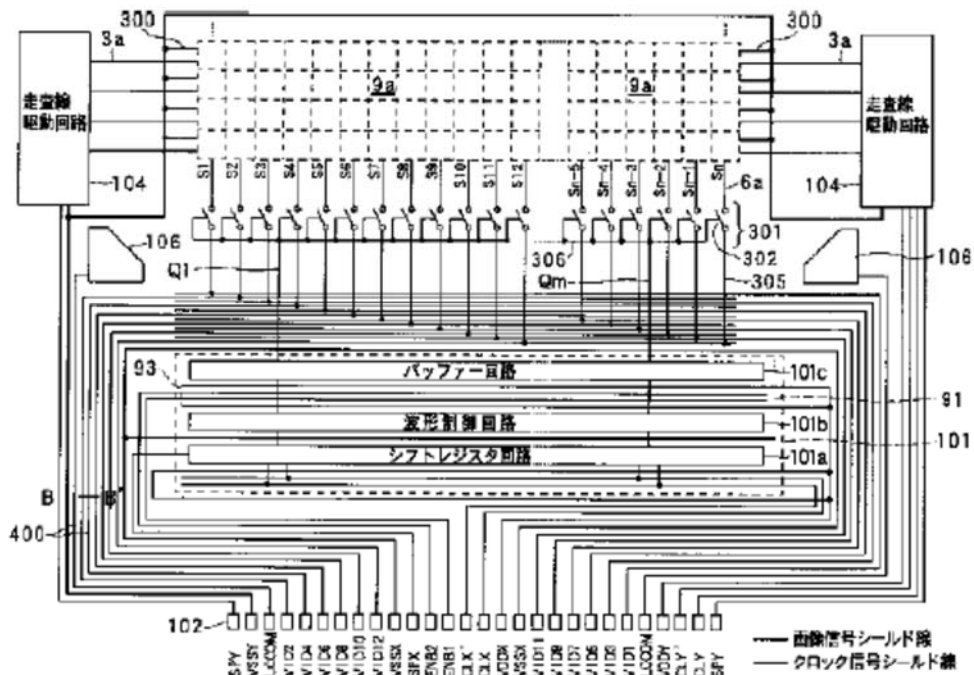
Muraide discloses pixel electrodes 9a, and TFTs 30 for controlling switching of the pixel electrodes 9a, are formed in a matrix that corresponds to an image display region on an element substrate of the electro-optical device. Sechen, ¶¶53-55; *Muraide*, ¶[0051], Figs. 1, 4.

in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

Muraide discloses this limitation. Sechen, ¶¶56-59.

As shown in Figure 4 (below), *Muraide* describes an element substrate with an image display region and a peripheral region thereto. *Muraide* discloses terminals 102 (along the bottom edge of the substrate of Figure 4), which are a plurality of external connection terminals. Figure 4 shows wiring lines coupled to the external connection terminals 102 at one end and coupled to peripheral circuits, including data line driving circuit 101, and scanning line driving circuit 104, at the other. *Muraide* teaches that the peripheral driving circuits drive the pixel portions of the image display region based on electric signals supplied from the external circuit connection terminals. Sechen, ¶¶56-59; *Muraide*, ¶¶[0001], [0078-80], Fig. 4.

【图 4】



a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

Muraide discloses this limitation. Sechen, ¶¶60-62.

Muraide describes its device as including “a counter electrode facing the plurality of pixel electrodes is ... on a counter substrate facing the substrate with an electro-optical material provided therebetween.” Sechen, ¶¶60-62; *Muraide*, ¶[0041]. Thus, *Muraide* discloses a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate.

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

Muraide discloses this limitation. Sechen, ¶¶63-65.

Muraide describes that a constant potential source may be a constant potential supplied to the counter electrode 21 of the counter substrate 20. Sechen, ¶¶63-65; *Muraide*, ¶[0061]. For example, as shown in Figure 4 of *Muraide*, vertical conductive terminals 106 are provided for electrically conducting the counter electrode 21 on the counter substrate 20 side.” Sechen, ¶¶63-65; *Muraide*, ¶[0085].

Muraide describes vertical conductive terminals 106 that electrically couple the TFT array substrate 1 and the counter electrode 21 on the counter substrate 20. *Muraide*, Figs. 3, 4. *Muraide* discloses a counter electrode potential line, wiring 400 (LCCOM), that supplies potential from the external input terminal 102 to the vertical conduction terminal 106 and then to the counter electrode 21 on the counter substrate 20. Sechen, ¶¶63-65; *Muraide*, ¶[0085]; Fig. 4.

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

Muraide discloses this limitation. Sechen, ¶¶66-67.

In *Muraide*, the vertical conduction terminals 106 are provided at the four corners of the image display area on the array substrate 1, and the vertical

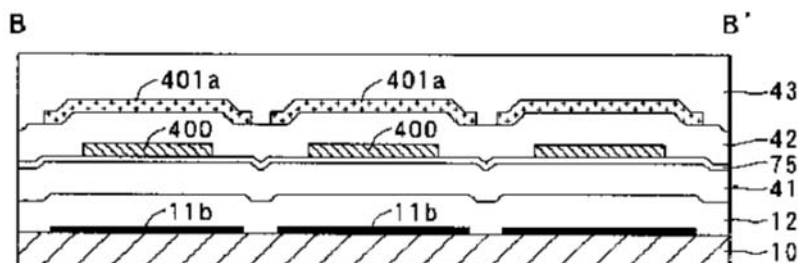
conduction terminal 106 is supplied via the external input terminal 102 and the wiring 400 (LCCOM). Sechen, ¶¶66-67; *Muraide*, ¶[0085], Fig. 4.

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

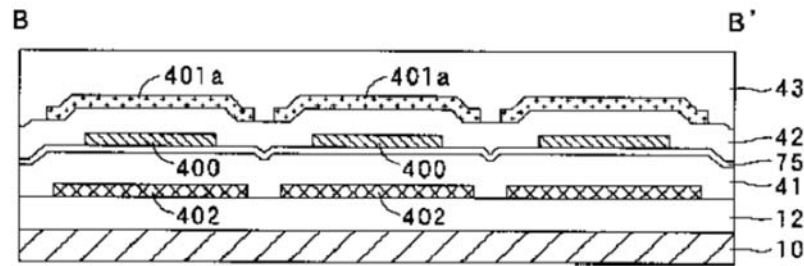
Muraide disclose this limitation. Sechen, ¶¶68-69.

Muraide discloses main wiring lines, such as “the wirings 400 (VID1) to 400 (VID12)” that are image signal lines and made of the same conductive film as the capacitance lines 300 in the image display region. Sechen, ¶¶68-69; *Muraide*, ¶[0087]. *Muraide* teaches that the plurality of wiring lines are laid out in a zig-zag pattern so they do not intersect each other in the peripheral region. Sechen, ¶¶68-69; *Muraide*, Fig. 7, Fig. 8; Fig. 4 (above).

【図 7】



【図 8】



the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.

This limitation is obvious over *Muraide* because the location of the counter electrode potential line is a mere design choice. Sechen, ¶70. In *Muraide*, the counter electrode potential line, wiring 400 (LCCOM), that supplies potential from the external input terminal 102 to the vertical conduction terminal 106 is located nearer to the center of the substrate with respect to the scanning line drive circuit 104. The other design choice is to locate the counter electrode potential line nearer to the edge of the substrate with respect to the scanning line drive circuit. It is a simple choice without changing any property or characteristics of the wiring layout. Sechen, ¶70. Such change of location of a component is mere design choice and, thus, is obvious under §103. *In re Kuhle*, 526 F.2d 553, 188 (CCPA 1975) (particular placement of a contact in conductivity measuring device is an obvious matter of design choice).

In addition to being merely an obvious design choice, this limitation is also disclosed or taught by multiple prior art references.

For example, *Sunao* discloses this limitation. Sechen, ¶¶71-73, 77.

Sunao discloses an LCD device with a matrix array substrate 2. The array substrate 2 is arranged with a plurality of signal lines 12 arranged in parallel on a transparent insulating substrate 4, and a plurality of scanning lines 14 arranged in parallel to intersect the plurality of signal lines 12 at right angles. Sechen, ¶¶71-73; *Sunao*, ¶[0013]. *Sunao* further discloses a signal line driving circuit 13 that is electrically connected to one end of signal line 12 for applying a video signal to the signal line 12, and a scanning line driving circuit 15 that is electrically connected to one end of the scanning line 14 for applying a scanning signal to the scanning line 14. Sechen, ¶¶71-73; *Sunao*, ¶[0014].

Sunao discloses its device has a counter electrode potential line being closest to edges of the element substrate. Sechen, ¶¶71-73. In particular, *Sunao* describes conductive pads 28 and counter electrode potential wirings 27 (e.g., the counter electrode potential line) for applying a potential to the counter electrode 7 are provided in the peripheral portion of the display region 11 on an insulating substrate 4. Sechen, ¶¶71-73; *Sunao*, ¶[0016]; Fig. 3 (below).

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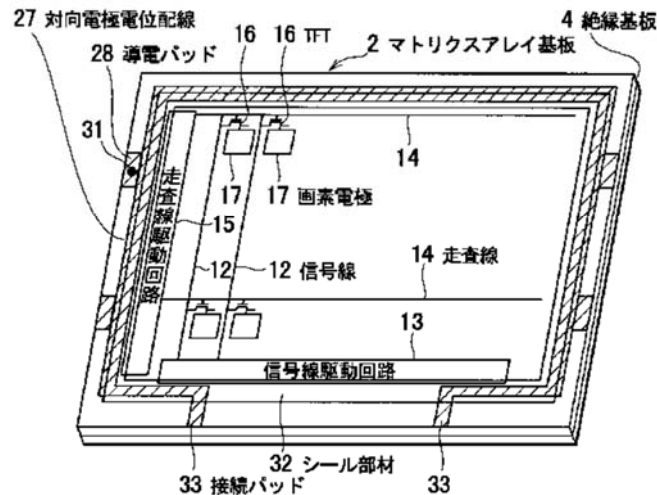


Figure 3 of *Sunao* teaches a counter electrode potential line 27 that is nearest to the edges of the element substrate of the main wiring lines. *Sunao* further discloses a “predetermined counter potential is supplied to the counter electrode potential wiring 27 from the outside from an external PCB, not shown, through the connection pad 33.” Sechen, ¶¶71-73; *Sunao*, ¶[0016].

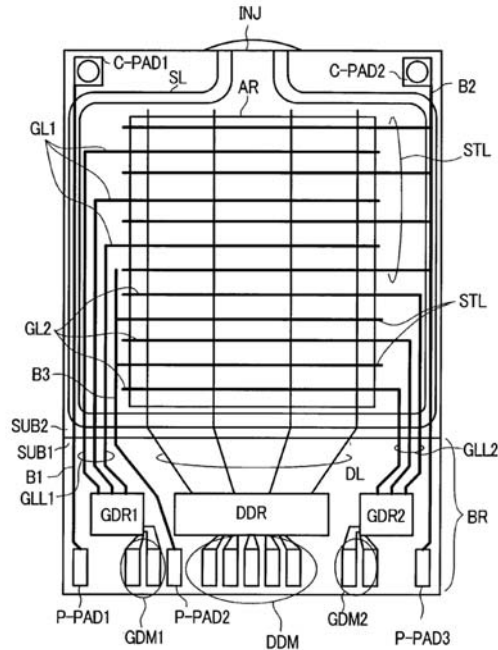
A POSITA would have found it obvious to combine *Muraide* and *Sunao*. Sechen, ¶¶74, 77. Specifically, a POSITA would have found it obvious to implement *Sunao*'s placement of the counter electrode potential line as closest to edges of the element substrate with *Muraide*'s display device. *Id.* A POSITA would have been motivated to combine *Sunao*'s placement with *Muraide*'s display device in order to further isolate the electrode potential line from the other wirings and the display reduce interference and potentially shrink the size of its device. *Id.* Further, as both *Muraide* and *Sunao* relate to displays, and specifically LCDs, a

POSITA would have found it straightforward to combine *Sunao*'s placement of the counter electrode potential line as closest to edges of the element substrate with *Muraide*'s display device, and the combination would have yielded predictable results. *Id.*

Alternatively, *Komeno* discloses this limitation. *Sechen*, ¶75, 77.

Komeno discloses a liquid crystal display device referred to as a TN type, in which a display region is formed by sealing liquid crystal in a gap defined by laminating a first substrate and a second substrate which constitute a pair of substrates. *Sechen*, ¶75; *Komeno*, ¶[0004]. In regard to the two substrates, *Komeno* describes how the second substrate (SUB 2) has counter electrodes that face opposite the pixel electrodes on the first substrate. *Komeno* discloses feeding pads P-PAD1, P-PAD3 which are formed on the driving circuit mounting region. The feeding pads are external terminals that provide electricity via lines B1, B2 to the counter electrode connection pads C-PAD1, C-PAD2. The counter electrode connections pads then supply power to the counter electrodes. *Sechen*, ¶75; *Komeno*, ¶[0108]. As shown in Figure 1 of *Komeno* (below), of the main wiring lines, wiring lines B1, B2 are located closest to the edges of the element substrate SUB1. *Sechen*, ¶75.

FIG. 1



A POSITA would have found it obvious to combine *Muraide* and *Komeno*. Sechen, ¶¶76-77. Specifically, a POSITA would have found it obvious to implement *Komeno*'s placement of the counter electrode potential line as closest to edges of the element substrate with *Muraide*'s display device. *Id.* A POSITA would have been motivated to combine *Komeno*'s placement of the counter electrode potential line with *Muraide*'s display device in order to further isolate the electrode potential line from the other wirings and the display area. *Id.* This combination would have allowed the device of *Muraide* to potentially further miniaturize. *Id.* Further, as both *Muraide* and *Komeno* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine

Komeno's teachings with *Muraide's* display device, and the combination would have yielded predictable results. *Id.*

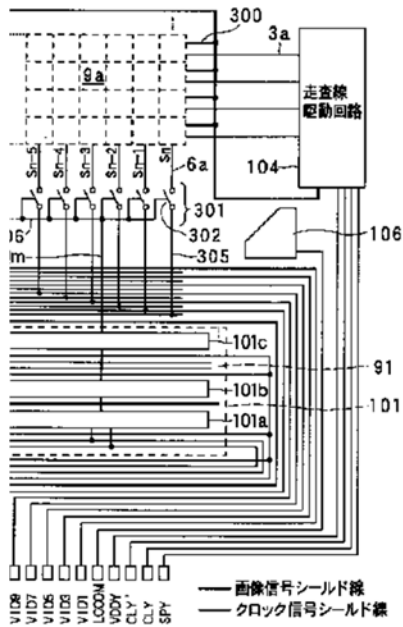
2. Claim 2

Claim 2 depends from claim 1 with the further limitation:

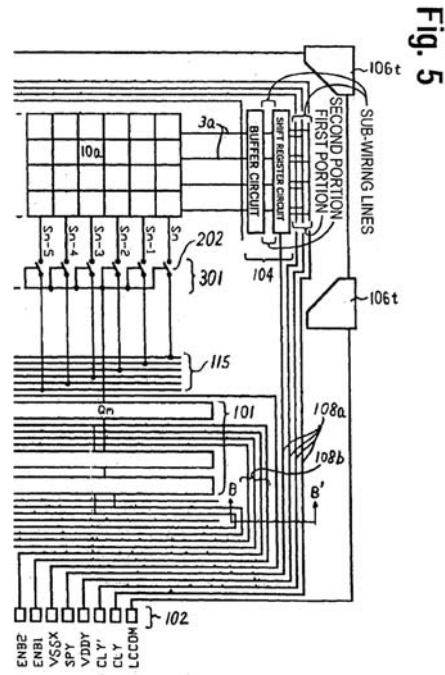
sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

Muraide discloses this limitation. Sechen, ¶¶78-80.

As shown below, the relevant portion of Figure 4 in *Muraide* (left side) is substantially the same as in Figure 5 of the '390 patent (right side). Interlayer conductive line routing is a common and necessary fabrication practice in making semiconductor structures, which is what essentially claimed in claim 2. Sechen, ¶¶78-80. The same structure in *Muraide* discloses or renders obvious the interlayer routing arrangements of claim 2. Sechen, ¶¶78-80.

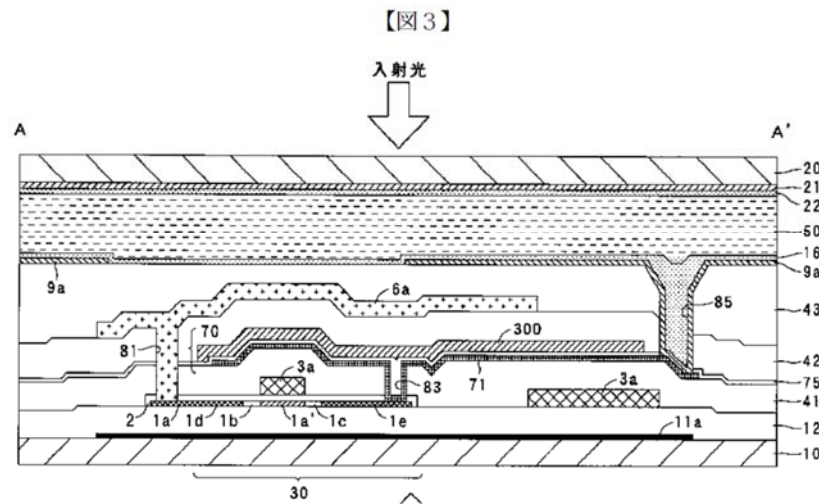


Muraide Fig. 4



'390 patent Fig. 5

Muraide also explicitly discloses this limitation. For example, Figure 4 of *Muraide* depicts sub-wiring lines where the first portions include at least lines 3a, and the second portions include at least the relay layer 71. As shown in part of Figure 4, in *Muraide*, the scanning line driving circuit 104 is in the peripheral region and intersects with certain main wiring lines, *e.g.*, SPY, CLY, CLY', VDDY. As shown in Figure 3 of *Muraide* below, lines 3a intersect with main wirings (which are made of the same conductive film as the capacitance line 300) via an insulating layer 41. Sechen, ¶¶78-80; *Muraide*, ¶[0088].



Muraide teaches that relay layer 71 and capacitance line 300 are formed on the first interlayer insulating film 41, *i.e.*, the relay layer 71 is in the same plane as the main wirings without intersection. Sechen, ¶¶78-80; *Muraide*, ¶[0071], Fig. 3.

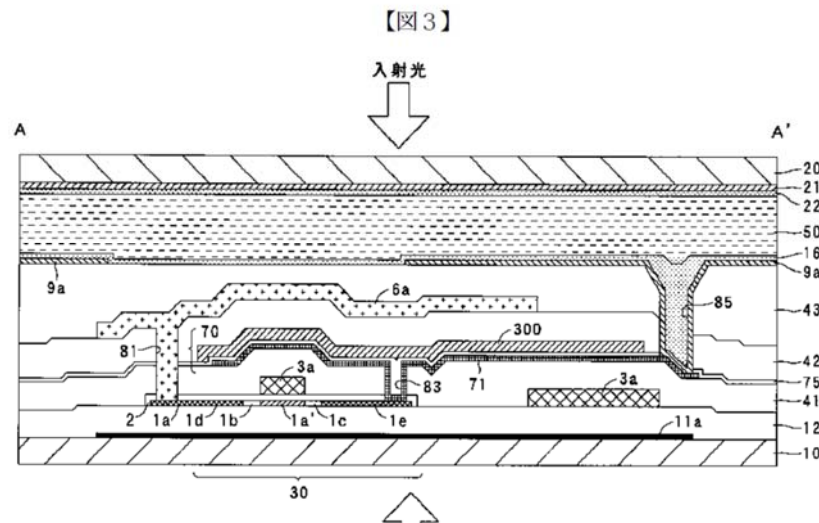
3. Claim 3

Claim 3 depends from claim 2 with the further limitation:

the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.

Muraide discloses this limitation. Sechen, ¶¶81-82.

Muraide describes that the relay layer 71 (the second portion) is electrically coupled to the semiconductor layer 1a through contact holes 83, and the scan lines 3a (the first portion) are the gate electrodes of the semiconductor layer 1a. Sechen, ¶¶81-82; *Muraide*, ¶[0069]-[0071], Fig. 3.



The contact holes are formed in the interlayer insulating (insulating layer 41). Sechen, ¶¶81-82.

4. Claim 4

Claim 4 depends from claim 1 with the further limitation:

the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.

Sunao discloses this limitation. Sechen, ¶¶83-85, 90.

Sunao discloses a scanning line driving circuit 15 that provides a scanning signal to the scanning line 14 as shown in Figure 3 of *Sunao* (below). Sechen, ¶¶83-85; *Sunao*, ¶[0014].

【図 3】

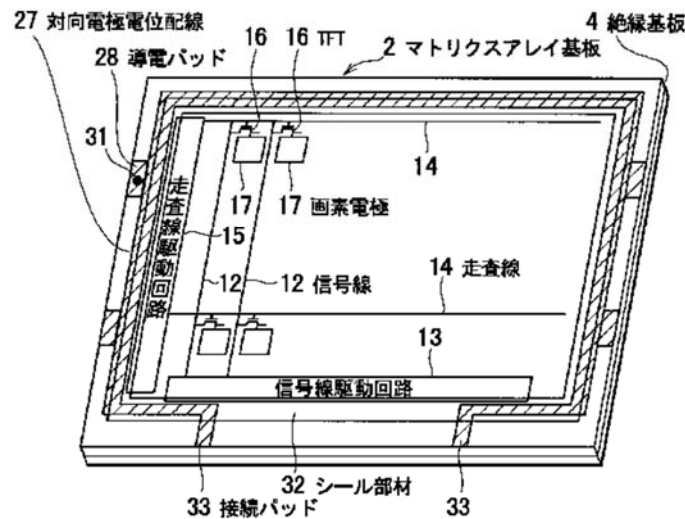


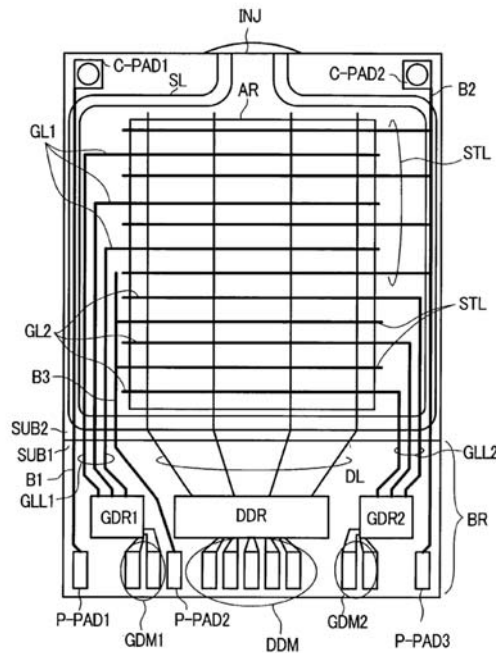
Figure 3 further shows conductive pads 28 and counter electrode potential wirings 27 that apply potential to the counter electrode 7 located in a peripheral portion of the image display region 11 on the element substrate 4. Electrode potential wiring 27 is connected via connection pad 33 to an external PCB. Sechen, ¶¶83-85; Sunao, ¶[0016]. Sunao further teaches peripheral driving circuits (“scanning line driving circuit 15”) being located nearer to the center of the element substrate than conductive pads 28 and counter electrode potential wirings 27. Sechen, ¶¶83-85.

For the reasons set forth in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Sunao*. Sechen, ¶¶86, 90.

Alternatively, *Komeno* discloses this limitation. Sechen, ¶¶87-88, 90. As shown in *Komeno* Figure 1, gate line driving circuits GDR1 and GDR2 are formed in the peripheral region BR, and feeding pads P-PAD1 and P-PAD3 are also

formed in the peripheral region BR. Further, counter electrodes are connected to the feeding pads P-PAD1, P-PAD3 formed on the driving circuit mounting region BR through counter electrode connection pads C-PAD1, C-PAD2 formed on corner portions of an upper side of the first substrate SUB1 and common lines B1, B2. Electricity is supplied through the feeding pads P-PAD1, P-PAD3. Sechen, ¶¶87-88; *Komeno*, ¶[0108]-[0110]; Fig. 1. Accordingly, with respect to the left/right side of the substrate, GDR1 is positioned nearer a center of the element substrate than (1) the conduction terminals P-PAD1/C-PAD1 and P-PAD3/C-PAD3, and (2) the counter electrode potential lines B1, B2. Sechen, ¶¶87-88; *Komeno*, ¶[0108]; Fig. 1.

FIG. 1



For the reasons set forth in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Komeno*. Sechen, ¶¶89-90.

5. Claim 5

Claim 5 depends from claim 4 with the further limitation of:

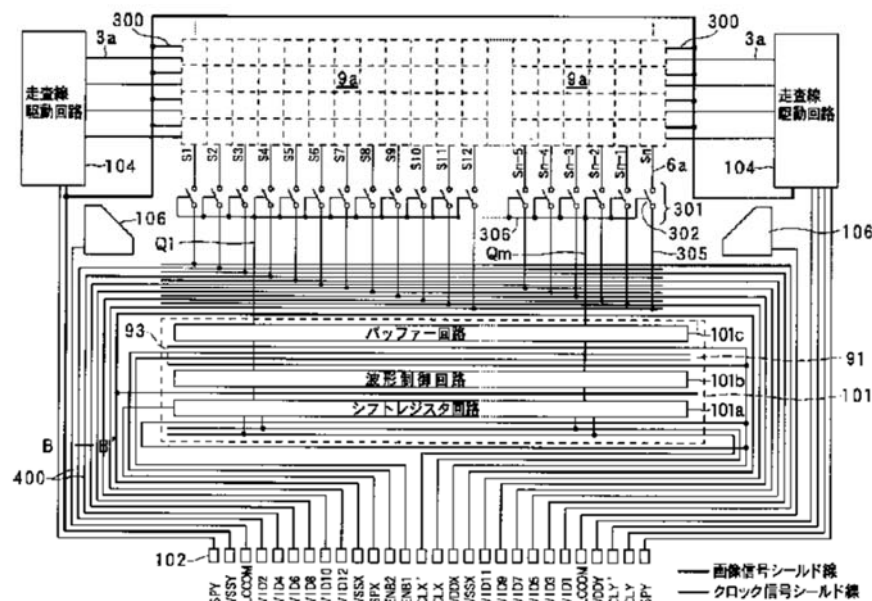
the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

Muraide discloses this limitation. Sechen, ¶¶91-94

Muraide describes a plurality of external connection terminals 102 along one side of an element substrate as shown in Figure 4 (below).

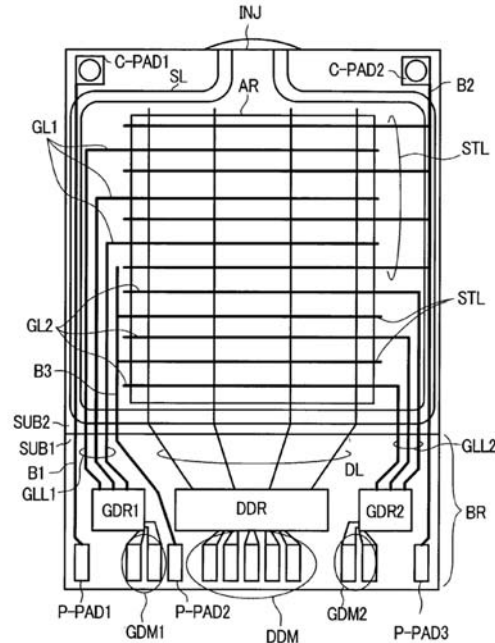
【図4】



Muraide describes an external connection terminal 102 that is connected to a counter electrode potential line (wiring 400 (LCCOM)), and is located near an end of the row of external connection terminal. Sechen, ¶91. In Figure 4, two connection terminals 102 are labelled LCCOM and both are located near the end of each side of the row of terminals 102 (third from the left side end and fourth from the right side end). Sechen, ¶91.

Alternatively, *Komeno* discloses this limitation. Sechen, ¶92. As shown in *Komeno* Figure 1 (below), a plurality of external connection terminals are arranged along the lower edge of the figure. Sechen, ¶92. *Komeno* teaches that counter electrodes are connected to the feeding pads P-PAD1, P-PAD3 formed on the driving circuit mounting region BR through counter electrode connection pads C-PAD1, C-PAD2 formed on corner portions of an upper side of the first substrate SUB1 and common lines B1, B2. Electricity is supplied through the feeding pads P-PAD1, P-PAD3. Sechen, ¶92; *Komeno*, ¶[0108]-[0110]; Fig. 1. Accordingly, *Komeno* teaches external circuit connection terminal P-PAD1 and P-PAD3, which are coupled to one end of the counter electrode potential line B1 and B2, that are near the end of an array of the plurality of external circuit connection terminals. In particular, they are located at the position closest to the left and right edges of the substrate as seen in Figure 1. Sechen, ¶92; *Komeno*, ¶[0108]; Fig. 1.

FIG. 1



For the reasons set forth in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Komeno*. Sechen, ¶¶93-94.

6. Claim 6

Claim 6 depends from claim 4 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

Muraide discloses this limitation. Sechen, ¶¶95-96.

Muraide discloses a clock signal (CLX) and an inverse clock signal (CLX'), which are part of the main wiring lines shown in Figure 4 above. *Muraide* discloses a counter electrode potential line (LCCOM). As shown in Figure 4,

Muriade discloses that the clock signals CLX and CLX' do not intersect with the potential line LCCOM. Sechen, ¶¶95-96.

7. Claim 7

Claim 7 depends from claim 1 with the further limitation:

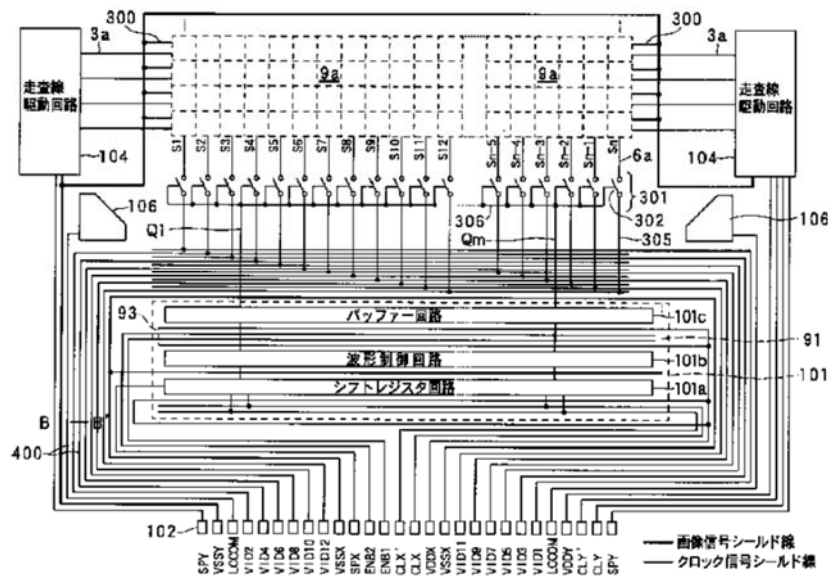
a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

Claim 7's requirement that "parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region" contradicts claim 1's requirement that "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Further, the '390 patent does not appear to disclose any such structure. Sechen, ¶97.

Nonetheless, to the extent claim 7 is determined not to be nonsensical, *Muraide* and *Sunao* teach and suggest this limitation. Sechen, ¶¶98-101.

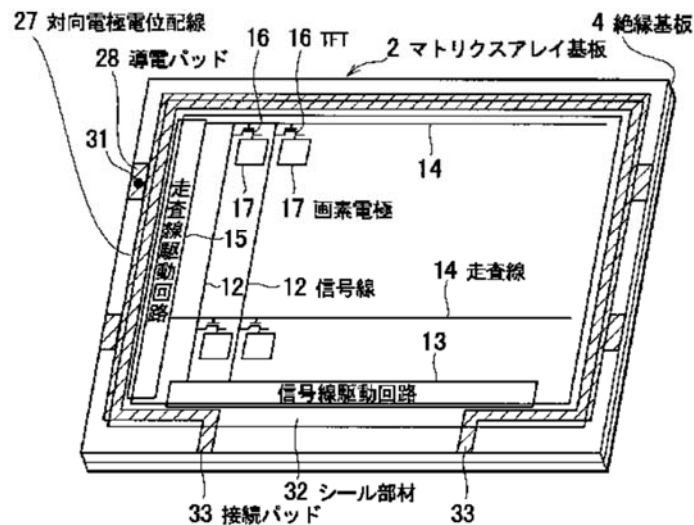
In *Muraide*, the scanning line drive circuits 104 are arranged nearer to the side edges of array substrate 1 than the conductive terminals 106 and counter electrode line LCCOM as seen in *Muraide* Figure 4 (below). Sechen, ¶¶98-101.

【図4】



Sunao Figure 3 teaches the scanning line driving circuit 15 is nearer to the center of the element substrate than the conductive pads 28. In addition, the signal line driving circuit 13 is nearer to the lower edge of the element substrate than the conductive pads 28. *Sechen*, ¶¶98-101.

【図3】



For the reasons set forth in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Sunao*. Sechen, ¶¶100-101.

8. Claim 8

Claim 8 depends from claim 7 with the further limitations of:

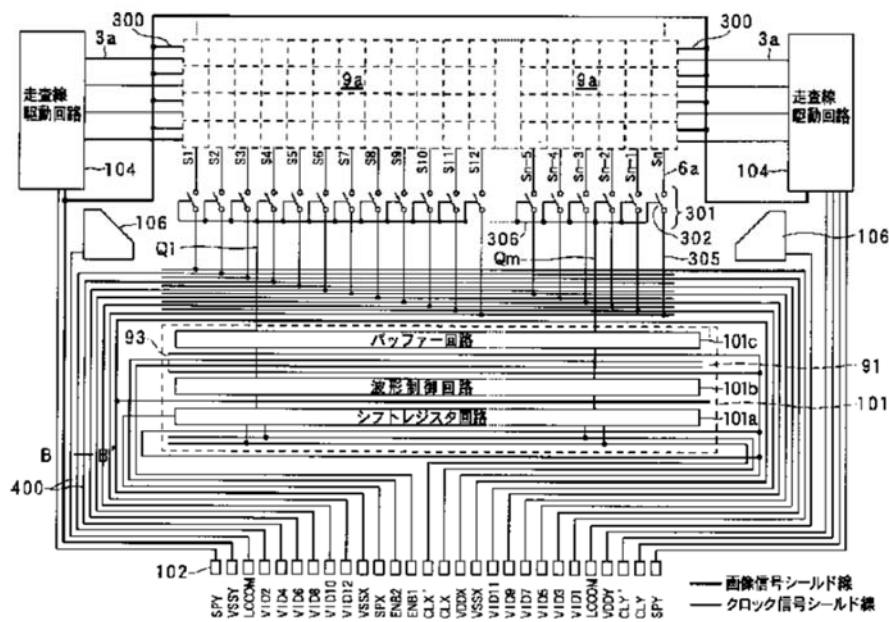
the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.

Muraide discloses this limitation. Sechen, ¶¶102-106.

Muraide describes a plurality of external connection terminals 102 along one side of an element substrate as shown in Figure 4 (below). Sechen, ¶¶102-106.

【図 4】



Muraide describes an external connection terminal 102 that is connected to a counter electrode potential line (wiring 400 (LCCOM)), and is located near an end of the row of external connection terminal. In Figure 4, two connection terminals 102 are labelled LCCOM and both are located near the end of each side of the row of terminals 102 (third from the left side end and fourth from the right side end). Sechen, ¶¶102-106. *Muraide* describes an external connection terminal 102 that is connected to a clock signal (CLY) and another external connection terminal 102 that is connected to an inverse clock signal (CLY'), both of which are located near the end of right side of the row of terminals 102. Sechen, ¶¶102-106.

9. Claim 9

Claim 9 depends from claim 7 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

Muraide discloses this limitation. Sechen, ¶¶107-109.

Muraide discloses a clock signal (CLX/CLY) and an inverse clock signal (CLX'/CLY'), which are part of the main wiring lines shown in Figure 4 above. Sechen, ¶¶107-109; *Muraide*, ¶[0079]-[0080]. *Muraide* discloses a counter electrode potential line (LCCOM). As shown in Figure 4, *Muraide* discloses that the clock signals CLX/CLY and CLX'/CLY' do not intersect with the counter electrode potential line LCCOM. Sechen, ¶¶107-109.

10. Claim 10

Claim 10 depends from claim 1 with the further limitation:

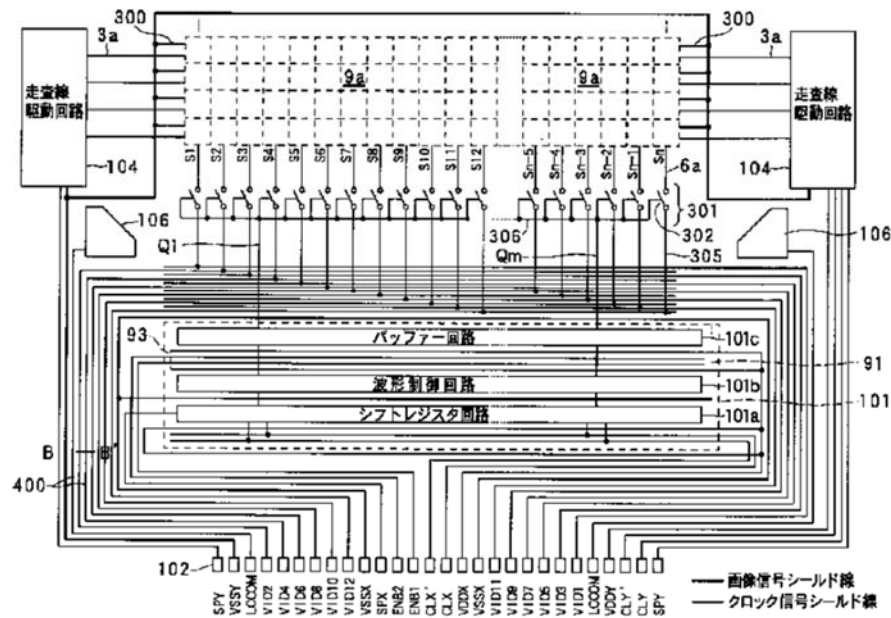
the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals and power source wiring lines that supply power source signals as electric signals, and

the pair of signal lines and power source wiring lines do not intersect each other.

Muraide discloses this limitation. Sechen, ¶¶110-111.

Muraide describes reference clock signals CLX and inverted clock signals CLX' of the reference clock signal CLX. These signals are configured for the internal shift register circuit of the data line drive circuit 101 and supplied via the external input terminals 102 through the wirings 400 (CLX), and the wirings 400 (CLX'). Sechen, ¶¶110-111; *Muraide*, ¶[0080]. *Muraide* discloses power source wiring lines VSSX and VDDX configured for the data line drive circuit 101 as power sources, which are supplied from an external control circuit via the external input terminals 102 and the signal wirings 400 (VSSX) and the wiring 400s (VDDX). *Id.* As shown in Figure 4, the clock signal and power source lines do not intersect each other. Sechen, ¶¶110-111; *Muraide*, ¶[0080]; Fig. 4.

【図4】



11. Claim 11

Claim 11 depends from claim 1 with the further limitation:

the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.

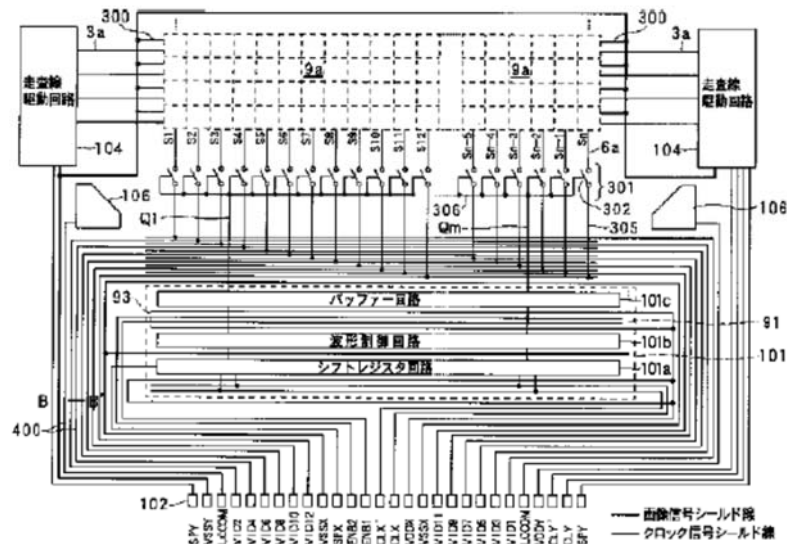
Muraide discloses this limitation. Sechen, ¶¶112-113.

Muraide discloses main wiring lines, such as the wirings 400 (VID1) to 400 (VID12) that are image signal lines are made of the same conductive film (for example, a multilayer film including a conductive polysilicon film and a conductive metal silicide film) as the capacitance lines 300 in the image display region. Sechen, ¶¶112-113; *Muraide*, ¶[0087]. As shown in Figure 4 below, main

wiring lines zig-zag to change route and avoid intersection between one another.

Sechen, ¶¶112-113.

【図4】



12. Claim 13

An electronic apparatus, comprising the electro-optical device according to claim 1.

Muraide discloses this limitation. Sechen, ¶¶114-115.

Muraide describes an “an electro-optical device.” Sechen, ¶¶114-115; *Muraide*, ¶[0001]. *Muraide* further discloses an electronic apparatus that may comprise the electro-optical device: “the electro-optical device in the above-described embodiment may be applied to a projector.” Sechen, ¶¶114-115; *Muraide*, ¶[0109].

C. **Ground 2: *Muraide* in Combination with *Sunao* or *Komeno* and in Further Combination with *Murade III* Renders Obvious Claims 2-3 and 12.**

1. **Claim 2**

Claim 2 depends from claim 1 with the further limitation:

sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

Murade III discloses this limitation. Sechen, ¶¶116-121.

Figures 5 and 6 of *Murade III* (below) are illustrative. Sechen, ¶¶116-119.

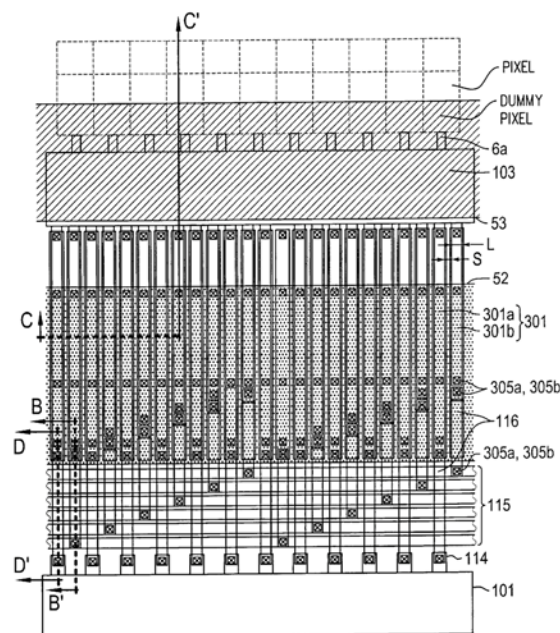


Fig. 5

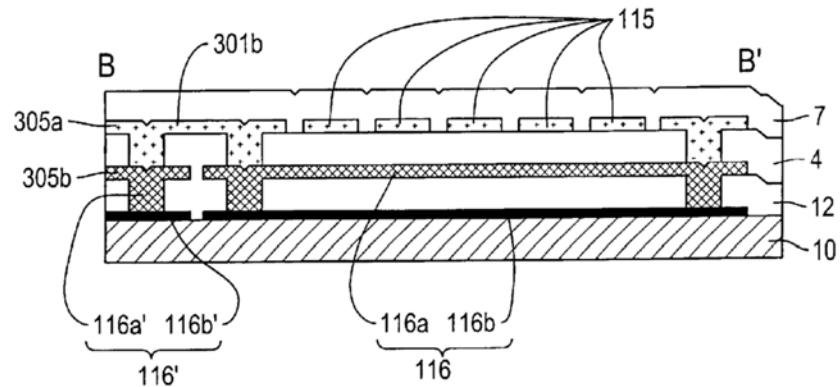


Fig. 6

Figure 5 shows sub-wiring lines, including lines 301 consisting of line 301a of the sampling circuit driving signal lines 114 extending from the data line driving circuit 101, and 301b of the image signal lines 115. Sechen, ¶¶116-119; *Murade III*, col. 18:38-65. Figure 6 shows “image signal lines 115, which are examples of peripheral wirings and leading wirings 301b, are formed using a single metal film.” Sechen, ¶¶116-119; *Murade III*, col. 18:66-19:2.

As seen in Figures 5 and 6, for the data line drive circuit 101, the first portions include the interconnecting lines 116, which is arranged to intersect with the signal lines 115 through the interlayer insulating film 4, and the second portions include the leading wirings 301b, which are formed at the same layer as the signal lines 115 and are arranged not to intersect with the signal lines 115. Sechen, ¶¶116-119.

Murade III specifically discloses first and second portions made of different conductive films. *Murade III* describes interconnecting lines 116 extending from

signal lines 115 to leading wirings 301b (shown in Figure 6) “are formed in the two-layer structure when viewed in the thickness direction of the TFT array substrate, wherein one layer is realized with the second conductive film 116a, and the other layer is realized with the first conductive film 116b.” Sechen, ¶¶116-119; *Murade III*, col. 19:4-13.

A POSITA would have found it obvious to combine *Muraide* and *Murade III*. Sechen, ¶¶120-121. Specifically, a POSITA would have found it obvious to implement *Murade III*’s sub-wiring line structure made of two different conductive films and separated by interlayer insulating film with *Muraide*’s display device. *Id.* A POSITA would have been motivated to combine *Murade III*’s structure with *Muraide*’s display device in order to further isolate the sub-wiring lines. *Id.* This combination would have allowed the device of *Muraide* to potentially further miniaturize. *Id.* Further, as both *Muraide* and *Murade III* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Murade III*’s structure with *Muraide*’s display device. *Id.* Finally, as both references relate to LCDs and describe similar functions combining the design of *Murade III* into *Muraide*’s display device would have yielded predictable results. *Id.*

2. Claim 3

Claim 3 depends from claim 2 with the further limitation:

the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.

Murade III discloses this limitation. Sechen, ¶¶122-126.

Murade III discloses, as shown in Figure 6 below, a contact hole that electrically couples the first and second portions of sub-wiring lines. Sechen, ¶¶122-124.

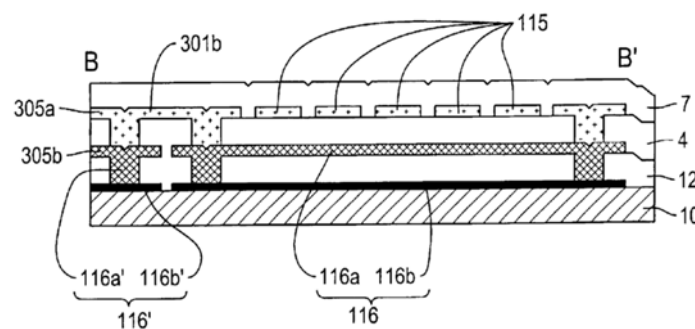


Fig. 6

As seen in Figure 6, contact hole 305b electrically connects the second conductive film 116a to the leading wiring 301b, which are formed in the second interlayer insulating film 4 during the process of forming the contact hole 5.

Sechen, ¶¶122-124; *Murade III*, col. 26:66-27:3.

A POSITA would have combined *Muraide* and *Murade III* for the reasons set forth in claim 2. Sechen, ¶125-126.

3. Claim 12

Claim 12 depends from claim 1 with the further limitation:

the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film.

Murade III discloses this limitation. Sechen, ¶¶127-129.

Murade III specifically discloses redundant wiring lines in two different conductive films. Sechen, ¶¶127-129; *Murade III*, col. 19:51-56 (“the interconnecting lines 116 have a redundant structure”); Fig. 6 (shown above). *Murade III* further discloses multilayer wirings where the different wirings are made of the same film as the conductive film of their respective layers. Sechen, ¶¶127-129; *Murade III*, col. 5:14-25.

A POSITA would have combined *Muraide* and *Murade III* for the reasons set forth in claim 2. Sechen, ¶¶127-129.

D. Ground 3: *Fujikawa* Anticipates Claims 1-5, 7, 8, 11, and 13.

1. Claim 1

An electro-optical device, comprising:

Fujikawa discloses this limitation. Sechen, ¶¶130-131.

Fujikawa teaches that its invention “provides an electrooptic device and an electronic device.” Sechen, ¶¶130-131; *Fujikawa*, abstract.

a plurality of pixel portions provided in an image display region on an element substrate;

Fujikawa discloses this limitation. Sechen, ¶¶132-133.

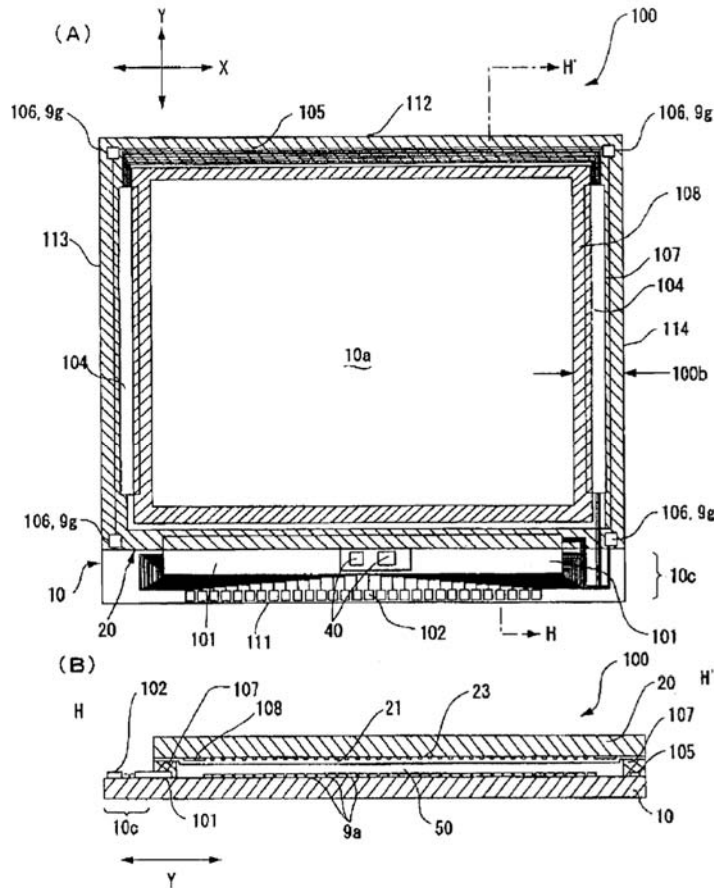
Fujikawa discloses a matrix of pixel electrodes that are formed on a TFT array substrate 10. Sechen, ¶¶132-133; *Fujikawa*, ¶¶[0049], [0050]. Figure 4 of *Fujikawa* depicts this image display region 10a of the liquid crystal device 100, where a plurality of pixels formed in a matrix so as to constitute the image display region 10a. Sechen, ¶¶132-133; *Fujikawa*, ¶[0053], Fig. 4.

in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

Fujikawa discloses this limitation. Sechen, ¶¶134-137.

As shown in *Fujikawa* 1 (below), *Fujikawa* discloses a peripheral region (“10c”) of an element substrate (“TFT array substrate 10”). At the bottom edge of Figure 1, multiple external connection terminals (“terminals 102”) are formed, and connected in a one-to-one manner to main wiring lines. Sechen, ¶¶134-137; *Fujikawa*, ¶¶[0046], [0050], [0053]; Fig. 1. Terminals 102 are made of a metal film with a plurality of lines 109 also made of a low-resistance metal film, such as an aluminum film, connected thereto. The plurality of main lines 109 transfer voltage and signals from the terminals 102 to a data-line driving circuit 101 and a scanning-line driving circuits 104. Sechen, ¶¶134-137; *Fujikawa*, ¶[0055]. The

data-line driving circuit 101 and scanning-line driving circuits 104 drive the pixels in the display region 10a based on the voltage and signals from the terminals 102 through the main lines 109. Sechen, ¶¶134-137; *Fujikawa*, ¶¶[0055]-[0058]; Figs. 1, 2.



Fujikawa Fig. 1

a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

Fujikawa discloses this limitation. Sechen, ¶¶138-139.

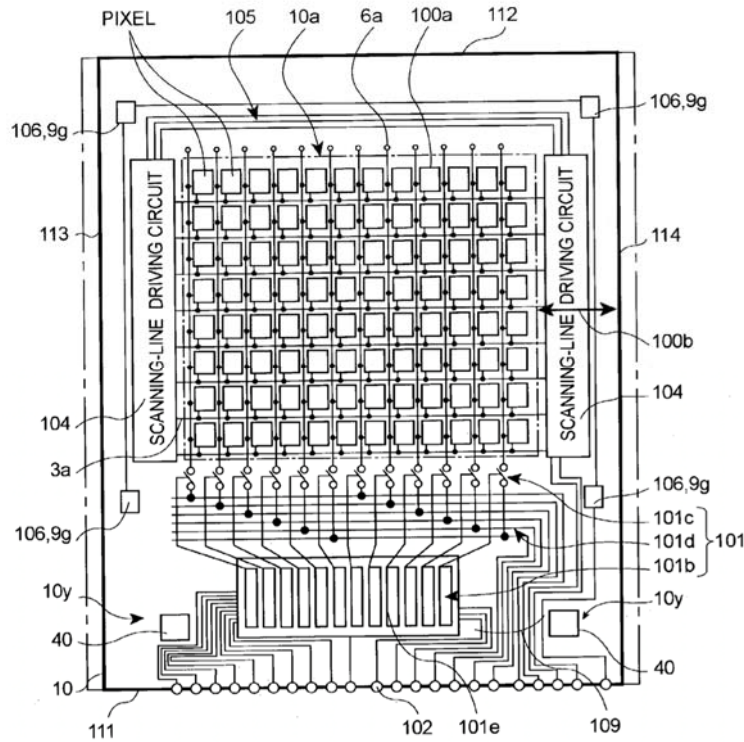
Fujikawa discloses a counter substrate that is arranged to face the element substrate (“TFT array substrate 10”). *Fujikawa* describes that TFT array substrate 10 and a counter substrate 20 that are bonded with a predetermined space therebetween by the sealing material. Sechen, ¶¶138-139; *Fujikawa*, ¶¶[0046], [0049]. Further, *Fujikawa* teaches that the counter electrode 21 is provided on the counter substrate 20 and a constant voltage (DCCOM) can be supplied to the terminals 102 in the peripheral region of the element (TFT array) substrate and then to the counter electrode 21 of the counter substrate 20. Sechen, ¶¶138-139; *Fujikawa*, ¶¶[0078], [0079], Fig. 9.

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

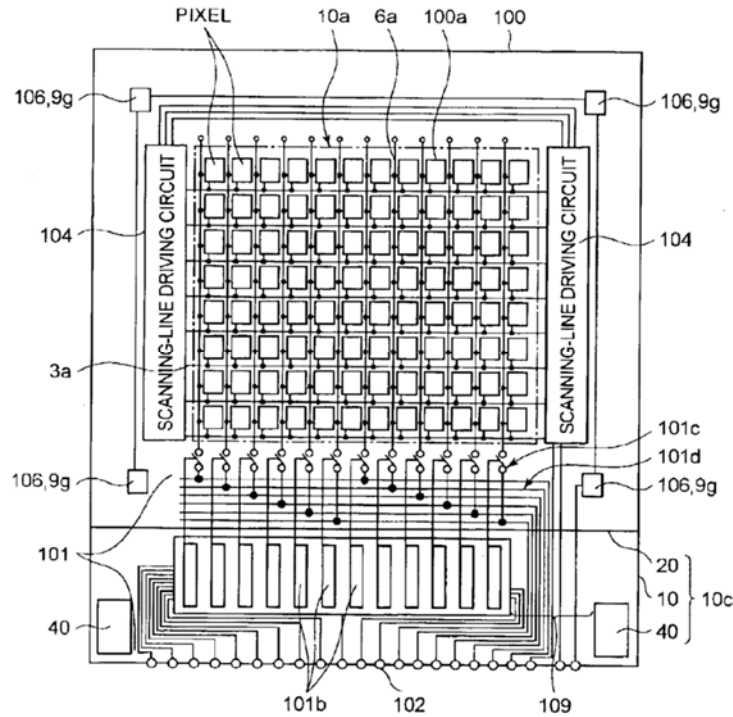
Fujikawa discloses this limitation. Sechen, ¶¶140-143.

Fujikawa discloses terminals 102 along the edge of the peripheral region of the TFT array substrate. As seen in the Figures (below), one of these terminals 102 supply power via a main wiring line 109 to conductive electrodes 9g and conductive materials 106. Conductive elements 9g and 106 electrically connect the TFT array substrate 10 and the counter substrate 20. As explained by *Fujikawa*: “Therefore, a constant voltage (DCCOM) supplied to the terminals 102 of the TFT array substrate 10 can be supplied to the counter electrodes 21 of the

counter substrate 20.” Sechen, ¶¶140-143; *Fujikawa*, ¶¶[0079], [0046], [0047], [0050], [0055], [0072], [0008].



Fujikawa Fig. 12



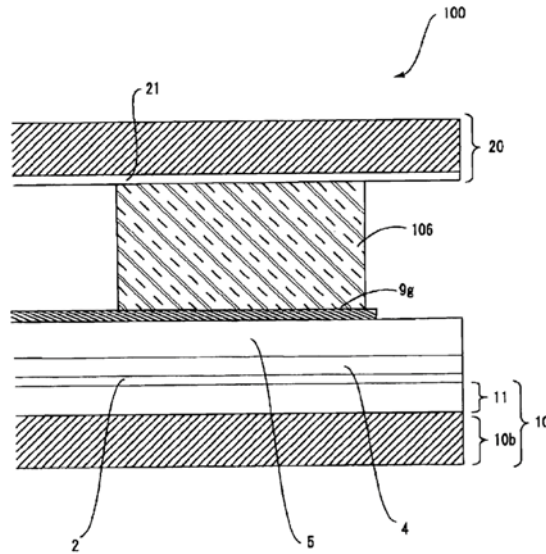
Fujikawa Figure 19

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

Fujikawa discloses this limitation. Sechen, ¶¶144-146.

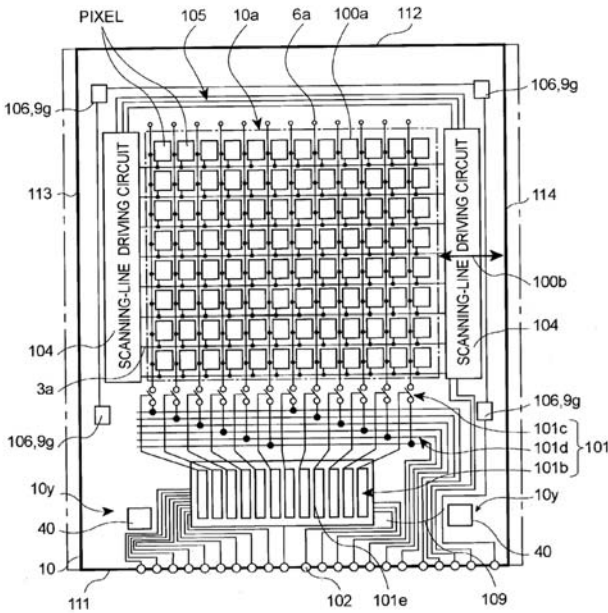
As set forth above, *Fujikawa* discloses conductive electrodes 9g on the TFT array substrate (element substrate) that overlap with the counter substrate 20.

Conductive electrodes 9g are electrically connected to counter electrodes 21 of the counter substrate 20 through conductive material 106 sandwiched between the substrates as seen in *Fujikawa* Figure 9 (below). Sechen, ¶¶144-146.

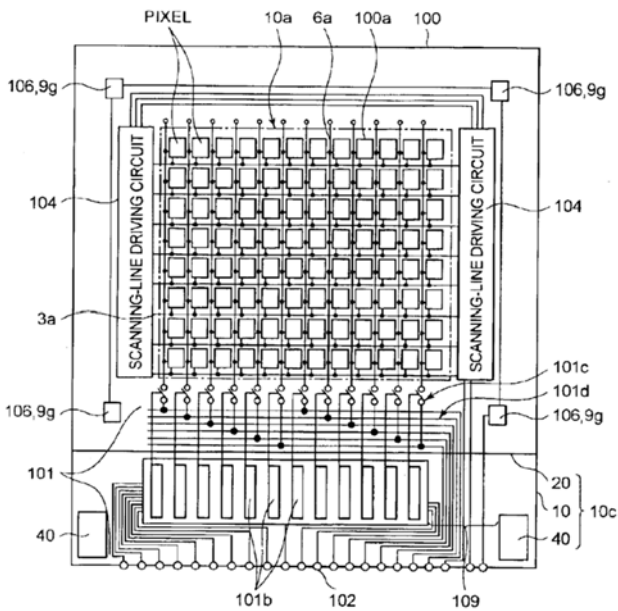


Fujikawa Fig. 9

As seen in *Fujikawa* Figures 12 and 19 (below), conduction terminals (conductive electrodes 9g and conductive materials 106) are formed in areas corresponding to four corners of the counter substrate 20, two being upper conduction terminals and two being lower conduction terminals. Sechen, ¶¶144-146; *Fujikawa*, ¶[0047]. Further, terminals 102 on the TFT array substrate supply power via a main wiring line 109 to conductive electrodes 9g and conductive materials 106. Thereby, a constant voltage (DCCOM) can be supplied to the counter electrodes 21 of the counter substrate 20. Sechen, ¶¶144-146; *Fujikawa*, ¶¶[0078], [0079], Fig. 9. As such, the wiring line 109 that is outermost on the right side in the Figures that leads to and connect the number of conduction terminals (conductive electrodes 9g and conductive materials 106) is a counter electrode potential line. Sechen, ¶¶144-146.



Fujikawa Fig. 12



Fujikawa Figure 19

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

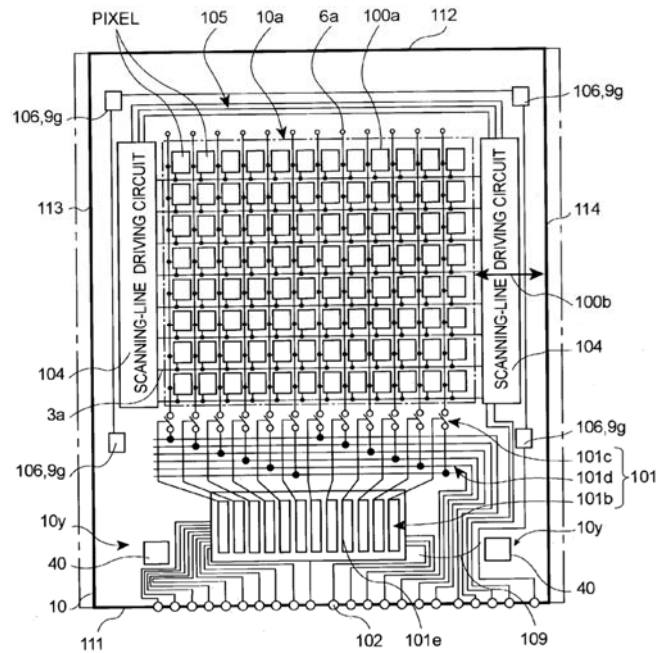
Fujikawa discloses this limitation. Sechen, ¶¶147-148.

Fujikawa discloses a plurality of main wiring lines 109 made of, for example, a low-resistance metal film, such as an aluminum film that are routed from terminals 102. Sechen, ¶¶147-148; *Fujikawa*, ¶[0055]. As seen in Figures 12 and 19 (above), the main wiring lines 109 are laid out in a zig-zag pattern so as to not intersect each other in the peripheral region. Sechen, ¶¶147-148.

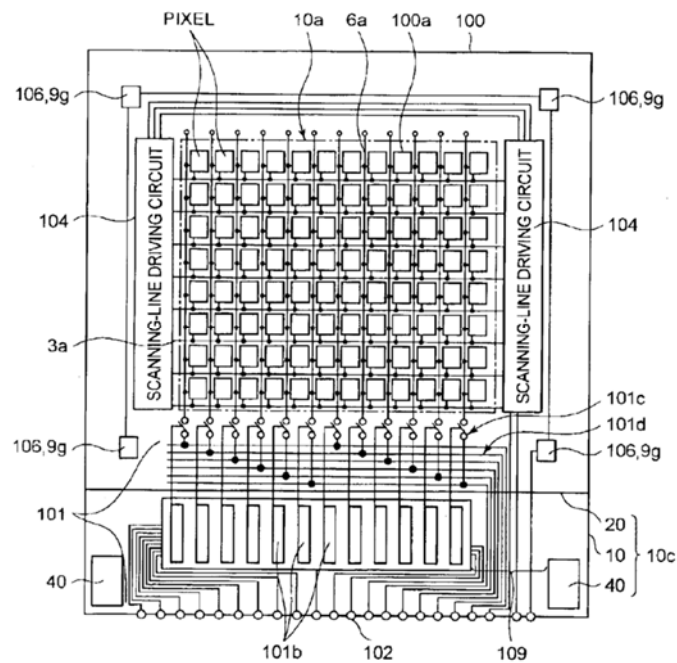
the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.

Fujikawa discloses this limitation. Sechen, ¶¶149-151.

Fujikawa discloses terminals 102 on the TFT array substrate supply power via a main wiring line 109 that leads to and connects conductive electrodes 9g and conductive materials 106. Thereby, a constant voltage (DCCOM) can be supplied to the counter electrodes 21 of the counter substrate 20. Sechen, ¶¶149-151; *Fujikawa*, ¶[0079]. Wiring line 109 that is outermost on the right side of in Figures 12 and 19 that leads to and connects conductive electrodes 9g and conductive materials 106 (conduction terminals) is a counter electrode potential line. Sechen, ¶¶149-151. The counter electrode potential line is also closest to edges of the element substrate, among the wiring lines 109. Sechen, ¶¶149-151; *Fujikawa*, Figs. 12, 19.



Fujikawa Fig. 12



Fujikawa Figure 19

2. Claim 2

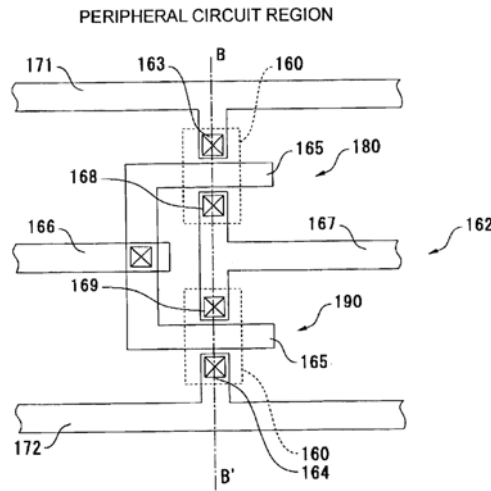
Claim 2 depends from claim 1 with the further limitation:

sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

Fujikawa discloses this limitation. Sechen, ¶¶152-157.

Fujikawa discloses sub-wiring lines which is internal wiring lines of the peripheral driving circuits, as shown in Figures 7 and 8 thereof. Sechen, ¶¶152-157. For example, as shown in Figure 7 (below), *Fujikawa* discloses the structure of a TFT that constitute a peripheral circuit, such as the scanning-line driving circuit 104 or a data-line driving circuit 101, including a high-potential line 171 and a low-potential line 172. Sechen, ¶¶152-157; *Fujikawa*, ¶¶[0074]-[0077]. These lines are electrically connected to source regions of the semiconductor films 160 through contact holes 163 and 164, which are located in the TFTs 180 and 190. Sechen, ¶¶152-157; *Fujikawa*, ¶¶[0074]-[0077]. Figure 7 further shows an input line 166, which is connected to a common gate electrode 165, and an output line 167, which is electrically connected to drain regions of the semiconductor films 160 through contact holes 168 and 169. Sechen, ¶¶152-157; *Fujikawa*, ¶¶[0074]-[0077].

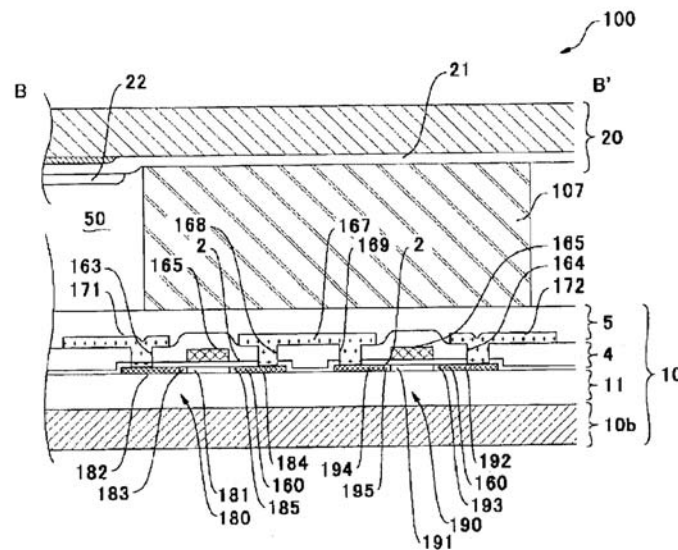
Interlayer conductive line routing is a common and necessary fabrication practice in making semiconductor structures. *Fujikawa* discloses or teaches several such arrangements. Sechen, ¶¶152-157.



Fujikawa Fig. 7

For example, in Figure 7, *Fujikawa* discloses that the first portions are the input lines 166, and the second portions are the vertical portions of the common gate electrodes 165. Sechen, ¶¶152-157; *Fujikawa*, ¶¶[0074]-[0077]. As shown in the cross-section view in *Fujikawa* Figure 8 below, the input lines 166 (at the plane of the output lines 167) is formed in the interlayer insulating film 5, which is on top of the insulating film 4. Sechen, ¶¶152-157; Fig. 8. On the other hand, the main wirings lines 109 are formed on top of the array substrate 10, which is on top of the interlayer insulating film 5, as shown in *Fujikawa* Figure 9 above. Sechen, ¶¶152-157. In other words, the input lines 166 are formed by a conductive film different from the main wiring lines 109, and are separated by the interlayer

insulating film 5. *Fujikawa* Figures 8 and 9 together teach that the input lines 166 are perpendicular to the main wiring lines 109 and, thus, intersect the main wiring lines 109. Sechen, ¶¶152-157. The vertical portions of the common gate electrodes 165 are formed as a conductive film in the interlayer insulating film 4 and on top of the protective underlayer 11 of the substrate. As the input lines 166 appear perpendicular to the main wiring lines 109, the vertical portions of the common gate electrodes 165 appear parallel to the main wirings 109 and, thus, do not intersect the main wirings lines 109. Sechen, ¶¶152-157; *Fujikawa*, ¶[0075], Figs. 7-9.



Fujikawa Figure 8

Thus, *Fujikawa* discloses first portions of the sub-wiring lines as input lines 166, and second portions as at least the vertical portions of the common gate electrodes 165. Among these portions, input lines 166 are perpendicular to the

main wiring lines 109 and, thus, intersect the main wiring lines 109, but the vertical portions of the common gate electrodes 165 appear parallel to the main wirings 109 and, thus, do not intersect the main wirings lines 109. Sechen, ¶¶152-157.

3. Claim 3

Claim 3 depends from claim 2 with the further limitation:

the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.

Fujikawa discloses this limitation. Sechen, ¶¶158-159.

As set forth and shown in Figure 7 above, *Fujikawa* discloses that input line 166 is connected to a common gate electrode 165, and an output line 167 is electrically connected to drain regions of the semiconductor films 160 through contact holes 168 and 169, respectively. Sechen, ¶¶158-159; *Fujikawa*, ¶¶[0074]-[0077]. That is, *Fujikawa* discloses first portions of the sub-wiring lines (input lines 166) and second portions of the sub-wiring lines (the vertical portions of the common gate electrodes 165) are electrically connected through contact holes. Sechen, ¶¶158-159.

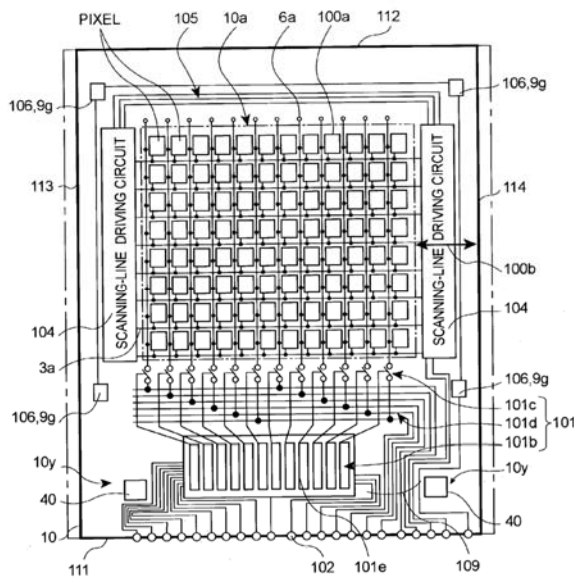
4. Claim 4

Claim 4 depends from claim 1 with the further limitation:

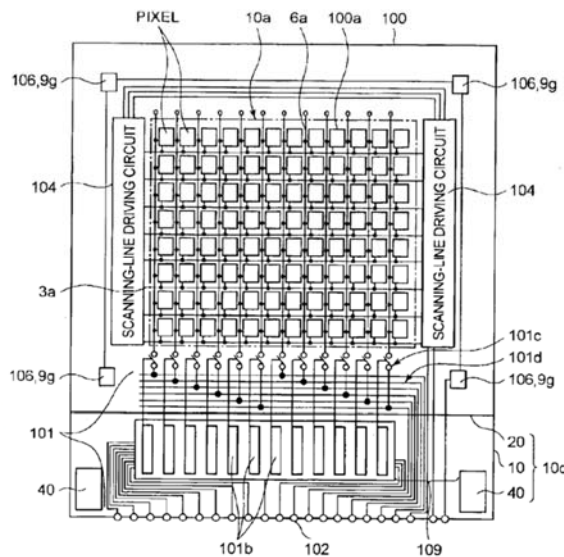
the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.

Fujikawa discloses this limitation. Sechen, ¶¶160-161.

As seen in *Fujikawa* Figures 12 and 19, the scanning line driving circuits 104 are nearer to the center of substrate 10 than the conductive electrodes 9g/conductive materials 106 and the main wiring line leading from one of the terminals 102 to conductive electrodes 9g (the counter electrode potential line), which is located at the outermost right in the Figures. Sechen, ¶¶160-161; *Fujikawa*, Figs. 12, 19.



Fujikawa Fig. 12



Fujikawa Fig. 19

5. Claim 5

Claim 5 depends from claim 4 with the further limitation:

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

Fujikawa discloses this limitation. Sechen, ¶¶162-163.

As seen in Figures 12 and 19 of *Fujikawa* (above), there are a plurality of external circuit connection terminals (102) along the lower edge (111) of the substrate. The main wiring line leading from one of the terminals 102 to conductive electrodes 9g (the counter electrode potential line), is positioned near the end of an array of the plurality of external circuit connection terminals (it is located at the outermost right in Figures 12 and 19). Sechen, ¶¶162-163; *Fujikawa*, ¶[0055].

6. Claim 7

Claim 7 depends from claim 1 with the further limitation:

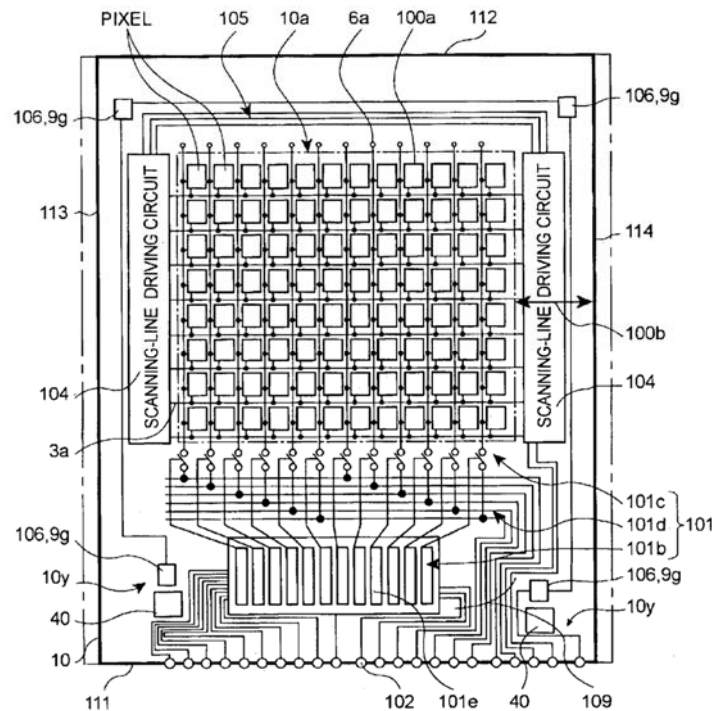
a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

Fujikawa discloses this limitation. Sechen, ¶¶164-166.

Claim 7's requirement that "parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region" contradicts claim 1's requirement that "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Further, the '390 patent does not appear to disclose any such structure. Sechen, ¶¶164-166.

Nonetheless, to the extent claim 7 is determined not to be nonsensical, *Fujikawa* teaches this limitation. Sechen, ¶¶164-166.

As shown *Fujikawa* Figure 14, which is another embodiment of *Fujikawa*, the scanning line driving circuit 104 is positioned closer to the center of substrate 10 than the conductive electrodes 9g/conductive materials 106 and the counter electrode potential line. However, portions of the data line driving circuit 101 is partially positioned closer to the lower and side edges of the substrate 10 than the conductive electrodes 9g/conductive materials 106 and the counter electrode potential line. Sechen, ¶¶164-166.



Fujikawa Fig. 14

7. Claim 8

Claim 8 depends from claim 7 with the further limitations of:

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.

As claim 8 depends from claim 7, it suffers from the same inconsistencies with claim 1. To the extent claim 8 is a proper claim, *Fujikawa* discloses this limitation. Sechen, ¶¶167-169.

Fujikawa discloses are a plurality of external circuit connection terminals (102) along the lower edge (111) of the substrate. Sechen, ¶¶167-169; Fig. 14; see also Figs. 12, 19. The main wiring line leading from one of the terminals 102 to conductive electrodes 9g (the counter electrode potential line), is located at the outermost right in the Figures. Sechen, ¶¶167-169. In other words, the counter electrode potential line is positioned near the end of an array of the plurality of external circuit connection terminals. Sechen, ¶¶167-169.

8. Claim 11

Claim 11 depends from claim 1 with the further limitation:

the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.

Fujikawa discloses this limitation. Sechen, ¶¶170-171.

Fujikawa discloses a plurality of main wiring lines 109 made of, for example, a low-resistance metal film, such as an aluminum film that are routed from terminals 102. Sechen, ¶¶170-171; *Fujikawa*, ¶[0055]. As seen in Figures 12 and 19 (above), the main wiring lines 109 are laid out in a zig-zag pattern so as to not intersect each other in the peripheral region. Sechen, ¶¶170-171.

9. Claim 13

An electronic apparatus, comprising the electro-optical device according to claim 1.

Fujikawa discloses this limitation. Sechen, ¶¶172-173.

Fujikawa discloses that its invention an electrooptic device and an electronic device. Sechen, ¶¶172-173; *Fujikawa*, abstract. *Fujikawa* further discloses such devices can be used as part of different devices (apparatuses), including “as display sections in electronic devices, such as portable telephones, portable computers, and video cameras.” Sechen, ¶¶172-173; *Fujikawa*, ¶[0004].

E. Ground 4: *Murade II* in Combination with *Sunao* or *Komeno* Renders Obvious Claims 1, 4-11 and 13.

1. Claim 1

An electro-optical device, comprising:

Murade II discloses an electro-optical device. Sechen, ¶¶174-175.

Murade II is titled an “Electro-optical device and electronic apparatus” Sechen, ¶¶174-175; *Murade II*, cover.

a plurality of pixel portions provided in an image display region on an element substrate;

Murade II discloses this limitation. Sechen, ¶¶176-177.

Murade II discloses an “image display area” that has a plurality of pixel electrodes. *Murade II* defines an image display area as being “a particular area of the liquid crystal apparatus where an image is displayed by changing the alignment of the liquid crystal.” Sechen, ¶¶176-177; *Murade II*, col. 15:31-35. *Murade II* discloses that the image display region is on an TFT array substrate (element substrate). Sechen, ¶¶176-177; *Murade II*, col. 13:61-64; Fig. 1.

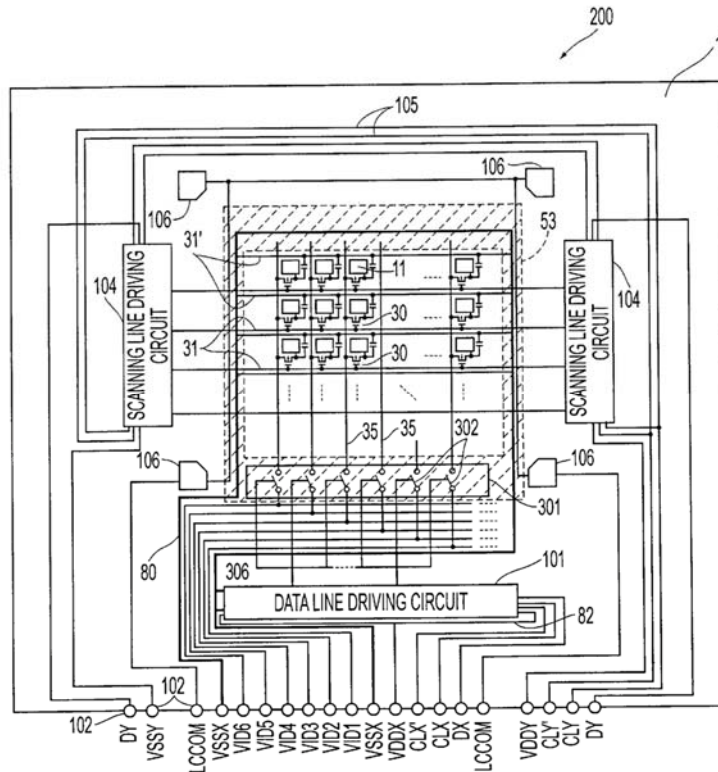
in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

Murade II discloses this limitation. Sechen, ¶¶178-179.

Figure 1 of *Murade II* (below) discloses components on a TFT substrate.

Murade II, col. 13:61-64. Figure 1 of *Murade II* depicts a liquid crystal apparatus 200 with a TFT array substrate 1. Sechen, ¶¶178-179. The image display region is shown in the center portion of the figure as identified by the plurality of pixel electrodes 11. Figure 1 of *Murade II* also depicts the relationship between the pixel display area and the peripheral area. Sechen, ¶¶178-179. External input terminals 102 are shown disposed along a lower side of the TFT array substrate 1, which correspond to the claimed external circuit connection terminals. Figure 1 shows a plurality of wiring lines connected to the external input terminals 102. The plurality of wiring lines are designated with different names as shown along the bottom of the figure. Sechen, ¶¶178-179. For example, “a clock signal having a name ‘CLX’ is represented by ‘clock signal CLX’ and the corresponding signal wiring is represented by ‘wiring CLX’).” (e.g., CLX).” Sechen, ¶¶178-179; *Murade II*, col. 15:42-52. In *Murade II*, peripheral driving circuits drive the pixel

portions via the wiring lines. In particular, *Murade II* discloses negative and positive power supplies that are supplied to the “scanning line driving circuits 104 from an external control circuit via the external input terminals 102 and further via wirings VSSY and VDDY.” Sechen, ¶¶178-179; *Murade II*, col. 15:53-57.



Murade II Figure 1

a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

Murade II discloses this limitation. Sechen, ¶¶180-182.

Murade II describes its liquid crystal apparatus 200 as including a TFT substrate and an opposite substrate 2 that has electrode 21 formed on the opposite substrate 2. Opposite substrate 2 faces the TFT (or element) substrate as shown in

Murade II Figure 13 (below). Sechen, ¶¶180-182; *Murade II*, col. 28:13-29; Fig. 13.

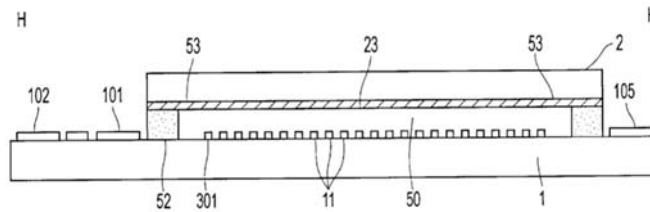


FIG. 13

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

Murade II discloses this limitation. Sechen, ¶¶183-184.

Murade II discloses a counter electrode potential line. For example, *Murade II* describes a signal and wiring designated LCCOM as “a power supply of a common electrode.” Sechen, ¶¶183-184. *Murade II* then describes how the LCCOM wiring supplies power via elements 106 on the TFT to a “common electrode provided on an opposite substrate.” Sechen, ¶¶183-184; *Murade II*, col. 19:45-50; Fig. 1. As shown in Figure 1 (above), LCCOM is one of the main wiring lines. Sechen, ¶¶183-184.

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

Murade II discloses this limitation. Sechen, ¶¶185-186.

Murade II discloses upper-to-lower “conducting elements 106” at the four corners of the image display area as seen in Figure 1 (above). The conducting elements 106 electrically connect the TFT substrate and opposite substrate. Sechen, ¶¶185-186; *Murade II*, col. 15:38-42. *Murade II* Figure 1 teaches the LCCOM line (counter potential electrode line) connects with conducting elements 106. Sechen, ¶¶185-186.

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

Murade II discloses this limitation. Sechen, ¶¶187-189.

Murade II discloses wiring lines that are made of a conductive film. For example, *Murade II* teaches that “wirings DY, VSSY, . . . , VDDX ... are made of the same low-resistance metal material as that used to form the data lines 35, such as Al (aluminum).” Sechen, ¶¶187-189; *Murade II*, col. 19:20-24. These various wiring lines are the main wiring lines that are “connected to the corresponding external input terminals 102” and are formed on the same layer (the first interlayer insulating layer 42 on the TFT array substrate 1). Sechen, ¶¶187-189; *Murade II*, col. 19:34-44. These wiring can thus be formed at the same time using the same low-resistance metal layer, such as an Al layer. *Id.*

In addition, *Murade II* discloses that these wiring lines are arranged so as not to intersect each other as seen in *Murade II* Figures 1-3 and 7(b). Sechen, ¶¶187-189.

the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.

For the same reasons set forth in regard to *Muraide* in Ground 1, this limitation is obvious over *Murade II* as being a mere design choice. *Murade II* teaches a counter electrode potential line located nearer to the center of the substrate with respect to the scanning line drive circuit. It is a simple choice design choice to locate the counter electrode potential line nearer to the edge than the scanning line drive circuit that does not change any property or characteristics of the wiring layout, and thus, is obvious under §103. Sechen, ¶190.

Alternatively, as set forth in Ground 1 (Section VI.B.1), *Sunao* discloses this limitation. Sechen, ¶191.

A POSITA would have found it obvious to combine *Murade II* and *Sunao*. Sechen, ¶¶192, 195. Specifically, a POSITA would have found it obvious to implement *Sunao*'s placement of the counter electrode potential line as closest to the edge of the substrate with *Murade II*'s display device. *Id.* A POSITA would have been motivated to combine *Sunao*'s placement of the counter electrode potential line with *Murade II*'s display device in order to further isolate the

electrode potential line from the other wirings and the display area. *Id.* This combination would have allowed the device of *Murade II* to potentially further miniaturize. *Id.* Further, as both *Murade II* and *Sunao* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Sunao*'s placement with *Murade II*'s display device. *Id.* Finally, as both references relate to LCDs and describe similar functions combining the design of *Sunao* into *Murade II*'s display device would have yielded predictable results. *Id.*

Alternatively, as set forth in Ground 1 (Section VI.B.1), *Komeno* discloses this limitation. Sechen, ¶193.

A POSITA would have found it obvious to combine *Murade II* and *Komeno*. Sechen, ¶¶194-195. Specifically, a POSITA would have found it obvious to implement *Komeno*'s placement of the of the counter electrode potential line as closest to the edge of the substrate with *Murade II*'s display device. *Id.* A POSITA would have been motivated to combine *Komeno*'s placement of the counter electrode potential line with *Murade II*'s display device in order to further isolate the electrode potential line from the other wirings and the display area. *Id.* This combination would have allowed the device of *Murade II* to potentially further miniaturize. *Id.* Further, as both *Murade II* and *Komeno* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Komeno*'s placement of the counter electrode potential line with *Murade II*'s

display device. *Id.* Finally, as both references relate to LCDs and describe similar functions combining the design of *Komeno* into *Murade II*'s display device would have yielded predictable results. *Id.*

2. Claim 4

Claim 4 depends from claim 1 with the further limitation:

the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.

As set forth in Ground 1 (Section VI.B.4), *Sunao* discloses this limitation. For the reasons set forth in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Sunao*. Sechen, ¶¶196, 198.

As set forth above in Ground 1 (Section VI.B.4), *Komeno* discloses this limitation. For the reasons set forth above in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Komeno*. Sechen, ¶¶197-198.

3. Claim 5

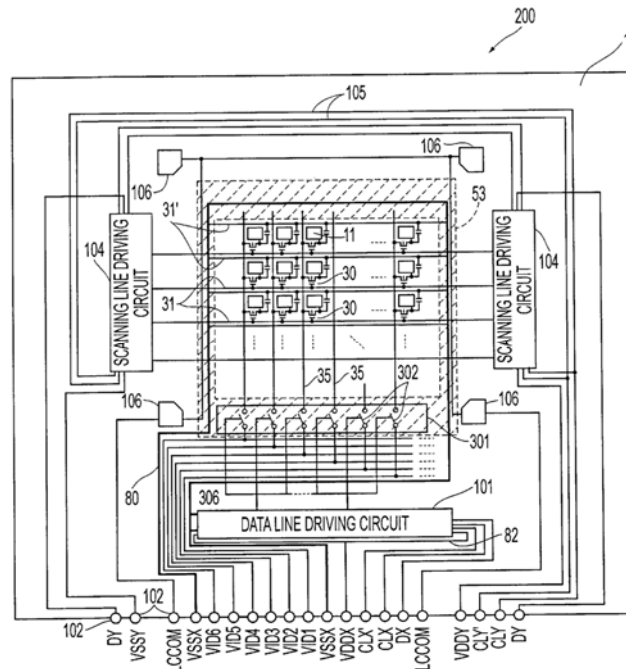
Claim 5 depends from claim 4 with the further limitation:

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

Murade II discloses this limitation. Sechen, ¶¶199-203.

Murade II teaches external circuit connection terminals (“external input terminals 102 in *Murade II*) as being disposed along one side of the TFT array substrate. Sechen, ¶¶199-203. *Murade II* further discloses an external connection terminal (“external input terminal 102”) being coupled to the counter electrode potential line (“LCCOM”). Sechen, ¶¶199-203; *Murade II*, col. 19:45-50. As seen in *Murade II* Figures 1-3, LCCOM is the third external input terminal at the left end of the substrate. Sechen, ¶¶199-203; Figs. 1-3.



Murade II Figure 1

Alternatively, *Komeno* discloses this limitation. As set forth in Section V.B.1 (Ground 1: *Muraide*), *Komeno* discloses the external circuit connection terminal coupled to one end of the counter electrode potential line being located closest to the left edge among the array of the plurality of the external circuit connection terminals. Sechen, ¶¶199-203.

For the reasons set forth in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine Murade II and *Komeno*. Sechen, ¶¶202-203.

4. Claim 6

Claim 6 depends from claim 4 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

Murade II discloses this limitation. Sechen, ¶¶204-206.

Murade II specifically discloses a “reference clock signal CLY for the scanning line driving circuit and an inverted clock signal CLY' thereof.” Sechen, ¶¶204-206; *Murade II*, col. 15:60-62. *Murade II* discloses a predetermined timing based on these clock signals (CLY, CLY'): “the scanning line driving circuits 104 apply a scanning signal in the form of a pulse to the scanning lines 31, line by line.” Sechen, ¶¶204-206; *Murade II*, col. 15:60-65. *Murade II* also discloses a counter electrode potential line (LCCOM). Sechen, ¶¶204-206; *Murade II*, col. 19:45-50.

Murade II Figures 2 and 3 (below) teaches laying out the clock signal lines in a configuration where they do not intersect the counter electrode potential line. Sechen, ¶¶204-206; *Murade II*, Figs. 2, 3.

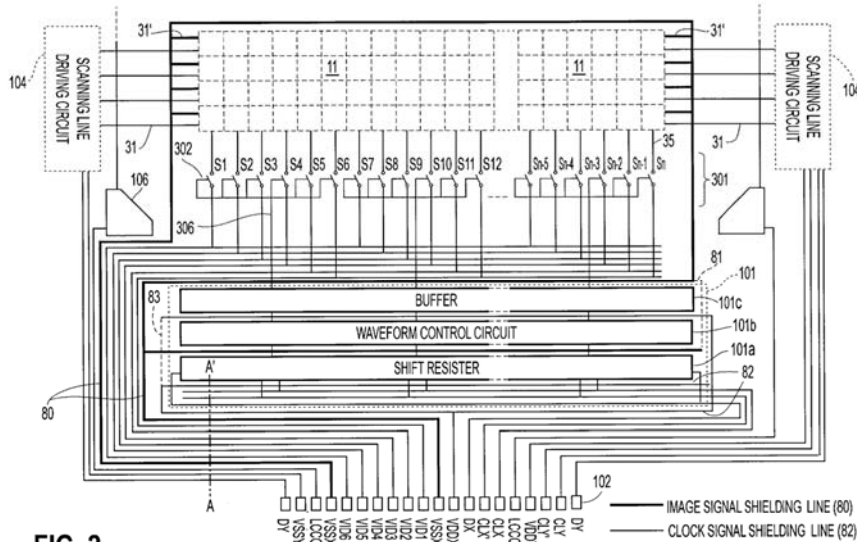


FIG. 2

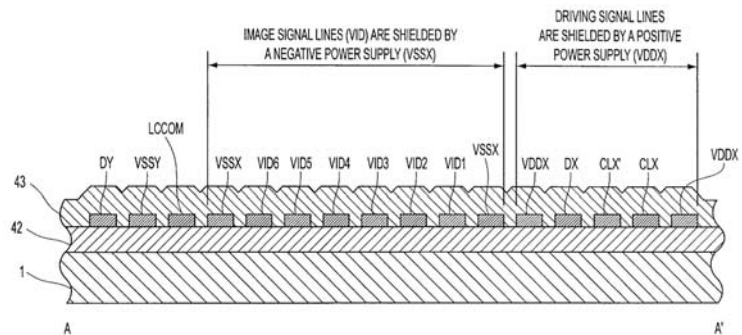


FIG. 3

5. Claim 7

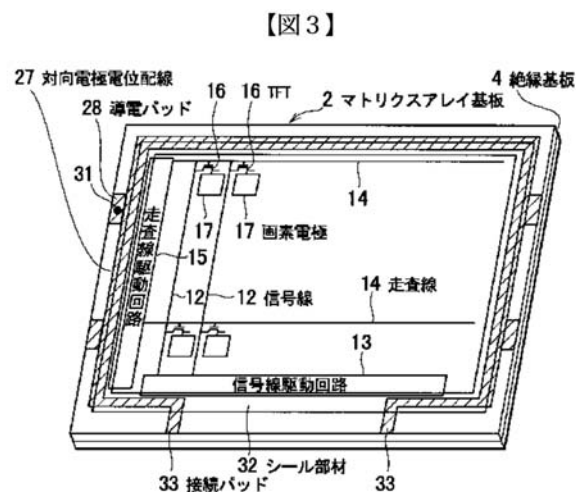
Claim 7 depends from claim 1 with the further limitation:

a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

Claim 7's requirement that "parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and

lower conduction terminals and the counter electrode potential lines in the peripheral region” contradicts claim 1’s requirement that “the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.” Further, the ’390 patent does not appear to disclose any such structure. Sechen, ¶207.

Nonetheless, to the extent claim 7 is determined not to be nonsensical, *Sunao* discloses this limitation. Sechen, ¶¶208-210. In *Sunao*, the scanning line driving circuit 15 is nearer to the center of the element substrate than the conductive pads 28. In addition, the signal line driving circuit 13 is nearer to the lower edge of the element substrate than the conductive pads 28. Sechen, ¶¶208-210.



For the reasons set forth above in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Sunao*. Sechen, ¶¶208-210.

6. Claim 8

Claim 8 depends from claim 7 with the further limitation:

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.

Murade II discloses this limitation. Sechen, ¶¶211-213.

Murade II teaches external circuit connection terminals (“external input terminals 102 in *Murade II*) as being disposed along one side of the TFT array substrate. Sechen, ¶¶211-213. *Murade II* further teaches an external connection terminal (“external input terminal 102”) being connected to the other end or one end of plurality of main wiring lines, for example, LCCOM. Sechen, ¶¶211-213; *Murade II*, col. 19:45-50. As seen in *Murade II* Figures 1-3, LCCOM is the third external input terminal at the left end of the substrate. Sechen, ¶¶211-213; Figs. 1-3.

7. Claim 9

Claim 9 depends from claim 7 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

Murade II discloses this limitation. Sechen, ¶¶214-216.

Murade II discloses a plurality of main wiring lines that includes a clock signal (CLY) and an inverse clock signal (CLY'). Sechen, ¶¶214-216; *Murade II*, col. 15:60-65. *Murade II* further discloses a “a signal LCCOM is input as a power supply of a common electrode via an external input terminal 102, and supplied via an wiring LCCOM and also via the upper-to-lower conducting elements 106, ... to a common electrode (refer to FIG. 10) provided on an opposite substrate.” Sechen, ¶¶214-216; *Murade II*, col. 19:45-50. *Murade II* teaches that these lines do not intersect each other. For example, Figures 1 and 2 (below) show no intersection between the clock signal lines and the power source wiring line (LCCOM). Sechen, ¶¶214-216; Figs. 1-3.

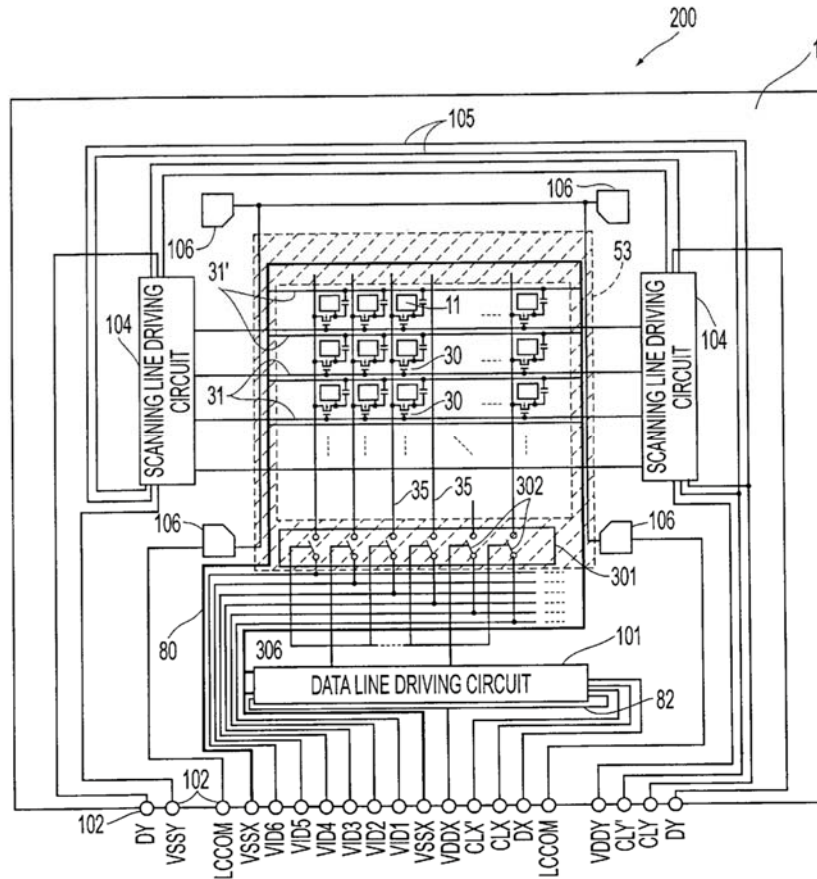
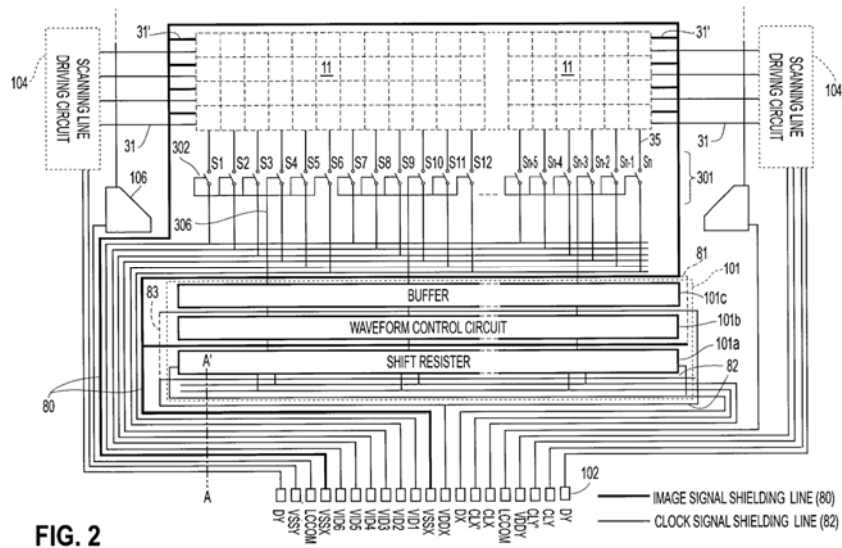
Fig. 1 of *Murade II*

FIG. 2

Fig. 2 of *Murade II*

8. Claim 10

Claim 10 depends from claim 1 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals and power source wiring lines that supply power source signals as electric signals, and

the pair of signal lines and power source wiring lines do not intersect each other.

Murade II discloses this limitation. Sechen, ¶¶217-219.

Murade II discloses a plurality of main wiring lines that includes a clock signal (CLY) and an inverse clock signal (CLY'). Sechen, ¶¶217-219; *Murade II*, col. 15:60-65. *Murade II* further discloses a “a signal LCCOM is input as a power supply of a common electrode via an external input terminal 102, and supplied via an wiring LCCOM and also via the upper-to-lower conducting elements 106, ... to a common electrode (refer to FIG. 10) provided on an opposite substrate.” Sechen, ¶¶217-219; *Murade II*, col. 19:45-50.

Murade II teaches that these lines do not intersect each other. For example, Figures 1 and 2 (shown above) show no intersection between the clock signal lines and the power source wiring line (LCCOM). Sechen, ¶¶217-219; Figs. 1-3.

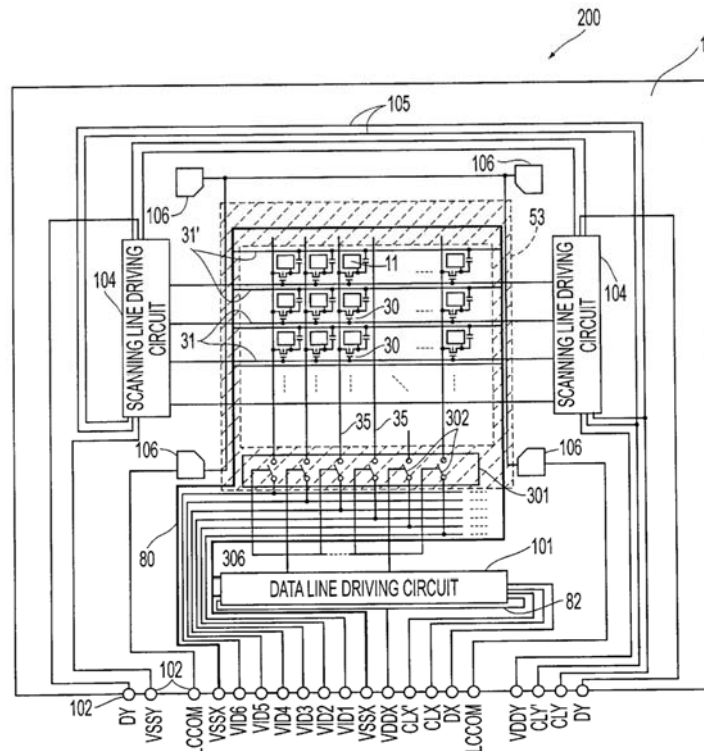
9. Claim 11

Claim 11 depends from claim 1 with the further limitation:

the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.

Murade II discloses this limitation. Sechen, ¶¶220-221.

Figure 1 of *Murade II* (below) is illustrative. Sechen, ¶¶220-221



As shown, the signal lines are planarly laid at the same layer and routed to zig-zag around each other in order to avoid intersection at the same layer. Sechen, ¶¶220-221; *Murade II*, Figs. 1, 3.

10. Claim 13

An electronic apparatus, comprising the electro-optical device according to claim 1.

Murade II discloses this limitation. Sechen, ¶¶222-223.

Murade II specifically discloses that: “Examples of electronic devices including the electro-optical apparatus 200 are described below with reference to FIGS. 14-18.” Sechen, ¶¶222-223; *Murade II*, col. 33:39-41.

F. Ground 5: *Murade II* in Combination with *Sunao* or *Komeno* and in Further Combination with *Murade III* Renders Obvious Claims 2, 3 and 12.

1. Claim 2

Claim 2 depends from claim 1 with the further limitation:

sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

Murade III discloses this limitation. Sechen, ¶¶224-229.

Murade III Figures 5 and 6 (below) are illustrative. Figure 5 shows sub-wiring lines, including lines 301 consisting of line 301a of the sampling circuit driving signal lines 114 extending from the data line driving circuit 101, and 301b of the image signal lines 115. Sechen, ¶¶224-229.

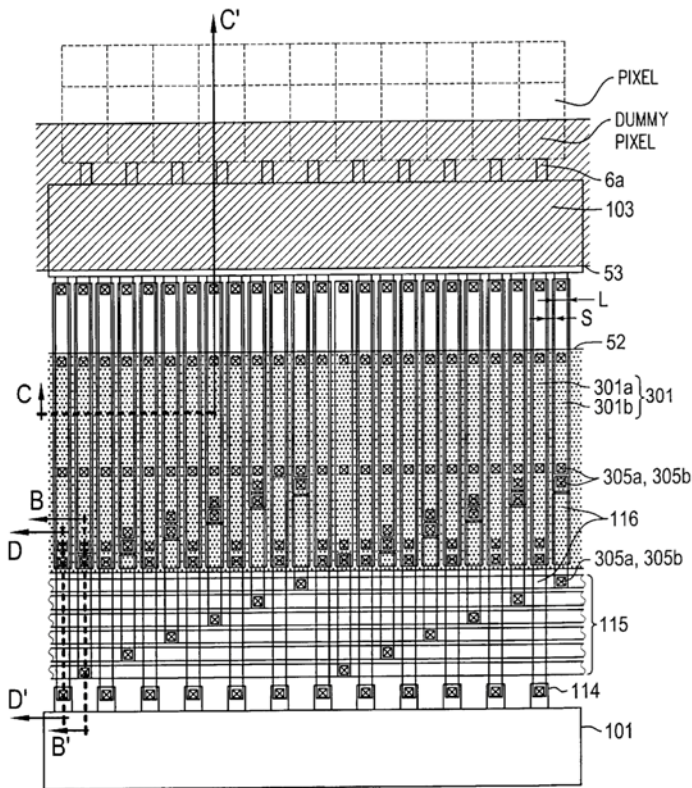


Fig. 5

Murade III Figure 6 shows “image signal lines 115, which are examples of peripheral wirings and leading wirings 301b, are formed using a single metal film.”

Sechen, ¶¶224-229; *Murade III*, col. 18:66-19:2.

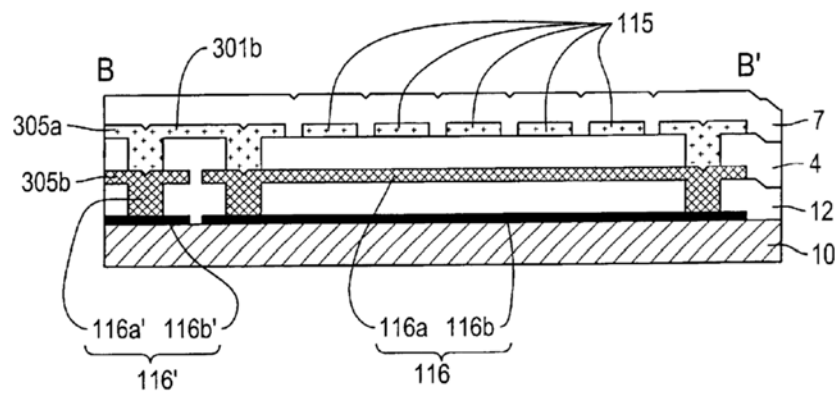


Fig. 6

Murade III specifically discloses first and second portions made of different conductive films. In particular, *Murade III* describes interconnecting lines 116 extending from signal lines 115 to leading wirings 301b (shown in Figure 6) “are formed in the two-layer structure when viewed in the thickness direction of the TFT array substrate, wherein one layer is realized with the second conductive film 116a, and the other layer is realized with the first conductive film 116b.” Sechen, ¶¶224-229; *Murade III*, col. 19:4-13. As seen in Figures 5 and 6, for the data line drive circuit 101, the first portions include the interconnecting lines 116, which is arranged to intersect with the signal lines 115 through the interlayer insulating film 4, and the second portions include the leading wirings 301b, which are formed at the same layer as the signal lines 115 and are arranged not to intersect with the signal lines 115. Sechen, ¶¶224-229.

A POSITA would have found it obvious to combine *Murade II* and *Murade III*. Sechen, ¶¶228-229. Specifically, a POSITA would have found it obvious to implement *Murade III*’s sub-wiring line structure made of two different conductive films and separated by interlayer insulating film with *Murade II*’s display device. *Id.* A POSITA would have been motivated to combine *Murade III*’s structure with *Murade II*’s display device in order to further isolate the sub-wiring lines. *Id.* This combination would have allowed the device of *Murade II* to potentially further miniaturize. *Id.* Further, as both *Murade II* and *Murade III* relate to displays, and

specifically LCDs, a POSITA would have found it straightforward to combine *Murade III*'s structure with *Murade II*'s display device, and the combination would have yielded predictable results. *Id.*

2. Claim 3

Claim 3 depends from claim 2 with the further limitation:

the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.

Murade III discloses this limitation. Sechen, ¶¶230-234.

Murade III discloses, as shown in Figure 6 below, a contact hole that electrically couples the first and second portions of sub-wiring lines. As seen in Figure 6, contact hole 305b electrically connects the second conductive film 116a to the leading wiring 301b, which are formed in the second interlayer insulating film 4 during the process of forming the contact hole 5. Sechen, ¶¶230-234; *Murade III*, col. 26:66-27:3.

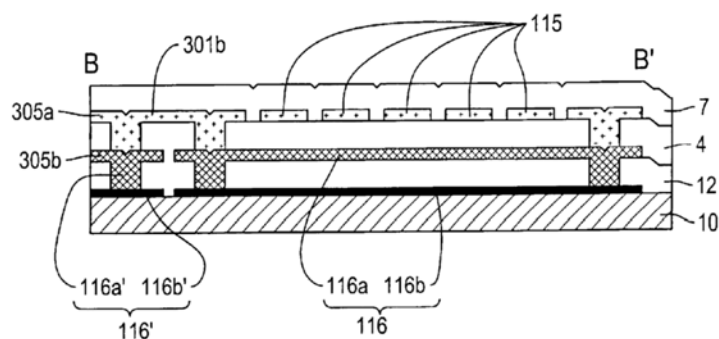


Fig. 6

A POSITA would have combined *Murade II* and *Murade III* for the reasons set forth in claim 2. Sechen, ¶¶233-234.

3. Claim 12

Claim 12 depends from claim 1 with the further limitation:

the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film.

Murade III discloses this limitation. Sechen, ¶¶235-237.

Murade III discloses redundant wiring lines in two different conductive films. Sechen, ¶¶235-237; *Murade III*, col. 19:51-56 (“the interconnecting lines 116 have a redundant structure”); Fig. 6 (shown above). *Murade III* discloses multilayer wirings where the different wirings are made of the same film as the conductive film of their respective layers. Sechen, ¶¶235-237; *Murade III*, col. 5:14-25.

A POSITA would have combined *Murade II* and *Murade III* for the reasons set forth in claim 2. Sechen, ¶¶236-237.

VII. GROUNDS FOR STANDING

Petitioner certifies that the '390 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the '390 patent challenging the claims on the grounds in this Petition.

VIII. CONCLUSION

Petitioner requests IPR and cancellation of the challenged claims because they are unpatentable under 35 U.S.C. § 102 and/or § 103 based on the foregoing grounds.

IX. MANDATORY NOTICES

I. Real Parties-in-Interest

The real parties-in-interest are HKC Corp. Ltd., Chongqing HKC Optoelectronics Technology Co., Ltd., and HKC Overseas Ltd.

A. Related Matters

Crystal Leap has asserted the '390 patent against the parties-in-interest on September 30, 2022, in *Crystal Leap Zrt v. HKC Corp. Ltd., Chongqing HKC Optoelectronics Technology Co., Ltd., and HKC Overseas Ltd.*, Case No. 2:22-cv-00382 (E.D. Tex.).

B. Lead and Back-Up Counsel, and Service Information

Lead Counsel	Back-up Counsel
Wenye Tan (Reg. No. 55,662) wtan@anovalaw.com Anova Law Group, PLLC 21495 Ridgetop Circle, Suite 300 Sterling, VA 20166 Tel: 571-379-9468	Li Jiang (Reg. No. 74,191) li.jiang@anovalaw.com Anova Law Group, PLLC 21495 Ridgetop Circle, Suite 300 Sterling, VA 20166 Tel: 202-365-8329

Petitioner consents to electronic service at the email addresses listed above.

II. CERTIFICATION UNDER 37 C.F.R. § 42.24(D)

This petition complies with the requirements of 37 C.F.R. § 42.24. As calculated by the word count feature of Microsoft Word, it contains 13,951 words, excluding the words contained in the following: Table of Contents, List of Exhibits, Mandatory Notices, Certification Under § 42.24(d), and Certificate of Service.

Dated: February 3, 2023

Respectfully submitted,

/Wenye Tan/

Wenye Tan (Reg. No. 55,662)

Li Jiang (Reg. No. 74,191)

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Petition for *Inter Partes* Review, the associated Powers of Attorney, and Exhibits 1001-1011 are being served on February 3, 2023, by Priority Mail Express or by means at least as fast and reliable as Priority Mail Express at the following address of record for the subject patent.

Public PAIR Address	Current Business Address
OLIFF PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850	OLIFF PLC 11 Canal Center Plaza, Suite 200 ALEXANDRIA, VA 22314

Courtesy copies of the same documents were served on February 3, 2023 by Priority Mail Express or by means at least as fast and reliable as Priority Mail Express at the following address of record for litigation counsel:

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