UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Chongqing HKC Optoelectronics Technology Co., Ltd.,

Petitioner

v.

138 East LCD Advancements Limited,

Patent Owner

Patent No. 7,116,390

Declaration of Carl Sechen, Ph.D.

HKC EXHIBIT 1002

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1. I, Professor Carl Sechen, make this declaration in connection with the proceeding identified above.

I. Introduction

2. I have been retained by counsel for Petitioner Chongqing HKC Optoelectronics Technology Co., Ltd. ("HKC"), as a technical expert in connection with the proceeding identified above. I submit this declaration in support of HKC.

3. I understand that this proceeding involves U.S. Patent No. 7,116,390 ("the '390 patent"), and I have been asked to provide my opinions as to the patentability of the claims of the '390 patent. I have been informed that a copy of the '390 patent is attached to the petition as Exhibit 1001.

4. This declaration sets forth the opinions that I have formed in this proceeding based on my study of the evidence, my understanding as an expert in the field, and my education, training, research, knowledge, and personal and professional experience.

5. I am being compensated for my time at the rate of $400 per hour for my work. This compensation is not contingent in any way upon the nature of my findings, the presentation of my findings in testimony, or the outcoming of this proceeding.

6. In forming my opinions, in addition to any materials cited in this report, I have reviewed the following materials:

- U.S. Patent No. 7,116,390, issued to Murade, filed on May 25, 2004, issued on October 3, 2006 ("'390 patent") (Ex. 1001)

- Prosecution History for U.S. Patent No. 7,116,390 ("'390 FW") (Ex. 1004)

- Japanese Patent App. No. JP2002049052A, filed on August 3, 2000, published on February 15, 2002, and its accompanying translation ("*Muraide*") (Ex. 1005)

- Japanese Patent App. No. JP2002196311A, filed on December 22, 2000, published on July 12, 2002, and its accompanying translation ("*Sunao*") (Ex. 1006)

- U.S. Published Patent Application No. US20030174271A1, filed on January 27, 2003, published on September 18, 2003 ("*Fujikawa*") (Ex. 1007)

- U.S. Patent No. 6,262,702, filed on October 23, 1998, issued on July 17, 2001 ("*Murade II*") (Ex. 1008)

- U.S. Published Patent Application No. 20030063248A, filed on Sept. 6, 2002, published on April 3, 2003 ("*Komeno*") (Ex. 1009)

- U.S. Patent No. 6,433,767, filed on February 1, 1999, issued on August 13, 2002 ("*Murade III*") (Ex. 1010)

II. Expert Qualifications

7. Based upon my educational and work experience, I believe I am well qualified to serve as a technical expert in this matter.

8. I have been told that my curriculum vitae is attached as Exhibit 1003 to the petition.

9. I expect to testify further, if requested, regarding the subject matter set forth in this declaration.

10. I have been a Professor of Electrical Engineering for 36 years. Since

August 15, 2005 to the present, I have been a Professor of Electrical and Computer Engineering at the University of Texas at Dallas. From July 1992 to August 2005, I was a Professor of Electrical Engineering at the University of Washington. From July 1986 through June 1992, I was an Assistant and then Associate Professor of Electrical Engineering at Yale University. Over these years, my research has focused on the design and computer-aided design of digital and analog integrated circuits. I have taught numerous students how to design digital, analog, and mixed signal integrated circuits and printed circuit boards, as part of the design courses that I have offered. More information about my academic work can be found in my curriculum vitae, which I have been told is Exhibit 1003 to the Petition.

11. As a professor, I have developed and taught numerous courses, For example, several courses that teach VLSI integrated circuit design in great detail. I have taught these courses continuously for the past 25 years. I have taught Verilog design to undergraduate and graduate students at the University of Washington and at the University of Texas at Dallas since 2001.

12. I have also been involved in numerous research projects on digital and analog VLSI design. I have taught numerous graduate researchers how to design digital and analog integrated circuits. My digital and analog VLSI design research has been funded by many companies over the years, including Intel, AMD, Cadence, LSI Logic, and Texas Instruments. Texas Instruments funded my work

on H.264 video encoding for more than three years. My VLSI and memory design research has also been supported by governmental agencies such as DARPA and the National Science Foundation. I have authored or coauthored over 200 papers and one book, the majority of which concern digital and analog integrated circuit design, as well as computer-aided design. I have also designed, fabricated and tested numerous integrated circuits. I am a co-inventor on four issued patents directed to transistor and computational logic technologies. Three of the patents concern transistor-level programmable logic.

13. I earned a B.E.E. degree in Electrical Engineering from the University of Minnesota. After that, I went on to the Massachusetts Institute of Technology, where I earned an M.S. degree in Electrical Engineering. I was awarded a Ph.D. in electrical engineering from the University of California at Berkeley in 1986. More details about my education are set forth in my attached curriculum vitae. *See* Exhibit 1003.

14. I was elected a Fellow of the IEEE in 2002 for contributions to placement and routing of ASICs. IEEE stands for Institute of Electrical and Electronics Engineers, which is the leading professional association for electrical engineers. The Board of Directors of the IEEE awards the rank of "Fellow" to individuals with an extraordinary record of accomplishments in any of the IEEE fields of interest. The total number of IEEE members who can be named Fellows

in any one year cannot exceed one-tenth of one percent of the total voting IEEE membership.

15. I also received a Distinguished Teaching Award from the University of Texas at Dallas in 2008. I also received a highly unusual *second* Distinguished Teaching Award from the University of Texas at Dallas in 2014. In 2002, I also received the Outstanding Research Advisor Award from the Department of Electrical engineering at the University of Washington and the Best Project Award from the NSF Center for the Design of Digital and Analog ICs. I also received the Semiconductor Research Corporation's Inventor's Recognition Award in 2001 for the development of output prediction logic. I received the 1994 SRC Technical Excellence Award, and I also received the Semiconductor Research Corporation's 1988 SRC Inventor's Award. Additional honors and awards are set forth in my CV. *See* Exhibit 1003.

16. All of the opinions stated in this report are based on my own personal knowledge and professional judgment.

III. Overview of the ’390 Patent

17. I have reviewed the ’390 patent and based on my review understand the ’390 patent to describe the following.

A. The ’390 Patent

18. The ’390 patent is titled “Electro-optical device and electronic

apparatus comprising the same, " and issued on October 3, 2006. '390 patent, cover. The patent specifically states that electro-optical devices include liquid crystal devices ("LCDs"). '390 patent, col. 1:8-9.

19. The '390 patent relates an electro-optical device, such as a driving circuit built-in liquid crystal device, obtained by mounting peripheral driving circuits on an element substrate. '390 patent, col. 1:8-10. The '390 patent itself describes prior art devices as having a plurality of pixel portions for displaying images arranged in a matrix in an image display region. The pixels are driven and controlled by pixel electrodes and thin film transistors (TFT), which are arranged within the pixel portions and wiring lines, such as scanning lines, data lines, and capacitance lines. The patent recognizes that the prior art describes scanning line driving circuits and a data line driving circuit for driving the scanning lines that are mounted in a peripheral region on the same element substrate. Therefore, in general, various wiring lines, such as power source signal lines, clock signal lines, image signal lines, and control signal lines are planarly laid out in the peripheral region, which connect a plurality of external circuit connection terminals arranged along one side of the element substrate to the peripheral driving circuits. '390 patent, col. 1:14-32.

20. The '390 patent describes a particular arrangement of these well-known components that supposedly reduces the interference between the

components so that a smaller device can be made. ’390 patent, col. 1:33-40. As shown in Figures 1 and 4 of the ’390 patent, the patent describes a TFT array substrate 10 (shown in Figure 1 below), and main wiring lines 108, which include a counter electrode potential line LCCOM (shown in Figure 4 below as the outermost terminals 102, and the far outside wiring line 108). ’390 patent, col. 12:61-13:5.

Fig. 1

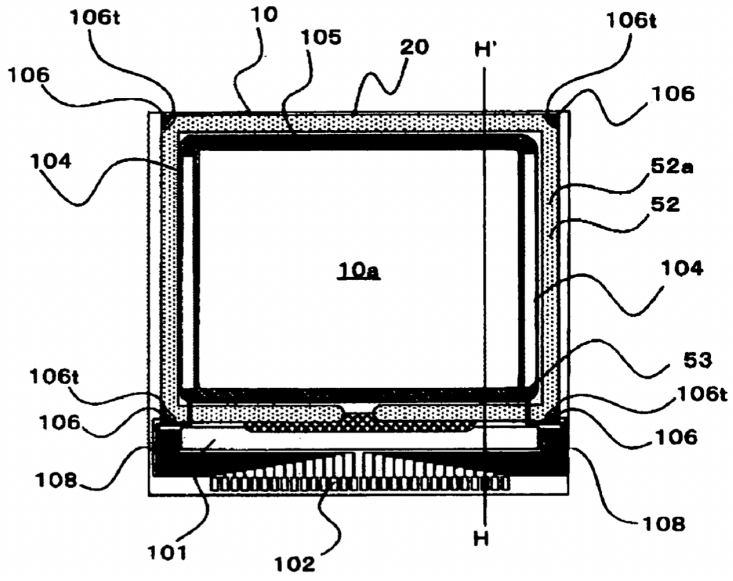
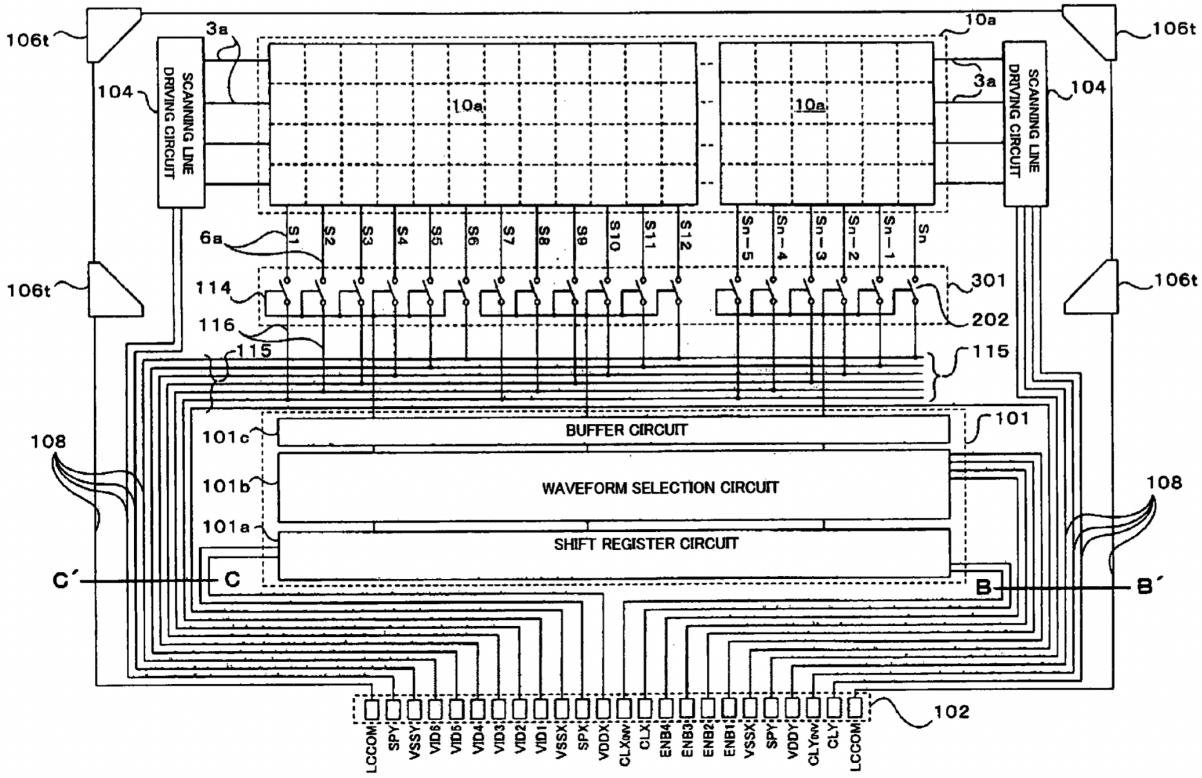


Fig. 4



21. The ’390 patent describes FIGS. 1 and 2 as disclosing an electro-optical device in which “a TFT array substrate 10 and a counter substrate 20 are arranged to face each other. A liquid crystal layer 50 is sealed between the TFT array substrate 10 and the counter substrate 20. The TFT array substrate 10 and the counter substrate 20 are attached to each other by a seal material 52 provided in a seal region 52 a positioned around an image display region 10a.” ’390 patent, col. 9:13-20.

22. In reference to Figure 1, the ’390 patent further describes a “peripheral region, the region positioned outside the seal region 52 a can include a data line driving circuit 101 and external circuit connection terminals 102, which

are provided along one side (that is, the lower side in FIG. 1) of the TFT array substrate 10. Scanning line driving circuits 104 are provided along two sides (that is, the left and right sides in FIG. 1) adjacent to the one side so as to be covered with the frame light-shielding film 53. Also, in order to connect with each other the two scanning line driving circuits 104 provided on both sides of the image display region 10 a, along the remaining one side (that is, the upper side in FIG. 1) of the TFT array substrate 10, a plurality of wiring lines 105 are provided so as to be covered with the frame light-shielding film 53." '390 patent, col. 9:46-60.

23. The patent further describes "a plurality of main wiring lines 108 each having one end connected to each of the external circuit connection terminals 102 are provided in the peripheral region. The other ends of the main wiring lines 108 are connected to the data line driving circuit 101 and the scanning line driving circuits 104." '390 patent, col. 9:61-67.

24. The patent describes and Figure 1 depicts "upper and lower conduction terminals 106t connected to one counter electrode potential line which is one of the main wiring lines 108 planarly laid out on the TFT array substrate 10 are provided in the vicinity of the four corners of the TFT array substrate 10. The upper and lower conduction materials 106 are arranged on the upper and lower conduction terminals 106t. The upper and lower conduction materials 106 contact the four corners of the counter electrode 21 and supply the counter electrode

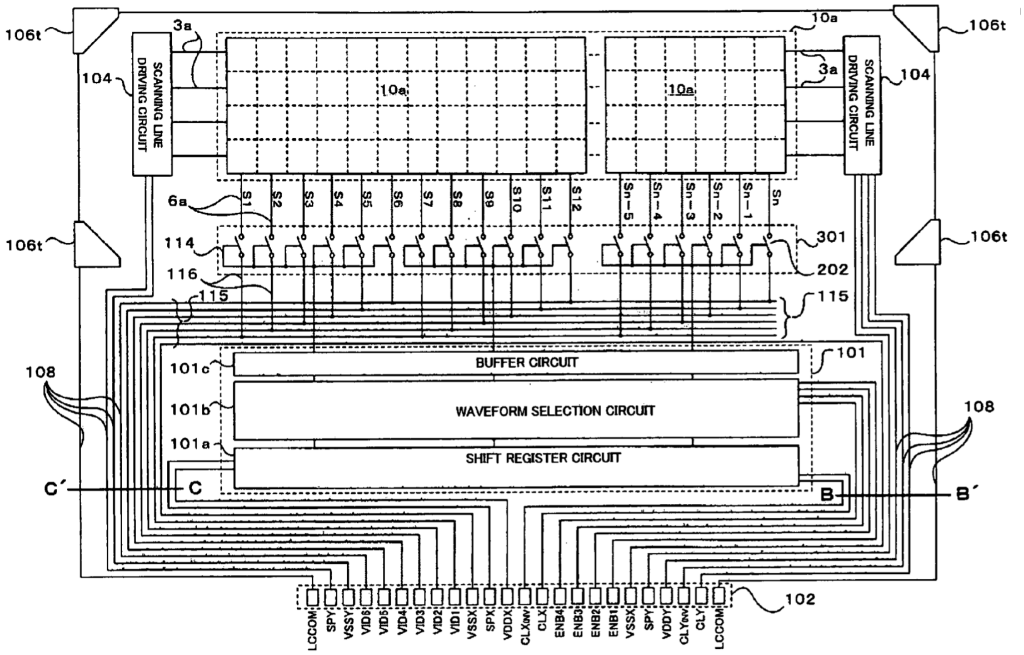
potential from the external circuit connection terminals 102 through the main wiring lines 108 to the counter electrode 21." '390 patent, col. 10:14-25.

25. Figure 4 of the '390 patent (below), further illustrates the arrangement of the counter electrode potential lines LCCOM in relation to the scanning line driving circuits 104 and conduction terminals. As described by the '390 patent, "the data line driving circuit 101 and sampling circuits 301, can supply image signals to the data lines 6 a, and the scanning line driving circuits 104, can supply scanning signals to the scanning lines 3 a are formed as driving circuits of the electro-optical device on the TFT array substrate 10. Also, the external circuit connection terminals 102 including a plurality of terminals for inputting various signals supplied to the driving circuits from external control circuits are formed along one side of the TFT array substrate 10 (refer to FIG. 1). The main wiring lines 108 are provided from the external circuit connection terminals 102." '390 patent, col. 11:29-40. The arrangement of these lines and connections are shown in Figure 4 of the patent below.

26. The patent further describes that "on the TFT array substrate 10, counter electrode potential line LLCCOM which is one of the main wiring lines 108 passes through the four corners of the TFT array substrate 10 while being connected to the upper and lower conduction terminals 106 t. A predetermined electric potential is supplied to the counter electrodes 21 through the upper and

lower conduction materials 106, the upper and lower conduction terminals 106 t, and the counter electrode potential line LLCCOM. It is possible to drive the liquid crystal interposed between the two electrodes, that is, the pixel electrode 9 a and the counter electrode 21 as mentioned above by supplying the electric potential." '390 patent, col. 12:61-13:5. These elements are also shown in Figure 4 below.

27. As further shown in Figure 4 below, the scanning line driving circuits 104 are arranged to be closer to the center of the TFT array substrate 10 than the counter electrode potential lines LCCOM provided along the edges of the TFT array substrate 10. Counter electrode potential line LCCOM passes through the four corners of the TFT array substrate 10 while being connected to the upper and lower conduction terminals 106t and surrounds the image display region 10a and various driving circuits. '390 patent, col. 13:6-19; Figs. 1, 4.



At the bottom of the figure, the outside most line is marked "LCCOM," which is depicted as running outside of the other lines and connecting to the conduction terminals 106t.

28. Thus, the '390 patent describes a standard electro-optical device, such as an LCD, in which driving circuits are mounted in a peripheral region on a substrate. The patent describes a particular arrangement of the peripheral driving circuits and standard wiring lines used in such devices which purportedly reduces the mutual interference among the lines and thereby allows the device to be smaller in size.

29. The patent claims recite the basic, well-known configuration of an electro-optical device, such as an LCD, that has a plurality of pixel portions provided in an image display region on an element substrate. The claimed device includes a region peripheral to the image display region that has a plurality of external circuit connection terminals, which are coupled by a plurality of main wiring lines to the peripheral driving circuits. In addition, the claimed device has a counter electrode provided in a peripheral region on a counter substrate that is arranged to face the element substrate, and a counter electrode potential line that supplies counter electrode potential to the counter electrode. The device must also include upper and lower conduction terminals in the peripheral region on the element substrate that are connected to the counter electrode potential line. The

plurality of main wiring lines must be made of the same conductive film and be planarly laid out so as not to intersect each other in the peripheral region. Finally, the counter electrode potential line must be closest to the edges of the element substrate, among the plurality of main wiring lines.

B. Prosecution History of the '390 Patent

30. The application that resulted the '390 patent was filed on May 25, 2004. '390 FW-0532.

31. Original claim 1 recited as follows:

> An electro-optical device, comprising:
>
> a plurality of pixel portions provided in an image display region on an element substrate;
>
> in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,
>
> the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region.

'390 FW-0279.

32. During examination, the pending claims were rejected over *Muraide* or *Muraide* in combination with *Yamazaki* (U.S Patent No. 6,011,607). '390 FW-0107-112. For example, in relation to original claim 1, the examiner found:

> Muraide discloses an electro-optical device, comprising: a plurality of pixel portions provided in an image display region (10a) on an element substrate (10); in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals (102), a plurality of main wiring lines (400) each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits (101 or 104) coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines, the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region, [see figs. 4 & 11].

'390 FW-0107-108. In addition, in regard to then pending claims 4 and 5, the examiner found:

> Muraide discloses the electro-optical device according to claim 1, further comprising a counter electrode provided in the peripheral region on a counter substrate (20) that is arranged to face the element substrate (10); and upper and lower conduction terminals (106) that are provide in the peripheral region on the element substrate, in order to connect a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is a at least one of the plurality of main wiring lines, [see figs. 3 & 4].

'390 FW-0110-111. The examiner further determined that Muraide anticipated claims 2, 3, 10, 11 and 13. '390 FW-0108-109.

33. The examiner also determined that Muraide disclosed many of the limitations of original claim 4 that the applicant added to claim 1 in a later amendment. For example, in regard to original claims 4 and 5 the examiner determined that:

> Muraide discloses the electro-optical device according to claim 1, further comprising: a counter electrode provided in the peripheral region on a counter substrate (20) that is arranged to face the element substrate (10); and upper and lower conduction terminals (106) that are provided in the peripheral region on the element substrate, in order to connect a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, [see figs. 3 & 4].

'390 FW-0110. In other words, *Muraide* disclosed essentially all limitations of the original claims.

34. The examiner noted that: "Muraide lacks disclosure of the counter electrode potential line to the plurality of main wiring lines being positioned near edges of the element substrate in the peripheral region, and the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower connection terminals and the counter electrode potential line in the peripheral region." '390 FW-0110.

35. In response, applicant amended independent claim 1 to add further limitations regarding the counter electrode, counter electrode potential line and upper and lower conduction terminals. '390 FW-0039 (mark-up of claim 1). In particular:

> a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;
>
> a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

> upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

'390 FW-0039. These limitations had been in original dependent claim 4. '390 FW-0279-280.

36. The applicant added one entirely new limitation in response to the examiner's rejection. Claim 1 gained a final limitation of: "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." '390 FW-0039.

37. Based on this amendment, the examiner allowed the claims. '390 FW-0006-0008.

IV. Person Of Ordinary Skill In The Art

38. I understand that patentability must be analyzed from the perspective of a hypothetical person of ordinary skill in the art in the same field as the patent at the time of the invention. I understand that "person of ordinary skill in the art" (POSITA), "person of ordinary skill," "skilled artisan," or a similar phrase are used to denote this hypothetical person of ordinary skill.

39. I understand a POSITA is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I further understand that factors that may be considered in determining the level of ordinary skill in the art may include: (1) type of problems encountered in the art; (2) prior art solutions to

those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) educational level of active workers in the field. I further understand that a POSITA is also a person of ordinary creativity, not an automaton. I understand that a POSITA will be able to fit the teachings of multiple patents together like pieces of a puzzle.

40. Based on my experience in teaching, researching, and consulting, and considering the factors identified in the preceding paragraphs, my opinion is that a person of ordinary skill in the art at the time of the alleged invention of the ’390 patent would have either a bachelor’s degree in electrical or computer engineering or an equivalent area with three years of experience in the field of display technology or a master’s degree with one year of experience in the field of display technology.

41. As of the filing date of the application that led to the ’390 patent and its foreign priority applications, I was at least a person of ordinary skill in the art.

V. Claim Construction

42. I have been informed that in an IPR, claim terms should now be construed under the same standard applied in district court cases, which I am told is sometimes referred to as the *Phillips* standard. I have applied that standard here, which I understand involves construing the terms based on how one of ordinary skill in the art would have understood the terms as of the claims' priority date in

light of the intrinsic record, including the claim language, patent specification, and prosecution history. I also understand that extrinsic evidence, such as dictionaries, may be relied on when construing the claims. However, I understand that extrinsic evidence is generally less significant to determining the legally operative meaning of a claim, especially where the intrinsic record demonstrates the scope of the claim.

43. Based on my review of the claims, patent specification, prosecution history, and certain extrinsic evidence discussed in this declaration, I do not see a need to articulate a specific construction for any of the claim terms beyond any discussion that appears in the analysis below. I understand that the Patent Owner has not provided any proposed claim construction for the claims.

VI. The Challenged Claims Are Unpatentable

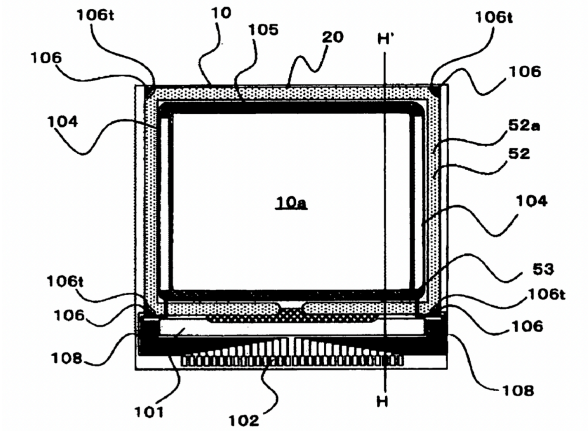
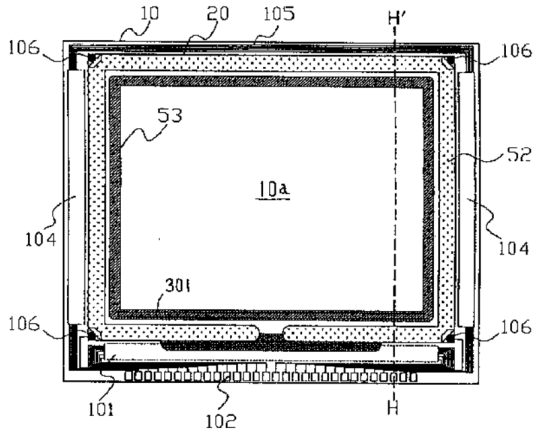
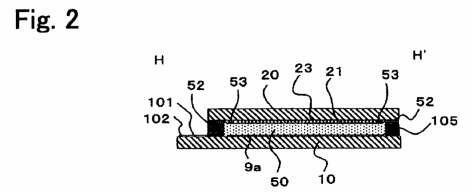
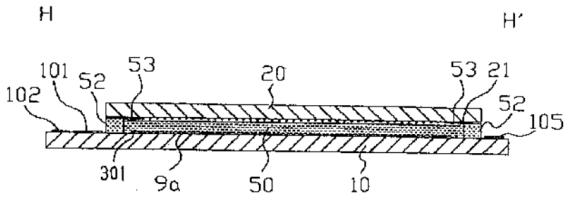
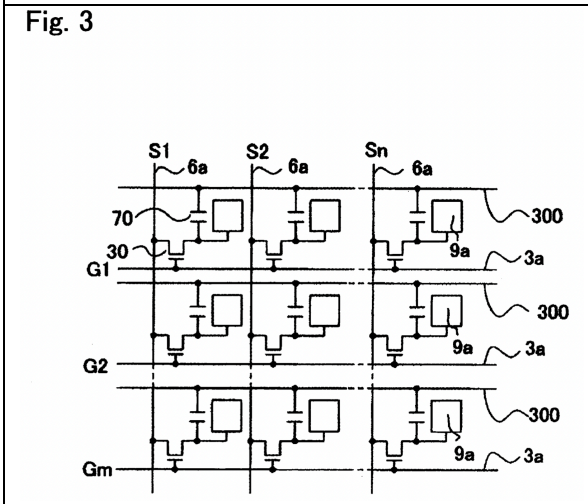
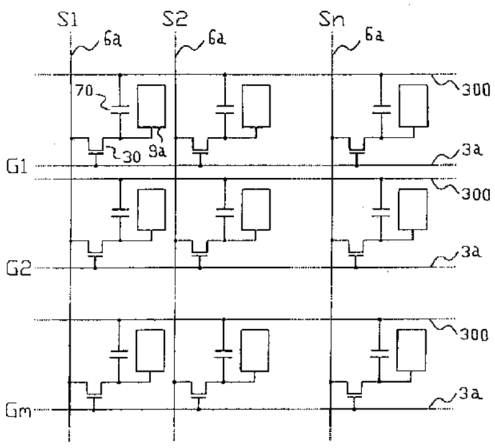
A. Overview of the Prior Art

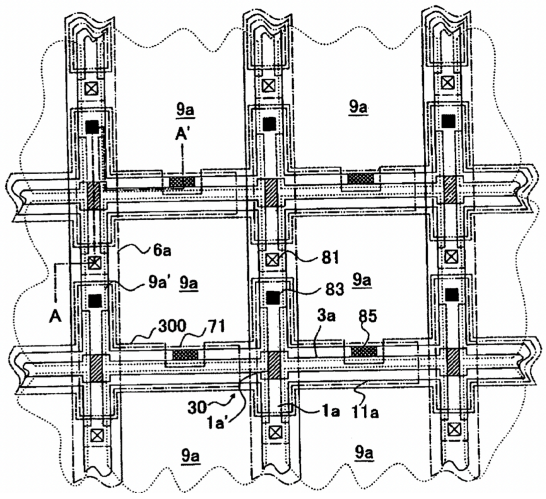
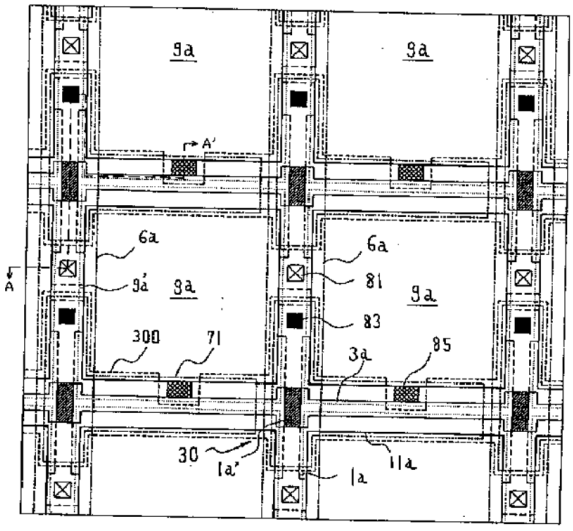
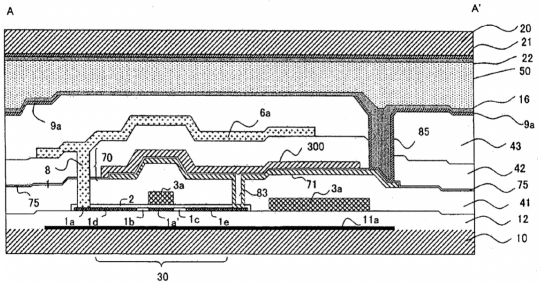
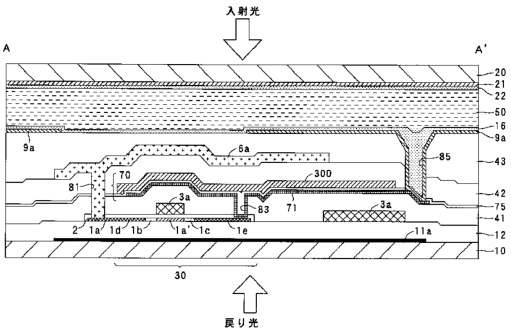
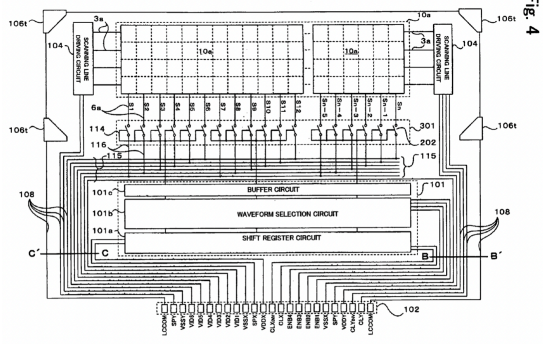
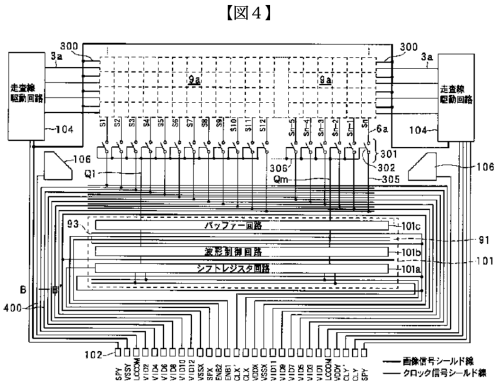
1. *Muraide*

44. *Muraide* describes an electro-optical device, such as an LCD, in which "data lines are driven in accordance with image signals, clock signals, and the like by peripheral circuits such as data line driving circuits and sampling circuits provided in peripheral regions on a TFT array substrate." *Muraide*, ¶[0001]. *Muraide* discloses a device with a pixel electrode (9a), a TFT(thin film transistor 30) connected to the pixel electrode (9a) and a capacitive line (300) on a picture display region of a TFT array substrate (10) and is further provided with a

data line (6a) and a scanning line (3a) connected to the TFT. *Muraide*, abstract. In the peripheral region, a peripheral circuit including a circuit related to data line driving, a signal line (400) connected to the peripheral circuit and made of a same film as the capacitive line, and a shield (401a) electrically screening the signal line (400) from at least one direction and formed from a same film as the data line are provided. *Muraide*, abstract.

45. Notably, the figures of the ’390 patent and *Muraide* are almost identical in many instances and often share the same element numbering. As such, they clearly disclose virtually the same electro-optical device as shown in the Table below.

’390 Patent Figures	*Muraide* Figures
Fig. 1  	【図１１】 
Fig. 2  	【図１２】 
Fig. 3  	【図１】 

’390 Patent Figures	*Muraide* Figures
Fig. 6 	【図２】 
Fig. 7 	【図３】 
Fig. 4 	【図４】 

2. *Sunao*

46. *Sunao* discloses a liquid crystal display device having a structure in which a liquid crystal layer is sandwiched between a matrix array substrate 2 and a counter substrate 3. A counter electrode 7 is formed on a whole surface of the counter substrate 3 and a metal cover frame 6 is arranged at an outer periphery of the liquid crystal display device. *Sunao*, abstract.

3. *Fujikawa*

47. *Fujikawa* discloses an electrooptic device in which a region that does not directly contribute to the display can be narrowed by improving the layout of peripheral circuits. *Fujikawa*, abstract. *Fujikawa* discloses an active matrix liquid crystal device using a thin-film transistor (TFT) as a pixel switching element, and a TFT array substrate 10 having pixel electrodes and pixel-switching TFTs formed on a transparent substrate. *Fujikawa* discloses a counter substrate 20 having counter electrodes formed on a transparent substrate that are bonded with a sealing material 107 with a predetermined space therebetween, and liquid crystal serving as an electrooptic substance being held between the substrates. *Fujikawa*, ¶¶[0004], [0046].

4. *Murade II*

48. *Murade II* discloses a liquid crystal apparatus, which includes a liquid crystal layer disposed between two substrates, pixel electrodes formed in a matrix fashion on a substrate, and TFTs serving for switching and controlling the pixel

electrodes for suppressing the intrusion of high-frequency clock noise into an image signal. Image signal lines extend on the substrate at both sides of a data line driving circuit. The image signal lines are electrically shielded from clock signal lines, for example, by shielding lines formed on the substrate, and maintained at a constant voltage. *Murade II*, abstract.

5. *Komeno*

49. *Komeno* discloses a liquid crystal display device referred to as a TN type, in which a display region is formed by sealing liquid crystal in a gap defined by laminating a first substrate and a second substrate which constitute a pair of substrates. *Komeno*, ¶[0004]. *Komeno* discloses that on the display region of the first substrate is a matrix consisting of a large number of data lines which are crossed at a right angle by scanning lines, and a pixel is formed in a region surrounded by a pair of data lines and a pair of scanning lines. *Komeno*, ¶[0004]. *Komeno* further discloses a second substrate that includes counter electrodes which face opposite the pixel electrodes and are used to apply an electric field to the liquid crystal of the pixel. *Komeno*, ¶[0005]. *Komeno* further discloses that each pixel is formed of the liquid crystal which is sandwiched between the pixel electrode provided to the first substrate and the counter electrode provided to the second substrate. *Komeno*, ¶[0005].

6. *Murade III*

50. *Murade III* discloses an electro-optical apparatus, such as a liquid crystal apparatus, that has a built-in peripheral circuit in which the resistance of input/output wirings in the peripheral circuit is reduced by effectively using thin films forming pixels. The liquid crystal apparatus includes a liquid crystal layer disposed between a pair of substrates and pixel electrodes formed in a matrix fashion on a TFT array substrate. *Murade III* (abstract). *Murade III* discloses a "conventional liquid crystal apparatus having built-in peripheral circuits, peripheral circuits such as a data line driving circuit, a scanning line driving circuit, and a sampling circuit are formed on a TFT array substrate, which is one of two substrates between which a liquid crystal is disposed." *Murade III,* col. 1:21-26.

B. Ground 1: *Muraide* in Combination with *Sunao* or *Komeno* Renders Obvious Claims 1-11 and 13.

1. Claim 1

An electro-optical device, comprising:

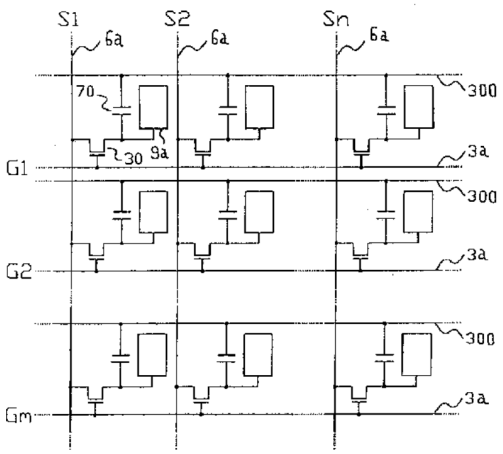
51. A POSITA would understand that *Muraide* relates to electro-optical devices. In fact, *Muraide* specifically identifies its invention as relating to "electro-optical devices such as liquid crystal devices." *Muraide*, ¶[0001].

52. Accordingly, it is my opinion that *Muraide* teaches the preamble of claim 1.

a plurality of pixel portions provided in an image display region on an element substrate:

53. A POSITA would understand that *Muraide* discloses the well-known, basic elements of an electro-optical device, such as an LCD display. *Muraide* LCD displays that consist of pixel portions, which are the portions corresponding to the liquid crystals that respond to electrical signals and enable a display to present an image. For example, *Muraide* Figure 1 shows an arrangement of pixels on an element substate.

【図１】

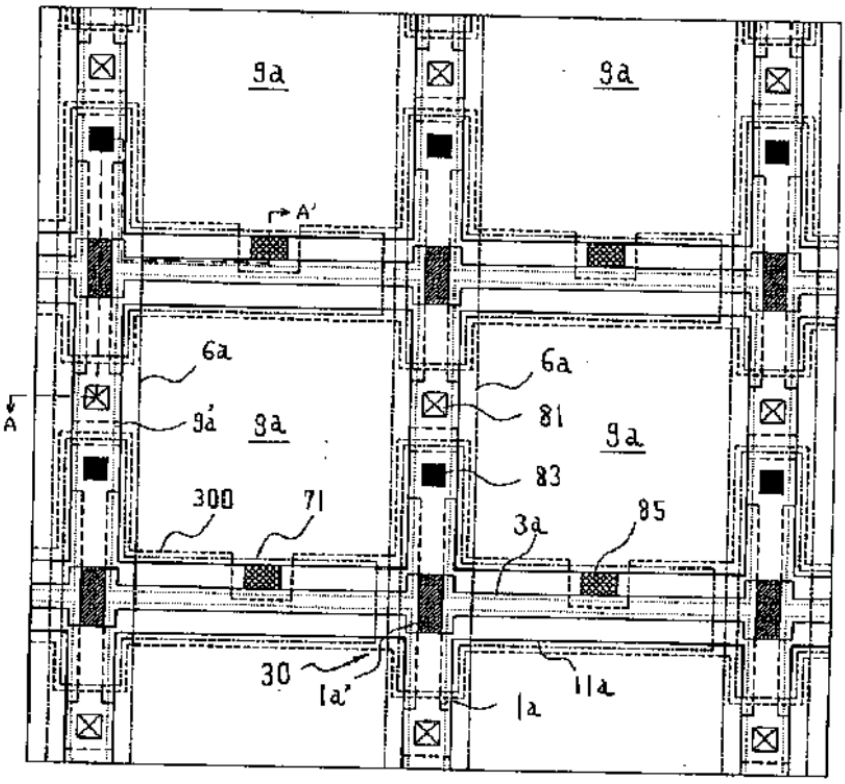


54. *Muraide* discloses pixel electrodes 9a, and TFTs 30 for controlling switching of the pixel electrodes 9a, are formed in a matrix that corresponds to an image display region on an element substrate of the electro-optical device. *Muraide*, ¶[0051], Figs. 1, 2, 4. *Muraide* teaches that: "In FIG. 2, a plurality of transparent pixel electrodes 9a (outline of which is shown by dotted line portions 9a') are provided in a matrix on the TFT array substrate of the electro-optical

device, and the data lines 6a and the scanning lines 3a are provided along the vertical and horizontal boundaries of the pixel electrodes 9a." *Muraide*, ¶[0051].

Muraide Figure 2 is shown below.

【図２】



55. Accordingly, it is my opinion that *Muraide* teaches this limitation of claim 1.

in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

56. A POSITA would understand *Muraide* to disclose a peripheral region of an image display region as having a variety of circuits and connecting wiring. For example, *Muraide* Figure 4 (below), depicts an element substrate with an image display region and a peripheral region thereto.

57. *Muraide* discloses "In FIG. 4, a data line driving circuit 101, a scanning line driving circuit 104, and a sampling circuit 301, as examples of peripheral circuits are formed in a peripheral region located around an image display region on a TFT array substrate of a liquid crystal device." *Muraide*, ¶[0078]. A POSITA would understand these peripheral circuits to be examples of peripheral driving circuits driving the pixel portions.

58. *Muraide* describes how the pixel portions are driven as:

> The scan line drive circuit 104 starts a built-in shift register circuit according to inputting of a start signal SPY using a negative power source VSSY and a positive power source VDDY configured for the scan line drive circuit 104 as power sources, which are supplied from an external control circuit via the external input terminals 102, the wirings 400 (VSSY), and the wirings 400 (VDDY). Then, the scanning signals are applied to the scanning lines 3a line-sequentially in a pulsed manner at predetermined timings based on

> a reference clock signal CLY for the built-in shift register circuit of the scanning line drive circuit 104 and an inverted clock signal CLY' of the reference clock signal CLY, which are supplied via the external input terminals 102, the wirings 400 (CLY), and the wirings 400 (CLY').

Muraide, ¶[0078]. Similarly, *Muraide* describes the role of the data-line driving circuits:

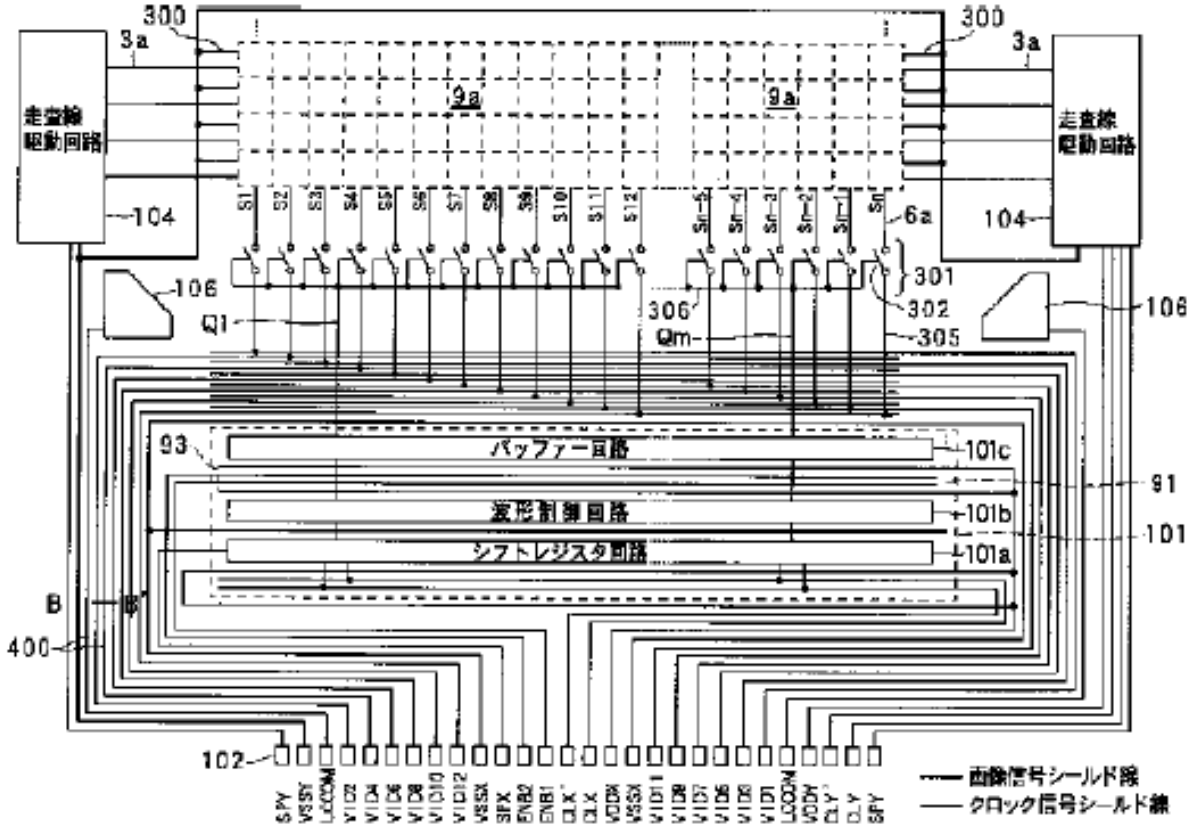
> The data line drive circuit 101 starts a built-in shift register circuit according to inputting of a start signal SPX using a negative power source VSSX and a positive power source VDDX configured for the data line drive circuit 101 as power sources, which are supplied from an external control circuit via the external input terminals 102 and the signal wirings 400 (VSSX) and the wiring 400s (VDDX).Then, based on the reference clock signals CLX and an inverted clock signals CLX' of the reference clock signal CLX configured for the internal shift register circuit of the data line drive circuit 101 and supplied via the external input terminals 102, the wirings 400 (CLX), and the wirings 400 (CLX'), for each of image signals VID1 to VID12 which are serial-parallel converted into, for example, 12 parallel signals supplied via the external input terminals 102 and the wiring 400 (VID1) to the wiring 400 (VID12), the sampling circuit drive signals Qm (m=1, 2,...) are supplied to the sampling circuit 301 via a sampling circuit drive signal lines 306 at predetermined timings in accordance with the timings at which the scanning line drive circuit 104 applies the scanning signals for each data line.

Muraide, ¶[0079].

59. *Muraide* discloses terminals 102 (along the bottom edge of the substrate of Figure 4), which are a plurality of external connection terminals. Figure 4 shows wiring lines coupled to the external connection terminals 102 at one end and coupled to peripheral circuits, including data line driving circuit 101,

and scanning line driving circuit 104, at the other. *Muraide* teaches that the peripheral driving circuits drive the pixel portions of the image display region based on electric signals supplied from the external circuit connection terminals. *Muraide*, ¶¶[0001], [0078-80]. *Muraide* Figure 4 is shown below.

【図４】

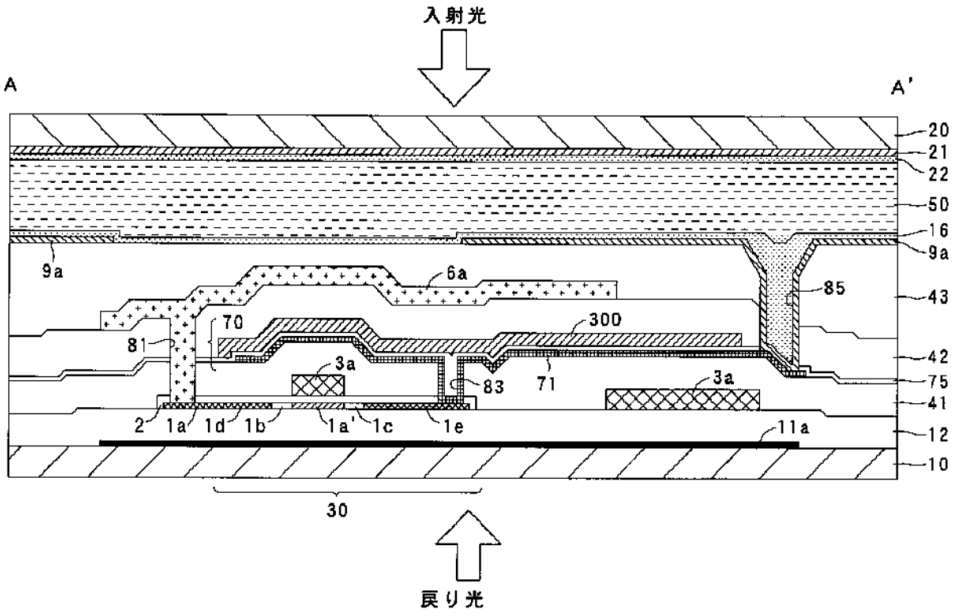


a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

60. A POSITA would understand *Muraide* to disclose a counter electrode on a counter substrate. *Muraide* specifically describes its device as including "a

counter electrode facing the plurality of pixel electrodes is … on a counter substrate facing the substrate with an electro-optical material provided therebetween." *Muraide*, ¶[0041]. Thus, *Muraide* discloses a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate. *Muraide* Figure 3 is shown below.

【図３】



61. As shown in *Muraide* Figure 3, the depiction of the counter substrate 20 and counter electrode 21 is essentially identical to their depiction in Figure 7 of the '390 patent.

62. Accordingly, it is my opinion that *Muraide* teaches this limitation of claim 1.

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

63. A POSITA would understand *Muraide* to teach a counter electrode potential line being connected to the counter electrode. *Muraide* describes that a constant potential source may be a constant potential supplied to the counter electrode 21 of the counter substrate 20. *Muraide*, ¶[0061]. For example, as shown in Figures 3 and 4 of *Muriade*, "vertical conductive terminals 106 for electrically conducting the TFT array substrate 1 and the counter electrode 21 on the counter substrate 20 side (see FIG. 3) are provided at four corners of the image display area (in FIG. 4, 2 corners of 4 are shown).The vertical conduction terminal 106 is supplied via the external input terminal 102 and the wiring 400 (LCCOM)." *Muraide*, ¶[0085].

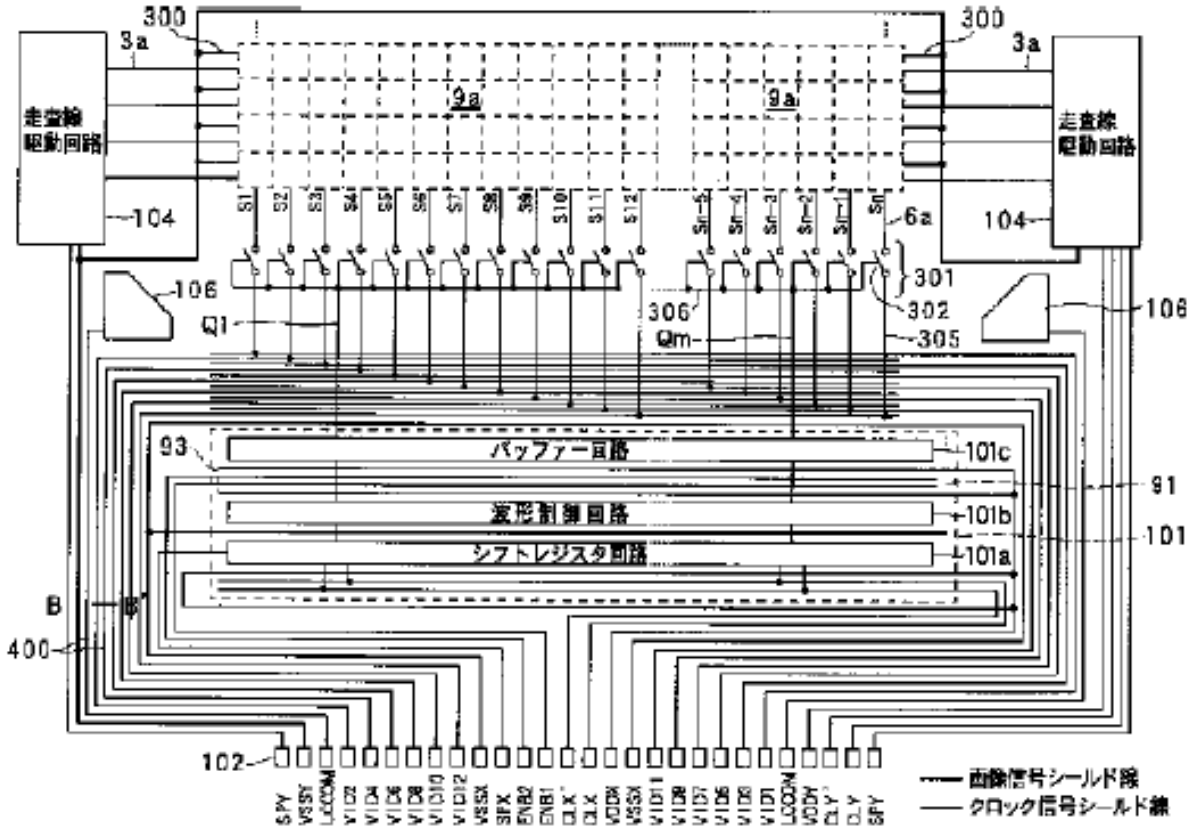
64. *Muraide* describes vertical conductive terminals 106 that electrically couple the TFT array substrate 1 and the counter electrode 21 on the counter substrate 20. *Muraide*, Figs. 3, 4. *Muraide* discloses a counter electrode potential line, wiring 400 (LCCOM), that supplies potential from the external input terminal 102 to the vertical conduction terminal 106 and then to the counter electrode 21 on the counter substrate 20. *Muraide*, ¶[0085]; Fig. 4.

65. Accordingly, it is my opinion that *Muraide* teaches this limitation of claim 1.

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

66. A POSITA would understand *Muraide* to teach upper and lower conduction terminals that are connected to the counter electrode potential line. In *Muraide*, the vertical conduction terminals 106 are provided at the four corners of the image display area on the array substrate 1, and the vertical conduction terminal 106 is supplied via the external input terminal 102 and the wiring 400 (LCCOM). *Muraide*, ¶[0085], Fig. 4. *Muraide* Figure 4 is shown below.

【図４】

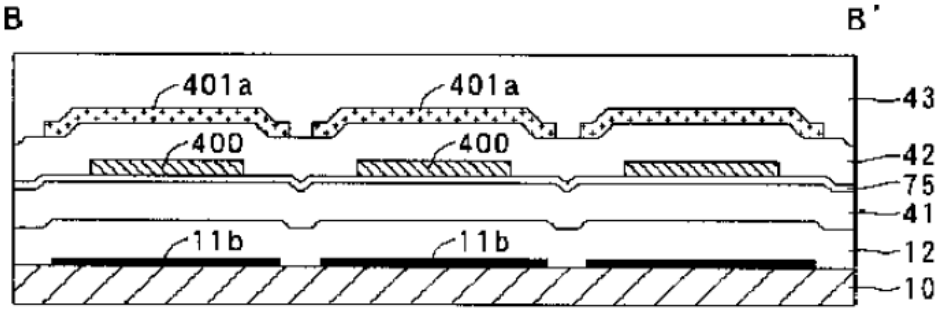


67. Accordingly, it is my opinion that *Muraide* teaches this limitation of claim 1.

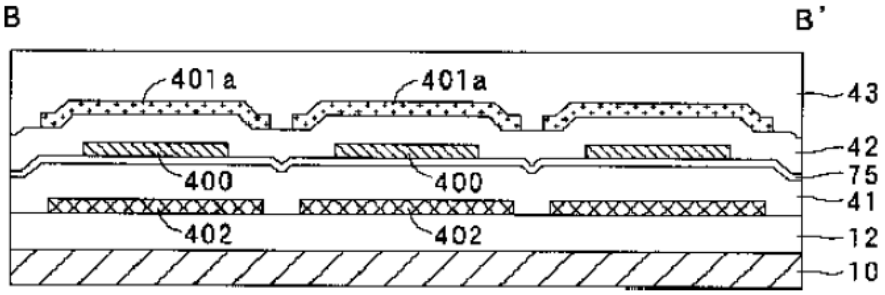
> **the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and**

68. A POSITA would understand *Muraide* to teach main wiring lines made out of a same conductive material that are laid out so that they do not intersect in the peripheral region. *Muraide* discloses main wiring lines, such as "the wirings 400 (VID1) to 400 (VID12)" that are image signal lines and made of the same conductive film as the capacitance lines 300 in the image display region. *Muraide*, ¶[0087]. *Muraide* teaches that the plurality of wiring lines are laid out in a zig-zag pattern so they do not intersect each other in the peripheral region. *Muraide*, Fig. 7, Fig. 8; Fig. 4 (above).

【図７】



【図８】



69. Accordingly, it is my opinion that *Muraide* teaches this limitation of claim 1.

> **the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.**

70. A POSITA would understand *Muraide* to render obvious this claim limitation as the determination of the location of the counter electrode potential line is a mere design choice. *Muraide* Figure 4 depicts the counter electrode potential line, wiring 400 (LCCOM), that supplies potential from the external input terminal 102 to the vertical conduction terminal 106, as being located nearer to the center of the substrate with respect to the scanning line drive circuit 104. The other obvious design choice is to locate the counter electrode potential line and conduction pads nearer to the edge of the substrate with respect to the scanning line drive circuit. This is a basic design choice that would not change any properties or characteristics of the wiring layout.

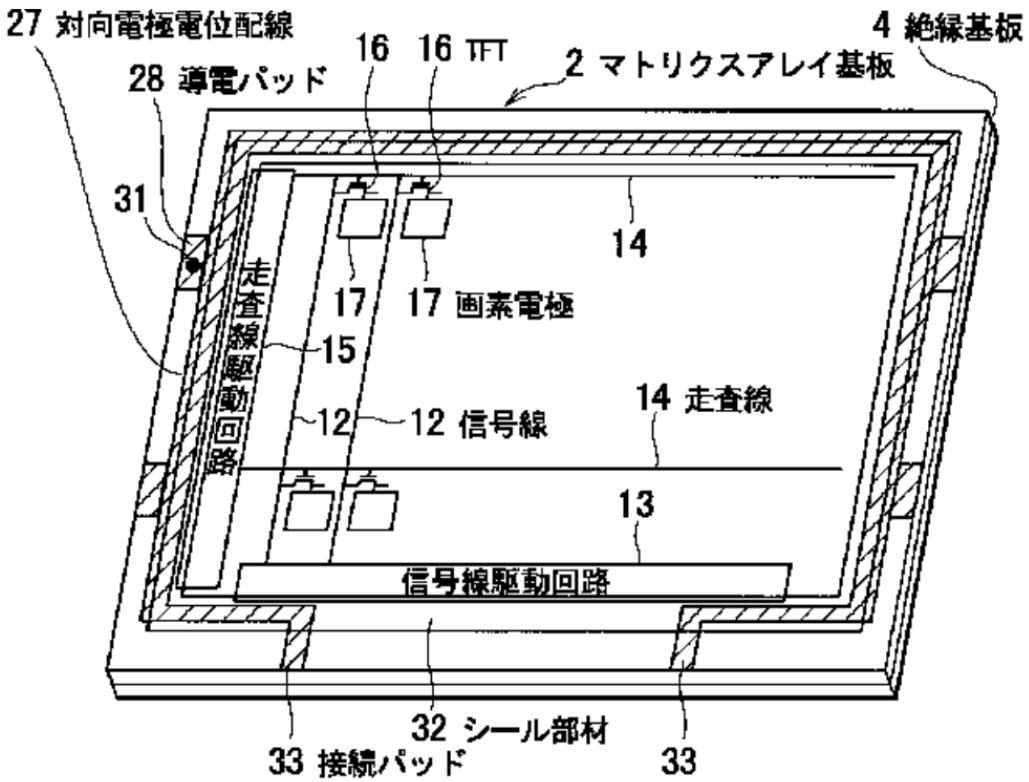
71. Alternatively, a POSITA would understand *Sunao* to disclose a counter electrode potential line that has been designed to run along the outer edge of an array substrate. *Sunao* discloses an LCD device with a matrix array substrate 2. The array substrate 2 has a plurality of signal lines 12 arranged in parallel on a transparent insulating substrate 4, and a plurality of scanning lines 14 arranged in parallel to intersect the plurality of signal lines 12 at right angles. *Sunao*, ¶[0013]. *Sunao* further discloses a signal line driving circuit 13 that is electrically connected to one end of signal line 12 for applying a video signal to the signal line 12, and a scanning line driving circuit 15 that is electrically connected to one end of the scanning line 14 for applying a scanning signal to the scanning line 14. *Sunao*, ¶[0014].

72. *Sunao* then discloses its device has a counter electrode potential line being closest to edges of the element substrate. *Sunao* describes conductive pads 28 and counter electrode potential wirings 27 (*e.g.*, the counter electrode potential line) for applying a potential to the counter electrode 7 are provided in the peripheral portion of the display region 11 on an insulating substrate 4. *Sunao*, ¶[0016]; Fig. 3. In particular, *Sunao* discloses "A conductive pad 28 for applying a potential to the counter electrode 7 and a counter electrode potential wiring 27 are provided in a peripheral portion of the display region 11 on the insulating substrate 4. The counter electrode potential wiring 27 is formed in a same process as the

signal line 12 and the scanning line 14." *Sunao*, ¶[0016].

73. Figure 3 of *Sunao* (shown below) depicts counter electrode potential line 27 being nearest to the edges of the element substrate of the main wiring lines. *Sunao* further discloses a "predetermined counter potential is supplied to the counter electrode potential wiring 27 from the outside from an external PCB, not shown, through the connection pad 33." *Sunao*, ¶[0016].

【図３】



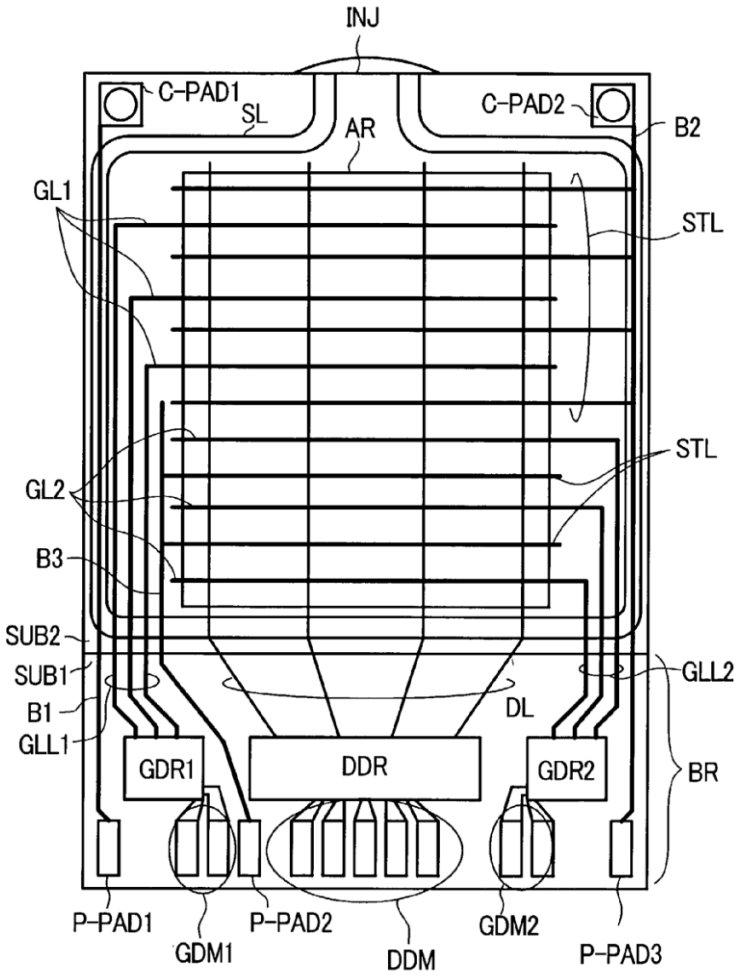
74. A POSITA would have found it obvious to combine *Muraide* and *Sunao*. Specifically, a POSITA would have found it obvious to implement

Sunao's placement of the counter electrode potential line as closest to edges of the element substrate with *Muraide's* display device. *Id*. A POSITA would have been motivated to combine *Sunao's* placement with *Muraide's* display device in order to further isolate the electrode potential line from the other wirings and the display to reduce interference and potentially shrink the size of its device. Further, as both *Muraide* and *Sunao* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Sunao's* placement of the counter electrode potential line as closest to edges of the element substrate with *Muraide's* display device. Finally, as both references relate to LCDs and describe similar functions combining the design of *Sunao* into *Muraide's* display device would have yielded predictable results. *Id*.

75. Alternatively, a POSITA would understand *Komeno* to disclose a counter electrode potential line that has been designed to run along the outer edge of an array substrate. *Komeno* discloses a liquid crystal display device referred to as a TN type, in which a display region is formed by sealing liquid crystal in a gap defined by laminating a first substrate and a second substrate which constitute a pair of substrates. *Komeno*, ¶[0004]. In regard to the two substrates, *Komeno* describes how the second substrate (SUB 2) has counter electrodes that face opposite the pixel electrodes on the first substrate. *Komeno* discloses feeding pads P-PAD1, P-PAD3 which are formed on the driving circuit mounting region. The

feeding pads are external terminals that provide electricity via lines B1, B2 to the counter electrode connection pads C-PAD1, C-PAD2. The counter electrode connection pads then supply power to the counter electrodes. *Komeno*, ¶[0108]. As shown in Figure 1 of *Komeno* (below), of the main wiring lines, wiring lines B1, B2 are located closest to the edges of the element substrate SUB1.

FIG. 1



76. A POSITA would have found it obvious to combine *Muraide* and *Komeno*. Specifically, a POSITA would have found it obvious to implement

Komeno's placement of the counter electrode potential line as closest to edges of the element substrate with *Muraide's* display device. *Id*. A POSITA would have been motivated to combine *Komeno's* placement of the counter electrode potential line with *Muraide's* display device in order to further isolate the electrode potential line from the other wirings and the display area. *Id*. This combination would have allowed the device of *Muraide* to potentially further miniaturize. Further, as both *Muraide* and *Komeno* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Komeno's* teachings with *Muraide's* display device. Finally, as both references relate to LCDs and describe similar functions combining the design of *Komeno* into *Muraide's* display device would have yielded predictable results. *Id*.

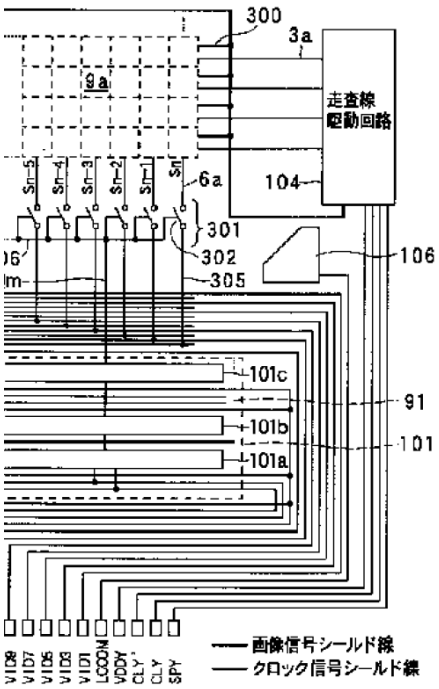
77. Accordingly, it is my opinion that *Muraide* in combination with *Sunao* or *Komeno* teaches and renders obvious this limitation of claim 1.

2. Claim 2

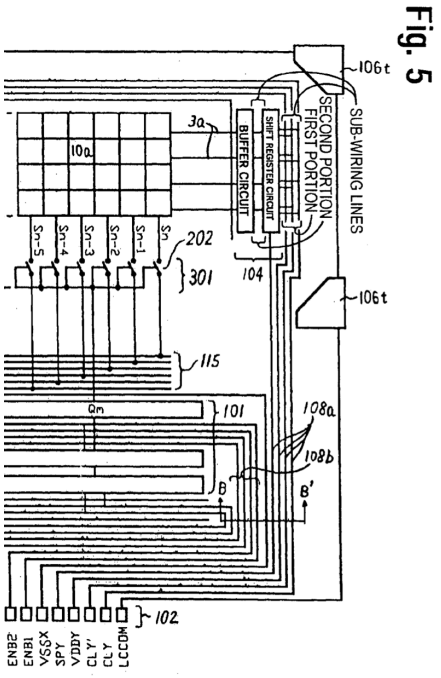
Claim 2 depends from claim 1 with the further limitation:

> **sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.**

78. A POSITA would understand *Muraide* to disclose first and second portions of sub-wiring lines made of different conductive films that were laid out so as not to intersect with each other. The structure described in this claim is merely an example of interlayer conductive line routing which is a common and necessary fabrication practice in making semiconductor structures. As shown below, the relevant portion of Figure 4 in *Muraide* (left side) is substantially the same as in Figure 5 of the ’390 patent (right side). The same structure in *Muraide* discloses or renders obvious the interlayer routing arrangements of claim 2.



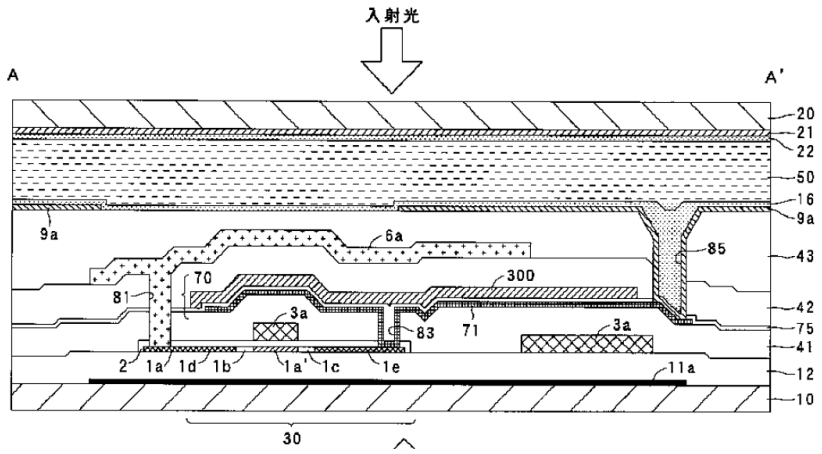
Muraide Fig. 4



'390 patent Fig. 5

79. In particular, Figure 4 of *Muraide* depicts sub-wiring lines where the first portions include at least lines 3a, and the second portions include at least the relay layer 71. As shown in part of Figure 4, in *Muraide*, the scanning line driving circuit 104 is in the peripheral region and intersects with certain main wiring lines, *e.g.*, SPY, CLY, CLY', VDDY, which extend from the plurality of connection terminals at the bottom of the Figure 4. As shown in Figure 3 of *Muraide* below, lines 3a intersect with main wirings (which are made of the same conductive film as the capacitance line 300) via an insulating layer 41. *Muraide,* ¶[0088]; ¶¶[0069]-[0073].

【図３】



Muraide teaches that: "The relay layer 71 and the capacitance line 300 are formed on the first interlayer insulating film 41, and a second interlayer insulating film 42 in which the contact hole 81 leading the high concentration source region 1d and the contact hole 85 leading to the relay layer 71 are defined respectively is formed on the relay layer 71 and the capacitance line 300." *Muraide*, ¶[0071]; Fig. 3. Thus, a POSITA would understand that that relay layer 71 and capacitance line 300 are formed on the first interlayer insulating film 41, *i.e.*, the relay layer 71 is in the same plane as the main wirings without intersection. *Muraide*, ¶[0071], Fig. 3.

80. Accordingly, it is my opinion that *Muraide* teaches claim 2. 1

3. Claim 3

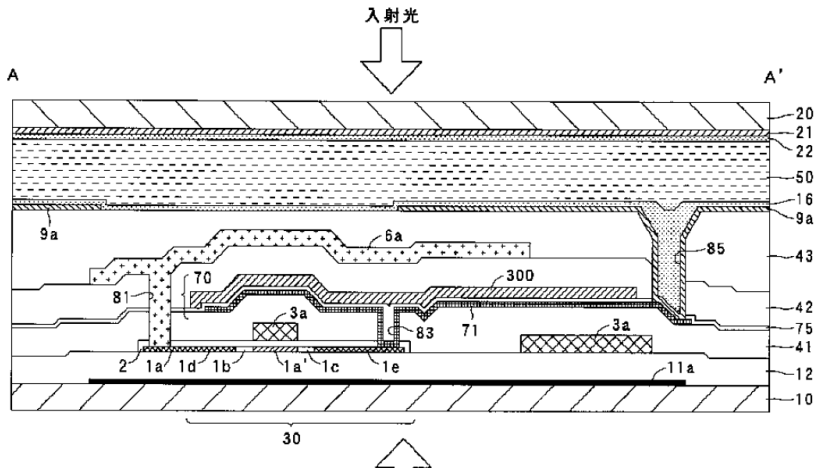
Claim 3 depends from claim 2 with the further limitation:

> **the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.**

81. A POSITA would understand that *Muraide* teaches that the first and

second portions of its sub-wiring lines are connected via contact holes. *Muraide* discloses in relation to *Muraide* Figure 3 that "On the scanning line 3a, a first interlayer insulating film 41 is formed in which a contact hole 81 leading to the high concentration source region 1d and a contact hole 83 leading to the high concentration drain region 1e are defined." *Muraide*, ¶[0070]. *Muraide* describes that the relay layer 71 (the second portion) is electrically coupled to the semiconductor layer 1a thought contact holes 83, and the scan lines 3a (the first portion) are the gate electrodes of the semiconductor layer a. *Muraide*, ¶[0069]-[0071], Fig. 3.

【図３】



As shown in Figure 3 above, the contact holes 81, 83 are formed in the interlayer insulating layer 41.

82. Accordingly, it is my opinion that *Muraide* teaches claim 3.

4. Claim 4

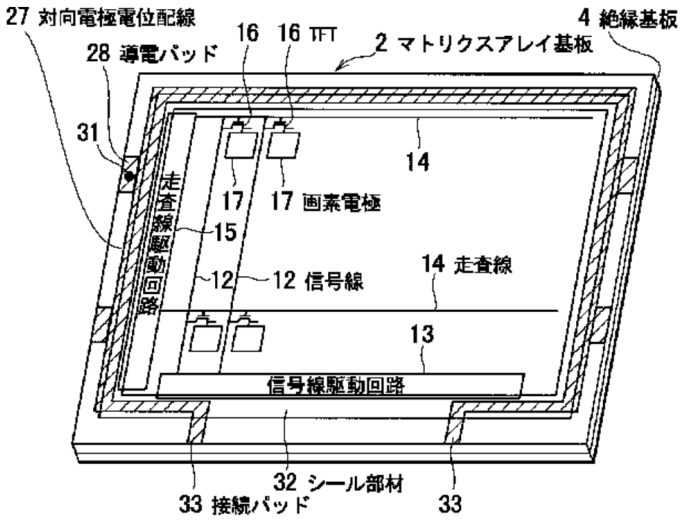
Claim 4 depends from claim 1 with the further limitation:

> **the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.**

83. A POSITA would understand that *Sunao* discloses peripheral driving circuits, such as the scanning line and data-line driving circuits, being closer to the center of the display than the conduction terminals and counter electrode potential line. *Sunao* teaches a "matrix array substrate 2 is arranged with a plurality of signal lines 12 arranged in parallel on a transparent insulating substrate 4, and a plurality of scanning lines 14 arranged in parallel to intersect the plurality of signal lines 12 at right angles. The signal lines 12 and the scanning lines 14 are electrically insulated by an insulating film." *Sunao*, ¶[0013]. *Sunao* further teaches that a "signal line driving circuit 13 for applying a video signal to the signal line 12 is electrically connected to one end of the signal line 12 , and a scanning line drive circuit 15 for applying a scanning signal to the scanning line 14 is electrically connected to one end of the scanning line 14." *Sunao*, ¶[0014].

84. *Sunao* thus discloses a scanning line driving circuit 15 that provides a scanning signal to the scanning line 14 as shown in *Sunao* Figure 3 below. *Sunao*, ¶[0014]; Fig. 3.

【図３】



85. *Sunao* further teaches a "conductive pad 28 for applying a potential to the counter electrode 7 and a counter electrode potential wiring 27 are provided in a peripheral portion of the display region 11 on the insulating substrate 4. The counter electrode potential wiring 27 is formed in a same process as the signal line 12 and the scanning line 14. A predetermined counter potential is externally supplied to the counter electrode potential wiring 27 through a connection pad 33 from an external PCB (not shown)." *Sunao*, ¶[0016]. *Sunao* Figure 3 (above) shows conductive pads 28 and counter electrode potential wirings 27 that apply potential to the counter electrode 7 located in a peripheral portion of the image display region 11 on the element substrate 4. *Sunao*, ¶[0016]. Electrode potential wiring 27 is connected via connection pad 33 to an external PCB. *Sunao*, ¶[0016]. *Sunao* thus discloses peripheral driving circuits ("scanning line driving circuit 15") being located nearer to the center of the element substrate than conductive pads 28

and counter electrode potential wirings 27.

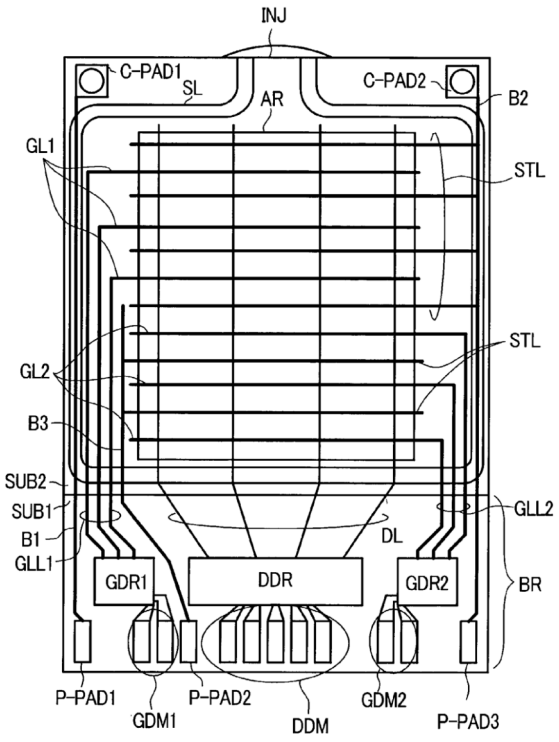
86. For the reasons set forth above in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Sunao*.

87. Alternatively, *Komeno* discloses this limitation. A POSITA would understand that *Komeno* discloses peripheral driving circuits, such as the scanning line and data-line driving circuits, being closer to the center of the display than the conduction terminals and counter electrode potential line. *Komeno* teaches that "On an inner surface of the second substrate SUB 2, counter electrodes which face the above-mentioned pixel electrodes in an opposed manner are formed. Further, in case of color display, color filters of a plurality of colors are provided above or below the counter electrodes. However, the color filters are omitted from the drawing along with the counter electrodes. The counter electrodes are connected to the feeding pads P-PAD1, P-PAD3 formed on the driving circuit mounting region BR through counter electrode connection pads C-PAD1, C-PAD2 formed on corner portions of an upper side of the first substrate SUB1 and common lines B1, B2." *Komeno*, ¶[0108].

88. As shown in *Komeno* Figure 1 (below), gate line driving circuits GDR1 and GDR2 are formed in the peripheral region BR, and feeding pads P-PAD1 and P-PAD3 are also formed in the peripheral region BR. *Komeno*, ¶[0108]-[0110]; Fig. 1. Counter electrodes are connected to the feeding pads P-PAD1, P-

PAD3 formed on the driving circuit mounting region BR through counter electrode connection pads C-PAD1, C-PAD2 which are formed on corner portions of an upper side of the first substrate SUB1 and common lines B1, B2. Electricity is supplied through the feeding pads P-PAD1, P-PAD3. *Komeno*, ¶[0108]-[0110]; Fig. 1. Figure 1 is shown below.

FIG. 1



Accordingly, with respect to the left/right side of the substrate, GDR1 is positioned nearer a center of the element substrate than (1) the conduction terminals P-PAD1/C-PAD1 and P-PAD3/C-PAD3, and (2) the counter electrode potential lines B1, B2.

89. For the reasons set forth above in regard to claim 1, a POSITA would

have been motivated to combine *Muraide* and *Komeno*.

90. Accordingly, it is my opinion that *Muraide* in combination with *Sunao* or *Komeno* teaches and renders obvious claim 4.

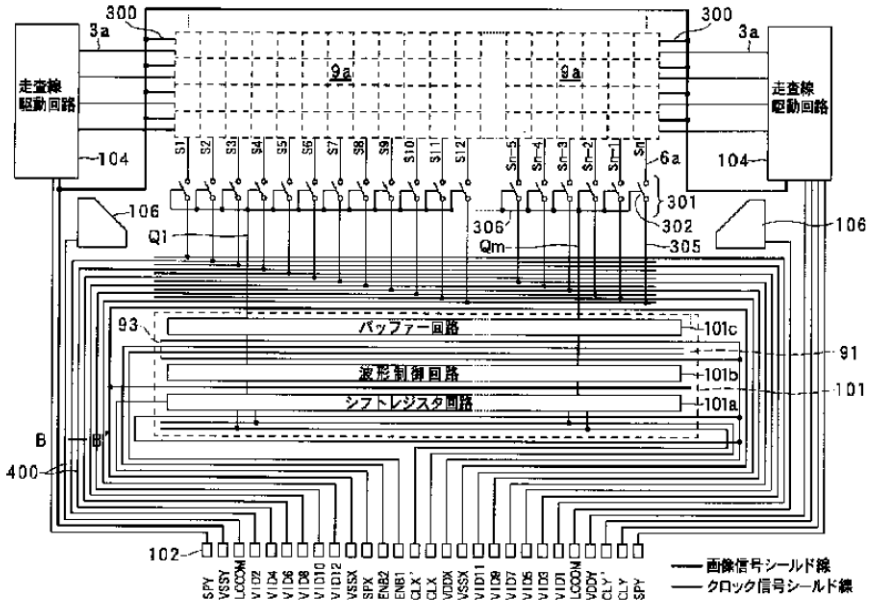
5. Claim 5

Claim 5 depends from claim 4 with the further limitation of:

> **the plurality of external circuit connection terminals being arranged along one side of the element substrate, and**
>
> **the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.**

91. A POSITA would understand that *Muraide* teaches external connection terminals along one edge of a substrate, with one such terminal being connected to a counter electrode potential line. As shown in Figure 4 of *Muraide,* a plurality of external connection terminals 102 are arranged along one side (the bottom portion of the figure) of an element substrate.

【図４】

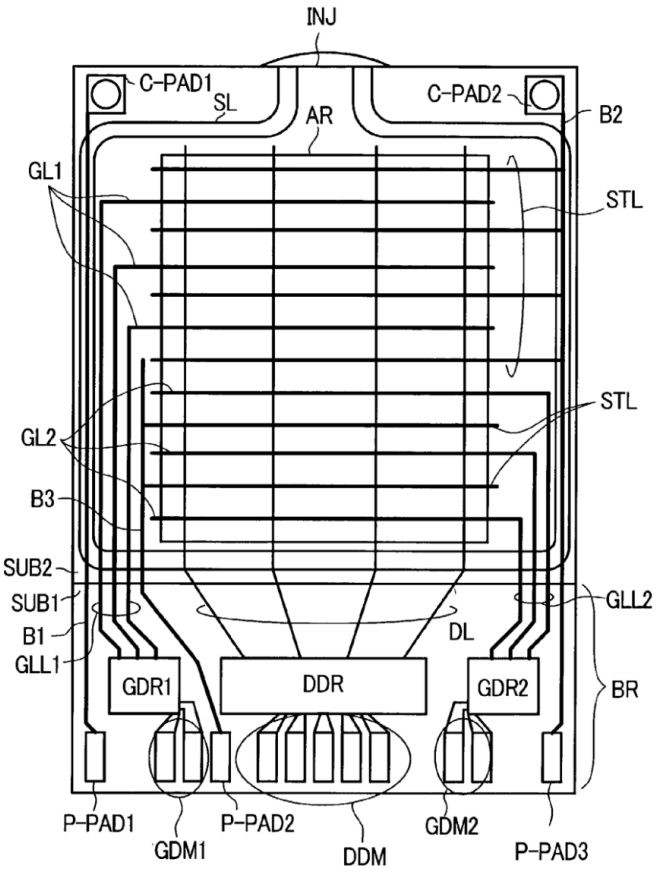


Muraide teaches that the "vertical conduction terminal 106 is supplied via the external input terminal 102 and the wiring 400 (LCCOM)." *Muraide*, ¶[0085]. As shown in Figure 4 of *Muraide*, an external connection terminal 102 that is connected to a counter electrode potential line (wiring 400 (LCCOM)) and is located near an end of the row of external connection terminals. In Figure 4, two connection terminals 102 are labelled LCCOM and both are located near the end of each side of the row of terminals 102 (third from the left side end and fourth from the right side end).

92. Alternatively, *Komeno* discloses this limitation. A POSITA would understand that *Komeno* teaches external connection terminals along one edge of a substrate, with one such terminal being connected to a counter electrode potential

line. *Komeno* teaches that counter electrodes are connected to the feeding pads P-PAD1, P-PAD3 formed on the driving circuit mounting region BR through counter electrode connection pads C-PAD1, C-PAD2 formed on corner portions of an upper side of the first substrate SUB1 and common lines B1, B2. *Komeno*, ¶[0108]. As shown in *Komeno* Figure 1 (below), a plurality of external connection terminals are arranged along the lower edge of the figure. Electricity is supplied through the feeding pads P-PAD1, P-PAD3. *Komeno*, ¶[0108]-[0110]; Fig. 1. Accordingly, *Komeno* teaches external circuit connection terminal P-PAD1 and P-PAD3, which are coupled to one end of the counter electrode potential line B1 and B2, that are near the end of an array of the plurality of external circuit connection terminals. In particular, they are located at the position closest to the left and right edges of the substrate as seen in Figure 1. *Komeno*, ¶[0108]; Fig. 1.

FIG. 1



93. For the reasons set forth above in in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Komeno*.

94. Accordingly, it is my opinion that *Muraide* alone or in combination with *Komeno* teaches or renders obvious claim 5.

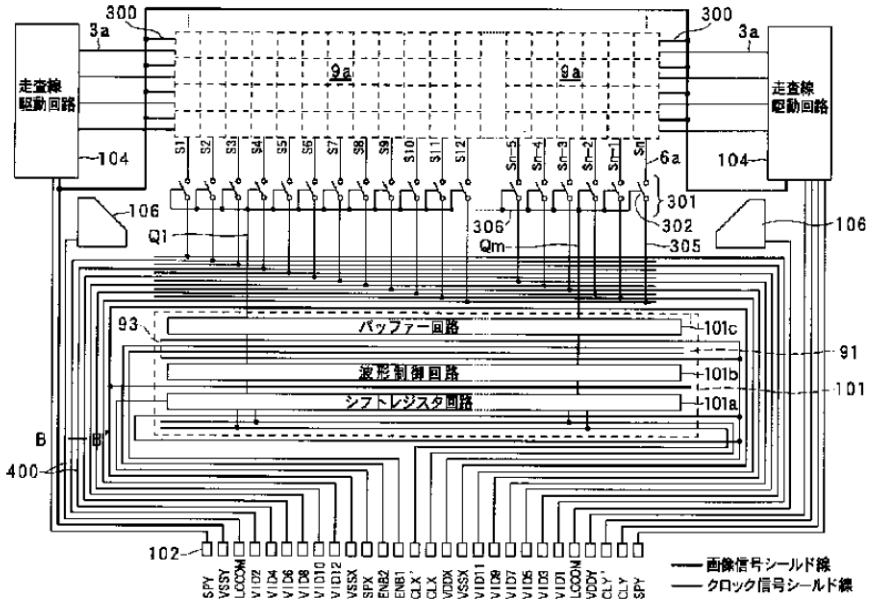
6. Claim 6

Claim 6 depends from claim 4 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

95. A POSITA would understand that *Muraide* teaches a clock signal and an inverse clock signal. *Muraide* discloses a clock signal (CLX) and an inverse clock signal (CLX'), which are part of the main wiring lines shown in *Muraide* Figure 4. *Muraide*, ¶[0080]. *Muraide* also discloses a counter electrode potential line (LCCOM). *Muraide*, ¶[0085]. As shown in Figure 4, *Muriade* discloses that the clock signals CLX and CLX' do not intersect with the counter electrode potential line LCCOM.

【図４】



96. Accordingly, it is my opinion that *Muraide* teaches claim 6.

7. Claim 7

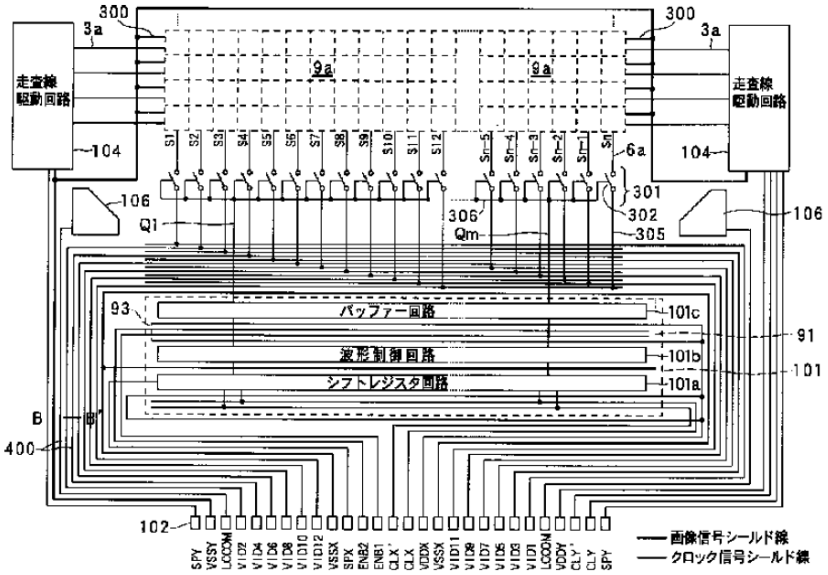
Claim 7 depends from claim 1 with the further limitation:

> **a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.**

97. A POSITA would understand that claim 7's requirement that parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region contradicts claim 1's requirement of "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines."

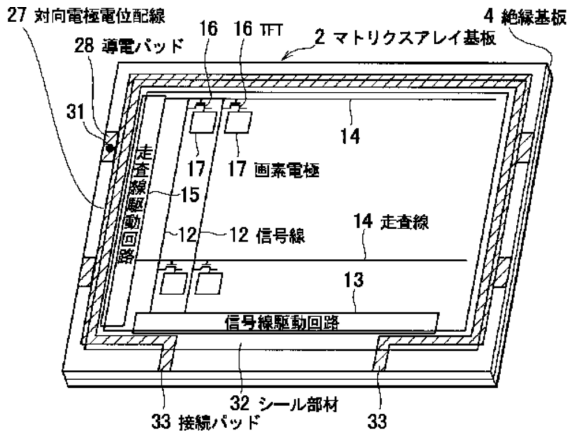
98. Despite this inconsistency, a POSITA would understand that *Muraide* discloses upper and lower conduction terminals and a counter electrode potential line that are closer to the center of the display than at least one of the driving circuits. For example, Figure 4 of *Muraide* discloses that the scanning line drive circuits 104 are arranged nearer to the side edges of array substrate 1 than the conductive terminals 106 and counter electrode line LCCOM.

【図４】



99. A POSITA would understand that *Sunao* discloses the first part of claim 7. As seen in *Sunao* Figure 3, *Sunao* teaches the scanning line driving circuit 15 is nearer to the center of the element substrate than the conductive pads 28, and the signal line driving circuit 13 is nearer to the lower edge of the element substrate than the conductive pads 28.

【図３】



100. For the reasons set forth above in regard to claim 1, a POSITA would have been motivated to combine *Muraide* and *Sunao.*

101. Accordingly, it is my opinion that *Muraide* in combination with *Sunao* teaches and renders obvious claim 7.

8. Claim 8

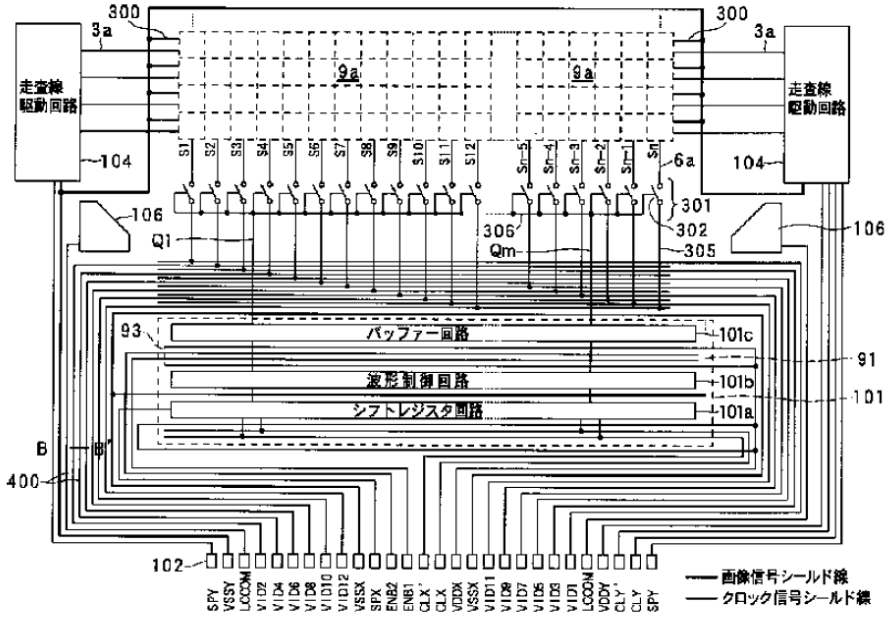
Claim 8 depends from claim 7 with the further limitations of:

> **the plurality of external circuit connection terminals being arranged along one side of the element substrate, and**
>
> **the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.**

102. As claim 8 depends from claim 7, it suffers from the same inconsistencies with claim 1.

103. A POSITA would understand that *Muraide* teaches external connection terminals in a row, at least one of which is connected to the other or one end of the plurality of main wiring lines and positioned near the end of the row of connection terminals. *Muraide* describes a plurality of external connection terminals 102 along one side of an element substrate as shown in Figure 4 (below).

【図４】



104. *Muraide* describes an external connection terminal 102 that is connected to a counter electrode potential line (wiring 400 (LCCOM)), and is located near an end of the row of external connection terminals. *Muraide*, ¶[0085]. In Figure 4, two connection terminals 102 are labelled LCCOM and both are located near the end of each side of the row of terminals 102 (third from the left side end and fourth from the right side end). The counter electrode potential line is part of the plurality of main wiring lines.

105. In addition, *Muraide* also describes an external connection terminal 102 that is connected to a clock signal (CLY) and another external connection terminal 102 that is connected to an inverse clock signal (CLY'), both of which are located near the end of right side of the row of terminals 102. The clock signal

wiring lines are part of the plurality of main wiring lines.

106. Accordingly, it is my opinion that *Muraide* teaches claim 8.

9. Claim 9

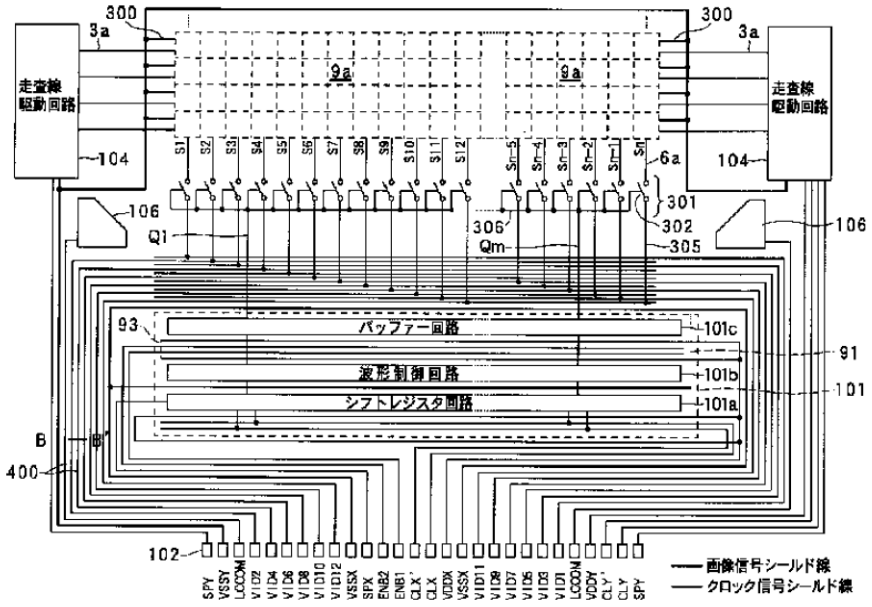
Claim 9 depends from claim 7 with the further limitation:

> **the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.**

107. As claim 9 depends from claim 7, it suffers from the same inconsistencies with claim 1.

108. A POSITA would understand that *Muraide* teaches a clock signal and an inverse clock signal. *Muraide* discloses a clock signal (CLX) and an inverse clock signal (CLX'), which are part of the main wiring lines shown in *Muraide* Figure 4. *Muraide*, ¶[0080]. *Muraide* also discloses a counter electrode potential line (LCCOM). *Muraide*, ¶[0085]. As shown in Figure 4, *Muriade* discloses that the clock signals CLX and CLX' do not intersect with the counter electrode potential line LCCOM.

【図４】



109. Accordingly, it is my opinion that *Muraide* teaches claim 9.

10. Claim 10

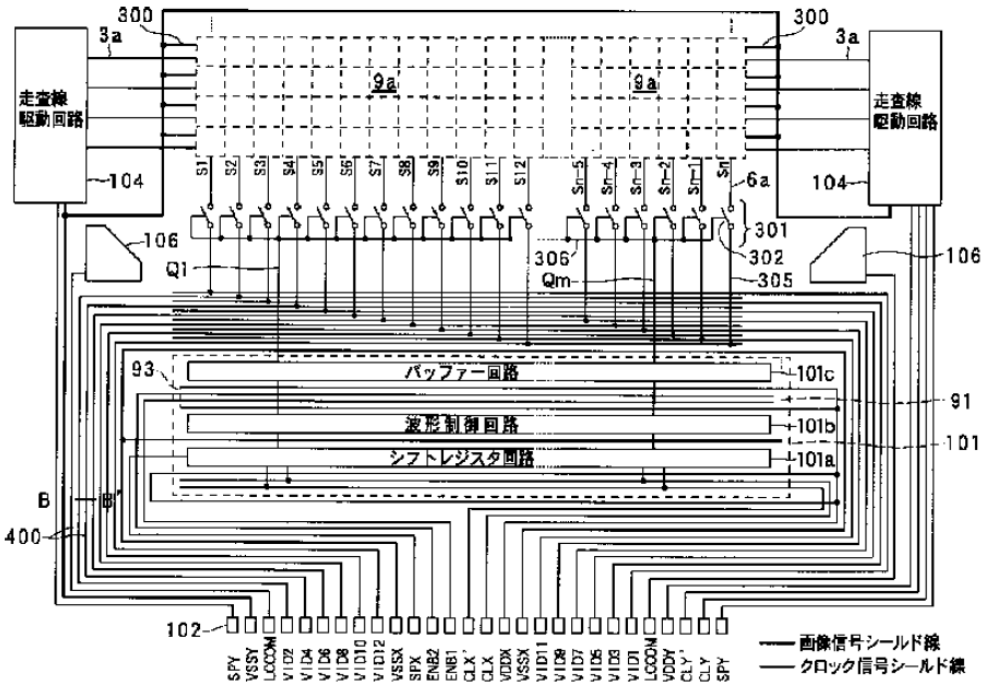
Claim 10 depends from claim 1 with the further limitation:

> **the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals and power source wiring lines that supply power source signals as electric signals, and**
>
> **the pair of signal lines and power source wiring lines do not intersect each other.**

110. A POSITA would understand that *Muraide* teaches clock signal lines and power source lines that do not intersect. *Muraide* describes reference clock signals CLX and inverted clock signals CLX' of the reference clock signal CLX. These signals are configured for the internal shift register circuit of the data line drive circuit 101 and supplied via the external input terminals 102 through the

wirings 400 (CLX and CLX'). *Muraide*, ¶[0080]. *Muraide* discloses power source wiring lines VSSX and VDDX configured for the data line drive circuit 101 as power sources, which are supplied from an external control circuit via the external input terminals 102 and the signal wirings 400 (VSSX and VDDX). *Muraide*, ¶[0080]. As shown in Figure 4, the clock signal and power source lines do not intersect each other. *Muraide*, ¶[0080]; Fig. 4.

【図４】



111. Accordingly, it is my opinion that *Muraide* teaches claim 10.

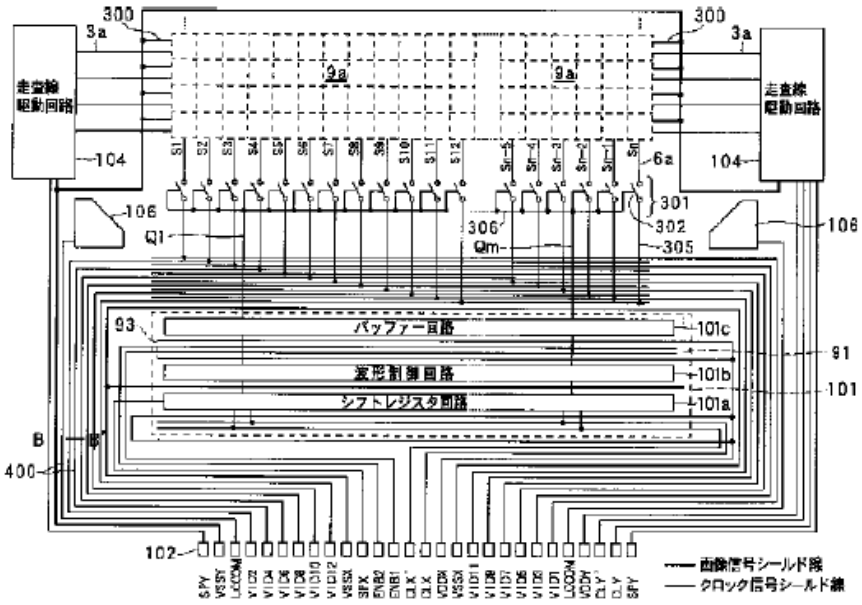
11. Claim 11

Claim 11 depends from claim 1 with the further limitation:

the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.

112. A POSITA would understand that *Muraide* discloses main wiring lines that have been laid out so as not to intersect each other. *Muraide* discloses main wiring lines, such as the wirings 400 (VID1 to VID12) that are image signal lines are made of the same conductive film (for example, a multilayer film including a conductive polysilicon film and a conductive metal silicide film) as the capacitance lines 300 in the image display region. *Muraide*, ¶[0087]. As shown in Figure 4 below, the main wiring lines zig-zag to change route and avoid intersection between one another.

【図４】



113. Accordingly, it is my opinion that *Muraide* teaches claim 11.

12. Claim 13

> **An electronic apparatus, comprising the electro-optical device according to claim 1.**

114. A POSITA would understand that *Muraide* teaches both an electronic apparatus and an electro-optical device. *Muraide* relates to an "an electro-optical device." *Muraide*, ¶[0001]. In addition, *Muraide* discloses an electronic apparatus that may comprise the electro-optical device: "the electro-optical device in the above-described embodiment may be applied to a projector." *Muraide*, ¶[0109].

115. Accordingly, it is my opinion that *Muraide* teaches claim 13. .

C. Ground 2: *Muraide* in Combination with *Sunao* or *Komeno* and in Further Combination with *Murade III* Renders Obvious Claims 2-3 and 12.

1. Claim 2

Claim 2 depends from claim 1 with the further limitation:

> **sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.**

116. A POSITA would understand *Murade III* to disclose first and second portions of sub-wiring lines made of different conductive films that were laid out

so as not to intersect with each other. *Murade III* teaches:

> As shown in FIGS. 4 and 5, the sampling circuit 103 is disposed in the area inside the sealing area and under the third light blocking film 53 (denoted by the hatching lines slanted to right in the figures) which is disposed on the opposite substrate 20, so as to serve as a partition for defining the boundary between the image displaying area and the outer area. In a part of the sealing area where extensions of the data lines 6 a extend, there are provided leading wirings 301 including leading wirings 301 a of the sampling circuit driving signal lines 114 extending from the data line driving circuit 101, and also including leading wirings 301 b of the image signal lines 115. On the other hand, in a part of the sealing area where extensions of the scanning lines 3 a extend, there are provided leading wirings 401 a of the scanning lines 3 a extending from the scanning line driving circuit 104. The leading wirings 401 may include an opposite electrode (common electrode) voltage line 112 disposed at an end of the lead wirings 401 and the leading wirings 401 b of the capacitance line 3 b.

Murade III, col. 18:38-65. Figures 5 and 6 of *Murade III* (below) depict this arrangement.

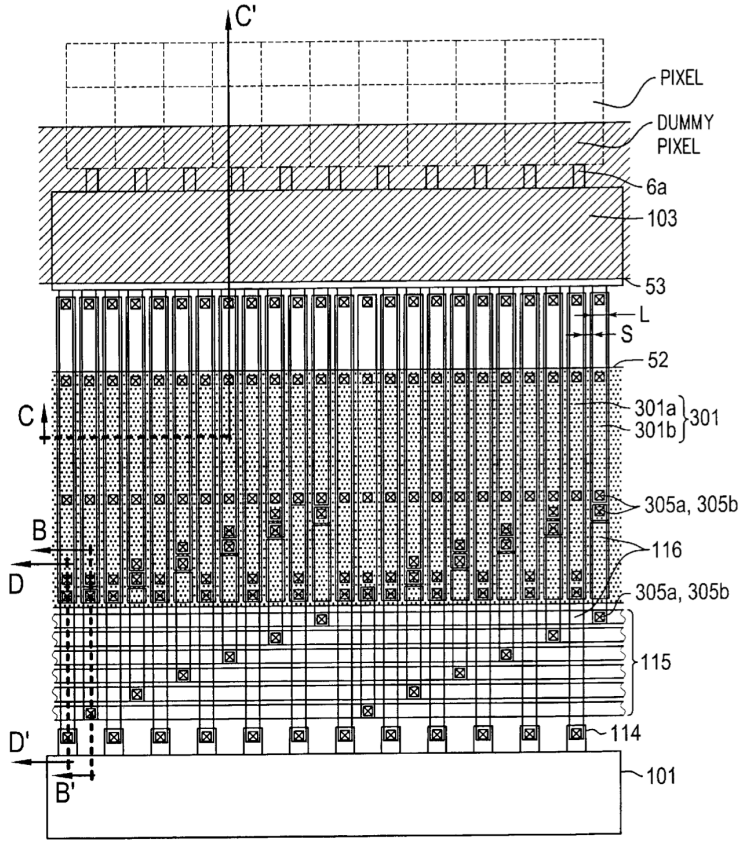


Fig. 5

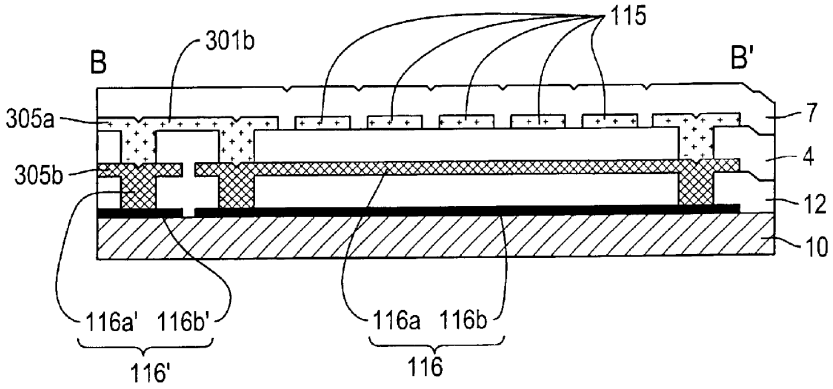


Fig. 6

117. As seen above, Figure 5 shows sub-wiring lines, including lines 301 consisting of line 301a of the sampling circuit driving signal lines 114 extending from the data line driving circuit 101, and 301b of the image signal lines 115.

Murade III, col. 18:38-65. Figure 6 shows "image signal lines 115, which are examples of peripheral wirings and leading wirings 301b, are formed using a single metal film." *Murade III*, col. 18:66-19:2.

118. A POSITA would understand Figures 5 and 6 to show that for the data line drive circuit 101, the first portions include the interconnecting lines 116, which is arranged to intersect with the signal lines 115 through the interlayer insulating film 4. Further, the second portions include the leading wirings 301b, which are formed at the same layer as the signal lines 115 and are arranged not to intersect with the signal lines 115.

119. A POSITA would understand that *Murade III* specifically discloses first and second portions made of different conductive films. *Murade III* describes interconnecting lines 116 extending from signal lines 115 to leading wirings 301b (shown in Figure 6) "are formed in the two-layer structure when viewed in the thickness direction of the TFT array substrate, wherein one layer is realized with the second conductive film 116a, and the other layer is realized with the first conductive film 116b." *Murade III*, col. 19:4-13.

120. A POSITA would have found it obvious to combine *Muraide* and *Murade III*. Specifically, a POSITA would have found it obvious to implement *Murade III's* sub-wiring line structure made of two different conductive films and separated by interlayer insulating film with *Muraide's* display device. *Id*. A

POSITA would have been motivated to combine *Murade III's* structure with *Muraide's* display device in order to further isolate the sub-wiring lines. *Id*. This combination would have allowed the device of *Muraide* to potentially further miniaturize. Further, as both *Muraide* and *Murade III* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Murade III's* structure with *Muraide's* display device. Finally, as both references relate to LCDs and describe similar functions combining the design of *Murade III* into *Muraide's* display device would have yielded predictable results. *Id*.

121. Accordingly, it is my opinion that *Muraide* in combination with *Murade III* teaches and renders obvious claim 2.

2. Claim 3

Claim 3 depends from claim 2 with the further limitation:

> **the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.**

122. A POSITA would understand that *Murade III* teaches that the first and second portions of its sub-wiring lines are connected via contact holes. *Murade III* discloses:

> The interconnecting lines 116, which extend from the image signal lines 115 to the leading wirings 301 b, are formed in the two-layer structure when viewed in the thickness direction of the TFT array substrate, wherein one layer is realized with the second conductive film 116 a, which is made of the same film as the polysilicon film used to form the scanning line 3 a, and which is electrically

> connected via the contact hole 305 a to the corresponding image signal line 115, and the other layer is realized with the first conductive film 116 b, which is made of the same film as the first light blocking film 11 a, and which is electrically connected via the contact hole 305 b to the corresponding interconnecting line 116 a. In order to further reduce the resistance of the leading wirings 301 b, the leading wirings 301 b may be coupled with the second conductive film 116 a′ and the first conductive film 116 b′.

Murade III, col. 19:4-29.

123. As shown in Figure 6 below, a contact hole electrically couples the first and second portions of sub-wiring lines.

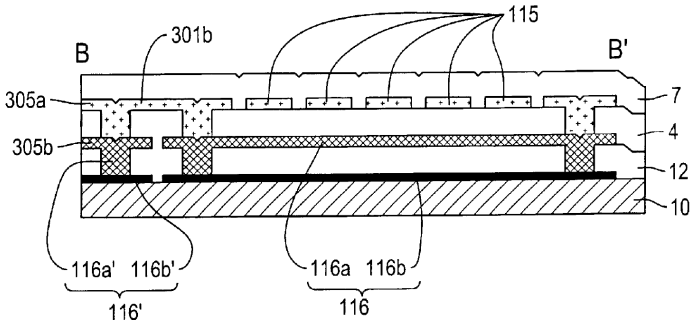


Fig. 6

124. As seen in Figure 6, contact hole 305b electrically connects the second conductive film 116a to the leading wiring 301b, which are formed in the second interlayer insulating film 4. *Murade III*, col. 26:66-27:3.

125. A POSITA would have combined *Muraide* and *Murade III* for the reasons set forth in claim 2 above.

126. Accordingly, it is my opinion that *Muraide* in combination with *Murade III* teaches and renders obvious claim 3.

3. Claim 12

Claim 12 depends from claim 1 with the further limitation:

> **the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film.**

127. A POSITA would understand that *Murade III* teaches main wiring lines wherein at least some of the main wiring lines are redundant and composed of different conductive film. *Murade III* specifically discloses "the interconnecting lines 116 have a redundant structure" that is implemented via two different conductive films. *Murade III*, col. 19:51-56; Fig. 6. *Murade III* further discloses multilayer wirings where the different wirings are made of the same film as the conductive film of their respective layers. *Murade III*, col. 5:14-25.

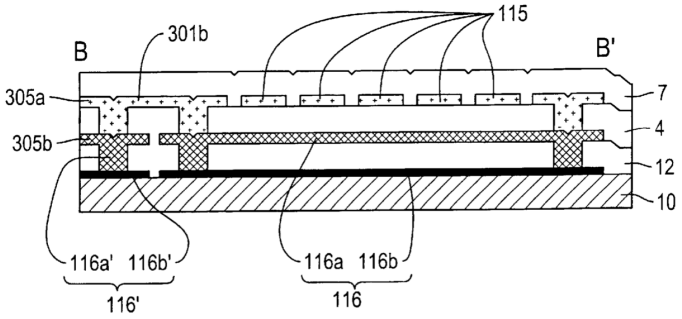


Fig. 6

128. A POSITA would have combined *Muraide* and *Murade III* for the reasons set forth in claim 2.

129. Accordingly, it is my opinion that *Muraide* in combination with *Murade III* teaches and renders obvious claim 12.

D. Ground 3: *Fujikawa* Anticipates Claims 1-5, 7, 8, 11, and 13.

1. Claim 1

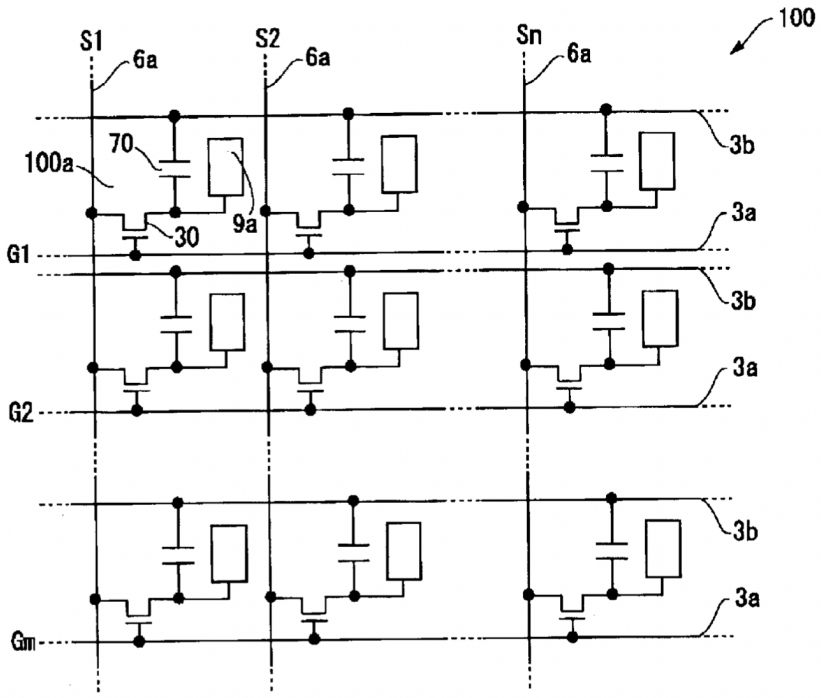
An electro-optical device, comprising:

130. A POSITA would understand that *Fujikawa* relates to electro-optical devices. *Fujikawa* specifically teaches that its invention "provides an electrooptic device and an electronic device." *Fujikawa*, abstract.

131. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

a plurality of pixel portions provided in an image display region on an element substrate;

132. A POSITA would understand that *Fujikawa* discloses the well-known, basic elements of an electro-optical device, such as an LCD display. For example, *Fujikawa* discloses a matrix of pixel electrodes that are formed on a TFT array substate 10. *Fujikawa*, ¶¶[0049], [0050]. Figure 4 of *Fujikawa* depicts image display region 10a of the liquid crystal device 100, where a plurality of pixels formed in a matrix so as to constitute the image display region 10a. *Fujikawa*, ¶[0053], Fig. 4. *Fujikawa* Figure 4 is below.



133. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

> **in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,**

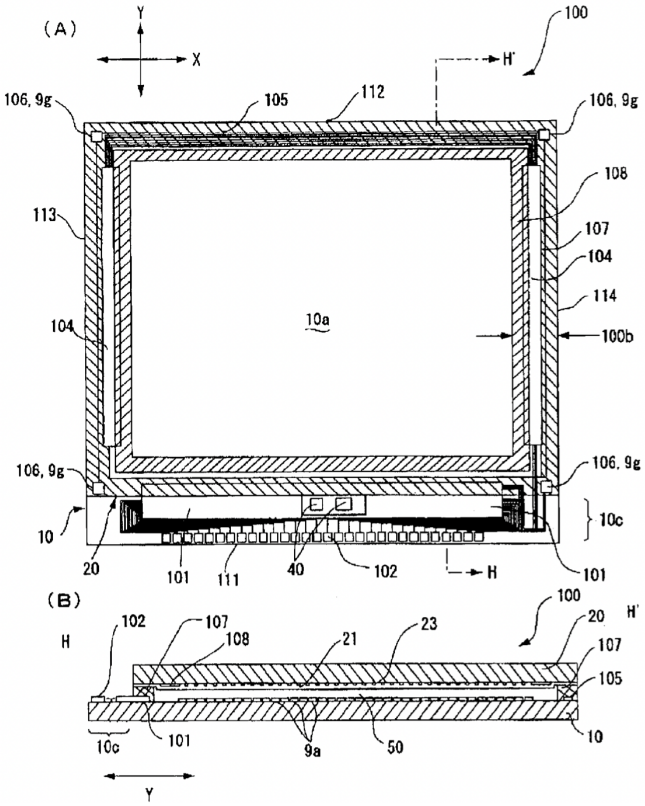
134. A POSITA would understand *Fujikawa* to disclose a peripheral region of an image display region as having a variety of circuits and connecting wiring. *Fujikawa* teaches: "On the outer periphery of the TFT array substrate 10, a data-line driving circuit 101 is formed along a substrate edge 111 so as to overlap with a

part of the scaling material 107, and scanning-line driving circuits 104 are formed along substrate edges 113 and 114. Multiple terminals 102 are formed on a region 10 c of the TFT array substrate 10 that protrudes from the counter substrate 20. A plurality of lines 105 are formed along a substrate edge 112 of the TFT array substrate 10 on the opposite side of the substrate edge 111 so as to connect the scanning-line driving circuits 104 on both sides of an image display region 10 a." *Fujikawa*, ¶[0046].

135. As shown in *Fujikawa* 1 (below), *Fujikawa* discloses a peripheral region ("10c") of an element substrate ("TFT array substrate 10"). At the bottom edge of Figure 1, multiple external connection terminals ("terminals 102") are formed, and connected in a one-to-one manner to main wiring lines. *Fujikawa,* ¶¶[0046], [0050], [0053]; Fig. 1. *Fujikawa* discloses that: "Multiple terminals 102 made of a metal film, such as an aluminum film, a metal silicide film, or a conductive film, such as an ITO film, are formed along a substrate edge 111 of the TFT array substrate 10, and a constant voltage, a modulation image signal, and various driving signals are input thereto. A plurality of lines 109 made of, for example, a low-resistance metal film, such as an aluminum film, for driving a scanning-line driving circuit 101 and data-line driving circuits 104, are routed from these terminals 102." *Fujikawa*, ¶[0055].

136. Thus, *Fujikawa* discloses terminals 102 that are made of a metal film

with a plurality of lines 109 also made of a low-resistance metal film, such as an aluminum film, connected thereto. The plurality of main lines 109 transfer voltage and signals from the terminals 102 to a data-line driving circuit 101 and scanning-line driving circuits 104. *Fujikawa*, ¶[0055]. The data-line driving circuit 101 and scanning-line driving circuits 104 drive the pixels in the display region 10a based on the voltage and signals from the terminals 102 through the main lines 109. *Fujikawa*, ¶¶[0055-[0058]; Figs. 1, 2.

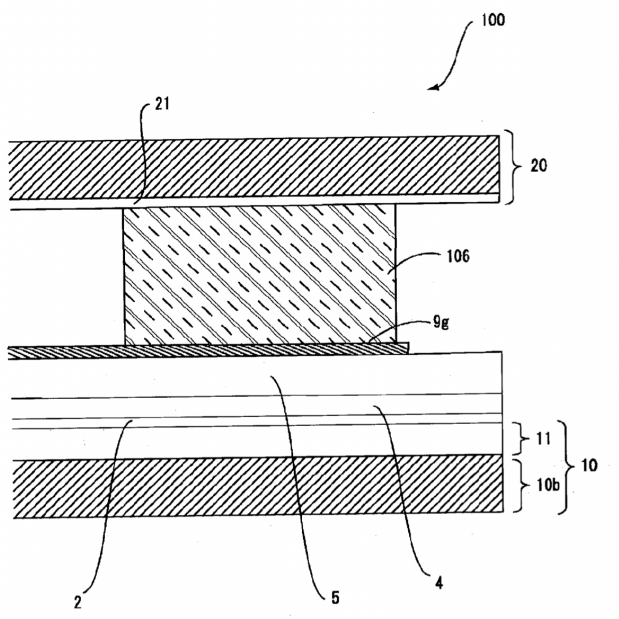


Fujikawa Fig. 1

137. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

138. A POSITA would understand *Fujikawa* to disclose a counter electrode on a counter substrate. In particular, *Fujikawa* teaches: "The TFT array substrate 10 and the counter substrate 20 are bonded with a predetermined space therebetween by the scaling material 107." *Fujikawa*, ¶[0046]. Thus, *Fujikawa* discloses a counter substrate that is arranged to face the element substrate ("TFT array substrate 10"), and teaches that the TFT array substrate 10 and the counter substrate 20 that are bonded with a predetermined space therebetween. *Fujikawa*, ¶¶[0046], [0049]. Further, *Fujikawa* teaches: "a plurality of conductive electrodes 9g are formed in the region of the TFT array substrate 10 overlapping with the counter substrate 20, and are electrically connected to the counter electrodes 21 of the counter substrate 20 through the conductive material 106 sandwiched between the substrates, as shown in FIG. 9." *Fujikawa*, ¶[0079]. Thus, *Fujikawa* discloses that the counter electrode 21 is provided on the counter substrate 20 and a constant voltage (DCCOM) can be supplied to the terminals 102 in the peripheral region of the element (TFT array) substrate and then to the counter electrode 21 of the counter substrate 20. *Fujikawa*, ¶¶[0078], [0079], Fig. 9. *Fujikawa* Figure 9 is shown below.



139. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

> **a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,**

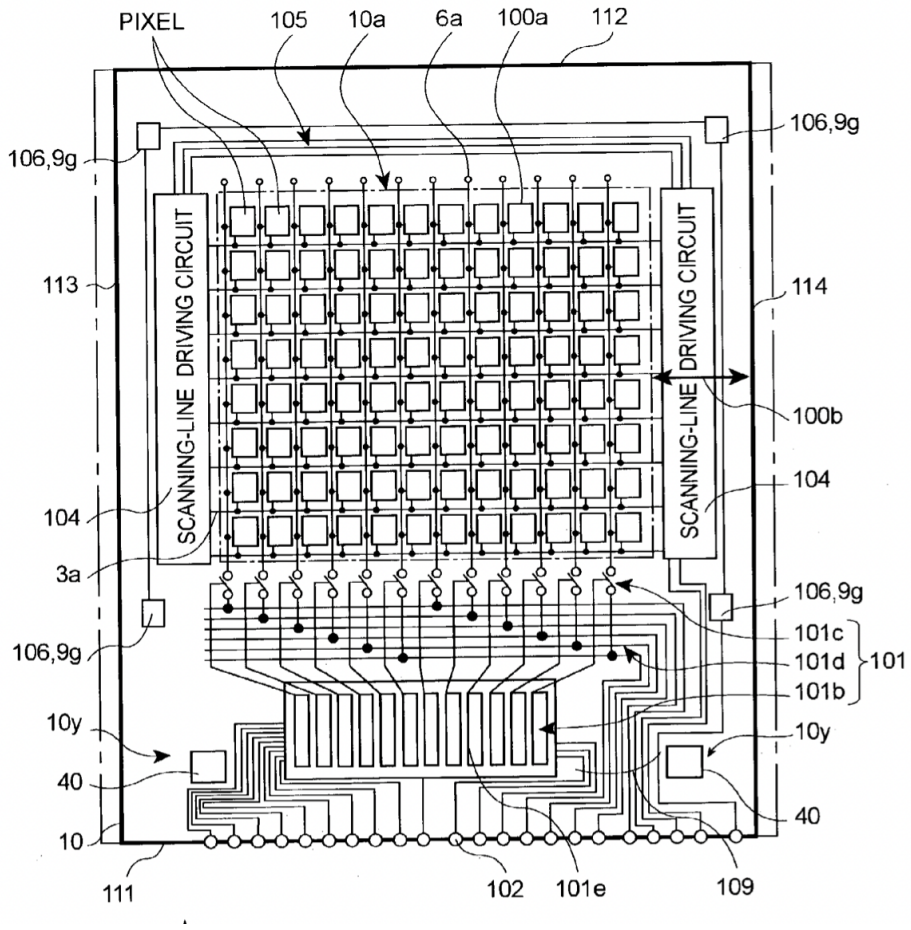
140. A POSITA would understand *Fujikawa* to teach a counter electrode potential line being connected to the counter electrode. *Fujikawa* describes its device as including: "Conductive electrodes 9g are formed in the regions on the periphery of the image display region 10a that overlap with the counter substrate 20, and are electrically connected to the counter electrodes of the counter substrate 20 through conductive materials 106 held between the substrates. Therefore, a constant voltage (DCCOM) supplied to the terminals 102 of the TFT array substrate 10 can be supplied to the counter electrodes of the counter substrate 20."

Fujikawa, ¶[0008]. *Fujikawa* further teaches that: "Multiple terminals 102 are formed on a region 10 c of the TFT array substrate 10 that protrudes from the counter substrate 20." In regard to the terminals, Fujikawa teaches that: "Multiple terminals 102 made of a metal film, such as an aluminum film, a metal silicide film, or a conductive film, such as an ITO film, are formed along a substrate edge 111 of the TFT array substrate 10, and a constant voltage, a modulation image signal, and various driving signals are input thereto. A plurality of lines 109 made of, for example, a low-resistance metal film, such as an aluminum film, for driving a scanning-line driving circuit 101 and data-line driving circuits 104, are routed from these terminals 102." *Fujikawa*, ¶[0055].

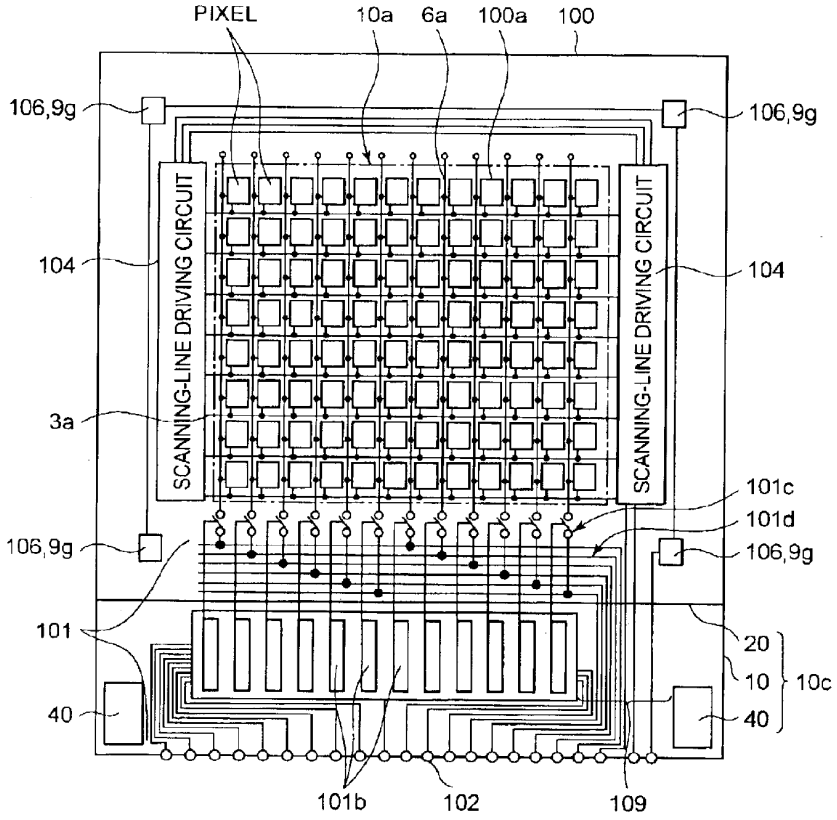
141. In addition, *Fujikawa* describes that "Conductive electrodes 9g and conductive materials 106 are formed in areas corresponding to four corners of the counter substrate 20 for electrical continuity between the TFT array substrate 10 and the counter substrate 20." *Fujikawa*, ¶[0047].

142. Thus, *Fujikawa* discloses terminals 102 along the edge of the peripheral region of the TFT array substrate. Figures 12 and 19 teach that one of these terminals 102 supply power via a main wiring line 109 to conductive electrodes 9g and conductive materials 106. Conductive elements 9g and 106 electrically connect the TFT array substrate 10 and the counter substrate 20. As explained by *Fujikawa*: "Therefore, a constant voltage (DCCOM) supplied to the

terminals 102 of the TFT array substrate 10 can be supplied to the counter electrodes 21 of the counter substrate 20." *Fujikawa*, ¶[0079], *see also* ¶¶[0046], [0047], [0050], [0055], [0072], [0008]. *Fujikawa* Figures 12 and 19 are shown below.



Fujikawa Fig. 12



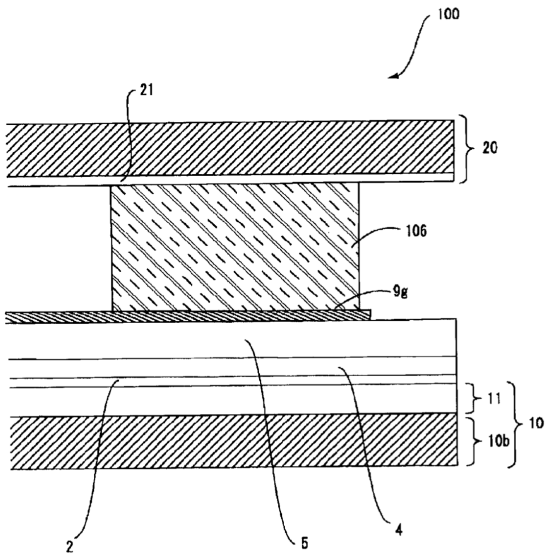
Fujikawa Figure 19

143. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

144. A POSITA would understand *Fujikawa* to teach upper and lower conduction terminals that are connected to the counter electrode potential line. *Fujikawa* describes that: "Conductive electrodes 9g and conductive materials 106 are formed in areas corresponding to four corners of the counter substrate 20 for electrical continuity between the TFT array substrate 10 and the counter substrate 20." *Fujikawa*, ¶[0047]. *Fujikawa* further teaches that "a plurality of conductive

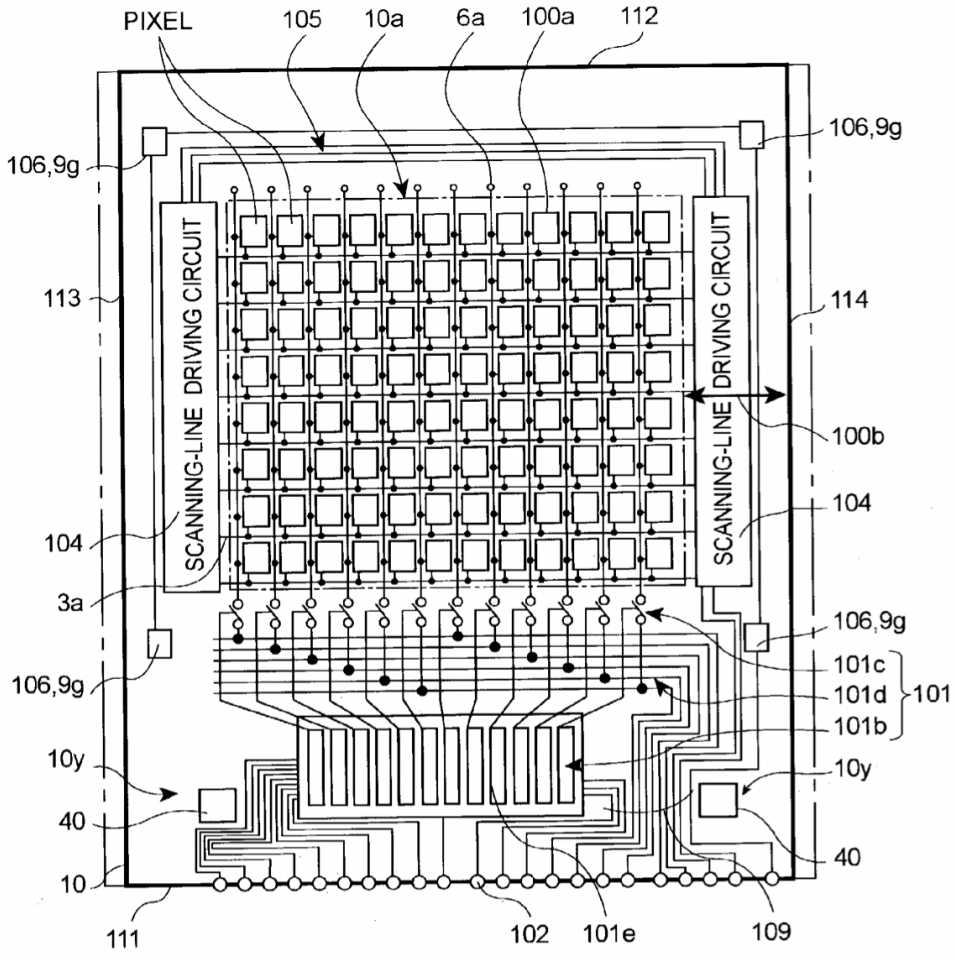
electrodes 9g are formed in the region of the TFT array substrate 10 overlapping with the counter substrate 20, and are electrically connected to the counter electrodes 21 of the counter substrate 20 through the conductive material 106 sandwiched between the substrates, as shown in FIG. 9." *Fujikawa*, ¶[0079]. Therefore, *Fujikawa* discloses conductive electrodes 9g on the TFT array substrate (element substrate) that overlap with the counter substrate 20. As seen in *Fujikawa* Figure 9 below, conductive electrodes 9g are electrically connected to counter electrodes 21 of the counter substrate 20 through conductive material 106 sandwiched between the substrates.



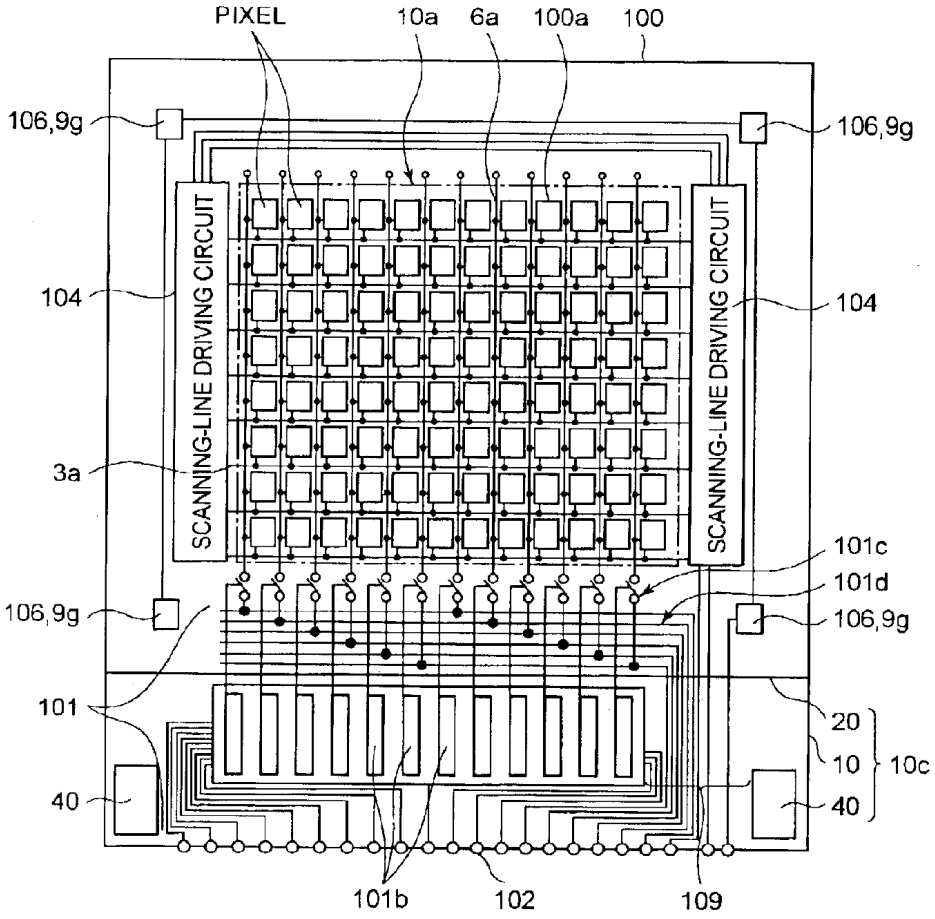
Fujikawa Fig. 9

145. As seen in *Fujikawa* Figures 12 and 19 (below), the conduction terminals (conductive electrodes 9g and conductive materials 106) are formed in areas corresponding to four corners of the counter substrate 20, two being upper conduction terminals and two being lower conduction terminals. *Fujikawa*,

¶[0047]. Further, terminals 102 on the TFT array substrate supply power via a main wiring line 109 to conductive electrodes 9g and conductive materials 106. Thereby, a constant voltage (DCCOM) can be supplied to the counter electrodes 21 of the counter substrate 20. *Fujikawa*, ¶¶[0078], [0079], Fig. 9. As such, the wiring line 109 that is outermost on the right side in the Figures that leads to and connects to the conduction terminals (conductive electrodes 9g and conductive materials 106) is a counter electrode potential line.



Fujikawa Fig. 12



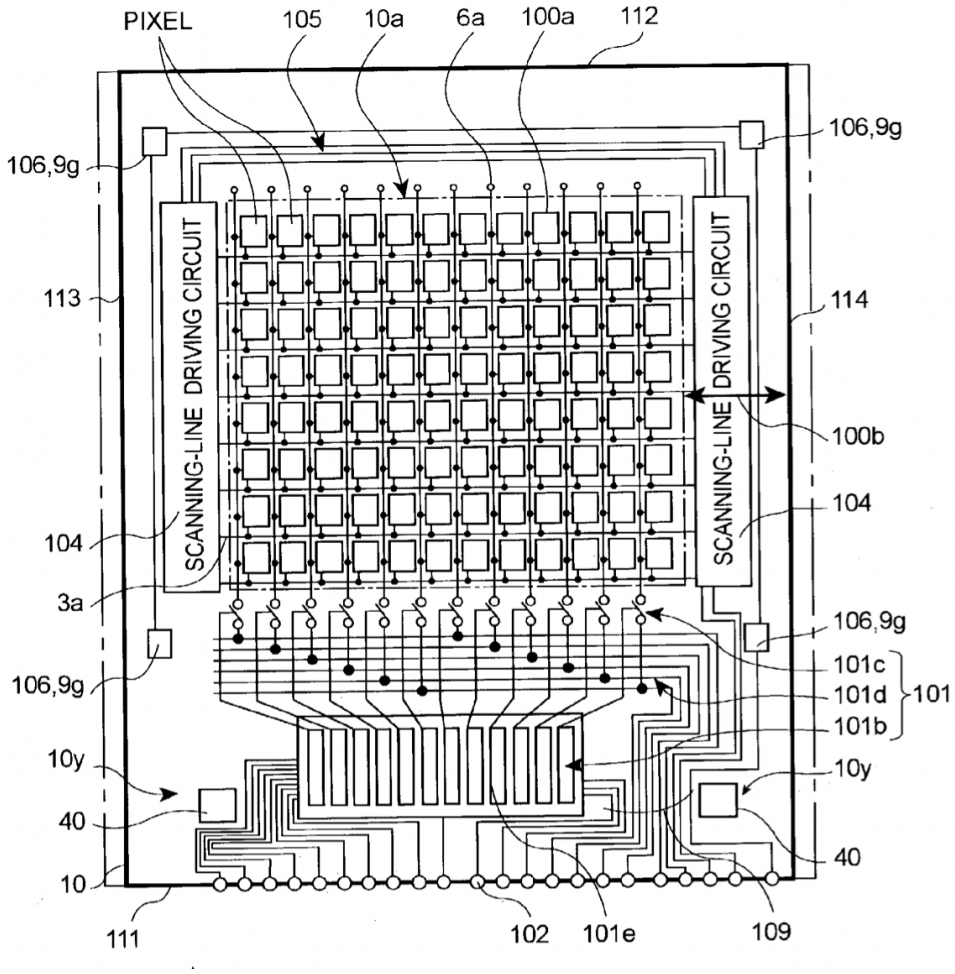
Fujikawa Figure 19

146. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

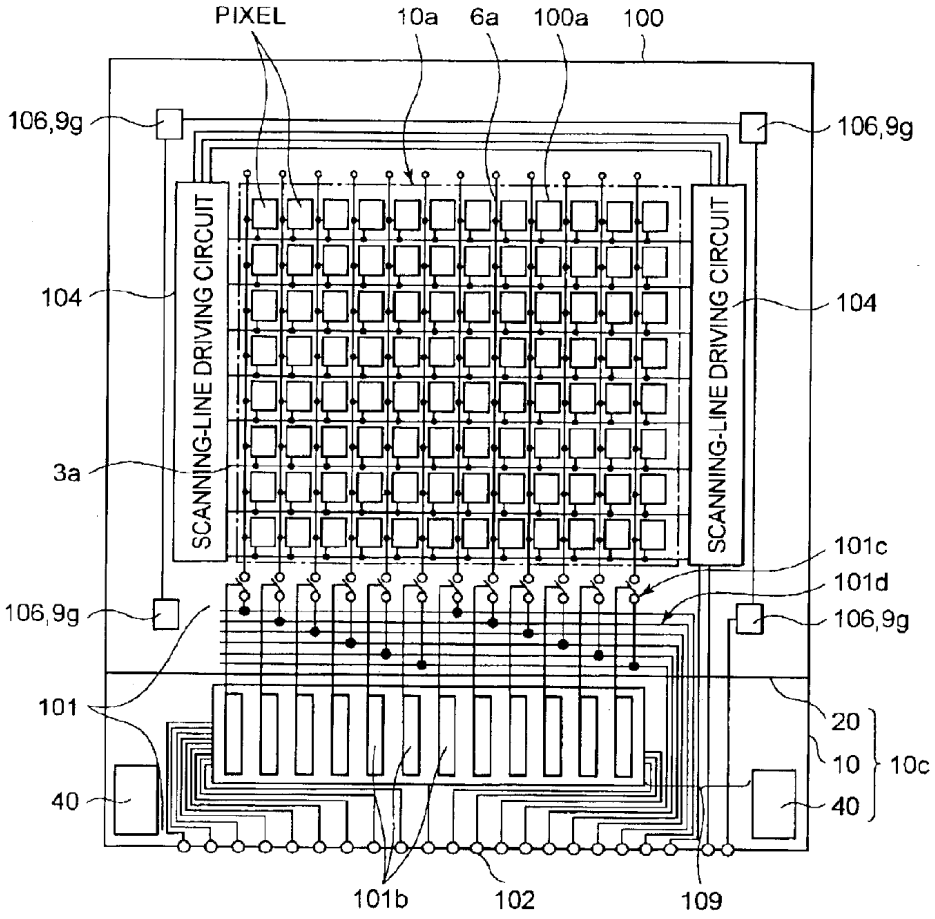
> **the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and**

147. A POSITA would understand *Fujikawa* to teach main wiring lines made out of a same conductive material that are laid out so that they do not intersect in the peripheral region. *Fujikawa* discloses: "A plurality of lines 109 made of, for example, a low-resistance metal film, such as an aluminum film, for

driving a scanning-line driving circuit 101 and data-line driving circuits 104, are routed from these terminals 102." *Fujikawa*, ¶[0055]. *Fujikawa* Figures 12 and 19 show that these main wiring lines 109 are laid out in a zig-zag pattern so as to not intersect each other in the peripheral region.



Fujikawa Fig. 12



Fujikawa Figure 19

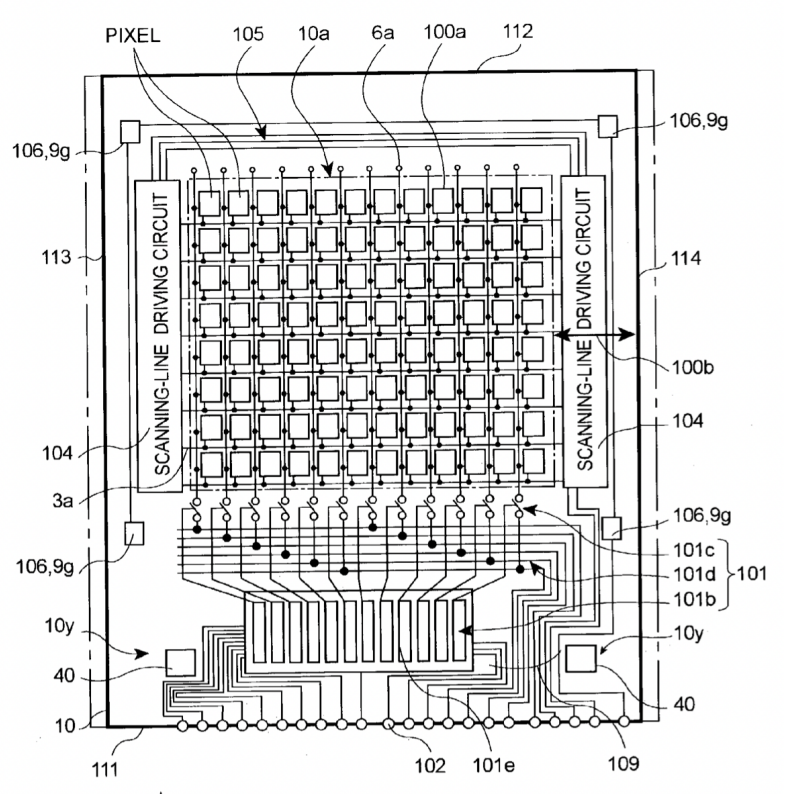
148. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

> **the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.**

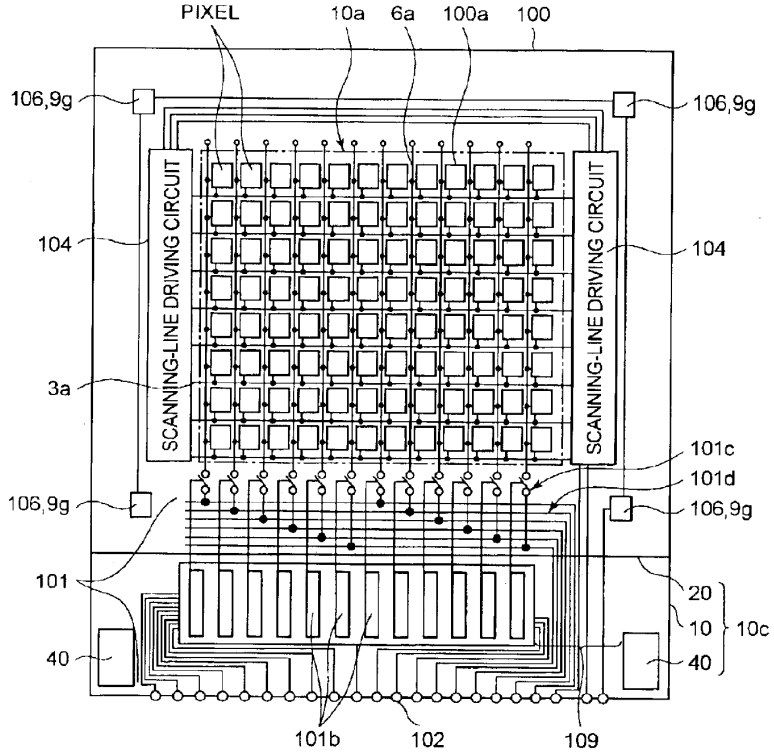
149. A POSITA would understand *Fujikawa* to disclose a counter electrode potential line that has been designed to run along the outer edge of an array substrate. *Fujikawa* describes that "Conductive electrodes 9g and conductive materials 106 are formed in areas corresponding to four corners of the counter

substrate 20 for electrical continuity between the TFT array substrate 10 and the counter substrate 20." *Fujikawa*, ¶[0047]. *Fujikawa* discloses terminals 102 along the edge of the peripheral region of the TFT array substrate. Figures 12 and 19 teach that one of these terminals 102 supply power via a main wiring line 109 to conductive electrodes 9g and conductive materials 106, that is, is a counter electrode potential line.

150. For example, as seen in Figures 12 and 19, *Fujikawa* discloses terminals 102 on the TFT array substrate able to supply power via a main wiring line 109 that leads to and connects to conductive electrodes 9g and conductive materials 106. Thereby, a constant voltage (DCCOM) can be supplied to the counter electrodes 21 of the counter substrate 20. *Fujikawa*, ¶[0079]. The wiring line 109 that is outermost on the right side in Figures 12 and 19 and that leads to conductive electrodes 9g and conductive materials 106 (conduction terminals) is a counter electrode potential line. The counter electrode potential line is also closest to edges of the element substrate, among the wiring lines 109. *Fujikawa* Figures 12 and 19 are shown below.



Fujikawa Fig. 12



Fujikawa Figure 19

151. Accordingly, it is my opinion that *Fujikawa* teaches this limitation of claim 1.

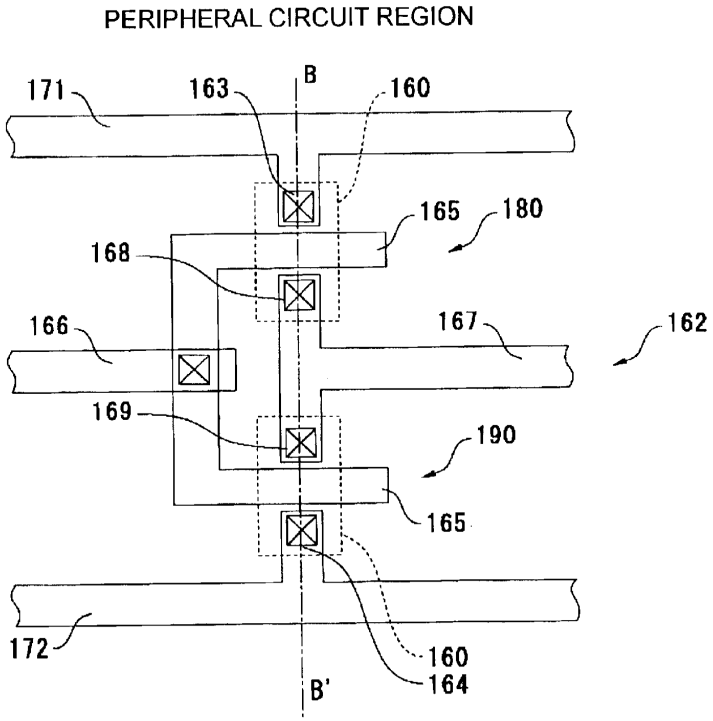
2. Claim 2

Claim 2 depends from claim 1 with the further limitation:

> **sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.**

152. A POSITA would understand *Fujikawa* to disclose first and second portions of sub-wiring lines made of different conductive films that were laid out so as not to intersect with each other. *Fujikawa* discloses sub-wiring lines which are internal wiring lines of the peripheral driving circuits. For example, as shown in Figure 7 (below), *Fujikawa* discloses the structure of a TFT that constitute a peripheral circuit, such as the scanning-line driving circuit 104 or a data-line driving circuit 101, including a high-potential line 171 and a low-potential line 172. *Fujikawa*, ¶¶[0074]-[0077]; Fig. 7. These lines are electrically connected to source regions of the semiconductor films 160 through contact holes 163 and 164,

which are located in the TFTs 180 and 190. *Fujikawa*, ¶¶[0074]-[0077]. Figure 7 further shows an input line 166, which is connected to a common gate electrode 165, and an output line 167, which is electrically connected to drain regions of the semiconductor films 160 through contact holes 168 and 169. *Fujikawa*, ¶¶[0074]-[0077].

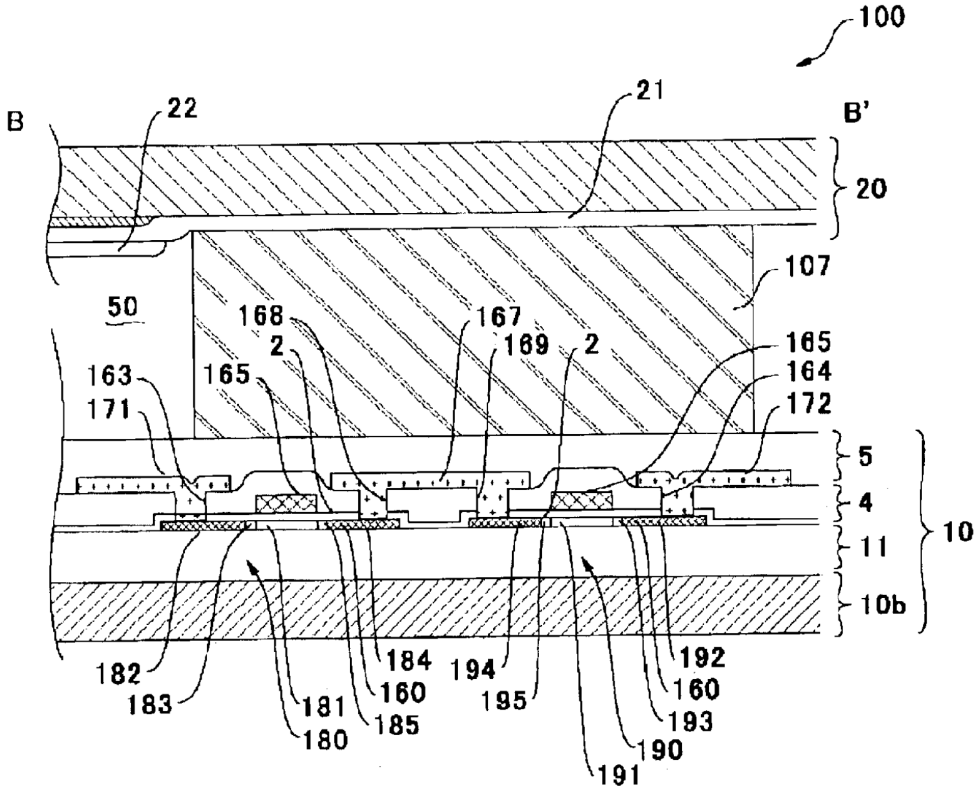


Fujikawa Fig. 7

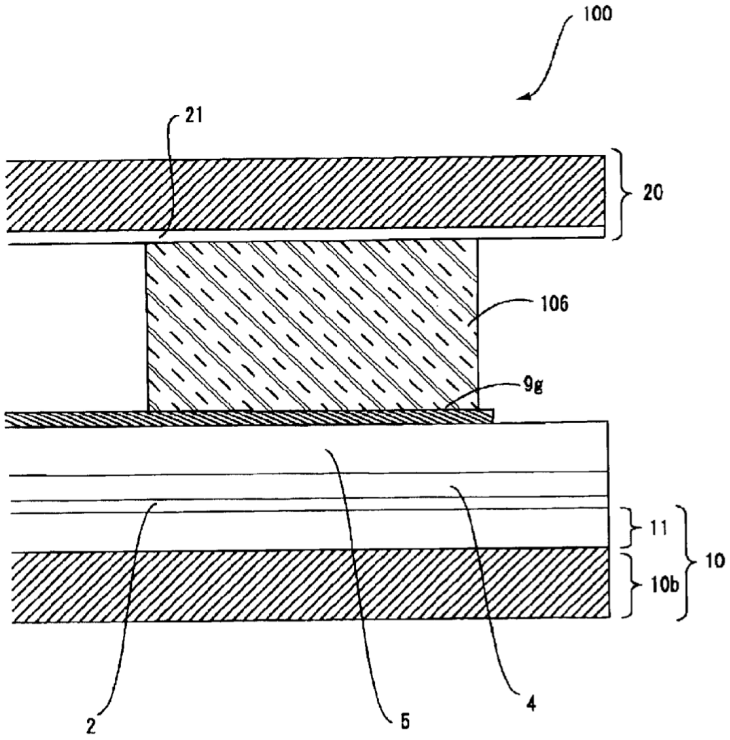
153. As noted above, claim 2 provides a structure that results from interlayer conductive line routing which is a common and necessary fabrication practice in making semiconductor structures. *Fujikawa* discloses or teaches several such arrangements.

154. For example, in Figure 7, *Fujikawa* discloses that the first portions are

the input lines 166, and the second portions are the vertical portions of the common gate electrodes 165. *Fujikawa*, ¶¶[0074]-[0077]. As shown in the cross-section view in *Fujikawa* Figure 8, the input lines 166 (at the plane of the output lines 167) are formed in the interlayer insulating film 5, which is on top of the insulating film 4. Fig. 8. On the other hand, the main wiring lines 109 are formed on top of the array substrate 10, which is on top of the interlayer insulating film 5, as shown in *Fujikawa* Figure 9. In other words, the input lines 166 are formed by a conductive film different from the main wiring lines 109, and are separated by the interlayer insulating film 5.



Fujikawa Figure 8



Fujikawa Fig. 9

155. *Fujikawa* Figures 8 and 9 together teach that the input lines 166 are perpendicular to the main wiring lines 109 and, thus, intersect the main wiring lines 109. The vertical portions of the common gate electrodes 165 are formed as a conductive film in the interlayer insulating film 4 and on top of the protective underlayer 11 of the substrate. As the input lines 166 appear perpendicular to the main wiring lines 109, the vertical portions of the common gate electrodes 165 appear parallel to the main wirings 109 and, thus, do not intersect the main wirings lines 109. *Fujikawa,* ¶[0075], Figs. 7-9.

156. Thus, *Fujikawa* discloses first portions of the sub-wiring lines as input lines 166, and second portions as at least the vertical portions of the common gate electrodes 165. Among these portions, input lines 166 are perpendicular to the

main wiring lines 109 and, thus, intersect the main wiring lines 109, but the vertical portions of the common gate electrodes 165 appear parallel to the main wirings 109 and, thus, do not intersect the main wirings lines 109.

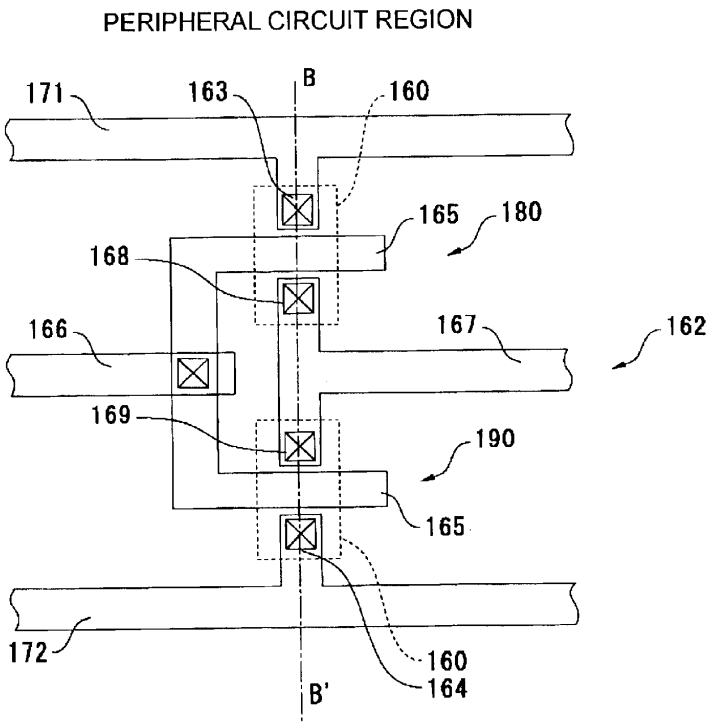
157. Accordingly, it is my opinion that *Fujikawa* teaches claim 2.

3. Claim 3

Claim 3 depends from claim 2 with the further limitation:

> **the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.**

158. A POSITA would understand that *Fujikawa* teaches that the first and second portions of its sub-wiring lines are connected via contact holes. As shown in *Fujikawa* Figure 7, *Fujikawa* discloses that input line 166 is connected to a common gate electrode 165, and an output line 167 is electrically connected to drain regions of the semiconductor films 160 through contact holes 168 and 169, respectively. *Fujikawa*, ¶¶[0074]-[0077]. That is, *Fujikawa* discloses first portions of the sub-wiring lines (input lines 166) and second portions of the sub-wiring lines (the vertical portions of the common gate electrodes 165) are electrically connected through contact holes.



Fujikawa Fig. 7

159. Accordingly, it is my opinion that *Fujikawa* teaches claim 3.

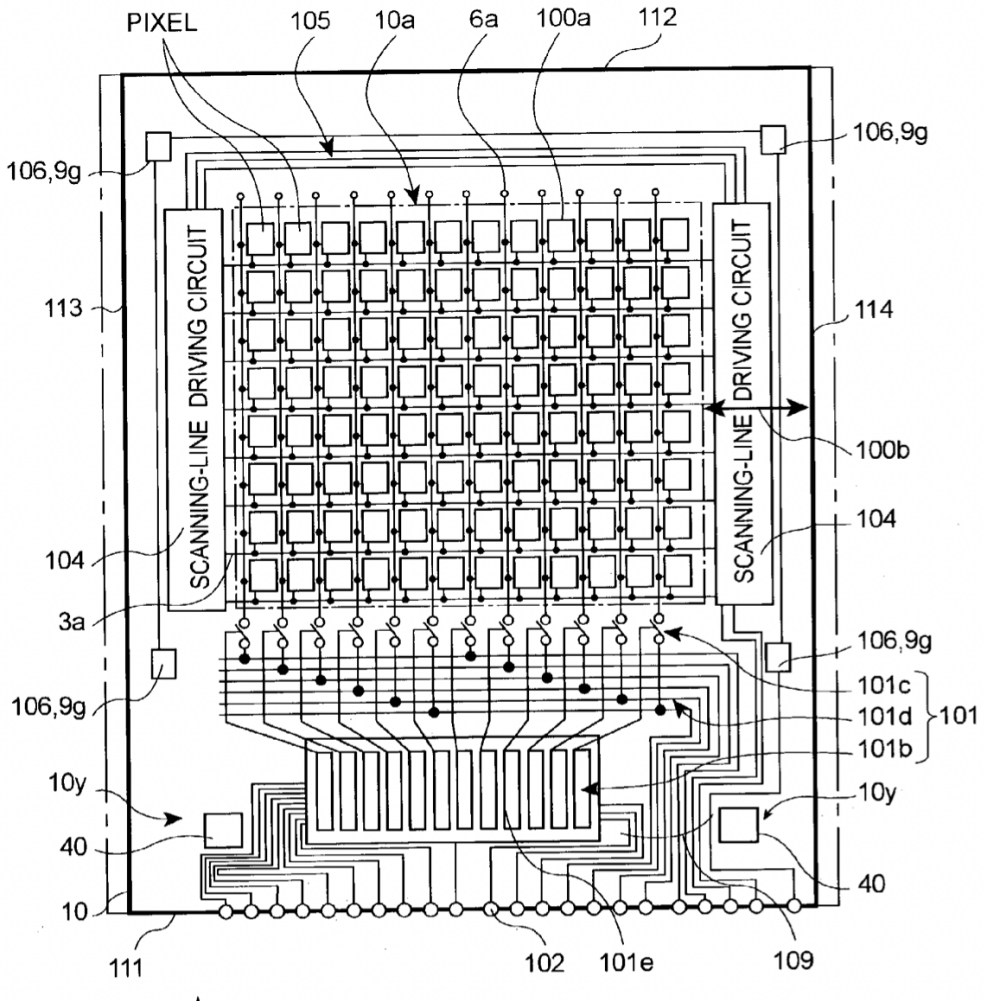
4. Claim 4

Claim 4 depends from claim 1 with the further limitation:

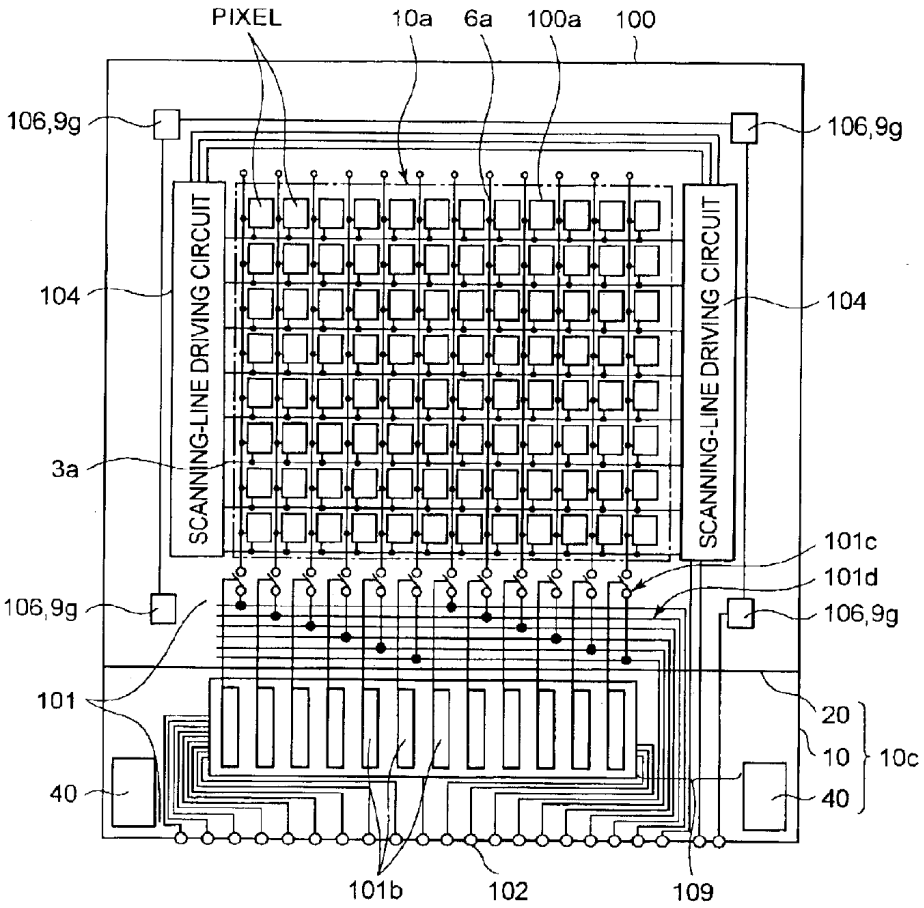
> **the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.**

160. A POSITA would understand that *Fujikawa* discloses peripheral driving circuits, such as the scanning line and data-line driving circuits, being closer to the center of the display than the conduction terminals and counter electrode potential line. As seen in *Fujikawa* Figures 12 and 19, the scanning line driving circuits 104 are nearer to the center of substrate 10 than the conductive

electrodes 9g/conductive materials 106 (106, 9g) and the main wiring line leading from one of the terminals 102 to conductive electrodes 9g (the counter electrode potential line), which is located at the outermost right in the Figures. *Fujikawa*, Figs. 12, 19.



Fujikawa Fig. 12



Fujikawa Fig. 19

161. Accordingly, it is my opinion that *Fujikawa* teaches claim 4.

5. Claim 5

Claim 5 depends from claim 4 with the further limitation:

> **the plurality of external circuit connection terminals being arranged along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.**

162. A POSITA would understand that *Fujikawa* teaches external connection terminals along one edge of a substrate, with one such terminal being

connected to a counter electrode potential line. As seen in Figures 12 and 19 of *Fujikawa*, there are a plurality of external circuit connection terminals (102) along the lower edge (111) of the substrate. The main wiring line leading from one of the terminals 102 to conductive electrodes 9g (the counter electrode potential line), is positioned near the end of an array of the plurality of external circuit connection terminals (it is located at the outermost right in the Figures). *Fujikawa*, ¶[0055].

163. Accordingly, it is my opinion that *Fujikawa* teaches claim 5.

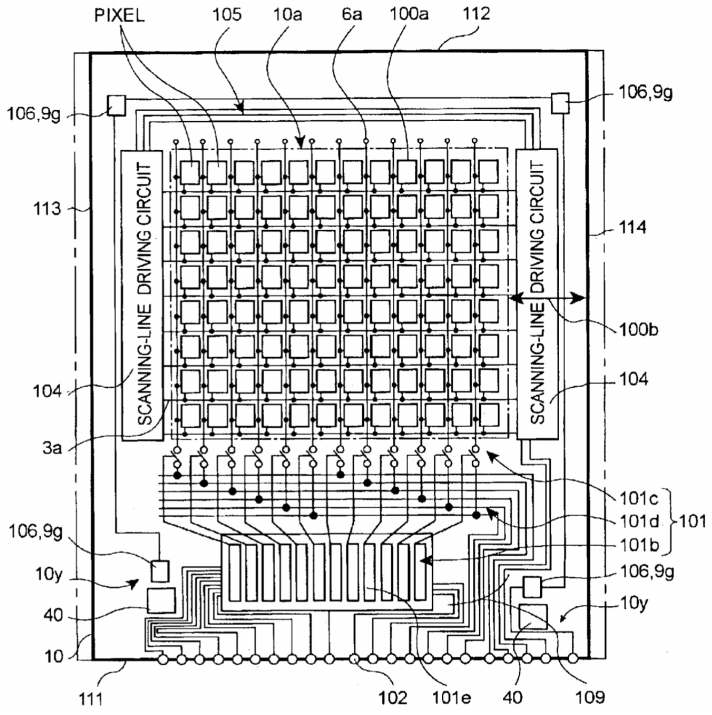
6. Claim 7

Claim 7 depends from claim 1 with the further limitation:

> **a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.**

164. A POSITA would understand that claim 7's requirement that parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region contradicts claim 1's requirement that "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Further, the '390 patent does not appear to disclose any such structure.

165. Despite this inconsistency, a POSITA would understand that *Fujikawa* discloses upper and lower conduction terminals and a counter electrode potential line that are closer to the center of the display than at least one of the driving circuits. As shown in *Fujikawa* Figure 14, which is another embodiment of *Fujikawa*, the scanning line driving circuit 104 is positioned closer to the center of substrate 10 than the conductive electrodes 9g/conductive materials 106 and the counter electrode potential line. However, portions of the data line driving circuit 101 are partially positioned closer to the lower and side edges of the substrate 10 than the conductive electrodes 9g/conductive materials 106 and the counter electrode potential line.



Fujikawa Fig. 14

166. Accordingly, it is my opinion that *Fujikawa* teaches claim 7.

7. Claim 8

Claim 8 depends from claim 7 with the further limitations of:

> **the plurality of external circuit connection terminals being arranged along one side of the element substrate, and**
>
> **the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.**

167. As claim 8 depends from claim 7, it suffers from the same inconsistencies with claim 1.

168. A POSITA would understand that *Fujikawa* teaches external connection terminals in a row, at least one of which is connected to the other or one end of the plurality of main wiring lines and positioned near the end of the row of connection terminals. *Fujikawa* discloses a plurality of external circuit connection terminals (102) along the lower edge (111) of the substrate. Fig. 14; *see also* Figs. 12, 19. The main wiring line leading from one of the terminals 102 to conductive electrodes 9g (the counter electrode potential line), is located at the outermost right in the Figures. In other words, the counter electrode potential line is positioned near the end of an array of the plurality of external circuit connection terminals.

169. Accordingly, it is my opinion that *Fujikawa* teaches claim 8.

8. Claim 11

Claim 11 depends from claim 1 with the further limitation:

> **the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.**

170. A POSITA would understand *Fujikawa* to teach main wiring lines made out of a same conductive material that are laid out so they do not intersect in the peripheral region. *Fujikawa* discloses a plurality of main wiring lines 109 made of, for example, a low-resistance metal film, such as an aluminum film that are routed from terminals 102. *Fujikawa*, ¶[0055]. As seen in Figures 12 and 19, the main wiring lines 109 are laid out in a zig-zag pattern so as to not intersect each other in the peripheral region.

171. Accordingly, it is my opinion that *Fujikawa* teaches claim 11.

9. Claim 13

> **An electronic apparatus, comprising the electro-optical device according to claim 1.**

172. A POSITA would understand that *Fujikawa* teaches both an electronic apparatus and an electro-optical device. *Fujikawa* discloses that its invention an electrooptic device and an electronic device. *Fujikawa*, abstract. *Fujikawa* further discloses such devices can be used as part of different devices (apparatuses), including "as display sections in electronic devices, such as portable telephones, portable computers, and video cameras." *Fujikawa*, ¶[0004].

173. Accordingly, it is my opinion that *Fujikawa* teaches claim 13.

E. Ground 4: *Murade II* in Combination with *Sunao* or *Komeno* Renders Obvious Claims 1, 4-11 and 13.

1. Claim 1

An electro-optical device, comprising:

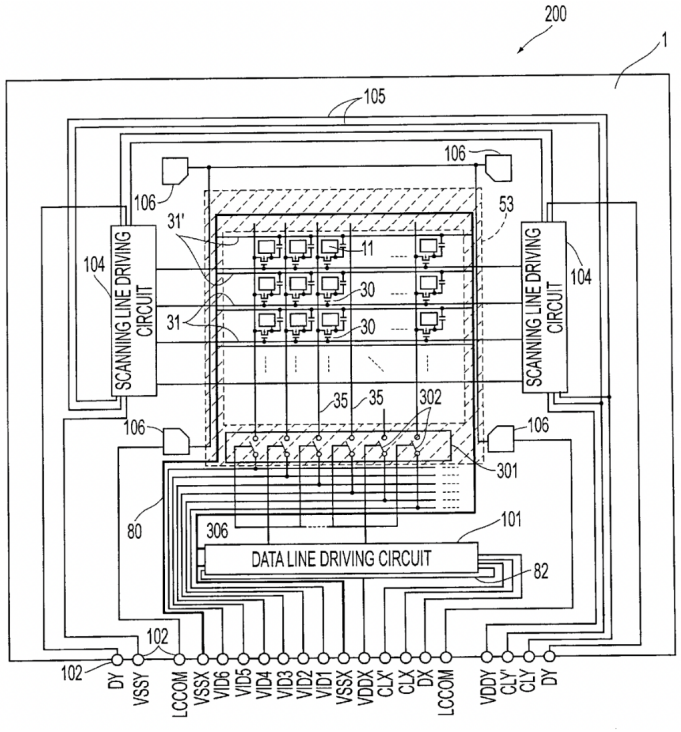
174. A POSITA would understand that *Murade II* relates to electro-optical devices. In particular, *Murade II* is titled an "Electro-optical device and electronic apparatus" *Murade II*, cover.

175. Accordingly, it is my opinion that *Murade II* teaches this limitation of claim 1.

a plurality of pixel portions provided in an image display region on an element substrate;

176. A POSITA would understand that *Murade II* discloses the well-known, basic elements of an electro-optical device, such as an LCD display. For example, *Murade II* discloses an "image display area" that has a plurality of pixel electrodes. In particular, *Murade II* describes: "At the upper side of an image display area defined by the plurality of pixel electrodes 11 (the image display area is a particular area of the liquid crystal apparatus where an image is displayed by changing the alignment of the liquid crystal), a plurality of wirings 105 are provided via which the scanning line driving circuits 104 formed at right and left sides of the image display area are connected to each other." *Murade II*, col. 15:31-38. *Murade II* discloses that the image display region is on an TFT array

substrate (element substrate). *Murade II*, col. 13:61-64; Fig. 1.



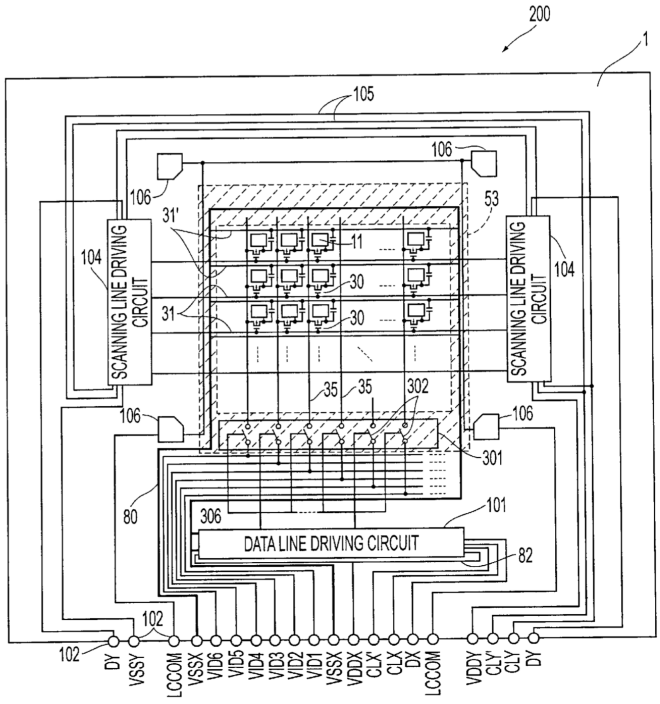
Murade II Fig. 1

177. Accordingly, it is my opinion that *Murade II* teaches and renders obvious this limitation of claim 1.

> **in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,**

178. A POSITA would understand *Murade II* to disclose a peripheral region of an image display region as having a variety of circuits and connecting wiring. For example, Figure 1 of *Murade II* discloses components on a TFT

substrate. *Murade II*, col. 13:61-64. In particular, *Murade II* Figure 1 depicts a liquid crystal apparatus 200 with a TFT array substrate 1. A POSITA would understand that the image display region is shown in the center portion of the figure as identified by the plurality of pixel electrodes 11. External input terminals 102 are shown disposed along a lower side of the TFT array substrate 1, which correspond to the claimed external circuit connection terminals. *Murade II* Figure 1 shows a plurality of wiring lines connected to the external input terminals 102. The plurality of wiring lines are designated with different names as shown along the bottom of the figure. For example, "a clock signal having a name 'CLX' is represented by 'clock signal CLX" and the corresponding signal wiring is represented by 'wiring CLX')." (e.g., CLX)." *Murade II*, col. 15:42-52. In *Murade II*, peripheral driving circuits drive the pixel portions via the wiring lines. In particular, *Murade II* discloses negative and positive power supplies that are supplied to the "scanning line driving circuits 104 from an external control circuit via the external input terminals 102 and further via wirings VSSY and VDDY." *Murade II*, col. 15:53-57.



Murade II Figure 1

179. Accordingly, it is my opinion that *Murade II* teaches this limitation of claim 1.

> **a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;**

180. A POSITA would understand *Murade II* to disclose a counter electrode on a counter substrate. *Murade II* describes its liquid crystal device as:

> A liquid crystal layer 50 is formed by putting a liquid crystal into a space which is surrounded by a sealing material 52 (refer to FIG. 13) between the TFT array substrate 1 and the opposite substrate 2 which are disposed so that the pixel electrodes 11 and the common electrode 21 face each other. When no electric field is applied from the pixel electrode 11 to the liquid crystal layer 50, the liquid crystal layer 50 is aligned in a predetermined direction determined by the alignment films 12 and 22. The liquid crystal layer 50 is made of, for example, one type of nematic liquid crystal or a

> mixture of two or more types of nematic liquid crystals. The sealing material 52 is an adhesive, such as a photo-curing resin or a thermal curing resin, by which the two substrates 1 and 2 are adhered to each other along their peripheries. The sealing material 52 contains a spacer by which the two substrates are spaced from each other by a predetermined distance.

Murade II, col. 28:13-29. *Murade II* further teaches that: "In FIGS. 1 to 3, a signal LCCOM is input as a power supply of a common electrode via an external input terminal 102, and supplied via an wiring LCCOM and also via the upper-to-lower conducting elements 106, described earlier, to a common electrode (refer to FIG. 10) provided on an opposite substrate." *Murade II*, col. 19:45-50.

181. Thus, Murade II teaches an electro-optical device 200 that includes a TFT substrate and an opposite substrate 2 that has electrode 21 formed on the opposite substrate 2. Opposite substrate 2 faces the TFT (or element) substrate as shown in *Murade II* Figure 13. *Murade II*, Fig. 13.

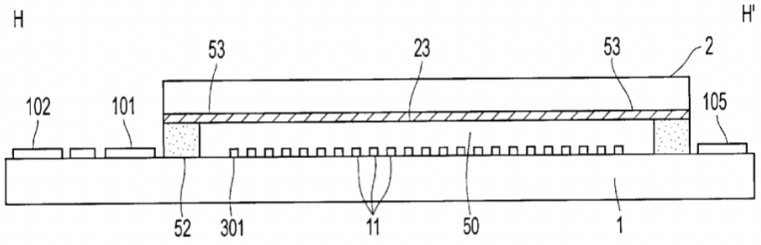
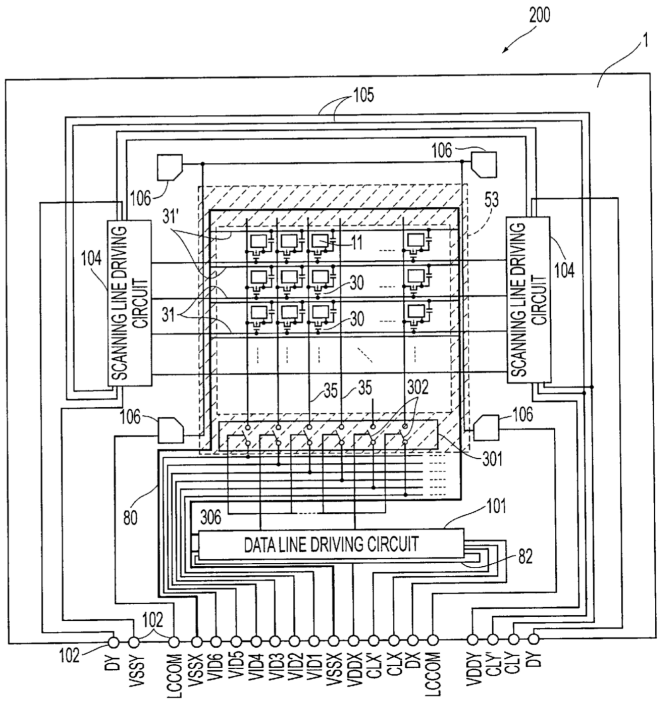


FIG. 13

182. Accordingly, it is my opinion that *Murade II* teaches and renders obvious this limitation of claim 1.

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

183. A POSITA would understand *Murade II* to teach a counter electrode potential line being connected to the counter electrode. *Murade II* discloses a counter electrode potential line. For example, *Murade II* describes a signal and wiring designated LCCOM as "a power supply of a common electrode." *Murade II*, col. 19:45-50. *Murade II* then describes how the LCCOM wiring supplies power via elements 106 on the TFT to a "common electrode provided on an opposite substrate." *Murade II*, col. 19:45-50; Fig. 1. As shown in Figure 1, LCCOM is one of the main wiring lines.

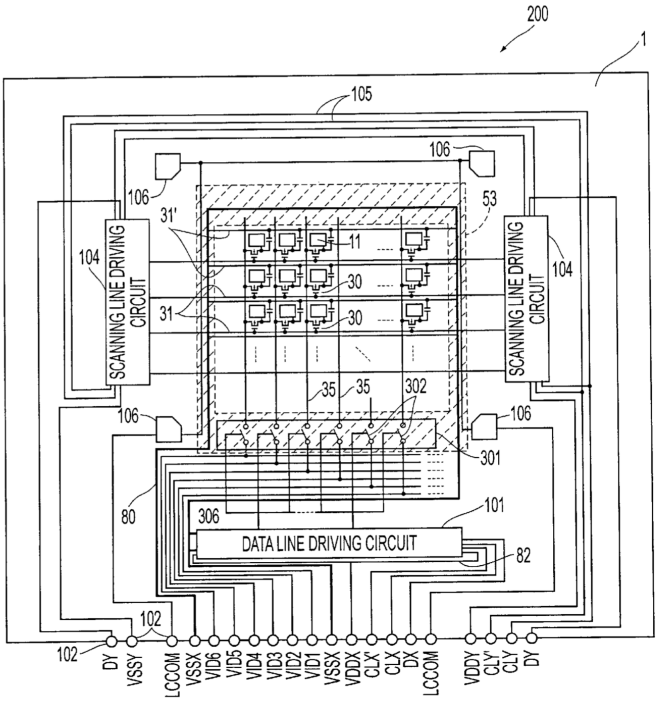


Murade II Figure 1

184. Accordingly, it is my opinion that *Murade II* teaches and renders obvious this limitation of claim 1.

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

185. A POSITA would understand *Murade II* to teach upper and lower conduction terminals that are connected to the counter electrode potential line. *Murade II* discloses upper-to-lower "conducting elements 106" at the four comers of the image display area as seen in *Murade II* Figure 1. *Murade II* describes these conducting elements as: "Upper-to-lower conducting elements 106 are disposed at four comers of the image display area so that the TFT array substrate 1 and the opposite substrate are electrically connected via the upper-to-lower conducting elements 106." *Murade II*, col. 15:38-42. In other words, the conducting elements 106 electrically connect the TFT substrate and opposite substrate. *Murade II*, col. 15:38-42. *Murade II* Figure 1 teaches the LCCOM line (counter potential electrode line) connects with conducting elements 106. *Murade II* Figure 1 is shown below with the LCCOM line leading to the conducting elements 106.



Murade II Figure 1

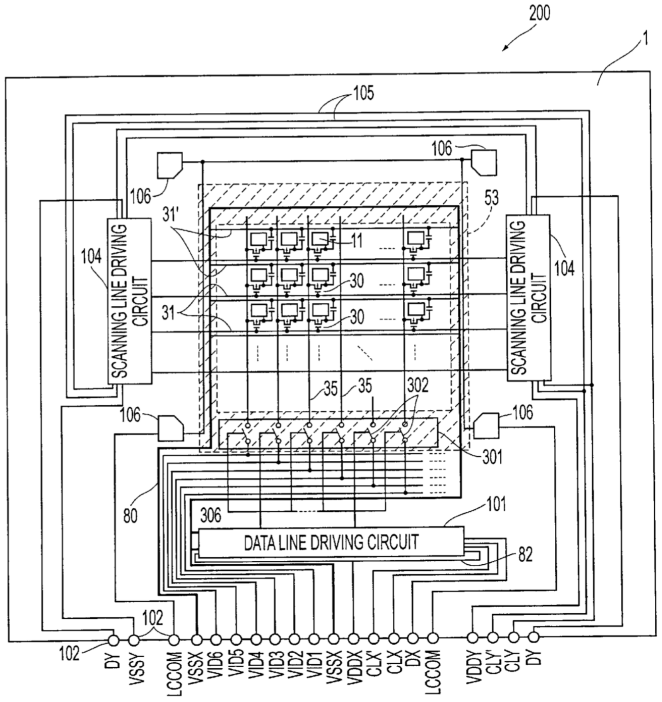
186. Accordingly, it is my opinion that *Murade II* teaches and renders obvious this limitation of claim 1.

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

187. A POSITA would understand *Murade II* to teach main wiring lines made out of a same conductive material that are laid out so that they do not intersect in the peripheral region. For example, *Murade II* discloses wiring lines that are made of a conductive film. For example, *Murade II* teaches that "wirings DY, VSSY, . . . , VDDX … are made of the same low-resistance metal material as that used to form the data lines 35, such as Al (aluminum)." *Murade II*, col. 19:20-24. These various wiring lines are the main wiring lines that are "connected to the

corresponding external input terminals 102" and are formed on the same layer (the first interlayer insulating layer 42 on the TFT array substrate 1). *Murade II*, col. 19:34-44. These wiring lines can thus be formed at the same time using the same low-resistance metal layer, such as an Al layer. *Murade II*, col. 19:34-44

188. In addition, *Murade II* discloses that these wiring lines are arranged so as not to intersect each other as seen in *Murade II* Figures 1-3, and 7(b). *Murade II* Figures 1-3, and 7(b) are shown below.



Murade II Figure 1

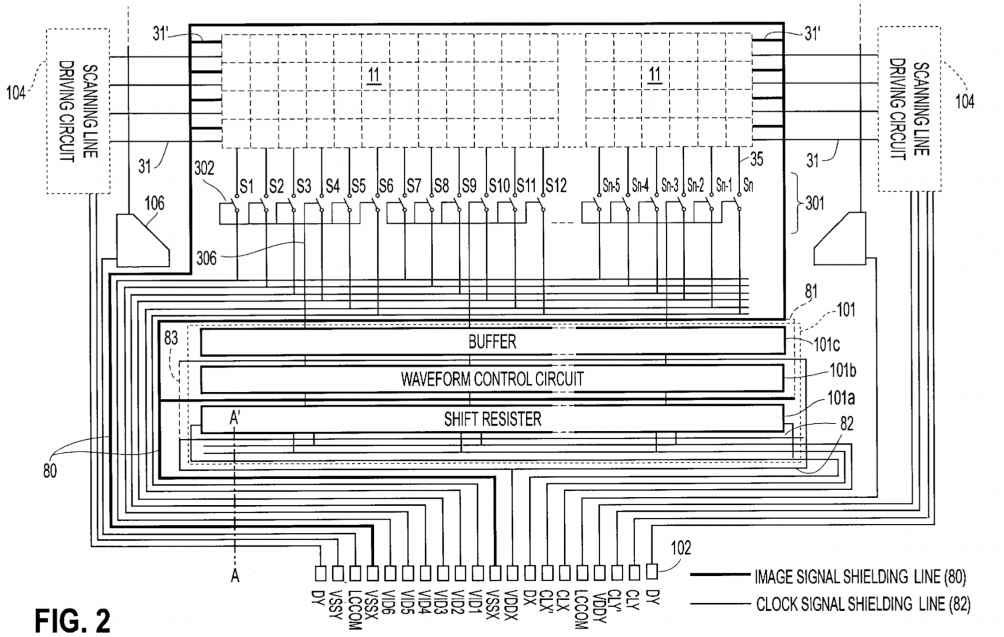
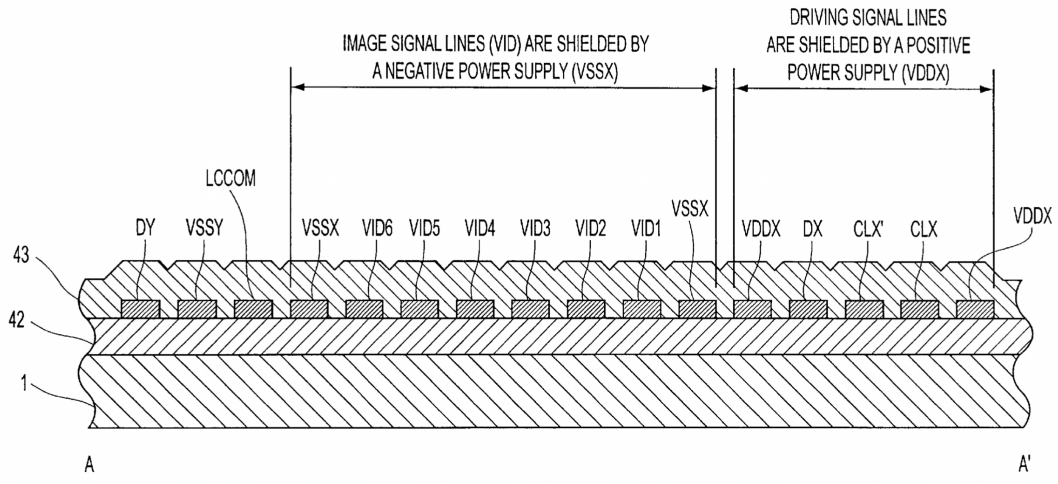


FIG. 2

Murade II Figure 2



Murade II Figure 3

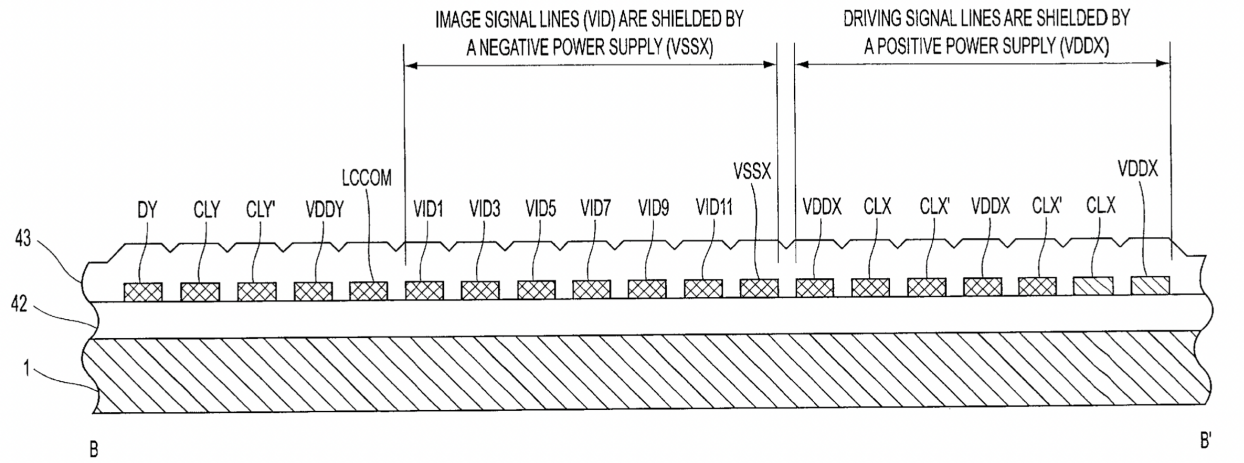


FIG. 7(b)

Murade II Figure 7

189. Accordingly, it is my opinion that *Murade II* teaches and renders obvious this limitation of claim 1.

> **the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.**

190. For the same reasons set forth above in regard to Ground 1 (*Muraide*), this limitation is obvious over *Murade II* as being a mere design choice. *Murade II* teaches a counter electrode potential line located nearer to the center of the substrate with respect to the scanning line drive circuit. It is a simple design choice to locate the counter electrode potential line nearer to the edge than the scanning line drive circuit that does not change any property or characteristics of the wiring layout, and thus, is obvious under §103.

191. Alternatively, as set forth above in Ground 1 (Section VI.B.1), *Sunao* discloses this limitation.

192. A POSITA would have found it obvious to combine *Murade II* and *Sunao*. Specifically, a POSITA would have found it obvious to implement *Sunao's* placement of the counter electrode potential line as closest to the edge of the substrate with *Murade II's* display device. *Id*. A POSITA would have been motivated to combine *Sunao's* placement of the counter electrode potential line with *Murade II's* display device in order to further isolate the electrode potential line from the other wirings and the display area. *Id*. This combination would have allowed the device of *Murade II* to potentially further miniaturize. Further, as both *Murade II* and *Sunao* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Sunao's* placment with *Murade II's* display device. Finally, as both references relate to LCDs and describe similar functions combining the design of *Sunao* into *Murade II's* display device would have yielded predictable results. *Id*.

193. Alternatively, as set forth above in Ground 1 (Section VI.B.1), *Komeno* discloses this limitation.

194. A POSITA would have found it obvious to combine *Murade II* and *Komeno*. Specifically, a POSITA would have found it obvious to implement *Komeno's* placement of the of the counter electrode potential line as closest to the edge of the substrate with *Murade II's* display device. *Id*. A POSITA would have been motivated to combine *Komeno's* placement of the counter electrode potential

line with *Murade II's* display device in order to further isolate the electrode potential line from the other wirings and the display area. *Id*. This combination would have allowed the device of *Murade II* to potentially further miniaturize. Further, as both *Murade II* and *Komeno* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Komeno's* placement of the counter electrode potential line with *Murade II's* display device. Finally, as both references relate to LCDs and describe similar functions combining the design of *Komeno* into *Murade II's* display device would have yielded predictable results. *Id*.

195. Accordingly, it is my opinion that *Murade II* in combination with either *Sunao* or *Komeno* teaches and renders obvious this limitation of claim 1.

2. Claim 4

Claim 4 depends from claim 1 with the further limitation:

> **the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.**

196. As set forth above in Ground 1 (Section VI.B.4), *Sunao* discloses this limitation. For the reasons set forth above in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Sunao*.

197. As set forth above in Ground 1 (Section VI.B.4), *Komeno* discloses this limitation. For the reasons set forth above in claim 1 of this Ground (Section

VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Komeno.*

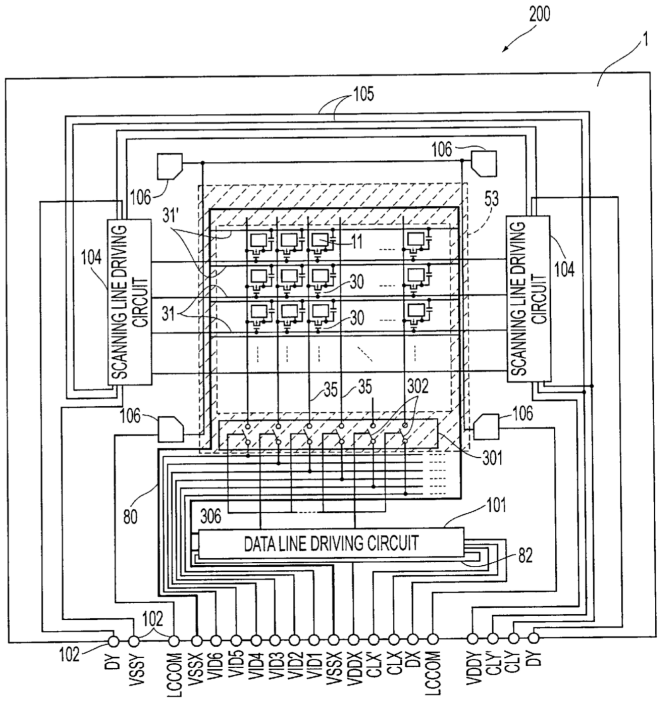
198. Accordingly, it is my opinion that *Murade II* in combination with either *Sunao* or *Komeno* teaches and renders obvious claim 4.

3. Claim 5

Claim 5 depends from claim 4 with the further limitation:

> **the plurality of external circuit connection terminals being arranged along one side of the element substrate, and**
>
> **the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.**

199. A POSITA would understand that *Murade II* teaches external connection terminals along one edge of a substrate, with one such terminal being connected to a counter electrode potential line. *Murade II* teaches external circuit connection terminals ("external input terminals 102 in *Murade II)* as being disposed along one side of the TFT array substrate. *Murade II* further discloses an external connection terminal ("external input terminal 102") being coupled to the counter electrode potential line ("LCCOM"). *Murade II*, col. 19:45-50. As seen in *Murade II* Figures 1-3, LCCOM is the third external input terminal at the left end of the substrate. *Murade II* Figures 1-3 are shown below.



Murade II Figure 1

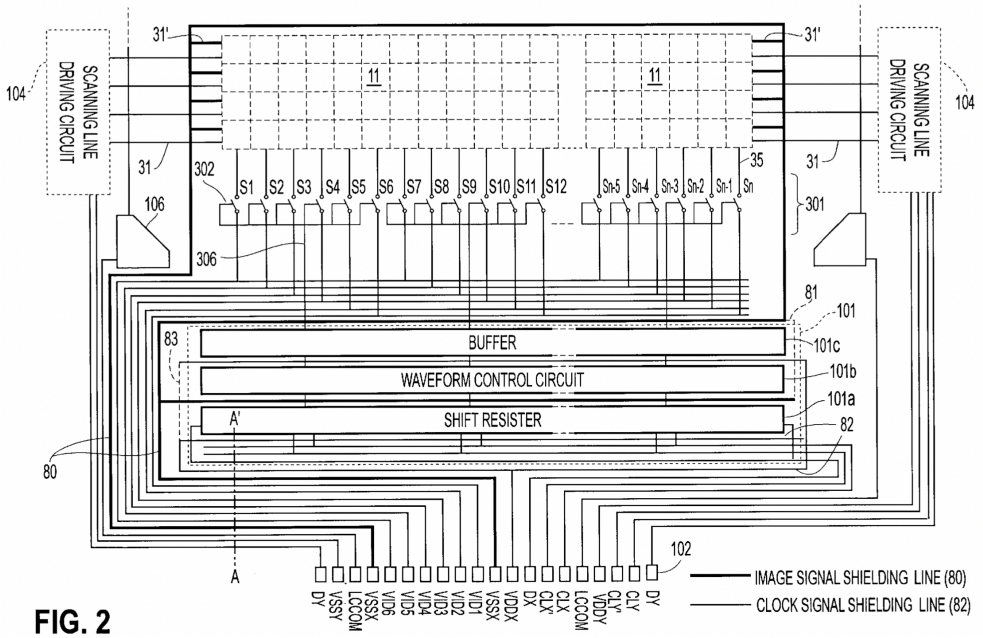
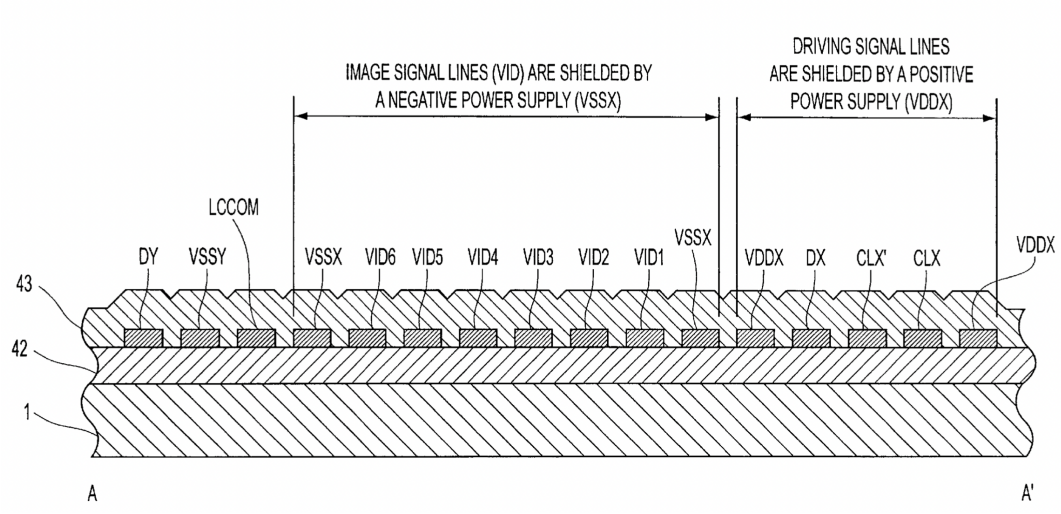


FIG. 2

Murade II Figure 2

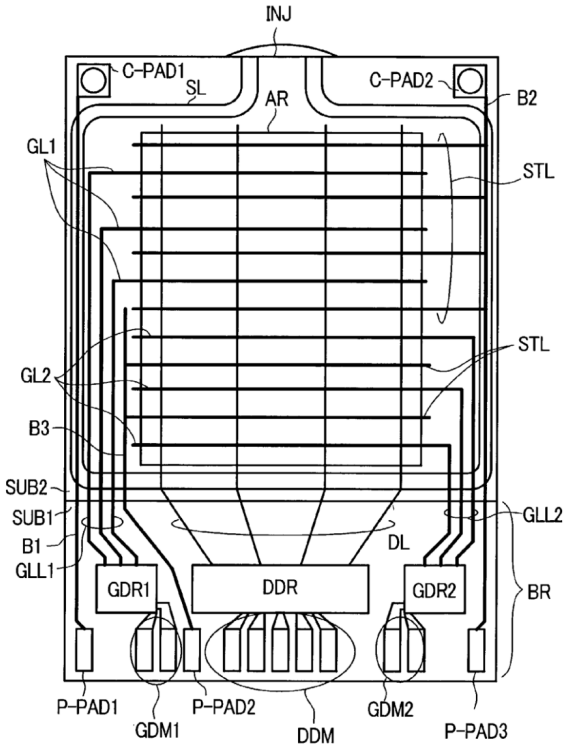


Murade II Figure 3

200. Alternatively, *Komeno* discloses this limitation.

201. As shown in *Komeno* Figure 1, a plurality of external connection terminals are arranged along the lower edge of the figure. *Komeno* teaches that counter electrodes are connected to the feeding pads P-PAD1, P-PAD3 formed on the driving circuit mounting region BR through counter electrode connection pads C-PAD1, C-PAD2 formed on corner portions of an upper side of the first substrate SUB1 and common lines B1, B2. Electricity is supplied through the feeding pads P-PAD1, P-PAD3. *Komeno*, ¶[0108]-[0110]; Fig. 1. Accordingly, *Komeno* teaches external circuit connection terminals P-PAD1 and P-PAD3, which are coupled to one end of the counter electrode potential lines B1 and B2, that are near the end of an array of the plurality of external circuit connection terminals. In particular, they are located at the position closest to the left and right edges of the substrate as seen in Figure 1. *Komeno*, ¶[0108]; Fig. 1.

FIG. 1



Komeno Figure 1

202. For the reasons set forth above in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Komeno*.

203. Accordingly, it is my opinion that *Murade II* alone or in combination with *Komeno* teaches and renders obvious claim 5.

4. Claim 6

Claim 6 depends from claim 4 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

204. A POSITA would understand that *Murade II* teaches clock signal lines and power source lines that do not intersect. *Murade II* specifically discloses a "reference clock signal CLY for the scanning line driving circuit and an inverted clock signal CLY′ thereof." *Murade II*, col. 15:60-62. Further, *Murade II* discloses a predetermined timing based on these clock signals (CLY, CLY′): "the scanning line driving circuits 104 apply a scanning signal in the form of a pulse to the scanning lines 31, line by line." *Murade II*, col. 15:60-65. *Murade II* further discloses an external connection terminal ("external input terminal 102") being coupled to the counter electrode potential line ("LCCOM"). *Murade II*, col. 19:45-50. As seen in *Murade II* Figures 1-3, LCCOM is the third external input terminal at the left end of the substrate. Thus, *Murade II* also discloses a counter electrode potential line (LCCOM). *Murade II*, col. 19:45-50.

205. *Murade II* Figures 2 and 3 disclose laying out the clock signal lines in a configuration where they do not intersect the counter electrode potential line. *Murade II* Figures 2 and 3 are shown below.

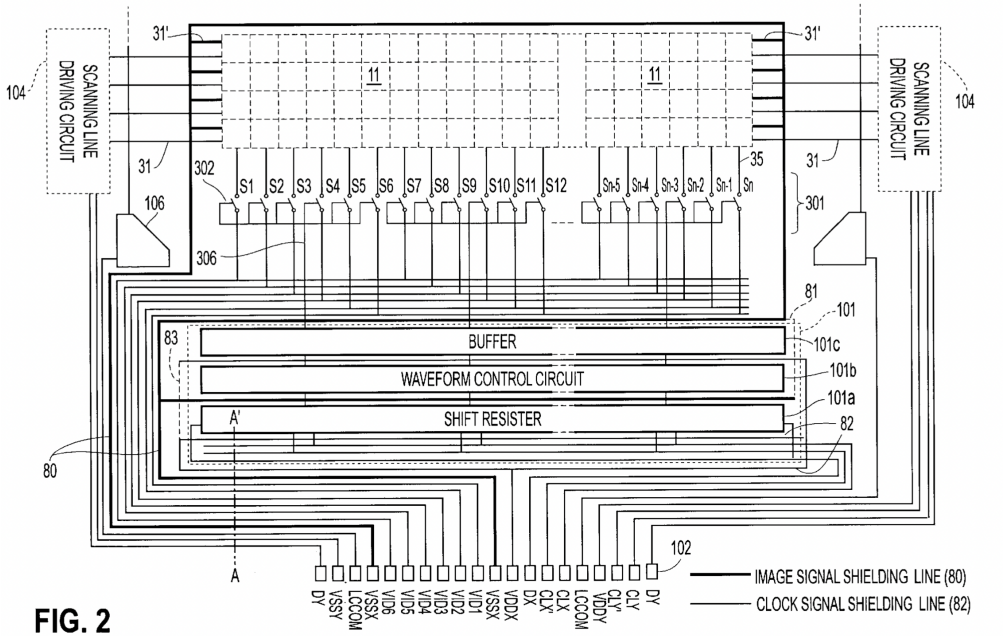
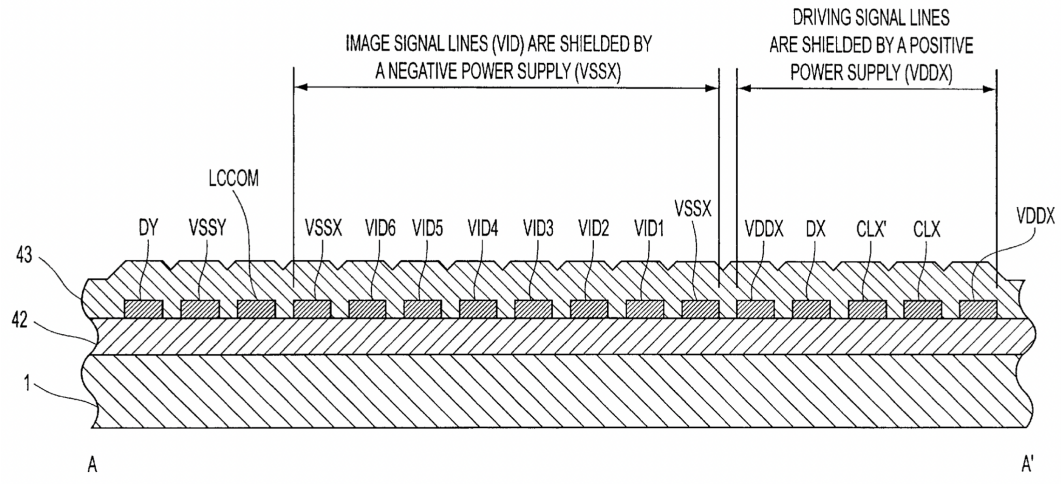


FIG. 2

Murade II Figure 2



Murade II Figure 3

206. Accordingly, it is my opinion that *Murade II* teaches claim 6.

5. Claim 7

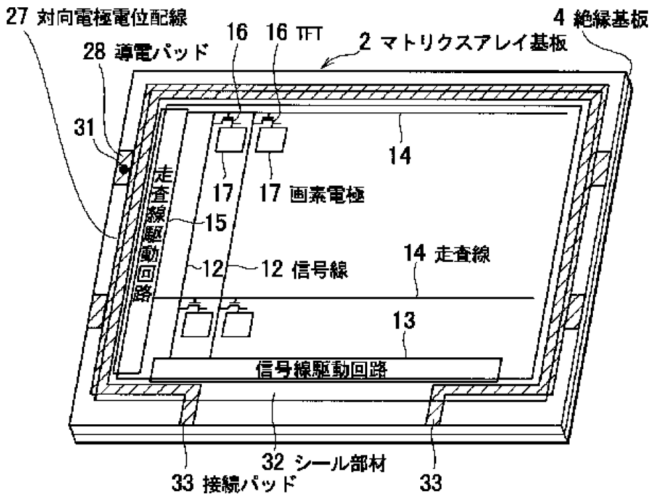
Claim 7 depends from claim 1 with the further limitation:

a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

207. A POSITA would understand that claim 7's requirement that parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region contradicts claim 1's requirement that "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Further, the '390 patent does not appear to disclose any such structure.

208. Despite this inconsistency, a POSITA would understand that *Sunao* discloses upper and lower conduction terminals and a counter electrode potential line that are closer to the center of the display than at least one of the driving circuits. In *Sunao*, the scanning line driving circuit 15 is nearer to the center of the element substrate than the conductive pads 28. In addition, the signal line driving circuit 13 is nearer to the lower edge of the element substrate than the conductive pads 28.

【図３】



Sunao Figure 3

209. For the reasons set forth above in claim 1 of this Ground (Section VI.E.1), a POSITA would have been motivated to combine *Murade II* and *Sunao.*

210. Accordingly, it is my opinion that *Murade II* in combination with *Sunao* teaches and renders obvious claim 7.

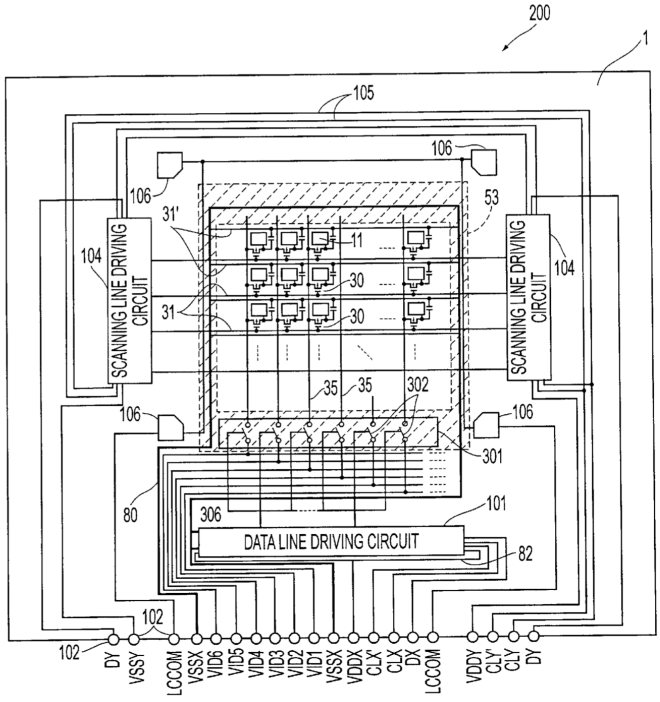
6. Claim 8

Claim 8 depends from claim 7 with the further limitation:

> **the plurality of external circuit connection terminals being arranged along one side of the element substrate, and**
>
> **the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.**

211. As claim 8 depends from claim 7, it suffers from the same inconsistencies with claim 1.

212. A POSITA would understand that *Murade II* teaches external connection terminals in a row, at least one of which is connected to the other or one end of the plurality of main wiring lines and positioned near the end of the row of connection terminals. As seen in *Murade II* Figures 1-3, *Murade II* teaches external circuit connection terminals ("external input terminals 102 in *Murade II)* as being disposed along one side of the TFT array substrate. *Murade II* further teaches an external connection terminal ("external input terminal 102") being connected to the other end or one end of plurality of main wiring lines, for example, LCCOM. *Murade II*, col. 19:45-50. As seen in *Murade II* Figures 1-3, LCCOM is the third external input terminal at the left end of the substrate. *Murade II* Figures 1-3 are shown below.



Murade II Figure 1

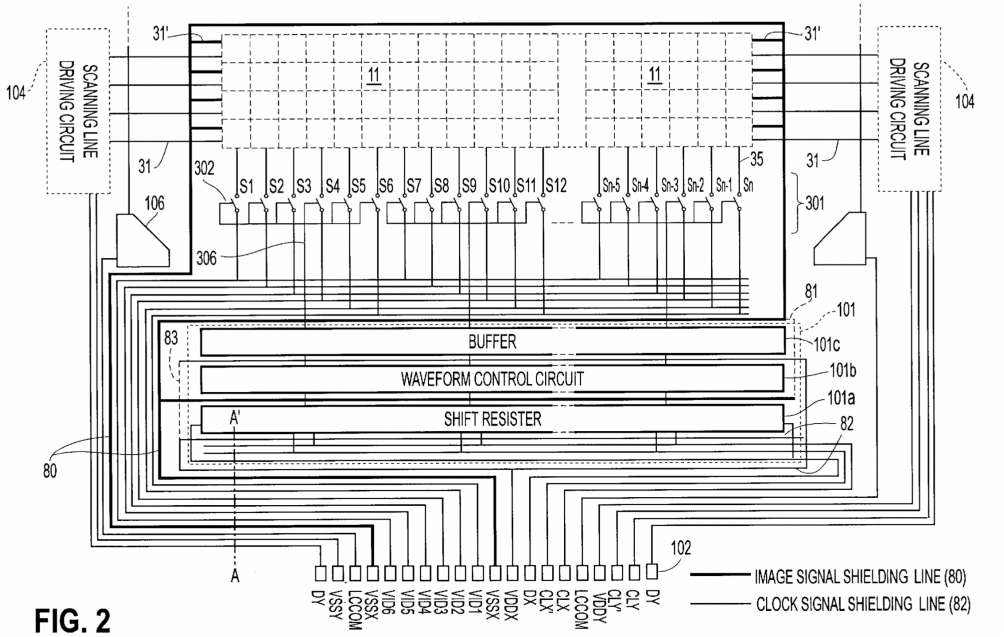
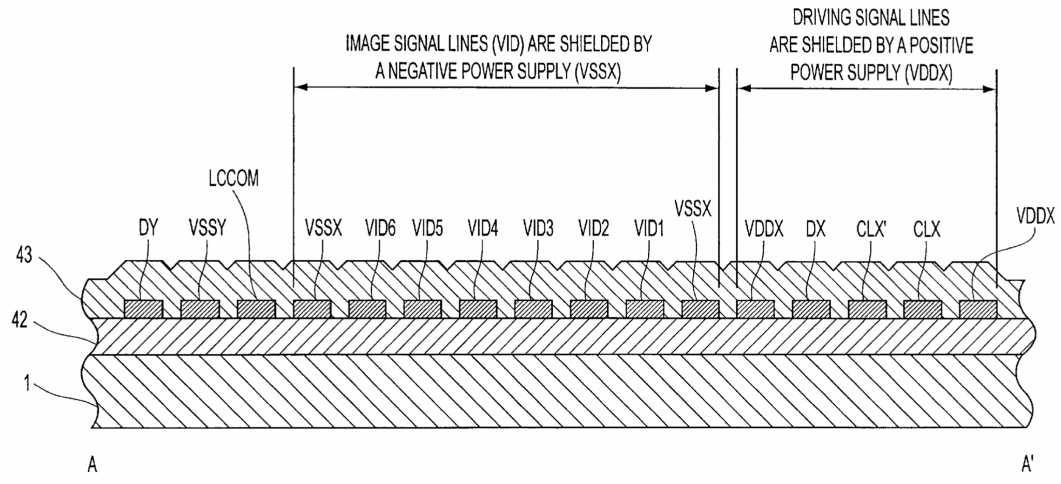


FIG. 2

Murade II Figure 2



Murade II Figure 3

213. Accordingly, it is my opinion that *Murade II* teaches claim 8.

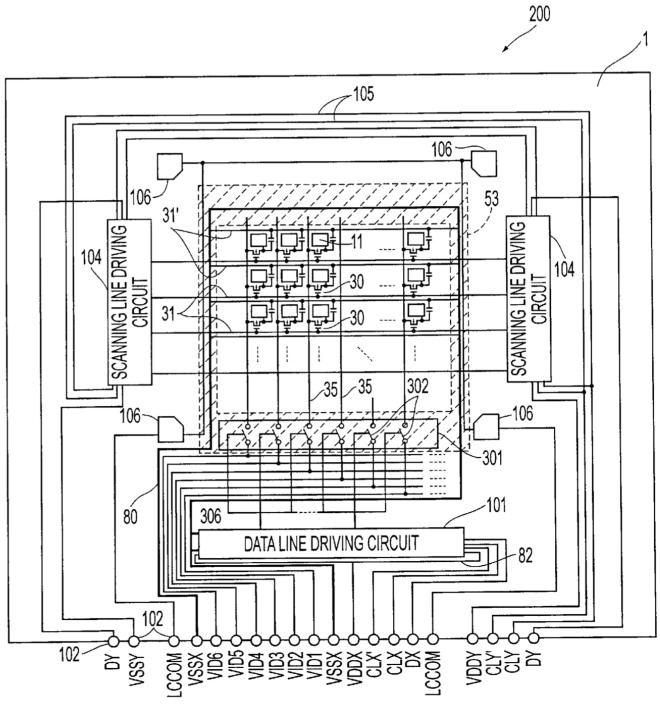
7. Claim 9

Claim 9 depends from claim 7 with the further limitation:

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

214. As claim 9 depends from claim 7, it suffers from the same inconsistencies with claim 1.

215. A POSITA would understand that *Murade II* teaches a clock signal and an inverse clock signal. For example, *Murade II* discloses a plurality of main wiring lines that includes a clock signal (CLY) and an inverse clock signal (CLY′). *Murade II*, col. 15:60-65. *Murade II* further discloses a "a signal LCCOM is input as a power supply of a common electrode via an external input terminal 102, and supplied via an wiring LCCOM and also via the upper-to-lower conducting elements 106, … to a common electrode (refer to FIG. 10) provided on an opposite substrate." *Murade II*, col. 19:45-50. *Murade II* teaches that these lines do not intersect each other. For example, Figures 1 and 2 show no intersection between the clock signal lines and the power source wiring line (LCCOM). *Murade II* Figures 1 and 2 are shown below.



Murade II Figure 1

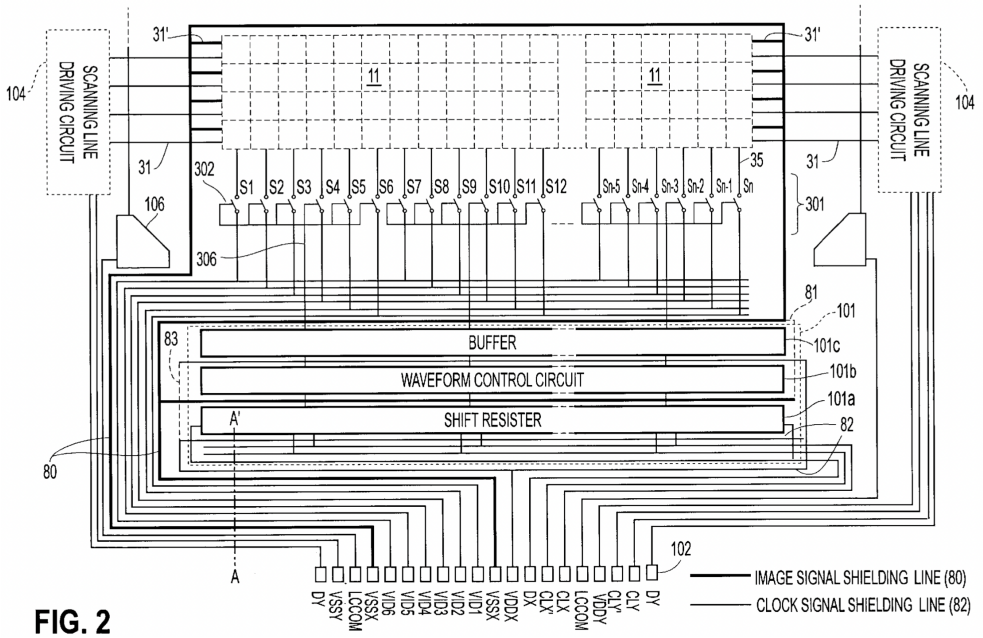


FIG. 2

Murade II Figure 2

216. Accordingly, it is my opinion that *Murade II* teaches claim 9.

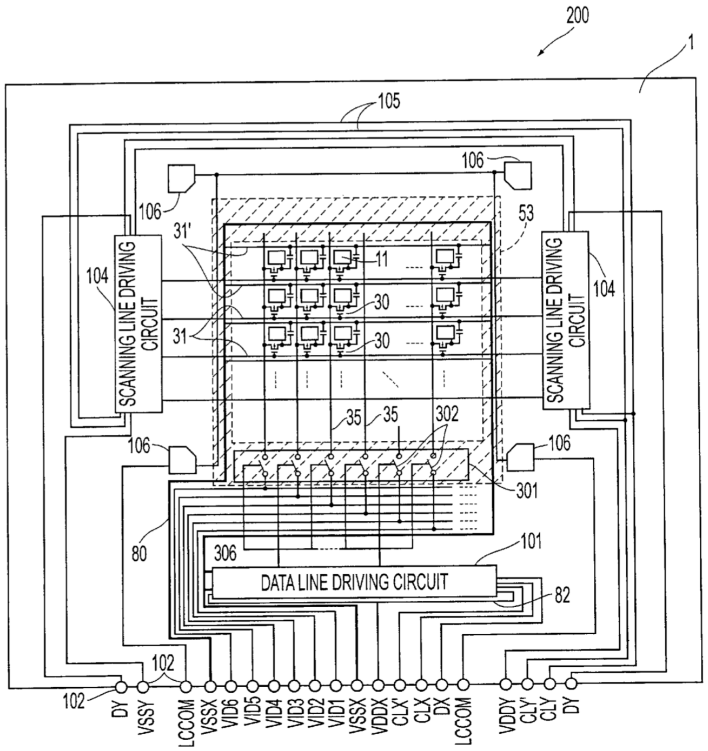
8. Claim 10

Claim 10 depends from claim 1 with the further limitation:

> **the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals and power source wiring lines that supply power source signals as electric signals, and**
>
> **the pair of signal lines and power source wiring lines do not intersect each other.**

217. A POSITA would understand that *Murade II* teaches clock signal lines and power source lines that do not intersect. *Murade II* discloses a plurality of main wiring lines that includes a clock signal (CLY) and an inverse clock signal (CLY′). *Murade II*, col. 15:60-65. Further, *Murade II* discloses a "a signal LCCOM is input as a power supply of a common electrode via an external input terminal 102, and supplied via an wiring LCCOM and also via the upper-to-lower conducting elements 106, … to a common electrode (refer to FIG. 10) provided on an opposite substrate." *Murade II*, col. 19:45-50.

218. *Murade II* teaches that these lines do not intersect each other. For example, Figures 1 and 2 show no intersection between the clock signal lines and the power source wiring line (LCCOM). Figures 1 and 2 are shown below.



Murade II Figure 1

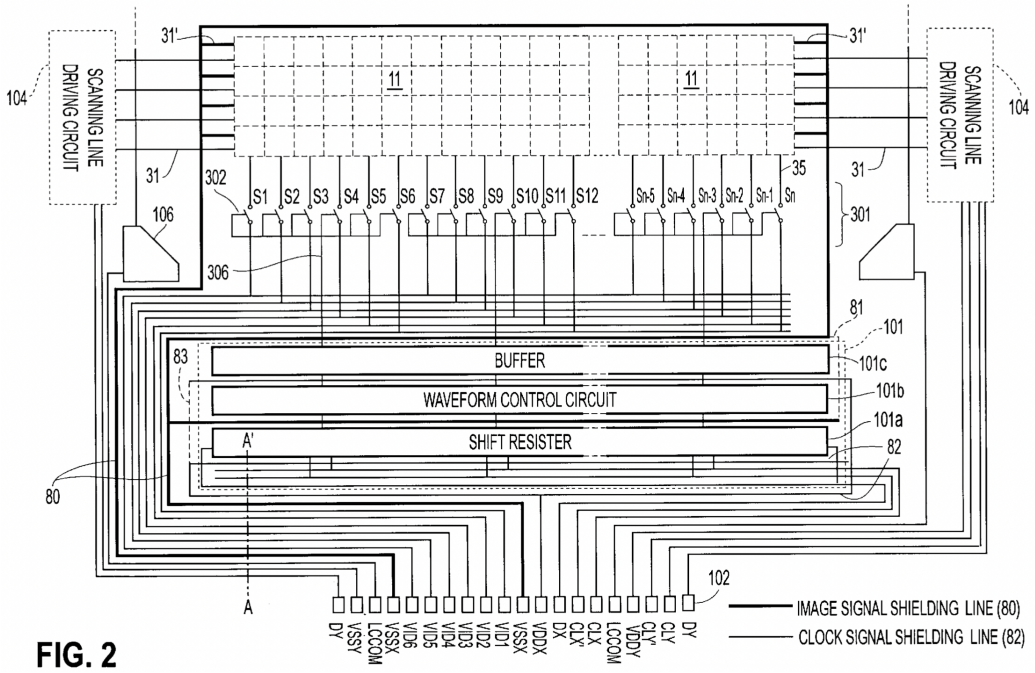


FIG. 2

Murade II Figure 2

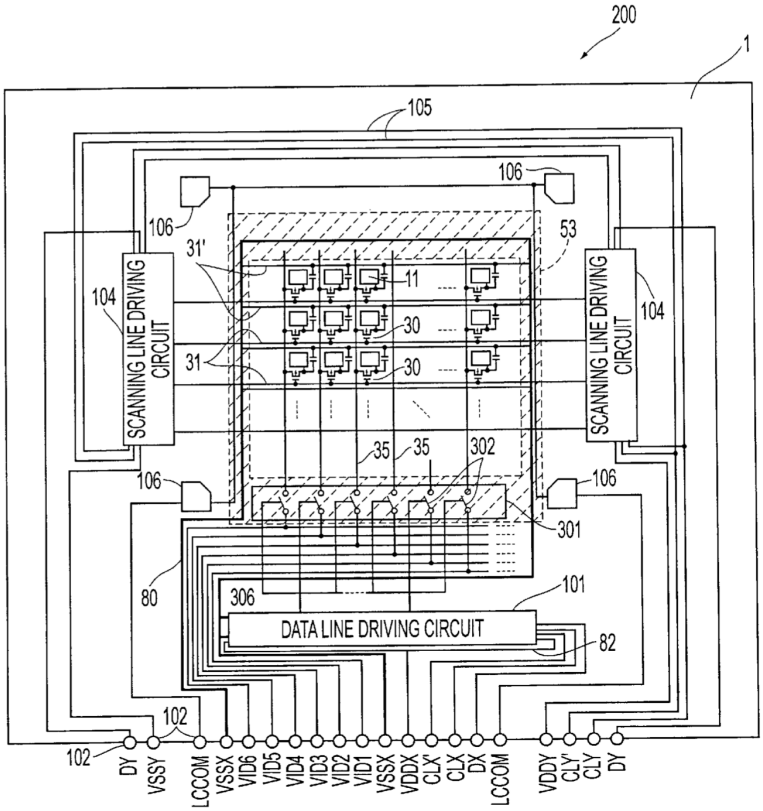
219. Accordingly, it is my opinion that *Murade II* teaches claim 10.

9. Claim 11

Claim 11 depends from claim 1 with the further limitation:

> **the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.**

220. A POSITA would understand *Murade II* to teach main wiring lines made out of a same conductive material that are laid out so that they do not intersect in the peripheral region. As shown in *Murade II* Figure 1, the signal lines are planarly laid out in same layer and routed to zig-zag around each other in order to avoid intersection at the same layer. *Murade II*, Figs. 1, 3.



Murade II Figure 1

221. Accordingly, it is my opinion that *Murade II* teaches claim 11.

10. Claim 13

An electronic apparatus, comprising the electro-optical device according to claim 1.

222. A POSITA would understand that *Murade II* teaches both an electronic apparatus and an electro-optical device. *Murade II* specifically discloses that: "Examples of electronic devices including the electro-optical apparatus 200 are described below with reference to FIGS. 14-18." *Murade II*, col. 33:39-41. *Murade II* then describes examples of a projector, laptop computer and pager as apparatuses for use with its electro-optical device. *Murade II*, Figs. 15-18. *Murade II* further discloses: "In addition to the electronic devices described above with reference to FIGS. 15-18, there are other examples of the electronic device shown in FIG. 14. They include a liquid crystal television set, a view-finder type or monitor direct view type video tape recorder, a car navigation system, a pocket-sized electronic notebook, an electronic calculator, a word processor, an engineering workstation (EWS), a portable telephone, a video telephone, a POS terminal, and an apparatus with a touch panel." *Murade II*, col. 35:29-37.

223. Accordingly, it is my opinion that *Murade II* teaches claim 13.

F. Ground 5: *Murade II* in Combination with *Sunao* or *Komeno* and in Further Combination with *Murade III* Renders Obvious Claims 2, 3 and 12.

1. Claim 2

Claim 2 depends from claim 1 with the further limitation:

sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

224. A POSITA would understand *Murade III* to disclose first and second portions of sub-wiring lines made of different conductive films that were laid out so as not to intersect with each other. *Murade III* teaches:

> As shown in FIGS. 4 and 5, the sampling circuit 103 is disposed in the area inside the sealing area and under the third light blocking film 53 (denoted by the hatching lines slanted to right in the figures) which is disposed on the opposite substrate 20, so as to serve as a partition for defining the boundary between the image displaying area and the outer area. In a part of the sealing area where extensions of the data lines 6 a extend, there are provided leading wirings 301 including leading wirings 301 a of the sampling circuit driving signal lines 114 extending from the data line driving circuit 101, and also including leading wirings 301 b of the image signal lines 115. On the other hand, in a part of the sealing area where extensions of the scanning lines 3 a extend, there are provided leading wirings 401 a of the scanning lines 3 a extending from the scanning line driving circuit 104. The leading wirings 401 may include an opposite electrode (common electrode) voltage line 112 disposed at an end of the lead wirings 401 and the leading wirings 401 b of the capacitance line 3 b.

Murade III, col. 18:38-65.Figures 5 and 6 of *Murade III* (below) depict this arrangement.

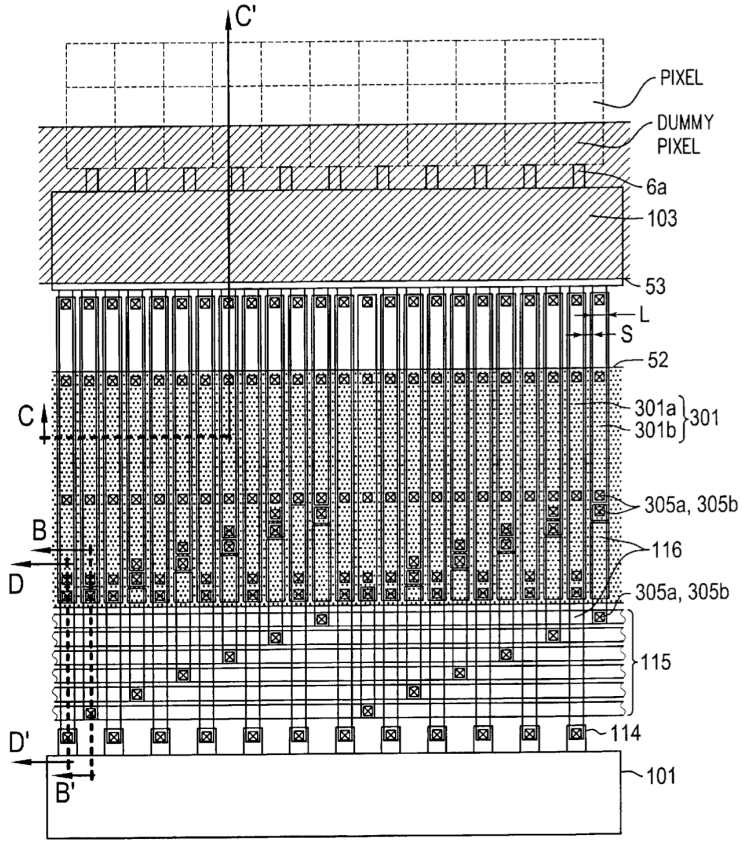


Fig. 5

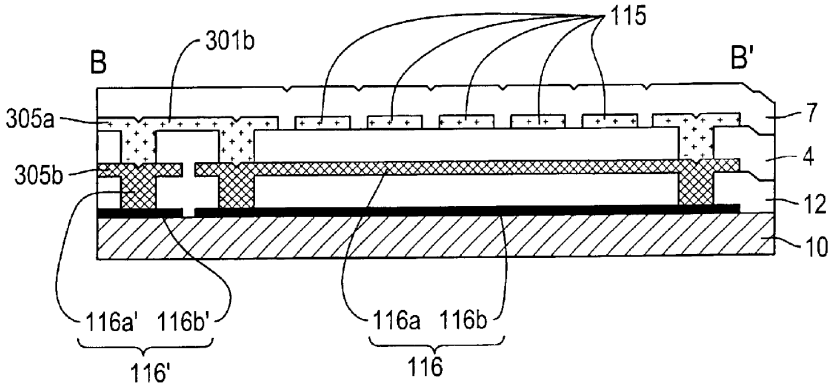


Fig. 6

225. As seen above, Figure 5 shows sub-wiring lines, including lines 301 consisting of line 301a of the sampling circuit driving signal lines 114 extending from the data line driving circuit 101, and 301b of the image signal lines 115.

Murade III, col. 18:38-65. Figure 6 shows "image signal lines 115, which are examples of peripheral wirings and leading wirings 301b, are formed using a single metal film." *Murade III*, col. 18:66-19:2.

226. A POSITA would understand Figures 5 and 6 to show that for the data line drive circuit 101, the first portions include the interconnecting lines 116, which are arranged to intersect with the signal lines 115 through the interlayer insulating film 4. Further, the second portions include the leading wirings 301b, which are formed at the same layer as the signal lines 115 and are arranged not to intersect with the signal lines 115.

227. A POSITA would understand that *Murade III* specifically discloses first and second portions made of different conductive films. *Murade III* describes interconnecting lines 116 extending from signal lines 115 to leading wirings 301b (shown in Figure 6) "are formed in the two-layer structure when viewed in the thickness direction of the TFT array substrate, wherein one layer is realized with the second conductive film 116a, and the other layer is realized with the first conductive film 116b." *Murade III*, col. 19:4-13.

228. A POSITA would have found it obvious to combine *Murade II* and *Murade III*. Specifically, a POSITA would have found it obvious to implement *Murade III's* sub-wiring line structure made of two different conductive films and separated by interlayer insulating film with *Murade II's* display device. *Id*. A

POSITA would have been motivated to combine *Murade III's* structure with *Murade II's* display device in order to further isolate the sub-wiring lines. *Id*. This combination would have allowed the device of *Murade II* to potentially further miniaturize. Further, as both *Murade II* and *Murade III* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Murade III's* structure with *Murade II's* display device. Finally, as both references relate to LCDs and describe similar functions combining the design of *Murade III* into *Murade II's* display device would have yielded predictable results. *Id*.

229. Accordingly, it is my opinion that *Murade II* in combination with *Murade III* teaches and renders obvious claim 2.

2. Claim 3

Claim 3 depends from claim 2 with the further limitation:

> **the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.**

230. A POSITA would understand that *Murade III* teaches that the first and second portions of its sub-wiring lines are connected via contact holes. *Murade III* discloses:

> The interconnecting lines 116, which extend from the image signal lines 115 to the leading wirings 301 b, are formed in the two-layer structure when viewed in the thickness direction of the TFT array substrate, wherein one layer is realized with the second conductive film 116 a, which is made of the same film as the polysilicon film used to form the scanning line 3 a, and which is electrically

> connected via the contact hole 305 a to the corresponding image signal line 115, and the other layer is realized with the first conductive film 116 b, which is made of the same film as the first light blocking film 11 a, and which is electrically connected via the contact hole 305 b to the corresponding interconnecting line 116 a. In order to further reduce the resistance of the leading wirings 301 b, the leading wirings 301 b may be coupled with the second conductive film 116 a′ and the first conductive film 116 b′.

Murade III, col. 19:4-29.

231. As shown in Figure 6 below, a contact hole that electrically couples the first and second portions of sub-wiring lines.

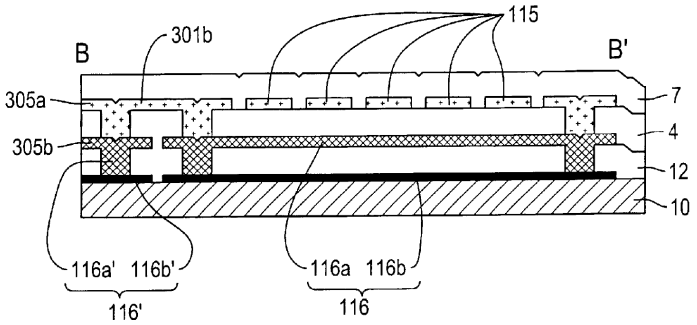


Fig. 6

232. As seen in Figure 6, contact hole 305b electrically connects the second conductive film 116a to the leading wiring 301b, which are formed in the second interlayer insulating film 4 during the process of forming the contact hole 5. *Murade III*, col. 26:66-27:3.

233. A POSITA would have combined *Murade II* and *Murade III* for the reasons set forth in claim 2 above.

234. Accordingly, it is my opinion that *Murade II* in combination with *Murade III* teaches and renders obvious claim 3.

3. Claim 12

Claim 12 depends from claim 1 with the further limitation:

> **the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film.**

235. A POSITA would understand that *Murade III* teaches main wiring lines wherein at least some of the main wiring lines are redundant and composed of different conductive film. *Murade III* specifically discloses "the interconnecting lines 116 have a redundant structure" that is implemented via two different conductive films. *Murade III*, col. 19:51-56; Fig. 6. *Murade III* further discloses multilayer wirings where the different wirings are made of the same film as the conductive film of their respective layers. *Murade III*, col. 5:14-25.

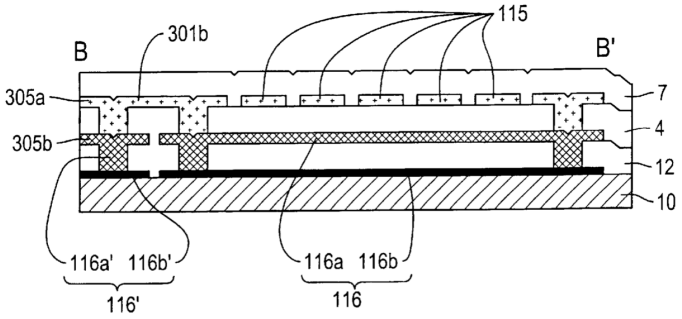


Fig. 6

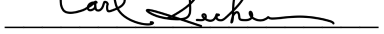
236. A POSITA would have combined *Murade II* and *Murade III* for the reasons set forth in claim 2.

237. Accordingly, it is my opinion that *Murade II* in combination with *Murade III* teaches and renders obvious claim 12.

VII. Conclusion

238. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

239. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 30 January 2023 By: 
Carl Sechen, Ph.D.