AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-382	9/30/2022	Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
CRYSTAL LEAP ZRT	HKC CORP. LTD.; CHONGQING HKC OPTOELECTRONICS TECHNOLOGY CO., LTD.; HKC OVERSEAS LTD.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,116,390	10/3/2006	Crystal Leap Zrt
2	7,335,913	2/26/2008	Crystal Leap Zrt
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

HKC EXHIBIT 1004

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 06/12/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/852,255	05/25/2004	Masao Murade	119570	4122

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	09/12/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH NHAN P	2871	349-149000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oliff & Berridge, PLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

08/31/2006 MBERHE1 00000018 10852255

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)	
Seiko Epson Corporation	Tokyo, Japan	01 FC:1501 1400.00 OP 02 FC:1504 300.00 OP

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

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- ☒ A check in the amount of the fee(s) is enclosed. **Check No. 183534 ($1700)**
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 15-0461 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date August 29, 2006

Typed or printed name Linda M. Saltiel Registration No. 51,122

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

25944 7590 06/12/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
NGUYEN, THANH NHAN P	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/12/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/852,255	05/25/2004	Masao Murade	119570	4122

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	09/12/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 06/12/2006

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/852,255	05/25/2004	Masao Murade	119570	4122

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	09/12/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH NHAN P	2871	349-149000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/852,255	05/25/2004	Masao Murade	119570	4122

25944 7590 06/12/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
NGUYEN, THANH NHAN P	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/12/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 113 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 113 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/852,255	MURADE, MASAO	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P. Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/15/2006*.

2. ☒ The allowed claim(s) is/are *1-12 and 16*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/15/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed on February 15, 2006 has been considered.

Drawings

The drawings were received on February 15, 2006. These drawings are acceptable.

Allowable Subject Matter

Claims 1-12 and 16 are allowed.

Reasons for Allowance

Claims 1-12 and 16 are allowable since there is no prior art of record that teaches or suggests an electro-optical device comprising a relationship of various elements as claimed with the specific allowable subject matter cited in the following claim:

Claim 1:

- in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines

- the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region
- the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines

Claims 2-12 and 16 are allowed since they depend on the allowed claim 1.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Muraide (JP 2002-049052) discloses an electro-optical device with almost every limitations as present invention claimed except a counter electrode potential line not being closest to edges of the element substrate, among the plurality of main wiring lines.

Murade (US 6,531,996) discloses an electro-optical apparatus (similarly as above reference.)

Yamazaki et al (US 6,011,607) discloses a liquid crystal display device comprising a peripheral driver circuit located inside a sealing material layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen
Examiner
Art Unit 2871

TN

David Nelms
Supervisory Patent Examiner
Technology Center 2800

OIPE IAP13 FEB 15 2006 PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 1/06) US Dept. of Commerce & TRADEMARK OFFICE	ATTY DOCKET NO. 119570	APPLICATION NO. 10/852,255
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Masao MURADE	
	FILING DATE May 25, 2004	GROUP 2871

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
TN	1.	2002/0171638 A1	11/21/2002	Ishiyama
TN	2.	6,979,839 B2	12/27/2005	Murade

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
TN	3.	KR A 2001-0105272 (corresponds to reference 2)	11/28/2001	Korea		
TN	4.	KR A 2002-0082425 (corresponds to reference 1)	10/31/2002	Korea		

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
	5/13/06

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: February 15, 2006

Notice of References Cited	Application/Control No. 10/852,255	Applicant(s)/Patent Under Reexamination MURADE, MASAO	
	Examiner (Nancy) Thanh-Nhan P. Nguyen	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,531,996	03-2003	Murade, Masao	345/98
*	B	US-6,011,607	01-2000	Yamazaki et al.	349/153
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 2002049052 A	02-2002	Japan	MURAIDE, MASAO	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PAT-NO: JP02002049052A

DOCUMENT-IDENTIFIER: JP 2002049052 A

TITLE: ELECTROOPTICAL DEVICE

PUBN-DATE: February 15, 2002

INVENTOR-INFORMATION:

NAME	COUNTRY
MURAIDE, MASAO	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SEIKO EPSON CORP	N/A

APPL-NO: JP2000236195

APPL-DATE: August 3, 2000

INT-CL (IPC): G02F001/1345 , G02F001/133 , G02F001/1368 , G09F009/00 , G09F009/30 , G09G003/20 , G09G003/36

ABSTRACT:

PROBLEM TO BE SOLVED: To display a high quality picture in an electrooptical device such as a liquid crystal device by reducing noise in signals on a signal line arranged on a peripheral region of a substrate with relatively simple construction of the device.

SOLUTION: The electrooptical device is provided with a pixel electrode (9a), a TFT(thin film transistor 30) connected thereto and a capacitive line (300) on a picture display region of a TFT array substrate (10) and further is

provided with a data line (6a) and a scanning line (3a) connected to the TFT. In the peripheral region a peripheral circuit including a circuit related to data line driving, a signal line (400) connected thereto and composed of the same film as the capacitive line, and a shield (401a) electrically screening the line (400) from at least a direction and composed of the same film as the data line are provided.

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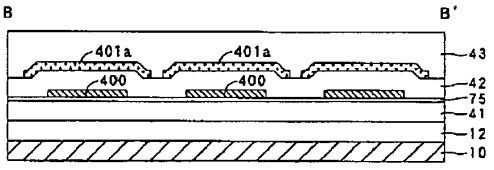
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(54)【発明の名称】　電気光学装置

(57)【要約】
【課題】　液晶装置等の電気光学装置において、比較的簡単な装置構成により、基板上の周辺領域に設けられた信号線上の信号におけるノイズを低減し、高品位の画像表示を行なう。
【解決手段】　電気光学装置は、ＴＦＴアレイ基板（１０）上の画像表示領域に、画素電極（９ａ）と、これに接続されたＴＦＴ（３０）及び容量線（３００）を備え、更にＴＦＴに接続されたデータ線（６ａ）及び走査線（３ａ）を備える。周辺領域に、データ線の駆動に係る回路を含む周辺回路と、これに接続されており容量線と同一膜からなる信号線（４００）と、これを少なくとも一方向から電気遮蔽するデータ線と同一膜からなるシールド（４０１ａ）を備える。



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【特許請求の範囲】

【請求項１】　基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導電膜からなる容量線と、該第１導電膜上に層間絶縁膜を介して積層された第２導電膜からなるデータ線とを備え、前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路と、該周辺回路に接続されており前記第１導電膜及び前記第２導電膜の一方からなる信号線と、該信号線を少なくとも一方向から電気遮蔽する前記第１導電膜及び前記第２導電膜の他方からなるシールドとを備えたことを特徴とする電気光学装置。

【請求項２】　前記シールドは、前記第２導電膜からなり、前記第１導電膜からなる前記信号線を上方から電気遮蔽することを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記シールドは、前記信号線を上方から電気遮蔽する本線部と該本線部から延設されて少なくとも前記層間絶縁膜に掘られた溝内に埋め込まれる側壁部分を更に有し、前記本線部及び前記側壁部分により前記信号線の断面上で見て前記信号線を三方から電気遮蔽することを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記シールドは、前記信号線の下方に他の層間絶縁膜を介して積層された他の導電膜からなる底壁部分を更に有し、前記本線部、前記側壁部分及び前記底壁部分により前記信号線を前記信号線の断面上で見て四方から電気遮蔽することを特徴とする請求項３に記載の電気光学装置。

【請求項５】　前記シールドは、前記第１導電膜からなり、前記第２導電膜からなる前記信号線を下方から電気遮蔽することを特徴とする請求項１に記載の電気光学装置。

【請求項６】　前記信号線は、画像信号を供給する画像信号線を含むことを特徴とする請求項１から５のいずれか一項に記載の電気光学装置。

【請求項７】　前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、

前記信号線は、前記画像信号を供給する画像信号線と前記サンプリング回路とを中継接続する中継配線を含むことを特徴とする請求項１から６のいずれか一項に記載の電気光学装置。

【請求項８】　前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、

前記信号線は、前記サンプリング回路のゲート信号線を含むことを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記信号線は、クロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線を含むことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。

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【請求項１０】　前記信号線は、画像信号を供給する画像信号線とクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線とを含み、

前記シールドは、前記画像信号線を電気遮蔽する第１部分と、前記制御信号線を電気遮蔽する第２部分とを含み、

前記第１部分は第１定電位に固定され且つ前記第２部分は前記第１定電位とは異なる第２定電位に固定されることを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記シールドは、１本の信号線毎に分断されていることを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項１２】　前記シールドは、複数の信号線毎に分断されていることを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項１３】　前記第１導電膜及び前記第２導電膜のうち少なくとも一方は、金属を含有する膜から形成されたことを特徴とする請求項１から１２のいずれか一項に記載の電気光学装置。

【請求項１４】　前記画像表示領域に、前記基板上において前記第１導電膜よりも下方に積層された第３導電膜からなる走査線を更に備え、

前記周辺領域に、前記信号線を下方から電気遮蔽する前記第３導電膜からなる他のシールドを更に備えたことを特徴とする請求項１から１３のいずれか一項に記載の電気光学装置。

【請求項１５】　前記画像表示領域に、前記データ線と前記画素電極との間に接続された薄膜トランジスタと、該薄膜トランジスタの少なくともチャネル領域を遮光する前記基板上において前記第１導電膜及び前記薄膜トランジスタよりも下方に積層された導電性の遮光膜とを更に備え、

前記周辺領域に、前記信号線を下方から電気遮蔽する前記遮光膜からなる他のシールドを更に備えたことを特徴とする請求項１から１４に記載の電気光学装置。

【請求項１６】　前記基板に電気光学物質を介して対向する対向基板上に、前記複数の画素電極に対向する対向電極を更に備えており、

前記シールドは、前記信号線のうち前記対向電極に対向する一部と前記対向電極との間において前記信号線の一部を上方から電気遮蔽する部分を含むことを特徴とする請求項１から１５のいずれか一項に記載の電気光学装置。

【請求項１７】　前記シールドは、電源配線の本線又は分岐配線からなることを特徴とする請求項１から１６のいずれか一項に記載の電気光学装置。

【請求項１８】　基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導

電膜からなる容量線と、該第１導電膜上に層間絶縁膜を介して積層された第２導電膜からなるデータ線とを備え、

前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路と、該周辺回路に画像信号を供給すると共に前記第１導電膜及び前記第２導電膜の一方からなる画像信号線と、該周辺回路にクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給すると共に前記第１導電膜及び前記第２導電膜の他方からなる制御信号線とを備えたことを特徴とする電気光学装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、液晶装置等の電気光学装置の技術分野に属し、特に、ＴＦＴアレイ基板上の周辺領域に設けられたデータ線駆動回路、サンプリング回路等の周辺回路により画像信号、クロック信号等に応じてデータ線を駆動する形式の電気光学装置の技術分野に属する。

【０００２】

【背景技術】ＴＦＴ駆動によるアクティブマトリクス駆動方式の電気光学装置においては、縦横に夫々配列された多数の走査線及びデータ線並びにこれらの各交点に対応して多数の画素電極がＴＦＴアレイ基板上に設けられている。そして、これらに加えて、データ線駆動回路、サンプリング回路、走査線駆動回路等の周辺回路、更にこのような周辺回路に接続された画像信号線や制御信号線（例えば、クロック信号線や波形選択信号線）などの信号線が、係るＴＦＴアレイ基板上の周辺領域に設けられる場合がある。

【０００３】この場合、データ線駆動回路には、画像信号の供給タイミングの基準となる基準クロック（以下、Ｘ側基準クロックと称す）や所謂ゴーストの発生を防ぐための波形選択信号などの制御信号、表示すべき画像の内容に対応する画像信号、正や負の定電位電源等が、ＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して夫々供給される。他方、走査線駆動回路には、走査信号の供給タイミングの基準となる基準クロック（以下、Ｙ側基準クロックと称す）、正や負の定電位電源等が、やはりＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して供給される。そして例えば、走査線駆動回路により、Ｙ側基準クロックに基づくタイミングで走査信号を走査線に線順次で供給する。これに対応してデータ線駆動回路が、入力された画像信号をサンプリングするサンプリング回路を、Ｘ側基準クロックに基づくタイミングで順次駆動して、サンプリング回路から画像信号がデータ線に供給される。これらの結果、走査線にゲート接続された各ＴＦＴは、走査信号の供給に応じて導通状態とされ、画像信号がデータ線及び当該ＴＦＴを介して画素電極に供給されて各画素における画像表示が

行われる。

【０００４】近年特に、表示画像の高解像度化に伴って、非常に高い周波数のシリアルな画像信号が入力されるようになってきている。例えば、画像信号のドット周波数は、近時の高解像度のパソコン画面において使用されるＸＧＡ表示モードでは約６５ＭＨｚであり、ＳＸＧＡ表示モードでは約１３５ＭＨｚであり、従来のＶＧＡ表示モードにおけるドット周波数（約３０ＭＨｚ）を遥かに上回る。これに対応すべく、特にデータ線駆動回路に供給されるＸ側基準クロックの周波数も非常に高くなる。更に、このように高い画像信号の周波数を、サンプリング回路でサンプリング可能な程度の周波数に落とすために、電気光学装置に入力される前段階で、高周波数のシリアルな画像信号を複数のパラレルな画像信号にシリアルーパラレル変換する処理が行われている。例えば、前述のＶＧＡ表示モードでは、６個程度のパラレルな画像信号への変換が行われており、ＸＧＡ表示モードやＳＸＧＡ表示モードでは、サンプリング回路の性能に応じて、例えば１２個或いは２４個程度のパラレルな画像信号への変換が必要となる。

【０００５】

【発明が解決しようとする課題】しかしながら、近年の表示画像の高品位化の要請の下では、このように基準クロックの周波数を高くすることによる、高周波のクロックノイズの発生が無視し得ないようになる。即ち、例えば従来の比較的周波数の低いＸ側基準クロックをデータ線駆動回路に供給してサンプリング回路を駆動する構成において、そのままクロック信号の周波数を上げたのでは、サンプリング回路に入力される画像信号中やサンプリング回路から出力される画像信号中に高周波のクロックノイズが発生して、データ線に供給すべき画像信号が変化してしまう。このように変化した画像信号の供給を受けたのでは、各画素電極により表示される画像もやはり変化してしまうという問題点がある。例えば、各画素において中間レベルの階調表示を行う時に、数ｍＶ～数十ｍＶ程度の微少なノイズが画像信号中に飛び込んだだけでも、表示画像中に視認可能な程度のノイズとして現れてしまう。これは、最高又は最低の液晶駆動電圧（例えば、０～５Ｖ間の電圧）に対応する白又は黒レベルの表示を行っている場合と比べて、中間レベルにおける液晶駆動電圧の変化に対する液晶の透過率の変化が急峻だからである。このように高精度の多階調表示を実現するためには、高周波のクロックノイズの問題は重大である。

【０００６】他方で、前述のようにシリアルーパラレル変換によるパラレルな画像信号の個数を増やすことによりサンプリング回路に供給される画像信号の周波数を下げることはできるが、電気光学装置の基板に設けねばならない画像信号入力用の外部入力端子の数や画像信号線の数は、このパラレルな画像信号の個数の増加に対応し

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て増やさねばならない。従って、限られた基板上の周辺領域に多数の信号線を極めて近接配置せねばならず、結果として、近接配置された一の信号線（例えば、クロック信号線）をノイズ源として他の信号線（例えば、画像信号線）上の信号中に飛び込むノイズが増大してしまうという問題点が生ずる。しかも、シリアルーパラレル変換によるパラレルな画像信号の個数を増やす程、画素電極への書き込み能力不足に起因して発生するブロックゴースト（即ち、パラレルな画像信号が供給される複数のデータ線に対応する画素電極群を一纏めとして発生するブロック状のゴースト）が画像表示領域内に占める面積が増加する。この結果、ブロックゴーストが視覚上目立つようになるという深刻な問題も生じる。

【０００７】本発明は上述の問題点に鑑みなされたものであり、基板上の周辺領域に設けられた信号線上の信号におけるノイズが低減されており、高品位の画像表示が可能な電気光学装置を提供することを課題とする。

【０００８】

【課題を解決するための手段】本発明の電気光学装置は上記課題を解決するために、基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導電膜からなる容量線と、該第１導電膜上に層間絶線膜を介して積層された第２導電膜からなるデータ線とを備え、前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路と、該周辺回路に接続されており前記第１導電膜及び前記第２導電膜の一方からなる信号線と、該信号線を少なくとも一方向から電気遮蔽する前記第１導電膜及び前記第２導電膜の他方からなるシールドとを備える。

【０００９】本発明の電気光学装置によれば、画像表示領域では、容量線をなす第１導電膜上に、データ線をなす第２導電膜が層間絶線膜を介して積層されている。周辺領域では、これら第１導電膜及び第２導電膜の一方から、周辺回路に接続された信号線が形成されており、これら第１導電膜及び第２導電膜の他方から、信号線を少なくとも一方向（例えば、上方や下方）から電気遮蔽するシールドが形成されている。従って、容量線をなす第１導電膜を利用して周辺領域における信号線を形成しつつ、データ線をなす第２導電膜を利用して係る信号線を電気遮蔽することにより、信号線上の信号への電磁ノイズの飛び込みを効果的に低減でき、又は信号線からの電磁ノイズの発生を効果的に低減できる。或いは、信号線をなす第２導電膜を利用して周辺領域における信号線を形成しつつ、容量線をなす第１導電膜を利用して係る信号線を電気遮蔽することにより、信号線上の信号への電磁ノイズの飛び込みを効果的に低減でき、又は信号線からの電磁ノイズの発生を効果的に低減できる。しかも、いずれの場合にも、周辺領域に信号線やシールドを形成するために専用の膜を別途形成しないで済むので、装置

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構成及び製造工程を簡略化する上でも有利である。特に、画像品位の向上のために画素ピッチを微細化し駆動周波数を高めた場合に、一般にこのような信号線に係るノイズは相対的に増加する。従って、本発明のように周辺領域に配線された画像信号線、制御信号線等の信号線を電気遮蔽する構成は、画素ピッチを微細化し或いは駆動周波数を高める上で大変有利である。

【００１０】尚、本発明における周辺回路のうち「データ線の駆動に係る回路」とは、例えばデータ線を駆動するデータ線駆動回路の他、データ線駆動回路からのサンプリング回路駆動信号による制御を受けて複数のデータ線に画像信号を所定のタイミングで印加するサンプリング回路、複数のデータ線に所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路等を含む、データ線の駆動或いはデータ線への画像信号の供給に関連する回路を全て含む広い意味である。また、「周辺回路」とは、このようなデータ線の駆動に係る回路以外に、例えば走査線の駆動に係る回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等の周辺領域に作りこまれる任意の回路をいう。

【００１１】以上の結果、比較的簡単な装置構成により、画像信号等におけるノイズが低減されており、高品位の画像表示が可能な電気光学装置を実現できる。

【００１２】本発明の電気光学装置の一態様では、前記シールドは、前記第２導電膜からなり、前記第１導電膜からなる前記信号線を上方から電気遮蔽する。

【００１３】この態様によれば、第１導電膜からなる画像信号線等の信号線は、第２導電膜からなるシールドにより上方から電気遮蔽される。従って、各信号線の主に上方や側方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを効果的に低減できる。

【００１４】この態様では、前記シールドは、前記信号線を上方から電気遮蔽する本線部と該本線部から延設されて少なくとも前記層間絶縁膜に掘られた溝内に埋め込まれる側壁部分を更に有し、前記本線部及び前記側壁部分により前記信号線の断面上で見て前記信号線を三方から電気遮蔽するように構成してもよい。

【００１５】このように構成すれば、第１導電膜からなる画像信号線等の信号線は、第２導電膜からなるシールドにより上方及び側方の三方から電気遮蔽される。従って、各信号線の主に上方や側方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを一層効果的に低減できる。

【００１６】この場合更に、前記シールドは、前記信号線の下方に他の層間絶線膜を介して積層された他の導電膜からなる底壁部分を更に有し、前記本線部、前記側壁部分及び前記底壁部分により前記信号線を前記信号線の断面上で見て四方から電気遮蔽するように構成してもよ

い。

【００１７】このように構成すれば、第１導電膜からなる画像信号線等の信号線は、第２導電膜及び他の導電膜からなるシールドにより上方、側方及び下方の四方から電気遮蔽される。従って、各信号線の四方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを非常に効果的に低減できる。

【００１８】本発明の電気光学装置の他の態様では、前記シールドは、前記第１導電膜からなり、前記第２導電膜からなる前記信号線を下方から電気遮蔽する。

【００１９】この態様によれば、第２導電膜からなる画像信号線等の信号線は、第１導電膜からなるシールドにより下方から電気遮蔽される。従って、各信号線の主に下方や側方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを効果的に低減できる。

【００２０】本発明の電気光学装置の他の態様では、前記信号線は、画像信号を供給する画像信号線を含む。

【００２１】この態様によれば、周辺領域において、画像信号線は電気遮蔽されているので、ノイズ源としての他の信号線や配線或いは回路や素子からの画像信号線上の画像信号への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的に高いＳ／Ｎを持つ画像信号に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００２２】本発明の電気光学装置の他の態様では、前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、前記信号線は、前記画像信号を供給する画像信号線と前記サンプリング回路とを中継接続する中継配線を含む。

【００２３】この態様によれば、周辺領域において、中継配線はシールドされているので、ノイズ源としての他の信号線や配線或いは回路や素子からの中継配線上の画像信号への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的に高いＳ／Ｎを持つ画像信号に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。特に、対向基板に設けられる対向電極に対向する中継配線部分については、当該中継配線部分と対向電極との寄生容量を低減する観点から、両者間に配置される上方シールドにより電気遮蔽すると効果的である。

【００２４】本発明の電気光学装置の他の態様では、前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、前記信号線は、前記サンプリング回路のゲート信号線を含む。

【００２５】この態様によれば、周辺領域において、サンプリング回路のゲート信号線はシールドされているので、ノイズ源としての他の信号線や配線或いは回路や素子からのゲート信号線上の制御信号（例えば、データ線駆動回路から出力されるサンプリング回路駆動信号）への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的にサンプリング回路における高精度のサンプリング動作により、画像表示領域において高品位の画像表示を行うことが可能となる。特に、対向基板に設けられる対向電極に対向するゲート信号線部分については、当該ゲート信号線部分と対向電極との寄生容量を低減する観点から、両者間に配置される上方シールドにより電気遮蔽すると効果的である。

【００２６】本発明の電気光学装置の他の態様では、前記信号線は、クロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線を含む。

【００２７】この態様によれば、周辺領域において、制御信号線は電気遮蔽されているので、ノイズ源としての他の信号線や配線或いは回路や素子からの制御信号線上の制御信号への電磁ノイズの飛び込みを効果的に低減できる。更に、一般に高周波数や高電位である制御信号は画像信号に対するノイズ源となり易い。従って、このように制御信号線を電気遮蔽することにより、ノイズ源としての当該制御信号線からの、他の信号線たる画像信号線等に供給される画像信号等への電磁ノイズの飛び込みを効果的に低減できる。よって、最終的に高いＳ／Ｎを持つ制御信号や画像信号等に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００２８】尚、以上説明した本発明の電気光学装置（各実施形態を含む）では、シールドは、好ましくは接地電位や他の定電位に固定される。

【００２９】本発明の電気光学装置の他の態様では、前記信号線は、画像信号を供給する画像信号線とクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線とを含み、前記シールドは、前記画像信号線を電気遮蔽する第１部分と、前記制御信号線を電気遮蔽する第２部分とを含み、前記第１部分は第１定電位に固定され且つ前記第２部分は前記第１定電位とは異なる第２定電位に固定される。

【００３０】この態様によれば、周辺領域において、画像信号線はシールドの第１部分により電気遮蔽されており、制御信号線はシールドの第２部分により電気遮蔽されているので、ノイズ源としての他の信号線や配線或いは回路や素子からの、画像信号線上の画像信号及び制御信号線上の制御信号への電磁ノイズの飛び込みを夫々効果的に低減できる。そして特に、シールドの第１部分と第２部分とは、相異なる定電位に固定されているので、同一の定電位配線を介して両信号線間でそれらの電位変動が相互に影響を及ぼす事態を未然防止できる。従って、最終的に高いＳ／Ｎを持つ画像信号や制御信号等に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００３１】本発明の電気光学装置の他の態様では、前記シールドは、１本の信号線毎に分断されている。

【００３２】この態様によれば、信号線は、１本毎に別個に電気遮蔽されているので、各信号線を他の全ての信号線から電気遮蔽できる。即ち、複数の信号線相互間の電磁波による悪影響を極力低減できる。

【００３３】本発明の電気光学装置の他の態様では、前記シールドは、複数の信号線毎に分断されている。

【００３４】この態様によれば、信号線は、複数の信号線毎に別個に電気遮蔽されているので、１本の信号線毎にシールドを設ける場合と比較して、容易にシールドを形成できる。この際、例えば複数の画素信号線など、相互に電磁波が及ぼす影響が基本的に小さい複数の信号線を同一シールドにより纏めて電気遮蔽するようにし、他方で、例えば画像信号線とクロック信号線など、相互に電磁波が及ぼす影響が基本的に大きい信号線を相互に別個のシールドにより電気遮蔽するようにすれば、このように複数の信号線を纏めて電気遮蔽する際の不利益（即ち、同一シールドで電気遮蔽される複数の信号線相互間におけるノイズの飛び込み）を抑えることができる。

【００３５】本発明の電気光学装置の他の態様では、前記第１導電膜及び前記第２導電膜のうち少なくとも一方は、金属を含有する膜から形成される。

【００３６】この態様によれば、例えば、Ａｌ（アルミニウム）膜、Ｃｒ（クロム）等の金属を含有する膜から第１導電膜や第２導電膜を形成することにより、これらの導電膜の低抵抗化を容易に図ることができる。

【００３７】本発明の電気光学装置の他の態様では、前記画像表示領域に、前記基板上において前記第１導電膜よりも下方に積層された第３導電膜からなる走査線を更に備え、前記周辺領域に、前記信号線を下方から電気遮蔽する前記第３導電膜からなる他のシールドを更に備える。

【００３８】この態様によれば、画像表示領域では、走査線をなす第３導電膜が、容量線をなす第１導電膜よりも下方に積層されている。周辺領域では、この第３導電膜から、信号線を下方から電気遮蔽する他のシールドが形成されている。従って、第１導電膜及び第２導電膜の一方からなる画像信号線等の信号線は、第１導電膜及び第２導電膜の他方からなるシールドと、第３導電膜からなるシールドとにより上下から或いは下方から冗長的に電気遮蔽される。従って、ノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを一層効果的に低減できる。尚、画像表示領域では、走査線及びデータ線によるアクティブマトリクス駆動或いはパッシブマトリクス駆動が可能となる。

【００３９】本発明の電気光学装置の他の態様では、前記画像表示領域に、前記データ線と前記画素電極との間に接続された薄膜トランジスタと、該薄膜トランジスタの少なくともチャネル領域を遮光する前記基板上において前記第１導電膜及び前記薄膜トランジスタよりも下方に積層された導電性の遮光膜とを更に備え、前記周辺領域に、前記信号線を下方から電気遮蔽する前記遮光膜からなる他のシールドを更に備える。

【００４０】この態様によれば、画像表示領域では、薄膜トランジスタの少なくともチャネル領域を遮光する遮光膜が、容量線をなす第１導電膜よりも下方に積層されている。周辺領域では、この遮光膜から、信号線を下方から電気遮蔽する他のシールドが形成されている。従って、第１導電膜及び第２導電膜の一方からなる画像信号線等の信号線は、第１導電膜及び第２導電膜の他方からなるシールドと、遮光膜からなるシールドとにより上下から或いは下方から冗長的に電気遮蔽される。従って、ノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを一層効果的に低減できる。尚、画像表示領域では、データ線及び薄膜トランジスタによるアクティブマトリクス駆動が可能となる。

【００４１】本発明の電気光学装置の他の態様では、前記基板に電気光学物質を介して対向する対向基板上に、前記複数の画素電極に対向する対向電極を更に備えており、前記シールドは、前記信号線のうち前記対向電極に対向する一部と前記対向電極との間において前記信号線の一部を上方から電気遮蔽する部分を含む。

【００４２】この態様によれば、対向基板に設けられる対向電極とこれに対向する信号線の一部との間に上方シールドが存在するので、当該信号線の一部と対向電極との間における寄生容量を低減できる。即ち、ノイズ源としての対向電極からの信号線上の画像信号等への電磁ノイズの飛び込みや、ノイズ源としての信号線からの対向電極上の定電位信号（例えば、反転しない定電位の信号、フレームやフィールド毎に反転する定電位の信号など）等への電磁ノイズの飛び込みを効果的に低減できる。

【００４３】本発明の電気光学装置の他の態様では、前記シールドは、電源配線の本線又は分岐配線からなる。

【００４４】この態様によれば、シールドは、電源配線の本線又は分岐配線からなるので、シールドを定電位に固定できる。しかも、周辺領域におけるシールドが占める領域を電源配線に割り当てることになるので、電源配線を比較的容易に幅広に構成することができ、安定した定電位を供給することも可能となる。またシールドと電源配線とを共用することで、装置構成及び製造工程の簡略化を図ることも可能となる。更に、シールドをこのように安定した定電位に固定することにより、電気遮蔽の性能も向上するので一層有利である。

【００４５】本発明の他の電気光学装置は上記課題を解決するために、基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導電膜からなる容量線と、該第１導電膜上に層間絶縁膜を介して積層された第２導電膜からなるデータ線とを備え、前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路

と、該周辺回路に画像信号を供給すると共に前記第１導電膜及び前記第２導電膜の一方からなる画像信号線と、該周辺回路にクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給すると共に前記第１導電膜及び前記第２導電膜の他方からなる制御信号線とを備える。

【００４６】本発明の他の電気光学装置によれば、画像表示領域では、容量線をなす第１導電膜上に、データ線をなす第２導電膜が層間絶線膜を介して積層されている。周辺領域では、これら第１導電膜及び第２導電膜の一方から、画像信号線が形成されており、これら第１導電膜及び第２導電膜の他方から、制御信号線が形成されている。従って、周辺領域において、同一導電膜をパターニングすることにより同一平面内に画像信号線と制御信号線とを形成する場合と比べると、画像信号線と制御信号線とを形成する二つの導電膜が基板に垂直な方向に離間した分だけ両者間における寄生容量は低減されたことになる。即ち、二つの信号線間の距離が大きくなるに連れて小さくなるノイズ源としての制御信号線からの画像信号線上の画像信号への電磁ノイズの飛び込み（或いはノイズ源としての画像信号線からの制御信号線上の制御信号への電磁ノイズの飛び込み）を低減できる。尚、このような構成を持つ電気光学装置に対して、上述した本発明に係る各種のシールドを設けてもよい。このように構成すれば、画送信号線と制御信号線とが基板に垂直な方向に離間したことによる電磁ノイズを低減する効果と、画像信号と制御信号線との間のシールドによる電磁ノイズを低減する効果との両者を享受できる。

【００４７】以上の結果、比較的簡単な装置構成により、画像信号等におけるノイズが低減されており、高品位の画像表示が可能な電気光学装置を実現できる。

【００４８】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにされる。

【００４９】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。以下の実施形態は、本発明の電気光学装置を液晶装置に適用したものである。

【００５０】先ず本発明の実施形態における電気光学装置の構成について、図１から図３を参照して説明する。図１は、電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。図２は、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。図３は、図２のＡ－Ａ’断面図である。尚、図３においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００５１】図１において、本実施形態における電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素には夫々、画素電極９ａと当該画素電極９ａをスイッチング制御するためのＴＦＴ３０とが形成されており、画像信号が供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されている。データ線６ａに書き込む画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給しても構わないし、相隣接する複数のデータ線６ａ同士に対して、グループ毎に供給するようにしても良い。また、ＴＦＴ３０のゲートに走査線３ａが電気的に接続されており、所定のタイミングで、走査線３ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。画素電極９ａを介して電気光学物質の一例としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板（後述する）に形成された対向電極（後述する）との間で一定期間保持される。液晶は、印加される電位レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能にする。ノーマリーホワイトモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が減少し、ノーマリーブラックモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が増加され、全体として電気光学装置からは画像信号に応じたコントラストを持つ光が出射する。ここで、保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極との間に形成される液晶容量と並列に蓄積容量７０を付加する。走査線３ａに並んで、蓄積容量７０の固定電位側容量電極を含むと共に定電位に固定された容量線３００が設けられている。

【００５２】図２において、電気光学装置のＴＦＴアレイ基板上には、マトリクス状に複数の透明な画素電極９ａ（点線部９ａ’により輪郭が示されている）が設けられており、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ及び走査線３ａが設けられている。

【００５３】また、半導体層１ａのうち図中右上がりの斜線領域で示したチャネル領域１ａ’に対向するように走査線３ａが配置されており、走査線３ａはゲート電極として機能する（特に、本実施形態では、走査線３ａは、当該ゲート電極となる部分において幅広に形成されている）。このように、走査線３ａとデータ線６ａとの交差する個所には夫々、チャネル領域１ａ’に走査線３ａがゲート電極として対向配置された画素スイッチング用のＴＦＴ３０が設けられている。

【００５４】図２及び図３に示すように、蓄積容量７０は、ＴＦＴ３０の高濃度ドレイン領域１ｅ（及び画素電極９ａ）に接続された画素電位側容量電極としての中継層７１と、固定電位側容量電極としての容量線３００の一部とが、誘電体膜７５を介して対向配置されることに

より形成されている。

【００５５】中継層７１は、蓄積容量７０の画素電位側容量電極としての機能の他、コンタクトホール８３及び８５を介して、画素電極９ａとＴＦＴ３０の高濃度ドレイン領域１ｅとを中継接続する中間導電層としての機能を持つ。

【００５６】容量線３００は平面的に見て、走査線３ａに沿ってストライプ状に伸びており、ＴＦＴ３０に重なる個所が図２中上下に突出している。このような容量線３００は好ましくは、膜厚５０ｎｍ程度の導電性のポリシリコン膜等からなる第１膜と、膜厚１５０ｎｍ程度の高融点金属を含む金属シリサイド膜等からなる第２膜とが積層された多層構造を持つように構成される。このように構成すれば、第２膜は、容量線３００或いは蓄積容量７０の固定電位側容量電極としての機能の他、ＴＦＴ３０の上側において入射光からＴＦＴ３０を遮光する遮光層としての機能を持つ。

【００５７】他方、ＴＦＴアレイ基板１０上におけるＴＦＴ３０の下側には、下側遮光膜１１ａが格子状に設けられている。下側遮光膜１１ａは、例えば、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）、Ｐｂ（鉛）等の高融点金属のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等からなる。

【００５８】そして、図２中縦方向に夫々伸びるデータ線６ａと図２中横方向に夫々伸びる容量線３００とが相交差して形成されること及び格子状に形成された下側遮光膜１１ａにより、ＴＦＴアレイ基板１０上におけるＴＦＴ３０の上側及び下側には夫々、平面的に見て格子状に遮光領域が構成されており、各画素の開口領域を規定している。

【００５９】また図３において、容量電極としての中継層７１と容量線３００との間に配置される誘電体膜７５は、例えば膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ膜、ＬＴＯ膜等の酸化シリコン膜、あるいは窒化シリコン膜等から構成される。蓄積容量７０を増大させる観点からは、膜の信頼性が十分に得られる限りにおいて、誘電体膜７５は薄い程良い。

【００６０】図２及び図３に示すように、データ線６ａは、コンタクトホール８１を介して、例えばポリシリコン膜からなる半導体層１ａのうち高濃度ソース領域１ｄに電気的に接続されている。尚、上述した中継層７１と同一膜からなる中継層を形成して、当該中継層及び２つのコンタクトホールを介してデータ線６ａと高濃度ソース領域１ｄとを電気的に接続してもよい。

【００６１】また容量線３００は、画素電極９ａが配置された画像表示領域からその周囲に延設され、定電位源と電気的に接続されて、固定電位とされる。このような定電位源としては、ＴＦＴ３０を駆動するための走査信号を走査線３ａに供給するための走査線駆動回路（後述する）や画像信号をデータ線６ａに供給するサンプリング回路を制御するデータ線駆動回路（後述する）に供給される正電源や負電源の定電位源でもよいし、対向基板２０の対向電極２１に供給される定電位でも構わない。更に、ＴＦＴ３０の下側に設けられる下側遮光膜１１ａについても、その電位変動がＴＦＴ３０に対して悪影響を及ぼすことを避けるために、容量線３００と同様に、画像表示領域からその周囲に延設して定電位源に接続するとよい。

【００６２】画素電極９ａは、中継層７１を中継することにより、コンタクトホール８３及び８５を介して半導体層１ａのうち高濃度ドレイン領域１ｅに電気的に接続されている。即ち、本実施形態では、中継層７１は、蓄積容量７０の画素電位側容量電極としての機能に加えて、画素電極９ａをＴＦＴ３０へ中継接続する機能を果たす。このように中継層７１は、層間距離が例えば１０００ｎｍ程度に長くても、両者間を一つのコンタクトホールで接続する技術的困難性を回避しつつ比較的小径の二つ以上の直列なコンタクトホールで両者間を良好に接続でき、画素開口率を高めることが可能となり、コンタクトホール開孔時におけるエッチングの突き抜け防止にも役立つ。

【００６３】図２及び図３において、電気光学装置は、ＴＦＴアレイ基板１０と、これに対向配置される透明な対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば石英基板、ガラス基板、シリコン基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。

【００６４】図３に示すように、ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９ａは例えば、ＩＴＯ（Indium Tin Oxide）膜などの透明導電性薄膜からなる。また配向膜１６は例えば、ポリイミド薄膜などの有機薄膜からなる。

【００６５】他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜２２は、ポリイミド薄膜などの有機薄膜からなる。

【００６６】対向基板２０には、格子状又はストライプ状の遮光膜を設けるようにしてもよい。このような構成を採ることで、前述の如く遮光領域を構成する容量線３００及びデータ線６ａと共に当該対向基板２０上の遮光膜により、対向基板２０側からの入射光がチャネル領域１ａ’や低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに侵入するのを、より確実に阻止できる。更に、このような対向基板２０上の遮光膜は、少なくとも入射光

が照射される面を高反射な膜で形成することにより、電気光学装置の温度上昇を防ぐ働きをする。

【００６７】このように構成された、画素電極９ａと対向電極２１とが対面するように配置されたＴＦＴアレイ基板１０と対向基板２０との間には、後述のシール材により囲まれた空間に電気光学物質の一例である液晶が封入され、液晶層５０が形成される。液晶層５０は、画素電極９ａと対向電極２１との間に電圧が生じていない状態で配向膜１６及び２２により所定の配向状態をとる。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、ＴＦＴアレイ基板１０及び対向基板２０をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのグラスファイバー或いはガラスビーズ等のギャップ材が混入されている。

【００６８】更に、画素スイッチング用のＴＦＴ３０下には、下地絶縁膜１２が設けられている。下地絶縁膜１２は、下側遮光膜１１ａからＴＦＴ３０を層間絶縁する機能の他、ＴＦＴアレイ基板１０の全面に形成されることにより、ＴＦＴアレイ基板１０の表面の研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用のＴＦＴ３０の特性の変化を防止する機能を有する。

【００６９】図３において、画素スイッチング用のＴＦＴ３０は、ＬＤＤ（Lightly DopedDrain）構造を有しており、走査線３ａ、当該走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ’、走査線３ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁薄膜２、半導体層１ａの低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ、半導体層１ａの高濃度ソース領域１ｄ並びに高濃度ドレイン領域１ｅを備えている。

【００７０】走査線３ａ上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８３が各々開孔された第１層間絶縁膜４１が形成されている。

【００７１】第１層間絶縁膜４１上には中継層７１及び容量線３００が形成されており、これらの上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び中継層７１へ通じるコンタクトホール８５が各々開孔された第２層間絶縁膜４２が形成されている。

【００７２】尚、本実施形態では、第１層間絶縁膜４１に対しては、１０００℃の焼成を行うことにより、半導体層１ａや走査線３ａを構成するポリシリコン膜に注入したイオンの活性化を図ってもよい。他方、第２層間絶縁膜４２に対しては、このような焼成を行わないことにより、容量線３００の界面付近に生じるストレスの緩和を図るようにしてもよい。

【００７３】第２層間絶縁膜４２上にはデータ線６ａが形成されており、これらの上には、中継層７１へ通じるコンタクトホール８５が形成された平坦化した第３層間絶縁膜４３が形成されている。画素電極９ａは、このように構成された第３層間絶縁膜４３の上面に設けられている。

【００７４】本実施形態では、第３層間絶縁膜４３の表面は、ＣＭＰ（Chemical Mechanical Polishing：化学的機械研磨）処理等により平坦化されており、その下方に存在する各種配線や素子による段差に起因する液晶層５０における液晶の配向不良を低減する。

【００７５】以上のように構成された本実施形態によれば、対向基板２０側からＴＦＴ３０のチャネル領域１ａ’及びその付近に入射光が入射しようとすると、データ線６ａ及び容量線３００からなる格子状の遮光層で遮光を行う。他方、ＴＦＴアレイ基板１０側から、ＴＦＴ３０のチャネル領域１ａ’及びその付近に戻り光が入射しようとすると、下側遮光膜１１ａで遮光を行う（特に、複板式のカラー表示用のプロジェクタ等で複数の電気光学装置をプリズム等を介して組み合わせて一つの光学系を構成する場合には、他の電気光学装置からプリズム等を突き抜けて来る投射光部分からなる戻り光は強力であるので、有効である。）。これらの結果、ＴＦＴ３０の特性が光リークにより変化することは殆ど無くなり、当該電気光学装置では、非常に高い耐光性が得られる。また、データ線６ａ及び走査線３ａが形成された各画素の非開口領域を利用して大きな蓄積容量７０を構築できる。

【００７６】次に、図４を参照して、本実施形態における周辺領域における配線及びシールドについて説明する。ここに、図４は、本実施形態におけるＴＦＴアレイ基板上に設けられたシールドを含む各種配線、周辺回路等の構成を示す図式的な平面図である。

【００７７】図５から図１０は夫々、シールド線、画像信号線及びクロック信号線等の配線の各種具体例を示す図４のＢ－Ｂ’断面図である。

【００７８】図４において、液晶装置のＴＦＴアレイ基板上における画像表示領域の周辺に位置する周辺領域には、周辺回路の一例として、データ線駆動回路１０１、走査線駆動回路１０４及びサンプリング回路３０１が形成されている。

【００７９】以下図４の説明において、ＴＦＴアレイ基板１の下辺に沿って複数設けられた外部入力端子１０２を介して入力される信号の配線４００は、説明の容易化のために信号名称と同一のアルファベット記号を配線４００の後に夫々括弧で付加して参照する（例えば、“クロック信号ＣＬＸ”の信号配線を“配線４００（ＣＬＸ）”と呼ぶ）ことにする。走査線駆動回路１０４は、外部制御回路から外部入力端子１０２並びに配線４００（ＶＳＳＹ）及び配線４００（ＶＤＤＹ）を介して供給される、走査線駆動回路１０４用の負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用いて、スタート信号ＳＰ

Yの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線４００（ＣＬＹ）及び配線４００（ＣＬＹ'）を介して供給される、走査線駆動回路１０４の内蔵シフトレジスタ回路用の基準クロック信号ＣＬＹ及びその反転クロック信号ＣＬＹ'に基づく所定タイミングで、走査線３ａに走査信号をパルス的に線順次で印加する。

【００８０】データ線駆動回路１０１は、外部制御回路から外部入力端子１０２並びに信号配線４００（ＶＳＳＸ）及び配線４００（ＶＤＤＸ）を介して供給される、データ線駆動回路１０１用の負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用いて、スタート信号ＳＰＸの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線４００（ＣＬＸ）及び配線４００（ＣＬＸ'）を介して供給される、データ線駆動回路１０１の内蔵シフトレジスタ回路用の基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＸ'に基づき、走査線駆動回路１０４が走査信号を印加するタイミングに合わせて、外部入力端子１０２及び配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）を介して供給される例えば１２個のパラレル信号にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ１２夫々について、データ線６ａ毎にサンプリング回路駆動信号Ｑｍ（ｍ＝１、２、…）をサンプリング回路３０１にサンプリング回路駆動信号線３０６を介して所定タイミングで供給する。

【００８１】サンプリング回路３０１は、ＴＦＴ３０２を各データ線６ａ毎に備えており、配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）が中継配線３０５を経由して、ＴＦＴ３０２のソース電極に接続されており、サンプリング回路駆動信号線３０６がＴＦＴ３０２のゲート電極に接続されている。そして、画像信号ＶＩＤ１～ＶＩＤ１２が入力されると、これらの画像信号をサンプリングする。また、サンプリング回路駆動信号線３０６を介して、データ線駆動回路１０１からサンプリング回路駆動信号Ｑｍが入力されると、画像信号ＶＩＤ１～ＶＩＤ１２夫々についてサンプリングされた画像信号を、１２本の隣接するデータ線６ａからなるグループ毎に順次印加する。

【００８２】以上のように、データ線駆動回路１０１とサンプリング回路３０１とは、１２個のパラレル信号に変換された画像信号ＶＩＤ１～ＶＩＤ１２をデータ線６ａに画像信号Ｓ１、Ｓ２、…として供給するように構成されている。本実施の形態では隣接する１２本のデータ線６ａに接続されるサンプリング回路３０１を同時に選択し、１２本のデータ線６ａからなるグループ毎に順次転送していく方式を述べたが、データ線６ａを６本毎に選択してもよいし、２４本毎に選択してもよい。或いは、２本以上の任意の本数を同時に選択してもよい。この際、少なくともパラレルな画像信号の個数だけ、画像信号用の外部入力端子１０２及び画像信号線が必要なことは言うまでもない。尚、パラレルな画像信号の個数とサンプリング回路３０１を同時に選択する数が相等しくなるように構成してもよいし、前者が後者よりも多くなるように構成してもよい。

【００８３】更に図４に示すように、データ線駆動回路１０１は、スタート信号ＳＰＸが入力されると、基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＫ'に基づく転送信号の順次生成を開始するシフトレジスタ回路１０１ａと、シフトレジスタ回路１０１ａからの転送信号を波形整形した後、サンプリング回路駆動信号線３０６を介してサンプリング回路３０１に供給する波形制御回路１０１ｂ及びバッファ回路１０１ｃとを備えている。また、サンプリング回路３０１は、１２個にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ１２に対応してＴＦＴ３０２が１２個ずつパラレルに各サンプリング回路駆動信号線３０６に接続されている。即ち、ＴＦＴ３０２から構成されるスイッチＳ１～Ｓ１２が左から１本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳ１３～Ｓ２４が左から２本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳｎ-11～Ｓｎが右端のサンプリング回路駆動信号線３０６に接続されている。

【００８４】制御信号の一つである波形選択信号としてのイネーブル信号ＥＮＢ１及びＥＮＢ２は、波形制御回路１０１ｂに入力される。この波形制御回路１０１ｂでは、シフトレジスタ回路１０１ａから順次出力されるパルスの幅を、イネーブル信号ＥＮＢ１及びＥＮＢ２のパルス幅に制限することにより、サンプリング回路３０１の選択期間を（相前後するサンプリング回路駆動信号Ｑ１、Ｑ２、…がハイレベルとなる期間が相互に重ならないように）制御する。これにより、同一の配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）から画像信号を受けるデータ線６ａ間におけるブロックゴーストの発生を防止する。従って、イネーブル信号ＥＮＢ１及びＥＮＢ２は、クロック信号ＣＬＸ及びＣＬＸ'と同じく、水平走査期間よりも短い周期を持つ高周波の制御信号である。

【００８５】尚、本実施形態では、画像表示領域の四隅には、ＴＦＴアレイ基板１と対向基板２０側の対向電極２１（図３参照）との間で電気的な導通をとるための上下導通端子１０６が設けられている（但し、図４では、そのうち２隅が図示されている）。上下導通端子１０６には、外部入力端子１０２並びに配線４００（ＬＣＣＯＭ）を介して供給される。

【００８６】次に、本実施形態の電気光学装置で採用可能なシールドの各種具体例を図５から図１０に夫々示す。ここに、図５から図１０は夫々、シールドの各種具体例の、図４のＢ－Ｂ'断面における構造を夫々示す断面図である。

【００８７】図５から図１０において、各具体例では夫々、画像信号線である配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）は、画像表示領域における容量線３００と同一の導電膜（例えば、導電性のポリシリコン膜と導電性の金属シリサイド膜とを含む多層膜）から構成されており、これらの配線４００は少なくとも、画像表示領域におけるデータ線６ａと同一膜（例えば、Ａｌ膜）からなるシールドにより電気遮蔽されている。

【００８８】即ち、図５の具体例では、容量線３００と同一導電膜からなる配線４００は、その上方から各配線４００に沿って且つ各配線４００を覆う領域に形成されたデータ線６ａと同一導電膜からなる上方シールド４０１ａにより、電気遮蔽されている。特にこの具体例では、上方シールド４０１ａは、１本の配線４００毎に分断されているので、各配線４００を他の全ての配線４００から相互に電気遮蔽できる。

【００８９】図６の具体例では、容量線３００と同一導電膜からなる配線４００は、その上方から複数の配線４００に沿って且つ複数の配線４００を纏めて覆う領域に形成されたデータ線６ａと同一導電膜からなる上方シールド４０１ｂにより、電気遮蔽されている。特にこの具体例では、上方シールド４０１ｂは、複数の信号線毎に分断されている。従って、１本の信号線毎に上方シールド４０１ａを設ける図５の具体例の場合と比較して、比較的容易に上方シールド４０１ｂを形成できる。この際、複数の画素信号線など、相互に電磁波が及ぼす影響が基本的に小さい複数の信号線を一つの上方シールド４０１ｂにより纏めて電気遮蔽するようにし、他方で、例えば画像信号線とクロック信号線など、相互に電磁波が及ぼす影響が基本的に大きい信号線を相互に別個の上方シールド４０１ｂにより電気遮蔽するとよい。即ち、これにより、複数の信号線を纏めて電気遮蔽する際の不利益を最小限に抑えることができる。

【００９０】図７の具体例では、図５に示した上方シールド４０１ａに加えて、画像表示領域における下側遮光膜１１ａと同一導電膜からなる下方シールド１１ｂより、配線４００は上下方向から電気遮蔽されている。

【００９１】図８の具体例では、図５に示した上方シールド４０１ａに加えて、画像表示領域における走査線３ａと同一導電膜からなる下方シールド４０２より、配線４００は上下方向から電気遮蔽されている。

【００９２】図９の具体例では、図７と同様の上方シールド４０１ｃ及び下方シールド１１ｂに加えて、上方シールド４０１ｃと同一導電膜から延設されてなり、下地絶縁膜１２、第１層間絶縁膜４１、誘電体膜７５及び第２層間絶縁膜４２に配線４００に沿って溝状に掘られた穴に埋め込まれた側方シールド４０１ｄにより、配線４００は上下左右方向から電気遮蔽されている。特にこの具体例では、シールドは、１本の配線４００毎に全周を電気遮蔽しているので、複数の配線４００相互間の電磁波による悪影響を極力低減できる。

【００９３】図１０の具体例では、図８と同様の上方シールド４０１ｃ及び下方シールド４０２に加えて、上方シールド４０１ｃと同一導電膜から延設されてなり且つ第１層間絶縁膜４１、誘電体膜７５及び第２層間絶縁膜４２に配線４００に沿って溝状に掘られた穴に埋め込まれた側方シールド４０１ｅにより、配線４００は上下左右方向から電気遮蔽されている。特にこの具体例では、シールドは、１本の配線４００毎に全周を電気遮蔽しているので、複数の配線４００相互間の電磁波による悪影響を極力低減できる。以上説明したように本実施形態の電気光学装置によれば、画像表示領域では、容量線３００をなす第１導電膜上に、データ線６ａをなす第２導電膜が層間絶縁膜を介して積層されている。周辺領域では、これら第１導電膜及び第２導電膜の一方から、周辺回路に接続された配線４００が形成されており、これら第１導電膜及び第２導電膜の他方から、配線４００を少なくとも一方向（例えば、上方や下方）から電気遮蔽するシールドが形成されている。従って、画像信号線等の配線４００上の画像信号等への電磁ノイズの飛び込みを効果的に低減できる。しかも、周辺領域に配線４００やシールドを形成するために専用の膜を別途形成しないで済むので、装置構成及び製造工程を簡略化する上でも有利である。特に、画像品位の向上のために画素ピッチを微細化し駆動周波数を高めた場合に、一般にこのような信号線に係るノイズ（例えば、クロック信号線や波形選択信号線等の制御信号線から画像信号線上の画像信号への電磁ノイズ、外部装置や他の回路等からの画像信号線上の画像信号への電磁ノイズ、クロック信号線や波形選択信号線等の制御信号線から外部装置や他の回路等への電磁ノイズなど）は相対的に増加する（即ち、Ｓ／Ｎは低下する）。従って、本実施形態のように周辺領域に配線された画像信号線、制御信号線等の配線４００を、上方シールド４０１ａ、４０１ｂ又は４０１ｃ、下方シールド１１ｂ又は４０２、側方シールド４０１ｄ又は４０１ｅ等のシールドにより電気遮蔽する構成は、画素ピッチを微細化し或いは駆動周波数を高める上で大変有利である。

【００９４】また本実施形態では特に配線４００として画像信号線を電気遮蔽するので、ノイズ源としての他の信号線や配線或いは回路や素子からの画像信号線上の画像信号Ｓ１、Ｓ２、…への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的に高いＳ／Ｎを持つ画像信号Ｓ１、Ｓ２、…に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００９５】また以上説明した実施形態では、図４に示した画像信号線とサンプリング回路３０１とを中継接続する中継配線３０５やサンプリング回路駆動信号線３０６を、図５から図１０に示したように上方、下方或いは側方から電気遮蔽してもよい。このようにすれば、中継

配線３０５上の画像信号Ｓ１、Ｓ２、…への電磁ノイズの飛び込みや、サンプリング回路駆動信号線３０６上のサンプリング回路駆動信号Ｑ１、Ｑ２、…への電磁ノイズの飛込みを効果的に低減できる。これらの中継配線３０５やサンプリング回路駆動信号線３０６は、対向基板２０に設けられる対向電極２１に対向する部分を含むので、これらの配線と対向電極２１との寄生容量を低減する観点から、両者間に配置される上方シールドにより電気遮蔽すると特に効果的である。

【００９６】更に以上説明した実施形態では、クロック信号線としての配線４００（ＣＬＸ）、配線４００（ＣＬＸ’）や、波形選択信号線としての配線４００（ＥＮＢ１）、配線４００（ＥＮＢ２）を図５から図１０に示したように上方、下方或いは側方から電気遮蔽してもよい。このように構成すれば、これらの制御信号線上にあり、一般には画像信号に対するノイズ源となり易い高周波数で高電位である制御信号に起因する高周波で強力な電磁ノイズが、画像信号線等上の画像信号に飛び込むことを効果的に阻止できる。

【００９７】以上説明した本発明の電気光学装置（各実施形態を含む）では、シールドは、好ましくは接地電位や他の定電位に固定される。この際特に、画像信号線（配線４００（ＶＩＤ１）、配線４００（ＶＩＤ２）、…など）と制御信号線（配線４００（ＣＬＸ）、配線４００（ＣＬＸ’）、…など）とを別々に電気遮蔽すると共に相互に異なる定電位に固定するのがより好ましい。このように構成すれば、同一の定電位配線を介して両信号線間でそれらの電位変動が相互に影響を及ぼす事態を未然防止できる。例えば、画像信号線を低電位（接地電位或いは数ボルト程度）の第１定電位の定電位線に接続することにより低電位で電気遮蔽し、制御信号線を高電位（十数ボルト程度）の第２定電位の定電位線に接続することにより高電位で電気遮蔽すればよい。

【００９８】加えて本実施形態では、シールドと電源配線の本線又は分岐配線とを共用するのが好ましい。このように構成すれば、装置構成及び製造工程の簡略化を図りつつ、シールドを定電位に固定できる。しかも、周辺領域におけるシールドが占める領域を電源配線に割り当てることになるので、電源配線を比較的容易に幅広に構成することができる。更に、シールドを幅広に形成することにより、シールドの性能も向上するので一層有利である。

【００９９】また図５から図１０に示した各種具体例では、配線４００を容量線３００と同一導電膜から形成し且つシールドを容量線３００と異なる導電層から形成したが、配線４００をデータ線６ａと同一導電膜から形成し且つシールドをデータ線６ａと異なる導電層から形成してもよいし、配線４００を走査線３ａと同一導電膜から形成し且つシールドを走査線３ａと異なる導電層から形成してもよいし、配線４００を下側遮光膜１１ａと同一導電膜から形成し且つシールドを下側遮光膜１１ａと異なる導電層から形成してもよい。

【０１００】更に、シールドの一部を、配線と同一膜から形成することも可能であり、この場合には主に側方から電気遮蔽することが可能である。本実施形態では、図４に示したように、同一平面内で、負電源ＶＳＳＹを供給する配線４００（ＶＳＳＹ）及び負電源ＶＳＳＸを供給する配線４００（ＶＳＳＸ）は、画像信号線たる配線４００（ＶＩＤ２）、配線４００（ＶＩＤ４）、配線４００（ＶＩＤ６）、…を囲んでおり、画像信号シールド線として機能している。同様に同一平面内で、正電源ＶＤＤＹを供給する配線４００（ＶＤＤＹ）及び負電源ＶＳＳＸを供給する配線４００（ＶＳＳＸ）は、画像信号線たる配線４００（ＶＩＤ１）、配線４００（ＶＩＤ３）、配線４００（ＶＩＤ５）、…を囲んでおり、画像信号シールド線として機能している。更に、正電源ＶＤＤＸを供給する配線４００（ＶＤＤＸ）は、やはり同一平面内で、クロック信号線たる配線４００（ＣＬＸ）、配線４００（ＣＬＸ’）等の制御信号線を囲んでおり、制御信号シールド線として機能している。同様に正電源ＶＤＤＹを供給する配線４００（ＶＤＤＹ）は、やはり同一平面内で、クロック信号線たる配線４００（ＣＬＹ）、配線４００（ＣＬＹ’）等の制御信号を囲んでおり、制御信号シールド線として機能している。特に図４中で、破線で示したように、制御信号シールド線としての配線４００（ＶＤＤＸ）の２つの先端は、接続部９３により相互に接続されてもよいし、同様に画像信号シールド線としての配線４００（ＶＳＳＸ）の２つの先端は、接続部９１により相互に接続されてもよい。

【０１０１】更にまた、積層された２つの導電膜を共に低抵抗のＡｌ膜から構成することも可能であり、これにより、低抵抗の配線を低抵抗の導電膜で電気遮蔽することが可能となり、非常に電磁ノイズが飛び込み難い構成が得られる。

【０１０２】以上説明した実施形態では、図３に示したように多数の導電層を積層することにより、画素電極９ａの下地面（即ち、第３層間絶縁膜４３の表面）におけるデータ線６ａや走査線３ａに沿った領域に段差が生じるのを、第３層間絶縁膜４３の表面を平坦化することで緩和しているが、これに代えて或いは加えて、ＴＦＴアレイ基板１０、下地絶縁膜１２、第１層間絶縁膜４１、第２層間絶縁膜４２或いは第３層間絶縁膜４３に溝を掘って、データ線６ａ等の配線やＴＦＴ３０等を埋め込むことにより平坦化処理を行ってもよいし、第２層間絶縁膜４２の上面の段差をＣＭＰ（Chemical Mechanical Polishing）処理等で研磨することにより、或いは有機ＳＯＧを用いて平らに形成することにより、当該平坦化処理を行ってもよい。

【０１０３】尚、以上説明した実施形態では、画素スイッチング用ＴＦＴ３０は、好ましくは図３に示したよう

にＬＤＤ構造を持つが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物の打ち込みを行わないオフセット構造を持ってよいし、走査線３ａの一部からなるゲート電極をマスクとして高濃度で不純物を打ち込み、自己整合的に高濃度ソース及びドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。また本実施形態では、画素スイッチング用ＴＦＴ３０のゲート電極を高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。このようにデュアルゲート或いはトリプルゲート以上でＴＦＴを構成すれば、チャネルとソース及びドレイン領域との接合部のリーク電流を防止でき、オフ時の電流を低減することができる。

【０１０４】加えて、以上説明した本発明の実施形態の変形として、周辺領域で配線４００に対して、図５から図１０に示した如き各種シールドを設けるのに代えて又は加えて、容量線３００、データ線６ａ、走査線３ａ及び下側遮光膜１１ａの４つの導電膜のうちの一つから、制御信号線たる配線４００（ＣＬＸ）、配線４００（ＣＬＹ）、…を形成すると共に、これら４つの導電膜の他の一つから、画像信号線たる配線４００（ＶＩＤ１）、配線４００（ＶＩＤ２）、…を形成してもよい。このように構成すれば、同一導電膜をパターニングすることにより同一平面内にこれら２種類の配線を形成する場合と比べると、両信号線は基板に垂直な方向に離間し且つ両信号線間に層間絶縁膜が配置されている分だけ、両信号線間におけるノイズの飛び込みを低減できるので有利である。即ち、シールドがなくとも、このように基板に垂直な方向に離間するように、これら２種類の信号線を形成することにより、ノイズを低減することが可能となるのである。更に、このような構成と上述した各種シールドとを組み合わせることにより、電磁ノイズを低減する効果を一層高めることができる。

【０１０５】（電気光学装置の全体構成）以上のように構成された各実施形態における電気光学装置の全体構成を図１１及び図１２を参照して説明する。尚、図１１は、ＴＦＴアレイ基板１０をその上に形成された各構成要素と共に対向基板２０の側から見た平面図であり、図１２は、図１１のＨ－Ｈ’断面図である。

【０１０６】図１２において、ＴＦＴアレイ基板１０の上には、シール材５２がその縁に沿って設けられており、その内側に並行して、画像表示領域１０ａの周辺を規定する額縁としての遮光膜５３が設けられている。シール材５２の外側の領域には、データ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、走査線駆動回路１０４が、この一辺に隣接する２辺に沿って設けられている。走査線３ａに供給される走査信号遅延が問題にならないのならば、走査線駆動回路１０４は片側だけでも良いことは言うまでもない。また、データ線駆動回路１０１を画像表示領域１０ａの辺に沿って両側に配列してもよい。更にＴＦＴアレイ基板１０の残る一辺には、画像表示領域１０ａの両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられている。また、対向基板２０のコーナー部の少なくとも１箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的に導通をとるための上下導通材１０６が設けられている。また図４に示したサンプリング回路３０１が額縁領域に設けられている。そして、図１２に示すように、図１１に示したシール材５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材５２によりＴＦＴアレイ基板１０に固着されている。

【０１０７】尚、ＴＦＴアレイ基板１０上には、これらのデータ線駆動回路１０１、走査線駆動回路１０４、サンプリング回路３０１等に加えて、複数のデータ線６ａに所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等を形成してもよい。

【０１０８】以上図１から図１２を参照して説明した実施形態では、データ線駆動回路１０１及び走査線駆動回路１０４をＴＦＴアレイ基板１０の上に設ける代わりに、例えばＴＡＢ（Tape Automated bonding）基板上に実装された駆動用ＬＳＩに、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して電気的及び機械的に接続するようにしてもよい。また、対向基板２０の投射光が入射する側及びＴＦＴアレイ基板１０の出射光が出射する側には各々、例えば、ＴＮモード、ＶＡ（Vertically Aligned）モード、ＰＤＬＣ（Polymer Dispersed LiquidCrystal）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【０１０９】以上説明した実施形態における電気光学装置は、プロジェクタに適用されるため、３枚の電気光学装置がＲＧＢ用のライトバルブとして各々用いられ、各ライトバルブには各々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が投射光として各々入射されることになる。従って、各実施形態では、対向基板２０に、カラーフィルタは設けられていない。しかしながら、画素電極９ａに対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２０上に形成してもよい。このようにすれば、プロジェクタ以外の直視型や反射型のカラー電気光学装置について、各実施形態における電気光学装置を適用できる。また、対向基板２０上に１画素１個対応するようにマイクロレンズを形成してもよい。あるいは、ＴＦＴアレイ基板１０上のＲＧＢに対向する画素電極９ａ下にカラーレジスト等でカラーフィルタ層を形成することも可能である。この

ようにすれば、入射光の集光効率を向上することで、明るい電気光学装置が実現できる。更にまた、対向基板２０上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー電気光学装置が実現できる。

【０１１０】本発明は、上述した実施形態に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨或いは思想に反しない範囲で適宜変更可能であり、そのような変更を伴なう電気光学装置及びその製造方法もまた本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【図１】本発明の実施形態の電気光学装置における画像表示領域を構成するマトリクス状の複数の画素に設けられた各種素子、配線等の等価回路である。

【図２】実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。

【図３】図２のＡ－Ａ’断面図である。

【図４】本実施形態におけるＴＦＴアレイ基板上に設けられたシールドを含む各種配線、周辺回路等の構成を示す図式的な平面図である。

【図５】本実施形態で採用可能なシールドの一具体例に係る図４のＢ－Ｂ’断面図である。

【図６】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図７】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図８】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図９】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図１０】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

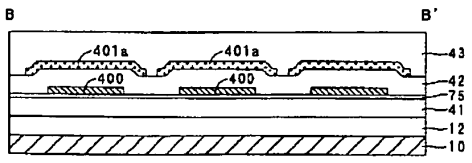
【図１１】実施形態の電気光学装置におけるＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図である。

【図１２】図１１のＨ－Ｈ’断面図である。

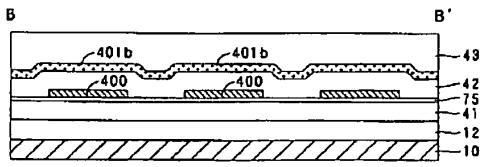
【符号の説明】

１ａ…半導体層
１ａ’…チャネル領域
１ｂ…低濃度ソース領域
１ｃ…低濃度ドレイン領域
１ｄ…高濃度ソース領域
１ｅ…高濃度ドレイン領域
２…絶縁薄膜
３ａ…走査線
６ａ…データ線
９ａ…画素電極
１０…ＴＦＴアレイ基板
１１ａ…下側遮光膜
１２…下地絶縁膜
１６…配向膜
２０…対向基板
２１…対向電極
２２…配向膜
３０…ＴＦＴ
５０…液晶層
７０…蓄積容量
７１…中継層
７５…誘電体膜
８１、８３、８５…コンタクトホール
１０１…データ線駆動回路
１０１ａ…シフトレジスタ回路
１０１ｂ…波形制御回路
１０１ｃ…バッファ回路
１０４…走査線駆動回路
３００…容量線
３０１…サンプリング回路
３０２…サンプリング回路のＴＦＴ
３０５…中継配線
３０６…サンプリング回路駆動信号線
４００…配線
４０１ａ、４０１ｂ、４０１ｃ…上方シールド
４０１ｄ、４０１ｅ…側方シールド
４０２…下方シールド

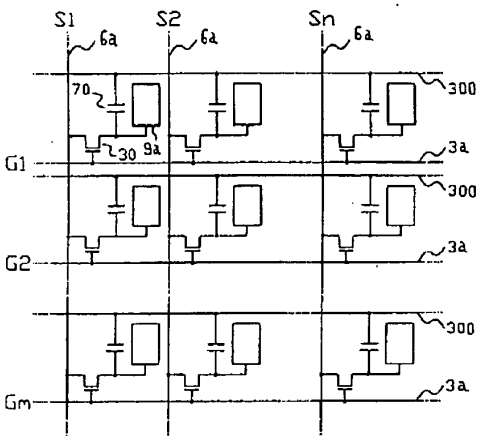
【図５】



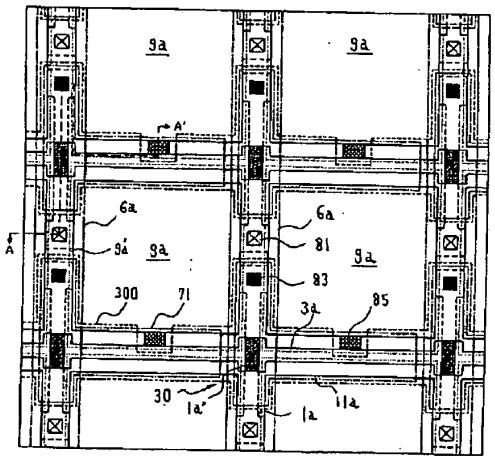
【図６】



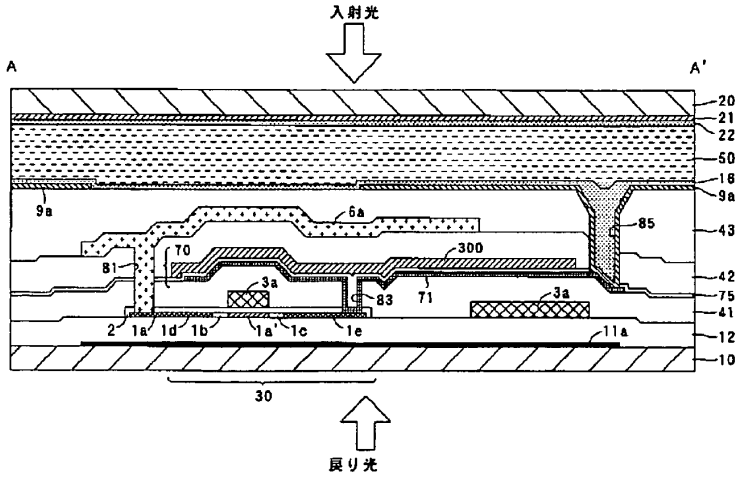
【図1】


S1
S2
Sn
6a
70
30
9a
300
3a
G1
G2
Gm

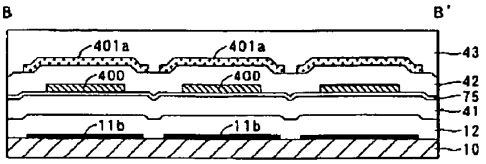
【図2】


9a
A
A'
6a
9a'
81
83
300
71
3a
85
30
1a'
1a
11a

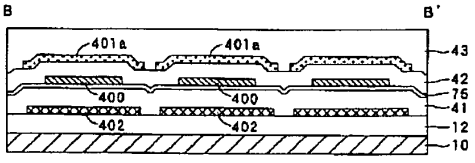
【図3】


入射光
A
A'
20
21
22
50
18
9a
6a
85
43
70
300
81
3a
83
71
42
75
41
2
1a
1d
1b
1a'
1c
1e
11a
12
10
30
戻り光

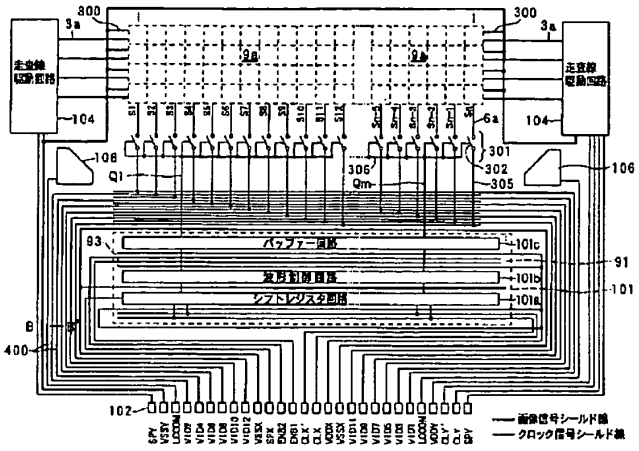
【図7】


B
B'
401a
401a
43
400
400
42
75
41
11b
11b
12
10

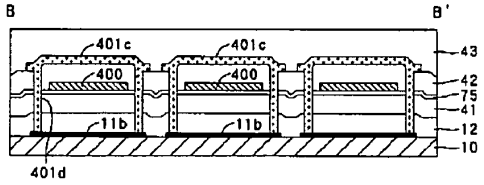
【図8】


B
B'
401a
401a
43
42
400
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75
41
402
402
12
10

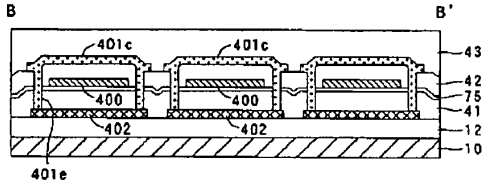
【図4】



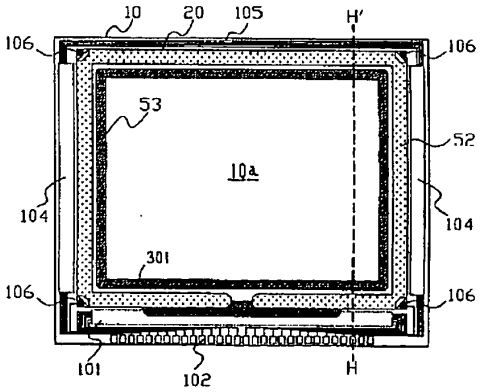
【図9】



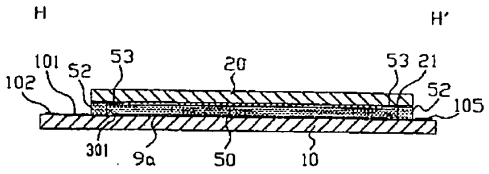
【図10】



【図11】



【図12】



フロントページの続き

(51)Int.Cl.[7]	識別記号	FI		テーマコード(参考)
G09F 9/30	330	G09F 9/30	338	5G435
	338	G09G 3/20	611C	

// G09G	3/20	611				623L
		623			3/36	
	3/36			G02F	1/136	500

Fターム(参考) 2H092 GA35 GA59 GA64 JB24 JB33
JB54 JB64 JB66 JB69 NA23
NA25 PA06 PA09 RA05
2H093 NA16 NC13 NC23 NC35 ND40
NE02 NE03 NG02
5C006 BB16 BC12 BC22 BC23 BF11
EB05 EC11 FA32
5C080 AA10 BB05 DD12 FF11 JJ02
JJ06
5C094 AA03 AA05 AA07 AA09 AA53
AA56 BA03 BA43 CA19 CA25
DA09 DA13 DB01 DB04 DB10
EA04 EA10 EB02 FA01 FA02
FB12 FB14 FB15 GA10
5G435 AA16 BB12 CC09 EE37 HH12
HH14

Issue Classification	Application/Control No. 10/852,255	Applicant(s)/Patent under Reexamination MURADE, MASAO
	Examiner (Nancy) Thanh-Nhan P. Nguyen	Art Unit 2871

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
349	149	G 2 F 1 /1345	/

CROSS REFERENCES											
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
349	150	151	152				/				/
345	87						/				/
							/				/
							/				/
							/				/

(Nancy) Thanh-Nhan P Nguyen 5/14/2006
(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

David Nelms
Supervisory Patent Examiner
(Primary Examiner) (Date)
Technology Center 2800
5/06

Total Claims Allowed: 13

O.G. Print Claim(s)	O.G. Print Fig.
1	5

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
4	4		34		64		94		124		154		184
5	5		35		65		95		125		155		185
7	6		36		66		96		126		156		186
8	7		37		67		97		127		157		187
6	8		38		68		98		128		158		188
9	9		39		69		99		129		159		189
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	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 4122

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/852,255	05/25/2004 RULE	349	2871	119570

APPLICANTS

Masao Murade, Suwa-shi, JAPAN;

** CONTINUING DATA ********N/A**********

** FOREIGN APPLICATIONS **********TN
JAPAN 2003-156832 06/02/2003 NO
JAPAN 2004-081532 03/19/2004 NO

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 07/21/2004

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☑ yes ☐ no 35 USC 119 (a-d) conditions met ☑ yes ☐ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature TN Initials	COUNTRY JAPAN	DRAWING 10	CLAIMS 16	CLAIMS 2

ADDRESS
25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA , VA
22320

TITLE
Electro-optical device and electronic apparatus comprising the same

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED 900	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/852,255	MURADE, MASAO
Examiner	**Art Unit**
(Nancy) Thanh-Nhan P. Nguyen	2871

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	5/14/06
1	1	=
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Claim		Date
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Claim		Date
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
10/852,255	MURADE, MASAO
Examiner	**Art Unit**
(Nancy) Thanh-Nhan P. Nguyen	2871

SEARCHED			
Class	Subclass	Date	Examiner
349	149	5/14/2006	TN
349	150		
349	151		
349	152		
345	87	5/14/2006	TN

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
349	**149 150**	**5/14/2006**	**TN**
349	151 152	5/14/2006	TN
345	87	5/14/2006	TN

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST UPDATE SEARCH -- see print out --	5/14/2006	TN
INTERFERENCE SEARCH --see print out --	5/14/2006	TN
Consulted with Primary Examiner Julie Ngo.	5/14/2006	TN

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((peripheral (off adj display)) NEAR (region area)) AND (display NEAR (region area)) AND (external ADJ circuit ADJ3 terminal) AND (wiring ADJ line) AND ((peripheral gate data scanning) ADJ driving) AND (intersect$5) AND ((counter common upper opposite) ADJ electrode) AND (potential adj line)	US-PGPUB	OR	ON	2006/05/14 22:21
L2	1	((peripheral (off adj display)) NEAR (region area)) AND (display NEAR (region area)) AND (external ADJ circuit ADJ3 terminal) AND (wiring ADJ line) AND ((peripheral gate data scanning) ADJ driving) AND (intersect$5) AND ((counter common upper opposite) ADJ electrode) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:22
L3	1	((peripheral (off adj display)) NEAR (region area)) AND (display NEAR (region area)) AND (external ADJ circuit ADJ3 terminal) AND (wiring ADJ line) AND ((peripheral gate data scanning) ADJ driving) AND (intersect$5) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:23
L4	1	((peripheral (off adj display)) NEAR (region area)) AND (display NEAR (region area)) AND (external ADJ circuit ADJ3 terminal) AND ((peripheral gate data scanning) ADJ driving) AND (intersect$5) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:23
L5	1	((peripheral (off adj display)) NEAR (region area)) AND (display NEAR (region area)) AND (external ADJ circuit) AND ((peripheral gate data scanning) ADJ driving) AND (intersect$5) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:23
L6	1	(external ADJ circuit) AND ((peripheral gate data scanning) ADJ driving) AND (intersect$5) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:24
L7	1	(external ADJ circuit) AND ((peripheral gate data scanning) ADJ driving) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:24

EAST Search History

L8	9	(external ADJ circuit) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:25
L9	26	(external NEAR3 circuit) AND (potential adj line).CLM.	US-PGPUB	OR	ON	2006/05/14 22:25

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	1	("20050162605").PN.	US-PGPUB; USPAT	OR	OFF	2006/05/14 11:40
L8	3358	345/87.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/14 12:26
L9	125	(349/149-152.ccls. 345/87.ccls.) and (external near2 circuit near2 terminal (potential adj line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/14 12:30
L10	11	(349/149-152.ccls. 345/87.ccls.) and (external near2 circuit near2 terminal (potential adj line)).CLM.	US-PGPUB	OR	ON	2006/05/14 12:29
L11	16	("349"/$.ccls. 345/87.ccls.) and (external near2 circuit near2 terminal (potential adj line)).CLM.	US-PGPUB	OR	ON	2006/05/14 12:29
L12	430	("349"/$.ccls. 345/87.ccls.) and (external near2 circuit near2 terminal (potential adj line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/14 12:31
S32	1	("20050162605").PN.	US-PGPUB; USPAT	OR	OFF	2006/05/13 15:20
S33	1	("6011607").PN.	US-PGPUB; USPAT	OR	OFF	2006/05/13 15:20
S34	4	("5742074" | "5745202" | "6406946" | "6680773").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/05/13 21:16
S35	1940	349/149-152.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/13 21:33
S36	1630	349/149-152.ccls. and (circuit terminal (potential adj line))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/14 12:27



IPW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/852,255

Examiner: T. NGUYEN

Filed: May 25, 2004

Docket No.: 119570

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the November 15, 2005 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims;

Amendments to the Drawings include an attached replacement sheet; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device, comprising:

a plurality of pixel portions provided in an image display region on an element substrate;

in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines,

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.

2. (Original) The electro-optical device according to Claim 1,

sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward

the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

3. (Original) The electro-optical device according to Claim 2,

the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.

4. (Currently Amended) The electro-optical device according to Claim 1, ~~further comprising:~~

~~a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate; and~~

~~upper and lower conduction terminals that are provided in the peripheral region on the element substrate, in order to connect a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, and the counter electrode,~~

~~the counter electrode potential line of the plurality of main wiring lines being positioned near edges of the element substrate in the peripheral region, and~~

the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.

5. (Original) The electro-optical device according to Claim 4,

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

6. (Currently Amended) The electro-optical device according to Claim 1, further comprising:

~~a counter electrode that is provided in the peripheral region on a counter substrate arranged to face the element substrate; and~~

~~upper and lower conduction terminals that are provided in the peripheral region on the element substrate, in order to couple a counter electrode potential line that supply counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, and the counter electrode,~~

~~the counter electrode potential line being positioned nearer edges of the element substrate than the one or plurality of main wiring lines excluding the counter electrode potential lines and nearer a center of the element substrate than the other or plurality of main wiring lines excluding the counter electrode potential line in the peripheral region,~~

a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

7. (Original) The electro-optical device according to Claim 6,

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.

8. (Original) The electro-optical device according to Claim 4,

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

9. (Original) The electro-optical device according to Claim 6,

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

10. (Original) The electro-optical device according to Claim 1,

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals and power source wiring lines that supply power source signals as electric signals, and

the pair of signal lines and power source wiring lines do not intersect each other.

11. (Original) The electro-optical device according to Claim 1,

the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.

12. (Original) The electro-optical device according to Claim 1,

the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film.

13-15. (Canceled)

16. (Original) An electronic apparatus, comprising the electro-optical device according to Claim 1.

Amendments to the Drawings:

The attached replacement drawing sheets makes changes to Figs. 5 and 7 and replace the original sheets with Figs. 5 and 7.

Attachment: Replacement Sheets

REMARKS

Claims 1-12 and 16 are pending in this application. By this Amendment, claims 1, 4 and 6 are amended and claims 13-15 are canceled. No new matter is added by this Amendment. Support for the language added to claim 1 is found, for example, in original claims 4 and 6.

I. Drawings

The Office Action objects to the drawings because:

- the reference "7" in Fig. 7 should be "70;"
- the sub-wiring lines with their first and second portions, as recited in claim 2, must be shown and labeled in the drawings; and
- the counter electrode potential line being positioned nearer edges of the element substrate than the one or plurality of main wiring lines excluding the counter electrode potential lines and nearer a center of the element substrate than the other or plurality of main wiring lines excluding the counter electrode potential line in the peripheral region, and a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, as recited in claim 6, must be shown and labeled in the drawings.

Applicant amends Fig. 7 to replace "7" with "70."

Applicant amends Fig. 5 to specifically identify the first portion and second portion of the sub-wiring lines.

Applicant notes that the line LCCOM (shown in at least Figs. 4 and 5) denotes the counter electrode potential line being positioned nearer edges of the element substrate than the one or plurality of main wiring lines excluding the counter electrode potential lines.

Applicant notes that the counter electrode potential line (LCCOM) being positioned nearer a center of the element substrate than the other or plurality of main wiring lines (108) excluding the counter electrode potential line in the peripheral region, is shown in at least Figs. 4 and 5.

Applicant notes that a part of the peripheral driving circuits (104) being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals (106t) and the counter electrode potential line (LCCOM) in the peripheral region, is shown in at least Figs. 4 and 5.

Applicant submits the requirements of the Patent Office have been met.

Withdrawal of the objections is respectfully requested.

II. Claim Objections

Claims 4, 6 and 14 are objected to for informalities.

Claim 14 is herein canceled; thus the objection to claim 14 is moot.

Claims 4 and 6 are objected to because "and the counter electrode," as recited in the last line of the second paragraph in each of these claims appears to be "extra." This feature is canceled from each of claims 4 and 6, thus the objection to claims 4 and 6 is moot.

III. Rejections Under 35 U.S.C. §102(b) and S103(a)

Claims 1-3, 10, 11, 13 and 14 are rejected under 35 U.S.C. §102(b) over JP 2002-049052 (Muraide); and claims 4-9, 12, 15 and 16 are rejected under 35 U.S.C. §103(a) over Muraide in view of U.S. Patent No. 6,011,607 (Yamazaki). These rejections are respectfully traversed.

Claim 1 recites that among the plurality of main wiring lines, the counter electrode potential line is the closest to edges of the element substrate. The Office Action acknowledges that Muraide fails to disclose this feature. However, the Office Action asserts that Yamazaki renders this feature obvious. In particular, the Office Action cites Fig. 1 of

Yamazaki and asserts that Yamazaki discloses a peripheral driver circuit integrally packed on the display, located inside the sealant, for the benefit of being protected from external moisture and contaminants. Applicant respectfully disagrees.

Yamazaki discloses a peripheral drive circuit region 103 of an active matrix display buried either in the liquid crystal material or in the sealing material, so that a user cannot directly touch it. See Fig. 1 and col. 1, lines 39-48 of Yamazaki. Here Yamazaki is clearly teaching either burying the peripheral drive circuit region in the sealant material or burying the peripheral drive circuit in the liquid crystal material (thus not in the peripheral region). Yamazaki does not disclose that among a plurality of main wiring lines, a counter electrode potential line, in the peripheral region, is the closest to edges of the element substrate.

However, the Office Action then asserts that it would have been obvious to dispose the peripheral drive circuit inside the sealant for the benefit of being protected from external moisture and contaminants and for long-term reliability, and therefore it would have also been obvious for:

1) the counter electrode potential line, among the plurality of main wiring lines, being positioned closest to edges of the element substrate in the peripheral region, as recited in claim 1;

2) the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, as recited in claim 4; and

3) the plurality of external circuit connection terminals being arranged along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals, as recited in dependent claim 5.

First, Yamazaki fails to disclose a peripheral driver circuit located inside the sealant in a peripheral region. However, even if Yamazaki did disclose such a feature, the Office Action has not identified adequate motivation as to why one or ordinary skill in the art would have been motivated, based on this feature, to modify Muraide so that:

1) the counter electrode potential line would be positioned closest to edges of the element substrate;

2) the peripheral driving circuits would be positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region; and

3) the plurality of external circuit connection terminals would be positioned along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals would be positioned near the end of an array of the plurality of external circuit connection terminals.

Muraide and/or Yamazaki simply do not disclose or suggest the above-identified features.

For the foregoing reasons, Muraide and Yamazaki, whether alone or in combination, fail to anticipate or render obvious the subject matter of claim 1, as well as the claims depending therefrom.

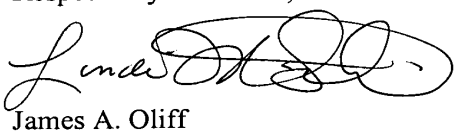
Withdrawal of the rejections is requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the pending claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Linda M. Saltiel
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JAO:LMS/axl

Date: February 15, 2006

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Fig. 5

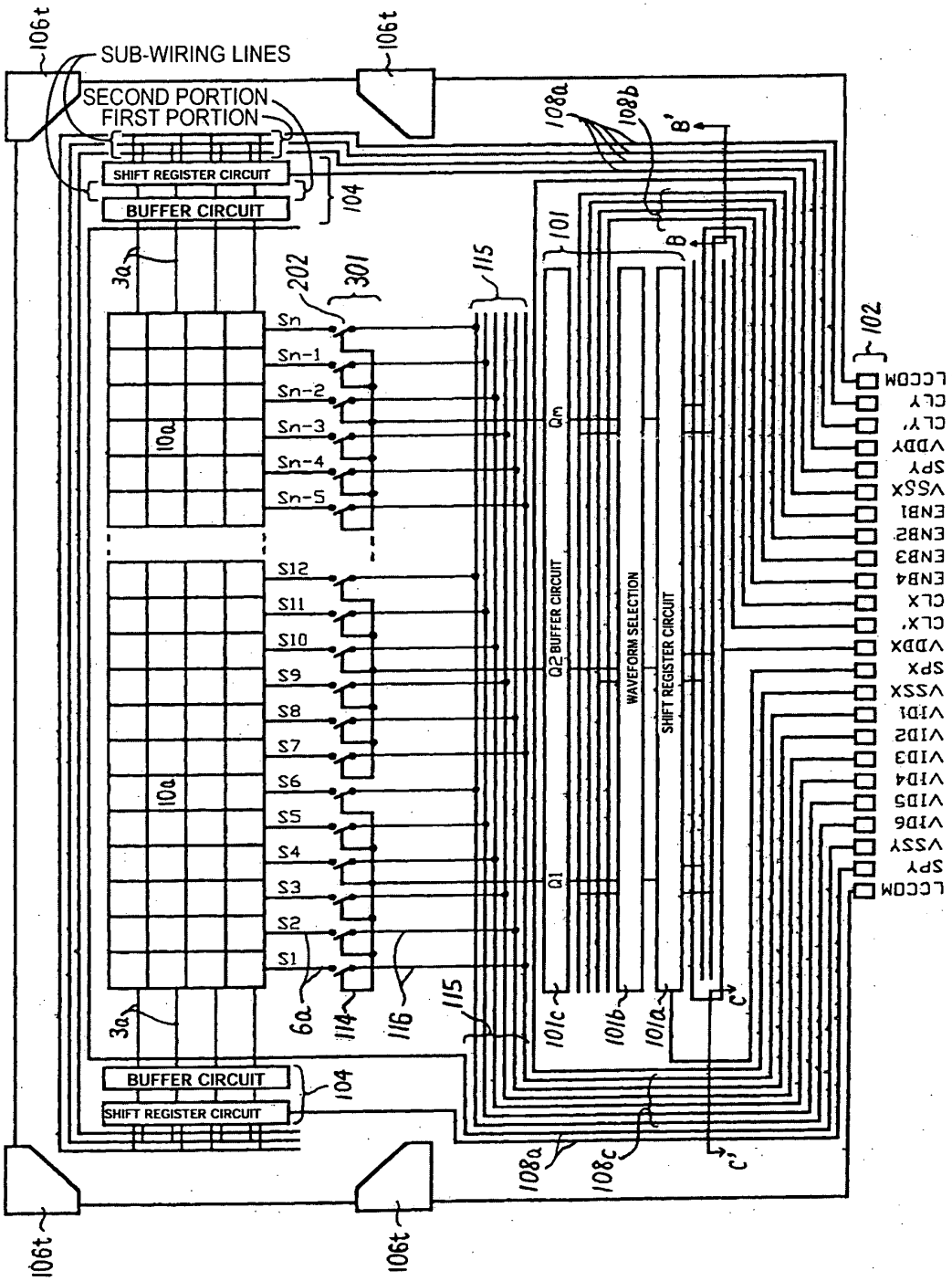
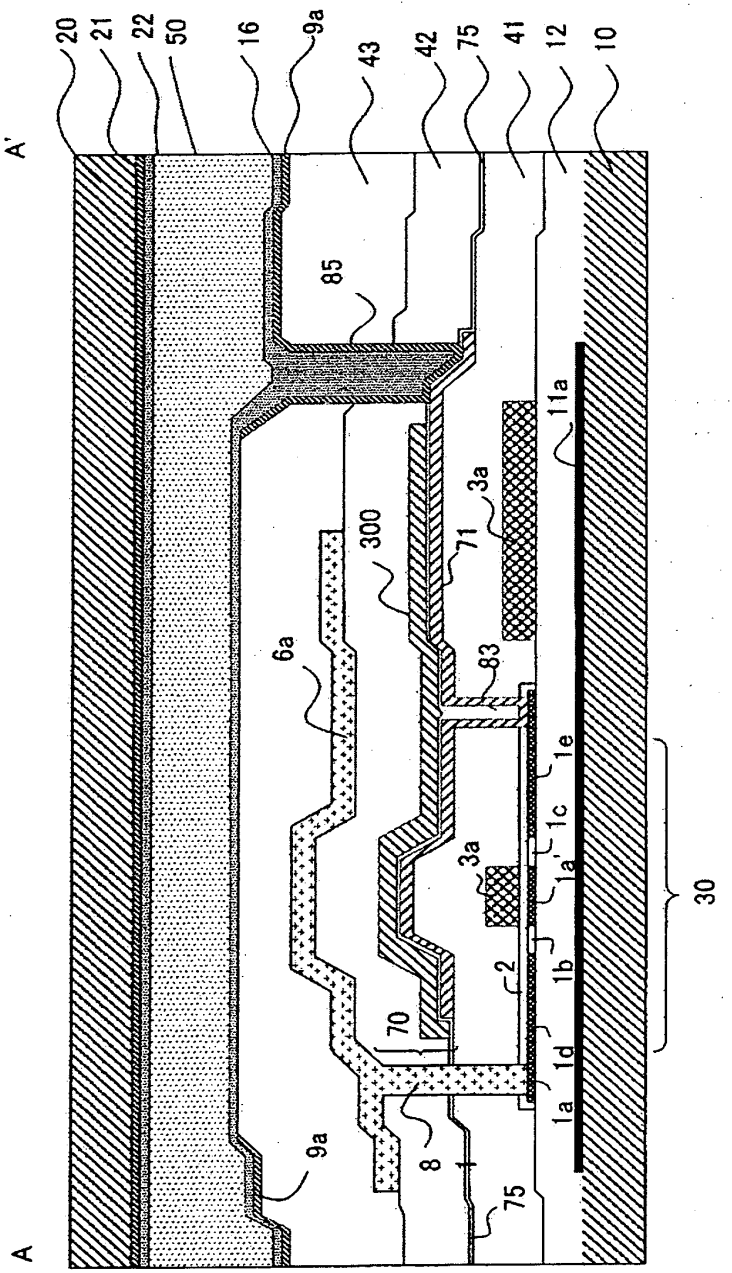
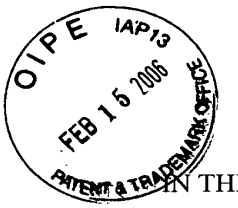


Fig. 7


A'
A
20
21
22
50
16
9a
43
42
75
41
12
10
85
11a
3a
71
300
6a
83
1e
1c
1a'
3a
2
1b
70
1d
1a
8
9a
75
30



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/852,255

Examiner: T. NGUYEN

Filed: May 25, 2004

Docket No.: 119570

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, Notice of Allowance or other action that closes prosecution (e.g., Quayle Action).

☒ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☒ 2. One or more reference cited herein was cited in a counterpart foreign application. See References 3 and 4.

☒ 3. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 4. Non-English language reference 3 corresponds to English language reference 2.

☒ 5. Non-English language reference 4 corresponds to English language reference 1.

Respectfully submitted,

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Date: February 15, 2006

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Form PTO-1449 (REV. 1/06) US Dept. of Commerce & TRADEMARK OFFICE	ATTY DOCKET NO. 119570	APPLICATION NO. 10/852,255
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Masao MURADE	
	FILING DATE May 25, 2004	GROUP 2871

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	1.	2002/0171638 A1	11/21/2002	Ishiyama
	2.	6,979,839 B2	12/27/2005	Murade

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	3.	KR A 2001-0105272 (corresponds to reference 2)	11/28/2001	Korea		
	4.	KR A 2002-0082425 (corresponds to reference 1)	10/31/2002	Korea		

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: February 15, 2006

특2001-0105272

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2001-083334 2001년03월22일 일본(JP)
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(54) 전기 광학 장치, 그 제조 방법 및 전자기기

요약

6개의 화상 신호선(122)은 데이터선(114)과 동일층으로 이루어지는 제 3 층의 배선이다. 여기서, 어떤 1개의 화상 신호선(122)으로부터 분기되어, 다른 화상 신호선(122)과 교차하는 배선(193)을, 제 1 층의 배선(112b)과 제 2 층의 배선(181b)과의 병렬 접속하여 이용한다. 이 중, 배선(112b)은 표시 영역에서의 주사선과 동일층으로 이루어지는 것이고, 배선(181b)은 표시 영역에서의 TFT의 배리어막과 동일층으로 이루어지기 때문에, 양 배선(112b),(181b)은 단독으로는 고저항이지만, 병렬 접속하는 것에 의해 저저항화를 도모한다. 또한, 다른 부분에서는, 제 2 층의 배선을 단독으로 이용하여, 설계할 때의 자유도를 향상시킨다.

이에 따라, 전기 광학 장치에 있어서, 샘플링 회로 등의 주변 회로를 설계할 때의 자유도를 향상시키거나, 주변 회로의 배선 저항을 저감시킨다.

대표도

도2

명세서

도면의 간단한 설명

도 1의 (a)는 본 발명의 실시예에 따른 전기 광학 장치의 액정 패널의 구성을 나타내는 사시도,

도 1의 (b)는 도 1의 (a)의 A-A' 선의 단면도,

도 2는 동(同) 액정 패널의 전기적인 구성을 나타내는 블럭도,

도 3은 동 액정 패널의 표시 영역에서의 등가 회로를 도시하는 도면,

도 4는 동 액정 패널의 동작을 설명하기 위한 타이밍 차트,

도 5는 동 액정 패널의 동작을 설명하기 위한 타이밍 차트,

도 6은 동 액정 패널의 표시 영역에서의 화소의 상세 구성을 나타내는 평면도,

도 7의 (a)는 도 6에 있어서의 B-B' 선의 단면도,

도 7의 (b)는 도 5에 있어서의 C-C' 선의 단면도,

도 7의 (c)는 동 액정 패널에 있어서의 축적 용량 소자의 구성을 나타내는 등가 회로,

도 8의 (a)는 동 액정 패널의 샘플링 회로 근방의 구성을 나타내는 평면도,

도 8의 (b)는 그 D-D' 선의 단면도,

도 9의 (a)는 동 액정 패널의 주사선 구동 회로의 일부 구성을 나타내는 평면도,

도 9의 (b)는 그 전기적 구성을 도시하는 도면,

도 10의 (a)~(c)는 각각 등 액정 패널에 있어서의 소자 기판의 제조 프로세스를 나타내는 단면도,

도 11의 (d)~(f)는 각각 등 액정 패널에 있어서의 소자 기판의 제조 프로세스를 나타내는 단면도,

도 12의 (g)~(i)는 각각 등 액정 패널에 있어서의 소자 기판의 제조 프로세스를 나타내는 단면도,

도 13의 (j)~(l)은 각각 등 액정 패널에 있어서의 소자 기판의 제조 프로세스를 나타내는 단면도,

도 14의 (m),(n)은 각각 등 액정 패널에 있어서의 소자 기판의 제조 프로세스를 나타내는 단면도,

도 15의 (a),(b)는 각각 본 발명의 변형예에 따른 전기 광학 장치의 샘플링 회로 근방의 구성을 나타내는 단면도,

도 16은 실시예에 따른 전기 광학 장치를 적용한 전자기기의 일례인 프로젝터의 구성을 나타내는 평면도,

도 17은 등 전자기기의 일례인 퍼스널 컴퓨터의 구성을 나타내는 사시도,

도 18은 등 전자기기의 일례인 휴대 전화의 구성을 나타내는 사시도.

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 주사선이나 데이터선을 구성하는 도전층과는 다른 도전층을 주변 회로에 이용하여, 주변 회로를 설계할 때의 자유도의 향상 등을 도모한 전기 광학 장치 및 그 제조 방법 및 해당 전기 광학 장치를 표시부에 이용한 전자기기에 관한 것이다.

일반적으로 전기 광학 장치, 예컨대, 전기 광학 물질에 액정을 이용하여 소정의 표시를 하는 액정 장치는 한 쌍의 기판 사이에 액정이 유지된 구성으로 되어 있다. 이 중, 예컨대 화소 전극을 3단자형의 스위칭 소자에 의해 구동하는 액티브 매트릭스형의 액정 장치는 다음과 같은 구성으로 되어 있다. 즉, 이러한 종류의 액정 장치는 한 쌍의 기판 중 한쪽의 기판에, 복수의 주사선과 복수의 데이터선이 서로 교차하도록 마련됨과 동시에, 이들의 교차 부분의 각각에는 박막 트랜지스터(Thin Film Transistor : 이하 「TFT」라고 칭함)에 대표되는 3단자형 스위칭 소자 및 화소 전극의 쌍이 마련된다. 여기서, TFT는 교차 부분에 대응하는 주사선에 공급되는 주사 신호가 액티브 레벨로 되면 온 상태로 되어, 대응하는 데이터선에 인가되는 화상 신호를 화소 전극에 공급하는 것이다.

또한, 다른쪽의 기판에는, 화소 전극에 대향하는 투명한 대향 전극이 마련된다.

한편, 이들의 주사선이나 데이터선을 구동하는 구동 회로는 주사선 구동 회로나, 데이터선 구동 회로, 샘플링 회로 등으로 구성된다. 이 중, 주사선 구동 회로는 주사선에 주사 신호를 소정 타이밍에서 공급하는 것이고, 또한 데이터선 구동 회로는 샘플링 신호를 소정 타이밍에서 공급하는 것이고, 또한 샘플링 회로는 데이터선마다 구비되는 샘플링 스위치에 의해서, 화상 신호선을 거쳐서 공급되는 화상 신호를, 샘플링 신호에 따라서 샘플링하여 대응하는 데이터선에 공급하는 것이다.

또한, 이를 구동 회로 자체를, 한쪽의 기판에서 화소 전극이 배열하는 영역(표시 영역)의 주변에 마련한 주변 회로 내장형의 전기 광학 장치가 개발되어 있다. 이 형태의 전기 광학 장치에서는, 제조 프로세스를 효율화하는 등의 관점에서, 구동 회로를 구성하는 능동 소자가 화소 전극에 접속된 스위칭 소자와 공통 프로세스로 형성된다. 예컨대, 상술한 액정 장치에 있어서, 구동 회로를 구성하는 소자는 화소 전극에 접속된 스위칭 소자와 동일 프로세스에 의해서 형성되는 TFT이다. 이러한 주변 회로 내장형의 전기 광학 장치는 구동 회로를 별도로 외부에 부착하는 형태의 전기 광학 장치와 비교하여, 장치 전체의 소형화나 비용 저하를 도모하는 데에 있어서 유리하다.

그런데 최근에는, 전기 광학 장치에 한정되지 않고 표시 장치 전반에 걸쳐, 예컨대 XGA(1024×768도트), SXGA(1365×1024도트), UXGA(1600×1200도트) 등과 같이, 고세밀화의 요청이 높아지고 있다.

발명이 이루고자 하는 기술적 과제

그러나, 고세밀화와 동시에 장치의 소형화를 도모하고자 하면, 이것에 대응하여 주사선의 배열 피치나 데이터선의 배열 피치를 대단히 좁게 하는 기술이 요구된다. 즉, 주사선 구동 회로는 주사선의 각각에 주사 신호를 공급하는 것이므로, 주사선 구동 회로를 구성하는 단위 회로(래치 회로) 등은 주사선의 배열 피치 내에 수납되어야 하다. 마찬가지로, 데이터선 구동 회로는 데이터선마다 마련되는 샘플링 스위치에 대하여 순서대로 샘플링 신호를 공급하는 것이므로, 데이터선 구동 회로를 구성하는 단위 회로 등은 데이터선의 배열 피치 또는 그 정수 배의 피치 내에 수납되어야 하다. 이와 같이, 주변 회로 내장형의 전기 광학 장치에 있어서, 고세밀화·소형화를 도모하고자 하면, 주사선 구동 회로나 데이터선 구동 회로에 있어서의 단위 회로 등을, 극히 한정된 공간 내에 수납하도록 형성해야 하기 때문에, 그 설계가 대단히 곤란하게 된다는 문제가 있었다.

본 발명은 상술한 사정에 감안하여 된 것으로, 그 목적으로 하는 것은 주변 회로에 있어서의 설계의 자유도 향상 등을 도모한 전기 광학 장치 및 그 제조 방법 및 해당 전기 광학 장치를 표시부에 이용한 전자기기를 제공하는 것에 있다.

본 발명의 상기 및 그 밖의 목적, 특징, 국면 및 이익 등은 첨부 도면을 참조로 하여 설명하는 이하의 상세한 실시예로부터 더욱 명백해질 것이다.

발명의 구성 및 작용

상술한 목적을 달성하기 위해서, 본 건의 제 1 발명에 따른 전기 광학 장치에 있어서는, 복수의 주사선 및 복수의 데이터선과, 상기 주사선 및 데이터선의 교차 부분에 대응하여 마련된 스위칭 소자 및 화소 전극의 쌍과, 상기 스위칭 소자와, 대응하는 화소 전극과의 사이를 전기적으로 접속하는 중간 도전막과, 상기 중간 도전막을 구성하는 도전층과 동일층으로 이루어지는 배선을 포함하고, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로를 구비하는 것을 특징으로 하고 있다.

이 구성에 따르면, 화소 전극이 배열하는 영역(표시 영역)에 있어서는, 스위칭 소자와 화소 전극과의 접속에 중간 도전막이 이용되지만, 이 중간 도전막과 동일한 도전층으로 이루어지는 배선이 주변 회로에 있어서도 이용되게 된다. 즉, 표시 영역에서 본래 이용되는 중간 도전막을, 본 발명에서는, 주변 회로 배선의 일부로도 이용하는 것이다. 이 때문에, 주변 회로에 있어서는, 새로운 배선층이 증가된 것으로 되기 때문에, 그 만큼 설계의 자유도가 향상되게 된다.

여기서, 본 발명에 있어서, 상기 중간 도전막은 스위칭 소자의 전극에 대응하여 마련된 제 1 콘택트 홀을 거쳐서 전기적으로 접속되는 한편, 상기 화소 전극은 제 2 콘택트 홀을 거쳐서 전기적으로 접속되는 구성이 바람직하다. 이 구성에서는, 스위칭 소자의 전극은 제 1 콘택트 홀을 거쳐서 중간 도전막에 접속되는 한편, 화소 전극은 제 2 콘택트 홀을 거쳐서 중간 도전막에 접속된다. 이 때문에, 중간 도전막은 화소 전극을 스위칭 소자의 타단에 접속할 때에, 버리어막으로서 기능하기 때문에, 콘택트 홀이 장거리에 걸치는 경우에 발생하는 불량을 저감하는 것이 가능해진다.

또한, 본 발명에 있어서, 일단이 상기 화소 전극에 접속되는 한편, 타단이 공통 접속되는 축적 용량 소자를 화소 전극마다 구비하고, 상기 중간 도전막은 상기 축적 용량 소자를 구성하는 전극의 일부를 이루는 구성도 바람직하다. 이 구성에 따르면, 화소 전극에 있어서의 전압 유지 특성이 축적 용량 소자에 의해 개선되지만, 이 때, 중간 도전막은 축적 용량 소자를 구성하는 전극의 일부로서 기능하게 된다.

또한, 본 발명에 있어서, 상기 중간 도전막은 차광성을 갖는 것이고, 상기 화소 전극을 투과 또는 반사하는 광의 일부가, 해당 중간 도전막에 의해서 규정되어 있는 구성으로 하여도 좋다. 이 구성에 따르면, 광의 투과 또는 반사 영역 중 중간 도전막에 의해서 규정되는 부분에서는, 적어도 전용의 차광막을 생략할 수 있으므로, 그 만큼 구성의 간략화가 가능해진다.

마찬가지로, 상술한 목적을 달성하기 위해서, 본 건의 제 2 발명에 따른 전기 광학 장치에 있어서는, 제 1, 제 2 및 제 3 도전층을, 이 순서로 형성하여 이루어지고, 상기 제 3 도전층은 상기 제 1 도전층보다도 저 저항인 전기 광학 장치로서, 상기 제 1 도전층으로 이루어지는 복수의 주사선과, 상기 제 3 도전층으로 이루어지고, 상기 복수의 주사선에 대하여 서로 교차하도록 형성된 복수의 데이터선과, 상기 주사선 및 상기 데이터선의 교차 부분에 대응하여 마련된 스위칭 소자 및 화소 전극의 쌍과, 제 2 도전층으로 이루어지고, 상기 스위칭 소자와 대응하는 화소 전극 사이를 전기적으로 접속하는 중간 도전막과, 상기 제 1, 제 2 및 제 3 도전층으로 이루어지는 배선을 각각 구비하여, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로를 구비하는 것을 특징으로 하고 있다.

이 구성에 따르면, 표시 영역에서는, 스위칭 소자와 화소 전극과의 접속에 중간 도전막이 이용되지만, 이 중간 도전막과 동일한 제 2 도전층으로 이루어지는 배선이 제 1 및 제 3 도전층으로 이루어지는 배선과 동시에 주변 회로에서도 이용되게 된다. 즉, 표시 영역에서 본래 이용되는 중간 도전막을, 본 발명에서는, 주변 회로에 있어서, 배선의 일부로서도 이용하는 것이다. 이 때문에, 주변 회로에서는, 1층만큼 새로운 배선층이 증가한 것으로 되기 때문에, 그 만큼 설계의 자유도가 향상되게 된다.

여기서, 본 발명에 있어서, 상기 중간 도전막은 스위칭 소자의 전극에 대응하여 마련된 제 1 콘택트 홀을 거쳐서 전기적으로 접속되는 한편, 상기 화소 전극은 제 2 콘택트 홀을 거쳐서 전기적으로 접속되는 구성이 바람직하다. 이 구성에서는, 스위칭 소자의 전극은 제 1 콘택트 홀을 거쳐서 중간 도전막에 접속되는 한편, 화소 전극은 제 2 콘택트 홀을 거쳐서 중간 도전막에 접속된다. 이 때문에, 중간 도전막은 화소 전극을 스위칭 소자의 타단에 접속할 때에, 버리어막으로서 기능하기 때문에, 콘택트 홀이 장거리에 걸치는 경우에 발생하는 불량을 저감하는 것이 가능해진다.

그런데, 본 발명에 있어서, 제 3 도전층은 제 1 도전층보다도 저 저항이기 때문에, 배선의 전부를 제 3 도전층에 의해 형성하는 것이 바람직하다. 단, 주변 회로에는 반드시 배선의 교차 부분이나 분기 부분 등이 존재하기 때문에, 배선의 전부를 제 3 도전층에 의해 형성하는 것은 불가능하다. 그래서, 본 발명에 있어서, 예컨대 고저항인 제 1 도전층으로 이루어지는 배선을 이용해야 하는 경우에, 상기 주변 회로는 상기 제 1 도전층으로 이루어지는 배선과 상기 제 2 도전층으로 이루어지는 배선이 전기적으로 병렬 접속된 병렬 배선을 갖는 구성이 바람직하다. 이와 같이, 제 1 도전층으로 이루어지는 배선과 제 2 도전층으로 이루어지는 배선이 전기적으로 병렬 접속된 병렬 배선을 이용하면, 제 1 또는 제 2 도전층으로 이루어지는 배선을 단독으로 이용하는 경우보다도, 그 배선 저항을 낮게 억제하는 것이 가능해진다.

이러한 병렬 배선을 이용해야 하는 부분으로는, 예컨대, 상기 제 3 도전층으로 이루어지는 배선으로부터 분기되는 분기 배선으로서, 해당 배선과는 다른 배선과 교차하는 부분이 고려된다. 이러한 분기 배선은 저 저항인 제 3 도전층으로 이루어져야 하지만, 제 3 도전층으로 이루어지는 배선으로서, 해당 배선과는 별도의 배선과 교차하는 부분은 동일한 제 3 도전층으로부터 형성할 수 없기 때문이다.

또한, 상기 주변 회로가 상기 제 3 도전층으로 이루어지고, h(h는 2이상의 정수)개의 데이터선에 대응하여 화상 신호를 공급하는 h개의 화상 신호선과, 상기 데이터선의 각각에 대응하여 마련되어, 상기 h개의 화상 신호선에 공급된 화상 신호 중, 대응하는 것을 소정의 샘플링 신호에 따라서 샘플링하여, 대응하는 데이터선에 공급하는 샘플링 스위치를 포함하는 경우, 병렬 배선을 이용해야 하는 부분으로서, 상기 화상 신호선으로부터 분기되어 상기 샘플링 스위치에 이르는 배선의 적어도 일부가 생각된다. 이러한 배선은 화소 전극에 인가되는 화상 신호를 공급하므로, 저 저항인 제 3 도전층으로 이루어져야 하지만, 다른 화

상 신호선과 교차시키기 위해서, 동일한 제 3 도전층으로부터 형성할 수가 없기 때문이다.

그런데, 본 발명에 있어서, 병렬 배선을 형성하는 경우, 상기 병렬 배선 중 상기 제 2 도전층으로 이루어지는 배선이, 해당 병렬 배선 중 상기 제 1 도전층으로 이루어지는 배선을 각각 노출하는 제 3 및 제 4 콘택트 홀의 사이를 도통하고, 상기 제 3 도전층으로 이루어지는 배선이, 상기 제 3 또는 제 4 콘택트 홀에 일치하는 위치에 마련되어, 상기 제 2 도전층으로 이루어지는 배선을 노출하는 제 5 콘택트 홀에 전기적으로 접속되어 있는 제 1 구성과, 상기 병렬 배선 중 상기 제 2 도전층으로 이루어지는 배선이, 해당 병렬 배선 중 상기 제 1 도전층으로 이루어지는 배선을 각각 노출하는 제 3 및 제 4 콘택트 홀의 사이를 도통하며, 상기 제 3 도전층으로 이루어지는 배선이 상기 제 3 및 제 4 콘택트 홀과는 다른 위치에 마련되어, 상기 제 1 도전층으로 이루어지는 배선을 노출하는 제 6 콘택트 홀에 전기적으로 접속되어 있는 제 2 구성이라고 생각된다. 여기서, 제 2 도전층에 휘어짐 등에 의한 응력이 걸려 있는 경우에, 제 2 도전층으로 이루어지는 배선을 노출시키는 것과 같은 콘택트 홀을 마련하면, 크랙이 발생해 버리는 경우가 있지만, 제 2 구성에서는, 제 2 도전층을 노출시키는 콘택트 홀을 마련하지 않기 때문에, 크랙의 발생에 따르는 불량의 저감을 도모할 수 있다.

또한, 제 1 또는 제 2 구성에 있어서는, 상기 병렬 배선 중 상기 제 2 도전층으로 이루어지는 배선이, 상기 제 3 및 제 4 콘택트 홀 사이에 마련된 하나 또는 복수의 콘택트 홀에 있어서도, 상기 제 1 도전층으로 이루어지는 배선과 도통되어 있는 것이 바람직하다. 이것에 의해, 병렬 배선에서는, 제 3 및 제 4 콘택트 홀 이외의 콘택트 홀에 있어서도, 병렬 접속되게 된다.

그런데, 본 발명에 있어서, 상기 주변 회로는, 그 일부의 영역에서, 상기 제 1, 제 2 및 제 3 도전층으로 이루어지는 배선을 구비하는 구성으로 하여도 좋다. 이 구성에 따르면, 동일 영역에서, 다른 3층 배선이 레이아웃되기 때문에, 공간의 축소화를 도모하는 것이 가능해진다.

또한, 본 발명에 있어서, 일단이 상기 화소 전극에 접속되는 한편, 타단이 공통 접속되는 축적 용량 소자를 화소 전극마다 구비하고, 상기 중간 도전막은 상기 축적 용량 소자를 구성하는 전극의 일부를 이루는 구성이 바람직하다. 이 구성에 따르면, 화소 전극에서의 전압 유지 특성이 축적 용량 소자에 의해 개선되지만, 이 때, 중간 도전막은 축적 용량 소자를 구성하는 전극의 일부로서 기능하게 된다.

이러한 축적 용량 소자는 상기 스위칭 소자의 전극과 상기 제 2 도전층으로 이루어지는 용량선에 의해 상기 스위칭 소자의 게이트 산화막을 유지하여 이루어지는 제 1 용량 소자와, 상기 중간 도전막과 상기 용량선에 의해 층간 절연막을 유지하여 이루어지는 제 2 용량 소자를 포함하는 구성이 바람직하다. 이 구성에 따르면, 축적 용량 소자는 제 1 용량 소자와 제 2 용량 소자를 포함하게 되기 때문에, 단일 용량의 구성과 비교하여, 용량의 증대를 도모하는 것이 가능해진다.

그런데, 본 발명에 있어서, 제 1 도전층은 폴리실리콘으로 이루어지는 것이 바람직하다. 그 이유는 주사선을 금속 박막이나 금속 실리사이드로부터 형성하면, 그 후의 고온 프로세스에서 박리가 발생하는 등의 문제가 생기기 때문이다.

또한, 본 발명에 있어서, 상기 제 3 도전층은 알루미늄으로 이루어지는 것이 바람직하다. 이것에 의해 제 3 도전층의 저저항화가 용이하게 된다.

또한, 본 발명에 있어서, 상기 제 2 도전층은 상기 제 3 도전층을 구성하는 재료보다도 고융점인 재료로 이루어지는 것이 바람직하다. 그 이유는 제 2 도전층을 형성한 후의 고온 프로세스에 의해, 용융이나 박리를 방지해야 하기 때문이다. 또, 이와 같이 고융점의 재료로서는, 폴리실리콘 외에, Ti(티탄), Cr(크롬), W(텅스텐), Ta(탄탈), Mo(몰리브덴) 또는 Pb(납)의 단체 혹은 이들의 합금, 금속 실리사이드 등을 들 수 있다.

다음에, 상술한 목적을 달성하기 위해서, 본 건의 제 3 발명에 따른 전기 광학 장치에 있어서는, 복수의 주사선 및 복수의 데이터선과, 상기 주사선 및 데이터선의 교차 부분에 대응하여 마련된 스위칭 소자 및 화소 전극의 쌍과, 상기 스위칭 소자와, 대응하는 화소 전극 사이를 전기적으로 접속하는 중간 도전막과, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로와, 상기 주변 회로에 접속되어 상기 중간 도전막을 구성하는 도전층과 동일층으로 이루어지는 배선을 구비하는 것을 특징으로 한다.

본 발명에서는, 주변 회로에 접속되는 배선을, 스위칭 소자와 화소 전극의 접속에 이용되는 중간 도전막과 동일한 도전층에 형성했다. 이 때문에, 새로운 배선층으로서 이용할 수 있기 때문에, 설계의 자유도가 향상된다.

여기서, 본 발명에 있어서, 상기 배선은 상기 데이터선을 구성하는 도전층과 동일층으로 이루어지는 화상 신호선에 대하여 하층에서 교차하는 것을 특징으로 한다. 이 구성에서는, 화상 신호선에 대하여 교차하는 배선을, 중간 도전막과 동일한 도전층을 배선으로서 이용할 수 있다.

또한, 상기 화상 신호선은 복수개의 화상 신호선이 배치되고, 각 화상 신호선에 대응하여 상기 배선이 접속되고, 각 배선의 크기는 거의 같은 것을 특징으로 한다. 이 구성에서는, 화상 신호에 접속되는 각 배선의 저항값을 같게 할 수 있어, 각 배선의 저항차에 의한 화상 신호의 격차를 방지하여, 양호한 표시가 가능하게 된다.

또한, 본 발명에 있어서, 상기 데이터선을 구성하는 도전층과 동일층으로 이루어지는 제 1 도전층과, 상기 데이터선을 구성하는 도전층과 동일층으로 되어 상기 제 1 도전층과 떨어진 위치에 형성된 제 2 도전층을 갖고, 상기 스위칭 소자의 반도체층과 동일층으로 이루어지는 제 3 도전층은 콘택트 홀을 거쳐서 상기 제 1 도전층과 상기 제 2 도전층에 대하여 전기적으로 접속되는 것을 특징으로 한다. 이 구성에 따르면, 스위칭 소자의 반도체층과 동일층으로 이루어지는 제 3 도전층을 바이패스로서 형성할 수 있다.

또한, 본 발명에 있어서, 상기 배선은 상기 제 3 도전층에 대하여 콘택트 홀을 거쳐서 전기적으로 접속되는 것을 특징으로 한다. 이 구성에 따르면, 배선과 제 3 도전층이 병렬하여 접속되기 때문에, 배선을 저저항으로 할 수 있다.

또한, 본 발명에 있어서, 상기 제 3 도전층은 폴리실리콘으로 이루어지는 것을 특징으로 한다. 이 구성

에 따르면, 배선을 고융점 금속 등으로 형성하여도, 배선은 폴리실리콘의 제 3 도전층에 대하여 콘택트 홀을 거쳐서 전기적으로 접속되기 때문에, 배선에 크랙이 생기는 일은 없다. 제 3 도전층은 제 1 도전층과 상기 제 2 도전층에 대하여 콘택트 홀을 거쳐서 전기적으로 접속되지만, 폴리실리콘으로 형성되어 있기 때문에, 폴리실리콘에 크랙이 생기는 일은 없다.

또한, 본 발명에 있어서, 상기 배선과 상기 제 3 도전층을 전기적으로 접속하는 콘택트 홀은 적어도 3개 갖는 것을 특징으로 한다. 이 구성에 따르면, 배선과 제 3 도전층 사이에서 여분의 배선을 형성할 수 있기 때문에, 배선이나 제 3 도전층에 크랙 등이 생기는 것에 의해 배선과 제 3 도전층 사이에서 단락되는 것을 방지할 수 있다.

또한, 본 발명에 있어서, 상기 제 1 도전층과 상기 제 2 도전층의 사이에, 상기 데이터선을 구성하는 도전층과 동일층으로 이루어지는 화상 신호선이 배치되어 있는 것을 특징으로 한다. 이 구성에 따르면, 데이터선을 구성하는 도전층과 동일층으로 이루어지는 화상 신호선이 제 1 도전층과 제 2 도전층에 간섭하는 일없이 배치할 수 있다.

또한, 본 건의 전자기기는 상술한 전기 광학 장치를 구비하기 때문에, 특히 주변 회로를 설계할 때의 자유도가 향상되게 된다.

다음에, 상기 목적을 달성하기 위해서, 본 건 제 4 발명에 따른 전기 광학 장치의 제조 방법에 있어서는, 복수의 주사선과 상기 복수의 주사선의 교차 부분에 대응하여 스위칭 소자 및 화소 전극의 쌍을 구비하는 전기 광학 장치의 제조 방법으로서, 상기 주사선 및 상기 데이터선이 교차해야 할 부분에 스위칭 소자를 형성하는 공정과, 상기 스위칭 소자에 접속되는 중간 도전막과, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로에 이용하는 배선을, 각각 동일한 도전층으로부터 형성하는 공정과, 상기 중간 도전막에 접속되는 화소 전극을 형성하는 공정을 구비하는 것을 특징이라고 하고있다. 이 제조 방법에 따르면, 상기 제 1 발명과 마찬가지로, 주변 회로에는, 새로운 배선층이 증가한 것으로 되기 때문에, 그 만큼, 설계의 자유도가 향상되게 된다.

또한, 상기 목적을 달성하기 위해서, 본 건 제 5 발명에 따른 전기 광학 장치의 제조 방법에 있어서는, 복수의 주사선과 상기 복수의 주사선의 교차 부분에 대응하여 스위칭 소자 및 화소 전극의 쌍을 구비하는 전기 광학 장치의 제조 방법으로서, 상기 주사선과 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로에 이용하는 배선을 각각 제 1 도전층으로 형성한 후에, 또한, 상기 주사선 및 상기 데이터선이 교차해야 할 부분에 스위칭 소자를 형성한 후에, 상기 스위칭 소자에 접속되는 중간 도전막과 상기 주변 회로에 이용하는 배선을 각각 제 2 도전층으로부터 형성하는 공정과, 상기 데이터선과 상기 주변 회로에 이용하는 배선을 각각 제 3 도전층으로부터 형성하는 공정과, 상기 중간 도전막에 접속되는 화소 전극을 형성하는 공정을 구비하는 것을 특징으로 하고 있다. 이 제조 방법에 따르면, 상기 제 2 발명과 마찬가지로, 주변 회로에는, 1층 분만큼 새로운 배선층이 증가한 것으로 되기 때문에, 그 만큼, 설계의 자유도가 향상되게 된다.

이하, 본 발명의 실시예에 대하여, 도면을 참조하여 설명한다.

(전기 광학 장치의 개략 구성)

우선, 본 실시예에 따른 전기 광학 장치에 대하여 설명한다. 이 전기 광학 장치는 전기 광학 물질로서 액정을 이용하여, 그 전기 광학적인 변화에 의해 소정의 표시를 행하는 것이다. 도 1의 (a)는 이 전기 광학 장치 중 외부 회로를 제외한 액정 패널(100)의 구성을 나타내는 사시도이며, 도 1의 (b)는 도 1의 (a)에 있어서의 A-A' 선의 단면도이다.

이들 도면에 나타내는 바와 같이, 액정 패널(100)은 각종 소자나 화소 전극(118) 등이 형성된 소자 기판(101)과, 대향 전극(108) 등이 마련된 대향 기판(102)이, 스페이서(도시 생략)를 포함하는 밀봉(seal)재(104)에 의해서 일정한 간격을 유지하여, 서로 전극 형성면이 대향되도록 접합됨과 동시에, 그 간격에 전기 광학 물질로서, 예컨대 TN(Twisted Nematic)형의 액정(105)이 봉입된 구성으로 되어 있다.

여기서, 소자 기판(101)에는 유리나 반도체, 석영 등이 이용되지만, 대향 기판(102)에는 유리 등이 이용된다. 또, 소자 기판(101)에 불투명한 기판이 이용되는 경우에는, 투과형이 아니라 반사형으로서 이용되는 것으로 된다. 또한, 밀봉재(104)는 대향 기판(102)의 주변을 따라 형성되지만, 액정(105)을 봉입하기 위해서 일부가 개구되어 있다. 이 때문에, 액정(105)의 봉입 후에, 그 개구 부분이 봉지재(106)에 의해서 봉지되어 있다.

다음에, 소자 기판(101)의 대향면으로서, 밀봉재(104)의 외측 1변의 영역(140a)에서는, 후술하는 데이터선 구동 회로가 형성되어, 샘플링 신호를 출력하는 구성으로 되어 있다. 또한, 이 1변에서 밀봉재(104)가 형성되는 근방의 영역(150a)에는, 화상 신호선이나 샘플링 회로 등을 형성하여도 좋다. 한편, 이 1변의 외주 부분에는, 복수의 실장 단자(107)가 형성되어, 외부 회로(도시 생략)로부터 각종 신호를 입력하는 구성으로 되어 있다.

또한, 이 1변에 인접하는 2변의 영역(130a)에는, 각각 주사선 구동 회로가 형성되어, 주사선을 양측에서 구동하는 구성으로 되어 있다. 또, 주사선에 공급되는 주사 신호의 지연이 문제로 되지 않는 것이면, 주사선 구동 회로를 한 쪽 1개만으로 형성하는 구성이라도 좋다.

그리고, 나머지의 1변의 영역(160a)에는, 후술하는 프리차지 회로가 형성되고, 또한 그 외측에는, 2개의 주사선 구동 회로에서 공용되는 배선 등을 형성하여도 좋다.

한편, 대향 기판(102)에 마련되는 대향 전극(108)은 소자 기판(101)과의 접합 부분에 있어서의 4모서리 중 적어도 1개소에서 도통재에 의해, 소자 기판(101)과 전기적으로 접속되는 구성으로 되어 있다.

그 밖에, 대향 기판(102)에는, 특히 도시하지 않지만, 화소 전극(118)과 대향하는 영역에, 필요에 따라서 착색층(컬러 필터)이 마련된다. 단, 후술하는 복판(腹板)식의 프로젝터와 같이 색광 변조의 용도에 적용

하는 경우에는, 대향 기판(102)에 착색층을 형성할 필요는 없다.

또, 종래, 대향 기판(102)에 있어서는, 착색층을 마련하는지 여부에 관계없이, 광의 리크에 의한 계조비의 저하를 방지하기 위해서, 화소 전극(118)과 대향하는 영역 이외의 부분에 차광막이 마련되어 있었지만, 본 실시예에서는, 후술하는 바와 같이, 소자 기판(101) 측에서 화소부에서의 차광 영역이 규정되기 때문에, 대향 기판(102)에 마련되고 있던 차광막이 생략되어 있다.

또한, 소자 기판(101) 및 대향 기판(102)의 대향면에는, 후술하는 바와 같이, 액정(105)에 있어서의 분자의 장축 방향이 양 기판 사이에서 약 90도 연속적으로 비틀어지도록 러빙 처리된 배향막(도 1에서는 생략)이 마련되는 한편, 그 각 배면 측에는 배향 방향에 따른 편광자(도시 생략)가 각각 마련된다. 또, 도 1의 (b)에 있어서는, 대향 전극(108)이나, 화소 전극(118), 실장 단자(107) 등에는 두께를 갖게 하고 있지만, 이것은 형성 위치를 나타내기 위한 편의적인 조치이며, 실제로는, 기판에 대하여 충분히 무시할 수 있을 정도로 얇다.

(전기적인 구성)

다음에, 상술한 액정 패널(100) 중 소자 기판(101)의 전기적인 구성에 대하여 설명한다. 도 2는 이 구성을 나타내는 개략도이다.

이 도면에 나타내는 바와 같이, 소자 기판(101)에는, 외부 회로로부터의 각종 신호를 입력하기 위해서 복수의 실장 단자(107)가 마련되고 있다. 이들의 실장 단자(107)를 거쳐서 입력되는 신호는 각종 배선을 거쳐서 각부에 공급되는 구성으로 되어 있다. 그러므로, 이들의 신호에 대하여 간단히 설명하기로 한다.

첫째, VID1 내지 VID6은, 도 4에 나타내는 바와 같이, 도트 클럭 DCLK에 동기하여 공급되는 1계통의 화상 신호 VID를, 6계통으로 분배함과 동시에 시간축으로 6배 신장한 것으로, 6개의 화상 신호선(122)을 거쳐서 샘플링 회로(150)에 공급된다.

또, 이 화상 신호 VID1~VID6은, 외부 회로에 의해서, 적절하게 극성 반전된다. 여기서, 본 실시예에 있어서의 극성 반전이란, 대향 전극(108)에 인가되는 전압 LCcom을 기준으로 하여, 교대로 정극성과 부극성으로 전압 레벨을 반전시키는 것을 말하지만, 극성을 반전하는지 여부에 대해서는, 일반적으로는, 데이터선으로의 화상 신호의 인가 방식이 ① 주사선 단위의 극성 반전인지, ② 데이터선 단위의 극성 반전인지, ③ 화소 단위의 극성 반전인지, ④ 프레임 단위의 극성 반전인지에 따라 정해지고, 그 반전 주기는 1수평 주사 기간, 도트 클럭 DCLK 또는 1수직 주사 기간의 주기로 설정된다. 단, 본 실시예에서는, 설명의 편의상, ① 주사선 단위의 극성 반전인 경우를 예로 들어 설명하지만, 본 발명을 이것에 한정시키는 것은 아니다.

둘째, VssY 및 VssX는 각각 주사선 구동 회로(130) 및 데이터선 구동 회로(140)에 있어서의 전원의 저위측 전압(접지 전위)이다. 또한, VddY 및 VddX는 각각 주사선 구동 회로(130) 및 데이터선 구동 회로(140)에 있어서의 전원의 고위측 전압이다. 이들 중 전원의 저위측 전압 VssY는 후술하는 축적 용량 소자의 접지 전위로 되어 있기 때문에, 용량선(175)을 거쳐서 각 화소에도 공급되어 있다.

셋째, LCcom은 대향 전극(108)에 인가되는 전압 신호이다. 이 때문에, 전압 신호 LCcom이 공급되는 2개의 전극(109)은 대향 기판(102)과 접합할 때에 이용되는 밀봉재(104)(도 1참조)의 모서리에 상당하는 지점에 각각 마련되고 있다. 따라서, 소자 기판(101)이 실제로 대향 기판(102)에 접합되면, 전극(109)과 대향 전극(108)이 도통재를 거쳐서 접속되어, 대향 전극(108)에 전압 신호 LCcom이 인가되는 구성으로 된다. 또, 전압 신호 LCcom은 시간축에 대하여 일정한 전압이며, 외부 회로가, 이 전압 신호 LCcom을 기준으로 하여, 화상 신호 VID1~VID6을, 1수평 주사 기간마다 고위측 및 저위측으로 나누어, 교류 구동하는 구성으로 되어 있다. 또한, 전극(109)이 마련되는 지점은 본 실시예에 있어서는 2개소이지만, 이 전극(109)이 마련되는 이유는 도통재를 거쳐서 대향 전극(108)에 전압 신호 LCcom을 인가하기 위함이므로, 전극(109)이 마련되는 지점은 적어도 1개소이면 충분하다. 이 때문에, 전극(109)이 마련되는 지점은 1개소여도 좋고, 3개소 이상이어도 좋다.

넷째, DY는, 도 4에 나타내는 바와 같이, 1수직 유효 주사 기간의 최초에 공급되는 전송 개시 펄스이며, CLY는 주사선 구동 회로(130)에서 이용되는 클럭 신호이다. 또, CLYinv는 클럭 신호 CLY를 레벨 반전시킨 반전 클럭 신호이다.

다섯째, DX는, 도 4에 나타내는 바와 같이, 1수평 유효 주사 기간의 최초에 공급되는 전송 개시 펄스이며, CLX는 데이터선 구동 회로(140)에 있어서 이용되는 클럭 신호이다. 또, CLXinv는 클럭 신호 CLX를 레벨 반전시킨 반전 클럭 신호이다. 또한, ENB1 및 ENB2는, 후술하는 바와 같이, 데이터선 구동 회로(140)에서의 시프트 레지스터의 각 출력 신호를, 소정의 펄스 폭으로 제한하기 위해서 이용되는 인에이블 신호이다. 또한, NRG는 프리차지 제어 신호이며, NRS는 프리차지 전압 신호이지만, 상세에 대해서는 후술하는 것으로 한다.

그런데, 소자 기판(101)의 표시 영역(100a)에 있어서는, 복수개의 주사선(112)이 행(Y)방향을 따라 평행하게 배열되고, 또한 복수개의 데이터선(114)이 열(X)방향을 따라 평행하게 배열되어, 이들의 각 교차 부분에 대응하여 화소가 마련되고 있다.

상세하게는, 도 3에 나타내는 바와 같이, 주사선(112)과 데이터선(114)이 교차하는 부분에 있어서는, 화소를 제어하기 위한 스위칭 소자인 TFT(116)의 게이트가 주사선(112)에 접속되는 한편, TFT(116)의 소스가 데이터선(114)에 접속됨과 동시에, TFT(116)의 드레인이 직사각형 형상의 투명한 화소 전극(118)에 접속되어 있다.

상술한 바와 같이, 액정 패널(100)에서는, 소자 기판(101)과 대향 기판(102)과의 전극 형성면 사이에 액정(105)이 유지되어 있기 때문에, 각 화소의 액정 용량은 화소 전극(118)과, 대향 전극(108)과, 이들 양 전극 사이에 유지된 액정(105)에 의하여 구성되게 된다. 여기서, 설명의 편의상, 주사선(112)의 총 개수를 「m」이라고 하고, 데이터선(114)의 총 개수를 「6n」이라고 하면(m, n은 각각 정수), 화소는 주사선을 「m」이라고 하고, 데이터선(114)의 총 개수를 「6n」이라고 하면(m, n은 각각 정수), 화소는 주사선

(112)과 데이터선(114)의 각 교차 부분에 대응하여, m행×6n열의 매트릭스 형상으로 배열되게 된다.

또한, 표시 영역(100a)에는, 이외에, 액정 용량의 리크를 방지하기 위한 축적 용량 소자(119)가, 화소마다 마련되고 있다. 이 축적 용량 소자(119)의 일단은 화소 전극(118)(TFT(116)의 드레인)에 접속되는 한편, 그 타단은 용량선(175)에 의해 공통 접속되어 있다. 이 때문에, 축적 용량 소자(119)는 액정 용량 소자와는 전기적으로 병렬로 되기 때문에, 액정 용량 소자의 유지 특성이 개선되어, 고계조비의 표시를 도모할 수 있게 된다. 또, 용량선(175)에는, 본 실시예에서는, 전원의 저위측 전압 VssV가 인가되는 구성이지만, 여기에는, 시간적으로 일정한 전압이 인가되면 좋기 때문에, 전원의 고위측 전압 VddV나, 전압 LCcom 등이 인가되는 구성이어도 좋다. 또한, 축적 용량 소자(119)를 포함한 화소의 상세 구성에 대해서는, 더욱 후술하는 것으로 한다.

그래서, 설명을 다시 도 2에 되돌리면, 주사선 구동 회로(130)는 수평 주사 기간 1H마다 순차적으로 액티브 레벨로 되는 주사 신호 G1, G2, …, Gm을, 1수직 유효 표시 기간 내에 각 주사선(112)에 출력하는 것이다. 상세한 구성에 대해서는 본 발명과 직접 관련되지 않으므로 도시를 생략하지만, 시프트 레지스터와 복수의 논리곱 회로(또는 부정 논리곱 회로)로 구성된다. 이 중, 시프트 레지스터는, 도 4에 나타내는 바와 같이, 1수직 유효 주사 기간의 최초에 공급되는 전송 개시 펄스 DY를, 클럭 신호 CLY(및 반전 클럭 신호 CLYinv)의 레벨이 천이할 때마다(상승 및 하강의 쌍방으로), 순차 시프트하여, 신호 G1', G2', G3', …, Gm'로서 출력하고, 각 논리곱 회로는 신호 G1', G2', G3', …, Gm' 중 서로 인접하는 신호끼리의 논리곱 신호를 구하여, 주사 신호 G1, G2, G3, …, Gm으로서 출력하는 것이다.

또한, 데이터선 구동 회로(140)는 순차적으로 액티브 레벨로 되는 샘플링 신호 S1, S2, …, Sn을 1수평 유효 주사 기간 내에 출력하는 것이다. 이 상세한 구성에 대해서도 본 발명과 직접 관련되지 않기 때문에 도시를 생략하지만, 시프트 레지스터와 복수의 논리곱 회로로 구성되어 있다. 이 중, 시프트 레지스터는, 도 4에 나타내는 바와 같이, 1수평 유효 주사 기간의 최초에 공급되는 전송 개시 펄스 DX를, 클럭 신호 CLX(및 반전 클럭 신호 CLXinv)의 레벨이 천이할 때마다 순차 시프트하여, 신호 S1', S2', S3', …, Sn'로서 출력하고, 각 논리곱 회로는 신호 S1', S2', S3', …, Sn'의 펄스 폭을, 인에이블 신호 ENB1 또는 ENB2를 이용하여, 서로 인접하는 것끼리 서로 중복하지 않도록, 기간 SMPa로 좁혀 샘플링 신호 S1, S2, S3, …, Sn으로서 출력하는 것이다.

계속해서, 샘플링 회로(150)는 데이터선(114)마다 마련되는 샘플링 스위치(151)로 구성되어 있다. 한편, 데이터선(114)은 6개마다 블럭화되어 있고, 도 2에 있어서, 왼쪽부터 세어 j(j는 1, 2, …, n)번째의 블럭에 속하는 데이터선(114)의 6개 중 가장 왼쪽에 위치하는 데이터선(114)의 일단에 접속되는 샘플링 스위치(151)는 화상 신호선(122)을 거쳐서 공급되는 화상 신호 VID1을, 샘플링 신호 Sj가 액티브로 되는 기간에서 샘플링하여, 해당 데이터선(114)에 공급하는 구성으로 되어 있다. 또한, 마찬가지로 i 번째의 블럭에 속하는 데이터선(114)의 6개 중 2번째에 위치하는 데이터선(114)의 일단에 접속되는 샘플링 스위치(151)는 화상 신호선(122)을 거쳐서 공급되는 화상 신호 VID2를, 샘플링 신호 Sj가 액티브로 되는 기간에서 샘플링하여, 해당 데이터선(114)에 공급하는 구성으로 되어 있다.

이하 마찬가지로, j번째의 블럭에 속하는 데이터선(114)의 6개 중 3, 4, 5, 6번째에 위치하는 데이터선(114)의 일단에 접속되는 샘플링 스위치(151)의 각각은 화상 신호선(122)을 거쳐서 공급되는 화상 신호 VID3, VID4, VID5, VID6의 각각을, 샘플링 신호 Sj가 액티브로 되는 기간에서 샘플링하여, 대응하는 데이터선(114)에 공급하는 구성으로 되어 있다. 즉, 샘플링 신호 Sj가 액티브 레벨로 되면, i 번째의 블럭에 속하는 6개의 데이터선(114)의 각각에는, 각각 화상 신호 VID1~VID6가 동시에 샘플링되는 구성으로 되어 있다.

한편, 표시 영역(100a)을 사이에 두어, 데이터선 구동 회로(140)와 반대측의 영역에는, 프리차지 회로(160)가 구비된다. 이 프리차지 회로(160)는 데이터선(114)마다 마련된 프리차징 스위치(161)로 이루어지고, 각 프리차징 스위치(161)는 프리차지 제어선(163)을 거쳐서 공급되는 프리차지 제어 신호 NRG가 액티브 레벨로 된 경우에, 프리차지 신호선(165)을 거쳐서 공급되는 프리차지 전압 신호 NRS를, 대응하는 데이터선(114)에 프리차지하는 구성으로 되어 있다.

여기서, 프리차지 제어 신호 NRG는, 도 5에 나타내는 바와 같이, 1수평 귀선 기간 중, 그 시간적인 전후단에서 격절(隔絶)된 기간에 있어서 액티브 레벨로 되는 신호이다. 또한, 프리차지 전압 신호 NRS는, 동 도면에 나타내는 바와 같이, 1수평 주사 기간 1H마다, 전압 LCcom을 기준으로 하여 전압 Vg+, Vg-로 레벨 반전하는 신호이다.

한편, 전압 LCcom은, 상술한 바와 같이, 대향 전극(108)에 인가되는 시간적으로 일정한 전압으로서, 화상 신호 VID1~VID6의 진폭 중심 전압이다. 또한, 전압 Vg+, Vg-는 전압 LCcom에 대한 차 전압의 실효값이 서로 동일하게 되는(절대값이 같음) 전압으로서, 각각 전압 LCcom보다도 고위측 전압, 저위측 전압이다. 여기서, 본 실시예가 전압 비인가 상태로 백색 표시를 행하는 노 매리 화이트 모드인 경우에, 정극측, 부극측에서 흑색 표시하기 위해서 화소 전극(118)에 인가해야 할 전압을 Vb+, Vb-라고 하면, 전압 Vg+는 전압 Vb+와 전압 LCcom의 중간 전압으로 설정되고, 또한, 전압 Vg-는 전압 Vb-과 전압 LCcom과의 중간 전압으로 설정된다.

즉, 전압 Vg+, 전압 Vb-는 각각 정극측, 부극측의 기입에 있어서의 중간(회색) 전압에 상당하는 것이다.

이러한 구성에 의한 프리차지 회로(160)에 따르면, 샘플링 신호 S1, S2, S3, …, Sn이 공급되는 1수평 유효 표시 기간보다도 앞의 1수평 귀선 기간에 있어서, 각 데이터선(114)이, 전압 Vg+ 또는 Vg-로, 미리 프리차지되기 때문에, 그 직후의 1수평 유효 표시 기간에 있어서, 화상 신호 VID1~VID6이 데이터선(114)에 샘플링될 때의 부하가 저감되는 것으로 된다.

또, 이들의 주사선 구동 회로(130)나, 데이터선 구동 회로(140), 샘플링 회로(150), 프리차지 회로(160) 등은, 제조 후에 결함의 유무를 판별하기 위한 검사 회로와 동시에, 표시 영역(100a)의 주변에 형성되기 때문에, 주변 회로로서 호칭되는 것이다. 단, 검사 회로에 대해서는, 본 건과는 직접 관계하지 않기 때문에, 그 설명에 대해서는 생략하는 것으로 한다.

(전기 광학 장치의 동작)

다음에, 상술한 구성에 따른 전기 광학 장치의 동작에 대하여 설명한다. 여기서 우선, 주사 신호 G1이 액티브 레벨로 되는 1수평 주사 기간 1H에 대하여 착안한다. 또, 이 1수평 주사 기간에서는, 설명의 편의상, 정극측의 기입을 실행하는 것으로 하면, 화상 신호 V1D1~V1D6은 대향 전극(108)에 인가되는 전압 LCcom에 대하여 고위측 전압으로 된다.

또한 이에 앞서, 프리차지 제어 신호 NRG가, 도 5에 나타내는 바와 같이, 그 귀선 기간의 전후 단에서의 격절된 기간에서 액티브 레벨로 된다. 이 때, 프리차지 전압 신호 NRS는 정극측의 기입에 대응하여 전압 Vg+로 된다. 이 때문에, 해당 기간에 있어서, 모든 데이터선(114)이 전압 Vg+에 프리차지되는 것으로 된다.

다음에, 1수평 귀선 기간이 종료하여, 1수평 유효 표시 기간으로 되면, 그 최초에 전송 개시 펄스 DX가, 도 4 또는 도 5에 나타내는 바와 같이, 데이터선 구동 회로(140)에 공급된다. 이 전송 개시 펄스 DX는 클럭 신호 CLX의 레벨이 천이할 때마다 순차 시프트된 신호 S1', S2', S3', …, Sn'로서 출력된다. 그리고, 이 신호 S1', S2', S3', …, Sn'의 각 펄스 폭이, 서로 인접하는 것끼리가 서로 중복하지 않도록 기간 SMPa로 좁혀지고, 샘플링 신호 S1, S2, S3, …, Sn으로서 출력된다.

한편, 1계통의 화상 신호 V1D는 외부 회로에 의해서, 도 4에 나타내는 바와 같이, 화상 신호 V1D1~V1D6에 분배됨과 동시에, 시간축에 대하여 6배로 신장되어, 액정 패널(100)에 공급된다.

여기서, 주사 신호 G1이 액티브 레벨로 되는 기간에 있어서, 샘플링 신호 S1이 액티브 레벨로 되면, 도 2에서 위로부터 세어 1개째의 TFT(116)가 전부 온 상태로 됨과 동시에, 왼쪽으로부터 1번째의 블럭에 속하는 6개의 데이터선(114)에, 각각 화상 신호 V1D1~V1D6이 샘플링된다. 그리고, 샘플링된 화상 신호 V1D1~V1D6은 해당 1개째의 주사선(112)과 해당 6개의 데이터선(114)과 교차하는 화소의 TFT(116)에 의해서, 각각 대응하는 화소 전극(118)에 인가되는 것으로 된다.

이 후, 샘플링 신호 S2가 액티브 레벨로 되면, 이번은 2번째의 블럭에 속하는 6개의 데이터선(114)에, 각각 화상 신호 V1D1~V1D6이 샘플링되고, 이들의 화상 신호 V1D1~V1D6이, 해당 1개째의 주사선(112)과 해당 6개의 데이터선(114)과 교차하는 화소의 TFT(116)에 의해서, 각각 대응하는 화소 전극(118)에 인가되는 것으로 된다.

이하 마찬가지로 해서, 샘플링 신호 S3, S4, ……, Sn이 순차적으로 액티브 레벨로 되면, 제 3 번째, 제 4 번째, …, 제 n 번째의 블럭에 속하는 6개의 데이터선(114)에 각각 화상 신호 V1D1~V1D6이 샘플링되고, 이들의 화상 신호 V1D1~V1D6이 해당 1개째의 주사선(112)과 해당 6개의 데이터선(114)과 교차하는 화소의 TFT(116)에 의해서, 각각 대응하는 화소 전극(118)에 인가되는 것으로 된다. 이것에 의해, 제 1 행 째의 화소 전부에 대한 기입이 완료되게 된다.

계속해서, 주사 신호 G2가 액티브로 되는 기간에 대하여 설명한다. 본 실시예에서는, 상술한 바와 같이, 주사선 단위의 극성 반전이 행해지기 때문에, 이 1수평 주사 기간에 있어서는, 부극측의 기입이 행해지게 된다. 이 때문에, 화상 신호 V1D1~V1D6은 대향 전극(108)에 인가되는 전압 LCcom에 대하여 저위측 전압으로 된다. 이것에 앞서, 귀선 기간에 있어서의 프리차지 전압 신호 NRS의 전압은 Vg-로 되기 때문에, 프리차지 제어 신호 NRG가 액티브 레벨로 된 경우에, 모든 데이터선(114)은 전압 Vg-에 프리차지되는 것으로 된다.

다른 동작에 대해서는 마찬가지이며, 샘플링 신호 S1, S2, S3, …, Sn이 순차적으로 액티브 레벨로 되어, 제 2 행 째 화소의 전부에 대한 기입이 완료되게 된다.

이하 마찬가지로 해서, 주사 신호 G3, G4, …, Gm이 액티브로 되어, 제 3 행 째, 제 4 행 째, …, 제 m 행 째의 화소에 대하여 기입이 행해지는 것으로 된다. 이것에 의해, 기수행 째의 화소에 대해서는 정극측의 기입이 행해지는 한편, 우수행 째의 화소에 대해서는 부극측의 기입이 행하여져, 이 1수직 주사 기간에 있어서는, 제 1 행 째 내지 제 m 행 째의 화소의 전부에 걸친 기입이 완료되게 된다.

그리고, 다음 1수직 주사 기간에 있어서도, 마찬가지의 기입이 행하여지지만, 이 때, 각 행의 화소에 대한 기입 극성이 교체된다. 즉, 다음 1수직 주사 기간에 있어서, 기수행 째의 화소에 대해서는 부극측의 화소에 대하여 기입이 행해지는 한편, 우수행 째의 화소에 대해서는 정극측의 기입이 행해지게 된다.

이와 같이, 1수직 주사 기간마다 화소에 대한 기입 극성이 교체되므로, 액정(105)에 직류 성분이 인가되는 일이 없게 되어, 그 열화가 방지되고 있다.

또한, 이러한 구동에서는, 데이터선(114)을 1개마다 구동하는 방식과 비교하면, 각 샘플링 스위치(151)에 의해서 화상 신호를 샘플링하는 시간이 6배로 되기 때문에, 각 화소에 있어서의 기입 시간이 충분히 확보된다. 이 때문에, 고계조비가 얻어지게 된다. 또한, 데이터선 구동 회로(140)에 있어서의 시프트 레지스터의 단수 및 클럭 신호 CLX의 주파수가 각각 1/6으로 저감되기 때문에, 단수의 저감화와 더불어 저소비 전력화도 도모되게 된다.

또한, 샘플링 신호 S1, S2, …, Sn의 액티브 기간은 클럭 신호 CLX의 반주기보다도 좁혀져, 기간 SMPa로 제한되어 있기 때문에, 인접하는 샘플링 신호끼리의 오버랩이 사전에 방지된다. 이 때문에, 어떤 블럭에 속하는 6개의 데이터선(114)에 샘플링되어야 되는 화상 신호 V1D1~V1D6이 이것에 인접하는 블럭에 속하는 6개의 데이터선(114)에도 동시 샘플링되는 사태가 방지되어, 고품질의 표시가 가능해져 있다.

(화소의 상세 구성)

다음에, 화소의 상세에 대하여 도 6및 도 7을 참조하여 설명한다. 도 6은 화소부의 상세 구성을 나타내는 평면도이며, 도 7의 (a)는 도 6에 있어서의 B-B' 선의 단면도이다. 또, 도 6에 있어서, 최상 도전층

으로 되는 화소 전극(118)에 대해서는, 설명의 이해를 위해, 그 윤곽만을 파선으로 나타내기로 한다.

우선, 도 7의 (a)에 나타내는 바와 같이, 소자 기판(101)의 기재인 기판(10)에는, 하지 절연막(40)을 거쳐서 폴리실리콘으로 이루어지는 반도체층(30)이 마련되고, 그 표면은 열 산화에 의한 절연막(32)으로 덮여 있다.

한편, 도 6에 나타내는 바와 같이, 데이터선(114)은 Y 방향으로 연장하고, 주사선(112)은 X 방향으로 연장하고 있다. 또한, 용량선(175)은 주사선(112)과 근접하여 평행하게 마련되고 있지만, 데이터선(114)과 교차하는 부분에서는, 데이터선(114)과 겹치도록, 전단측(도 6에 있어서 상측)으로 돌출하여 형성되어 있다.

여기서, 반도체층(30)은 데이터선(114) 및 용량선(175)이 교차하는 부분으로부터, 용량선(175)의 연장 방향(도 6에 있어서 오른쪽 방향), 데이터선(114)의 하층에 있어서의 용량선(175)의 돌출 방향(동 도의 위쪽 방향) 및 그 반대 방향(동 도의 아래쪽 방향)의 총 3방향으로 연장되어 대략 T자 형상으로, 또한 이들의 배선으로 덮어지도록 형성되어 있다.

또한, 반도체층(30) 중 주사선(112)과 겹치는 부분이 채널 영역(30a)으로 되어 있다. 바꾸어 말하면, 주사선(112) 중 반도체층(30)과 교차하는 부분이 게이트 전극(1166)으로서 이용되고 있다. 또, 게이트 전극(1166)을 포함하는 주사선(112) 및 용량선(175)은, 후술하는 바와 같이, 예컨대 폴리실리콘 등으로 형성되어 있다.

또한, 반도체층(30)에 있어서, 채널 영역(30a)의 소스 측에는, 저농도(lightly doped) 소스 영역(30b), 고농도(heavily doped) 소스 영역(116S)이 마련되는 한편, 드레인 측에는, 저농도 드레인 영역(30c), 고농도 드레인 영역(116D)이 마련되어, 소위 LDD(Lightly Doped Drain) 구조로 되어 있다.

이 중, 고농도 소스 영역(116S)은 절연막(32), 제 1 층간 절연막(41) 및 제 2 층간 절연막(42)을 개구하는 콘택트 홀(52)에 의해서, 알루미늄 등으로 이루어지는 데이터선(114)에 접속되어 있다.

한편, 고농도 드레인 영역(116D)은 절연막(32) 및 제 1 층간 절연막(41)을 개구하는 콘택트 홀(51)에 의해서, 고융점 금속이나 폴리실리콘 등으로 이루어지는 중간 도전막(181)의 일단에 접속되어 있다. 한편, 이 중간 도전막(181)의 타단은 제 2 층간 절연막(42) 및 제 3 층간 절연막(43)을 개구하는 콘택트 홀(53)에 의해서, 화소 전극(118)에 접속되어 있다. 즉, 화소 전극(118)은 중간 도전막(181)을 거쳐서, TFT(116)의 고농도 드레인 영역(116D)에 접속되어 있다.

여기서, 화소 전극(118)을 고농도 드레인 영역(116D)에 직접적으로 접속하지 않고서, 중간 도전막(181)을 거쳐서 간접적으로 접속하는 구성으로 한 것은 다음과 같은 이유에 의한다. 즉, 화소 전극(118)은 액정 용량 소자에 전압을 인가하기 위한 전극이기 때문에, 액정(105)에 가까운 부분에 형성되고, 반대로 반도체층(30)은 먼 부분에 형성된다. 또한, 반도체층(30)과 화소 전극(118) 사이에는, 본 실시예와 같이 TFT(116)가 플레너형이면, 주사선(112)이나 데이터선(114) 등의 배선층이 용간 절연막을 거쳐서 적층되기 때문에, 반도체층(30)과 화소 전극(118)의 거리는 필연적으로 커진다. 이 때문에, 화소 전극(118)을 고농도 드레인 영역(116D)에 직접적으로 접속하는 구성에서는, 비교적 깊이가 있는 콘택트 홀을, 예컨대 건식 에칭에 의해 형성해야 한다. 단, 이러한 깊이가 있는 콘택트 홀을 형성할 때에, 지나치게 에칭하면, 반도체층(30)을 돌파한다는 불량이 발생한다. 특히, 반도체층(30)과 절연막과의 선택 비에 대차가 없고, 그 위에, 반도체층(30)의 막두께가 에칭해야 할 절연막의 두께에 비하여 지극히 얇다고 하는 사정은 이러한 콘택트 홀을 마련하는 것을 더욱 곤란하게 하고 있다.

그래서, 첫째, 고농도 드레인 영역(116D)의 대응 위치에 콘택트 홀(51)을 마련하여, 절연막(32) 및 제 1 층간 절연막(41)을 개구하고, 둘째, 이 콘택트 홀(51)을 거쳐서 전기적으로 접속되는 중간 도전막(181)을 형성하여, 이 중간 도전막(181)을 고농도 드레인 영역(116D)의 배리어막으로서 기능시키고 있는 것이다. 이것에 의해, 화소 전극(118) 형성 전에 콘택트 홀(53)를 개구할 때에, 중간 도전막(181)을 에칭 스토퍼로서 이용하는 것에 따라, 과잉 에칭에 의한 반도체층(30)의 돌파를 방지하고 있는 것이다.

그런데, 이 중간 도전막(181)은, 특히 도 6에 나타내는 바와 같이, 인접하는 데이터선(114)의 사이에서 용량선(175)을 거의 덮음과 동시에, 그 일부가 주사선(112)에 걸려 있다(단지, 전기적으로는 절연되어 있음). 또한, 화소 전극(118)이 형성되지 않는 영역은 Y 방향에서는 데이터선(114)으로 덮여지고, X 방향에서는 주사선(112) 및 중간 도전막(181)으로 덮여지고 있다. 여기서 중간 도전층(181)으로는 폴리실리콘이라도 좋고, Ti(티탄), Cr(크롬), W(텅스텐), Ta(탄탈), Mo(몰리브덴) 또는 Pb(납)의 단체 혹은 이들의 합금, 금속 실리사이드라도 좋다. 따라서, 화소부에서의 차광 영역은 데이터선(114), 주사선(112) 및 중간 도전막(181)에 의해 완전히 규정되기 때문에, 대향 기판(102)에 별도로 마련되고 있었던 차광막을 생략하는 것이 가능해진다. 아울러, 반도체층(30)은 데이터선(114), 주사선(112), 용량선(175) 및 중간 도전막으로 덮여져 있기 때문에, 기판의 상측으로부터의 광이 TFT(116)로 침입하는 것이 방지되게 된다. 또한, 반도체층(30)의 하측에서, 기판(10) 및 하지 절연막(40) 사이에 차광막을 형성하여도 좋다. 이것에 의해, 기판의 하측으로부터의 광이 TFT(116)에 침입하는 것을 방지할 수 있기 때문에, 광 조사에 의한 TFT(116)의 특성 변화의 방지가 도모되고 있다.

다음에, 축적 용량 소자(119)의 상세 구성에 대하여, 도 6 및 도 7의 (a)에 더하여, 도 7의 (b) 및 동 도의 (c)를 참조하여 설명한다. 여기서, 도 7의 (b)는 도 6에 있어서의 C-C'선의 단면도이며, 도 7의 (c)는 축적 용량 소자(119)의 등가 회로를 도시하는 도면이다.

우선, 반도체층(30) 중 고농도 드레인 영역(116D)에 인접하는 영역(30f)은 고농도의 도핑에 의해 저저항화되고, 평면적으로는, 용량선(175)의 하층에 있어서 대략 L자형 형상으로 되어 있다. 한편, 중간 도전막(181)은 용량선(175)과는 제 1 층간 절연막(41)을 거쳐서, 또한 상술한 바와 같이, X 방향에서 용량선(175)을 덮도록 형성되어 있다. 따라서, 축적 용량 소자(119)는, 도 7의 (b) 또는 동 도의 (c)에 나타내는 바와 같이, 2개의 용량 소자를 병렬화한 것으로 된다. 상세하게는, 축적 용량 소자(119)는 영역(30f)을 한쪽의 전극으로 하고, 용량선(175)을 다른쪽의 전극으로 하며, 반도체층(30)의 표면에 형성된 절연막(32)을 유지하여 이루어지는 제 1 용량 소자와, 중간 도전막(181)을 한쪽의 전극으로 하고, 용량선

(175)를 다른쪽의 전극으로 하여, 제 1 층간 절연막(41)을 유지하여 이루어지는 제 2 용량 소자의 병렬 접속에 의해 구성되어 있다. 이 때문에, 축적 용량 소자(119)는 단일의 용량 소자로 이루어지는 경우와 비교하여 용량이 증가하기 때문에, 액정 용량 소자의 유지 특성이 개선되어, 표시의 고품질화가 도모되게 된다.

또, 최상층(즉, 액정(108)과 접하는 면)의 전면에는, 폴리이미드 등의 유기막으로 이루어진 배향막(61)이 형성되어, 대향 기판(102)과 접합하기 전에 러빙 처리가 실시된다.

(주변 회로의 상세 구성)

다음에, 주변 회로의 상세에 대하여, 샘플링 회로(150)의 일부 영역과, 주사선 구동 회로(130)의 일부 영역을 예로 들어 각각 설명한다. 또, 주변 회로를 구성하는 능동 소자나 배선은 후의 제조 프로세스에서 상술하는 바와 같이, 표시 영역에서의 TFT(116)나, 주사선(112)(및 용량선(175)), 층간 도전막(181), 데이터선(114)과 공통 프로세스로 형성된다.

이 중, 표시 영역(101a)에서, 배선은 주사선(112)(및 용량선(175)), 층간 도전막(181), 데이터선(114)의 순서로 형성되기 때문에, 이하의 설명에서는, 주변 회로에 있어서의 배선 중 주사선(112)을 구성하는 도전층과 동일층으로 이루어지는 배선을 제 1 층의 배선이라고 호칭하고, 또한, 층간 도전막(181)을 구성하는 도전층과 동일층으로 이루어지는 배선을 제 2 층의 배선이라고 호칭하며, 또한, 데이터선(114)을 구성하는 도전층과 동일층으로 이루어지는 배선을 제 3 층의 배선이라고 호칭하는 것으로 한다. 또, 층간 도전막(181)을 구성하는 도전층은 종래에는 주변 회로 영역에 이용되고 있지 않았기 때문에, 본 실시예에 있어서의 제 3 층의 배선은 종래의 전기 광학 장치에 있어서의 제 2 층의 배선에 상당하게 된다.

이와 같이, 주변 회로에 있어서, 제 1 층 내지 제 3 층까지의 3층 분의 배선을 이용하면, 주변 회로를 설계할 때의 자유도가, 2층 분의 배선밖에 이용하고 있지 않던 종래보다도, 각 단에 향상한다. 또한, 제 2 층의 배선을 다음에 기술하는 바와 같이, 이용하는 것에 따라, 배선 저항의 저감화나, 회로 형성 영역의 축소화를 도모하는 것이 가능해진다.

(샘플링 회로의 근방 영역)

그래서 우선, 샘플링 회로(150)의 일부 영역에 대하여, 도 8의 (a) 및 동 도의 (b)를 참조하고 설명한다. 또, 여기서는, 왼쪽부터 j번째의 블럭에 대응하여 출력되는 샘플링 신호 SJ와, 6개의 화상 신호선(122)으로부터 해당 블럭에 속하는 6개의 데이터선(114)에 이르기까지의 경로와의 관계를 중심으로 하여 설명하는 것으로 한다. 또, j는, 도 2의 설명과 마찬가지로, 블럭을 일반화하여 설명하기 위한 것으로서, 본 실시예에서는 「1」부터 「n」 중 어느 것인가 하나의 정수이다.

도 8의 (a)는 이 영역의 상세 구성을 나타내는 평면도이다. 우선, 데이터선 구동 회로(140)로부터 출력되는 샘플링 신호 SJ는 제 3 층의 배선(391), 하층의 배선(191), 제 3 층의 배선(393) 및 6개의 제 1 층의 배선(412)이라는 경로로 공급된다. 여기서, 각 배선끼리는, 콘택트 홀을 거쳐서 접속되고, 또한, 제 1 층의 배선(412)은, 그대로 샘플링 스위치(151)를 구성하는 TFT의 게이트 전극으로 되어 있다.

한편, 화상 신호 VID1~VID6 중 화상 신호 VID1은 다음과 같은 경로로 샘플링 스위치(151)에 공급되어 있다. 즉, 화상 신호 VID1은 제 3 층으로 이루어지는 화상 신호선(122), 하층의 배선(193), 제 3 층의 배선(395), 하층의 배선(195) 및 제 3 층의 배선(397)이라는 경로를 거쳐서, 샘플링 스위치(151)를 구성하는 TFT의 소스 영역에 공급되어 있다. 다른 화상 신호 VID2~VID6에 대해서도 마찬가지의 경로를 거쳐서, 샘플링 스위치(151)를 구성하는 TFT의 소스 영역에 공급되어 있다. 그리고, 각 샘플링 스위치(151)를 구성하는 TFT의 드레인 영역에는, 각각 제 3 층의 데이터선(114)이 접속되어 있다.

이와 같이 샘플링 회로(150)의 각종 배선에는 원칙으로서 제 3 층의 배선이 이용되지만, 이 제 3 층의 배선과 교차하는 부분 및 게이트 전극으로서 이용되는 부분에는 예외로서 하층의 배선이 이용되고 있다.

여기서, 도 8의 (a)에 있어서의 D-D'선의 단면 구조에 대하여, 도 8의 (b)를 참조하여 설명한다. 이 도면에 나타내는 바와 같이, 화상 신호 VID1이 공급되는 화상 신호선(122)으로부터 분기되어, 다른 화상 신호선(122)과는 하층에서 교차하는 배선(193)은 제 1 층의 배선(112b)과 제 2 층의 배선(181b)이 병렬 접속된 병렬 배선으로 되어 있다. 상세하게는, 배선(181b)은, 그 양단에 있어서, 제 1 층간 절연막(41)을 개구하는 콘택트 홀(55_1),(56_1)을 거쳐서 배선(112b)과 병렬 접속되어 있다. 또한, 화상 신호 VID1이 공급되는 화상 신호선(122)은 콘택트 홀(551)과 동일 위치에 마련된 콘택트 홀(55_2)을 거쳐서 배선(181b)과 접속되는 한편, 배선(395)은 콘택트 홀(56_1)과 동일 위치에 마련된 콘택트 홀(56_2)을 거쳐서 배선(181b)과 접속되어 있다.

또, 화상 신호 VID1 이외의 다른 화상 신호 VID2~VID6이 공급되는 화상 신호선(122)으로부터 분기되는 배선(193)에 대해서도, 마찬가지로 제 1 층의 배선(112b)과 제 2 층의 배선(181b)이 병렬 접속된 병렬 배선으로 되어 있다. 또한, 화상 신호선(122)으로부터 분기·교차하는 배선(193) 외에, 샘플링 신호 SJ가 공급되는 배선(393)과 교차하기 위한 배선(195)에 대해서도, 마찬가지로 제 1 층의 배선(112c)과 제 2 층의 배선(181c)이 병렬 접속된 병렬 배선으로 되어 있다.

여기서, 샘플링 회로(150)에 있어서, 배선(193),(195)에, 제 1 층의 배선과 제 2 층의 배선의 병렬 배선을 이용하고 있는 것은, 다음 이유에 의한다. 즉, 화상 신호 VID1~VID6은 화소 전극(118)에 최종적으로 인가되어 표시 상태를 직접적으로 규정하는 아날로그 신호이기 때문에, 그 공급 경로는 조금이라도 저 저항인 것이 바람직하다. 이 때문에, 화상 신호선(122)에 대해서는 알루미늄으로 이루어지는 제 3 층이 이용되지만, 여기에서 분기되는 배선에 대해서는, 일부라도 제 3 층 이외의 층을 이용하여야 하다. 이 때문에, 종래에는, 이 부분에는, 주사선(112)을 구성하는 도전층으로 이루어지는 배선 즉, 제 1 층의 배선이 이용되고 있었다. 그러나, 제 1 층은, 상술한 바와 같이, 폴리실리콘 등이기 때문에, 제 3 층을 구성

하는 알루미늄 등과 비교하여 훨씬 고저항이다. 이 때문에, 제 1 층의 배선 길이가 매우 짧아도, 그 저항분에 의한 영향은 무시할 수 없을 정도로 크다.

그래서, 본 실시예에서는, 화상 신호 VID1~VID6의 공급 경로 중 제 3 층 이외의 층으로 이루어지는 배선을 이용해야 하는 부분에는, 본래, 표시 영역에서 이용되고 있었던 제 2 층을 주변 회로 영역에서도 이용함과 동시에, 이 제 2 층으로 이루어지는 배선과, 제 1 층의 배선을 병렬 접속하고 있는 것이다. 이 때문에, 해당 부분의 저항값은 단일 층의 배선으로 이루어지는 경우와 비교하여, 대략 절반 정도까지 저감되게 된다. 따라서, 본 실시예에서는, 화상 신호 VID1~VID6은 공급 경로에 있어서의 파형 둔화나 전압 강하 등이 방지된 후에, 데이터선(114)에 공급되기 때문에, 양호한 표시가 가능해진다.

또, 화상 신호선(122)으로부터 분기되는 병렬 배선(193)은, 도 8의 (a)에 나타내는 바와 같이, 화상 신호 VID1~VID6의 각각에 걸쳐, 대략 동일 길이·대략 동일 폭으로 되어 있다. 이것은, 본 실시예에서는, 배선(193)이 제 1 층의 배선(112b)과 제 2 층의 배선(181b)의 병렬 접속으로부터 구성되어, 그 배선 저항이 저감되어 있지만, 제 3 층의 배선과 비교하면 여전히 크기 때문에, 배선(193)의 저항값이 화상 신호 VID1~VID6의 각각에 걸쳐 서로 같게 하기 위한 조치이다.

또한, 화상 신호 VID1~VID6의 공급 경로로부터 벗어나지만, 샘플링 신호 Sj를 화상 신호선(122)과 교차하기 위해서 공급하는 배선(191)에 대해서도, 마찬가지로 제 1 층의 배선과 제 2 층의 배선과의 병렬 접속으로 되어 있다. 이것은 샘플링 신호 Sj의 파형 둔화 등에 의한 지연 방지의 관점에서, 샘플링 신호 Sj의 공급 경로에 대해서도, 조금이라도 저 저항인 것이 요청되고 있기 때문이다.

이와 같이, 본 실시예에 있어서, 샘플링 회로(150)의 각종 배선에는, 원칙으로서 저 저항인 제 3 층의 배선이 이용되는 한편, 제 3 층의 배선과 교차해야 하는 부분에는, 제 1 층의 배선과 제 2 층의 배선의 병렬 배선이 이용되고 있다. 여기서, 주변 회로 전체로 보면, 이와 같이 병렬 배선을 이용해야 하는 부분은 샘플링 회로(150)에 있어서의 배선(191),(193),(195) 이외에도 다수 존재한다. 예컨대, 도 2에 있어서의 프리차지 제어선(163)은 각 프리차징 스위치(161)를 구성하는 TFT의 게이트 전극에 각각 분기해야 하지만, 분기 후, 프리차지 전압 신호선(165)과 교차해야 하는 부분이 존재한다. 또한, 용량선(175)은 표시 영역(100a) 내에서는 주사선(112)과 같은 제 1 층의 배선이지만, 그 이외의 영역에서는, 실장 단자(107)로부터 연장되어 공통 접속되는 것과의 관계상, 제 3 층의 배선으로 구성되어야 한다. 이러한 용량선(175)에 대하여, 프리차지 제어선(163), 프리차지 전압 신호선(165)은, 도 2에 나타내는 바와 같이, 교차해야 하는 부분이 존재한다. 또한, 주사선 구동 회로(130)에 있어서, 시프트 레지스터를 구성하는 단위 회로에는, 전원전압 VddY, VssY와 동시에, 클럭 신호 CLY 및 반전 클럭 신호 CLYinv를 공급해야 한다. 이 때문에, 클럭 신호 CLY 및 반전 클럭 신호 CLYinv의 기간 배선으로부터 분기되는 배선에 대해서는, 적어도 전원 전압 VddY, VssY가 공급되는 배선과 교차해야 하는 부분이 존재한다. 마찬가지로, 데이터선 구동 회로(140)에 있어서, 시프트 레지스터를 구성하는 단위 회로에는, 전원 전압 VddX, VssX와 함께, 클럭 신호 CLX 및 반전 클럭 신호 CLXinv를, 각 논리곱 회로에는, 전원 전압 VddX, VssX와 함께, 인에이블 신호 ENB1, ENB2를, 각각 공급해야 한다. 이 때문에, 클럭 신호 CLX 및 반전 클럭 신호 CLXinv의 기간 배선으로부터 분기되는 배선과, 인에이블 신호 ENB1, ENB2의 기간 배선으로부터 분기되는 배선에 대해서는, 각각 적어도 전원 전압 VddY, VssY가 공급되는 배선과 교차해야 하는 부분이 존재한다. 그리고, 이와 같이 제 3 층의 배선과 교차해야 하는 부분에, 제 1 층의 배선과 제 2 층의 배선을 병렬 접속한 병렬 배선을 이용함으로써, 해당 부분의 저저항화를 도모하는 것이 가능해진다.

(주사선 구동 회로의 일부 영역)

계속해서, 주사선 구동 회로(130)의 일부 영역에 대하여 도 9의 (a) 및 동 도의 (b)를 참조하여 설명한다. 여기서, 도 9의 (a)는 주사선 구동 회로(130)의 일부 영역의 구성을 나타내는 평면도이며, 동 도의 (b)는 그 등가 회로를 도시하는 도면이다. 또, 도면에 나타내어지는 영역은 주사선 구동 회로(130)를 구성하는 시프트 레지스터 중 전송 개시 펄스 DY를 클럭 신호 CLY 및 반전 클럭 신호 CLYinv에 따라서 전송하기 위한 회로를 부분적으로 뽑아 낸 것이다.

도 9의 (a)에 나타내는 바와 같이, 주사선 구동 회로(130)에는, 제 1 층, 제 2 층, 제 3 층의 배선이 이용되고 있다. 그리고, 이 영역에서도, 원칙으로서 제 3 층의 배선이 이용되고 있지만, 예외로서, 제 3 층의 배선과 교차하는 부분 및 게이트 전극으로서 이용되는 부분에는, 제 1 층의 배선이 이용되고, 또한 한쪽 TFT의 소스 전극으로부터 다른쪽의 TFT의 드레인 전극에 이르는 배선의 일부에는, 제 2 층의 배선(181d)이 이용되고 있다. 특히, 영역(132)에서는, 제 1 층의 배선(112d), 제 2 층의 배선(181d) 및 제 3 층의 배선(114d)이 서로 층간 절연막(여기서는 도시 생략)을 거쳐 적층되어 형성되고 있다.

여기서, 주사선 구동 회로(130)에 있어서, 상술한 샘플링 회로(150)와는 달리, 제 2 층의 배선(181d)을 단독으로 이용함과 동시에, 3층의 배선을 동일 영역에 형성하는 것은 다음 이유에 의한다. 즉, 데이터선 구동 회로(130)는 샘플링 신호 S1, S2, …, Sn을, 각각 6개의 데이터선(114)마다 공급하기 때문에, 데이터선 구동 회로(130)를 구성하는 시프트 레지스터의 단위 회로나 논리곱 회로에 대해서는, 도 8의 (a)에 있어서의 데이터선 피치의 6배의 피치 내로 받아들이면 된다. 이것에 대하여, 주사선 구동 회로(130)는 주사 신호 G1, G2, …, Gm을 m개의 주사선(112)의 각각에 대하여 각각 공급해야 하기 때문에, 주사선 구동 회로(140)를 구성하는 시프트 레지스터의 단위 회로나 논리곱 회로에 대해서는, 도 9의 (a)에 있어서의 주사선 피치와 등배의 피치 내로 받아들여야 하다. 즉, 주사선 구동 회로(130)에서는, 그 단위 회로나 논리곱 회로를, 데이터선 구동 회로(140)와 비교하여, 보다 좁은 영역 내에서 형성해야 한다. 여기서 가령, 제 2 층의 배선(181d)을 이용하지 않고, 3개의 배선을, 제 1 층 및 제 3 층만으로 형성하는 경우, 하나의 배선을 제 1 층으로부터, 나머지 2개의 배선을 제 3 층으로부터, 각각 형성해야 하지만, 이 경우, 동일 영역에서, 제 3 층의 배선을 이중으로 겹쳐 형성하는 것은 불가능하다. 이 때문에, 다른 영역에서, 제 3 층의 배선을 나란하게 형성하는 수밖에 없기 때문에, 그만큼 폭이 넓은 영역을 필요로 하게 된다. 따라서, 이러한 구성에서는, 주사선 구동 회로(130)를 구성하는 단위 회로나 논리곱 회로를, 보다 좁은 영역 내에서 형성해야 한다고 하는 요청에 반(反)하게 된다. 이에 대하여, 본 실시예에서는, 제 2 층의 배선(181d)을 단독으로 이용하여, 동일한 영역(132)에서 제 1 층의 배선(112d), 제 2 층의 배선(181d) 및

제 3 층의 배선(114d)을, (층간 절연막을 거쳐서 절연을 도모한 후에) 서로 겹쳐 형성함으로써, 회로 형성에 필요한 영역의 폭을 작게 할 수 있게 된다.

또, 주사선 구동 회로(130)에 있어서는, 회로 형성에 필요한 영역의 폭이 좁은 것을 요구되지 않는 부분으로, 제 3 층의 배선과 교차해야 하는 부분에는, 제 1 층의 배선과 제 2 층의 배선의 병렬 배선을 이용하여도 좋은 것은 물론이다.

(제조 프로세스)

다음에, 본 실시예에 따른 전기 광학 장치의 제조 프로세스에 대하여, 소자 기판(101)의 표시 영역과 주변 회로 영역을 중심으로 하여 설명한다. 또, 여기 기재하는 주변 회로 영역으로는, 도 8의 (b)에 있어서, 어떤 1개의 화상 신호선(122)으로부터 분기되어, 다른 화상 신호선(122)과 교차하는 배선(193)의 근방 영역을 예시하는 것으로 한다.

우선, 도 10의 (a) 나타내는 바와 같이, 예컨대, 석영 기판이나, 유리 기판, 실리콘 기판 등의 기판(10)의 표면에, 하지 절연막(40)을 형성한다. 상세하게는, 하지 절연막(40)은, 예컨대 상압법(常壓法)이나 감압 CVD(Chemical Vapor Deposition)법 등에 의해, NSG(비도핑된 실리케이트 유리)나, PSG(인 실리케이트 유리), BSG(보론 실리케이트 유리), BPSG(보론 인 실리케이트 유리)등의 고절연성 유리 또는 산화 실리콘막, 질화 실리콘막 등으로부터, 약 50~1500㎚의 두께로, 바람직하게는 약 600~800㎚ 정도의 두께로 형성된다.

계속해서, 하지 절연막(40)의 상면 전체에, 예컨대 감압 CVD법 등에 의해서, 아몰퍼스 실리콘 층을 약 100㎚의 두께로 형성하여, 열처리 등에 의해 고체상 성장시킴으로써 폴리실리콘 층을 형성한다. 이 때, N 채널형의 TFT를 형성하는 경우에는, Sb(안티몬)나, As(비소), P(인) 등의 V족 원소의 불순물을, 단지 이온 주입 등에 의해 도핑하는 한편, P 채널형 TFT를 형성하는 경우에는, Al(알루미늄)이나, B(보론), Ga(갈륨) 등의 III족 원소의 불순물을, 마찬가지로, 단지 이온 주입 등에 의해 도핑한다. 그리고, 동 도의 (b)에 나타내는 바와 같이, 폴리실리콘 층을, 포토리소그래피나 에칭 등에 의해서 패터닝하여, 표시 영역에서의 TFT(116)의 반도체층(30)을 섬 형상으로 형성한다. 또, 이 때, 주변 회로 전체에 있어서는, 주사선 구동 회로(130)나, 데이터선 구동 회로(140), 샘플링 회로(150), 프리차지 회로(160)를 구성하는 TFT의 반도체층에 대해서도 마찬가지로 형성한다. 또한, TFT(116)의 반도체층(30) 중 용량선(175)이 형성되는 영역(30f)에 대해서는, P(인) 등의 불순물을 고농도로 도핑하여, 미리 저저항화를 도모하여 두어도 좋다.

또한, 도 10의 (c)에 나타내는 바와 같이, 반도체층(30)의 표면을 열 산화 처리하여, 게이트 절연막(32)을 해당 반도체층(30)의 표면에 형성한다. 이 공정에 의해, 반도체층(30)은 최종적으로 약 30~150㎚의 두께, 바람직하게는 약 35~45㎚의 두께로 되는 한편, 게이트 절연막(32)은 약 60~150㎚의 두께, 바람직하게는 약 30㎚의 두께로 된다.

다음에, 게이트 절연막(32) 및 하지 절연막(40)의 상면에, 폴리실리콘 층을 감압 CVD법 등에 의해 퇴적한다. 그리고, 도 11의 (d)에 나타내는 바와 같이, 이 폴리실리콘 층을 포토리소그래피나 에칭 등에 의해서 패터닝하고, 표시 영역에 있어서는 TFT(116)의 게이트 전극을 겸용하는 주사선(112)과, 축적 용량 소자(119)에 있어서 다른쪽의 전극을 이루는 용량선(175)을 형성하며, 또한 주변 회로 영역에 있어서는 병렬 배선(193) 중 한쪽의 배선(112b)을 형성한다. 즉, 주변 회로 전체에서는, 게이트 전극을 포함해서 제 1 층의 배선을 형성한다.

계속해서, 동 도의 (e)에 나타내는 바와 같이, 반도체층(30)에 적절한 불순물을 도핑한다. 상세하게는, 표시 영역에서의 TFT(116)를 N 채널형으로 하는 경우, 소스·드레인 영역 중 채널 영역(30a)에 인접하는 영역에 대하여, 주사선(112)의 일부인 게이트 전극을 확산 마스크로서, P 등의 V족 원소의 불순물을 저농도로 도핑한다. 동시에, 주변 회로 전체에 있어서의 N 채널형 TFT에 대해서도, 마찬가지로 제 1 층의 배선의 일부인 게이트 전극을 확산 마스크로서, 불순물을 저농도로 도핑한다. 계속해서, 게이트 전극보다도 폭이 넓은 레지스트를 형성하고, 이것을 마스크로서, 마찬가지로 P 등의 V족 원소의 불순물을 고농도로 도핑한다. 이것에 의해 N 채널형 TFT은 채널 영역(30a)의 소스 측에는, 저농도 소스 영역(30b), 고농도 소스 영역(116S)이 마련되는 한편, 드레인 측에는, 저농도 드레인 영역(30c), 고농도 드레인 영역(116D)이 마련되어, LDD 구조로 된다. 또, 도시는 생략하지만, 이들의 N 채널형 TFT의 반도체층(30)을 레지스트로 마스크한 후, 주변 회로 전체에 있어서의 P 채널형 TFT에 대해서도 마찬가지로, 채널 영역에 인접하는 영역에 대하여, 제 1 층의 배선의 일부인 게이트 전극을 마스크로서, 예컨대 B(보론) 등의 III족 원소의 불순물을 도핑하여 저농도 영역을 형성하고, 계속해서, 동(同) 게이트 전극보다도 폭이 넓은 레지스트를 마스크로서, 동일하게 B 등의 III족 원소의 불순물을 도핑하여 고농도 영역을 형성한다. 또한, 각 채널형 TFT를 LDD 구조로 하지 않고, 오프셋 구조의 TFT로도 좋고, 또한 단순한 셀프 얼라인형(자기 정합형)의 TFT라도 좋다.

다음에, 동 도의 (f)에 나타내는 바와 같이, 주사선(112)이나, 제 1 층의 배선(112b), 반도체층(30), 하지 절연막(40) 등을 덮도록, 제 1 층간 절연막(41)을, 예컨대 CVD 법 등에 의해서 퇴적한다. 또, 제 1 층간 절연막(41)의 재질로서는, 하지 절연막(40)과 마찬가지로, NSG나, PSG, BSG, BPSG 등의 실리케이트 유리 막이나, 질화실리콘막, 산화실리콘막 등을 들 수 있다.

또한, 도 12의 (g)에 나타내는 바와 같이, 표시 영역에 있어서는 콘택트 홀(51)을, 주변 회로 영역에 있어서는 제 1 층의 배선(112b)과 접속하기 위한 콘택트 홀(55_1),(56_1)을, 각각 건식 에칭 등에 의해 형성한다. 상세하게는, 콘택트 홀(51)은 TFT(116)의 고농도 드레인 영역(116D)에 대응한 위치에 있어서, 제 1 층간 절연막(41) 및 게이트 절연막(32)을 개구하도록 형성되는 한편, 콘택트 홀(55_1),(56_1)은 제 1 층의 배선(112b)의 양단 위치에 있어서, 각각 제 1 층간 절연막(41)을 개구하도록 형성된다. 또, 주변 회로 전체에 있어서, 제 1 층의 배선과 제 2 층의 배선의 도통을 도모하는 경우에는, 이 도통 부분에 대응하여 마찬가지로 콘택트 홀(도시 생략)이 형성된다.

다음에, 제 1 층간 절연막(41)의 위에, 고융점 금속이나 금속 실리사이드나 또는 폴리실리콘 등으로 이루어지는 도전층을, 스퍼터링 등에 의해서 약 50~500㎚의 두께로, 바람직하게는 약 200㎚ 정도의 두께로 퇴적한다. 도전층은 고융점 금속이나 금속 실리사이드와 폴리실리콘을 다층으로 형성하여도 좋은 것은 물론이다. 이에 따라 도전층의 용력 완화나 콘택트 홈의 저저항화를 실현할 수 있다. 그리고, 이 도전층을, 동 도의 (h)에 나타내는 바와 같이, 포토리소그래피나 에칭 등에 의해서 패터닝하고, 표시 영역에 있어서는, TFT(116)의 고농도 드레인 영역(116D)에 접속되는 중간 도전막(181)으로서 형성하는 한편, 주변 회로 영역에 있어서는, 병렬 배선(193) 중 다른쪽의 배선(181b)을 형성한다. 즉, 주변 회로 전체로서는, 제 2 층의 배선을 형성한다.

계속해서, 동 도의 (i)에 나타내는 바와 같이, 중간 도전막(181)이나, 제 2 층의 배선(18b), 제 1 층간 절연막(41)을 덮도록, 제 2 층간 절연막(42)을, CVD 법 등에 의해서 약 500~1500㎚의 두께로 퇴적한다. 또, 제 2 층간 절연막(42)의 재질로서는, 하지 절연막(40)이나 제 1 층간 절연막(41)과 마찬가지로, NSG나, PSG, BSG, BPSG 등의 실리케이트 유리막이나, 질화실리콘막, 산화실리콘막 등을 들 수 있다.

다음에, 도 13의 (j)에 나타내는 바와 같이, 표시 영역에 있어서는 콘택트 홈(52)을, 주변 회로 영역에 있어서는 제 2 층의 배선(181b)과 접속하기 위한 콘택트 홈(55_2),(56_2)을, 각각 형성한다. 상세하게는, 콘택트 홈(52)은 TFT(116)의 고농도 소스 영역(116S)에 대응한 위치에 있어서, 제 2 층간 절연막(42), 제 1 층간 절연막(41) 및 게이트 절연막(32)을 개구하도록 형성되는 한편, 콘택트 홈(55_2),(56_2)은, 제 2 층의 배선(181b)의 양단 위치에 있어서, 각각 제 2 층간 절연막(42)을 개구하도록 형성된다. 또, 주변 회로 전체에 있어서, 제 2 층의 배선과 제 3 층의 배선의 도통을 도모하는 경우에는, 이 도통 부분에 대응하여 마찬가지로 콘택트 홈(도시 생략)이 형성된다.

또한, 콘택트 홈(52),(552),(562)이 형성된 제 2 층간 절연막(42) 상에, 알루미늄 등의 저 저항 금속으로 이루어지는 도전막을, 스퍼터링 등에 의해서, 약 50~500㎚의 두께로 퇴적한다. 그리고, 이 도전막을, 동 도의 (k)에 나타내는 바와 같이, 포토리소그래피나 에칭 등에 의해서 패터닝하고, 표시 영역에 있어서는 TFT(116)의 소스 전극을 겸용하는 데이터선(114)으로서 형성하는 한편, 주변 회로 영역에 있어서는 배선(391)이나 화상 신호선(122)으로서 형성한다. 즉, 주변 회로 전체에서는, 제 3 층의 배선을 형성한다.

계속해서, 동 도의 (l)에 나타내는 바와 같이, 데이터선(114)이나, 화상 신호선(122) 등의 제 3 층의 배선을 덮도록, 제 3 층간 절연막(43)을 CVD 법 등에 의해서 약 500~1500㎚의 두께로 퇴적한다. 또, 제 3 층간 절연막(43)의 재질로는, 하지 절연막(40)이나, 제 1 층간 절연막(41), 제 2 층간 절연막(42)과 마찬가지로, NSG나, PSG, BSG, BPSG 등의 실리케이트 유리막이나, 질화실리콘막, 산화실리콘막 등을 들 수 있다.

다음에, 도 14의 (m)에 나타내는 바와 같이, 콘택트 홈(53)을, 중간 도전막(181)에 있어서의 소정의 위치에 있어서, 제 3 층간 절연막(43) 및 제 2 층간 절연막(42)을 개구하도록, 건식 에칭 등에 의해 형성한다.

그리고, 콘택트 홈(53)이 형성된 제 3 층간 절연막(42)의 표면에, ITO 등의 투명 도전성막을, 스퍼터링 등에 의해서 약 50~200㎚의 두께로 퇴적한 후, 포토리소그래피나 에칭 등에 의해서 소정의 형상(도 5참조)으로 패터닝하여, 동 도의 (n)에 나타내는 바와 같이, 화소 전극(118)을 형성한다. 이 다음의 공정에 대해서는 도시를 생략하지만, 폴리이미드 등의 유기 용액을, 기판(10)에 있어서 대향면으로 이루어지는 화소 전극(118) 및 제 3 층간 절연막(43)의 전면에 도포·소성한다. 이에 의해, 배향막(61)이 형성되게 된다. 또, 이 배향막(61)에는, 소정의 방향으로 러빙 처리가 실시된다.

그리고, 이와 같이 형성된 소자 기판(101)은 그것과는 약 90도 회전시킨 방향으로 러빙 처리된 대향 기판(102)과, 밀봉재(104)에 의해 접합된 후에, 액정(105)이 봉입 봉지되어, 도 1에 나타내는 바와 같은 전기 광학 장치로 된다.

또, 소자 기판(101)에 있어서는, 배향막(61)이 전면에 걸쳐 형성되지만, 액정 봉지 후에는 플라즈마 처리 등에 의해, 주변 회로 영역으로서, 대향 기판(102)으로부터 게시한 부분에 형성된 배향막이 제거된다. 이 때문에, 주변 회로 영역에서의 최상층은 배향막(61)이 아니라 제 3 층간 절연막(43)으로 된다.

이러한 제조 방법에 따르면, 표시 영역에서, TFT(116)의 고농도 드레인 영역(116D)에 대한 배리어막으로서 이용되고 있던 중간 도전막(181)과 동일층의 도전막을, 주변 회로에 있어서의 제 2 층의 배선으로서 이용하는 것이, 특별한 프로세스를 추가하는 일없이 가능해진다. 또한, 3층 분의 배선을 이용하는 것에 따라, 주변 회로의 설계에 있어서의 자유도를 각 단에 향상시키는 것이 가능해진다. 아울러, 제 1 층의 배선과 동시에 병렬 접속되는 것으로, 해당 배선의 저저항화를 도모하는 것이 가능해지고, 또한 제 2 층의 배선을, 단독으로 이용하는 것에 따라, 동일 영역에서 3층의 배선을 형성하는 것이 가능해진다.

(응용예)

또, 상술한 실시예에 있어서, 제 3 층의 배선이 제 1 층의 배선과 제 2 층의 배선의 병렬 배선에 접속되는 경우, 해당 제 3 층의 배선은 제 2 층의 배선에 접속되는 구성으로 되어 있었다. 예컨대, 도 8의 (b)에 있어서, 화상 신호선(122)은 병렬 배선(193) 중 제 2 층의 배선(181b)에 접속되는 구성으로 되어 있었다.

상술한 바와 같이, 제 2 층의 도전층은 용력이 발생하기 쉬운(휘어지기 쉬운) 고융점 금속 등으로 구성하는 경우, 이러한 고융점 금속의 배선(181b)에 접속하기 위한 콘택트 홈(55_2),(56_2)을 개구하면, 개구에 따른 용력 집중에 의해서 제 2 층간 절연막(42)에 크랙 등이 발생할 가능성이 있다. 또한, 콘택트 홈(55_2),(56_2)에 의해서, 제 2 층의 배선(181b)을 노출시키면, 해당 배선(181b)에서 불순물이 발산되어, 불량화의 원인으로도 된다.

그래서, 제 3 층의 배선을 제 1 층의 배선(112b)과 제 2 층의 배선(181b)의 병렬 배선(193)의 일단에 접

속하는 경우에는, 예컨대 도 15의 (a)에 나타내는 바와 같이, 제 2 층의 배선(181b)을, 약간 내측의 콘택트 홀(57_1),(58_1)을 거쳐 제 1 배선(112b)에 접속하여, 병렬 배선(193)으로 합과 동시에, 제 3 층의 배선을, 외측의 콘택트 홀(57_2) 또는 콘택트 홀(58_2)을 거쳐서 제 1 층의 배선(112b)에 접속하는 구성이 바람직하다고 생각한다. 이 구성에서는, 제 2 층간 절연막(42)이 형성된 후에 있어서는, 제 2 층의 배선(181b)이 노출되는 경우는 없다. 이 때문에, 콘택트 홀의 개구에 따른 응력 집중이 발생하지 않기 때문에, 제 2 층간 절연막(42)에 있어서의 크랙이 방지되고, 또한 해당 배선(181b)에서 불순물이 발산되는 것도 방지할 수 있게 된다.

또한, 병렬 배선(193)은 제 1 배선(112b) 및 제 2 배선(181b)의 양단에 있어서만 접속을 도모하는 구성이지만, 도 15의 (b)에 나타내는 바와 같이, 양단 이외의 1이상의 지점에 콘택트 홀(58),(59)을 마련하여, 이 지점에서도 접속하여, 양 배선의 접속을 보다 확실하게 하는 구성으로 하여도 좋다. 또, 이와 같이 제 1 배선(112b)과 제 2 배선(181b)의 접속을, 양단 이외의 1이상의 콘택트 홀을 거쳐서 도모하는 구성에 있어서도, 제 3 층의 배선을, 외측의 콘택트 홀을 거쳐서 제 1 층의 배선(112b)에 접속하여도 좋다.

(기타)

또한, 상술한 실시예에 있어서는, 6개의 데이터선(114)이 1블럭으로 정리되고, 1블럭에 속하는 6개의 데이터선(114)에 대하여, 6계통으로 변환된 화상 신호 V1O1~V1O6을 동시에 샘플링하여 공급하는 구성으로 했지만, 변환 수 및 동시에 인가하는 데이터선 수(즉, 1블럭을 구성하는 데이터선 수)는 「6」 개로 한정되는 것은 아니다. 예컨대, 샘플링 회로(150)에 있어서의 샘플링 스위치(151)의 응답 속도가 충분히 높은 것이면, 화상 신호를 수평으로 변환하는 일없이 1개의 화상 신호선에 직렬 전송하여, 데이터선(114)마다 점순차적으로 샘플링하도록 구성하여도 좋다. 또, 이러한 구성에서는, 데이터선 구동 회로(140)를 구성하는 시프트 레지스터나 논리곱 회로를 데이터선 피치와 동배로 형성해야 하기 때문에, 주사선 구동 회로(130)와 마찬가지로, 제 2 층의 배선을 단독으로 이용할 필요가 있을 지도 모른다.

또한, 변환 및 동시에 인가하는 데이터선의 수를 「3」 이나, 「12」, 「24」 등으로 하여, 3개나, 12개, 24개 등의 데이터선에 대하여, 3계통 변환이나, 12계통, 24계통 변환 등으로 한 화상 신호를 동시에 공급하는 구성으로 하여도 좋다. 또, 변환 수 및 동시에 인가하는 데이터선 수로서는, 컬러의 화상 신호가 3개의 원색에 따른 신호로 이루어지는 것과의 관계상, 3의 배수인 것이 제어나 회로 등을 간이화하는데에 있어서 바람직하다. 단, 후술하는 프로젝터와 같이 단순한 광 변조의 용도일 경우에는, 3의 배수인 것이 필요하지 않다. 또한, 복수개의 샘플링 스위치를 동시에 제어하는 것은 아니고, 수평 변환된 화상 신호 V1O1~V1O6을 순차 시프트하여 공급하여, 샘플링 스위치(151)를 순서대로 제어하는 구성으로서도 좋다.

또한, 상술한 실시예에 있어서는, 위에서 아래 방향으로 주사선(112)을 주사하는 한편, 왼쪽에서 오른쪽 방향으로 블럭을 선택하는 구성으로 했지만, 이것과는 역방향으로 선택하는 구성이어도 좋고, 용도에 따라 어느 하나의 방향을 선택 가능하게 하는 구성이어도 좋다.

또한, 상술한 실시예에 있어서는, 소자 기판(101)에 플래너형의 TFT(116) 등이 형성되어 있지만, 본 발명은 이것에 한정되지 않는다. 예컨대, TFT(116)를 바닥(bottom) 게이트형으로 구성하여도 좋다. 또한, 소자 기판(101)을 반도체 기판으로 구성함과 동시에, 여기에, TFT(116)에 대신 전계 효과형 트랜지스터를 형성하여도 좋다. 또한, SOI(Silicon On Insulator)의 기술을 적용하여, 사파이어, 석영, 유리 등의 절연성 기판에 실리콘 단결정막을 형성하여, 여기에 각종 소자를 만들어 넣은 소자 기판(101)으로 하여도 좋다. 단, 소자 기판(101)이 투명성을 갖지 않는 경우, 화소 전극(118)을 알루미늄으로 형성하거나, 별도의 반사층을 형성하는 등으로 하여, 액정 패널(100)을 반사형으로서 이용할 필요가 있다.

또한, 상술한 실시예에서는, 액정으로서 TN형을 이용했지만, BTN(Bi-stable Twisted Nematic)형 · 강유전형 등의 메모리 성을 갖는 쌍안정형이나, 고분자 분산형, 그 위에, 분자의 장축 방향과 단축 방향에서 가시광의 흡수에 이방성을 갖는 염료(게스트)를 일정한 분자 배열의 액정(호스트)에 용해하여, 염료 분자를 액정 분자와 평행하게 배열시킨 게스트 호스트형 등의 액정을 이용하여도 좋다.

또한, 전압 무인가 시에는 액정 분자가 양 기판에 대하여 수직 방향으로 배열되는 한편, 전압 인가 시에는 액정 분자가 양 기판에 대하여 수평 방향으로 배열된다는 수직 배향(호메오 트로픽 배향)의 구성으로 하여도 좋고, 전압 무인가 시에는 액정 분자가 양 기판에 대하여 수평 방향으로 배열되는 한편, 전압 인가 시에는 액정 분자가 양 기판에 대하여 수직 방향으로 배열된다는 수평(평행) 배향(호모지니어스 배향)의 구성으로 하여도 좋다. 이와 같이, 본 발명에서는, 액정이나 배향 방식으로서, 여러 가지의 것에 적용하는 것이 가능하다.

또한, 전기 광학 장치로는, 액정 장치의 이외에, EL(electro luminescence)나, 플라즈마 발광이나 전자 방출에 의한 형광 등을 이용하여, 그 전기 광학 효과에 의해 표시를 행하는 여러 가지의 전기 광학 장치에 적용 가능하다. 이 때, 전기 광학 물질로는, EL, 미러 장치, 가스, 형광체 등으로 이루어진다. 또, 전기 광학 물질로서 EL을 이용하는 경우, 소자 기판(101)에 있어서 EL이 화소 전극(118)과 투명 도전막의 대향 전극(108) 사이에 개재하게 되기 때문에, 대향 기판(102)은 불필요하게 된다. 이와 같이, 본 발명은 상술한 구성과 유사한 구성을 갖는 전기 광학 장치 모두에 적용할 수 있다.

(전자기기)

다음에, 상술한 실시예에 따른 전기 광학 장치를 이용한 전자기기의 몇 개인가에 대하여 설명한다.

(그 1 : 프로젝터)

우선, 상술한 액정 패널(100)을 광밸브로서 이용한 프로젝터에 대하여 설명한다. 도 16은 이 프로젝터의

구성을 나타내는 평면도이다. 이 도면에 나타내는 바와 같이, 프로젝터(2100) 내부에는, 할로겐 램프 등의 백색 광원으로 이루어지는 램프 유닛(2102)이 마련되어 있다. 이 램프 유닛(2102)으로부터 사출된 투사광은 내부에 배치된 3장의 미러(2106) 및 2장의 다이크로익 미러(2108)에 의해서 RGB의 3원색으로 분리되고, 각 원색에 대응하는 광밸브(100R),(100G),(100B)에 각각 유도된다. 여기서, 광밸브(100R),(100G),(100B)의 구성은 상술한 실시예에 따른 액정 패널(100)과 마찬가지이고, 화상 신호를 입력하는 처리 회로(도시 생략)로부터 공급되는 R, G, B의 원색 신호로 각각 구동되는 것이다. 또한, B색의 광은 다른 R색이나 G색과 비교하면, 광로가 길기 때문에, 그 손실을 막기 위해서, 입사 렌즈(2122), 릴레이(relay) 렌즈(2123) 및 사출 렌즈(2124)로 이루어지는 릴레이 렌즈계(2121)를 거쳐서 유도된다.

그런데, 광밸브(100R),(100G),(100B)에 의해서 각각 변조된 광은 다이클로익 프리즘(2112)에 3방향으로부터 입사된다. 그리고, 이 다이클로익 프리즘(2112)에 있어서, R색 및 B색의 광은 90도로 굴절하는 한편, G색의 광은 직진한다. 따라서, 각 색의 화상이 합성된 후, 스크린(2120)에는, 투사 렌즈(2114)에 의해서 컬러 화상이 투사되는 것으로 된다.

또, 광밸브(100R),(100G),(100B)에는, 다이클로익 미러(2108)에 의해서, R, G, B의 각 원색에 대응하는 광이 입사하기 때문에, 상술한 바와 같이, 컬러 필터를 마련할 필요는 없다. 또한, 광밸브(100R),(100B)의 투과상은 다이클로익 미러(2112)에 의해 반사한 후에 투사되는 데 비하여, 광밸브(100G)의 투과상은 그대로 투사되기 때문에, 광밸브(100R),(100B)에 의한 표시상을, 광밸브(100G)에 의한 표시상에 대하여 좌우 반전시키는 구성으로 되어 있다.

(그 2 : 모바일형 컴퓨터)

다음에, 상술한 액정 패널(100)을, 모바일형의 퍼스널 컴퓨터에 적용한 예에 대하여 설명한다. 도 17은 이 퍼스널 컴퓨터의 구성을 나타내는 사시도이다. 도면에 있어서, 컴퓨터(2200)는 키보드(2202)를 구비한 본체부(2204)와, 표시부로서 이용되는 액정 패널(100)을 구비하고 있다. 또, 이 액정 패널(100)의 배면에는, 시인성을 높이기 위한 백라이트 유닛(도시 생략)이 마련된다.

(그 3 : 휴대 전화)

또한, 상술한 액정 패널(100)을 휴대 전화의 표시부에 적용한 예에 대하여 설명한다. 도 18은 이 휴대 전화의 구성을 나타내는 사시도이다. 도면에 있어서, 휴대 전화(2300)는 복수의 조작 버튼(2302) 외에, 수화구(2304), 송화구(2306)와 동시에, 상술한 액정 패널(100)을 구비하는 것이다. 또, 이 액정 패널(100)의 배면에도, 시인성을 높이기 위한 백라이트 유닛(도시 생략)이 마련된다.

또, 전자기기로는, 도 16, 도 17 및 도 18을 참조하여 설명한 외에도, 액정 텔레비전이나, 뷰파인더형·모니터 직시형의 비디오 테이프 레코더, 카 네비게이션 장치, 호출기, 전자 수첩, 전자 계산기, 워드프로세서, 워크스테이션, 화상 전화, POS단말, 디지털 스틸 카메라, 터치 패널을 갖춘 기기 등등을 들 수 있다. 그리고, 이들의 각종의 전자기기에 대하여, 실시예나 응용 형태에 따른 전기 광학 장치가 적용 가능한 것은 말할 필요도 없다.

발명의 효과

이상 설명한 바와 같이 본 발명에 따르면, 표시 영역에서의 스위칭 소자의 타단과 화소 전극과의 접속에 이용되는 중간 도전막과 동일한 도전층으로 이루어지는 배선을 이용할 수 있기 때문에, 주변 회로를 설계할 때의 자유도를 향상시키는 것이 가능해진다.

이상 본 발명자에 의해서 이루어진 발명을 상기 실시예에 따라 구체적으로 설명하였지만, 본 발명은 상기 실시예에 한정되는 것이 아니고, 그 요지를 이탈하지 않는 범위에서 여러 가지로 변경 가능한 것은 물론이다.

(57) 청구의 범위

청구항 1

복수의 주사선 및 복수의 데이터선과,

상기 주사선 및 데이터선의 교차 부분에 대응하여 마련된 스위칭 소자 및 화소 전극의 쌍과,

상기 스위칭 소자와 대응하는 화소 전극 사이를 전기적으로 접속하는 중간 도전막과,

상기 중간 도전막을 구성하는 도전층과 동일층으로 이루어지는 배선을 포함하여, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로

를 구비하는 것을 특징으로 하는 전기 광학 장치.

청구항 2

제 1 항에 있어서,

상기 중간 도전막은 스위칭 소자의 전극에 대응하여 마련된 제 1 콘택트 홀을 거쳐서 전기적으로 접속되는 한편, 상기 화소 전극은 제 2 콘택트 홀을 거쳐서 전기적으로 접속되는 것을 특징으로 하는 전기 광학 장치.

청구항 3

제 1 항에 있어서,

일단(一端)이 상기 화소 전극에 접속되는 한편, 타단(他端)이 공통 접속되는 축적 용량 소자를, 화소 전극마다 구비하되,

상기 중간 도전막은 상기 축적 용량 소자를 구성하는 전극의 일부를 이루는 것을 특징으로 하는

전기 광학 장치.

청구항 4

제 1 항에 있어서,

상기 중간 도전막은 차광성을 갖고,

상기 화소 전극을 투과 또는 반사하는 광의 일부가, 해당 중간 도전막에 의해서 규정되어 있는 것을 특징으로 하는

전기 광학 장치.

청구항 5

제 1, 제 2 및 제 3 도전층을, 이 순서로 형성하여 이루어지고, 상기 제 3 도전층은 상기 제 1 도전층보다도 저 저항인 전기 광학 장치에 있어서,

상기 제 1 도전층으로 이루어지는 복수의 주사선과,

상기 제 3 도전층으로 이루어지고, 상기 복수의 주사선에 대하여 서로 교차하도록 형성된 복수의 데이터선과,

상기 주사선 및 상기 데이터선의 교차 부분에 대응하여 마련된 스위칭 소자 및 화소 전극의 쌍과,

상기 제 2 도전층으로 이루어지고, 상기 스위칭 소자와 대응하는 화소 전극 사이를 전기적으로 접속하는 중간 도전막과,

상기 제 1, 제 2 및 제 3 도전층으로 이루어지는 배선을 각각 구비하여, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로

를 구비하는 것을 특징으로 하는 전기 광학 장치.

청구항 6

제 5 항에 있어서,

상기 중간 도전막은 스위칭 소자의 전극에 대응하여 마련된 제 1 콘택트 홀을 거쳐서 전기적으로 접속되는 한편, 상기 화소 전극은 제 2 콘택트 홀을 거쳐서 전기적으로 접속되는 것을 특징으로 하는 전기 광학 장치.

청구항 7

제 5 항에 있어서,

상기 주변 회로는 상기 제 1 도전층으로 이루어지는 배선과 상기 제 2 도전층으로 이루어지는 배선이 전기적으로 병렬 접속된 병렬 배선을 갖는 것을 특징으로 하는 전기 광학 장치.

청구항 8

제 7 항에 있어서,

상기 병렬 배선은 상기 제 3 도전층으로 이루어지는 배선으로부터 분기되는 분기 배선으로서, 해당 배선과는 다른 배선과 교차하는 부분에 이용되고 있는 것을 특징으로 하는 전기 광학 장치.

청구항 9

제 7 항에 있어서,

상기 주변 회로는

상기 제 3 도전층으로 이루어지고, h(h는 2이상의 정수)개의 데이터선에 대응하여 화상 신호를 공급하는

h개의 화상 신호선과,

상기 데이터선의 각각에 대응하여 마련되어, 상기 h개의 화상 신호선에 공급된 화상 신호 중 대응하는 것을 소정의 샘플링 신호에 따라서 샘플링하여, 대응하는 데이터선에 공급하는 샘플링 스위치를 포함하되,

상기 병렬 배선은 상기 화상 신호선으로부터 분기하여 상기 샘플링 스위치에 이르는 배선의 적어도 일부에 이용되고 있는 것을 특징으로 하는

전기 광학 장치.

청구항 10

제 7 항에 있어서,

상기 병렬 배선 중 상기 제 2 도전층으로 이루어지는 배선이, 해당 병렬 배선 중 상기 제 1 도전층으로 이루어지는 배선을 각각 노출하는 제 3 및 제 4 콘택트 홀 사이를 도통시키고,

상기 제 3 도전층으로 이루어지는 배선이, 상기 제 3 또는 제 4 콘택트 홀에 일치하는 위치에 마련되어, 상기 제 2 도전층으로 이루어지는 배선을 노출하는 제 5 콘택트 홀에 전기적으로 접속되어 있는 것을 특징으로 하는

전기 광학 장치.

청구항 11

제 7 항에 있어서,

상기 병렬 배선 중 상기 제 2 도전층으로 이루어지는 배선이, 해당 병렬 배선 중 상기 제 1 도전층으로 이루어지는 배선을 각각 노출하는 제 3 및 제 4 콘택트 홀 사이를 도통시키고,

상기 제 3 도전층으로 이루어지는 배선이, 상기 제 3 및 제 4 콘택트 홀과는 다른 위치에 마련되어, 상기 제 1 도전층으로 이루어지는 배선을 노출하는 제 6 콘택트 홀에 전기적으로 접속되어 있는 것을 특징으로 하는

전기 광학 장치.

청구항 12

제 10 항 또는 제 11 항에 있어서,

상기 병렬 배선 중 상기 제 2 도전층으로 이루어지는 배선이 상기 제 3 및 제 4 콘택트 홀 사이에 마련된 하나 또는 복수의 콘택트 홀에 있어서도 상기 제 1 도전층으로 이루어지는 배선과 도통하고 있는 것을 특징으로 하는 전기 광학 장치.

청구항 13

제 5 항에 있어서,

상기 주변 회로는, 그 일부의 영역에서, 상기 제 1, 제 2 및 제 3 도전층으로 이루어지는 배선을 구비하는 것을 특징으로 하는 전기 광학 장치.

청구항 14

제 5 항에 있어서,

일단이 상기 화소 전극에 접속되는 한편, 타단이 공통 접속되는 축적 용량 소자를 화소 전극마다 구비하되,

상기 중간 도전막은 상기 축적 용량 소자를 구성하는 전극의 일부를 이루는 것을 특징으로 하는

전기 광학 장치.

청구항 15

제 14 항에 있어서,

상기 축적 용량 소자는

상기 스위칭 소자의 전극과 상기 제 2 도전층으로 이루어지는 용량선 사이에 상기 스위칭 소자의 게이트 산화막을 유지하여 이루어지는 제 1 용량 소자와,

상기 중간 도전막과 상기 용량선 사이에 층간 절연막을 유지하여 이루어지는 제 2 용량 소자를 포함하는 것을 특징으로 하는

전기 광학 장치.

청구항 16

제 5 항에 있어서,

상기 중간 도전막은 차광성을 갖고,

상기 화소 전극을 투과 또는 반사하는 광의 일부가, 해당 중간 도전막에 의해서 규정되어 있는 것을 특징으로 하는

전기 광학 장치.

청구항 17

제 5 항에 있어서,

상기 제 1 도전층은 폴리실리콘으로 이루어지는 것을 특징으로 하는 전기 광학 장치.

청구항 18

제 5 항에 있어서,

상기 제 3 도전층은 알루미늄으로 이루어지는 것을 특징으로 하는 전기 광학 장치.

청구항 19

제 5 항에 있어서,

상기 제 2 도전층은 상기 제 3 도전층을 구성하는 재료보다도 고융점인 재료로 이루어지는 것을 특징으로 하는 전기 광학 장치.

청구항 20

복수의 주사선 및 복수의 데이터선과,

상기 주사선 및 데이터선의 교차 부분에 대응하여 마련된 스위칭 소자 및 화소 전극의 쌍과,

상기 스위칭 소자와 대응하는 화소 전극 사이를 전기적으로 접속하는 중간 도전막과,

상기 스위칭 소자의 각각을 구동하기 위한 주변 회로와,

상기 주변 회로에 접속되어 상기 중간 도전막을 구성하는 도전층과 동일층으로 이루어지는 배선

을 구비하는 것을 특징으로 하는 전기 광학 장치.

청구항 21

제 20 항에 있어서,

상기 배선은 상기 데이터선을 구성하는 도전층과 동일층으로 이루어지는 화상 신호선에 대하여 하층에서 교차하는 것을 특징으로 하는 전기 광학 장치.

청구항 22

제 21 항에 있어서,

상기 화상 신호선은, 복수의 화상 신호선이 배치되고, 각 화상 신호선에 대응하여 상기 배선이 접속되며, 각 배선의 크기는 거의 동일한 것을 특징으로 하는 전기 광학 장치.

청구항 23

제 20 항에 있어서,

상기 데이터선을 구성하는 도전층과 동일층으로 이루어지는 제 1 도전층과, 상기 데이터선을 구성하는 도전층과 동일층으로 이루어지고 상기 제 1 도전층과 떨어진 위치에 형성된 제 2 도전층을 갖고,

상기 스위칭 소자의 반도체층과 동일층으로 이루어지는 제 3 도전층은, 콘택트 홀을 거쳐서 상기 제 1 도전층과 상기 제 2 도전층에 대하여 전기적으로 접속되는 것을 특징으로 하는

전기 광학 장치.

청구항 24

제 23 항에 있어서,

상기 배선은 상기 제 3 도전층에 대하여 콘택트 홀을 거쳐서 전기적으로 접속되는 것을 특징으로 하는 전기 광학 장치.

청구항 25

제 24 항에 있어서,

상기 제 3 도전층은 폴리실리콘으로 이루어지는 것을 특징으로 하는 전기 광학 장치.

청구항 26

제 24 항에 있어서,

상기 배선과 상기 제 3 도전층을 전기적으로 접속하는 콘택트 홀을 적어도 3개 갖는 것을 특징으로 하는 전기 광학 장치.

청구항 27

제 23 항에 있어서,

상기 제 1 도전층과 상기 제 2 도전층의 사이에, 상기 데이터선을 구성하는 도전층과 동일층으로 이루어지는 화상 신호선이 배치되어 있는 것을 특징으로 하는 전기 광학 장치.

청구항 28

청구항 1 내지 27 중 어느 한 항에 기재된 전기 광학 장치를 구비하는 것을 특징으로 하는 전자기기.

청구항 29

복수의 주사선과, 상기 복수의 주사선과의 교차 부분에 대응하여 스위칭 소자 및 화소 전극의 쌍을 구비하는 전기 광학 장치의 제조 방법에 있어서,

상기 주사선 및 상기 데이터선이 교차해야 할 부분에 스위칭 소자를 형성하는 공정과,

상기 스위칭 소자에 접속되는 중간 도전막과, 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로에 이용하는 배선을, 각각 동일한 도전층으로 형성하는 공정과,

상기 중간 도전막에 접속되는 화소 전극을 형성하는 공정

를 구비하는 것을 특징으로 하는 전기 광학 장치의 제조 방법.

청구항 30

복수의 주사선과, 상기 복수의 주사선의 교차 부분에 대응하여 스위칭 소자 및 화소 전극의 쌍을 구비하는 전기 광학 장치의 제조 방법에 있어서,

상기 주사선과 상기 스위칭 소자의 각각을 구동하기 위한 주변 회로에 이용하는 배선을 각각 제 1 도전층으로 형성한 후에, 또한 상기 주사선 및 상기 데이터선이 교차해야 할 부분에 스위칭 소자를 형성한 후에,

상기 스위칭 소자에 접속되는 중간 도전막과 상기 주변 회로에 이용하는 배선을 각각 제 2 도전층으로 형성하는 공정과,

상기 데이터선과 상기 주변 회로에 이용하는 배선을 각각 제 3 도전층으로 형성하는 공정과,

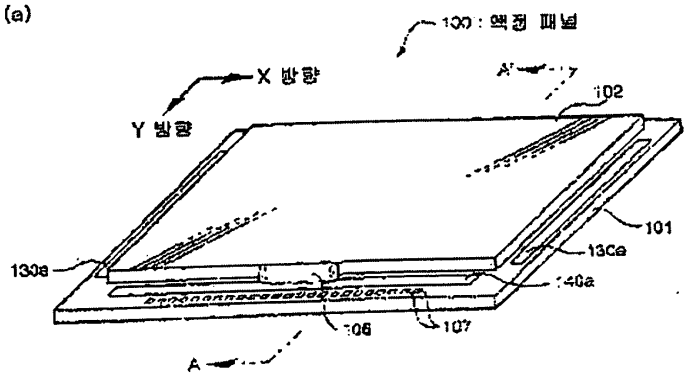
상기 중간 도전막에 접속되는 화소 전극을 형성하는 공정

을 구비하는 것을 특징으로 하는 전기 광학 장치의 제조 방법.

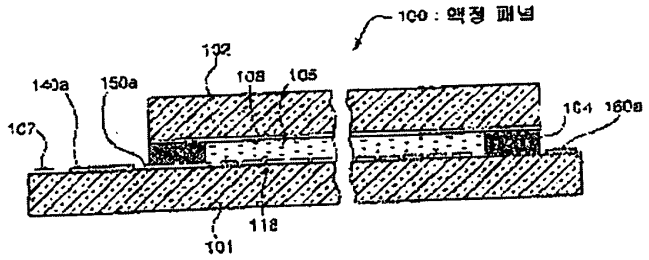
도면

도면1

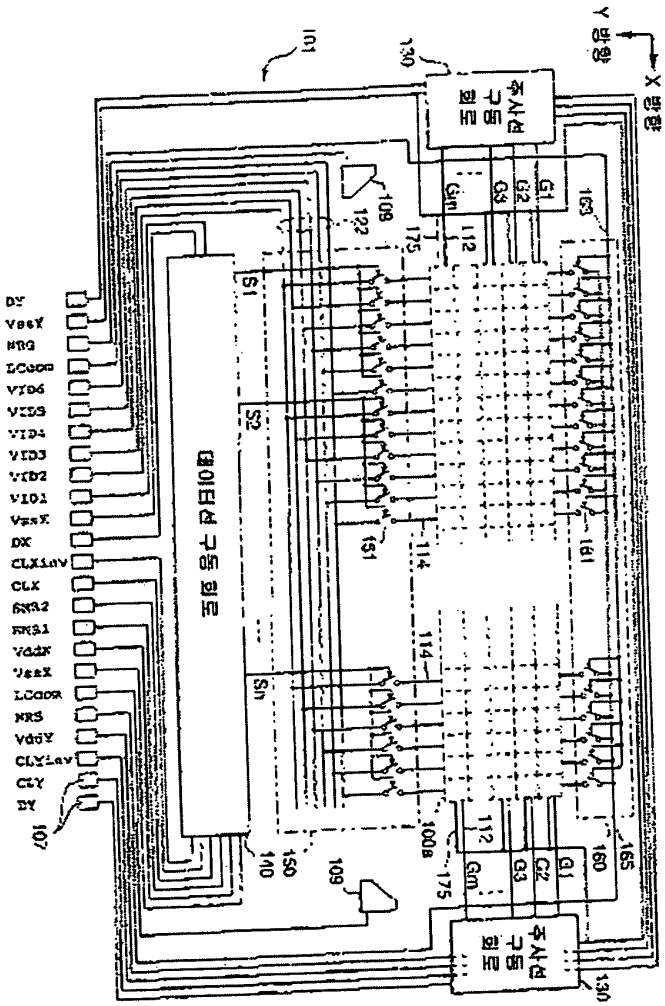
(a)


100 : 액정 패널
X 방향
Y 방향
A'
102
101
130a
140a
106
107
A

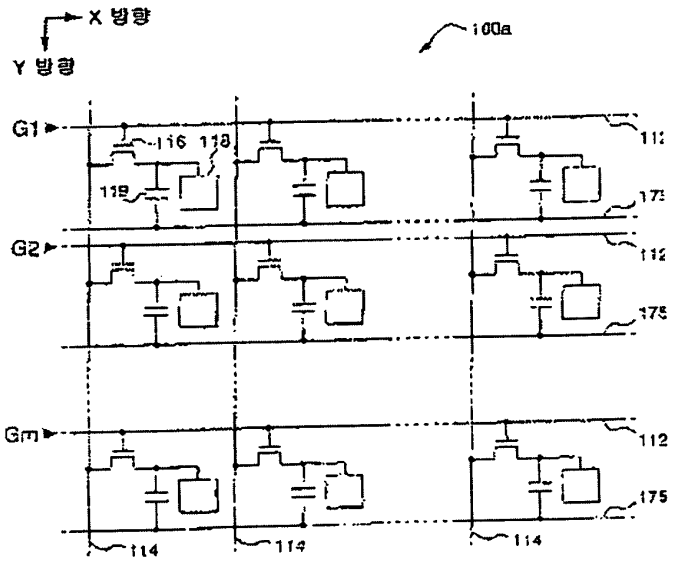
(b)


100 : 액정 패널
102
140a
150a
108
105
104
160a
107
118
101

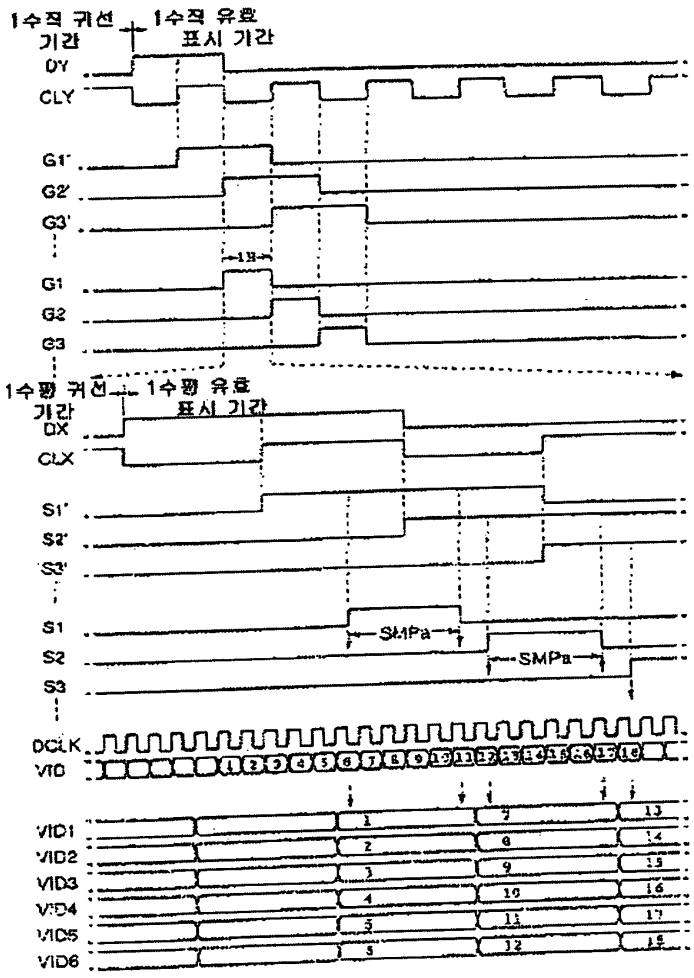
도면2


Y 방향
X 방향
101
130
주사선 구동 회로
G1
G2
G3
Gm
163
108
122
175
112
S1
S2
Sn
데이터선 구동 회로
151
114
161
DY
VssY
NRS
LCmos
VID6
VID5
VID4
VID3
VID2
VID1
VssX
DX
CLXinV
CLX
6NR2
RNR1
VddX
VssX
LCmosR
NRS
VddY
CLYinV
CLY
DY
107
150
140
109
100a
160
165

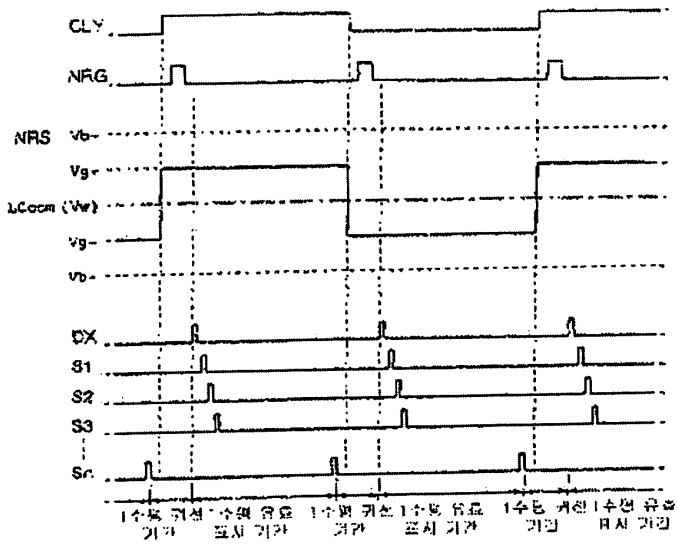
도면3



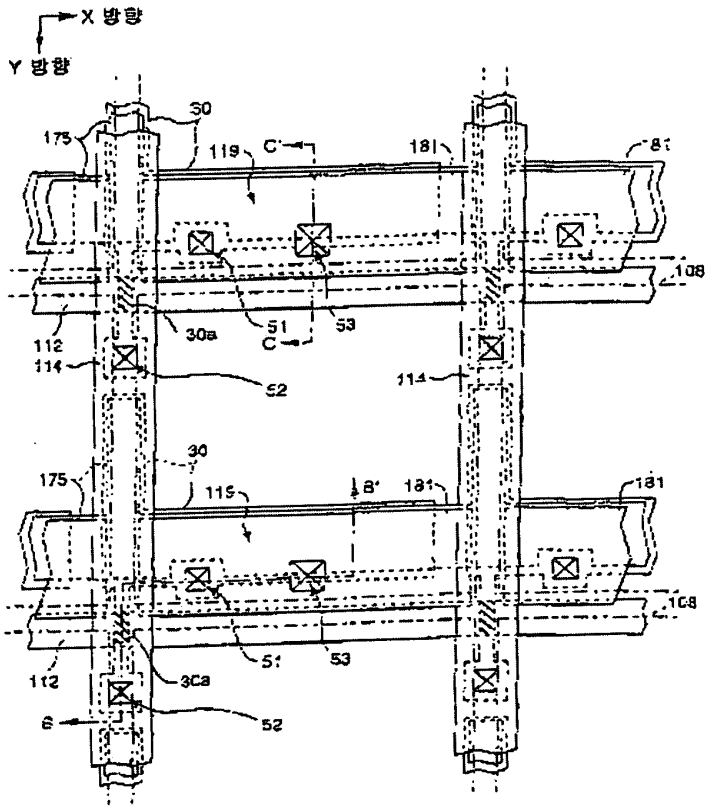
도면4


1수직 귀선 기간
1수직 유효 표시 기간
DY
CLY
G1'
G2'
G3'
1H
G1
G2
G3
1수평 귀선 기간
1수평 유효 표시 기간
DX
CLX
S1'
S2'
S3'
S1
S2
S3
SMPa
SMPa
DCLK
VID
VID1
VID2
VID3
VID4
VID5
VID6

도면5

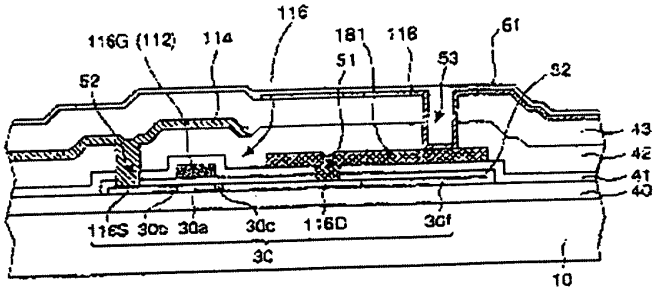


도면8

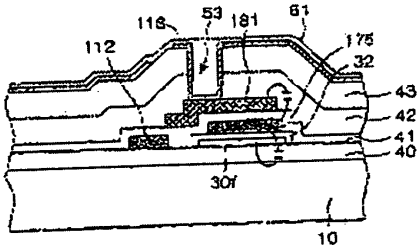


도면7

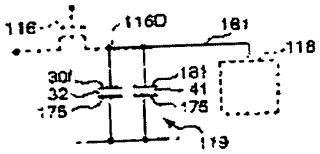
(a) B-B'선 단면도



(b) C-C' 선 단면도

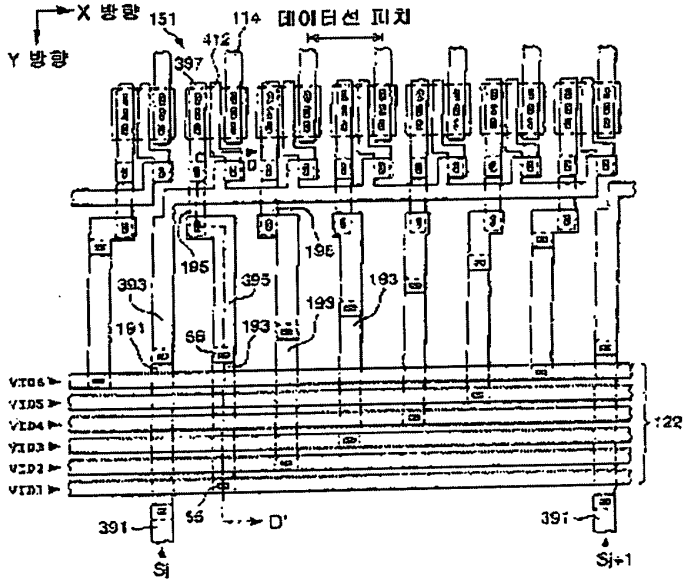


(c) 축적 용량 소자의 등가 회로

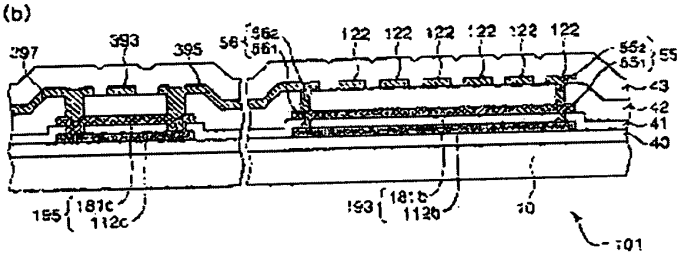


도면8

(a)

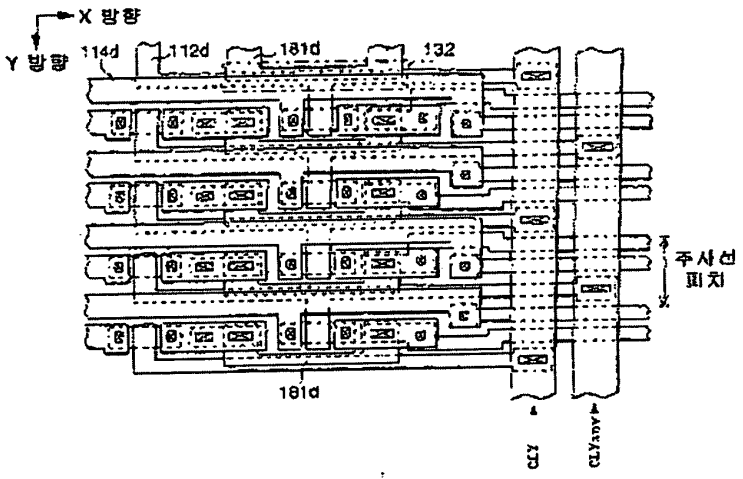

X 방향
Y 방향
151
114
데이터선 피치
397
412
195
393
395
193
191
56
VID6
VID5
VID4
VID3
VID2
VID1
122
391
D'
Sj
Sj+1

(b)

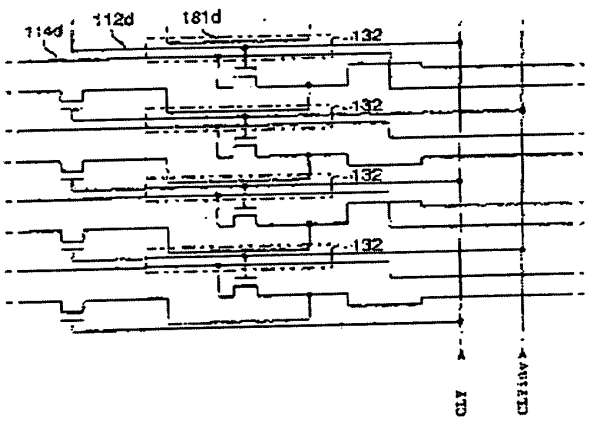

397
393
395
56
562
561
122
552
551
55
43
42
41
40
195
181c
112c
193
181b
112b
30
101

도면9

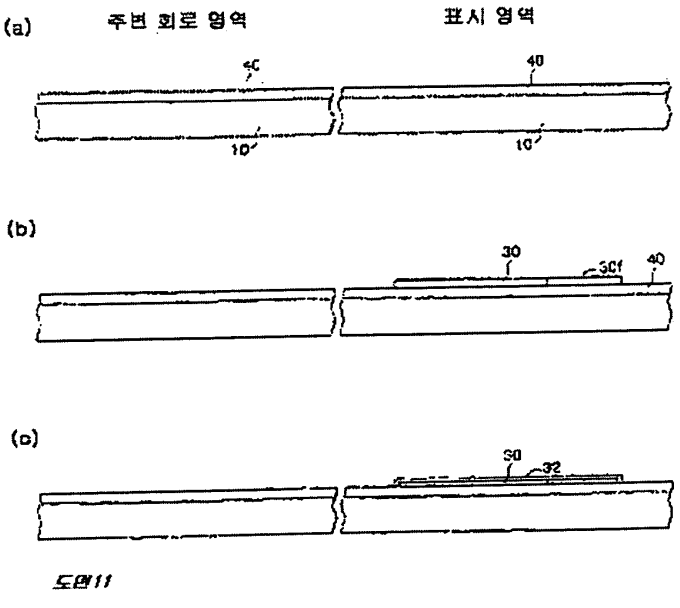
(a)


X 방향
Y 방향
114d
112d
181d
132
주사선 피치
181d
CLY
CLYinv

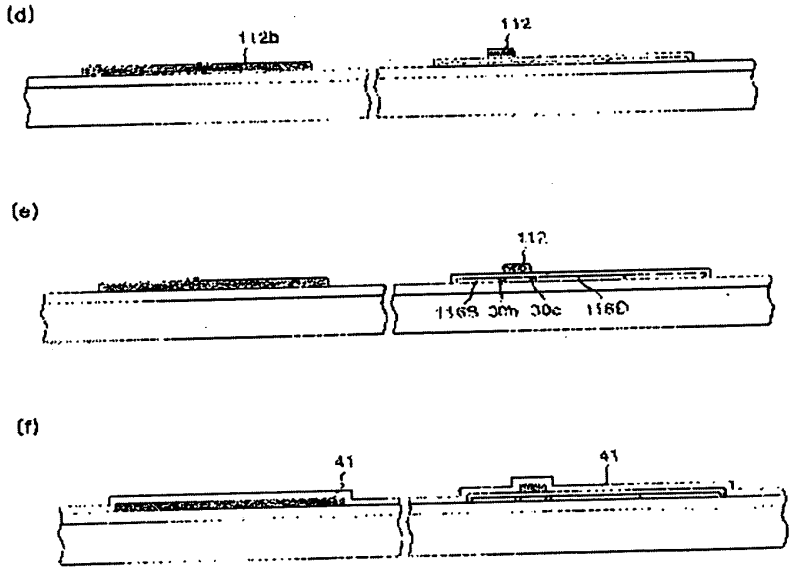
(b)


114d
112d
181d
132
132
132
132
CLY
CLYinv

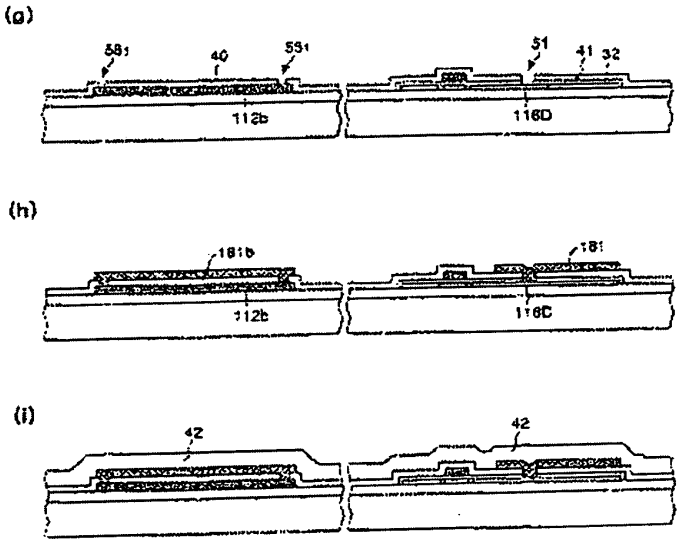
도면10


(a)
주변 회로 영역
표시 영역
40
40
10
10
(b)
30
30f
40
(c)
30
32

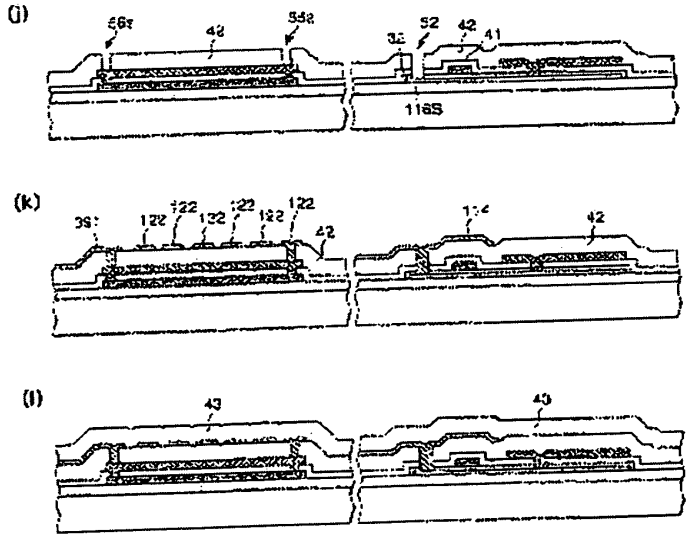
도면11


(d)
112b
112
(e)
112
116S
30m
30c
116D
(f)
41
41

도면12

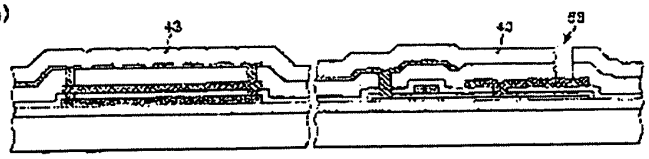

(a)
581
40
551
51
41
32
112b
116D
(h)
181b
181
112b
116C
(i)
42
42

도면13

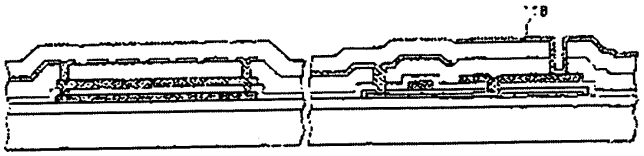

(j)
56t
42
55a
52
42
41
116S
(k)
122
122
122
122
122
42
42
(l)
43
43

도면14

(m)

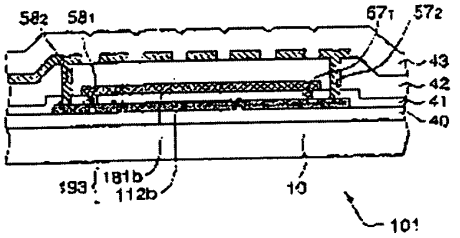


(n)

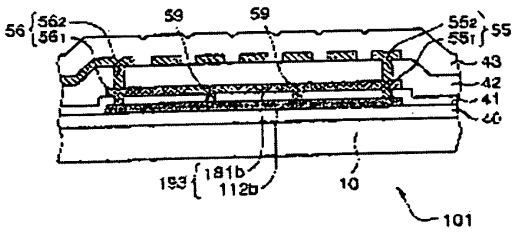


도면15

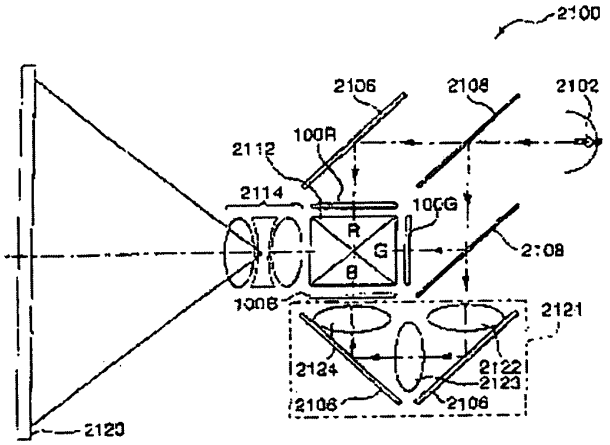
(a)



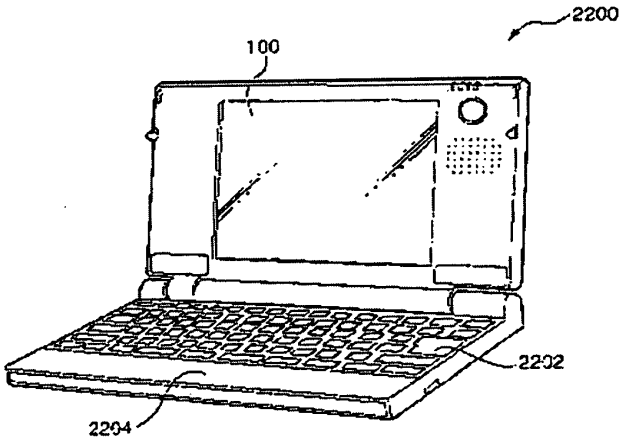
(b)



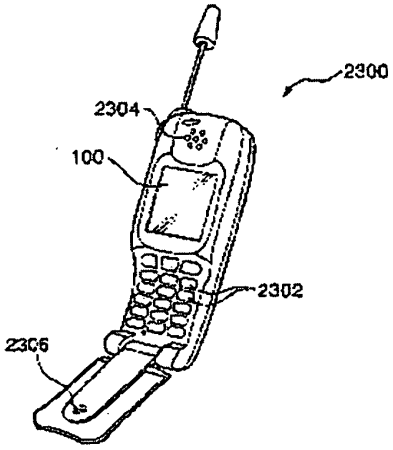
도면16


2100
2106
2108
2102
100R
2112
2114
100G
R
G
B
2108
100B
2121
2124
2122
2123
2106
2106
2120

도면17


2200
100
2202
2204

도면18



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(74) 대리인	한양특허법인

심사청구 : 있음

(54) 전극 구동 장치 및 전자기기

요약

본 발명은 교차시키지 않고 복수의 배선을 배치시키는 것이 가능한 전극 구동 장치 및 전자기기를 제공한다.

전극 구동 장치는, 사변형 영역(20)내에 나열된 제1 ~ 3 전극 패턴(21 ~ 23)과, 제1 ~ 3 배선 패턴(31 ~ 33)과, 제1 ~ 3 단자(41 ~ 43)를 갖는다. 제3 배선 패턴(33)을 경계로 하여, 제1 배선 패턴(31)측에 제1 단자(41)가 배치되고, 제2 배선 패턴(32)측에 제2 단자(42)가 배치되어 있다. 제3 단자(43)는 제1 단자(41)와 제2 단자(42) 사이에 배치되어 있다.

대표도

도1

명세서

도면의 간단한 설명

도 1(a) ~ 1(b)는 제1 실시 형태의 전극 구동 장치를 나타내는 도면,

도 2는 제2 실시 형태의 전극 구동 장치를 나타내는 도면,

도 3은 제3 실시 형태의 전극 구동 장치를 나타내는 도면,

도 4는 제4 실시 형태의 전극 구동 장치를 나타내는 도면,

도 5는 제5 실시 형태의 전극 구동 장치를 나타내는 도면,

도 6은 실시 형태의 전자기기를 나타내는 도면,

도 7은 실시 형태의 전자기기를 나타내는 도면이다.

<도면의 주요부분에 대한 부호의 설명>

11 : 제1 기판	12 : 제2 기판
14 : 전기 광학 물질	20 : 사변형 영역
21 : 제1 전극 패턴	22 : 제2 전극 패턴
23 : 제3 전극 패턴	24 : 제1 변
25 : 정점	26 : 제2 변
31 : 제1 배선 패턴	32 : 제2 배선 패턴
33 : 제3 배선 패턴	34 : 제4 배선 패턴
40 : 전자부품	41 : 제1 단자
42 : 제2 단자	43 : 제3 단자
44 : 제4 단자	45 : 제5 단자(입력 단자)

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 전극 구동 장치 및 전자기기에 관한 것이다.

액티브 매트릭스 방식의 액정 표시장치에 있어서, 매트릭스 형상의 신호 전극 및 주사 전극이 제1 기판에 형성되고, 대향하는 제2 기판에 대향 전극이 형성되어 있다. 또, 신호 전극 및 주사 전극에 신호를 공급하는 배선이 제1 기판에 형성되고, 대향 전극에 신호를 공급하는 배선도 제1 기판에 형성되어 있다. 종래에 배선이 교차하는 경우가 있어, 그 경우 다층 기판을 사용하는 등의 조치가 필요했다. 이러한 문제는 액정 표시장치에 국한되지 않고, 복수의 배선을 배치할 때 발생할 수 있다.

발명이 이루고자 하는 기술적 과제

본 발명은 이러한 문제점을 해결하는 것으로, 그 목적은 교차시키지 않고 복수의 배선을 배치시키는 것이 가능한 전극 구동 장치 및 전자기기를 제공하는 것에 있다.

(1) 본 발명의 전극 구동 장치는, 사변형 영역 내에 나열된 제1 및 제2 전극 패턴과,

상기 제1 및 제2 전극 패턴이 형성된 제1 기판과,

상기 제1 전극 패턴에 전기적으로 접속되어 상기 사변형 영역의 제1 변으로부터 외측 방향으로 형성되어 이루어지는 제1 배선 패턴과,

상기 제2 전극 패턴에 전기적으로 접속되어 상기 사변형 영역의 상기 제1 변에 인접하는 제2 변으로부터 외측 방향으로 형성되어 이루어지는 제2 배선 패턴과,

상기 제1 및 제2 배선 패턴보다도 상기 제1 및 제2 변으로 형성되는 정점에 가까운 위치로부터 상기 사변형 영역의 외측 방향으로 형성되어 이루어지는 제3 배선 패턴과,

상기 제1 기판에 대향하는 제2 기판과,

상기 제2 기판에 형성되고, 상기 제3 배선 패턴에 전기적으로 접속된 제3 전극 패턴과,

상기 제1 배선 패턴에 전기적으로 접속된 제1 단자와, 상기 제2 배선 패턴에 전기적으로 접속된 제2 단자와, 상기 제3 배선 패턴에 전기적으로 접속된 제3 단자를 포함하는 적어도 하나의 전자부품을 갖고,

상기 제3 배선 패턴을 경계로 하여, 상기 제1 배선 패턴측에 상기 제1 단자가 배치되고, 상기 제2 배선 패턴측에 상기 제2 단자가 배치되고,

상기 제3 단자는 상기 제1 단자와 상기 제2 단자 사이에 배치되어 있다.

본 발명에 의하면, 제1, 제 2 및 제3 배선 패턴이 교차하지 않고 배치된다.

(2) 이 전극 구동 장치에 있어서,

상기 제1 및 제2 전극 패턴은 매트릭스 형상으로 형성되어 있어도 된다.

(3) 이 전극 구동 장치에 있어서,

상기 제1 기판에는 제3 기판이 부착되고,

상기 적어도 하나의 전자부품은 상기 제3 기판에 실장되고,

상기 제1, 제2 및 제3 배선 패턴은 상기 제1 기판 및 상기 제3 기판에 형성되어 있어도 된다.

(4) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은 상기 제1 기판에 실장되고,

상기 제1, 제2 및 제3 배선 패턴은 상기 제1 기판에 형성되어 있어도 된다.

(5) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은 상기 제1, 제2 및 제3 단자를 갖는 하나의 전자부품이어도 된다.

(6) 이 전극 구동 장치에 있어서,

상기 전자부품은 주변장치형 부품으로서, 배열순에서 상기 제1 및 제2 단자 사이에 상기 제3 단자가 배열되어 있어도 된다.

(7) 이 전극 구동 장치에 있어서,

상기 전자부품은 입력 단자를 갖고,

배열순에서 상기 제3 단자와 상기 입력 단자 사이에 상기 제2 단자가 배치되어 있어도 된다.

(8) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은, 상기 제1 단자가 설치된 제1 전자부품과, 상기 제2 단자가 설치된 제2

전자부품으로 이루어지고,

상기 제3 단자는 상기 제1 및 제2 전자부품의 한쪽에 설치되어 있어도 된다.

(9) 이 전극 구동 장치에 있어서,

상기 제1 변 옆에 상기 제1 전자부품이 배치되고,

상기 제1 변과 상기 제2 전자부품 사이에 상기 제1 전자부품이 배치되어 있어도 된다.

(10) 이 전극 구동 장치에 있어서,

상기 제1 및 제2 전자부품을 전기적으로 접속하는 접속 패턴을 또한 갖고,

상기 제2 배선 패턴과 상기 접속 패턴 사이에 상기 제3 배선 패턴이 배치되어 있어도 된다.

(11) 이 전극 구동 장치에 있어서,

상기 제2 전자부품은 입력 단자를 갖고,

상기 제3 단자와 상기 입력 단자 사이에 상기 제2 단자가 배치되어 있어도 된다.

(12) 이 전극 구동 장치에 있어서,

상기 제2 배선 패턴에 전기적으로 접속된 전자 회로를 더 구비하고 있어도 된다.

(13) 이 전극 구동 장치에 있어서,

상기 제3 배선 패턴에 전기적으로 접속된 전자 회로를 더 구비하고 있어도 된다.

(14) 이 전극 구동 장치에 있어서,

상기 제1 변의 양단에 인접하는 2개의 변의 각각이 상기 제2 변이며, 상기 제2 변으로부터 상기 제2 배선 패턴이 형성되어 있어도 된다.

(15) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은 상기 제1, 제2 및 제3 단자 중 적어도 하나로부터 출력하는 신호를 생성하는 기능을 갖고 있어도 된다.

(16) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은 입력된 신호를 상기 제1, 제2 및 제3 단자 중 적어도 하나에 통과시키는 경로를 갖고 있어도 된다.

(17) 이 전극 구동 장치에 있어서,

상기 경로는 상기 적어도 하나의 전자부품의 전원 전압보다도 높은 전압의 신호를 통과시키는 것이어도 된다.

(18) 이 전극 구동 장치에 있어서,

상기 전원 전압보다도 높은 전압의 신호는 공통 전압 V_{com}이어도 된다.

(19) 이 전극 구동 장치에 있어서,

상기 제3 배선 패턴이 형성된 상기 정점을 제외한 상기 사변형 영역의 모서리부로부터 인출되고, 상기 제3 전극 패턴에 전기적으로 접속되어 이루어지는 제4 배선 패턴과,

상기 적어도 하나의 전자부품에 설치되고, 상기 제4 배선 패턴에 전기적으로 접속되는 제4 단자를 더 갖고 있어도 된다.

(20) 이 전극 구동 장치에 있어서,

상기 제4 배선 패턴은 공통 전압 V_{com}을 공급하기 위한 것이어도 된다.

(21) 이 전극 구동 장치에 있어서,

상기 제3 및 제4 배선 패턴 사이에 상기 제2 배선 패턴이 배치되어 있어도 된다.

(22) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은 상기 제4 단자로부터 출력하는 신호를 생성하는 기능을 갖고 있어도 된다.

(23) 이 전극 구동 장치에 있어서,

상기 적어도 하나의 전자부품은 입력된 신호를 상기 제4 단자로 통과시키는 경로를 갖고 있어도 된다.

(24) 이 전극 구동 장치에 있어서,

상기 제3 배선 패턴은 공통 전압 V_{com}을 공급하기 위한 것이어도 된다.

(25) 이 전극 구동 장치에 있어서,

상기 제1 기판과 상기 제2 기판 사이에 전기 광학 물질이 설치되어 이루어져 전기 광학장치를 구성하여도 된다.

(26) 이 전극 구동 장치에 있어서,

상기 제1 기판과 상기 제2 기판 사이에 액정이 설치되어 이루어져 액정 장치를 구성해도 된다.

(27) 본 발명의 전자기기는 상기 전극 구동 장치를 갖는다.

발명의 구성 및 작용

이하, 본 발명의 실시 형태에 대해 도면을 참조하여 설명한다.

(제1 실시 형태)

도 1(a)는 제1 실시 형태의 전극 구동 장치를 나타내는 도면이며, 도 1(b)는 도 1(a)의 1B-1B선 단면도이다.

전극 구동 장치는 제1 기판(11)을 갖는다. 제1 기판(11)에 대향하여 제2 기판(12)이 설치되어 있다. 제1 및 제2 기판(11, 12)의 적어도 한쪽(한쪽만 또는 양쪽)은 유리 등으로 이루어지는 투명 기판이다. 제1 및 제2 기판(11, 12)은 적어도 표면에서 전기적으로 절연체로 형성되어 이루어진다. 제1 및 제2 기판(11, 12)의 형상은 도 1(a)에 도시하는 사변형(직사각형을 포함)에 한정되지 않는다. 본 실시 형태에서는 제1 기판(11)이 제2 기판(12)보다도 크다.

본 실시 형태에서, 전극 구동 장치는 제3 기판(13)을 갖는다. 제3 기판(13)은 제1 기판(11)에 접속되어 있다. 제3 기판(13)으로서 플렉시블 기판(필름)을 사용하여도 된다.

전극 구동 장치는 제1 전극 패턴(21)을 갖는다. 도 1(a)에 나타내는 제1 전극 패턴(21)은, 도면의 상하 방향으로 연장되는 복수의 전극으로 이루어진다. 액티브 매트릭스형의 액정 장치에서는, 제1 전극 패턴(21)은 신호 전극(또는 주사 전극)이다. 전극 구동 장치는 제2 전극 패턴(22)을 갖는다. 도 1(a)에 나타내는 제2 전극 패턴(22)은 도면의 좌우 방향으로 연장되는 복수의 전극으로 이루어진다. 액티브 매트릭스형의 액정 장치에 있어서는, 제2 전극 패턴(22)은 주사 전극(또는 신호 전극)이다. 또한, 액티브 매트릭스형 액정 장치는 도시하지 않은 화소 전극을 갖고, 주사 전극을 통해 제어되는 능동 소자(예를 들면, 트랜지스터)에 의해 신호 전극과 화소 전극의 전기적인 접속이 온·오프된다.

제1 및 제2 전극 패턴(21, 22)은 매트릭스 형상으로 형성되어 있어도 된다. 본 실시 형태에서는, 제1 및 제2 전극 패턴(21, 22)은 제1 기판(11)에 형성되어 있다. 제1 및 제2 전극 패턴(21, 22)은 사변형 영역(20)내에 나열되어 있다. 도 1(a)에 나타낸 예에서는, 사변형 영역(20)은 사변형의 제2 기판(12)의 외형에 의해 구획되는 영역이다.

전극 구동 장치는 제3 전극 패턴(23)을 갖는다. 제3 전극 패턴(23)은 제2 기판(12)에 형성되어 있다. 액티브 매트릭스형의 액정 장치에 있어서는, 제3 전극 패턴(23)은 공통 전극이다. 그 경우, 제3 전극 패턴(23)은 제2 기판(12)에서의 제1 기판(11)측의 면에 형성되어 있다.

본 실시 형태에서는, 전극 구동 장치는 전기 광학 장치(액정 장치·플라즈마 디스플레이 장치·전기장 발광(electroluminescence) 디스플레이 장치 등)로서, 제1 및 제2 기판(11, 12) 사이에 전기 광학 물질(액정·방전 가스·발광 재료 등)(14)이 형성되어 있다. 전기 광학 물질(14)은 도시하지 않은 실링재에 의해 밀봉된다. 전극 구동 장치는 전극 구동 패널이어도 된다. 전극 구동 패널은 전기 광학 패널(액정 패널·플라즈마 디스플레이 패널·전기장 발광 디스플레이 패널 등)이어도 된다.

전극 구동 장치는 제1 배선 패턴(31)을 갖는다. 제1 배선 패턴(31)은 복수의 배선으로 구성되어 있어도 된다. 제1 배선 패턴(31)은 제1 전극 패턴(21)에 전기적으로 접속되어 이루어진다. 제1 전극 패턴(21)을 구성하는 복수 전극의 각각에, 제1 배선 패턴(31)을 구성하는 복수의 배선 각각이 전기적으로 접속되어도 된다. 제1 전극 패턴 및 제1 배선 패턴(21, 31)은 일체 연속적으로 형성되어 있어도 된다. 제1 배선 패턴(31)은 사변형 영역(20)의 제1 변(24)으로부터 외측 방향으로 형성되어 있다.

전극 구동 장치는 제2 배선 패턴(32)을 갖는다. 제2 배선 패턴(32)은 복수의 배선으로 구성되어 있어도 된다. 제2 배선 패턴(32)은 제2 전극 패턴(22)에 전기적으로 접속되어 이루어진다. 제2 전극 패턴(22)을 구성하는 복수의 전극 각각에, 제2 배선 패턴(32)을 구성하는 복수의 배선 각각이 전기적으로 접속되어도 된다. 제2 전극 패턴 및 제2 배선 패턴(22, 32)은 일체 연속적으로 형성되어도 된다. 제2 배선 패턴(32)은 사변형 영역(20)의 제2 변(26)으로부터 외측 방향으로 형성되어 있다. 제2 변(26)은 제1 변(24)에 인접한다.

제2 배선 패턴(32)에는 전자 회로(36)가 전기적으로 접속되어 있다. 상세하게는, 제2 전극 패턴(22)과 제2 단자(42) 사이에 전자 회로(36)가 배치되어 있다. 전자 회로(36)는 제2 전극 패턴(예를 들면 주사 전극)(22)을 구동하는 것으로, Y 드라이버 또는 게이트 드라이버라 불리도 된다. 전자 회로(36)가 칩이면, 그 칩은 기판(도 1(a)의 예에서는 제1 기판(11))에 실장된다. 전자 회로(36)는 저온 폴리실리콘 등으로, 기판(도 1(a)의 예에서는 제1 기판(11)) 상에 형성하여도 된다.

제1 및 제2 변(24, 26)에 의해 형성되는 정점(25)으로부터, 또는 그 부근으로부터 제3 배선 패턴(33)이 형성되어 있다. 즉, 제3 배선 패턴(33)은 제1 및 제2 배선 패턴(31, 32)보다도 정점에 가까운 위치로부터 형성되어 있다. 제3 배선 패턴(33)은 사변형 영역(20)의 외측 방향으로 형성되어 있다. 도 1(a)에 나타내는 제3 배선 패턴(33)은 하나의 배선인데, 복수의 배선으로 구성되어 있어도 된다. 또, 제3 배선 패턴(33)은 도전부(16)를 통해 제3 전극 패턴(23)에 전기적으로 접속되어 있다.

제1 ~ 제3 배선 패턴(31 ~ 33)은 교차하지 않고 배치되어 있다. 또, 제1 및 제3 배선 패턴(31, 33) 사이에 제2 배선 패턴(32)이 배치되어 있다.

본 실시 형태에서는 상술한 정점(25)을 제외한 사변형 영역(20)의 모서리부로부터 제4 배선 패턴(34)이 형성되어 있다. 여기서, 모서리부란 사변형 영역(20)의 모서리 및 그 부근을 포함한다. 제4 배선 패턴(34)은 사변형 영역(20)의 외측 방향으로 형성되어 있다. 도 1(a)에 나타내는 제4 배선 패턴(34)은 하나

의 배선인데, 복수의 배선으로 구성되어 있어도 된다. 또, 제4 배선 패턴(34)은 도전부(18)를 통해 제3 전극 패턴(23)에 전기적으로 접속되어 있다.

제1 ~ 제4 배선 패턴(31 ~ 34)은 제1 기판(11)에 형성되어 있다. 본 실시 형태에서는 제1 ~ 제4 배선 패턴(31 ~ 34)은 제3 기판에도 형성되어 있다. 예를 들면, 제1 기판(11)에 형성된 복수의 배선 패턴과, 제3 기판(13)에 형성된 복수의 배선 패턴이 접합되어, 제1 ~ 제4 배선 패턴(31 ~ 34)이 구성되어도 된다. 그 접합에는 금속 접합을 적용해도 되고, 이방성 도전 재료를 사용해도 된다.

본 실시 형태에서는 제5 배선 패턴(35)을 갖는다. 제5 배선 패턴(35)은 후술하는 전자부품(40)과 외부를 전기적으로 접속하는 것이다. 제5 배선 패턴(35)은 제3 기판(13)에 형성되어 있다.

본 실시 형태에서는 제1 기판(11)에 제6 배선 패턴(37)이 형성되어 있다. 제6 배선 패턴(37)은 제4 배선 패턴(34)과 전기적으로 접속되어 있다. 또, 제6 배선 패턴(37)은 도전부(17, 19)를 통해 제3 전극 패턴(23)에 전기적으로 접속되어 있다. 도전부(17, 19)는 도전부(16, 18)와 동일한 구성이어도 된다. 도 1에 나타낸 예에서는, 사변형 영역(20)의 4개의 모서리부에 도전부(16 ~ 19)가 형성되어 있고, 4개의 모서리부로부터 제3 전극 패턴(23) 전체에 공통 전압 V_{com}을 공급할 수 있다. 이것에 의하면, 제3 전극 패턴(23)의 전압을 신속하게 변화시킬 수 있고, 전압의 균일성도 높아진다.

전극 구동 장치는 적어도 하나의(도 1(a)의 예에서는 하나의) 전자부품(40)을 갖는다. 전자부품(40)은 제1 전극 패턴(예를 들면 신호 전극)(21)을 구동하고, X 드라이버 또는 소오스 드라이버라 불러도 된다. 본 실시 형태에서는, 전자부품(40)은 전자 회로(36)를 제어하는 기능을 갖는다. 이러한 컨트롤러로서의 기능 외에, 전자부품(40)은, RAM, 전원 회로, 발신 회로 등을 내장하고 있다.

도 1(a)에 나타낸 전자부품(40)은 주변장치형 부품으로서, 단부에 복수의 단자가 나열되어 있다. 전자부품(40)은 제1 변(24) 옆에 배치되어 있다. 본 실시 형태에서는, 전자부품(40)은 제3 기판(13)에 실장되어 있다. 전자부품(40)의 실장 형태는 TAB(Tape Automated Bonding)이어도 되고, 페이스-다운 실장이어도 된다. 실장 대상이 되는 기판(도 1(a)의 예에서는 제3 기판(13))이 필름이면 COF(Chip On Film)라고 불리고, 유리이면 COG(Chip On Glass)라고 불린다. 전자부품(40)과 기판(도 1(a)의 예에서는 제3 기판(13))으로 TCP(Tape Carrier Package)를 구성하여도 된다.

전자부품(40)은 적어도 하나(도 1(a)의 예에서는 복수)의 제1 단자(41)를 갖는다. 제1 단자(41)는 제1 배선 패턴(31)과 전기적으로 접속되어 있다. 전자부품(40)은 적어도 하나(도 1(a)의 예에서는 복수)의 제2 단자(42)를 갖는다. 제2 단자(42)는 제2 배선 패턴(32)과 전기적으로 접속되어 있다. 전자부품(40)은 적어도 하나(도 1(a)의 예에서는 하나이거나 복수이어도 된다)의 제3 단자(43)를 갖는다. 제3 단자(43)는 제3 배선 패턴(33)과 전기적으로 접속되어 있다.

전자부품(40)은 적어도 하나(도 1(a)의 예에서는 하나이거나 복수이어도 된다)의 제4 단자(44)를 갖는다. 제4 단자(44)는 제4 배선 패턴(34)과 전기적으로 접속되어 있다. 전자부품(40)은 적어도 하나(도 1(a)의 예에서는 복수)의 제5 단자(입력 단자)(45)를 갖는다. 제5 단자(입력 단자)(45)는 제5 배선 패턴(35)과 전기적으로 접속되어 있다.

전자부품(40)은 제1 ~ 제4 단자(41 ~ 44) 중 적어도 하나로부터 출력하는 신호를 생성하는 기능을 갖는다. 예를 들면, 전자부품(40)은 제3 전극 패턴(공통 전극)(23)에 인가하는 (공통 전압 V_{com})를 생성하고, 제3 단자(43)로부터 출력한다. 도 1에 나타낸 예에서는, 공통 전압 V_{com}은 제4 단자(44)로부터도 출력되고, 제4 배선 패턴(34)을 통해 제3 전극 패턴(23)에 인가된다. 제4 패턴(34)에는 제6 배선 패턴(37)이 전기적으로 접속되어 있으므로, 제6 배선 패턴(37)으로부터도 공통 전압 V_{com}은 제3 전극 패턴(23)에 인가된다.

본 실시 형태에서는, 배열순에서 제1 및 제2 단자(41, 42) 사이에 제3 단자(43)가 배치되어 있다. 또, 배열순에서 제3 단자(43)와 제5 단자(입력 단자)(45) 사이에 제2 단자(42)가 배치되어 있다. 또, 제1 단자(41)는 제3 배선 패턴(33)보다도 제1 배선 패턴(31)측에 배치되어 있다. 제2 단자(42)는 제3 배선 패턴(33)보다도 제2 배선 패턴(32)측에 배치되어 있다. 제3 단자(43)는 제1 및 제2 단자(41, 42) 사이에 배치되어 있다.

이러한 배열로 되어 있으므로, 본 실시 형태에 의하면 제3 배선 패턴(33)을 제1 및 제2 배선 패턴(31, 32)과 교차하지 않도록 배치할 수 있다.

다음으로, 본 실시 형태의 전극 구동 장치의 동작을 설명한다. 제5 배선 패턴(35)으로부터 제5 단자(45)에 복수의 신호(전압)가 입력된다. 전자부품(40)에서 입력 신호가 RAM에 기억되고, 필요한 전압이나 신호가 생성된다. 그리고, 제1 단자(41)로부터 출력되는 신호에 의해, 제1 배선 패턴(31)을 통해 제1 전극 패턴(신호 전극)(21)이 구동된다. 또, 제2 단자(42)로부터 출력되는 신호에 의해, 전자 회로(36)를 제어하고, 전자 회로(36)는 제2 전극 패턴(주사 전극)(22)을 구동한다. 제2 단자(42)로부터는 전자 회로(36)에 대해 전원도 공급한다. 제3 단자(43)로부터 출력되는 전압(공통 전압 V_{com})은 제3 배선 패턴(33)을 통해 제3 전극 패턴(23)에 인가된다. 제4 단자(44)로부터 출력되는 전압(공통 전압 V_{com})은 제4 배선 패턴(34)을 통해 제3 전극 패턴(23)에 인가된다.

(제2 실시 형태)

도 2는 제2 실시 형태의 전극 구동 장치를 나타내는 도면이다. 본 실시 형태는 제1 실시 형태의 변형례이며, 동일한 구성에 대해서는 설명을 생략한다. 본 실시 형태의 전극 구동 장치는 전자부품(50)을 갖는다. 전자부품(50)은 입력된 신호를 제1 ~ 제4 단자(51 ~ 54) 중 적어도 하나에 통과시키는 경로(56)를 갖는다. 여기서, 신호란 전압이나 전원을 포함하고, 공통 전압 V_{com}이어도 된다. 경로(56)는 전자부품(50)의 전원 전압(예를 들면, 1.8V, 3V)보다도 높은 전압의 신호를 통과할 수 있도록, 고 내압의 회로 레이아웃 또는 배선 레이아웃으로 하여도 된다. 이에 의해, 경로(56)는 공통 전압 V_{com}(예를 들면, -1.0 ~ 4.0V, 진폭 5V)과 같은 신호도 통과시킬 수 있다. 도 2에 나타낸 예에서는, 복수 중 하나의 제5 단자

(55)는 경로(56)에 의해 제3 및 제4 단자(53, 54)에 전기적으로 접속되어 있다. 경로(56)는 능동 소자를 갖고 있지 않은 배선이다. 이렇게 전자부품(50)의 내부를 신호가 통과할 수 있음으로써, 제3 배선 패턴(33)을 제1 또는 제2 배선 패턴(31, 62)과 교차시키지 않고 배치할 수 있다.

본 실시 형태의 전극 구동 장치는 전자 회로(68)를 갖는다. 전자 회로(68)는 필요한 전압 또는 전원을 생성하는 전원 회로이다. 전자 회로(68)는 제2 배선 패턴(62)에 전기적으로 접속되어 전자 회로(36)에 전원을 공급한다. 또, 전자 회로(68)는 전자부품(50)의 제5 단자(55)에 전기적으로 접속되어 있다. 그리고, 전자 회로(68)로부터 공급된 전원은, 상술한 경로(56)를 통해 전자부품(50)의 외부(도 2의 예에서는, 제3 및 제4 배선 패턴(33, 34)을 통해 제3 전극 패턴(23)(도 1(a) 참조))에 공급된다.

(제3 실시 형태)

도 3은 제3 실시 형태의 전극 구동 장치를 나타내는 도면이다. 본 실시 형태는 제1 및 제2 실시 형태의 변형례이며, 동일 구성에 대해서는 설명을 생략한다. 본 실시 형태의 전극 구동 장치는, 전자부품(70)을 갖는다. 전자부품(70)은 입력된 신호를 제1 ~ 제4 단자(71 ~ 74) 중 적어도 하나에 통과시키는 경로(76, 78)를 갖는다. 여기서 신호란 전압이나 전원을 포함하고, 공통 전압 V_{com}이어도 된다. 경로(76, 78)는 전자부품(70)의 전원 전압(예를 들면, 1.8V, 3V)보다도 높은 전압의 신호를 통과할 수 있도록, 고내압의 회로 레이아웃 또는 배선 레이아웃으로 하여도 된다. 이에 의해, 경로(76, 78)는 공통 전압 V_{com}(예를 들면, -1.0 ~ 4.0V, 진폭 5V)과 같은 신호도 통과시킬 수 있다. 도 3에 나타내는 예에서는, 제5 단자(75)는 경로(76)에 의해 제2 단자(72)에 전기적으로 접속되어 있다. 경로(72)는 능동 소자를 갖고 있지 않은 배선이다. 제2 단자(72)는 제2 배선 패턴(82)에 전기적으로 접속되어 있다. 또한, 제2 배선 패턴(82)에는 제2 단자(72)와 전자 회로(36) 사이에 전자 회로(68)가 전기적으로 접속되어 있다.

또, 제3 단자(73)는 경로(78)에 의해 제4 단자(74)에 전기적으로 접속되어 있다. 경로(78)는 능동 소자를 갖고 있지 않은 배선이다. 제3 단자(73)는 제3 배선 패턴(83)에 전기적으로 접속되고, 제4 단자(74)는 제4 배선 패턴(34)에 전기적으로 접속되어 있다. 또한, 제3 배선 패턴(83)은 전자 회로(68)에도 전기적으로 접속되어 있다.

전자부품(80)의 경로(76, 78)에 의해 전자부품(70)의 내부를 신호가 통과할 수 있다. 따라서, 제3 또는 제4 배선 패턴(83, 84)을 제1 또는 제2 배선 패턴(81, 82)과 교차시키지 않고 배치할 수 있다.

전자 회로(68)는 필요한 전압 또는 전원을 생성하는 전원 회로이다. 전자 회로(68)는 제2 배선 패턴(82)에 전기적으로 접속되어 전자 회로(36)에 전원을 공급한다. 또, 전자 회로(68)는 제3 배선 패턴(83)에 전기적으로 접속되어 전원을 공급할 수 있도록 되어 있다. 또, 제3 배선 패턴(83)은 제3 단자(73)에 전기적으로 접속되고, 전자 회로(68)로부터 공급된 전원은 상술한 경로(78)를 통해 전자부품(70)의 외부(도 3의 예에서는 제4 배선 패턴(34)을 통해 제3 전극 패턴(23)(도 1(a) 참조))에 공급된다.

(제4 실시 형태)

도 4는 제4 실시 형태의 전극 구동 장치를 나타내는 도면이다. 전극 구동 장치는 제1 및 제2 기판(111, 112)(제1 실시 형태에서 설명한 제1 및 제2 기판(11, 12)의 내용이 해당한다)을 갖는다. 본 실시 형태에서도 제2 기판(112)의 외형에 의해 형성되는 사변형 영역(120) 내에 도시 생략한 제1 및 제2 전극 패턴이 나열되어 있다. 제1 기판(111)에는 제3 기판(113)(제1 실시 형태에서 설명한 제3 기판(13)의 내용이 해당한다)이 부착되어 있다.

전극 구동 장치는 제1 및 제2 전자부품(140, 150)을 갖는다. 도 4에 나타내는 제1 및 제2 전자부품(140, 150)은 제3 기판(113)에 실장되어 있다. 실장 형태는 제1 실시 형태에서 설명했다. 사변형 영역(120)의 제1 변(124) 옆에 제1 부품(140)이 배치되어 있다. 그리고, 제1 변(120)과 제2 부품(150) 사이에 제1 부품(140)이 배치되어 있다.

제1 및 제2 전자부품(140, 150)은 모두 주변장치형 부품으로서, 단부에 복수이 단자가 나열되어 있다. 제1 전자부품(140)은 제1 단자(141)(제1 실시 형태에서 설명한 제1 단자(41)의 내용이 해당한다)를 갖는다. 제2 전자부품(150)은 제2 단자(152)(제1 실시 형태에서 설명한 제3 단자(42)의 내용이 해당한다)를 갖는다. 제3 단자(153)(제1 실시 형태에서 설명한 제3 단자(43)의 내용이 해당한다)는 제1 및 제2 전자부품(140, 150)의 한쪽(도 4의 예에서는 제2 전자부품(150))에 설치되어 있다. 또, 제1 및 제2 전자부품(140, 150)의 한쪽(도 4의 예에서는 제2 전자부품(150))은, 제4 및 제5 단자(154, 155)(제1 실시 형태에서 설명한 제4 및 제5 단자(154, 155)의 내용이 해당한다)를 갖는다. 또한, 제5 단자(155)는 입력 단자이다. 또한, 제1 및 제2 전자부품(140, 150)은 각각 제6 단자(146, 156)를 갖는다.

제1 변(124)으로부터 형성된 제1 배선 패턴(131)(제1 실시 형태에서 설명한 제1 배선 패턴(31)의 내용이 해당한다)은 제1 단자(141)에 전기적으로 접속되어 있다.

제2 변(126)으로부터 형성된 제2 배선 패턴(132)(제1 실시 형태에서 설명한 제2 배선 패턴(32)의 내용이 해당한다)은 제2 단자(152)에 전기적으로 접속되어 있다. 본 실시 형태에서는, 제1 변(124)의 양단에 인접하는 2개의 제2 변(126)의 각각으로부터 제2 배선 패턴(132)이 형성되어 있다.

본 실시 형태에서는, 제1 변(124)과 2개의 제2 변(126)에 의해 2개의 정점이 형성된다. 그 2개의 정점의 각각에 가까운 위치로부터, 제3 배선 패턴(133)이 형성되어 있다. 이 이외의 점에서는 제3 배선 패턴(133)에는 제1 실시 형태에서 설명한 제3 배선 패턴(33)의 내용이 해당한다.

본 실시 형태에서, 제4 배선 패턴(134)은 제2 배선 패턴(132)보다도 제2 변(126)에서의 제1 변(124)과는 반대측의 선단에 가까운 위치(모서리부)로부터 형성되어 있다. 또, 2개의 제2 변(126)에 대응하여 2개의 제4 배선 패턴(134)이 형성되어 있다.

본 실시 형태의 전극 구동 장치는, 제5 배선 패턴(135)(제1 실시 형태에서 설명한 제5 배선 패턴(35)의 내용이 해당한다)를 갖는다. 또, 제1 및 제2 전자부품(140, 150)의 제6 단자(146, 156)를 전기적으로 접속하는 제6 배선 패턴(접속 패턴)(136)이 형성되어 있다.

제1 전자부품(140)에 있어서, 제1 단자(141)는 제1 변(124)측의 단부에 설치되어 있다. 또, 제1 단자(141)는 제6 단자(146)와는 반대측의 단부에 설치되어 있다.

제2 전자부품(150)에서는, 배열순에서 제2 단자(152)는 제3 단자(153)와 제5 단자(입력 단자)(135) 사이에 설치되어 있다. 배열순에서 제6 단자(156)와 제2 단자(152) 사이에, 제3 단자(153)가 설치되어 있다. 배열순에서 제3 단자(153)와 제4 단자(154) 사이에 제2 단자(152)가 설치되어 있다.

본 실시 형태에서, 제3 배선 패턴(133)은 제2 배선 패턴(132)과 제6 배선 패턴(접속 패턴)(136) 사이에 형성되어 있다. 따라서, 제3 배선 패턴(133)을 제2 배선 패턴(132)과 교차시키지 않도록 형성할 수 있다. 또, 제2 배선 패턴(132)이 제3 및 제4 배선 패턴(133, 134) 사이에 형성되어 있다. 따라서, 제4 배선 패턴(134)을 제2 배선 패턴(132)과 교차시키지 않도록 형성할 수 있다.

기타 내용에 대해서는 제1 실시 형태에서 설명한 내용이 해당한다. 예를 들면, 제1 단자(141)는 제3 배선 패턴(133)보다도 제1 배선 패턴(131)측에 배치되어 있다. 제2 단자(152)는 제3 배선 패턴(133)보다도 제2 배선 패턴(132)측에 배치되어 있다. 제3 단자(153)는 제1 및 제2 단자(141, 152) 사이에 배치되어 있다. 환언하면, 제3 단자(153)를 통과하는 도시 생략한 선(제3 배선 패턴(133)이어도 된다)을 경계로 하여, 한쪽 측에 제1 단자(141)가 배치되고, 다른쪽 측에 제2 단자(152)가 배치되어 있다. 본 실시 형태에 의하면, 상술한 구성을 가지므로, 교차시키지 않고 복수의 배선을 형성할 수 있다.

(제5 실시 형태)

도 5는 제5 실시 형태의 전극 구동 장치를 나타내는 도면이다. 본 실시 형태에서는, 전자부품(240)이 제1 기판(211)(제1 실시 형태에서 설명한 제1 기판(11)의 내용이 해당한다)에 실장되어 있다(C08). 또, 제1 ~ 제3 배선 패턴(231 ~ 233)도 제1 기판(211)에 형성되어 있다.

전자부품(240)은 제1 ~ 제5 단자(241 ~ 245)를 갖는 점에서, 제1 실시 형태에서 설명한 전자부품(40)의 내용이 해당한다. 또, 전자부품(240)의 제3 및 제4 단자(243, 244)에 대해 제4 실시 형태에서 설명한 제2 전자부품(150)의 제3 및 제4 단자(153, 154)의 내용이 해당한다. 즉, 도 5에 나타내는 전자부품(240)은 도 4에 나타내는 제2 전자부품(140)으로부터 제6 단자(156)를 제거하고, 그 대신에 제1 단자(241)를 설치한 구성을 갖는다.

제1 ~ 제5 배선 패턴(231 ~ 235)은 제4 실시 형태에서 설명한 제1 ~ 제5 배선 패턴(131 ~ 135)의 내용이 해당한다. 단, 제1 배선 패턴(231)도 전자부품(240)에 전기적으로 접속되어 있다. 본 실시 형태에는 상기 어느 한 실시 형태에서 설명한 내용을 적용할 수 있다. 본 실시 형태에서도 복수의 배선을 교차시키지 않고 형성할 수 있다. 또한, 본 실시 형태에서는, 제1 기판(211)에 전자부품(240)이 실장되어 있으나, 제3 기판을 설치하고, 이 제3 기판에 전자부품(240)을 실장하여도 된다. 상세하게는, 제1 실시 형태에서 설명하였다.

상술한 어느 한 실시 형태의 전극 구동 장치를 갖는 전자기기로서, 도 6에는 노트북형 퍼스널 컴퓨터(1000)가 도시되고, 도 7에는 휴대 전화(2000)가 도시되어 있다.

본 발명은, 상술한 실시 형태에 한정되지 않고, 여러 가지 변형이 가능하다. 예를 들면, 본 발명은 실시 형태에서 설명한 구성과 실질적으로 동일한 구성(예를 들면, 기능, 방법 및 결과가 동일한 구성, 또는 목적 및 결과가 동일한 구성)을 포함한다. 또, 본 발명은 실시 형태에서 설명한 구성의 본질적이지 않은 부분을 치환한 구성을 포함한다. 또, 본 발명은 실시 형태에서 설명한 구성과 동일한 작용 효과를 나타내는 구성 또는 동일한 목적을 달성할 수 있는 구성을 포함한다. 또, 본 발명은 실시 형태에서 설명한 구성에 공지 기술을 부가한 구성을 포함한다.

발명의 효과

본 발명에 의하면, 교차시키지 않고 복수의 배선을 배치시킬 수 있다.

(57) 청구의 범위

청구항 1

사변형 영역 내에 나열된 제1 및 제2 전극 패턴과,

상기 제1 및 제2 전극 패턴이 형성된 제1 기판과,

상기 제1 전극 패턴에 전기적으로 접속되어 상기 사변형 영역의 제1 변으로부터 외측 방향으로 형성되어 이루어지는 제1 배선 패턴과,

상기 제2 전극 패턴에 전기적으로 접속되어 상기 사변형 영역의 상기 제1 변에 인접하는 제2 변으로부터 외측 방향으로 형성되어 이루어지는 제2 배선 패턴과,

상기 제1 및 제2 배선 패턴보다도 상기 제1 및 제2 변으로 형성되는 정점에 가까운 위치로부터 상기 사변형 영역의 외측 방향으로 형성되어 이루어지는 제3 배선 패턴과,

상기 제1 기판에 대향하는 제2 기판과,

상기 제2 기판에 형성되고, 상기 제3 배선 패턴에 전기적으로 접속된 제3 전극 패턴과,

상기 제1 배선 패턴에 전기적으로 접속된 제1 단자와, 상기 제2 배선 패턴에 전기적으로 접속된 제2 단자와, 상기 제3 배선 패턴에 전기적으로 접속된 제3 단자를 포함하는 적어도 하나의 전자부품을 갖고,

상기 제3 배선 패턴을 경계로 하여, 상기 제1 배선 패턴측에 상기 제1 단자가 배치되고, 상기 제2 배선 패턴측에 상기 제2 단자가 배치되고,

상기 제3 단자는 상기 제1 단자와 상기 제2 단자 사이에 배치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 2

제1항에 있어서,

상기 제1 및 제2 전극 패턴은 매트릭스 형상으로 형성되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 3

제1항 또는 제2항에 있어서,

상기 제1 기판에는 제3 기판이 부착되고,

상기 적어도 하나의 전자부품은 상기 제3 기판에 실장되고,

상기 제1, 제2 및 제3 배선 패턴은 상기 제1 기판 및 상기 제3 기판에 형성되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 4

제1항 또는 제2항에 있어서,

상기 적어도 하나의 전자부품은 상기 제1 기판에 실장되고,

상기 제1, 제2 및 제3 배선 패턴은 상기 제1 기판에 형성되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 5

제1항 또는 제2항에 있어서,

상기 적어도 하나의 전자부품은 상기 제1, 제2 및 제3 단자를 갖는 하나의 전자부품인 것을 특징으로 하는 전극 구동 장치.

청구항 6

제5항에 있어서,

상기 전자부품은 주변장치형 부품으로서, 배열순에서 상기 제1 및 제2 단자 사이에 상기 제3 단자가 배열되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 7

제6항에 있어서,

상기 전자부품은 입력 단자를 갖고,

배열순에서 상기 제3 단자와 상기 입력 단자 사이에 상기 제2 단자가 배치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 8

제1항 또는 제2항에 있어서,

상기 적어도 하나의 전자부품은, 상기 제1 단자가 설치된 제1 전자부품과, 상기 제2 단자가 설치된 제2 전자부품으로 이루어지고,

상기 제3 단자는 상기 제1 및 제2 전자부품의 한쪽에 설치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 9

제8항에 있어서,

상기 제1 변 옆에 상기 제1 전자부품이 배치되고,

상기 제1 변과 상기 제2 전자부품 사이에 상기 제1 전자부품이 배치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 10

제9항에 있어서,

상기 제1 및 제2 전자부품을 전기적으로 접속하는 접속 패턴을 또한 갖고,

상기 제2 배선 패턴과 상기 접속 패턴 사이에 상기 제3 배선 패턴이 배치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 11

제9항에 있어서,

상기 제2 전자부품은 입력 단자를 갖고,

상기 제3 단자와 상기 입력 단자 사이에 상기 제2 단자가 배치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 12

제1항 또는 제2항에 있어서,

상기 제2 배선 패턴에 전기적으로 접속된 전자 회로를 더 구비하여 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 13

제1항 또는 제2항에 있어서,

상기 제3 배선 패턴에 전기적으로 접속된 전자 회로를 더 구비하여 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 14

제1항 또는 제2항에 있어서,

상기 제1 변의 양단에 인접하는 2개의 변의 각각이 상기 제2 변이며, 상기 제2 변으로부터 상기 제2 배선 패턴이 형성되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 15

제1항 또는 제2항에 있어서,

상기 적어도 하나의 전자부품은 상기 제1, 제2 및 제3 단자 중 적어도 하나로부터 출력하는 신호를 생성하는 것을 특징으로 하는 전극 구동 장치.

청구항 16

제1항 또는 제2항에 있어서,

상기 적어도 하나의 전자부품은 입력된 신호를 상기 제1, 제2 및 제3 단자 중 적어도 하나에 통과시키는 경로를 갖는 것을 특징으로 하는 전극 구동 장치.

청구항 17

제16항에 있어서,

상기 경로는 상기 적어도 하나의 전자부품의 전원 전압보다도 높은 전압의 신호를 통과시키는 것임을 특징으로 하는 전극 구동 장치.

청구항 18

제17항에 있어서,

상기 전원 전압보다도 높은 전압의 신호는 공통 전압 V_{com}인 것을 특징으로 하는 전극 구동 장치.

청구항 19

제1항 또는 제2항에 있어서,

상기 제3 배선 패턴이 형성된 상기 정점을 제외한 상기 사변형 영역의 모서리부로부터 인출되고, 상기 제3 전극 패턴에 전기적으로 접속되어 이루어지는 제4 배선 패턴과,

상기 적어도 하나의 전자부품에 설치되고, 상기 제4 배선 패턴에 전기적으로 접속되는 제4 단자를 더 갖는 것을 특징으로 하는 전극 구동 장치.

청구항 20

제19항에 있어서,

상기 제4 배선 패턴은 공통 전압 V_{com}을 공급하기 위한 것임을 특징으로 하는 전극 구동 장치.

청구항 21

제19항에 있어서,

상기 제3 및 제4 배선 패턴 사이에 상기 제2 배선 패턴이 배치되어 이루어지는 것을 특징으로 하는 전극 구동 장치.

청구항 22

제19항에 있어서,

상기 적어도 하나의 전자부품은 상기 제4 단자로부터 출력하는 신호를 생성하는 기능을 갖는 것을 특징으로 하는 전극 구동 장치.

청구항 23

제19항에 있어서,

상기 적어도 하나의 전자부품은 입력된 신호를 상기 제4 단자로 통과시키는 경로를 갖는 것을 특징으로 하는 전극 구동 장치.

청구항 24

제1항 또는 제2항에 있어서,

상기 제3 배선 패턴은 공통 전압 V_{com}을 공급하기 위한 것임을 특징으로 하는 전극 구동 장치.

청구항 25

제1항 또는 제2항에 있어서,

상기 제1 기판과 상기 제2 기판 사이에 전기 광학 물질이 설치되어 이루어져 전기 광학 장치를 구성하는 것을 특징으로 하는 전극 구동 장치.

청구항 26

제1항 또는 제2항에 있어서,

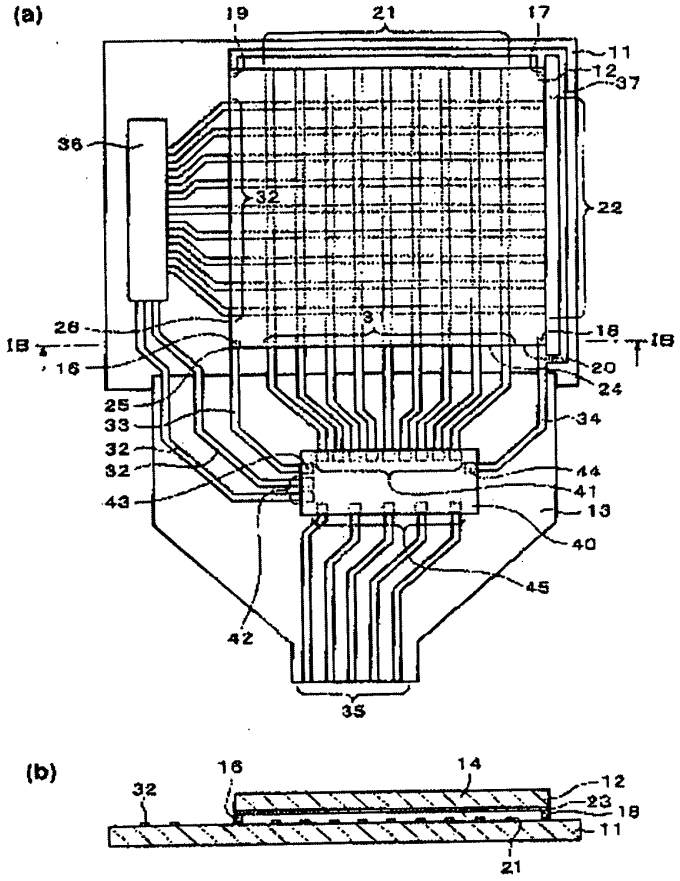
상기 제1 기판과 상기 제2 기판 사이에 액정이 설치되어 이루어져 액정 장치를 구성하는 것을 특징으로 하는 전극 구동 장치.

청구항 27

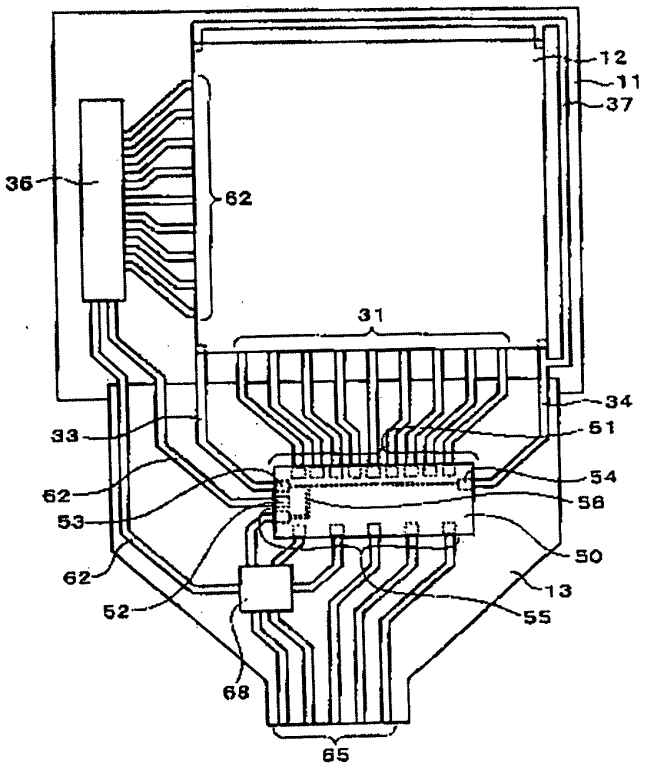
제25항에 기재된 전극 구동 장치를 갖는 것을 특징으로 하는 전자기기.

도면

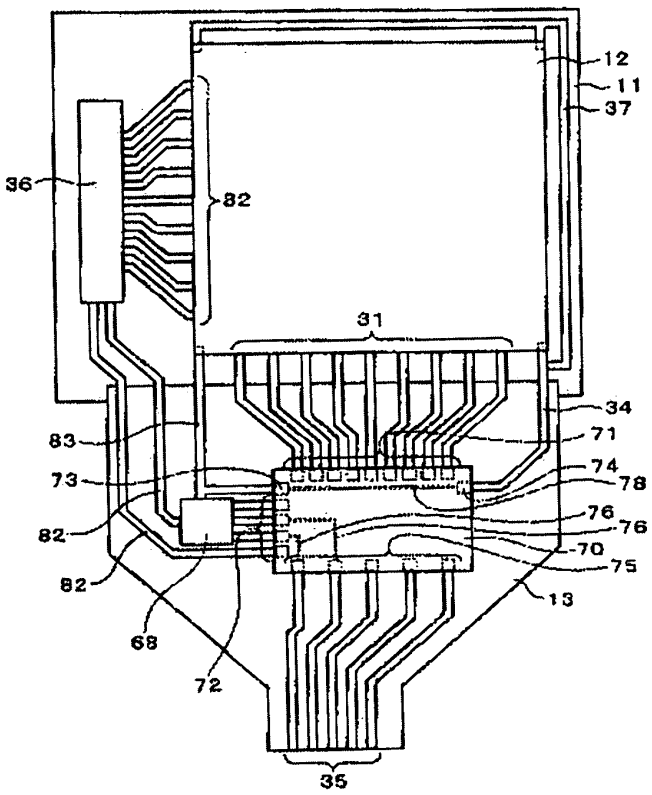
도면1


(a)
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(b)
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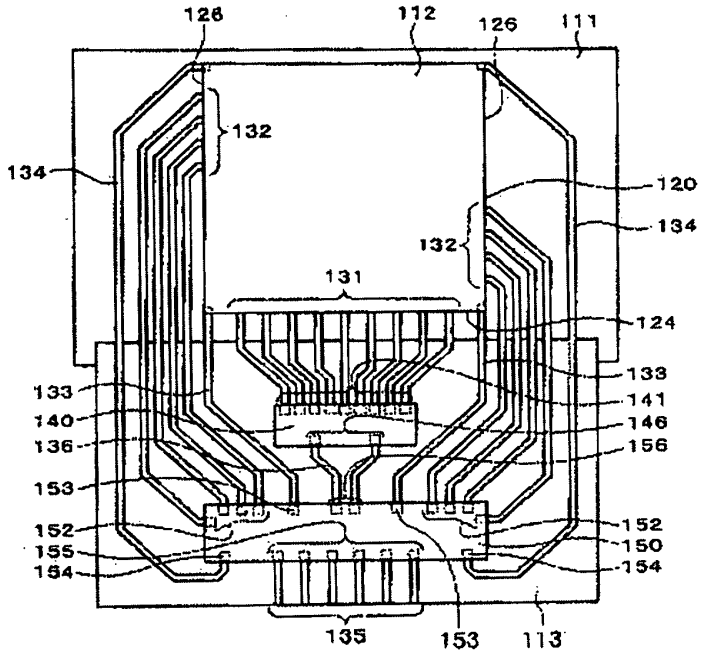
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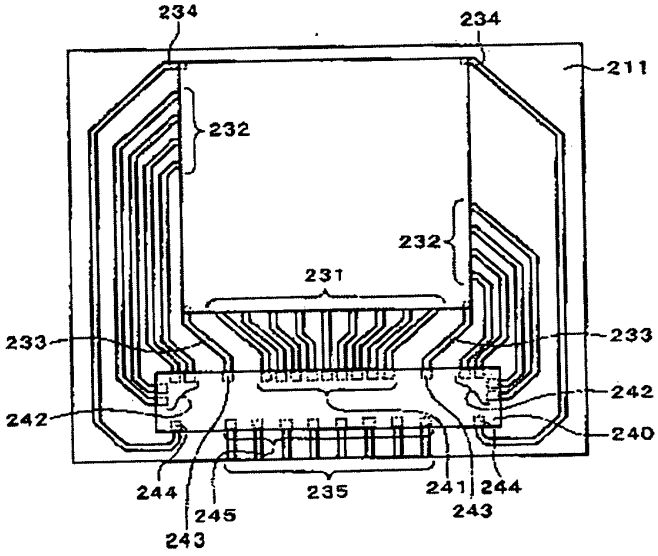
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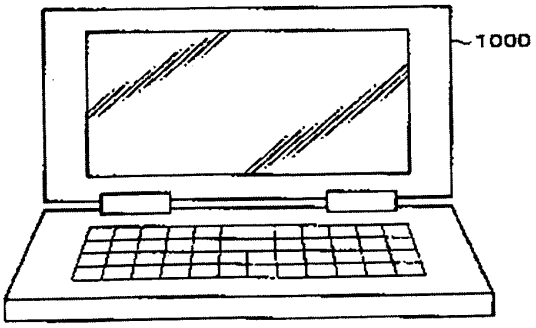
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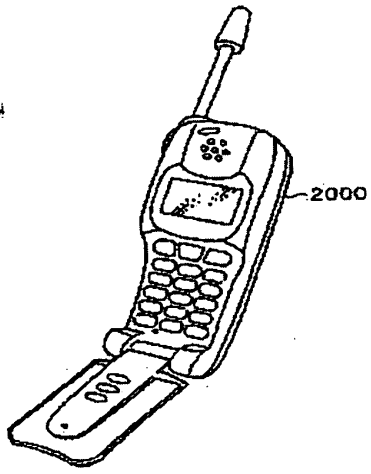
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/852,255	05/25/2004	Masao Murade	119570	4122

25944 7590 11/15/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
NGUYEN, THANH NHAN P	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/852,255	MURADE, MASAO	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P. Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/04;9/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because of the minor informalities such as in fig. 7, element '7' should be changed to '70' to match with description in specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 2, the "sub-wiring lines" with its first and second portions must be shown and labeled or the feature(s) canceled from the claim(s). Similarly, the features discloses in claim 6, start

from "the counter electrode potential line... a part of the peripheral driving circuits... in the peripheral region" must be shown and labeled or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claim 14 is objected to because of the following informalities: Claim 14 currently read as "... according to claim 12..." It should have been read as "... according to claim 13..." since "the image signal wiring lines" was not introduced earlier in claim 12, but 13.

2. Claim 4 and 6 are objected to because of the following informalities: in the second limitation in the claim (4 and 6), after "which is at least... wiring lines", "and the counter electrode" seems to be extra, and therefore, for the examination purpose, "and the counter electrode" has been crossed out.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 10, 11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Muraide JP 2002-049052.

Referring to claim 1, Muraide discloses an electro-optical device, comprising: a plurality of pixel portions provided in an image display region (10a) on an element substrate (10); in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals (102), a plurality of main wiring lines (400) each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits (101 or 104) coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines, the plurality of main wiring lines being made of a same conductive

film and being planarly laid out so as not to intersect each other in the peripheral region, [see figs. 4 & 11].

Referring to claims 2 and 3, Muraide discloses sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines (305) being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region; wherein the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film, [see fig. 4].

Referring to claim 10, Muraide discloses the plurality of main wiring lines (400) including a pair of clock signal lines (CLX, CLY) that supply a clock signal (CLX, CLY) and an inverse signal thereof (CLX', CLY') as electric signals and power source wiring lines that supply power source signals as electric signals, and the pair of signal lines and power source wiring lines do not intersect each other, [see fig. 4].

Referring to claim 11, Muraide discloses the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other, [see fig. 4].

Referring to claim 13, Muraide discloses a electro-optical device, comprising: a plurality of pixel portions provided in an image display region (10a) on an element substrate (10); a plurality of external circuit connection terminals (102) provided in a peripheral region of the image display region on the element substrate; scanning line driving circuits (104); a data line driving circuit (101); scanning line driving circuit wiring lines each having one end coupled to each of the external circuit connection terminals and having the other ends coupled to the scanning line driving circuits; data line driving circuit wiring lines each having one end coupled to each of the external circuit connection terminals and having the other ends coupled to the data line driving circuit; and image signal wiring lines each having one end coupled to each of the external circuit connection terminals, the image signal wiring lines supplying image signals of the plurality of pixel portions, the scanning line driving circuit wiring lines, the data line driving circuit wiring lines, and the image signal wiring lines being planarly laid out so as not to intersect each other in the peripheral region, [see fig. 4 & 11].

Referring to claim 14, Muraide discloses the image signal wiring lines being arranged between the scanning line driving circuit wiring lines and the data line driving circuit wiring lines, [see fig. 4].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-9, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muraide JP 2002-049052 in view of Yamazaki et al U.S. Patent No. 6,011,607.

Referring to claims 4 and 5, Muraide discloses the electro-optical device according to claim 1, further comprising: a counter electrode provided in the peripheral region on a counter substrate (20) that is arranged to face the element substrate (10); and upper and lower conduction terminals (106) that are provided in the peripheral region on the element substrate, in order to connect a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, [see figs. 3 & 4].

Muraide lacks disclosure of the counter electrode potential line of the plurality of main wiring lines being positioned near edges of the element substrate in the peripheral region, and the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, wherein the plurality of external circuit connection terminals being arranged along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

Back to figure 4 of Muraide reference, those limitations that Muraide lacks disclosure of as mentioned above would be met if the scanning line driving circuits

placed inside the sealant, which made the scanning line driving circuits be nearer to the center of the display.

Yamazaki et al discloses the peripheral driver circuit are integrally packed on the display, located inside the sealant, [see fig. 1 – element '103' for the peripheral driver circuit; '102' for the sealant], for the benefit of being protected from the external moisture and contaminants. This also enhances the long-term reliability of the peripheral driver circuit, [see abstract]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have discloses the peripheral driver circuit are located inside the sealant for the benefit of being protected from the external moisture and contaminants and long-term reliability, and therefore, it would have been also obvious to one ordinary skill in the art to achieve the counter electrode potential line of the plurality of main wiring lines being positioned near edges of the element substrate in the peripheral region, and the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, wherein the plurality of external circuit connection terminals being arranged along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

Claim 6 and 7 are met the similarly discussion regarding claims 4 and 5 rejection above.

Referring to claims 8 and 9, Muraide discloses the plurality of main wiring lines including a pair of clock signal lines (CLX, CLY) that supply a clock signal (CLX, CLY) and an inverse signal (CLX', CLY') thereof as electric signals, respectively, and that do not intersect the counter electrode potential line, [see fig. 4].

Referring to claim 12, even though Muraide lacks disclosure of the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film, it would have been obvious to one ordinary skill in the art to have redundant wiring lines for the benefit of having high reliability device.

Claim 15 is met the discussion regarding claims 12 and 4 rejection above.

Referring to claim 16, adapting an electro-optical device according to claim 1 in an electronic apparatus as personal computer is an intended use limitation, and therefore does not patentably distinguish the invention.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Muraide JP 2002-049052.

Yamazaki et al U.S. Patent No. 6,011,607.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on M-F/9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen
Examiner
Art Unit 2871
-- November 11, 2005 --

TN

ANDREW SCHECHTER
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/852,255	Applicant(s)/Patent Under Reexamination MURADE, MASAO	
	Examiner (Nancy) Thanh-Nhan P. Nguyen	Art Unit 2871	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,011,607	01-2000	Yamazaki et al.	349/153
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
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	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Sheet 1 of 1

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 119570	APPLICATION NO. New U.S. Patent Application
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Masao MURADE	
		FILING DATE May 25, 2004	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
TN	1	JP A 11-202367 w/ Abst & Trans	7/30/1999	Japan	—	—
TN	2	JP A 11-223832 w/ Abst & Trans	8/17/1999	Japan	—	—
TN	3	JP A 2002-49052 w/ Abst & Trans	5/15/2002	Japan	—	—

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
	11/11/05

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: May 25, 2004

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Form PTO-1449 (REV. 8-83) US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 119570	APPLICATION NO. 10/852,255
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Masao MURADE	
	FILING DATE May 25, 2004	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
TN	1	JP A 10-253984 w/Abstract and Translation	9/25/1998	Japan		
TN	2	JP A 2000-137205 w/Abstract and Translation	5/16/2000	Japan		
TN	3	JP A 2000-162634 w/Abstract and Translation	6/16/2000	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
	11/11/05

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 14, 2005

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/852,255	MURADE, MASAO
Examiner	**Art Unit**
(Nancy) Thanh-Nhan P. Nguyen	2871

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/852,255	MURADE, MASAO	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P. Nguyen	2871	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search & PLUS search -- see printout.	11/11/2005	TN

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp

L1	149	(("5345416") or ("4806795") or ("5276352") or ("5564696") or ("5579256") or ("5602771") or ("5854508") or ("5943285") or ("5943106") or ("5945846") or ("5969544") or ("6041013") or ("6049500") or ("6160744") or ("6212089") or ("6212089") or ("6424589") or ("5561626") or ("5488498") or ("6330044") or ("5008728") or ("6084821") or ("6160753") or ("4496894") or ("4499754") or ("4527136") or ("4589007") or ("4811295") or ("4922117") or ("4939592") or ("4970685") or ("5200918") or ("5278466") or ("5349218") or ("5376842") or ("5402318") or ("5412262") or ("5444276") or ("5446700") or ("5497109") or ("5528540") or ("5619048") or ("5714801") or ("5719806") or ("5726929") or ("5744820") or ("5761149") or ("5793664") or ("5812440") or ("5867440") or ("5875133") or ("5883427") or ("6008869") or ("6014337") or ("6044028") or ("6052301") or ("6055276") or ("6104630") or ("6104289") or ("6107869") or ("6111799") or ("6127741") or ("6157561") or ("6157569") or ("6181005") or ("6192000") or ("6249477") or ("6274912") or ("6282147") or ("6337593") or ("6339358") or ("6404661") or ("6445041") or ("6504187") or ("6587174") or ("6646916") or ("6717881") or ("6788562") or ("6822900") or ("6952049") or ("4383148") or ("4596000") or ("4791639") or ("4956561") or ("4996168") or ("5012427") or ("5014243") or ("5185650") or ("5239196") or ("5331572") or ("5378925") or ("5408750") or ("5539223") or ("5572480") or ("5604674") or ("5652457") or ("5656836") or ("5700704") or ("5731219") or ("5737053") or ("5767554") or ("5834851") or ("5847420") or ("5978621") or ("6111621") or ("6140155") or ("6157052") or ("6163443") or ("6335884") or ("6388329") or ("6515913") or ("6545366") or ("6657901") or ("6953709") or ("5657139") or ("5757444") or ("5774100") or ("5852488") or ("5231637") or ("5311048") or ("5371032") or ("5414285") or	US-PGPUB; USPAT	OR	OFF	2005/11/12 17:20

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L8	193	349/152.ccls. and (circuit and seal$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/12 20:52
L9	2	("20040246246" | "6774968").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/11/12 20:55
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S4	4	S2 and murade.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/12 18:10

PLUS Search Results for S/N 10852255, Searched October 17, 2005

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PLUS Search Results for S/N 10852255, Searched October 04, 2005

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PLUS Search Results for S/N 10852255, Searched September 23, 2005

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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5231637	6011608	6646916	6704068	4575840	
5239196	6014337	6657901	6717633	4574679	
5278466	6025901	6686987	6770908	4583215	

OIPE IAP45 SEP 14 2005 PATENT & TRADEMARK OFFICE

IFW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2871

Application No.: 10/852,255

Examiner: Unknown

Filed: May 25, 2004

Docket No.: 119570

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. English language Abstracts of the non-English language references are attached hereto.

☒ 3. Computer-generated English language translations of the following Japanese Patent Publications have been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and are attached, but have not been reviewed for accuracy.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

John S. Kern
Registration No. 42,719

JAO:JSK/kap
Date: September 14, 2005

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Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 119570	APPLICATION NO. 10/852,255
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Masao MURADE	
		FILING DATE May 25, 2004	GROUP 2871

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 10-253984 w/Abstract and Translation	9/25/1998	Japan		
	2	JP A 2000-137205 w/Abstract and Translation	5/16/2000	Japan		
	3	JP A 2000-162634 w/Abstract and Translation	6/16/2000	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 14, 2005

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-162634

(43)Date of publication of application : 16.06.2000

(51)Int.CI. G02F 1/1345
G02F 1/136
G09F 9/30
H01L 29/786

(21)Application number : 11-025008

(22)Date of filing : 02.02.1999

(71)Applicant : SEIKO EPSON CORP

(72)Inventor : MURAIDE MASAO

(30)Priority

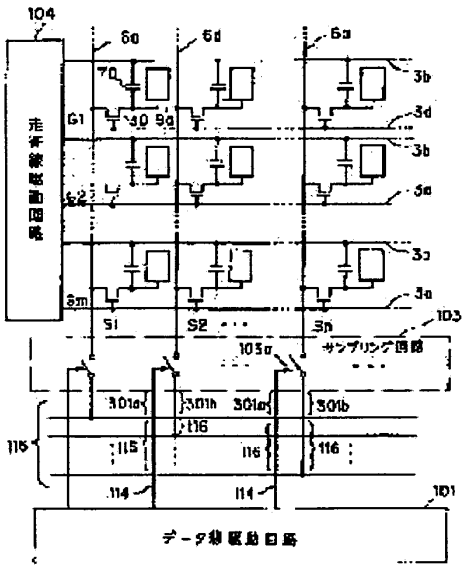
Priority number :	Priority date :	Priority country :
10020002	30.01.1998	JP
10219433	03.08.1998	JP
10272118	25.09.1998	JP

(54) ELECTRO-OPTIC DEVICE AND ITS MANUFACTURE, AND ELECTRONIC DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain an image display of high quality by composing a peripheral wire of a 1st wire part, including a 1st conductive film forming a light shielding film and a 2nd wire part including at least one of plural thin films constituting a thin-film transistor, a data line, and a scanning line.

SOLUTION: A liquid crystal device is equipped with a data line drive circuit 101, which drives data lines 6a, a scanning line drive circuit 104 which in turn drives scanning lines 3a, and a sampling circuit 103 which samples an image signal at the periphery of an image display area on a TFT array substrate where the data lines 6a, scanning lines 3a, etc., are formed. Further, N image signal lines 115 are wired sat the periphery of the image display area. Especially repeating wires 116 which become long in lesponge to the number(N) of the image signal lines 115 are constituted in a double-wiring structure so as to make the resistance small. Consequently, while the signal delay of image signals is suppressed, a serial-parallel conversion number(N) and the number of the image signal 115 can be increased.



LEGAL STATUS

[Date of request for examination]	23.06.2003
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3674356
[Date of registration]	13.05.2005
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line on the substrate, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor arranged so that a channel field may be covered superficially at least, It has circumference wiring connected to the circumference circuit and said circumference circuit for supplying a signal to at least one side of said scanning line and said data line. Said circumference wiring The electro-optic device characterized by having the 2nd wiring section containing at least one electric conduction film of two or more thin films which constitute the 1st wiring section containing the 1st electric conduction film which forms said light-shielding film, and said thin film transistor, said data line and said scanning line.
[Claim 2] It is the electro-optic device according to claim 1 which said 1st wiring section has at least one 2nd electric conduction film in two or more thin films which constitute said thin film transistor, said data line, and said scanning line, and said 1st electric conduction film, and is characterized by said 2nd wiring section containing the different 3rd electric conduction film, as for said 2nd electric conduction film of two or more thin films which constitute said thin film transistor, said data line, and said scanning line.
[Claim 3] Said 2nd electric conduction film is an electro-optic device according to claim 2 characterized by being high resistance rather than said 1st electric conduction film.
[Claim 4] The 1st interlayer insulation film which intervenes between said light-shielding films and said thin film transistors, It has further the 2nd interlayer insulation film which intervenes between said 2nd electric conduction film and said 3rd electric conduction film. Said 1st wiring section The electro-optic device according to claim 2 or 3 characterized by consisting of junction wiring which crosses in three dimensions respectively through said 1st and 2nd interlayer insulation films to the other sections of said 1st wiring section while electrical connection is carried out to said a part of 2nd wiring section.
[Claim 5] Said circumference circuit is an electro-optic device according to claim 4 characterized by including the sampling circuit for sampling said picture signal, the data-line drive circuit to which drive this sampling circuit to predetermined timing, and said two or more data lines are made to supply said picture signal on said picture signal line through said sampling circuit, and the scanning-line drive circuit which drives said scanning line including a picture signal line for said circumference wiring to supply said picture signal from an external circuit connection terminal.
[Claim 6] It is the electro-optic device according to claim 5 which N (however, N two or more natural numbers) serial-parallel conversion of said picture signal is carried out, and N of said picture signal line are prepared in juxtaposition, and is characterized by the picture signal line of this N book including said junction wiring in the part which crosses mutually.
[Claim 7] It is the electro-optic device according to claim 5 or 6 which equips said sampling circuit with two or more sampling circuit drive signal lines for supplying a sampling circuit driving signal further from said data-line drive circuit, and is characterized by the part where this sampling circuit drive signal line intersects said picture signal line at least consisting of said junction wiring.
[Claim 8] Said 1st electric conduction film which constitutes said 1 wiring section, and said 2nd electric

conduction film are an electro-optic device given in any 1 term of claims 2-7 characterized by carrying out electrical connection mutually through the contact hole established in said 1st interlayer insulation film.

[Claim 9] It is an electro-optic device given in any 1 term of claims 2-8 characterized by for said 3rd electric conduction film consisting of a metal membrane which forms said data line, and said 2nd electric conduction film consisting of polish recon film which forms said scanning line.

[Claim 10] Said electrooptic material is pinched between the opposite substrates which counter said substrate. In the seal field on said substrate which comes to paste up said substrate and opposite substrate by the sealant, and counters said sealant Cross to the perimeter of electrooptic material and the laminating of said 1st electric conduction film, said 2nd electric conduction film, and said 3rd electric conduction film is carried out at least. The drawer wiring section by the side of said data line pulled out through said seal field and said scanning line is an electro-optic device given in any 1 term of claims 2-9 characterized by consisting of at least one of said 1st electric conduction film, 2nd electric conduction film, and 3rd electric conduction film, respectively.

[Claim 11] Said drawer wiring section is an electro-optic device according to claim 10 characterized by coming to carry out electrical connection of at least two of said 1st electric conduction film, 2nd electric conduction film, and 3rd electric conduction film mutually through a contact hole, respectively.

[Claim 12] It is the electro-optic device according to claim 10 characterized by for said drawer wiring section consisting of wiring formed from one of said 1st electric conduction film, 2nd electric conduction film, and 3rd electric conduction film, respectively, and others and 2 of said 1st electric conduction film, 2nd electric conduction film, and 3rd electric conduction film consisting of dummy wiring which does not function as wiring in said seal field.

[Claim 13] An electro-optic device given in any 1 term of claims 2-12 characterized by covering said 1st electric conduction film with said 2nd electric conduction film in said 1st wiring section.

[Claim 14] It is the electro-optic device according to claim 13 characterized by the wiring width of face of said 1st electric conduction film being below the wiring width of face of said 2nd electric conduction film in said 1st wiring section.

[Claim 15] The thin film transistor connected to the scanning line, two or more data lines, and two or more said each scanning line and said each data line on the substrate, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor in which the channel field was established superficially at least in the wrap location, It has the sampling circuit which samples said picture signal supplied to two or more picture signal lines which supply a picture signal, and these two or more picture signal lines, and is supplied to each of two or more of said data lines. Some wiring [at least] which connects said picture signal line and said sampling circuit is the electro-optic devices characterized by consisting of the 1st electric conduction film of the same film as said light-shielding film.

[Claim 16] Some sampling circuit drive signal lines [at least] which supply a sampling circuit driving signal to said sampling circuit are the electro-optic devices according to claim 15 characterized by consisting of said 1st electric conduction film.

[Claim 17] It comes to insert electrooptic material between the substrates of a pair. On one substrate of the substrate of this pair The thin film transistor connected to the scanning line, two or more data lines, and two or more said each scanning line and said each data line, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor in which the channel field was established superficially at least in the wrap location, In the manufacture approach of the electro-optic device equipped with the sampling circuit which samples said picture signal supplied to two or more picture signal lines which supply a picture signal, and these two or more picture signal lines, and is supplied to each of two or more of said data lines The process which forms the 1st electric conduction film which becomes some wiring which connects said picture signal line and said sampling circuit, and said light-shielding film with the same ingredient, The process which forms the 1st interlayer

insulation film on said 1st electric conduction film and said light-shielding film, The process which forms the 2nd electric conduction film connected to said 1st electric conduction film through the contact hole formed in said 1st interlayer insulation film while forming said scanning line on this 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said scanning line and said 2nd electric conduction film, The manufacture approach of the electro-optic device characterized by having the process which forms said picture signal line connected to said data line connected to said thin film transistor through the contact hole of said 2nd interlayer insulation film, and said 2nd electric conduction film.

[Claim 18] It comes to insert electrooptic material between the substrates of a pair. On one substrate of the substrate of this pair The thin film transistor connected to the scanning line, two or more data lines, and two or more said each scanning line and said each data line, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor in which the channel field was established superficially at least in the wrap location, In the manufacture approach of the electro-optic device equipped with the sampling circuit which samples said picture signal supplied to two or more picture signal lines which supply a picture signal, and these two or more picture signal lines, and is supplied to each of two or more of said data lines The process which forms the 1st electric conduction film which becomes some wiring which connects said picture signal line and said sampling circuit, and said light-shielding film with the same ingredient, The process which forms the 1st interlayer insulation film on this 1st electric conduction film and said light-shielding film, The semi-conductor layer which serves as the source of said thin film transistor, and a drain on this 1st interlayer insulation film, and the process which carries out laminating formation of the gate electrode one by one at a gate-dielectric-film list, The process which forms the 2nd interlayer insulation film on said gate electrode, and said data line connected to said thin film transistor through the contact hole of said 2nd interlayer insulation film are formed. The manufacture approach of the electro-optic device characterized by having the process which forms the picture signal line connected to said 1st electric conduction film through the contact hole of said 1st and 2nd interlayer insulation films.

[Claim 19] Electronic equipment characterized by equipping claims 1-16 with the electro-optic device of a publication.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.

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3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention belongs to the technical field of electro-optic devices, such as liquid crystal equipment of the active-matrix drive method by the thin film transistor (TFT is called suitably below), and the manufacture approach of those, is circumference circuit built-in [which builds

in circumference circuits, such as a data-line drive circuit and a scanning-line drive circuit, especially], and belongs to the technical field of electro-optic devices, such as liquid crystal equipment of the format which prepared the light-shielding film in the TFT bottom, and the manufacture approach of those.

[0002]

[Description of the Prior Art] Conventionally, in circumference circuit built-in liquid crystal equipment, on the other hand, the substrate of the pair which pinches liquid crystal comes out, and circumference circuits, such as a data-line drive circuit, a scanning-line drive circuit, and a sampling circuit, are formed on a certain TFT array substrate. As for these circumference circuits, it is more common than viewpoints, such as manufacture effectiveness, to be formed of the manufacture process using the same structure as TFT (for TFT for pixel switching to be called suitably below) for performing switching control of the picture signal which is formed in each pixel section and impressed to each pixel electrode. And in the image display field which counters liquid crystal, much the data lines and the scanning lines carry out a phase crossover, and are wired at a TFT array substrate top. Moreover, I/O wiring of a circumference circuit is wired in the seal field which counters the sealant for being outside this image display field and enclosing liquid crystal, or the boundary region further located in that outside. As I/O wiring of a circumference circuit, drawer wiring from the data line, the scanning line, and a capacity line etc. is prepared in the bottom of a seal field, and, more specifically, the picture signal line connected to the external circuit connection terminal, a control signal line, power-source wiring, a clock signal line, etc. are formed in the boundary region.

[0003] If a picture signal is supplied to a picture signal line through an external circuit connection terminal, it consists of liquid crystal equipment equipped with the sampling circuit especially as a circumference circuit so that each sampling switch of a sampling circuit may sample a picture signal for every data line with the sampling circuit driving signal outputted from a data-line drive circuit to predetermined timing.

[0004] Here, although a picture signal line is a signal line which supplies the picture signal itself which specifies the applied voltage applied to liquid crystal therefore, it becomes very important, when preventing image quality degradation that delay of the picture signal is low. For this reason, it is low resistance most among the wiring materials which constitute liquid crystal equipment, and a picture signal line is formed from metal membranes, such as aluminum (aluminum) used for usually forming the data line.

[0005] On the other hand, the technique which forms the scanning line from the metal membrane metallurgy group silicide film is not put in practical use from the reason of film peeling in the scanning line occurring in the elevated-temperature process after scanning-line formation, but the scanning line is usually formed by the polish recon film. The sheet resistance of this polish recon film increases dozens times as compared with the sheet resistance which consists of metal membranes, such as aluminum, and wiring resistance becomes large. Therefore, when a picture signal line is temporarily formed from the polish recon film, and the wiring resistance concerned becomes large, signal delay arises and image quality degradation is caused. For this reason, a picture signal line is formed from a metal membrane as mentioned above in fact.

[0006] Thus, it is possible to wire by the metal membrane in the same layer on a substrate (that is, formed of the same process) until it will result [from the external circuit connection terminal prepared in the substrate edge] in each sampling switch of a sampling circuit with the constituted circumference circuit built-in liquid crystal equipment, if there is a picture signal line. However, for example, the case where two or more picture signal lines are needed according to the number of serial-parallel conversion to the picture signal by which serial-parallel conversion was carried out that it should correspond to the RF drive in liquid crystal equipment, When two or more picture signal lines are needed according to a color to the color picture signal of RGB, while resulting in each sampling switch, it can wire, if at least one picture signal line does not cross by other picture signal lines and somewhere. That is, it becomes

impossible to wire in two or more picture signal lines of all only using the metal membrane in the same layer. For this reason, it is coped with, using the polish recon film which is in another layer through an interlayer insulation film to the metal membrane concerned as junction wiring (the 1st wiring section). the part which more specifically crosses -- one wiring -- low -- it constitutes as the 2nd wiring section which consists of a metal membrane [****]. And wiring of another side is constituted as the 1st wiring section which consists of polish recon film by which electrical connection was carried out to the wiring part which consists of a metal membrane through the contact hole punctured before and behind the crossing part so that the bottom of the 2nd wiring section or a top may be made to cross in three dimensions through an interlayer insulation film.

[0007] the 1st wiring section which consists of polish recon film only the part which crosses as mentioned above -- carrying out -- the other part -- low -- since the die length of the 2nd wiring section which consists of a metal membrane [****], then junction wiring which consists of polish recon film is very short and ends, it did not almost have it that the rise of the time constant of the whole picture signal line by existence of junction wiring which consists of the polish recon film concerned poses a problem practically.

[0008]

[Problem(s) to be Solved by the Invention] Under a general request called the latest improvement in image quality, the drive frequency of liquid crystal equipments, such as the so-called XGA method and a SXGA method, is becoming still higher, and number of serial-parallel conversion, 24 [for example,], phases etc. are becoming a large number considerably in connection with this.

[0009] However, in this way, if serial-parallel conversion is carried out at a large number, naturally the number of the picture signal lines by which a parallel arrangement is carried out will also increase, and the die length of junction wiring using the above-mentioned polish recon film will become long according to this. Here, since wiring resistance becomes large in proportion to die length, wiring resistance of junction wiring becomes high and it originates in this, and the time constant of a picture signal line becomes large, and comes to cause degradation of image quality. For example, when the time constant of a picture signal line becomes large, there is a problem which the potential shake of a picture signal is caused by increase of coupling capacity, or the picture signal for Rhine (train) of a self-stage is written in Rhine (train) of the next step, and a ghost and a cross talk produce.

[0010] Moreover, in forming separately junction wiring in a seal field or a boundary region temporarily from the metal membrane which is not used in the pixel section, the manufacture effectiveness in the manufacture process which used planar technique falls, a cost rise is caused, and the fundamental advantage of circumference circuit built-in liquid crystal equipment may be lost.

[0011] This invention is made in view of the trouble mentioned above, and the electric resistance in I/O wiring of a circumference circuit can be lowering it by deployment of the thin film which constitutes the pixel section in electro-optic devices, such as circumference circuit built-in liquid crystal equipment, and let it be a technical problem to offer the electro-optic device in which image display is possible and its manufacture approach of high quality.

[0012]

[Means for Solving the Problem] The scanning line of plurality [top / substrate] in order that the 1st electro-optic device of this invention may solve the above-mentioned technical problem, The thin film transistor connected to the data line, and two or more of said each scanning line and said each data line, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor arranged so that a channel field may be covered superficially at least, It has circumference wiring connected to the circumference circuit and said circumference circuit for supplying a signal to at least one side of said scanning line and said data line. Said circumference wiring It is characterized by having the 2nd wiring section containing at least one electric conduction film of two or more thin films which constitute the 1st wiring section containing the 1st electric conduction film which forms said light-shielding film, and said thin film transistor, said data line and said scanning line.

[0013] According to the 1st electro-optic device of this invention, on the substrate, even if there are few thin film transistors, the light-shielding film is prepared so that a channel field may be covered superficially. Therefore, it is shaded by the light-shielding film and the channel field of a thin film transistor can prevent property degradation by invasion of the light to a thin film transistor etc. Especially in this invention, circumference wiring has the 2nd wiring section which consists of electric conduction film which is one of two or more thin film layers which constitute a thin film transistor, the data line, and the scanning line, and the 1st wiring section which consists of the same film as a light-shielding film. For example, if it forms by a metal simple substance, a metal, or a metal silicide layer containing at least one of Ti (titanium), Cr (chromium), W (tungsten), Ta (tantalum), Mo (molybdenum), and Pb(s) (lead) which are the conductive refractory metal film about the 1st electric conduction film etc., it will become possible to lower wiring resistance notably. Under the present circumstances, since a light-shielding film combines both a protection-from-light function and the function as circumference wiring to a thin film transistor, when attaining simplification of a configuration, and the simplification of manufacture, it is advantageous.
[0014] Since I/O of various kinds of signals, such as a picture signal in a circumference circuit, is performed by circumference wiring of low resistance the above result, Even if it raises the drive frequency of an electro-optic device or makes the number of serial-parallel conversion, and the number of picture signals by which a parallel input is carried out increase further High-definition image display is able to reduce the potential shake by capacity coupling in circumference wiring of the picture signal line like the conventional example mentioned above etc., a ghost, a cross talk, etc., and to carry out.
[0015] In the mode of 1 of the 1st electro-optic device of this invention, said 1st wiring section has at least one 2nd electric conduction film in two or more thin films which constitute said thin film transistor, said data line, and said scanning line, and said 1st electric conduction film, and it is characterized by said 2nd wiring section containing the different 3rd electric conduction film from said 2nd electric conduction film of two or more thin films which constitute said thin film transistor, said data line, and said scanning line.
[0016] this voice -- if it depends like -- for example, the 3rd electric conduction film -- for example, a metal membrane etc. -- low -- by the metal membrane [****] the 2nd electric conduction film -- for example, the 3rd electric conduction film, such as polish recon film, -- high -- the case where it forms in a thin film layer [****] -- as much as possible -- low -- although it is desirable to form wiring with the 3rd electric conduction film which consists of a metal membrane [****], the 2nd electric conduction film may be used for the part where wiring crosses as some wiring In that case, since resistance is high compared with the 3rd electric conduction film, problems, such as signal delay, may generate the 2nd electric conduction film. Then, resistance of the circumference wiring [itself] can also be lowered by carrying out electrical connection of the 1st and 2nd electric conduction film instead of wiring which consists of the 2nd electric conduction film, and considering as duplex wiring. For example, if it forms by a metal simple substance, an alloy, or metal silicide etc. which forms the 2nd electric conduction film from the polish recon film, and contains at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are the conductive refractory metal film about the 1st electric conduction film, resistance of the 1st wiring section can be governed by the sheet resistance of the 1st electric conduction film. That is, large low resistance-ization is attained like the former by carrying out electrical connection of the 1st electric conduction film as compared with wiring which consists of a polish recon film independent. And about the resistance in the 2nd wiring section of this invention, since it is made to low resistance by using the 3rd electric conduction film, such as aluminum (aluminum), for example, circumference wiring which carried out electrical connection of the 1st wiring section and the 2nd wiring section to the serial can be formed into low resistance.
[0017] In addition, even if the part which consists of the 2nd electric conduction film or the 1st electric conduction film which consists of polish recon film in the 1st wiring section etc. with a foreign matter etc. is disconnected on the way, the redundant structure that a flow can be taken in the part of another

side is realizable.
[0018] In addition, although circumference wiring of this invention has the 1st wiring section and the 2nd wiring section Redundancy-wiring is added to the 2nd wiring section which has the 3rd electric conduction film like ****. Also as multiplex wiring of a duplex, Mie, etc. It cannot be overemphasized that there is no change in there being no change in having the single wiring section concerned, adding still redundancy-wiring further to the 1st wiring section which has the 1st electric conduction film and the 2nd electric conduction film like ****, and having the duplex wiring section concerned also as four-fold [Mie,] multiplex wiring etc.
[0019] Said 2nd electric conduction film in the 1st electro-optic device of this invention may be high resistance from said 1st electric conduction film.
[0020] Thus, if constituted, the 3rd electric conduction film will be low resistance most among the thin film layers which constitute thin film transistors, such as for example, aluminum film, and another side and the 2nd electric conduction film will be low resistance the 2nd of the thin film layers which constitute thin film transistors, such as for example, polish recon film. Since resistance can be lowering with the 1st electric conduction film in the 1st wiring section, resistance of the circumference wiring [itself] can also be lowered.
[0021] The 1st interlayer insulation film which intervenes between said light-shielding films and said thin film transistors in the 1st electro-optic device of this invention, It has further the 2nd interlayer insulation film which intervenes between said 2nd electric conduction film and said 3rd electric conduction film, and it consists of junction wiring which crosses in three dimensions respectively through said 1st and 2nd interlayer insulation films to the other sections of said double wiring section while electrical connection of said 1st wiring section is carried out to said a part of 2nd wiring section.
[0022] According to this mode, junction wiring crosses in three dimensions respectively through the 1st and 2nd interlayer insulation films to the other sections of the 2nd wiring section while electrical connection is carried out to a part of 2nd wiring section (namely, a top or the bottom). Therefore, the part which crosses mutually is required and a desired pattern can be wired through junction wiring in circumference wiring which cannot be arranged in the same layer.
[0023] In the 1st electro-optic device of this invention said circumference wiring The picture signal line for supplying said picture signal from an external circuit connection terminal is included. Said circumference circuit The sampling circuit for sampling said picture signal, and the data-line drive circuit to which drive this sampling circuit to predetermined timing, and said two or more data lines are made to supply said picture signal on said picture signal line through said sampling circuit, You may constitute so that the scanning-line drive circuit which drives said scanning line may be included.
[0024] Thus, if constituted, the part which crosses mutually is required and a desired pattern can be wired through junction wiring in the picture signal line which cannot be arranged in the same layer.
[0025] In the 1st electro-optic device of this invention, N (however, N two or more natural numbers) serial-parallel conversion of said picture signal is carried out, N of said picture signal line are prepared in juxtaposition, and the picture signal line of this N book may be constituted so that said junction wiring may be included in the part which crosses mutually.
[0026] Thus, if constituted, since there are many picture signals with which the parallel input of the number of serial-parallel conversion (N) is carried out like [since it is large / in the case of the color picture signal of RGB etc.], for example, when long junction wiring needs to be taken As compared with the case where junction wiring is formed, resistance of junction wiring and the increment in a time constant can be suppressed from a polish recon film independent like the conventional example mentioned above.,
[0027] In the 1st electro-optic device of this invention, it has further two or more sampling circuit drive signal lines for supplying a sampling circuit driving signal to said sampling circuit from said data-line drive circuit, and this sampling circuit drive signal line may be constituted so that the part which intersects said picture signal line at least may consist of said junction wiring.

[0028] If constituted, thus, the sampling circuit drive signal line from a data-line drive circuit to a sampling circuit For example, it becomes possible to wire using junction wiring which intersects a picture signal line. As compared with the case where the degree of freedom of a wiring layout forms from the 2nd electric conduction film independent, such as polish recon film, like increase and the conventional example which mentioned above junction wiring in a sampling circuit drive signal line also in this case further, the increment in the time constant in a sampling circuit drive signal line can be suppressed.
[0029] In the 1st electro-optic device of this invention, said 1st electric conduction film which constitutes said 1st wiring section, and said 2nd electric conduction film may be constituted as electrical connection is mutually carried out through the contact hole established in said 1st interlayer insulation film.
[0030] Thus, if constituted, the 1st wiring section with the high dependability by which electrical connection was mutually carried out through the contact hole can be obtained. And such a contact hole can be formed comparatively easily using the manufacture process in Pixel TFT.
[0031] In the 1st electro-optic device of this invention, said 3rd electric conduction film may consist of a metal membrane which forms said data line, and said 2nd electric conduction film may consist of polish recon film which forms said scanning line.
[0032] Thus, if constituted, since the 2nd wiring section is formed from metal membranes, such as aluminum, it can carry out [low ****]-izing. Moreover, although the part which consists of polish recon film is high resistance at about dozens times as compared with the case of a metal membrane, a duplex wires with the 1st electric conduction film, and resistance of ** and the 1st wiring section becomes possible [forming low resistance farther than resistance of the polish recon film]. if for example, the 1st electric conduction film is formed from the metal membrane, the alloy, or metal silicide containing at least one of the conductive refractory metal film Ti, Cr, W, Ta, Mo, and Pb -- the polish recon film -- as compared with the case of being independent, it becomes possible to lower a time constant to several [1/] (about [for example,] -- one half and about 1/3).
[0033] In the 1st electro-optic device of this invention, it comes to pinch electrooptic material between the opposite substrates which counter said substrate. In the seal field on one [which comes to paste up said substrate and said opposite substrate by the sealant, and counters said sealant / said] substrate Cross to the perimeter of said electrooptic material and the laminating of said 1st electric conduction film, said 2nd electric conduction film, and said 3rd electric conduction film is carried out at least. The drawer wiring section pulled out in the installation direction of said data line and said scanning line through said seal field may consist of at least one of said 1st electric conduction film, 2nd electric conduction film, and 3rd electric conduction film, respectively.
[0034] Thus, if constituted, electrooptic material is enclosed by the sealant between the substrates of a pair, and the so-called electrooptic material cel is constituted. Here, since it crosses to the perimeter of electrooptic material and the laminating of the 1st electric conduction film, the 2nd electric conduction film, and the 3rd electric conduction film is carried out to the seal field at least, it becomes possible to suppress the variation crossed to the perimeter of the electrooptic material of the gap between both substrates including the various thin films in a seal field. When mixing the gap material which follows, for example, has a predetermined outer diameter in a sealant and controlling the gap of an electrooptic material cel, it becomes possible to perform gap control more correctly and good. And since the drawer wiring section pulled out in the installation direction of the data line and the scanning line through a seal field, respectively consists of at least one of the 1st electric conduction film, the 2nd electric conduction film, and the 3rd electric conduction film, respectively, it becomes possible [performing signal supply into an image display field without a problem].
[0035] Said drawer wiring section may consist of modes in which the laminating of the 1st electric conduction film, the 2nd electric conduction film, and the 3rd electric conduction film is carried out to the seal field in the 1st electro-optic device of this invention so that it may consist of a duplex with which electrical connection of at least two of said 1st electric conduction film, the 2nd electric

conduction film, and the 3rd electric conduction film was mutually carried out through the contact hole, or the Mie wiring section, respectively. Thus, if constituted, low resistance-ization in the drawer wiring section can be attained.

[0036] Or said drawer wiring section may consist of the single wiring section formed from one of said 1st electric conduction film, the 2nd electric conduction film, and the 3rd electric conduction film, respectively, and others and 2 of said 1st electric conduction film, the 2nd electric conduction film, and the 3rd electric conduction film may be constituted so that it may consist of dummy wiring which does not function as wiring in said seal field. Thus, if constituted, it will become possible to suppress the variation in the gap between both the substrates in a seal field comparatively simply by the thickness of dummy wiring.

[0037] In the 1st electro-optic device of this invention, said 1st electric conduction film may have the configuration covered with said 2nd electric conduction film.

[0038] Since according to this mode increase of capacity coupling with the part which consists of this 1st electric conduction film can be controlled in the wiring sections, such as a picture signal line, for example, it intersects the part which consists of this 1st electric conduction film by covering the 1st electric conduction film superficially with the 2nd electric conduction film among the 1st wiring sections, increase of the time constant in the wiring section by this capacity coupling can be controlled. If the structure where the 1st electric conduction film and the 2nd electric conduction film intervene especially is taken, increase of capacity coupling between the 1st electric conduction film and the 2nd electric conduction film at the time of using a light-shielding film for the duplex wiring section can be controlled. Consequently, degradation of the picture signal in wiring of a picture signal line etc. can be prevented effectively.

[0039] In the 1st electro-optic device of this invention, the wiring width of face of said 1st electric conduction film may be below the wiring width of face of the part which consists of said 2nd electric conduction film.

[0040] Thus, if constituted, increase of capacity coupling between the 1st electric conduction film and the 2nd electric conduction film can be controlled certainly.

[0041] In order that the 2nd electro-optic device of this invention may solve the above-mentioned technical problem, on a substrate The thin film transistor connected to the scanning line, two or more data lines, and two or more said each scanning line and said each data line, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor in which the channel field was established superficially at least in the wrap location, It has the sampling circuit which samples said picture signal supplied to two or more picture signal lines which supply a picture signal, and these two or more picture signal lines, and is supplied to each of two or more of said data lines. Some wiring [at least] which connects said picture signal line and said sampling circuit consists of the 1st electric conduction film of the same film as said light-shielding film.

[0042] According to the 2nd electro-optic device of this invention, since some junction wiring [at least] which connects a picture signal line and a sampling circuit consists of the 1st electric conduction film of the same film as a conductive light-shielding film, it can attain low resistance-ization in wiring. For example, if the 1st electric conduction film is formed with the conductive refractory metal film, it will become possible to lower the wiring resistance in the junction wiring concerned notably. Under the present circumstances, since the 1st electric conduction film combines both a protection-from-light function and the function as wiring to a thin film transistor, when attaining simplification of a configuration, and the simplification of manufacture, it is advantageous.

[0043] Since the input of the picture signal in a sampling circuit is performed by wiring of low resistance the above result, even if it raises the drive frequency of an electro-optic device or makes the number of serial-parallel conversion, and the number of picture signals by which a parallel input is carried out increase further, the potential shake by capacity coupling in junction wiring of the picture signal line like the conventional example mentioned above etc., a ghost, a cross talk, etc. are reduced, and can perform

high-definition image display.
[0044] In the mode of 1 of the 2nd electro-optic device of this invention, some sampling circuit drive signal lines [at least] which supply a sampling circuit driving signal to said sampling circuit consist of said 1st electric conduction film.
[0045] According to this mode, since some sampling circuit drive signal lines [at least] consist of the 1st electric conduction film, it can attain low resistance-ization in a sampling circuit drive signal line. Consequently, since the input of the sampling circuit driving signal in a sampling circuit is performed by the sampling circuit drive signal line of low resistance, high-definition image display can be performed.
[0046] In order that the manufacture approach of the 1st electro-optic device of this invention may solve the above-mentioned technical problem, it comes to insert electrooptic material between the substrates of a pair. On one substrate of the substrate of this pair The thin film transistor connected to the scanning line, two or more data lines, and two or more said each scanning line and said each data line, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor in which the channel field was established superficially at least in the wrap location, In the manufacture approach of the electro-optic device equipped with the sampling circuit which samples said picture signal supplied to two or more picture signal lines which supply a picture signal, and these two or more picture signal lines, and is supplied to each of two or more of said data lines The process which forms the 1st electric conduction film which becomes some wiring which connects said picture signal line and said sampling circuit, and said light-shielding film with the same ingredient, The process which forms the 1st interlayer insulation film on said 1st electric conduction film and said light-shielding film, The process which forms the 2nd electric conduction film connected to said 1st electric conduction film through the contact hole formed in said 1st interlayer insulation film while forming said scanning line on this 1st interlayer insulation film, It has the process which forms said picture signal line connected to the process which forms the 2nd interlayer insulation film on said scanning line and said 2nd electric conduction film, said data line connected to said thin film transistor through the contact hole of said 2nd interlayer insulation film, and said 2nd electric conduction film.
[0047] According to the manufacture approach of the 1st electro-optic device of this invention, the 1st electric conduction film and light-shielding film which connect a picture signal line and a sampling circuit are formed with the same ingredient. Therefore, simplification of a production process is attained. Next, the 2nd electric conduction film connected to the 1st electric conduction film through the contact hole which the 1st interlayer insulation film was formed on the 1st electric conduction film and a light-shielding film, and the scanning line was formed on this 1st interlayer insulation film, and was formed in the 1st interlayer insulation film is formed. Next, the 2nd interlayer insulation film is formed on the scanning line and the 2nd electric conduction film, and the picture signal line connected to the data line and the 2nd electric conduction film which are connected to a thin film transistor through the contact hole of the 2nd interlayer insulation film is formed. Since the input of the picture signal in a sampling circuit is performed by junction wiring of low resistance the above result, even if it raises the drive frequency of an electro-optic device or makes the number of serial-parallel conversion, and the number of picture signals by which a parallel input is carried out increase further, the electro-optic device in which high-definition image display is possible can be manufactured.
[0048] In order that the manufacture approach of the 2nd electro-optic device of this invention may solve the above-mentioned technical problem, it comes to insert electrooptic material between the substrates of a pair. On one substrate of the substrate of this pair The thin film transistor connected to the scanning line, two or more data lines, and two or more said each scanning line and said each data line, The pixel electrode connected to said thin film transistor, and the conductive light-shielding film of said thin film transistor superficially formed in the wrap location in the channel field at least, In the manufacture approach of the electro-optic device equipped with two or more picture signal lines which supply a picture signal, and the sampling circuit which samples said picture signal supplied to said two or more picture signal lines, and is supplied to each of two or more of said data lines The process which

forms the 1st electric conduction film which becomes some junction wiring [at least] which connects said picture signal line and said sampling circuit, and said light-shielding film with the same ingredient, The process which forms the 1st interlayer insulation film on this 1st electric conduction film and said light-shielding film, The semi-conductor layer which serves as the source of said thin film transistor, and a drain on this 1st interlayer insulation film, and the process which carries out laminating formation of the gate electrode one by one at a gate-dielectric-film list, The process which forms the 2nd interlayer insulation film on said gate electrode, and said data line connected to said thin film transistor through the contact hole of said 2nd interlayer insulation film are formed. It has the process which forms the picture signal line connected to said 1st electric conduction film through the contact hole of said 1st and 2nd interlayer insulation films.

[0049] According to the manufacture approach of the 2nd electro-optic device of this invention, the 1st electric conduction film and light-shielding film which connect a picture signal line and a sampling circuit are formed with the same ingredient. Therefore, simplification of a production process is attained. Next, the 1st interlayer insulation film is formed on the 1st electric conduction film and a light-shielding film, on this 1st interlayer insulation film, laminating formation of the gate electrode is carried out one by one at the semi-conductor layer used as the source of a thin film transistor, and a drain, and a gate-dielectric-film list, and the 2nd interlayer insulation film is further formed on a gate electrode. Next, the data line connected to a thin film transistor through the contact hole of the 2nd interlayer insulation film is formed. Next, the picture signal line connected to the 1st electric conduction film is formed through the contact hole of the 1st and 2nd interlayer insulation films. Since the input of a picture signal is performed by junction wiring of low resistance the above result, even if it raises the drive frequency of an electro-optic device or makes the number of serial-parallel conversion, and the number of picture signals by which a parallel input is carried out increase further, the electro-optic device in which high-definition image display is possible can be manufactured.

[0050] The electronic equipment of this invention is characterized by having the above-mentioned electro-optic device. According to this configuration, signal delay can be suppressed and the electronic equipment in which high-definition image display is possible can be offered.

[0051] Such an operation and other gains of this invention are made clear from the operation gestalt explained below.

[0052]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing. In addition, the operation gestalt of this invention explains liquid crystal equipment as an example as an electro-optic device.

[0053] (The configuration and actuation of liquid crystal equipment) The configuration and actuation of the operation gestalt of liquid crystal equipment by this invention are explained with reference to drawing 10 from drawing 1 .

[0054] First, the circuitry of liquid crystal equipment is explained with reference to the block diagram of drawing 1 .

[0055] Drawing 1 shows the circumference circuit located around equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes an image display field on the TFT array substrate of liquid crystal equipment] a matrix, and wiring, and an image display field.

[0056] In drawing 1 , two or more formation of TFT30 for two or more pixels formed in the shape of [which constitutes the image display field of the liquid crystal equipment by this operation gestalt] a matrix to control pixel electrode 9a and pixel electrode 9a is carried out at the shape of a matrix, and electrical connection of the data-line 6a to which a picture signal is supplied is carried out to the source concerned of TFT30. The picture signals S1, S2, --, Sn written in data-line 6a are supplied to this order line sequential. Especially with this operation gestalt, serial-parallel conversion of the picture signals S1, S2, --, Sn is carried out at N (however, N two or more natural numbers) phase. In addition, you may constitute so that it may supply for every group to data-line 6a of N book which adjoins each other from

the picture signal line 115 of N book. If such a configuration is taken, the drive frequency of the data-line drive circuit 101 can be reduced, and reliable liquid crystal equipment can be realized.
[0057] Moreover, electrical connection of the scanning-line 3a is carried out to the gate of TFT30, and it consists of predetermined timing so that the scan signals G1, G2, --, Gm may be impressed to scanning-line 3a in pulse line sequential at this order. Electrical connection of the pixel electrode 9a is carried out to the drain of TFT30, and it writes in the picture signals S1, S2, --, Sn supplied from data-line 6a in TFT30 which is a switching element when only a fixed period closes the switch to predetermined timing. Fixed period maintenance of the picture signals S1, S2, --, Sn of the predetermined level written in the liquid crystal as electrooptic material through pixel electrode 9a is carried out between the counterelectrodes (it mentions later) formed in the opposite substrate (it mentions later). When the orientation and order of molecular association change with the voltage levels impressed, liquid crystal modulates light and enables a gradation display. According to the electrical potential difference impressed when it was in no MARI White mode, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from liquid crystal equipment as a whole. Here, in order to prevent the held picture signal leaking, storage capacitance 70 is added to the liquid crystal capacity and juxtaposition which are formed between pixel electrode 9a and a counterelectrode. For example, as for the electrical potential difference of pixel electrode 9a, only time amount also with triple figures longer than the time amount to which picture signals S1 and S2 and --Sn were supplied is held with storage capacitance 70. Thereby, it is improved further and a maintenance property can realize the high liquid crystal equipment of a contrast ratio. In addition, it cannot be overemphasized that capacity line 3b which is wiring for forming capacity as an approach of forming storage capacitance 70 may be prepared, and capacity may be formed between scanning-line 3a of the preceding paragraph.
[0058] In drawing 1 , liquid crystal equipment equips the perimeter of the image display field on the TFT array substrate with which data-line 6a, scanning-line 3a, etc. were formed as mentioned above with the sampling circuit 103 which samples the data-line drive circuit 101 which drives data-line 6a, the scanning-line drive circuit 104 which drives scanning-line 3a, and a picture signal as an example of a circumference circuit. Furthermore, around the image display field, the picture signal line 115 of N book for supplying the picture signals S1, S2, --, Sn by which serial-parallel conversion was carried out is wired from the external circuit connection terminal as an example of circumference wiring by N phase like ****.
[0059] As this number of serial-parallel conversion (N), if the sampling capacity in the sampling circuit 103 concerned is relatively high, serial-parallel conversion of a three phase circuit, serial-parallel conversion of six phases, etc. are sufficient, for example, and if sampling capacity is relatively low, serial-parallel conversion of 12 phases, serial-parallel conversion of 24 phases, etc. are desirable.
[0060] Since low resistance is formed especially here by making into duplex wiring structure junction wiring 116 which becomes long according to the number of serial-parallel conversion (N), i.e., the number of the picture signal line 115, (N) so that it may explain in full detail behind with this operation gestalt Suppressing signal delay of a picture signal effectively, the number of serial-parallel conversion (N) and the number of the picture signal line 115 can be increased, and the drive frequency of liquid crystal equipment is raised, without therefore degrading image quality. In addition, it is desirable when simplifying control and a circuit, in case video presentation, such as an NTSC display and a PAL display, is carried out to it being the multiple of 3 from the relation of a color picture signal consisting of a signal concerning three colors (red, blue, green) as this number of serial-parallel conversion (N).
[0061] Even if it does not perform serial-parallel conversion like ****, when forming two or more picture signal lines 115 like [in the case of the color picture signal of RGB], the structure concerning the junction wiring 116 grade in this operation gestalt explained below formed into low resistance is effective.

[0062] Furthermore, with this operation gestalt, low resistance-ization of the sampling circuit drive signal line 114 from the data-line drive circuit 101 to [so that it may explain in full detail behind] a sampling circuit 103 can also be attained according to the duplex wiring structure.
[0063] The data-line drive circuit 101 supplies a sampling circuit driving signal to the control terminal of each sampling switch 103a which constitutes a sampling circuit 103 through the sampling circuit drive signal line 114 according to the scanning-line drive circuit 104 sending a scan signal to scanning-line 3a in order in pulse. A sampling circuit 103 samples the picture signal supplied to the picture signal line 115 from the external circuit according to this sampling circuit driving signal, and supplies it to data-line 6a.
[0064] In addition, each sampling switch 103a which constitutes a sampling circuit 103 consists of TFT(s), such as an n channel mold which can be preferably manufactured from viewpoints, such as manufacture effectiveness, according to the same manufacture process as TFT30 in the pixel section, a p channel mold, and a complementary type.
[0065] Next, the configuration of the pixel section in the image display field of liquid crystal equipment is explained with reference to drawing 2 and drawing 3 . Drawing 2 is a top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, the pixel electrode, the light-shielding film, etc. were formed adjoins each other, and drawing 3 is the A-A' sectional view of drawing 2 . In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 3 .
[0066] In drawing 2 , on the TFT array substrate of liquid crystal equipment, two or more transparent pixel electrode 9a (the profile is shown by dotted-line section 9a') is prepared in the shape of a matrix, and data-line 6a, scanning-line 3a, and capacity line 3b are prepared respectively along the boundary of pixel electrode 9a in every direction. Electrical connection of the data-line 6a is carried out to the below-mentioned source field among semi-conductor layer 1a through the contact hole 5, and electrical connection of the pixel electrode 9a is carried out to the below-mentioned drain field among semi-conductor layer 1a through the contact hole 8. Moreover, scanning-line 3a is arranged so that the below-mentioned channel field may be countered among semi-conductor layer 1a. And 1st light-shielding film 11a in the pixel section is prepared in the field shown with the slash of a drawing Nakamigi riser. That is, in the pixel section, 1st light-shielding film 11a looks at TFT including the channel field of semi-conductor layer 1a from a TFT array substrate side, and is respectively prepared in the wrap location superficially. In addition, although the prevention function of the optical leak in Pixel TFT will be demonstrated if 1st light-shielding film 11a covers the joint of the channel field of semi-conductor layer 1a and a channel field, and a source drain field at least In order to give the wiring function for making 1st light-shielding film 11a into constant potential, from the reason for specifying the opening field (namely, field which light penetrates) of the pixel section etc., 1st light-shielding film 11a is prepared in the shape of stripes along with scanning-line 3a especially with this operation gestalt.
[0067] As shown in drawing 3 , liquid crystal equipment is equipped with the TFT array substrate 10 which constitutes an example of the substrate of while it is transparence, and the opposite substrate 20 which it is the transparence by which opposite arrangement is carried out at this, and also constitutes an example of the substrate of a way. The TFT array substrate 10 consists for example, of a quartz substrate, and the opposite substrate 20 consists of a glass substrate or a quartz substrate. Pixel electrode 9a is prepared in the TFT array substrate 10, and the orientation film 16 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. Pixel electrode 9a consists of transparent conductive thin films, such as for example, ITO (Indium Tin Oxide) film. Moreover, the orientation film 16 consists of organic thin films, such as for example, a polyimide thin film.
[0068] Moreover, TFT30 for pixel switching which carries out switching control of each pixel electrode 9a is formed in the location which adjoins each pixel electrode 9a at the TFT array substrate 10.
[0069] On the other hand, it crosses to the opposite substrate 20 all over the, the counterelectrode

(common electrode) 21 is formed, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 22 consists of organic thin films, such as a polyimide thin film.

[0070] As further shown in the opposite substrate 20 at drawing 3 , the 2nd light-shielding film 23 is formed in fields other than the opening field of each pixel. For this reason, incident light does not invade into channel field 1a' of semi-conductor layer 1a of TFT30 for pixel switching, source side LDD (Lightly Doped Drain) field 1b, and drain side LDD field 1c from the opposite substrate 20 side. Furthermore, the 2nd light-shielding film 23 has functions, such as improvement in contrast, and color mixture prevention of color material.

[0071] Thus, it is constituted, and between the TFT array substrates 10 and the opposite substrates 20 which have been arranged so that pixel electrode 9a and a counterelectrode 21 may meet, liquid crystal is enclosed with the space surrounded by the below-mentioned sealant, and the liquid crystal layer 50 is formed. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 16 and 22 in the condition that the electric field from pixel electrode 9a are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant 52 may stick the TFT array substrate 10 and the opposite substrate 20 around those, and spacers, such as glass fiber for making distance between both substrates into a predetermined value or a glass bead, are mixed.

[0072] As shown in drawing 3 , in the location which counters TFT30 for pixel switching respectively, 1st light-shielding film 11a is respectively prepared between the TFT array substrate 10 and each TFT30 for pixel switching. 1st light-shielding film 11a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are the desirable opaque refractory metal film, an alloy, or metal silicide. If constituted from such an ingredient, 1st light-shielding film 11a is destroyed by high temperature processing performed after the formation process of 1st light-shielding film 11a on the TFT array substrate 10, or it can avoid fusing by it. Since 1st light-shielding film 11a is formed, the situation in which the return light from the TFT array substrate 10 side etc. carries out incidence to channel field 1a' of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c can be prevented, and the property of TFT30 for pixel switching does not deteriorate according to generating of a photocurrent.

[0073] Furthermore, the 1st interlayer insulation film 12 is formed between 1st light-shielding film 11a and two or more TFT30 for pixel switching. The 1st interlayer insulation film 12 is formed in order to carry out electric insulation of the semi-conductor layer 1a which constitutes TFT30 for pixel switching from 1st light-shielding film 11a.

[0074] Storage capacitance 70 is constituted by installing the insulating thin film 2 prepared with this operation gestalt between the gate electrode which consists of a part of scanning-line 3a, and semi-conductor layer 1a from the location which counters scanning-line 3a, using as a dielectric film, installing semi-conductor layer 1a, considering as the 1f of the 1st storage capacitance electrodes, and using as the 2nd storage capacitance electrode a part of capacity line 3b which counters these further. More, it is installed in the bottom of data-line 6a and scanning-line 3a, and into the capacity line 3b part similarly prolonged along with data-line 6a and scanning-line 3a, opposite arrangement is carried out through the insulating thin film 2, and let high concentration drain field 1e of semi-conductor layer 1a be the 1f of the 1st storage capacitance electrodes at the detail. Since especially the insulating thin film 2 as a dielectric of storage capacitance 70 is exactly gate dielectric film of TFT30 formed on the polish recon film of high temperature oxidation, it can be made into the thin insulator layer of high pressure-proofing, and can constitute storage capacitance 70 from small area as mass storage capacitance comparatively.

[0075] In drawing 3 TFT30 for pixel switching Channel field 1a' of semi-conductor layer 1a in which it has LDD structure and a channel is formed of the electric field from scanning-line 3a and this scanning-

line 3a, The insulating thin film 2, data-line 6a which insulate scanning-line 3a and semi-conductor layer 1a, 1d list of high concentration source fields of low concentration source field (source side LDD field) 1b of semi-conductor layer 1a and low concentration drain field (drain side LDD field) 1c, and semi-conductor layer 1a is equipped with high concentration drain field 1e. One to which it corresponds of two or more pixel electrode 9a is connected to high concentration drain field 1e. Low concentration drain field 1c and high concentration drain field 1e are formed in low concentration source field 1b and 1d list of high concentration source fields to semi-conductor layer 1a like the after-mentioned by doping the impurity ion the object for n molds of predetermined concentration, or for p molds according to whether the channel of n mold or p mold is formed. TFT of an n-type channel has the advantage that a working speed is quick, and it is used as TFT30 for pixel switching which is the switching element of a pixel in many cases. Data-line 6a is constituted from the thin film of protection-from-light nature, such as alloy film, such as metal membrane metallurgy group silicide, such as aluminum, by especially this operation gestalt. Moreover, on scanning-line 3a, the insulating thin film 2, and the 1st interlayer insulation film 12, the 2nd interlayer insulation film 4 with which the contact hole 8 which leads to the contact hole 5 and high concentration drain field 1e which lead to 1d of high concentration source fields was formed respectively is formed. Electrical connection of the data-line 6a is carried out to 1d of high concentration source fields through the 1d [of this high concentration source field] contact hole 5. Furthermore, on data-line 6a and the 2nd interlayer insulation film 4, the 3rd interlayer insulation film 7 with which the contact hole 8 to high concentration drain field 1e was formed is formed. Electrical connection of the pixel electrode 9a is carried out to high concentration drain field 1e through the contact hole 8 to this high concentration drain field 1e. The above-mentioned pixel electrode 9a is prepared in the top face of the 3rd interlayer insulation film 7 constituted in this way.

[0076] Although TFT30 for pixel switching has LDD structure as mentioned above preferably, it may be TFT of the self aryne mold which may have the offset structure which does not drive impurity ion into low concentration source field 1b and low concentration drain field 1c, drives in impurity ion by high concentration by using as a mask the gate electrode which consists of a part of scanning-line 3a, and forms a high concentration source field and a high concentration drain field in self align.

[0077] Moreover, although considered as the single gate structure which has arranged one gate electrode which consists of a part of scanning-line 3a of TFT30 for pixel switching among 1d [of high concentration source fields], and high concentration drain field 1e with this operation gestalt, two or more gate electrodes may be arranged among these. Under the present circumstances, to each gate electrode, the same signal is made to be impressed. Thus, if TFT is constituted above the dual gate (double-gate) or the triple gate, the leakage current of a channel field and a source drain field joint can be prevented, and the current at the time of OFF can be reduced. If at least one of these gate electrodes is made into LDD structure or offset structure, the OFF state current can be reduced further and the stable switching element can be obtained.

[0078] Although a photocurrent will occur according to the photo-electric-conversion effectiveness and the transistor characteristics of TFT30 for pixel switching will generally deteriorate here if light carries out incidence of channel field 1a' of semi-conductor layer 1a, low concentration source field 1b, low concentration drain field 1c, etc. With this operation gestalt, since data-line 6a is formed from the metal membrane of protection-from-light nature, such as aluminum, so that it may lap from the bottom, scanning-line 3a The incidence of the incident light to channel field 1a' of semi-conductor layer 1a and low concentration source field 1b, and low concentration drain field 1c can be prevented effectively at least. Moreover, as mentioned above, since 1st light-shielding film 11a is prepared in the TFT30 bottom for pixel switching, the incidence of the return light to channel field 1a' of semi-conductor layer 1a and low concentration source field 1b, and low concentration drain field 1c can be prevented effectively at least.

[0079] In addition, especially with this operation gestalt, electrical connection of the 1st light-shielding film 11a is carried out to the constant source of potential, and let it be constant potential. Therefore,

potential fluctuation of 1st light-shielding film 11a does not have a bad influence on 1st light-shielding film 11a to TFT30 for pixel switching by which opposite arrangement is carried out. In this case, although constant sources of potential, such as a negative supply supplied to the circumference circuits (for example, a scanning-line drive circuit, a data-line drive circuit, etc.) for driving the liquid crystal equipment concerned as a constant source of potential and a positive supply, a touch-down power source, the constant source of potential supplied to a counterelectrode 21 are mentioned, with this operation gestalt, 1st light-shielding film 11a shall be connected to the negative supply of a scanning-line drive circuit. Thus, if the power source of a circumference circuit etc. is used, it is necessary to prepare neither potential wiring of dedication, nor an external circuit connection terminal, and 1st light-shielding film 11a will be made to constant potential.

[0080] Next, I/O wiring or circumference wiring in a circumference circuit of liquid crystal equipment is explained with reference to drawing 7 from drawing 4 .

[0081] Drawing 4 is the part plan of a TFT array substrate in which circumference wiring was prepared, drawing 5 is the expansion top view expanding and showing junction wiring of drawing 4 , and the drawer wiring section, drawing 6 R> 6 is the B-B' sectional view of drawing 4 and drawing 5 , and drawing 7 is the C-C' sectional view of drawing 4 and drawing 5 .

[0082] In drawing 4 , from the external circuit connection terminal 102 prepared in the periphery of the TFT substrate array substrate 10, scanning-line drive signal-line 105a is wired in the scanning-line drive circuit 104, and two or more picture signal lines 115 are wired to the field between the data-line drive circuit 101 and the seal field where the sealant 52 which encloses liquid crystal has been arranged.

[0083] And in the inside [field / seal], as shown in drawing 4 and drawing 5 , the sampling circuit 103 is arranged under the 3rd light-shielding film 53 (the inside of drawing, slash field upward slanting to the right) as a frame prepared on the opposite substrate 20, in order to divide the outside of an image display field and this image display field. Moreover, in the bottom of the seal field on the production of data-line 6a, the drawer wiring 301 by the side of the data line containing drawer wiring 301a of the sampling circuit drive signal line 114 from the data-line drive circuit 101 and drawer wiring 301b from the picture signal line 115 is formed. On the other hand, in the bottom of the seal field on the production of scanning-line 3a, drawer wiring 401of scanning-line 3a a is prepared. Moreover, it cannot be overemphasized that drawer wiring 401of capacity line 3b b may be prepared. The counterelectrode potential wiring 112 may be installed in the drawer wiring 401 and juxtaposition by the side of these scanning lines. It connects with the counterelectrode 21 (refer to drawing 3) formed in the opposite substrate 20 through vertical flow terminal 106a and the vertical flow material 106, and this counterelectrode potential wiring 112 supplies common potential. Moreover, the data-line drive circuit 101 may be adjoined and the inspection terminal 111 for inputting the signal of predetermined checking may be formed in the data-line drive circuit 101.

[0084] As shown in the B-B' sectional view of drawing 6 , an example slack picture signal line 115 of circumference wiring and drawer wiring 301b are formed by metal membranes (the 3rd electric conduction film), such as aluminum formed at the same process as forming data-line 6a. On the other hand, the junction wiring 116 which pulls out from the picture signal line 115 and results in wiring 301b 2nd electric conduction film 116a by which electrical connection was carried out to the picture signal line 115 which is formed from the same film as the polish recon film which forms scanning-line 3a, and corresponds through contact hole 305a, And by 1st electric conduction film 116b by which is formed from the same film as 1st light-shielding film 11a, and electrical connection was carried out to junction wiring 116a through contact hole 305b, it has the duplex wiring structure wired by the duplex in the thickness direction of a TFT array substrate. Moreover, in order to form drawer wiring 301b into low resistance further, 2nd electric conduction film 116a' and 1st electric conduction film 116b' may be prepared.

[0085] For this reason, as compared with the case where junction wiring is formed from a polish recon film independent, the resistance in the junction wiring 116 can be lowering by conductive 1st electric

conduction film 116b like the former. Since 1st electric conduction film 116b is formed from a metal simple substance, an alloy, or metal silicide containing at least one of W, Ti, Cr(s), Ta, Mo, and Pb(s) which are the conductive refractory metal film etc., more specifically, it can govern the resistance of a direction which met wiring in the junction wiring 116 by the sheet resistance of 1st electric conduction film 116b. Namely, although it has resistance of an about [100-200Kohm] in the case of 1.3 inches of vertical angles, or about 0.9 inches small liquid crystal equipment, for example, has a wiring time constant for about about ten microseconds in it since the polish recon film has the sheet resistance which is 25ohms / ** extent when thickness is 300nm Since 1st electric conduction film 116b can be reduced to 10ohms / ** extent when sheet resistance is 200nm of thickness, it becomes possible [making this wiring time constant small at about several microseconds]. Therefore, generating of a cross talk, a ghost, etc. who produce the bottom of the picture signal line 115 in the potential shake of the picture signal by capacity coupling of the junction wiring 116 and the picture signal line 115 which were wired by crossing can be reduced. And since signal delay of a picture signal can be controlled with constituting especially the liquid crystal equipment concerned as a high model of drive frequencies, such as XGA and SXGA, as mentioned above even if the number of serial-parallel conversion (N) and the number (N) of the picture signal line 115 increase, highly minute and high-definition liquid crystal equipment is realizable.

[0086] In addition, even if either 2nd electric conduction film 116a or 1st electric conduction film 116b is disconnected on the way with a foreign matter etc. so that drawing 6 may show, redundant structure that a flow can be taken on the other hand is realized. And also when 2nd electric conduction film 116a and 1st electric conduction film 116b broke through the 1st interlayer insulation film 12 and short-circuit mutually, it is not necessary to become a defective article. Therefore, according to this operation gestalt, the rate of a defective is low and the liquid crystal equipment in which reliable high-definition image display is possible can be realized. And in building the junction wiring 116 concerned, it is the same process as the process which forms 1st light-shielding film 11a for shading TFT for pixel switching, and low resistance of the junction wiring 116 can be realized, without increasing a process, since 1st electric conduction film 116b can be formed.

[0087] Moreover, the sampling circuit drive signal line 114 shown in drawing 4 and drawing 5 has the duplex wiring structure which crosses the lower part of the picture signal line 115 like the junction wiring 116 shown in drawing 6 . Thus, if constituted, like the conventional example, as compared with the case where it forms from a polish recon film independent, resistance of the sampling circuit drive signal line 114 and the increment in a time constant can be suppressed, and it can apply to a high-frequency drive.

[0088] Furthermore, as shown in drawing 6 and drawing 7 , 2nd electric conduction film 116a' and 1st electric conduction film 116b' are prepared as redundancy wiring, and drawer wiring 301b from picture signal line 115a under a seal field has Mie wiring structure. Therefore, it considers as wiring of very low resistance, and as moreover shown in drawing 5 , electrical connection is mutually carried out by contact hole 305a and contact hole 305b by two or more places under the seal field, and redundancy is increasing. The dependability of drawer wiring 301b is very high these results. In addition, the same effectiveness is acquired even if it adopts the duplex wiring structure which pulls out either 2nd electric conduction film 116a' and 3rd electric conduction film 116b', and is considered as redundancy wiring of wiring 301b. Moreover, you may constitute so that drawer wiring 301a of the sampling circuit drive signal line 114 may have the wiring structure more than a duplex or Mie similarly.

[0089] On the other hand, the drawer wiring 401 by the side of the scanning line shown in drawing 4 is respectively prolonged in the direction in alignment with scanning-line 3a, wiring which adjoin each other sets spacing and they are arranged. And the drawer wiring 401 consists of same polish recon film as scanning-line 3a, and dummy wiring which consisted of same aluminum film as data-line 6a is prepared after each drawer wiring 401. In addition, like the case of the drawer wiring 301 by the side of the data line mentioned above, although the resistance about the drawer wiring 401 by the side of the scanning line does not usually pose a problem, the drawer wiring 401 by the side of the scanning line may be

constituted so that it may have the wiring structure more than a duplex or Mie.
[0090] It crosses to a seal field around the liquid crystal layer 50. On the TFT array substrate 10 Therefore, 1st electric conduction film 116b, 116b' and the layered product which contains the 1st interlayer insulation film 12, the 2nd interlayer insulation film 4, and the 3rd interlayer insulation film 7 in 2nd electric conduction film 116a, 116a', and the 3rd electric conduction film (aluminum film) list will be formed uniformly. It becomes possible [height], since the height of the front face of the 3rd interlayer insulation film 7 in the seal field in the side of the upper and lower sides of an image display field and the height of the front face of the 3rd interlayer insulation film 7 in the side of right and left of an image display field are in agreement to suppress the variation in the gap between both the substrates in the whole seal field. When mixing the gap material which follows, for example, has a predetermined outer diameter in a sealant and controlling the gap of a liquid crystal cell, it becomes possible to perform gap control more correctly and good. If constituted especially in this way, even if the drawer wiring 301 by the side of the data line or the drawer wiring 401 by the side of the scanning line is disconnected in response to the stress by gap material in the bottom of a seal field, it will not become a critical defect for multiplex wiring structure.
[0091] In addition, as long as it thinks the purpose of such gap control as important, it may pull out, as shown in drawing 6 , and it may stop carrying out electrical connection for 2nd electric conduction film 116a' and 1st electric conduction film 116b' to wiring 301b, and these 2nd electric conduction film 116a' and 1st electric conduction film 116b' may be constituted as dummy wiring for gap control.
[0092] With this operation gestalt, as shown in drawing 5 , in the seal field, the drawer wiring 301 is equipped with the stripe-like flat-surface pattern, and the clearance for light transmission corresponding to the wiring spacing S is prepared between wiring which has width of face L, respectively and adjoins each other. Therefore, if incidence of the light is carried out through the TFT array substrate 10 when the sealant 52 which consists of a photo-setting resin is used, light can fully be irradiated through the clearance for light transmission in this laminated structure at a sealant 52. Therefore, photo-curing of the sealant 52 which consists of a photo-setting resin can be carried out good by the light from substrates [both] side. Since it is not necessary to give excessive heat to liquid crystal equipment compared with the case of heat curing, and the heat deterioration of each component of liquid crystal equipment is prevented or generating of the equipment defect by heat distortion is prevented, it is [be / it / if / photo-curing can be carried out especially in this way,] advantageous. Moreover, since there is little time amount of an optical exposure and it ends, a damage is not given to the orientation film 16 and 22 (refer to drawing 3). Therefore, since it is maintained while the tilt angle of liquid crystal has been high, image quality degradation by the poor orientation (disclination) of liquid crystal can be prevented.
[0093] Moreover, in drawing 4 and drawing 5 , the dummy pixel with the same configuration as the pixel which constitutes an image display field is formed in the bottom of the 3rd light-shielding film 53 as a frame. Although there is no need of constituting the pixel for a display under the 3rd light-shielding film 53 prepared so that the poor orientation field of liquid crystal etc. might be hidden, you may make it only predetermined width of face prepare a dummy pixel outside the edge of an image display field in this way for property stabilization of the pixel near the edge of an image display field.
[0094] furthermore -- a book -- operation -- a gestalt -- **** -- especially -- junction -- wiring -- 116 -- opposite -- a substrate -- a side -- from -- seeing -- a light-shielding film -- from -- becoming -- the -- one -- electric conduction -- the film -- 116 -- b -- 116 -- b -- ' -- a polish -- recon -- the film -- from -- becoming -- the -- two -- electric conduction -- the film -- 116 -- a -- 116 -- a -- ' -- covering -- having -- a configuration -- having -- a thing -- being desirable . In drawing 7 , the wiring width of face W1 of 2nd electric conduction film 116a' is the same as the wiring width of face W2 of 1st electric conduction film 116b', or it is more specifically desirable to be materialized under the seal field shown in the bottom of being [115] more than it, i.e., the W1 >= picture signal line which the relation it is unrelated to W2 showed to drawing 6 , and drawing 7 . Thus, if

constituted, it can set to drawing 6 , increase of capacity coupling between 1st electric conduction film 116b and the picture signal line 115 can be controlled, and increase of the time constant in the picture signal line 115 and the junction wiring 116 by this capacity coupling can be controlled. In the part which crosses especially, since 2nd electric conduction film 116a intervened between 1st electric conduction film 116b and the picture signal line 115 and 1st electric conduction film 116b and the picture signal line 115 have separated distance comparatively, increase of the above-mentioned capacity coupling can be controlled.

[0095] Although the junction wiring 116 shown in drawing 6 and drawing 7 has taken the duplex wiring structure which consisted of 2nd electric conduction film 116a and 1st electric conduction film 116b, it may delete 2nd electric-conduction film 116a and 116a' in the duplex wiring structure shown in these drawings, and as shown in drawing 8 and drawing 9 , it may take the single wiring structure which consisted of 1st electric-conduction film 116c and 116c'. Thus, if constituted, the profits by redundant structure will not be obtained, but since only the part in which the 1st interlayer insulation film 12 exists becomes small as compared with the case where prepare 2nd electric conduction film 116a between the 1st interlayer insulation film 12 and the 2nd interlayer insulation film 4, and the junction wiring 116 is constituted, the capacity between the picture signal lines 115 and 1st electric conduction film 116c under the picture signal line 115 shown in drawing 6 is advantageous.

[0096] On the other hand, in drawing 4 and drawing 5 , since the picture signal line 115 consists of 3rd electric conduction film (aluminum film) formed on the 2nd interlayer insulation film 4, it cannot consist of aluminum film like [signal line / 114 / which pulls out from the data-line drive circuit 101 which intersects this, and results in wiring 301a / sampling circuit drive] the case of the junction wiring 116 shown in drawing 6 or drawing 8 . For this reason, the three-dimensional junction wiring 116 like drawing 10 which passes along a lower layer or the upper layer of the picture signal line 115 etc. is needed for the sampling circuit drive signal lines 114. In addition, drawing 10 is a sectional view in alignment with D-D' of drawing 5 . Moreover, the device which lowers a time constant as much as possible is required for the junction wiring 116. Then, a method which is described below can be considered.

[0097] The 116d of the 1st electric conduction film consists of refractory metal film or metal alloy film of the same film as 1st light-shielding film 11a, such as W (tungsten), etc., and it is having the bottom of the 1st interlayer insulation film 12 let it pass in drawing 10 (1), so that the picture signal line 115 may be intersected. And through the contact hole punctured by the 1st interlayer insulation film 12 and the 2nd interlayer insulation film 4 in the both sides of the picture signal line 115, it is constituted so that electrical connection of the sampling circuit drive signal line 114 by the side of the data-line drive circuit 101 and the drawer wiring 301a by the side of a seal field may be carried out, respectively. if such a configuration is taken -- junction wiring -- low -- since it can form with a refractory metal [****] etc., it becomes possible to lower wiring resistance and delay of a picture signal is not caused.

[0098] In drawing 10 (2), junction wiring consists of 116d of 1st electric conduction film which consists of the refractory metal film or metal alloy film, such as the same W as 2nd electric conduction film 116e and 1st light-shielding film 11a which consist of the same polish recon film as scanning-line 3a, etc., and it lets the bottom of the 2nd interlayer insulation film 4 and the 1st interlayer insulation film 12 pass, respectively so that the picture signal line 115 may be intersected. And through the contact hole punctured by the 1st interlayer insulation film 12 and the 2nd interlayer insulation film 4 in the both sides of the picture signal line 115 by a diagram, respectively, it is constituted so that electrical connection of the sampling circuit drive signal line 114 by the side of the data-line drive circuit 101 and the drawer wiring 301a by the side of a seal field may be carried out, respectively. If such a configuration is taken, since the 116d of the 1st electric conduction film and 2nd electric conduction film 116e will be formed in the lower layer of the picture signal line 115 through the 1st interlayer insulation film 12 and the 2nd interlayer insulation film 4, redundant structure is realizable. the 116d of moreover, the 1st electric conduction film -- low -- since it consists of a refractory metal [****] or metal alloy film, it becomes possible to lower wiring resistance and signal delay of a picture signal is not caused. In addition,

although it was made to carry out electrical connection of the 116d of the 1st electric conduction film, and the 2nd electric conduction film 116e directly, it may be made to carry out electrical connection to drawer wiring 301a by the side of the 116d of the 1st electric conduction film, the sampling circuit drive signal line 114, or a seal field directly.

[0099] In drawing 10 (3), junction wiring is added to the 116d of the 1st electric conduction film and 2nd electric conduction film 116e which were constituted almost like junction wiring which makes the redundant structure in drawing 10 (2). It lets the 116f of the 4th electric conduction film which consists of refractory metal film or metal alloy film for specifying a part of pixel opening field further at least on the 3rd interlayer insulation film 7 etc. pass so that the picture signal line 115 may be intersected, and the 4th interlayer insulation film 117 is formed on it. And through the contact hole punctured by the 3rd interlayer insulation film 7 in the both sides of the picture signal line 115 by a diagram, it is constituted so that electrical connection of the sampling circuit drive signal line 114 by the side of the data-line drive circuit 101 and the drawer wiring 301a by the side of a seal field may be carried out with the 116f of the 4th electric conduction film, respectively. If such a configuration is taken, since junction wiring will be formed in the vertical layer of the picture signal line 115 through the 1st interlayer insulation film 12, the 2nd interlayer insulation film 4, and the 3rd interlayer insulation film 7 from three layers of the 116d of the 1st electric conduction film, 2nd electric conduction film 116e, and the 116f of the 4th electric conduction film, the further redundant structure is realizable. moreover, the 116d of the 1st electric conduction film and the 116f of the 4th electric conduction film -- low -- since it consists of refractory metal film [****] or metal alloy film, it becomes possible to lower wiring resistance still further, and signal delay of a picture signal is not caused.

[0100] Although the picture signal line 115 and junction wiring 116 for sampling circuit drive signal-line 114 were formed into low resistance with this operation gestalt using the 1st electric conduction film formed at the same process as 1st light-shielding film 11a as explained above, the application part of junction wiring of this invention is restricted to neither these picture signal lines 115 nor the sampling circuit drive signal line 114. For example, it sets in the data-line drive circuit 101, the scanning-line drive circuit 104, and the circumference circuit of sampling circuit 103 grade. Junction wiring which consists of polish recon film formed at the same process as scanning-line 3a formed in the part where wiring which consist of aluminum film crosses through an interlayer insulation film, It is possible like the case of the gestalt of above-mentioned operation to transpose junction wiring of the arbitration in a circumference circuit to the monolayer or multiplex wiring formed into low resistance using the 1st electric conduction film, and to constitute it. Improvement in the speed of the drive by especially low resistance-ization of junction wiring the data-line drive circuit 101 and for scanning-line drive circuit 104 preventing delay of the shift register which constitutes those circuits can be attained. Moreover, low resistance-ization of junction wiring for a sampling circuit or precharge circuits can suppress the provincial accent of a sampling circuit driving signal or a precharge circuit driving signal, and the good writing of a picture signal of it is attained, and, finally it can aim at improvement in image quality. In addition, even if junction wiring constitutes multiplex wiring from electric conduction film more than two-layer, it is satisfactory in any way.

[0101] (Manufacture process of liquid crystal equipment) Next, the manufacture process of the operation gestalt of liquid crystal equipment with the above configurations is explained with reference to drawing 14 from drawing 11 . Drawing 11 and drawing 12 are process drawings in which making each class by the side of the TFT array substrate in each process correspond to the B-B' cross section of drawing 4 like drawing 6 , and showing it, and drawing 13 and drawing 14 are process drawings in which making each class by the side of the TFT array substrate in each process correspond to the A-A' cross section of drawing 2 like drawing 3 , and showing it. In addition, since the manufacture process in a B-B cross section and the manufacture process in a C-C' cross section are fundamentally performed in parallel to coincidence, the following explanation is also given to juxtaposition about both processes.

[0102] As shown in the process (1) of drawing 11 and drawing 13 , the TFT array substrates 10, such as

a quartz substrate and hard glass, are prepared. Here, preferably, annealing treatment is carried out at inert gas ambient atmospheres, such as N2 (nitrogen), and an about 900-1300-degree C elevated temperature, and it pretreats so that distortion produced in the TFT array substrate 10 in the elevated-temperature process carried out behind may decrease. That is, it is good to heat-treat the TFT array substrate 10 at the same temperature or the temperature beyond it in advance according to the temperature by which high temperature processing is carried out at the maximum elevated temperature in a manufacture process.

[0103] thus, the metal simple substance, the alloy, or metal silicide which contains at least one of Ti, Cr, W, Ta, Mo, Pb(s), etc. which are the conductive refractory metal film all over the processed TFT array substrate 10 -- sputtering -- about 100-500nm thickness -- the light-shielding film 11 of about 200nm thickness is formed preferably.

[0104] Then, as shown in the process (2) of drawing 13 , 1st light-shielding film 11a is formed by performing a photolithography and etching to the this formed light-shielding film 11.

[0105] 1st electric conduction film 116b and 116b' is formed by performing a photolithography and etching to the light-shielding film 11 this formed in coincidence as shown in the process (2) of drawing 11 .

[0106] As shown in the process (3) of drawing 11 and drawing 13 , next, on 1st light-shielding film 11a and 1st electric conduction film 116b With ordinary pressure or a reduced pressure CVD method, for example, TEOS (tetrapod ethyl orthochromatic silicate) gas, The 1st interlayer insulation film 12 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, silicon oxide film, etc. is formed using TEB (tetrapod ethyl boat rate) gas, TMOP (tetrapod methyl oxy-FOSU rate) gas, etc. The thickness of this 1st interlayer insulation film 12 may be about 500-2000nm.

[0107] Next, as shown in the process (4) of drawing 11 and drawing 13 , about 450-550 degrees C of amorphous silicon film are preferably formed comparatively on the 1st interlayer insulation film 12 with the reduced pressure CVD (for example, CVD with a pressure of about 20-40Pa) using the mono-silane gas of flow rate about 400 to 600 cc/min, disilane gas, etc. of about 500 degrees C in a low-temperature environment. Then, in nitrogen-gas-atmosphere mind, by performing annealing treatment of 4 - 6 hours preferably at about 600-700 degrees C for about 1 to 10 hours, solid phase growth of the polish recon film 1 is carried out until it becomes the thickness of about 100nm preferably in about 50-200nm thickness.

[0108] Under the present circumstances, when creating TFT30 for pixel switching of an n channel mold, the impurity ion of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn), may be slightly doped by an ion implantation etc. to the channel field concerned. Moreover, when using TFT30 for pixel switching as a p channel mold, the impurity ion of III group elements, such as B (boron), Ga (gallium), and In (indium), may be slightly doped by an ion implantation etc. In addition, the polish recon film 1 may be directly formed with a reduced pressure CVD method etc. without passing through the amorphous silicon film. Or drive silicon ion into the polish recon film deposited with the reduced pressure CVD method etc., once make it amorphous (amorphous-izing), it is made to recrystallize by annealing treatment etc. after that, and the polish recon film 1 may be formed.

[0109] Next, as shown in the process (5) of drawing 13 , semi-conductor layer 1a of the **** predetermined pattern shown in drawing 2 is formed according to a photolithography process, an etching process, etc. That is, the 1f of the 1st storage capacitance electrodes installed from semi-conductor layer 1a which constitutes TFT30 for pixel switching is formed in the field in which capacity line 3b is formed especially along with scanning-line 3a.

[0110] As shown in the process (6) of drawing 13 , the 1f of the 1st storage capacitance electrodes with semi-conductor layer 1a which constitutes TFT30 for pixel switching next, the temperature of about 900-1300 degrees C, and by oxidizing thermally with the temperature of about 1000 degrees C preferably Form the thermal oxidation silicon film with a comparatively thin thickness of about 30nm, and the high-temperature-oxidation silicon film (HTO film) and a silicon nitride film are further deposited on

the comparatively thin thickness of about 50nm with a reduced pressure CVD method etc. The insulating thin film 2 used as the gate dielectric film of TFT30 for pixel switching and the dielectric film for capacity formation with multilayer structure is formed. consequently, the thickness of semi-conductor layer 1a -- the thickness of about 30-150nm -- desirable -- the thickness of about 35-50nm -- becoming -- the thickness of the insulating thin film 2 -- the thickness of about 20-150nm -- it becomes the thickness of about 30-100nm preferably. Thus, by shortening elevated-temperature thermal oxidation time amount, when using especially an about 8 inches large-sized substrate, the camber by heat can be prevented. However, the insulating thin film 2 may be formed only by oxidizing the polish recon film 1 thermally.

[0111] In addition, although not limited especially in the process (6) of drawing 13 , the part of the 1f of the 1st storage capacitance electrodes may be made to dope and form for example, P ion into low resistance in about 3x1012/cm2 of doses.

[0112] next, contact hole 305a which results in the 1st interlayer insulation film 12 in the process (7) of drawing 11 at 1st electric conduction film 116b and 116b' -- dry etching, such as reactive ion etching and reactant ion beam etching, -- or it forms by wet etching. Under the present circumstances, there is an advantage that the direction which punctured contact hole 305a etc. can make a puncturing configuration almost the same as mask shape by anisotropic etching like reactive ion etching and reactant ion beam etching. However, if it punctures combining dry etching and wet etching, since these contact hole 305a etc. will be made in the shape of a taper, the advantage that the open circuit at the time of wiring connection can be prevented is acquired.

[0113] Next, as shown in the process (8) of drawing 11 and drawing 13 , after depositing the polish recon film 3 with a reduced pressure CVD method etc., thermal diffusion of the P is carried out and the polish recon film 3 is electric-conduction-ized. Or the doped silicon film which introduced P ion into membrane formation and coincidence of the polish recon film 3 may be used.

[0114] Next, as shown in the process (9) of drawing 13 , scanning-line 3a of the **** predetermined pattern shown in drawing 2 R> 2 and capacity line 3b are formed according to a photolithography process, an etching process, etc.

[0115] As shown in the process (9) of drawing 11 at coincidence, 2nd electric conduction film 116a and 116a' which constitutes the junction wiring 116 of the **** predetermined pattern shown in drawing 4 and drawing 5 and drawer wiring 301b is formed.

[0116] Next, as shown in the process (10) of drawing 13 , when TFT30 for pixel switching shown in drawing 3 is set to TFT of an n channel mold with LDD structure, in order to form low concentration source field 1b and low concentration drain field 1c in semi-conductor layer 1a first, the impurity ion 17 of V group elements, such as P, is doped by low concentration by using scanning-line 3a as a diffusion mask (for example, P ion -- the dose of one to 3x1013-/cm2). Thereby, semi-conductor layer 1a under scanning-line 3a becomes channel field 1a'.

[0117] Then, as shown in the process (11) of drawing 13 , in order to form 1d of high concentration source fields and high concentration drain field 1e which constitute TFT30 for pixel switching after forming the resist layer 18 on scanning-line 3a with a mask with width of face wider than the gate electrode which is a part of scanning-line 3a, similarly impurity ion 17' of V group elements, such as P, is doped by high concentration (for example, P ion -- the dose of one to 3x1015-/cm2). Moreover, to semi-conductor layer 1a, when using TFT30 for pixel switching as a p channel mold, in order to form 1d of high concentration source fields, and high concentration drain field 1e in low concentration source field 1b and a low concentration drain field 1c list, the impurity ion of III group elements, such as B, is used and doped. In addition, it is good also as TFT of offset structure, without, for example, performing a low-concentration dope, and it is good also as TFT of a self aryne mold by the ion-implantation technique using P ion, B ion, etc., using scanning-line 3a as a mask.

[0118] In parallel to these processes, the data-line drive circuit 101 with the complementary-type structure which consists of an n channel mold TFT and a p channel mold TFT, and the circumference

circuit of scanning-line drive circuit 104 grade are formed in the periphery on the TFT array substrate 10. Thus, if semi-conductor layer 1a of TFT30 for pixel switching is formed by the polish recon film in this operation gestalt, at the time of formation of TFT30 for pixel switching, it is the same process mostly, and the data-line drive circuit 101 and the circumference circuit of scanning-line drive circuit 104 grade can be formed, and it is advantageous on manufacture.

[0119] Next, as shown in the process (12) of drawing 12 and drawing 14 , the 2nd interlayer insulation film 4 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, silicon oxide film, etc. using TEOS gas etc. with ordinary pressure or a reduced pressure CVD method is formed so that 2nd electric conduction film 116a and 116a' may be superficially covered in capacity line 3b and a scanning-line 3a list with scanning-line 3a in TFT30 for pixel switching. The thickness of the 2nd interlayer insulation film 4 has desirable about 500-1500nm.

[0120] next, the contact hole 5 to data-line in order [to activate 1d of high concentration source fields, and high concentration drain field 1e], and after performing about 1000-degree C annealing treatment about 20 minutes in phase of process (13) of drawing 12 and drawing 14 6a -- dry etching, such as reactive ion etching and reactant ion beam etching, -- or it forms by wet etching. Moreover, contact hole 305b for pulling out with 2nd electric conduction film 116a, and carrying out electrical connection of the wiring 301b is also punctured to the 2nd interlayer insulation film 4 according to the same process as a contact hole 5.

[0121] As shown in the process (14) of drawing 12 and drawing 14 , on the 2nd interlayer insulation film 4 next, by sputtering etc. As it deposits on about 300nm preferably in about 100-500nm thickness by making low resistance metal metallurgy group silicide, such as aluminum of protection-from-light nature, etc. into a metal membrane 6 and is further shown in a process (15) The picture signal line 115 and drawer wiring 301b are formed in a data-line 6a list according to a photolithography process, an etching process, etc.

[0122] Next, as shown in the process (16) of drawing 12 and drawing 14 , the 3rd interlayer insulation film 7 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, silicon oxide film, etc. using TEOS gas etc. with ordinary pressure or a reduced pressure CVD method is formed so that a data-line 6a top may be covered. The thickness of the 3rd interlayer insulation film 7 has desirable about 500-1500nm.

[0123] Next, in the phase of the process (17) of drawing 14 , the contact hole 8 for carrying out electrical connection of pixel electrode 9a and the high concentration drain field 1e is formed by dry etching, such as reactive ion etching and reactant ion beam etching, in TFT30 for pixel switching.

[0124] Next, on the 3rd interlayer insulation film 7, as shown in the process (18) of drawing 12 and drawing 14 , as the transparent conductive thin films 9, such as ITO film, are deposited on the thickness of about 50-200nm and are further shown in the process (19) of drawing 12 and drawing 14 by sputtering etc., pixel electrode 9a is formed according to a photolithography process, an etching process, etc. In addition, when using the liquid crystal equipment concerned for the liquid crystal equipment of a reflective mold, pixel electrode 9a may be formed from an opaque ingredient with high reflection factors, such as aluminum.

[0125] Then, after applying the coating liquid of the orientation film of a polyimide system on pixel electrode 9a, the orientation film 16 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc.

[0126] On the other hand, about the opposite substrate 20 shown in drawing 3 , a glass substrate etc. is prepared first, and after the 2nd light-shielding film 23 and the 3rd light-shielding film 53 (refer to drawing 4 and drawing 5) carry out sputtering of the chromium metal, they are formed through a photolithography process and an etching process. In addition, the 2nd light-shielding film 23 and the 3rd light-shielding film 53 may form others, carbon, and Ti, such as Cr, nickel, and aluminum, from ingredients, such as resin black distributed to the photoresist. [metallic material]

[0127] Then, a counterelectrode 21 is formed by spatter processing etc. all over the opposite substrate

20 by depositing transparent conductive thin films, such as ITO, on the thickness of about 50-200nm. Furthermore, after applying the coating liquid of the orientation film of a polyimide system all over a counterelectrode 21, the orientation film 22 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc.

[0128] Finally, the liquid crystal with which the TFT array substrate 10 and the opposite substrate 20 with which each class was formed as mentioned above are stuck by the sealant so that the orientation film 16 and 22 may meet, and they come to mix two or more kinds of pneumatic liquid crystals to the space between both substrates by vacuum suction etc. is attracted, and the liquid crystal layer 50 of predetermined thickness is formed.

[0129] (The whole liquid crystal equipment configuration) The whole operation gestalt configuration of ** of the liquid crystal equipment constituted as mentioned above is explained with reference to drawing 15 and drawing 16 . In addition, drawing 15 is the top view which looked at the TFT array substrate 10 from the opposite substrate 20 side with each component formed on it, and drawing 16 is a H-H' sectional view of drawing 16 shown including the opposite substrate 20.

[0130] In drawing 15 , on the TFT array substrate 10, the sealant 52 is formed along the edge and the 3rd light-shielding film 53 as a frame which consists of an ingredient which is the same as the 2nd light-shielding film 23, or is different is formed in parallel to the inside. The data-line drive circuit 101 and the external circuit connection terminal 102 are formed in the field of the outside of a sealant 52 along with one side of the TFT array substrate 10, and the scanning-line drive circuit 104 is established in it along with two sides which adjoin this one side. If the scan signal delay supplied to scanning-line 3a does not become a problem, the thing only with one side sufficient [the scanning-line drive circuit 104] cannot be overemphasized. Moreover, the data-line drive circuit 101 may be arranged on both sides along the side of an image display field. For example, the data line of an odd number train supplies a picture signal from the data-line drive circuit arranged along one side of an image display field, and you may make it the data line of an even number train supply a picture signal from the data-line drive circuit arranged along the side of the opposite side of said image display field. Thus, if it is made to drive data-line 6a in the shape of a ctenidium, since the occupancy area of the data-line drive circuit 101 is extensible, it becomes possible to constitute a complicated circuit. Furthermore, two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of an image display field is formed in one side in which the TFT array substrate 10 remains. Moreover, in at least one place of the corner section of the opposite substrate 20, the vertical flow material 106 for taking a flow electrically between the TFT array substrate 10 and the opposite substrate 20 is formed. And as shown in drawing 16 , the opposite substrate 20 with the almost same profile as the sealant 52 shown in drawing 15 has fixed to the TFT array substrate 10 by the sealant 52 concerned.

[0131] On the TFT array substrate 10 of the liquid-crystal equipment in the operation gestalt explained with reference to drawing 16 from drawing 1 above, the precharge circuit which writes in the precharge signal of predetermined potential further to the timing preceded with a picture signal about each data-line 6a for the write-in unloading to data-line 6a of a picture signal may be formed, and the inspection circuit for inspecting the quality of the liquid-crystal equipment concerned at the manufacture middle or the time of shipment, a defect, etc. may be formed. Moreover, you may make it connect with LSI for a drive mounted on the TAB (Tape Automated Bonding) substrate instead of preparing a part of data-line drive circuit 101 and circumference circuit of scanning-line drive circuit 104 grade on the TFT array substrate 10 electrically and mechanically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10. Moreover, according to the exception of modes of operation, such as TN (Twisted Nematic) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, a polarizing plate, etc. are respectively arranged in a predetermined direction at the side in which the outgoing radiation light of the side in which the incident light of the opposite substrate 20 carries out incidence, and the TFT array substrate 10 carries out outgoing radiation.

[0132] Since the liquid crystal equipment in this operation gestalt explained above is applied to an electrochromatic display projector, the liquid crystal equipment of three sheets will be respectively used as a light valve for RGB, and incidence of the light of each color respectively decomposed through the dichroic mirror for RGB color separation will be respectively carried out to each light valve as incident light. Therefore, with this operation gestalt, the color filter is not prepared in the opposite substrate 20. However, the color filter of RGB may be formed in the predetermined field which counters pixel electrode 9a in which the 2nd light-shielding film 23 is not formed on the opposite substrate 20 with the protective coat. If it does in this way, the liquid crystal equipment in an operation gestalt is applicable to electrochromatic display equipments, such as electrochromatic display television of direct viewing types other than a liquid crystal projector, or a reflective mold. Furthermore, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 20. If it does in this way, bright liquid crystal equipment is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 20 again may be formed. According to this opposite substrate with a die clo IKKU filter, brighter electrochromatic display equipment is realizable.

[0133] Although [the liquid crystal equipment in the operation gestalt explained above] incidence of the incident light is carried out from the opposite substrate 20 side as usual, since 1st light-shielding film 11a is prepared, incidence of the incident light is carried out from the TFT array substrate 10 side, and it may be made to carry out outgoing radiation from the opposite substrate 20 side. That is, even if it attaches liquid crystal equipment in a liquid crystal projector in this way, it can prevent light carrying out incidence to channel field 1a' of semi-conductor layer 1a and low concentration source field 1b, and low concentration drain field 1c, and it is possible to display a high-definition image. Here, in order to prevent the reflection by the side of the rear face of the TFT array substrate 10 conventionally, the polarizing plate with which AR (Anti Reflection) coat was carried out for acid resisting needs to be arranged separately, and AR film needed to be stuck. However, with this operation gestalt, since [of the front face of the TFT array substrate 10, and semi-conductor layer 1a] 1st light-shielding film 11a is formed at least between channel field 1a' and low concentration source field 1b, and low concentration drain field 1c, such a polarizing plate and AR film by which AR coat was carried out are used, or the need of using the substrate which carried out AR processing of TFT array substrate 10 itself is lost. Therefore, according to this operation gestalt, ingredient cost can be reduced, and a contaminant, a blemish, etc. do not drop the yield at the time of polarizing plate attachment, and it is very advantageous. Moreover, since lightfastness is excellent, even if it uses the bright light source, or it carries out polarization conversion by the polarization beam splitter and it raises efficiency for light utilization, image quality degradation of the cross talk by light etc. is not produced.

[0134] Moreover, although explained as a switching element prepared in each pixel that it was the poly-Si TFT of a forward stagger mold or a planar mold, the operation gestalt is effective also to TFT of other formats, such as TFT of a reverse stagger mold, and an amorphous silicon TFT.

[0135] (Electronic equipment) Next, the operation gestalt of electronic equipment equipped with the electro-optic device explained to the detail above is explained with reference to drawing 19 from drawing 17 .

[0136] The outline configuration of the electronic equipment which equipped drawing 17 with liquid crystal equipment 100 as an example of an electro-optic device in this way is shown first.

[0137] In drawing 17 , electronic equipment is constituted in preparation for the source 1000 of a display information output, the display information processing circuit 1002, the drive circuit 1004, liquid crystal equipment 100, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM

(Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a picture signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a serial-parallel conversion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the drive circuit 1004 with a clock signal CLK. The drive circuit 1004 drives liquid crystal equipment 100. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes liquid crystal equipment 100, the drive circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.

[0138] Next, the example of the electronic equipment constituted in this way from drawing 18 by drawing 19 is shown respectively.

[0139] Drawing 18 shows an example slack liquid crystal projector 1100 of electronic equipment. Three liquid crystal display modules containing the liquid crystal equipment 100 with which the drive circuit 1004 mentioned above was carried on the TFT array substrate are prepared for this liquid crystal projector 1100, and it is respectively used for it as light valves 100R, 100G, and 100B for RGB. In a liquid crystal projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be respectively led to the light valves 100R, 100G, and 100B corresponding to each color. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors respectively modulated with light valves 100R, 100G, and 100B is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.

[0140] Drawing 19 shows other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic equipment (PC). The liquid crystal equipment 100 mentioned above is formed in the top covering case, and while holding CPU, memory, a modem, etc. further, it has the body 1204 with which the keyboard 1202 was incorporated.

[0141] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 19 from drawing 18 above etc. is mentioned as an example of the electronic equipment shown in drawing 17 .

[0142] As explained above, according to this operation gestalt, various kinds of electronic equipment equipped with the liquid crystal equipment in which high-definition image display with high manufacture effectiveness is possible is realizable.

[0143]

[Effect of the Invention] According to the electro-optic device of this invention, since the picture signal etc. was supplied, even if it raises the drive frequency of an electro-optic device with circumference wiring of junction wiring which low-resisted using the light-shielding film, the potential shake of a picture signal line etc. and the capacity line by capacity coupling with junction wiring etc., a cross talk, a ghost, etc. are reduced, and can perform high-definition image display.

[Translation done.]

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damages caused by the use of this translation.
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the liquid crystal equipment which includes a circumference circuit in equal circuit lists prepared in two or more pixels of the shape of a matrix which constitutes the image formation field in the operation gestalt of liquid crystal equipment, such as various components and wiring.
[Drawing 2] It is the top view of two or more pixel groups where the TFT array substrate with which the data line in the operation gestalt of liquid crystal equipment, the scanning line, the pixel electrode, the light-shielding film, etc. were formed adjoins each other.
[Drawing 3] It is the A-A' sectional view of drawing 2 .
[Drawing 4] It is the part plan of a TFT array substrate in which circumference wiring was prepared.
[Drawing 5] It is the expansion top view expanding and showing junction wiring of drawing 4 , and the drawer wiring section.
[Drawing 6] They are drawing 4 and the B-B' sectional view of drawing 5 .
[Drawing 7] They are drawing 4 and the C-C' sectional view of drawing 5 .
[Drawing 8] It is the sectional view showing the deformation mode in drawing 4 and the B-B' cross section of drawing 5 .
[Drawing 9] It is the sectional view showing the deformation mode in drawing 4 and the C-C' sectional view of drawing 5 .
[Drawing 10] It is the sectional view showing the various modes of junction wiring for sampling circuit drive signal lines in the D-D' cross section of drawing 5 .
[Drawing 11] It is process drawing (the 1) showing order later on about the part corresponding to drawing 6 for the manufacture process of the operation gestalt of liquid crystal equipment.
[Drawing 12] It is process drawing (the 2) showing order later on about the part corresponding to drawing 6 for the manufacture process of the operation gestalt of liquid crystal equipment.
[Drawing 13] It is process drawing (the 1) showing order later on about the part corresponding to drawing 3 for the manufacture process of the operation gestalt of liquid crystal equipment.
[Drawing 14] It is process drawing (the 2) showing order later on about the part corresponding to drawing 3 for the manufacture process of the operation gestalt of liquid crystal equipment.
[Drawing 15] It is the top view which looked at the TFT array substrate in the operation gestalt of liquid crystal equipment from the opposite substrate side with each component formed on it.
[Drawing 16] It is the H-H' sectional view of drawing 15 .
[Drawing 17] It is the block diagram showing the outline configuration of the operation gestalt of the electronic equipment by this invention.
[Drawing 18] It is the sectional view showing a liquid crystal projector as an example of electronic equipment.
[Drawing 19] It is the front view showing a personal computer as other examples of electronic equipment.
[Description of Notations]
1a -- Semi-conductor layer

1a' -- Channel field
1b -- Low concentration source field (source side LDD field)
1c -- Low concentration drain field (drain side LDD field)
1d -- High concentration source field
1e -- High concentration drain field
1f -- The 1st storage capacitance electrode
2 -- Insulating thin film
3a -- Scanning line
3b -- Capacity line
4 -- The 2nd interlayer insulation film
5 -- Contact hole
6a -- Data line
7 -- The 3rd interlayer insulation film
8 -- Contact hole
9a -- Pixel electrode
10 -- TFT array substrate
11a -- The 1st light-shielding film
12 -- The 1st interlayer insulation film
20 -- Opposite substrate
21 -- Counterelectrode
23 -- The 2nd light-shielding film
30 -- TFT
50 -- Liquid crystal layer
52 -- Sealant
53 -- The 3rd light-shielding film
70 -- Storage capacitance
101 -- Data-line drive circuit
103 -- Sampling circuit
104 -- Scanning-line drive circuit
114 -- Sampling circuit drive signal line
115 -- Picture signal line
116 -- Junction wiring
301 401 -- Drawer wiring

[Translation done.]

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審査請求　未請求　請求項の数19　ＯＬ　（全 24 頁）　最終頁に続く

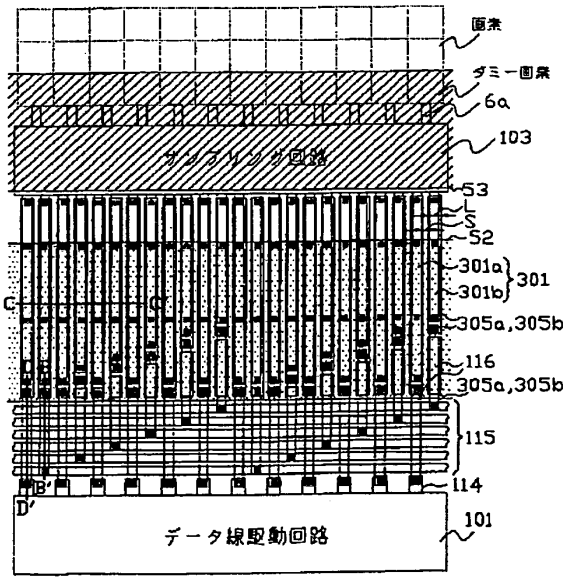
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(54)【発明の名称】　電気光学装置及びその製造方法並びに電子機器

(57)【要約】
【課題】　周辺回路内蔵型の液晶装置等の電気光学装置において、画素部を構成する薄膜の有効利用により周辺回路の入出力配線における電気抵抗を低めて、高品質の画像表示を可能にする。
【解決手段】　液晶装置は、一対の基板間に挟持された液晶層（５０）と、ＴＦＴアレイ基板（１０）にマトリクス状に設けられた画素電極（９ａ）とを備える。高融点金属からなる第１遮光膜（１１ａ）が、画素スイッチング用ＴＦＴ（３０）、走査線（３ａ）、容量線（３ｂ）等の下側に形成されている。画像信号線（１１５）等の周辺配線は、データ線（６ａ）と同じ金属膜からなる第２配線部と、これに立体的に交差可能な、走査線と同じポリシリコン膜及び遮光膜からなる第１配線部とを含む。



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【特許請求の範囲】

【請求項１】　基板上に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆うように配置された導電性の遮光膜と、前記走査線と前記データ線の少なくとも一方に信号を供給するための周辺回路と、前記周辺回路に接続された周辺配線とを備えており、

前記周辺配線は、前記遮光膜を形成する第１導電膜を含む第１配線部と、前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜の少なくとも一つの導電膜を含む第２配線部とを有することを特徴とする電気光学装置。

【請求項２】　前記第１配線部は前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜のうちの少なくとも一つの第２導電膜と前記第１導電膜とを有し、前記第２配線部は前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜のうちの前記第２導電膜とは異なる第３導電膜を含むことを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記第２導電膜は、前記第１導電膜よりも高抵抗であることを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記遮光膜と前記薄膜トランジスタとの間に介在する第１層間絶縁膜と、

前記第２導電膜と前記第３導電膜との間に介在する第２層間絶縁膜とを更に備えており、

前記第１配線部は、前記第２配線部の一部に電気接続されると共に前記第１配線部の他部に対し前記第１及び第２層間絶縁膜を夫々介して立体的に交差する中継配線からなることを特徴とする請求項２又は３に記載の電気光学装置。

【請求項５】　前記周辺配線は、外部回路接続端子から前記画像信号を供給するための画像信号線を含み、

前記周辺回路は、前記画像信号をサンプリングするためのサンプリング回路と、該サンプリング回路を所定タイミングで駆動して前記画像信号線上の前記画像信号を前記サンプリング回路を介して前記複数のデータ線に供給させるデータ線駆動回路と、前記走査線を駆動する走査線駆動回路とを含むことを特徴とする請求項４に記載の電気光学装置。

【請求項６】　前記画像信号は、Ｎ（但し、Ｎは２以上の自然数）シリアルーパラレル変換されており、前記画像信号線は、並列にＮ本設けられており、

該Ｎ本の画像信号線は、相互に交差する箇所において前記中継配線を含むことを特徴とする請求項５に記載の電気光学装置。

【請求項７】　前記データ線駆動回路から前記サンプリング回路にサンプリング回路駆動信号を供給するための

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複数のサンプリング回路駆動信号線を更に備えており、該サンプリング回路駆動信号線は、少なくとも前記画像信号線に交差する箇所が前記中継配線からなることを特徴とする請求項５又は６に記載の電気光学装置。

【請求項８】　前記１配線部を構成する前記第１導電膜及び前記第２導電膜は、前記第１層間絶縁膜に設けられたコンタクトホールを介して相互に電気接続されていることを特徴とする請求項２から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記第３導電膜は前記データ線を形成する金属膜からなり、

前記第２導電膜は前記走査線を形成するポリシリコン膜からなることを特徴とする請求項２から８のいずれか一項に記載の電気光学装置。

【請求項１０】　前記基板に対向する対向基板との間に前記電気光学物質が挟持されて、前記基板と対向基板とはシール材により接着されてなり、

前記シール材に対向する前記基板上のシール領域には、電気光学物質の周囲に渡って少なくとも前記第１導電膜、前記第２導電膜及び前記第３導電膜が積層されており、

前記シール領域を介して引き出される前記データ線及び前記走査線側の引き出し配線部は夫々、前記第１導電膜と第２導電膜と第３導電膜のうちの少なくとも１つからなることを特徴とする請求項２から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記引き出し配線部は夫々、前記第１導電膜と第２導電膜と第３導電膜のうち少なくとも２つが相互にコンタクトホールを介して電気接続されてなることを特徴とする請求項１０に記載の電気光学装置。

【請求項１２】　前記引き出し配線部は夫々、前記第１導電膜と第２導電膜と第３導電膜のうち一つから形成された配線からなり、

前記第１導電膜と第２導電膜と第３導電膜のうち他の２つは、前記シール領域において配線として機能しないダミー配線からなることを特徴とする請求項１０に記載の電気光学装置。

【請求項１３】　前記第１配線部において、前記第１導電膜が前記第２導電膜により覆われていることを特徴とする請求項２から１２のいずれか一項に記載の電気光学装置。

【請求項１４】　前記第１配線部において、前記第１導電膜の配線幅は、前記第２導電膜の配線幅以下であることを特徴とする請求項１３に記載の電気光学装置。

【請求項１５】　基板上に複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、

前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給

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する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えており、前記画像信号線と前記サンプリング回路とを接続する配線の少なくとも一部は、前記遮光膜と同一膜の第１導電膜からなることを特徴とする電気光学装置。

【請求項１６】　前記サンプリング回路にサンプリング回路駆動信号を供給するサンプリング回路駆動信号線の少なくとも一部は、前記第１導電膜からなることを特徴とする請求項１５に記載の電気光学装置。

【請求項１７】　一対の基板間に電気光学物質が挿入されてなり、該一対の基板の一方の基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えた電気光学装置の製造方法において、

前記画像信号線と前記サンプリング回路とを接続する配線の一部となる第１導電膜と前記遮光膜とを同一材料により形成する工程と、

前記第１導電膜及び前記遮光膜の上に第１層間絶縁膜を形成する工程と、

該第１層間絶縁膜上に前記走査線を形成すると共に前記第１層間絶縁膜に形成したコンタクトホールを介して前記第１導電膜に接続される第２導電膜を形成する工程と、

前記走査線及び前記第２導電膜上に第２層間絶縁膜を形成する工程と、

前記第２層間絶縁膜のコンタクトホールを介して前記薄膜トランジスタに接続される前記データ線及び前記第２導電膜に接続される前記画像信号線を形成する工程とを有することを特徴とする電気光学装置の製造方法。

【請求項１８】　一対の基板間に電気光学物質が挿入されてなり、該一対の基板の一方の基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えた電気光学装置の製造方法において、

前記画像信号線と前記サンプリング回路とを接続する配線の一部となる第１導電膜と前記遮光膜とを同一材料により形成する工程と、

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該第１導電膜及び前記遮光膜の上に第１層間絶縁膜を形成する工程と、

該第１層間絶縁膜上に前記薄膜トランジスタのソース及びドレインとなる半導体層、ゲート絶縁膜並びにゲート電極を順次積層形成する工程と、

前記ゲート電極上に第２層間絶縁膜を形成する工程と、

前記第２層間絶縁膜のコンタクトホールを介して前記薄膜トランジスタに接続される前記データ線を形成し、前記第１及び第２層間絶縁膜のコンタクトホールを介して前記第１導電膜に接続される画像信号線を形成する工程とを有することを特徴とする電気光学装置の製造方法。

【請求項１９】　請求項１から１６に記載の電気光学装置を備えたことを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、薄膜トランジスタ（以下適宜、ＴＦＴと称する）によるアクティブマトリクス駆動方式の液晶装置等の電気光学装置及びその製造方法の技術分野に属し、特に、データ線駆動回路や走査線駆動回路などの周辺回路を内蔵する周辺回路内蔵型で、ＴＦＴの下側に遮光膜を設けた形式の液晶装置等の電気光学装置及びその製造方法の技術分野に属する。

【０００２】

【従来の技術】従来、周辺回路内蔵型の液晶装置においては、液晶を挟持する一対の基板の一方であるＴＦＴアレイ基板上に、データ線駆動回路、走査線駆動回路、サンプリング回路などの周辺回路が形成される。これらの周辺回路は、製造効率等の観点より、各画素部に設けられ各画素電極に印加される画像信号のスイッチング制御を行うためのＴＦＴ（以下適宜、画素スイッチング用ＴＦＴと称する）と同一の構造を用いた製造プロセスにより形成されるのが一般的である。そして、ＴＦＴアレイ基板上には、液晶に対向する画像表示領域内に多数のデータ線及び走査線が相交差して配線される。また、この画像表示領域外にあり液晶を封入するためのシール材に対向するシール領域や更にその外側に位置する周辺領域には、周辺回路の入出力配線が配線されている。より具体的には、周辺回路の入出力配線として、データ線、走査線及び容量線からの引き出し配線等がシール領域下に設けられており、外部回路接続端子に接続された画像信号線、制御信号線、電源配線、クロック信号線などが周辺領域に設けられている。

【０００３】特に周辺回路としてサンプリング回路を備えた液晶装置では、外部回路接続端子を介して画像信号が画像信号線に供給されると、データ線駆動回路から所定タイミングで出力されるサンプリング回路駆動信号によりサンプリング回路の各サンプリングスイッチが画像信号をデータ線毎にサンプリングするように構成されている。

【０００４】ここで、画像信号線は、液晶にかける印加

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電圧を規定する画像信号そのものを供給する信号線であるが故に、その画像信号の遅延が低いことが、画質劣化を防ぐ上で極めて重要となる。このため、液晶装置を構成する配線材料のうち最も低抵抗であり、通常はデータ線を形成するのに用いられるＡｌ(アルミニウム)等の金属膜から画像信号線は形成される。

【０００５】これに対し、走査線を金属膜や金属シリサイド膜から形成する技術は、走査線形成後の高温プロセスにおいて、走査線における膜剥れが起きてしまう等の理由から実用化されておらず、走査線は通常ポリシリコン膜で形成される。このポリシリコン膜のシート抵抗は、例えば、Ａｌ等の金属膜からなるシート抵抗と比較して、数十倍になり、配線抵抗が大きくなる。従って、仮にポリシリコン膜から画像信号線を形成した場合には、当該配線抵抗が大きくなることにより信号遅延が生じ、画質劣化が引き起こされるのである。このため実際には、画像信号線は、前述のように金属膜から形成される。

【０００６】このように構成された周辺回路内蔵型の液晶装置では、画像信号線が一本であれば、基板端部に設けられた外部回路接続端子からサンプリング回路の各サンプリングスイッチに至るまで、基板上の同一層にある（即ち、同一工程により形成される）金属膜により配線することが可能である。しかし、例えば液晶装置における高周波駆動に対応すべくシリアルーパラレル変換された画像信号に対しシリアルーパラレル変換数に応じて画像信号線が複数本必要となる場合や、ＲＧＢのカラー画像信号に対し色別に画像信号線が複数本必要となる場合などには、各サンプリングスイッチに至る間に、少なくとも一本の画像信号線が他の画像信号線とどこかで交差せねば配線できないことになる。即ち、同一層にある金属膜のみを用いて複数の画像信号線の全てを配線することは不可能となる。このため、当該金属膜に対し層間絶縁膜を介して別層にあるポリシリコン膜を中継配線（第１配線部）として用いて対処している。より具体的には、交差する箇所では、一方の配線を、低抵抗な金属膜からなる第２配線部として構成する。そして、他方の配線を、層間絶縁膜を介して第２配線部の下又は上を立体的に交差させるように、交差する箇所の前後に開孔されたコンタクトホールを介して金属膜からなる配線部分に電気接続されたポリシリコン膜からなる第１配線部として構成する。

【０００７】以上のように交差する箇所だけをポリシリコン膜からなる第１配線部とし、それ以外の箇所を低抵抗な金属膜からなる第２配線部とすれば、ポリシリコン膜からなる中継配線の長さは、非常に短くて済むため、当該ポリシリコン膜からなる中継配線の存在による画像信号線全体の時定数の上昇が実用上問題となることは殆どなかった。

【０００８】

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【発明が解決しようとする課題】近時の画質向上という一般的要請の下、所謂ＸＧＡ方式、ＳＸＧＡ方式など液晶装置の駆動周波数は益々高くなってきており、これに伴って、シリアルーパラレル変換数も、例えば２４相など、かなり多数になってきている。

【０００９】しかしながら、このように多数にシリアルーパラレル変換すると、並列配置される画像信号線の数も当然に多くなり、これに応じて前述のポリシリコン膜を用いた中継配線の長さは長くなる。ここで、配線抵抗は長さに比例して大きくなるため、中継配線の配線抵抗は高くなり、これに起因して画像信号線の時定数は大きくなってしまい、画質の劣化を引き起こすようになる。例えば、画像信号線の時定数が大きくなると、カップリング容量の増大により画像信号の電位揺れが引き起こされたり、次段のライン（列）に自段のライン（列）用の画像信号が書込まれてゴーストやクロストークが生じたりする問題がある。

【００１０】また仮に、シール領域や周辺領域における中継配線を、画素部では用いられない金属膜等から別途形成するのでは、プレーナ技術を用いた製造プロセスにおける製造効率が低下してコスト上昇を招いてしまい、周辺回路内蔵型の液晶装置の基本的利点が失われかねない。

【００１１】本発明は上述した問題点に鑑みなされたものであり、周辺回路内蔵型の液晶装置等の電気光学装置において、画素部を構成する薄膜の有効利用により周辺回路の入出力配線における電気抵抗が低められており、高品質の画像表示が可能な電気光学装置及びその製造方法を提供することを課題とする。

【００１２】

【課題を解決するための手段】本発明の第１の電気光学装置は上記課題を解決するために、基板上に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆うように配置された導電性の遮光膜と、前記走査線と前記データ線の少なくとも一方に信号を供給するための周辺回路と、前記周辺回路に接続された周辺配線とを備えており、前記周辺配線は、前記遮光膜を形成する第１導電膜を含む第１配線部と、前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜の少なくとも一つの導電膜を含む第２配線部とを有することを特徴とする。

【００１３】本発明の第１の電気光学装置によれば、基板上に遮光膜が薄膜トランジスタの少なくともチャネル領域を平面的に覆うように設けられている。従って、薄膜トランジスタのチャネル領域は、遮光膜により遮光されており、薄膜トランジスタへの光の侵入等による特性劣化を防止できる。本発明では特に、周辺配線は、薄膜トランジスタ、データ線及び走査線を構成する複数の薄

膜層のうちの一つである導電膜からなる第２配線部と、遮光膜と同一膜からなる第１配線部とを有する。例えば、第１導電膜を導電性の高融点金属膜であるＴｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）及びＰｂ（鉛）のうちの少なくとも一つを含む、金属単体、金属又は金属シリサイド層等により形成すれば配線抵抗を顕著に低めることが可能となる。この際、遮光膜は、薄膜トランジスタに対する遮光機能と周辺配線としての機能の両方を兼ね備えるので、構成の簡易化及び製造の単純化を図る上で有利である。

【００１４】以上の結果、低抵抗の周辺配線により、周辺回路における画像信号等の各種の信号の入出力が行われるため、電気光学装置の駆動周波数を高めたり、更にシリアルーパラレル変換数やパラレル入力される画像信号数を増加させたりしても、前述した従来例の如き画像信号線等の周辺配線における容量カップリングによる電位揺れ、ゴースト、クロストークなどは低減され、高品位の画像表示が行うことも可能である。

【００１５】本発明の第１の電気光学装置の一の態様では、前記第１配線部は前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜のうちの少なくとも一つの第２導電膜と前記第１導電膜とを有し、前記第２配線部は前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜のうちの前記第２導電膜とは異なる第３導電膜を含むことを特徴とする。

【００１６】この態様によれば、例えば、第３導電膜が例えば金属膜などの低抵抗な金属膜で、第２導電膜が例えばポリシリコン膜などの第３導電膜よりも高抵抗な薄膜層で形成した場合、できるだけ低抵抗な金属膜からなる第３導電膜により配線を形成することが好ましいが、配線同士が交差する個所は、第２導電膜を配線の一部として用いることがある。その場合、第２導電膜は第３導電膜に比べて抵抗が高いため、信号遅延等の問題が発生する場合がある。そこで、第２導電膜からなる配線の代わりに第１及び第２導電膜を電気接続して二重配線とすることにより、周辺配線自体の抵抗も低めることができる。例えば、第２導電膜をポリシリコン膜から形成し、且つ第１導電膜を導電性の高融点金属膜であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂのうちの少なくとも一つを含む金属単体、合金又は金属シリサイド等により形成すれば、第１配線部の抵抗を第１導電膜のシート抵抗により支配できる。即ち、従来の如くポリシリコン膜単独からなる配線と比較して第１導電膜を電気接続することにより大幅な低抵抗化が可能となる。そして、本発明の第２配線部における抵抗については、例えばＡｌ（アルミニウム）等の第３導電膜を用いることにより低抵抗にできるので、第１配線部と第２配線部とを直列に電気接続した周辺配線を低抵抗化することができる。

【００１７】これに加えて、異物等により第１配線部におけるポリシリコン膜等からなる第２導電膜又は第１導電膜からなる部分が途中で断線しても、他方の部分で導通がとれるという冗長構造が実現できる。

【００１８】尚、本発明の周辺配線は、第１配線部及び第２配線部を有するが、上述の如き第３導電膜を有する第２配線部に対して冗長的な配線を加えて二重、三重等の多重配線としても、当該一重配線部を有することに変わりはなく、更に、上述の如き第１導電膜と第２導電膜を有する第１配線部に対して更に冗長的な配線を加えて三重、四重等の多重配線としても、当該二重配線部を有することに変わりはないことは言うまでもない。

【００１９】本発明の第１の電気光学装置における前記第２導電膜は、前記第１導電膜よりも高抵抗であってよい。

【００２０】このように構成すれば、第３導電膜は、例えばアルミニウム膜など薄膜トランジスタを構成する薄膜層のうち最も低抵抗であり、他方、第２導電膜は、例えばポリシリコン膜など薄膜トランジスタを構成する薄膜層のうち２番目に低抵抗である。第１配線部において第１導電膜により抵抗が低められているので、周辺配線自体の抵抗も低められている。

【００２１】本発明の第１の電気光学装置において、前記遮光膜と前記薄膜トランジスタとの間に介在する第１層間絶縁膜と、前記第２導電膜と前記第３導電膜との間に介在する第２層間絶縁膜とを更に備えており、前記第１配線部は、前記第２配線部の一部に電気接続されると共に前記２重配線部の他部に対し前記第１及び第２層間絶縁膜を夫々介して立体的に交差する中継配線からなる。

【００２２】この態様によれば、中継配線は、第２配線部の一部に電気接続されると共に第２配線部の他部に対し第１及び第２層間絶縁膜を夫々介して立体的に（即ち、上又は下側を）交差する。従って、相互に交差する箇所が必要であり、同一層では配設不可能な周辺配線を、中継配線を介して所望のパターンに配線できる。

【００２３】本発明の第１の電気光学装置において、前記周辺配線は、外部回路接続端子から前記画像信号を供給するための画像信号線を含み、前記周辺回路は、前記画像信号をサンプリングするためのサンプリング回路と、該サンプリング回路を所定タイミングで駆動して前記画像信号線上の前記画像信号を前記サンプリング回路を介して前記複数のデータ線に供給させるデータ線駆動回路と、前記走査線を駆動する走査線駆動回路とを含むように構成してもよい。

【００２４】このように構成すれば、相互に交差する箇所が必要であり、同一層では配設不可能な画像信号線を、中継配線を介して所望のパターンに配線できる。

【００２５】本発明の第１の電気光学装置において、前記画像信号は、Ｎ（但し、Ｎは２以上の自然数）シリアルーパラレル変換されており、前記画像信号線は、並列

にN本設けられており、該N本の画像信号線は、相互に交差する箇所において前記中継配線を含むように構成してもよい。

【００２６】このように構成すれば、例えば、シリアルーパラレル変換数（N）が大きいため或いはＲＧＢのカラー画像信号などの場合のようにパラレル入力される画像信号の数が多いため、中継配線を長くとる必要がある場合や、 前述した従来例の如くポリシリコン膜単独から中継配線を形成した場合と比較して、中継配線の抵抗や時定数の増加を抑えることができる。

【００２７】本発明の第１の電気光学装置において、前記データ線駆動回路から前記サンプリング回路にサンプリング回路駆動信号を供給するための複数のサンプリング回路駆動信号線を更に備えており、該サンプリング回路駆動信号線は、少なくとも前記画像信号線に交差する箇所が前記中継配線からなるように構成してもよい。

【００２８】このように構成すれば、データ線駆動回路からサンプリング回路に至るサンプリング回路駆動信号線を、例えば画像信号線と交差する中継配線を用いて配線することが可能となり、配線レイアウトの自由度が増し、更にこの場合にも、サンプリング回路駆動信号線における中継配線を前述した従来例の如くポリシリコン膜等の第２導電膜単独から形成した場合と比較して、サンプリング回路駆動信号線における時定数の増加を抑えることができる。

【００２９】本発明の第１の電気光学装置において、前記第１配線部を構成する前記第１導電膜及び前記第２導電膜は、前記第１層間絶縁膜に設けられたコンタクトホールを介して相互に電気接続されているように構成してもよい。

【００３０】このように構成すれば、コンタクトホールを介して相互に電気接続された信頼性の高い第１配線部を得ることが出来る。しかも、このようなコンタクトホールは、画素ＴＦＴにおける製造プロセスを利用して比較的容易に形成することが可能である。

【００３１】本発明の第１の電気光学装置において、前記第３導電膜は前記データ線を形成する金属膜からなり、前記第２導電膜は前記走査線を形成するポリシリコン膜からなってよい。

【００３２】このように構成すれば、第２配線部は、例えばアルミニウム等の金属膜から形成されるので、低抵抗化できる。また、ポリシリコン膜からなる部分は金属膜の場合と比較して数十倍程度に高抵抗ではあるが、第１導電膜により二重に配線されば、第１配線部の抵抗は、ポリシリコン膜の抵抗よりも遥かに低抵抗化することが可能となる。例えば、第１導電膜を、導電性の高融点金属膜Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂのうちの少なくとも一つを含む金属膜、合金又は金属シリサイドから形成すれば、ポリシリコン膜単独の場合と比較して、時定数を数分の一（例えば、約１／２や１／３程度に）に低めることが可能となる。

【００３３】本発明の第１の電気光学装置において、前記基板に対向する対向基板との間に電気光学物質が挟持されてなり、前記基板と前記対向基板とはシール材により接着されてなり、前記シール材に対向する前記一方の基板上のシール領域には、前記電気光学物質の周囲に渡って少なくとも前記第１導電膜、前記第２導電膜及び前記第３導電膜が積層されており、前記シール領域を介して前記データ線及び前記走査線の延設方向に引き出される引き出し配線部は夫々、前記第１導電膜と第２導電膜と第３導電膜のうちの少なくとも１つからなってよい。

【００３４】このように構成すれば、シール材により、一対の基板間で電気光学物質が封入され、所謂電気光学物質セルが構成される。ここで、シール領域には、電気光学物質の周囲に渡って少なくとも第１導電膜、第２導電膜及び第３導電膜が積層されているので、シール領域における各種薄膜を含めた両基板間のギャップの電気光学物質の周囲に渡ってのバラツキを抑えることが可能となる。従って、例えば、シール材中に所定外径をもつギャップ材を混入して電気光学物質セルのギャップを制御する場合に、ギャップ制御をより正確且つ良好に行うことが可能となる。そして、シール領域を介してデータ線及び走査線の延設方向にそれぞれ引き出される引き出し配線部は夫々、第１導電膜、第２導電膜及び第３導電膜のうちの少なくとも１つからなるので、画像表示領域内への信号供給を問題無く行うことが可能となる。

【００３５】本発明の第１の電気光学装置におけるシール領域に第１導電膜、第２導電膜及び第３導電膜が積層される態様では、前記引き出し配線部は夫々、前記第１導電膜、第２導電膜及び第３導電膜のうち少なくとも２つが相互にコンタクトホールを介して電気接続された二重又は三重配線部からなるように構成してもよい。このように構成すれば、引き出し配線部における低抵抗化を図れる。

【００３６】或いは、前記引き出し配線部は夫々、前記第１導電膜、第２導電膜及び第３導電膜のうち一つから形成された一重配線部からなり、前記第１導電膜、第２導電膜及び第３導電膜のうち他の２つは、前記シール領域において配線として機能しないダミー配線からなるように構成してもよい。このように構成すれば、ダミー配線の膜厚により比較的簡単にシール領域における両基板間のギャップのバラツキを抑えることが可能となる。

【００３７】本発明の第１の電気光学装置において、前記第１導電膜は前記第２導電膜により覆われる形状を持ってよい。

【００３８】この態様によれば、第１配線部のうち第１導電膜を第２導電膜により平面的に覆うことにより、この第１導電膜からなる部分と交差する、例えば画像信号線などの配線部において、この第１導電膜からなる部分との容量カップリングの増大を抑制できるため、この容

量カップリングによる配線部における時定数の増大を抑制できる。特に、第１導電膜と第２導電膜が介在する構造を採れば、遮光膜を二重配線部に利用した場合の、第１導電膜と第２導電膜との間の容量カップリングの増大を抑制できる。この結果、画像信号線等の配線における画像信号等の劣化を効果的に防止できる。

【００３９】本発明の第１の電気光学装置において、前記第１導電膜の配線幅は、前記第２導電膜からなる部分の配線幅以下であってよい。

【００４０】このように構成すれば、第１導電膜と第２導電膜との間の容量カップリングの増大を確実に抑制できる。

【００４１】本発明の第２の電気光学装置は上記課題を解決するために、基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えており、前記画像信号線と前記サンプリング回路とを接続する配線の少なくとも一部は、前記遮光膜と同一膜の第１導電膜からなる。

【００４２】本発明の第２の電気光学装置によれば、画像信号線とサンプリング回路とを接続する中継配線の少なくとも一部は、導電性の遮光膜と同一膜の第１導電膜からなるので、配線における低抵抗化を図ることが出来る。例えば、第１導電膜を導電性の高融点金属膜により形成すれば、当該中継配線における配線抵抗を顕著に低めることが可能となる。この際、第１導電膜は、薄膜トランジスタに対する遮光機能と配線としての機能の両方を兼ね備えるので、構成の簡易化及び製造の単純化を図る上で有利である。

【００４３】以上の結果、低抵抗の配線により、サンプリング回路における画像信号の入力が行われるため、電気光学装置の駆動周波数を高めたり、更にシリアルーパラレル変換数やパラレル入力される画像信号数を増加させたりしても、前述した従来例の如き画像信号線等の中継配線における容量カップリングによる電位揺れ、ゴースト、クロストークなどは低減され、高品位の画像表示が行える。

【００４４】本発明の第２の電気光学装置の一の態様では、前記サンプリング回路にサンプリング回路駆動信号を供給するサンプリング回路駆動信号線の少なくとも一部は、前記第１導電膜からなる。

【００４５】この態様によれば、サンプリング回路駆動信号線の少なくとも一部は、第１導電膜からなるので、サンプリング回路駆動信号線における低抵抗化を図ることが出来る。この結果、低抵抗のサンプリング回路駆動信号線により、サンプリング回路におけるサンプリング回路駆動信号の入力が行われるため、高品位の画像表示が行える。

【００４６】本発明の第１の電気光学装置の製造方法は上記課題を解決するために、一対の基板間に電気光学物質が挿入されてなり、該一対の基板の一方の基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えた電気光学装置の製造方法において、前記画像信号線と前記サンプリング回路とを接続する配線の一部となる第１導電膜と前記遮光膜とを同一材料により形成する工程と、前記第１導電膜及び前記遮光膜の上に第１層間絶縁膜を形成する工程と、該第１層間絶縁膜上に前記走査線を形成すると共に前記第１層間絶縁膜に形成したコンタクトホールを介して前記第１導電膜に接続される第２導電膜を形成する工程と、前記走査線及び前記第２導電膜上に第２層間絶縁膜を形成する工程と、前記第２層間絶縁膜のコンタクトホールを介して前記薄膜トランジスタに接続される前記データ線及び前記第２導電膜に接続される前記画像信号線を形成する工程とを有する。

【００４７】本発明の第１の電気光学装置の製造方法によれば、画像信号線とサンプリング回路とを接続する第１導電膜と遮光膜とが同一材料により形成される。従って、製造工程の簡略化が図られる。次に、第１導電膜及び遮光膜の上に第１層間絶縁膜が形成され、この第１層間絶縁膜上に走査線が形成され、第１層間絶縁膜に形成したコンタクトホールを介して第１導電膜に接続される第２導電膜が形成される。次に、走査線及び第２導電膜上に第２層間絶縁膜が形成され、第２層間絶縁膜のコンタクトホールを介して薄膜トランジスタに接続されるデータ線及び第２導電膜に接続される画像信号線が形成される。以上の結果、低抵抗の中継配線により、サンプリング回路における画像信号の入力が行われるため、電気光学装置の駆動周波数を高めたり、更にシリアルーパラレル変換数やパラレル入力される画像信号数を増加させたりしても、高品位の画像表示が可能な電気光学装置を製造できる。

【００４８】本発明の第２の電気光学装置の製造方法は上記課題を解決するために、一対の基板間に電気光学物質が挿入されてなり、該一対の基板の一方の基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆

う位置に形成された導電性の遮光膜と、画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えた電気光学装置の製造方法において、前記画像信号線と前記サンプリング回路とを接続する中継配線の少なくとも一部となる第１導電膜と前記遮光膜とを同一材料により形成する工程と、該第１導電膜及び前記遮光膜の上に第１層間絶縁膜を形成する工程と、該第１層間絶縁膜上に前記薄膜トランジスタのソース及びドレインとなる半導体層、ゲート絶縁膜並びにゲート電極を順次積層形成する工程と、前記ゲート電極上に第２層間絶縁膜を形成する工程と、前記第２層間絶縁膜のコンタクトホールを介して前記薄膜トランジスタに接続される前記データ線を形成し、前記第１及び第２層間絶縁膜のコンタクトホールを介して前記第１導電膜に接続される画像信号線を形成する工程とを有する。

【００４９】本発明の第２の電気光学装置の製造方法によれば、画像信号線とサンプリング回路とを接続する第１導電膜と遮光膜とが同一材料により形成される。従って、製造工程の簡略化が図られる。次に、第１導電膜及び遮光膜の上に第１層間絶縁膜が形成され、この第１層間絶縁膜上に、薄膜トランジスタのソース及びドレインとなる半導体層、ゲート絶縁膜並びにゲート電極が順次積層形成され、更に、ゲート電極上に第２層間絶縁膜が形成される。次に、第２層間絶縁膜のコンタクトホールを介して薄膜トランジスタに接続されるデータ線が形成される。次に、第１及び第２層間絶縁膜のコンタクトホールを介して、第１導電膜に接続される画像信号線が形成される。以上の結果、低抵抗の中継配線により、画像信号の入力が行われるため、電気光学装置の駆動周波数を高めたり、更にシリアルーパラレル変換数やパラレル入力される画像信号数を増加させたりしても、高品位の画像表示が可能な電気光学装置を製造できる。

【００５０】本発明の電子機器は、上記の電気光学装置を備えたことを特徴とする。かかる構成によれば、信号遅延を抑えて高品位な画像表示可能な電子機器を提供することができる。

【００５１】本発明のこのような作用及び他の利得は次に説明する実施形態から明らかにする。

【００５２】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。尚、本発明の実施形態では電気光学装置として液晶装置を例として説明する。

【００５３】（液晶装置の構成及び動作）本発明による液晶装置の実施形態の構成及び動作について、図１から図１０を参照して説明する。

【００５４】先ず、液晶装置の回路構成について図１のブロック図を参照して説明する。

【００５５】図１は、液晶装置のＴＦＴアレイ基板上において画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路及び画像表示領域の周辺に位置する周辺回路を示している。

【００５６】図１において、本実施形態による液晶装置の画像表示領域を構成するマトリクス状に形成された複数の画素は、画素電極９ａと画素電極９ａを制御するためのＴＦＴ３０がマトリクス状に複数形成されており、画像信号が供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気接続されている。データ線６ａに書き込む画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給されている。本実施形態では特に、画像信号Ｓ１、Ｓ２、…、Ｓｎは、Ｎ（但し、Ｎは２以上の自然数）相にシリアルーパラレル変換されている。尚、Ｎ本の画像信号線１１５から相隣接するＮ本のデータ線６ａ同士に対してグループ毎に供給するように構成しても良い。このような構成を採れば、データ線駆動回路１０１の駆動周波数を低減でき、信頼性の高い液晶装置を実現できる。

【００５７】また、ＴＦＴ３０のゲートに走査線３ａが電気接続されており、所定のタイミングで、走査線３ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。画素電極９ａを介して電気光学物質としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板（後述する）に形成された対向電極（後述する）との間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能にする。ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として液晶装置からは画像信号に応じたコントラストを持つ光が出射する。ここで、保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極との間に形成される液晶容量と並列に蓄積容量７０を付加する。例えば、画素電極９ａの電圧は、画像信号Ｓ１、Ｓ２、…Ｓｎが供給された時間よりも３桁も長い時間だけ蓄積容量７０により保持される。これにより、保持特性は更に改善され、コントラスト比の高い液晶装置が実現できる。尚、蓄積容量７０を形成する方法としては、容量を形成するための配線である容量線３ｂを設けても良いし、前段の走査線３ａとの間で容量を形成しても良いことは言うまでもない。

【００５８】図１において、液晶装置は、上述のようにデータ線６ａ、走査線３ａ等が形成されたＴＦＴアレイ基板上における画像表示領域の周囲に、周辺回路の例と

して、データ線６ａを駆動するデータ線駆動回路１０１、走査線３ａを駆動する走査線駆動回路１０４及び画像信号をサンプリングするサンプリング回路１０３を備えている。更に、画像表示領域の周囲には、周辺配線の一例として、外部回路接続端子から上述の如きＮ相にシリアルーパラレル変換された画像信号Ｓ１、Ｓ２、…、Ｓｎを供給するためのＮ本の画像信号線１１５が配線されている。

【００５９】このシリアルーパラレル変換数（Ｎ）としては、例えば、当該サンプリング回路１０３におけるサンプリング能力が相対的に高ければ、３相のシリアルーパラレル変換、６相のシリアルーパラレル変換等で足りるし、サンプリング能力が相対的に低ければ、１２相のシリアルーパラレル変換、２４相のシリアルーパラレル変換等が好ましい。

【００６０】ここで特に本実施形態では、後に詳述するようにシリアルーパラレル変換数（Ｎ）即ち画像信号線１１５の本数（Ｎ）に応じて長くなる中継配線１１６を二重配線構造にすることにより低抵抗化しているために、画像信号の信号遅延を効果的に抑えつつ、シリアルーパラレル変換数（Ｎ）及び画像信号線１１５の本数を増やすことが出来、よって画質を劣化させることなく液晶装置の駆動周波数を高められる。尚、このシリアルーパラレル変換数（Ｎ）としては、カラー画像信号が３つの色（赤、青、緑）に係る信号からなることとの関係から３の倍数であると、ＮＴＳＣ表示やＰＡＬ表示等のビデオ表示をする際に制御や回路を簡易化する上で好ましい。

【００６１】上述の如きシリアルーパラレル変換を行わなくても、ＲＧＢのカラー画像信号の場合などのように複数の画像信号線１１５を設ける場合には、以下に説明する本実施形態における低抵抗化された中継配線１１６等に係る構造は有効である。

【００６２】更に本実施形態では、後に詳述するようにデータ線駆動回路１０１からサンプリング回路１０３に至るサンプリング回路駆動信号線１１４の低抵抗化もその二重配線構造により図ることができる。

【００６３】データ線駆動回路１０１は、走査線駆動回路１０４がパルス的に走査線３ａに順番に走査信号を送るのに合わせて、サンプリング回路駆動信号線１１４を介してサンプリング回路駆動信号をサンプリング回路１０３を構成する各サンプリングスイッチ１０３ａの制御端子に供給する。サンプリング回路１０３は、このサンプリング回路駆動信号に応じて、外部回路から画像信号線１１５に供給された画像信号をサンプリングして、データ線６ａに供給する。

【００６４】尚、サンプリング回路１０３を構成する各サンプリングスイッチ１０３ａは、製造効率等の観点から好ましくは、画素部におけるＴＦＴ３０と同一製造プロセスにより製造可能なｎチャネル型、ｐチャネル型、相補型等のＴＦＴから構成される。

【００６５】次に、液晶装置の画像表示領域内における画素部の構成について図２及び図３を参照して説明する。図２は、データ線、走査線、画素電極、遮光膜等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であり、図３は、図２のＡ－Ａ’断面図である。尚、図３においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００６６】図２において、液晶装置のＴＦＴアレイ基板上には、マトリクス状に複数の透明な画素電極９ａ（点線部９ａ’により輪郭が示されている）が設けられており、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ、走査線３ａ及び容量線３ｂが設けられている。データ線６ａは、コンタクトホール５を介して半導体層１ａのうち後述のソース領域に電気接続されており、画素電極９ａは、コンタクトホール８を介して半導体層１ａのうち後述のドレイン領域に電気接続されている。また、半導体層１ａのうち後述のチャネル領域に対向するように走査線３ａが配置されている。そして、図中右上がりの斜線で示した領域に画素部における第１遮光膜１１ａが設けられている。即ち第１遮光膜１１ａは、画素部において、半導体層１ａのチャネル領域を含むＴＦＴをＴＦＴアレイ基板の側から見て各々平面的に覆う位置に設けられている。尚、第１遮光膜１１ａは、少なくとも半導体層１ａのチャネル領域及びチャネル領域とソース・ドレイン領域の接合部を覆えば、画素ＴＦＴにおける光リークの防止機能は発揮されるが、第１遮光膜１１ａを定電位にするための配線機能を持たせるためや画素部の開口領域（即ち、光が透過する領域）を規定するため等の理由から、本実施形態では特に、第１遮光膜１１ａは、走査線３ａに沿って縞状に設けられている。

【００６７】図３に示すように、液晶装置は、透明な一方の基板の一例を構成するＴＦＴアレイ基板１０と、これに対向配置される透明な他方の基板の一例を構成する対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば石英基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９ａは例えば、ＩＴＯ（Indium Tin Oxide)膜などの透明導電性薄膜からなる。また配向膜１６は例えば、ポリイミド薄膜などの有機薄膜からなる。

【００６８】また、ＴＦＴアレイ基板１０には、各画素電極９ａに隣接する位置に、各画素電極９ａをスイッチング制御する画素スイッチング用ＴＦＴ３０が設けられている。

【００６９】他方、対向基板２０には、その全面に渡って対向電極（共通電極）２１が設けられており、その下

側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜２２は、ポリイミド薄膜などの有機薄膜からなる。

【００７０】対向基板２０には、更に図３に示すように、各画素の開口領域以外の領域に第２遮光膜２３が設けられている。このため、対向基板２０の側から入射光が画素スイッチング用ＴＦＴ３０の半導体層１ａのチャネル領域１ａ’やソース側ＬＤＤ（Lightly Doped Drain）領域１ｂ及びドレイン側ＬＤＤ領域１ｃに侵入することはない。更に、第２遮光膜２３は、コントラストの向上、色材の混色防止などの機能を有する。

【００７１】このように構成され、画素電極９ａと対向電極２１とが対面するように配置されたＴＦＴアレイ基板１０と対向基板２０との間には、後述のシール材により囲まれた空間に液晶が封入され、液晶層５０が形成される。液晶層５０は、画素電極９ａからの電界が印加されていない状態で配向膜１６及び２２により所定の配向状態を採る。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、ＴＦＴアレイ基板１０及び対向基板２０をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのグラスファイバー或いはガラスビーズ等のスペーサが混入されている。

【００７２】図３に示すように、画素スイッチング用ＴＦＴ３０に各々対向する位置においてＴＦＴアレイ基板１０と各画素スイッチング用ＴＦＴ３０との間には、第１遮光膜１１ａが各々設けられている。第１遮光膜１１ａは、好ましくは不透明な高融点金属膜であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂのうちの少なくとも一つを含む、金属単体、合金又は、金属シリサイド等から構成される。このような材料から構成すれば、ＴＦＴアレイ基板１０上の第１遮光膜１１ａの形成工程の後に行われる高温処理により、第１遮光膜１１ａが破壊されたり溶融しないようにできる。第１遮光膜１１ａが形成されているので、ＴＦＴアレイ基板１０の側からの戻り光等が画素スイッチング用ＴＦＴ３０のチャネル領域１ａ’や低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃに入射する事態を未然に防ぐことができ、光電流の発生により画素スイッチング用ＴＦＴ３０の特性が劣化することはない。

【００７３】更に、第１遮光膜１１ａと複数の画素スイッチング用ＴＦＴ３０との間には、第１層間絶縁膜１２が設けられている。第１層間絶縁膜１２は、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａを第１遮光膜１１ａから電気絶縁するために設けられるものである。

【００７４】本実施形態では、走査線３ａの一部からなるゲート電極と半導体層１ａとの間に設ける絶縁薄膜２を、走査線３ａに対向する位置から延設して誘電体膜として用い、半導体層１ａを延設して第１蓄積容量電極１ｆとし、更にこれらに対向する容量線３ｂの一部を第２蓄積容量電極とすることにより、蓄積容量７０が構成されている。より詳細には、半導体層１ａの高濃度ドレイン領域１ｅが、データ線６ａ及び走査線３ａの下に延設されて、同じくデータ線６ａ及び走査線３ａに沿って延びる容量線３ｂ部分に絶縁薄膜２を介して対向配置されて、第１蓄積容量電極１ｆとされている。特に蓄積容量７０の誘電体としての絶縁薄膜２は、高温酸化によりポリシリコン膜上に形成されるＴＦＴ３０のゲート絶縁膜に他ならないので、薄く且つ高耐圧の絶縁膜とすることができ、蓄積容量７０は比較的小面積で大容量の蓄積容量として構成できる。

【００７５】図３において、画素スイッチング用ＴＦＴ３０は、ＬＤＤ構造を有しており、走査線３ａ、該走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ’、走査線３ａと半導体層１ａとを絶縁する絶縁薄膜２、データ線６ａ、半導体層１ａの低濃度ソース領域（ソース側ＬＤＤ領域）１ｂ及び低濃度ドレイン領域（ドレイン側ＬＤＤ領域）１ｃ、半導体層１ａの高濃度ソース領域１ｄ並びに高濃度ドレイン領域１ｅを備えている。高濃度ドレイン領域１ｅには、複数の画素電極９ａのうちの対応する一つが接続されている。低濃度ソース領域１ｂ及び高濃度ソース領域１ｄ並びに低濃度ドレイン領域１ｃ及び高濃度ドレイン領域１ｅは後述のように、半導体層１ａに対し、ｎ型又はｐ型のチャネルを形成するかに応じて所定濃度のｎ型用又はｐ型用の不純物イオンをドープすることにより形成されている。ｎ型チャネルのＴＦＴは、動作速度が速いという利点があり、画素のスイッチング素子である画素スイッチング用ＴＦＴ３０として用いられることが多い。本実施形態では特にデータ線６ａは、Ａｌ等の金属膜や金属シリサイド等の合金膜などの遮光性の薄膜から構成されている。また、走査線３ａ、絶縁薄膜２及び第１層間絶縁膜１２の上には、高濃度ソース領域１ｄへ通じるコンタクトホール５及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８が各々形成された第２層間絶縁膜４が形成されている。この高濃度ソース領域１ｄへのコンタクトホール５を介して、データ線６ａは高濃度ソース領域１ｄに電気接続されている。更に、データ線６ａ及び第２層間絶縁膜４の上には、高濃度ドレイン領域１ｅへのコンタクトホール８が形成された第３層間絶縁膜７が形成されている。この高濃度ドレイン領域１ｅへのコンタクトホール８を介して、画素電極９ａは高濃度ドレイン領域１ｅに電気接続されている。前述の画素電極9.aは、このように構成された第３層間絶縁膜７の上面に設けられている。

【００７６】画素スイッチング用ＴＦＴ３０は、好ましくは上述のようにＬＤＤ構造を持つが、低濃度ソース領

域１ｂ及び低濃度ドレイン領域１ｃに不純物イオンの打ち込みを行わないオフセット構造を持ってよいし、走査線３ａの一部からなるゲート電極をマスクとして高濃度で不純物イオンを打ち込み、自己整合的に高濃度ソース領域及び高濃度ドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。

【００７７】また本実施形態では、画素スイッチング用ＴＦＴ３０の走査線３ａの一部からなるゲート電極を高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。この際、各々のゲート電極には同一の信号が印加されるようにする。このようにデュアルゲート（ダブルゲート）或いはトリプルゲート以上でＴＦＴを構成すれば、チャネル領域とソース・ドレイン領域接合部のリーク電流を防止でき、オフ時の電流を低減することができる。これらのゲート電極の少なくとも１個をＬＤＤ構造或いはオフセット構造にすれば、更にオフ電流を低減でき、安定したスイッチング素子を得ることができる。

【００７８】ここで、一般には、半導体層１ａのチャネル領域１ａ’、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ等は、光が入射すると光電変換効果により光電流が発生してしまい画素スイッチング用ＴＦＴ３０のトランジスタ特性が劣化するが、本実施形態では、走査線３ａを上側から重なるようにデータ線６ａがＡｌ等の遮光性の金属膜から形成されているので、少なくとも半導体層１ａのチャネル領域１ａ’及び低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃへの入射光の入射を効果的に防ぐことが出来る。また、前述のように、画素スイッチング用ＴＦＴ３０の下側には、第１遮光膜１１ａが設けられているので、少なくとも半導体層１ａのチャネル領域１ａ’及び低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃへの戻り光の入射を効果的に防ぐことが出来る。

【００７９】尚、本実施形態では特に、第１遮光膜１１ａは定電位源に電気接続されており、定電位とされる。従って、第１遮光膜１１ａに対向配置される画素スイッチング用ＴＦＴ３０に対し第１遮光膜１１ａの電位変動が悪影響を及ぼすことはない。この場合、定電位源としては、当該液晶装置を駆動するための周辺回路（例えば、走査線駆動回路、データ線駆動回路等）に供給される負電源、正電源等の定電位源、接地電源、対向電極２１に供給される定電位源等が挙げられるが、本実施形態では、第１遮光膜１１ａは走査線駆動回路の負電源に接続されるものとする。このように周辺回路等の電源を利用すれば、専用の電位配線や外部回路接続端子を設ける必要なく、第１遮光膜１１ａを定電位にできる。

【００８０】次に、液晶装置の周辺回路における入出力配線或いは周辺配線について、図４から図７を参照して説明する。

【００８１】図４は、周辺配線が設けられたＴＦＴアレイ基板の部分平面図であり、図５は、図４の中継配線及び引き出し配線部を拡大して示す拡大平面図であり、図６は、図４及び図５のＢ－Ｂ’断面図であり、図７は、図４及び図５のＣ－Ｃ’断面図である。

【００８２】図４において、ＴＦＴ基板アレイ基板１０の周辺部に設けられた外部回路接続端子１０２からは、走査線駆動回路１０４に走査線駆動信号線１０５ａが配線されており、データ線駆動回路１０１と液晶を封入するシール材５２が配置されたシール領域との間の領域に、複数の画像信号線１１５が配線されている。

【００８３】そして、図４及び図５に示すように、サンプリング回路１０３は、シール領域よりも内側において、画像表示領域と該画像表示領域外とを仕切るために対向基板２０上に設けられた額縁としての第３遮光膜５３（図中、右上がりの斜線領域）下に配置されている。また、データ線６ａの延長線上におけるシール領域下には、データ線駆動回路１０１からのサンプリング回路駆動信号線１１４の引き出し配線３０１ａ及び画像信号線１１５からの引き出し配線３０１ｂを含むデータ線側の引き出し配線３０１が設けられている。他方、走査線３ａの延長線上におけるシール領域下には、走査線３ａの引き出し配線４０１ａが設けられている。また、容量線３ｂの引き出し配線４０１ｂを設けても良いということは言うまでもない。これら、走査線側の引き出し配線４０１と並列に対向電極電位配線１１２を設置してもよい。この対向電極電位配線１１２は、上下導通端子１０６ａ及び上下導通材１０６を介して対向基板２０に形成された対向電極２１（図３参照）に接続され、共通電位を供給する。また、データ線駆動回路１０１に所定検査用の信号を入力するための検査端子１１１を、データ線駆動回路１０１に隣接して設けても良い。

【００８４】図６のＢ－Ｂ’断面図に示すように、周辺配線の一例たる画像信号線１１５及び引き出し配線３０１ｂは、データ線６ａを形成するのと同一工程で形成されるＡｌ等の金属膜（第３導電膜）で形成されている。他方、画像信号線１１５から引き出し配線３０１ｂに至る中継配線１１６は、走査線３ａを形成するポリシリコン膜と同一膜から形成されておりコンタクトホール３０５ａを介して対応する画像信号線１１５に電気接続された第２導電膜１１６ａ、及び第１遮光膜１１ａと同一膜から形成されておりコンタクトホール３０５ｂを介して中継配線１１６ａに電気接続された第１導電膜１１６ｂにより、ＴＦＴアレイ基板の厚み方向に二重に配線された二重配線構造を有する。また、引き出し配線３０１ｂを更に低抵抗化するため第２導電膜１１６ａ’及び第1導電膜１１６ｂ’を設けても良い。

【００８５】このため、従来の如くポリシリコン膜単独から中継配線を形成する場合と比較して、中継配線１１６における抵抗が導電性の第１導電膜１１６ｂにより低

められている。より具体的には、第１導電膜１１６ｂは、導電性の高融点金属膜であるW、Ｔｉ、Ｃｒ、Ｔａ、Ｍｏ及びＰｂのうちの少なくとも一つを含む、金属単体、合金又は金属シリサイド等から形成されているので、中継配線１１６における配線に沿った方向の抵抗を、第１導電膜１１６ｂのシート抵抗により支配できる。即ち、ポリシリコン膜は、例えば膜厚が３００ｎｍの場合、２５Ω／□程度のシート抵抗値を持つため、対角１．３インチや０．９インチ程度の小型の液晶装置の場合には、１００～２００ＫΩ程度の抵抗を有し、例えば、十数μ秒程度の配線時定数を有するが、第１導電膜１１６ｂはシート抵抗が膜厚２００ｎｍの場合１０Ω／□程度まで低減することができるため、この配線時定数を数μ秒程度にまで小さくすることが可能となる。従って、画像信号線１１５の下を交差して配線された中継配線１１６と画像信号線１１５との容量カップリングによる画像信号の電位揺れで生じる、クロストーク、ゴースト等の発生を低減できる。そして、特に当該液晶装置を前述のようにＸＧＡ、ＳＸＧＡ等の駆動周波数の高い機種として構成することで、シリアルーパラレル変換数（Ｎ）や画像信号線１１５の本数（Ｎ）が増えても、画像信号の信号遅延を抑制できるため、高精細で高品位な液晶装置を実現できる。

【００８６】これに加えて図６から分かるように、異物等により第２導電膜１１６ａ及び第１導電膜１１６ｂの一方が途中で断線しても、他方で導通がとれるという冗長構造が実現されている。しかも、第２導電膜１１６ａ及び第１導電膜１１６ｂが、第1層間絶縁膜１２を突き破って相互にショートしてしまった場合にも、欠陥品とならないで済む。従って、本実施形態によれば、不良品率が低く、信頼性の高い高品位の画像表示が可能な液晶装置を実現できる。しかも、当該中継配線１１６を構築するにあたっては、画素スイッチング用ＴＦＴを遮光するための第1遮光膜１１ａを形成する工程と同一工程で、第１導電膜１１６ｂを形成できるので、工程を増やすことなく、中継配線１１６の低抵抗が実現できる。

【００８７】また、図４及び図５に示したサンプリング回路駆動信号線１１４は、図６に示した中継配線１１６と同様に、画像信号線１１５の下方を交差する二重配線構造を有する。このように構成すれば、従来例の如くポリシリコン膜単独から形成した場合と比較して、サンプリング回路駆動信号線１１４の抵抗や時定数の増加を抑えることができ、高周波数駆動に適用できる。

【００８８】更に図６及び図７に示すように、シール領域下における画像信号線１１５ａからの引き出し配線３０１ｂは、第２導電膜１１６ａ’及び第１導電膜１１６ｂ’が冗長配線として設けられており、三重配線構造を有する。従って、極めて低抵抗の配線とされており、しかも図５に示したようにコンタクトホール３０５ａ及びコンタクトホール３０５ｂによりシール領域下において複数箇所で相互に電気接続されており冗長度が増している。これらの結果、引き出し配線３０１ｂの信頼性は非常に高い。尚、第２導電膜１１６ａ’及び第３導電膜１１６ｂ’のいずれか一方を引き出し配線３０１ｂの冗長配線とする二重配線構造を採用しても、同じ効果が得られる。また、サンプリング回路駆動信号線１１４の引き出し配線３０１ａも同様に、二重或いは三重以上の配線構造を有するように構成してもよい。

【００８９】他方、図４に示した走査線側の引き出し配線４０１は各々、走査線３ａに沿った方向に延びており、相隣接する配線同士は間隔をおいて配列されている。そして、引き出し配線４０１は、走査線３ａと同じポリシリコン膜から構成されており、各引き出し配線４０１の上には、データ線６ａと同じＡｌ膜から構成されたダミー配線が設けられている。尚、走査線側の引き出し配線４０１についての抵抗は通常問題とならないが、上述したデータ線側の引き出し配線３０１の場合と同様に、走査線側の引き出し配線４０１を、二重或いは三重以上の配線構造を有するように構成してもよい。

【００９０】従って、シール領域には、液晶層５０の周囲に渡ってＴＦＴアレイ基板１０上に第１導電膜１１６ｂ、１１６ｂ’、第２導電膜１１６ａ、１１６ａ’、第３導電膜（Ａｌ膜）並びに第1層間絶縁膜１２、第２層間絶縁膜４及び第３層間絶縁膜７を含む積層体が万遍なく形成されていることになり、画像表示領域の上下の辺におけるシール領域における第３層間絶縁膜７の表面の高さと、画像表示領域の左右の辺における第３層間絶縁膜７の表面の高さとは一致するので、シール領域全体における両基板間のギャップのバラツキを抑えることが可能となる。従って、例えば、シール材中に所定外径をもつギャップ材を混入して液晶セルのギャップを制御する場合に、ギャップ制御をより正確且つ良好に行うことが可能となる。特にこのように構成すると、シール領域下においてギャップ材による応力を受けてデータ線側の引き出し配線３０１又は走査線側の引き出し配線４０１が断線しても、多重配線構造のため、致命欠陥とはならない。

【００９１】尚、このようなギャップ制御の目的を重視するのであれば、図６に示したように引き出し配線３０１ｂに対し第２導電膜１１６ａ’及び第１導電膜１１６ｂ’を電気接続するのを止めて、これらの第２導電膜１１６ａ’及び第１導電膜１１６ｂ’をギャップ制御用のダミー配線として構成してもよい。

【００９２】本実施形態では図５に示すように、シール領域において、引き出し配線３０１は、ストライプ状の平面パターンを備えており、夫々幅Ｌを有して相隣接する配線間に配線間隔Ｓに対応する光透過用の隙間が設けられている。従って、光硬化性樹脂からなるシール材５２を用いた場合に、ＴＦＴアレイ基板１０を介して光を入射すれば、この積層構造における光透過用の隙間を通

ってシール材５２に光を十分に照射することが出来る。従って、光硬化性樹脂からなるシール材５２を、両方の基板の側からの光により良好に光硬化させることが出来る。特に、このように光硬化できれば、熱硬化の場合と比べて余分な熱を液晶装置に与えなくて済むので、液晶装置の各構成要素の熱劣化を防いだり、熱歪みによる装置欠陥の発生を防いだり出来るので有利である。また、光照射の時間が少なくて済むため、配向膜１６及び２２（図３参照）にダメージを与えることがない。従って、液晶のティルト角が高いまま維持されるので、液晶の配向不良（ディスクリネーション）による画質劣化を防ぐことが出来る。

【００９３】また、図４及び図５において、額縁としての第３遮光膜５３下には画像表示領域を構成する画素と同一構成を持つダミー画素が形成されている。液晶の配向不良領域等を隠すように設けられた第３遮光膜５３下に表示用の画素を構成する必要は無いが、画像表示領域の縁付近の画素の特性安定化のために、このように画像表示領域の縁よりも外に所定幅だけダミー画素を設けるようにしても良い。

【００９４】更に本実施形態では特に、中継配線１１６は、対向基板側から見て、遮光膜からなる第１導電膜１１６ｂ、１１６ｂ’がポリシリコン膜からなる第２導電膜１１６ａ、１１６ａ’により覆われる形状を持つのが好ましい。より具体的には、例えば図７において、第２導電膜１１６ａ’の配線幅Ｗ１が、第1導電膜１１６ｂ’の配線幅Ｗ２と同じか或いはそれ以上であること、即ち、Ｗ１≧Ｗ２となる関係が、図６に示した画像信号線１１５下及び図７に示したシール領域下で成立するのが好ましい。このように構成すれば、図６において、第1導電膜１１６ｂと画像信号線１１５との間における容量カップリングの増大を抑制でき、この容量カップリングによる画像信号線１１５や中継配線１１６における時定数の増大を抑制できる。特に、交差する個所において、第２導電膜１１６ａが第1導電膜１１６ｂと画像信号線１１５との間に介在し、第1導電膜１１６ｂと画像信号線１１５とは比較的距離を隔てているので、前述の容量カップリングの増大を抑制できる。

【００９５】図６及び図７に示した中継配線１１６は、第２導電膜１１６ａ及び第１導電膜１１６ｂから構成された二重配線構造を採っているが、これらの図に示した二重配線構造における第２導電膜１１６ａ及び１１６ａ’を削除して、図８及び図９に示すように、第１導電膜１１６ｃ及び１１６ｃ’から構成された一重配線構造を採ってもよい。このように構成すれば、冗長構造による利益は得られないが、図６に示した画像信号線１１５下における画像信号線１１５と第１導電膜１１６ｃとの間の容量は、第１層間絶縁膜１２及び第２層間絶縁膜４の間に第２導電膜１１６ａを設けて中継配線１１６を構成する場合と比較して、第１層間絶縁膜１２が存在する分だけ小さくなるので有利である。

【００９６】他方、図４及び図５において、画像信号線１１５は第２層間絶縁膜４上に形成された第３導電膜（Ａｌ膜）から構成されているため、これと交差するデータ線駆動回路１０１から引き出し配線３０１ａに至るサンプリング回路駆動信号線１１４についても、図６や図８に示した中継配線１１６の場合と同様に、Ａｌ膜から構成することはできない。このため、画像信号線１１５の下層又は上層等を通る図１０の如き立体的な中継配線１１６がサンプリング回路駆動信号線１１４用に必要となる。尚、図１０は図５のＤ－Ｄ’に沿った断面図である。また、中継配線１１６はできる限り時定数を下げる工夫が必要である。そこで以下に述べるような方式が考えられる。

【００９７】図１０（１）において、第１導電膜１１６ｄは、第１遮光膜１１ａと同一膜のＷ（タングステン）等の高融点金属膜あるいは金属合金膜等から構成されており、画像信号線１１５と交差するように第１層間絶縁膜１２の下を通されている。そして、画像信号線１１５の両側において第１層間絶縁膜１２及び第２層間絶縁膜４に開孔されたコンタクトホールを介して、データ線駆動回路１０１側のサンプリング回路駆動信号線１１４とシール領域側の引き出し配線３０１ａとを夫々電気接続するように構成されている。このような構成を採れば、中継配線を低抵抗な高融点金属等で形成できるため、配線抵抗を下げることが可能となり、画像信号の遅延を招かない。

【００９８】図１０（２）において、中継配線は、走査線３ａと同一のポリシリコン膜からなる第２導電膜１１６ｅと第１遮光膜１１ａと同一のＷ等の高融点金属膜あるいは金属合金膜等からなる第１導電膜１１６ｄとから構成されており、画像信号線１１５と交差するように第２層間絶縁膜４及び第１層間絶縁膜１２の下を夫々通されている。そして、図で画像信号線１１５の両側において第１層間絶縁膜１２及び第２層間絶縁膜４に夫々開孔されたコンタクトホールを介して、データ線駆動回路１０１側のサンプリング回路駆動信号線１１４とシール領域側の引き出し配線３０１ａとを夫々電気接続するように構成されている。このような構成を採れば、画像信号線１１５の下層に第１層間絶縁膜１２及び第２層間絶縁膜４を介して第１導電膜１１６ｄ及び第２導電膜１１６ｅを形成するため、冗長構造が実現できる。また、第１導電膜１１６ｄは、低抵抗な高融点金属あるいは金属合金膜等からなるため、配線抵抗を下げることが可能となり、画像信号の信号遅延を招かない。尚、第１導電膜１１６ｄと第２導電膜１１６ｅとを直接に電気接続するようにしたが、第１導電膜１１６ｄとサンプリング回路駆動信号線１１４或いはシール領域側の引き出し配線３０１ａと直接に電気接続するようにしてもよい。

【００９９】図１０（３）において、中継配線は、図１

０（２）における冗長構造をなす中継配線とほぼ同様に構成された第１導電膜１１６ｄ及び第２導電膜１１６ｅに加えて、第３層間絶縁膜７上に更に、少なくとも画素開口領域の一部を規定するための高融点金属膜あるいは金属合金膜等からなる第４導電膜１１６ｆが、画像信号線１１５と交差するように通されており、その上に第４層間絶縁膜１１７が形成されている。そして、図で画像信号線１１５の両側において第３層間絶縁膜７に開孔されたコンタクトホールを介して、データ線駆動回路１０１側のサンプリング回路駆動信号線１１４とシール領域側の引き出し配線３０１ａとを第４導電膜１１６ｆと共に夫々電気接続するように構成されている。このような構成を採れば、画像信号線１１５の上下層に第１層間絶縁膜１２、第２層間絶縁膜４及び第３層間絶縁膜７を介して第１導電膜１１６ｄ、第２導電膜１１６ｅ、第４導電膜１１６ｆの３層から中継配線を形成するため、更なる冗長構造が実現できる。また、第１導電膜１１６ｄ及び第４導電膜１１６ｆは、低抵抗な高融点金属膜あるいは金属合金膜等からなるため、配線抵抗をなお一層下げることが可能となり、画像信号の信号遅延を招かない。

【０１００】以上説明したように本実施形態では、画像信号線１１５やサンプリング回路駆動信号線１１４用の中継配線１１６を、第１遮光膜１１ａと同一工程で形成される第１導電膜を利用して低抵抗化したが、本発明の中継配線の適用箇所は、これらの画像信号線１１５やサンプリング回路駆動信号線１１４に限られない。例えば、データ線駆動回路１０１、走査線駆動回路１０４、サンプリング回路１０３等の周辺回路内において、Ａｌ膜からなる配線同士が交差する箇所に層間絶縁膜を介して形成される走査線３ａと同一工程で形成されるポリシリコン膜からなる中継配線などの、周辺回路内の任意の中継配線を第１導電膜を利用して低抵抗化された単層あるいは多重配線に置き換えて構成することが、上述の実施の形態の場合と同様に可能である。特に、データ線駆動回路１０１や走査線駆動回路１０４用の中継配線の低抵抗化は、それらの回路を構成するシフトレジスタの遅延を防ぐことによる駆動の高速化を図ることができる。また、サンプリング回路やプリチャージ回路用の中継配線の低抵抗化は、サンプリング回路駆動信号やプリチャージ回路駆動信号のなまりを抑えることができ、画像信号の良好な書込みが可能となり、最終的には画質向上を図れる。尚、中継配線は２層以上の導電膜から多重配線を構成しても何等問題はない。

【０１０１】（液晶装置の製造プロセス）次に、以上のような構成を持つ液晶装置の実施形態の製造プロセスについて、図１１から図１４を参照して説明する。図１１及び図１２は、各工程におけるＴＦＴアレイ基板側の各層を、図６と同様に図４のＢ－Ｂ’断面に対応させて示す工程図であり、図１３及び図１４は、各工程におけるＴＦＴアレイ基板側の各層を、図３と同様に図２のＡ－Ａ’断面に対応させて示す工程図である。尚、Ｂ－Ｂ断面における製造プロセスとＣ－Ｃ’断面における製造プロセスとは基本的に同時に並行して行われるものであるので、以下の説明も両プロセスについて並列に行う。

【０１０２】図１１及び図１３の工程（１）に示すように、石英基板、ハードガラス等のＴＦＴアレイ基板１０を用意する。ここで、好ましくはN_2（窒素）等の不活性ガス雰囲気且つ約９００～１３００℃の高温でアニール処理し、後に実施される高温プロセスにおけるＴＦＴアレイ基板１０に生じる歪みが少なくなるように前処理しておく。即ち、製造プロセスにおける最高温で高温処理される温度に合わせて、事前にＴＦＴアレイ基板１０を同じ温度かそれ以上の温度で熱処理しておくと良い。

【０１０３】このように処理されたＴＦＴアレイ基板１０の全面に、導電性の高融点金属膜であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂ等のうち少なくとも一つを含む金属単体、合金又は金属シリサイドを、スパッタリングにより、１００～５００ｎｍ程度の膜厚、好ましくは約２００ｎｍの膜厚の遮光膜１１を形成する。

【０１０４】続いて、図１３の工程（２）に示すように、該形成された遮光膜１１にフォトリソグラフィ及びエッチングを行うことにより、第１遮光膜１１ａを形成する。

【０１０５】同時に、図１１の工程（２）に示すように、該形成された遮光膜１１にフォトリソグラフィ及びエッチングを行うことにより、第１導電膜１１６ｂ及び１１６ｂ’を形成する。

【０１０６】次に図１１及び図１３の工程（３）に示すように、第１遮光膜１１ａ及び第１導電膜１１６ｂ上に、例えば、常圧又は減圧ＣＶＤ法等によりＴＥＯＳ（テトラ・エチル・オルソ・シリケート）ガス、ＴＥＢ（テトラ・エチル・ボートレート）ガス、ＴＭＯＰ（テトラ・メチル・オキシ・フォスレート）ガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第１層間絶縁膜１２を形成する。この第１層間絶縁膜１２の膜厚は、例えば、約５００～２０００ｎｍとする。

【０１０７】次に図１１及び図１３の工程（４）に示すように、第１層間絶縁膜１２の上に、約４５０～５５０℃、好ましくは約５００℃の比較的低温環境中で、流量約４００～６００ｃｃ／ｍｉｎのモノシランガス、ジシランガス等を用いた減圧ＣＶＤ（例えば、圧力約２０～４０ＰａのＣＶＤ）により、アモルファスシリコン膜を形成する。その後、窒素雰囲気中で、約６００～７００℃にて約１～１０時間、好ましくは、４～６時間のアニール処理を施すことにより、ポリシリコン膜１を約５０～２００ｎｍの厚さ、好ましくは約１００ｎｍの厚さとなるまで固相成長させる。

【０１０８】この際、ｎチャネル型の画素スイッチング

用ＴＦＴ３０を作成する場合には、当該チャネル領域にＳｂ（アンチモン）、Ａｓ（砒素）、Ｐ（リン）などのＶ族元素の不純物イオンを僅かにイオン注入等によりドープしても良い。また、画素スイッチング用ＴＦＴ３０をｐチャネル型とする場合には、Ｂ（ボロン）、Ｇａ（ガリウム）、Ｉｎ（インジウム）などのIII族元素の不純物イオンを僅かにイオン注入等によりドープしても良い。尚、アモルファスシリコン膜を経ないで、減圧ＣＶＤ法等によりポリシリコン膜１を直接形成しても良い。或いは、減圧ＣＶＤ法等により堆積したポリシリコン膜にシリコンイオンを打ち込んで一旦非晶質化（アモルファス化）し、その後アニール処理等により再結晶化させてポリシリコン膜１を形成しても良い。

【０１０９】次に図１３の工程（５）に示すように、フォトリソグラフィ工程、エッチング工程等により、図２に示した如き所定パターンの半導体層１ａを形成する。即ち、特に走査線３ａに沿って容量線３ｂが形成される領域には、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａから延設された第１蓄積容量電極１ｆを形成する。

【０１１０】次に図１３の工程（６）に示すように、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａと共に第１蓄積容量電極１ｆを約９００～１３００℃の温度、好ましくは約１０００℃の温度により熱酸化することにより、約３０ｎｍの比較的薄い厚さの熱酸化シリコン膜を形成し、更に減圧ＣＶＤ法等により高温酸化シリコン膜（ＨＴＯ膜）や窒化シリコン膜を約５０ｎｍの比較的薄い厚さに堆積し、多層構造を持つ画素スイッチング用ＴＦＴ３０のゲート絶縁膜や容量形成用誘電体膜となる絶縁薄膜２を形成する。この結果、半導体層１ａの厚さは、約３０～１５０ｎｍの厚さ、好ましくは約３５～５０ｎｍの厚さとなり、絶縁薄膜２の厚さは、約２０～１５０ｎｍの厚さ、好ましくは約３０～１００ｎｍの厚さとなる。このように高温熱酸化時間を短くすることにより、特に８インチ程度の大型基板を使用する場合に熱によるそりを防止することができる。但し、ポリシリコン膜１を熱酸化することのみにより、絶縁薄膜２を形成してもよい。

【０１１１】尚、図１３の工程（６）において特に限定されないが、第１蓄積容量電極１ｆの部分に、例えば、Ｐイオンをドーズ量約3×10^{12}／ｃｍ^{2}でドープして、低抵抗化させてもよい。

【０１１２】次に、図１１の工程（７）において、第１層間絶縁膜１２に第１導電膜１１６ｂ及び１１６ｂ’に至るコンタクトホール３０５ａを反応性イオンエッチング、反応性イオンビームエッチング等のドライエッチングにより或いはウエットエッチングにより形成する。この際、反応性イオンエッチング、反応性イオンビームエッチングのような異方性エッチングにより、コンタクトホール３０５ａ等を開孔した方が、開孔形状をマスク形状とほぼ同じにできるという利点がある。但し、ドライエッチングとウエットエッチングとを組み合わせて開孔すれば、これらのコンタクトホール３０５ａ等をテーパ状にできるので、配線接続時の断線を防止できるという利点が得られる。

【０１１３】次に図１１及び図１３の工程（８）に示すように、減圧ＣＶＤ法等によりポリシリコン膜３を堆積した後、Ｐを熱拡散し、ポリシリコン膜３を導電化する。又は、Ｐイオンをポリシリコン膜３の成膜と同時に導入したドープトシリコン膜を用いてもよい。

【０１１４】次に、図１３の工程（９）に示すように、フォトリソグラフィ工程、エッチング工程等により、図２に示した如き所定パターンの走査線３ａ及び容量線３ｂを形成する。

【０１１５】同時に図１１の工程（９）に示すように、図４及び図５に示した如き所定パターンの中継配線１１６及び引き出し配線３０１ｂを構成する第２導電膜１１６ａ及び１１６ａ’を形成する。

【０１１６】次に図１３の工程（１０）に示すように、図３に示した画素スイッチング用ＴＦＴ３０をＬＤＤ構造を持つｎチャネル型のＴＦＴとする場合、半導体層１ａに、先ず低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃを形成するために、走査線３ａを拡散マスクとして、Ｐなどのｖ族元素の不純物イオン１７を低濃度で（例えば、Ｐイオンを$1\sim3\times10^{13}$／ｃｍ^{2}のドーズ量にて）ドープする。これにより走査線３ａ下の半導体層１ａはチャネル領域１ａ’となる。

【０１１７】続いて、図１３の工程（１１）に示すように、画素スイッチング用ＴＦＴ３０を構成する高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを形成するために、走査線３ａの一部であるゲート電極よりも幅の広いマスクでレジスト層１８を走査線３ａ上に形成した後、同じくＰなどのＶ族元素の不純物イオン１７’を高濃度で（例えば、Ｐイオンを$1\sim3\times10^{15}$／ｃｍ^{2}のドーズ量にて）ドープする。また、画素スイッチング用ＴＦＴ３０をｐチャネル型とする場合、半導体層１ａに、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを形成するために、ＢなどのIII族元素の不純物イオンを用いてドープする。尚、例えば、低濃度のドープを行わずに、オフセット構造のＴＦＴとしてもよく、走査線３ａをマスクとして、Ｐイオン、Ｂイオン等を用いたイオン注入技術によりセルフアライン型のＴＦＴとしてもよい。

【０１１８】これらの工程と並行して、ｎチャネル型ＴＦＴ及びｐチャネル型ＴＦＴから構成される相補型構造を持つデータ線駆動回路１０１及び走査線駆動回路１０４等の周辺回路をＴＦＴアレイ基板１０上の周辺部に形成する。このように、本実施形態において画素スイッチング用ＴＦＴ３０の半導体層１ａをポリシリコン膜で形

成すれば、画素スイッチング用ＴＦＴ３０の形成時にほぼ同一工程で、データ線駆動回路１０１及び走査線駆動回路１０４等の周辺回路を形成することができ、製造上有利である。

【０１１９】次に図１２及び図１４の工程（１２）に示すように、画素スイッチング用ＴＦＴ３０における走査線３ａと共に容量線３ｂ及び走査線３ａ並びに第２導電膜１１６ａ及び１１６ａ’を平面的に覆うように、例えば、常圧又は減圧ＣＶＤ法でＴＥＯＳガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第２層間絶縁膜４を形成する。第２層間絶縁膜４の膜厚は、約５００～１５００ｎｍが好ましい。

【０１２０】次に図１２及び図１４の工程（１３）の段階で、高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを活性化するために約１０００℃のアニール処理を２０分程度行った後、データ線６ａに対するコンタクトホール５を、反応性イオンエッチング、反応性イオンビームエッチング等のドライエッチングにより或いはウエットエッチングにより形成する。また、第２導電膜１１６ａと引き出し配線３０１ｂを電気接続するためのコンタクトホール３０５ｂも、コンタクトホール５と同一の工程により第２層間絶縁膜４に開孔する。

【０１２１】次に図１２及び図１４の工程（１４）に示すように、第２層間絶縁膜４の上に、スパッタリング等により、遮光性のＡｌ等の低抵抗金属や金属シリサイド等を金属膜６として、約１００～５００ｎｍの厚さ、好ましくは約３００ｎｍに堆積し、更に工程（１５）に示すように、フォトリソグラフィ工程、エッチング工程等により、データ線６ａ並びに画像信号線１１５及び引き出し配線３０１ｂを形成する。

【０１２２】次に図１２及び図１４の工程（１６）に示すように、データ線６ａ上を覆うように、例えば、常圧又は減圧ＣＶＤ法でＴＥＯＳガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第３層間絶縁膜７を形成する。第３層間絶縁膜７の膜厚は、約５００～１５００ｎｍが好ましい。

【０１２３】次に図１４の工程（１７）の段階において、画素スイッチング用ＴＦＴ３０において、画素電極９ａと高濃度ドレイン領域１ｅとを電気接続するためのコンタクトホール８を、反応性イオンエッチング、反応性イオンビームエッチング等のドライエッチングにより形成する。

【０１２４】次に図１２及び図１４の工程（１８）に示すように、第３層間絶縁膜７の上に、スパッタリング等により、ＩＴＯ膜等の透明導電性薄膜９を、約５０～２００ｎｍの厚さに堆積し、更に図１２及び図１４の工程（１９）に示すように、フォトリソグラフィ工程、エッチング工程等により、画素電極９ａを形成する。尚、当該液晶装置を反射型の液晶装置に用いる場合には、Ａｌ等の反射率の高い不透明な材料から画素電極９ａを形成してもよい。

【０１２５】続いて、画素電極９ａの上にポリイミド系の配向膜の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により、配向膜１６が形成される。

【０１２６】他方、図３に示した対向基板２０については、ガラス基板等が先ず用意され、第２遮光膜２３及び第３遮光膜５３（図４及び図５参照）が、例えば金属クロムをスパッタリングした後、フォトリソグラフィ工程、エッチング工程を経て形成される。尚、第２遮光膜２３及び第３遮光膜５３は、Ｃｒ、Ｎｉ、Ａｌなどの金属材料の他、カーボンやＴｉをフォトレジストに分散した樹脂ブラックなどの材料から形成してもよい。

【０１２７】その後、対向基板２０の全面にスパッタ処理等により、ＩＴＯ等の透明導電性薄膜を、約５０～２００ｎｍの厚さに堆積することにより、対向電極２１を形成する。更に、対向電極２１の全面にポリイミド系の配向膜の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により、配向膜２２が形成される。

【０１２８】最後に、上述のように各層が形成されたＴＦＴアレイ基板１０と対向基板２０とは、配向膜１６及び２２が対面するようにシール材により貼り合わされ、真空吸引等により、両基板間の空間に、例えば複数種類のネマティック液晶を混合してなる液晶が吸引されて、所定膜厚の液晶層５０が形成される。

【０１２９】（液晶装置の全体構成）以上のように構成された液晶装置の各の実施形態の全体構成を図１５及び図１６を参照して説明する。尚、図１５は、ＴＦＴアレイ基板１０をその上に形成された各構成要素と共に対向基板２０の側から見た平面図であり、図１６は、対向基板２０を含めて示す図１６のＨ－Ｈ’断面図である。

【０１３０】図１５において、ＴＦＴアレイ基板１０の上には、シール材５２がその縁に沿って設けられており、その内側に並行して、例えば第２遮光膜２３と同じ或いは異なる材料から成る額縁としての第３遮光膜５３が設けられている。シール材５２の外側の領域には、データ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、走査線駆動回路１０４が、この一辺に隣接する２辺に沿って設けられている。走査線３ａに供給される走査信号遅延が問題にならないのならば、走査線駆動回路１０４は片側だけでも良いことは言うまでもない。また、データ線駆動回路１０１を画像表示領域の辺に沿って両側に配列してもよい。例えば奇数列のデータ線は画像表示領域の一方の辺に沿って配設されたデータ線駆動回路から画像信号を供給し、偶数列のデータ線は前記画像表示領域の反対側の辺に沿って配設されたデータ線駆動回路から

画像信号を供給するようにしてもよい。この様にデータ線６ａを櫛歯状に駆動するようにすれば、データ線駆動回路１０１の占有面積を拡張することができるため、複雑な回路を構成することが可能となる。更にＴＦＴアレイ基板１０の残る一辺には、画像表示領域の両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられている。また、対向基板２０のコーナー部の少なくとも１箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的に導通をとるための上下導通材１０６が設けられている。そして、図１６に示すように、図１５に示したシール材５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材５２によりＴＦＴアレイ基板１０に固着されている。

【０１３１】以上図１から図１６を参照して説明した実施形態における液晶装置のＴＦＴアレイ基板１０上には更に、画像信号のデータ線６ａへの書込み負荷軽減のために各データ線６ａについて画像信号に先行するタイミングで所定電位のプリチャージ信号を書き込むプリチャージ回路を形成してもよいし、製造途中や出荷時の当該液晶装置の品質、欠陥等を検査するための検査回路等を形成してもよい。また、データ線駆動回路１０１、走査線駆動回路１０４等の周辺回路の一部を、ＴＦＴアレイ基板１０の上に設ける代わりに、例えばＴＡＢ（Tape Automated Bonding）基板上に実装された駆動用ＬＳＩに、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して電気的及び機械的に接続するようにしてもよい。また、対向基板２０の投射光が入射する側及びＴＦＴアレイ基板１０の出射光が出射する側には各々、例えば、ＴＮ（ツイステッドネマティック）モード、等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【０１３２】以上説明した本実施形態における液晶装置は、カラー液晶プロジェクタに適用されるため、３枚の液晶装置がＲＧＢ用のライトバルブとして各々用いられ、各ライトバルブには各々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が投射光として各々入射されることになる。従って、本実施形態では、対向基板２０に、カラーフィルタは設けられていない。しかしながら、第２遮光膜２３の形成されていない画素電極９ａに対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２０上に形成してもよい。このようにすれば、液晶プロジェクタ以外の直視型や反射型のカラー液晶テレビなどのカラー液晶装置に実施形態における液晶装置を適用できる。更に、対向基板２０上に１画素1個対応するようにマイクロレンズを形成してもよい。このようにすれば、入射光の集光効率を向上することで、明るい液晶装置が実現できる。更にまた、対向基板２０上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー液晶装置が実現できる。

【０１３３】以上説明した実施形態における液晶装置では、従来と同様に入射光を対向基板２０の側から入射することとしたが、第１遮光膜１１ａを設けているので、ＴＦＴアレイ基板１０の側から入射光を入射し、対向基板２０の側から出射するようにしても良い。即ち、このように液晶装置を液晶プロジェクタに取り付けても、半導体層１ａのチャネル領域１ａ’及び低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃに光が入射することを防ぐことが出来、高画質の画像を表示することが可能である。ここで、従来は、ＴＦＴアレイ基板１０の裏面側での反射を防止するために、反射防止用のＡＲ（Anti Reflection)被膜された偏光板を別途配置したり、ＡＲフィルムを貼り付ける必要があった。しかし、本実施形態では、ＴＦＴアレイ基板１０の表面と半導体層１ａの少なくともチャネル領域１ａ’及び低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃとの間に第１遮光膜１１ａが形成されているため、このようなＡＲ被膜された偏光板やＡＲフィルムを用いたり、ＴＦＴアレイ基板１０そのものをＡＲ処理した基板を使用する必要が無くなる。従って、本実施形態によれば、材料コストを削減でき、また偏光板貼り付け時に、ごみ、傷等により、歩留まりを落とすことがなく大変有利である。また、耐光性が優れているため、明るい光源を使用したり、偏光ビームスプリッタにより偏光変換して、光利用効率を向上させても、光によるクロストーク等の画質劣化を生じない。

【０１３４】また、各画素に設けられるスイッチング素子としては、正スタガ型又はプレーナー型のポリシリコンＴＦＴであるとして説明したが、逆スタガ型のＴＦＴやアモルファスシリコンＴＦＴ等の他の形式のＴＦＴに対しても、実施形態は有効である。

【０１３５】（電子機器）次に、以上詳細に説明した電気光学装置を備えた電子機器の実施形態について図１７から図１９を参照して説明する。

【０１３６】先ず図１７に、このように電気光学装置の一例として液晶装置１００を備えた電子機器の概略構成を示す。

【０１３７】図１７において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、液晶装置１００、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、画像信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回

路１００２は、増幅・極性反転回路、シリアルーパラレル変換回路、ローテーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号CLKと共に駆動回路１００４に出力する。駆動回路１００４は、液晶装置１００を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、液晶装置１００を構成するＴＦＴアレイ基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【０１３８】次に図１８から図１９に、このように構成された電子機器の具体例を各々示す。

【０１３９】図１８は電子機器の一例たる液晶プロジェクタ１１００を示す。この液晶プロジェクタ１１００には、上述した駆動回路１００４がＴＦＴアレイ基板上に搭載された液晶装置１００を含む液晶表示モジュールを３個用意し、各々ＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いられている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂに各々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにより各々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１４０】図１９は電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００を示す。上述した液晶装置１００がトップカバーケース内に設けられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１４１】以上図１８から図１９を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図１７に示した電子機器の例として挙げられる。

【０１４２】以上説明したように、本実施形態によれば、製造効率が高く高品位の画像表示が可能な液晶装置を備えた各種の電子機器を実現できる。

【０１４３】

【発明の効果】本発明の電気光学装置によれば、遮光膜を利用して低抵抗した中継配線等の周辺配線により、画像信号等を供給するようにしたので、電気光学装置の駆動周波数を高めても、画像信号線等と中継配線等との容量カップリングによる容量線の電位揺れ、クロストーク、ゴースト等は低減され、高品位の画像表示が行える。

【図面の簡単な説明】

【図１】液晶装置の実施形態における画像形成領域を構成するマトリクス状の複数の画素に設けられた各種素子、配線等の等価回路並びに周辺回路を含む液晶装置のブロック図である。

【図２】液晶装置の実施形態におけるデータ線、走査線、画素電極、遮光膜等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。

【図３】図２のＡ－Ａ’断面図である。

【図４】周辺配線が設けられたＴＦＴアレイ基板の部分平面図である。

【図５】図４の中継配線及び引き出し配線部を拡大して示す拡大平面図である。

【図６】図４及び図５のＢ－Ｂ’断面図である。

【図７】図４及び図５のＣ－Ｃ’断面図である。

【図８】図４及び図５のＢ－Ｂ’断面における変形態様を示す断面図である。

【図９】図４及び図５のＣ－Ｃ’断面図における変形態様を示す断面図である。

【図１０】図５のＤ－Ｄ’断面におけるサンプリング回路駆動信号線用の中継配線の各種態様を示す断面図である。

【図１１】液晶装置の実施形態の製造プロセスを、図６に対応する部分について順を追って示す工程図（その１）である。

【図１２】液晶装置の実施形態の製造プロセスを、図６に対応する部分について順を追って示す工程図（その２）である。

【図１３】液晶装置の実施形態の製造プロセスを、図３に対応する部分について順を追って示す工程図（その１）である。

【図１４】液晶装置の実施形態の製造プロセスを、図３に対応する部分について順を追って示す工程図（その２）である。

【図１５】液晶装置の実施形態におけるＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図である。

【図１６】図１５のＨ－Ｈ’断面図である。

【図１７】本発明による電子機器の実施形態の概略構成を示すブロック図である。

【図１８】電子機器の一例として液晶プロジェクタを示す断面図である。

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【図１９】電子機器の他の例としてパーソナルコンピュータを示す正面図である。

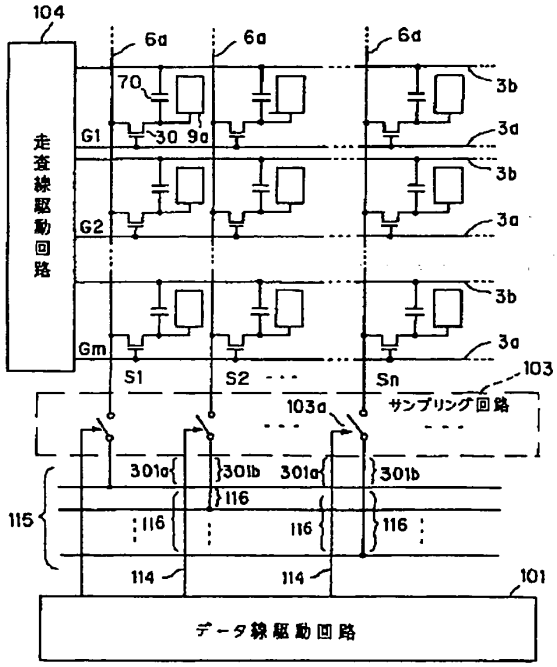
【符号の説明】

１ａ…半導体層
１ａ’…チャネル領域
１ｂ…低濃度ソース領域（ソース側ＬＤＤ領域）
１ｃ…低濃度ドレイン領域（ドレイン側ＬＤＤ領域）
１ｄ…高濃度ソース領域
１ｅ…高濃度ドレイン領域
１ｆ…第１蓄積容量電極
２…絶縁薄膜
３ａ…走査線
３ｂ…容量線
４…第２層間絶縁膜
５…コンタクトホール
６ａ…データ線
７…第３層間絶縁膜
８…コンタクトホール
９ａ…画素電極

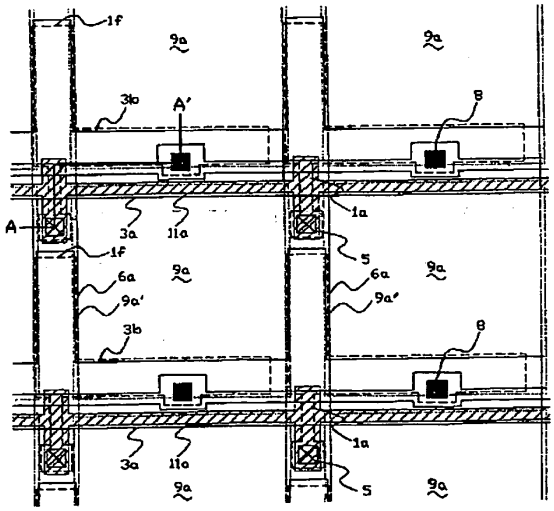
36

１０…ＴＦＴアレイ基板
１１ａ…第１遮光膜
１２…第１層間絶縁膜
２０…対向基板
２１…対向電極
２３…第２遮光膜
３０…ＴＦＴ
５０…液晶層
５２…シール材
５３…第３遮光膜
７０…蓄積容量
１０１…データ線駆動回路
１０３…サンプリング回路
１０４…走査線駆動回路
１１４…サンプリング回路駆動信号線
１１５…画像信号線
１１６…中継配線
３０１、４０１…引き出し配線

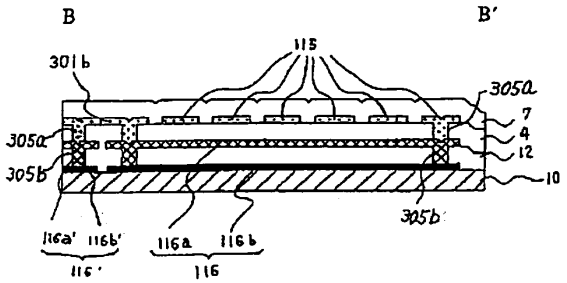
【図１】



【図２】

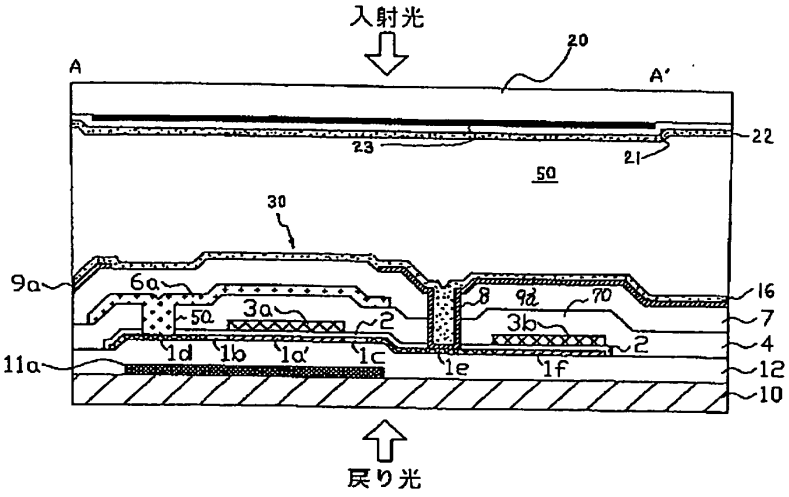


【図６】

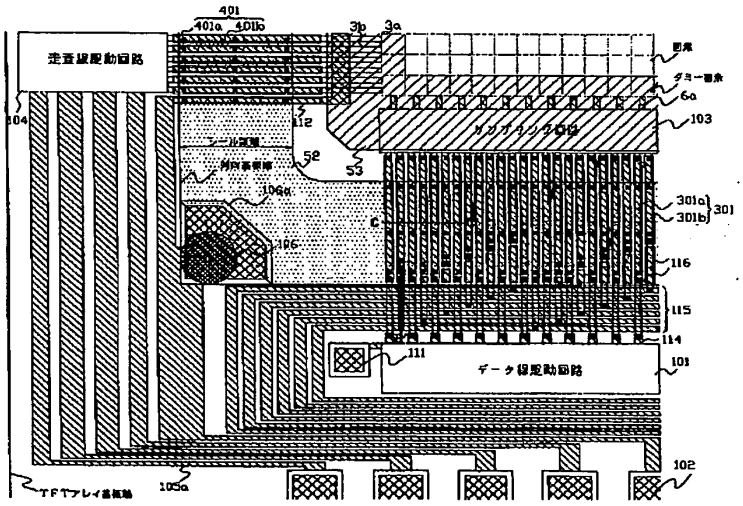


(20)

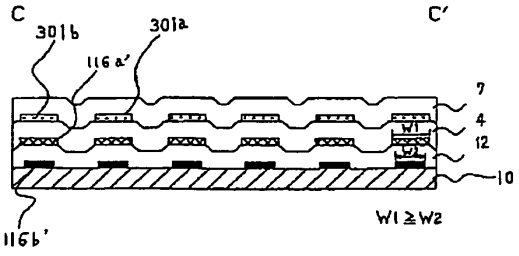
【図３】


入射光
20
A
A'
22
23
21
50
30
9a
6a
5a
3a
2
8
9d
70
16
7
3b
2
4
1d
1b
1a'
1c
1e
1f
12
11a
10
戻り光

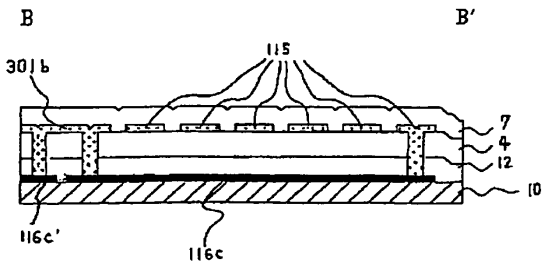
【図４】


401
401a
401b
3b
3a
走査線駆動回路
6a
103
52
53
301a
301b
301
116
115
114
111
データ線駆動回路
101
102
104
105a

【図７】

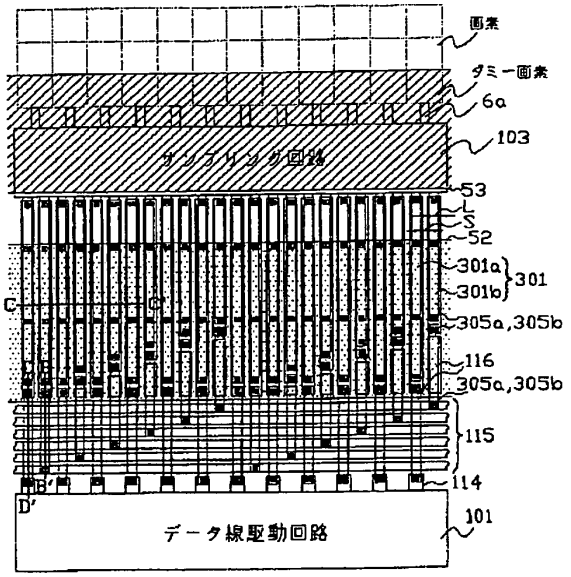

C
C'
301b
301a
116a'
7
4
12
10
W1≧W2
116b'

【図８】

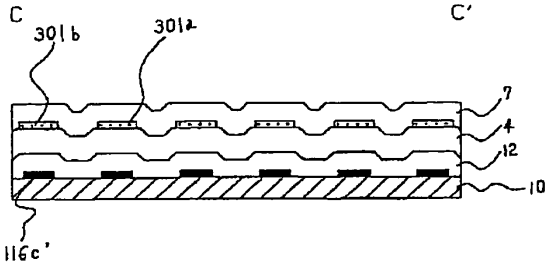

B
B'
115
301b
7
4
12
10
116c'
116c

(21)

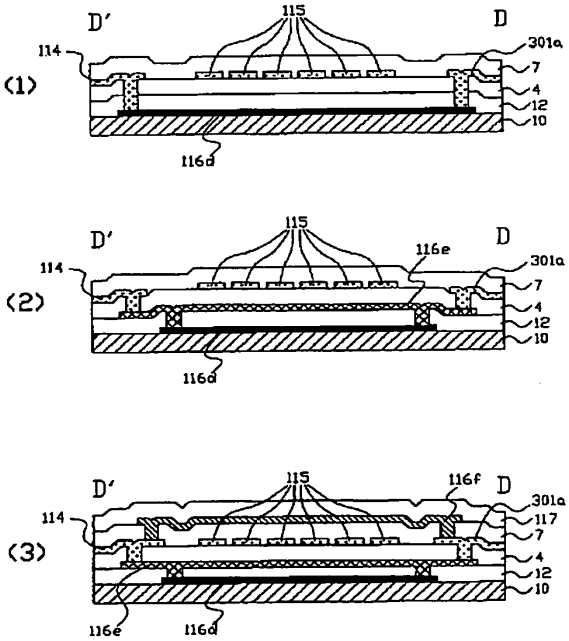
【図５】



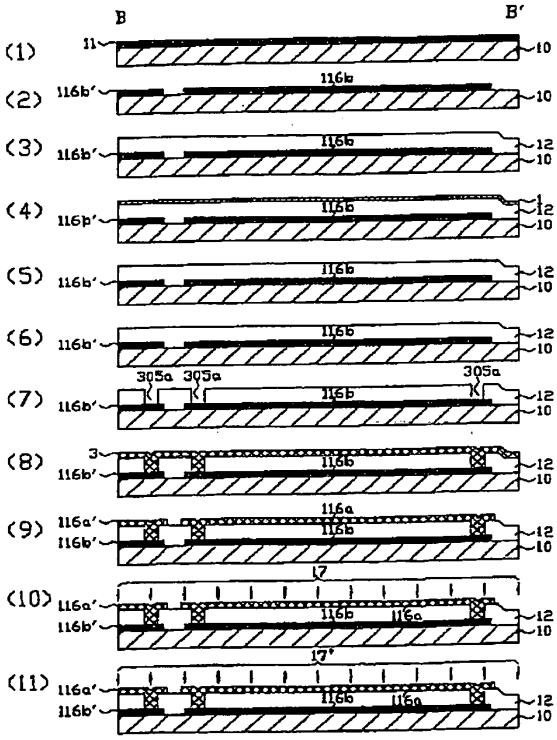
【図９】



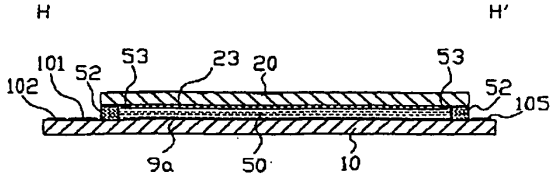
【図１０】



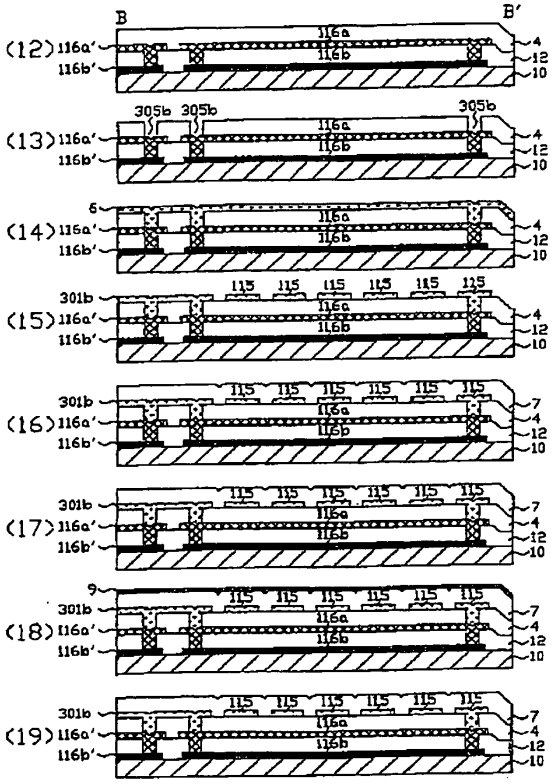
【図１１】



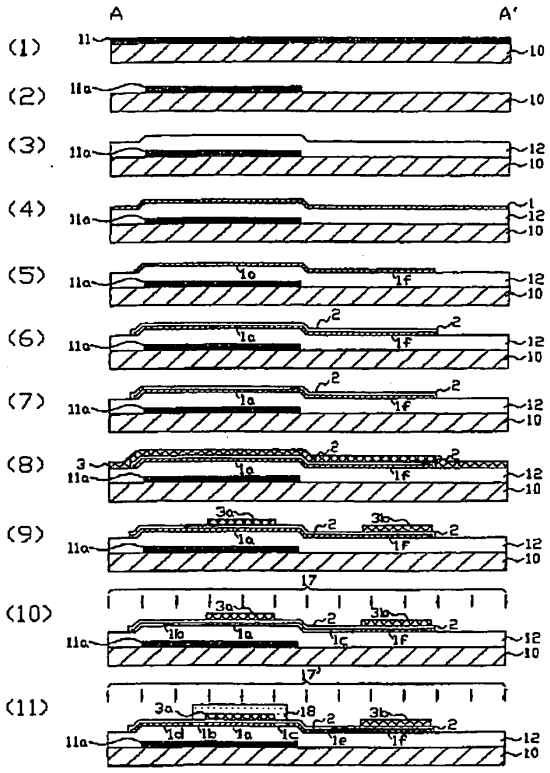
【図１６】



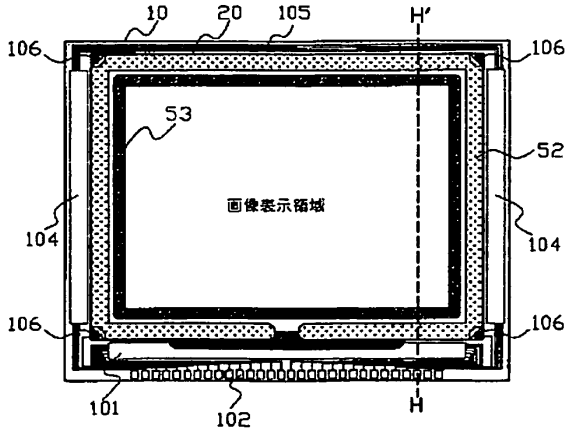
【図１２】



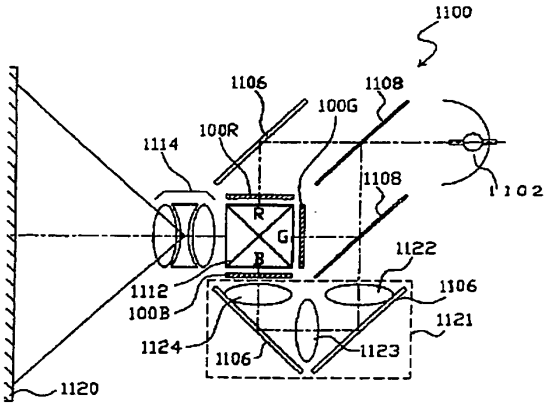
【図１３】



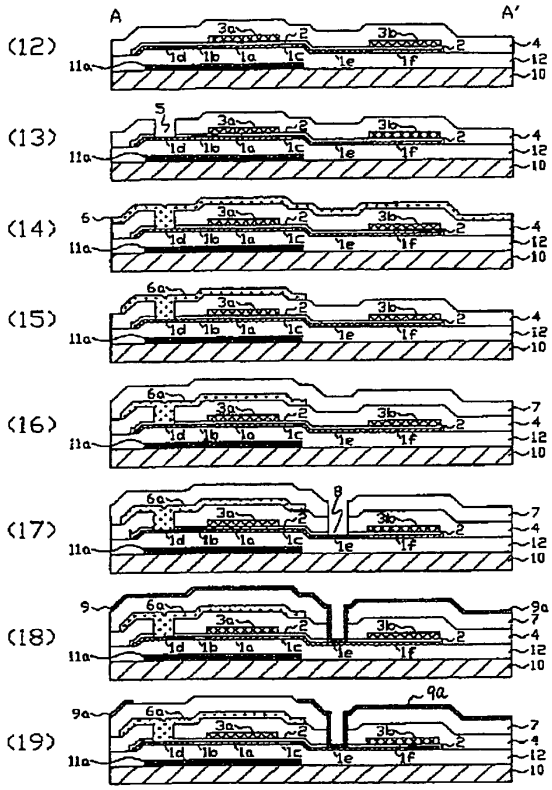
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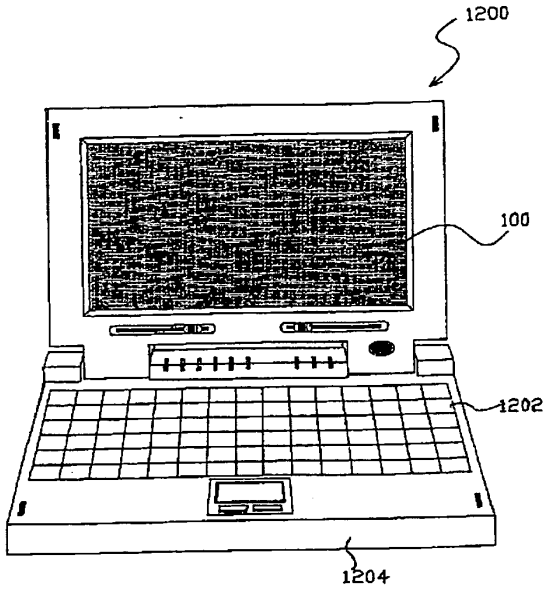
【図１８】



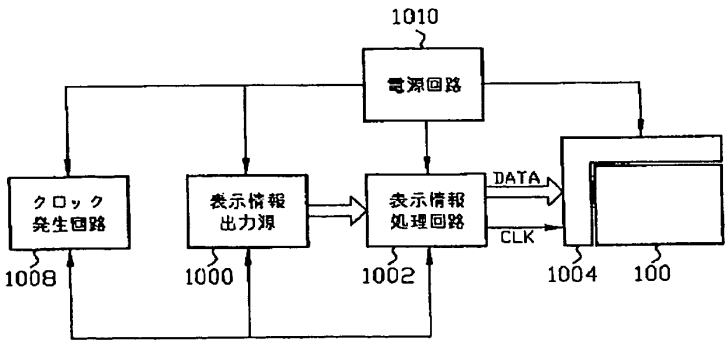
【図１４】



【図１９】



【図１７】



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AA55 BA03 BA43 CA19 DA09
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GB10
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【公報種別】特許法第１７条の２の規定による補正の掲載
【ＳＴ公報種別】A5
【公開日】２０００年（２０００）６月１６日
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G09F 9/30 338
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【手続補正書】
【提出日】２００３年（２００３）６月２３日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】発明の名称
【補正方法】変更
【補正の内容】

【発明の名称】電気光学装置及びその製造方法、ＴＦＴアレイ基板並びに電子機器【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正の内容】

【特許請求の範囲】
【請求項１】
基板上に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に対応して設けられた薄膜トランジスタと、前記薄膜トランジスタに対応して設けられた画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆うように配置された導電性の遮光膜と、前記走査線と前記データ線の少なくとも一方に信号を供給するための周辺回路と、前記周辺回路に接続された周辺配線とを備えており、
前記周辺配線は、前記遮光膜を形成する第１導電膜を含む第１配線部と、前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜の少なくとも一つの導電膜を含む第２配線部とを有することを特徴とする電気光学装置。
【請求項２】
前記第１配線部は前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜のうちの少なくとも一つの第２導電膜と前記第１導電膜とを有し、前記第２配線部は前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜のうちの前記第２導電膜とは異なる第３導電膜を含むことを特徴とする請求項１に記載の電気光学装置。
【請求項３】

前記第２導電膜は、前記第１導電膜よりも高抵抗であることを特徴とする請求項２に記載の電気光学装置。

【請求項４】

前記遮光膜と前記薄膜トランジスタとの間に介在する第１層間絶縁膜と、

前記第２導電膜と前記第３導電膜との間に介在する第２層間絶縁膜と

を更に備えており、

前記第１配線部は、前記第２配線部の一部に電気接続されると共に前記第１配線部の他部に対し前記層間絶縁膜を夫々介して立体的に交差する中継配線からなることを特徴とする請求項２又は３に記載の電気光学装置。

【請求項５】

前記周辺配線は、外部回路接続端子から前記画像信号を供給するための画像信号線を含み、

前記周辺回路は、前記画像信号をサンプリングするためのサンプリング回路と、該サンプリング回路を所定タイミングで駆動して前記画像信号線上の前記画像信号を前記サンプリング回路を介して前記複数のデータ線に供給させるデータ線駆動回路と、前記走査線を駆動する走査線駆動回路とを含むことを特徴とする請求項４に記載の電気光学装置。

【請求項６】

前記画像信号は、Ｎ（但し、Ｎは２以上の自然数）シリアルーパラレル変換されており、前記画像信号線は、並列にＮ本設けられており、該Ｎ本の画像信号線は、相互に交差する箇所において前記中継配線を含むことを特徴とする請求項５に記載の電気光学装置。

【請求項７】

前記データ線駆動回路から前記サンプリング回路にサンプリング回路駆動信号を供給するための複数のサンプリング回路駆動信号線を更に備えており、

該サンプリング回路駆動信号線は、少なくとも前記画像信号線に交差する箇所が前記中継配線からなることを特徴とする請求項５又は６に記載の電気光学装置。

【請求項８】

前記１配線部を構成する前記第１導電膜及び前記第２導電膜は、前記第１層間絶縁膜に設けられたコンタクトホールを介して相互に電気接続されていることを特徴とする請求項２から７のいずれか一項に記載の電気光学装置。

【請求項９】

前記第３導電膜は前記データ線を形成する金属膜からなり、

前記第２導電膜は前記走査線を形成するポリシリコン膜からなることを特徴とする請求項２から８のいずれか一項に記載の電気光学装置。

【請求項１０】

前記基板に対向する対向基板との間に前記電気光学物質が挟持されて、前記基板と対向基板とはシール材により接着されてなり、

前記シール材に対向する前記基板上のシール領域には、電気光学物質の周囲に渡って少なくとも前記第１導電膜、前記第２導電膜及び前記第３導電膜が積層されており、

前記シール領域を介して引き出される前記データ線及び前記走査線側の引き出し配線部は夫々、前記第１導電膜と第２導電膜と第３導電膜のうちの少なくとも１つからなることを特徴とする請求項２から９のいずれか一項に記載の電気光学装置。

【請求項１１】

前記第１配線部において、前記第１導電膜が前記第２導電膜により覆われていることを特徴とする請求項２から１０のいずれか一項に記載の電気光学装置。

【請求項１２】

基板上に複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に対応して設けられた薄膜トランジスタと、

前記薄膜トランジスタに対応して設けられた画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングし

日本国特許庁(JP)
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日本国特許庁(JP)
日本国特許庁(JP)
日本国特許庁(JP)
特許法第17条の2の規定による補正の掲載
日本国特許庁(JP)
特開平11-223832
特開2000-162634

て前記複数のデータ線の各々に供給するサンプリング回路とを備えており、
前記画像信号線と前記サンプリング回路とを接続する配線の少なくとも一部は、前記遮光膜と同一膜の第１導電膜からなることを特徴とする電気光学装置。

【請求項１３】
前記サンプリング回路にサンプリング回路駆動信号を供給するサンプリング回路駆動信号線の少なくとも一部は、前記第１導電膜からなることを特徴とする請求項１２に記載の電気光学装置。

【請求項１４】
基板上に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に対応して設けられた薄膜トランジスタと、前記薄膜トランジスタに対応して設けられた画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆うように配置された導電性の遮光膜と、前記走査線と前記データ線の少なくとも一方に信号を供給するための周辺回路と、前記周辺回路に接続された周辺配線とを備えており、
前記周辺配線は、前記遮光膜を形成する第１導電膜を含む第１配線部と、前記薄膜トランジスタ、前記データ線及び前記走査線を構成する複数の薄膜の少なくとも一つの導電膜を含む第２配線部とを有することを特徴とするＴＦＴアレイ基板。

【請求項１５】
基板上に複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に対応して設けられた薄膜トランジスタと、
前記薄膜トランジスタに対応して設けられた画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えており、
前記画像信号線と前記サンプリング回路とを接続する配線の少なくとも一部は、前記遮光膜と同一膜の第１導電膜からなることを特徴とするＴＦＴアレイ基板。

【請求項１６】
一対の基板間に電気光学物質が挿入されてなり、該一対の基板の一方の基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えた電気光学装置の製造方法において、
前記画像信号線と前記サンプリング回路とを接続する配線の一部となる第１導電膜と前記遮光膜とを同一材料により形成する工程と、
前記第１導電膜及び前記遮光膜の上に第１層間絶縁膜を形成する工程と、
該第１層間絶縁膜上に前記走査線を形成すると共に前記第１層間絶縁膜に形成したコンタクトホールを介して前記第１導電膜に接続される第２導電膜を形成する工程と、
前記走査線及び前記第２導電膜上に第２層間絶縁膜を形成する工程と、
前記第２層間絶縁膜のコンタクトホールを介して前記薄膜トランジスタに接続される前記データ線及び前記第２導電膜に接続される前記画像信号線を形成する工程と
を有することを特徴とする電気光学装置の製造方法。

【請求項１７】
一対の基板間に電気光学物質が挿入されてなり、該一対の基板の一方の基板上には、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタに接続された画素電極と、前記薄膜トランジスタの少なくともチャネル領域を平面的に覆う位置に設けられた導電性の遮光膜と、画像信号を供給する複数の画像信号線と、該複数の画像信号線に供給される前記画像信号をサンプリングして前記複数のデータ線の各々に供給するサンプリング回路とを備えた電気光学装置の製造方法において、

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特許法第17条/2/規定ニヨル補正/掲載
日本国特許庁(JP)
特開平11-223832
特開2000-162634
前記画像信号線と前記サンプリング回路とを接続する配線の一部となる第１導電膜と前記遮光膜とを同一材料により形成する工程と、
該第１導電膜及び前記遮光膜の上に第１層間絶縁膜を形成する工程と、
該第１層間絶縁膜上に前記薄膜トランジスタのソース及びドレインとなる半導体層、ゲート絶縁膜を順次積層形成する工程と、
前記ゲート電極上に第２層間絶縁膜を形成する工程と、
前記第２層間絶縁膜のコンタクトホールを介して前記薄膜トランジスタに接続される前記データ線を形成し、前記第１及び第２層間絶縁膜のコンタクトホールを介して前記第１導電膜に接続される画像信号線を形成する工程と
を有することを特徴とする電気光学装置の製造方法。
【請求項１８】
請求項１から１３に記載の電気光学装置を備えたことを特徴とする電子機器。

PATENT ABSTRACTS OF JAPAN

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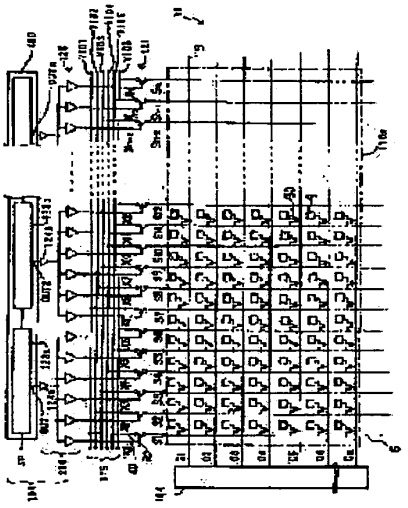
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(54) DRIVING CIRCUIT FOR ELECTROOPTICAL DEVICE AND ELECTROOPTICAL DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide the driving circuit of an electrooptical device capable of obtaining a satisfactory display picture in which a ghost or the like is never generated.

SOLUTION: This device has plural picture signal lines 115 supplying picture signals, sampling switches 121 sampling picture signals to be supplied to the plural signal lines 115 to supply the sampled signals to respective data lines, a shift register 400 outputting sampling control signals commonly by every block consisting of plural sampling switches, first output buffer circuits 124 connected to the output terminals of the shift register 400 and second output buffer circuits 125 connected in parallel with output ends of the first buffer circuits and, moreover, the output ends of the plural buffer circuits 125 are respectively connected to the sampling switches 121 in the respective blocks.



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CLAIMS

[Claim(s)]
[Claim 1] The switching element connected to the data line, two or more scanning lines, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, Two or more sampling switches which sample the picture signal supplied to said two or more picture signal lines, and are supplied to said each data line, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits connected to the outgoing end of each 1st buffer circuit of the above at juxtaposition. Each of the outgoing end of two or more of said 2nd buffer circuits is the drive circuit of the electro-optic device characterized by coming to connect with the sampling switch within said block.
[Claim 2] Each of two or more sampling switches within one block is the drive circuit of the electro-optic device according to claim 1 characterized by coming to connect with the 2nd different buffer circuit.
[Claim 3] Two or more sampling switches within one block are the drive circuits of the electro-optic device according to claim 1 characterized by coming to connect with the 2nd one buffer circuit.
[Claim 4] At least one side of said 1st buffer circuit and said 2nd buffer circuit is the drive circuit of the electro-optic device according to claim 1 or 2 characterized by consisting of an inverter.
[Claim 5] The switching element connected to the data line, two or more scanning lines, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, Two or more sampling switches which sample the picture signal supplied to said two or more picture signal lines, and are supplied to said each data line, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It is the drive circuit of the electro-optic device which has two or more buffer circuits connected to the outgoing end of said shift register at juxtaposition, and is characterized by coming to connect each of the outgoing end of two or more of said buffer circuits with the sampling switch within said block.
[Claim 6] The switching element connected to the data line, two or more scanning lines, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, The sampling switch which samples the picture signal supplied to said two or more picture signal lines, and is supplied to said each data line, Junction wiring which connects said picture signal line and said sampling switch, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits connected to the outgoing end of each 1st buffer circuit of the above at juxtaposition. The sampling control signal line which connects two or more of said 2nd buffer circuit and said sampling switches is the drive circuit of the electro-optic device characterized by coming to cross in a picture signal line

along the gap of said junction wiring.
[Claim 7] The switching element connected to the data line, two or more scanning lines, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, The sampling switch which samples the picture signal supplied to said two or more picture signal lines, and is supplied to said each data line, Junction wiring which connects said picture signal line and said sampling switch, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits connected to the outgoing end of each 1st buffer circuit of the above at juxtaposition. The output line which connects said 1st buffer circuit and said 2nd buffer circuit branches, after crossing said picture signal line, and it is connected to juxtaposition in said two or more 2nd buffer circuits. The sampling control signal supplied from each 2nd buffer circuit of the above is the drive circuit of the electro-optic device characterized by supplying said sampling switch through the sampling control signal line connected to said 2nd buffer circuit.
[Claim 8] Each of two or more sampling switches within one block is the drive circuit of the electro-optic device according to claim 7 characterized by coming to connect with the 2nd different buffer circuit.
[Claim 9] Two or more sampling switches within a block are the drive circuits of the electro-optic device according to claim 7 characterized by coming to connect with the 2nd one buffer circuit.
[Claim 10] The switching element connected to the data line, two or more scanning lines, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, Two or more sampling switches which sample the picture signal supplied to said two or more picture signal lines, and are supplied to said each data line, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the buffer circuit connected to the outgoing end of said shift register at juxtaposition. After the output line which connects the outgoing end and said buffer circuit of said shift register crosses said picture signal line, it branches to plurality and is connected to juxtaposition in said two or more buffer circuits. The sampling control signal supplied from said two or more buffer circuits is the drive circuit of the electro-optic device characterized by supplying said sampling switch through a sampling control signal line.
[Claim 11] The electro-optic device which equipped any 1 term of claim 1 thru/or claim 10 with the drive circuit of the electro-optic device of a publication.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the configuration of the drive circuit used for the electro-optic device of a active-matrix mold etc. It is related with the drive circuit of an electro-optic device and electro-optic device which sample the picture signal from two or more picture signal lines to coincidence, and perform coincidence writing to two or more data lines in detail.
[0002]
[Description of the Prior Art] For example, with the liquid crystal equipment of a active-matrix mold, it has the pixel which consists of a pixel electrode connected to the switching element which consists of a thin film transistor connected to the scanning line, two or more data lines, and two or more each scanning line and each data line, and the switching element as an example of an electro-optic device. Actuation which writes a picture signal in the 1 scanning line at the liquid crystal layer of each pixel through switching elements, such as a thin film transistor by which two or more connection was made, is carried out by point sequential drive.
[0003] It is necessary to carry out sequential switching of the sampling switch prepared for every data line at the rate of a point sequential drive, and to sample a picture signal with such liquid crystal equipment of a active-matrix mold, for an above-mentioned point sequential drive. At this time, the problem that the switching characteristic of a sampling switch cannot fully follow to the frequency of an input picture signal arises. In the case of an indicating equipment with a built-in driver which generally makes a driver circuit to a pixel and coincidence, compared with the case of the indicating equipment which used the external driver, the drive capacity of the thin film transistor for a sampling is low, and becomes more remarkable [the problem]. Moreover, in the case of the high definition display which has many pixels, since the frequency of an input picture signal becomes high, it becomes more remarkable [the above-mentioned problem].
[0004] For this reason, the technique which changes a picture signal into six serial-parallel signals, lengthens the data length per pixel like the liquid crystal equipment shown in drawing 13 , and makes low signal frequency inputted into liquid crystal equipment is indicated. By this serial-parallel conversion, even if the frequency characteristics of the thin film transistor as a sampling switch are not enough, the data length per pixel is lengthened and resolution can be made high.
[0005] Six sampling switches 121 are connected to the buffer 124 which undergoes the output from a shift register 400, respectively, and coincidence constitutes these six sampling switches 121 from liquid crystal equipment of drawing 13 possible [a change]. And he is trying to output at coincidence picture signal VID1-VID6 supplied to the picture signal line 115 by making coincidence turn on every six sampling switches 121 to the six data lines 6 which adjoin each other. By taking such a configuration, spacing of the sampling by the sampling switch 121 can be lengthened, and it also becomes easy to use a thin film transistor as a sampling switch.
[0006]
[Problem(s) to be Solved by the Invention] However, when the configuration of drawing 13 is adopted, the problem of being easy to generate a ghost is in the image of liquid crystal equipment. Generally, the joint structure of a sampling switch and the data line has bad frequency characteristics. Moreover, the phase of the sampling control signal which controls a sampling switch varies. The picture signal which should be written in essentially will be written not only in the block but in the pixel of 1-block beyond by these causes, and a ghost will occur according to them. That is, since there are many sampling switches with which a sampling control signal is supplied to coincidence, **** which must be essentially sampled to the time amount will sample by the time amount which shifted rather than it, and will cause a ghost. If the number of 24 [6, 12,] of the sampling switch especially driven to coincidence increases, the effect on the whole block driven to coincidence will also become large.
[0007] Then, this invention aims at offering the drive circuit of the electro-optic device which can obtain a good display image without a ghost's etc. generating.

[0008]
[Means for Solving the Problem] In order that the drive circuit of the electro-optic device of this invention may solve the above-mentioned technical problem, two or more data lines, The switching element connected to the scanning line, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, Two or more sampling switches which sample the picture signal supplied to said two or more picture signal lines, and are supplied to said each data line, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits connected to the outgoing end of each 1st buffer circuit of the above at juxtaposition. It is characterized by coming to connect each of the outgoing end of two or more of said 2nd buffer circuits with the sampling switch within said block.
[0009] According to the drive circuit of the electro-optic device of this invention, a sampling control signal means has the 1st buffer circuit prepared in common for said every block, and two or more 2nd buffer circuits connected to each 1st buffer circuit, and it comes to supply the output of two or more of said 2nd buffer circuits two or more sampling switches within said block.
[0010] Therefore, since the load in the case of driving a sampling switch through the buffer circuit by which division connection was made as compared with the case that the buffer circuit is connected in common for every block of a sampling switch, to some sampling switches within a block becomes light, the wave-like turbulence of the sampling signal which it is hard coming to mix a noise in the output side of a buffer circuit, and is supplied to a sampling switch can be controlled. For this reason, the voltage variation of the data line resulting from the wave-like turbulence of a sampling control signal can be controlled effectively, and the electro-optic device which does not cause a ghost's etc. image quality degradation can be realized.
[0011] Moreover, since it connects with the outgoing end of a respectively different buffer circuit, the sampling switch to which a sampling control signal is supplied in common can decrease sharply propagation of the sampling control signal between different sampling switches. For this reason, when it originates in the capacity formed in the sampling switch, for example and a sampling switch turns on, even if a noise mixes in a sampling control signal, it is prevented effectively that that noise spreads to the sampling control signal of other sampling switches. Therefore, an electro-optic device has very few ghosts, or an image without a ghost can be displayed on it.
[0012] Each of the sampling switch of the plurality [circuit / of the electro-optic device of this invention / drive] within one block is characterized by coming to connect with the 2nd different buffer circuit.
[0013] According to this mode, a sampling control signal is inputted into each sampling switch through the 2nd buffer circuit prepared independently for every sampling switch. For this reason, since the load in the case of driving a sampling switch becomes very light, it is hard coming to mix a noise in the output side of the 2nd buffer circuit, and the wave-like turbulence of a sampling control signal can be controlled remarkably. Therefore, an electro-optic device can be driven with a sufficient precision.
[0014] Moreover, since it connects with the outgoing end of the 2nd respectively different buffer circuit, the sampling control signal which supplies a sampling control signal to each sampling switch can decrease sharply propagation of the signal between the sampling control signals of a different sampling switch, or can extinguish propagation of such a signal. For this reason, even if a noise mixes between sampling control signal lines, it is prevented effectively that that noise spreads on the sampling control signal line of other sampling switches. Therefore, an electro-optic device has very few ghosts, or an image without a ghost can be displayed on it.
[0015] In one mode of the drive circuit of the electro-optic device by this invention, it is characterized by coming to connect two or more sampling switches within one block with the 2nd one buffer circuit.

[0016] According to this mode, since two or more sampling switches are connected to the 2nd one buffer circuit, it can prevent that the total of the 2nd buffer circuit increases in vain, and a tooth space can be used effectively.
[0017] In one mode of the drive circuit of the electro-optic device by this invention, an inverter is used as said impedance converter.
[0018] According to this mode, since the impedance of the output side of an inverter can be made low, the wave-like turbulence of the sampling control signal line which it is hard coming to mix a noise in a sampling control signal line, and is supplied to each element can be controlled effectively.
[0019] In the drive circuit of the electro-optic device by this invention, in two modes The switching element connected to the data line, two or more scanning lines, and two or more of said each data line and said each scanning line, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the pixel electrode connected to said switching element, and supply a picture signal, Two or more sampling switches which sample the picture signal supplied to said two or more picture signal lines, and are supplied to said each data line, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has two or more buffer circuits connected to the outgoing end of said shift register at juxtaposition, and is characterized by coming to connect each of the outgoing end of two or more of said buffer circuits with the sampling switch within said block.
[0020] Since the load in the case of driving a sampling switch through the buffer circuit by which division connection was made as compared with the case that the buffer circuit is connected in common for every block of a sampling switch, to some sampling switches within a block becomes light according to this mode of this invention, the wave-like turbulence of the sampling signal which it is hard coming to mix a noise in the output side of a buffer circuit, and is supplied to a sampling switch can be controlled. For this reason, the voltage variation of the data line resulting from the wave-like turbulence of a sampling control signal can be controlled effectively, and the electro-optic device which does not cause a ghost's etc. image quality degradation can be realized.
[0021] Moreover, since it connects with the outgoing end of a respectively different buffer circuit, the sampling switch to which a sampling control signal is supplied in common can decrease sharply propagation of the sampling control signal between different sampling switches. For this reason, when it originates in the capacity formed in the sampling switch, for example and a sampling switch turns on, even if a noise mixes in a sampling control signal, it is prevented effectively that that noise spreads to the sampling control signal of other sampling switches. Therefore, an electro-optic device has very few ghosts, or an image without a ghost can be displayed on it.
[0022] The drive circuit of the electro-optic device of this invention Two or more data lines and two or more scanning lines, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the switching element connected to said each data line and said each scanning line, and the pixel electrode connected to said switching element, and supply a picture signal, The sampling switch which samples the picture signal supplied to said two or more picture signal lines, and is supplied to said each data line, Junction wiring which connects said picture signal line and said sampling switch, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits connected to the outgoing end of each 1st buffer circuit of the above at juxtaposition. It is characterized by the sampling control signal line which connects two or more of said 2nd buffer circuit and said sampling switches coming to cross in a picture signal line along the gap of said junction wiring.
[0023] Since the load in the case of driving a sampling switch through the buffer circuit by which division connection was made as compared with the case that the buffer circuit is connected in common for every block of a sampling switch, to some sampling switches within a block becomes light according to this mode of this invention, the wave-like turbulence of the sampling signal which it is hard coming to

mix a noise in the output side of a buffer circuit, and is supplied to a sampling switch can be controlled. For this reason, the voltage variation of the data line resulting from the wave-like turbulence of a sampling control signal can be controlled effectively, and the electro-optic device which does not cause a ghost's etc. image quality degradation can be realized.

[0024] Moreover, since it connects with the outgoing end of a respectively different buffer circuit, the sampling switch to which a sampling control signal is supplied in common can decrease sharply propagation of the sampling control signal between different sampling switches. For this reason, when it originates in the capacity formed in the sampling switch, for example and a sampling switch turns on, even if a noise mixes in a sampling control signal, it is prevented effectively that that noise spreads to the sampling control signal of other sampling switches. Therefore, an electro-optic device has very few ghosts, or an image without a ghost can be displayed on it.

[0025] The drive circuit of the electro-optic device of this invention Two or more data lines and two or more scanning lines, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the switching element connected to said each data line and said each scanning line, and the pixel electrode connected to said switching element, and supply a picture signal, The sampling switch which samples the picture signal supplied to said two or more picture signal lines, and is supplied to said each data line, Junction wiring which connects said picture signal line and said sampling switch, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits connected to the outgoing end of each 1st buffer circuit of the above at juxtaposition. The output line which connects said 1st buffer circuit and said 2nd buffer circuit branches, after crossing said picture signal line, and it is connected to juxtaposition in said two or more 2nd buffer circuits. It is characterized by supplying the sampling control signal supplied to said sampling switch through the sampling control signal line connected to said 2nd buffer circuit from each 2nd buffer circuit of the above.

[0026] According to this mode of this invention, the output line which connects the 1st buffer circuit and the 2nd buffer circuit crosses a picture signal line, and since the 2nd buffer circuit is prepared after crossing, while a sampling control signal can suppress the effect by the picture signal, leading about can be shortened more at wiring. In the drive circuit of the electro-optic device of this invention, each of two or more sampling switches within one block is characterized by coming to connect with the 2nd different buffer circuit.

[0027] According to this mode, a sampling control signal is inputted into each sampling switch through the 2nd buffer circuit prepared independently for every sampling switch. For this reason, since the load in the case of driving a sampling switch becomes very light, it is hard coming to mix a noise in the output side of the 2nd buffer circuit, and the wave-like turbulence of a sampling control signal can be controlled remarkably. Therefore, an electro-optic device can be driven with a sufficient precision.

[0028] Moreover, since it connects with the outgoing end of the 2nd respectively different buffer circuit, the sampling control signal which supplies a sampling control signal to each sampling switch can decrease sharply propagation of the signal between the sampling control signals of a different sampling switch, or can extinguish propagation of such a signal. For this reason, even if a noise mixes between sampling control signal lines, it is prevented effectively that that noise spreads on the sampling control signal line of other sampling switches. Therefore, an electro-optic device has very few ghosts, or an image without a ghost can be displayed on it.

[0029] In the drive circuit of the electro-optic device by this invention, it is characterized by coming to connect two or more sampling switches within one block with the 2nd one buffer circuit.

[0030] According to this mode, since two or more sampling switches are connected to the 2nd one buffer circuit, it can prevent that the total of the 2nd buffer circuit increases in vain, and a tooth space can be used effectively.

[0031] The drive circuit of the electro-optic device of this invention Two or more data lines and two or

more scanning lines, Two or more picture signal lines which are the drive circuits of the electro-optic device which has the switching element connected to said each data line and said each scanning line, and the pixel electrode connected to said switching element, and supply a picture signal, Two or more sampling switches which sample the picture signal supplied to said two or more picture signal lines, and are supplied to said each data line, The shift register which consists of two or more sampling switches and which outputs a transfer signal in common for every block, It has the buffer circuit connected to the outgoing end of said shift register at juxtaposition. After the output line which connects the outgoing end and said buffer circuit of said shift register crosses said picture signal line, it branches to plurality and is connected to juxtaposition in said two or more buffer circuits. It is characterized by supplying the sampling control signal supplied to said sampling switch through a sampling control signal line from said two or more buffer circuits.

[0032] According to this mode of this invention, the output line which connects the outgoing end and buffer circuit of a shift register crosses a picture signal line, and since the buffer circuit is prepared after crossing, while being able to suppress the effect of the noise of the picture signal to a sampling control signal, leading about can be shortened more at wiring.

[0033]

[Embodiment of the Invention] - Explain the 1st operation gestalt which applied the drive circuit of the electro-optic device by this invention to active matrix liquid crystal equipment using drawing 1 - drawing 4 below 1st operation gestalt -.

[0034] Drawing 1 is equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of liquid crystal equipment] a matrix, and wiring.

[0035] In drawing 1 , as a switching element for two or more pixels formed in the shape of [which constitutes image display field 110a of the liquid crystal equipment by this operation gestalt] a matrix to control the pixel electrode 9 and the pixel electrode 9, two or more formation is carried out at the shape of a matrix, and the thin film transistor (TFT is called hereafter.) 30 is connected in the source concerned of TFT30 electrically [the data line 6 with which a picture signal is supplied].

[0036] The picture signals S1, S2, --, Sn written in the data line 6 especially with this operation gestalt Serial-parallel conversion is beforehand carried out by the serial-parallel conversion circuit in the picture signal processing circuit which supplies picture signals S1, S2, --, Sn to the liquid crystal equipment concerned at n (n is two or more integers) individual. It is constituted so that the picture signal which consists of the n data lines 6 which adjoin each other and by which serial-parallel conversion was carried out for every block may be supplied to coincidence. About the number of serial-parallel conversion, generally, as long as a dot frequency is relatively low or the sampling capacity in the below-mentioned sampling switch is relatively high, you may set up small, for example like three-phase-circuit expansion and 6 phase expansion. On the contrary, as long as a dot frequency is relatively high or sampling capacity is relatively low, you may set up greatly, for example like 12 phase expansion and 24 phase expansion. In addition, it is desirable when simplifying control and a circuit, in case video presentation, such as an NTSC display and a PAL display, is carried out to it being the multiple of 3 from the relation of a color picture signal consisting of a signal concerning three colors (red, blue, yellow) as this number of serial-parallel conversion (phase expansion). Moreover, if an example is taken at the existing TFT manufacturing technology in the case of high dot frequencies, such as the latest XGA method, a SXGA method, and an EWS method, it is desirable to set up the number of serial-parallel conversion greatly, for example like 12 phase expansion and 24 phase expansion.

[0037] Moreover, the scanning line 3 is electrically connected to the gate of TFT30, and it consists of predetermined timing so that the scan signals G1, G2, --, Gm may be impressed to the scanning line 3 in pulse line sequential at this order. It connects with the drain of TFT30 electrically, and the pixel electrode 9 writes in the picture signals S1, S2, --, Sn supplied from the data line 6 in TFT30 which is a switching element when only a fixed period closes the switch to predetermined timing. Fixed period maintenance of the picture signals S1, S2, --, Sn of the predetermined level written in liquid crystal

through the pixel electrode 9 is carried out between the counterelectrodes (it mentions later) formed in the opposite substrate (it mentions later). When the orientation and order of molecular association change with the voltage levels impressed, liquid crystal modulates light and enables a gradation display. According to the electrical potential difference impressed when it was in no MARI White mode, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from liquid crystal equipment as a whole. Here, in order to prevent the held picture signal leaking, storage capacitance (not shown) is added to the liquid crystal capacity and juxtaposition which are formed between the pixel electrode 9 and a counterelectrode. For example, as for the electrical potential difference of the pixel electrode 9, only time amount also with triple figures longer than the time amount to which the source electrical potential difference was impressed is held with storage capacitance. Thereby, it is improved further and a maintenance property can realize the high liquid crystal equipment of a contrast ratio.

[0038] Next, the drive circuit of the liquid crystal equipment of this operation gestalt is explained. On the TFT array substrate 10 of the circumference of this image display field 110a, the data-line drive circuit 101, the scanning-line drive circuit 104, and the drive circuit of sampling switch 121 grade are prepared with image display field 110a in which the scanning line, the data line, etc. were formed as mentioned above.

[0039] The scanning-line drive circuit 104 is the predetermined timing according to the Vertical Synchronizing signal of the picture signal supplied from an external picture signal processing circuit, and supplies the scan signals G1 and G2 and --Gm by line sequential in pulse to the scanning line 3.

[0040] The scanning-line drive circuit 104 minds [3] the sampling control signal line 40 according to sending a scan signal, and the data-line drive circuits 101 are the sampling control signals X1 and X2... Xn is supplied to a sampling switch 121. A sampling switch 121 samples the picture signals VID1-VID6 supplied to the picture signal line 115 according to this sampling control signal, and supplies them to the data line 6. With this operation gestalt, since serial-parallel conversion of the picture signal is carried out at six phases, a common sampling control signal is supplied to the sampling switch 121 connected to the six data lines 6 which adjoin each other, it considers as an ON state at coincidence, and picture signals VID1-VID6 are supplied to these six data lines through the junction wiring 80 at coincidence from the picture signal line 115.

[0041] Next, a more detailed configuration is explained with the actuation about the data-line drive circuit 101 and a sampling switch 121.

[0042] The data-line drive circuit 101 is equipped with the shift register circuit 400 which carries out the sequential output of the transfer signal, and the buffer circuit 200 for outputting the transfer signal by which the sequential output was carried out as a sampling control signal, and is constituted. The shift register circuit 400 consists of latch circuits 123 which consist of two or more steps of delayed type flip-flop circuits by which the series connection was carried out, and if the start pulse SP which synchronized with the Horizontal Synchronizing signal of picture signals VID1-VID6 is inputted from an external picture signal processing circuit, latch circuit 123a of a left end stage will start transfer operation based on a reference clock signal (and the reversal clock signal) first.

[0043] Thus, the transfer signals OUT1 and OUT2 from a latch circuit 123, --, OUTn are outputted to a sampling switch 121 as a sampling control signal through a buffer circuit 200. A buffer circuit 200 consists of two steps of the 1st buffer circuit 124 and the 2nd buffer circuit 125 by which the series connection was carried out, and a sampling control signal is supplied to a sampling switch 121 for every block through a buffer circuit 200 at coincidence. Next, the concrete configuration of the 1st buffer circuit 124 and the 2nd buffer circuit 125 which are included in a buffer circuit 200 is explained.

[0044] As shown in drawing 1 , each latch circuit 123 of a shift register circuit 400 is connected to the 1st buffer circuit 124, respectively, and the 1st buffer circuit 124 is further connected to the serial in

the 2nd six buffer circuit 125, respectively. namely, -- 1st buffer circuit 124a -- the 1- the 7-12th buffer circuits [2nd] 125 are connected to 2nd buffer circuit [1st] 124b for the 6th buffer circuit [2nd] 125, respectively.

[0045] Moreover, the 2nd outgoing end of 2nd buffer circuit 124b is connected to the 2nd six sampling switch 121 at the 1st six sampling switch 121 through six sampling control signal lines 40 by which a degree adjoins each other through six sampling control signal lines 40 by which the 1st outgoing end of 2nd buffer circuit 125a adjoins each other, respectively. The outgoing end of the 2nd buffer circuit 125 of eye ** (N+1) watch is connected to the sampling switch 121 of eye ** (N+1) watch like the following, respectively.

[0046] Semiconductor devices, such as a field-effect transistor, can constitute each of the above-mentioned sampling switch 121. As a sampling switch 121, when using a field-effect transistor, the sampling control signal line 40 is connected to the gate, and it connects with the source through the junction wiring 80 at the picture signal line 115, and it is constituted by the drain so that it may connect with the data line 6.

[0047] The 1st buffer circuit 124 of the above and the 2nd buffer circuit 125 function as an impedance converter, and all have a high input impedance, and the output impedance is made low.

[0048] The 2nd buffer circuit 125 of the above must be equipped with current serviceability required since a sampling switch 121 is driven. For example, since volume load will be connected to the 2nd buffer circuit 125 equivalent when a gate terminal is connected to the outgoing end of the 2nd buffer circuit 125, using a field-effect transistor as a sampling switch 121, the current serviceability for performing charge and discharge at sufficient rate to volume load is needed.

[0049] Moreover, 1st buffer 124 circuit must be equipped with the current serviceability which needs an input edge to drive six buffer circuits connected to juxtaposition. That is, since the 2nd six buffer circuit 125 is connected to an outgoing end in the 1st buffer circuit 124, the current serviceability for performing charge and discharge at sufficient rate to this load is needed. In addition, even if it does not form the 1st buffer circuit 124, when there is capacity which can carry out the direct drive of the 2nd buffer circuit 125 to a shift register 400, the 1st buffer circuit 124 is removed and you may make it connect the outgoing end of a shift register 400 to the 2nd buffer circuit 125 directly.

[0050] As 1st buffer 124 circuit or the 2nd buffer circuit 125, the circuit which piled up two steps of inverters Inv by the complementary transistor as shown in drawing 2 (a) can be used. Moreover, the circuit shown, for example in drawing 2 (b) can be used. If it is the circuit which can make a latter impedance lower than the impedance of the preceding paragraph, it can be widely used as an impedance converter.

[0051] In using an inverter, in order that the signal of I/O may be reversed, modification must be added to a circuit if needed so that the logic as the whole drive circuit may have consistency. In addition, when using an inverter for both 1st buffer circuit 124 of drawing 1 , and 2nd buffer circuit 125, even if it does not add modification to other parts, the same actuation as the 1st operation gestalt can be secured.

[0052] The picture signal from the display information processing circuit 600 shown in drawing 3 is changed into serial-parallel, and is outputted to the liquid crystal equipment 100 which has the above-mentioned configuration. This display information processing circuit 600 may be formed as an external circuit (IC) separated from liquid crystal equipment 100. One picture signal VID is inputted into this display information processing circuit 600. And the display information processing circuit 600 develops the image information of a picture signal VID to six serial-parallel conversion signals, and outputs these signals as picture signals VID1-VID6.

[0053] (Configuration of a pixel field) The configuration of the pixel of the TFT array substrate 10 constituted by the above-mentioned equal circuit next is explained with reference to drawing 4 .

[0054] Drawing 4 (a) is the top view of a pixel group where the data line, the scanning line, and the TFT array substrate 10 with which the pixel electrode was formed adjoined. Drawing 4 (b) is the C-C' sectional view of drawing 4 (a).

[0055] Each pixel is constituted in drawing 4 (a) and drawing 4 (b) by TFT30 for pixel switching which is an example of the switching element connected to two or more transparent pixel electrode 9 and each pixel electrode 9 in the shape of a matrix. Electrical installation of the 1st conductive layer which the data line 6, the scanning line 3, and capacity line 3' are prepared respectively along the boundary of the pixel electrode 9 in every direction, and constitutes the data line 6 is carried out to the 1d of the below-mentioned source fields among semi-conductor layer 1a which consists of metals, such as aluminum and chromium, and consists of amorphous silicon film, polish recon film, etc. of TFT30 through contact hole 5a formed in the 1st interlayer insulation film 4. Electrical installation of the pixel electrode 9 is carried out to the below-mentioned drain field 1e among semi-conductor layer 1a of a thin film transistor 30 through the contact hole 8 formed in the 1st interlayer insulation film 4 and the 2nd interlayer insulation film 7. Moreover, the scanning line 3 is arranged so that field 1a' for channel formation of the semi-conductor layer 1a (field of the slash of the drawing 2 Nakamigi going down) may be countered through gate dielectric film 2. Although the 2nd conductive layer which constitutes the scanning line 3 may be formed with a metal like aluminum and chromium, when exposed to an elevated temperature 600 degrees C or more in a production process, it may form by polish recon. Storage capacitance uses as one electrode the 1f of the 1st storage capacitance electrodes installed from semi-conductor layer 1a of TFT30 for pixel switching, and uses as a dielectric film gate dielectric film 2 and the insulator layer formed in coincidence, and capacity line 3' formed in the scanning line 3 and coincidence is constituted as an electrode (the 2nd storage capacitance electrode) of another side. Since sufficient storage capacitance will be obtained by using precise gate dielectric film 2 as a dielectric with a thin film even if the lap area of the 1f of the 1st storage capacitance electrodes and 2nd storage capacitance electrode 3' is small if such a configuration is taken, a raise in a numerical aperture and detailed-izing of a pixel can be realized easily.

[0056] The orientation film 16 with which predetermined orientation processing of rubbing processing etc. was performed as shown in drawing 4 (b) is formed in the pixel electrode 9 bottom. The pixel electrode 9 consists of transparent conductive thin films, such as for example, ITO (Indium Tin Oxide) film. Moreover, the orientation film 16 consists of organic thin films, such as for example, a polyimide thin film.

[0057] On the other hand, it crosses to the opposite substrate 20 all over the, the counterelectrode 21 is formed, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 22 consists of organic thin films, such as a polyimide thin film. Furthermore, a light-shielding film 23 may be formed with a metal membrane, metal alloy film, or black organic film of non-light transmission nature etc. so that the field which the disclination of TFT30 for pixel switching or liquid crystal generates may be covered. Thereby, the high image display of a contrast ratio is realizable. You may make it form a light-shielding film 23 in the TFT array substrate 10. If such a configuration is taken, since it is not necessary to take into consideration the precision at the time of sticking the TFT array substrate 10 and the opposite substrate 20, it is stabilized and the liquid crystal equipment 100 with which permeability does not vary can be offered.

[0058] The liquid crystal as electrooptic material is enclosed between the TFT array substrate 10 which has the above-mentioned configuration, and the opposite substrate 20, and the liquid crystal layer 50 is formed in it. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film in the condition that the electric field from the pixel electrode 9 are not impressed.

[0059] Generally here field 1for channel formation a', the amorphous silicon film which forms low concentration source field 1b, low concentration drain field 1c, etc., or polish recon film of semi-conductor layer 1a Although a photocurrent will occur according to the photo-electric-conversion effectiveness and the transistor characteristics of TFT30 will deteriorate if light carries out incidence Since the data line 6 is formed from the metal thin film of protection-from-light nature, such as

aluminum (aluminum), with the 1st operation gestalt so that the scanning line 3 may be covered from the bottom The incidence of the incident light (namely, drawing 3 light from a top) to field 1for channel formation a' of semi-conductor layer 1a and source side LDD (Lightly Doped Drain) field 1b, and drain side LDD field 1c can be prevented effectively at least. Moreover, if a light-shielding film (not shown) is prepared in the TFT30 bottom so that field 1for channel formation a' of semi-conductor layer 1a and the LDD fields 1b and 1c may be covered at least through an interlayer insulation film, the incidence of return light (namely, drawing 4 (b) light from the bottom) can be prevented effectively.

[0060] Next, the layout of a sampling switch is explained using drawing 5 . Two or more 2nd buffers 125 connected to the 1st buffer circuit 124 and the 1st buffer circuit 124 for every block of the sampling switch 121 to which a sampling control signal is supplied in common are formed, and the 1st wiring 41 which is six branching wiring which connects the 1st buffer circuit 124 and the 2nd buffer circuit 125 is formed by the 1st conductive layer. And it branches to parallel six and connects with the 2nd buffer circuit 125, and the 1st wiring 41 is constituted so that the output signal (sampling control signal) of the 2nd buffer circuit 125 may be inputted into the gate electrode of a sampling switch 121 through the sampling control signal line 40. The sampling control signal line 40 consists of the 2nd wiring 42 which intersects a picture signal line, the 3rd wiring 43 further extended from the 2nd wiring 42, and the 4th wiring 48 used as the gate electrode of a sampling switch.

[0061] As shown in drawing 5 , the 2nd wiring 42 connected to the output terminal of the 2nd buffer 125 and the 3rd wiring 43 are formed in parallel with the junction wiring 80 connected to the picture signal line 115, and the 2nd wiring 42 and the 3rd wiring 43, and the one wiring junction wiring 80 are arranged at a time by turns. Since the picture signal line 115 is formed of the 1st conductive layer like the data line 6, the 2nd wiring 42 which constitutes the sampling control signal line 40 is [the line] good for the 1st conductive layer to form by the 2nd conductive layer like another layer 3, for example, the scanning line. Moreover, the 3rd wiring 43 which does not intersect the picture signal line 115 among the sampling control signal lines 40 will be further formed into low resistance, if it is made the two-layer structure of the 1st conductive layer and the 2nd conductive layer as mentioned above and connects through contact holes 44 and 45.

[0062] Since the buffer circuit 125 which became independent every sampling switch 121 is used, the impedance of the sampling control signal line 40 can be made low. For this reason, it is stabilized, a sampling switch 121 can be made to be able to switch, and, therefore, the image quality of a display image can be raised.

[0063] Next, actuation of the drive circuit of the 1st operation gestalt is explained. A picture signal VID is an analog signal with which the data corresponding to each pixel of liquid crystal equipment 100 were serially located in a line, and as shown in drawing 3 , the display information processing circuit 600 samples a picture signal VID by making a dot clock DC into a reference clock. And serial-parallel conversion of this image information is carried out at six picture signals VID1-VID6 of a data length longer than the sampling period of a picture signal VID. That is, the display information processing circuit 600 is equipped with the function which elongates the data length of the image information of a picture signal VID, and the function to change the serial picture signal VID into a parallel signal.

[0064] The picture signals VID1-VID6 outputted to the picture signal line 115 elongate in order the data for 6 pixels with which a picture signal VID continues to the data length for six periods of a dot clock DC. Each head of this picture signal for 6 pixels is located in the head of the pixel [6th] data, and each picture signal VID1-VID6 is outputted to the same timing.

[0065] By drawing 6 , while giving a pixel number (1-18) to each pixel data of a picture signal VID in order, the image number of the original pixel data changed into picture signals VID1-VID6 is attached, and this shows both correspondence relation. In the period for dot clock DC6 period when the pixel data of the pixel numbers 1-6 are outputted as picture signals VID1-VID6, a shift register 400 outputs an output signal OUT1. Subsequently, in the period for dot clock DC6 period when the pixel data of the pixel numbers 7-12 are outputted as VID1-VID6, an output signal OUT2 is outputted from a shift

register 400. Thus, a shift register 400 carries out the sequential output of output signals OUT1, OUT2, and OUT3 and -- in the period for dot clock DC6 period when a new serial-parallel conversion signal is outputted.

[0066] If an output signal OUT1 is outputted to the 1st buffer circuit 124 from latch circuit 123a of a shift register 400, the output of a buffer circuit 124 will start and the 2nd buffer circuit 125 will output a sampling control signal to six sampling control signal lines 40 by this at coincidence. The sampling control signals X1-X6 supplied to six sampling control signal lines 40 are supplied to six sampling switches 121.

[0067] According to the sampling control signal supplied to a sampling switch 121, the picture signals VID1-VID6 supplied to the picture signal line 115 are supplied to the data line 6, respectively. For example, writing is performed to the pixel electrode 9 through TFT30 of six pixels connected to the 1st scanning line 3 and the above-mentioned data line 6. Thus, writing is performed to coincidence about six pixels (pixel numbers 1-6) chosen by the six data lines 6 and the one scanning line 3.

[0068] Subsequently, when an output signal OUT2 is outputted to 1st buffer circuit 124b from latch circuit 123b of a shift register 400, the output of 1st buffer circuit 124b starts, and the 2nd six buffer circuit 125 outputs a sampling control signal to six sampling control signal lines 40 which adjoin each other at coincidence, and makes six sampling switches 121 turn on by this. For this reason, writing is performed to coincidence about the following six pixels (pixel numbers 7-12) chosen by the six data lines 6 and the one above-mentioned scanning line 3.

[0069] Like the following, by the output signal from a shift register 400, a sampling switch 121 turns on six at a time one by one, and every 6 pixels writing is performed. Thus, it can write in about all the pixels of the 1st scanning line 3. The image of one frame is formed by repeating the above-mentioned actuation, outputting a sequential-scanning signal about all the scanning lines 3 of the 2nd henceforth.

[0070] He forms the 2nd buffer circuit 125 to each of a sampling switch 121, and is trying to drive the 2nd six buffer circuit 125 by the 1st one buffer circuit 124 with the 1st operation gestalt. That is, the sampling switch 121 within one block is connected to the 2nd buffer circuit 125 different, respectively. For this reason, the 2nd buffer circuit 125 will become light [that load] that what is necessary is to drive only one sampling switch 121, respectively.

[0071] Moreover, although six sampling control signal lines 40 by which a sampling signal is outputted to coincidence will be mutually connected through the 2nd six buffer circuit 125, since the 2nd buffer circuit 125 has the property in which the signal of an output side hardly affects an input side, the input edge of the 2nd buffer circuit 125 is not changed in response to the effect of an outgoing end. For this reason, the signal of one of the sampling control signal lines 40 hardly affects the electrical potential difference of the input side of the 2nd buffer circuit 125. In addition, the outgoing end of the 1st buffer circuit 124 is connected to the input side of the 2nd buffer circuit 125, and since the impedance is made low, the electrical potential difference of the input edge of the 2nd buffer circuit 125 cannot be changed still more easily.

[0072] For this reason, even if a noise mixes in the sampling control signal line 40 by a certain cause, for example, in response to the effect of that noise, the electrical potential difference of the input side of the 2nd buffer circuit 125 is changed, and thereby, the whole sampling control signal line 40 does not drive, and is not necessarily shaken by the 2nd buffer circuit 125. Similarly, even if a noise mixes in either of the sampling control signal lines 40, other sampling control signal lines are not shaken by the 2nd buffer circuit 125 by this.

[0073] Moreover, since the output side of the 2nd buffer circuit 125 is made into low impedance, going into the direct sampling control signal line 40 through capacity coupling does not almost have the noise of the data signal S1 supplied to the picture signals VID1-VID6 supplied from the picture signal line 115, or the data line 6, S2 --, or each part etc., either.

[0074] Thus, with the 1st operation gestalt, since the 2nd buffer circuit 125 is formed every sampling control signal line 40, it is hard to mix various noises in the sampling control signal line 40, and they can

maintain the purity of a sampling signal highly. For this reason, according to the drive circuit of the 1st operation gestalt, a ghost etc. does not occur but a good display image can be obtained.

[0075] The drive circuit by this invention is invented based on the analysis of the cause of generating of the ghost phenomenon in the conventional drive circuit. Hereafter, in order to clarify the operation effectiveness of the drive circuit by this invention, the device of ghost generating in the conventional drive circuit etc. is explained using drawing 13 .

[0076] In the drive circuit of drawing 13 , six sampling control signal lines 40 which consist of six sampling switches 121 and by which a sampling control signal is supplied to coincidence for every block are connected to one buffer circuit 124 in common. On the other hand, the sampling control signal line 40 within one block, the picture signal line 115 and the sampling control signal line 40, and the data line 6 are in the condition of having been combined through the capacity (they being the capacity between the gate sources, the capacity between gate drains, etc. when using a field-effect transistor as a sampling switch 121) formed in a sampling switch 121, respectively.

[0077] For this reason, for example, if the electrical potential difference of the data line 6 is rapidly changed with ON of a sampling switch 121, the component (differential wave) corresponding to that fluctuation will become the sampling control signal line 40 with a surroundings lump noise through the above-mentioned capacity. However, since the sampling control signal line 40 within one block is connected in common, the noise which invaded into one sampling control signal line 40, for example is further spread easily on other sampling control signal lines 40 within a block. As mentioned above, since the noise which appears in the sampling control signal line 40 depends for the range of fluctuation on the picture signal at that time (electrical-potential-difference value) depending on the range of fluctuation of the data line 6 when a sampling switch 121 turns on in coincidence, the noise component on which the sampling control signal line 40 is overlapped after all will have the electrical-potential-difference value of a picture signal, and correlation.

[0078] Such a phenomenon is applied as it is also about the effect of the sampling control signal line [either / of the sampling control signal lines 40] on others. Therefore, the electrical potential difference of the sampling control signal line 40 is changed according to the electrical potential difference of the picture signal line 115 at the time of the writing to the pixel electrode 9, and, moreover, it turns out that fluctuation of the sampling control signal line 40 becomes what synchronized mutually.

[0079] And the voltage variation of the sampling control signal line 40 fluctuates the electrical potential difference of the data line 6 through the sampling switch 121 within a block. For example, since it changes a drain electrical potential difference according to the property of the component with fluctuation of the gate voltage connected to the sampling control signal line 40 in using a field-effect transistor etc. as a sampling switch 121, all the electrical potential differences of the data line 6 are changed.

[0080] Thus, the electrical potential difference of the sampling control signal line 40 changes in response to the effect of the electrical potential difference of the picture signal line 115 whole at the time of the writing to the pixel electrode 9, and the change fluctuates the electrical potential difference of the data-line 6 whole. That is, since the data line 6 is changed in response to the effect of the electrical-potential-difference value of other picture signal lines in which direct continuation is not carried out by the sampling switch 121, an image is made to produce a ghost.

[0081] Moreover, since the sampling control signal line 40 is connected to the common buffer circuit 124, it cannot but differ in the sampling control signal line 40 in the 1st operation gestalt, and leading about cannot but become long, for example. For this reason, an impedance tends to rise near the sampling switch 121, and the sampling control signal line 40 increases with [of a noise] a jump comparatively. For this reason, the above ghosts become the situation which is easier to generate.

[0082] Thus, in order that the electrical potential difference of the data line 6 may originally be changed in response to the effect of a picture signal with the unrelated data line 6 and a noise may tend [comparatively] to ride on the sampling control signal line 40, it is difficult in the conventional drive

circuit to obtain a ghost's good image which is not.
[0083] On the other hand, in the drive circuit of the 1st operation gestalt, the 2nd buffer circuit 125 was prepared every sampling switch 121, and the sampling switch 121 is switched through the 2nd buffer circuit 125. For this reason, between different sampling control signal lines 40, the 2nd buffer 125 will surely be inserted and association between different sampling control signal lines 40 can be intercepted nearly completely.
[0084] That is, in the drive circuit of the gestalt of the 1st operation, since the noise is not spread on another sampling control signal line 40 even if a noise invades into one sampling control signal line 40, for example, the electrical potential difference of the data line 6 is not changed.
[0085] Moreover, since the outgoing end of the 2nd buffer 125 is connected to each of the sampling control signal line 40, leading about of wiring of the sampling control signal line 40 can be shortened, and the rise of the impedance is suppressed. For this reason, a noise cannot fly at the sampling control signal line 40 easily.
[0086] Therefore, in the drive circuit of the gestalt of the 1st operation, a ghost who is seen by the conventional driving gear does not occur, but a good display image can be obtained.
[0087] - Explain the 2nd operation gestalt of the drive circuit of the electro-optic device by this invention using drawing 7 below 2nd operation gestalt -. With the 2nd operation gestalt, the shape of a pulse form of a sampling control signal shall be differed from the 1st operation gestalt. In addition, the explanation is omitted about the same component as the 1st operation gestalt.
[0088] with the 1st operation gestalt, the pulse width of a sampling control signal is set as the same pulse width (a part for dot clock DC6 period) as a serial-parallel conversion signal -- **** (drawing 2) -- Pulse width of the sampling signal outputted to the sampling control signal line 40 with the 2nd operation gestalt as shown in drawing 6 is made smaller than the pulse width of the picture signals VID1-VID6 of the picture signal line 115. The pulse of the sampling control signals X1-X6, X7-X12, X13-X18, and -- is located between the standup of a picture signal, and falling.
[0089] Thus, if the pulse of a sampling signal is set as the period which does not lap with the standup and falling of a picture signal, writing can be performed at the period which is stable. Therefore, a highly precise signal can be supplied to the data line 6, and a much more good image can be obtained.
[0090] In addition, although pulse width of a sampling control signal is made into the width of face for dot clock DC4 period in drawing 7 , the pulse width of a sampling control signal can be suitably chosen in the range which can be written in to the liquid crystal layer 50.
[0091] - Explain the 3rd operation gestalt of the drive circuit of the electro-optic device by this invention using drawing 8 below 3rd operation gestalt -. Drawing 8 is the representative circuit schematic of the 3rd operation gestalt. In addition, about the same component as the 1st operation gestalt, the same sign is attached and the explanation is omitted.
[0092] With the 3rd operation gestalt, as shown in drawing 8 , the 2nd three buffer circuit 125 is connected to the outgoing end of each 1st buffer circuit 124 connected to the outgoing end of a shift register 400, respectively, respectively. Moreover, two sampling switches 121 are connected to each 2nd buffer circuit 125, respectively.
[0093] Next, the layout of the 3rd operation gestalt is explained using drawing 9 .
[0094] The 2nd wiring 42 with which the sampling control signal line 121 crossed in parallel with the junction wiring 80 towards the sampling switch 121 from the output terminal of 2nd buffer 125 circuit, It consists of the 3rd wiring 43 which was connected to the 2nd wiring 42 and installed further, the picture signal line 115 and the connection wiring 45 installed in parallel, and the 4th wiring 48 which was pulled out from each gate electrode of each sampling switch 121, and was connected with the connection wiring 45. The junction wiring 80 of two is installed in the gap of the 3rd wiring 43 connected to the 2nd wiring 42 and the 2nd wiring in parallel with the 2nd wiring 42 and the 3rd wiring 43. Furthermore, the 3rd wiring 43 is connected to the connection wiring 46 through a contact hole 47, and the connection wiring 46 is installed so that the junction wiring 80 may be intersected. Moreover, the 3rd wiring 43 is duplex

wiring of the 1st conductive layer and the 2nd conductive layer between contact holes 44 and 45. The connection wiring 45 consists of the 1st conductive layer, and is connected with the 4th wiring 48 extended by the tandem type so that it might connect with a sampling switch 121 through the contact hole 47.

[0095] With the 3rd operation gestalt, two sampling control signal lines 40 inputted into two adjacent sampling switches 121 are mutually connected to the 2nd buffer circuit 125 in common. Therefore, if it compares with the conventional drive circuit shown in drawing 13 , since the load of a buffer circuit 125 is light, it is hard to mix a noise in the output side of a buffer circuit 125, therefore fluctuation of a sampling control signal can be controlled good. For this reason, the precision of the signal of the data line can be raised and, therefore, fitness can obtain an image.

[0096] moreover, since the effect on between the data lines 6 left two or more is eliminated by the buffer circuit 125, the image is displayed on the duplex on the screen -- as -- it is hard to recognize and a ghost can be eliminated as a matter of fact.

[0097] Although he is trying to supply a sampling control signal to two sampling switches from the 2nd one buffer circuit 125, you may make it supply a sampling control signal to three or more sampling switches from one buffer circuit with the 3rd operation gestalt.

[0098] - Explain the 4th operation gestalt of the drive circuit of the electro-optic device by this invention using drawing 10 below 4th operation gestalt -. Drawing 10 is the representative circuit schematic of the 4th operation gestalt. In addition, about the same component as the 1st operation gestalt, the same sign is attached and the explanation is omitted.

[0099] With the 4th operation gestalt, as shown in drawing 10 , the 1st buffer circuit 124 and the 2nd buffer circuit 125 are separated mutually, the picture signal line 115 is arranged, and the 1st wiring which is an output line of ** is branched by the 2nd buffer circuit 125 side from the 1st buffer circuit 124. That is, it branches, after installing so that the picture signal line 115 may be crossed, and crossing, and it connects with juxtaposition in two or more 2nd buffer circuits, and the 1st parallel connected to the 1st buffer circuit is ******.

[0100] By adopting such a layout, with the 4th operation gestalt, leading about of wiring of the sampling control signal line 40 applicable to the output line of the 2nd buffer 125 can be shortened further, and it can avoid with [of the noise from the picture signal line 115 to the sampling control signal line 40] a jump. In addition, when there is capacity which can carry out the direct drive of the large 2 buffer circuits 125 to SHITOREJISUTA 400 even if it does not form the 1st buffer circuit 124 in this operation gestalt as the operation gestalt 1 explained, the 1st buffer circuit 124 is removed and you may make it connect the outgoing end of a shift register 400 to the 2nd buffer circuit 125 directly.

[0101] (The whole liquid crystal display layout) Hereafter, using drawing 11 and drawing 12 , about the whole liquid crystal display layout of the active-matrix mold with which this invention is applied, the case of the gestalt of the 1st operation is mentioned as an example, and is explained.

[0102] In drawing 11 , on the TFT array substrate 10, the sealant 152 is formed along the edge and the light-shielding film 153 as a frame is formed in parallel to the inside. The data-line drive circuit 101 and the mounting terminal 102 are formed in the field of the outside of a sealant 152 along with one side of the TFT array substrate 10, and the scanning-line drive circuit 104 is established in it along with two sides which adjoin this one side. A shift register 400 and the 1st and 2nd buffer circuits 124,125 are included in the data-line drive circuit 101. If the scan signal delay supplied to the scanning-line drive circuit 104 does not become a problem, as shown in drawing 1 , the thing only with one side sufficient [the scanning-line drive circuit 104] cannot be overemphasized. Moreover, the data-line drive circuit 101 may be arranged on both sides along the side of an image display field. For example, the data line of an odd number train supplies a picture signal from the data-line drive circuit arranged along one side of the image display field DA, and you may make it the data line of an even number train supply a picture signal from the data-line drive circuit arranged along the side of the opposite side of the image display field DA. Thus, if it is made to drive the data line in the shape of a ctenidium, since the occupancy area

of a data-line drive circuit is extensible, it becomes possible to constitute a complicated circuit. Furthermore, two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of the image display field DA is formed in one side in which the TFT array substrate 10 remains, and if it hides in the bottom of the light-shielding film 153 as a frame and a sampling circuit 121 is formed further, since the layout field of the data-line drive circuit 101 is extensible, built-in of a large-scale circuit and the miniaturization of liquid crystal equipment 100 are realizable. Moreover, in at least one place of the corner section of the opposite substrate 20, the flow material 106 for taking an electric flow between the TFT array substrate 10 and the opposite substrate 20 is formed. And as shown in drawing 12 , the opposite substrate 20 with the almost same profile as the sealant 152 shown in drawing 11 fixes to the TFT array substrate 10 by the sealant 152 concerned, and liquid crystal 50 is enclosed with the interior.

[0103] As mentioned above, on the TFT array substrate 10 of the liquid crystal equipment in the gestalt of each operation explained with reference to drawing 1 - drawing 12 , the inspection circuit for inspecting the quality of the liquid crystal equipment concerned at the manufacture middle or the time of shipment, a defect, etc. may be formed further. Moreover, you may make it connect with LSI for a drive mounted on TAB (tape automated bonding substrate) instead of forming the data-line drive circuit 101 and the scanning-line drive circuit 104 on the TFT array substrate 10 electrically and mechanically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10. Moreover, according to the exception of modes of operation, such as TN (Twisted Nematic) mode, STN (super TN) mode, and D-STN (double-STN) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, a polarizing plate, etc. are respectively arranged in a predetermined direction at the side in which the outgoing radiation light of the side in which the incident light of the opposite substrate 20 carries out incidence, and the TFT array substrate 10 carries out outgoing radiation.

[0104] It is also possible to drive each pixel using TFT or to use with the gestalt of the above-mentioned implementation, other than TFT (for example, active components, such as TFD (thin-film diode)), and it is also possible to constitute liquid crystal equipment as liquid crystal equipment of a passive matrix mold further. Moreover, it is applicable also to the drive circuit of the display which comes to form a switching element in a silicon substrate. Furthermore, this invention is widely applicable also about electro-optic devices other than liquid crystal equipment.

[0105] (Electronic equipment) Next, the gestalt of operation of the electronic equipment equipped with liquid crystal equipment 100 as an example of the electro-optic device explained to the detail above is explained with reference to drawing 16 from drawing 14 .

[0106] The outline configuration of the electronic equipment which equipped drawing 14 with liquid crystal equipment 100 in this way is shown first.

[0107] In drawing 14 , electronic equipment is constituted in preparation for the source 1000 of a display information output, the display information processing circuit 1002, the drive circuit 1004, liquid crystal equipment 100, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a picture signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a serial-parallel conversion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the drive circuit 1004 with a clock signal CLK. The drive circuit 1004 drives liquid crystal equipment 100. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the substrate for liquid crystal equipments which constitutes liquid crystal equipment 100, the drive

circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.
[0108] Next, the example of the electronic equipment constituted in this way from drawing 15 by drawing 16 is shown respectively.
[0109] In drawing 15 , an example slack liquid crystal projector 1100 of electronic equipment prepares three liquid crystal display modules containing the liquid crystal equipment 100 with which the drive circuit 1004 mentioned above was carried on the substrate for liquid crystal equipments, and is constituted as a projector respectively used as light valves 100R, 100G, and 100B for RGB. In a liquid crystal projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be respectively led to the light valves 100R, 100G, and 100B corresponding to each color. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors respectively modulated with light valves 100R, 100G, and 100B is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.
[0110] In drawing 16 , the liquid crystal equipment 100 mentioned above is formed in the top covering case, and other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic equipment (PC) are equipped with the body 1204 with which the keyboard 1202 was incorporated while they hold CPU, memory, a modem, etc. further.
[0111] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 16 from drawing 15 above etc. is mentioned as an example of the electronic equipment shown in drawing 14 .
[0112] As explained above, according to the gestalt of this operation, various kinds of electronic equipment equipped with the liquid crystal equipment in which high-definition image display with high manufacture effectiveness is possible is realizable.
[0113]
[Effect of the Invention] Since according to this invention it has the 1st buffer circuit connected to the outgoing end of said shift register, and two or more 2nd buffer circuits respectively connected to the outgoing end of said 1st buffer circuit and the outgoing end of two or more of said 2nd buffer circuits is connected to the sampling switch within said block, as explained above, while being able to control the wave-like turbulence of a sampling control signal good, invasion of the noise through a sampling control signal line can be prevented. Therefore, there are very few ghosts or a good image without a ghost can be obtained.

[Translation done.]

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1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The representative circuit schematic showing the drive circuit of the electro-optic device of the 1st operation gestalt.
[Drawing 2] It is the representative circuit schematic in which it is drawing showing the circuit of an impedance converter, and the representative circuit schematic in which (a) shows a buffer circuit, and (b) show the circuit of an inverter.
[Drawing 3] Drawing showing the connection relation between a display information processing circuit and liquid crystal equipment.
[Drawing 4] It is the top view of the pixel group of the 1st operation gestalt of this invention, and (b) is the C-C' sectional view of drawing 4 (a).
[Drawing 5] Drawing showing the layout of the drive circuit of the 1st operation gestalt.
[Drawing 6] The timing chart which shows actuation of the drive circuit of the electro-optic device of the 1st operation gestalt.
[Drawing 7] The timing chart which shows actuation of the drive circuit of the electro-optic device of the 2nd operation gestalt.
[Drawing 8] The representative circuit schematic of the drive circuit of the 3rd operation gestalt.
[Drawing 9] The layout pattern of the drive circuit of the electro-optic device of the 3rd operation gestalt.
[Drawing 10] The representative circuit schematic of the electro-optic device of the 4th operation gestalt.
[Drawing 11] The top view showing the whole electro-optic device configuration.
[Drawing 12] The sectional view in the H-H' line of drawing 10 .
[Drawing 13] The representative circuit schematic showing the drive circuit of the conventional electro-optic device.
[Drawing 14] It is the block diagram showing the outline configuration of the gestalt of operation of the electronic equipment by this invention.
[Drawing 15] It is the sectional view showing a liquid crystal projector as an example of electronic equipment.
[Drawing 16] It is the front view showing a personal computer as other examples of electronic equipment.
[Description of Notations]
100 Liquid Crystal Equipment
101 Scanning-Line Drive Circuit
121 Sampling Switch
400 Shift Register
124 1st Buffer Circuit
125 2nd Buffer Circuit
115 Picture Signal Line

[Translation done.]

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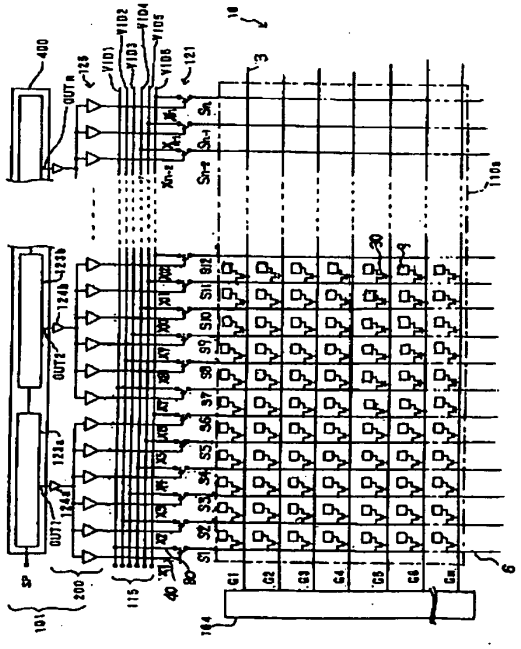
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最終頁に続く

(54)【発明の名称】　電気光学装置の駆動回路及び電気光学装置

(57)【要約】
【課題】　ゴースト等の発生がない良好な表示画像を得ることができる電気光学装置の駆動回路を提供する。
【解決手段】　画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、複数のサンプリングスイッチからなるブロック毎に共通にサンプリング制御信号を出力するシフトレジスタと、前記シフトレジスタの出力端に接続された第１バッファ回路と、前記第１バッファ回路の出力端に並列に接続された複数の第２バッファ回路とを有し、前記複数の第２バッファ回路の出力端は前記ブロック内のサンプリングスイッチに接続されてなることを特徴とする。



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【特許請求の範囲】

【請求項１】　複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、

画像信号を供給する複数の画像信号線と、

前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、

複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、

前記シフトレジスタの出力端に接続された第１バッファ回路と、

各前記第１バッファ回路の出力端に並列に接続された複数の第２バッファ回路とを有し、

前記複数の第２バッファ回路の出力端の夫々は前記ブロック内のサンプリングスイッチに接続されてなることを特徴とする電気光学装置の駆動回路。

【請求項２】　１つのブロック内の複数のサンプリングスイッチの各々は、異なる第２バッファ回路に接続されてなることを特徴とする請求項１に記載の電気光学装置の駆動回路。

【請求項３】　１つのブロック内の複数のサンプリングスイッチは１つの第２バッファ回路に接続されてなることを特徴とする請求項１に記載の電気光学装置の駆動回路。

【請求項４】　前記第１バッファ回路と前記第２バッファ回路の少なくとも一方はインバータからなることを特徴とする請求項１又は２に記載の電気光学装置の駆動回路。

【請求項５】　複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、

画像信号を供給する複数の画像信号線と、

前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、

複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、

前記シフトレジスタの出力端に並列に接続された複数のバッファ回路とを有し、

前記複数のバッファ回路の出力端の夫々は前記ブロック内のサンプリングスイッチに接続されてなることを特徴とする電気光学装置の駆動回路。

【請求項６】　複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、

画像信号を供給する複数の画像信号線と、

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前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給するサンプリングスイッチと、

前記画像信号線と前記サンプリングスイッチとを接続する中継配線と、

複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、

前記シフトレジスタの出力端に接続された第１バッファ回路と、

各前記第１バッファ回路の出力端に並列に接続された複数の第２バッファ回路とを有し、

前記複数の第２バッファ回路と前記サンプリングスイッチとを接続するサンプリング制御信号線は、前記中継配線の間隙に沿って画像信号線を交差してなることを特徴とする電気光学装置の駆動回路。

【請求項７】　複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、

画像信号を供給する複数の画像信号線と、

前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給するサンプリングスイッチと、

前記画像信号線と前記サンプリングスイッチとを接続する中継配線と、

複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、

前記シフトレジスタの出力端に接続された第１バッファ回路と、

各前記第１バッファ回路の出力端に並列に接続された複数の第２バッファ回路とを有し、

前記第１バッファ回路と前記第２バッファ回路とを接続する出力線は前記画像信号線を交差した後に分岐されて前記複数の第２バッファ回路に並列に接続され、各前記第２バッファ回路から供給されるサンプリング制御信号は前記第２バッファ回路に接続されたサンプリング制御信号線を介して前記サンプリングスイッチに供給されることを特徴とする電気光学装置の駆動回路。

【請求項８】　１つのブロック内の複数のサンプリングスイッチの各々は、異なる第２バッファ回路に接続されてなることを特徴とする請求項７に記載の電気光学装置の駆動回路。

【請求項９】　ブロック内の複数のサンプリングスイッチは１つの第２バッファ回路に接続されてなることを特徴とする請求項７に記載の電気光学装置の駆動回路。

【請求項１０】　複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、

画像信号を供給する複数の画像信号線と、

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前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、

複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、

前記シフトレジスタの出力端に並列に接続されたバッファ回路とを有し、前記シフトレジスタの出力端と前記バッファ回路とを接続する出力線は前記画像信号線を交差した後に複数に分岐して前記複数のバッファ回路に並列に接続され、前記複数のバッファ回路から供給されるサンプリング制御信号はサンプリング制御信号線を介して前記サンプリングスイッチに供給されることを特徴とする電気光学装置の駆動回路。

【請求項１１】　請求項１乃至請求項１０のいずれか一項に記載の電気光学装置の駆動回路を備えた電気光学装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、アクティブマトリクス型の電気光学装置等に用いられる駆動回路の構成に関する。詳しくは、複数の画像信号線からの画像信号を同時にサンプリングして複数のデータ線に同時書き込みを行なう電気光学装置の駆動回路及び電気光学装置に関する。

【０００２】

【従来の技術】例えば、電気光学装置の一例として、アクティブマトリクス型の液晶装置では、複数の走査線と、複数のデータ線と、各走査線と各データ線に接続された薄膜トランジスタ等からなるスイッチング素子とスイッチング素子に接続された画素電極とからなる画素とを有している。一走査線に複数接続された薄膜トランジスタ等のスイッチング素子を介して、各画素の液晶層に画像信号を書き込む動作を、点順次駆動により実施している。

【０００３】このようなアクティブマトリクス型の液晶装置では、上述の点順次駆動のために、データ線ごとに設けられたサンプリングスイッチを点順次駆動の速度で順次スイッチングさせ、画像信号をサンプリングする必要がある。このとき、サンプリングスイッチのスイッチング特性が入力画像信号の周波数に対して十分に追従できないという問題が生ずる。一般にドライバ回路を画素と同時に作り込むドライバー内蔵の表示装置の場合は、外付けドライバを用いた表示装置の場合に比べてサンプリング用薄膜トランジスタの駆動能力が低く、その問題がより顕著となる。また、多数の画素を有する高精細な表示装置の場合は、入力画像信号の周波数が高くなることから、上記問題がより顕著となる。

【０００４】このため、図１３に示す液晶装置のように、画像信号を例えば６つのシリアルーパラレル信号に変換し、１画素あたりのデータ長を長くして、液晶装置

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に入力される信号周波数を低くする技術が開示されている。このシリアルーパラレル変換により、例えばサンプリングスイッチとしての薄膜トランジスタの周波数特性が十分でなくても、１画素あたりのデータ長を長くして、解像度を高くできる。

【０００５】図１３の液晶装置では、シフトレジスタ４００からの出力を受けるバッファ１２４には、それぞれ６つのサンプリングスイッチ１２１が接続され、これら６つのサンプリングスイッチ１２１を同時に切替可能に構成されている。そして、６つずつサンプリングスイッチ１２１を同時にオンさせることにより、画像信号線１１５に供給される画像信号ＶＩＤ１－ＶＩＤ６を６本の相隣接するデータ線６に同時に出力するようにしている。このような構成を採ることにより、サンプリングスイッチ１２１によるサンプリングの間隔を長くすることができ、薄膜トランジスタをサンプリングスイッチとして使用することも容易となる。

【０００６】

【発明が解決しようとする課題】しかしながら、図１３の構成を採用した場合、液晶装置の画像にゴーストが発生しやすいという問題がある。一般に、サンプリングスイッチとデータ線の結合構造は周波数特性が悪い。また、サンプリングスイッチを制御するサンプリング制御信号の位相がばらつく。これらの原因により、本来書き込むべき画像信号がそのブロックだけでなく１ブロック先の画素にも書き込まれてしまい、ゴーストが発生してしまうのである。つまり、同時にサンプリング制御信号が供給されるサンプリングスイッチの数が多いために、本来その時間にサンプリングしなければならないはずが、それよりもずれた時間でサンプリングしてしまい、ゴーストを引き起こすことになるのである。特に、同時に駆動されるサンプリングスイッチの本数が６本、１２本、あるいは２４本等増えると、同時に駆動されるブロック全体への影響も大きくなる。

【０００７】そこで、本発明は、ゴースト等の発生がない良好な表示画像を得ることができる電気光学装置の駆動回路を提供することを目的とする。

【０００８】

【課題を解決するための手段】本発明の電気光学装置の駆動回路は、上記課題を解決するため、複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、前記シフトレジスタの出力端に接続された第１バッファ回路と、各前記第１バッファ回路の出力端に並列に接続

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された複数の第２バッファ回路とを有し、前記複数の第２バッファ回路の出力端の夫々は前記ブロック内のサンプリングスイッチに接続されてなることを特徴とする。

【０００９】本発明の電気光学装置の駆動回路によれば、サンプリング制御信号手段は、前記ブロック毎に共通に設けられた第１バッファ回路と、各第１バッファ回路に接続された複数の第２バッファ回路とを有し、前記複数の第２バッファ回路の出力が前記ブロック内の複数のサンプリングスイッチに供給されてなる。

【００１０】したがって、バッファ回路がサンプリングスイッチのブロック毎に共通に接続されているだけの場合と比較して、ブロック内のいくつかのサンプリングスイッチに分割接続されたバッファ回路を介してサンプリングスイッチを駆動する場合の負荷が軽くなるため、バッファ回路の出力側にノイズが混入しにくくなり、サンプリングスイッチに供給されるサンプリング信号の波形の乱れを抑制することができる。このため、サンプリング制御信号の波形の乱れに起因するデータ線の電圧変動を効果的に抑制することができ、ゴースト等の画質劣化を招かない電気光学装置を実現できる。

【００１１】また、共通にサンプリング制御信号が供給されるサンプリングスイッチは、各々異なるバッファ回路の出力端に接続されているから、異なるサンプリングスイッチ間のサンプリング制御信号の伝播を大幅に減少させることができる。このため、例えばサンプリングスイッチに形成された容量等に起因して、サンプリングスイッチがオンしたときなどにサンプリング制御信号にノイズが混入したとしても、そのノイズが他のサンプリングスイッチのサンプリング制御信号に伝播することが効果的に防止される。したがって、電気光学装置にはゴーストの極めて少ない、あるいはゴーストのない画像を表示することができる。

【００１２】本発明の電気光学装置の駆動回路は、１つのブロック内の複数のサンプリングスイッチの各々は、異なる第２バッファ回路に接続されてなることを特徴とする。

【００１３】この態様によれば、各サンプリングスイッチには、それぞれのサンプリングスイッチごとに独立して設けられた第２バッファ回路を介してサンプリング制御信号が入力される。このため、サンプリングスイッチを駆動する場合の負荷が極めて軽くなるため、第２バッファ回路の出力側にノイズが混入しにくくなり、サンプリング制御信号の波形の乱れを著しく抑制することができる。したがって、電気光学装置を精度よく駆動することができる。

【００１４】また、各サンプリングスイッチにサンプリング制御信号を供給するサンプリング制御信号は、各々異なる第２バッファ回路の出力端に接続されているから、異なるサンプリングスイッチのサンプリング制御信号間における信号の伝播を大幅に減少させることができ、あるいはこのような信号の伝播を消滅させることができる。このため、サンプリング制御信号線間にノイズが混入したとしても、そのノイズが他のサンプリングスイッチのサンプリング制御信号線に伝播することが効果的に防止される。したがって、電気光学装置にはゴーストの極めて少ない、あるいはゴーストのない画像を表示することができる。

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【００１５】本発明による電気光学装置の駆動回路の一態様では、１つのブロック内の複数のサンプリングスイッチは１つの第２バッファ回路に接続されてなることを特徴とする。

【００１６】この態様によれば、１つの第２バッファ回路に複数のサンプリングスイッチが接続されるので、第２バッファ回路の総数がいたずらに増加することを防止でき、スペースを有効活用することができる。

【００１７】本発明による電気光学装置の駆動回路の一態様では、前記インピーダンス変換器としてインバータを用いる。

【００１８】この態様によれば、インバータの出力側のインピーダンスを低くすることができるので、サンプリング制御信号線にノイズが混入しにくくなり、各要素に供給されるサンプリング制御信号線の波形の乱れを効果的に抑制することができる。

【００１９】本発明による電気光学装置の駆動回路に二態様では、複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、前記シフトレジスタの出力端に並列に接続された複数のバッファ回路とを有し、前記複数のバッファ回路の出力端の夫々は前記ブロック内のサンプリングスイッチに接続されてなることを特徴とする。

【００２０】本発明のこの態様によれば、バッファ回路がサンプリングスイッチのブロック毎に共通に接続されているだけの場合と比較して、ブロック内のいくつかのサンプリングスイッチに分割接続されたバッファ回路を介してサンプリングスイッチを駆動する場合の負荷が軽くなるため、バッファ回路の出力側にノイズが混入しにくくなり、サンプリングスイッチに供給されるサンプリング信号の波形の乱れを抑制することができる。このため、サンプリング制御信号の波形の乱れに起因するデータ線の電圧変動を効果的に抑制することができ、ゴースト等の画質劣化を招かない電気光学装置を実現できる。

【００２１】また、共通にサンプリング制御信号が供給されるサンプリングスイッチは、各々異なるバッファ回

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路の出力端に接続されているから、異なるサンプリングスイッチ間のサンプリング制御信号の伝播を大幅に減少させることができる。このため、例えばサンプリングスイッチに形成された容量等に起因して、サンプリングスイッチがオンしたときなどにサンプリング制御信号にノイズが混入したとしても、そのノイズが他のサンプリングスイッチのサンプリング制御信号に伝播することが効果的に防止される。したがって、電気光学装置にはゴーストの極めて少ない、あるいはゴーストのない画像を表示することができる。

【００２２】本発明の電気光学装置の駆動回路は、複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給するサンプリングスイッチと、前記画像信号線と前記サンプリングスイッチとを接続する中継配線と、複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、前記シフトレジスタの出力端に接続された第１バッファ回路と、各前記第１バッファ回路の出力端に並列に接続された複数の第２バッファ回路とを有し、前記複数の第２バッファ回路と前記サンプリングスイッチとを接続するサンプリング制御信号線は、前記中継配線の間隙に沿って画像信号線を交差してなることを特徴とする。

【００２３】本発明のこの態様によれば、バッファ回路がサンプリングスイッチのブロック毎に共通に接続されているだけの場合と比較して、ブロック内のいくつかのサンプリングスイッチに分割接続されたバッファ回路を介してサンプリングスイッチを駆動する場合の負荷が軽くなるため、バッファ回路の出力側にノイズが混入しにくくなり、サンプリングスイッチに供給されるサンプリング信号の波形の乱れを抑制することができる。このため、サンプリング制御信号の波形の乱れに起因するデータ線の電圧変動を効果的に抑制することができ、ゴースト等の画質劣化を招かない電気光学装置を実現できる。

【００２４】また、共通にサンプリング制御信号が供給されるサンプリングスイッチは、各々異なるバッファ回路の出力端に接続されているから、異なるサンプリングスイッチ間のサンプリング制御信号の伝播を大幅に減少させることができる。このため、例えばサンプリングスイッチに形成された容量等に起因して、サンプリングスイッチがオンしたときなどにサンプリング制御信号にノイズが混入したとしても、そのノイズが他のサンプリングスイッチのサンプリング制御信号に伝播することが効果的に防止される。したがって、電気光学装置にはゴーストの極めて少ない、あるいはゴーストのない画像を表示することができる。

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【００２５】本発明の電気光学装置の駆動回路は、複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給するサンプリングスイッチと、前記画像信号線と前記サンプリングスイッチとを接続する中継配線と、複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、前記シフトレジスタの出力端に接続された第１バッファ回路と、各前記第１バッファ回路の出力端に並列に接続された複数の第２バッファ回路とを有し、前記第１バッファ回路と前記第２バッファ回路とを接続する出力線は前記画像信号線を交差した後に分岐して前記複数の第２バッファ回路に並列に接続され、各前記第２バッファ回路から供給されるサンプリング制御信号は前記第２バッファ回路に接続されたサンプリング制御信号線を介して前記サンプリングスイッチに供給されることを特徴とする。

【００２６】本発明のこの態様によれば、第１バッファ回路と第２バッファ回路とを接続する出力線が画像信号線を交差し、交差した後に第２バッファ回路が設けられているため、サンプリング制御信号が画像信号による影響を抑えることができるとともに、配線に引き回しをより短くすることができる。本発明の電気光学装置の駆動回路において、１つのブロック内の複数のサンプリングスイッチの各々は、異なる第２バッファ回路に接続されてなることを特徴とする。

【００２７】この態様によれば、各サンプリングスイッチには、それぞれのサンプリングスイッチごとに独立して設けられた第２バッファ回路を介してサンプリング制御信号が入力される。このため、サンプリングスイッチを駆動する場合の負荷が極めて軽くなるため、第２バッファ回路の出力側にノイズが混入しにくくなり、サンプリング制御信号の波形の乱れを著しく抑制することができる。したがって、電気光学装置を精度よく駆動することができる。

【００２８】また、各サンプリングスイッチにサンプリング制御信号を供給するサンプリング制御信号は、各々異なる第２バッファ回路の出力端に接続されているから、異なるサンプリングスイッチのサンプリング制御信号間における信号の伝播を大幅に減少させることができ、あるいはこのような信号の伝播を消滅させることができる。このため、サンプリング制御信号線間にノイズが混入したとしても、そのノイズが他のサンプリングスイッチのサンプリング制御信号線に伝播することが効果的に防止される。したがって、電気光学装置にはゴーストの極めて少ない、あるいはゴーストのない画像を表示することができる。

【００２９】本発明による電気光学装置の駆動回路では、１つのブロック内の複数のサンプリングスイッチは１つの第２バッファ回路に接続されてなることを特徴とする。

【００３０】この態様によれば、１つの第２バッファ回路に複数のサンプリングスイッチが接続されるので、第２バッファ回路の総数がいたずらに増加することを防止でき、スペースを有効活用することができる。

【００３１】本発明の電気光学装置の駆動回路は、複数のデータ線と、複数の走査線と、前記各データ線と前記各走査線に接続されたスイッチング素子と、前記スイッチング素子に接続された画素電極とを有する電気光学装置の駆動回路であって、画像信号を供給する複数の画像信号線と、前記複数の画像信号線に供給される画像信号をサンプリングして前記各データ線に供給する複数のサンプリングスイッチと、複数のサンプリングスイッチからなるブロック毎に共通に転送信号を出力するシフトレジスタと、前記シフトレジスタの出力端に並列に接続されたバッファ回路とを有し、前記シフトレジスタの出力端と前記バッファ回路とを接続する出力線は前記画像信号線を交差した後に複数に分岐して前記複数のバッファ回路に並列に接続され、前記複数のバッファ回路から供給されるサンプリング制御信号をサンプリング制御信号線を介して前記サンプリングスイッチに供給することを特徴とする。

【００３２】本発明のこの態様によれば、シフトレジスタの出力端とバッファ回路とを接続する出力線が画像信号線を交差し、交差した後にバッファ回路が設けられているため、サンプリング制御信号への画像信号のノイズの影響を抑えることができるとともに、配線に引き回しをより短くすることができる。

【００３３】

【発明の実施の形態】－第１実施形態－

以下、図１～図４を用いて、本発明による電気光学装置の駆動回路をアクティブマトリクス型液晶装置に適用した第１実施形態について説明する。

【００３４】図１は、液晶装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。

【００３５】図１において、本実施形態による液晶装置の画像表示領域１１０ａを構成するマトリクス状に形成された複数の画素は、画素電極９と画素電極９を制御するためのスイッチング素子として、例えば薄膜トランジスタ（以下、ＴＦＴと称す。）３０とがマトリクス状に複数形成されており、画像信号が供給されるデータ線６が当該ＴＦＴ３０のソースに電気的に接続されている。

【００３６】本実施形態では特に、データ線６に書き込まれる画像信号Ｓ１、Ｓ２、…、Ｓｎは、当該液晶装置に画像信号Ｓ１、Ｓ２、…、Ｓｎを供給する画像信号処理回路内のシリアルーパラレル変換回路によって予めｎ（ｎは２以上の整数）個にシリアルーパラレル変換されており、相隣接するｎ本のデータ線６からなるブロック毎に、シリアルーパラレル変換された画像信号を同時に供給するように構成されている。シリアルーパラレル変換数については一般には、ドット周波数が相対的に低いか或いは後述のサンプリングスイッチにおけるサンプリング能力が相対的に高ければ、例えば３相展開、６相展開等のように小さく設定してもよい。逆に、ドット周波数が相対的に高いか或いはサンプリング能力が相対的に低ければ、例えば１２相展開、２４相展開等のように大きく設定してもよい。尚、このシリアルーパラレル変換（相展開）数としては、カラー画像信号が３つの色（赤、青、黄）に係る信号からなることとの関係から、３の倍数であると、ＮＴＳＣ表示やＰＡＬ表示等のビデオ表示をする際に制御や回路を簡易化する上で好ましい。また、近時のＸＧＡ方式、ＳＸＧＡ方式、ＥＷＳ方式等の高ドット周波数の場合には、既存のＴＦＴ製造技術に鑑みれば、例えば１２相展開、２４相展開等のようにシリアルーパラレル変換数を大きく設定するのが好ましい。

【００３７】また、ＴＦＴ３０のゲートに走査線３が電気的に接続されており、所定のタイミングで、走査線３にパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９は、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６から供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。画素電極９を介して液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板（後述する）に形成された対向電極（後述する）との間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能にする。ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として液晶装置からは画像信号に応じたコントラストを持つ光が出射する。ここで、保持された画像信号がリークするのを防ぐために、画素電極９と対向電極との間に形成される液晶容量と並列に蓄積容量（図示せず）を付加する。例えば、画素電極９の電圧は、ソース電圧が印加された時間よりも３桁も長い時間だけ蓄積容量により保持される。これにより、保持特性は更に改善され、コントラスト比の高い液晶装置が実現できる。

【００３８】次に、本実施形態の液晶装置の駆動回路を説明する。上述のように走査線、データ線等が設けられた画像表示領域１１０ａと共に、該画像表示領域１１０ａの周辺のＴＦＴアレイ基板１０上には、データ線駆動

回路１０１、走査線駆動回路１０４及びサンプリングスイッチ１２１等の駆動回路が設けられている。

【００３９】走査線駆動回路１０４は、外部の画像信号処理回路から供給される画像信号の垂直同期信号に応じた所定タイミングで、走査線３に対して走査信号Ｇ１、Ｇ２、…Ｇｍをパルス的に線順次で供給する。

【００４０】データ線駆動回路１０１は、走査線駆動回路１０４が走査線３に走査信号を送るのに合わせて、サンプリング制御信号線４０を介してサンプリング制御信号Ｘ１、Ｘ２…Ｘｎをサンプリングスイッチ１２１に供給する。サンプリングスイッチ１２１は、このサンプリング制御信号に応じて、画像信号線１１５に供給される画像信号ＶＩＤ１～ＶＩＤ６をサンプリングしてデータ線６に供給する。本実施形態では、画像信号が６相にシリアルーパラレル変換されているため、相隣接する６本のデータ線６に接続されたサンプリングスイッチ１２１には、共通のサンプリング制御信号が供給されて同時にオン状態とされ、画像信号線１１５から中継配線８０を介して画像信号ＶＩＤ１～ＶＩＤ６がこの６本のデータ線に同時に供給される。

【００４１】次に、データ線駆動回路１０１及びサンプリングスイッチ１２１に関してより詳細な構成についてその動作と共に説明する。

【００４２】データ線駆動回路１０１は、転送信号を順次出力するシフトレジスタ回路４００と、順次出力された転送信号をサンプリング制御信号として出力するためのバッファ回路２００とを備えて構成されている。シフトレジスタ回路４００は、直列接続された複数段の遅延型フリップフロップ回路等からなるラッチ回路１２３で構成されており、画像信号ＶＩＤ１～ＶＩＤ６の水平同期信号に同期したスタートパルスＳＰが外部の画像信号処理回路から入力されると、先ず左端段のラッチ回路１２３ａが基準クロック信号（及びその反転クロック信号）に基づいて転送動作を開始する。

【００４３】このようにラッチ回路１２３からの転送信号ＯＵＴ１、ＯＵＴ２、…、ＯＵＴｎは、バッファ回路２００を介してサンプリング制御信号として、サンプリングスイッチ１２１に出力される。バッファ回路２００は、直列接続された第１バッファ回路１２４と第２バッファ回路１２５との２段からなり、バッファ回路２００を介してサンプリング制御信号がブロック毎に同時にサンプリングスイッチ１２１に供給される。次に、バッファ回路２００に含まれる第１バッファ回路１２４及び第２バッファ回路１２５の具体的な構成について説明する。

【００４４】図１に示されるように、シフトレジスタ回路４００の各ラッチ回路１２３はそれぞれ第１バッファ回路１２４に接続され、さらに第１バッファ回路１２４はそれぞれ６つの第２バッファ回路１２５に直列に接続されている。すなわち、第１番目のバッファ回路１２４ａには第１～第６番目の第２バッファ回路１２５が、第２番目の第１バッファ回路１２４ｂには第７～１２番目の第２バッファ回路１２５がそれぞれ接続されている。

【００４５】また、第１番目の第２バッファ回路１２５ａの出力端は相隣接する６本のサンプリング制御信号線４０を介して第１番目の６つのサンプリングスイッチ１２１に、第２番目の第２バッファ回路１２４ｂの出力端は次の相隣接する６本のサンプリング制御信号線４０を介して第２番目の６つのサンプリングスイッチ１２１にそれぞれ接続される。以下同様にして、第（Ｎ＋１）番目の第２バッファ回路１２５の出力端は第（Ｎ＋１）番目のサンプリングスイッチ１２１に、それぞれ接続される。

【００４６】上記サンプリングスイッチ１２１の各々は、例えば電界効果トランジスタ等の半導体素子により構成することができる。サンプリングスイッチ１２１として、例えば電界効果トランジスタを用いる場合には、ゲートにはサンプリング制御信号線４０が接続され、ソースには中継配線８０を介して画像信号線１１５に接続され、ドレインにはデータ線６に接続されるように構成されている。

【００４７】上記第１バッファ回路１２４および第２バッファ回路１２５はインピーダンス変換器として機能し、いずれも入力インピーダンスが高く、かつ出力インピーダンスが低くされている。

【００４８】上記第２バッファ回路１２５はサンプリングスイッチ１２１を駆動するために必要な電流供給能力を備えなければならない。例えばサンプリングスイッチ１２１として電界効果トランジスタを用い、第２バッファ回路１２５の出力端にゲート端子が接続される場合には、第２バッファ回路１２５には等価的に容量負荷が接続されることとなるので、容量負荷に対して十分な速度で充放電を行うための電流供給能力が必要となる。

【００４９】また、第１バッファ１２４回路は入力端が並列に接続された６つのバッファ回路を駆動するのに必要な電流供給能力を備えなければならない。すなわち、第１バッファ回路１２４には出力端に６つの第２バッファ回路１２５が接続されるので、この負荷に対して十分な速度で充放電を行うための電流供給能力が必要となる。なお、第１バッファ回路１２４を設けなくても、シフトレジスタ４００に第２バッファ回路１２５を直接駆動できる能力がある場合には、第１バッファ回路１２４を取り除き、シフトレジスタ４００の出力端を直接第２バッファ回路１２５に接続するようにしてもよい。

【００５０】第１バッファ１２４回路あるいは第２バッファ回路１２５として、例えば図２（ａ）に示すような、相補型トランジスタによるインバータＩｎｖを２段重ねた回路を用いることができる。また、例えば図２（ｂ）に示す回路を用いることができる。後段のインピーダンスを前段のインピーダンスよりも低くできる回路

であれば、広くインピーダンス変換器として使用することができる。

【００５１】インバータを用いる場合には、入出力の信号が反転するため、駆動回路全体としての論理が整合するように、必要に応じて回路に変更を加えなければならない。なお、図１の第１バッファ回路１２４および第２バッファ回路１２５の両者にインバータを用いる場合には、他の部分に変更を加えなくても、第１実施形態と同様の動作を確保することができる。

【００５２】上記の構成を有する液晶装置１００には、図３に示す表示情報処理回路６００からの画像信号がシリアルーパラレルに変換されて出力される。この表示情報処理回路６００は、液晶装置１００から分離された外付け回路（ＩＣ）として設けられていてもよい。この表示情報処理回路６００には、一本の画像信号ＶＩＤが入力される。そして、表示情報処理回路６００は画像信号ＶＩＤの画像情報を６つのシリアルーパラレル変換信号に展開し、これらの信号を画像信号ＶＩＤ１～ＶＩＤ６として出力する。

【００５３】（画素領域の構成）次に上述の等価回路により構成されたＴＦＴアレイ基板１０の画素の構成について、図４を参照して説明する。

【００５４】図４（ａ）は、データ線、走査線、画素電極が形成されたＴＦＴアレイ基板１０の隣接した画素群の平面図である。図４（ｂ）は、図４（ａ）のＣ－Ｃ'断面図である。

【００５５】図４（ａ）及び図４（ｂ）において、各画素は、マトリクス状に複数の透明な画素電極９と各画素電極９に接続されたスイッチング素子の一例である画素スイッチング用ＴＦＴ３０とにより構成されている。画素電極９の縦横の境界に各々沿ってデータ線６、走査線３及び容量線３'が設けられており、データ線６を構成する第１導電層は、アルミニウム、クロム等の金属からなり、第１層間絶縁膜４に形成されたコンタクトホール５ａを介してＴＦＴ３０のアモルファスシリコン膜やポリシリコン膜等からなる半導体層１ａのうち後述のソース領域１ｄに電気的接続されている。画素電極９は、第１層間絶縁膜４及び第２層間絶縁膜７に形成されたコンタクトホール８を介して薄膜トランジスタ３０の半導体層１ａのうち後述のドレイン領域１ｅに電気的接続されている。また、ゲート絶縁膜２を介して半導体層１ａのうちのチャネル形成用領域１ａ'（図２中右下りの斜線の領域）に対向するように走査線３が配置されている。走査線３を構成する第２導電層はアルミニウム、クロムのような金属で形成する場合もあるが、製造工程において６００℃以上の高温にさらされる場合はポリシリコンで形成する場合がある。蓄積容量は、画素スイッチング用ＴＦＴ３０の半導体層１aから延設された第１蓄積容量電極１ｆを一方の電極とし、ゲート絶縁膜２と同時に形成された絶縁膜を誘電体膜とし、走査線３と同時に形成された容量線３'を他方の電極（第２蓄積容量電極）として構成されている。このような構成を採れば、薄膜で緻密なゲート絶縁膜２を誘電体とすることで、第１蓄積容量電極１ｆと第２蓄積容量電極３'の重なり面積が小さくても、十分な蓄積容量が得られるため、画素の高開口率化や微細化が容易に実現することができる。

【００５６】画素電極９の上側には、図４（ｂ）に示すようにラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９は例えば、ＩＴＯ（Indium Tin Oxide）膜などの透明導電性薄膜からなる。また配向膜１６は例えば、ポリイミド薄膜などの有機薄膜からなる。

【００５７】他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜２２は、ポリイミド薄膜などの有機薄膜からなる。更に、画素スイッチング用ＴＦＴ３０や液晶のディスクリネーションが発生する領域を覆うように非光透過性の金属膜、金属合金膜、或いは黒色有機膜等により遮光膜２３を設けても良い。これにより、コントラスト比の高い画像表示を実現することができる。遮光膜２３はＴＦＴアレイ基板１０に設けるようにしても良い。このような構成を採れば、ＴＦＴアレイ基板１０と対向基板２０を貼り合わせる際の精度を考慮する必要がないため、透過率のばらつかない液晶装置１００を安定して提供することができる。

【００５８】上記の構成を有するＴＦＴアレイ基板１０と、対向基板２０との間には、電気光学物質としての液晶が封入され、液晶層５０が形成される。液晶層５０は、画素電極９からの電界が印加されていない状態で配向膜により所定の配向状態を採る。

【００５９】ここで、一般には、半導体層１ａのチャネル形成用領域１ａ'、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ等を形成するアモルファスシリコン膜あるいはポリシリコン膜は、光が入射すると光電変換効果により光電流が発生してしまいＴＦＴ３０のトランジスタ特性が劣化するが、第１実施形態では、走査線３を上側から覆うようにデータ線６がＡｌ（アルミニウム）等の遮光性の金属薄膜から形成されているので、少なくとも半導体層１ａのチャネル形成用領域１ａ'及びソース側ＬＤＤ（Lightly Doped Drain）領域１ｂ、ドレイン側ＬＤＤ領域１ｃへの投射光（即ち、図３で上側からの光）の入射を効果的に防ぐことが出来る。また、ＴＦＴ３０の下側に、層間絶縁膜を介して、少なくとも半導体層１ａのチャネル形成用領域１ａ'及びＬＤＤ領域１ｂ、１ｃを覆うように遮光膜（図示せず）を設ければ戻り光（即ち、図４（ｂ）で下側からの光）の入射を効果的に防ぐことが出来る。

【００６０】次に、図５を用いてサンプリングスイッチ

のレイアウトについて説明する。共通にサンプリング制御信号が供給されるサンプリングスイッチ１２１のブロック毎に第１バッファ回路１２４と第１バッファ回路１２４に接続された複数の第２バッファ１２５が設けられており、第１バッファ回路１２４と第２バッファ回路１２５とを接続する６つの分岐配線である第１配線４１が第１導電層で形成されている。そして、第１配線４１はパラレルに６つに分岐して第２バッファ回路１２５に接続され、第２バッファ回路１２５の出力信号（サンプリング制御信号）が、サンプリング制御信号線４０を介してサンプリングスイッチ１２１のゲート電極に入力されるように構成されている。サンプリング制御信号線４０は画像信号線に交差する第２配線４２と、第２配線４２からさらに延長された第３配線４３と、サンプリングスイッチのゲート電極となる第４配線４８からなる。

【００６１】図５に示されるように、第２バッファ１２５の出力端子に接続された第２配線４２及び第３配線４３は、画像信号線１１５に接続された中継配線８０と平行に設けられ、また第２配線４２及び第３配線４３と中継配線８０とは１配線ずつ交互に配置されている。画像信号線１１５はデータ線６と同様に第１導電層により形成されているため、サンプリング制御信号線４０を構成する第２配線４２は第１導電層とは別層、例えば走査線３と同様に第２導電層で形成するとよい。またサンプリング制御信号線４０のうち画像信号線１１５に交差しない第３配線４３は、上述のように第１導電層及び第２導電層の２層構造にしてコンタクトホール４４、４５を介して接続すれば、さらに低抵抗化される。

【００６２】サンプリングスイッチ１２１毎に独立したバッファ回路１２５を用いているので、サンプリング制御信号線４０のインピーダンスを低くすることができる。このため、サンプリングスイッチ１２１を安定してスイッチングさせることができ、よって表示画像の画質を向上させることができる。

【００６３】次に、第１実施形態の駆動回路の動作について説明する。画像信号ＶＩＤは液晶装置１００の各画素に対応するデータが時系列的に並んだアナログ信号であり、図３に示すように、表示情報処理回路６００はドットクロックＤＣを基準クロックとして画像信号ＶＩＤをサンプリングする。そして、この画像情報を画像信号ＶＩＤのサンプリング周期よりも長いデータ長の６本の画像信号ＶＩＤ1～ＶＩＤ６にシリアルーパラレル変換する。すなわち、表示情報処理回路６００は画像信号ＶＩＤの画像情報のデータ長を伸張する機能と、シリアルな画像信号ＶＩＤをパラレルな信号に変換する機能とを備えるものである。

【００６４】画像信号線１１５に出力される画像信号ＶＩＤ１～ＶＩＤ６は、画像信号ＶＩＤの連続する６画素分のデータを、順番にドットクロックＤＣの６周期分のデータ長に伸張したものである。この６画素分の画像信号の先頭はいずれも６画素目のデータの先頭に位置しており、それぞれの画像信号ＶＩＤ１～ＶＩＤ６は同一のタイミングで出力される。

【００６５】図６では、画像信号ＶＩＤの個々の画素データに順番に画素番号（１～１８）を付すとともに、画像信号ＶＩＤ１～ＶＩＤ６に変換した元の画素データの画像番号を付しており、これにより両者の対応関係を示している。画素番号１～６の画素データが画像信号ＶＩＤ１～ＶＩＤ６として出力されるドットクロックＤＣ６周期分の期間では、シフトレジスタ４００が出力信号ＯＵＴ１を出力する。次いで、画素番号７～１２の画素データがＶＩＤ１～ＶＩＤ６として出力されるドットクロックＤＣ６周期分の期間では、シフトレジスタ４００から出力信号ＯＵＴ２が出力される。このように、シフトレジスタ４００は、新たなシリアルーパラレル変換信号が出力されるドットクロックＤＣ６周期分の期間において、出力信号ＯＵＴ１，ＯＵＴ２，ＯＵＴ３，…を順次出力する。

【００６６】シフトレジスタ４００のラッチ回路１２３ａから第１バッファ回路１２４に出力信号ＯＵＴ１が出力されると、バッファ回路１２４の出力が立ち上がり、これによって、第２バッファ回路１２５は６本のサンプリング制御信号線４０に同時にサンプリング制御信号を出力する。６本のサンプリング制御信号線４０に供給されるサンプリング制御信号Ｘ１～Ｘ６は、６つのサンプリングスイッチ１２１に供給される。

【００６７】サンプリングスイッチ１２１に供給されるサンプリング制御信号に応じて、画像信号線１１５に供給される画像信号ＶＩＤ１～ＶＩＤ６は、それぞれデータ線６に供給される。例えば第１番目の走査線３と、上記データ線６とに接続された６つの画素のＴＦＴ３０を介して、画素電極９に書き込みが行われる。このように、６本のデータ線６と、１本の走査線３とによって選択された６つの画素（画素番号１～６）について、同時に書き込みが行われる。

【００６８】次いで、シフトレジスタ４００のラッチ回路１２３ｂから第１バッファ回路１２４ｂに出力信号ＯＵＴ２が出力されると、第１バッファ回路１２４ｂの出力が立ち上がり、これによって、６つの第２バッファ回路１２５は６本の相隣接するサンプリング制御信号線４０に同時にサンプリング制御信号を出力し、６つのサンプリングスイッチ１２１をオンさせる。このため、６本のデータ線６と、上記の１本の走査線３とによって選択された次の６つの画素（画素番号７～１２）について、同時に書き込みが行われる。

【００６９】以下同様にして、シフトレジスタ４００からの出力信号によって、順次６つずつサンプリングスイッチ１２１がオンし、６画素ずつの書き込みが実行される。このようにして、第１番目の走査線３の全画素について書き込みを行うことができる。第２番目以降の走査

線３のすべてについて順次走査信号を出力しながら上記動作を繰り返すことにより、１フレームの画像が形成される。

【００７０】第１実施形態では、サンプリングスイッチ１２１のそれぞれに対して第２バッファ回路１２５を設け、１つの第１バッファ回路１２４によって６つの第２バッファ回路１２５を駆動するようにしている。つまり、１つのブロック内のサンプリングスイッチ１２１はそれぞれ異なる第２バッファ回路１２５に接続されている。このため、第２バッファ回路１２５はそれぞれ１つのサンプリングスイッチ１２１のみを駆動すればよく、その負荷が軽いものとなる。

【００７１】また、同時にサンプリング信号が出力される６本のサンプリング制御信号線４０は互いに６つの第２バッファ回路１２５を介して接続されることになるが、第２バッファ回路１２５は出力側の信号が入力側にほとんど影響を与えないという性質を有するので、第２バッファ回路１２５の入力端が出力端の影響を受けて変動することはない。このため、いずれかのサンプリング制御信号線４０の信号は、第２バッファ回路１２５の入力側の電圧にほとんど影響を与えることはない。なお、第２バッファ回路１２５の入力側には第１バッファ回路１２４の出力端が接続されており、そのインピーダンスは低くされているから、なおさら第２バッファ回路１２５の入力端の電圧は変動しにくい。

【００７２】このため、例えばサンプリング制御信号線４０に何らかの原因でノイズが混入しても、そのノイズの影響を受けて第２バッファ回路１２５の入力側の電圧が変動し、これによりサンプリング制御信号線４０の全体が第２バッファ回路１２５によって駆動され揺さぶられるということはない。同様に、サンプリング制御信号線４０のいずれかにノイズが混入したとしても、これによって他のサンプリング制御信号線が第２バッファ回路１２５によって揺さぶられることはない。

【００７３】また、第２バッファ回路１２５の出力側は低インピーダンスとされているから、画像信号線１１５から供給される画像信号ＶＩＤ１～ＶＩＤ６やデータ線６に供給されるデータ信号Ｓ１、Ｓ２…、あるいは各部のノイズ等が、容量結合を介して直接サンプリング制御信号線４０に入るということもほとんどない。

【００７４】このように、第１実施形態では、各サンプリング制御信号線４０毎に第２バッファ回路１２５を設けているので、各種ノイズがサンプリング制御信号線４０に混入しにくく、サンプリング信号の純度を高く維持することができる。このため、第１実施形態の駆動回路によれば、ゴースト等が発生せず、良好な表示画像を得ることができるものである。

【００７５】本発明による駆動回路は、従来の駆動回路におけるゴースト現象の発生原因の解析に基づいて、発明されたものである。以下、本発明による駆動回路の作用効果を明らかにするため、図１３を用いて従来の駆動回路におけるゴースト発生の機構等について説明する。

【００７６】図１３の駆動回路では、６つのサンプリングスイッチ１２１からなるブロック毎に、同時にサンプリング制御信号が供給される６本のサンプリング制御信号線４０は共通に１つのバッファ回路１２４に接続されている。一方、１つのブロック内のサンプリング制御信号線４０と画像信号線１１５、およびサンプリング制御信号線４０、データ線６は、それぞれサンプリングスイッチ121に形成される容量（例えばサンプリングスイッチ１２１として電界効果トランジスタを用いる場合には、そのゲート・ソース間容量、ゲート・ドレイン間容量等）を介して結合された状態にある。

【００７７】このため、例えば、サンプリングスイッチ１２１のオンに伴ってデータ線６の電圧が急激に変動すると、その変動に見合った成分（微分波形）が上記容量を介してサンプリング制御信号線４０に回り込みノイズとなる。ところが、１つのブロック内のサンプリング制御信号線４０は共通に接続されているので、例えば１つのサンプリング制御信号線４０に侵入したノイズは、さらにブロック内の他のサンプリング制御信号線４０にも容易に伝播する。上記のように、サンプリングスイッチ１２１が同時にオンしたときにサンプリング制御信号線４０に現れるノイズはデータ線６の変動幅に依存し、その変動幅はそのときの画像信号（電圧値）に依存するから、結局サンプリング制御信号線４０に重畳されるノイズ成分は画像信号の電圧値と相関があることになる。

【００７８】このような現象は、サンプリング制御信号線４０のいずれかから他のサンプリング制御信号線への影響についてもそのまま当てはまる。したがって、サンプリング制御信号線４０の電圧は、画素電極９への書き込み時における画像信号線１１５の電圧に応じて変動し、しかもサンプリング制御信号線４０の変動は互いに同期したものとなることが判る。

【００７９】そしてサンプリング制御信号線４０の電圧変動は、ブロック内のサンプリングスイッチ１２１を介してデータ線６の電圧を変動させる。例えば、サンプリングスイッチ１２１として電界効果トランジスタ等を用いる場合には、サンプリング制御信号線４０に接続されたゲート電圧の変動にともなって、その素子の特性に従いドレイン電圧が変動するので、データ線６の電圧がすべて変動する。

【００８０】このように、サンプリング制御信号線４０の電圧は、画素電極９への書き込み時における画像信号線１１５全体の電圧の影響を受けて変化し、その変化がデータ線６全体の電圧を変動させる。すなわち、データ線６はサンプリングスイッチ１２１によって直接接続されることのない、他の画像信号線の電圧値の影響を受けて変動するので、画像にゴーストを生じさせることになる。

【００８１】また、例えばサンプリング制御信号線４０は共通のバッファ回路１２４に接続されているので、第１実施形態におけるサンプリング制御信号線４０とは異なり、引き回しが長くならざるを得ない。このため、サンプリング制御信号線４０はサンプリングスイッチ121の近くでインピーダンスが上昇しやすく、比較的ノイズの飛びつきが多くなる。このため、上記のようなゴーストがより発生しやすい状況となる。

【００８２】このように従来の駆動回路では、データ線６の電圧が本来そのデータ線６とは無関係の画像信号の影響を受けて変動し、また、サンプリング制御信号線４０に比較的ノイズが乗りやすいため、ゴーストの全くない、良好な画像を得ることは困難である。

【００８３】これに対して、第１実施形態の駆動回路では、各サンプリングスイッチ１２１毎に第２バッファ回路１２５を用意し、第２バッファ回路１２５を介してサンプリングスイッチ１２１をスイッチングしている。このため、異なるサンプリング制御信号線４０の間には必ず第２バッファ１２５が挿入されることとなり、異なるサンプリング制御信号線４０間の結合をほぼ完全に遮断することができる。

【００８４】すなわち、第１の実施の形態の駆動回路では、例えば１つのサンプリング制御信号線４０にノイズが侵入したとしても、そのノイズは別のサンプリング制御信号線４０には伝播しないので、データ線６の電圧が変動することはない。

【００８５】また、サンプリング制御信号線４０の各々に第２バッファ１２５の出力端が接続されているので、サンプリング制御信号線４０の配線の引き回しを短くすることができ、そのインピーダンスの上昇が抑えられる。このため、サンプリング制御信号線４０にノイズが飛びつきにくい。

【００８６】したがって、第１の実施の形態の駆動回路では、従来の駆動装置に見られるようなゴーストが発生せず、良好な表示画像を得ることができる。

【００８７】－第２実施形態－

以下、図７を用いて、本発明による電気光学装置の駆動回路の第２実施形態について説明する。第２実施形態では、サンプリング制御信号のパルスの形状を第１実施形態と異なるものとしている。なお、第１実施形態と同一の構成要素についてはその説明を省略する。

【００８８】第１実施形態では、サンプリング制御信号のパルス幅はシリアル－パラレル変換信号と同一のパルス幅（ドットクロックＤＣ６周期分）に設定されている（図２）が、第２実施形態では、図６に示すようにサンプリング制御信号線４０に出力されるサンプリング信号のパルス幅を、画像信号線１１５の画像信号ＶＩＤ１～ＶＩＤ６のパルス幅よりも小さくして、サンプリング制御信号Ｘ１～Ｘ６、Ｘ７～Ｘ１２、Ｘ１３～Ｘ１８、…のパルスを画像信号の立ち上がりと立ち下がりの間に位置させている。

【００８９】このように、サンプリング信号のパルスを画像信号の立ち上がりおよび立ち下がりに重ならない期間に設定すれば、画像信号が安定している期間に書き込みを実行できる。したがって、高精度の信号をデータ線６に供給することができ、より一層良好な画像を得ることができる。

【００９０】なお、図７ではサンプリング制御信号のパルス幅をドットクロックＤＣ４周期分の幅としているが、サンプリング制御信号のパルス幅は液晶層５０に対する書き込みが可能な範囲で適宜選択することができる。

【００９１】－第３実施形態－

以下、図８を用いて本発明による電気光学装置の駆動回路の第３実施形態について説明する。図８は第３実施形態の等価回路図である。なお、第１実施形態と同一の構成要素については、同一符号を付してその説明を省略する。

【００９２】第３実施形態では、図８に示すように、シフトレジスタ４００の出力端にそれぞれ接続された各第１バッファ回路１２４の出力端には、それぞれ３つの第２バッファ回路１２５が接続されている。また、各第２バッファ回路１２５には、それぞれ２つのサンプリングスイッチ１２１が接続されている。

【００９３】次に図９を用いて第３実施形態のレイアウトについて説明する。

【００９４】サンプリング制御信号線１２１は、第２バッファ１２５回路の出力端子からサンプリングスイッチ１２１に向けて、中継配線８０と平行に交差された第２配線４２と、第２配線４２に接続されてさらに延設された第３配線４３と、画像信号線１１５と平行に延設された接続配線４５と、各サンプリングスイッチ１２１の各ゲート電極から引き出され、接続配線４５と接続された第４配線４８とからなる。第２配線４２と第２配線に接続された第３配線４３の間隙には２本の中継配線８０が第２配線４２及び第３配線４３に平行に延設されている。さらに、第３配線４３はコンタクトホール４７を介して接続配線４６に接続され、接続配線４６は中継配線８０に交差するように延設されている。また、第３配線４３はコンタクトホール４４と４５の間は第１導電層と第２導電層の二重配線となっている。接続配線４５は第１導電層からなり、サンプリングスイッチ１２１に接続されるように櫛型に延長された第４配線４８とコンタクトホール４７を介して接続されている。

【００９５】第３実施形態では、隣り合った２つのサンプリングスイッチ121に入力される２つのサンプリング制御信号線４０が互いに共通に第２バッファ回路１２５に接続されている。従って、図１３に示す従来の駆動回路と比較すればバッファ回路１２５の負荷が軽いため、バッファ回路１２５の出力側にはノイズが混入しに

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くく、したがって、サンプリング制御信号の変動を良好に抑制することができる。このため、データ線の信号の精度を高めることができ、よって良好が画像を得ることができる。

【００９６】また、２つ以上離れたデータ線６間への影響はバッファ回路１２５によって排除されるため、画面上で像が二重に表示されているようには認識し難く、事実上、ゴーストを排除することができる。

【００９７】第３実施形態では、１つの第２バッファ回路１２５から２つのサンプリングスイッチにサンプリング制御信号を供給するようにしているが、１つのバッファ回路から３つ以上のサンプリングスイッチにサンプリング制御信号を供給するようにしてもよい。

【００９８】－第４実施形態－

以下、図１０を用いて本発明による電気光学装置の駆動回路の第４実施形態について説明する。図１０は第４実施形態の等価回路図である。なお、第１実施形態と同一の構成要素については、同一符号を付してその説明を省略する。

【００９９】第４実施形態では、図１０に示すように、第１バッファ回路１２４と第２バッファ回路１２５とを互いに画像信号線１１５を隔てて配置し、第１バッファ回路１２４からのの出力線である第１配線を第２バッファ回路１２５の側で分岐させている。つまり、第１バッファ回路に接続された第１は緯線は画像信号線１１５を交差するように延設し、交差した後に分岐して複数の第２バッファ回路に並列に接続され、ている。

【０１００】このようなレイアウトを採用することにより、第４実施形態では第２バッファ１２５の出力線に該当するサンプリング制御信号線４０の配線の引き回しをより一層短くすることができ、また、画像信号線１１５からサンプリング制御信号線４０へのノイズの飛びつきを避けることができる。尚、実施形態１で説明したように、本実施形態においても第１バッファ回路１２４を設けなくても、シトレジスタ４００に大２バッファ回路１２５を直接駆動できる能力がある場合には、第１バッファ回路１２４を取り除き、シフトレジスタ４００の出力端を直接第２バッファ回路１２５に接続するようにしても良い。

【０１０１】（液晶表示装置の全体レイアウト）以下、図１１および図１２を用いて、本発明が適用されるアクティブマトリクス型の液晶表示装置の全体レイアウトについて第１の実施の形態の場合を例に挙げて説明する。

【０１０２】図１１において、ＴＦＴアレイ基板１０の上には、シール材１５２がその縁に沿って設けられており、その内側に並行して、額縁としての遮光膜１５３が設けられている。シール材１５２の外側の領域には、データ線駆動回路１０１及び実装端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、走査線駆動回路１０４が、この一辺に隣接する２辺に沿って設けら

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れている。シフトレジスタ４００、第１及び第２バッファ回路１２４，１２５はデータ線駆動回路１０１に含まれる。走査線駆動回路１０４に供給される走査信号遅延が問題にならないのならば、図１に示すように走査線駆動回路１０４は片側だけでも良いことは言うまでもない。また、データ線駆動回路１０１を画像表示領域の辺に沿って両側に配列してもよい。例えば奇数列のデータ線は画像表示領域ＤＡの一方の辺に沿って配設されたデータ線駆動回路から画像信号を供給し、偶数列のデータラインは画像表示領域ＤＡの反対側の辺に沿って配設されたデータ線駆動回路から画像信号を供給するようにしてもよい。この様にデータ線を櫛歯状に駆動するようにすれば、データ線駆動回路の占有面積を拡張することができるため、複雑な回路を構成することが可能となる。更にＴＦＴアレイ基板１０の残る一辺には、画像表示領域ＤＡの両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられており、更に、額縁としての遮光膜１５３の下に隠れてサンプリング回路１２１を設けるようにすると、データ線駆動回路１０１のレイアウト領域を拡張することができるため、大規模回路の内蔵や液晶装置１００の小型化が実現できる。また、対向基板２０のコーナー部の少なくとも１箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的導通をとるための導通材１０６が設けられている。そして、図１２に示すように、図１１に示したシール材１５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材１５２によりＴＦＴアレイ基板１０に固着され、内部に液晶５０が封入される。

【０１０３】以上、図１～図１２を参照して説明した各実施の形態における液晶装置のＴＦＴアレイ基板１０上には更に、製造途中や出荷時の当該液晶装置の品質、欠陥等を検査するための検査回路等を形成してもよい。また、データ線駆動回路１０１及び走査線駆動回路１０４をＴＦＴアレイ基板１０の上に設ける代わりに、例えばＴＡＢ（テープオートメイテッドボンディング基板）上に実装された駆動用ＬＳＩに、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して電気的及び機械的に接続するようにしてもよい。また、対向基板２０の投射光が入射する側及びＴＦＴアレイ基板１０の出射光が出射する側には各々、例えば、ＴＮ（ツイステッドネマティック）モード、ＳＴＮ（スーパーＴＮ）モード、Ｄ－ＳＴＮ（ダブル－ＳＴＮ）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【０１０４】上記実施の形態では、ＴＦＴを用いて各画素を駆動してもよいし、あるいはＴＦＴ以外の、例えばＴＦＤ（薄膜ダイオード）等のアクティブ素子を用いることも可能であり、さらに液晶装置をパッシブマトリクス型の液晶装置として構成することも可能である。ま

た、シリコン基板にスイッチング素子を形成してなる表示装置の駆動回路にも適用可能である。さらに、本発明は液晶装置以外の電気光学装置についても、広く適用することができる。

【０１０５】（電子機器）次に、以上詳細に説明した電気光学装置の一例として液晶装置１００を備えた電子機器の実施の形態について図１４から図１６を参照して説明する。

【０１０６】先ず図１４に、このように液晶装置１００を備えた電子機器の概略構成を示す。

【０１０７】図１４において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、液晶装置１００、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、画像信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回路１００２は、増幅・極性反転回路、シリアルーパラレル変換回路、ローテーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号CLKと共に駆動回路１００４に出力する。駆動回路１００４は、液晶装置１００を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、液晶装置１００を構成する液晶装置用基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【０１０８】次に図１５から図１６に、このように構成された電子機器の具体例を各々示す。

【０１０９】図１５において、電子機器の一例たる液晶プロジェクタ１１００は、上述した駆動回路１００４が液晶装置用基板上に搭載された液晶装置１００を含む液晶表示モジュールを３個用意し、各々ＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂに各々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにより各々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１１０】図１６において、電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００は、上述した液晶装置１００がトップカバーケース内に設けられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１１１】以上図１５から図１６を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図１４に示した電子機器の例として挙げられる。

【０１１２】以上説明したように、本実施の形態によれば、製造効率が高く高品位の画像表示が可能な液晶装置を備えた各種の電子機器を実現できる。

【０１１３】

【発明の効果】以上に説明したように、本発明によれば前記シフトレジスタの出力端に接続された第１バッファ回路と、前記第１バッファ回路の出力端に各々接続された複数の第２バッファ回路とを有し、前記複数の第２バッファ回路の出力端は前記ブロック内のサンプリングスイッチに接続されているので、サンプリング制御信号の波形の乱れを良好に抑制できるとともに、サンプリング制御信号線を介してのノイズの侵入を防ぐことができる。したがってゴーストの極めて少ない、あるいはゴーストのない、良好な画像を得ることができる。

【図面の簡単な説明】

【図１】第１実施形態の電気光学装置の駆動回路を示す等価回路図。

【図２】インピーダンス変換器の回路を示す図であり、（ａ）はバッファ回路を示す等価回路図、（ｂ）はインバータの回路を示す等価回路図。

【図３】表示情報処理回路および液晶装置の接続関係を示す図。

【図４】本発明の第１実施形態の画素群の平面図であり、（ｂ）は図４（ａ）のＣ－Ｃ’断面図。

【図５】第１実施形態の駆動回路のレイアウトを示す図。

【図６】第１実施形態の電気光学装置の駆動回路の動作を示すタイミングチャート。

【図７】第２実施形態の電気光学装置の駆動回路の動作を示すタイミングチャート。

【図８】第３実施形態の駆動回路の等価回路図。

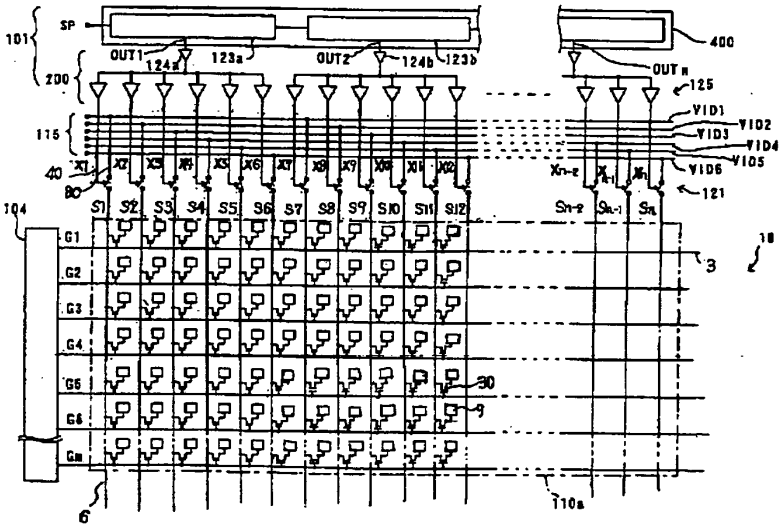
【図９】第３実施形態の電気光学装置の駆動回路のレイアウト図。

【図１０】第４実施形態の電気光学装置の等価回路図。
【図１１】電気光学装置全体構成を示す平面図。
【図１２】図１０のＨ－Ｈ’線における断面図。
【図１３】従来の電気光学装置の駆動回路を示す等価回路図。
【図１４】本発明による電子機器の実施の形態の概略構成を示すブロック図である。
【図１５】電子機器の一例として液晶プロジェクタを示す断面図である。
【図１６】電子機器の他の例としてパーソナルコンピュータを示す正面図である。

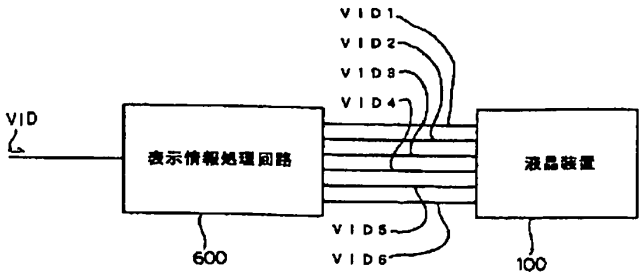
【符号の説明】

１００	液晶装置
１０１	走査線駆動回路
１２１	サンプリングスイッチ
４００	シフトレジスタ
１２４	第１バッファ回路
１２５	第２バッファ回路
１１５	画像信号線

【図１】

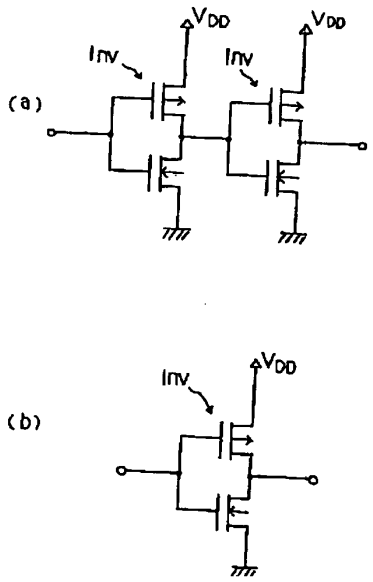


【図３】

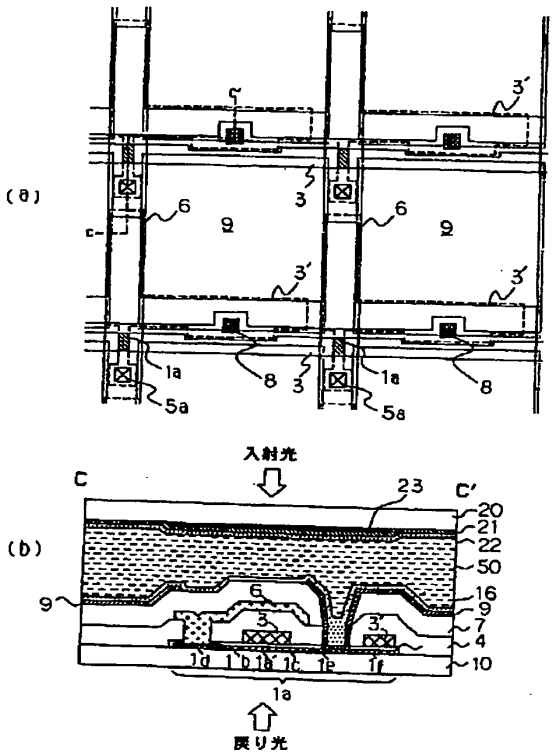


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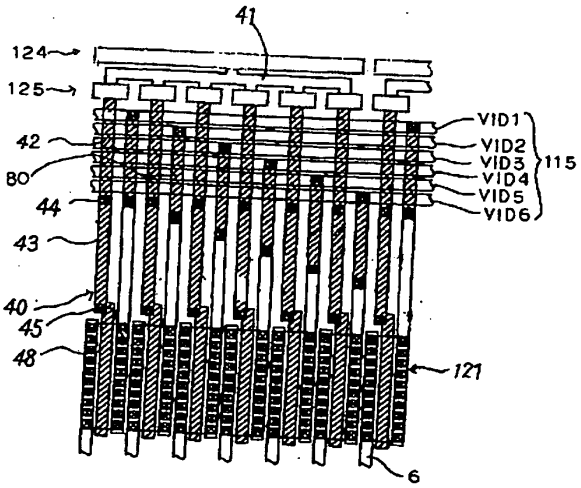
【図２】



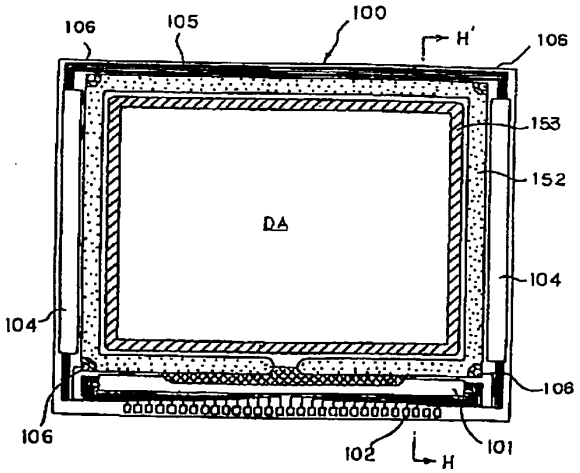
【図４】



【図５】

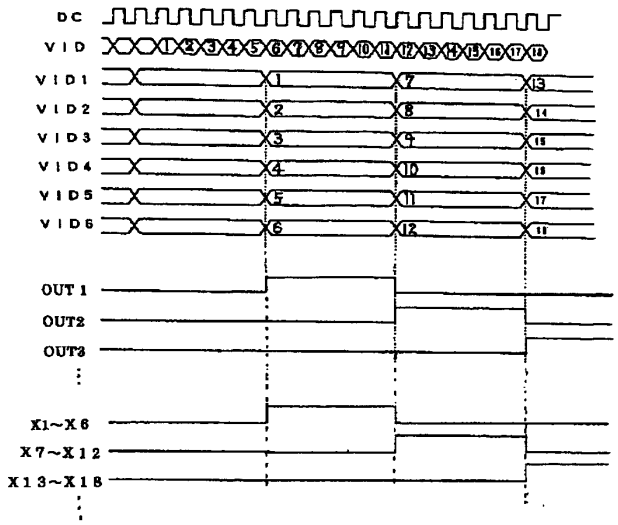


【図１１】

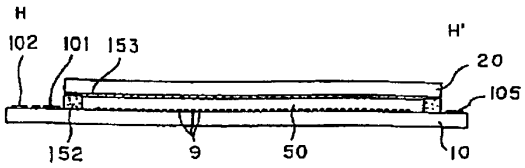


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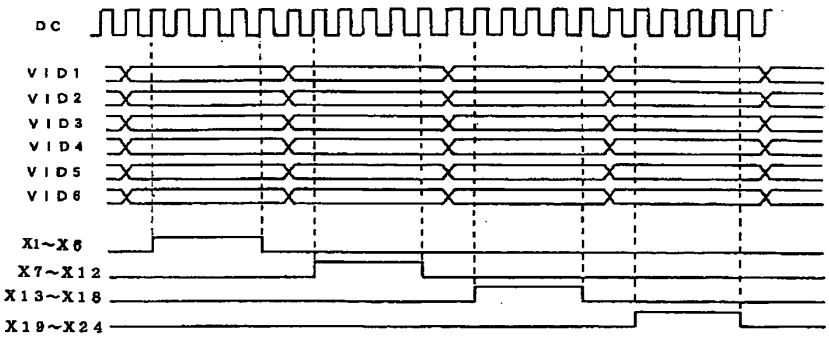
【図６】



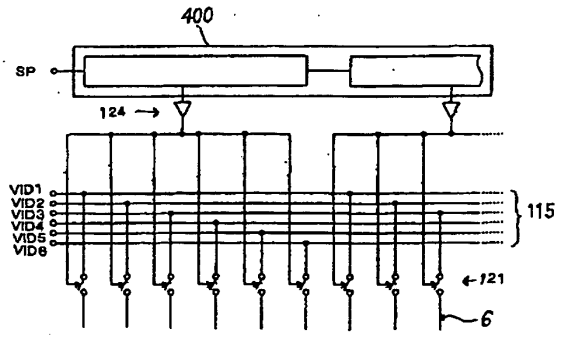
【図１２】



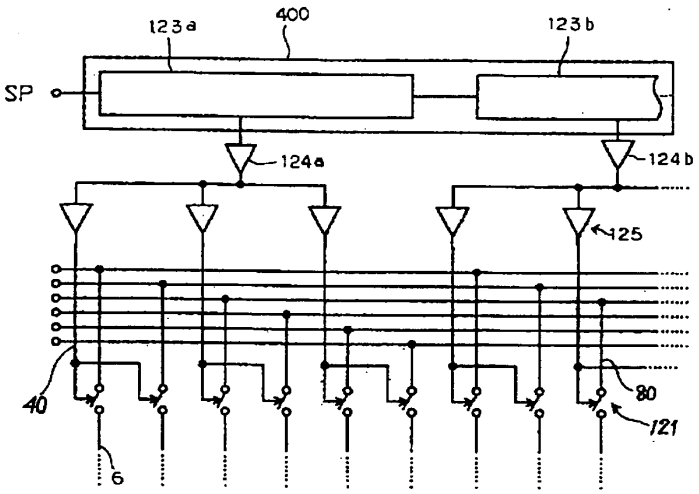
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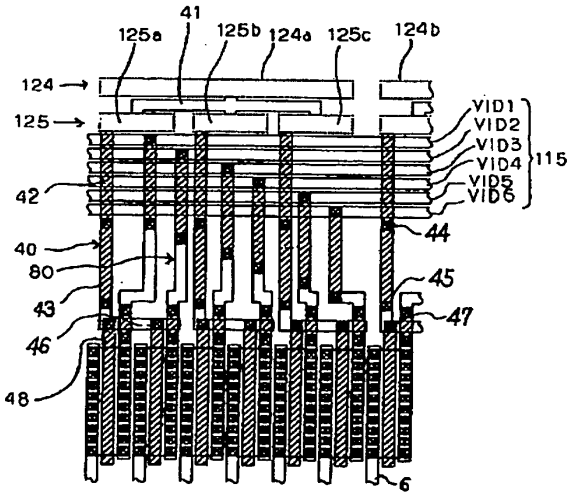
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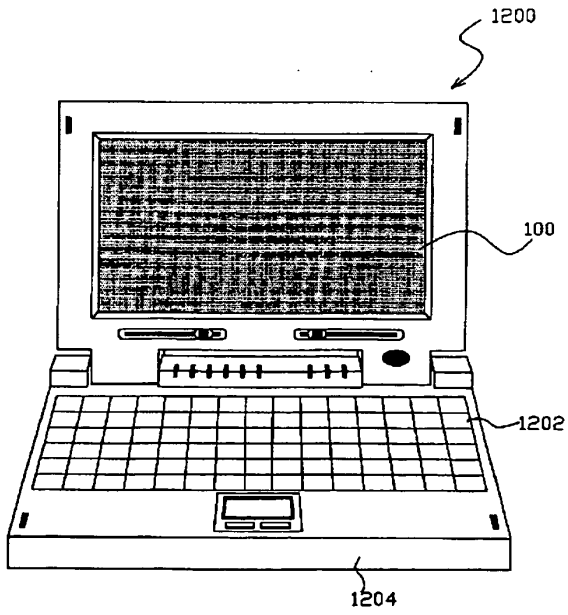
【図８】


123a
400
123b
SP
124a
124b
125
40
80
121
6

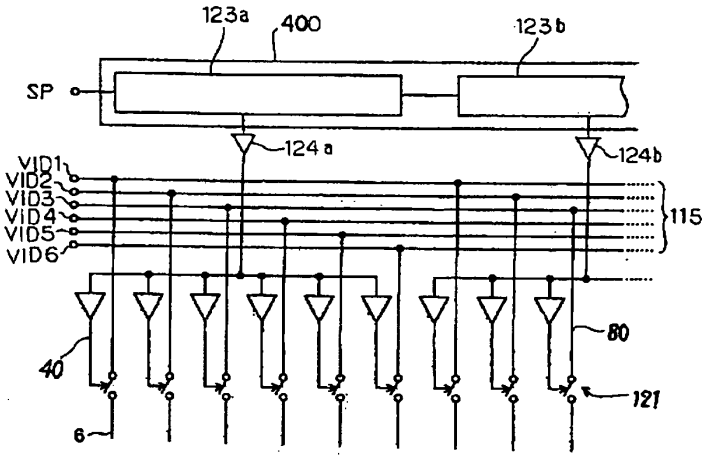
【図９】


41
125a
125b
124a
125c
124b
124
125
VID1
VID2
VID3
VID4
VID5
VID6
115
42
44
40
80
45
43
47
46
48
6

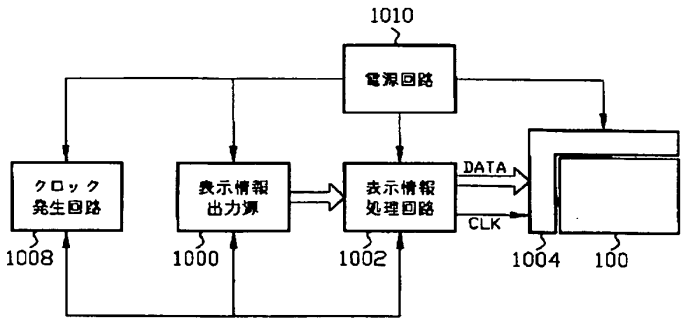
【図１６】


1200
100
1202
1204

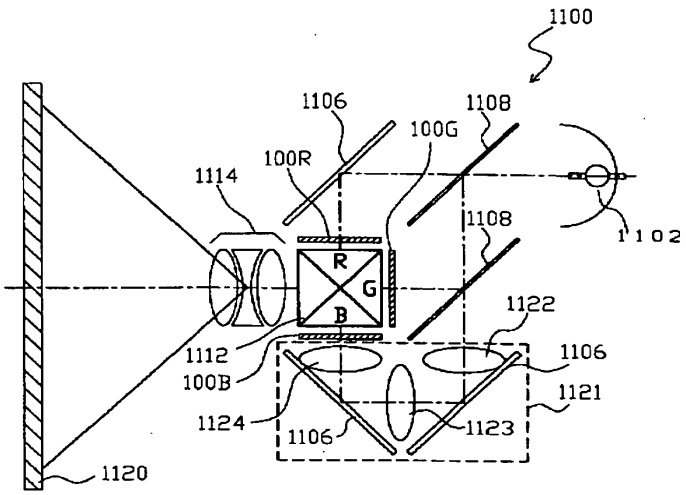
【図１０】


123a
400
123b
SP
124a
124b
VID1
VID2
VID3
VID4
VID5
VID6
115
80
40
121
6

【図１４】


1010
電源回路
クロック
発生回路
表示情報
出力源
表示情報
処理回路
DATA
CLK
1008
1000
1002
1004
100

【図１５】



フロントページの続き

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JJ06 KK02 KK43

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(71)Applicant : HITACHI LTD

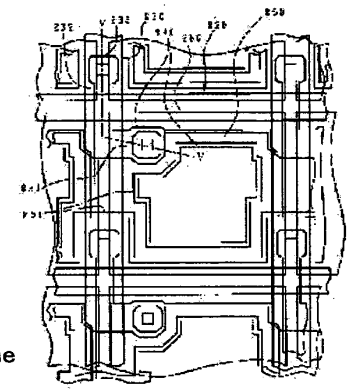
(72)Inventor : KAITO TAKUO
ABE HIRONOBU
SATO TOSHIHIRO

(54) LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To mitigate the electric field generated between pixel electrode and wiring arranged on its periphery, and to prevent the generation of domain, by disposing holding capacitor elements along the peripheral part of pixel region.

SOLUTION: The region enclosed by a gate signal wiring 220 and a drain line 230 constitutes one pixel region. A semiconductor layer 240 consisting of polysilicon is subjected to a heat treatment on its surface, by which a silicon oxidized film is formed thereon. This silicon film functions as a gate oxidized film in the region forming a thin-film transistor(TFT) and as a dielectric film in a region forming the holding capacitor element 250, respectively. The holding capacitor element 250 is provided with such a function as to accumulate the video signals after the off of the TFT for long and is formed along the periphery so as to enclose the pixel region. The electric fields generated between a pixel electrode 260 and the wirings, such as gate signal line 220 or drain signal line 230, arranged in the periphery of the pixel electrode are mitigated.



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CLAIMS

[Claim(s)]
[Claim 1] The liquid crystal display characterized by to carry out arrangement formation at the shape of a matrix at the liquid crystal pinched between the 1st substrate, the 2nd substrate, and the 1st substrate of the above and the 2nd substrate of the above, and the 1st substrate of the above, to have two or more pixel fields which have a switching element, and the retention volume component prepared for every above-mentioned pixel field, and to prepare the above-mentioned retention-volume component along with the periphery of the above-mentioned pixel field.
[Claim 2] The liquid crystal pinched between the 1st substrate, the 2nd substrate, and the 1st substrate of the above and the 2nd substrate of the above, Two or more pixel fields which arrangement formation is carried out at the shape of a matrix at the 1st substrate of the above, and have Pori silicon and a thin film transistor, The liquid crystal display characterized by having the drive circuit field which drives the above-mentioned thin film transistor, and the retention volume component prepared for every above-mentioned pixel field, and preparing the above-mentioned retention volume component along with the periphery of the above-mentioned pixel field.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is applied to the liquid crystal display equipped with a drive circuit on the substrate of the TFT (Thin Film Transisitor:, i.e., thin film transistor) method which consists of Pori silicon transistors especially about the liquid crystal display which has a minute pixel, and relates to an effective technique.
[0002]
[Description of the Prior Art] It has an active element for every pixel with the simple matrix liquid crystal indicating equipment which drives the pixel which consists of crossover fields of XY electrode of

the shape of a stripe established, respectively so that it might cross as a conventional liquid crystal display, when it saw from this substrate and a perpendicular direction on each opposite front face of a vertical substrate, and is divided roughly into the active matrix liquid crystal indicating equipment to which switching operation of this active element is carried out.

[0003] In order that the description of an active matrix liquid crystal indicating equipment may impress liquid crystal driver voltage (gradation electrical potential difference) to a pixel electrode through active elements, such as a thin film transistor, it does not have a cross talk between each pixel, and the special drive approach for preventing a cross talk like a simple matrix liquid crystal indicating equipment does not need to be used for it, and it is in a multi-gradation display being possible.

[0004] The active matrix liquid crystal indicating equipment of the TFT method which uses an amorphous silicon transistor or the Pori silicon transistor (polycrystal silicon transistor) for one of the active matrix liquid crystal indicating equipment of this as a thin film transistor is known.

[0005] In addition, henceforth [this] and in this specification, the liquid crystal display of the TFT method which used the a-SiTFT liquid crystal display and the Pori silicon transistor for the liquid crystal display of the TFT method which used [the amorphous silicon transistor] p-SiTr and an amorphous silicon transistor for a-SiTr and the Pori silicon transistor is called a p-SiTFT liquid crystal display.

[0006] The a-SiTFT liquid crystal display is widely used as a display of a personal computer or television.

[0007] However, in the a-SiTFT liquid crystal display, the drive circuit for driving liquid crystal needed to be prepared on the outskirts of external of a liquid crystal display panel (namely, a liquid crystal display component, LCD (Liquid Crystal Display)).

[0008] On the other hand, the liquid crystal display of the TFT method which used p-SiTr is developed and produced commercially in recent years.

[0009] By the liquid crystal display panel (a p-SiTFT liquid crystal display panel is called hereafter) of a p-SiTFT liquid crystal display, p-SiTr is arranged and formed on a quartz or a glass substrate like the liquid crystal display panel of an a-SiTFT liquid crystal display at the shape of a matrix.

[0010] Furthermore, since the working speed of p-SiTr is more nearly high-speed than a-SiTr, it is possible to also make the circumference circuit from a p-SiTFT liquid crystal display panel on the same substrate.

[0011] Drawing 11 is the outline top view of the pixel section circumference of the conventional p-SiTFT liquid crystal display panel (TFT-LCD).

[0012] In drawing 11 , 230 shows a drain signal line and the domain where in a semi-conductor layer and 220 a gate signal line and 260 generated a pixel electrode and 250, and a retention volume component and 261 generated [240] opening and 252.

[0013]

[Problem(s) to be Solved by the Invention] In the conventional liquid crystal display as shown in drawing 11 , the drain wire 230 and the gate line 220 were wired around each pixel electrode 260, by the electric field between these wiring and the pixel electrode 260, the domain 252 occurred and the fall of contrast etc. had had the bad influence on image quality. As this cure, a protection-from-light pattern is formed in one of substrate sides between two substrates, and the method of hiding the generated domain 252 is used. However, in order to hide a part of opening 261 by the protection-from-light pattern, there was a problem to which a numerical aperture falls victim and the display screen becomes dark. Especially in the p-SiTFT liquid crystal display which has a minute pixel, the effect of the electric field by wiring of the pixel electrode 260 circumference is large, and a numerical aperture is greatly influenced by the generating field of a domain.

[0014] This invention solves such a technical problem, one of the purpose of the eases the electric field produced between a pixel electrode and wiring arranged around it, and it is to offer the liquid crystal display of structure which can prevent generating of a domain.

[0015] Moreover, other purposes of this invention are to offer the liquid crystal display of the structure which has improved the numerical aperture.

[0016]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application. That is, arrangement formation is carried out at the shape of a matrix at the liquid crystal pinched between the (1) 1st substrate, the 2nd substrate, and the 1st substrate of the above and the 2nd substrate of the above, and the 1st substrate of the above, and it has two or more pixel fields which have a switching element, and the retention-volume component prepared for every above-mentioned pixel field, and considers as the liquid crystal display of a configuration of preparing the above-mentioned retention volume component along with the periphery of the above-mentioned pixel field.
[0017] (2) The liquid crystal pinched between the 1st substrate, the 2nd substrate, and the 1st substrate of the above and the 2nd substrate of the above, Two or more pixel fields which arrangement formation is carried out at the shape of a matrix at the 1st substrate of the above, and have Pori silicon and a thin film transistor, It has the drive circuit field which drives the above-mentioned thin film transistor, and the retention volume component prepared for every above-mentioned pixel field, and considers as the liquid crystal display of a configuration of preparing the above-mentioned retention volume component along with the periphery of the above-mentioned pixel field.
[0018] Thus, with the constituted liquid crystal display, in order to prepare a retention volume component between wiring and the pixel electrodes which were prepared around the pixel electrode, generating of a domain can be prevented by that by which the electric field generated around a pixel electrode are eased (the potential difference of a pixel electrode and surrounding wiring is lost). Moreover, since generating of a domain can be prevented and the protection-from-light pattern for hiding a domain becomes unnecessary, a numerical aperture is improvable.
[0019]
[Embodiment of the Invention] Hereafter, the gestalt of implementation of invention of this invention is explained to a detail with reference to a drawing.
[0020] In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0021] The outline top view in which drawing 2 (a) shows the physical relationship of each part of the liquid crystal display panel by which this invention is applied, and drawing 2 (b) are the outline sectional views in the A-A' cutting plane line of drawing 2 (a).
[0022] drawing 2 -- setting -- 110 -- a TFT substrate and 120 -- for the vertical-scanning circuit section and 183, as for a sealant and 121, the horizontal scanning circuit section and 165 are [a color filter substrate and 111 / a viewing area and 182 / a common electrode and 140] liquid crystal. While the pixel which becomes the viewing area 111 on the TFT substrate 110 from a thin film transistor, a pixel electrode, etc. is formed in the shape of a matrix, the drive circuit which consists of the vertical-scanning circuit section 182 and horizontal scanning circuit section 183 grade is formed around a viewing area 111. On the other hand, a color filter and common electrode 121 grade are formed in the color filter substrate 120. The TFT substrate 110 and the color filter substrate 120 are ******(ed) by having been prepared around the viewing area 111 by the sealant 165, and the container for liquid crystal enclosure is formed. In this container, liquid crystal 140 is enclosed and a liquid crystal display panel is formed.
[0023] Drawing 3 is the outline top view of the TFT substrate 110 shown in drawing 2 .
[0024] In drawing 3 , the gate signal line 220 which extends horizontally (x directions, the direction of a train), and is installed perpendicularly (the direction of y, line writing direction), and the drain signal line 230 which is insulated with these gate signal line 220, and is installed horizontally [extend perpendicularly and] are formed in the field by the side of the liquid crystal of the TFT substrate 110 in a viewing area 111 in this field. A pixel field is formed near the intersection of each [these] signal line. The pixel field prepared is arranged in the shape of a matrix, and forms a viewing area 111. [two or more] In addition, in drawing 3 , an equal circuit shows only one upper left pixel field for simplification,

and others are carrying out the illustration abbreviation. As for a thin film transistor and 115, 210 is [liquid crystal capacity and 116] retention volume. A thin film transistor 210 is turned on and off by the scan signal from the gate signal line 220, and the video signal from the drain signal line 230 minds a thin film transistor 210, and is written in and held as liquid crystal driver voltage (gradation electrical potential difference) at a pixel electrode. A pixel electrode forms one electrode of the liquid crystal capacity 115, and the common electrode 121 shown in drawing 2 forms the electrode of another side.

[0025] 170 is a connection terminal block for connecting with an external circuit, and, generally is collected and formed in the circumference edge of the TFT substrate 110. Various kinds of signals to the vertical-scanning circuit 182 and the horizontal scanning circuit 183 are told through a wiring layer 171 from the connection terminal block 170. As shown in drawing 2 , the common electrode 121 needs to prepare a flow member so that it may go over spacing of the TFT substrate 110 and the color filter substrate 120, in order to connect electrically the connection terminal block 170 and the common electrode 121, since it is prepared in the color filter substrate 120. For this reason, the contact section 177 is formed, conductive paste etc. is prepared between the common electrode 121 and the contact section 177, and electrical installation is performed.

[0026] Drawing 1 is the outline top view of the pixel section circumference of the p-SiTFT liquid crystal display panel in which the gestalt of 1 operation of this invention is shown.

[0027] Drawing 1 shows the configuration around of [one pixel section] the pixels of a large number arranged in the shape of [in the viewing area 111 of said TFT substrate 110] a matrix, and the field surrounded with the gate signal line 220 and the drain signal line 230 constitutes a 1-pixel field in drawing 1 .

[0028] In drawing 1 , the semi-conductor layer 240 which consists of Pori silicon is first formed in the main front face of the TFT substrate 110. This semi-conductor layer 240 is formed in the formation field of a thin film transistor (sign 210 reference of drawing 3), and the formation field of the retention volume component 250.

[0029] That front face is heat-treated, silicon oxide is formed, and, as for the semi-conductor layer 240 which consists of this Pori silicon, this silicon oxide functions as a dielectric film in the formation field of the retention volume component 250 as gate oxide in the formation field of a thin film transistor, respectively. Although this retention volume component 250 gives the function of accumulating the video signal after a thin film transistor turns off for a long time With the gestalt of this operation, so that a pixel field (or pixel opening) may be surrounded That is, along with the periphery of a pixel field, this retention volume component 250 is formed and it is used also for easing the electric field generated between wiring of the gate signal line 220 arranged around the pixel electrode 260 and this pixel electrode, or drain signal-line 230 grade.

[0030] The semi-conductor layer 240 which consists of Pori silicon in the formation field of the retention volume component 250 forms one electrode of the retention volume component 250 by doping the impurity of n mold through said silicon oxide.

[0031] Moreover, it is parallel to the gate signal line 220 which extends in the drawing Nakamizu common direction, and the retention volume wiring 251 is formed, like said semi-conductor layer 240, it is formed along with the periphery of a pixel field, and one electrode of the retention volume component 250 is formed around pixel electrode 260.

[0032] In addition, in the formation field of a thin film transistor, the impurity of n mold will be doped, the semi-conductor layer 240 will have conductivity in the part projected from both the sides of the gate signal line 220, and the source electrode 231 and the drain electrode 232 are formed in this part. Moreover, in the lower layer part of the gate signal line 220, the gate signal line 220 achieves the duty of a mask to the dope of said n type of impurity.

[0033] Furthermore, the drain signal line 230 which extends perpendicularly is horizontally installed by the TFT substrate 110, and is formed in it. This drain signal line 230 consists of aluminum, and is connected through the drain electrode 232 and the contact hole 233 of a thin film transistor.

[0034] Next, the manufacture approach of a TFT substrate which showed the pixel section is explained to drawing 1 for every step below with the manufacture approach of complementary MOS in a liquid crystal drive circuit using drawing 7 from drawing 4 . in addition, the formation field (it is equivalent to the cross section in the V-V cutting plane line of drawing 1) of the thin film transistor [in / on ****** and / in the left-hand side in drawing / each pixel] TFT -- moreover, the drawing Nakamigi side shows the formation field of the complementary MOS mold transistor formed in fields other than a viewing area. Moreover, the top view of the pixel section circumference within a production process is shown in drawing 10 R> 0 from drawing 8 .

[0035] The step 1. (drawing 4 (a)) main front face prepares the fully washed glass substrate 500.

[0036] The Pori silicon (poly-Si) layer 501 for forming the semi-conductor layer 240 of drawing 1 is formed by the deposition method throughout the main front face of the step 2. (drawing 4 (b)) glass substrate 500.

[0037] Selective etching of the step 3. (drawing 4 (c), drawing 8) this Pori silicon layer 501 is carried out. It is made for this Pori silicon layer 501 to make the formation field of the thin film transistor 210 (drawing 3) in a viewing area, and the retention volume component 250, and the formation field of the switching element (especially complementary MOS transistor) in fields other than a viewing area remain by this selective etching. In addition, the top view of this Pori silicon layer 501 (namely, semi-conductor layer 240 of drawing 1) after this step termination is shown in drawing 8 .

[0038] Step 4. (drawing 4 (d)) Silicon oxide 502 is formed in the front face of the Pori silicon layer 501 which remained by performing thermal oxidation processing. This silicon oxide 502 turns into gate oxide of the thin film transistor 210 grade formed behind.

[0039] Step 5. (drawing 4 (e)) The photoresist film 503 is applied throughout the main front face processed in this way, and the formation field of said retention volume component 250 is made to expose by the selection removal.

[0040] Then, high-concentration p mold impurity is doped using the ion implantation approach, and the Pori silicon layer 501 in the formation field of this retention volume component 250 is made to electric-conduction-ize. The part of this electric-conduction-ized Pori silicon layer 501 serves as one electrode of the retention volume component 250 formed behind.

[0041] Step 6. (drawing 5 (a)) Said extant photoresist film 503 is removed and the Pori silicon layer 504 by which Lynn (p) was doped is formed in the whole region for example, using the deposition method.

[0042] Step 7. (drawing 5 (b), drawing 9) While selective etching of said Pori silicon layer 504 is carried out and this forms each gate wiring 220 (drawing 1) of a thin film transistor 210 (drawing 3) and the complementary MOS mold transistor, and a gate electrode, the retention volume wiring 251 and the electrode of another side of the retention volume component 250 are formed. In addition, the top view after this step termination is shown in drawing 9 (the Pori silicon layer 501, the Pori silicon layer 504, gate wiring 220).

[0043] Step 8. (drawing 5 (c)) and said silicon oxide 502 exposed from the Pori silicon layer 504 by using the extant Pori silicon layer 504 as a mask are etched.

[0044] Silicon oxide 505 is formed in those front faces by oxidizing thermally lightly the Pori silicon layer 504 currently formed as the Pori silicon layer 501 exposed by etching of said silicon oxide 502, a gate electrode, etc.

[0045] Covering the whole region of p mold MOS transistor 270 among step 9. (drawing 5 (d)) complementary MOS mold transistors, MOS transistor 280 of n mold makes the photoresist film 506 form and expose. In addition, this p mold MOS transistor is a transistor which has a different conductivity type from a thin film transistor 210.

[0046] Then, high-concentration n mold impurity is doped for high-concentration n mold impurity using the ion implantation approach in the whole region of the front face processed in this way.

[0047] Step 10. (drawing 6 (a)) After removing the extant photoresist film 506 (drawing 5 (d)) and forming the still newer FOREJISUTO film 507 in the whole region, selection removal of this photoresist

film 507 is carried out. Only p mold MOS transistor 270 is made to expose among the complementary MOS mold transistors by this selection removal.
[0048] Then, p mold impurity which consists of boron fluoride (BF2) is doped by the ion implantation approach, and this forms the source electrode 271 and the drain electrode 272 of this MOS transistor.
[0049] Step 11. (drawing 6 (b)) The extant photoresist film 507 is removed, for example, sequential formation of silicon oxide and the phosphorus silicate glass film is carried out by vapor growth, and the insulator layer 508 of two-layer structure is formed.
[0050] Selective etching of the step 12. (drawing 6 (c)) insulator layer 508 is carried out. This selective etching is made in order to form a part of drain field of a thin film transistor 210, the source of each transistor of the complementary MOS mold transistor, the contact hole 233 of ** which makes the one section each of a drain field expose, and CH.
[0051] The aluminum film 509 is formed throughout an insulator layer 508 including the step 13. (drawing 6 (d)) contact hole 233 and the formation part of CH.
[0052] Selective etching of the step 14. (drawing 7 (a), drawing 10) aluminum film 509 is carried out, and the wiring layer (drain signal line 230) which has a connection in said contact hole 233 by this selective etching is formed. In addition, the top view after this step termination is shown in drawing 10 .
[0053] Step 15. (drawing 7 (b)) Throughout the front face in which the wiring layer was formed in this way, the insulator layer 510 which consists of silicon oxide is formed.
[0054] Then, selective etching removes the insulator layer 510 of the field section which corresponds on a pixel field and the outskirts of it.
[0055] Selective etching of the insulator layer 508 of the first layer equivalent to the part used as a step 16. (drawing 7 (c)) pixel field is carried out, and the Pori silicon layer 501 positioned in the lower layer of this insulator layer is made to expose.
[0056] Step 17. (drawing 7 (d)) The transparence electric conduction film is formed throughout the front face processed in this way, and by carrying out selective etching of this transparence electric conduction film, said pixel field and the transparence electric conduction film in the circumference of it are made to remain, and let this be the pixel electrode 260.
[0057] As mentioned above, although this invention was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of implementation of said invention, and does not deviate from the summary. For example, although this invention is applied to the active matrix liquid crystal indicating equipment of the TFT method which uses the Pori silicon transistor and its effectiveness is the largest, it is applicable also to the active matrix liquid crystal indicating equipment of the TFT method which uses an amorphous silicon transistor.
[0058]
[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
[0059] (1) Ease the electric field generated between wiring arranged around a pixel electrode and a pixel electrode, and prevent generating of a domain.
[0060] (2) It is not necessary to prepare the protection-from-light pattern for hiding a domain, and a numerical aperture improves. Moreover, poor doubling of a protection-from-light pattern and a TFT pattern is lost.
[0061] (3) the retention volume electrode which existed in prevention of generating of a domain from the former -- using -- **** -- the existing **** for manufacture processes -- things are made.
[0062] (4) Along with the periphery of a pixel field, by forming a retention volume electrode stair-like, it can consider as the configuration which a rapid level difference does not produce around the pixel section, and can decrease in the poor orientation generated because there is a level difference, and generating of a domain can be prevented.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline top view of the pixel section circumference of the p-SiTFT liquid crystal display panel in which the gestalt of 1 operation of this invention is shown.
[Drawing 2] The outline top view in which (a) shows the physical relationship of each part of the liquid crystal display panel by which this invention is applied, and (b) are the outline sectional views in the A-A' cutting plane line of (a).
[Drawing 3] It is the outline top view of the TFT substrate shown in drawing 2 .
[Drawing 4] It is the process sectional view showing the manufacture approach of the TFT substrate shown in drawing 1 .
[Drawing 5] It is the process sectional view showing the manufacture approach of the TFT substrate shown in drawing 1 .
[Drawing 6] It is the process sectional view showing the manufacture approach of the TFT substrate shown in drawing 1 .
[Drawing 7] It is the process sectional view showing the manufacture approach of the TFT substrate shown in drawing 1 .
[Drawing 8] It is the process top view of the pixel section circumference in the process shown in drawing 4 (c).
[Drawing 9] It is the process top view of the pixel section circumference in the process shown in drawing 5 (b).
[Drawing 10] It is the process top view of the pixel section circumference in the process shown in drawing 7 (a).
[Drawing 11] It is the outline top view of the pixel section circumference of the conventional p-SiTFT liquid crystal display panel.
[Description of Notations]
220 [-- A drain electrode, 233 / -- A contact hole, 240 / -- The semi-conductor layer which consists of Pori silicon, 250 / -- A retention volume component, 251 / -- Retention volume wiring.] -- A gate signal line, 230 -- A drain signal line, 231 -- A source electrode, 232

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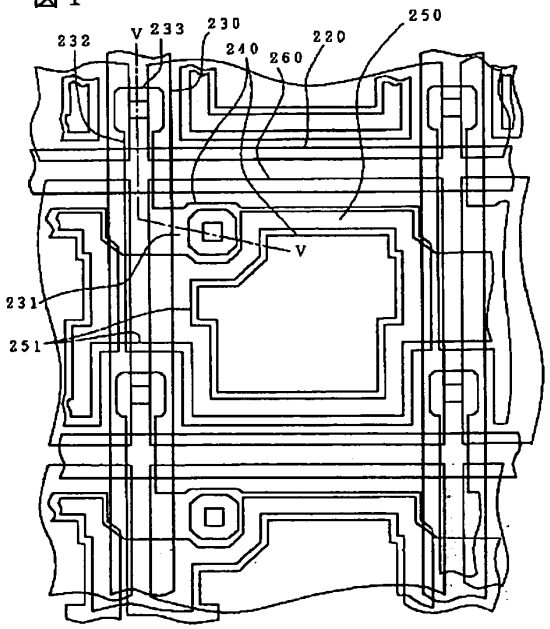
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(54)【発明の名称】液晶表示装置

(57)【要約】
【課題】画素電極とその周辺に配置された配線との間に生じる電界を緩和し、ドメインの発生を防止し、また、開口率を改善する。
【解決手段】スイッチング素子としてポリ・シリコン・薄膜トランジスタを有し、マトリクス状に配置され、ゲート信号線２２０とドレイン信号線２３０とで囲まれた画素領域の周辺部に沿って、保持容量素子２５０を形成する。

図１



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【特許請求の範囲】

【請求項１】第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板にマトリクス状に配置形成され、スイッチング素子を有する複数の画素領域と、上記画素領域毎に設けられた保持容量素子とを有し、

上記画素領域の周辺部に沿って、上記保持容量素子を設けたことを特徴とする液晶表示装置。

【請求項２】第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板にマトリクス状に配置形成され、ポリ・シリコン・薄膜トランジスタを有する複数の画素領域と、上記薄膜トランジスタを駆動する駆動回路領域と、上記画素領域毎に設けられた保持容量素子とを有し、

上記画素領域の周辺部に沿って、上記保持容量素子を設けたことを特徴とする液晶表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、微小画素を有する液晶表示装置に関し、特に、ポリ・シリコン・トランジスタで構成されるＴＦＴ（Thin Film Transisitor：すなわち、薄膜トランジスタ）方式の基板上に駆動回路を備える、液晶表示装置に適用して有効な技術に関するものである。

【０００２】

【従来の技術】従来の液晶表示装置としては、上下基板の各対向表面に該基板と垂直方向から見た場合に交差するようにそれぞれ設けたストライプ状のＸＹ電極の交差領域で構成される画素を駆動する単純マトリクス型液晶表示装置と、画素毎に能動素子を有し、この能動素子をスイッチング動作させるアクティブマトリクス型液晶表示装置に大別される。

【０００３】アクティブマトリクス型液晶表示装置の特徴は、例えば薄膜トランジスタ等の能動素子を介して画素電極に液晶駆動電圧（階調電圧）を印加するため、各画素間のクロストークがなく、単純マトリクス型液晶表示装置のようにクロストークを防止するための特殊な駆動方法を用いる必要がなく、多階調表示が可能なことにある。

【０００４】このアクティブマトリクス型液晶表示装置の一つに、薄膜トランジスタとして、アモルファス・シリコン・トランジスタ、あるいは、ポリ・シリコン・トランジスタ（多結晶シリコン・トランジスタ）を使用するＴＦＴ方式のアクティブマトリクス型液晶表示装置が知られている。

【０００５】なおこれ以降、本明細書中では、アモルファス・シリコン・トランジスタをａ－ＳｉＴｒ、ポリ・シリコン・トランジスタをｐ－ＳｉＴｒ、アモルファス・シリコン・トランジスタを使用したＴＦＴ方式の液晶表示装置をａ－ＳｉＴＦＴ液晶表示装置、ポリ・シリコン・トランジスタを使用したＴＦＴ方式の液晶表示装置をｐ－ＳｉＴＦＴ液晶表示装置と称する。

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【０００６】ａ－ＳｉＴＦＴ液晶表示装置は、パソコンあるいはテレビの表示装置として広く使用されている。

【０００７】しかしながら、ａ－ＳｉＴＦＴ液晶表示装置では、液晶を駆動するための駆動回路を、液晶表示パネル（すなわち、液晶表示素子、ＬＣＤ(Liquid Crystal Display)）の外部周辺に設ける必要があった。

【０００８】これに対して、近年、ｐ－ＳｉＴｒを使用したＴＦＴ方式の液晶表示装置が開発され、製品化されている。

【０００９】ｐ－ＳｉＴＦＴ液晶表示装置の液晶表示パネル（以下、ｐ－ＳｉＴＦＴ液晶表示パネルと称する）では、ａ－ＳｉＴＦＴ液晶表示装置の液晶表示パネル同様、石英あるいはガラス基板上にｐ－ＳｉＴｒを、マトリクス状に配置、形成する。

【００１０】さらに、ｐ－ＳｉＴｒの動作速度がａ－ＳｉＴｒよりも高速であるため、ｐ－ＳｉＴＦＴ液晶表示パネルでは、その周辺回路も同一基板上に作り込むことが可能である。

【００１１】図１１は、従来のｐ－ＳｉＴＦＴ液晶表示パネル（ＴＦＴ－ＬＣＤ）の画素部周辺の概略平面図である。

【００１２】図１１において、２３０はドレイン信号線、２４０は半導体層、２２０はゲート信号線、２６０は画素電極、２５０は保持容量素子、２６１は開口部、２５２は発生したドメインを示す。

【００１３】

【発明が解決しようとする課題】図１１に示すような従来の液晶表示装置では、各画素電極２６０の周辺にはドレイン線２３０、ゲート線２２０が配線されており、これら配線と画素電極２６０との間の電界によってドメイン２５２が発生し、コントラストの低下など、画質に悪影響を及ぼしていた。この対策として、２枚の基板のうちいずれか一方の基板面に遮光パターンを形成し、発生したドメイン２５２を隠す方法が用いられている。しかし、開口部２６１の一部を遮光パターンで隠すため、開口率が犠牲となり、表示画面が暗くなる問題があった。特に、微小画素を有するｐ－ＳｉＴＦＴ液晶表示装置では、画素電極２６０周辺の配線による電界の影響が大きく、ドメインの発生領域によって開口率が大きく左右される。

【００１４】本発明は、このような課題を解決するものであり、その目的の一つは、画素電極とその周辺に配置された配線との間に生じる電界を緩和し、ドメインの発生を防止し得る構造の液晶表示装置を提供することにある。

【００１５】また、本発明の他の目的は、開口率を改善した構造の液晶表示装置を提供することにある。

【００１６】

【課題を解決するための手段】本願において開示される発明のうち代表的なものの概要を簡単に説明すれば、下記の通りである。すなわち、（1）第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板にマトリクス状に配置形成され、スイッチング素子を有する複数の画素領域と、上記画素領域毎に設けられた保持容量素子とを有し、上記画素領域の周辺部に沿って、上記保持容量素子を設ける構成の液晶表示装置とする。

【００１７】（2）第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板にマトリクス状に配置形成され、ポリ・シリコン・薄膜トランジスタを有する複数の画素領域と、上記薄膜トランジスタを駆動する駆動回路領域と、上記画素領域毎に設けられた保持容量素子とを有し、上記画素領域の周辺部に沿って、上記保持容量素子を設ける構成の液晶表示装置とする。

【００１８】このように構成された液晶表示装置では、画素電極の周辺に設けられた配線と画素電極との間に保持容量素子を設けるために、画素電極周辺に発生する電界が緩和される（画素電極と周辺の配線との電位差がなくなる）ので、ドメインの発生を防止することができる。また、ドメインの発生を防止できるので、ドメインを隠すための遮光パターンが不要となるため、開口率を改善することができる。

【００１９】

【発明の実施の形態】以下、図面を参照して本発明の発明の実施の形態を詳細に説明する。

【００２０】なお、発明の実施の形態を説明するための全図において、同一の機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【００２１】図２（ａ）は、本発明が適用される液晶表示パネルの各部の位置関係を示す概略平面図、図２（ｂ）は図２（ａ）のＡ－Ａ’切断線における概略断面図である。

【００２２】図２において、１１０はＴＦＴ基板、１２０はカラーフィルタ基板、１１１は表示領域、１８２は垂直走査回路部、１８３は水平走査回路部、１６５はシール材、１２１は共通電極、１４０は液晶である。ＴＦＴ基板１１０上の表示領域１１１には薄膜トランジスタ、画素電極等からなる画素がマトリクス状に形成されると共に、表示領域１１１の周辺には垂直走査回路部１８２、水平走査回路部１８３等からなる駆動回路等が形成される。他方、カラーフィルタ基板１２０には、カラーフィルタと共通電極１２１等が形成される。ＴＦＴ基板１１０とカラーフィルタ基板１２０とは、表示領域１１１の周辺に設けられたにシール材１６５により貼合わされ、液晶封入用の容器を形成する。この容器内に液晶１４０が封入され、液晶表示パネルが形成される。

【００２３】図３は、図２に示したＴＦＴ基板１１０の概略平面図である。

【００２４】図３において、表示領域１１１におけるＴＦＴ基板１１０の液晶側の面には、該面において、例えば、水平方向（ｘ方向、列方向）に延在し、かつ垂直方向（ｙ方向、行方向）に並設されるゲート信号線２２０と、これらゲート信号線２２０と絶縁されて垂直方向に延在し、かつ水平方向に並設されるドレイン信号線２３０とが形成される。これら各信号線の交点近傍には、画素領域が形成される。複数設けられる画素領域はマトリックス状に配置され、表示領域１１１を形成する。なお図３では、簡略化のため左上の一つの画素領域のみを等価回路で示し、他は図示省略している。２１０は薄膜トランジスタ、１１５は液晶容量、１１６は保持容量である。薄膜トランジスタ２１０は、ゲート信号線２２０からの走査信号によってオン・オフされ、ドレイン信号線２３０からの映像信号が薄膜トランジスタ２１０を介して画素電極に液晶駆動電圧（階調電圧）として、書き込み・保持される。画素電極は液晶容量１１５の一方の電極を形成し、図２に示す共通電極１２１が他方の電極を形成する。

【００２５】１７０は外部回路と接続するための接続端子群で、一般にＴＦＴ基板１１０の周辺端部に集められて形成される。垂直走査回路１８２及び水平走査回路１８３への各種の信号は接続端子群１７０から配線層１７１を介して伝えられる。図２に示すように、共通電極１２１はカラーフィルタ基板１２０に設けられるため、接続端子群１７０と共通電極１２１とを電気的に接続するには、ＴＦＴ基板１１０とカラーフィルタ基板１２０との間隔をわたるように導通部材を設ける必要がある。このため、コンタクト部１７７が設けられ、共通電極１２１とコンタクト部１７７との間に、導電ペースト等が設けられ、電気的接続が行われる。

【００２６】図１は、本発明の一実施の形態を示すｐ－ＳｉＴＦＴ液晶表示パネルの画素部周辺の概略平面図である。

【００２７】図１は、前記ＴＦＴ基板１１０の表示領域１１１内のマトリクス状に配置された多数の画素のうちの一つの画素部周辺の構成を示しており、図１において、ゲート信号線２２０とドレイン信号線２３０とで囲まれた領域が一画素領域を構成する。

【００２８】図１において、まずＴＦＴ基板１１０の主表面にポリ・シリコンからなる半導体層２４０が形成されている。この半導体層２４０は、薄膜トランジスタ（図３の符号２１０参照）の形成領域および保持容量素子２５０の形成領域に形成されている。

【００２９】このポリ・シリコンからなる半導体層２４０は、その表面が熱処理されてシリコン酸化膜が形成されており、このシリコン酸化膜は、薄膜トランジスタの形成領域においてはゲート酸化膜として、また、保持容量素子２５０の形成領域においては誘電体膜としてそれ

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ぞれ機能するようになっている。この保持容量素子２５０は、薄膜トランジスタがオフした後の映像信号を長く蓄積する等の機能をもたせるものであるが、本実施の形態では、画素領域（あるいは画素開口部）を囲むように、すなわち、画素領域の周辺部に沿って、この保持容量素子２５０を形成し、画素電極２６０と該画素電極周辺に配置されたゲート信号線２２０またはドレイン信号線２３０等の配線との間で発生する電界を緩和することにも用いられている。

【００３０】保持容量素子２５０の形成領域におけるポリ・シリコンからなる半導体層２４０は、例えばｎ型の不純物が前記シリコン酸化膜を通してドープされることにより保持容量素子２５０の一方の電極を形成する。

【００３１】また、図中水平方向に延在するゲート信号線２２０に平行して、保持容量配線２５１が形成されており、画素電極２６０周辺では前記半導体層２４０と同じように、画素領域の周辺部に沿って形成され、保持容量素子２５０の一方の電極を形成する。

【００３２】なお、半導体層２４０は薄膜トランジスタの形成領域では、ゲート信号線２２０の両脇から突出した部分において、ｎ型の不純物がドープされ、導電性を有することとなり、この部分においてソース電極２３１およびドレイン電極２３２が形成される。またゲート信号線２２０の下層の部分では、前記ｎ型の不純物のドープに対してゲート信号線２２０がマスクの役目をはたす。

【００３３】さらに、ＴＦＴ基板１１０には垂直方向に延在するドレイン信号線２３０が水平方向に並設されて形成されている。このドレイン信号線２３０は、例えばアルミニウムからなり、薄膜トランジスタのドレイン電極２３２とコンタクト孔２３３を介して接続されている。

【００３４】次に、図１に画素部を示したＴＦＴ基板の製造方法を、液晶駆動回路内のコンプリメンタリＭＯＳの製造方法とともに、図４から図７を用いて以下ステップ毎に説明する。なお、同各図において、図中左側は各画素における薄膜トランジスタＴＦＴの形成領域（図１のＶ－Ｖ切断線における断面に相当する）を、また、図中右側は表示領域以外の領域に形成されたコンプリメンタリＭＯＳ型トランジスタの形成領域を示している。また、製造工程内での画素部周辺の平面図を図８から図１０に示す。

【００３５】ステップ１．（図４（ａ））

主表面が充分に洗浄されたガラス基板５００を用意する。

【００３６】ステップ２．（図４（ｂ））

ガラス基板５００の主表面の全域に例えばデポジション法によって、図１の半導体層２４０を形成するためのポリ・シリコン（ｐｏｌｙ－Ｓｉ）層５０１を形成する。

【００３７】ステップ３．（図４（ｃ）、図８）

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該ポリ・シリコン層５０１を選択エッチングする。この選択エッチングにより、該ポリ・シリコン層５０１は、表示領域における薄膜トランジスタ２１０（図３）および保持容量素子２５０の形成領域、表示領域以外の領域におけるスイッチング素子（特にコンプリメンタリＭＯＳトランジスタ）の形成領域に残存させるようにする。なお、図８に本ステップ終了後の該ポリ・シリコン層５０１（すなわち、図１の半導体層２４０）の平面図を示す。

【００３８】ステップ４．（図４（ｄ））

残存されたポリ・シリコン層５０１の表面に熱酸化処理を施すことにより、シリコン酸化膜５０２を形成する。このシリコン酸化膜５０２は、後に形成される薄膜トランジスタ２１０等のゲート酸化膜となるものである。

【００３９】ステップ５．（図４（ｅ））

このように加工された主表面の全域にフォトレジスト膜５０３を塗布し、その選択除去により前記保持容量素子２５０の形成領域を露呈させる。

【００４０】その後、イオン打ち込み方法を用いて高濃度のｐ型不純物をドープして、該保持容量素子２５０の形成領域におけるポリ・シリコン層５０１を導電化させる。この導電化されたポリ・シリコン層５０１の部分は、後に形成される保持容量素子２５０の一方の電極となるものである。

【００４１】ステップ６．（図５（ａ））

残存されている前記フォトレジスト膜５０３を除去し、リン（ｐ）がドープされたポリ・シリコン層５０４を例えばデポジション法を用いて全域に形成する。

【００４２】ステップ７．（図５（ｂ）、図９）

前記ポリ・シリコン層５０４を選択エッチングし、これにより薄膜トランジスタ２１０（図３）およびコンプリメンタリＭＯＳ型トランジスタの各ゲート配線２２０（図１）や、ゲート電極を形成するとともに、保持容量配線２５１や、保持容量素子２５０の他方の電極を形成する。なお、図９に本ステップ終了後の平面図を示す（ポリ・シリコン層５０１、ポリ・シリコン層５０４、ゲート配線２２０）。

【００４３】ステップ８．（図５（ｃ））

そして、残存されているポリ・シリコン層５０４をマスクとしてポリ・シリコン層５０４から露呈されている前記シリコン酸化膜５０２をエッチングする。

【００４４】前記シリコン酸化膜５０２のエッチングにより露呈されたポリ・シリコン層５０１、およびゲート電極等として形成されているポリ・シリコン層５０４を軽く熱酸化することにより、それらの表面にシリコン酸化膜５０５を形成する。

【００４５】ステップ９．（図５（ｄ））

コンプリメンタリＭＯＳ型トランジスタのうち、ｐ型ＭＯＳトランジスタ２７０の全域を覆ってフォトレジスト膜５０６を形成する、また、ｎ型のＭＯＳ型トランジス

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タ２８０は露呈させる。なお、該ｐ型ＭＯＳ型トランジスタは、薄膜トランジスタ２１０と異なる導電型を有するトランジスタである。

【００４６】その後、このように加工された表面の全域に高濃度のｎ型不純物をイオン打ち込み方法を用いて高濃度のｎ型不純物をドープする。

【００４７】ステップ１０．（図６（ａ））

残存されているフォトレジスト膜５０６（図５（ｄ））を除去し、さらに新たなフォレジスト膜５０７を全域に形成した後、このフォトレジスト膜５０７を選択除去する。この選択除去によって、コンプリメンタリＭＯＳ型トランジスタのうち、ｐ型ＭＯＳ型トランジスタ２７０のみを露呈させる。

【００４８】その後、フッ化ボロン（BF_2）からなるｐ型不純物をイオン打ち込み方法によりドープし、これにより該ＭＯＳトランジスタのソース電極２７１およびドレイン電極２７２を形成する。

【００４９】ステップ１１．（図６（ｂ））

残存しているフォトレジスト膜５０７を除去し、例えば気相成長法によってシリコン酸化膜およびリンシリケートガラス膜を順次形成して、２層構造の絶縁膜５０８を形成する。

【００５０】ステップ１２．（図６（ｃ））

絶縁膜５０８を選択エッチングする。この選択エッチングは、薄膜トランジスタ２１０のドレイン領域の一部、コンプリメンタリＭＯＳ型トランジスタのそれぞれのトランジスタのソース、ドレイン領域の各一部を露呈させるめのコンタクト孔２３３、ＣＨを形成するためになされる。

【００５１】ステップ１３．（図６（ｄ））

コンタクト孔２３３、ＣＨの形成部分を含んで絶縁膜５０８の全域にアルミニウム膜５０９を形成する。

【００５２】ステップ１４．（図７（ａ）、図１０）

アルミニウム膜５０９を選択エッチングし、この選択エッチングにより前記コンタクト孔２３３において接続部を有する配線層（ドレイン信号線２３０）が形成される。なお、図１０に本ステップ終了後の平面図を示す。

【００５３】ステップ１５．（図７（ｂ））

このように配線層が形成された表面の全域に、シリコン酸化膜からなる絶縁膜５１０を形成する。

【００５４】その後、画素領域およびその周辺に相当する領域部の絶縁膜５１０を選択エッチングによって除去する。

【００５５】ステップ１６．（図７（ｃ））

画素領域となる部分に相当する一層目の絶縁膜５０８を選択エッチングし、この絶縁膜の下層に位置づけられるポリ･シリコン層５０１を露呈させる。

【００５６】ステップ１７．（図７（ｄ））

このように加工された表面全域に透明導電膜を形成し、この透明導電膜を選択エッチングすることにより前記画

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素領域およびその周辺における透明導電膜を残存させ、これを画素電極２６０とする。

【００５７】以上、本発明を発明の実施の形態に基づき具体的に説明したが、本発明は、前記発明の実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更し得ることは言うまでもない。例えば、本発明は、ポリ･シリコン・トランジスタを使用するＴＦＴ方式のアクティブマトリクス型液晶表示装置に適用して最も効果が大きいが、アモルファス･シリコン・トランジスタを使用するＴＦＴ方式のアクティブマトリクス型液晶表示装置にも適用可能である。

【００５８】

【発明の効果】本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば下記の通りである。

【００５９】（１）画素電極と画素電極周辺に配置された配線との間に発生する電界を緩和し、ドメインの発生を防止する。

【００６０】（２）ドメインを隠すための遮光パターンを設ける必要がなく、開口率が向上する。また、遮光パターンとＴＦＴパターンとの合わせ不良が無くなる。

【００６１】（３）ドメインの発生の防止に、従来から存在した保持容量電極を用いており、既存の製造プロセス用いることができる。

【００６２】（４）画素領域の周辺部に沿って、保持容量電極を階段状に形成することで、画素部周辺で急激な段差が生じない構成とし、段差があることで発生する配向不良を減少することができ、ドメインの発生を防止できる。

【図面の簡単な説明】

【図１】本発明の一実施の形態を示すｐ－ＳｉＴＦＴ液晶表示パネルの画素部周辺の概略平面図である。

【図２】（ａ）は本発明が適用される液晶表示パネルの各部の位置関係を示す概略平面図、（ｂ）は（ａ）のＡ－Ａ’切断線における概略断面図である。

【図３】図２に示したＴＦＴ基板の概略平面図である。

【図４】図１に示したＴＦＴ基板の製造方法を示す工程断面図である。

【図５】図１に示したＴＦＴ基板の製造方法を示す工程断面図である。

【図６】図１に示したＴＦＴ基板の製造方法を示す工程断面図である。

【図７】図１に示したＴＦＴ基板の製造方法を示す工程断面図である。

【図８】図４（ｃ）に示した工程における画素部周辺の工程平面図である。

【図９】図５（ｂ）に示した工程における画素部周辺の工程平面図である。

【図１０】図７（ａ）に示した工程における画素部周辺の工程平面図である。

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【図１１】従来のｐ－ＳｉＴＦＴ液晶表示パネルの画素部周辺の概略平面図である。

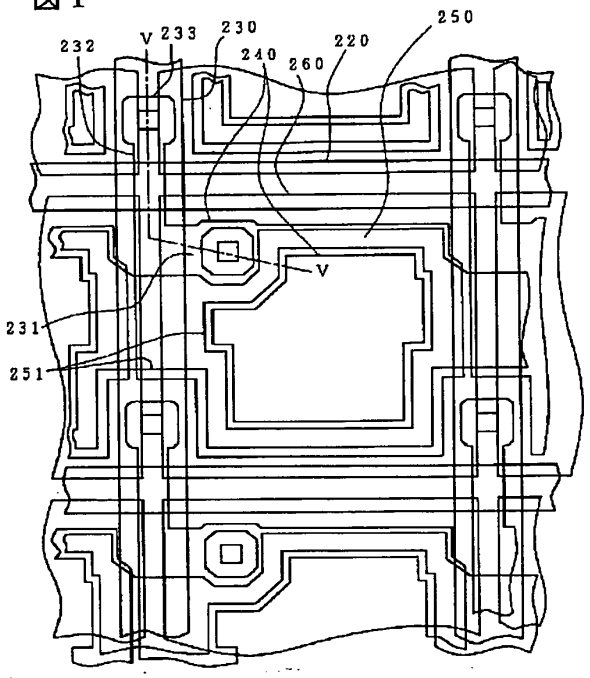
【符号の説明】

２２０…ゲート信号線、２３０…ドレイン信号線、２３１…ソース電極、２３２…ドレイン電極、２３３…コンタクト孔、２４０…ポリ・シリコンからなる半導体層、２５０…保持容量素子、２５１…保持容量配線。

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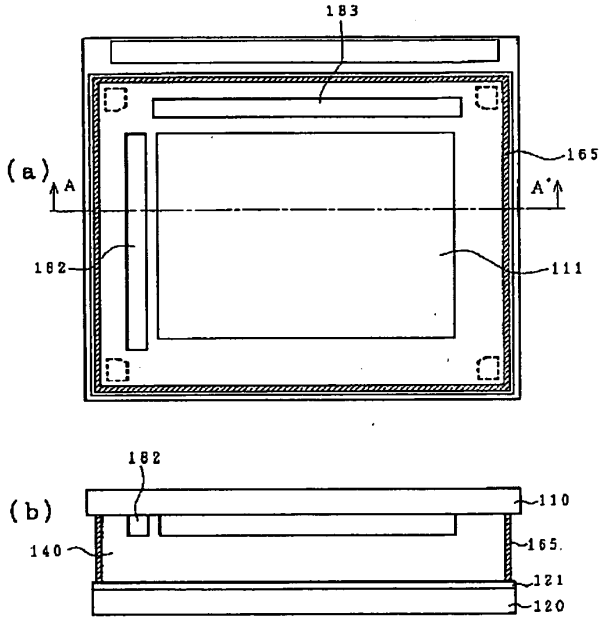
【図1】

図1



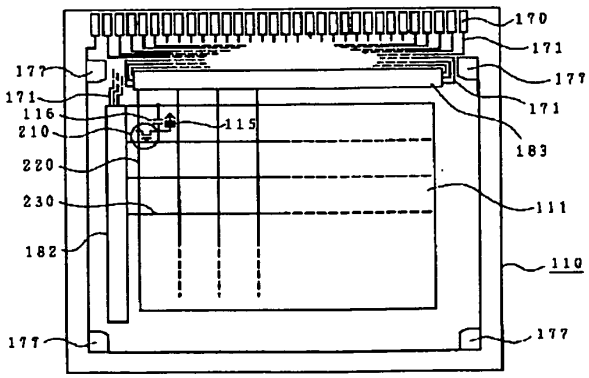
【図2】

図2



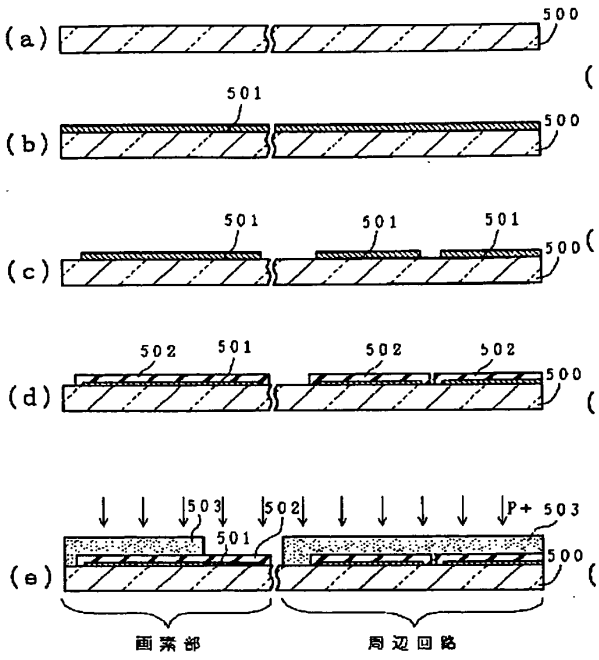
【図3】

図3



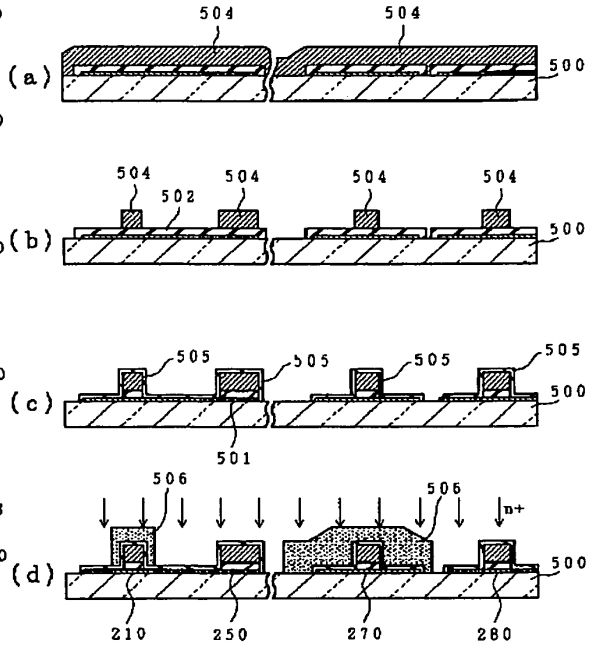
【図4】

図4



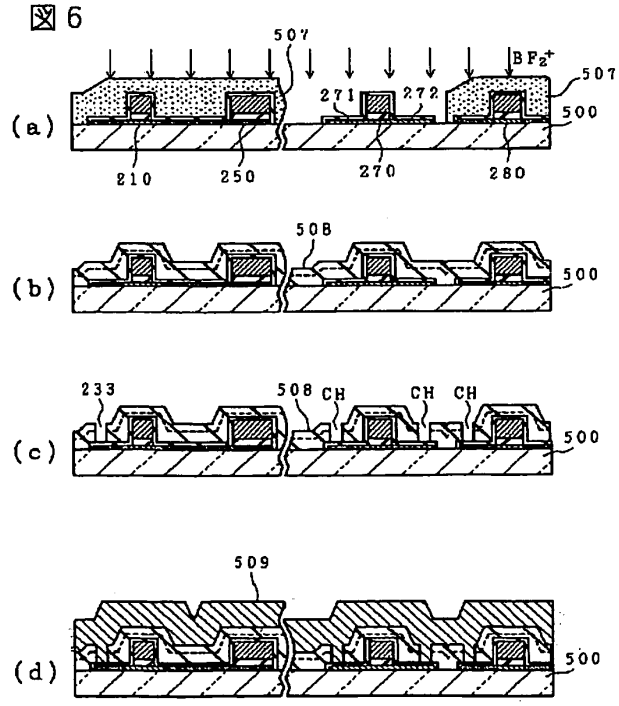
【図5】

図5



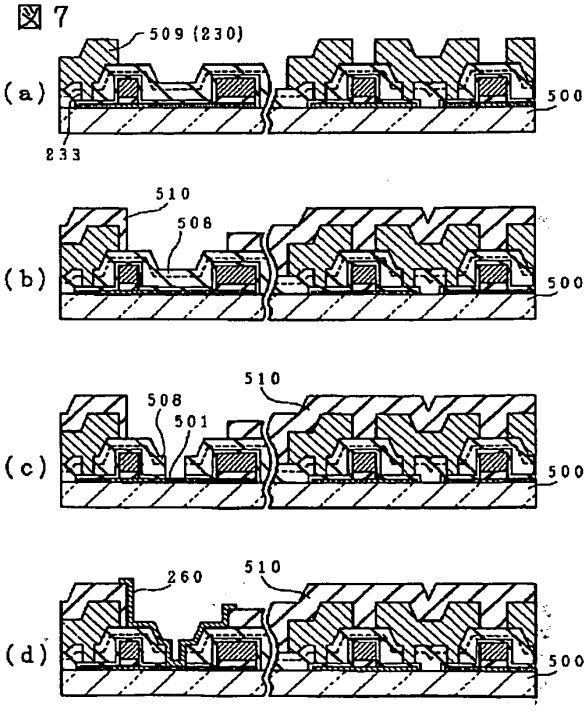
【図6】

図6



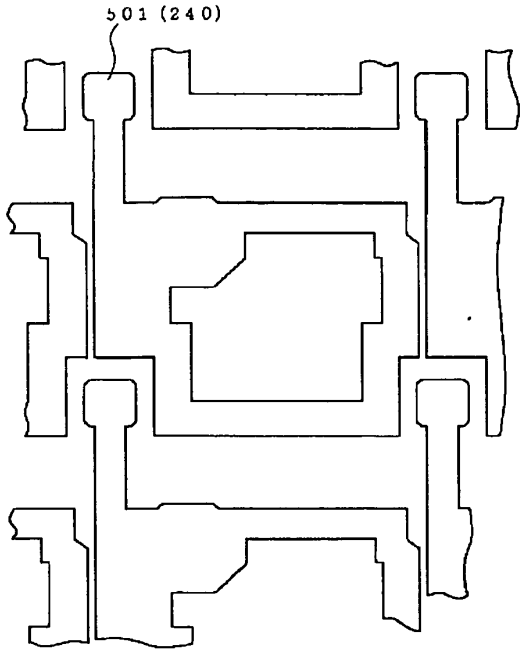
【図7】

図7



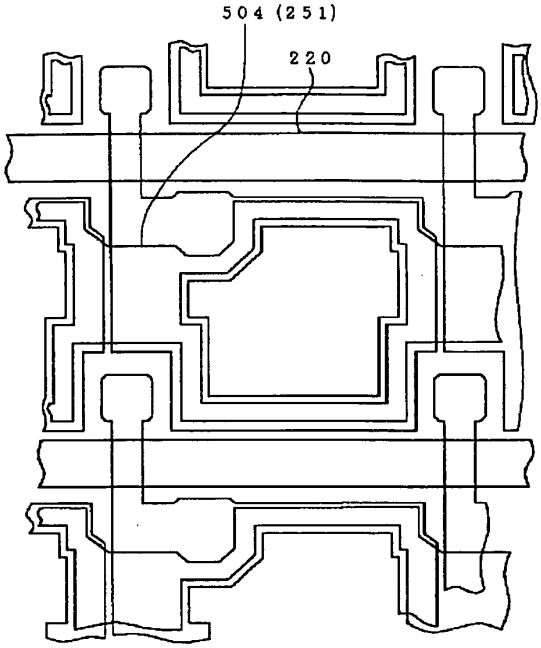
【図８】

図８



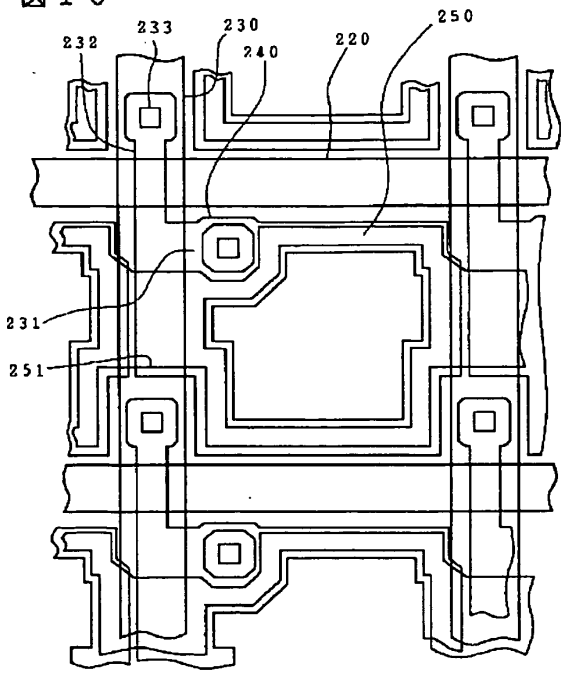
【図９】

図９



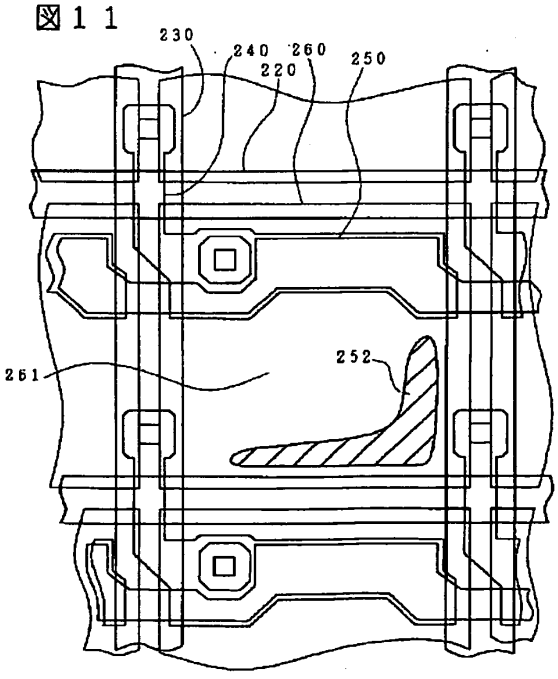
【図１０】

図１０



【図１１】

図１１



【公開番号】特開平１０－２５３９８４
【公報種別】特許法第１７条の２の規定による補正の掲載
【ＳＴ公報種別】A5
【公開日】平成１０年（１９９８）９月２５日
【出願番号】特願平９－５４４０５
【発行日】２００５年（２００５）１月６日
【部門区分】第６部門第２区分
【国際特許分類第７版】
G02F 1/136
G02F 1/1343
G09F 9/30
H01L 29/786
【ＦＩ】
G02F 1/136 500
G02F 1/1343
G09F 9/30 338
H01L 29/78 612 C

【手続補正書】
【提出日】２００４年（２００４）２月１３日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正の内容】

【特許請求の範囲】
【請求項１】
第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板上に形成された複数のドレイン信号線と複数の保持容量配線と、上記第１の基板上にマトリクス状に配置形成され、スイッチング素子を有する複数の画素領域と、上記画素領域毎に設けられた保持容量素子とを有し、
上記保持容量素子は、上記保持容量配線と上記スイッチング素子に接続された半導体層との間で形成されており、上記ドレイン信号線に沿って形成されていることを特徴とする液晶表示装置。
【請求項２】
第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板上に形成されたゲート信号線とドレイン信号線と、上記ゲート信号線と上記ドレイン信号線とに接続された薄膜トランジスタと、上記薄膜トランジスタに接続された画素電極と、保持容量配線とを有する液晶表示装置であって、
上記薄膜トランジスタと上記画素電極とに接続された半導体層と、上記保持容量配線との間で保持容量素子が形成され、
上記保持容量素子は上記ドレイン信号線に沿って形成されていることを特徴とする液晶表示装置。
【請求項３】
上記保持容量素子を形成する上記半導体層と上記薄膜トランジスタのソース電極を形成する半導体層とは同一の層であることを特徴とする請求項２に記載の液晶表示装置。
【請求項４】
上記第１の基板上に上記保持容量素子を形成する上記半導体層が形成され、上記半導体層の上に上記保持容量配線が形成され、上記保持容量配線の上に上記画素電極が形成されていることを特徴とする請求項２に記載の液晶表示装置。

日本国特許庁(JP)
日本国特許庁(JP)
日本国特許庁(JP)
日本国特許庁(JP)
日本国特許庁(JP)
日本国特許庁(JP)
特許法第17条ノ2ノ規定ニヨル補正ノ掲載
日本国特許庁(JP)
特開平11-223832
特開2000-162634
特開平10-253984

【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】００１６
【補正方法】変更
【補正の内容】

【００１６】
【課題を解決するための手段】
上記課題を解決するために、本発明は、第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板上に形成された複数のドレイン信号線と複数の保持容量配線と、上記第１の基板上にマトリクス状に配置形成され、スイッチング素子を有する複数の画素領域と、上記画素領域毎に設けられた保持容量素子とを有し、上記保持容量素子は、上記保持容量配線と上記スイッチング素子に接続された半導体層との間で形成されており、上記ドレイン信号線に沿って形成されていることを特徴とする。
また、第１の基板と、第２の基板と、上記第１の基板と上記第２の基板との間に挟持された液晶と、上記第１の基板上に形成されたゲート信号線とドレイン信号線と、上記ゲート信号線と上記ドレイン信号線とに接続された薄膜トランジスタと、上記薄膜トランジスタに接続された画素電極と、保持容量配線とを有する液晶表示装置であって、上記薄膜トランジスタと上記画素電極とに接続された半導体層と、上記保持容量配線との間で保持容量素子が形成され、上記保持容量素子は上記ドレイン信号線に沿って形成されていることを特徴とする。
また、上記保持容量素子を形成する上記半導体層と上記薄膜トランジスタのソース電極を形成する半導体層とは同一の層であることを特徴とする。
また、上記第１の基板上に上記保持容量素子を形成する上記半導体層が形成され、上記半導体層の上に上記保持容量配線が形成され、上記保持容量配線の上に上記画素電極が形成されていることを特徴とする。【手続補正３】
【補正対象書類名】明細書
【補正対象項目名】００１７
【補正方法】削除
【補正の内容】

OIPE
SEP 2 2 2004
PATENT & TRADEMARK OFFICE

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Attn: **Mail Stop Missing Parts**

Application No.: 10/852,255

Filed: May 25, 2004

Docket No.: 119570

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

RESPONSE TO NOTICE TO FILE MISSING PARTS WITH DECLARATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts of Application - Filing Date Granted (copy attached) mailed on July 22, 2004, submitted herewith is the executed Declaration of the inventor and a Power of Attorney. Any specification attached to and referenced in the Declaration is a copy of the specification and any amendments thereto which were filed in the Office in order to obtain a filing date for the application.

Attached is our Check No. 158764 for ☒ $130.00 ☐ $65.00 (entitlement to small entity status is asserted) for the fee under 37 C.F.R. §1.16(e).

Entry of these documents should complete all of the filing formalities and fully satisfy all requirements of the Notice to File Missing Parts. Accordingly, examination and allowance of this application in due course are respectfully solicited.

The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) associated with this communication to Deposit Account No. 15-0461. Two duplicate copies of this paper are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

John S. Kern
Registration No. 42,719

JAO:JSK/al

Date: September 22, 2004

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/852,255	05/25/2004	Masao Murade	119570

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

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CONFIRMATION NO. 4122

FORMALITIES LETTER

OC000000013298663

Date Mailed: 07/22/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
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09/23/2004 EFLORES 00000056 10852255
01 FC:1051 130.00 OP

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PART 1 - ATTORNEY/APPLICANT COPY

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Seiko Epson Ref. No.: J0009628US01 Attorney's Ref. No.: 119570

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。	As a below named inventor, I hereby declare that:
私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。	My residence, post office address and citizenship are as stated next to my name.
下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
電気光学装置及びこれを備えた電子機器	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME
上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、	the specification of which is attached hereto unless the following box is checked:
☒ 2004年5月25日に提出され、米国出願番号または特許協定条約 国際出願番号を 10/852,255 とし、（該当する場合） _____ に訂正されました。	☒ was filed on May 25, 2004 as United States Application Number or PCT International Application Number 10/852,255 and was amended on _____ (if applicable).
私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。	I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。	I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office. Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks. Washington, DC 20231.

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Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条（ａ）－（ｄ）項又は３６５条（ｂ）項に基き下記の、米国以外の国の少なくとも１ヶ国を指定している特許協力条約３６５条（ａ）項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
2003-156832 (Number) (番号)	Japan (Country) (国名)	02/June/2003 (Day/Month/Year Filed) (出願年月日)	☐
2004-081532 (Number) (番号)	Japan (Country) (国名)	19/March/2004 (Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条（ｅ）項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条（ｃ）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１章５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration
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委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

書類送付先：
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P.O. Box 19928
Alexandria, Virginia 22320

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Alexandria, Virginia 22320

直接電話連絡先： (名前及び電話番号)
OLIFF & BERRIDGE, PLC
(703) 836-6400

Direct Telephone Calls to: *(name and telephone number)*
OLIFF & BERRIDGE, PLC
(703) 836-6400

唯一または第一発明者名
村出 正夫

Full name of sole or first inventor
Masao MURADE

発明者の署名 日付
村出 正夫 2004年7月20日

Inventor's signature Date
Masao Murade July 20, 2004

住所
日本国, 長野県, 諏訪市

Residence
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国籍
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第二共同発明者

Full name of second joint inventor, if any

第二共同発明者の署名 日付

Second inventor's signature Date

住所
日本国, _____, _____

Residence
_____, _____, Japan

国籍

Citizenship

私書箱

Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/852,255	05/25/2004	Masao Murade	119570

CONFIRMATION NO. 4122

25944
OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

FORMALITIES LETTER

OC000000013298663

Date Mailed: 07/22/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

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PART 3 - OFFICE COPY

NONPROVISIONAL PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

Attorney Docket No.: 119570

Date: May 25, 2004

16018 U.S. PTO 10/852255 052504

MAIL STOP PATENT APPLICATION

Customer Number: 25944

NONPROVISIONAL APPLICATION TRANSMITTAL
RULE §1.53(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the nonprovisional patent application

For (Title): ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

By (Inventor): Masao MURADE

☒ Formal drawings (Figs. 1-12; 10 sheets) are attached.
☐ Use Figure _____ for front page of Publication.
☐ A Declaration and Power of Attorney is filed herewith.
☐ This application claims benefit of Provisional Application No. _____ filed _____.
(A Preliminary Amendment is attached to reflect this claim in the Specification if not already present.)
☒ This patent application is assigned to SEIKO EPSON CORPORATION.
☐ The executed Assignment is filed herewith.
☒ An Information Disclosure Statement is filed herewith.
☐ Entitlement to small entity status is hereby asserted.
☐ A Preliminary Amendment is filed herewith.
☒ Priority of foreign applications No. 2003-156832 filed June 2, 2003 in Japan and No. 2004-081532 filed March 19, 2004 in Japan is claimed (35 U.S.C. §119).
☒ A certified copy of the above corresponding foreign applications is filed herewith.
☐ This application is NOT to be published under 35 U.S.C. 122(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing.
☒ The filing fee is calculated below:

CLAIMS IN THE APPLICATION AFTER ENTRY OF ANY PRELIMINARY AMENDMENT NOTED ABOVE

FOR:	NO. FILED	NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
BASIC FEE				$ 385	OR		$ 770
TOTAL CLAIMS	16 - 20	= 0	x 9 =	$	OR	x 18	$
INDEP CLAIMS	2 - 3	= 0	x 43 =	$	OR	x 86	$
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+ 145 =	$	OR	+ 290	$
			TOTAL	$	OR	TOTAL	$ 770

* If the difference is less than zero, enter "0".

☒ Check No. 154404 in the amount of $770.00 to cover the filing fee is attached. Except as otherwise noted herein, the Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

John S. Kern
Registration No. 42,719

JAO:JSK/mxm

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

BACKGROUND OF THE INVENTION

1. Field of Invention

[0001] The present invention relates to an electro-optical device, such as a driving circuit built-in liquid crystal device, obtained by mounting peripheral driving circuits on an element substrate and an electronic apparatus including the electro-optical device.

2. Description of Related Art

[0002] In an electro-optical device, such as a liquid crystal device, a plurality of pixel portions driven for displaying images are arranged in a matrix in an image display region. Pixel electrodes and thin film transistors (TFT) for switch controlling the pixel electrodes are arranged within the pixel portions and wiring lines, such as scanning lines, data lines, and capacitance lines are provided along the gaps among the pixel electrodes adjacent to each other in vertical and horizontal directions in each pixel portion. In particular, in the case of the driving circuit built-in liquid crystal device, scanning line driving circuits and a data line driving circuit for driving the scanning lines and the data lines are mounted in a peripheral region on the same element substrate. Therefore, in general, various wiring lines, such as power source signal lines, clock signal lines, image signal lines, and control signal lines are planarly laid out in the peripheral region, which connect a plurality of external circuit connection terminals arranged along one side of the element substrate to the peripheral driving circuits.

[0003] Here, as it is desirable to miniaturize the electro-optical device or the element substrate, a technology of laying out various wiring lines planarly is provided so that various wiring lines connecting the external circuit connection terminals to the peripheral circuits are provided in the restricted peripheral region in such a way that mutual noise among the various wiring lines arranged to be close to each other is reduced. According to such an electro-optical device, it can be possible to realize high quality images by improving a driving frequency or a degree of precision while miniaturizing the device or the element substrate.

SUMMARY OF THE INVENTION

[0004] However, according to the conventional technology of providing various wiring lines in the peripheral region, a plurality of wiring lines (main wiring lines) each having one end connected to each of the plurality of external circuit connection terminals exist in the restricted peripheral region. Furthermore, the number of main wiring lines or the

number of external circuit connection terminals tends to increase as the driving method becomes complicated. Therefore, at least several main wiring lines must have the other ends intersected to other main wiring lines in order to be routed to the peripheral driving circuits or upper and lower conduction terminals. In each of the intersections, a laminated structure established on the element substrate must be provided which forms a relay wiring line portion made of another conductive film laminated on or under the conductive film that constitutes at least one main wiring line. Considering that the main wiring lines are made of the conductive film having the lowest resistance among the laminated structures established on the element substrate, such as aluminum, that the relay wiring line portions are made of another conductive film, that is, a conductive film whose resistance is not the lowest causes a technical problem in that resistance remarkably increases in the main wiring lines. Increase in the resistance in the main wiring lines easily deteriorates picture quality due to the uses of the main wiring lines.

[0005] It is very difficult to improve picture quality by reducing a pixel pitch or a wiring line pitch while miniaturizing the device by reducing the size of the peripheral region. Furthermore, when the above-mentioned relay wiring lines are provided, resistance caused by contact resistance or contact hole resistance increases and the laminated structures on the element substrate become complicated, as well as the manufacturing processes involved, which negatively impact the reliability of the device and the production yield, respectively.

[0006] Accordingly, it is an object of the invention to provide an electro-optical device capable of effectively reducing the resistance of main wiring lines and of preventing mutual interference among signals of the main wiring lines thus allowing high quality display images, and to provide an electronic apparatus comprising the electro-optical device.

[0007] The invention can provide an electro-optical device, having a plurality of pixel portions provided in an image display region on an element substrate. The device can also include in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end connected to each of the plurality of external circuit connection terminals, and peripheral driving circuits connected to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines. In addition, the plurality of main wiring lines are made of the same conductive film and are planarly laid out so as not to intersect each other in the peripheral region.

[0008] According to the electro-optical device of the invention, during the operation thereof, various electric signals, such as image signals, clock signals, inverse signals, power source signals, and control signals are supplied to the peripheral driving circuits connected to the other ends of the main wiring lines through the external circuit connection terminals and the main wiring lines each having one end connected to each of the external circuit connection terminals. Counter electrode potential is supplied to the upper and lower conduction terminals provided in the peripheral region through the external circuit connection terminals and the main wiring lines each having one end connected to each of the external circuit connection terminals. The counter electrode potential is supplied to counter electrodes provided on the counter substrate through the upper and lower conduction materials. The scanning lines and the data lines are driven by the various electric signals supplied as mentioned above by the peripheral driving circuits such as the scanning line driving circuits and the data line driving circuits so that the main wiring lines display images by a predetermined method. For example, the plurality of pixel portions may be active matrix driven.

[0009] According to the electro-optical device of the invention, in particular, the plurality of main wiring lines are made of the same conductive film and are planarly laid out in the peripheral region so as not to intersect each other. Therefore, when the conductive film having excellent conductivity is included in the laminated structures established on the element substrate to thus be used as the above-mentioned same conductive film, or when the conductive film having the most excellent conductivity among the laminated structures established on the element substrate is used as the above-mentioned same conductive film, it is possible to establish the plurality of main wiring lines as wiring lines having excellent conductivity. Also, even if the number of main wiring lines or the number of external circuit connection terminals increases as the driving method becomes complicated, since the plurality of main wiring lines are planarly laid out so as not to intersect each other, it is not necessary to provide the relay wiring portions in the intersections.

[0010] When the main wiring lines are made of the conductive film having the lowest resistance among the laminated structures established on the element substrate such as aluminum, it is possible to remarkably reduce the resistance of the main wiring lines compared with the case in which the relay wiring line portions made of another conductive film in the laminated structures, whose resistance is now higher, are used. Therefore, it is possible to effectively prevent the picture quality from deteriorating due to the increase in the

resistance of the main wiring lines. In other words, it is possible to improve the picture quality by reducing the pixel pitch or the wiring line pitch while miniaturizing the device by reducing the size of the peripheral region.

[0011] Also, since it is not necessary to provide the relay wiring line portions in the main wiring lines as mentioned above, it is possible to prevent the resistance from increasing due to the contact resistance or the contact hole resistance in the main wiring lines, and it is possible to simplify the laminated structures on the element substrate and the manufacturing processes. Therefore, it is possible to improve the reliability and the production yield of the device. Furthermore, it is possible to remarkably reduce the mutual interference between the two kinds of electric signals carried by the two main wiring lines, which occurs when the two main wiring lines intersect each other through a thin interlayer insulating film, by planarly laying out the plurality of main wiring lines so as not to intersect each other.

[0012] According to the electro-optical device of the invention, it can be possible to effectively reduce the resistance of the main wiring lines and to prevent mutual interference among the signals of the main wiring lines. As a result, it is possible to display high quality images.

[0013] According to an aspect of the electro-optical device of the invention, sub-wiring lines can include at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines are made of a conductive film different from the same conductive film and is planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof are formed of the same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

[0014] According to this aspect, sub-wiring lines such as the internal wiring lines, extending wiring lines, and branch wiring lines can be provided in the peripheral region. Among them, the internal wiring lines of the peripheral driving circuits connect the plurality of arranged circuits that constitute a shift register in the peripheral driving circuits to each other.

[0015] The extending wiring lines extend the scanning lines, the data lines, and the capacitance lines from the image display region to the peripheral region. The branch wiring

lines supply various electric signals commonly used in the plurality of peripheral driving circuits, such as the power source signals and the clock signals.

[0016] In the sub-wiring lines, in the above-mentioned first portion, second and third film layers are laminated onto a conductive film having the most excellent conductivity separated by an interlayer insulating film. The sub-wiring lines are planarly laid out so as to intersect the main wiring lines. Also, the second portion is made of the conductive film having the excellent conductivity like the main wiring line, and is planarly laid out so as not to intersect the main wiring lines. Therefore, it is possible to improve the conductivity of the sub-wiring lines as long as the sub-wiring lines do not conflict with the main wiring lines.

[0017] According to this aspect, the first portion and the second portion of the sub-wiring lines are electrically connected to each other through contact holes formed in the interlayer insulating film.

[0018] According to this structure, the sub-wiring lines may function as one wiring line composed of the first portion and the second portion that extend in a state of intersecting each other through contact holes so as to avoid the main wiring lines. Alternatively, it is possible to connect the first portion to the second portion by methods other than the method of using the contact hole.

[0019] According to another aspect of the electro-optical device of the invention, the electro-optical device further can further include a counter electrode provided in the peripheral region on a counter substrate arranged to face the element substrate, and upper and lower conduction terminals provided in the peripheral region on the element substrate, in order to connect a counter electrode potential line for supplying counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, and the counter electrode, the counter electrode potential line of the plurality of main wiring lines is positioned near the edges of the element substrate in the peripheral region, and the peripheral driving circuits are positioned nearer the center of the element substrate than both the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.

[0020] According to this aspect, during operation, the counter electrode potential is supplied to the upper and lower conduction terminals provided in the peripheral region through the external circuit connection terminals and the main wiring lines each having one end connected to each of the external circuit connection terminals. The counter electrode potential is supplied to the counter electrodes provided on the counter substrate through the

upper and lower conduction materials mounted on the upper and lower conduction terminals. Therefore, vertical electric fields are generated between the counter electrodes and the pixel electrodes provided in the pixel portions to thus drive an electro-optical material such as a liquid crystal interposed between the two substrates. In particular, in the peripheral region, the counter electrode potential lines are positioned near the edges of the element substrate among the plurality of main wiring lines. For example, the counter electrode potential lines extend along the edges of the element substrate from the external connection terminals. Since the peripheral driving circuits are positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines, it is possible to simply obtain a plane layout in which the main wiring lines excluding the counter electrode potential lines do not intersect the counter electrode potential lines.

[0021] Preferably, the counter electrode potential line of the plurality of main wiring lines is positioned near the edges of the element substrate in the peripheral region. Therefore, it is possible to simply obtain the plane layout in which all of the main wiring lines excluding the counter electrode potential lines do not intersect the counter electrode potential lines.

[0022] According to this aspect, the plurality of external circuit connection terminals may be arranged along one side of the element substrate, and the external circuit connection terminal of the plurality of the external circuit connection terminals, which is connected to one end of the counter electrode potential line, may be positioned near the end of an array of the plurality of external circuit connection terminals. According to this structure, in the peripheral region, the counter electrode potential lines extend from the external circuit connection terminals near the edges and are thus routed near the edges of the element substrate. Therefore, it is possible to simply obtain a plane layout in which the main wiring lines excluding the counter electrode potential lines do not intersect the counter electrode potential lines.

[0023] In addition, the external circuit connection terminal, which is connected to one end of the counter electrode potential line, is positioned at the end in the arrangement of the plurality of external circuit connection terminals in the peripheral region. For example, near the position in which the plurality of external circuit connection terminals are arranged, the tips of the counter electrode potential lines that extend along the right edge of the element substrate are connected to the rightmost external circuit connection terminal and the tips of the counter electrode potential line that extends along the left edge of the element substrate are connected to the leftmost external circuit connection terminal. Therefore, in the

peripheral region near the external circuit connection terminals, it is possible to simply obtain the plane layout in which all of the main wiring lines excluding the counter electrode potential lines do not intersect the counter electrode potential lines.

[0024] According to another aspect of the electro-optical device of the invention, the electro-optical device further includes a counter electrode provided in the peripheral region on a counter substrate arranged to face the element substrate, and upper and lower conduction terminals provided in the peripheral region on the element substrate, in order to connect a counter electrode potential line for supplying counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, and the counter electrode. Also, the counter electrode potential line can be positioned nearer the edges of the element substrate than the one or plurality of main wiring lines excluding the counter electrode potential lines and nearer the center of the element substrate than the other or plurality of main wiring lines excluding the counter electrode potential line in the peripheral region, a part of the peripheral driving circuits is partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits are partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

[0025] According to this aspect, during operation, the counter electrode potential can be supplied to the upper and lower conduction terminals provided in the peripheral region through the external circuit connection terminals and the main wiring lines each having one end connected to each of the external circuit connection terminals. The counter electrode potential is supplied to the counter electrodes provided in the counter substrate through the upper and lower conduction materials. In particular, in the peripheral region, the counter electrode potential lines are positioned nearer the edges of the element substrate than the one or plurality of main wiring lines excluding the counter electrode potential lines. On the other hand, in the peripheral region, the counter electrode potential lines are positioned nearer the center of the element substrate than the other or plurality of main wiring lines excluding the counter electrode potential lines. Therefore, it is possible to simply obtain the plane layout in which the main wiring lines excluding the counter electrode potential lines do not intersect the counter electrode potential lines.

[0026] According to this aspect, the plurality of external circuit connection terminals may be arranged along one side of the element substrate, and the external circuit

connection terminal of the plurality of external circuit connection terminals, which is connected to the one end of one or plurality of main wiring lines excluding the counter electrode potential lines, may be positioned near the end of an array of the plurality of external circuit connection terminals.

[0027] According to this structure, in the peripheral region, the other one or plurality of main wiring lines excluding the counter electrode potential lines extend from the external circuit connection terminals near the edges and thus are routed near the edges of the element substrate. On the other hand, the one or plurality of main wiring lines excluding the counter electrode potential lines extend from the external circuit connection terminals near the center and thus are routed near the center of the element substrate. Therefore, it is possible to simply obtain the plane layout in which the main wiring lines excluding the counter electrode potential lines do not intersect the counter electrode potential lines.

[0028] According to various aspects having the above-mentioned counter electrodes, the plurality of main wiring lines may include a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

[0029] According to the above structure, since the clock signal lines and the counter electrode potential lines which remarkable mutual interference occurs if they intersect each other do not intersect each other, it is possible to effectively prevent the electric potential of the clock signals from changing in accordance with the changes in the counter electrode potential or to prevent the counter electrode potential from changing in accordance with the changes in the electric potential of the clock signals. Therefore, it is possible to display high quality images.

[0030] According to another aspect of the electro-optical device of the invention, the plurality of main wiring lines can include a pair of clock signal lines for supplying a clock signal and an inverse signal thereof as electric signals and power source wiring lines for supplying power source signals as electric signals and the pair of signal lines and power source wiring lines do not intersect each other. According to this aspect, since the clock signal lines and the power source wiring lines therebetween which remarkable mutual interference occurs if they intersect each other do not intersect each other, it is possible to effectively prevent the electric potential of the clock signals from changing in accordance with the changes in the electric potential of the power source signals or to prevent the electric

potential of the power source signals from changing in accordance with the changes in the electric potential of the clock signals. Therefore, it is possible to display high quality images.

[0031] According to another aspect of the electro-optical device of the invention, the plurality of main wiring lines are planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other. According to this aspect, the main wiring lines travel in zigzags so as to prevent the main lines from intersecting each other although the length of the main wiring lines increases. It is possible to reduce the resistance of the wiring line to offset the increased length of the wiring line by reducing the resistance of the same conductive film that constitutes the main wiring lines and to obtain advantages by not using relay wiring lines required for the intersections among the main wiring lines.

[0032] Also, according to this aspect, the main wiring lines are preferably planarly laid out so that the number of intersections is mathematically or geometrically minimal and are preferably arranged to reduce the number of intersections in spite of being in zigzags. On the other hand, it can be possible to lay out the main wiring lines and the sub-wiring lines in the peripheral region in plan view while increasing the wiring line pitch and preventing the main wiring lines from intersecting each other by allowing the above-mentioned sub-wiring lines to intersect each other.

[0033] According to another aspect of the electro-optical device of the invention, the plurality of main wiring lines can include at least partially redundant wiring lines composed of a different conductive film formed in a layer different from the same conductive film. According to this aspect, since the main wiring lines include the redundant wiring lines composed of other conductive films formed in other layers as well as the wiring line portions composed of the same conductive film, it is possible to reduce the resistance of the main wiring lines. Furthermore, even if one of the two wiring line portions that constitute the redundant structure is short-circuited, the redundant wiring line may function as a wiring line. Therefore, it is possible to improve the reliability of the electro-optical device.

[0034] In addition, an electro-optical device according to the invention can include a plurality of pixel portions provided in an image display region on an element substrate, a plurality of external circuit connection terminals provided in a peripheral region of the image display region on the element substrate, scanning line driving circuits, a data line driving circuit, scanning line driving circuit wiring lines each having one end connected to each of the external circuit connection terminals and having the other ends connected to the scanning line driving circuits, data line driving circuit wiring lines each having one end connected to each

of the external circuit connection terminals and having the other ends connected to the data line driving circuit, and image signal wiring lines each having one end connected to each of the external circuit connection terminals, the image signal wiring lines supplying image signals of the plurality of pixel portions. Also, the scanning line driving circuit wiring lines, the data line driving circuit wiring lines, and the image signal wiring lines are planarly laid out so as not to intersect each other in the peripheral region.

[0035] According to an aspect of the electro-optical device of the invention, the image signal wiring lines can be arranged between the scanning line driving circuit wiring lines and the data line driving circuit wiring lines.

[0036] According to another aspect of the electro-optical device of the invention, the electro-optical device can further include a counter electrode provided in the peripheral region on the counter substrate arranged to face the element substrate, and a counter electrode potential line having one end connected to the external circuit connection terminals and having the other end for supplying counter potential to the counter electrode, and the counter electrode potential line may be arranged so as to surround the scanning line driving circuit wiring lines.

[0037] An electronic apparatus according to the invention can include the electro-optical device according to the above-mentioned invention (including various aspects).

[0038] Since the electronic apparatus according to the invention includes the above-mentioned electro-optical device according to the invention, it is possible to realize various electronic apparatuses, such as television sets, mobile telephones, electronic organizers, word processors, view finder type or monitor direct view type video tape recorders, work stations, picture telephones, POS terminals, and touch panels capable of displaying high quality images since various electric signals are appropriately supplied by the main wiring lines. Also, it is possible to realize electrophoresis devices, such as electronic papers as the electronic apparatus according to the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] The invention will be described with reference to the accompanying drawings, wherein the numerals reference like elements, and wherein:

[0040] Fig. 1 is a plan view illustrating the entire structure of an electro-optical device according to an embodiment of the present invention;

[0041] Fig. 2 is a sectional view taken along the line H-H' of Fig. 1;

[0042] Fig. 3 is an equivalent circuit diagram illustrating various elements and wiring lines in a plurality of pixels formed in a matrix, which constitute the image display region of the electro-optical device;

[0043] Fig. 4 is an equivalent circuit diagram illustrating the structures of various driving circuits and various signal wiring lines formed on a TFT array substrate;

[0044] Fig. 5 is an equivalent circuit diagram illustrating the structures of various driving circuits and various signal wiring lines formed on a TFT array substrate;

[0045] Fig. 6 is a plan view of a plurality of pixel groups adjacent to each other on the TFT array substrate on which data lines, scanning lines, and pixel electrodes are formed in the electro-optical device according to the embodiment of the present invention;

[0046] Fig. 7 is a sectional view taken along the line A-A' of Fig. 6;

[0047] Fig. 8 is a sectional view taken along the line B-B' of Fig. 4 or 5;

[0048] Fig. 9 is a sectional view taken along the line C-C' of Fig. 4 or 5;

[0049] Fig. 10 is a sectional view of main wiring lines and redundant wiring lines according to a modified embodiment of the present invention;

[0050] Fig. 11 is another sectional view of the main wiring lines and the redundant wiring lines according to the modified embodiment of the present invention; and

[0051] Fig. 12 is a schematic sectional view illustrating a color liquid crystal projector according to an example of a projection color display device according to an embodiment of an electronic apparatus according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0052] The effects and other advantages of the invention will become apparent from the following preferred embodiments of the invention.

[0053] Hereinafter, the embodiments of the invention will now be described with reference to the drawings. According to the following embodiments, an electro-optical device according to the invention is applied to a TFT active matrix driving liquid crystal device.

[0054] The entire structure of the electro-optical device according to the present embodiment will now be described with reference to Figs. 1 and 2. Here, Fig. 1 is a plan view illustrating the entire structure of the electro-optical device according to the present embodiment. Fig. 2 is a sectional view taken along the line H-H' of Fig. 1. Here, a driving circuit built-in TFT active matrix driving liquid crystal device that is an example of an electro-optical device is taken as an example.

[0055] In Figs. 1 and 2, in the electro-optical device according to the present embodiment, a TFT array substrate 10 and a counter substrate 20 are arranged to face each other. A liquid crystal layer 50 is sealed between the TFT array substrate 10 and the counter substrate 20. The TFT array substrate 10 and the counter substrate 20 are attached to each other by a seal material 52 provided in a seal region 52a positioned around an image display region 10a.

[0056] The seal material 52 is made of a photocurable resin and a thermosetting resin for attaching the two substrates to each other. After coating the TFT array substrate 10 with the seal material 52 during the manufacturing process, the seal material 52 is hardened by radiating ultraviolet rays onto the same and heating the same. Also, in the seal material 52, gap materials, such as glass fibers or glass beads, for setting the distance (the gap between the substrates) between the TFT array substrate 10 and the counter substrate 20 as a predetermined value are dispersed. Instead of or in addition to dispersing the gap materials in the seal material 52, in particular, in the case of a large electro-optical device, the gap materials may be dispersed in the liquid crystal layer 50.

[0057] In parallel to the inside of the seal region 52a where the seal material 52 is arranged, a frame light-shielding film 53 having a light-shielding property, that defines the frame region of the image display region 10a is provided on the side of the counter substrate 20. However, a part or all of the frame light-shielding film 53 may be provided as a built-in light-shielding film on the side of the TFT array substrate 10.

[0058] According to the present embodiment, a peripheral region can be defined around the image display region 10a. That is, as viewed from the center of the TFT array substrate 10, the portion positioned nearer the edge than the frame light-shielding film 53 is defined as the peripheral region.

[0059] In the peripheral region, the region positioned outside the seal region 52a can include a data line driving circuit 101 and external circuit connection terminals 102, which are provided along one side (that is, the lower side in Fig. 1) of the TFT array substrate 10. Scanning line driving circuits 104 are provided along two sides (that is, the left and right sides in Fig. 1) adjacent to the one side so as to be covered with the frame light-shielding film 53. Also, in order to connect with each other the two scanning line driving circuits 104 provided on both sides of the image display region 10a, along the remaining one side (that is, the upper side in Fig. 1) of the TFT array substrate 10, a plurality of wiring lines 105 are provided so as to be covered with the frame light-shielding film 53.

[0060] According to the present embodiment, in particular, a plurality of main wiring lines 108 each having one end connected to each of the external circuit connection terminals 102 are provided in the peripheral region. The other ends of the main wiring lines 108 are connected to the data line driving circuit 101 and the scanning line driving circuits 104. Also, the structures and the operations of the circuits on the TFT array substrate 10 and a plane layout of the main wiring lines 108 will now be described in detail.

[0061] In Fig. 2, on the TFT array substrate 10, an alignment film can be formed on a pixel electrode 9a after wiring lines such as pixel switching TFTs, scanning lines, and data lines are formed. On the other hand, a light-shielding film 23 in a matrix or in stripes is formed on the counter substrate 20 excluding a counter electrode 21, followed by a topmost layer of alignment film. Also, the liquid crystal layer 50 is made of liquid crystal obtained by mixing one kind or various kinds of nematic liquid crystal with each other and is in a predetermined alignment state between the pair of alignment films.

[0062] In Fig. 1, upper and lower conduction terminals 106t connected to one counter electrode potential line which is one of the main wiring lines 108 planarly laid out on the TFT array substrate 10 are provided in the vicinity of the four corners of the TFT array substrate 10. The upper and lower conduction materials 106 are arranged on the upper and lower conduction terminals 106t. The upper and lower conduction materials 106 contact the four corners of the counter electrode 21 and supply the counter electrode potential from the external circuit connection terminals 102 through the main wiring lines 108 to the counter electrode 21.

[0063] Next, the structure of the pixel portion of the electro-optical device according to the embodiment of the invention will now be described with reference to Fig. 3. Here, Fig. 3 is an equivalent circuit diagram illustrating various elements and wiring lines in a plurality of pixels formed in a matrix, which constitute the image display region of the electro-optical device.

[0064] In Fig. 3, pixel electrodes 9a and TFTs 30 for switch controlling the pixel electrodes 9a are provided in the plurality of pixel portions formed in a matrix in the image display region 10a (refer to Fig. 1) of the electro-optical device according to the present embodiment, respectively. Data lines 6a to which image signals S1, S2, ···, and Sn (to be described in greater detail below) are supplied are electrically connected to the sources of the TFTs 30.

[0065] In addition, the scanning lines 3a are electrically connected to the gates of the TFTs 30 so as to apply linearly and sequentially scanning signals G1, G2, ···, and Gm to the scanning lines 3a in pulse at a predetermined timing. The pixel electrodes 9a are electrically connected to the drains of the TFTs 30 so as to write the image signals S1, S2, ···, and Sn supplied from the data lines 6a at a predetermined timing by switching off the switches of the TFTs 30 that are switching elements for only a predetermined period of time.

[0066] The image signals S1, S2, ···, Sn of a predetermined level, which are written in the liquid crystal as an example of an electro-optical material through the pixel electrodes 9a are held between the pixel electrodes and the counter electrodes 21 formed on the counter substrate for a predetermined period. In the liquid crystal, the alignment or the order of molecular association changes in accordance with the level of an applied voltage, thereby being able to modulate light and to display gray scales. In case of a normally white mode, the transmittance ratio of incident light decreases in accordance with the voltage applied in each pixel unit, while in case of a normally black mode, the transmittance ratio of incident light increases in accordance with the voltage applied to each pixel unit. Therefore, light having contrast in proportion to the image signals emits from the electro-optical device as a whole.

[0067] Here, in order to prevent the held image signals from leaking, storage capacitors 70 are additionally provided in parallel to the liquid crystal capacitors formed between the pixel electrodes 9a and the counter electrodes 21 (refer to Figs. 1 and 2). The storage capacitors 70 are provided in parallel to the scanning lines 3a and include capacitance electrodes having a fixed electric potential and capacitance lines 300 having a predetermined electric potential. The storage capacitors 70 improve the charge holding characteristics of the pixel electrodes. Also, the electric potential of the capacitance lines 300 may be always fixed to one voltage value or may be fixed to a plurality of voltage values while fluctuating over a predetermined period.

[0068] Subsequently, the structures of the circuits and the plane layout of the main wiring lines on the TFT array substrate of the electro-optical device according to the present embodiment will now be described with reference to Figs. 4 and 5. Here, Fig. 4 is an equivalent circuit diagram illustrating the structures of various driving circuits and various signal wiring lines formed on the TFT array substrate. Fig. 5 is an equivalent circuit diagram illustrating the structures of various driving circuits and various signal wiring lines, in which Fig. 4 is described in greater detail. Also, hereinafter, signal names and signal wiring lines input to the TFT array substrate 10 through the external circuit connection terminals 102 are

referred to by an abbreviation representing the signals and adding the letter L to represent the line carrying that signal. That is, for example, the signal wiring line of a "clock signal CLX" being a signal name is referred to as a "clock signal line LCLX".

[0069] As illustrated in Figs. 4 and 5, the data line driving circuit 101 and sampling circuits 301, can supply image signals to the data lines 6a, and the scanning line driving circuits 104, can supply scanning signals to the scanning lines 3a are formed as driving circuits of the electro-optical device on the TFT array substrate 10. Also, the external circuit connection terminals 102 including a plurality of terminals for inputting various signals supplied to the driving circuits from external control circuits are formed along one side of the TFT array substrate 10 (refer to Fig. 1). The main wiring lines 108 are provided from the external circuit connection terminals 102.

[0070] The data line driving circuit 101 includes a shift register circuit 101a, a waveform selection circuit 101b, and a buffer circuit 101c as main components. The shift register circuit 101a starts a transferring operation in accordance with a start signal SPX supplied from the external control circuits using a negative power source VSSX and a positive power source VDDX supplied from the external control circuits through the external circuit connection terminals 102 and a wiring line LVSSX and a wiring line LVDDX of the main wiring lines 108 as power sources. Next, transfer signals are sequentially output to the waveform selection circuit 101b at a predetermined timing based on a clock signal CLX and an antiphase clock signal CLX_{INV} for the shift register circuit 101a, which are supplied through the external circuit connection terminals 102 and a clock signal line LCLX and an antiphase clock signal line $LCLX_{INV}$ of the main wiring lines 108.

[0071] The waveform selection circuit 101b referred to as an enable circuit restricts the pulse widths of the transfer signals sequentially output from the shift register circuit 101a to the pulse widths of enable signals ENB1 to ENB4 input from the external control circuits through the external circuit connection terminals 102 to thus define the respective sampling periods in the following sampling circuits 301. More specifically, the waveform selection circuit 101b is provided corresponding to each stage of the above-mentioned shift register circuit 101a. For example, the selection of a waveform in a temporal axis is controlled so that data lines 6a are driven only when the transfer signals formed by a NAND circuit and an inverter, then sequentially output from the shift register circuit 101a are at a high level and any one of the enable signals ENB1 to ENB4 is at a high level.

[0072] The buffer circuit 101c buffers the transfer signal whose waveform is selected and supplies the transfer signal as a sampling circuit driving signal to the sampling circuits 301 through sampling circuit driving signal lines 114. The buffer circuit 101c also may perform signal processings such as a level shift processing and an inverting processing.

[0073] The sampling circuits 301 include a plurality of TFTs 202 that is an example of switching circuit elements for sampling the image signals. However, as shown in the drawing, first conductive channel TFTs, n-channel TFTs, or p-channel TFTs may be used as the switching circuit elements. Also, complementary TFTs may be also used as the switching circuit elements. The lower ends of the data lines 6a in Fig. 3 are connected to the drains of the TFTs 202. Image signal lines 115 are connected to the sources of the TFTs 202 through extending wiring lines 116. At the same time, the sampling circuit driving signal lines 114 connected to the data line driving circuit 101 are connected to the gates of the TFTs 202. Image signals VID1 to VID6 on the image signal lines 115 are sampled by the sampling circuits 301 as the sampling circuit driving signals are supplied from the data line driving circuit 101 through the sampling circuit driving signal lines 114 and are supplied to the respective data lines 6a.

[0074] The image signals S1, S2, ···, and Sn supplied from the external circuit connection terminals 102 through the main wiring lines 108 and written in the data lines 6a by the sampling circuits 301 as mentioned above may be linearly and sequentially supplied in this order. However, according to the present embodiment, each of the image signals S1, S2, ···, and Sn is supplied to each set composed of six data lines 6a corresponding to the image signals VID1 to VID6 serial-parallel developed into six phases. The number of phases is not restricted to six phases. For example, image signals developed into nine, twelve, or twenty-four phases may be supplied to each set of data lines 6a whose number corresponds to the number of developed phases.

[0075] The scanning line driving circuits 104 include the shift register circuits and the buffer circuits as components and start a transfer operation to the built-in shift register circuits in accordance with a start signal SPY supplied from the external control circuits using the negative power source VSSY and the positive power source VDDY supplied from the external control circuits through the external circuit connection terminals 102 and the wiring line LVSSY and the wiring line LVDDY of the main wiring lines 108 as power sources. Subsequently, the scanning line driving circuits 104 linearly and sequentially apply the scanning signals to the above-mentioned scanning lines 3a in pulse at a predetermined timing

based on the clock signal CLY and the antiphase clock signal CLY_{INV} for the built-in shift register circuits, which are supplied through the external circuit connection terminals 102 and the clock signal line LCLY and the antiphase clock signal line $LCLY_{INV}$ of the main wiring lines 108.

[0076] On the TFT array substrate 10, counter electrode potential line LLCCOM which is one of the main wiring lines 108 passes through the four corners of the TFT array substrate 10 while being connected to the upper and lower conduction terminals 106t. A predetermined electric potential is supplied to the counter electrodes 21 through the upper and lower conduction materials 106, the upper and lower conduction terminals 106t, and the counter electrode potential line LLCCOM. It is possible to drive the liquid crystal interposed between the two electrodes, that is, the pixel electrode 9a and the counter electrode 21 as mentioned above by supplying the electric potential.

[0077] According to the present embodiment, in particular, the scanning line driving circuits 104 are arranged further inside than the seal region 52a illustrated in Fig. 1. That is, in Figs. 4 and 5, the scanning line driving circuits 104 are arranged to be closer to the center of the TFT array substrate 10 than the counter electrode potential lines LLCCOM provided along the edges of the TFT array substrate 10 so as to pass through the four upper and lower conduction terminals 106t and to surround the image display region 10a and various driving circuits. Therefore, compared with the case in which the scanning line driving circuits 104 are arranged outside the seal region 52a in the peripheral region, it is possible to reduce the space of the peripheral region in the TFT array substrate 10 and to miniaturize the entire device. Furthermore, it is possible to lay out the group of the plurality of main wiring lines 108a including the counter electrode potential lines LLCCOM and the various signal wiring lines that reach the scanning line driving circuits 104 and the group of the plurality of main wiring lines 108b including the various signal wiring lines that reach the data line driving circuit 101 in plan view without intersecting each other. Also, it is possible to lay out the group of the main wiring lines 108a that reach the scanning line driving circuits 104 in plan view without intersecting each other. Also, it is possible to lay out the group of the main wiring lines 108b that reach the data line driving circuit 101 in plan view without intersecting each other excluding intersecting portions required for being connected to the shift register 101a, the waveform selection circuit 101b, and the buffer circuit 101c. Also, it is possible to lay out the main wiring lines 108c that reach the sampling circuits 301, that is, image signal lines 115, without intersecting each other, excluding the intersecting portions required to intersect in order to be connected to the sampling circuits 301.

[0078] Next, with reference to Figs. 4 and 5, the detailed structures of the external circuit connection terminals 102 and the various signal wiring lines connected to the external circuit connection terminals 102 will now be described. Also, hereinafter, the external circuit connection terminals of the signals input to the TFT array substrate 10 are referred to by an abbreviation representing the signals and adding the letter T to represent the terminal carrying the signal. That is, for example, the connection terminal of a "clock signal CLX" is referred to as a clock signal "terminal TCLX".

[0079] As mentioned above, the external circuit connection terminals 102 provided along one side of the TFT array substrate 10 are composed of a plurality of groups of terminals divided into four groups, one each for the counter electrode potential lines, the scanning line driving circuits, the image signals, and the data line driving circuit. More specifically, the external circuit connection terminals 102 include two terminals TLCCOM for the counter electrode potential lines LLCCOM, a terminal TSPY, a terminal TVSSY, a terminal TVDDY, a terminal TCLX, and a terminal $TCLX_{INV}$ for the scanning line driving circuits 104, terminals TVID1 to TVID6 for the image signals VID1 to VID6, and a terminal TVSSX, a terminal TSPX, a terminal TVDDX, a terminal TCLX, a terminal $TCLX_{INV}$, terminals TENB1 to TENB4, and a terminal TVSSX for the data line driving circuit 101.

[0080] According to the present embodiment, in particular, as illustrated in Figs. 4 and 5, the two terminals TLCCOM for supplying a counter electrode potential LCCOM of the external circuit connection terminals 102 are arranged one on each end, that is, the right end and the left end. The counter electrode potential lines LLCCOM, each of whose ends are connected to one of the two terminals TLCCOM, are connected to the four upper and lower conduction terminals 106t as mentioned above so as to surround the outer circumference of the seal region 52. Alternatively, only one upper and lower conduction terminal 106t may exist.

[0081] Next, the terminal TCLY, the terminal $TCLY_{INV}$, the terminal TVDDY, and the terminal TSPY for driving the scanning line driving circuits 104 are arranged in parallel after the rightmost TLCCOM terminal in this order. On the other hand, the terminal TSPY and the terminal TVSSY for driving the scanning line driving circuits 104 are arranged in parallel in this order after the leftmost TLCCOM terminal when ordered from left to right.

[0082] Since the terminals TLCCOM for the counter electrode potential lines and the groups of terminals for the scanning line driving circuits 104 are arranged as mentioned above, it is possible to arrange the plurality of main wiring lines 108a connected to the groups

of terminals for the scanning line driving circuits 104, that is, the plurality of signal wiring lines for driving the scanning line driving circuits 104, further inside (that is, closer to the center of the TFT array substrate 10) than the counter electrode potential lines LLCCOM connected to the terminals TLCCOM. As illustrated in Fig. 5, the clock signal line LCLY, the antiphase clock signal line $LCLY_{INV}$, and the wiring line LVDDY that is an electrostatic potential line are arranged outside the right scanning line driving circuit 104 and the left scanning line driving circuit 104 and inside the counter electrode potential lines LLCCOM so as to be electrically connected to the right and left scanning line driving circuits 104 rather than the right scanning line driving circuit 104 in the drawing. That is, according to the present embodiment, when the scanning line driving circuits 104 are arranged further inside than the seal region 52a, the counter electrode potential lines LLCCOM and the groups of the signal wiring lines for driving the above-mentioned scanning line driving circuits 104 do not intersect on the substrate. Therefore, the counter electrode potential lines LLCCOM and the group of the signal wiring lines 108a for driving the scanning line driving circuits 104 may be formed on the same wiring line layers and be formed simultaneously in the manufacturing processes.

[0083] When the counter electrode potential lines LLCCOM and the group of the signal wiring lines for the scanning line driving circuits 104 are formed of separate wiring line layers with an interlayer insulating film interposed so as to intersect each other in plan view, in particular, the counter electrode potential lines LLCCOM and the group of the signal wiring lines for the scanning line driving circuits 104 may interfere with each other by the noise of the signals generated from the respective signal wiring lines in the intersections. Therefore, as mentioned above, according to the present embodiment, since the counter electrode potential lines LLCCOM and the group of the signal wiring lines for the scanning line driving circuits 104 are formed of the same wiring line layers without intersecting each other in plan view, it is possible to prevent such a problem.

[0084] Furthermore, when the terminals TLCCOM that are the external circuit connection terminals 102 for supplying the counter electrode potential LCCOM and the group of terminals for driving the scanning line driving circuits 104 are arranged to establish a position relationship contrary to that illustrated in Fig. 4 or Fig. 5, that is, when the terminals TLCCOM are closer to the center, it is necessary to intersect the wiring lines connected to the respective terminals on the substrate and to thus adopt a means of connecting any one main wiring line 108 to another wiring line layer. In this case, since the separate wiring line layers are connected to each other through contact holes formed in the interlayer insulating film, the

manufacturing processes become complicated and, in particular, the resistance of the wiring lines increase in the portions where the wiring line layers are connected to each other. Therefore, it is possible to easily form the counter electrode potential lines LLCCOM and the plurality of main wiring lines 108a for driving the scanning line driving circuits 104 during the manufacturing processes and to appropriately prevent signals from being delayed due to the resistance of the wiring lines by adopting the arrangement of the external circuit connection terminals 102 illustrated in Figs. 4 and 5 according to the present embodiment, that is, by arranging the terminals TLCCOM closer to the end.

[0085] Also, when the scanning line driving circuits 104 are formed further outside than the seal region 52a, the terminals TLCCOM for supplying the counter electrode potential and the group of terminals for the scanning line driving circuits 104 are preferably arranged to establish a position relationship contrary to that of the above-mentioned example so that they do not intersect each other on the substrate. By doing so, as mentioned above, it is possible to prevent the main wiring lines 108 from intersecting each other on the substrate and to prevent the resistance of the wiring lines from increasing since none of the main wiring lines 108 is connected to another wiring line layer.

[0086] Here, according to the present embodiment, the counter electrode potential lines LLCCOM and the respective main wiring lines 108a for driving the scanning line driving circuits 104 are preferably made of a metal film or an alloy film of low resistance such as aluminum. By doing so, it is possible to reduce the time constant of the signal wiring lines and to thus prevent signals from being delayed due to the surrounding of the wiring lines. In addition, when the main wiring lines 108a are made of the metal film or the alloy film of the low resistance, the plurality of main wiring lines 108 including the counter electrode potential lines LLCCOM can be routed in zigzags so as not to intersect each other. That is, since the wiring lines travel in zigzags, the length of the wiring lines increase, thus increasing the resistance of the wiring lines. However, since the counter electrode potential lines LLCCOM and the main wiring lines 108a are made of the metal film or the alloy film of low resistance, it is possible to offset the disadvantages of increased length from being routed in zigzags. To the contrary, since it is possible to prevent the main wiring lines 108 from intersecting each other by routing the main wiring lines 108 in zigzags, it is possible to lay out more main wiring lines 108 in plan view in the restricted peripheral region.

[0087] Also, in the external circuit connection terminals 102, terminals TVID1 to TVID6 for the image signals, a terminal TVSSX, a terminal TSPX, a terminal TVDDX, a

terminal TCLX, a terminal $TCLX_{INV}$, terminals TENB1 to TENB4, and a terminal TVSSX for the data line driving circuit 101 are arranged in parallel in this order after the terminal TSPY and the terminal TVSSY for the scanning line driving circuits 104, when ordered from left to right.

[0088] Here, the six image signal lines 115 that are the main wiring lines 108c connected to the terminals TVID1 to TVID6 reach the region between the sampling circuits 301 and the data line driving circuit 101 without intersecting each other on the substrate and without intersecting any other signal wiring lines connected to the external circuit connection terminals 102 on the substrate. To be specific, the image signal lines 115 are arranged between the wiring line LVSSY of the main wiring lines 108a for driving the scanning line driving circuits 104 and the wiring line LVSSX of the main wiring lines 108b for driving the data line driving circuit 101. In order to be electrically connected to the sampling circuits 301, the image signal lines 115 are connected to the extending wiring lines 116 through the contact holes (not shown). The extending wiring lines 116 are arranged so as to intersect the other image signal lines 115.

[0089] Also, the plurality of main wiring lines 108b connected to the respective terminals for the data line driving circuit, that is, the wiring line LVSSX that is an electrostatic potential line and the wiring line LVDDX that is an electrostatic wiring line, a start signal line LSPX, the clock signal line LCLX, and the antiphase clock signal line $LCLX_{INV}$, and the enable signal lines LENB1 to LENB4 are arranged so as to reach the data line driving circuit 101 without intersecting each other on the substrate and without intersecting any other main wiring lines 108 connected to the external circuit connection terminals 102 on the substrate. To be specific, the wiring line LVSSX is arranged so as to surround the data line driving circuit 101 inside the main wiring lines 108a and the main wiring lines 108c. The start signal line LSPX, the clock signal line LCLX, the antiphase clock signal line $LCLX_{INV}$, and the enable signal lines LENB1 to LENB4 that are the other main wiring lines 108b are arranged inside the wiring line LVSSX and are connected to the extending wiring lines through the contact holes so as to be electrically connected to the shift register 101a, the waveform selection circuit 101b, and the buffer circuit 101c of the data line driving circuit 101. The extending wiring lines are arranged so as to intersect the other main wiring lines 108b.

[0090] Since the external circuit connection terminals 102 are arranged as mentioned above, according to the present embodiment, the plurality of main wiring lines 108

connected to the respective terminals are arranged without intersecting each other on the substrate. Therefore, all of the main wiring lines 108 connected to the external circuit connection terminals 102 can be formed on the same wiring line layers and be formed simultaneously in the manufacturing processes. As a result, it is possible to simplify the manufacturing processes. Furthermore, as mentioned above, it is possible to prevent the main wiring lines 108 that intersect each other from interfering with each other at intersection point and to prevent the signals from being delayed due to the contact resistance or the wiring line resistance generated in the contact holes during the arrangement of the wiring lines.

[0091] According to the present embodiment, the terminals TVID1 to TVID6 for the image signals are preferably arranged so that both ends of each of the terminals TVID1 to TVID6 are inserted into the terminals for the electrostatic potential lines or the signal wiring lines that belong to a low frequency control signal, and that the terminals TVID1 to TVID6 are separated from the terminals for the signal wiring lines that belong to a high frequency control signal as far as possible. To be more specific, as illustrated in Fig. 4 or 5, the terminals TVID1 to TVID6 for the image signals are arranged so as to be inserted into the terminal TVSSY and the terminal TVSSX for the electrostatic potential lines and to be remote from the terminal $TCLX_{INV}$, the terminal TCLX, and the terminals TENB1 to TENB4 for the wiring lines that belong to the high frequency control signal for driving the data line driving circuit 101. In general, since electronic waves are reduced in proportion to the increase in the distance and the presence of the obstacles, it is possible to reduce the high frequency clock noise in the image signal lines 115 by arranging the wiring lines according to the present embodiment. That is, since the image signal lines 115 are arranged so as to be as far as possible from the group of wiring lines for the high frequency control signal, it is possible to reduce the influence of the noise. Also, the image signal lines 115 are electrically shielded from the wiring lines for the high frequency control signal by interposing the electrostatic potential lines. Therefore, it is possible to display high quality images without deteriorating the picture quality due to the influence of the noise.

[0092] The structures of the pixel portions of the electro-optical device by which the above-mentioned circuit operations are realized by the data lines 6a, the scanning lines 3a, and the TFTs 30 will now be described with reference to Figs. 6 and 7. Here, Fig. 6 is a plan view of a plurality of pixel groups adjacent to each other on the TFT array substrate on which data lines, scanning lines, and pixel electrodes are formed in the electro-optical device according to the embodiment of the present invention. Fig. 7 is a sectional view taken along the line A-A'.

[0093] In Fig. 6, the plurality of pixel electrodes 9a are provided on the TFT array substrate 10 in a matrix (the outlines are denoted by the dotted line portions 9a'). The data lines 6a and the scanning lines 3a are formed along the horizontal and vertical boundaries, respectively, of the pixel electrodes 9a. The data lines 6a are made of the metal film or the alloy film such as aluminum film. The scanning lines 3a are made of the conductive poly silicon film. The scanning lines 3a are arranged to face channel regions 1a' marked with forward leaning oblique lines in semiconductor layers 1a and function as gate electrodes. That is, the pixel switching TFTs 30 in which the main line portions of the scanning lines 3a face the channel regions 1a' as the gate electrodes are provided in the portions where the scanning lines 3a intersect the data lines 6a.

[0094] As illustrated in Fig. 7, the electro-optical device includes the transparent TFT array substrate 10 and the transparent counter substrate 20 arranged to face the TFT array substrate 10. The TFT array substrate 10 is made of a quartz substrate, a glass substrate, or a silicon substrate. The counter substrate 20 is made of a glass substrate or the quartz substrate. The pixel electrodes 9a are provided above the TFT array substrate 10. The alignment film 16 on which a predetermined alignment process, such as a rubbing process, has been performed is provided on the pixel electrodes 9a. The pixel electrodes 9a are made of a transparent conductive film, such as an indium tin oxide (ITO) film. On the other hand, the counter electrodes 21 are formed over the entire surface of the counter substrate 20. An alignment film 22 on which a predetermined alignment process, such as the rubbing process, has been performed is provided under the counter electrodes 21. The counter electrodes 21 are made of the transparent conductive film such as the ITO film like the above-mentioned pixel electrodes 9a. The alignment films 16 and 22 are made of a transparent organic film, such as a polyimide film. The liquid crystal layer 50 is in a predetermined alignment state by the alignment films 16 and 22 in a state where electric fields are not applied from the pixel electrodes 9a.

[0095] As illustrated in Fig. 7, the TFTs 30 have a lightly doped drain (LDD) structure and include the scanning lines 3a that function as the gate electrodes as mentioned above, the channel regions 1a' of the semiconductor layers 1a, which are made of the poly silicon film and whose channels are formed by the electric fields from the scanning lines 3a, insulating films 2 including gate insulating films for insulating the scanning lines 3a from the semiconductor layers 1a, the low concentration source regions 1b and the low concentration

drain regions 1c and the high concentration source regions 1d and the high concentration drain regions 1e in the semiconductor layers 1a.

[0096] Also, as illustrated in Fig. 7, the TFTs 30 preferably have the LDD structure. However, the TFTs 30 may alternatively have an offset structure in which impurities are not implanted into the low concentration source regions 1b and the low concentration drain regions 1c. The TFTs 30 may be self-aligning TFTs in which high concentration impurities are implanted using the gate electrodes formed of parts of the scanning lines 3a as masks and the high concentration source regions and the high concentration drain regions are formed by self-matching. Also, according to the present embodiment, a single gate structure in which only one gate electrode of the pixel switching TFT 30 is arranged between the high concentration source region 1d and the high concentration drain region 1e is used. However, two or more gate electrodes may be arranged between the high concentration source region 1d and the high concentration drain region 1e. As mentioned above, when the TFT is constituted of dual gates or multiple gates, it is possible to prevent current from leaking in the portions where the channels are connected to the source and drain regions and to thus reduce the amount of current during the off state of the switch. Furthermore, the semiconductor layers 1a that form the TFTs 30 may be non-single crystalline layers or single crystalline layers. The single crystalline layers may be formed by a well-known method such as a contact method. It is possible to improve the performances of peripheral circuits by making the semiconductor layers 1a out of single crystalline layers.

[0097] On the other hand, in Fig. 7, a storage capacitor 70 is composed of the high concentration drain region 1e of the TFT 30 and a relay layer 71 as the pixel potential capacitance electrode connected to the pixel electrode 9a, and a part of the capacitance line 300 as the fixed potential capacitance electrode. The two capacitance electrodes face each other through a dielectric film 75.

[0098] The capacitance lines 300 are made of a metal monomer, an alloy, a metal silicide, or a polysilicide including some amount of at least one refractory metal such as Ti, Cr, W, Ta, or Mo, or a material obtained by laminating two or more of these materials. The capacitance lines 300 may be made of the Al film.

[0099] The relay layers 71 are made of the conductive poly silicon film and function as the pixel potential capacitance electrodes. The relay layers 71 may be made of a single layer film or a multi-layer film including a metal or an alloy like the capacitance lines 300, as described below. The relay layers 71 relay connect the pixel electrodes 9a to the high

concentration drain regions 1e of the TFTs 30 through contact holes 83 and 85 via a relay, as well as function as the pixel potential capacitance electrodes.

[0100] The capacitance lines 300 function as the fixed potential capacitance electrodes and are arranged to face the relay layers 71. As illustrated in Fig. 6, the capacitance lines 300 overlap the regions in which the scanning lines 3a are formed in plan view. To be more specific, the capacitance lines 300 include the main line portions that extend along the scanning lines 3a, protrusions that protrude from the intersections between the scanning lines 3a and the data lines 6a to the upper portion along the data lines 6a, and connection portions corresponding to the contact holes 85. The protrusions use the regions on the scanning lines 3a and under the data lines 6a, thus increasing the available space in the regions where the storage capacitors 70 are formed. Also, the capacitance lines 300 preferably extend from the image display region 10a in which the pixel electrodes 9a are arranged into the peripheries of the image display region 10a to be electrically connected to electrostatic potential sources and to have fixed potential. As mentioned above, the electrostatic potential sources, such as the positive power source VDDX and the negative power source VSSX supplied to the data line driving circuits 101 or the counter electrode potentials LCCOM supplied to the counter electrodes 21 of the counter substrate 20 may be used as the electrostatic potential sources.

[0101] As illustrated in Fig. 7, the dielectric films 75 are made of a thin high temperature oxide (HTO) or a low temperature oxide (LTO) film having a thickness of about 5 to 200 nm such as a silicon oxide film or a silicon nitride film. In view of increasing the performance of the storage capacitors 70, the thinner the dielectric films 75 are, the better, as long as it is possible to secure sufficient reliability.

[0102] In Figs. 6 and 7, other than the above components, lower light-shielding films 11a are provided below the TFTs 30. The lower light-shielding films 11a are patterned in a matrix to thus define the apertures of the respective pixels. The lower light-shielding films 11a are made of a single layer film or a multi-layer film including the metal or the alloy like the above-mentioned capacitance lines 300. Also, the apertures are defined by the data lines 6a in Fig. 6 and the capacitance lines 300 formed so as to intersect the data lines 6a. The lower light-shielding films 11a preferably extend from the image display region 10a into the peripheries of the image display region 10a to thence be connected to the electrostatic potential sources like the above-mentioned capacitance lines 300, in order to prevent the changes in the potential from undesirably affecting the TFTs 30.

[0103] Basic insulating films 12 are provided under the TFTs 30. The basic insulating films 12 are formed over the entire surface of the TFT array substrate 10 to thus prevent the characteristics of the pixel switching TFTs 30 from changing due to the rough surface of the abraded TFT array substrate 10 or the contaminants left after cleaning the TFT array substrate 10, as well as to insulate the TFTs 30 from the lower light-shielding films 11a.

[0104] Furthermore, a first interlayer insulating film 41 containing contact holes 81 that lead to the high concentration source regions 1d and contact holes 83 that lead to the high concentration drain regions 1e is formed on top of the scanning lines 3a.

[0105] The relay layers 71 and the capacitance lines 300 are formed on top of the first interlayer insulating film 41. A second interlayer insulating film 42 containing the contact holes 81 that lead to the high concentration source regions 1d and the contact holes 85 that lead to the relay layers 71 is formed on top of the relay layers 71 and the capacitance lines 300.

[0106] Furthermore, the data lines 6a are formed on top of the second interlayer insulating film 42. A third interlayer insulating film 43 containing the contact holes 85 that lead to the relay layers 71 is formed on top of the data lines 6a.

[0107] Next, with reference to Fig. 7, corresponding to the sectional structures of the above-mentioned pixel portions, in particular, the sectional structures of the various signal wiring lines connected to the external circuit connection terminals according to the present embodiment will now be described. Here, Fig. 8 is a sectional view taken along the line B-B' of Fig. 4 or 5. Fig. 9 is a sectional view taken along the line C-C' of Fig. 4 or 5.

[0108] As illustrated in Fig. 8, all of the main wiring lines 108 connected to the terminals $TCLV_{INV}$ to TLCCOM corresponding to the right half of the view illustrated in Fig. 4 or 5 among the plurality of external circuit connection terminals 102 are simultaneously made of the same wiring line layer in the same manufacturing process on top of the second interlayer insulating film 42 illustrated in Fig. 7. Similarly, as illustrated in Fig. 9, the main wiring lines 108 connected to the terminals TVDDX to TLCCOM corresponding to the left half of the view illustrated in Fig. 4 or 5 among the plurality of external circuit connection terminals 102 are simultaneously made of the same wiring layer in the same manufacturing process on top of the second interlayer insulating film 42 illustrated in Fig. 7. That is, all of the main wiring lines 108 connected to the external circuit connection terminals 102 are made of the same wiring line layer formed at the same time as the wiring line layer of the data lines 6a formed on top of the second interlayer insulating film with reference to Fig. 7. The

respective external circuit connection terminals 102 are arranged in the order illustrated in Fig. 4 or 5 so that the main wiring lines 108 connected to the external circuit connection terminals 102 are arranged without intersecting each other on the substrate.

[0109] As mentioned above, since the various main wiring lines 108 connected to the external circuit connection terminals 102 can be made of the same wiring line layer, it is possible to easily form the main wiring lines 108 in the manufacturing processes. Furthermore, since the main wiring lines 108 can be made of the same wiring line layer as the data lines 6a, it is possible to further simplify the manufacturing processes. Furthermore, since the data lines 6a are made of a metal film or an alloy film of low resistance, such as an aluminum film as mentioned above, the various main wiring lines 108 connected to the external circuit connection terminals 102 formed at the same time as the data lines 6a can also be made of the signal wiring lines of the low resistance. Therefore, it is possible to prevent signals from being delayed.

[0110] An alternate configuration of the above-mentioned embodiment will be described with reference to Figs. 10 and 11. Here, Figs. 10 and 11 are sectional views of the main wiring lines and the redundant wiring lines according to the modification. Fig. 10 is a sectional view taken along the line C-C' of Figs. 4 or 5, like in Fig. 9 in the section orthogonal to the direction in which the main wiring lines and the redundant wiring lines extend. Fig. 11 is a sectional view taken along the section along the direction in which the main wiring lines and the redundant wiring lines extend.

[0111] As illustrated in Figs. 10 and 11, according to the modified embodiment, like in Fig. 9, the wiring lines LVDDX, LSPX, and LVSSX that are the plurality of main wiring lines 108 made of the aluminum film have redundant wiring lines 600, respectively. The redundant wiring lines 600 are made of a layer different from that of the main wiring lines 108, for example, of the same conductive film as the capacitance lines 300 such as refractory metal. Also, the redundant wiring lines 600 extend in a state of overlapping the corresponding main wiring lines 108 in plan view and have almost the same plane layout as that of the main wiring lines 108 in the regions that have the redundant structure. Furthermore, the redundant wiring lines 600 are electrically connected to the corresponding main wiring lines 108 through a plurality of contact holes 601 and function as the redundant wiring lines of the connected main wiring lines 108. The other structures are the same as the embodiments described with reference to Figs. 1 to 9.

[0112] Therefore, according to the present modified embodiment, it is possible to reduce the resistance of the main wiring lines 108 by adopting the redundant structures. Furthermore, even if one of the main wiring lines 108 or one of the redundant wiring lines that form the redundant structures is shorted, the redundant structures may continue to function as wiring lines. Therefore, it is possible to reduce the number of possible failure modes and to thus improve manufacturing yield.

[0113] Next, an embodiment of a projection color display device that is an example of an electronic apparatus in which the above-mentioned electro-optical device is used as a light valve will now be described with respect to the entire structure, in particular, the optical structure thereof. Here, Fig. 12 is a schematic sectional of a projection color display device.

[0114] In Fig. 12, a liquid crystal projector 1100 that is an example of a projection color display device according to the present embodiment includes three liquid crystal modules each including a liquid crystal device in which driving circuits are mounted on a TFT array substrate. The three liquid crystal modules are used as light valves 100R, 100G, and 100B for RGB. In the liquid crystal projector 1100, when projection light is emitted from a lamp unit 1102 that is a white light source such as a metal halide lamp, the projection light is divided into light components R, G, and B corresponding to the three primitive colors of RGB by three pieces of mirror 1106 and two pieces of dichroic mirror 11108 so that the divided light components are incident to the light valves 100R, 100G, and 100B corresponding to the respective colors. At this time, in particular, the light B is received through a relay lens system 1121 composed of an incidence lens 1122, a relay lens 11223, and an emission lens 1124 in order to prevent light loss due to a long light path. The light components corresponding to the three primitive colors modulated by the light valves 100R, 100G, and 100B are resynthesized by the dichroic prism 1112 and are projected to a screen 1120 through the projection lens 1114 as color images.

[0115] It should be understood that the present invention is not restricted to the above-mentioned embodiments and various changes in form and details may be made without departing from the spirit and scope of the invention as defined by the appended claims and the entire specification. The electro-optical device and the electronic apparatus in accordance with such modifications are included in the technical scope of the present invention.

WHAT IS CLAIMED IS:

1. An electro-optical device, comprising:

a plurality of pixel portions provided in an image display region on an element substrate;

in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region.

2. The electro-optical device according to Claim 1,

sub-wiring lines including at least one of internal wiring lines of the peripheral driving circuits, extending wiring lines extended from the peripheral driving circuits toward the pixel portions, and branch wiring lines branched from the main wiring lines, and first portions of the sub-wiring lines being made of a conductive film different from the same conductive film and being planarly laid out so as to intersect the main wiring lines with an interlayer insulating film therebetween in the peripheral region, and second portions thereof being formed of a same conductive film and are planarly laid out so as not to intersect the main wiring lines in the peripheral region.

3. The electro-optical device according to Claim 2,

the first portion and the second portion being electrically coupled to each other through contact holes formed in the interlayer insulating film.

4. The electro-optical device according to Claim 1, further comprising:

a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate; and

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, in order to connect a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, and the counter electrode,

the counter electrode potential line of the plurality of main wiring lines being positioned near edges of the element substrate in the peripheral region, and

the peripheral driving circuits being positioned nearer a center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region.

5. The electro-optical device according to Claim 4,

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of the external circuit connection terminals, which is coupled to one end of the counter electrode potential line, being positioned near the end of an array of the plurality of external circuit connection terminals.

6. The electro-optical device according to Claim 1, further comprising:

a counter electrode that is provided in the peripheral region on a counter substrate arranged to face the element substrate; and

upper and lower conduction terminals that are provided in the peripheral region on the element substrate, in order to couple a counter electrode potential line that supply counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, and the counter electrode,

the counter electrode potential line being positioned nearer edges of the element substrate than the one or plurality of main wiring lines excluding the counter electrode potential lines and nearer a center of the element substrate than the other or plurality of main wiring lines excluding the counter electrode potential line in the peripheral region,

a part of the peripheral driving circuits being partially positioned nearer the center of the element substrate than the upper and lower conduction terminals and the counter electrode potential line in the peripheral region, and the other parts of the peripheral driving circuits being partially positioned nearer the edges of the element substrate than the upper and lower conduction terminals and the counter electrode potential lines in the peripheral region.

7. The electro-optical device according to Claim 6,

the plurality of external circuit connection terminals being arranged along one side of the element substrate, and

the external circuit connection terminal of the plurality of external circuit connection terminals, which is connected to the other end or one end of plurality of main wiring lines, being positioned near the end of an array of the plurality of external circuit connection terminals.

8. The electro-optical device according to Claim 4,

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

9. The electro-optical device according to Claim 6,

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals, respectively, and that do not intersect the counter electrode potential line.

10. The electro-optical device according to Claim 1,

the plurality of main wiring lines including a pair of clock signal lines that supply a clock signal and an inverse signal thereof as electric signals and power source wiring lines that supply power source signals as electric signals, and

the pair of signal lines and power source wiring lines do not intersect each other.

11. The electro-optical device according to Claim 1,

the plurality of main wiring lines being planarly laid out so that the main wiring lines travel in zigzags so as not to intersect each other.

12. The electro-optical device according to Claim 1,

the plurality of main wiring lines including at least partially redundant wiring lines composed of a different conductive film formed in a layer different from a same conductive film.

13. An electro-optical device, comprising:

a plurality of pixel portions provided in an image display region on an element substrate;

a plurality of external circuit connection terminals provided in a peripheral region of the image display region on the element substrate;

scanning line driving circuits;

a data line driving circuit;

scanning line driving circuit wiring lines each having one end coupled to each of the external circuit connection terminals and having the other ends coupled to the scanning line driving circuits;

data line driving circuit wiring lines each having one end coupled to each of the external circuit connection terminals and having the other ends coupled to the data line driving circuit; and

image signal wiring lines each having one end coupled to each of the external circuit connection terminals, the image signal wiring lines supplying image signals of the plurality of pixel portions,

the scanning line driving circuit wiring lines, the data line driving circuit wiring lines, and the image signal wiring lines being planarly laid out so as not to intersect each other in the peripheral region.

14. The electro-optical device according to Claim 12,

the image signal wiring lines being arranged between the scanning line driving circuit wiring lines and the data line driving circuit wiring lines.

15. The electro-optical device according to Claim 12, further comprising:

a counter electrode that is provided in the peripheral region on the counter substrate arranged to face the element substrate; and

a counter electrode potential line having one end coupled to the external circuit connection terminals and having the other end that supplies counter potential to the counter electrode, and

the counter electrode potential line being arranged so as to surround the scanning line driving circuit wiring lines.

16. An electronic apparatus, comprising the electro-optical device according to Claim 1.

ABSTRACT OF THE DISCLOSURE

The invention provides an electro-optical device that can include, in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end connected to each of the plurality of external circuit connection terminals, and peripheral driving circuits connected to the other ends of the main wiring lines, the peripheral driving circuits for driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines. The plurality of main wiring lines can be made of the same conductive film and are planarly laid out so as not to intersect each other in the peripheral region.

Fig. 1

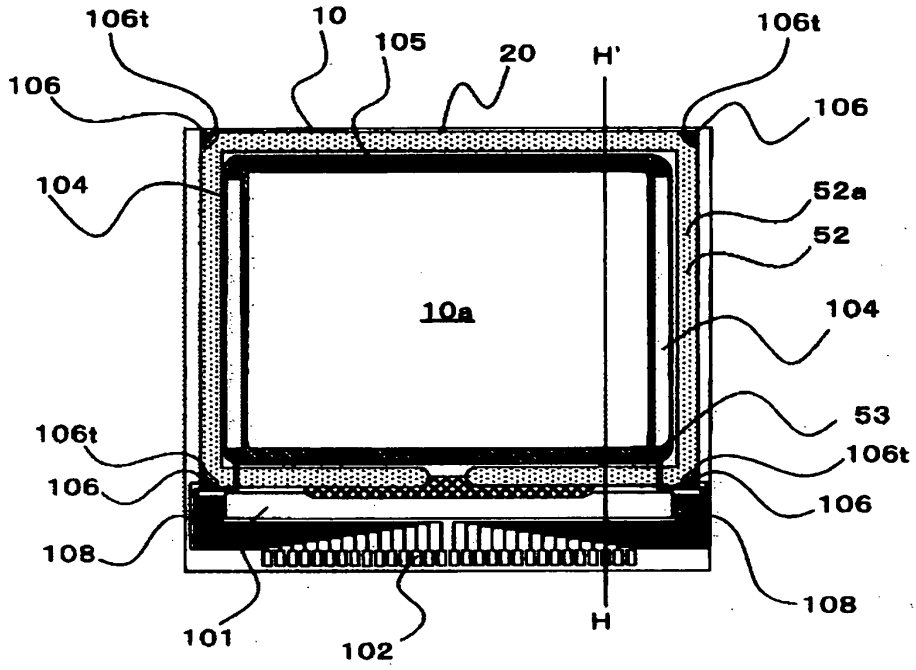

106t
10
105
20
H'
106t
106
106
104
52a
52
10a
104
53
106t
106t
106
106
108
108
101
102
H

Fig. 2

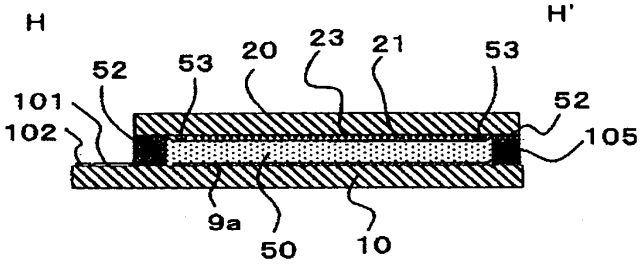

H
H'
52
53
20
23
21
53
101
102
52
105
9a
50
10

Fig. 3

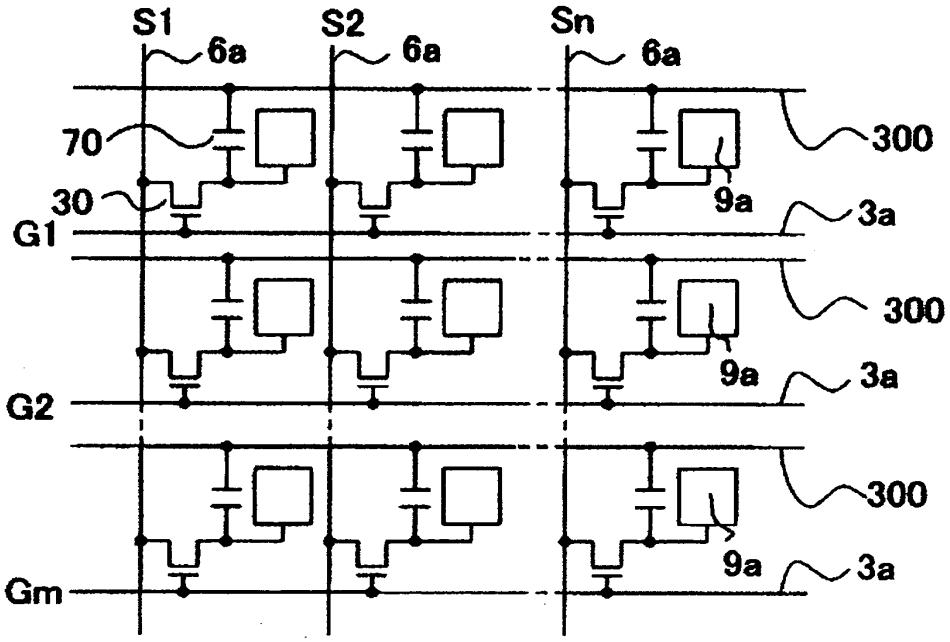


Fig. 4

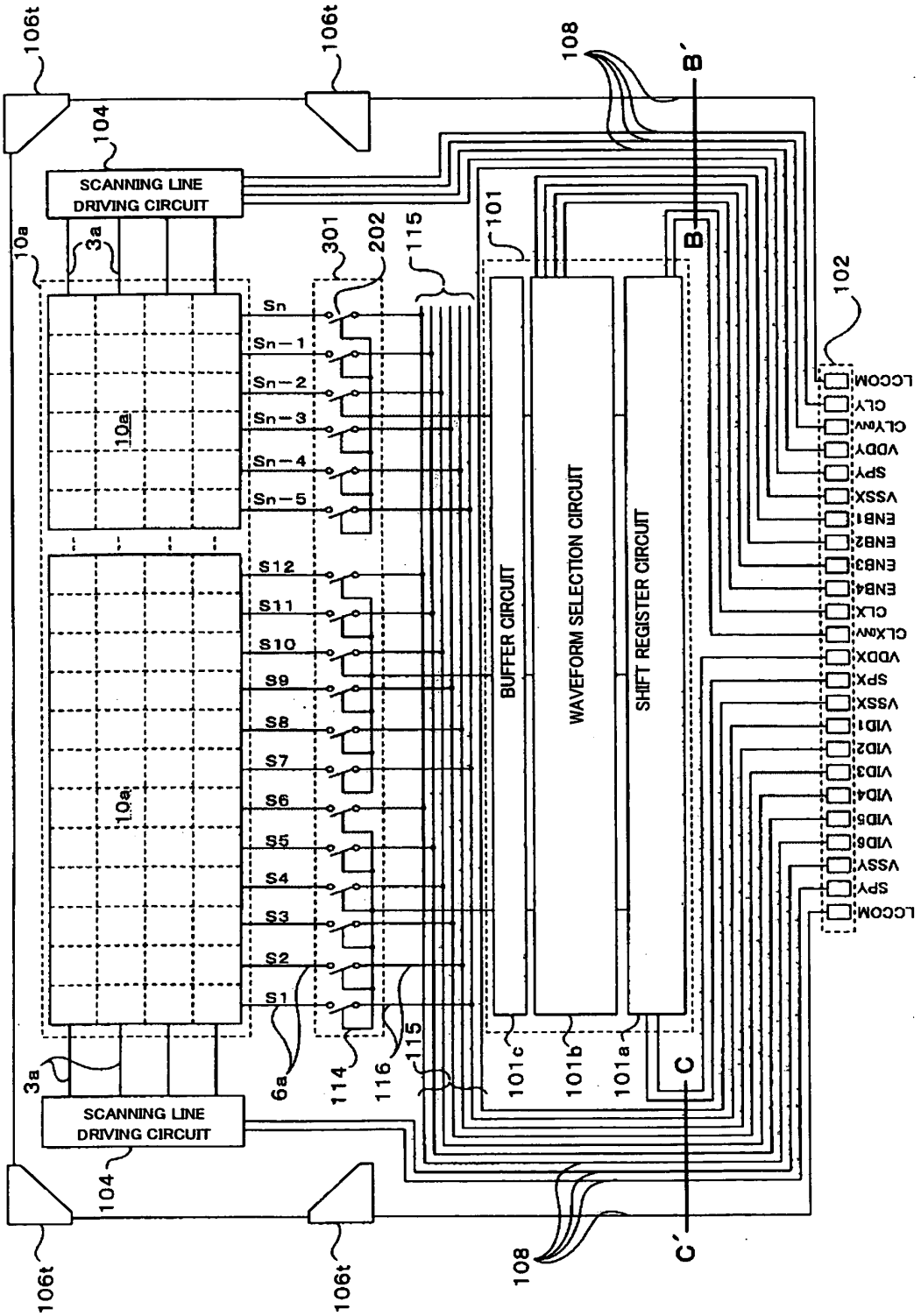

106t
106t
108
B'
104
SCANNING LINE DRIVING CIRCUIT
10a
3a
301
202
115
101
B
102
Sn
Sn−1
Sn−2
Sn−3
Sn−4
Sn−5
10a
S12
S11
S10
S9
S8
S7
S6
S5
S4
S3
S2
S1
10a
BUFFER CIRCUIT
WAVEFORM SELECTION CIRCUIT
SHIFT REGISTER CIRCUIT
LCCOM
CLY
CLYINV
VDDY
SPY
VSSX
ENB1
ENB2
ENB3
ENB4
CLX
CLXINV
VDDX
SPX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSY
SPY
LCCOM
3a
6a
114
116
115
101c
101b
101a
C
C'
SCANNING LINE DRIVING CIRCUIT
104
106t
106t
108

Fig. 5

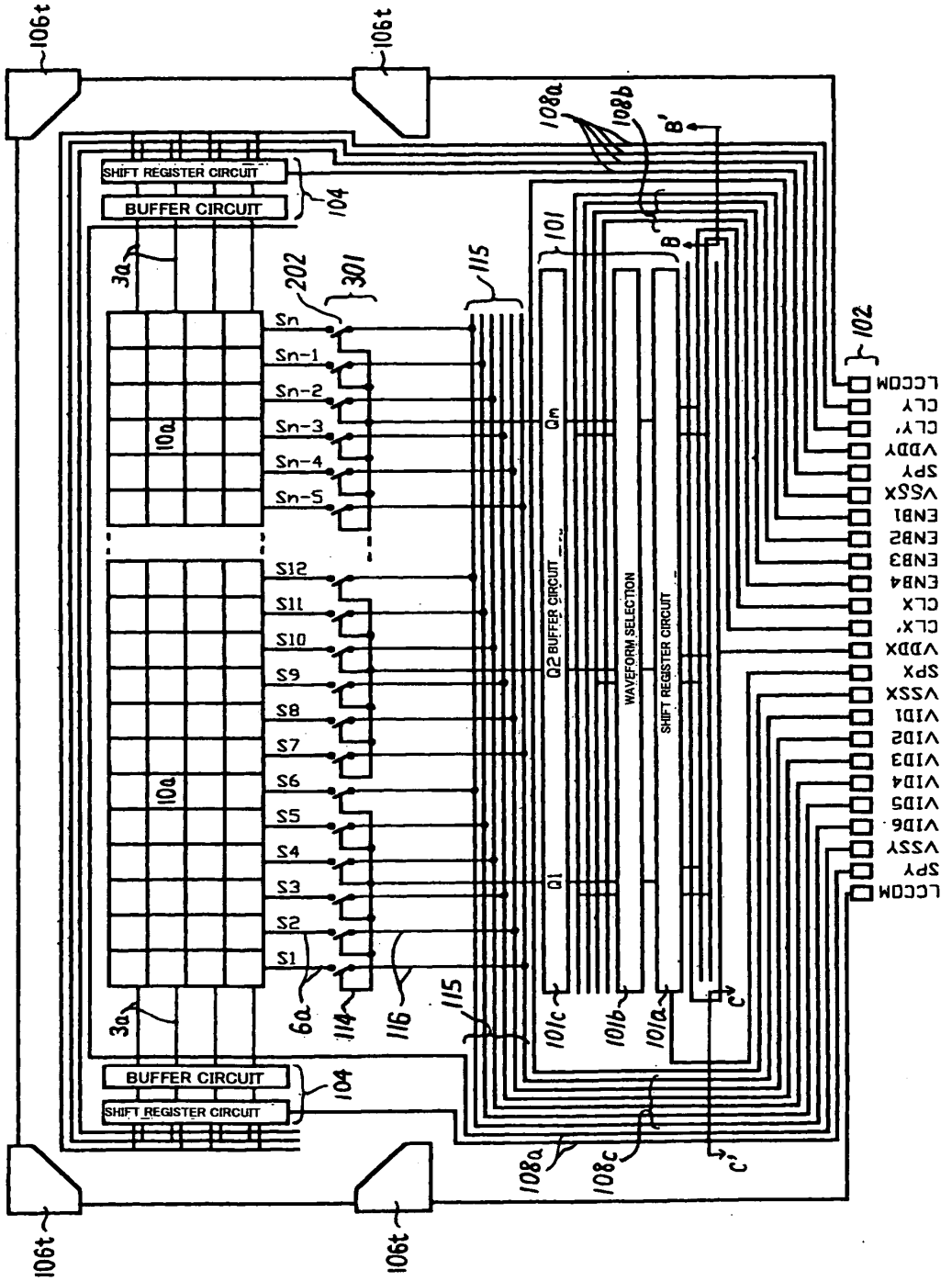

SHIFT REGISTER CIRCUIT
BUFFER CIRCUIT
104
106t
108a
108b
B'
B
101
102
115
202
301
3a
10a
6a
114
116
Sn
Sn-1
Sn-2
Sn-3
Sn-4
Sn-5
S12
S11
S10
S9
S8
S7
S6
S5
S4
S3
S2
S1
Qn
Q2
Q1
BUFFER CIRCUIT
WAVEFORM SELECTION
SHIFT REGISTER CIRCUIT
101c
101b
101a
C'
108c
LCCOM
CLY
CLY'
VDDY
SPY
VSSX
ENB1
ENB2
ENB3
ENB4
CLX
CLX'
VDDX
SPX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSY
SPY
LCCOM

Fig. 6

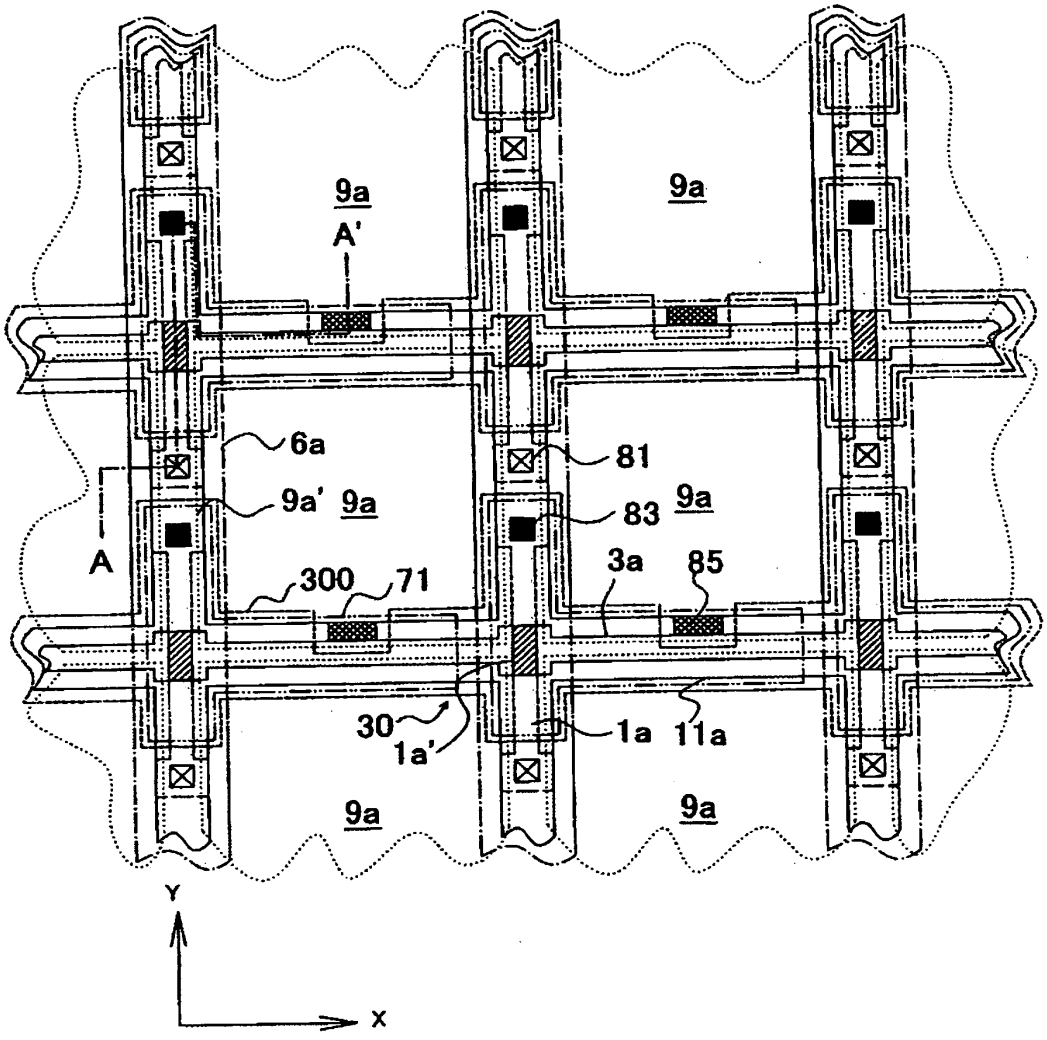


Fig. 7

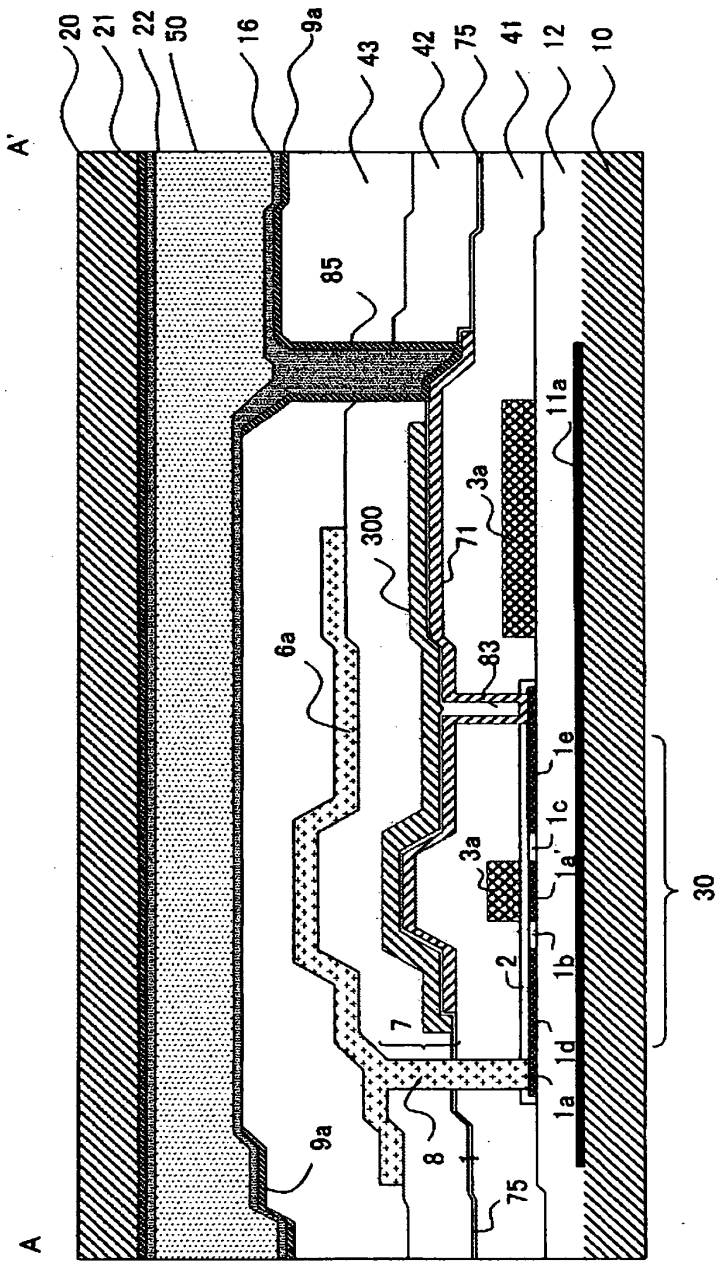

A'
A
20
21
22
50
16
9a
43
42
75
41
12
10
85
11a
3a
71
300
6a
83
1e
1c
1a'
1b
1d
1a
2
7
8
9a
75
30

Fig. 8

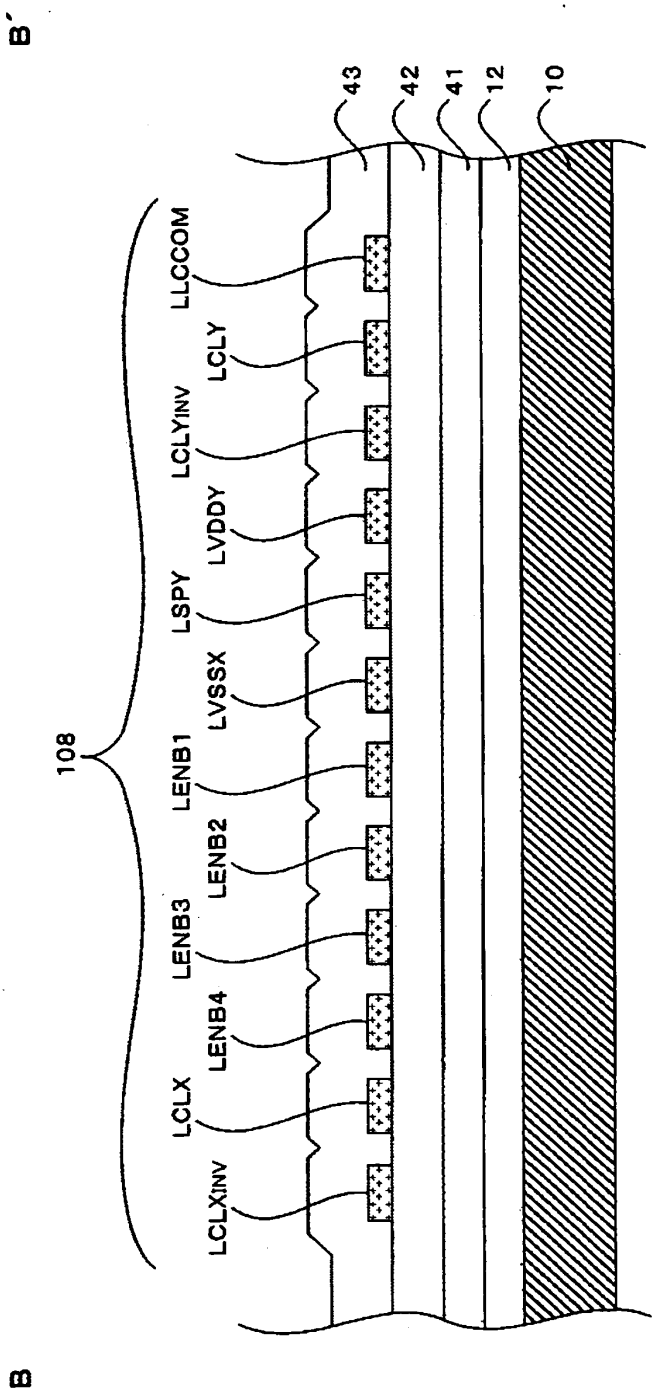

B'
B
108
LCLXINV
LCLX
LENB4
LENB3
LENB2
LENB1
LVSSX
LSPY
LVDDY
LCLYINV
LCLY
LLCCOM
43
42
41
12
10

Fig. 9

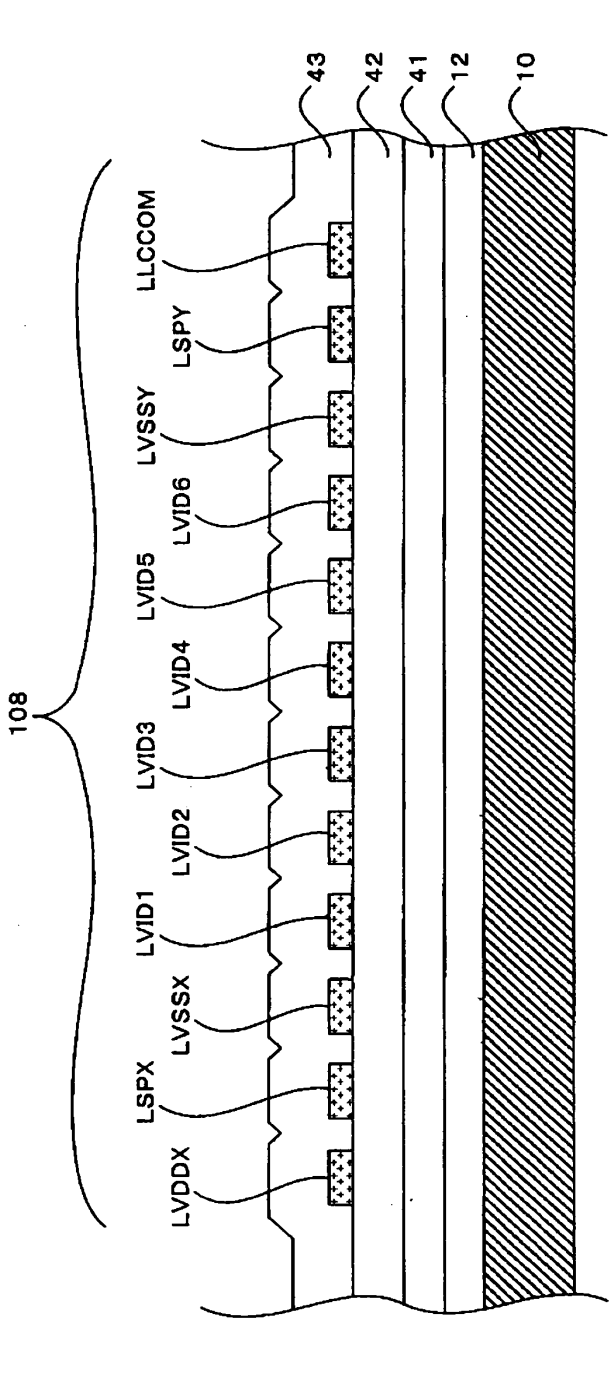

C'
C
108
LVDDX
LSPX
LVSSX
LVID1
LVID2
LVID3
LVID4
LVID5
LVID6
LVSSY
LSPY
LLCCOM
43
42
41
12
10

Fig. 10

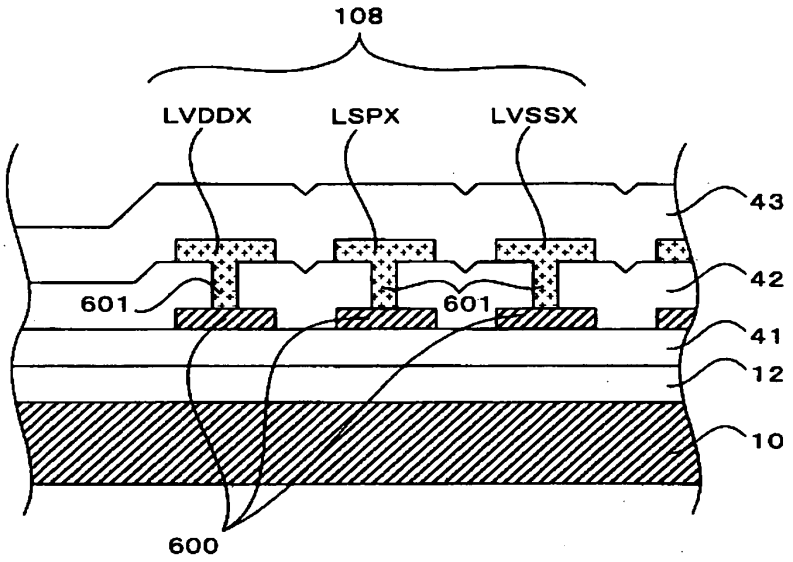

108
LVDDX
LSPX
LVSSX
43
42
601
601
41
12
10
600

Fig. 11

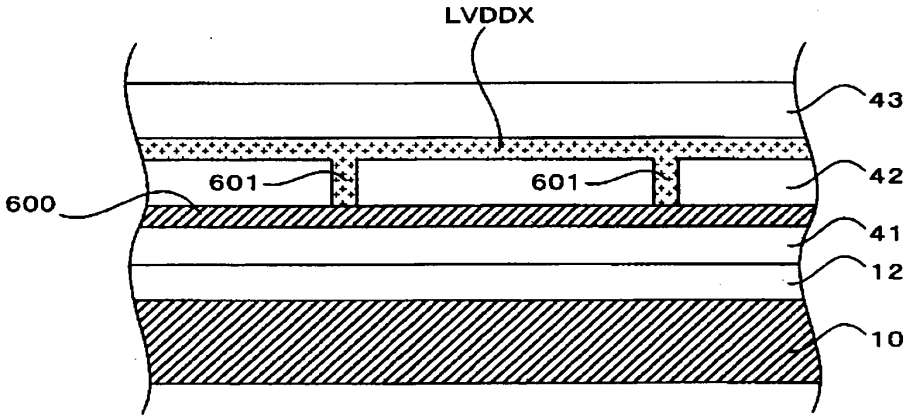
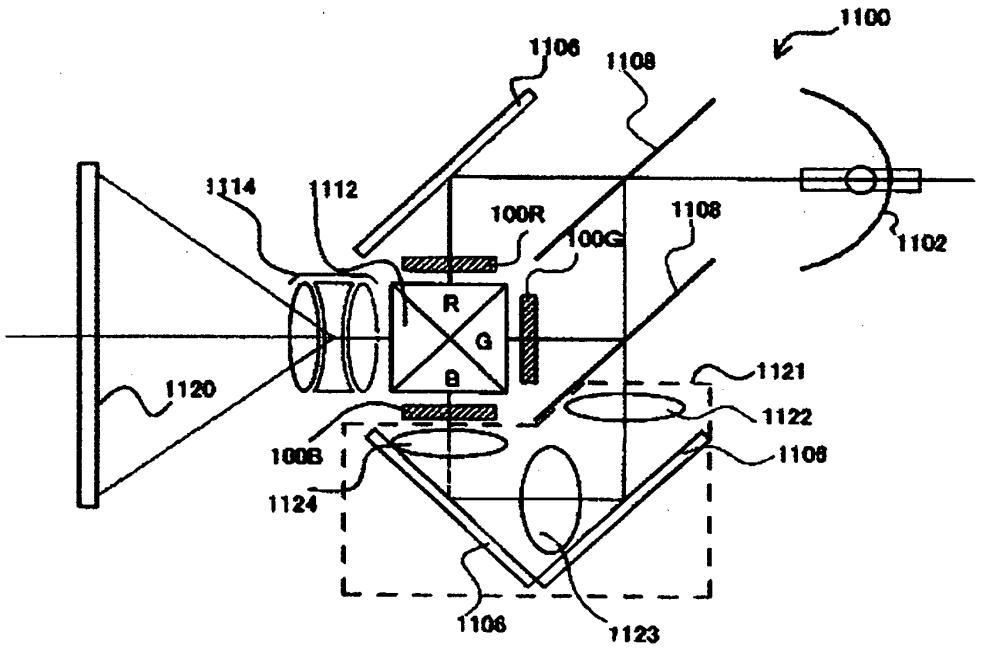

LVDDX
43
601
601
42
600
41
12
10

Fig. 12


1100
1106
1108
1114
1112
100R
100G
1108
1102
R
G
B
1120
1121
1122
1106
1124
1106
1123

Application Data Sheet

Application Information

Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R:	None
Title::	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME
Attorney Docket Number::	119570
Total Drawing Sheets::	10
Small Entity::	No

Applicant Information

Applicant Authority type::	Inventor
Primary Citizenship Country::	Japan
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Country of Residence::	Japan

Correspondence Information

Correspondence Customer Number:: 25944

Foreign Priority Information			
Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2003-156832	06/02/2003	Yes
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Assignee Information	
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Country of mailing address::	Japan
Postal or Zip Code of mailing address::	163-0811

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: New U.S. Patent Application

Filed: May 25, 2004 Docket No.: 119570

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. English-language Abstracts of non-English language reference Nos. 1-3 are attached hereto.

☒ 3. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See References 1-3.

Respectfully submitted,

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John S. Kern
Registration No. 42,719

JAO:JSK/mxm
Date: May 25, 2004

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Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 119570	APPLICATION NO. New U.S. Patent Application
INFORMATION DISCLOSURE STATEMENT		APPLICANT Masao MURADE	
(Use several sheets if necessary)		FILING DATE May 25, 2004	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 11-202367 w/ Abst & Trans	7/30/1999	Japan		
	2	JP A 11-223832 w/ Abst & Trans	8/17/1999	Japan		
	3	JP A 2002-49052 w/ Abst & Trans	5/15/2002	Japan		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: May 25, 2004

PATENT ABSTRACTS OF JAPAN

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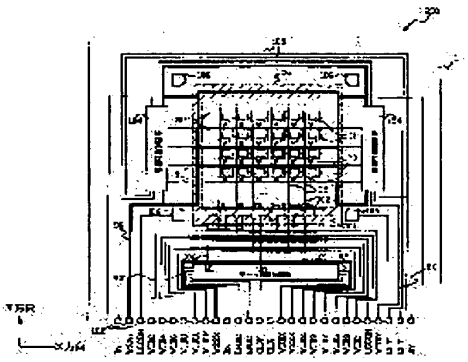
(51)Int.CI. G02F 1/136
G02F 1/133
G09G 3/36

(21)Application number : 10-015149
(22)Date of filing : 09.01.1998

(71)Applicant : SEIKO EPSON CORP
(72)Inventor : MURADE MASAO

(54) ELECTRO-OPTIC DEVICE AND ELECTRONIC EQUIPMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the generation of the clock noise or the like of a high frequency in image signals under the condition of the increase of image signal lines by the increase of a phase development number in the electro-optic device of an active matrix driving system.
SOLUTION: A liquid crystal device 200 is provided with a liquid crystal layer clamped between a pair of substrates, picture element electrodes 11 provided in a matrix shape on the substrate 1 and a TFT 30 for switching-controlling them. The image signal lines VID1-VID12 are pulled around from both sides of a data line driving circuit 101 on the substrate and the shield lines 80, 80', 82 and 86 of a constant potential for electrically shielding them from clock signal lines CLX and CLX' or the like are wired on the substrate.



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[Date of final disposal for application]
[Patent number]
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[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

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特開平11－202367

(43)公開日　平成11年(1999)７月30日

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	1/133	５５０		1/133	５５０
Ｇ０９Ｇ	3/36		Ｇ０９Ｇ	3/36	

審査請求　未請求　請求項の数16　ＦＤ　（全 22 頁）

(21)出願番号　特願平10－15149

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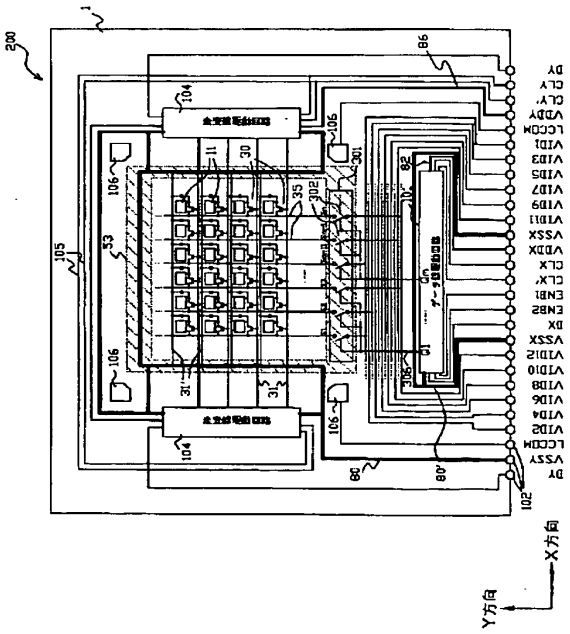
(74)代理人　弁理士　鈴木　喜三郎　（外２名）

(54)【発明の名称】　電気光学装置及び電子機器

(57)【要約】

【課題】　アクティブマトリクス駆動方式の電気光学装置において、相展開数の増加による画像信号線の増加という条件下で、画像信号中の高周波のクロックノイズ等の発生を低減する。

【解決手段】　液晶装置（２００）は、一対の基板間に挟持された液晶層と、基板（１）にマトリクス状に設けられた画素電極（１１）と、これをスイッチング制御するＴＦＴ（３０）とを備える。画像信号線（ＶＩＤ１～ＶＩＤ１２）は、基板上でデータ線駆動回路（１０１）の両側から引き回されており、これらをクロック信号線（ＣＬＸ、ＣＬＸ’）等から電気的にシールドする定電位のシールド線（８０、８０’、８２、８６）が基板上に配線されている。



(2)

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【特許請求の範囲】

【請求項１】　基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に接続された複数のスイッチング素子と、前記複数のスイッチング素子に接続された複数の画素電極と、画像信号が供給される複数の画像信号線と、クロック信号を含む制御信号が供給される複数の制御信号線と、前記画像信号線及び前記制御信号線を夫々介して前記画像信号及び前記制御信号が入力され、前記画像信号に対応するデータ信号を前記制御信号に基づいて前記複数のデータ線に供給するデータ信号供給手段とを備えており、

前記複数の画像信号線のうち第１画像信号線群は前記基板上で前記データ信号供給手段の一方の側へ引き回されており、前記複数の画像信号線のうち第２画像信号線群は前記第１基板上で前記データ信号供給手段の他方の側へ引き回されており、前記第１及び第２画像信号線群を前記複数の制御信号線から夫々電気的にシールドする少なくとも１本の導電線を前記基板上に更に備えたことを特徴とする電気光学装置。

【請求項２】　前記導電線は、前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短い周期を持つ高周波制御信号を供給する高周波制御信号線から、前記第１及び第２画像信号線群をシールドすることを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記第１及び第２画像信号線群と前記高周波制御信号線との間には、前記導電線と共に前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短くない周期を持つ低周波制御信号を供給する低周波制御信号線が配線されていることを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記第１画像信号線群に接続されており外部画像信号源から前記画像信号が夫々入力される複数の第１外部入力端子と、前記第２画像信号線群に接続されており前記外部画像信号源から前記画像信号が夫々入力される複数の第２外部入力端子と、前記制御信号線に接続されており外部制御信号源から前記制御信号が夫々入力される複数の第３外部入力端子と、前記導電線に夫々接続された複数の第４外部入力端子とを前記基板の周辺部上に更に備えており、前記第１及び第２外部入力端子の間には、前記第３外部入力端子が配置されており、前記第１及び第３外部入力端子の間並びに前記第３及び第２外部入力端子の間には、前記第４外部入力端子が夫々配置されていることを特徴とする請求項１に記載の電気光学装置。

【請求項５】　前記導電線は、前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短い周期を持つ高周波制御信号を供給する高周波制御信号線から、前記第１及び第２画像信号線群をシールドし、

前記第３外部入力端子のうち前記第４外部入力端子に隣

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接する端子は、前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短くない周期を持つ低周波制御信号を供給する低周波制御信号線に接続されていることを特徴とする請求項４に記載の電気光学装置。

【請求項６】　前記導電線は、前記データ信号供給手段に定電位のデータ線駆動用電源を供給するデータ線駆動用定電位線から構成された部分を含むことを特徴とする請求項１から５のいずれか一項に記載の電気光学装置。

【請求項７】　前記データ線駆動用定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、

該第１定電位線から構成された前記導電線部分は、前記基板上で前記第１及び第２画像信号線群を囲み、

前記第２定電位線から構成された前記導電線部分は、前記基板上で前記制御信号線を囲むことを特徴とする請求項６に記載の電気光学装置。

【請求項８】　前記導電線は、前記複数の画素電極により規定される画面表示領域及び前記複数のデータ線を前記基板上で囲むように延設されたこと特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記基板に対向して対向基板が設けられており、前記画面表示領域の輪郭に沿って前記基板及び対向基板のうち少なくとも一方に形成された遮光性の周辺見切りを更に備えており、

前記導電線は前記周辺見切りに対向する位置において前記周辺見切りに沿って前記基板に設けられた部分を含むことを特徴とする請求項８に記載の電気光学装置。

【請求項１０】　前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記画素電極に所定量の容量を付与する容量線を前記基板上に更に備えており、該容量線が前記導電線に接続されたことを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項１２】　走査信号を前記複数の走査線に供給する走査信号供給手段を前記基板上に更に備えており、

前記導電線は、前記走査信号供給手段に定電位の走査線駆動用電源を供給する走査線駆動用定電位線から構成された部分を含むことを特徴とする請求項１から１１のいずれか一項に記載の電気光学装置。

【請求項１３】　前記走査信号供給手段は、前記複数の画素電極により規定される画面表示領域の両側に設けられており、

前記走査線駆動用定電位線から構成された前記導電線部分は、前記画面表示領域及び前記複数のデータ線を前記第１基板上で囲むように且つ前記走査線供給手段に前記走査線駆動用電源を冗長的に供給するように延設されていることを特徴とする請求項１２に記載の電気光学装置。

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【請求項１４】　前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記制御信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、
前記第１画像信号線群に含まれる画像信号線と前記第２画像信号線群に含まれる画像信号線とは、前記データ線駆動回路と前記サンプリング回路との間において、少なくとも１本の画像信号線毎に前記データ線駆動回路の両側から櫛歯状に交互に引き回されていることを特徴とする請求項１から１３のいずれか一項に記載の電気光学装置。
【請求項１５】　前記データ信号供給手段は、前記データ線毎に前記データ信号の電圧極性を反転し、
前記第１画像信号線群に含まれる画像信号線と前記第２画像信号線群に含まれる画像信号線とは、相隣接する２本のデータ線に対応する２本の画像信号線を対にして前記データ線駆動回路の両側から櫛歯状に交互に引き回されていることを特徴とする請求項１４に記載の電気光学装置。
【請求項１６】　請求項１から１５に記載の電気光学装置を備えたことを特徴とする電子機器。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、薄膜トランジスタ（以下、ＴＦＴと称す）駆動等によるアクティブマトリクス駆動方式の液晶装置等の電気光学装置及びこれを用いた電子機器の技術分野に属し、特にＴＦＴアレイ基板上に設けられたデータ線駆動回路によりクロック信号等の制御信号に基づいてデータ線を高周波で駆動する形式の電気光学装置及びこれを用いた電子機器の技術分野に属する。
【０００２】
【従来の技術】従来、ＴＦＴ駆動によるアクティブマトリクス駆動方式の液晶装置においては、縦横に夫々配列された多数の走査線及びデータ線並びにこれらの各交点に対応して多数の画素電極がＴＦＴアレイ基板上に設けられている。そして、これらに加えて、データ線駆動回路、サンプリング回路等を含みデータ線にデータ信号を供給するデータ信号供給手段や、走査線駆動回路等を含み走査線に走査信号を供給する走査信号供給手段が、このようなＴＦＴアレイ基板上に設けられる場合がある。
【０００３】この場合、データ信号供給手段には、データ信号の供給タイミングの基準となるデータ線駆動回路を動作させるためのデータ線側基準クロックなどの制御信号、表示すべき画像の内容に対応しておりデータ信号の基となる画像信号、正や負の定電位電源等が、ＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して夫々供給される。他方、走査信号供給手段には、走査信号の供給タイミングの基準となる走査線駆動回路を動作させるための走査線側基準クロック、正や負の定電位電源等が、やはりＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して供給される。そして走査信号供給手段においては、例えば走査線駆動回路により、走査線側基準クロックに基づくタイミングで走査信号を走査線に線順次で供給する。これに対応してデータ信号供給手段においては、例えば入力された画像信号をサンプリングするサンプリング回路を、データ線駆動回路がデータ線側基準クロックに基づくタイミングで順次駆動して、サンプリング回路からデータ信号がデータ線に供給される。これらの結果、走査線にゲート接続された各ＴＦＴは、走査信号の供給に応じて導通状態とされ、データ信号が当該ＴＦＴを介して画素電極に供給されて各画素における画像表示が行われる。

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【０００４】近年特に、液晶プロジェクタ用の液晶装置等では、表示画像の高解像度化に伴って、非常に高い周波数のシリアルな画像信号が入力されるようになってきている。例えば、画像信号のドット周波数は、近時の高解像度のパソコン画面において使用されるＸＧＡ表示モードやＳＸＧＡ表示モードになると、夫々約６５ＭＨｚと約１３５ＭＨｚであり、従来のＶＧＡ表示モードにおけるドット周波数（約３０ＭＨｚ）を遥かに上回る。これに対応すべく、特にデータ信号供給手段に供給されるデータ線側基準クロックの周波数も非常に高くなってきている。
【０００５】
【発明が解決しようとする課題】しかしながら、近年の表示画像の高品位化の要請の下では、このように基準クロックの周波数を高くすることによる、高周波のクロックノイズの発生が無視し得ないようになる。即ち、例えば従来の比較的周波数の低いデータ線側基準クロックをデータ線駆動回路に供給してサンプリング回路を駆動する構成において、そのままクロック信号の周波数を上げたのでは、サンプリング回路に入力される画像信号中やサンプリング回路から出力されるデータ信号中に高周波のクロックノイズが発生して、データ線に供給すべきデータ信号が劣化してしまう。このように劣化したデータ信号の供給を受けたのでは、各画素電極により表示される画像もやはり劣化してしまうという問題点がある。例えば、各画素において中間レベルの階調表示を行う時に、１０ｍＶ程度の微少なノイズが画像信号中に飛び込んだだけでも、表示画像中に視認可能な程度のノイズとして現れてしまう。これは、最高又は最低の液晶駆動電圧（例えば、０～５Ｖ間の電圧）に対応する白又は黒レベルの表示を行っている場合と比べて、中間レベルにおける液晶駆動電圧の変化に対する液晶の透過率の変化が急峻だからである。このように高精度の多階調表示を実現するためには、高周波のクロックノイズの問題は重大である。
【０００６】他方で、相展開数を増やすことによりサンプリング回路に供給される画像信号の周波数を下げるこ

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とはできるが、液晶パネルの基板に設けねばならない画像信号入力用の外部入力端子の数は、相展開数の増加に対応して増やさねばならない。即ち、例えば６相展開の場合には、画像信号入力用の外部入力端子は６個必要となり、１２相展開の場合には、１２個必要となる。更に、これらの画像信号入力用の外部入力端子からサンプリング回路まで引き回す配線の数も同様に相展開数だけ必要となる。これらの結果、画像信号用の配線が液晶パネルの基板面上を占める割合が増加して、サンプリング回路、データ線駆動回路等からなるデータ信号供給手段を形成する領域を基板上に確保するのが困難となる。ここで仮に従来のように、外部入力端子が設けられた基板の縁から見て、データ線駆動回路の一方の側へクロック信号等の制御信号用の配線を引き回し、データ線駆動回路の他方の側へ多数の画像信号用の配線を引き回したのでは、各側に引き回される配線数が顕著に異なるため、データ線駆動回路の周囲における配線の配置バランスが非常に悪くなる（即ち、配線が片側に偏る）という問題点が生じる。この場合、液晶パネルの基板を大きくして配線領域やデータ線駆動回路を形成する領域を確保することは可能であるが、これでは、限られた基板サイズでの画面の大型化という液晶パネルの技術分野における基本的要請に反してしまう。

【０００７】本発明は上述の問題点に鑑みなされたものであり、画像信号の相展開数の増加に伴って配線数や外部入力端子数が増加してもこれらをバランス良く配線や配置することができ、しかも画像信号に対して高周波のクロック信号等の制御信号が及ぼす高周波のクロックノイズ等の悪影響を低減でき、高品位の画像表示を行える液晶装置及び当該液晶装置を備えた電子機器を提供することを課題とする。

【０００８】

【課題を解決するための手段】請求項１に記載の電気光学装置は上記課題を解決するために、基板上に複数のデータ線と、該複数のデータ線に交差する複数の走査線と、前記複数のデータ線及び走査線に接続された複数のスイッチング素子と、前記複数のスイッチング素子に接続された複数の画素電極と、画像信号が供給される複数の画像信号線と、クロック信号を含む制御信号が供給される複数の制御信号線と、前記画像信号線及び前記制御信号線を夫々介して前記画像信号及び前記制御信号が入力され、前記画像信号に対応するデータ信号を前記制御信号に基づいて前記複数のデータ線に供給するデータ信号供給手段とを備えており、前記複数の画像信号線のうち第１画像信号線群は前記基板上で前記データ信号供給手段の一方の側へ引き回されており、前記複数の画像信号線のうち第２画像信号線群は前記基板上で前記データ信号供給手段の他方の側へ引き回されており、前記第１及び第２画像信号線群を前記複数の制御信号線から夫々電気的にシールドする少なくとも１本の導電線を前記基板上に更に備えたことを特徴とする。

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【０００９】請求項１に記載の電気光学装置によれば、画像信号は、画像信号線を介して、データ信号供給手段に供給される。これと並行して、クロック信号、イネーブル信号等を含む制御信号は、制御信号線を介して、データ信号供給手段に供給される。すると、例えばデータ線駆動回路、サンプリング回路等を含んで構成されるデータ信号供給手段により、制御信号に基づいて画像信号に対応するデータ信号が、複数のデータ線に供給される。ここで特に、基板に配線された導電線により、画像信号線は、クロック信号線、イネーブル信号線等の制御信号線から夫々電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、クロック信号線等の制御信号線から画像信号線への高周波のクロックノイズ等の飛び込みを低減できる。

【００１０】他方で、基板に形成されるか又は基板に接続された走査線駆動回路等を含む走査信号供給手段により、走査信号が走査線を介してスイッチング素子に供給される。これと並行して、上述のように高周波のクロックノイズ等が低減された画像信号に対応するデータ信号が、データ線を介してスイッチング素子に供給され、更にスイッチング素子を介して供給されるデータ信号により画素電極に印加される電圧が変化し、当該画素電極に対向する液晶が駆動される。

【００１１】以上の結果、表示すべき画像の解像度が高く、例えば多相展開された画像信号が入力される場合にも、高周波のクロックノイズ等の発生により画質が劣化することは殆ど又は全く無くなり、高品位の画像表示が可能とされる。しかも、第１画像信号線群は、基板上でデータ信号供給手段の一方の側へ引き回されており、第２画像信号線群は基板上でデータ信号供給手段の他方の側へ引き回されている。従って、例えば１２相展開、２４相展開、…というように相展開数を増やすことによりデータ信号供給手段に供給される画像信号の周波数を下げつつ、多相展開に対応する多数の画像信号線については、データ信号供給手段の両側にバランス良く配置できる。この結果、サンプリング回路或いはサンプリング回路、データ線駆動回路等からなるデータ信号供給手段を形成する領域を基板上に容易に確保することができる。従って、限られた基板サイズでの画面の大型化を図ることも可能となる。

【００１２】請求項２に記載の電気光学装置は請求項１に記載の電気光学装置において、前記導電線は、前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短い周期を持つ高周波制御信号を供給する高周波制御信号線から、前記第１及び第２画像信号線群をシールドすることを特徴とする。

【００１３】請求項２に記載の電気光学装置によれば、導電線により、画像信号線は、複数の制御信号線のうち高周波制御信号（例えば、クロック信号、イネーブル信

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号等）を供給する高周波制御信号線から電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、高周波制御信号線から画像信号線への高周波のクロックノイズ等の飛び込みを低減できる。尚、低周波制御信号（例えば、データ線駆動回路内のシフトレジスタ用のスタート信号等）については、画像信号やデータ信号中の高周波ノイズの原因とはならないため、これを供給する低周波制御信号線を導電線によりシールドしてもよく、シールドしなくてもよい。

【００１４】請求項３に記載の電気光学装置は請求項２に記載の電気光学装置において、前記第１及び第２画像信号線群と前記高周波制御信号線との間には、前記導電線と共に前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短くない周期を持つ低周波制御信号を供給する低周波制御信号線が配線されていることを特徴とする。

【００１５】請求項３に記載の電気光学装置によれば、第１及び第２画像信号線群の中で高周波制御信号線に近い側に位置する画像信号線は、低周波制御信号線と導電線との少なくとも合計２本の配線の存在により、高周波制御信号線から離間され且つ電気的にシールドされている。即ち、画像信号やデータ信号中の高周波ノイズの原因とはならない低周波制御信号（例えば、データ線駆動回路内のシフトレジスタ用のスタート信号等）を供給する低周波制御信号線を、高周波制御信号線と画像信号線との間に導電線と共に配置することにより、高周波制御信号線の画像信号線に対するクロックノイズ等の悪影響を更に低減できる。特に、一般に距離及び障害物の介在に応じて電磁波は減少するので、制御信号線と画像信号線との間に導電線や低周波制御信号線をなるべく多く配線する構成により、高周波制御信号線から画像信号線に印加される電磁波が減少する。このように、導電線以外に低周波制御信号線を高周波制御信号線と画像信号線との間に介在させることは基板上スペースの有効利用及びノイズ低減の観点から見て有利である。

【００１６】請求項４に記載の電気光学装置は請求項１に記載の電気光学装置において、前記第１画像信号線群に接続されており外部画像信号源から前記画像信号が夫々入力される複数の第１外部入力端子と、前記第２画像信号線群に接続されており前記外部画像信号源から前記画像信号が夫々入力される複数の第２外部入力端子と、前記制御信号線に接続されており外部制御信号源から前記制御信号が夫々入力される複数の第３外部入力端子と、前記導電線に夫々接続された複数の第４外部入力端子とを前記基板の周辺部上に更に備えており、前記第１及び第２外部入力端子の間には、前記第３外部入力端子が配置されており、前記第１及び第３外部入力端子の間並びに前記第３及び第２外部入力端子の間には、前記第４外部入力端子が夫々配置されていることを特徴とする。

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【００１７】請求項４に記載の電気光学装置によれば、基板の周辺部上において、第１及び第２画像信号線群に夫々接続された複数の第１及び第２外部入力端子の間には、制御信号線に接続された複数の第３外部入力端子が配置されている。即ち、第１から第４外部入力端子が設けられた基板の周辺部上において、中央に制御信号線に接続された複数の第３外部入力端子が集中配置されており、その両側に第１及び第２画像信号線群に夫々接続された複数の第１及び第２外部入力端子が配置されている。そして、これらの間に、導電線に接続された第４外部入力端子が配置されている。従って、第１及び第２画像信号線群と制御信号線との間に基板上で距離を置くと共に、これらの間に導電線を配線する構成を容易に得ることができる。特に、当該電気光学装置に入力される前段階で、クロック信号等の制御信号が、画像信号に対しクロックノイズ等を発生させてしまう事態を効果的に阻止し得る。仮に、画像信号線に接続された複数の外部入力端子と制御信号線に接続された複数の外部入力端子とが混在していたり、隣接していたりすれば、当該電気光学装置に入力される前段階で、画像信号線と制御信号線とが隣接或いは近接する配線部分が不可避となり、画像信号中にクロックノイズ等が飛び込んでしまうのである。このように本発明によれば、電気光学装置に入力される前後において、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。尚、より好ましくは、基板の周辺部において外部入力端子を形成可能な領域において、第１及び第２外部入力端子を可能な限り両側に寄せて配置すると共に、両者の間に配置される第３外部入力端子との間に可能な限り間隔を空けて、この間隔に導電線に接続された第４外部入力端子を配置する。

【００１８】請求項５に記載の電気光学装置は請求項４に記載の電気光学装置において、前記導電線は、前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短い周期を持つ高周波制御信号を供給する高周波制御信号線から、前記第１及び第２画像信号線群をシールドし、前記第３外部入力端子のうち前記第４外部入力端子に隣接する端子は、前記複数の制御信号線のうち少なくとも前記画像信号の水平走査期間よりも短くない周期を持つ低周波制御信号を供給する低周波制御信号線に接続されていることを特徴とする。

【００１９】請求項５に記載の電気光学装置によれば、導電線により、画像信号線は、高周波制御信号線から電気的にシールドされている。ここで特に、制御信号線に接続された第３外部入力端子のうち導電線に接続された第４外部入力端子に隣接する端子は、低周波制御信号線に接続されているので、画像信号線は、低周波制御信号線と導電線との少なくとも合計２本の配線の存在により、高周波制御信号線から離間され且つ電気的にシールドされる。

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【００２０】請求項６に記載の電気光学装置は請求項１に記載の電気光学装置において、前記導電線は、前記データ信号供給手段に定電位のデータ線駆動用電源を供給するデータ線駆動用定電位線から構成された部分を含むことを特徴とする。

【００２１】請求項６に記載の電気光学装置によれば、導電線は、前記データ信号供給手段に定電位のデータ線駆動用電源を供給するデータ線駆動用定電位線から構成された部分を含むので、外部入力端子や配線そのものを共用することにより、言い換えれば定電位線を延設して導電線とすることにより、構成の簡略化と省スペース化を図ることが出来、特に導電線を定電位とすることも極めて容易となる。

【００２２】請求項７に記載の電気光学装置は請求項６に記載の電気光学装置において、前記データ線駆動用定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、該第１定電位線から構成された前記導電線部分は、前記基板上で第１及び第２画像信号線群を囲み、前記第２定電位線から構成された前記導電線部分は、前記基板上で前記第１基板上で前記制御信号線を囲むことを特徴とする。

【００２３】請求項７に記載の電気光学装置によれば、第１及び第２画像信号線群は、例えば接地電位の負電源を供給するための第１定電位線から構成された導電線部分により、基板上で囲まれている。制御信号線は、例えば正電源を供給するための第２定電位線から構成された導電線部分により、基板上で囲まれている。従って、画像信号線は、第１基板上で制御信号線から２重にシールドされた構成が得られる。

【００２４】請求項８に記載の電気光学装置は請求項１から７のいずれか一項に記載の電気光学装置において、前記導電線は、前記複数の画素電極により規定される画面表示領域及び前記複数のデータ線を前記基板上で囲むように延設されたこと特徴とする。

【００２５】請求項８に記載の電気光学装置によれば、導電線により、画面表示領域及び複数のデータ線は、基板上で囲まれているので、当該画面表示領域及び複数のデータ線も、クロック信号線等の制御信号線からシールドされることになる。従って、データ信号供給手段から出力されたデータ信号、スイッチング素子や画素電極に到達したデータ信号等における、高周波のクロックノイズ等の発生を低減できる。

【００２６】請求項９に記載の電気光学装置は請求項８に記載の電気光学装置において、前記基板に対向して対向基板が設けられており、前記画面表示領域の輪郭に沿って前記基板及び対向基板のうち少なくとも一方に形成された遮光性の周辺見切りを更に備えており、前記導電線は前記周辺見切りに対向する位置において前記周辺見切りに沿って前記基板に設けられた部分を含むことを特徴とする。

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【００２７】請求項９に記載の電気光学装置によれば、導電線は、基板の周辺見切り下に設けられているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を基板の周辺部分に余裕を持って形成することができ、導電線形成により液晶装置における有効表示面積の減少することも殆ど又は全くない。

【００２８】請求項１０に記載の電気光学装置は請求項１から９のいずれか一項に記載の液晶装置において、前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする。

【００２９】請求項１０に記載の電気光学装置によれば、導電線は例えば、Ａｌ（アルミニウム）等の、データ線と同一の低抵抗金属材料から形成されているので、導電線の引き回し領域が、たとえ長くても、導電線の抵抗は実用上十分に低く抑えられる。即ち、抵抗増加によりシールドの効果を下げることなく、例えば他の配線や回路等の隙間を縫ってジグザグに導電線を長く配線したり、画面表示領域等までも含めた広い領域に導電線を長く配線することが可能となるので、比較的簡単な構成により、当該シールドの効果を全体として、より高めることが出来る。更に、当該電気光学装置の製造プロセスにおいて、導電線及びデータ線を、同一の低抵抗金属材料から同一工程により形成できる。即ち、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。

【００３０】請求項１１に記載の電気光学装置は請求項１から１０のいずれか一項に記載の電気光学装置において、前記画素電極に所定量の容量を付与する容量線を更に備えており、該容量線が前記導電線に接続されたことを特徴とする。

【００３１】請求項１１に記載の電気光学装置によれば、容量線により画素電極に所定量の容量が付与されているので、デューティー比が小さくても高精細な表示が可能とされる。そして、容量線は導電線に接続されている。従って、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。

【００３２】請求項１２に記載の電気光学装置は請求項１から１１のいずれか一項に記載の電気光学装置において、走査信号を前記複数の走査線に順次供給する走査信号供給手段を前記基板上に更に備えており、前記導電線は、前記走査信号供給手段に定電位の走査線駆動用電源を供給する走査線駆動用定電位線から構成された部分を含むことを特徴とする。

【００３３】請求項１２に記載の電気光学装置によれば、走査線駆動用定電位線から構成された導電線部分に

より、画像信号線は、制御信号線から電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、制御信号線から画像信号線への高周波のクロックノイズ等の飛び込みを低減できる。

【００３４】請求項１３に記載の電気光学装置は請求項１２に記載の電気光学装置において、前記走査信号供給手段は、前記複数の画素電極により規定される画面表示領域の両側に設けられており、前記走査線駆動用定電位線から構成された前記導電線部分は、前記画面表示領域及び前記複数のデータ線を前記基板上で囲むように且つ前記走査線供給手段に前記走査線駆動用電源を冗長的に供給するように延設されている。

【００３５】請求項１３に記載の電気光学装置によれば、走査線駆動用定電位線から構成された導電線部分により、画面表示領域及び複数のデータ線は、基板上で囲まれているので、当該画面表示領域及び複数のデータ線も、クロック信号線等の制御信号線からシールドされることになる。従って、データ信号供給手段から出力されたデータ信号、スイッチング素子や画素電極に到達したデータ信号等における、高周波のクロックノイズ等の発生を低減できる。更に、走査線駆動用定電位線から構成された導電線部分は、画面表示領域の両側に設けられた走査線供給手段に走査線駆動用電源を冗長的に供給するように延設されているので、たとえ、走査線駆動用定電位線から構成された導電線部分や、それ以外の部分で走査線駆動用定電位線に断線が生じても、装置欠陥になり難いので有利である。

【００３６】請求項１４に記載の電気光学装置は請求項１から１３のいずれか一項に記載の電気光学装置において、前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記制御信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記第１画像信号線群に含まれる画像信号線と前記第２画像信号線群に含まれる画像信号線とは、前記データ線駆動回路と前記サンプリング回路との間において、少なくとも１本の画像信号線毎に前記データ線駆動回路の両側から櫛歯状に交互に引き回されていることを特徴とする。

【００３７】請求項１４に記載の電気光学装置によれば、第１画像信号線群に含まれる画像信号線（例えば、奇数番目のデータ線に対応する画像信号線ＶＩＤ１、３、５、７、…）と第２画像信号線群に含まれる画像信号線（例えば、偶数番目のデータ線に対応する画像信号線ＶＩＤ２、４、６、８、…）とは、少なくとも１本の画像信号線毎にデータ線駆動回路の両側から櫛歯状に交互に引き回されている。従って、データ線駆動回路の周囲で画像信号線やデータ線を規則正しく且つバランス良く配線することができる。

【００３８】請求項１５に記載の電気光学装置は請求項１４に記載の電気光学装置において、前記データ信号供給手段は、前記データ線毎に前記データ信号の電圧極性を反転し、前記第１画像信号線群に含まれる画像信号線と前記第２画像信号線群に含まれる画像信号線とは、相隣接する２本のデータ線に対応する２本の画像信号線を対にして前記データ線駆動回路の両側から櫛歯状に交互に引き回されていることを特徴とする。

【００３９】請求項１５に記載の電気光学装置によれば、データ信号供給手段により、データ線毎にデータ信号の電圧極性が反転され、所謂１Ｓ反転やドット反転といった反転駆動が行われ、表示画面上のフリッカが低減される。ここで、第１画像信号線群に含まれる画像信号線（例えば、相隣接する２本のデータ線に対応する２本おきの画像信号線ＶＩＤ１、２、５、６…）と第２画像信号線群に含まれる画像信号線（例えば、相隣接する２本のデータ線に対応する２本おきの画像信号線ＶＩＤ３、４、７、８…）とは、相隣接する２本のデータ線に対応する２本の画像信号線を対にしてデータ線駆動回路の両側から櫛歯状に交互に引き回されている。従って、相隣接する画像信号線には逆極性の画像信号が供給されることになり、同一のノイズ源に起因したノイズ成分については、これら両者間で打ち消し合う効果が働くので、ノイズを低減する上で有利である。

【００４０】請求項１６に記載の電子機器は、請求項１から１５に記載の電気光学装置を備えたことを特徴とする。

【００４１】請求項１６に記載の電子機器によれば、電子機器は、上述した本願発明の液晶装置を備えており、高周波のクロックノイズ等が低減されており、高品位の画像表示が可能となる。

【００４２】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにする。

【００４３】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて説明する。

【００４４】（液晶装置の構成）電気光学装置の一例として、液晶装置の実施の形態の構成について図１から図８に基づいて説明する。図１は、液晶装置の実施の形態におけるＴＦＴアレイ基板上に設けられた導電線（以下、シールド線と称す。）を含む各種配線、周辺回路等の構成を示す平面図であり、図２は、図１のシールド線のより詳細な２次元的レイアウトを示す平面図であり、図３（ａ）及び（ｂ）は夫々、シールド線、画像信号線及びクロック信号線等の配線を示す図２のＡ－Ａ’断面図及びＢ－Ｂ’断面図であり、図５は、図１の画素部分の拡大平面図であり、図６は、ＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図であり、図７は、対向基板を含めて示す図６のＨ－Ｈ’断面図である。図８は、図１の画像信号線の２次元的レイアウトの一例を示す概略平面図（図８（ａ））及び他の例を示す概略平面図（図８（ｂ））である。

【００４５】図１において、液晶装置２００は、例えば石英基板、ハードガラス等からなるＴＦＴアレイ基板１を備えている。ＴＦＴアレイ基板１上には、マトリクス状に設けられた複数の画素電極１１と、Ｘ方向に複数配列されており夫々がＹ方向に沿って伸びるデータ線３５と、Ｙ方向に複数配列されており夫々がＸ方向に沿って伸びる走査線３１と、各データ線３５と画素電極１１との間に夫々介在すると共に該間における導通状態及び非導通状態を、走査線３１を介して夫々供給される走査信号に応じて夫々制御するスイッチング素子の一例としての複数のＴＦＴ３０とが形成されている。またＴＦＴアレイ基板１上には、後述の蓄積容量（図９参照）のための配線である容量線３１’が、走査線３１に沿ってほぼ平行に形成されている。

【００４６】ＴＦＴアレイ基板１上には更に、データ信号供給手段の一例を構成するサンプリング回路３０１及びデータ線駆動回路１０１と、走査信号供給手段の一例を構成する走査線駆動回路１０４とが形成されている。また、複数の画素電極１１により規定される画面表示領域（即ち、実際に液晶の配向状態変化により画像が表示される液晶パネルの領域）の上辺には、画面表示領域の両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられており、画面表示領域の四隅には、ＴＦＴアレイ基板１と対向基板との間で電気的導通をとるための導通材からなる銀点１０６が設けられている。但し、上下導通箇所は少なくとも１カ所で良い。以下図１から図８の説明において、ＴＦＴアレイ基板１の下辺に沿って複数設けられた外部入力端子１０２を介して入力される信号名称と、その信号配線とは、説明の容易化のために同一のアルファベット記号を信号及び配線の後に夫々付加して参照する（例えば、信号名称である“クロック信号ＣＬＸ”に対し、その信号配線を“配線ＣＬＸ”と呼ぶ）ことにする。

【００４７】走査線駆動回路１０４は、外部制御回路から外部入力端子１０２並びに配線ＶＳＳＹ及びＶＤＤＹを介して供給される、走査線駆動回路１０４用の負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用いて、スタート信号ＤＹの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線ＣＬＹ及びＣＬＹ’を介して供給される、走査線駆動回路１０４の内蔵シフトレジスタ回路用の基準クロック信号ＣＬＹ及びその反転クロック信号ＣＬＹ’に基づく所定タイミングで、走査線３１に走査信号をパルス的に線順次で印加する。

【００４８】データ線駆動回路１０１は、外部制御回路から外部入力端子１０２並びに信号配線ＶＳＳＸ及びＶＤＤＸを介して供給される、データ線駆動回路用の負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用いて、スタート信号ＤＸの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線ＣＬＸ及びＣＬＸ’を介して供給される、データ線駆動回路１０１の内蔵シフトレジスタ回路用の基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＸ’に基づき、走査線駆動回路１０４が走査信号を印加するタイミングに合わせて、外部入力端子１０２及び配線ＶＩＤ１～ＶＩＤ１２を介して供給される例えば１２相展開された画像信号ＶＩＤ１～ＶＩＤ１２夫々について、データ線３５毎にサンプリング回路駆動信号をサンプリング回路３０１にサンプリング回路駆動信号線３０６を介して所定タイミングで供給する。

【００４９】サンプリング回路３０１は、ＴＦＴ３０２を各データ線３５毎に備えており、配線ＶＩＤ１～ＶＩＤ１２がＴＦＴ３０２のソース電極に接続されており、サンプリング回路駆動信号線３０６がＴＦＴ３０２のゲート電極に接続されている。そして、画像信号ＶＩＤ１～ＶＩＤ１２が入力されると、これらの画像信号をサンプリングする。また、サンプリング回路駆動信号線３０６を介して、データ線駆動回路１０１からサンプリング回路駆動信号が入力されると、画像信号ＶＩＤ１～ＶＩＤ１２夫々についてサンプリングされた画像信号を、１２本の隣接するデータ線３５からなるグループ毎に順次印加する。

【００５０】以上のように、データ線駆動回路１０１とサンプリング回路３０１とは、１２相展開された画像信号ＶＩＤ１～ＶＩＤ１２をデータ線３５にデータ信号として供給するように構成されている。本実施の形態では隣接する１２本のデータ線３５に接続されるサンプリング回路３０１を同時に選択し、１２本のデータ線３５からなるグループ毎に順次転送していく方式を述べたが、データ線３５を６本毎に選択してもよいし、２４本毎に選択してもよい。或いは、２本以上の任意の本数を同時に選択してもよい。また、サンプリング回路３０１のＴＦＴ３０２の能力が高ければ、データ線毎に順次に選択してもよい。この際、少なくとも画像信号の相展開数だけ、画像信号用の外部入力端子１０２及び画像信号線が必要なことは言うまでもない。本実施の形態では特に、以下に述べるようにデータ線駆動回路１０１の両側から配線ＶＩＤ１～ＶＩＤ１２が引き回されているので、この本数（相展開数）は多くてもＴＦＴアレイ基板１上にバランス良く配線できる。尚、画像信号の相展開数とサンプリング回路３０１を同時に選択する数が相等しくなるように構成してもよいし、前者が後者よりも多くなるように構成してもよい。

【００５１】図２に示すように、データ線駆動回路１０１は、スタート信号ＤＸが入力されると、基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＫ’に基づく転送信号の順次生成を開始するシフトレジスタ回路１０１ａと、シフトレジスタ回路１０１ａからの転送信号を波形整形しバッファリングした後、サンプリング回路駆動信号線３０６を介してサンプリング回路３０１に供給

する波形制御回路１０１ｂ及びバッファ回路１０１ｃとを備えている。また、サンプリング回路３０１は、１２相展開された画像信号ＶＩＤ１～ＶＩＤ１２に対応してＴＦＴ３０２が１２個ずつパラレルに各サンプリング回路駆動信号線３０６に接続されている。即ち、ＴＦＴ３０２から構成されるスイッチＳ１～Ｓ１２が左から１本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳ１３～Ｓ２４が左から２本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳｎ-11～Ｓｎが右端のサンプリング回路駆動信号線３０６に接続されている。図１では省略し図２で示したイネーブル信号ＥＮＢ１及びＥＮＢ２は、波形制御回路１０１ｂ内に設けられたイネーブル回路に入力される。このイネーブル回路では、シフトレジスタ回路１０１ａから順次出力されるパルスの幅を、イネーブル信号ＥＮＢ１及びＥＮＢ２のパルス幅に制限することにより、サンプリング回路３０１の選択期間を制御する。これにより、データ線１２本分ずつ離れて同一の配線（ＶＩＤ１～１２）から画像信号を受けるデータ線３５間におけるゴーストの発生を防止する。従って、イネーブル信号ＥＮＢ１及びＥＮＢ２は、クロック信号ＣＬＸ及びＣＬＸ’と同じく、水平走査期間よりも短い周期を持つ高周波制御信号に属する。他方、シフトレジスタ回路１０１ａに入力されるスタート信号ＤＸは、クロック信号ＣＬＹ及びＣＬＹ’や走査線駆動回路側のシフトレジスタに入力されるスタート信号ＤＹと同じく、水平走査期間よりも短くない周期を持つ低周波制御信号に属する。

【００５２】ここで、シフトレジスタ回路１０１ａの具体的な回路構成及び動作について図３を参照して説明する。尚、図３（ａ）は、イネーブル回路を含むシフトレジスタ回路を示す回路図であり、図３（ｂ）は、このシフトレジスタ回路における各種信号のタイミングチャートである。

【００５３】先ず、図３（ａ）において、シフトレジスタ回路１０１ａの各段の出力に対応してイネーブル回路１１２が夫々設けられている。シフトレジスタ回路１０１ａの各段は、右方向（左から右へ向かう方向）に対応する転送方向で各段から転送信号が順次出力されるように、所定周期の基準クロック信号ＣＬＸ及びその反転信号ＣＬＸ’の２値レベルが変化する毎に転送信号に帰還をかけて次段に転送する２つのクロックドインバータを夫々含んで構成されている。また、イネーブル回路１１２は、シフトレジスタ回路１０１ａの奇数段目から出力される転送信号のパルス幅を第１イネーブル信号ＥＮＢ１のパルス幅に制限すると共に偶数段目から出力される転送信号のパルス幅を第２イネーブル信号ＥＮＢ２のパルス幅に制限するように、転送信号とイネーブル信号ＥＮＢ１又はＥＮＢ２との排他的論理積をとるＮＡＮＤ回路と、その結果を反転させるインバータ回路とから構成されている。シフトレジスタ回路１０１ａには、転送信号の転送をスタートさせるための信号ＤＸが図中左側から入力される。

【００５４】図３（ｂ）のタイミングチャートに示すタイミングで、この信号ＤＸ、クロック信号ＣＬＸ及びその反転信号ＣＬＸ’と、第１及び第２イネーブル信号ＥＮＢ１及びＥＮＢ２とが入力されると、上述のように構成されたシフトレジスタ回路１０１ａからは、クロック信号ＣＬＸの半周期だけ順次遅れる転送信号が順次出力される。すると、イネーブル回路１１２により、この転送信号のパルス幅が信号ＥＮＢ１及びＥＮＢ２のパルス幅に制限されて、クロック信号ＣＬＸのパルス幅よりも幅の狭いパルスから夫々なるサンプリング回路駆動信号Ｑ１、Ｑ２、Ｑ３、…、Ｑｎ（但し、ｎは奇数）が、図２に示した波形制御回路１０１ｂ及びバッファ回路１０１ｃを介してサンプリング回路３０１に順次供給される。

【００５５】本実施の形態では特に、図１及び図２に示すように、ＴＦＴアレイ基板１には、負電源ＶＳＳＹ用の配線ＶＳＳＹを兼ねた定電位のシールド線８０、負電源ＶＳＳＸ用の配線ＶＳＳＸを兼ねた定電位のシールド線８０’、正電源ＶＤＤＸ用の配線ＶＤＤＸを兼ねた定電位のシールド線８２、及び正電源ＶＤＤＹ用の配線ＶＤＤＹを兼ねた定電位のシールド線８６が配線されている。これらのシールド線８０、８０’、８２及び８６により、画像信号線である配線ＶＩＤ１～ＶＩＤ１２は、配線ＣＬＸ及びＣＬＸ’並びに配線ＥＮＢ１及びＥＮＢ２から電気的にシールドされている。従って、クロック信号ＣＬＸの周波数が高い場合でも、高周波制御信号線である配線ＣＬＸ及びＣＬＸ’並びに配線ＥＮＢ１及びＥＮＢ２から配線ＶＩＤ１～ＶＩＤ１２への高周波のクロックノイズ等の飛び込みを低減できる。

【００５６】しかも、図１及び図２に示したように、第１画像信号線群の一例を構成する奇数番目の画像信号線ＶＩＤ１、３、５、７、９及び１１は、ＴＦＴアレイ基板１上をＸ方向に見てデータ線駆動回路１０１の右側へ引き回されており、第２画像信号線群の一例を構成する偶数番目の画像信号線ＶＩＤ２、４、６、８、１０及び１２は、ＴＦＴアレイ基板１上でデータ線駆動回路１０１の左側へ引き回されている。従って、例えば１２相展開というように比較的多相の相展開数を行うことにより、サンプリング回路３０１に供給される画像信号ＶＩＤ１～１２の周波数を下げつつ、多数の配線ＶＩＤ１～１２については、データ線駆動回路１０１の両側にバランス良く配置できる。この結果、サンプリング回路３０１及びデータ線駆動回路１０１からなるデータ信号供給手段を形成する領域をＴＦＴアレイ基板１上に容易に確保することができる。従って、限られた基板サイズにおける画面の大型化が図られる。

【００５７】本実施の形態では特に、図２に示したように、定電位のシールド線８０’により、画像信号線たる

配線ＶＩＤ１～１２は、前述の高周波制御信号に属するクロック信号ＣＬＸ及びＣＬＸ’並びにイネーブル信号ＥＮＢ１及びＥＮＢ２を供給する高周波制御信号線たる配線ＣＬＸ及びＣＬＸ’並びに配線ＥＮＢ１及びＥＮＢ２から電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、これらの高周波制御信号線から配線ＶＩＤ１～１２への高周波のクロックノイズ等の飛び込みを低減できる。他方、前述の低周波制御信号に属するスタート信号ＤＸ及びＤＹ、並びにクロック信号ＣＬＹ及びＣＬＹ’については、配線ＶＩＤ１～１２上の画像信号や、これに基づいて供給されたデータ線３５上のデータ信号中の高周波ノイズの原因とはならない。このため、低周波制御信号線たる配線ＤＸ、ＤＹ、ＣＬＹ及びＣＬＹ’は、定電位のシールド線によりシールドしてもよく、シールドしなくてもよい。本実施の形態では、図２に示したように、右側では配線ＶＩＤ１、３、…、１１は、定電位の配線ＶＤＤＹからなるシールド線８６により配線ＤＹ、ＣＬＹ及びＣＬＹ’からシールドされており、左側では配線ＶＩＤ２、４、…、１２は定電位の配線ＶＳＳＹからなるシールド線８０により配線ＤＹからシールドされている。また、配線ＤＸからは、シールド線８０’により配線ＶＩＤ１～１２はシールドされている。

【００５８】更に本実施の形態では特に、右側（奇数番目）の画像信号線群の中で高周波制御信号線たる配線ＣＬＸ及びＣＬＸ’に近い側に位置する配線ＶＩＤ１１は、配線ＶＳＳＸ及びＶＤＤＸから夫々なる２本のシールド線８０’及び８２の存在により、これらの配線ＣＬＸ及びＣＬＸ’から離間されており、且つ電気的にシールドされている。また、左側（偶数番目）の画像信号線群の中で高周波制御信号線たる配線ＣＬＸ及びＣＬＸ’に近い側に位置する配線ＶＩＤ１２は、配線ＶＳＳＸからなる１本のシールド線８０’及び低周波制御信号線たる配線ＤＸの存在により、これらの配線ＣＬＸ及びＣＬＸ’から離間されており、且つ電気的にシールドされている。即ち、画像信号やデータ信号中の高周波ノイズの原因とはならない低周波制御信号線に属する配線ＤＸを、高周波制御信号線たる配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１２との間に、シールド線８０’と共に配置することにより、配線ＣＬＸ及びＣＬＸ’のＶＩＤ１２に対するクロックノイズ等の悪影響を更に低減できる。一般に距離及び障害物の介在に応じて電磁波は減少するので、配線ＣＬＸ及びＣＬＸ’や配線ＥＮＢ１及びＥＮＢ２と配線ＶＩＤ１～１２との間にシールド線（配線８０、８０’、８２、８６等の定電位の配線）や低周波制御信号線（配線ＤＸ、ＤＹ、ＣＬＹ、ＣＬＹ’等の低周波制御信号が供給される配線）をなるべく多く配線する構成により、クロックノイズを発生させる電磁波が減少して、クロックノイズ等が低減する。このように、シールド線以外に低周波制御信号線を高周波制御信号線と画像信号線との間に介在させることはＴＦＴ基板１上スペースの有効利用及びノイズ低減の観点から見て有利である。

【００５９】また図２に示したように本実施の形態では、ＴＦＴアレイ基板１の周辺部上において、配線ＶＩＤ１～１２に夫々接続された外部入力端子１０２は両側に配置されており、その間に配線ＥＮＢ１、ＥＮＢ２、ＣＬＸ’及びＣＬＸに接続された外部入力端子１０２が集中配置されている。そして、配線ＶＩＤ１２に接続された外部入力端子１０２と配線ＥＮＢ１に接続された外部入力端子１０２との間に、シールド線８０’（配線ＶＳＳＸ）に接続された外部入力端子１０２が配置されている。また、配線ＶＩＤ１１に接続された外部入力端子１０２と配線ＣＬＸに接続された外部入力端子１０２との間に、シールド線８０’（配線ＶＳＳＸ）に接続された外部入力端子１０２が配置されている。従って、配線ＶＩＤ１～１２と配線ＥＮＢ１、ＥＮＢ２、ＣＬＸ’及びＣＬＸとの間にシールド線８０’を配線する構成を容易に得ることができる。特に、液晶装置２００に入力される前段階で、例えば、表示情報処理回路等の外部回路から液晶装置２００への配線中で、クロック信号ＣＬＸ等が、画像信号ＶＩＤ１～１２に対しクロックノイズ等を発生させてしまう事態を効果的に阻止し得る。このように本実施の形態によれば、液晶装置２００に入力される前後において、クロック信号用の配線から画像信号用の配線への高周波のクロックノイズの飛び込み等を低減できる。尚、より好ましくは、ＴＦＴアレイ基板１の周辺部において外部入力端子１０２を形成可能な領域において、配線ＶＩＤ１～１２用の外部入力端子１０２を可能な限り両側（右側及び左側）に寄せて配置すると共に、中央に集中配置される配線ＣＬＸ’等用の外部入力端子１０２との間に可能な限り間隔を空けて、この間隔にシールド線８０’等用の外部入力端子１０２を配置する。

【００６０】本実施の形態では、配線ＶＳＳＹ、ＶＳＳＸ、ＶＤＤＸ及びＶＳＳＹを夫々延設してシールド線８０、８０’、８２及び８６とすることにより、外部入力端子や配線を共用することが可能となり、装置構成の簡略化と省スペース化を図ることが出来る。また、シールド線８０、８０’、８２及び８６の電位は、このように定電位線との共用化により、容易に定電位とされる。但し、電源用の配線とシールド線を別個に配線してもよい。

【００６１】本実施の形態では、図２に示すように、負電源ＶＳＳＸが入力される外部入力端子１０２が２つ設けられている。そして、配線ＶＩＤ１～ＶＩＤ１２は、負電源ＶＳＳＸの電位（負電位）とされたシールド線８０’により、ＴＦＴアレイ基板１上で囲まれている。特に、シフトレジスタ回路１０１ａと波形制御回路１０１ｂとの間にも、データ線３５と同じＡｌ等の金属層から

形成されたシールド線８０’は延設されている。そして、延設されたシールド線８０’の先端部は、後述のように第１層間絶縁層を介してＡｌ等の金属層の下方において、例えば走査線３１と同じポリシリコン等の導電性層から形成されたシールド線接続部８１を介して、波形制御回路１０１ｂ及びバッファ回路１０１ｃを囲むようにしてシールド線８０’に接続されている。

【００６２】他方、図２に示すように、配線ＣＬＸ及びＣＬＸ’は、データ線駆動回路１０１に隣接する部分においては、正電源ＶＤＤＸの電位（正電位）とされたシールド線８２により、ＴＦＴアレイ基板１上で囲まれている。特に、波形制御回路１０１ｂとバッファ回路１０１ｃとの間にも、データ線３５と同じＡｌ等の金属層から形成されたシールド線８２は延設されており、その先端部は、例えば走査線３１と同じポリシリコン等の導電性層から形成されたシールド線接続部８３を介して波形制御回路１０１ｂ及びシフトレジスタ回路１０１ａを囲むようにしてシールド線８２に接続されている。

【００６３】従って、配線ＶＩＤ１～ＶＩＤ１２は、ＴＦＴアレイ基板１上で配線ＣＬＸ及びＣＬＸ’並びに配線ＥＮＢ１及びＥＮＢ２から２重にシールドされた構成が採られており、シフトレジスタ回路１０１ａ並びに波形制御回路１０１ｂ及びバッファ回路１０１ｃに対するシールドも信頼性が高いものとされている。但し、このように囲む構成を採らなくても、配線ＣＬＸ、ＣＬＸ’、ＥＮＢ１及びＥＮＢ２と配線ＶＩＤ１～ＶＩＤ１２との間にシールド線８０、８０’、８２及び８６が少なくとも一本介在するように構成すれば、シールドの効果は多少なりとも得られる。

【００６４】本実施の形態では図１及び図２に示したように、シールド線８０により、画面表示領域及び複数のデータ線３５は、ＴＦＴアレイ基板１上で囲まれている。このため、当該画面表示領域及び複数のデータ線３５も、配線ＣＬＸ、ＣＬＸ’、ＥＮＢ１及びＥＮＢ２からシールドされている。従って、データ線駆動回路１０１から出力されたサンプリング回路駆動信号、ＴＦＴ３０や画素電極１１に到達したデータ信号等における、高周波のクロックノイズの発生等を低減できる。但し、このように画面表示領域までも囲む構成を採らなくても、サンプリング回路３０１に至るまでの配線ＶＩＤ１～ＶＩＤ６をシールド線８０、８０’、８２又は８６によりシールドするように構成すれば、シールドの効果は多少なりとも得られる。この場合図１から分かるように、シールド線８０は、配線ＶＳＳＹから延設されており、画面表示領域の両側に設けられた走査線駆動回路１０４に電源信号ＶＳＳＹを冗長的に供給するように延設されている。このため、たとえ、シールド線８０或いは配線ＶＳＳＹに断線が生じても、装置欠陥になり難いので有利である。

【００６５】図４（ａ）及び（ｂ）の断面図に夫々示すように、外部入力端子１０２に接続された各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸは、例えば、Ａｌ（アルミニウム）等の、データ線３５と同一の低抵抗金属材料から形成されている。従って、シールド線８０（配線ＶＳＳＹ）、８０’（配線ＶＳＳＸ）、８２（配線ＶＤＤＸ）及び８６（配線ＶＤＤＹ）の引き回し領域が、たとえ長くても、各シールド線８０、８０’、８２及び８６の抵抗は実用上十分に低く抑えられる。即ち、図２に示したように、他の各種配線やシフトレジスタ回路１０１ａ並びに波形制御回路１０１ｂ及びバッファ回路１０１ｃの隙間を縫ってジグザグにシールド線８２や８０’を長く配線でき、更に画面表示領域までも含めた広い領域にシールド線８０を長く配線できる。このように比較的簡単な構成により、当該シールドの効果を全体として高めることが出来る。また図４（ａ）及び（ｂ）に示すように、各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸは、ＴＦＴアレイ基板１に形成された第１層間絶縁層４２上に、即ち同一層上に形成されている。従って、シールドの効果がより効率良く発揮される。更に、このように構成すると、液晶装置２００の製造プロセスにおいて、各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸを、例えば、Ａｌ層等の同一の低抵抗金属層から同一工程により一括して形成できるので、製造上有利である。

【００６６】尚、図１から図４に示した外部入力端子１０２から入力される信号ＬＣＣＯＭは、共通電極の電源信号であり、配線ＬＣＣＯＭ及び前述の銀点１０６を介して、後述の対向基板に設けられた共通電極（図９参照）に供給される。

【００６７】ここで図５の平面図に示すように、容量線３１’は、ＴＦＴアレイ基板１上において走査線３１（ゲート電極）と平行に、例えば走査線３１と同じく導電性のポリシリコン層等から形成されており、シールド線８０にコンタクトホール８０ａを介して接続されている。このように構成すれば、容量線３１’を定電位とするための配線をシールド線８０で兼用でき、容量線３１’を定電位にするために必要な外部入力端子も、シールド線８０用の外部入力端子１０２で兼用できる。

【００６８】本実施の形態では特に、サンプリング回路３０１は、図１中斜線領域で示すように且つ図６及び図７に示すように、対向基板２に形成された遮光性の周辺見切り５３に対向する位置においてＴＦＴアレイ基板１上に設けられており、データ線駆動回路１０１及び走査線駆動回路１０４は、液晶層５０に面しないＴＦＴアレイ基板１の狭く細長い周辺部分上に設けられている。ＴＦＴアレイ基板１の上には、画面表示領域の周囲において両基板を貼り合わせて液晶層５０を包囲するシール部材の一例としての光硬化性樹脂からなるシール材５２が、画面表示領域に沿って設けられている。そして、対向基板２上における画面表示領域とシール材５２との間には、遮光性の周辺見切り５３が設けられている。

【００６９】周辺見切り５３は、後に画面表示領域に対応して開口部が設けられた遮光性のケースにＴＦＴアレイ基板１が入れられた場合に、当該画面表示領域が製造誤差等により当該ケースの開口の縁に隠れてしまわないように、即ち、例えばＴＦＴアレイ基板１のケースに対する数百μｍ程度のずれを許容するように、画面表示領域の周囲に少なくとも５００μｍ以上の幅を持つ帯状の遮光性材料から形成されたものである。このような遮光性の周辺見切り５３は、例えば、Ｃｒ（クロム）、Ｎｉ（ニッケル）、Ａｌ（アルミニウム）等の金属材料を用いたスパッタリング、フォトリソグラフィ工程及びエッチング工程等により対向基板２に形成される。或いは、カーボンやＴｉ（チタン）をフォトレジストに分散した樹脂ブラックなどの材料から形成される。また、ＴＦＴアレイ基板１上に遮光性の周辺見切り５３を設けてもよい。周辺見切り５３をＴＦＴアレイ基板１上に内蔵すれば、ＴＦＴアレイ基板１と対向基板２との貼り合わせ工程での精度のばらつきで画素の開口領域が影響を受けることがないため、液晶パネルの透過率を高精度に維持することができる。

【００７０】シール材５２の外側の領域には、画面表示領域の下辺に沿ってデータ線駆動回路１０１及び外部入力端子（実装端子）１０２が設けられており、画面表示領域の左右の２辺に沿って走査線駆動回路１０４が画面表示領域の両側に設けられている。そして、シール材５２とほぼ同じ輪郭を持つ対向基板２が当該シール材５２によりＴＦＴアレイ基板１に固着されている。

【００７１】以上のようにシールド線８０及びサンプリング回路３０１は、ＴＦＴアレイ基板１上の周辺見切り５３の下に設けられているので、ＴＦＴアレイ基板１上の省スペース化が図られ、例えば、走査線駆動回路１０４やデータ線駆動回路１０１をＴＦＴアレイ基板１の周辺部分に余裕を持って形成することができ、シールド線８０の形成により液晶装置２００における有効表示面積が減少することも殆ど又は全くない。

【００７２】図８（ａ）に、図１及び図２に示した走査線駆動回路１０１とサンプリング回路３０１との間における配線ＶＩＤ１～１２の引き回し方式を拡大して示す。同図において、奇数番目の画像信号線たる配線ＶＩＤ１、…、１１と偶数番目の画像信号たる配線ＶＩＤ２、…、１２とは、各配線毎に両側から櫛歯状に交互に引き回されている。従って、データ線駆動回路１０１の周囲において、配線ＶＩＤ１～１２及びサンプリング回路駆動信号線３０６は、大変規則性良く且つバランス良く配線さている。

【００７３】ところで、本実施の形態では、液晶を直流駆動により劣化させないためや表示画面上のフリッカを防止するため等に、液晶駆動電圧を反転させる各種の方式、例えば、フィールド又はフレーム反転駆動、走査線反転駆動（所謂１Ｈ反転駆動）、データ線反転駆動（所謂１Ｓ反転駆動）、ドット反転駆動などを採用可能である。ここで特に、１Ｓ反転やドット反転といった相隣接するデータ線間で電圧極性を反転させて液晶駆動を行う場合には、図８（ａ）に示したように一本の配線ＶＩＤ１～１２毎に櫛歯状にするよりも、図８（ｂ）に示すように、相隣接する２本のデータ線３５に対応する２本の配線ＶＩＤ１及び２、５及び６等を夫々一対として２本おきに一方の側（例えば右側）から引き回すと共に、それら以外の相隣接する２本のデータ線３５に対応する２本の配線ＶＩＤ３及び４、７及び８等を夫々一対として２本おきに逆側（例えば左側）から引き回すと共に、データ線駆動回路１０１とサンプリング回路３０１の間で２本の配線を一対として夫々両側から櫛歯状にするのがより好ましい。このように配線すれば、ＴＦＴアレイ基板１上で相隣接する各対の配線１及び２、３及び４、…から供給される画像信号は夫々逆極性とされてデータ線３５に供給されるので、これらの信号中に存在する同一のノイズ源に起因したノイズ成分については、これら各対をなす両者間で打ち消し合う効果が働くので、ノイズを低減するのに役立つ。

【００７４】（液晶パネル部分の構成）次に、液晶装置２００が含む液晶パネル部分の具体的構成について図９及び図１０を参照して説明する。ここに、図９は液晶パネルのＴＦＴ３０部分における断面図であり、図１０は周辺見切りの下における液晶パネルのシールド線８０に沿った断面図である。尚、図９及び図１０においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００７５】図９の断面図において、液晶パネル１０は、各画素に設けられるＴＦＴ３０部分において、ＴＦＴアレイ基板１並びにその上に積層された半導体層３２、ゲート絶縁層３３、走査線３１（ゲート電極）、第１層間絶縁層４２、データ線３５（ソース電極）、第２層間絶縁層４３、画素電極１１及び配向膜１２を備えている。液晶パネル１０はまた、例えばガラス基板から成る対向基板２並びにその上に積層された共通電極２１、配向膜２２及び遮光層２３を備えている。液晶パネル１０は更に、これらの両基板間に挟持された液晶層５０を備えている。

【００７６】ここでは先ず、これらの層のうち、ＴＦＴ３０を除く各層の構成について順に説明する。

【００７７】第１及び第２層間絶縁層４２及び４３は夫々、５０００～１５０００Å程度の厚みを持つＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる。尚、ＴＦＴアレイ基板１上に、ＴＦＴ３０の下地となる層間絶縁層をシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等から形成してもよい。

【００７８】画素電極１１は例えば、ＩＴＯ膜（Ｉｎｄｉｕｍ Ｔｉｎ Ｏｘｉｄｅ膜）などの透明導電性薄膜

からなる。このような画素電極１１は、スパッタリング処理等によりＩＴＯ膜等を約５００～２０００Åの厚さに堆積した後、フォトリソグラフィ工程、エッチング工程を施すこと等により形成される。尚、当該液晶パネル１０を反射型の液晶装置に用いる場合には、Ａｌ等の反射率の高い不透明な材料から画素電極１１を形成してもよい。

【００７９】配向膜１２は例えば、ポリイミド薄膜などの有機薄膜からなる。このような配向膜１２は、例えばポリイミド系の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により形成される。

【００８０】共通電極２１は、対向基板２の全面に渡って形成されている。このような共通電極２１は、例えばスパッタリング処理等によりＩＴＯ膜等を約５００～２０００Åの厚さに堆積して形成される。

【００８１】配向膜２２は、例えば、ポリイミド薄膜などの有機薄膜からなる。このような配向膜２２は、例えばポリイミド系の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により形成される。

【００８２】遮光層２３は、ＴＦＴ３０に対向する所定領域に設けられている。このような遮光層２３は、前述の周辺見切り５３同様に、ＣｒやＮｉなどの金属材料を用いたスパッタリング、フォトリソグラフィ及びエッチング等の工程により形成されたり、カーボンやＴｉをフォトレジストに分散した樹脂ブラックなどの材料から形成される。遮光層２３は、ＴＦＴ３０の半導体層（ポリシリコン膜）３２に対する遮光の他に、コントラストの向上、色材の混色防止などの機能を有する。

【００８３】液晶層５０は、画素電極１１と共通電極２１とが対面するように配置されたＴＦＴアレイ基板１と対向基板２との間において、シール材５２（図６及び図７参照）により囲まれた空間に液晶が真空吸引等により封入されることにより形成される。液晶層５０は、画素電極１１からの電界が印加されていない状態で配向膜１２及び２２により所定の配向状態を採る。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、二つの基板１及び２をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのスペーサが混入されている。

【００８４】次に、ＴＦＴ３０に係る各層の構成について順に説明する。

【００８５】ＴＦＴ３０は、走査線３１（ゲート電極）、走査線３１からの電界によりチャネルが形成される半導体層３２、走査線３１と半導体層３２とを絶縁するゲート絶縁層３３、半導体層３２に形成されたソース領域３４、データ線３５（ソース電極）、及び半導体層３２に形成されたドレイン領域３６を備えている。ドレイン領域３６には、複数の画素電極１１のうちの対応する一つが接続されている。ソース領域３４及びドレイン領域３６は後述のように、半導体層３２に対し、ｎ型又はｐ型のチャネルを形成するかに応じて所定濃度のＮ型用又はＰ型用のドーパントをドープすることにより形成されている。Ｎ型チャネルのＴＦＴは、動作速度が速いという利点があり、画素のスイッチング素子であるＴＦＴ３０として用いられることが多い。

【００８６】ＴＦＴ３０を構成する半導体層３２は、例えば、ＴＦＴアレイ基板１上にａ－Ｓｉ（アモルファスシリコン）膜を形成後、アニール処理を施して約５００～２０００Åの厚さに固相成長させることにより形成する。この際、Ｎチャネル型のＴＦＴ３０の場合には、Ｓｂ（アンチモン）、Ａｓ（砒素）、Ｐ（リン）などのＶ族元素のドーパントを用いたイオン注入等によりドープしてもよい。また、ｐチャネル型のＴＦＴ３０の場合には、Ｂ（ボロン）、Ｇａ（ガリウム）、Ｉｎ（インジウム）などのIII族元素のドーパントを用いたイオン注入等によりドープする。特にＴＦＴ３０をＬＤＤ（Ｌｉｇｈｔｌｙ　Ｄｏｐｅｄ　Ｄｒａｉｎ）構造を持つＮチャネル型のＴＦＴとする場合、Ｐ型の半導体層３２に、ソース領域３４及びドレイン領域３６のうちチャネル側に夫々隣接する一部にＰなどのＶ族元素のドーパントにより低濃度ドープ領域を形成し、同じくＰなどのＶ族元素のドーパントにより高濃度ドープ領域を形成する。また、Ｐチャネル型のＴＦＴ３０とする場合、Ｎ型の半導体層３２に、 Ｂなどの III族元素のドーパントを用いてソース領域３４及びドレイン領域３６を形成する。このようにＬＤＤ構造とした場合、ショートチャネル効果を低減できる利点が得られる。尚、ＴＦＴ３０は、ＬＤＤ構造における低濃度ドープ領域にイオン注入したオフセット構造のＴＦＴとしてもよいし、ゲート電極をマスクとして高濃度の不純物イオンをドープすることにより自己整合的に高濃度なソース及びドレイン領域を形成するセルフアライン型のＴＦＴとしてもよい。

【００８７】また本実施の形態では、図９において、ＴＦＴ３０のソース・ドレイン間に、ゲート絶縁膜２を介して、同一の走査信号が供給される２つのゲート電極３１を設けて、デユアルゲート（ダブルゲート）構造のＴＦＴとしてもよい。これにより、ＴＦＴ３０のリーク電流を低減することができる。また、デユアルゲート構造のＴＦＴを、上述のＬＤＤ構造、或いはオフセット構造を持つようにすれば、更にＴＦＴ３０のリーク電流を低減することができ、高いコントラスト比を実現することができる。また、デユアルゲート構造により、冗長性を持たすことができ、大幅に画素欠陥を低減できるだけでなく、高温動作時でも、リーク電流が低いため、高コントラスト比の画質を実現することができる。尚、ＴＦＴ３０のソース・ドレイン間に設けるゲート電極３１は３つ以上でもよいことは言うまでもない。

【００８８】ゲート絶縁層３３は、半導体層３２を約９００～１３００℃の温度により熱酸化することにより、３００～１５００Å程度の比較的薄い厚さの熱酸化膜を形成して得る。

【００８９】走査線３１（ゲート電極）は、減圧ＣＶＤ法等によりポリシリコン膜を堆積した後、フォトリソグラフィ工程、エッチング工程等により形成される。或いは、Ｗ（タングステン）、Ｍｏ（モリブデン）等の高融点金属膜又は金属シリサイド膜から形成されてもよい。この場合、走査線３１（ゲート電極）を、遮光層２３が覆う領域の一部又は全部に対応する遮光膜として配置すれば、金属膜や金属シリサイド膜の持つ遮光性により、遮光層２３の一部又は全部を省略することも可能となる。この場合特に、対向基板２とＴＦＴアレイ基板１との貼り合わせずれによる画素開口率の低下を防ぐことが出来る利点がある。

【００９０】データ線３５（ソース電極）は、画素電極１１と同様にＩＴＯ膜等の透明導電性薄膜から形成してもよい。或いは、スパッタリング処理等により、約１０００～５０００Åの厚さに堆積されたＡｌ等の低抵抗金属や金属シリサイド等から形成してもよい。

【００９１】また、第１層間絶縁層４２には、ソース領域３４へ通じるコンタクトホール３７及びドレイン領域３６へ通じるコンタクトホール３８が夫々形成されている。このソース領域３４へのコンタクトホール３７を介して、データ線３５（ソース電極）はソース領域３４に電気的接続される。更に、第２層間絶縁層４３には、ドレイン領域３６へのコンタクトホール３８が形成されている。このドレイン領域３６へのコンタクトホール３８を介して、画素電極１１はドレイン領域３６に電気的接続される。前述の画素電極１１は、このように構成された第２層間絶縁層４３の上面に設けられている。各コンタクトホールは、例えば、反応性エッチング、反応性イオンビームエッチング等のドライエッチングにより形成される。

【００９２】尚、一般にはチャネルが形成される半導体層３２は、光が入射すると光電変換効果により光電流が発生してしまいＴＦＴ３０のトランジスタ特性が劣化するが、本実施の形態では、対向基板２には各ＴＦＴ３０に夫々対向する位置に遮光層２３が形成されているので、入射光が半導体層３２に入射することが防止される。更にこれに加えて又は代えて、ゲート電極を上側から覆うようにデータ線３５（ソース電極）をＡｌ等の不透明な金属薄膜から形成すれば、遮光層２３と共に又は単独で、半導体層３２への入射光（即ち、図９で上側からの光）の入射を効果的に防ぐことが出来る。

【００９３】図９において、画素電極１１には蓄積容量７０が夫々設けられている。この蓄積容量７０は、より具体的には、半導体層３２と同一工程により形成される第１蓄積容量電極層３２’、ゲート絶縁層３３と同一工程により形成される絶縁層３３’、走査線３１と同一工程により形成される容量線３１’（第２蓄積容量電極）、第１及び第２層間絶縁層４２及び４３、並びに第１及び第２層間絶縁層４２及び４３を介して容量線３１’に対向する画素電極１１の一部から構成されている。このように蓄積容量７０が設けられているため、デューティー比が小さくても高精細な表示が可能とされる。

【００９４】図１０の断面図に示すように、周辺見切り５３に対向し且つ複数の走査線３１の上方の位置において第１層間絶縁層４２上をシールド線８０は通過する。そして、このシールド線８０は、その殆どの部分が、前述したデータ線（ソース電極）３５と同一工程で形成されたＡｌ等の金属薄膜からなる低抵抗な配線である。このように液晶装置２００の製造プロセスにおいて、シールド線８０とデータ線３５とを一括して形成できるので、製造上有利である。

【００９５】本実施の形態では特に、ＴＦＴ３０はポリシリコンタイプのＴＦＴであるので、ＴＦＴ３０の形成時に同一薄膜形成工程で、サンプリング回路３０１、データ線駆動回路１０１、走査線駆動回路１０４等の同じくポリシリコンＴＦＴタイプのＴＦＴ３０２等から構成された周辺回路を形成できるので製造上有利である。例えば、これらの周辺回路は、Ｎチャネル型ポリシリコンＴＦＴ及びＰチャネル型ポリシリコンＴＦＴから構成される相補構造の複数のＴＦＴからＴＦＴアレイ基板１上の周辺部分に形成される。

【００９６】尚、図９及び図１０には示されていないが、液晶パネル１０においては、対向基板２の投射光が入射する側及びＴＦＴアレイ基板１の投射光が出射する側には夫々、例えば、ＴＮ（ツイステッドネマティック）モード、ＳＴＮ（スーパーＴＮ）モード、Ｄ－ＳＴＮ（ダブルーＳＴＮ）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【００９７】また、以上説明した液晶パネル１０は、カラー液晶プロジェクタに適用されるため、３つの液晶パネル１０がＲＧＢ用のライトバルブとして夫々用いられ、各パネルには夫々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が入射光として夫々入射されることになる。従って、各実施の形態では、対向基板２に、カラーフィルタは設けられていない。しかしながら、液晶パネル１０においても遮光層２３の形成されていない画素電極１１に対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２上に形成してもよい。このようにすれば、液晶プロジェクタ以外の直視型や反射型のカラー液晶テレビなどのカラー液晶装置に本実施の形態の液晶パネルを適用できる。更に、対向基板２上に１画素1個対応するようにマイクロ

レンズを形成してもよい。このようにすれば、入射光の集光効率を向上することで、明るい液晶パネルが実現できる。更にまた、対向基板２上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー液晶パネルが実現できる。

【００９８】液晶パネル１０において、ＴＦＴアレイ基板１側における液晶分子の配向不良を抑制するために、第２層間絶縁層４３の上に更に平坦化膜をスピンコート等で塗布してもよく、又はＣＭＰ処理を施してもよい。或いは、第２層間絶縁層４３を平坦化膜で形成してもよい。

【００９９】液晶パネル１０のスイッチング素子は、正スタガ型又はコプラナー型のポリシリコンＴＦＴであるとして説明したが、逆スタガ型のＴＦＴやアモルファスシリコンＴＦＴ等の他の形式のＴＦＴに対しても、本実施の形態は有効である。

【０１００】液晶パネル１０においては、一例として液晶層５０をネマティック液晶から構成したが、液晶を高分子中に微小粒として分散させた高分子分散型液晶を用いれば、配向膜１２及び２２、並びに前述の偏光フィルム、偏光板等が不要となり、光利用効率が高まることによる液晶パネルの高輝度化や低消費電力化の利点が得られる。更に、画素電極１１をＡｌ等の反射率の高い金属膜から構成することにより、液晶パネル１０を反射型液晶装置に適用する場合には、電圧無印加状態で液晶分子がほぼ垂直配向されたＳＨ（スーパーホメオトロピック）型液晶などを用いても良い。更にまた、液晶パネル１０においては、液晶層５０に対し垂直な電界（縦電界）を印加するように対向基板２の側に共通電極２１を設けているが、液晶層５０に平行な電界（横電界）を印加するように一対の横電界発生用の電極から画素電極１１を夫々構成する（即ち、対向基板２の側には縦電界発生用の電極を設けることなく、ＴＦＴアレイ基板１の側に横電界発生用の電極を設ける）ことも可能である。このように横電界を用いると、縦電界を用いた場合よりも視野角を広げる上で有利である。その他、各種の液晶材料（液晶層）、動作モード、液晶配列、駆動方法等に本実施の形態を適用することが可能である。

【０１０１】以上説明した実施の形態において更に、周辺見切り５３下やＴＦＴアレイ基板１の周辺部に、プリチャージ回路、検査回路等の周知の周辺回路を設けてもよい。プリチャージ回路は、コントラスト比の向上、データ線の電位レベルの安定、表示画面上のラインむらの低減等を目的として、データ線に対し、データ線駆動回路から供給されるデータ信号に先行するタイミングで、プリチャージ信号を供給することにより、データ信号をデータ線に書き込む際の負荷を軽減する回路である。例えば、特開平７－２９５５２０号公報に、このようなプリチャージ回路の一例が開示されている。他方、検査回路は、周辺見切り５３下やＴＦＴアレイ基板の周辺部に、製造途中や出荷時の当該液晶装置の品質、欠陥等を検査するための回路である。

【０１０２】また、以上の実施の形態において、特開平９－１２７４９７号公報、特公平３－５２６１１号公報、特開平３－１２５１２３号公報、特開平８－１７１１０１号公報等に開示されているように、ＴＦＴアレイ基板１上においてＴＦＴ３０に対向する位置（即ち、ＴＦＴ３０の下側）にも、例えばＷ（タングステン）、Ｍｏ（モリブデン）等の高融点金属や金属シリサイドからなる遮光層を設けてもよい。このようにＴＦＴ３０の下側にも遮光層を設ければ、ＴＦＴアレイ基板１の側からの戻り光等がＴＦＴ３０に入射するのを未然に防ぐことができる。従って、当該液晶装置２００を液晶プロジェクタ用のライトバルブとして好適に用いることが出来る。

【０１０３】更にまた、以上の実施の形態において、ＴＦＴ３０に代えてＭＩＭ（Metal Insulator Metal）等の２端子型非線形素子等からスイッチング素子を構成してもよい。この場合、データ線及び走査線のうち一方の線を対向基板に配置して対向電極として機能させ、ＴＦＴアレイ基板に設けられた他方の線と画素電極との間にスイッチング素子を夫々配置して液晶駆動する。このように構成しても、画素信号線やデータ線をクロック信号線からシールドすることにより、高周波のクロックノイズの画像信号やデータ信号への飛び込みを防止する効果は発揮される。

【０１０４】（液晶装置の動作）次に、以上のように構成された液晶装置２００の動作について図１を参照して説明する。

【０１０５】先ず、走査線駆動回路１０４は、所定タイミングで走査線３１に走査信号をパルス的に線順次で印加する。

【０１０６】これと並行して、１２本の配線ＶＩＤ１～ＶＩＤ１２からパラレルな画像信号を受けると、サンプリング回路３０１は、これらの画像信号をサンプリングする。データ線駆動回路１０１は、走査線駆動回路１０４がゲート電圧を印加するタイミングに合わせて、１２本の配線ＶＩＤ１～ＶＩＤ１２夫々について一つのデータ線毎にサンプリング回路駆動信号を供給して、サンプリング回路３０１のＴＦＴ３０２をオン状態とする。これにより、隣接する１２本のデータ線３５に対して、サンプリング回路３０１にサンプリングされたデータ信号を順次印加する。即ち、データ線駆動回路１０１とサンプリング回路３０１により、配線ＶＩＤ１～ＶＩＤ１２から入力された１２相展開されたパラレルな画像信号ＶＩＤ１～ＶＩＤ１２は、データ線３５に供給される。

【０１０７】このように、走査信号（ゲート電圧）及びデータ信号（ソース電圧）の両方が印加されたＴＦＴ３

０においては、ソース領域３４、半導体層３２に形成されたチャネル及びドレイン領域３６を介して画素電極１１に電圧が印加される。そして、この画素電極１１の電圧は、ソース電圧が印加された時間よりも例えば３桁も長い時間だけ蓄積容量（図９参照）により保持される。ここで特に、シールド線８０、８０’、８２及び８６により、配線ＶＩＤ１～ＶＩＤ１２は、配線ＣＬＸ及びＣＬＸ’並びに配線ＥＮＢ１及びＥＮＢ２からシールドされているので、クロック信号ＣＬＸの周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’並びに配線ＥＮＢ１及びＥＮＢ２から配線ＶＩＤ１～ＶＩＤ１２への高周波のクロックノイズ等の飛び込みを低減できる。

【０１０８】以上のように、画素電極１１に電圧が印加されると、液晶層５０におけるこの画素電極１１と共通電極２１とに挟まれた部分における液晶の配向状態が変化し、ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として液晶パネル１０からは画像信号に応じたコントラストを持つ光が出射する。

【０１０９】以上の結果、表示すべき画像の解像度が高く、高周波のシリアルな画像信号ＶＩＤ１～ＶＩＤ１２が入力される場合にも、これに対応して周波数が高いクロック信号ＣＬＸを用いつつ、高周波のクロックノイズの発生により画質が劣化することは殆ど又は全く無くなり、高品位の画像表示が可能とされる。しかも、１２相展開という比較的多数の相に相展開した結果、画像信号の周波数を落とすことにより、通常性能のサンプリング回路によりサンプリングを行うことが可能とされている。

【０１１０】（電子機器）次に、以上詳細に説明した液晶装置２００を備えた電子機器の実施の形態について図１１から図１５を参照して説明する。

【０１１１】先ず図１１に、このように液晶装置２００を備えた電子機器の概略構成を示す。

【０１１２】図１１において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、液晶パネル１０、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、テレビ信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回路１００２は、増幅・極性反転回路、相展開回路、ローテーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号ＣＬＫと共に駆動回路１００４に出力する。駆動回路１００４は、液晶パネル１０を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、液晶パネル１０を構成するＴＦＴアレイ基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【０１１３】次に図１２から図１５に、このように構成された電子機器の具体例を夫々示す。

【０１１４】図１２において、電子機器の一例たる液晶プロジェクタ１１００は、上述した駆動回路１００４がＴＦＴアレイ基板上に搭載された液晶パネル１０を含む液晶モジュールを３個用意し、夫々ＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂに夫々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにより夫々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１１５】本実施の形態においては特に、前述のように遮光層をＴＦＴの下側にも設けておけば、当該液晶パネル１０からの入射光に基づく液晶プロジェクタ内の投射光学系による反射光、入射光が通過する際のＴＦＴアレイ基板の表面からの反射光、他の液晶パネルから出射した後にダイクロイックプリズム１１１２を突き抜けてくる入射光の一部（Ｒ光及びＧ光の一部）等が、戻り光としてＴＦＴアレイ基板の側から入射しても、画素電極のスイッチング用のＴＦＴ等のチャネルに対する遮光を十分に行うことができる。この場合、小型化に適したプリズムを投射光学系に用いても、各液晶パネルのＴＦＴアレイ基板とプリズムとの間において、戻り光防止用のＡＲフィルムを貼り付けたり、偏光板にＡＲ被膜処理を施したりすることが不要となるので、構成を小型且つ簡易化する上で大変有利である。

【０１１６】図１３において、電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００は、上述した液晶パネル１０がトップカバーケース内に備えられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１１７】図１４において、電子機器の他の例たるペ

ージャ１３００は、金属フレーム１３０２内に前述の駆動回路１００４がＴＦＴアレイ基板上に搭載されて液晶モジュールをなす液晶パネル１０が、バックライト１３０６ａを含むライトガイド１３０６、回路基板１３０８、第１及び第２のシールド板１３１０及び１３１２、二つの弾性導電体１３１４及び１３１６、並びにフィルムキャリアテープ１３１８と共に収容されている。この例の場合、前述の表示情報処理回路１００２（図１１参照）は、回路基板１３０８に搭載してもよく、液晶パネル１０のＴＦＴアレイ基板上に搭載してもよい。更に、前述の駆動回路１００４を回路基板１３０８上に搭載することも可能である。

【０１１８】尚、図１４に示す例はページャであるので、回路基板１３０８等が設けられている。しかしながら、駆動回路１００４や更に表示情報処理回路１００２を搭載して液晶モジュールをなす液晶パネル１０の場合には、金属フレーム１３０２内に液晶パネル１０を固定したものを液晶装置として、或いはこれに加えてライトガイド１３０６を組み込んだバックライト式の液晶装置として、生産、販売、使用等することも可能である。

【０１１９】また図１５に示すように、駆動回路１００４や表示情報処理回路１００２を搭載しない液晶パネル１０の場合には、駆動回路１００４や表示情報処理回路１００２を含むＩＣ１３２４がポリイミドテープ１３２２上に実装されたＴＣＰ（Tape Carrier Package）１３２０に、ＴＦＴアレイ基板１の周辺部に設けられた異方性導電フィルムを介して物理的且つ電気的に接続して、液晶装置として、生産、販売、使用等することも可能である。

【０１２０】以上図１２から図１５を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図１１に示した電子機器の例として挙げられる。

【０１２１】以上説明したように、本実施の形態によれば、高周波のクロックノイズの発生が低減されており、高品位の画像表示が可能であり、しかも基板サイズに比べて画面表示領域が大きい液晶装置２００を備えた各種の電子機器を実現できる。

【０１２２】

【発明の効果】本発明の電気光学装置によれば、基板に配線された定電位の導電線により、画像信号線は、クロック信号線等の制御信号線からシールドされているので、クロック信号線から画像信号線への高周波のクロックノイズ等の飛び込みを低減でき、高解像度の画像を表示するための高周波数の画像信号に応じて高品位の画像表示を行える。しかも、画像信号線をデータ信号供給手段の両側へ引き回わす構成により、多相展開に対応する多数の画像信号線を配線する場合にも、データ信号供給手段の両側にバランス良く配線でき、限られた基板サイズでの画面の大型化を図ることも可能となる。また、画面表示領域及び複数のデータ線をもシールドすることにより、データ線上のデータ信号等における、高周波のクロックノイズの発生を低減でき、より高品位の画像表示が可能となる。

【０１２３】また、本発明の電子機器によれば、高周波のクロックノイズが低減されており、基板サイズに比べて画面表示領域が大きい高品位の画像表示が可能な、液晶プロジェクタ、パーソナルコンピュータ、ページャ等の様々な電子機器を実現可能となる。

【図面の簡単な説明】

【図１】　液晶装置の実施の形態においてＴＦＴアレイ基板上に形成されたシールド線を含む各種配線、周辺回路等の概略平面図である。

【図２】　図１のシールド線の２次元的レイアウトをより詳細に示す概略平面図である。

【図３】　図２に示したシフトレジスタ回路における回路図（ａ）及びタイミングチャート（ｂ）である。

【図４】　図１のＴＦＴアレイ基板上に形成されたシールド線、画像信号線、クロック信号線のＡ－Ａ’断面図（ａ）及びＢ－Ｂ’断面図（ｂ）である。

【図５】　図１のＴＦＴアレイ基板上に形成された画素電極、走査線、データ等の画面表示領域端部における拡大平面図である。

【図６】　図１の液晶装置の全体構成を示す平面図である。

【図７】　図１の液晶装置の全体構成を示す断面図である。

【図８】　図１の画像信号線（配線ＶＩＤ１～１２）の２次元的レイアウトの一例を示す概略平面図（ａ）及び他の例を示す概略平面図（ｂ）である。

【図９】　図１の液晶装置の画面表示領域に設けられたＴＦＴ部分における断面図である。

【図１０】　図１の液晶装置の周辺見切り領域に設けられたシールド線部分における断面図である。

【図１１】　本発明による電子機器の実施の形態の概略構成を示すブロック図である。

【図１２】　電子機器の一例としての液晶プロジェクタを示す断面図である。

【図１３】　電子機器の他の例としてのパーソナルコンピュータを示す正面図である。

【図１４】　電子機器の一例としてのページャを示す分解斜視図である。

【図１５】　電子機器の一例としてのＴＣＰを用いた液晶装置を示す斜視図である。

【符号の説明】

１…ＴＦＴアレイ基板

(18)

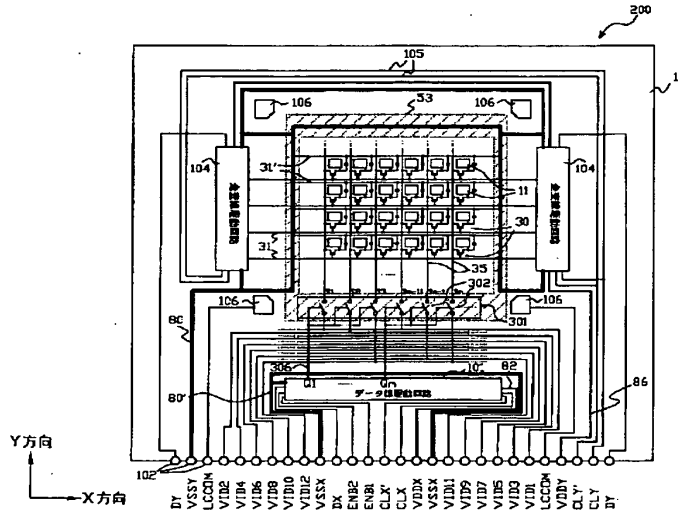
33

2…対向基板
10…液晶パネル
11…画素電極
12…配向膜
21…共通電極
22…配向膜
23…遮光層
30…ＴＦＴ
31…走査線（ゲート電極）
32…半導体層
33…ゲート絶縁層
34…ソース領域
35…データ線（ソース電極）
36…ドレイン領域
37、38…コンタクトホール

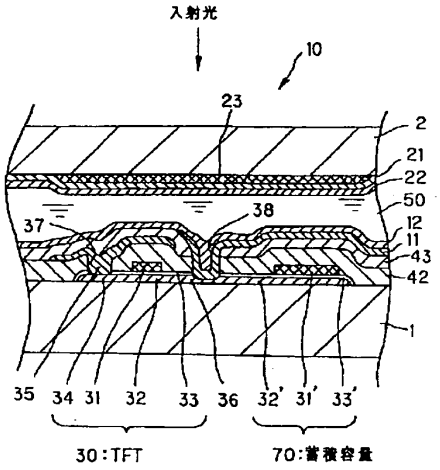
34

42…第１層間絶縁層
43…第２層間絶縁層
50…液晶層
52…シール材
53…周辺見切り
70…蓄積容量
80、80’、82、86…シールド線（定電位線）
101…データ線駆動回路
102…外部入力端子（実装端子）
104…走査線駆動回路
112…イネーブル回路
200…液晶装置
301…サンプリング回路
302…ＴＦＴ

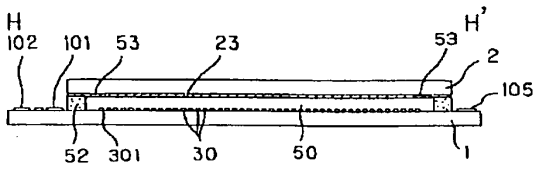
【図１】



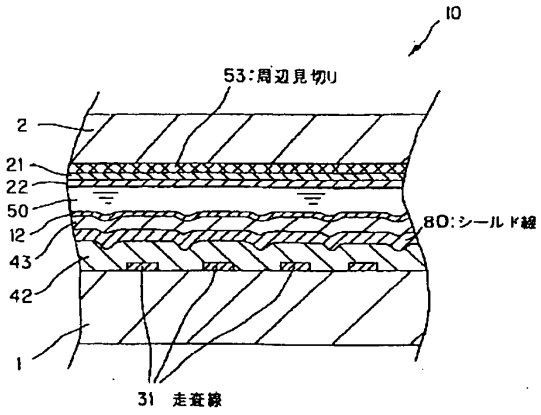
【図９】



【図７】

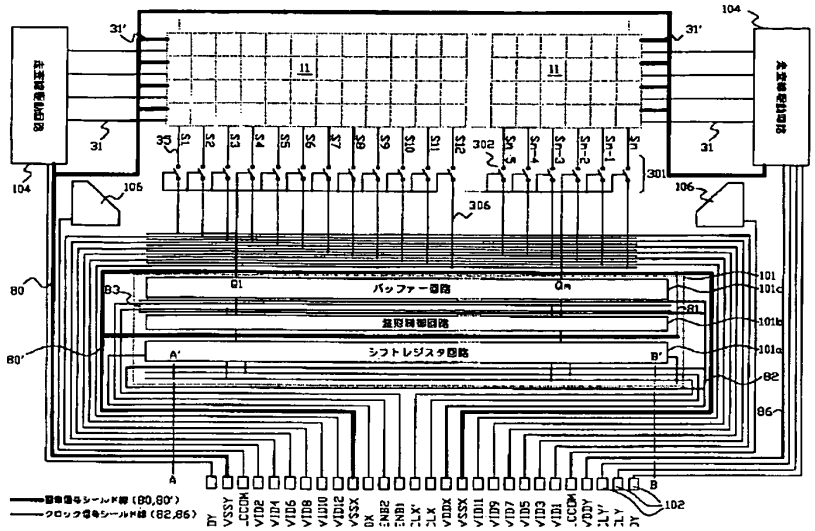


【図１０】

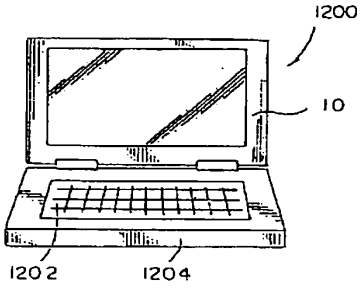


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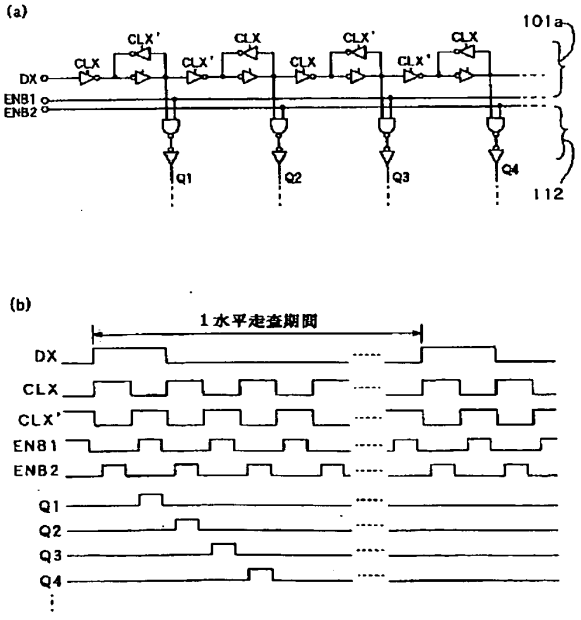
【図２】



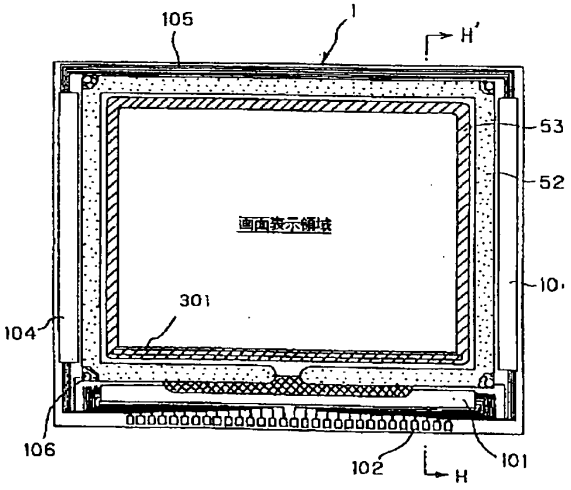
【図１３】



【図３】

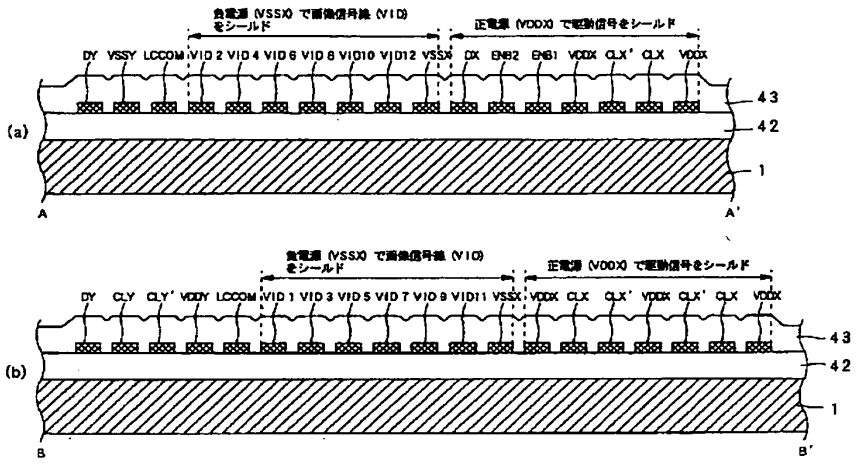


【図６】

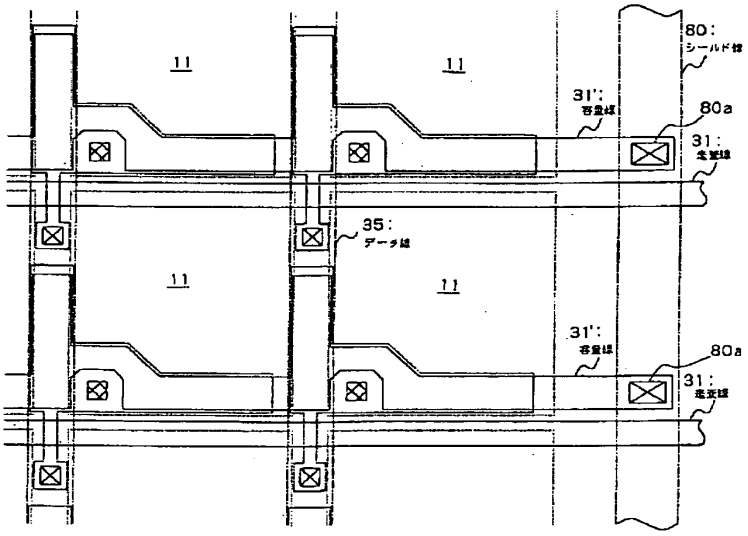


(20)

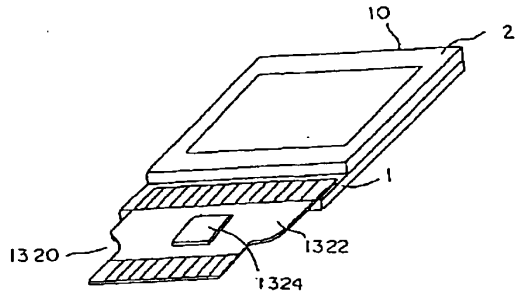
【図４】


負電源 (VSSX) で画像信号線 (VID) をシールド
正電源 (VDDX) で駆動信号をシールド
DY VSSY LCCOM VID2 VID4 VID6 VID8 VID10 VID12 VSSX DX ENB2 ENB1 VDDX CLX' CLX VDDX
43
42
(a)
1
A
A'
負電源 (VSSX) で画像信号線 (VID) をシールド
正電源 (VDDX) で駆動信号をシールド
DY CLY CLY' VDDY LCCOM VID1 VID3 VID5 VID7 VID9 VID11 VSSX VDDX CLX CLX' VDDX CLX' CLX VDDX
43
42
(b)
1
B
B'

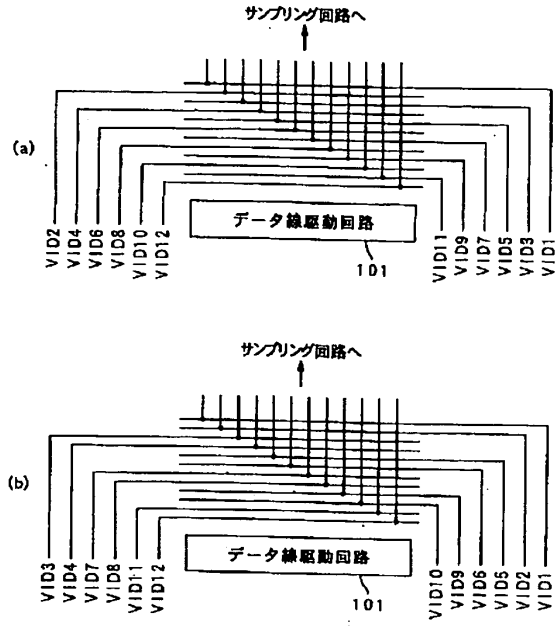
【図５】


11
11
80:
シールド線
31':
容量線
80a
31:
走査線
35:
データ線
11
11
31':
容量線
80a
31:
走査線

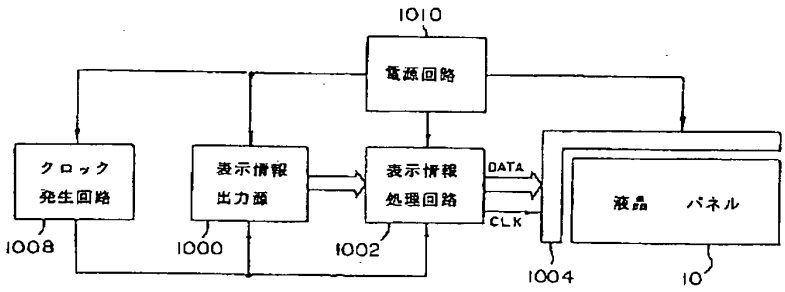
【図１５】


10
2
1
1320
1322
1324

【図８】

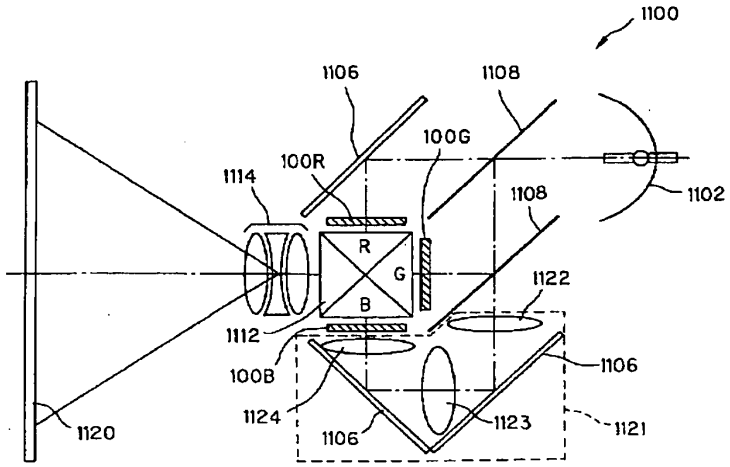

サンプリング回路へ
(a)
データ線駆動回路
101
VID2
VID4
VID6
VID8
VID10
VID12
VID11
VID9
VID7
VID5
VID3
VID1
サンプリング回路へ
(b)
データ線駆動回路
101
VID3
VID4
VID7
VID8
VID11
VID12
VID10
VID9
VID6
VID5
VID2
VID1

【図１１】

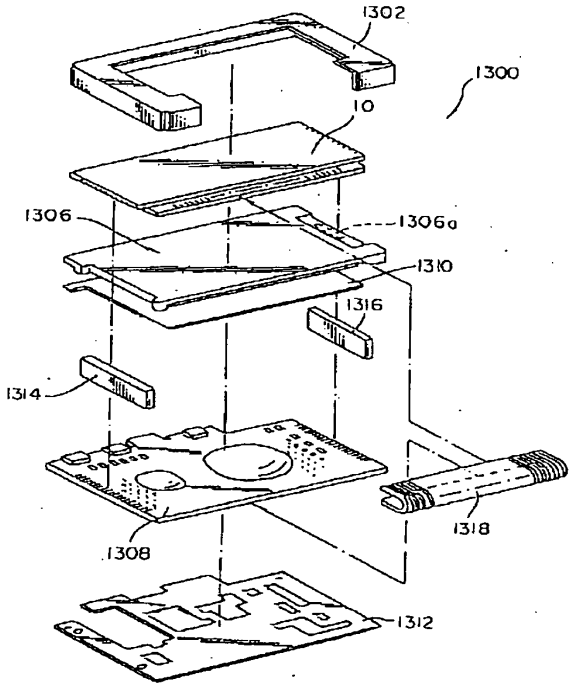

1010
電源回路
クロック
発生回路
1008
表示情報
出力源
1000
表示情報
処理回路
1002
DATA
CLK
液晶 パネル
1004
10

(22)

【図１２】


1100
1106
1108
100G
100R
1114
1102
1108
R
G
B
1122
1112
1106
100B
1124
1123
1121
1106
1120

【図１４】


1302
1300
10
1306
1306a
1310
1316
1314
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1308
1312

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CLAIMS

[Claim(s)]
[Claim 1] Two or more scanning lines which intersect two or more data lines and these two or more data lines on a substrate, Two or more switching elements connected to two or more of said data lines and scanning lines, Two or more pixel electrodes connected to said two or more switching elements, and two or more picture signal lines by which a picture signal is supplied, Said picture signal and said control signal are inputted respectively through two or more control signal lines by which a control signal including a clock signal is supplied, and said picture signal line and said control signal line. It has a data signal supply means to supply the data signal corresponding to said picture signal to said two or more data lines based on said control signal. The 1st picture signal track group is taken about on said substrate among said two or more picture signal lines to said one data signal supply means side. The 2nd picture signal track group is taken about on said 1st substrate among said two or more picture signal lines to the another side side of said data signal supply means. The electro-optic device characterized by having further at least one electric conduction line which shields electrically said 1st and 2nd picture signal track group from said two or more control signal lines, respectively on said substrate.
[Claim 2] Said electric conduction line is an electro-optic device according to claim 1 characterized by shielding said 1st and 2nd picture signal track group from the RF control signal line which supplies the RF control signal which has a period [at least] shorter than the horizontal scanning period of said picture signal among said two or more control signal lines.
[Claim 3] The electro-optic device according to claim 2 characterized by wiring the low frequency control signal line which supplies the low frequency control signal which has the period which is not shorter than the horizontal scanning period of said picture signal at least among said two or more control signal lines with said electric conduction line between said 1st and 2nd picture signal track group and said RF control signal line.
[Claim 4] Two or more 1st external input terminals into which it connects with said 1st picture signal track group, and said picture signal is inputted from the source of an external picture signal, respectively, Two or more 2nd external input terminals into which it connects with said 2nd picture signal track group, and said picture signal is inputted from said source of an external picture signal, respectively, Two or more 3rd external input terminals into which it connects with said control signal line, and said control signal is inputted from the source of an external control signal, respectively, It has further two or more 4th external input terminals connected to said electric conduction line, respectively on the periphery of said substrate. Between said 1st and 2nd external input terminals The electro-optic device according to claim 1 characterized by arranging said 3rd external input terminal and arranging said 4th external input terminal between said 3rd and 2nd external input terminals at the list between said 1st and 3rd external input terminals, respectively.
[Claim 5] Said electric conduction line from the RF control signal line which supplies the RF control signal which has a period [at least] shorter than the horizontal scanning period of said picture signal among said two or more control signal lines The terminal which shields said 1st and 2nd picture signal track group, and adjoins said 4th external input terminal among said 3rd external input terminals The

electro-optic device according to claim 4 characterized by connecting with the low frequency control signal line which supplies the low frequency control signal which has the period which is not shorter than the horizontal scanning period of said picture signal at least among said two or more control signal lines.
[Claim 6] Said electric conduction line is an electro-optic device given in any 1 term of claims 1-5 characterized by including the part which consisted of constant potential lines for a data-line drive which supply the power source for a data-line drive of constant potential to said data signal supply means.
[Claim 7] said constant potential line for a data-line drive -- difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part It is the electro-optic device according to claim 6 characterized by surrounding said 1st and 2nd picture signal track group on said substrate, and the amount of [said / which consisted of potential lines the 2nd law] said electric conduction line part surrounding said control signal line on said substrate.
[Claim 8] Said electric conduction line is an electro-optic device given in any 1 term of claims 1-7 by which it is installing [so that the screen-display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said substrate] characterized.
[Claim 9] It is the electro-optic device according to claim 8 which said substrate is countered, and the opposite substrate is formed, is further equipped with circumference abandonment of the protection-from-light nature formed at least in one side among said substrate and the opposite substrate along with the profile of said screen-display field, and is characterized by for said electric-conduction line to contain the part prepared in said substrate along with said circumference abandonment in the location which counters said circumference abandonment.
[Claim 10] Said electric conduction line and said data line are an electro-optic device given in any 1 term of claims 1-9 characterized by being formed from the same low resistance metallic material.
[Claim 11] An electro-optic device given in any 1 term of claims 1-10 characterized by having further the capacity line which gives the capacity of the specified quantity to said pixel electrode on said substrate, and connecting this capacity line to said electric conduction line.
[Claim 12] It is an electro-optic device given in any 1 term of claims 1-11 which are further equipped with a scan signal supply means to supply a scan signal to said two or more scanning lines, on said substrate, and are characterized by said electric conduction line containing the part which consisted of constant potential lines for a scanning-line drive which supply the power source for a scanning-line drive of constant potential to said scan signal supply means.
[Claim 13] A part for said electric-conduction line part which said scan signal supply means is formed in the both sides of the screen-display field specified with said two or more pixel electrodes, and consisted of said constant potential lines for a scanning-line drive is an electro-optic device according to claim 12 characterized by to be installed so that said screen-display field and said two or more data lines may be surrounded on said 1st substrate, and so that said power source for a scanning-line drive may be to said scanning-line supply means in redundancy.
[Claim 14] The sampling circuit where said data signal supply means samples said picture signal, It has the data-line drive circuit which drives this sampling circuit based on said control signal. The picture signal line contained in said 1st picture signal track group, and the picture signal line contained in said 2nd picture signal track group An electro-optic device given in any 1 term of claims 1-13 characterized by taking about by turns in the shape of a ctenidium from the both sides of said data-line drive circuit for every at least one picture signal line between said data-line drive circuits and said sampling circuits.
[Claim 15] For the picture signal line which reverses the electrical-potential-difference polarity of said data signal for said every data line, and is contained in said 1st picture signal track group, and the picture signal line contained in said 2nd picture signal track group, said data signal supply means is an electro-optic device according to claim 14 characterized by making into a pair two picture signal lines corresponding to the two data lines which adjoin each other, and taking about by turns in the shape of a ctenidium from the both sides of said data-line drive circuit.

[Claim 16] Electronic equipment characterized by equipping claims 1-15 with the electro-optic device of a publication.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of the electronic equipment using electro-optic devices, such as liquid crystal equipment of a active-matrix drive method, and this by thin film transistor (TFT is called hereafter) drive etc., and belongs to the technical field of the electro-optic device of the format of driving the data line by the RF based on control signals, such as a clock signal, by the data-line drive circuit especially prepared on the TFT array substrate, and the electronic equipment using this.
[0002]
[Description of the Prior Art] Conventionally, in the liquid crystal equipment of the active-matrix drive method by TFT drive, many pixel electrodes are prepared on the TFT array substrate at many the scanning lines and the data-line lists which were arranged in all directions, respectively corresponding to each of these intersections. And in addition to these, a data signal supply means to supply a data signal to the data line including a data-line drive circuit, a sampling circuit, etc., and a scan signal supply means to supply a scan signal to the scanning line including a scanning-line drive circuit etc. may be established on such a TFT array substrate.
[0003] In this case, control signals, such as a data-line side reference clock for operating the data-line drive circuit used as the criteria of the supply timing of a data signal, the picture signal which supports the contents of the image which should be displayed and serves as a radical of a data signal, forward, a negative constant potential power source, etc. are supplied to a data signal supply means through the external input terminal and wiring which were prepared in the TFT array substrate, respectively. On the other hand, the scanning-line side reference clock for operating the scanning-line drive circuit used as the criteria of the supply timing of a scan signal, forward, a negative constant potential power source, etc. are supplied to a scan signal supply means through the external input terminal and wiring which were too prepared in the TFT array substrate. And in a scan signal supply means, a scan signal is supplied to the scanning line to the timing based on a scanning-line side reference clock, for example by the scanning-line drive circuit line sequential. A data-line drive circuit carries out the sequential drive of the sampling circuit which samples the picture signal inputted in the data signal supply means corresponding to this, for example to the timing based on a data-line side reference clock, and a data signal is supplied to the data line from a sampling circuit. These results, each TFT by which gate connection was made is made into switch-on at the scanning line according to supply of a scan signal, a data signal is supplied to a pixel electrode through the TFT concerned, and image display in each pixel is performed.
[0004] With the liquid crystal equipment for liquid crystal projectors, a picture signal with a serial, very high frequency is increasingly inputted recent years especially with high-resolution-izing of a display image. For example, if the dot frequency of a picture signal becomes the XGA display mode and SXGA display mode which are used in the personal computer screen of the latest high resolution, they will be about 65MHz and about 135MHz, respectively, and will easily exceed the dot frequency (about 30MHz)

in the conventional VGA display mode. The frequency of the data-line side reference clock supplied to especially a data signal supply means is also becoming very high that it should correspond to this.
[0005]
[Problem(s) to be Solved by the Invention] However, under the request of high-definition-izing of a display image in recent years, generating of the clock noise of a RF by making the frequency of a reference clock high in this way cannot ignore now. That is, in the configuration which supplies the conventional data-line side reference clock with a comparatively low frequency to a data-line drive circuit, for example, and drives a sampling circuit, by having raised the frequency of a clock signal as it was, the clock noise of high frequency will occur in the data signal outputted from the inside of the picture signal inputted into a sampling circuit, or a sampling circuit, and the data signal which should be supplied at the data line will deteriorate. Thus, in having received supply of the data signal which deteriorated, there is a trouble displayed with each pixel electrode of carrying out image mist beam degradation. For example, when performing the gradation display of middle level in each pixel, it will also appear that the about 10mV very small noise jumped in into the picture signal as a noise of extent which can be checked by looking in a display image. This is because change of the permeability of the liquid crystal to change of the liquid crystal driver voltage in middle level is steep compared with the case where the display of the white corresponding to the highest or minimum liquid crystal driver voltage (for example, electrical potential difference between 0 - 5V) or black level is being performed. Thus, in order to realize a highly precise multi-gradation display, the problem of the clock noise of a RF is serious.
[0006] Although the frequency of the picture signal supplied to a sampling circuit by increasing the number of phase expansions on the other hand can be lowered, the number of the external input terminals for a picture signal input which must be prepared in the substrate of a liquid crystal panel must be increased corresponding to the increment in the number of phase expansions. That is, in 6 phase expansion, six external input terminals for a picture signal input are needed, and, in 12 phase expansion, needed 12 pieces, for example. Furthermore, the number of wiring taken about from the external input terminal for these picture signal inputs to a sampling circuit is needed only for the number of phase expansions similarly. These results, the rate that wiring for picture signals occupies the substrate side top of a liquid crystal panel increases, and it becomes difficult to secure on a substrate the field which forms the data signal supply means which consists of a sampling circuit, a data-line drive circuit, etc. It sees like before temporarily here from the edge of a substrate in which the external input terminal was prepared. In having taken about wiring for control signals, such as a clock signal, to one data-line drive circuit side, and having taken about wiring for many picture signals to the another side side of a data-line drive circuit Since the numbers of wiring taken about by each ** differ notably, the trouble that the arrangement balance of wiring in the perimeter of a data-line drive circuit gets very bad (that is, wiring inclines toward one side) arises. In this case, although it is possible to secure the field which enlarges the substrate of a liquid crystal panel and forms a wiring field and a data-line drive circuit, now, it will be contrary to the fundamental request in the technical field of a liquid crystal panel called enlargement of the screen in the limited substrate size.
[0007] This invention is made in view of an above-mentioned trouble , even if the number of wiring and the number of external input terminals increase with the increment in the number of phase expansions of a picture signal , bad influences , such as the clock noise which is the RF on which these can be wired and arranged with sufficient balance and control signals , such as a clock signal of a RF , moreover exert them to a picture signal , can reduce , and let it be a technical problem to offer electronic equipment equipped with the liquid crystal equipment which can perform high-definition image display , and the liquid crystal equipment concerned .
[0008]
[Means for Solving the Problem] The data line of plurality [top / substrate] in order that an electro-optic device according to claim 1 may solve the above-mentioned technical problem, Two or more scanning lines which intersect these two or more data lines, and two or more switching elements connected to two or more of said data lines and scanning lines, Two or more pixel electrodes connected

to said two or more switching elements, and two or more picture signal lines by which a picture signal is supplied, Said picture signal and said control signal are inputted respectively through two or more control signal lines by which a control signal including a clock signal is supplied, and said picture signal line and said control signal line. It has a data signal supply means to supply the data signal corresponding to said picture signal to said two or more data lines based on said control signal. The 1st picture signal track group is taken about on said substrate among said two or more picture signal lines to said one data signal supply means side. The 2nd picture signal track group is taken about on said substrate among said two or more picture signal lines to the another side side of said data signal supply means. It is characterized by having further at least one electric conduction line which shields electrically said 1st and 2nd picture signal track group from said two or more control signal lines, respectively on said substrate.

[0009] According to the electro-optic device according to claim 1, a picture signal is supplied to a data signal supply means through a picture signal line. In parallel to this, the control signal containing a clock signal, an enable signal, etc. is supplied to a data signal supply means through a control signal line. Then, based on a control signal, the data signal corresponding to a picture signal is supplied to two or more data lines by the data signal supply means constituted, for example including a data-line drive circuit, a sampling circuit, etc. The picture signal line is electrically shielded from control signal lines, such as a clock signal line and an enable signal line, by the electric conduction line wired by the substrate especially here, respectively. Therefore, even when the frequency of a clock signal is high, diving, such as a clock noise of the RF from control signal lines, such as a clock signal line, to a picture signal line, can be reduced.

[0010] A scan signal is supplied to a switching element through the scanning line by the scan signal supply means including the scanning-line drive circuit which was formed in the substrate or was connected to the substrate on the other hand. The electrical potential difference impressed to a pixel electrode by the data signal which the data signal corresponding to the picture signal with which the clock noise of high frequency etc. was reduced as mentioned above is supplied to a switching element through the data line in parallel to this, and is further supplied through a switching element changes, and the liquid crystal which counters the pixel electrode concerned drives.

[0011] also when the picture signal with which the resolution of the image which should be displayed was high with the picture signal, for example, polyphase expansion was carried out the above result is inputted, image quality deteriorates according to generating of the clock noise of a RF etc. -- most -- or it is completely lost and high-definition image display is made possible. And the 1st picture signal track group is taken about on the substrate to one data signal supply means side, and the 2nd picture signal track group is taken about on the substrate to the another side side of a data signal supply means. About the picture signal line of a large number corresponding to polyphase expansion, it can arrange with balance sufficient on both sides of a data signal supply means, lowering the frequency of the picture signal supplied to a data signal supply means by following, for example, increasing the number of phase expansions like 12 phase expansion, 24 phase expansion, and --. Consequently, the field which forms the data signal supply means which consists of a sampling circuit or a sampling circuit, a data-line drive circuit, etc. is easily securable on a substrate. Therefore, it also becomes possible to attain enlargement of the screen in the limited substrate size.

[0012] An electro-optic device according to claim 2 is characterized by said electric conduction line shielding said 1st and 2nd picture signal track group from the RF control signal line which supplies the RF control signal which has a period [at least] shorter than the horizontal scanning period of said picture signal among said two or more control signal lines in an electro-optic device according to claim 1.

[0013] According to the electro-optic device according to claim 2, the picture signal line is electrically shielded by the electric conduction line from the high frequency control signal line which supplies high frequency control signals (for example, a clock signal, an enable signal, etc.) among two or more control signal lines. Therefore, even when the frequency of a clock signal is high, diving, such as a clock noise of the RF from a RF control signal line to a picture signal line, can be reduced. In addition, about low

frequency control signals (for example, start signal for the shift registers in a data-line drive circuit etc.), since it does not become the cause of the RF noise in a picture signal or a data signal, the low frequency control signal line which supplies this may be shielded by the electric conduction line, and it is not necessary to shield it.

[0014] An electro-optic device according to claim 3 is characterized by wiring the low frequency control signal line which supplies the low frequency control signal which has the period which is not shorter than the horizontal scanning period of said picture signal at least among said two or more control signal lines with said electric conduction line between said 1st and 2nd picture signal track group and said RF control signal line in an electro-optic device according to claim 2.

[0015] According to the electro-optic device according to claim 3, the picture signal line located in the side near a RF control signal line in the 1st and 2nd picture signal track group is estranged from a RF control signal line by existence of wiring of a total of two at least as a low frequency control signal line and an electric conduction line, and is shielded electrically. That is, bad influences, such as a clock noise to the picture signal line of a high frequency control signal line, can be further reduced by arranging the low frequency control signal line which supplies the low frequency control signals (for example, start signal for the shift registers in a data-line drive circuit etc.) leading to the high frequency noise in a picture signal or a data signal with an electric conduction line between a high frequency control signal line and a picture signal line. Since an electromagnetic wave generally decreases especially according to mediation of distance and an obstruction, the electromagnetic wave impressed to a picture signal line from a RF control signal line decreases by the configuration which wires as mostly as possible an electric conduction line and a low frequency control signal line between a control signal line and a picture signal line. Thus, it sees from a viewpoint of a deployment of a substrate top tooth space, and noise reduction and is advantageous to make a low frequency control signal line intervene between a RF control signal line and a picture signal line in addition to an electric conduction line.

[0016] An electro-optic device according to claim 4 is set to an electro-optic device according to claim 1. Two or more 1st external input terminals into which it connects with said 1st picture signal track group, and said picture signal is inputted from the source of an external picture signal, respectively, Two or more 2nd external input terminals into which it connects with said 2nd picture signal track group, and said picture signal is inputted from said source of an external picture signal, respectively, Two or more 3rd external input terminals into which it connects with said control signal line, and said control signal is inputted from the source of an external control signal, respectively, It has further two or more 4th external input terminals connected to said electric conduction line, respectively on the periphery of said substrate. Between said 1st and 2nd external input terminals Said 3rd external input terminal is arranged and it is characterized by arranging said 4th external input terminal, respectively between said 3rd and 2nd external input terminals at the list between said 1st and 3rd external input terminals.

[0017] According to the electro-optic device according to claim 4, among two or more 1st and 2nd external input terminals connected to the 1st and 2nd picture signal track group on the periphery of a substrate, respectively, two or more 3rd external input terminals connected to the control signal line are arranged. That is, intensive arrangement of two or more 3rd external input terminals connected to the control signal line in the center on the periphery of the substrate with which the 1st to 4th external input terminal was prepared is carried out, and two or more 1st and 2nd external input terminals connected to the both sides at the 1st and 2nd picture signal track group, respectively are arranged. And the 4th external input terminal connected to the electric conduction line among these is arranged. Therefore, while keeping one's distance on a substrate between the 1st and 2nd picture signal track group and a control signal line, the configuration which wires an electric conduction line among these can be obtained easily. Control signals, such as a clock signal, can prevent effectively the situation of generating a clock noise etc. to a picture signal, on the preceding paragraph story especially inputted into the electro-optic device concerned. If two or more external input terminals temporarily connected to two or more external input terminals connected to the picture signal line and a control signal line are intermingled or it adjoins, it is the preceding paragraph story inputted into the electro-optic device concerned, and a picture signal line and a control signal line will become unescapable [the wiring part

which adjoins or approaches], and a clock noise etc. will jump in into a picture signal. Thus, according to this invention, before and after inputting into an electro-optic device, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced. In addition, more preferably, while bringing near the 1st and 2nd external input terminal by both sides as much as possible and arranging it in the field which can form an external input terminal in the periphery of a substrate, spacing is vacated as much as possible between the 3rd external input terminals arranged among both, and the 4th external input terminal connected to the electric conduction line at this interval is arranged.
[0018] An electro-optic device according to claim 5 is set to an electro-optic device according to claim 4. Said electric conduction line From the RF control signal line which supplies the RF control signal which has a period [at least] shorter than the horizontal scanning period of said picture signal among said two or more control signal lines The terminal which shields said 1st and 2nd picture signal track group, and adjoins said 4th external input terminal among said 3rd external input terminals It is characterized by connecting with the low frequency control signal line which supplies the low frequency control signal which has the period which is not shorter than the horizontal scanning period of said picture signal at least among said two or more control signal lines.
[0019] According to the electro-optic device according to claim 5, the picture signal line is electrically shielded from the RF control signal line by the electric conduction line. Since the terminal contiguous to the 4th external input terminal connected to the electric conduction line among the 3rd external input terminals connected to the control signal line especially here is connected to the low frequency control signal line, a picture signal line is estranged from a RF control signal line by existence of wiring of a total of two at least as a low frequency control signal line and an electric conduction line, and is shielded electrically.
[0020] An electro-optic device according to claim 6 is characterized by said electric conduction line containing the part which consisted of constant potential lines for a data-line drive which supply the power source for a data-line drive of constant potential to said data signal supply means in an electro-optic device according to claim 1.
[0021] According to the electro-optic device according to claim 6, an electric conduction line Since the part which consisted of constant potential lines for a data-line drive which supply the power source for a data-line drive of constant potential to said data signal supply means is included In other words, by sharing an external input terminal and the wiring itself, it also becomes very easy by installing a potential line and considering as an electric conduction line to be able to attain simplification and space-saving-izing of a configuration, especially to make an electric conduction line into constant potential.
[0022] An electro-optic device according to claim 7 is set to an electro-optic device according to claim 6. Said constant potential line for a data-line drive difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part The 1st and 2nd picture signal track group is surrounded on said substrate, and a part for said said electric conduction line part which consisted of potential lines the 2nd law is characterized by surrounding said control signal line on said 1st substrate on said substrate.
[0023] According to the electro-optic device according to claim 7, the 1st and 2nd picture signal track group is surrounded by the amount of [by which potential lines were consisted of the 1st law in order to supply the negative supply of for example, touch-down potential] electric conduction line part on the substrate. The control signal line is surrounded by the amount of [by which potential lines were consisted of the 2nd law in order to supply a positive supply] electric conduction line part on the substrate. Therefore, the configuration from which the picture signal line was shielded [line / control signal] by the duplex on the 1st substrate is obtained.
[0024] An electro-optic device according to claim 8 is installing [so that the screen-display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said substrate] characterized by said electric conduction line in an electro-optic device given in any 1 term of claims 1-7.
[0025] According to the electro-optic device according to claim 8, by the electric conduction line, since

a screen-display field and two or more data lines are surrounded on the substrate, a screen-display field and two or more data lines concerned will also be shielded from control signal lines, such as a clock signal line. Therefore, generating of the clock noise of a RF in the data signal outputted from the data signal supply means, the data signal which reached the switching element and the pixel electrode etc. can be reduced.

[0026] An electro-optic device according to claim 9 is set to an electro-optic device according to claim 8. Counter said substrate, the opposite substrate is formed and it has further circumference abandonment of the protection-from-light nature formed at least in one side among said substrate and the opposite substrate along with the profile of said screen-display field. It is characterized by said electric conduction line containing the part prepared in said substrate along with said circumference abandonment in the location which counters said circumference abandonment.

[0027] since the electric conduction line is formed in the bottom of circumference abandonment of a substrate according to the electro-optic device according to claim 9, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line drive circuit and a data-line drive circuit in the circumference part of a substrate with allowances, and the display area in liquid crystal equipment also decreases by electric conduction line formation -- most -- or there is completely nothing.

[0028] An electro-optic device according to claim 10 is characterized by forming said electric conduction line and said data line from the same low resistance metallic material in liquid crystal equipment given in any 1 term of claims 1-9.

[0029] According to the electro-optic device according to claim 10, since the electric conduction line is formed from the same low resistance metallic material as the data lines, such as aluminum (aluminum), even if the leading-about field of an electric conduction line is long, resistance of an electric conduction line will be suppressed low practically enough. That is, since it becomes possible to wire the large field which sewed clearances, such as other wiring and a circuit, for example, wired zigzag for a long time, or included the electric conduction line in it to the screen-display field etc. for a long time in an electric conduction line, without lowering the effectiveness of shielding by the increment in resistance, a comparatively easy configuration can raise the effectiveness of the shielding concerned more as a whole. Furthermore, in the manufacture process of the electro-optic device concerned, an electric conduction line and the data line can be formed according to the same process from the same low resistance metallic material. That is, the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.

[0030] The electro-optic device according to claim 11 equips said pixel electrode with the capacity line which gives the capacity of the specified quantity further in the electro-optic device given in any 1 term of claims 1-10, and it is characterized by connecting this capacity line to said electric conduction line.

[0031] According to the electro-optic device according to claim 11, since the capacity of the specified quantity is given to the pixel electrode by the capacity line, even if duty ratio is small, a high definition display is enabled. And the capacity line is connected to the electric conduction line. Therefore, the bad influence to the switching element and pixel electrode by potential fluctuation of a capacity line is prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction lines.

[0032] The electro-optic device according to claim 12 is further equipped with the scan signal supply means which carries out sequential supply of the scan signal at said two or more scanning lines on said substrate in the electro-optic device given in any 1 term of claims 1-11, and said electric conduction line is characterized by including the part which consisted of constant potential lines for a scanning-line drive which supply the power source for a scanning-line drive of constant potential to said scan signal supply means.

[0033] According to the electro-optic device according to claim 12, the picture signal line is electrically shielded by the amount of [which consisted of constant potential lines for a scanning-line drive]

electric conduction line part from the control signal line. Therefore, even when the frequency of a clock signal is high, diving, such as a clock noise of the RF from a control signal line to a picture signal line, can be reduced.
[0034] An electro-optic device according to claim 13 is set to an electro-optic device according to claim 12. Said scan signal supply means The amount of [which is prepared in the both sides of the screen-display field specified with said two or more pixel electrodes, and consisted of said constant potential lines for a scanning-line drive] said electric conduction line part It is installed so that said screen-display field and said two or more data lines may be surrounded on said substrate, and so that said source for a scanning-line drive may be supplied to said scanning-line supply means in redundancy.
[0035] Since a screen-display field and two or more data lines are surrounded by the amount of [which consisted of constant potential lines for a scanning-line drive] electric conduction line part on the substrate according to the electro-optic device according to claim 13, a screen-display field and two or more data lines concerned will also be shielded from control signal lines, such as a clock signal line. Therefore, generating of the clock noise of a RF in the data signal outputted from the data signal supply means, the data signal which reached the switching element and the pixel electrode etc. can be reduced. Furthermore, since it is installed so that the power source for a scanning-line drive may be supplied to the scanning-line supply means formed in the both sides of a screen-display field in redundancy, even if an open circuit arises on the constant potential line for a scanning-line drive in a part for the electric conduction line part which consisted of constant potential lines for a scanning-line drive, and the other part, since the amount of [which consisted of constant potential lines for a scanning-line drive] electric-conduction line part cannot become an equipment defect easily, it will be advantageous.
[0036] An electro-optic device according to claim 14 is set to an electro-optic device given in any 1 term of claims 1-13. Said data signal supply means It has the sampling circuit which samples said picture signal, and the data-line drive circuit which drives this sampling circuit based on said control signal. The picture signal line contained in said 1st picture signal track group, and the picture signal line contained in said 2nd picture signal track group It is characterized by taking about by turns in the shape of a ctenidium from the both sides of said data-line drive circuit for every at least one picture signal line between said data-line drive circuits and said sampling circuits.
[0037] The picture signal line which is contained in the 1st picture signal track group according to the electro-optic device according to claim 14 The picture signal line contained in for example, (the picture signal line 1, 3, 5, and VID 7 corresponding to the odd-numbered data line and --), and the 2nd picture signal track group It takes about by turns in the shape of a ctenidium from the both sides of a data-line drive circuit for every at least one picture signal line with for example, (the picture signal line 2, 4, 6, and VID 8 corresponding to the even-numbered data line and --). Therefore, a picture signal line and the data line can be wired with regularly and sufficient balance around a data-line drive circuit.
[0038] An electro-optic device according to claim 15 is set to an electro-optic device according to claim 14. Said data signal supply means The picture signal line which reverses the electrical-potential-difference polarity of said data signal for said every data line, and is contained in said 1st picture signal track group, and the picture signal line contained in said 2nd picture signal track group It is characterized by making into a pair two picture signal lines corresponding to the two data lines which adjoin each other, and taking about by turns in the shape of a ctenidium from the both sides of said data-line drive circuit.
[0039] According to the electro-optic device according to claim 15, the electrical-potential-difference polarity of a data signal is reversed for every data line by the data signal supply means, a reversal drive called the 1S so-called reversal and dot reversal is performed, and the flicker on the display screen is reduced. The picture signal line (for example, the picture signal line 1, 2, and VID 5 in every two corresponding to the two data lines which adjoin each other, 6 --) contained in the 1st picture signal track group here, and the picture signal line contained in the 2nd picture signal track group Two picture signal lines corresponding to the two data lines which adjoin for example, (the picture signal line 3, 4, and VID 7 in every two corresponding to the two data lines which adjoin each other and 8 --) are made into a pair, and it takes about by turns in the shape of a ctenidium from the both sides of a data-line drive

circuit. Therefore, about the noise component which the picture signal of reversed polarity will be supplied to the picture signal line which adjoins each other, and originated in the same noise source, since the effectiveness mutually negated among these both works, when reducing a noise, it is advantageous.
[0040] Electronic equipment according to claim 16 is characterized by equipping claims 1-15 with the electro-optic device of a publication.
[0041] According to electronic equipment according to claim 16, it has liquid crystal equipment of the invention in this application mentioned above, the clock noise of a RF etc. is reduced, and the high-definition image display of electronic equipment becomes possible.
[0042] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.
[0043]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing.
[0044] (Configuration of liquid crystal equipment) As an example of an electro-optic device, the configuration of the gestalt of operation of liquid crystal equipment is explained based on drawing 8 from drawing 1 . Drawing 1 is the top view showing the configuration of various wiring containing the electric conduction line (shielding wire is called hereafter.) formed on the TFT array substrate in the gestalt of operation of liquid crystal equipment, a circumference circuit, etc. drawing 2 It is the top view showing the more detailed two-dimensional layout of the shielding wire of drawing 1 . Drawing 3 (a) and (b) are the A-A'sectional view and B-B' sectional views of drawing 2 showing wiring of shielding wire, a picture signal line, a clock signal line, etc., respectively. Drawing 5 It is the expansion top view of the pixel part of drawing 1 , drawing 6 is the top view which looked at the TFT array substrate from the opposite substrate side with each component formed on it, and drawing 7 is a H-H' sectional view of drawing 6 shown including an opposite substrate. Drawing 8 is the outline top view (drawing 8 (b)) showing the outline top view (drawing 8 (a)) and other examples which show an example of the two-dimensional layout of the picture signal line of drawing 1 .
[0045] Liquid crystal equipment 200 is equipped with the TFT array substrate 1 which consists of a quartz substrate, hard glass, etc. in drawing 1 . Two or more pixel electrodes 11 prepared in the shape of a matrix on the TFT array substrate 1, The data line 35 which two or more arrays are carried out in the direction of X, and is extended along the direction of Y, respectively, The scanning line 31 which two or more arrays are carried out in the direction of Y, and is extended along the direction of X, respectively, While intervening between each data line 35 and the pixel electrode 11, respectively, two or more TFT30 as an example of the switching element which controls the switch-on and the non-switch-on between these according to the scan signal supplied through the scanning line 31, respectively, respectively is formed. Moreover, on the TFT array substrate 1, capacity line 31' which is wiring for the below-mentioned storage capacitance (refer to drawing 9) is formed almost in parallel along with the scanning line 31.
[0046] On the TFT array substrate 1, the sampling circuit 301 and the data-line drive circuit 101 which constitute an example of a data signal supply means, and the scanning-line drive circuit 104 which constitutes an example of a scan signal supply means are formed further. moreover, to the surface of the screen-display field (namely, field of the liquid crystal panel with which an image is actually displayed by the orientation change of state of liquid crystal) specified with two or more pixel electrodes 11 Two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of a screen-display field is formed, and the fish eye 106 which consists of flow material for taking an electric flow between the TFT array substrate 1 and an opposite substrate is formed in the four corners of a screen-display field. However, a vertical flow part is good at at least one place. The signal name inputted through the external input terminal 102 prepared along the lower side of the TFT array substrate 1 in explanation of drawing 8 and its signal wiring are made into what (for example, the signal wiring is called "Wiring CLX" to the "clock signal CLX" which is a signal name) the alphabet notation same for easy-izing of explanation is added, respectively, and is referred to for after a signal and wiring

from drawing 1 below. [two or more]
[0047] The scanning-line drive circuit 104 starts a built-in shift register circuit by the input of a start signal DY, using the negative supply VSSY and positive supply VDDY for scanning-line drive circuit 104 which are supplied to external input terminal 102 list through Wiring VSSY and VDDY from an external control circuit as a power source. and -- an external input -- a terminal -- 102 -- a list -- wiring -- CLY -- and -- CLY -- ' -- minding -- supplying -- having -- the scanning line -- a drive -- a circuit -- 104 -- built-in -- a shift register circuit -- ** -- a reference clock -- a signal -- CLY -- and -- the -- reversal -- a clock signal -- CLY -- ' -- being based -- predetermined -- timing -- the scanning line 31 -- a scan signal -- a pulse ---like -- line sequential -- impressing .
[0048] The data-line drive circuit 101 starts a built-in shift register circuit by the input of start signal DX, using the negative supply VSSX and positive supply VDDX for data-line drive circuits which are supplied to external input terminal 102 list through signal wiring VSSX and VDDX from an external control circuit as a power source. And external input terminal 102 list is supplied through Wiring CLX and CLX'. It is based on the reference clock signal CLX for the built-in shift register circuits of the data-line drive circuit 101, and its reversal clock signal CLX'. It doubles with the timing to which the scanning-line drive circuit 104 impresses a scan signal. About picture signal [which is supplied through the external input terminal 102 and wiring VID1-VID12 / which was developed 12 phases, for example] VID1 - VID12 each A sampling circuit driving signal is minded every data line 35, the sampling circuit drive signal line 306 is minded [301], and it supplies to predetermined timing.
[0049] The sampling circuit 301 is equipped with TFT302 every data line 35, wiring VID1-VID12 is connected to the source electrode of TFT302, and the sampling circuit drive signal line 306 is connected to the gate electrode of TFT302. And an input of picture signals VID1-VID12 samples these picture signals. Moreover, if a sampling circuit driving signal is inputted from the data-line drive circuit 101 through the sampling circuit drive signal line 306, sequential impression of the picture signal sampled about picture signal VID1 - VID12 each will be carried out for every group who consists of the 12 adjoining data lines 35.
[0050] As mentioned above, the data-line drive circuit 101 and the sampling circuit 301 are constituted so that the picture signals VID1-VID12 by which 12 phase expansion was carried out may be supplied to the data line 35 as a data signal. Although the gestalt of this operation described the method which chooses as coincidence the sampling circuit 301 connected to the 12 adjoining data lines 35, and consists of the 12 data lines 35 and which carries out the sequential transfer for every group, the data line 35 may be chosen every six and you may choose every 24. Or the number of two or more arbitration may be chosen as coincidence. Moreover, as long as the capacity of TFT302 of a sampling circuit 301 is high, you may choose one by one for every data line. Under the present circumstances, it cannot be overemphasized that the external input terminal 102 and picture signal line for picture signals only of the number of phase expansions of a picture signal are the need at least. Since wiring VID1-VID12 is taken about from the both sides of the data-line drive circuit 101 so that especially the gestalt of this operation may describe below, even if there are many these numbers (the number of phase expansions), they can wire with sufficient balance on the TFT array substrate 1. In addition, you may constitute so that the number of phase expansions of a picture signal and the number which chooses a sampling circuit 301 as coincidence may spread a phase etc. and it may become, and you may constitute so that the former may increase more than the latter.
[0051] As shown in drawing 2 , if start signal DX is inputted, after the data-line drive circuit 101 shapes in waveform and buffers the transfer signal from shift-register-circuit 101a which starts sequential generation of the reference clock signal CLX and the transfer signal based on the reversal clock signal CLK', and shift-register-circuit 101a, it is equipped with wave control circuit 101b and buffer circuit 101c which are supplied to a sampling circuit 301 through the sampling circuit drive signal line 306. Moreover, corresponding to the picture signals VID1-VID12 with which 12 phase expansion of the sampling circuit 301 was carried out, 12 TFT(s)302 are connected at a time to each sampling circuit drive signal line 306 at parallel. That is, the switches S1-S12 which consist of TFT(s)302 are connected to 1 Motome's sampling circuit drive signal line 306 from the left, switches S13-S24 are connected to 2

Motome's sampling circuit drive signal line 306 from the left, and switch Sn-11 - Sn are connected to the right end sampling circuit drive signal line 306. In drawing 1 , the enable signals ENB1 and ENB2 which were omitted and were shown by drawing 2 are inputted into the enabling circuit prepared in wave control circuit 101b. The selection period of a sampling circuit 301 is controlled by this enabling circuit by restricting the width of face of the pulse by which a sequential output is carried out from shift-register-circuit 101a to the pulse width of enable signals ENB1 and ENB2. Generating of the ghost between the data lines 35 which separate every 12 data lines and receive a picture signal from the same wiring (VID 1-12) by this is prevented. Therefore, enable signals ENB1 and ENB2 belong to the RF control signal which has a period shorter than a horizontal scanning period as well as a clock signal and CLX'. On the other hand, start signal DX inputted into shift-register-circuit 101a belongs to the low frequency control signal which has the period which is not shorter than a horizontal scanning period as well as the start signal DY inputted into the shift register by the side of a clock signal CLY, and CLY' and a scanning-line drive circuit.

[0052] Here, the concrete circuitry and actuation of shift-register-circuit 101a are explained with reference to drawing 3 . In addition, drawing 3 (a) is the circuit diagram showing a shift register circuit including an enabling circuit, and drawing 3 (b) is the timing chart of the various signals in this shift register circuit.

[0053] First, in drawing 3 (a), the enabling circuit 112 is formed corresponding to the output of each stage of shift-register-circuit 101a, respectively. Each stage of shift-register-circuit 101a is constituted including respectively two clocked inverters transmitted to the next step, applying feedback to a transfer signal, whenever the reference clock signal CLX of a predetermined period and the binary level of the reversal signal CLX' change so that the sequential output of the transfer signal may be carried out from each stage in the direction of transfer corresponding to the right (direction which goes to the right from the left). Moreover, the enabling circuit 112 consists of a NAND circuit which takes a transfer signal, an enable signal ENB1, or an exclusive AND with ENB2, and an inverter circuit which reverses the result so that the pulse width of the transfer signal outputted from an even level eye may be restricted to the pulse width of the 2nd enable signal ENB2, while restricting the pulse width of the transfer signal outputted from the odd level eye of shift-register-circuit 101a to the pulse width of the 1st enable signal ENB1. The signal DX for starting a transfer of a transfer signal is inputted into shift-register-circuit 101a from the left-hand side in drawing.

[0054] From shift-register-circuit 101a which consisted of timing shown in the timing chart of drawing 3 (b) as mentioned above when this signal DX, a clock signal CLX and its reversal signal CLX', and the 1st and 2nd enable signals ENB1 and ENB2 were inputted, the sequential output of the transfer signal in which only the half period of a clock signal CLX is one by one is carried out. Then, the pulse width of this transfer signal is restricted to the pulse width of signals ENB1 and ENB2 by the enabling circuit 112, and sequential supply of the sampling circuit driving signals Q1, Q2, Q3, --, Qn (however, n odd number) which consist of a pulse with width of face narrower than the pulse width of a clock signal CLX, respectively is carried out in a sampling circuit 301 through wave control circuit 101b and buffer circuit 101c which were shown in drawing 2 .

[0055] Especially with the gestalt of this operation, as shown in drawing 1 and drawing 2 , shielding-wire 80' of the constant potential which served as the shielding wire 80 of the constant potential which served as the wiring VSSY for negative supplies VSSY, and the wiring VSSX for negative supplies VSSX to the TFT array substrate 1, the shielding wire 82 of the constant potential which served both as the wiring VDDX for positive supplies VDDX, and the shielding wire 86 of the constant potential which served as the wiring VDDY for positive supplies VDDY are wired. Such shielding wire 80, 80', and the wiring VID1-VID12 that is picture signal lines by 82 and 86 are electrically shielded by Wiring CLX and the CLX' list from wiring ENB1 and ENB2. Therefore, even when the frequency of a clock signal CLX is high, diving, such as a clock noise of the RF to the wiring VID1-VID12 from wiring ENB1 and ENB2, can be reduced in Wiring CLX and the CLX' list which are a RF control signal line.

[0056] As shown in drawing 1 and drawing 2 , and the odd-numbered picture signal line 1, 3, 5, 7, 9, and VID 11 which constitutes an example of the 1st picture signal track group See the TFT array

substrate 1 top in the direction of X, and it takes about on the right-hand side of the data-line drive circuit 101. The even-numbered picture signal line 2, 4, 6, 8, 10, and VID 12 which constitutes an example of the 2nd picture signal track group is taken about on the TFT array substrate 1 on the left-hand side of the data-line drive circuit 101. About much wiring 1-VID 12, it can arrange with balance sufficient on both sides of the data-line drive circuit 101, lowering the frequency of the picture signals 1-VID 12 supplied to a sampling circuit 301 by following, for example, performing the number of phase expansions of a polyphase comparatively like 12 phase expansion. Consequently, the field which forms the data signal supply means which consists of a sampling circuit 301 and a data-line drive circuit 101 is easily securable on the TFT array substrate 1. Therefore, enlargement of the screen in the limited substrate size is attained.

[0057] Especially with the gestalt of this operation, as shown in drawing 2 , the picture signal line slack wiring 1-VID 12 is electrically shielded from wiring ENB1 and ENB2 by shielding-wire 80' of constant potential by the clock signal CLX and the CLX 'high frequency control signal line slack wiring CLX and CLX which supplies enable signals ENB1 and ENB2 to list' list belonging to the above-mentioned high frequency control signal. Therefore, even when the frequency of a clock signal is high, diving, such as a clock noise of the RF to the wiring 1-VID 12 from these RF control signal lines, can be reduced. On the other hand, it does not become the cause of the RF noise in the start signals DX and DY belonging to the above-mentioned low frequency control signal, and the data signal on the data line 35 supplied to the list about a clock signal CLY and CLY' based on the picture signal on wiring VID 1-12, and this. For this reason, the low frequency control signal line slack wiring DX, DY, and CLY and CLY' may be shielded with the shielding wire of constant potential, and it is not necessary to shield them. With the gestalt of this operation, as shown in drawing 2 , on the right-hand side, wiring 1, 3, --, VID 11 is shielded from Wiring DY and CLY and CLY' by the shielding wire 86 which consists of wiring VDDY of constant potential, and, on the left-hand side, wiring 2, 4, --, VID 12 is shielded from Wiring DY by the shielding wire 80 which consists of wiring VSSY of constant potential. Moreover, wiring 1-VID 12 is shielded by shielding-wire 80' from Wiring DX.

[0058] Furthermore, with the gestalt of this operation, especially the wiring VID11 located in the side near the RF control signal line slack wiring CLX and CLX' in a right-hand side (the oddth) picture signal track group is estranged from these Wiring CLX and CLX' by two shielding-wire 80' and the existence of 82 which consist of wiring VSSX and VDDX, respectively, and is shielded electrically. Moreover, the wiring VID12 located in the side near the RF control signal line slack wiring CLX and CLX' in a left-hand side (the eventh) picture signal track group is estranged from these Wiring CLX and CLX' by existence of one shielding-wire 80' and the low frequency control signal line slack wiring DX which consist of wiring VSSX, and is shielded electrically. That is, bad influences, such as a clock noise to VID12 of Wiring CLX and CLX', can be further reduced by arranging the wiring DX belonging to the low frequency control signal line leading to the RF noise in a picture signal or a data signal with shielding-wire 80' between the RF control signal line slack wiring CLX, and CLX' and wiring VID12. since an electromagnetic wave generally decreases according to mediation of distance and an obstruction -- between Wiring CLX and CLX' and wiring ENB1 and ENB2, and wiring 1-VID 12 -- shielding wire (wiring 80 and 80' --) By the configuration which wires as mostly as possible wiring of the constant potential of 82 and 86 grades, and a low frequency control signal line (wiring with which low frequency control signals, such as Wiring DX, DY, and CLY and CLY', are supplied), the electromagnetic wave which generates a clock noise decreases and a clock noise etc. decreases. Thus, it sees from a viewpoint of a deployment of the TFT substrate 1 top tooth space, and noise reduction and is advantageous to make a low frequency control signal line intervene between a RF control signal line and a picture signal line in addition to shielding wire.

[0059] Moreover, as shown in drawing 2 , with the gestalt of this operation, the external input terminal 102 connected to wiring 1-VID 12 on the periphery of the TFT array substrate 1, respectively is arranged at both sides, and intensive arrangement of the external input terminal 102 connected to wiring ENB1 and ENB2, CLX', and CLX between them is carried out. And the external input terminal 102 connected to shielding-wire 80' (wiring VSSX) between the external input terminals 102 connected to

the external input terminal 102 connected to wiring VID12 and wiring ENB1 is arranged. Moreover, the external input terminal 102 connected to shielding-wire 80' (wiring VSSX) between the external input terminals 102 connected to the external input terminal 102 connected to wiring VID11 and Wiring CLX is arranged. Therefore, the configuration which wires shielding-wire 80' between wiring 1-VID 12, wiring ENB1 and ENB2, CLX', and CLX can be obtained easily. It is the preceding paragraph story especially inputted into liquid crystal equipment 200, for example, liquid crystal equipment 200 is wired from external circuits, such as a display information processing circuit, and a clock signal CLX etc. can prevent effectively the situation of generating a clock noise etc. to picture signals 1-VID 12. Thus, according to the gestalt of this operation, before and after inputting into liquid crystal equipment 200, the diving of the clock noise of the RF to wiring for picture signals from wiring for clock signals etc. can be reduced. In addition, more preferably, while bringing near the external input terminal 102 wiring VID1 - for 12 by both sides (right-hand side and left-hand side) as much as possible and arranging it in the field which can form the external input terminal 102 in the periphery of the TFT array substrate 1, spacing is vacated as much as possible in the center between the external input terminals 102 of business, such as wiring CLX' by which intensive arrangement is carried out, and the external input terminal 102 of business, such as shielding-wire 80', is arranged at this spacing.

[0060] With the gestalt of this operation, it becomes possible to install Wiring VSSY, VSSX, and VDDX and VSSY, respectively, and to share an external input terminal and wiring shielding wire 80, 80', and by being referred to as 82 and 86, and simplification and space-saving-izing of an equipment configuration can be attained. Moreover, shielding wire 80, 80', and potential of 82 and 86 are easily made constant potential by common use-ization with a constant potential line in this way. However, you may wire wiring for power sources, and shielding wire separately.

[0061] With the gestalt of this operation, as shown in drawing 2 , two external input terminals 102 into which a negative supply VSSX is inputted are formed. And wiring VID1-VID12 is surrounded on the TFT array substrate 1 by shielding-wire 80' made into the potential (negative potential) of a negative supply VSSX. Especially shielding-wire 80' formed from metal layers, such as the same aluminum as the data line 35, also between shift-register-circuit 101a and wave control circuit 101b is installed. And through the shielding-wire connection 81 which metal layers, such as aluminum, set caudad through the insulating layer between the 1st layer like the after-mentioned, for example, was formed from conductive layers, such as the same polish recon as the scanning line 31, as the point of installed shielding-wire 80' surrounds wave control circuit 101b and buffer circuit 101c, it is connected to shielding-wire 80'.

[0062] On the other hand, as shown in drawing 2 , Wiring CLX and CLX' are surrounded on the TFT array substrate 1 in the part which adjoins the data-line drive circuit 101 by the shielding wire 82 made into the potential (forward potential) of a positive supply VDDX. Especially the shielding wire 82 formed from metal layers, such as the same aluminum as the data line 35, also between wave control circuit 101b and buffer circuit 101c is installed, and as the point surrounds wave control circuit 101b and shift-register-circuit 101a through the shielding-wire connection 83 formed from conductive layers, such as the same polish recon as the scanning line 31, it is connected to shielding wire 82.

[0063] Therefore, the configuration shielded by the duplex is taken by Wiring CLX and the CLX' list from wiring ENB1 and ENB2 on the TFT array substrate 1, and let wiring VID1-VID12 be what has dependability high [shielding to wave control circuit 101b and buffer circuit 101c] at the shift-register-circuit 101a list. However, if it constitutes as intervened in shielding wire 80, 80', and at least one 82 and 86 between Wiring CLX, CLX', and ENB1 and ENB2 and wiring VID1-VID12 even if it does not take the configuration surrounded in this way, the effectiveness of shielding will be acquired somewhat.

[0064] With the gestalt of this operation, as shown in drawing 1 and drawing 2 , a screen-display field and two or more data lines 35 are surrounded on the TFT array substrate 1 by shielding wire 80. For this reason, a screen-display field and two or more data lines 35 concerned are also shielded from Wiring CLX, CLX', and ENB1 and ENB2. Therefore, generating of the clock noise of a RF in the sampling circuit driving signal outputted from the data-line drive circuit 101, the data signal which reached TFT30 and the pixel electrode 11 etc. can be reduced. However, if it constitutes so that the wiring VID1-VID6

until it reaches a sampling circuit 301 may be shielded by shielding wire 80, 80', 82, or 86 even if it does not take the configuration surrounded to a screen-display field in this way, the effectiveness of shielding will be acquired somewhat. In this case, shielding wire 80 is installed from Wiring VSSY, and it is installed so that the power-source signal VSSY may be supplied to the scanning-line drive circuit 104 established in the both sides of a screen-display field in redundancy, so that drawing 1 may show. For this reason, even if an open circuit arises in shielding wire 80 or Wiring VSSY, since it is hard to become an equipment defect, it will be advantageous.

[0065] As shown in drawing 4 (a) and the sectional view of (b), respectively, it is formed from the various wiring DY connected to the external input terminal 102, VSSY, --, the low resistance [with same VDDX] metallic material as the data lines 35, such as aluminum (aluminum). Therefore, even if shielding wire 80 (wiring VSSY), 80' (wiring VSSX), and the leading-about field of 82 (wiring VDDX) and 86 (wiring VDDY) are long, each shielding wire 80, 80', and resistance of 82 and 86 will be suppressed low practically enough. That is, as shown in drawing 2 , the clearance between wave control circuit 101b and buffer circuit 101c is sewn in other various wiring or a shift-register-circuit 101a list, and the large field which could wire zigzag for a long time and included shielding wire 82 and 80' in it to the screen-display field further can be wired for a long time in shielding wire 80. Thus, a comparatively easy configuration can raise the effectiveness of the shielding concerned as a whole. Moreover, as shown in drawing 4 (a) and (b), it is formed the various wiring DY, VSSY, --, on the insulating layer 42 between the 1st layer by which VDDX was formed in the TFT array substrate 1, i.e., the same layer. Therefore, the effectiveness of shielding is demonstrated more efficiently. Furthermore, if constituted in this way, since the various wiring DY, VSSY, --, VDDX are put in block according to the same process and can be formed in the manufacture process of liquid crystal equipment 200 from a low resistance metal layer for example, with same aluminum layer etc., it is advantageous on manufacture.

[0066] In addition, the signal LCCOM inputted from the external input terminal 102 shown in drawing 4 from drawing 1 is a power-source signal of a common electrode, and is supplied to the common electrode (refer to drawing 9) prepared in the below-mentioned opposite substrate through Wiring LCCOM and the above-mentioned fish eye 106.

[0067] As shown in the top view of drawing 5 here, capacity line 31' is formed from the conductive polish recon layer same with the scanning line 31 etc. in parallel with the scanning line 31 (gate electrode) on the TFT array substrate 1, and is connected to shielding wire 80 through contact hole 80a. Thus, if constituted, wiring for making capacity line 31' into constant potential can be made to serve a double purpose with shielding wire 80, and an external input terminal required in order to make capacity line 31' into constant potential can also be made to serve a double purpose with the external input terminal 102 for shielding-wire 80.

[0068] Especially with the gestalt of this operation, the sampling circuit 301 is formed on the TFT array substrate 1 in the location which counters the circumference abandonment 53 of the protection-from-light nature formed in the opposite substrate 2 as shown in drawing 6 and drawing 7 , as the slash field in drawing 1 shows, and the data-line drive circuit 101 and the scanning-line drive circuit 104 are formed on the narrow long and slender circumference part of the TFT array substrate 1 which does not face the liquid crystal layer 50. On the TFT array substrate 1, the sealant 52 which consists of a photo-setting resin as an example of the seal member which sticks both substrates in the perimeter of a screen-display field, and surrounds the liquid crystal layer 50 is formed along the screen-display field. And between the screen-display fields and sealants 52 on the opposite substrate 2, the circumference abandonment 53 of protection-from-light nature is formed.

[0069] When put into the TFT array substrate 1 by the case of protection-from-light nature where opening was behind prepared corresponding to the screen-display field, the circumference abandonment 53 so that the screen-display field concerned may not hide in the edge of opening of the case concerned according to a manufacture error etc. That is, it is formed from the band-like protection-from-light nature ingredient which has width of face of at least 500 micrometers or more in the perimeter of a screen-display field so that the gap of about hundreds of micrometers to the case of the TFT array

substrate 1 may be permitted, for example. Such circumference abandonment 53 of protection-from-light nature is formed in the opposite substrate 2 of sputtering, the photolithography process, the etching process, etc. of having used metallic materials, such as Cr (chromium), nickel (nickel), and aluminum (aluminum). Or it is formed from ingredients, such as resin black which distributed carbon and Ti (titanium) to the photoresist. Moreover, the circumference abandonment 53 of protection-from-light nature may be formed on the TFT array substrate 1. If the circumference abandonment 53 is built in on the TFT array substrate 1, since the opening field of a pixel will not be influenced with dispersion in the precision in the lamination process of the TFT array substrate 1 and the opposite substrate 2, the permeability of a liquid crystal panel is maintainable with high precision.

[0070] The data-line drive circuit 101 and the external input terminal (mounting terminal) 102 are formed in the field of the outside of a sealant 52 along the lower side of a screen-display field, and the scanning-line drive circuit 104 is established in the both sides of a screen-display field along with two sides of right and left of a screen-display field. And the opposite substrate 2 with the almost same profile as a sealant 52 has fixed to the TFT array substrate 1 by the sealant 52 concerned.

[0071] as mentioned above, since shielding wire 80 and a sampling circuit 301 are established in the bottom of the circumference abandonment 53 on the TFT array substrate 1, space-saving-ization on the TFT array substrate 1 is attained, for example, can form the scanning-line drive circuit 104 and the data-line drive circuit 101 in the circumference part of the TFT array substrate 1 with allowances, and the display area in liquid crystal equipment 200 also decreases by formation of shielding wire 80 -- most -- or there is completely nothing.

[0072] The leading-about method of the wiring 1-VID 12 between the scanning-line drive circuits 101 and sampling circuits 301 which were shown in drawing 1 and drawing 2 is expanded and shown in drawing 8 (a). In this drawing, the odd-numbered picture signal line slack wiring 1, --, VID 11 and the even-numbered picture signal slack wiring 2, --, VID 12 are taken about by turns in the shape of a ctenidium from both sides for every wiring. therefore, the perimeter of the data-line drive circuit 101 -- setting -- wiring 1-VID 12 and the sampling circuit drive signal line 306 -- very much -- regularity -- good -- and balance -- good -- wiring -- now, it is.

[0073] By the way, with the gestalt of this operation, in order not to degrade liquid crystal by direct-current drive and to prevent the flicker on the display screen, various kinds of methods which reverse liquid crystal driver voltage, for example, the field, a frame reversal drive, a scanning-line reversal drive (the so-called 1H reversal drive), a data-line reversal drive (the so-called 1S reversal drive), a dot reversal drive, etc. are employable. In reversing an electrical-potential-difference polarity among the data lines which adjoin each other, such as 1S reversal and dot reversal, and performing a liquid crystal drive especially here As it is shown in drawing 8 (b) rather than it makes it the shape of a ctenidium every wiring VID 1-12 of one, as shown in drawing 8 (a) While taking about from one side (for example, right-hand side) every two by making into a pair the wiring VID1 of two, 2 and 5, and 6 grades corresponding to the two data lines 35 which adjoin each other, respectively While taking about from a reverse side (for example, left-hand side) every two by making into a pair the wiring VID3 of two, 4 and 7, and 8 grades corresponding to the two data lines 35 with which it adjoins other than these each other, respectively It is more desirable to make it the shape of a ctenidium from both sides by making wiring of two into a pair between the data-line drive circuit 101 and a sampling circuit 301, respectively. Thus, about the noise component which originated in the same noise source which exists in these signals since it was supplied to the data line 35, the picture signal supplied from the wiring 1 of each set which adjoins each other on the TFT array substrate 1 and 2, 3 and 4, and -- having been used as reversed polarity, respectively when wiring, since the effectiveness mutually negated among both who make these each sets works, it is useful to reducing a noise.

[0074] (Configuration of a liquid crystal panel part) Next, the concrete configuration of the liquid crystal panel part which liquid crystal equipment 200 contains is explained with reference to drawing 9 and drawing 10 . It is the sectional view where drawing 9 is a sectional view in TFT30 part of a liquid panel, and drawing 10 met here at the shielding wire 80 of the liquid crystal panel under circumference abandonment. In addition, in order to make each class and each part material into the magnitude of

extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 9 and drawing 10 .
[0075] In the sectional view of drawing 9 , the liquid crystal panel 10 is equipped with an insulating layer 43, the pixel electrode 11, and the orientation film 12 in TFT30 part prepared in each pixel between an insulating layer 42, the data line 35 (source electrode), and the 2nd layer between the semi-conductor layer 32 by which the laminating was carried out to the TFT array substrate 1 list on it, the gate insulating layer 33, the scanning line 31 (gate electrode), and the 1st layer. The liquid crystal panel 10 is equipped with the common electrode 21, the orientation film 22, and the protection-from-light layer 23 by which the laminating was carried out to the opposite substrate 2 list which consists of a glass substrate on it again. The liquid crystal panel 10 is further equipped with the liquid crystal layer 50 pinched among both these substrates.
[0076] Here, the configuration of each class except TFT30 is first explained in order among these layers.

[0077] Insulating layers 42 and 43 consist of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, silicon oxide film, etc. with the thickness of about 5000-15000A between the 1st and the 2nd layer, respectively. In addition, the layer insulation layer used as the substrate of TFT30 may be formed from the silicate glass film, a silicon nitride film, the silicon oxide film, etc. on the TFT array substrate 1.
[0078] The pixel electrode 11 consists of transparent conductive thin films, such as for example, ITO film (Indium Tin Oxide film). Such a pixel electrode 11 is formed by giving a photolithography process and an etching process etc., after depositing the ITO film etc. on the thickness of about 500-2000A by sputtering processing etc. In addition, when using the liquid crystal panel 10 concerned for the liquid crystal equipment of a reflective mold, the pixel electrode 11 may be formed from an opaque ingredient with high reflection factors, such as aluminum.
[0079] The orientation film 12 consists of organic thin films, such as for example, a polyimide thin film. Such orientation film 12 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc., after applying the coating liquid of for example, a polyimide system.
[0080] It goes across the common electrode 21 all over the opposite substrate 2, and it is formed. Such a common electrode 21 deposits the ITO film etc. on the thickness of about 500-2000A for example, by sputtering processing etc., and is formed.
[0081] The orientation film 22 consists of organic thin films, such as for example, a polyimide thin film. Such orientation film 22 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc., after applying the coating liquid of for example, a polyimide system.
[0082] The protection-from-light layer 23 is formed in the predetermined field which counters TFT30. Like the above-mentioned circumference abandonment 53, such a protection-from-light layer 23 is formed of processes, such as sputtering and the photolithography using metallic materials, such as Cr and nickel, and etching, or is formed from ingredients, such as resin black which distributed carbon and Ti to the photoresist. The protection-from-light layer 23 has functions other than the protection from light to the semi-conductor layer (polish recon film) 32 of TFT30, such as improvement in contrast, and color mixture prevention of color material.
[0083] The liquid crystal layer 50 is formed when liquid crystal is enclosed with the space surrounded by the sealant 52 (refer to drawing 6 and drawing 7) between the TFT array substrates 1 and the opposite substrates 2 which have been arranged so that the pixel electrode 11 and the common electrode 21 may meet by vacuum suction etc. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 12 and 22 in the condition that the electric field from the pixel electrode 11 are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant 52 may stick two substrates 1 and 2 around those, and the spacer for making distance between both substrates into a predetermined value is mixed.

[0084] Next, the configuration of each class concerning TFT30 is explained in order.
[0085] TFT30 is equipped with the source field 34 formed in the gate insulating layer 33 which insulates the semi-conductor layer 32 in which a channel is formed of the electric field from the scanning line 31 (gate electrode) and the scanning line 31, and the scanning line 31 and the semi-conductor layer 32, and the semi-conductor layer 32, the data line 35 (source electrode), and the drain field 36 formed in the semi-conductor layer 32. One to which it corresponds of two or more pixel electrodes 11 is connected to the drain field 36. The source field 34 and the drain field 36 are formed by doping the object for the N type of predetermined concentration, or the dopant for P type to the semi-conductor layer 32 like the after-mentioned according to whether the channel of n mold or p mold is formed. TFT of an N type channel has the advantage that a working speed is quick, and it is used as TFT30 which is the switching element of a pixel in many cases.
[0086] The semi-conductor layer 32 which constitutes TFT30 is formed by performing annealing treatment and making the thickness of about 500-2000A carry out solid phase growth after forming the a-Si (amorphous silicon) film for example, on the TFT array substrate 1. Under the present circumstances, in the case of TFT30 of an N channel mold, you may dope by the ion implantation which used the dopant of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn). Moreover, in the case of TFT30 of a p channel mold, it dopes by the ion implantation which used the dopant of III group elements, such as B (boron), Ga (gallium), and In (indium). When setting especially TFT30 to TFT of an N channel mold with LDD (Lightly Doped Drain) structure, among the source field 34 and the drain field 36, a low concentration dope field is formed in the part which adjoins at a channel side, respectively by the dopant of V group elements, such as P, and, similarly a high concentration dope field is formed in the semi-conductor layer 32 of P type by the dopant of V group elements, such as P. Moreover, when referred to as TFT30 of a P channel mold, the dopant of III group elements, such as B, is used for the semi-conductor layer 32 of N type, and the source field 34 and the drain field 36 are formed. Thus, when it considers as LDD structure, the advantage which can reduce the short channel effect is acquired. In addition, TFT30 is good for the low concentration dope field in LDD structure also as TFT of the offset structure which carried out the ion implantation, and good also as TFT of the self aryne mold which forms the source [high concentration / in self align], and a drain field by doping high-concentration impurity ion by using a gate electrode as a mask.
[0087] Moreover, with the gestalt of this operation, two gate electrodes 31 with which the same scan signal is supplied through gate dielectric film 2 between the source drains of TFT30 are formed in drawing 9 , and it is good also as TFT of dual gate (double-gate) structure. Thereby, the leakage current of TFT30 can be reduced. Moreover, if it has above-mentioned LDD structure or offset structure for TFT of dual gate structure, the leakage current of TFT30 can be reduced further and a high contrast ratio can be realized. Moreover, it not only can reduce a pixel defect sharply, but in the time of elevated-temperature actuation, since leakage current is low, the image quality of a high contrast ratio is realizable [with dual gate structure / it can give redundancy, and]. In addition, it cannot be overemphasized that three or more are sufficient as the gate electrode 31 prepared between the source drains of TFT30.
[0088] The gate insulating layer 33 forms and obtains the thermal oxidation film with a comparatively thin thickness of about 300-1500A by oxidizing the semi-conductor layer 32 thermally with the temperature of about 900-1300 degrees C.
[0089] After the scanning line 31 (gate electrode) deposits the polish recon film with a reduced pressure CVD method etc., it is formed of a photolithography process, an etching process, etc. Or it may be formed from the refractory metal film or metal silicide film, such as W (tungsten) and Mo (molybdenum). in this case, it also becomes possible to omit a part or all of the protection-from-light layer 23 by the protection-from-light nature which the metal membrane metallurgy group silicide film has if the protection-from-light layer 23 arranges the scanning line 31 (gate electrode) as the part or the light-shielding film which boils all and corresponds of a wrap field. In this case, there is an advantage which can prevent decline in the pixel numerical aperture by the lamination gap with the opposite substrate 2 and the TFT array substrate 1 especially.

[0090] The data line 35 (source electrode) may be formed from transparent conductive thin films, such as ITO film, like the pixel electrode 11. Or you may form by sputtering processing etc. from low resistance metal metallurgy group silicide, such as aluminum deposited on the thickness of about 1000 to 5000 NA, etc.
[0091] Moreover, the contact hole 38 which leads to the contact hole 37 and the drain field 36 which lead to the source field 34 is formed in the insulating layer 42 between the 1st layer, respectively. Electrical installation of the data line 35 (source electrode) is carried out to the source field 34 through the contact hole 37 to this source field 34. Furthermore, the contact hole 38 to the drain field 36 is formed in the insulating layer 43 between the 2nd layer. Electrical installation of the pixel electrode 11 is carried out to the drain field 36 through the contact hole 38 to this drain field 36. The above-mentioned pixel electrode 11 is formed in the top face of an insulating layer 43 between the 2nd layer constituted in this way. Each contact hole is formed of dry etching, such as for example, reactant etching and reactant ion beam etching.
[0092] In addition, if light carries out incidence of the semi-conductor layer 32 in which a channel is generally formed, a photocurrent will occur according to the photo-electric-conversion effectiveness, the transistor characteristics of TFT30 will deteriorate, but with the gestalt of this operation, since the protection-from-light layer 23 is formed in the location which counters the opposite substrate 2 at each TFT30, respectively, it is prevented that incident light carries out incidence to the semi-conductor layer 32. furthermore, this -- adding -- or -- replacing with -- a gate electrode -- the wrap from a top -- if the data line 35 (source electrode) is formed from opaque metal thin films, such as aluminum, like -- the protection-from-light layer 23 -- or the incidence of the incident light (namely, drawing 9 light from a top) to the semi-conductor layer 32 can be prevented effectively independently.
[0093] In drawing 9 , storage capacitance 70 is formed in the pixel electrode 11, respectively. 1st storage capacitance electrode layer 32' more specifically [this storage capacitance 70] formed of the same process as the semi-conductor layer 32, insulating-layer 33' formed of the same process as the gate insulating layer 33, and the capacity line 31 formed of the same process as the scanning line 31 -- ' (the 2nd storage capacitance electrode) -- It consists of some of insulating layers 42 and 43 and pixel electrodes 11 which counter a list at capacity line 31' through the 1st and the insulating layers 42 and 43 between the 2nd layer between the 1st and the 2nd layer. Thus, since storage capacitance 70 is formed, even if duty ratio is small, a high definition display is enabled.
[0094] As shown in the sectional view of drawing 10 , the circumference abandonment 53 is countered and shielding wire 80 passes through an insulating-layer 42 top between the 1st layer in the upper location of two or more scanning lines 31. and it consists of metal thin films, such as aluminum formed at the process as the data line (source electrode) 35 mentioned above that almost all those parts of this shielding wire 80 are the same, -- low -- it is wiring [****]. Thus, in the manufacture process of liquid crystal equipment 200, since shielding wire 80 and the data line 35 can be formed collectively, it is advantageous on manufacture.
[0095] Since the circumference circuit which is the same film formation process, and a sampling circuit 301, the data-line drive circuit 101, and scanning-line drive circuit 104 grade are the same, and consisted of poly-Si TFT type TFT302 grades at the time of formation of TFT30 since TFT30 was polish recon type TFT especially with the gestalt of this operation can be formed, it is advantageous on manufacture. For example, these circumference circuits are formed in the circumference part on the TFT array substrate 1 from two or more TFT(s) of the complementary structure which consists of N channel mold poly-Si TFT and P channel mold poly-Si TFT.
[0096] In addition, although not shown in drawing 9 and drawing 10 , it sets to a liquid crystal panel 10. To the side in which the incident light of the side in which the incident light of the opposite substrate 2 carries out incidence, and the TFT array substrate 1 carries out outgoing radiation, respectively For example, TN (Twisted Nematic) mode and STN (super TN) mode, According to the exception of modes of operation, such as D-STN (double-STN) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, a polarizing plate, etc. are arranged in a predetermined direction.

[0097] Moreover, since the liquid crystal panel 10 explained above is applied to an electrochromatic display projector, three liquid crystal panels 10 will be used as a light valve for RGB, respectively, and incidence of the light of each color decomposed through the dichroic mirror for RGB color separation, respectively will be carried out to each panel as incident light, respectively. Therefore, with the gestalt of each operation, the color filter is not prepared in the opposite substrate 2. However, the color filter of RGB may be formed in the predetermined field which counters the pixel electrode 11 with which the protection-from-light layer 23 is not formed in the liquid crystal panel 10 on the opposite substrate 2 with the protective coat. If it does in this way, the liquid crystal panel of the gestalt of this operation is applicable to electrochromatic display equipments, such as electrochromatic display television of direct viewing types other than a liquid crystal projector, or a reflective mold. Furthermore, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 2. If it does in this way, a bright liquid crystal panel is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 2 again may be formed. According to this opposite substrate with a die clo IKKU filter, a brighter electrochromatic display panel is realizable.

[0098] In order to set to a liquid crystal panel 10 and to control the poor orientation of the liquid crystal molecule by the side of the TFT array substrate 1, the flattening film may be further applied on a spin coat etc. on an insulating layer 43 between the 2nd layer, or CMP processing may be performed. Or an insulating layer 43 may be formed by the flattening film between the 2nd layer.

[0099] Although it was explained that the switching element of a liquid crystal panel 10 was the poly-Si TFT of a forward stagger mold or a coplanar mold, the gestalt of this operation is effective also to TFT of other formats, such as TFT of a reverse stagger mold, and an amorphous silicon TFT.

[0100] In a liquid crystal panel 10, although the liquid crystal layer 50 was constituted from a pneumatic liquid crystal as an example, if the polymer dispersed liquid crystal which distributed liquid crystal as a minute grain in the macromolecule is used, the above-mentioned polarization film, a polarizing plate, etc. will become unnecessary in the orientation film 12 and 22 and a list, and the advantage of a raise in the brightness of a liquid crystal panel or low-power-izing by efficiency for light utilization increasing will be acquired. Furthermore, when applying a liquid crystal panel 10 to high-reflective-liquid-crystal equipment by constituting the pixel electrode 11 from a metal membrane with high reflection factors, such as aluminum, SH (super HOMEOTORO pick) mold liquid crystal with which perpendicular orientation of the liquid crystal molecule was mostly carried out in the state of no electrical-potential-difference impressing may be used. Furthermore, although the common electrode 21 is provided in the opposite substrate 2 side in the liquid crystal panel 10 again so that perpendicular electric field (vertical electric field) may be impressed to the liquid crystal layer 50 What (that is, the electrode for horizontal electric-field generating is prepared in the TFT array substrate 1 side, without preparing the electrode for vertical electric-field generating in the opposite substrate 2 side) the pixel electrode 11 is constituted also for from an electrode for horizontal electric-field generating of a pair, respectively so that electric field (horizontal electric field) parallel to the liquid crystal layer 50 may be impressed is possible. Thus, if horizontal electric field are used, it is advantageous when extending an angle of visibility rather than the case where vertical electric field are used. In addition, it is possible to apply the gestalt of this operation to various kinds of liquid crystal ingredients (liquid crystal layer), a mode of operation, a liquid crystal array, the drive approach, etc.

[0101] In the gestalt of the operation explained above, well-known circumference circuits, such as a precharge circuit and an inspection circuit, may be further established in the periphery of the bottom of the circumference abandonment 53, or the TFT array substrate 1. A precharge circuit is the timing preceded with the data signal supplied from a data-line drive circuit to the data line for the purpose of reduction of improvement in a contrast ratio, the stability of the potential level of the data line, and the Rhine unevenness on a display screen etc., and is a circuit which mitigates the load at the time of writing a data signal in the data line by supplying a precharge signal. For example, an example of such a precharge circuit is indicated by JP,7-295520,A. On the other hand, an inspection circuit is a circuit for

inspecting the quality of the liquid crystal equipment concerned at the manufacture middle or the time of shipment, a defect, etc. to the periphery of the bottom of the circumference abandonment 53, or a TFT array substrate.
[0102] Moreover, in the gestalt of the above operation, the protection-from-light layer which consists of refractory metal metallurgy group silicide, such as W (tungsten) and Mo (molybdenum), may be prepared also in the location (namely, under TFT30) which counters on the TFT array substrate 1 at TFT30 as indicated by JP,9-127497,A, JP,3-52611,B, JP,3-125123,A, JP,8-171101,A, etc. Thus, if a protection-from-light layer is prepared also in the TFT30 bottom, it can prevent that the return light from the TFT array substrate 1 side etc. carries out incidence to TFT30. Therefore, the liquid crystal equipment 200 concerned can be suitably used as a light valve for liquid crystal projectors.
[0103] Furthermore, in the gestalt of the above operation, it may replace with TFT30 and a switching element may consist of 2 terminal mold nonlinear devices, such as MIM (Metal Insulator Metal), etc. again. In this case, arrange one line to an opposite substrate among the data line and the scanning line, and it is made to function as a counterelectrode, and a switching element is arranged, respectively between the line of another side established in the TFT array substrate, and a pixel electrode, and a liquid crystal drive is carried out between. Thus, even if constituted, the effectiveness of preventing the diving to the picture signal and data signal of a clock noise of high frequency is demonstrated by shielding a pixel signal line and the data line from a clock signal line.
[0104] (Actuation of liquid crystal equipment) Next, actuation of the liquid crystal equipment 200 constituted as mentioned above is explained with reference to drawing 1 .
[0105] First, the scanning-line drive circuit 104 impresses a scan signal to the scanning line 31 by line sequential in pulse to predetermined timing.
[0106] If a parallel picture signal is received from the wiring VID1-VID12 of 12 in parallel to this, a sampling circuit 301 will sample these picture signals. The scanning-line drive circuit 104 supplies a sampling circuit driving signal for every data line about wiring [of 12] VID1 - VID12 each according to the timing which impresses gate voltage, and the data-line drive circuit 101 makes TFT302 of a sampling circuit 301 an ON state. Thereby, sequential impression of the data signal sampled by the sampling circuit 301 is carried out to the 12 adjoining data lines 35. That is, the parallel picture signals VID1-VID12 which were inputted from wiring VID1-VID12 and which were developed 12 phases are supplied to the data line 35 by the data-line drive circuit 101 and the sampling circuit 301.
[0107] Thus, in TFT30 to which both the scan signal (gate voltage) and the data signal (source electrical potential difference) were impressed, an electrical potential difference is impressed to the pixel electrode 11 through the channel and the drain field 36 which were formed in the source field 34 and the semi-conductor layer 32. And as for the electrical potential difference of this pixel electrode 11, only time amount also with triple figures longer than the time amount to which the source electrical potential difference was impressed is held with storage capacitance (refer to drawing 9). Since especially the wiring VID1-VID12 is shielded by shielding wire 80, 80', and 82 and 86 from wiring ENB1 and ENB2 at Wiring CLX and a CLX' list, even when the frequency of a clock signal CLX is high, diving, such as a clock noise of the RF to the wiring VID1-VID12 from wiring ENB1 and ENB2, can be reduced in Wiring CLX and a CLX' list here.
[0108] As mentioned above, if an electrical potential difference is impressed to the pixel electrode 11, the orientation condition of the liquid crystal in the part pinched by this pixel electrode 11 and common electrode 21 in the liquid crystal layer 50 changes, and if it is in no MARI White mode According to the impressed electrical potential difference, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from a liquid crystal panel 10 as a whole.
[0109] image quality deteriorates according to generating of the clock noise of a RF, using [the resolution of the image which should be displayed is high the above result, and] the clock signal CLX with a high frequency corresponding to this, also when the serial picture signals VID1-VID12 of a RF are inputted -- most -- or it is completely lost and high-definition image display is made possible. And it

is supposed by dropping the frequency of a picture signal on many phases comparatively, as a result of [of 12 phase expansion] carrying out phase expansion that it is possible to usually sample by the sampling circuit of the engine performance.
[0110] (Electronic equipment) Next, the gestalt of operation of electronic equipment equipped with the liquid crystal equipment 200 explained to the detail above is explained with reference to drawing 15 from drawing 11 .
[0111] The outline configuration of the electronic equipment which equipped drawing 11 with liquid crystal equipment 200 in this way is shown first.
[0112] In drawing 11 , electronic equipment is constituted in preparation for the source 1000 of a information output, the display information processing circuit 1002, the drive circuit 1004, a liquid crystal panel 10, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a TV signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a phase expansion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the drive circuit 1004 with a clock signal CLK. The drive circuit 1004 drives a liquid crystal panel 10. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes a liquid crystal panel 10, the drive circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.
[0113] Next, the example of the electronic equipment constituted in this way from drawing 12 by drawing 15 is shown, respectively.
[0114] In drawing 12 , an example slack liquid crystal projector 1100 of electronic equipment prepares three liquid crystal modules with which the drive circuit 1004 mentioned above contains the liquid crystal panel 10 carried on the TFT array substrate, and is constituted as a projector used as light valves 100R, 100G, and 100B for RGB, respectively. In a liquid crystal projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be led to the light valves 100R, 100G, and 100B corresponding to each color, respectively. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors modulated with light valves 100R, 100G, and 100B, respectively is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.
[0115] If the protection-from-light layer is especially prepared also in the TFT bottom as mentioned above in the gestalt of this operation The reflected light by the incident light study system in the liquid crystal projector based on the incident light from the liquid crystal panel 10 concerned, A part of incident light (a part of R light and G light) which runs through a dichroic prism 1112 after carrying out outgoing radiation from the reflected light from the front face of the TFT array substrate at the time of incident light passing and other liquid crystal panels Even if it carries out incidence from a TFT array substrate side as a return light, protection from light to channels, such as TFT for switching of a pixel electrode, can fully be performed. In this case, in a configuration, since it becomes unnecessary to stick AR film for return light prevention, or to perform AR coat processing between the TFT array substrate of each liquid crystal panel and prism at a polarizing plate even if it uses the prism suitable for a miniaturization for an incident light study system, small and when being simplified, it is very advantageous.

[0116] In drawing 13 , other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic equipment (PC) are equipped with the body 1204 with which the keyboard 1202 was incorporated while it has the liquid crystal panel 10 mentioned above in the top covering case and they hold CPU, memory, a modem, etc. further.
[0117] In drawing 14 , the drive circuit 1004 of the above-mentioned [other example slack pagers 1300 of electronic equipment] in the metal frame 1302 is held in the light guide [in which the liquid crystal panel 10 which is carried at a TFT array substrate top and forms a liquid crystal module contains back light 1306a] 1306, circuit board 1308, 1st, and 2nd shielding plates 1310 and 1312 or 2 elastic conductors 1314 and 1316, and a list with the tape carrier package tape 1318. In the case of this example, the above-mentioned display information processing circuit 1002 (refer to drawing 11) may be carried in the circuit board 1308, and may be carried on the TFT array substrate of a liquid crystal panel 10. Furthermore, it is also possible to carry the above-mentioned drive circuit 1004 on the circuit board 1308.
[0118] In addition, since the example shown in drawing 14 is a pager, the circuit board 1308 grade is prepared. However, it is also possible to carry out production, sale, use, etc. as back light-type liquid crystal equipment which incorporated [in the case of the drive circuit 1004 or the liquid crystal panel 10 which carries the display information processing circuit 1002 further, and forms a liquid crystal module] the light guide 1306 by using as liquid crystal equipment what fixed the liquid crystal panel 10 in the metal frame 1302 in addition to this.
[0119] moreover, as shown in drawing 15 , in the case of the liquid crystal panel 10 which carries neither the drive circuit 1004 nor the display information processing circuit 1002 To TCP (Tape Carrier Package)1320 mounted on the polyimide tape 1322, IC1324 including the drive circuit 1004 or the display information processing circuit 1002 It is also possible to connect physically and electrically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 1, and to carry out production, sale, use, etc. as liquid crystal equipment.
[0120] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 15 from drawing 12 above etc. is mentioned as an example of the electronic equipment shown in drawing 11 .
[0121] According to the gestalt of this operation, as explained above, generating of the clock noise of a RF is reduced, high-definition image display is possible and various kinds of electronic equipment by which the screen-display field was moreover equipped with large liquid crystal equipment 200 compared with substrate size can be realized.
[0122]
[Effect of the Invention] According to the electro-optic device of this invention, by the electric conduction line of the constant potential wired by the substrate, since the picture signal line is shielded from control signal lines, such as a clock signal line, diving, such as a clock noise of the RF from a signal line to a picture signal line, can be reduced, and high-definition image display can be performed according to the picture signal of the high frequency for displaying the image of high resolution. And also when drawing a picture signal line to the both sides of a data signal supply means and wiring the picture signal line of a large number corresponding to polyphase expansion by the ****** configuration, the both sides of a data signal supply means can be wired with sufficient balance, and it also becomes possible to attain enlargement of the screen in the limited substrate size. Moreover, by shielding a screen-display field and two or more data lines, generating of the clock noise of a RF in the data signal on the data line etc. can be reduced, and more nearly high-definition image display becomes possible.
[0123] Moreover, according to the electronic equipment of this invention, the clock noise of a RF is reduced and it becomes realizable compared with substrate size about various electronic equipment, such as the liquid crystal projector and personal computer in which high-definition image display with a large screen-display field is possible, and a pager.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] They are outline top views containing the shielding wire formed on the TFT array substrate in the gestalt of operation of liquid crystal equipment, such as various wiring and a circumference circuit.
[Drawing 2] It is the outline top view showing more the two-dimensional layout of the shielding wire of drawing 1 in a detail.
[Drawing 3] It is the circuit diagram (a) and timing chart (b) in the shift register circuit shown in drawing 2 .
[Drawing 4] It is the A-A'sectional view (a) and B-B' sectional view (b) of the shielding wire formed on the TFT array substrate of drawing 1 , a picture signal line, and a clock signal line.
[Drawing 5] It is an expansion top view in screen-display field edges, such as a pixel electrode formed on the TFT array substrate of drawing 1 , the scanning line, and data.
[Drawing 6] It is the top view showing the whole liquid crystal equipment configuration of drawing 1 .
[Drawing 7] It is the sectional view showing the whole liquid crystal equipment configuration of drawing 1 .
[Drawing 8] It is the outline top view (b) showing the outline top view (a) and other examples which show an example of the two-dimensional layout of the picture signal line (wiring 1-VID 12) of drawing 1 .
[Drawing 9] It is a sectional view in the TFT part prepared in the screen-display field of the liquid crystal equipment of drawing 1 .
[Drawing 10] It is a sectional view in the shielding-wire part prepared in the circumference sacrifice field of the liquid crystal equipment of drawing 1 .
[Drawing 11] It is the block diagram showing the outline configuration of the gestalt of operation of the electronic equipment by this invention.
[Drawing 12] It is the sectional view showing the liquid crystal projector as an example of electronic equipment.
[Drawing 13] It is the front view showing the personal computer as other examples of electronic equipment.
[Drawing 14] It is the decomposition perspective view showing the pager as an example of electronic equipment.
[Drawing 15] It is the perspective view showing the liquid crystal equipment using TCP as an example of electronic equipment.
[Description of Notations]
1 -- TFT array substrate
2 -- Opposite substrate
10 -- Liquid crystal panel
11 -- Pixel electrode
12 -- Orientation film

21 -- Common electrode
22 -- Orientation film
23 -- Protection-from-light layer
30 -- TFT
31 -- Scanning line (gate electrode)
32 -- Semi-conductor layer
33 -- Gate insulating layer
34 -- Source field
35 -- Data line (source electrode)
36 -- Drain field
37 38 -- Contact hole
42 -- Insulating layer between the 1st layer
43 -- Insulating layer between the 2nd layer
50 -- Liquid crystal layer
52 -- Sealant
53 -- Circumference abandonment
70 -- Storage capacitance
82 80, 80', 86 -- Shielding wire (constant potential line)
101 -- Data-line drive circuit
102 -- External input terminal (mounting terminal)
104 -- Scanning-line drive circuit
112 -- Enabling circuit
200 -- Liquid crystal equipment
301 -- Sampling circuit
302 -- TFT

[Translation done.]

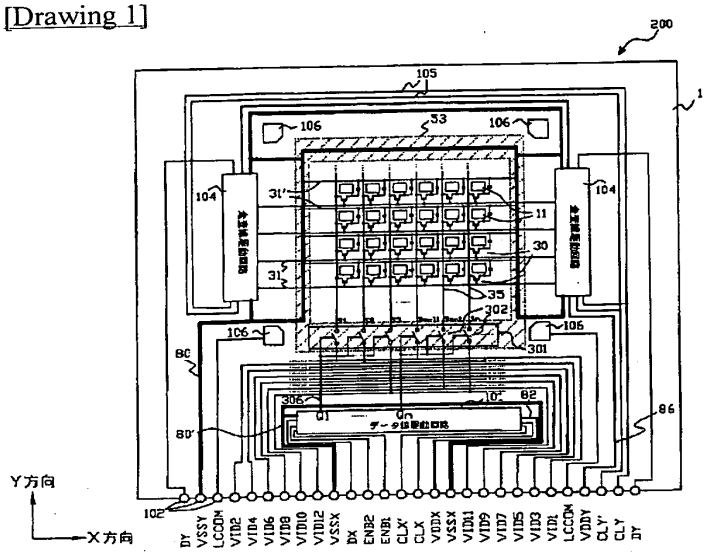
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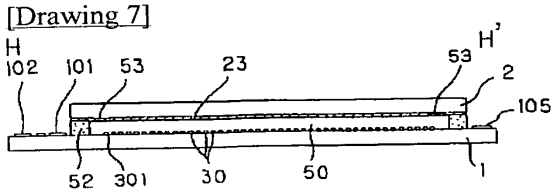
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DRAWINGS

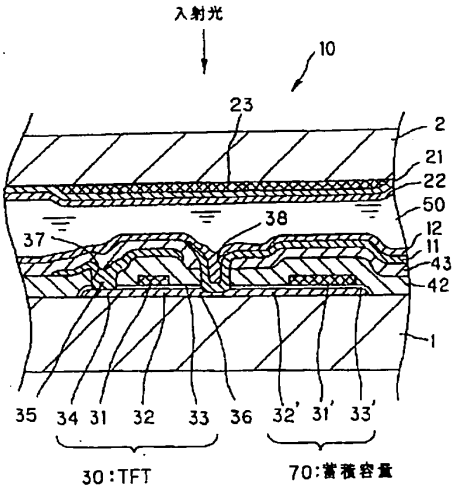
[Drawing 1]



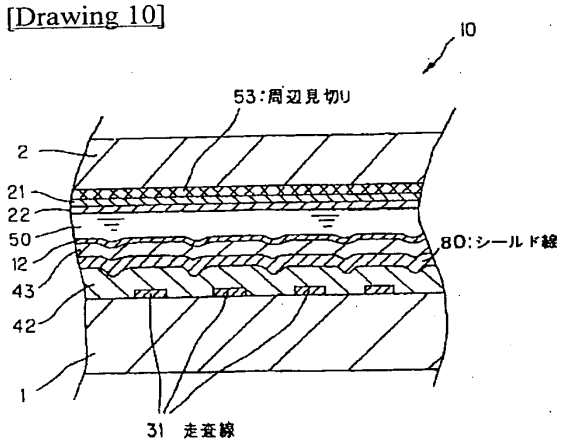
[Drawing 7]



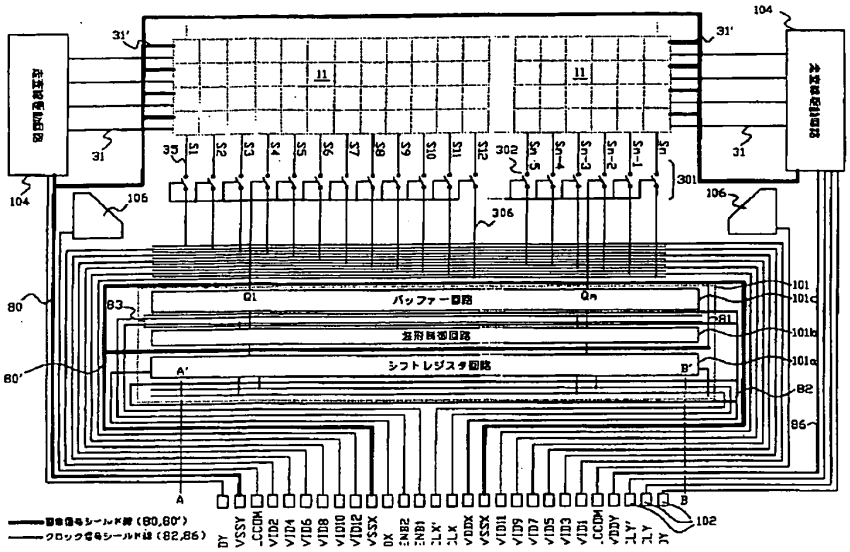
[Drawing 9]



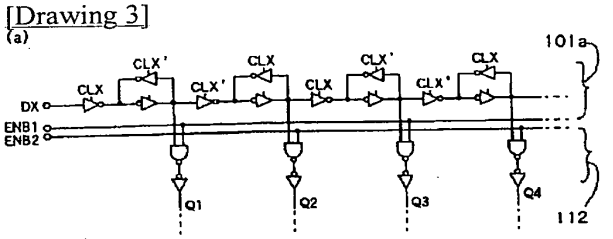
[Drawing 10]

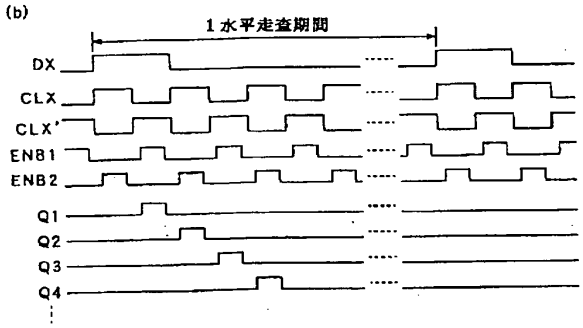


[Drawing 2]

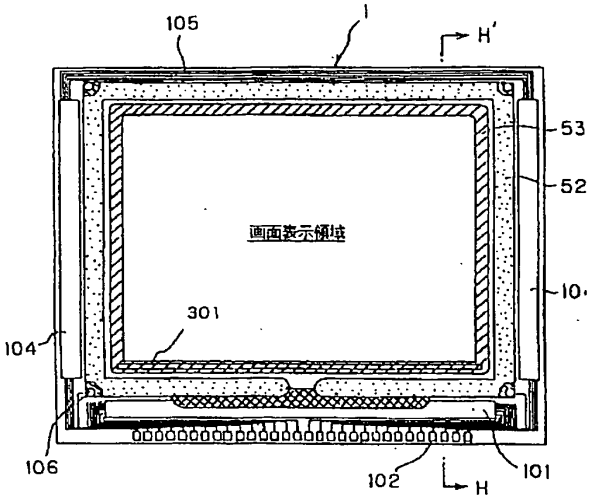


[Drawing 3]

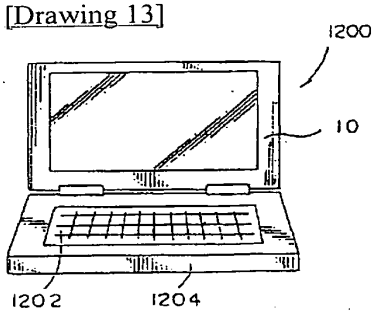




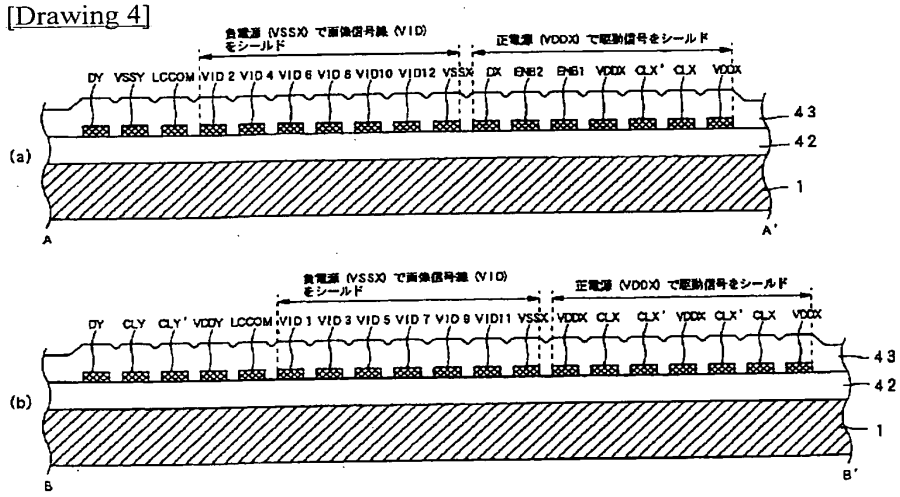
[Drawing 6]



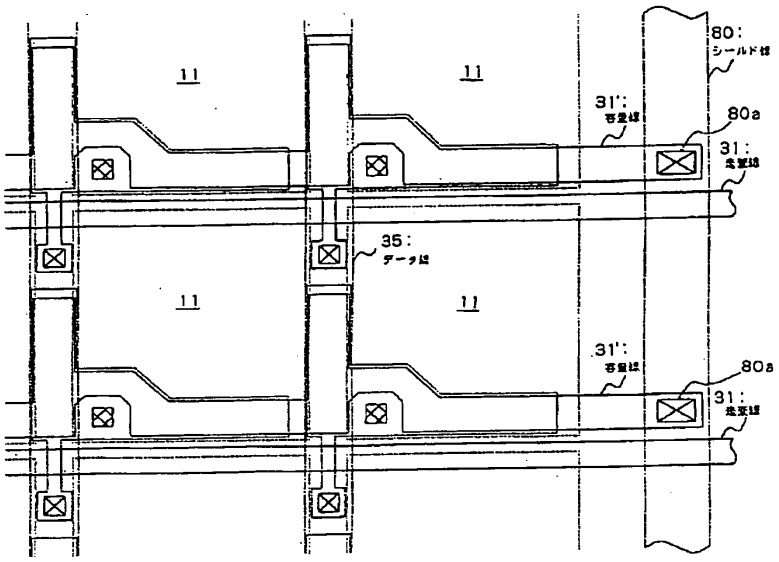
[Drawing 13]



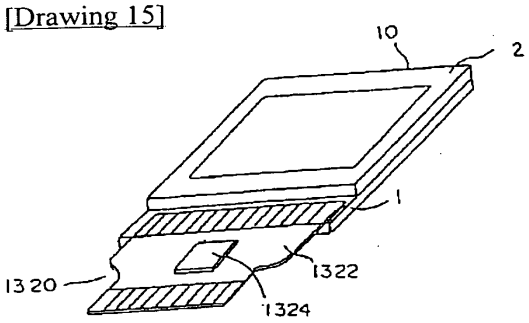
[Drawing 4]



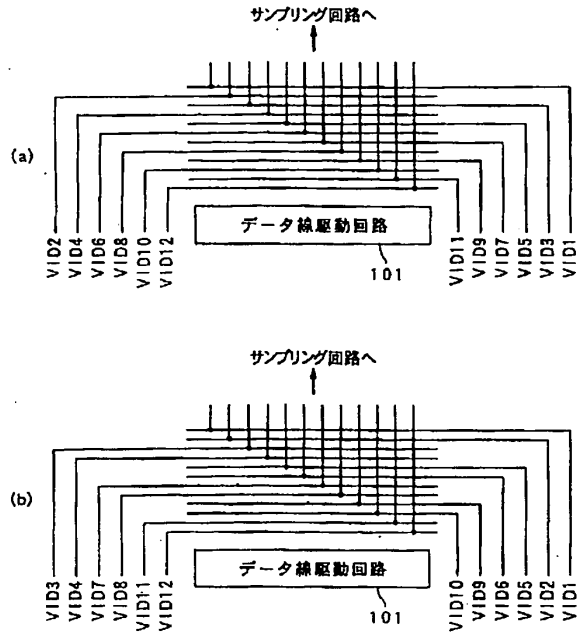
[Drawing 5]



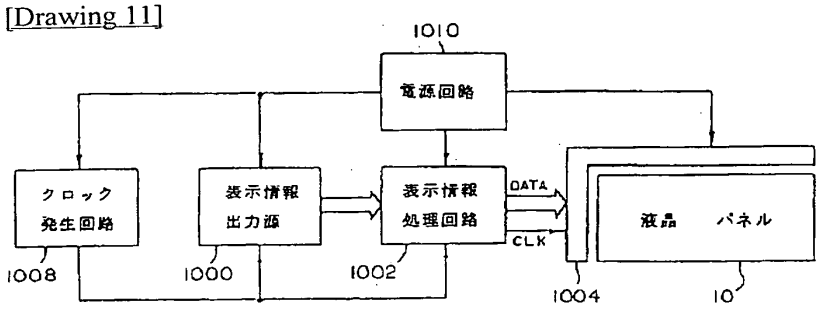
[Drawing 15]



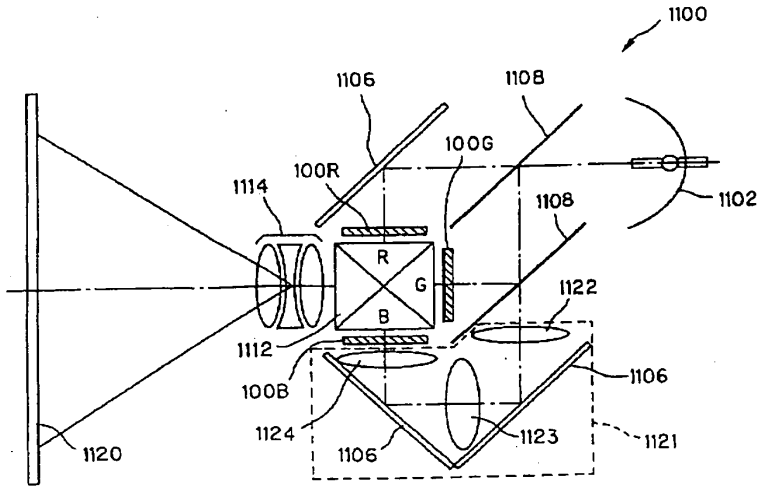
[Drawing 8]



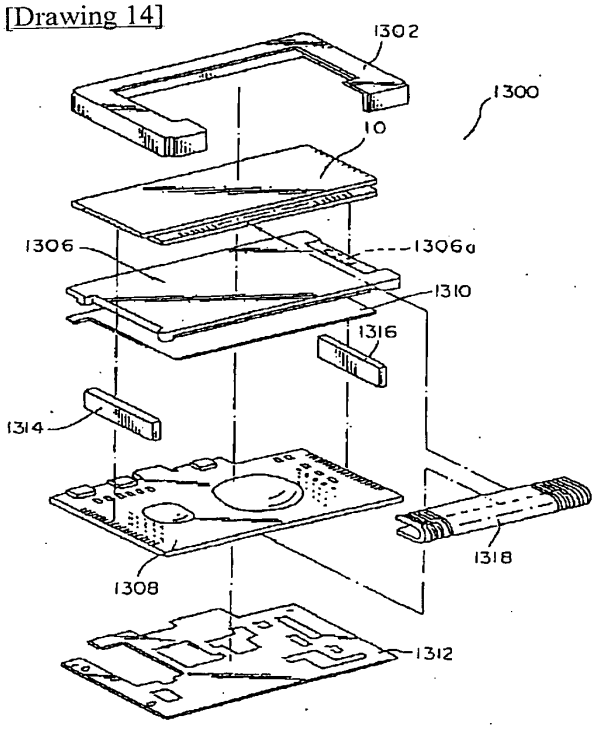
[Drawing 11]



[Drawing 12]



[Drawing 14]



[Translation done.]

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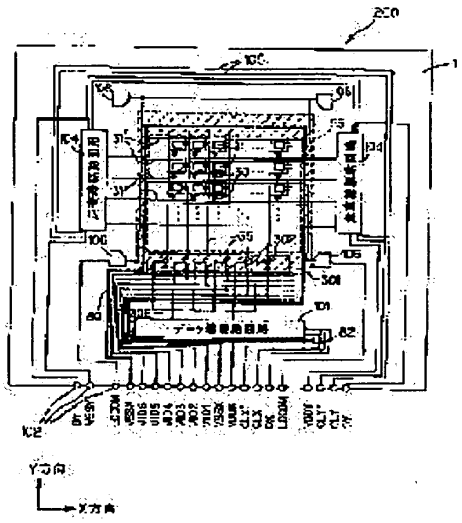
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(71)Applicant : SEIKO EPSON CORP
(72)Inventor : MURADE MASAO

(30)Priority
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(54) ELECTROOPTIC DEVICE AND ELECTRONIC EQUIPMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the occurrence of high frequency clock noise in an inputted image signal and a data signal formed on the basis thereof in an electrooptic device such as an active matrix drive type liquid crystal device.
SOLUTION: A liquid crystal device 200 has a liquid crystal layer sandwiched between a couple of substrates, pixel electrodes 11 provided in matrix on the substrate 1, and TFTs 30 which perform switching control over the electrodes, Shield wires 80 and 82 of a constant potential which electrically shield image signal lines VID1 to VID6 from clock signal lines CLX and CLX' are wired on the substrates. Thus, a high quality image can be displayed according to the high frequency image signal for displaying a high resolution image.



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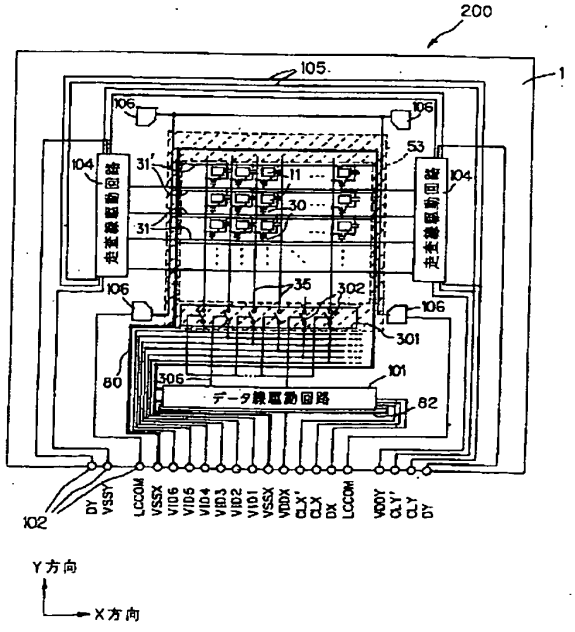
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(54)【発明の名称】　電気光学装置及び電子機器

(57)【要約】

【課題】　アクティブマトリクス駆動方式の液晶装置等の電気光学装置において、入力された画像信号中やこれに基づいて生成されるデータ信号中の高周波のクロックノイズの発生を低減する。

【解決手段】　液晶装置（２００）は、一対の基板間に挟持された液晶層と、基板（１）にマトリクス状に設けられた画素電極（１１）と、これをスイッチング制御するＴＦＴ（３０）とを備える。画像信号線（ＶＩＤ１～ＶＩＤ６）をクロック信号線（ＣＬＸ、ＣＬＸ’）から電気的にシールドする定電位のシールド線（８０、８２）が基板上に配線されている。



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【特許請求の範囲】

【請求項１】　基板上には複数の走査線と、前記複数の走査線に交差する複数のデータ線と、前記複数の走査線とデータ線に接続された複数のスイッチング素子と、前記複数のスイッチング素子に接続された複数の画素電極と、クロック信号に基づいて画像信号に対応するデータ信号を前記複数のデータ線に供給するデータ信号供給手段と、第１外部入力端子から入力される前記画像信号を前記データ信号供給手段に供給する画像信号線と、第２外部入力端子から入力される前記クロック信号を前記データ信号供給手段に供給するクロック信号線と、前記画像信号線を前記クロック信号線から電気的にシールドする定電位の導電線とを備えたことを特徴とする電気光学装置。

【請求項２】　前記導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むことを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、

該第１定電位線から構成された前記導電線部分は、前記基板上で前記画像信号線を囲み、

前記第２定電位線から構成された前記導電線部分は、前記基板上で前記クロック信号線を囲むことを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記定電位線からの電源供給を受けて前記クロック信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記画像信号線と前記クロック信号線とは、前記基板上で前記データ線駆動回路に対して反対方向から引き回されていることを特徴とする請求項２又は３に記載の電気光学装置。

【請求項５】　前記第１及び第２外部入力端子は、前記基板の周辺部において相互に所定間隔を隔てて配置されており、前記第１及び第２外部入力端子の間には、前記定電位の電源を前記定電位線に入力するための第３外部入力端子が配置されていることを特徴とする請求項２から４のいずれか一項に記載の電気光学装置。

【請求項６】　前記導電線は、前記複数の画素電極により規定される画像表示領域及び前記複数のデータ線を前記第１基板上で囲むように延設されたこと特徴とする請求項１から５のいずれか一項に記載の電気光学装置。

【請求項７】　前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁を更に備えており、

前記導電線は前記額縁に対向する位置において前記額縁に沿って前記基板に設けられた部分を含むことを特徴とする請求項６に記載の電気光学装置。

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【請求項８】　前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記画像信号線及びクロック信号線の間に介在する前記導電線部分並びに前記画像信号線及びクロック信号線は、前記基板に平行な同一平面上に形成された同一の低抵抗金属層から構成されたことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。

【請求項１０】　前記画素電極に所定量の容量を付与する容量線を更に備えており、該容量線が前記導電線に接続されたことを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁と、前記画素電極に容量を付与する容量線とを更に備えており、前記導電線は前記額縁に対向する位置に延設されるとともに、前記対向する位置において前記導電線に前記容量線が接続されていることを特徴とする請求項１から６のいずれか一項に記載の電気光学装置。

【請求項１２】　請求項１から１１に記載の電気光学装置を備えたことを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、薄膜トランジスタ（以下適宜、ＴＦＴと称す）駆動によるアクティブマトリクス駆動方式の電気光学装置及びこれを用いた電子機器の技術分野に属し、特に、ＴＦＴアレイ基板上に設けられたデータ線駆動回路によりクロック信号に基づいてデータ線を高周波で駆動する形式の電気光学装置及びこれを用いた電子機器の技術分野に属する。

【０００２】

【従来の技術】従来、ＴＦＴ駆動によるアクティブマトリクス駆動方式の液晶装置等の電気光学装置においては、縦横に夫々配列された多数の走査線及びデータ線並びにこれらの各交点に対応して多数の画素電極がＴＦＴアレイ基板上に設けられている。そして、これらに加えて、データ線駆動回路、サンプリング回路等を含みデータ線にデータ信号を供給するデータ信号供給手段や、走査線駆動回路等を含み走査線に走査信号を供給する走査信号供給手段が、このようなＴＦＴアレイ基板上に設けられる場合がある。

【０００３】この場合、データ信号供給手段には、データ信号の供給タイミングの基準となるデータ線側基準クロック、表示すべき画像の内容に対応しておりデータ信号の基となる画像信号、正や負の定電位電源等が、ＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して夫々供給される。他方、走査信号供給手段には、走査

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信号の供給タイミングの基準となる走査線側基準クロック、正や負の定電位電源等が、やはりＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して供給される。そして走査信号供給手段においては、例えば走査線駆動回路により、走査線側基準クロックに基づくタイミングで走査信号を走査線に線順次で供給する。これに対応してデータ信号供給手段においては、例えば入力された画像信号をサンプリングするサンプリング回路を、データ線駆動回路がデータ線側基準クロックに基づくタイミングで順次駆動して、サンプリング回路からデータ信号がデータ線に供給される。これらの結果、走査線にゲート接続された各ＴＦＴは、走査信号の供給に応じて導通状態とされ、データ信号が当該ＴＦＴを介して画素電極に供給されて各画素における画像表示が行われる。

【０００４】近年特に、液晶プロジェクタ用の液晶装置等では、表示画像の高解像度化に伴って、非常に高い周波数のシリアルな画像信号が入力されるようになってきている。これに対応すべく、特にデータ信号供給手段に供給されるデータ線側基準クロックの周波数も非常に高くされる。

【０００５】

【発明が解決しようとする課題】しかしながら、近年の表示画像の高品位化の要請の下では、このように基準クロックの周波数を高くすることによる、高周波のクロックノイズの発生が無視し得ないようになる。

【０００６】即ち、例えば従来の比較的周波数の低いデータ線側基準クロックをデータ線駆動回路に供給してサンプリング回路を駆動する構成において、そのままクロック信号の周波数を上げたのでは、サンプリング回路に入力される画像信号中やサンプリング回路から出力されるデータ信号中に高周波のクロックノイズが発生して、データ線に供給すべきデータ信号が劣化してしまう。このように劣化したデータ信号の供給を受けたのでは、各画素電極により表示される画像もやはり劣化してしまうという問題点がある。

【０００７】本発明は上述の問題点に鑑みなされたものであり、入力された画像信号中やこれに基づいて生成されるデータ信号中の高周波のクロックノイズの発生を低減でき、高品位の画像表示を行える電気光学装置及び当該電気光学装置を備えた電子機器を提供することを課題とする。

【０００８】

【課題を解決するための手段】請求項１に記載の電気光学装置は上記課題を解決するために、基板上には複数の走査線と、前記複数の走査線に交差する複数のデータ線と、前記複数の走査線とデータ線に接続された複数のスイッチング素子と、前記複数のスイッチング素子に接続された複数の画素電極と、クロック信号に基づいて画像信号に対応するデータ信号を前記複数のデータ線に供給するデータ信号供給手段と、第１外部入力端子から入力

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される前記画像信号を前記データ信号供給手段に供給する画像信号線と、第２外部入力端子から入力される前記クロック信号を前記データ信号供給手段に供給するクロック信号線と、前記画像信号線を前記クロック信号線から電気的にシールドする定電位の導電線とを備えたことを特徴とする。

【０００９】請求項１に記載の電気光学装置によれば、第１外部入力端子から入力される画像信号は、基板に配線された画像信号線を介して、データ信号供給手段に供給される。これと並行して、第２外部入力端子から入力されるクロック信号は、基板に配線されたクロック信号線を介して、データ信号供給手段に供給される。すると、基板に設けられた、例えばデータ線駆動回路、サンプリング回路等を含んで構成されるデータ信号供給手段により、クロック信号に基づいて画像信号に対応するデータ信号が、複数のデータ線に供給される。ここで特に、基板に配線された定電位の導電線により、画像信号線は、クロック信号線から電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。

【００１０】他方で、基板に形成されるか又は基板に接続された走査線駆動回路等を含む走査信号供給手段により、走査信号が走査線を介してスイッチング素子に供給される。これと並行して、上述のように高周波のクロックノイズが低減された画像信号に対応するデータ信号が、データ線を介してスイッチング素子に供給され、更にスイッチング素子を介して供給されるデータ信号により画素電極に印加される電圧が変化し、当該画素電極に対向する液晶が駆動される。以上の結果、表示すべき画像の解像度が高く、高周波のシリアルな画像信号が入力される場合にも、これに対応して周波数が高いクロック信号を用いつつ、高周波のクロックノイズの発生により画質が劣化することは殆ど又は全く無くなり、高品位の画像表示が可能とされる。

【００１１】請求項２に記載の電気光学装置は請求項１に記載の電気光学装置において、前記導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むことを特徴とする。

【００１２】請求項２に記載の電気光学装置によれば、導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むので、外部入力端子や配線そのものを共用することにより、言い換えれば定電位線を延設して導電線とすることにより、構成の簡略化と省スペース化を図ることが出来、特に導電線を定電位とすることも極めて容易となる。

【００１３】請求項３に記載の電気光学装置は請求項２に記載の電気光学装置において、前記定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、該第１定電位線から構

成された前記導電線部分は、前記基板上で前記画像信号線を囲み、前記第２定電位線から構成された前記導電線部分は、前記基板上で前記クロック信号線を囲むことを特徴とする。

【００１４】請求項３に記載の電気光学装置によれば、画像信号線は、例えば接地電位の負電源を供給するための第１定電位線から構成された導電線部分により、基板上で囲まれている。クロック信号線は、例えば正電源を供給するための第２定電位線から構成された導電線部分により、基板上で囲まれている。従って、画像信号線は、基板上でクロック信号線から２重にシールドされた構成が得られる。

【００１５】請求項４に記載の電気光学装置は請求項２又は３に記載の電気光学装置において、前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記定電位線からの電源供給を受けて前記クロック信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記画像信号線と前記クロック信号線とは、前記基板上で前記データ線駆動回路に対して反対方向から引き回されていることを特徴とする。

【００１６】請求項４に記載の電気光学装置によれば、走査信号供給手段において、画像信号は、サンプリング回路によりサンプリングされる。そして、定電位線からの電源供給を受けるデータ線駆動回路により、クロック信号に基づいてサンプリング回路が駆動されて、サンプリングされた画像信号がデータ信号としてデータ線に供給される。ここで特に、画像信号線とクロック信号線とは、基板上でデータ線駆動回路に対して反対方向から引き回されているが、一般に距離及び障害物の介在に応じて電磁波は減少するので、クロック信号線から画像信号線に印加される電磁波が両信号線間の距離に応じて且つデータ線駆動回路の存在に応じて減少する。従って、クロック信号の周波数が高い場合でも、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを更に低減できる。

【００１７】請求項５に記載の電気光学装置は請求項２から４のいずれか一項に記載の電気光学装置において、前記第１及び第２外部入力端子は、前記基板の周辺部において相互に所定間隔を隔てて配置されており、前記第１及び第２外部入力端子の間には、前記定電位の電源を前記定電位線に入力するための第３外部入力端子が配置されていることを特徴とする。

【００１８】請求項５に記載の電気光学装置によれば、第１及び第２外部入力端子は、第３外部入力端子を間に介して、基板の周辺部において相互に所定間隔を隔てて配置されており、好ましくは、基板の周辺部において外部入力端子を形成可能な領域において可能な限り相互に離して配置される。従って、例えば画像信号線とクロック信号線とを隣接配置した場合と比較して、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。

【００１９】請求項６に記載の電気光学装置は請求項１から５のいずれか一項に記載の電気光学装置において、前記導電線は、前記複数の画素電極により規定される画像表示領域及び前記複数のデータ線を前記基板上で囲むように延設されたこと特徴とする。

【００２０】請求項６に記載の電気光学装置によれば、導電線により、画像表示領域及び複数のデータ線は、基板上で囲まれているので、当該画像表示領域及び複数のデータ線も、クロック信号線からシールドされることになる。従って、データ信号供給手段から出力されたデータ信号、スイッチング素子や画素電極に到達したデータ信号等における、高周波のクロックノイズの発生を低減できる。

【００２１】請求項７に記載の電気光学装置は請求項６に記載の電気光学装置において、前記基板に対向して対向基板が設けられてなり、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁を更に備えており、前記導電線は前記額縁に対向する位置において前記額縁に沿って前記基板に設けられた部分を含むことを特徴とする。

【００２２】請求項７に記載の電気光学装置によれば、導電線は、基板の額縁下に設けられているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を第１基板の周辺部分に余裕を持って形成することができ、導電線形成により電気光学装置における有効表示面積が減少することも殆ど又は全くない。

【００２３】請求項８に記載の電気光学装置は請求項１から７のいずれか一項に記載の電気光学装置において、前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする。

【００２４】請求項８に記載の電気光学装置によれば、導電線は例えば、Ａｌ（アルミニウム）等の、データ線と同一の低抵抗金属材料から形成されているので、導電線の引き回し領域が、たとえ長くても、導電線の抵抗は実用上十分に低く抑えられる。即ち、抵抗増加によりシールドの効果を下げることなく、例えば他の配線や回路等の隙間を縫ってジグザグに導電線を長く配線したり、画像表示領域等までも含めた広い領域に導電線を長く配線することが可能となるので、比較的簡単な構成により、当該シールドの効果を全体として、より高めることが出来る。更に、当該電気光学装置の製造プロセスにおいて、導電線及びデータ線を、同一の低抵抗金属材料から同一工程により形成できる。即ち、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。

【００２５】請求項９に記載の電気光学装置は請求項１から８のいずれか一項に記載の電気光学装置において、

前記画像信号線及びクロック信号線の間に介在する前記導電線部分並びに前記画像信号線及びクロック信号線は、前記第１基板に平行な同一平面上に形成された同一の低抵抗金属層から構成されたことを特徴とする。

【００２６】請求項９に記載の電気光学装置によれば、画像信号線及びクロック信号線の間に介在する導電線部分は、画像信号線やクロック信号線と、基板に平行な同一平面上に形成されているので、シールドの効果がより効率良く発揮される。ここで、同一平面上とは、基板の上に直接これらを配線してもよく、或いは基板上に形成された下地となる絶縁層上やＴＦＴ等のスイッチング素子の半導体層上に形成された層間絶縁層上にこれらを配線してもよいという意味である。更に、当該電気光学装置の製造プロセスにおいて、導電線、画像信号線及びクロック信号線を、例えば、Ａｌ層等の同一の低抵抗金属層から一括して形成できるので、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。

【００２７】請求項１０に記載の電気光学装置は請求項１から９のいずれか一項に記載の電気光学装置において、前記画素電極に所定量の容量を付与する容量線を更に備えており、該容量線が前記導電線に接続されたことを特徴とする。

【００２８】請求項１０に記載の電気光学装置によれば、容量線により画素電極に所定量の容量が付与されているので、デューティー比が小さくても高精細な表示が可能とされる。そして、容量線は導電線に接続されている。従って、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。

【００２９】請求項１１に記載の電気光学装置は、前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁と、前記画素電極に容量を付与する容量線とを更に備えており、前記導電線は前記額縁に対向する位置に延設されるとともに、前記対向する位置において前記導電線に前記容量線が接続されていることを特徴とする。

【００３０】請求項１１に記載の電気光学装置によれば、導電線は、基板の額縁に対向配置されているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を第１基板の周辺部分に余裕を持って形成することができ、導電線形成により電気光学装置における有効表示面積が減少することも殆ど又は全くない。また、容量線は導電線に接続されているため、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。また、導電線と容量線との接続は額縁に対向配置されるため、ＴＦＴ基板上有効表示面積を減少させることなく、スペースを有効利用することができる。

【００３１】請求項１２に記載の電子機器は、請求項１から１０に記載の電気光学装置を備えたことを特徴とする。

【００３２】請求項１２に記載の電子機器によれば、電子機器は、上述した本願発明の電気光学装置を備えており、高周波のクロックノイズが低減されており、高品位の画像表示が可能となる。

【００３３】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにする。

【００３４】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて説明する。尚、本実施形態では電気光学装置の一例として液晶装置を用いて説明する。

【００３５】（液晶装置の構成）液晶装置の実施の形態の構成について図１から図６に基づいて説明する。図１は、液晶装置の実施の形態におけるＴＦＴアレイ基板上に設けられた各種配線、周辺回路等の構成を示す平面図であり、図２は、図１のより詳細な２次元的レイアウトを示す平面図であり、図３は、画像信号線及びクロック信号線等の配線を示す図２のＡ－Ａ’断面図であり、図４は、図１の画素部分の拡大平面図であり、図５は、ＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図であり、図６は、対向基板を含めて示す図５のＨ－Ｈ’断面図である。

【００３６】図１において、液晶装置２００は、例えば石英基板、ハードガラス等からなるＴＦＴアレイ基板１を備えている。ＴＦＴアレイ基板１上には、マトリクス状に設けられた複数の画素電極１１と、Ｘ方向に複数配列されており夫々がＹ方向に沿って伸びるデータ線３５と、Ｙ方向に複数配列されており夫々がＸ方向に沿って伸びる走査線３１と、各データ線３５と画素電極１１との間に夫々介在すると共に該間における導通状態及び非導通状態を、走査線３１を介して夫々供給される走査信号に応じて夫々制御するスイッチング素子の一例としての複数のＴＦＴ３０とが形成されている。またＴＦＴアレイ基板１上には、後述の蓄積容量（図６参照）のための配線である容量線３１’（蓄積容量電極）が、走査線３１と平行に形成されている。

【００３７】ＴＦＴアレイ基板１上には更に、データ信号供給手段の一例を構成するサンプリング回路３０１及びデータ線駆動回路１０１と、走査線駆動回路１０４とが形成されている。また、複数の画素電極１１により規定される画像表示領域（即ち、実際に液晶の配向状態変

化により画像が表示される液晶装置の領域）の上辺には、画像表示領域の両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられており、画像表示領域の四隅には、ＴＦＴアレイ基板１と対向基板との間で電気的導通をとるための上下導通端子１０６が設けられている。以下図１から図３の説明において、ＴＦＴアレイ基板１の下辺に沿って複数設けられた外部入力端子１０２を介して入力される信号名称と、その信号配線とは、説明の容易化のために同一のアルファベット記号を信号及び配線の後に夫々付加して参照する（例えば、信号名称である“クロック信号ＣＬＸ”に対し、その信号配線を“配線ＣＬＸ”と呼ぶ）ことにする。

【００３８】走査線駆動回路１０４は、外部制御回路から外部入力端子１０２並びに配線ＶＳＳＹ及びＶＤＤＹを介して供給される、走査線駆動回路用の負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用いて、走査線駆動回路用のスタート信号ＤＹの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線ＣＬＹ及びＣＬＹ’を介して供給される、走査線駆動回路用の基準クロック信号ＣＬＹ及びその反転クロック信号ＣＬＹ’に基づく所定タイミングで、走査線３１に走査信号をパルス的に線順次で印加する。

【００３９】データ線駆動回路１０１は、外部制御回路から外部入力端子１０２並びに信号配線ＶＳＳＸ及びＶＤＤＸを介して供給される、データ線駆動回路用の負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用いて、データ線駆動回路用のスタート信号ＤＸの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線ＣＬＸ及びＣＬＸ’を介して供給されるデータ線駆動回路用の基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＸ’に基づき、走査線駆動回路１０４が走査信号を印加するタイミングに合わせて、外部入力端子１０２及び配線ＶＩＤ１～ＶＩＤ６を介して供給される例えば６相にシリアル-パラレル変換された画像信号ＶＩＤ１～ＶＩＤ６夫々について、データ線３５毎にサンプリング回路駆動信号をサンプリング回路３０１にサンプリング回路駆動信号線３０６を介して所定タイミングで供給する。

【００４０】サンプリング回路３０１は、ＴＦＴ３０２を各データ線３５毎に備えており、配線ＶＩＤ１～ＶＩＤ６がＴＦＴ３０２のソース電極に接続されており、サンプリング回路駆動信号線３０６がＴＦＴ３０２のゲート電極に接続されている。そして、画像信号ＶＩＤ１～ＶＩＤ６が入力されると、これらの画像信号をサンプリングする。また、サンプリング回路駆動信号線３０６を介して、データ線駆動回路１０１からサンプリング回路駆動信号が入力されると、画像信号ＶＩＤ１～ＶＩＤ６夫々についてサンプリングされた画像信号を、６つの隣接するデータ線３５からなるグループ毎に順次印加する。以上のように、データ線駆動回路１０１とサンプリング回路３０１とは、６相にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ６をデータ線３５にデータ信号として供給するように構成されている。本実施の形態では隣接する６つのデータ線３５に接続されるサンプリング回路３０１を同時に選択し、６つのデータ線３５からなるグループ毎に順次転送していく方式を述べたが、データ線３５を１本毎に選択してもよいし、隣接する２、３、…、５本或いは７本以上を同時に選択してもよい。また、データ線３５に供給される画像信号のシリアルーパラレル変換数は６相のみならず、サンプリング回路３０１を構成するＴＦＴ３０２の書き込み特性が良ければ、５相以下でもよいし、画像信号の周波数が高ければ、７相以上に増やしてもよい。この際、少なくとも画像信号のシリアルーパラレル変換数だけ、画像信号用の外部入力端子１０２及び画像信号線が必要なことは言うまでもない。

【００４１】図２に示すように、データ線駆動回路１０１は、スタート信号ＤＸが入力されると、基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＫ’に基づく転送信号の順次生成を開始するシフトレジスタ回路１０１ａと、シフトレジスタ回路１０１ａからの転送信号を波形整形しバッファリングした後、サンプリング回路駆動信号線３０６を介してサンプリング回路３０１に供給する波形制御回路１０１ｂ及びバッファ回路１０１ｃとを備えている。また、サンプリング回路３０１は、６相にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ６に対応してＴＦＴ３０２が６個ずつパラレルに各サンプリング回路駆動信号線３０６に接続されている。即ち、ＴＦＴ３０２から構成されるスイッチＳ１～Ｓ６が左から１本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳ７～Ｓ１２が左から２本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳｎ－５～Ｓｎが右端のサンプリング回路駆動信号線３０６に接続されている。

【００４２】本実施の形態では特に、図１及び図２に示すように、ＴＦＴアレイ基板１には、負電源ＶＳＳＸ用の配線ＶＳＳＸを兼ねた定電位の導電線（以下、シールド線と称す）８０及び正電源ＶＤＤＸ用の配線ＶＤＤＸを兼ねた定電位のシールド線８２が配線されている。これらのシールド線８０及び８２により、配線ＶＩＤ１～ＶＩＤ６は、配線ＣＬＸ及びＣＬＸ’から電気的にシールドされている。従って、クロック信号ＣＬＸの周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’から配線ＶＩＤ１～ＶＩＤ６への高周波のクロックノイズの飛び込みを低減できる。

【００４３】尚、走査線駆動用のクロック信号ＣＬＹ（及びその反転クロック信号ＣＬＹ’）の周波数は、データ線駆動用の上述のクロック信号ＣＬＸ（及びその反転クロック信号ＣＬＸ’）の周波数に比べて遥かに低

い。従って、クロック信号ＣＬＹ及びＣＬＹ’については、高周波のクロックノイズが問題となることは少ない。しかしながら、本実施の形態においては、図１及び図２に示したように、シールド線８０及び８２により、配線ＣＬＹ及びＣＬＹ’からも、配線ＶＩＤ１～ＶＩＤ６は、シールドされるように配線されている。すなわち、外部入力端子１０２から延設され、データ線駆動回路１０１の負電源ＶＳＳＸを兼ねたシールド線８０は、対向基板２に設けられた遮光性の額縁５３下に沿って、画像表示領域を囲むように配線される。従って、画像信号用の配線ＶＩＤ１～ＶＩＤ６ばかりではなく、サンプリング回路３０１のＴＦＴ３０２を介してデータ信号が書き込まれるデータ線３５への周辺回路からのノイズの飛び込みをも低減できる。

【００４４】特に本実施の形態では、配線ＶＳＳＸ及びＶＤＤＸを夫々延設してシールド線８０及び８２とすることにより、外部入力端子や配線を共用することが可能となり、装置構成の簡略化と省スペース化を図ることが出来る。また、シールド線８０及び８２の電位は、このように定電位線との共用化により、容易に定電位とされる。但し、電源用の配線とシールド線を別個に配線してもよい。

【００４５】また、データ線駆動回路１０１及び走査線駆動回路１０４を駆動するための電源電圧が互いに同じであれば、正電源の電位（正電位）であるＶＤＤＸ及びＶＤＤＹ、負電源の電位（負電位）であるＶＳＳＸ及びＶＳＳＹはそれぞれ共用させてもよい。このような構成を採れば、外部入力端子及びそれから延設される配線が削減できるので有利である。

【００４６】本実施の形態では、図２に示すように、負電源ＶＳＳＸが入力される外部入力端子１０２が２つ設けられており、配線ＶＳＳＸもこれに対応して２本設けられている。そして、配線ＶＩＤ１～ＶＩＤ６は、負電源ＶＳＳＸの電位（負電位）とされたシールド線８０により、ＴＦＴアレイ基板１上で囲まれている。特に、シフトレジスタ回路１０１ａと波形制御回路１０１ｂとの間にも、データ線３５と同じＡｌ等の金属層から形成されたシールド線８０は延設されている。そして、延設されたシールド線８０の先端部は、後述のように第１層間絶縁層を介してＡｌ等の金属層の下方において、例えば走査線３１と同じポリシリコン等の導電層から形成されたシールド線接続部８１を介して、波形制御回路１０１ｂ及びバッファ回路１０１ｃを囲むようにしてシールド線８０に接続されている。

【００４７】他方、図２に示すように、配線ＣＬＸ及びＣＬＸ’は、データ線駆動回路１０１に隣接する部分においては、正電源ＶＤＤＸの電位（正電位）とされたシールド線８２により、ＴＦＴアレイ基板１上で囲まれている。特に、波形制御回路１０１ｂとバッファ回路１０１ｃとの間にも、データ線３５と同じＡｌ等の金属層から形成されたシールド線８２は延設されており、その先端部は、例えば走査線３１と同じポリシリコン等の導電層から形成されたシールド線接続部８３を介して波形制御回路１０１ｂ及びシフトレジスタ回路１０１ａを囲むようにしてシールド線８２に接続されている。

【００４８】従って、配線ＶＩＤ１～ＶＩＤ６は、ＴＦＴアレイ基板１上で配線ＣＬＸ及びＣＬＸ’から２重にシールドされた構成が採られており、シフトレジスタ回路１０１ａ並びに波形制御回路１０１ｂ及びバッファ回路１０１ｃに対するシールドも信頼性が高いものとされている。但し、このように囲む構成を採らなくても、配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１～ＶＩＤ６との間にシールド線８０又は８２が少なくとも一本介在するように構成すれば、シールドの効果は多少なりとも得られる。

【００４９】本実施の形態では、図１及び図２に示したように、配線ＶＩＤ１～ＶＩＤ６と配線ＣＬＸ及びＣＬＸ’とは、ＴＦＴアレイ基板１上でＸ方向に沿って反対向きに（即ち、前者は時計回りに、後者は反時計回りに）引き回されている。従って、これらの配線間の距離が全体として大きくなるため、且つこれらの配線間にあるデータ線駆動回路１０１の介在に応じてこれらの配線間を伝達する電磁波は減少するので、クロック信号ＣＬＸ及びＣＬＸ’の周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’から、配線ＶＩＤ１～ＶＩＤ６への高周波のクロックノイズの飛び込みを更に低減できる。また、配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１～ＶＩＤ６の引き回しは、その方向が入れ替わっても何ら問題はない。すなわち、配線ＣＬＸ及びＣＬＸ’を負電源ＶＳＳＸでシールドし、配線ＶＩＤ１～ＶＩＤ６を正電源ＶＤＤＸでシールドしてもよい。但し、このように反対方向に引き回す構成を採らなくても、配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１～ＶＩＤ６との間にシールド線８０又は８２が少なくとも一本介在するように構成すれば、シールドの効果は多少なりとも得られる。

【００５０】本実施の形態では、クロック信号ＣＬＸ及びＣＬＸ’用の外部入力端子１０２と、画像信号ＶＩＤ１～ＶＩＤ６用の外部入力端子１０２とは、負電源ＶＳＳＸ用、正電源ＶＤＤＸ用及びスタート信号ＤＸ用の３つの外部入力端子１０２を間に介して、相互に所定間隔を隔てて配置されている。そして好ましくは、ＴＦＴアレイ基板１の周辺部において外部入力端子１０２を形成可能な領域において、可能な限りクロック信号ＣＬＸ及びＣＬＸ’用の外部入力端子１０２と、画像信号ＶＩＤ１～ＶＩＤ６用の外部入力端子１０２とは、相互に離して配置され、少なくとも一個以上の外部入力端子１０２が両者間に配置される。このように構成すれば、例えば画像信号線とクロック信号線とを隣接配置した場合と比較して、クロック用の配線から画像信号用の配線への高周波のクロックノイズの飛び込みを低減できる。

【００５１】本実施の形態では図１及び図２に示したように、シールド線８０により、画像表示領域及び複数のデータ線３５は、ＴＦＴアレイ基板１上で囲まれている。このため、当該画像表示領域及び複数のデータ線３５も、配線ＣＬＸ及びＣＬＸ’からシールドされている。従って、データ線駆動回路１０１から出力されたサンプリング回路駆動信号、ＴＦＴ３０や画素電極１１に到達したデータ信号等における、高周波のクロックノイズの発生を低減できる。但し、このように画像表示領域までも囲む構成を採らなくても、サンプリング回路３０１に至るまでの配線ＶＩＤ１～ＶＩＤ６をシールド線８０又は８２によりシールドするように構成すれば、シールドの効果は多少なりとも得られる。

【００５２】図３に断面図で示すように、シールド線８０及び８２を含む外部入力端子１０２に接続された各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸは、例えば、Ａｌ（アルミニウム）等の、データ線３５と同一の低抵抗金属材料から形成されている。従って、シールド線８０及び８２の引き回し領域が、たとえ長くても、シールド線８０及び８２の抵抗は実用上十分に低く抑えられる。即ち、図２に示したように、他の各種配線やシフトレジスタ回路１０１ａ並びに波形制御回路１０１ｂ及びバッファ回路１０１ｃの隙間を縫ってジグザグにシールド線８２を長く配線でき、更に画像表示領域までも含めた広い領域にシールド線８０を長く配線できる。このように比較的簡単な構成により、当該シールドの効果を全体として高めることが出来る。また図３に示すように、シールド線８０及び８２を含む外部入力端子１０２に接続された各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸは、ＴＦＴアレイ基板１に形成された第１層間絶縁層４２上に、即ち同一層上に形成されている。従って、シールドの効果がより効率良く発揮される。更に、このように構成すると、液晶装置２００の製造プロセスにおいて、各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸを、例えば、Ａｌ層等の同一の低抵抗金属層から同一工程により一括して形成できるので、製造上有利である。

【００５３】尚、図１から図３に示した外部入力端子１０２から入力される信号ＬＣＣＯＭは、共通電極の電源信号であり、配線ＬＣＣＯＭ及び前述の上下導通端子１０６上の導通材を介して、後述の対向基板に設けられた共通電極（図７参照）に供給される。

【００５４】ここで図４の平面図に示すように、容量線３１’は、ＴＦＴアレイ基板１上において走査線３１と平行に、例えば走査線３１と同じく導電性のポリシリコン層等から形成されており、シールド線８０にコンタクトホール８０ａを介して接続されている。このように構成すれば、容量線３１’を定電位とするための配線をシールド線８０で兼用でき、容量線３１’を定電位にするために必要な外部入力端子も、シールド線８０用の外部入力端子１０２で兼用できる。

【００５５】本実施の形態では特に、サンプリング回路３０１は、図１中斜線領域で示すように且つ図５及び図６に示すように、対向基板２に形成された遮光性の額縁５３に対向する位置においてＴＦＴアレイ基板１上に設けられており、データ線駆動回路１０１及び走査線駆動回路１０４は、液晶層５０に面しないＴＦＴアレイ基板１の狭く細長い周辺部分上に設けられている。ＴＦＴアレイ基板１の上には、画像表示領域の周囲において両基板を貼り合わせて液晶層５０を包囲するシール部材の一例としての光硬化性樹脂からなるシール材５２が、画像表示領域に沿って設けられている。そして、対向基板２上における画像表示領域とシール材５２との間には、遮光性の額縁５３が設けられている。

【００５６】額縁５３は、後に画像表示領域に対応して開口が開けられた遮光性のケースにＴＦＴアレイ基板１が入れられた場合に、当該画像表示領域が製造誤差等により当該ケースの開口の縁に隠れてしまわないように、即ち、例えばＴＦＴアレイ基板１のケースに対する数百μｍ程度のずれを許容するように、画像表示領域の周囲に例えば５００μｍ以上の幅を持つ帯状の遮光性材料から形成されたものである。このような遮光性の額縁５３は、例えば、Ｃｒ（クロム）、Ｎｉ（ニッケル）、Ａｌ（アルミニウム）等の金属材料を用いたスパッタリング、フォトリソグラフィ及びエッチングにより対向基板２に形成される。或いは、カーボンやＴｉ（チタン）をフォトレジストに分散した樹脂ブラックなどの材料から形成される。

【００５７】シール材５２の外側の領域には、画像表示領域の下辺に沿ってデータ線駆動回路１０１及び外部入力端子１０２が設けられており、画像表示領域の左右の２辺に沿って走査線駆動回路１０４が画像表示領域の両側に設けられている。そして、シール材５２とほぼ同じ輪郭を持つ対向基板２が当該シール材５２によりＴＦＴアレイ基板１に固着されている。

【００５８】以上のようにシールド線８０及びサンプリング回路３０１は、ＴＦＴアレイ基板１上の額縁５３に対向配置、即ち本実施形態の場合は額縁５３の下に設けるようにすれば、ＴＦＴアレイ基板１上の省スペース化が図られ、例えば、走査線駆動回路１０４やデータ線駆動回路１０１をＴＦＴアレイ基板１の周辺部分に余裕を持って形成することができ、シールド線８０の形成により液晶装置２００における有効表示面積が減少することも殆ど又は全くない。またシールド線８０は額縁５３に対向する位置に延設されるとともに、対向する位置においてシールド線８０と容量線３１’とを接続するようにすれば、ＴＦＴ基板上の有効表示面積を減少させることなく、スペースを有効利用することができる。

【００５９】（液晶装置全体の構成）次に、液晶装置２００の具体的構成について図７及び図８を参照して説明する。ここに、図７は液晶装置のＴＦＴ３０部分を示し

ており、図４におけるＢ－Ｂ’に沿った断面図であり、図８は額縁の下における液晶装置のシールド線８０に沿った断面図である。尚、図７及び図８においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００６０】図７の断面図において、液晶装置２００は、各画素に設けられるＴＦＴ３０部分において、ＴＦＴアレイ基板１並びにその上に積層された半導体層３２、ゲート絶縁層３３、走査線３１（ゲート電極）、第１層間絶縁層４２、データ線３５、第２層間絶縁層４３、画素電極１１及び配向膜１２を備えている。液晶装置２００はまた、例えばガラス基板から成る対向基板２並びにその上に積層された共通電極２１、配向膜２２及び遮光膜２３を備えている。液晶装置２００は更に、これらの両基板間に挟持された電気光学物質として液晶層５０を備えている。

【００６１】ここでは先ず、これらの層のうち、ＴＦＴ３０を除く各層の構成について順に説明する。

【００６２】第１及び第２層間絶縁層４２及び４３は夫々、５０００～１５０００オングストローム程度の層みを持つＮＳＧ（ノンシリケートガラス）、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）などのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる。尚、ＴＦＴアレイ基板１上に、ＴＦＴ３０の下地となる層間絶縁層をシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等から形成してもよい。

【００６３】画素電極１１は例えば、ＩＴＯ（インジウム・ティン・オキサイド）膜などの透明導電性薄膜からなる。このような画素電極１１は、スパッタリング処理等によりＩＴＯ膜等を約５００～２０００オングストロームの厚さに堆積した後、フォトリソグラフィ工程、エッチング工程を施すこと等により形成される。尚、当該液晶装置２００を反射型の液晶装置に用いる場合には、Ａｌ等の反射率の高い不透明な材料から画素電極１１を形成してもよい。

【００６４】配向膜１２は例えば、ポリイミド薄膜などの有機薄膜からなる。このような配向膜１２は、例えばポリイミド系の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により形成される。

【００６５】共通電極２１は、対向基板２の全面に渡って形成されている。このような共通電極２１は、例えばスパッタリング処理等によりＩＴＯ膜等を約５００～２０００オングストロームの厚さに堆積した後、フォトリソグラフィ工程、エッチング工程を施すこと等により形成される。

【００６６】配向膜２２は、例えば、ポリイミド薄膜などの有機薄膜からなる。このような配向膜２２は、例えばポリイミド系の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により形成される。

【００６７】遮光膜２３は、ＴＦＴ３０に対向する所定領域に設けられている。このような遮光膜２３は、前述の額縁５３同様に、ＣｒやＮｉなどの金属材料を用いたスパッタリング、フォトリソグラフィ及びエッチングにより形成されたり、カーボンやＴｉをフォトレジストに分散した樹脂ブラックなどの材料から形成される。遮光膜２３は、ＴＦＴ３０の半導体層３２に対する遮光の他に、コントラストの向上、色材の混色防止などの機能を有する。

【００６８】液晶層５０は、画素電極１１と共通電極２１とが対面するように配置されたＴＦＴアレイ基板１と対向基板２との間において、シール材５２（図５及び図６参照）により囲まれた空間に液晶が真空吸引等により封入されることにより形成される。液晶層５０は、画素電極１１からの電界が印加されていない状態で配向膜１２及び２２により所定の配向状態を採る。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、二つの基板１及び２をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのスペーサが混入されている。

【００６９】次に、ＴＦＴ３０に係る各層の構成について順に説明する。

【００７０】ＴＦＴ３０は、走査線３１、走査線３１からの電界によりチャネルが形成される半導体層３２、走査線３１と半導体層３２とを絶縁するゲート絶縁層３３、半導体層３２に形成されたソース領域３４、データ線３５、及び半導体層３２に形成されたドレイン領域３６を備えている。ドレイン領域３６には、複数の画素電極１１のうちの対応する一つが接続されている。ソース領域３４及びドレイン領域３６は後述のように、半導体層３２に対し、ｎ型又はｐ型のチャネルを形成するかに応じて所定濃度のｎ型用又はｐ型用のドーパントをドープすることにより形成されている。ｎ型チャネルのＴＦＴは、動作速度が速いという利点があり、画素のスイッチング素子であるＴＦＴ３０として用いられることが多い。

【００７１】ＴＦＴ３０を構成する半導体層３２は、例えば、ＴＦＴアレイ基板１上にａ－Ｓｉ（アモルファスシリコン）膜を形成後、アニール処理を施して約５００～２０００オングストロームの厚さに固相成長させることにより形成する。この際、ｎチャネル型のＴＦＴ３０の場合には、Ｓｂ（アンチモン）、Ａｓ（砒素）、Ｐ（リン）などのＶ族元素のドーパントを用いたイオン注入等によりドープしてもよい。また、ｐチャネル型のＴＦＴ３０の場合には、Ｂ（ボロン）、Ｇａ（ガリウム）、Ｉｎ（インジウム）などのIII族元素のドーパントを用いたイオン注入等によりドープする。特にＴＦＴ

３０をＬＤＤ（Ｌｉｇｈｔｌｙ　ＤｏｐｅｄＤｒａｉｎ）構造を持つｎチャネル型のＴＦＴとする場合、ｐ型の半導体層３２に、ソース領域３４及びドレイン領域３６のうちチャネル側に夫々隣接する一部にＰなどのＶ族元素のドーパントにより低濃度ドープ領域を形成し、同じくＰなどのＶ族元素のドーパントにより高濃度ドープ領域を形成する。また、ｐチャネル型のＴＦＴ３０とする場合、ｎ型の半導体層３２に、Ｂなどの III族元素のドーパントを用いてソース領域３４及びドレイン領域３６を形成する。このようにＬＤＤ構造とした場合、ショートチャネル効果を低減できる利点が得られる。尚、ＴＦＴ３０は、ＬＤＤ構造における低濃度ドープ領域にイオン注入したオフセット構造のＴＦＴとしてもよいし、ゲート電極をマスクとして高濃度の不純物イオンをドープすることにより自己整合的に高濃度なソース及びドレイン領域を形成するセルフアライン型のＴＦＴとしてもよい。また、ゲート電極を２個直列に設けデュアルゲート構造としてもよいし、ゲート電極を３個以上直列に設けてもよいことは言うまでもない。このような構成を採れば、ＴＦＴ３０のオフ時におけるリーク電流が低減され、クロストーク等の発生を抑制できるため、高品位な液晶装置を提供することができる。

【００７２】ゲート絶縁層３３は、半導体層３２を約９００～１３００℃の温度により熱酸化することにより、３００～１５００オングストローム程度の比較的薄い厚さの熱酸化膜を形成して得ることができる。これにより半導体層３２とゲート絶縁層３３の界面状態の優れた良質の絶縁膜を形成することができる。

【００７３】走査線３１は、減圧ＣＶＤ法等によりポリシリコン膜を堆積した後、フォトリソグラフィ工程、エッチング工程等により形成される。或いは、Ａｌ等の金属膜又は金属シリサイド膜から形成されてもよい。この場合、走査線３１を、遮光膜２３が覆う領域の一部又は全部に対応する遮光膜として配置すれば、金属膜や金属シリサイド膜の持つ遮光性により、遮光膜２３の一部又は全部を省略することも可能となる。この場合特に、対向基板２とＴＦＴアレイ基板１との貼り合わせずれによる画素開口率の低下を防ぐことが出来る利点がある。

【００７４】データ線３５は、画素電極１１と同様にＩＴＯ膜等の透明導電性薄膜から形成してもよい。或いは、スパッタリング処理等により、約１０００～５０００オングストロームの厚さに堆積されたＡｌ等の低抵抗金属や金属シリサイド等から形成してもよい。

【００７５】また、第１層間絶縁層４２には、ソース領域３４へ通じるコンタクトホール３７及びドレイン領域３６へ通じるコンタクトホール３８が夫々形成されている。このソース領域３４へのコンタクトホール３７を介して、データ線３５はソース領域３４に電気的接続される。更に、第２層間絶縁層４３には、ドレイン領域３６へのコンタクトホール３８が形成されている。このドレイン領域３６へのコンタクトホール３８を介して、画素電極１１はドレイン領域３６に電気的接続される。前述の画素電極１１は、このように構成された第２層間絶縁層４３の上面に設けられている。各コンタクトホールは、例えば、反応性エッチング、反応性イオンビームエッチング等のドライエッチングにより形成すれば、開口サイズの微細化が可能となり、画素の高開口率化が実現できる。

【００７６】尚、一般にはチャネルが形成される半導体層３２は、光が入射するとｐ－Ｓｉが有する光電変換効果により光電流が発生してしまいＴＦＴ３０のトランジスタ特性が劣化するが、本実施の形態では、対向基板２には各ＴＦＴ３０に夫々対向する位置に遮光膜２３が形成されているので、入射光が半導体層３２に入射することが防止される。更にこれに加えて又は代えて、ゲート電極を上側から覆うようにデータ線３５をＡｌ等の不透明な金属薄膜から形成すれば、遮光膜２３と共に又は単独で、半導体層３２への入射光（即ち、図７で上側からの光）の入射を効果的に防ぐことが出来る。

【００７７】図７において、画素電極１１には蓄積容量７０が夫々設けられている。この蓄積容量７０は、より具体的には、半導体層３２と同一工程により形成される第１蓄積容量電極３２’、ゲート絶縁層３３と同一工程により形成される誘電体層３３’、走査線３１と同一工程により形成される容量線３１’（第２蓄積容量電極）、第１及び第２層間絶縁層４２及び４３、並びに第１及び第２層間絶縁層４２及び４３を介して容量線３１’に対向する画素電極１１の一部から構成されている。このように蓄積容量７０が設けられているため、デューティー比が小さくても高精細な表示が可能とされる。

【００７８】図８の断面図に示すように、額縁５３に対向し且つ複数の走査線３１の上方の位置において第１層間絶縁層４２上をシールド線８０は通過する。そして、このシールド線８０は、その殆どの部分が、前述したデータ線３５と同一工程で形成されたＡｌ等の金属薄膜からなる低抵抗な配線である。このように液晶装置２００の製造プロセスにおいて、シールド線８０とデータ線３５とを一括して形成できるので、製造上有利である。

【００７９】本実施の形態では特に、ＴＦＴ３０の形成時に同一薄膜形成工程で、サンプリング回路３０１、データ線駆動回路１０１、走査線駆動回路１０４等の周辺回路を形成できるので製造上有利である。例えば、これらの周辺回路は、ｎチャネル型ポリシリコンＴＦＴ及びｐチャネル型ポリシリコンＴＦＴから構成される相補型構造の複数のＴＦＴからＴＦＴアレイ基板１上の周辺部分に形成される。

【００８０】尚、図７及び図８には示されていないが、液晶装置２００においては、対向基板２の投射光が入射する側及びＴＦＴアレイ基板１の投射光が出射する側に

は夫々、例えば、ＴＮ（ツイステッドネマティック）モード、ＳＴＮ（スーパーＴＮ）モード、Ｄ－ＳＴＮ（ダブルーＳＴＮ）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【００８１】また、以上説明した液晶装置２００は、カラー液晶プロジェクタに適用されるため、３つの液晶装置２００がＲＧＢ用のライトバルブとして夫々用いられ、各装置には夫々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が入射光として夫々入射されることになる。従って、各実施の形態では、対向基板２に、カラーフィルタは設けられていない。しかしながら、液晶装置２００においても遮光膜２３の形成されていない画素電極１１に対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２上に形成してもよい。あるいは、ＴＦＴアレイ基板１上の各画素に対応するように、ＲＧＢのカラーレジストによりカラーフィルター層を内蔵しても良い。このようにすれば、液晶プロジェクタ以外の直視型や反射型のカラー液晶テレビなどのカラー液晶装置に本実施の形態の液晶装置を適用できる。更に、対向基板２上に１画素1個対応するようにマイクロレンズを形成してもよい。このようにすれば、入射光の集光効率を向上することで、明るい液晶装置が実現できる。更にまた、対向基板２上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー液晶装置が実現できる。

【００８２】液晶装置２００において、ＴＦＴアレイ基板１側における液晶分子の配向不良を抑制するために、第２層間絶縁層４３の上に更に平坦化膜をスピンコート等で塗布してもよく、又はＣＭＰ（Chemical Mechanical Polishing)処理を施してもよい。或いは、第２層間絶縁層４３を平坦化膜で形成してもよい。

【００８３】液晶装置２００のスイッチング素子は、正スタガ型又はコプラナー型のポリシリコンＴＦＴであるとして説明したが、逆スタガ型のＴＦＴやアモルファスシリコンＴＦＴ等の他の形式のＴＦＴに対しても、本実施の形態は有効である。

【００８４】液晶装置２００においては、一例として液晶層５０をネマティック液晶から構成したが、液晶を高分子中に微小粒として分散させた高分子分散型液晶を用いれば、配向膜１２及び２２、並びに前述の偏光フィルム、偏光板等が不要となり、光利用効率が高まることによる液晶装置の高輝度化や低消費電力化の利点が得られる。更に、画素電極１１をＡｌ等の反射率の高い金属膜から構成することにより、液晶装置２００を反射型液晶装置に適用する場合には、電圧無印加状態で液晶分子がほぼ垂直配向されたＳＨ（スーパーホメオトロピック）型液晶などを用いても良い。更にまた、液晶装置２００においては、液晶層５０に対し垂直な電界（縦電界）を印加するように対向基板２の側に共通電極２１を設けているが、液晶層５０に平行な電界（横電界）を印加するように一対の横電界発生用の電極から画素電極１１を夫々構成する（即ち、対向基板２の側には縦電界発生用の電極を設けることなく、ＴＦＴアレイ基板１の側に横電界発生用の電極を設ける）ことも可能である。このように横電界を用いると、縦電界を用いた場合よりも視野角を広げる上で有利である。その他、各種の液晶材料（液晶相）、動作モード、液晶配列、駆動方法等に本実施の形態を適用することが可能である。また、上述の実施形態では基板上にＴＦＴを形成する構成を用いて説明したがこのような構成に限らず、シリコン基板にスイッチング素子を形成する構成でも適用可能である。また、電気光学物質として液晶を用いて説明したが液晶に限らず、エレクトロルミネッセンス、あるいはプラズマディスプレイ等にも適用可能である。

【００８５】以上説明した実施の形態において更に、額縁５３下やＴＦＴアレイ基板１の周辺部に、プリチャージ回路、検査回路等の周知の周辺回路を設けてもよい。プリチャージ回路は、コントラスト比の向上、データ線３５の電位レベルの安定、表示画面上のラインむらの低減等を目的として、データ線３５に対し、データ線駆動回路１０１から供給されるデータ信号に先行するタイミングで、プリチャージ信号を供給することにより、データ信号をデータ線３５に書き込む際の負荷を軽減する回路である。例えば、特開平７－２９５５２０号公報に、このようなプリチャージ回路の一例が開示されている。他方、検査回路は、額縁５３下やＴＦＴアレイ基板の周辺部に、製造途中や出荷時の当該液晶装置の品質、欠陥等を検査するための回路である。

【００８６】また、以上の実施の形態において、特開平９－１２７４９７号公報、特公平３－５２６１１号公報、特開平３－１２５１２３号公報、特開平８－１７１１０１号公報等に開示されているように、ＴＦＴアレイ基板１上においてＴＦＴ３０に対向する位置（即ち、ＴＦＴ３０の下側）にも、例えば高融点金属からなる遮光層を設けてもよい。このようにＴＦＴ３０の下側にも遮光層を設ければ、ＴＦＴアレイ基板１の側からの戻り光等がＴＦＴ３０に入射するのを未然に防ぐことができる。従って、当該液晶装置２００をプロジェクタ用のライトバルブとして好適に用いることが出来る。

【００８７】更にまた、以上の実施の形態において、ＴＦＴ３０に代えてＴＦＤ（Thin Film Diode)等の２端子型非線形素子等からスイッチング素子を構成してもよい。この場合、データ線及び走査線のうち一方の線を対向基板に配置して共通電極として機能させ、ＴＦＴアレイ基板に設けられた他方の線と画素電極との間にスイッ

チング素子を夫々配置して液晶駆動する。このように構成しても、画素信号線やデータ線をクロック信号線からシールドすることにより、高周波のクロックノイズの画像信号やデータ信号への飛び込みを防止する効果は発揮される。

【００８８】（液晶装置の動作）次に、以上のように構成された液晶装置２００の動作について図１を参照して説明する。

【００８９】先ず、走査線駆動回路１０４は、所定タイミングで走査線３１に走査信号をパルス的に線順次で印加する。

【００９０】これと並行して、６つの配線ＶＩＤ１～ＶＩＤ６からパラレルな画像信号を受けると、サンプリング回路３０１は、これらの画像信号をサンプリングする。データ線駆動回路１０１は、走査線駆動回路１０４がゲート電圧を印加するタイミングに合わせて、６つの配線ＶＩＤ１～ＶＩＤ６夫々について一つのデータ線毎にサンプリング回路駆動信号を供給して、サンプリング回路３０１のＴＦＴ３０２をオン状態とする。これにより、隣接する６つのデータ線３５に対して、サンプリング回路３０１にサンプリングされたデータ信号を順次印加する。即ち、データ線駆動回路１０１とサンプリング回路３０１により、配線ＶＩＤ１～ＶＩＤ６から入力された６相にシリアルーパラレル変換されたパラレルな画像信号ＶＩＤ１～ＶＩＤ６は、データ線３５に供給される。

【００９１】このように、走査信号（ゲート電圧）及びデータ信号（ソース電圧）の両方が印加されたＴＦＴ３０においては、ソース領域３４、半導体層３２に形成されたチャネル及びドレイン領域３６を介して画素電極１１に電圧が印加される。そして、この画素電極１１の電圧は、ソース電圧が印加された時間よりも例えば３桁も長い時間だけ蓄積容量（図７参照）により保持される。ここで特に、シールド線８０及び８２により、配線ＶＩＤ１～ＶＩＤ６は、配線ＣＬＸ及びＣＬＸ’からシールドされているので、クロック信号ＣＬＸの周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’から配線ＶＩＤ１～ＶＩＤ６への高周波のクロックノイズの飛び込みを低減できる。

【００９２】以上のように、画素電極１１に電圧が印加されると、液晶層５０におけるこの画素電極１１と共通電極２１とに挟まれた部分における液晶の配向状態が変化し、ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として液晶装置２００からは画像信号に応じたコントラストを持つ光が出射する。

【００９３】以上の結果、表示すべき画像の解像度が高く、高周波のシリアルな画像信号ＶＩＤ１～ＶＩＤ６が入力される場合にも、これに対応して周波数が高いクロック信号ＣＬＸ及びＣＬＸ’を用いつつ、高周波のクロックノイズの発生により画質が劣化することは殆ど又は全く無くなり、高品位の画像表示が可能とされる。

【００９４】（電子機器）次に、以上詳細に説明した液晶装置２００を備えた電子機器の実施の形態について図９から図１３を参照して説明する。

【００９５】先ず図９に、このように液晶装置２００を備えた電子機器の概略構成を示す。

【００９６】図９において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、液晶装置２００、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、テレビ信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回路１００２は、増幅・極性反転回路、シリアルーパラレル変換回路、ローテーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号ＣＬＫと共に駆動回路１００４に出力する。駆動回路１００４は、液晶装置２００を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、液晶装置２００を構成するＴＦＴアレイ基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【００９７】次に図１０から図１３に、このように構成された電子機器の具体例を夫々示す。

【００９８】図１０において、電子機器の一例たる液晶プロジェクタ１１００は、上述した駆動回路１００４がＴＦＴアレイ基板上に搭載された液晶装置２００を含む液晶モジュールを３個用意し、夫々ＲＧＢ用のライトバルブ２００Ｒ、２００Ｇ及び２００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ２００Ｒ、２００Ｇ及び２００Ｂに夫々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ２００Ｒ、２００Ｇ及び２００Ｂにより夫々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投

射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【００９９】本実施の形態においては特に、前述のように遮光層をＴＦＴの下側にも設けておけば、当該液晶装置２００からの入射光に基づく液晶プロジェクタ内の投射光学系による反射光、入射光が通過する際のＴＦＴアレイ基板の表面からの反射光、他の液晶装置から出射した後にダイクロイックプリズム１１１２を突き抜けてくる入射光の一部（Ｒ光及びＧ光の一部）等が、戻り光としてＴＦＴアレイ基板の側から入射しても、画素スイッチング用のＴＦＴ３０等のチャネルに対する遮光を十分に行うことができる。この場合、小型化に適したプリズムを投射光学系に用いても、各液晶装置のＴＦＴアレイ基板とプリズムとの間において、戻り光防止用のＡＲ（Anti Reflection)フィルムを貼り付けたり、偏光板にＡＲ被膜処理を施したりすることが不要となるので、構成を小型且つ簡易化する上で大変有利である。

【０１００】図１１において、電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００は、上述した液晶装置２００がトップカバーケース内に備えられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１０１】図１２において、電子機器の他の例たるページャ１３００は、金属フレーム１３０２内に前述の駆動回路１００４がＴＦＴアレイ基板上に搭載されて液晶モジュールをなす液晶装置２００が、バックライト１３０６ａを含むライトガイド１３０６、回路基板１３０８、第１及び第２のシールド板１３１０及び１３１２、二つの弾性導電体１３１４及び１３１６、並びにフィルムキャリアテープ１３１８と共に収容されている。この例の場合、前述の表示情報処理回路１００２（図９参照）は、回路基板１３０８に搭載してもよく、液晶装置２００のＴＦＴアレイ基板上に搭載してもよい。更に、前述の駆動回路１００４を回路基板１３０８上に搭載することも可能である。

【０１０２】尚、図１２に示す例はページャであるので、回路基板１３０８等が設けられている。しかしながら、駆動回路１００４や更に表示情報処理回路１００２を搭載して液晶モジュールをなす液晶装置２００の場合には、金属フレーム１３０２内に液晶装置２００を固定したものを液晶装置として、或いはこれに加えてライトガイド１３０６を組み込んだバックライト式の液晶装置として、生産、販売、使用等することも可能である。

【０１０３】また図１３に示すように、駆動回路１００４や表示情報処理回路１００２を搭載しない液晶装置２００の場合には、駆動回路１００４や表示情報処理回路１００２を含むＩＣ１３２４がポリイミドテープ１３２２上に実装されたＴＣＰ（Tape Carrier Package）１３２０に、ＴＦＴアレイ基板１の周辺部に設けられた異方性導電フィルムを介して物理的且つ電気的に接続して、液晶装置として、生産、販売、使用等することも可能である。

【０１０４】以上図１０から図１３を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図９に示した電子機器の例として挙げられる。

【０１０５】以上説明したように、本実施の形態によれば、高周波のクロックノイズの発生が低減されており、高品位の画像表示が可能な液晶装置２００を備えた各種の電子機器を実現できる。

【０１０６】

【発明の効果】請求項１に記載の電気光学装置によれば、第１基板に配線された定電位の導電線により、画像信号線は、クロック信号線からシールドされているので、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減でき、従って、高解像度の画像を表示するための高周波数の画像信号に応じて高品位の画像表示を行える。

【０１０７】請求項２に記載の電気光学装置によれば、導電線及び定電位線の配線自体や外部入力端子を共用することにより、構成の簡略化と省スペース化を図ることが出来るので、比較的簡易な構成により高品位の画像表示を行える電気光学装置を実現できる。

【０１０８】請求項３に記載の電気光学装置によれば、画像信号線を、クロック信号線から２重にシールドする構成により、画像信号やデータ信号中の高周波のクロックノイズの発生をより強力に且つ信頼性高く低減し得る。

【０１０９】請求項４に記載の電気光学装置によれば、画像信号線とクロック信号線とをデータ線駆動回路に対して反対向きに引き回すことにより、画像信号線への高周波のクロックノイズの飛び込みを更に低減できるので、簡単な構成上の工夫により効率良くシールドの効果を高めることが出来る。

【０１１０】請求項５に記載の電気光学装置によれば、第１及び第２外部入力端子を、第３外部入力端子を間に介して相互に所定間隔を隔てて配置することにより、画像信号線への高周波のクロックノイズの飛び込みを低減できるので、簡単な構成上の工夫により効率良くシールドの効果を高めることが出来る。

【０１１１】請求項６に記載の電気光学装置によれば、画像表示領域及び複数のデータ線をクロック信号線からシールドできるので、データ線上のデータ信号等における、高周波のクロックノイズの発生を低減でき、より高品位の画像表示が可能となる。

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【０１１２】請求項７に記載の電気光学装置によれば、導電線は基板の額縁下に設けられているので、基板上のスペースの有効利用を図ることができる。

【０１１３】請求項８及び９に記載の電気光学装置によれば、比較的簡易な製造工程により、シールド効果の高い導電線を形成することができ、低コストで高品位の画像表示が可能な電気光学装置を実現できる。

【０１１４】請求項１０に記載の電気光学装置によれば、容量線の電位変動によるスイッチング素子や画素電極への悪影響を防止しつつ、容量線を定電位とするための定電位線や外部入力端子を他の配線や端子で兼用できるので、比較的簡易な構成により高品位の画像表示が可能となる。

【０１１５】請求項１１に記載の電子機器によれば、高周波のクロックノイズが低減されており、高品位の画像表示が可能な、液晶プロジェクタ、パーソナルコンピュータ、ページャ等の様々な電子機器を実現可能となる。

【図面の簡単な説明】

【図１】　液晶装置の実施の形態においてＴＦＴアレイ基板上に形成された各種配線、周辺回路等の概略平面図である。

【図２】　図１の２次元的レイアウトをより詳細に示す概略平面図である。

【図３】　図１のＴＦＴアレイ基板上のＡ－Ａ’線に沿った断面図である。

【図４】　図１のＴＦＴアレイ基板上に形成された画素電極、走査線、データ等の画像表示領域端部における拡大平面図である。

【図５】　図１の液晶装置の全体構成を示す平面図である。

【図６】　図１の液晶装置の全体構成を示す断面図である。

【図７】　図１の液晶装置の画像表示領域に設けられた画素スイッチング用ＴＦＴの断面図である。

【図８】　図１の液晶装置の額縁領域に設けられたシールド線部分における断面図である。

【図９】　本発明による電子機器の実施の形態の概略構成を示すブロック図である。

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【図１０】　電子機器の一例としての液晶プロジェクタを示す断面図である。

【図１１】　電子機器の他の例としてのパーソナルコンピュータを示す正面図である。

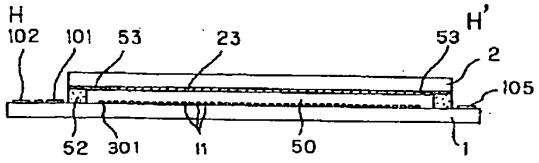
【図１２】　電子機器の一例としてのページャを示す分解斜視図である。

【図１３】　電子機器の一例としてのＴＣＰを用いた液晶装置を示す斜視図である。

【符号の説明】

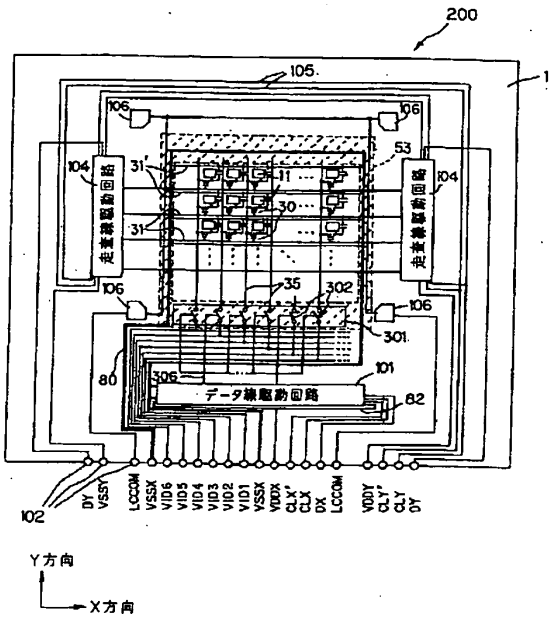
１…ＴＦＴアレイ基板
２…対向基板
１１…画素電極
１２…配向膜
２１…共通電極
２２…配向膜
２３…遮光膜
３０…ＴＦＴ
３１…走査線（ゲート電極）
３２…半導体層
３３…ゲート絶縁層
３４…ソース領域
３５…データ線
３６…ドレイン領域
３７、３８…コンタクトホール
４２…第１層間絶縁層
４３…第２層間絶縁層
５０…液晶層
５２…シール材
５３…額縁
７０…蓄積容量
８０、８２…シールド線（定電位線）
１０１…データ線駆動回路
１０２…外部入力端子
１０４…走査線駆動回路
２００…液晶装置
３０１…サンプリング回路
３０２…ＴＦＴ

【図６】

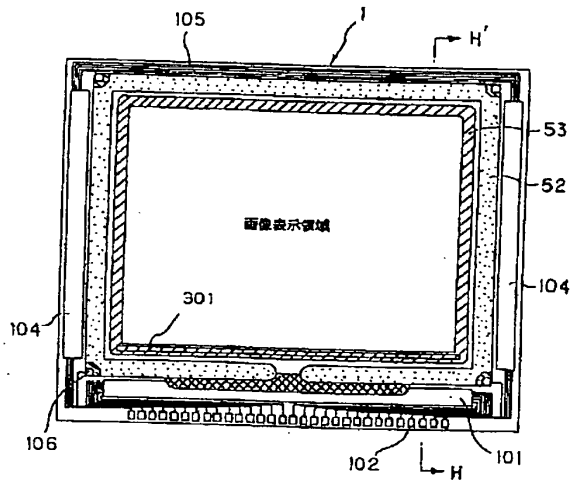


(15)

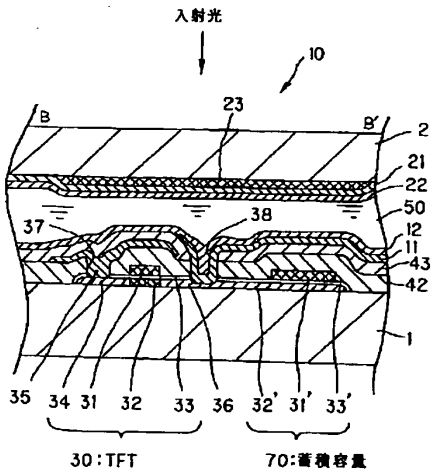
【図１】


200
105
1
106
104
走査線駆動回路
31
11
30
53
35
302
301
80
306
データ線駆動回路
101
82
102
DY
VSSY
LCCOM
VSSX
VID6
VID5
VID4
VID3
VID2
VID1
VSSX
VDDX
CLX'
CLX
DX
LCCOM
VDDY
CLY'
CLY
DY
Y方向
X方向

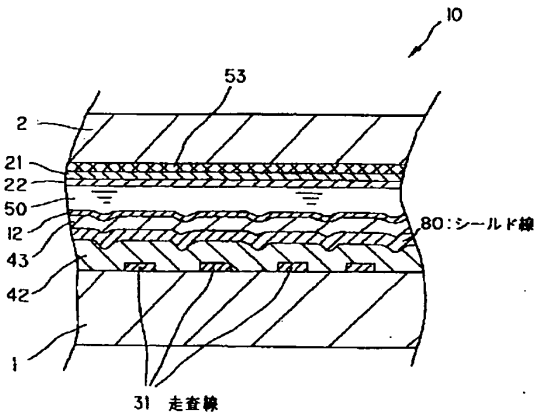
【図５】


105
1
H'
53
52
画像表示領域
104
301
104
106
102
101
H

【図７】

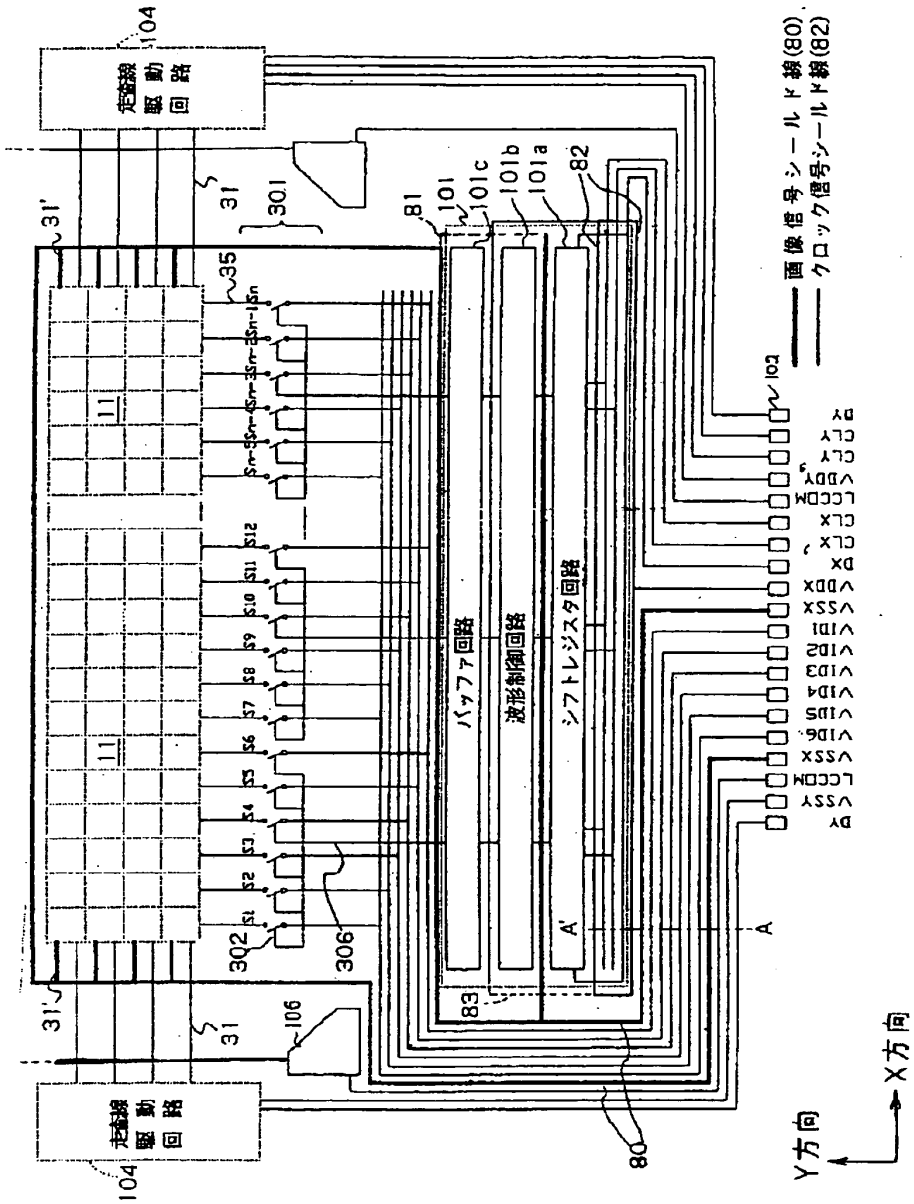

入射光
10
23
B
B'
2
21
22
50
37
38
12
11
43
42
1
35
34
31
32
33
36
32'
31'
33'
30:TFT
70:蓄積容量

【図８】


10
53
2
21
22
50
12
43
42
1
80:シールド線
31 走査線

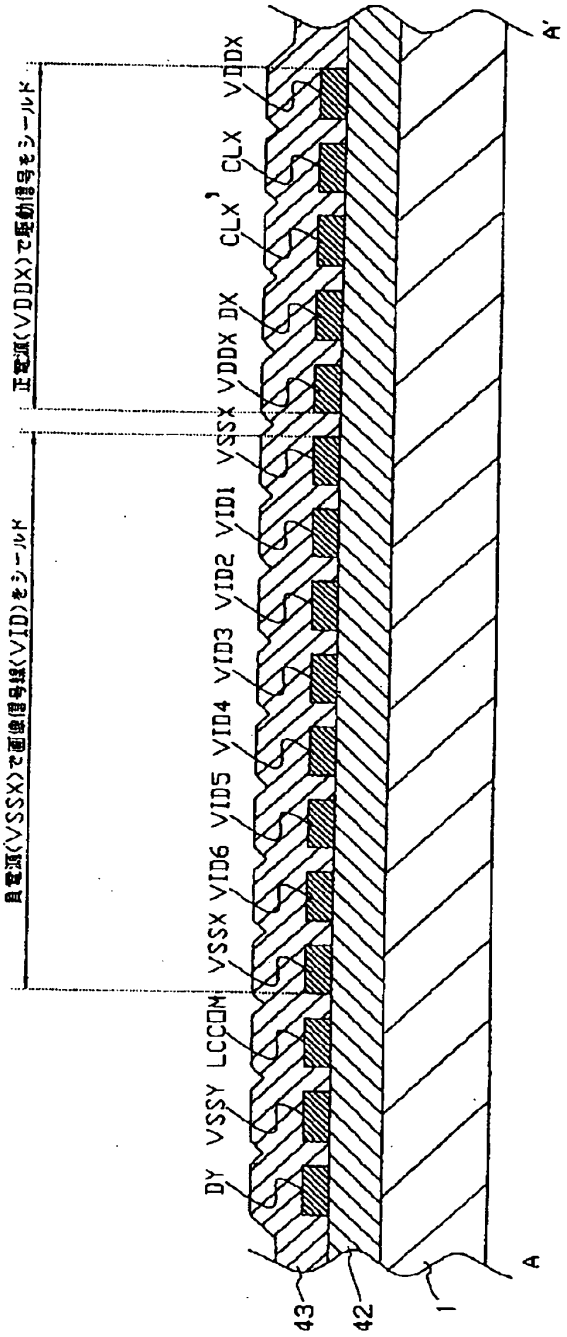
(16)

【図２】

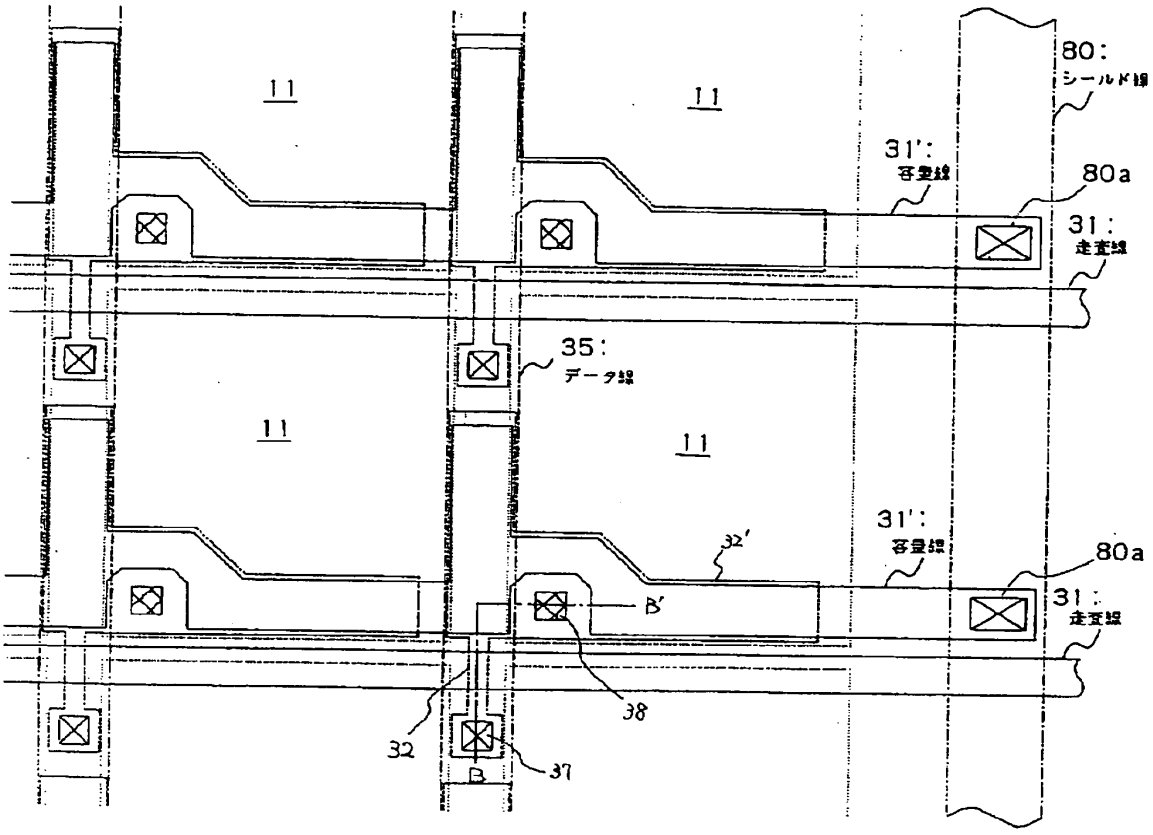

走査線駆動回路
104
31'
31
301
81
101
101c
101b
101a
82
35
11
11
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
302
306
83
106
80
A
A'
バッファ回路
波形制御回路
シフトレジスタ回路
画像信号シールド線(80)
クロック信号シールド線(82)
102
DY
CLY
CLY'
VDDY
LCCOM
CLX
CLX'
DX
VDDX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSX
LCCOM
VSSY
DY
Y方向
X方向

(17)

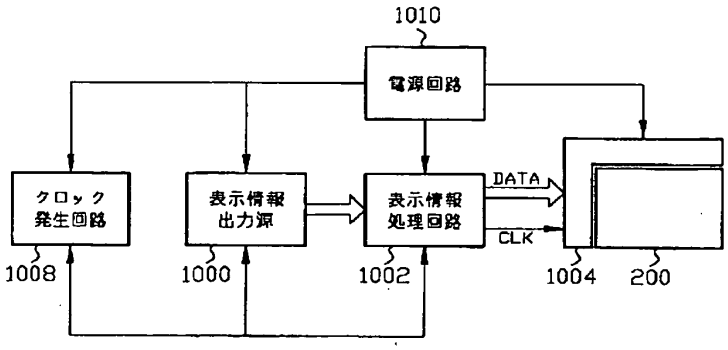
【図３】


正電源(VDDX)で駆動信号をシールド
負電源(VSSX)で画像信号線(VID)をシールド
VDDX
CLX
CLX'
DX
VDDX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSX
LCCOM
VSSY
DY
A'
A
43
42
1

【図４】

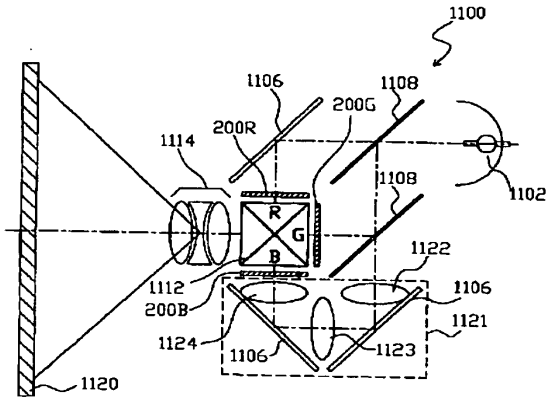

11
11
80:
シールド線
31':
容量線
80a
31:
走査線
35:
データ線
11
11
31':
容量線
80a
31:
走査線
32'
B'
38
32
37
B

【図９】

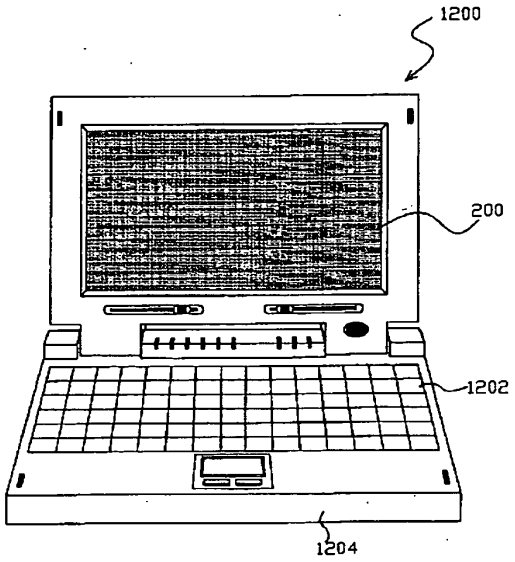

1010
電源回路
クロック
発生回路
表示情報
出力源
表示情報
処理回路
DATA
CLK
1008
1000
1002
1004
200

(19)

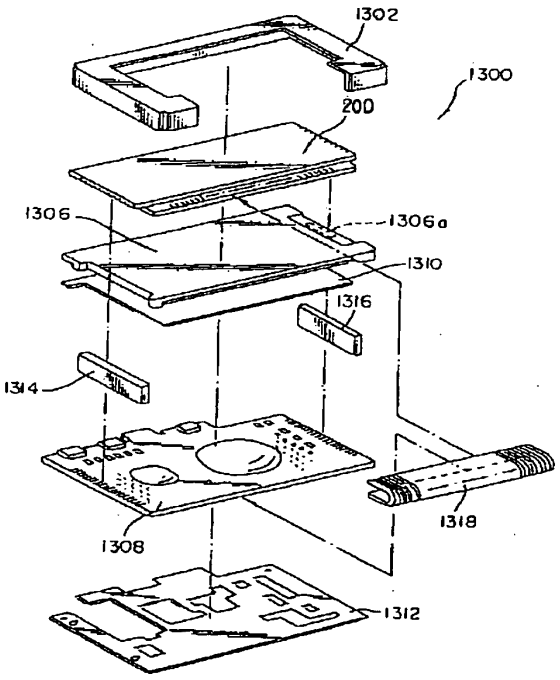
【図１０】



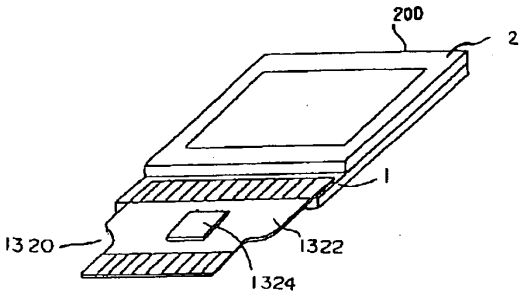
【図１１】



【図１２】



【図１３】



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3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Two or more data lines which intersect two or more scanning lines and said two or more scanning lines on a substrate, Two or more switching elements connected to two or more of said scanning lines and data lines, Two or more pixel electrodes connected to said two or more switching elements, and a data signal supply means to supply the data signal corresponding to a picture signal to said two or more data lines based on a clock signal, The picture signal line which supplies said picture signal inputted from the 1st external input terminal to said data signal supply means, The electro-optic device characterized by having the clock signal line which supplies said clock signal inputted from the 2nd external input terminal to said data signal supply means, and the electric conduction line of the constant potential which shields said picture signal line electrically from said clock signal line.
[Claim 2] Said electric conduction line is an electro-optic device according to claim 1 characterized by including the part which consisted of constant potential lines which supply the power source of constant potential to said data signal supply means.
[Claim 3] said law -- a potential line -- difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part It is the electro-optic device according to claim 2 characterized by surrounding said picture signal line on said substrate, and the amount of [said / which consisted of potential lines the 2nd law] said electric conduction line part surrounding said clock signal line on said substrate.
[Claim 4] Said data signal supply means is an electro-optic device according to claim 2 or 3 which is equipped with the sampling circuit which samples said picture signal, and the data-line drive circuit which drives this sampling circuit based on said clock signal in response to the current supply from said constant potential line, and is characterized by taking about said picture signal line and said clock signal line from an opposite direction to said data-line drive circuit on said substrate.
[Claim 5] said 1st and 2nd external input terminal separates and arranges predetermined spacing mutually in the periphery of said substrate -- having -- **** -- between said 1st and 2nd external input terminals -- said law -- the power source of potential -- said law -- an electro-optic device given in any 1 term of claims 2-4 characterized by arranging the 3rd external input terminal for inputting into a potential line.
[Claim 6] Said electric conduction line is an electro-optic device given in any 1 term of claims 1-5 by which it is installing [so that the image display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said 1st substrate] characterized.
[Claim 7] It is the electro-optic device according to claim 6 which said substrate was countered, and the opposite substrate was formed, is further equipped with the frame of the protection-from-light nature formed at least in one side among said substrate and said opposite substrate along with the profile of image display field, and is characterized by said electric conduction line containing the part prepared in said substrate along with said frame in the location which counters said frame.
[Claim 8] Said electric conduction line and said data line are an electro-optic device given in any 1 term

of claims 1-7 characterized by being formed from the same low resistance metallic material.
[Claim 9] It is an electro-optic device given in any 1 term of claims 1-8 characterized by consisting of same low resistance metal layers formed by said electric conduction line part part list which intervenes between said picture signal line and a clock signal line on the same flat surface where said picture signal line and a clock signal line are parallel to said substrate.
[Claim 10] An electro-optic device given in any 1 term of claims 1-9 characterized by equipping said pixel electrode with the capacity line which gives the capacity of the specified quantity further, and connecting this capacity line to said electric conduction line.
[Claim 11] The frame of the protection-from-light nature which said substrate was countered, and the opposite substrate was formed and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, It is an electro-optic device given in any 1 term of claims 1-6 which equip said pixel electrode with the capacity line which gives capacity further, and are characterized by connecting said capacity line to said electric conduction line in said location which counters while said electric conduction line is installed in the location which counters said frame.
[Claim 12] Electronic equipment characterized by equipping claims 1-11 with the electro-optic device of a publication.

[Translation done.]

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3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of the electronic equipment using the electro-optic device of a active-matrix drive method and this by thin film transistor (TFT is called suitably below) drive, and belongs to the technical field of the electro-optic device of the format of driving the data line by the RF based on a clock signal by the data-line drive circuit especially prepared on the TFT array substrate, and the electronic equipment using this.
[0002]
[Description of the Prior Art] Conventionally, in electro-optic devices, such as liquid crystal equipment of the active-matrix drive method by TFT drive, many pixel electrodes are prepared on the TFT array substrate at many the scanning lines and the data-line lists which were arranged in all directions, respectively corresponding to each of these intersections. And in addition to these, a data signal supply means to supply a data signal to the data line including a data-line drive circuit, a sampling circuit, etc., and a scan signal supply means to supply a scan signal to the scanning line including a scanning-line drive circuit etc. may be established on such a TFT array substrate.
[0003] In this case, the data-line side reference clock used as the criteria of the supply timing of a data signal, the picture signal which supports the contents of the image which should be displayed and serves as a radical of a data signal, forward, a negative constant potential power source, etc. are supplied to a data signal supply means through the external input terminal and wiring which were prepared in the TFT array substrate, respectively. On the other hand, forward [used as the criteria of the supply timing of a scan signal / the scanning-line side reference clock and forward], a negative constant potential power source, etc. are supplied to a scan signal supply means through the external input terminal and wiring which were too prepared in the TFT array substrate. And in a scan signal supply means, a scan signal is supplied to the scanning line to the timing based on a scanning-line side reference clock, for example by the scanning-line drive circuit line sequential. A data-line drive circuit carries out the sequential drive of the sampling circuit which samples the picture signal inputted in the data signal supply means corresponding to this, for example to the timing based on a data-line side reference clock, and a data signal is supplied to the data line from a sampling circuit. These results, each TFT by which gate connection was made is made into switch-on at the scanning line according to supply of a scan signal, a data signal is supplied to a pixel electrode through the TFT concerned, and image display in each pixel is performed.
[0004] With the liquid crystal equipment for liquid crystal projectors, a picture signal with a serial, very high frequency is increasingly inputted recent years especially with high-resolution-izing of a display image. That it should correspond to this, the frequency of the data-line side reference clock supplied to especially a data signal supply means is also very high, and it is carried out.
[0005]
[Problem(s) to be Solved by the Invention] However, under the request of high-definition-izing of a display image in recent years, generating of the clock noise of a RF by making the frequency of a

reference clock high in this way cannot ignore now.
[0006] That is, in the configuration which supplies the conventional data-line side reference clock with a comparatively low frequency to a data-line drive circuit, for example, and drives a sampling circuit, by having raised the frequency of a clock signal as it was, the clock noise of high frequency will occur in the data signal outputted from the inside of the picture signal inputted into a sampling circuit, or a sampling circuit, and the data signal which should be supplied at the data line will deteriorate. Thus, in having received supply of the data signal which deteriorated, there is a trouble displayed with each pixel electrode of carrying out image mist beam degradation.
[0007] This invention is made in view of an above-mentioned trouble, and generating of the clock noise of the RF in the data signal generated based on the inside of the inputted picture signal or this can be reduced, and let it be a technical problem to offer electronic equipment equipped with the electro-optic device which can perform high-definition image display, and the electro-optic device concerned.
[0008]
[Means for Solving the Problem] Two or more scanning lines [top / substrate] in order that an electro-optic device according to claim 1 may solve the above-mentioned technical problem, Two or more data lines which intersect said two or more scanning lines, and two or more switching elements connected to two or more of said scanning lines and data lines, Two or more pixel electrodes connected to said two or more switching elements, and a data signal supply means to supply the data signal corresponding to a picture signal to said two or more data lines based on a clock signal, The picture signal line which supplies said picture signal inputted from the 1st external input terminal to said data signal supply means, It is characterized by having the clock signal line which supplies said clock signal inputted from the 2nd external input terminal to said data signal supply means, and the electric conduction line of the constant potential which shields said picture signal line electrically from said clock signal line.
[0009] According to the electro-optic device according to claim 1, the picture signal inputted from the 1st external input terminal is supplied to a data signal supply means through the picture signal line wired by the substrate. In parallel to this, the clock signal inputted from the 2nd external input terminal is supplied to a data signal supply means through the clock signal line wired by the substrate. Then, based on a clock signal, the data signal corresponding to a picture signal is supplied to two or more data lines by the data signal supply means which was formed in the substrate, for example, is constituted including a data-line drive circuit, a sampling circuit, etc. The picture signal line is electrically shielded from the clock signal line by the electric conduction line of the constant potential wired by the substrate especially here. Therefore, even when the frequency of a clock signal is high, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced.
[0010] A scan signal is supplied to a switching element through the scanning line by the scan signal supply means including the scanning-line drive circuit which was formed in the substrate or was connected to the substrate on the other hand. The electrical potential difference impressed to a pixel electrode by the data signal which the data signal corresponding to the picture signal with which the clock noise of high frequency was reduced as mentioned above is supplied to a switching element through the data line in parallel to this, and is further supplied through a switching element changes, and the liquid crystal which counters the pixel electrode concerned drives. image quality deteriorates according to generating of the clock noise of a RF, using [the resolution of the image which should be displayed is high the above result, and] a clock signal with a high frequency corresponding to this, also when the serial picture signal of a RF is inputted -- most -- or it is completely lost and high-definition image display is made possible.
[0011] An electro-optic device according to claim 2 is characterized by said electric conduction line containing the part which consisted of constant potential lines which supply the power source of constant potential to said data signal supply means in an electro-optic device according to claim 1.
[0012] Since the part which consisted of constant potential lines by which an electric conduction line supplies the power source of constant potential to said data signal supply means according to the electro-optic device according to claim 2 is included, in other words, it also becomes very easy by sharing an external input terminal and the wiring itself to be able to attain simplification and space-saving-izing of

a configuration, especially to make an electric conduction line into constant potential by installing a constant potential line and considering as an electric conduction line.
[0013] An electro-optic device according to claim 3 is set to an electro-optic device according to claim 2. Said constant potential line difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part Said picture signal line is surrounded on said substrate, and a part for said said electric conduction line part which consisted of potential lines the 2nd law is characterized by surrounding said clock signal line on said substrate.
[0014] According to the electro-optic device according to claim 3, the picture signal line is surrounded by the amount of [by which potential lines were consisted of the 1st law in order to supply the negative supply of for example, touch-down potential] electric conduction line part on the substrate. The clock signal line is surrounded by the amount of [by which potential lines were consisted of the 2nd law in order to supply a positive supply] electric conduction line part on the substrate. Therefore, the configuration from which the picture signal line was shielded [line / clock signal] by the duplex on the substrate is obtained.
[0015] The electro-optic device according to claim 4 is equipped with the sampling circuit where said data signal supply means samples said picture signal, and the data-line drive circuit which drives this sampling circuit based on said clock signal in response to the current supply from said constant potential line in the electro-optic device according to claim 2 or 3, and said picture signal line and said clock signal line are characterized by taking about from an opposite direction to said data-line drive circuit on said substrate.
[0016] According to the electro-optic device according to claim 4, a picture signal is sampled by the sampling circuit in a scan signal supply means. And the picture signal with which the sampling circuit drove and was sampled by the data-line drive circuit which receives the current supply from a constant potential line based on the clock signal is supplied to the data line as a data signal. Especially, although the picture signal line and the clock signal line are taken about from the opposite direction to the data-line drive circuit on the substrate, since an electromagnetic wave generally decreases according to mediation of distance and an obstruction, the electromagnetic wave impressed to a picture signal line decreases here according to existence of a data-line drive circuit from a clock signal line, corresponding to the distance between both signal lines. Therefore, even when the frequency of a clock signal is high, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced further.
[0017] In an electro-optic device given in any 1 term of claims 2-4, in the periphery of said substrate, said 1st and 2nd external input terminal separates predetermined spacing mutually, and is arranged, and an electro-optic device according to claim 5 is characterized by arranging the 3rd external input terminal for inputting the power source of said constant potential into said constant potential line between said and 2nd external input terminals.
[0018] According to the electro-optic device according to claim 5, in between, the 1st and 2nd external input terminal separates predetermined spacing mutually, is arranged in the periphery of a substrate, through the 3rd external input terminal, mutually, and is preferably detached and arranged as much as possible mutually in the field which can form an external input terminal in the periphery of a substrate. As compared with the case where followed, for example, contiguity arrangement of a picture signal line and the clock signal line is carried out, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced.
[0019] An electro-optic device according to claim 6 is installing [so that the image display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said substrate] characterized by said electric conduction line in an electro-optic device given in any 1 term of claims 1-5.
[0020] According to the electro-optic device according to claim 6, by the electric conduction line, since an image display field and two or more data lines are surrounded on the substrate, an image display field

and two or more data lines concerned will also be shielded from a clock signal line. Therefore, generating of the clock noise of a RF in the data signal outputted from the data signal supply means, the data signal which reached the switching element and the pixel electrode can be reduced.
[0021] An electro-optic device according to claim 7 is set to an electro-optic device according to claim 6. It has further the frame of the protection-from-light nature which countered said substrate, and it came to prepare an opposite substrate, and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field. It is characterized by said electric conduction line containing the part prepared in said substrate along with said frame in the location counters said frame.
[0022] since the electric conduction line is formed in the bottom of the frame of a substrate according to the electro-optic device according to claim 7, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line drive circuit and a data-line drive circuit in the circumference part of the 1st substrate with allowances, and the display area in an electro-optic device also decreases by electric conduction line formation -- most -- or there is completely nothing.
[0023] An electro-optic device according to claim 8 is characterized by forming said electric conduction line and said data line from the same low resistance metallic material in an electro-optic device given in any 1 term of claims 1-7.
[0024] According to the electro-optic device according to claim 8, since the electric conduction line is formed from the same low resistance metallic material as the data lines, such as aluminum (aluminum), even if the leading-about field of an electric conduction line is long, resistance of an electric conduction line will be suppressed low practically enough. That is, since it becomes possible to wire the large field which sewed clearances, such as other wiring and a circuit, for example, wired zigzag for a long time, or included the electric conduction line in it to the image display field etc. for a long time in an electric conduction line, without lowering the effectiveness of shielding by the increment in resistance, a comparatively easy configuration can raise the effectiveness of the shielding concerned more as a whole. Furthermore, in the manufacture process of the electro-optic device concerned, an electric conduction line and the data line can be formed according to the same process from the same low resistance metallic material. That is, the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.
[0025] An electro-optic device according to claim 9 is characterized by said picture signal line and a clock signal line consisting of same low resistance metal layers formed on the same flat surface parallel to said 1st substrate at said electric conduction line part part list which intervenes between said picture signal line and a clock signal line in an electro-optic device given in any 1 term of claims 1-8.
[0026] According to the electro-optic device according to claim 9, since a part for the electric conduction line part which intervenes between a picture signal line and a clock signal line is formed on the picture signal line, the clock signal line, and the same flat surface parallel to a substrate, the effectiveness of shielding is demonstrated more efficiently. Here, the same flat-surface top means that you may wire these on the layer insulation layer formed on the semi-conductor layer of switching elements, such as an insulating-layer top used as the substrate which could wire these directly on the substrate or was formed on the substrate, and TFT. Furthermore, in the manufacture process of the electro-optic device concerned, since an electric conduction line, a picture signal line, and a clock signal line can be collectively formed from a low resistance metal layer for example, with same aluminum layer etc., the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.
[0027] The electro-optic device according to claim 10 equips said pixel electrode with the capacity line which gives the capacity of the specified quantity further in the electro-optic device given in any 1 term of claims 1-9, and it is characterized by connecting this capacity line to said electric conduction line.
[0028] According to the electro-optic device according to claim 10, since the capacity of the specified quantity is given to the pixel electrode by the capacity line, even if duty ratio is small, a high definition display is enabled. And the capacity line is connected to the electric conduction line. Therefore, the bad influence to the switching element and pixel electrode by potential fluctuation of a capacity line is

prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction lines.
[0029] The frame of the protection-from-light nature which the electro-optic device according to claim 11 countered said substrate, and the opposite substrate was formed, and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, Said pixel electrode is further equipped with the capacity line which gives capacity, and said electric conduction line is characterized by connecting said capacity line to said electric conduction line in said location which counters while it is installed in the location which counters said frame.
[0030] since opposite arrangement of the electric conduction line is carried out at the frame of a substrate according to the electro-optic device according to claim 11, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line drive circuit and a data-line drive circuit in the circumference part of the 1st substrate with allowances, and the display area in an electro-optic device also decreases by electric conduction line formation -- most -- or there is completely nothing. Moreover, since the capacity line is connected to the electric conduction line, the bad influence to the switching element and pixel electrode by potential fluctuation of a capacity line is prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction lines. Moreover, the connection between an electric conduction line and a capacity line can use a tooth space effectively for a frame, without decreasing a TFT substrate top display area, since opposite arrangement is carried out.
[0031] Electronic equipment according to claim 12 is characterized by equipping claims 1-10 with the electro-optic device of a publication.
[0032] According to electronic equipment according to claim 12, it has the electro-optic device of the invention in this application mentioned above, the clock noise of a RF is reduced, and the high-definition image display of electronic equipment becomes possible.
[0033] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.
[0034]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing. In addition, this operation gestalt explains, using liquid crystal equipment as an example of an electro-optic device.
[0035] (Configuration of liquid crystal equipment) The configuration of the gestalt of operation of liquid crystal equipment is explained based on drawing 6 from drawing 1 . Drawing 1 is the top view showing the configuration of a various wiring, a circumference circuit, etc. which were prepared on the TFT array substrate in the gestalt of operation of liquid crystal equipment. Drawing 2 It is the top view showing the more detailed two-dimensional layout of drawing 1 . Drawing 3 It is the A-A' sectional view of drawing 2 showing wiring of a picture signal line, a clock signal line, etc. drawing 4 It is the expansion top view of the pixel part of drawing 1 , drawing 5 is the top view which looked at the TFT array substrate from the opposite substrate side with each component formed on it, and drawing 6 is a H-H' sectional view of drawing 5 shown including an opposite substrate.
[0036] Liquid crystal equipment 200 is equipped with the TFT array substrate 1 which consists of a quartz substrate, hard glass, etc. in drawing 1 . Two or more pixel electrodes 11 prepared in the shape of a matrix on the TFT array substrate 1, The data line 35 which two or more arrays are carried out in the direction of X, and is extended along the direction of Y, respectively, The scanning line 31 which two or more arrays are carried out in the direction of Y, and is extended along the direction of X, respectively, While intervening between each data line 35 and the pixel electrode 11, respectively, two or more

TFT30 as an example of the switching element which controls the switch-on and the non-switch-on between these according to the scan signal supplied through the scanning line 31, respectively, respectively is formed. Moreover, on the TFT array substrate 1, capacity line 31' (storage capacitance electrode) which is wiring for the below-mentioned storage capacitance (refer to drawing 6) is formed in parallel with the scanning line 31.

[0037] On the TFT array substrate 1, the sampling circuit 301 and the data-line drive circuit 101 which constitute an example of a data signal supply means, and the scanning-line drive circuit 104 are formed further. moreover, to the surface of the image display field (namely, field of the liquid crystal equipment with which an image is actually displayed by the orientation change of state of liquid crystal) specified with two or more pixel electrodes 11 Two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of an image display field is formed, and the vertical flow terminal 106 for taking an electric flow between the TFT array substrate 1 and an opposite substrate is formed in the four corners of an image display field. The signal name inputted through the external input terminal 102 prepared along the lower side of the TFT array substrate 1 in explanation of drawing 3 and its signal wiring are made into what (for example, the signal wiring is called "Wiring CLX" to the "clock signal CLX" which is a signal name) the alphabet notation same for easy-izing of explanation is added, respectively, and is referred to for after a signal and wiring from drawing 1 below. [two or more]

[0038] The scanning-line drive circuit 104 starts a built-in shift register circuit by the input of the start signal DY for scanning-line drive circuits, using the negative supply VSSY and positive supply VDDY for scanning-line drive circuits which are supplied to external input terminal 102 list through Wiring VSSY and VDDY from an external control circuit as a power source. and -- an external input -- a terminal -- 102 -- a list -- wiring -- CLY -- and -- CLY -- ' -- minding -- supplying -- having -- the scanning line -- a drive -- a circuit -- ** -- a reference clock -- a signal -- CLY -- and -- the -- reversal -- a clock signal -- CLY -- ' -- being based -- predetermined -- timing -- the scanning line 31 -- a scan signal -- a pulse ---like -- line sequential -- impressing .

[0039] The data-line drive circuit 101 starts a built-in shift register circuit by the input of start signal DX for data-line drive circuits, using the negative supply VSSX and positive supply VDDX for data-line drive circuits which are supplied to external input terminal 102 list through signal wiring VSSX and VDDX from an external control circuit as a power source. and the reference clock signal CLX for data-line drive circuits supplied to external input terminal 102 list through Wiring CLX and CLX' and its reversal clock signal CLX -- ' -- being based -- It doubles with the timing to which the scanning-line drive circuit 104 impresses a scan signal. About picture signal [which is supplied through the external input terminal 102 and wiring VID1-VID6 / by which serial-parallel conversion was carried out] VID1 - VID6 each, for example to six phases A sampling circuit driving signal is minded every data line 35, the sampling circuit drive signal line 306 is minded [301], and it supplies to predetermined timing.

[0040] The sampling circuit 301 is equipped with TFT302 every data line 35, wiring VID1-VID6 is connected to the source electrode of TFT302, and the sampling circuit drive signal line 306 is connected to the gate electrode of TFT302. And an input of picture signals VID1-VID6 samples these picture signals. Moreover, if a sampling circuit driving signal is inputted from the data-line drive circuit 101 through the sampling circuit drive signal line 306, sequential impression of the picture signal sampled about picture signal VID1 - VID6 each will be carried out for every group who consists of the six adjoining data lines 35. As mentioned above, the data-line drive circuit 101 and the sampling circuit 301 are constituted so that the picture signals VID1-VID6 by which serial-parallel conversion was carried out may be supplied to six phases as a data signal at the data line 35. Although the gestalt of this operation described the method which chooses as coincidence the sampling circuit 301 connected to the six adjoining data lines 35, and consists of the six data lines 35 and which carries out the sequential transfer for every group, the data line 35 may be chosen for [every] and adjoining 2, 3, --, 5, or 7 or more may be chosen as coincidence. Moreover, as long as the write-in property of TFT302 which constitutes not only six phases but the sampling circuit 301 of the number of serial-parallel conversion of the picture signal supplied to the data line 35 is good, five or less phases are sufficient as it, and as long as the frequency of a picture signal is high, it may be increased to seven or more phases. Under the

present circumstances, it cannot be overemphasized that the external input terminal 102 and picture signal line for picture signals only of the number of serial-parallel conversion of a picture signal are the need at least.

[0041] As shown in drawing 2 , if start signal DX is inputted, after the data-line drive circuit 101 shapes in waveform and buffers the transfer signal from shift-register-circuit 101a which starts sequential generation of the reference clock signal CLX and the transfer signal based on the reversal clock signal CLK', and shift-register-circuit 101a, it is equipped with wave control circuit 101b and buffer circuit 101c which are supplied to a sampling circuit 301 through the sampling circuit drive signal line 306. Moreover, corresponding to the picture signals VID1-VID6 with which serial-parallel conversion of the sampling circuit 301 was carried out at six phases, six TFT(s)302 are connected at a time to each sampling circuit drive signal line 306 at parallel. That is, the switches S1-S6 which consist of TFT(s)302 are connected to 1 Motome's sampling circuit drive signal line 306 from the left, switches S7-S12 are connected to 2 Motome's sampling circuit drive signal line 306 from the left, and switch Sn-5 - Sn are connected to the right end sampling circuit drive signal line 306.

[0042] Especially with the gestalt of this operation, as shown in drawing 1 and drawing 2 , the shielding wire 82 of the constant potential which served as the electric conduction line (shielding wire is called hereafter) 80 of the constant potential which served as the wiring VSSX for negative supplies VSSX, and the wiring VDDX for positive supplies VDDX to the TFT array substrate 1 is wired. By such shielding wire 80 and 82, wiring VID1-VID6 is electrically shielded from Wiring CLX and CLX'. Therefore, even when the frequency of a clock signal CLX is high, the diving of the clock noise of the RF to Wiring CLX and the wiring VID1-VID6 from CLX' can be reduced.

[0043] In addition, the frequency of the clock signal CLY (and the reversal clock signal CLY') for a scanning-line drive is far low compared with the frequency of the above-mentioned clock signal CLX (and the reversal clock signal CLX') for a data-line drive. Therefore, about a clock signal CLY and CLY', it is rare for the clock noise of a RF to pose a problem. However, in the gestalt of this operation, as shown in drawing 1 and drawing 2 , wiring VID1-VID6 is wired also from Wiring CLY and CLY', by shielding wire 80 and 82, so that it may shield. That is, along the bottom of the frame 53 of the protection-from-light nature prepared in the opposite substrate 2, the shielding wire 80 which was installed from the external input terminal 102 and served as the negative supply VSSX of the data-line drive circuit 101 is wired so that an image display field may be surrounded. Therefore, not only the wiring VID1-VID6 for picture signals but the diving of the noise from the circumference circuit to the data line 35 with which a data signal is written in through TFT302 of a sampling circuit 301 can be reduced.

[0044] Especially, with the gestalt of this operation, by installing Wiring VSSX and VDDX, respectively and considering as shielding wire 80 and 82, it becomes possible to share an external input terminal and wiring, and simplification and space-saving-izing of an equipment configuration can be attained. Moreover, potential of shielding wire 80 and 82 is easily made constant potential by common use-ization with a constant potential line in this way. However, you may wire wiring for power sources, and shielding wire separately.

[0045] Moreover, as long as the supply voltage for driving the data-line drive circuit 101 and the scanning-line drive circuit 104 is mutually the same, VSSX and VSSY which are the potential (negative potential) of VDDX which is the potential (forward potential) of a positive supply and VDDY, and a negative supply may be made to share, respectively. If such a configuration is taken, since wiring installed from an external input terminal and it is reducible, it is advantageous.

[0046] With the gestalt of this operation, as shown in drawing 2 , two external input terminals 102 into which a negative supply VSSX is inputted are formed, and the-two wiring VSSX is formed corresponding to this. And wiring VID1-VID6 is surrounded on the TFT array substrate 1 by the shielding wire 80 made into the potential (negative potential) of a negative supply VSSX. Especially the shielding wire 80 formed from metal layers, such as the same aluminum as the data line 35, also between shift-register-circuit 101a and wave control circuit 101b is installed. And through the shielding-wire connection 81 which metal layers, such as aluminum, set caudad through the insulating layer

between the 1st layer like the after-mentioned, for example, was formed from conductive layers, such as the same polish recon as the scanning line 31, as the point of the installed shielding wire 80 surrounds wave control circuit 101b and buffer circuit 101c, it is connected to shielding wire 80.
[0047] On the other hand, as shown in drawing 2 , Wiring CLX and CLX' are surrounded on the TFT array substrate 1 in the part which adjoins the data-line drive circuit 101 by the shielding wire 82 made into the potential (forward potential) of a positive supply VDDX. Especially the shielding wire 82 formed from metal layers, such as the same aluminum as the data line 35, also between wave control circuit 101b and buffer circuit 101c is installed, and as the point surrounds wave control circuit 101b and shift-register-circuit 101a through the shielding-wire connection 83 formed from conductive layers, such as the same polish recon as the scanning line 31, it is connected to shielding wire 82.
[0048] Therefore, the configuration shielded by the duplex is taken from Wiring CLX and CLX' on the TFT array substrate 1, and let wiring VID1-VID6 be what has dependability high [shielding to wave control circuit 101b and buffer circuit 101c] at the shift-register-circuit 101a list. However, if it constitutes as intervened in shielding wire 80 or at least one 82 between Wiring CLX, and CLX' and wiring VID1-VID6 even if it does not take the configuration surrounded in this way, the effectiveness of shielding will be acquired somewhat.
[0049] With the gestalt of this operation, as shown in drawing 1 and drawing 2 , wiring VID1-VID6, Wiring CLX, and CLX' are taken about by the opposite sense along the direction of X on the TFT array substrate 1 (namely, the former a clockwise rotation, latter is counter clockwise). Therefore, since the electromagnetic wave which transmits between these wiring according to mediation of the data-line drive circuit 101 among these wiring decreases since the distance during these wiring becomes large as a whole and, even when the frequency of a clock signal CLX and CLX' is high, the diving of the clock noise of the RF to Wiring CLX and the wiring VID1-VID6 from CLX' can be reduced further. Moreover, even if, as for leading about of Wiring CLX, and CLX' and wiring VID1-VID6, the direction interchanges, it is satisfactory in any way. That is, Wiring CLX and CLX' may be shielded by the negative supply VSSX, and wiring VID1-VID6 may be shielded by the positive supply VDDX. However, if it constitutes as intervened in shielding wire 80 or at least one 82 between Wiring CLX, and CLX' and wiring VID1-VID6 even if it does not take the configuration taken about to an opposite direction in this way, the effectiveness of shielding will be acquired somewhat.
[0050] With the gestalt of this operation, in between, through three external input terminals 102 for the object for negative supply VSSX, the object for positive supply VDDX, and start signal DX, a clock signal CLX and the external input terminal 102 for CLX', and the external input terminal 102 a picture signal VID1 - for VID6 separate predetermined spacing mutually, and are arranged mutually. And in the periphery of the TFT array substrate 1, in the field which can form the external input terminal 102, the external input terminal 102 of a clock signal CLX and the external input terminal 102 for CLX', and the for a picture signal VID1 - for VID6 as possible detaches mutually, and is arranged, and the external input terminal 102 more than a piece is preferably arranged among both at least. Thus, if constituted, as compared with the case where contiguity arrangement of a picture signal line and the clock signal line is carried out, for example, the diving of the clock noise of the RF to wiring for picture signals from wiring for clocks can be reduced.
[0051] With the gestalt of this operation, as shown in drawing 1 and drawing 2 , an image display field and two or more data lines 35 are surrounded on the TFT array substrate 1 by shielding wire 80. For this reason, an image display field and two or more data lines 35 concerned are also shielded from Wiring CLX and CLX'. Therefore, generating of the clock noise of a RF in the sampling circuit driving signal outputted from the data-line drive circuit 101, the data signal which reached TFT30 and the pixel electrode 11 can be reduced. However, if it constitutes so that the wiring VID1-VID6 until it reaches a sampling circuit 301 may be shielded by shielding wire 80 or 82 even if it does not take the configuration surrounded to an image display field in this way, the effectiveness of shielding will be acquired somewhat.
[0052] It is formed from the various wiring DY connected to the external input terminal 102 which contains shielding wire 80 and 82 in drawing 3 as shown in a sectional view, VSSY, --, the low

resistance [with same VDDX] metallic material as the data lines 35, such as aluminum (aluminum). Therefore, even if the leading-about field of shielding wire 80 and 82 is long, resistance of shielding wire 80 and 82 will be suppressed low practically enough. That is, as shown in drawing 2 , the clearance between wave control circuit 101b and buffer circuit 101c is sewn in other various wiring or a shift-register-circuit 101a list, and the large field which could wire zigzag for a long time and included shielding wire 82 in it to the image display field further can be wired for a long time in shielding wire 80. Thus, a comparatively easy configuration can raise the effectiveness of the shielding concerned as a whole. Moreover, as shown in drawing 3 , it is formed the various wiring DY connected to the external input terminal 102 containing shielding wire 80 and 82, VSSY, --, on the insulating layer 42 between the 1st layer by which VDDX was formed in the TFT array substrate 1, i.e., the same layer. Therefore, the effectiveness of shielding is demonstrated more efficiently. Furthermore, if constituted in this way, since the various wiring DY, VSSY, --, VDDX are put in block according to the same process and can be formed in the manufacture process of liquid crystal equipment 200 from a low resistance metal layer for example, with same aluminum layer etc., it is advantageous on manufacture.

[0053] In addition, the signal LCCOM inputted from the external input terminal 102 shown in drawing 3 from drawing 1 is a power-source signal of a common electrode, and is supplied to the common electrode (refer to drawing 7) prepared in the below-mentioned opposite substrate through the flow material on Wiring LCCOM and the above-mentioned vertical flow terminal 106.

[0054] As shown in the top view of drawing 4 here, capacity line 31' is formed from the conductive polish recon layer same with the scanning line 31 etc. in parallel with the scanning line 31 on the TFT array substrate 1, and is connected to shielding wire 80 through contact hole 80a. Thus, if constituted, wiring for making capacity line 31' into constant potential can be made to serve a double purpose with shielding wire 80, and an external input terminal required in order to make capacity line 31' into constant potential can also be made to serve a double purpose with the external input terminal 102 for shielding-wire 80.

[0055] Especially with the gestalt of this operation, the sampling circuit 301 is formed on the TFT array substrate 1 in the location which counters the frame 53 of the protection-from-light nature formed in the opposite substrate 2 as shown in drawing 5 and drawing 6 , as the slash field in drawing 1 shows, and the data-line drive circuit 101 and the scanning-line drive circuit 104 are formed on the narrow long and slender circumference part of the TFT array substrate 1 which does not face the liquid crystal layer 50. On the TFT array substrate 1, the sealant 52 which consists of a photo-setting resin as an example of the seal member which sticks both substrates in the perimeter of an image display field, and surrounds the liquid crystal layer 50 is formed along the image display field. And between the image display fields and sealants 52 on the opposite substrate 2, the frame 53 of protection-from-light nature is formed.

[0056] When put into the TFT array substrate 1 by the case of protection-from-light nature which opening was able to open behind corresponding to the image display field, a frame 53 so that the image display field concerned may not hide in the edge of opening of the case concerned according to a manufacture error etc. That is, it is formed from the band-like protection-from-light nature ingredient which has width of face of 500 micrometers or more in the perimeter of an image display field so that the gap of about hundreds of micrometers to the case of the TFT array substrate 1 may be permitted, for example. The frame 53 of such protection-from-light nature is formed in the opposite substrate 2 of sputtering and the photolithography which used metallic materials, such as Cr (chromium), nickel (nickel), and aluminum (aluminum), and etching. Or it is formed from ingredients, such as resin black which distributed carbon and Ti (titanium) to the photoresist.

[0057] The data-line drive circuit 101 and the external input terminal 102 are formed in the field of the outside of a sealant 52 along the lower side of an image display field, and the scanning-line drive circuit 104 is established in the both sides of an image display field along with two sides of right and left of an image display field. And the opposite substrate 2 with the almost same profile as a sealant 52 has fixed to the TFT array substrate 1 by the sealant 52 concerned.

[0058] As mentioned above shielding wire 80 and a sampling circuit 301 If the case of opposite arrangement, i.e., this operation gestalt, is prepared in the bottom of a frame 53 at the frame 53 on the

TFT array substrate 1 Space-saving-ization on the TFT array substrate 1 is attained, for example, the scanning-line drive circuit 104 and the data-line drive circuit 101 can be formed in the circumference part of the TFT array substrate 1 with allowances. the display area in liquid crystal equipment 200 also decreases by formation of shielding wire 80 -- most -- or there is completely nothing. Moreover, shielding wire 80 can use a tooth space effectively, without decreasing the display area on a TFT substrate, if shielding wire 80 and capacity line 31' are connected in the location which counters while being installed in the location which counters a frame 53.
[0059] (Configuration of the whole liquid crystal equipment) Next, the concrete configuration of liquid crystal equipment 200 is explained with reference to drawing 7 and drawing 8 . It is the sectional view where it is the sectional view which drawing 7 shows TFT30 part of liquid crystal equipment, and met at B-B' in drawing 4 , and drawing 8 met the shielding wire 80 of the liquid crystal equipment under a frame here. In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 7 and drawing 8 .
[0060] In the sectional view of drawing 7 , liquid crystal equipment 200 is equipped with an insulating layer 43, the pixel electrode 11, and the orientation film 12 between an insulating layer 42, the data line 35, and the 2nd layer in TFT30 part prepared in each pixel between the semi-conductor layer 32 by which the laminating was carried out to the TFT array substrate 1 list on it, the gate insulating layer 33, the scanning line 31 (gate electrode), and the 1st layer. Liquid crystal equipment 200 is equipped with the common electrode 21, the orientation film 22, and light-shielding film 23 by which the laminating was carried out to the opposite substrate 2 list which consists of a glass substrate on it again. Liquid crystal equipment 200 is further equipped with the liquid crystal layer 50 as electrooptic material pinched among both these substrates.
[0061] Here, the configuration of each class except TFT30 is first explained in order among these layers.

[0062] Insulating layers 42 and 43 consist of silicate glass film, such as NSG (non silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (boron phosphorus silicate glass), a silicon nitride film, silicon oxide film, etc. with about 5000-15000A **** between the 1st and the 2nd layer, respectively. In addition, the layer insulation layer used as the substrate of TFT30 may be formed from the silicate glass film, a silicon nitride film, the silicon oxide film, etc. on the TFT array substrate 1.
[0063] The pixel electrode 11 consists of transparent conductive thin films, such as for example, ITO (indium Tin oxide) film. Such a pixel electrode 11 is formed by giving a photolithography process and an etching process etc., after depositing the ITO film etc. on the thickness of about 500-2000A by sputtering processing etc. In addition, when using the liquid crystal equipment 200 concerned for the liquid crystal equipment of a reflective mold, the pixel electrode 11 may be formed from an opaque ingredient with high reflection factors, such as aluminum.
[0064] The orientation film 12 consists of organic thin films, such as for example, a polyimide thin film. Such orientation film 12 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc., after applying the coating liquid of for example, a polyimide system.
[0065] It goes across the common electrode 21 all over the opposite substrate 2, and it is formed. Such a common electrode 21 is formed by giving a photolithography process and an etching process etc., after depositing the ITO film etc. on the thickness of about 500-2000A for example, by sputtering processing etc.
[0066] The orientation film 22 consists of organic thin films, such as for example, a polyimide thin film. Such orientation film 22 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc., after applying the coating liquid of for example, a polyimide system.
[0067] The light-shielding film 23 is formed in the predetermined field which counters TFT30. Like the above-mentioned frame 53, such a light-shielding film 23 is formed of sputtering and the

photolithography using metallic materials, such as Cr and nickel, and etching, or is formed from ingredients, such as resin black which distributed carbon and Ti to the photoresist. A light-shielding film 23 has functions other than the protection from light to the semi-conductor layer 32 of TFT30, such as improvement in contrast, and color mixture prevention of color material.
[0068] The liquid crystal layer 50 is formed when liquid crystal is enclosed with the space surrounded by the sealant 52 (refer to drawing 5 and drawing 6) between the TFT array substrates 1 and the opposite substrates 2 which have been arranged so that the pixel electrode 11 and the common electrode 21 may meet by vacuum suction etc. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 12 and 22 in the condition that the electric field from the pixel electrode 11 are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant 52 may stick two substrates 1 and 2 around those, and the spacer for making distance between both substrates into a predetermined value is mixed.
[0069] Next, the configuration of each class concerning TFT30 is explained in order.
[0070] TFT30 is equipped with the source field 34 formed in the gate insulating layer 33 which insulates the semi-conductor layer 32 in which a channel is formed of the electric field from the scanning line 31 and the scanning line 31, and the scanning line 31 and the semi-conductor layer 32, and the semi-conductor layer 32, the data line 35, and the drain field 36 formed in the semi-conductor layer 32. One to which it corresponds of two or more pixel electrodes 11 is connected to the drain field 36. The source field 34 and the drain field 36 are formed by doping the dopant the object for n molds of predetermined concentration, or for p molds to the semi-conductor layer 32 like the after-mentioned according to whether the channel of n mold or p mold is formed. TFT of an n-type channel has the advantage that a working speed is quick, and it is used as TFT30 which is the switching element of a pixel in many cases.

[0071] The semi-conductor layer 32 which constitutes TFT30 is formed by performing annealing treatment and making the thickness of about 500-2000A carry out solid phase growth after forming the a-Si (amorphous silicon) film for example, on the TFT array substrate 1. Under the present circumstances, in the case of TFT30 of an n channel mold, you may dope by the ion implantation which used the dopant of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn). Moreover, in the case of TFT30 of a p channel mold, it dopes by the ion implantation which used the dopant of III group elements, such as B (boron), Ga (gallium), and In (indium). When setting especially TFT30 to TFT of an n channel mold with LDD (Lightly DopedDrain) structure, among the source field 34 and the drain field 36, a low concentration dope field is formed in the part which adjoins at a channel side, respectively by the dopant of V group elements, such as P, and, similarly a high concentration dope field is formed in the semi-conductor layer 32 of p mold by the dopant of V group elements, such as P. Moreover, when referred to as TFT30 of a p channel mold, the dopant of III group elements, such as B, is used for the semi-conductor layer 32 of n mold, and the source field 34 and the drain field 36 are formed. Thus, when it considers as LDD structure, the advantage which can reduce the short channel effect is acquired. In addition, TFT30 is good for the low concentration dope field in LDD structure also as TFT of the offset structure which carried out the ion implantation, and good also as TFT of the self aryne mold which forms the source [high concentration / in self align], and a drain field by doping high-concentration impurity ion by using a gate electrode as a mask. Moreover, a gate electrode is prepared in a two-piece serial, it is good also as dual gate structure, and it cannot be overemphasized that a gate electrode may be prepared in a three or more piece serial. If such a configuration is taken, since the leakage current at the time of OFF of TFT30 is reduced and generating of a cross talk etc. can be controlled, high-definition liquid crystal equipment can be offered.
[0072] The gate insulating layer 33 can form and obtain the thermal oxidation film with a comparatively thin thickness of about 300-1500A by oxidizing the semi-conductor layer 32 thermally with the temperature of about 900-1300 degrees C. The good insulator layer which was excellent in the interface condition of the semi-conductor layer 32 and the gate insulating layer 33 by this can be formed.
[0073] After the scanning line 31 deposits the polish recon film with a reduced pressure CVD method

etc., it is formed of a photolithography process, an etching process, etc. Or it may be formed from a metal membrane or metal silicide film, such as aluminum. in this case, it also becomes possible to omit a part or all of a light-shielding film 23 by the protection-from-light nature which the metal membrane metallurgy group silicide film has if a light-shielding film 23 arranges the scanning line 31 as the part or the light-shielding film which boils all and corresponds of a wrap field. In this case, there is an advantage which can prevent decline in the pixel numerical aperture by the lamination gap with the opposite substrate 2 and the TFT array substrate 1 especially.
[0074] The data line 35 may be formed from transparent conductive thin films, such as ITO film, like the pixel electrode 11. Or you may form by sputtering processing etc. from low resistance metal metallurgy group silicide, such as aluminum deposited on the thickness of about 1000-5000A, etc.
[0075] Moreover, the contact hole 38 which leads to the contact hole 37 and the drain field 36 which lead to the source field 34 is formed in the insulating layer 42 between the 1st layer, respectively. Electrical installation of the data line 35 is carried out to the source field 34 through the contact hole 37 to this source field 34. Furthermore, the contact hole 38 to the drain field 36 is formed in the insulating layer 43 between the 2nd layer. Electrical installation of the pixel electrode 11 is carried out to the drain field 36 through the contact hole 38 to this drain field 36. The above-mentioned pixel electrode 11 is formed in the top face of an insulating layer 43 between the 2nd layer constituted in this way. If each contact hole is formed by dry etching, such as for example, reactant etching and reactant ion beam etching, detailed-ization of opening size of it is attained, and it can realize high numerical aperture-ization of a pixel.
[0076] In addition, if light carries out incidence of the semi-conductor layer 32 in which a channel is generally formed, a photocurrent will occur according to the photo-electric-conversion effectiveness which p-Si has, the transistor characteristics of TFT30 will deteriorate, but with the gestalt of this operation, since the light-shielding film 23 is formed in the location which counters the opposite substrate 2 at each TFT30, respectively, it is prevented that incident light carries out incidence to the semi-conductor layer 32. furthermore, this -- adding -- or -- replacing with -- a gate electrode -- the wrap from a top -- if the data line 35 is formed from opaque metal thin films, such as aluminum, like -- a light-shielding film 23 -- or the incidence of the incident light (namely, drawing 7 light from a top) to the semi-conductor layer 32 can be prevented effectively independently.
[0077] In drawing 7 , storage capacitance 70 is formed in the pixel electrode 11, respectively. 1st storage capacitance electrode 32' more specifically [this storage capacitance 70] formed of the same process as the semi-conductor layer 32, dielectric layer 33' formed of the same process as the gate insulating layer 33, and the capacity line 31 formed of the same process as the scanning line 31 -- ' (the 2nd storage capacitance electrode) -- It consists of some of insulating layers 42 and 43 and pixel electrodes 11 which counter a list at capacity line 31' through the 1st and the insulating layers 42 and 43 between the 2nd layer between the 1st and the 2nd layer. Thus, since storage capacitance 70 is formed, even if duty ratio is small, a high definition display is enabled.
[0078] As shown in the sectional view of drawing 8 , a frame 53 is countered and shielding wire 80 passes through an insulating-layer 42 top between the 1st layer in the upper location of two or more scanning lines 31. and it consists of metal thin films, such as aluminum formed at the process as the data line 35 mentioned above that almost all those parts of this shielding wire 80 are the same, -- low -- it is wiring [****]. Thus, in the manufacture process of liquid crystal equipment 200, since shielding wire 80 and the data line 35 can be formed collectively, it is advantageous on manufacture.
[0079] Since it is the same film formation process and a sampling circuit 301, the data-line drive circuit 101, and the circumference circuit of scanning-line drive circuit 104 grade can be formed especially with the gestalt of this operation at the time of formation of TFT30, it is advantageous on manufacture. For example, these circumference circuits are formed in the circumference part on the TFT array substrate 1 from two or more TFT(s) of the complementary-type structure which consists of n channel mold poly-Si TFT and p channel mold poly-Si TFT.
[0080] In addition, although not shown in drawing 7 and drawing 8 , it sets to liquid crystal equipment 200. To the side in which the incident light of the side in which the incident light of the opposite

substrate 2 carries out incidence, and the TFT array substrate 1 carries out outgoing radiation, respectively For example, TN (Twisted Nematic) mode and STN (super TN) mode, According to the exception of modes of operation, such as D-STN (double-STN) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, a polarizing plate, etc. are arranged in a predetermined direction.

[0081] Moreover, since the liquid crystal equipment 200 explained above is applied to an electrochromatic display projector, three liquid crystal equipments 200 will be used as a light valve for RGB, respectively, and incidence of the light of each color decomposed through the dichroic mirror for RGB color separation, respectively will be carried out to each equipment as incident light, respectively. Therefore, with the gestalt of each operation, the color filter is not prepared in the opposite substrate 2. However, the color filter of RGB may be formed in the predetermined field which counters the pixel electrode 11 with which a light-shielding film 23 is not formed in liquid crystal equipment 200 on the opposite substrate 2 with the protective coat. Or a color filter layer may be built in by the color resist of RGB so that it may correspond to each pixel on the TFT array substrate 1. If it does in this way, the liquid crystal equipment of the gestalt of this operation is applicable to electrochromatic display equipments, such as electrochromatic display television of direct viewing types other than a liquid crystal projector, or a reflective mold. Furthermore, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 2. If it does in this way, bright liquid crystal equipment is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 2 again may be formed. According to this opposite substrate with a die clo IKKU filter, brighter electrochromatic display equipment is realizable.

[0082] In order to set to liquid crystal equipment 200 and to control the poor orientation of the liquid crystal molecule by the side of the TFT array substrate 1, the flattening film may be further applied on a spin coat etc. on an insulating layer 43 between the 2nd layer, or CMP (Chemical Mechanical Polishing) processing may be performed. Or an insulating layer 43 may be formed by the flattening film between the 2nd layer.

[0083] Although it was explained that the switching element of liquid crystal equipment 200 was the poly-Si TFT of a forward stagger mold or a coplanar mold, the gestalt of this operation is effective also to TFT of other formats, such as TFT of a reverse stagger mold, and an amorphous silicon TFT.

[0084] In liquid crystal equipment 200, although the liquid crystal layer 50 was constituted from a pneumatic liquid crystal as an example, if the polymer dispersed liquid crystal which distributed liquid crystal as a minute grain in the macromolecule is used, the above-mentioned polarization film, a polarizing plate, etc. will become unnecessary in the orientation film 12 and 22 and a list, and the advantage of a raise in the brightness of liquid crystal equipment or low-power-izing by efficiency for light utilization increasing will be acquired. Furthermore, when applying liquid crystal equipment 200 to high-reflective-liquid-crystal equipment by constituting the pixel electrode 11 from a metal membrane with high reflection factors, such as aluminum, SH (super HOMEOTORO pick) mold liquid crystal with which perpendicular orientation of the liquid crystal molecule was mostly carried out in the state of no electrical-potential-difference impressing may be used. Furthermore, although the common electrode 21 is provided in the opposite substrate 2 side in liquid crystal equipment 200 again so that perpendicular electric field (vertical electric field) may be impressed to the liquid crystal layer 50 What (that is, the electrode for horizontal electric-field generating is prepared in the TFT array substrate 1 side, without preparing the electrode for vertical electric-field generating in the opposite substrate 2 side) the pixel electrode 11 is constituted also for from an electrode for horizontal electric-field generating of a pair, respectively so that electric field (horizontal electric field) parallel to the liquid crystal layer 50 may be impressed is possible. Thus, if horizontal electric field are used, it is advantageous when extending an angle of visibility rather than the case where vertical electric field are used. In addition, it is possible to apply the gestalt of this operation to various kinds of liquid crystal ingredients (liquid crystal phase), a mode of operation, a liquid crystal array, the drive approach, etc. Moreover, with an above-mentioned

operation gestalt, although explained using the configuration which forms TFT on a substrate, the configuration which forms a switching element is also applicable not only to such a configuration but a silicon substrate. Moreover, although explained using liquid crystal as electrooptic material, it is applicable not only to liquid crystal but electroluminescence or a plasma display etc.
[0085] In the gestalt of the operation explained above, well-known circumference circuits, such as a precharge circuit and an inspection circuit, may be further established in the periphery of the bottom of a frame 53, or the TFT array substrate 1. A precharge circuit is the timing preceded with the data signal supplied from the data-line drive circuit 101 to the data line 35 for the purpose of reduction of improvement in a contrast ratio, the stability of the potential level of the data line 35, and the Rhine unevenness on a display screen etc., and is a circuit which mitigates the load at the time of writing a data signal in the data line 35 by supplying a precharge signal. For example, an example of such a precharge circuit is indicated by JP,7-295520,A. On the other hand, an inspection circuit is a circuit for inspecting the quality of the liquid crystal equipment concerned at the manufacture middle or the time of shipment, a defect, etc. to the periphery of the bottom of a frame 53, or a TFT array substrate.
[0086] Moreover, in the gestalt of the above operation, the protection-from-light layer which consists of a refractory metal may be prepared also in the location (namely, under TFT30) which counters on the TFT array substrate 1 at TFT30 as indicated by JP,9-127497,A, JP,3-52611,B, JP,3-125123,A, JP,8-171101,A, etc. Thus, if a protection-from-light layer is prepared also in the TFT30 bottom, it can prevent that the return light from the TFT array substrate 1 side etc. carries out incidence to TFT30. Therefore, the liquid crystal equipment 200 concerned can be suitably used as a light valve for projectors.
[0087] Furthermore, in the gestalt of the above operation, it may replace with TFT30 and a switching element may consist of 2 terminal mold nonlinear devices, such as TFD (Thin Film Diode), etc. again. In this case, arrange one line to an opposite substrate among the data line and the scanning line, and it is made to function as a common electrode, and a switching element is arranged, respectively between the line of another side established in the TFT array substrate, and a pixel electrode, and a liquid crystal drive is carried out between. Thus, even if constituted, the effectiveness of preventing the diving to the picture signal and data signal of a clock noise of high frequency is demonstrated by shielding a pixel signal line and the data line from a clock signal line.
[0088] (Actuation of liquid crystal equipment) Next, actuation of the liquid crystal equipment 200 constituted as mentioned above is explained with reference to drawing 1 .
[0089] First, the scanning-line drive circuit 104 impresses a scan signal to the scanning line 31 by line sequential in pulse to predetermined timing.
[0090] If a parallel picture signal is received from six wiring VID1-VID6 in parallel to this, a sampling circuit 301 will sample these picture signals. The scanning-line drive circuit 104 supplies a sampling circuit driving signal for every data line about six wiring VID1 - VID6 each according to the timing which impresses gate voltage, and the data-line drive circuit 101 makes TFT302 of a sampling circuit 301 an ON state. Thereby, sequential impression of the data signal sampled by the sampling circuit 301 is carried out to the six adjoining data lines 35. That is, the parallel picture signals VID1-VID6 by which serial-parallel conversion was carried out are supplied to six phases inputted from wiring VID1-VID6 by the data-line drive circuit 101 and the sampling circuit 301 at the data line 35.
[0091] Thus, in TFT30 to which both the scan signal (gate voltage) and the data signal (source electrical potential difference) were impressed, an electrical potential difference is impressed to the pixel electrode 11 through the channel and the drain field 36 which were formed in the source field 34 and the semi-conductor layer 32. And as for the electrical potential difference of this pixel electrode 11, only time amount also with triple figures longer than the time amount to which the source electrical potential difference was impressed is held with storage capacitance (refer to drawing 7). With shielding wire 80 and 82, since especially the wiring VID1-VID6 is shielded from Wiring CLX and CLX', even when the frequency of a clock signal CLX is high, it can reduce the diving of the clock noise of the RF to Wiring CLX and the wiring VID1-VID6 from CLX' here.
[0092] As mentioned above, if an electrical potential difference is impressed to the pixel electrode 11,

the orientation condition of the liquid crystal in the part pinched by this pixel electrode 11 and common electrode 21 in the liquid crystal layer 50 changes, and if it is in no MARI White mode According to the impressed electrical potential difference, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from liquid crystal equipment 200 as a whole.
[0093] image quality deteriorates according to generating of the clock noise of a RF, using [the resolution of the image which should be displayed is high the above result, and] the clock signal CLX with a high frequency, and CLX' corresponding to this, also when the serial picture signals VID1-VID6 of a RF are inputted -- most -- or it is completely lost and high-definition image display is made possible.
[0094] (Electronic equipment) Next, the gestalt of operation of electronic equipment equipped with the liquid crystal equipment 200 explained to the detail above is explained with reference to drawing 13 from drawing 9 .
[0095] The outline configuration of the electronic equipment which equipped drawing 9 with liquid crystal equipment 200 in this way is shown first.
[0096] In drawing 9 , electronic equipment is constituted in preparation for the source 1000 of a display information output, the display information processing circuit 1002, the drive circuit 1004, liquid crystal equipment 200, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a TV signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a serial-parallel conversion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the drive circuit 1004 with a clock signal CLK. The drive circuit 1004 drives liquid crystal equipment 200. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes liquid crystal equipment 200, the drive circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.
[0097] Next, the example of the electronic equipment constituted in this way from drawing 10 by drawing 13 is shown, respectively.
[0098] In drawing 10 , an example slack liquid crystal projector 1100 of electronic equipment prepares three liquid crystal modules containing the liquid crystal equipment 200 with which the drive circuit 1004 mentioned above was carried on the TFT array substrate, and is constituted as a projector used as light valves 200R, 200G, and 200B for RGB, respectively. In a liquid crystal projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be led to the light valves 200R, 200G, and 200B corresponding to each color, respectively. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors modulated with light valves 200R, 200G, and 200B, respectively is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.
[0099] If the protection-from-light layer is especially prepared also in the TFT bottom as mentioned above in the gestalt of this operation The reflected light by the incident light study system in the liquid crystal projector based on the incident light from the liquid crystal equipment 200 concerned, A part of

incident light (a part of R light and G light) which runs through a dichroic prism 1112 after carrying out outgoing radiation from the reflected light from the front face of the TFT array substrate at the time of incident light passing and other liquid crystal equipments Even if it carries out incidence from a TFT array substrate side as a return light, protection from light to the channel of the TFT30 grade for pixel switching can fully be performed. In this case, in a configuration, since it becomes unnecessary to stick AR (Anti Reflection) film for return light prevention, or to perform AR coat processing between the TFT array substrate of each liquid crystal equipment and prism at a polarizing plate even if it uses the prism suitable for a miniaturization for an incident light study system, small and when being simplified, it is very advantageous.

[0100] In drawing 11 , other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic equipment (PC) are equipped with the body 1204 with which the keyboard 1202 was incorporated while it has liquid crystal equipment 200 mentioned above in the top covering case and they hold CPU, memory, a modem, etc. further.

[0101] In drawing 12 , the drive circuit 1004 of the above-mentioned [other example slack pagers 1300 of electronic equipment] in the metal frame 1302 is held in the light guide [in which the liquid crystal equipment 200 which is carried at a TFT array substrate top and forms a liquid crystal module contains back light 1306a] 1306, circuit board 1308, 1st, and 2nd shielding plates 1310 and 1312 or 2 elastic conductors 1314 and 1316, and a list with the tape carrier package tape 1318. In the case of this example, the above-mentioned display information processing circuit 1002 (refer to drawing 9) may be carried in the circuit board 1308, and may be carried on the TFT array substrate of liquid crystal equipment 200. Furthermore, it is also possible to carry the above-mentioned drive circuit 1004 on the circuit board 1308.

[0102] In addition, since the example shown in drawing 12 is a pager, the circuit board 1308 grade is prepared. However, it is also possible to carry out production, sale, use, etc. as back light-type liquid crystal equipment which incorporated [in the case of the drive circuit 1004 or the liquid crystal equipment 200 which carries the display information processing circuit 1002 further, and forms a liquid crystal module] the light guide 1306 by using as liquid crystal equipment what fixed liquid crystal equipment 200 in the metal frame 1302 in addition to this.

[0103] moreover, as shown in drawing 13 , in the case of the liquid crystal equipment 200 which carries neither the drive circuit 1004 nor the display information processing circuit 1002 To TCP (Tape Carrier Package)1320 mounted on the polyimide tape 1322, IC1324 including the drive circuit 1004 or the display information processing circuit 1002 It is also possible to connect physically and electrically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 1, and to carry out production, sale, use, etc. as liquid crystal equipment.

[0104] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 13 from drawing 10 above etc. is mentioned as an example of the electronic equipment shown in drawing 9 .

[0105] As explained above, according to the gestalt of this operation, generating of the clock noise of a RF is reduced and various kinds of electronic equipment equipped with the liquid crystal equipment 200 in which high-definition image display is possible can be realized.

[0106]

[Effect of the Invention] According to the electro-optic device according to claim 1, by the electric conduction line of the constant potential wired by the 1st substrate, since the picture signal line is shielded from the clock signal line, high-definition image display can be performed according to the picture signal of the high frequency for being able to reduce the diving of the clock noise of the RF from a clock signal line to a picture signal line, therefore displaying the image of high resolution.

[0107] Since simplification and space-saving-izing of a configuration can be attained by sharing the wiring itself and the external input terminal of an electric conduction line and a constant potential line

according to the electro-optic device according to claim 2, the electro-optic device which can perform high-definition image display by the comparatively simple configuration is realizable.
[0108] the configuration which shields a picture signal line from a clock signal line to a duplex according to the electro-optic device according to claim 3 -- generating of the clock noise of the RF in a picture signal or a data signal -- more -- powerful -- and dependability -- it can decrease highly.
[0109] Since the diving of the clock noise of the RF to a picture signal line can be further reduced by taking about a picture signal line and a clock signal line to the opposite sense to a data-line drive circuit according to the electro-optic device according to claim 4, the device on an easy configuration can raise the effectiveness of shielding efficiently.
[0110] Since the diving of the clock noise of the RF to a picture signal line can be reduced by separating predetermined spacing mutually and arranging the 1st and 2nd external input terminal mutually through the 3rd external input terminal in between according to the electro-optic device according to claim 5, the device on an easy configuration can raise the effectiveness of shielding efficiently.
[0111] According to the electro-optic device according to claim 6, since an image display field and two or more data lines can be shielded from a clock signal line, generating of the clock noise of a RF in the data signal on the data line etc. can be reduced, and more nearly high-definition image display becomes possible.
[0112] According to the electro-optic device according to claim 7, since the electric conduction line is formed in the bottom of the frame of a substrate, a deployment of the tooth space on a substrate can be aimed at.
[0113] According to the electro-optic device given in claims 8 and 9, by the comparatively simple production process, the high electric conduction line of a shielding effect can be formed, and the electro-optic device in which image display high-definition by low cost is possible can be realized.
[0114] Since the constant potential line and external input terminal for making a capacity line into constant potential can be made to serve a double purpose with other wiring or a terminal according to the electro-optic device according to claim 10, preventing the bad influence to the switching element and pixel electrode by potential fluctuation of a capacity line, high-definition image display becomes possible by the comparatively simple configuration.
[0115] According to electronic equipment according to claim 11, the clock noise of high frequency is reduced and it becomes realizable about various electronic equipment, such as the liquid crystal projector and personal computer in which high-definition image display is possible, and a pager.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] They are outline top views formed on the TFT array substrate in the gestalt of operation of liquid crystal equipment, such as various wiring and a circumference circuit.
[Drawing 2] It is the outline top view showing the two-dimensional layout of drawing 1 in a detail more.

[Drawing 3] It is the sectional view which met the A-A' line on the TFT array substrate of drawing 1 .
[Drawing 4] It is an expansion top view in image display field edges, such as a pixel electrode formed on the TFT array substrate of drawing 1 , the scanning line, and data.
[Drawing 5] It is the top view showing the whole liquid crystal equipment configuration of drawing 1 .
[Drawing 6] It is the sectional view showing the whole liquid crystal equipment configuration of drawing 1 .
[Drawing 7] It is the sectional view of TFT for pixel switching established in the image display field of the liquid crystal equipment of drawing 1 .
[Drawing 8] It is a sectional view in the shielding-wire part prepared in the frame field of the liquid crystal equipment of drawing 1 .
[Drawing 9] It is the block diagram showing the outline configuration of the gestalt of operation of the electronic equipment by this invention.
[Drawing 10] It is the sectional view showing the liquid crystal projector as an example of electronic equipment.
[Drawing 11] It is the front view showing the personal computer as other examples of electronic equipment.
[Drawing 12] It is the decomposition perspective view showing the pager as an example of electronic equipment.
[Drawing 13] It is the perspective view showing the liquid crystal equipment using TCP as an example of electronic equipment.
[Description of Notations]
1 -- TFT array substrate
2 -- Opposite substrate
11 -- Pixel electrode
12 -- Orientation film
21 -- Common electrode
22 -- Orientation film
23 -- Light-shielding film
30 -- TFT
31 -- Scanning line (gate electrode)
32 -- Semi-conductor layer
33 -- Gate insulating layer
34 -- Source field

35 -- Data line
36 -- Drain field
37 38 -- Contact hole
42 -- Insulating layer between the 1st layer
43 -- Insulating layer between the 2nd layer
50 -- Liquid crystal layer
52 -- Sealant
53 -- Frame
70 -- Storage capacitance
80 82 -- Shielding wire (constant potential line)
101 -- Data-line drive circuit
102 -- External input terminal
104 -- Scanning-line drive circuit
200 -- Liquid crystal equipment
301 -- Sampling circuit
302 -- TFT

[Translation done.]

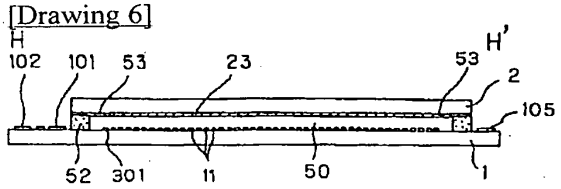
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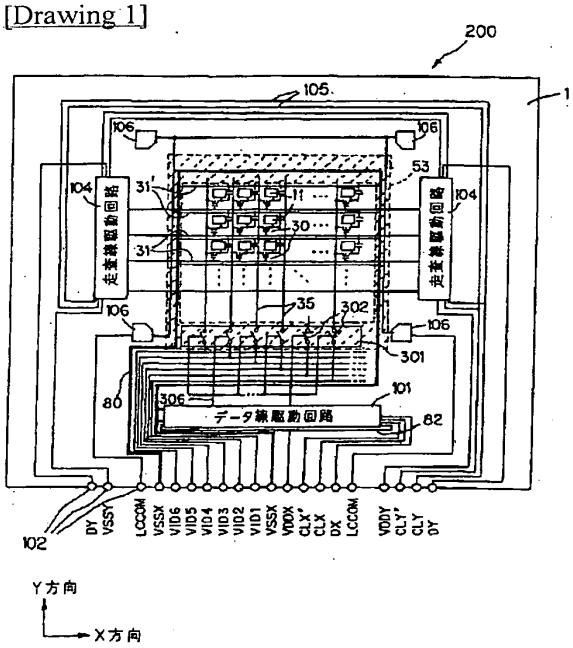
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DRAWINGS

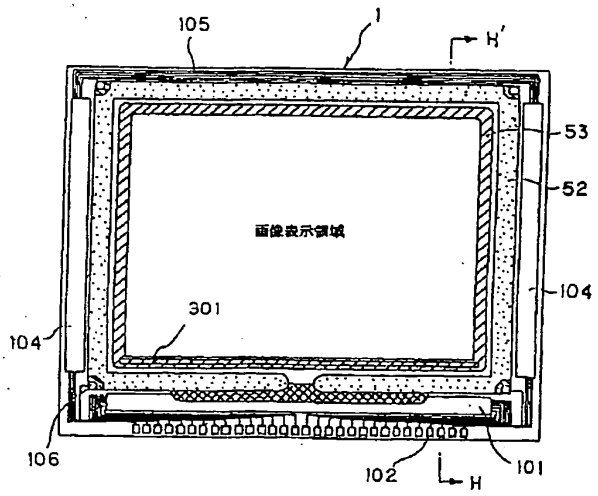
[Drawing 6]



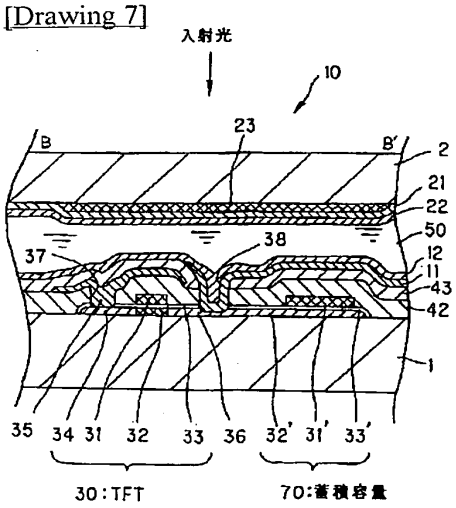
[Drawing 1]



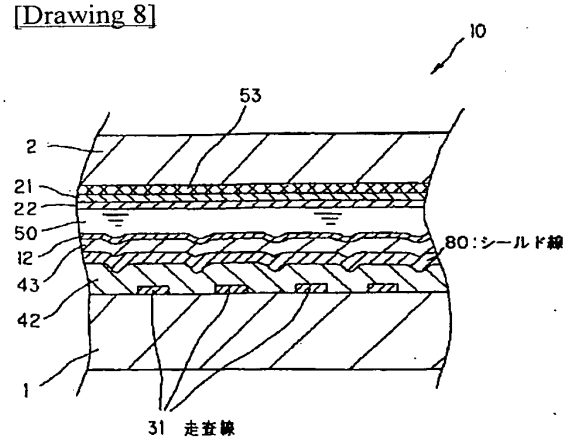
[Drawing 5]



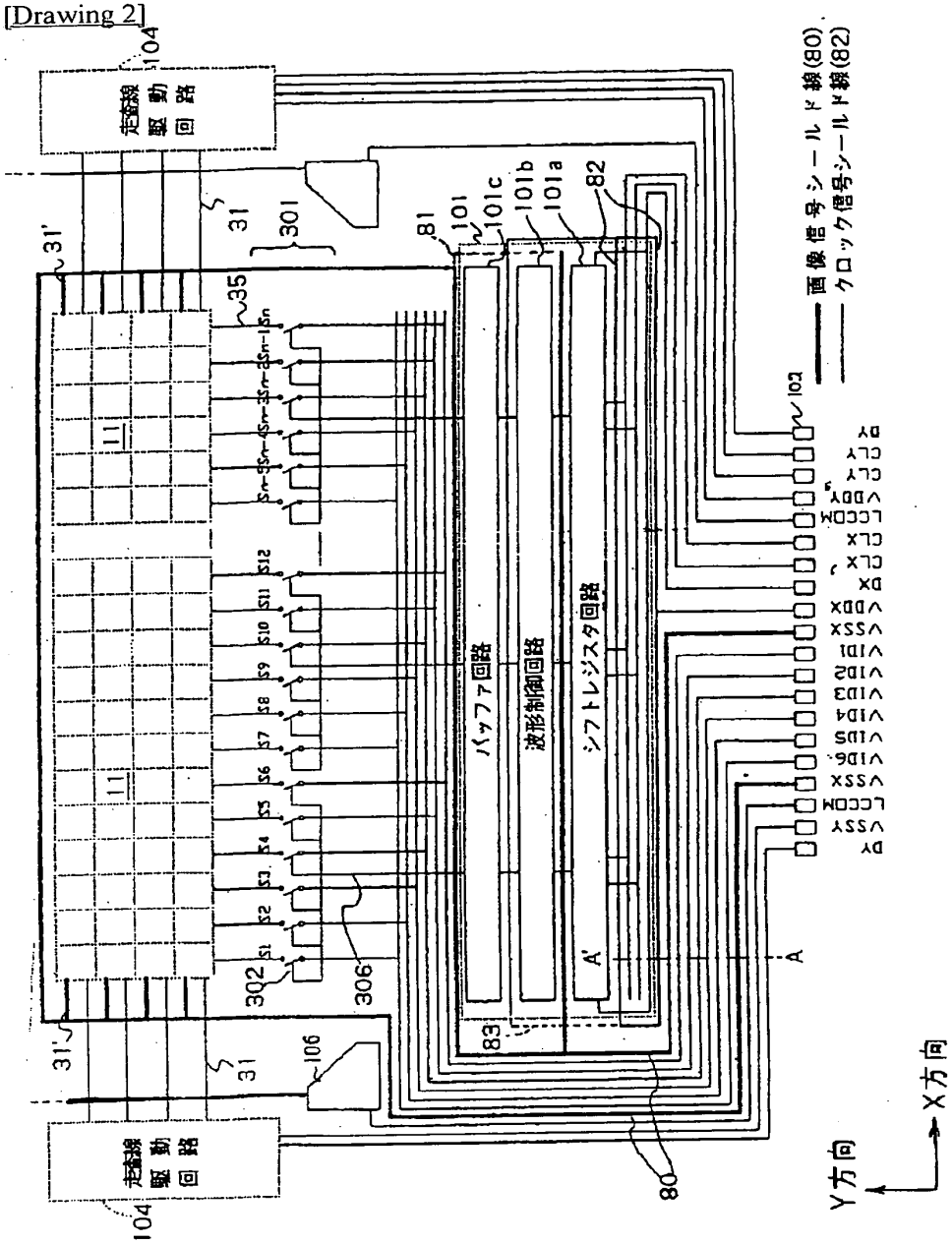
[Drawing 7]



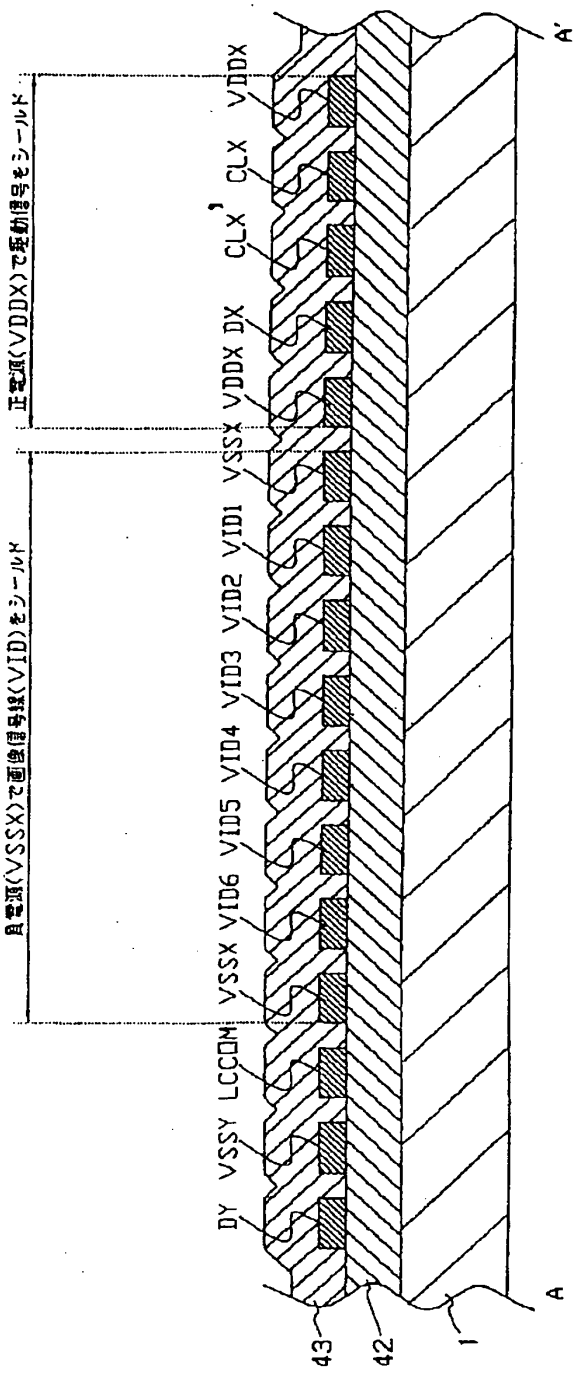
[Drawing 8]



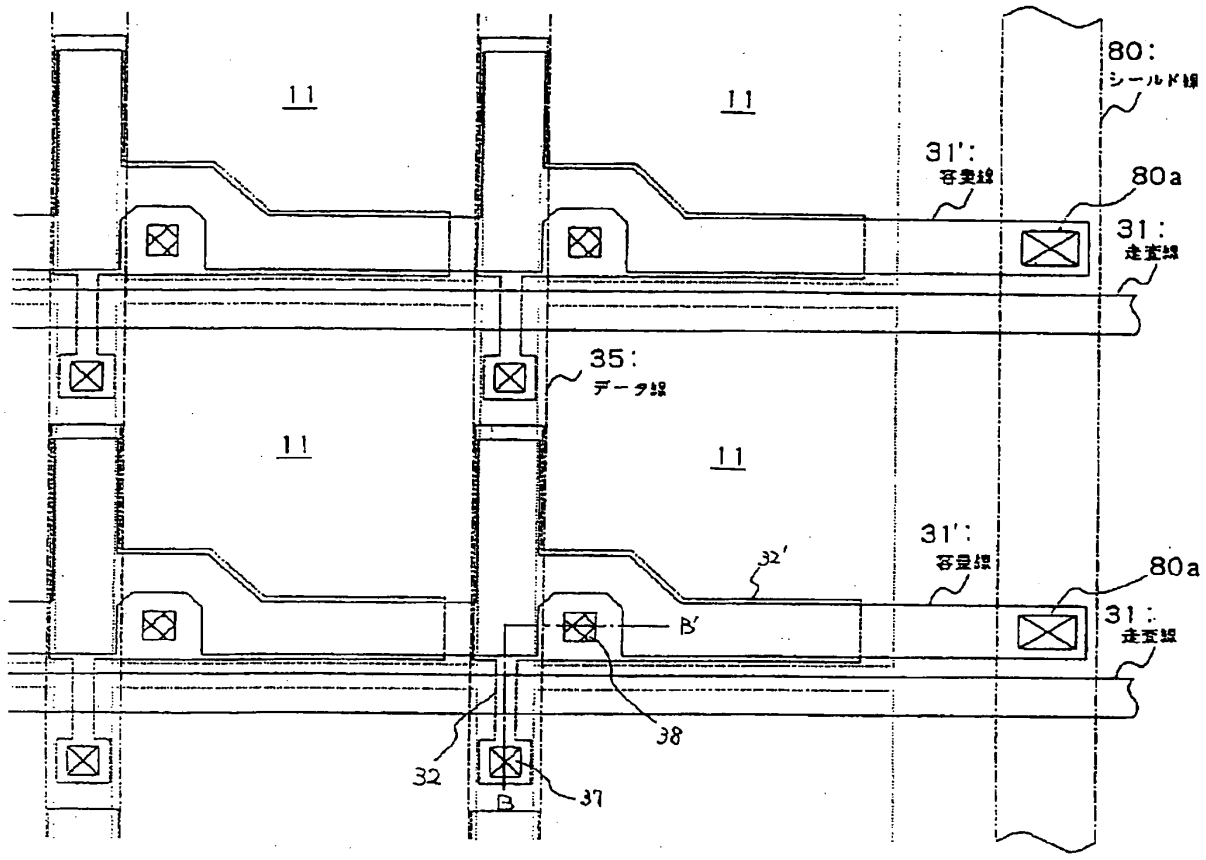
[Drawing 2]



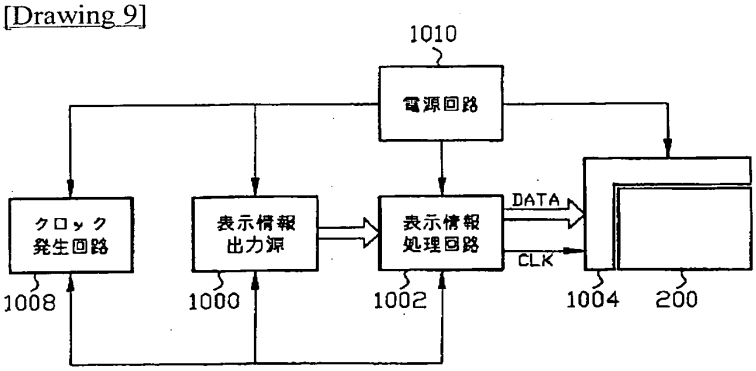
[Drawing 3]


正電源(VDDX)で駆動信号をシールド
負電源(VSSX)で画像信号線(VID)をシールド
A'
VDDX
CLX
CLX'
DX
VDDX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSX
LCCOM
VSSY
DY
A
43
42
1

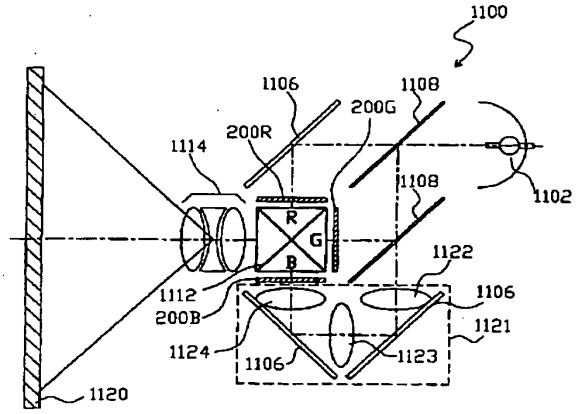
[Drawing 4]



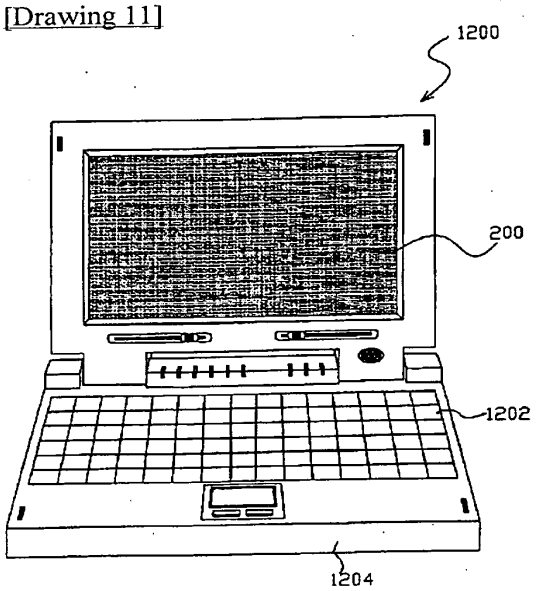
[Drawing 9]



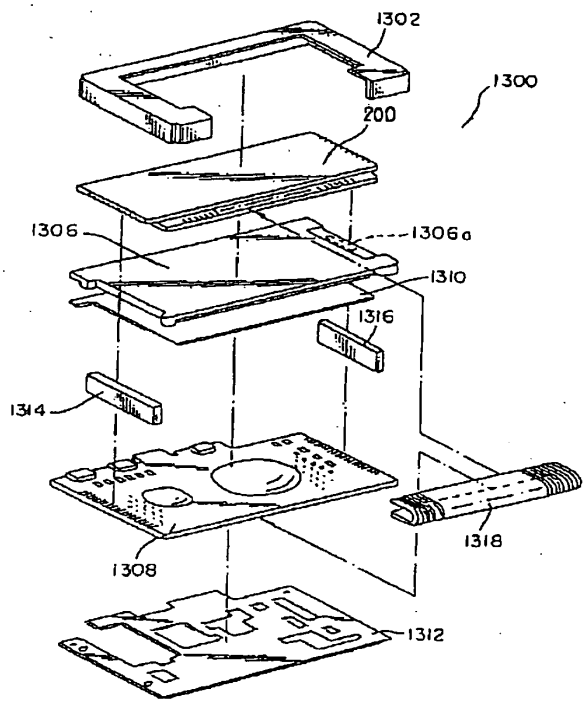
[Drawing 10]



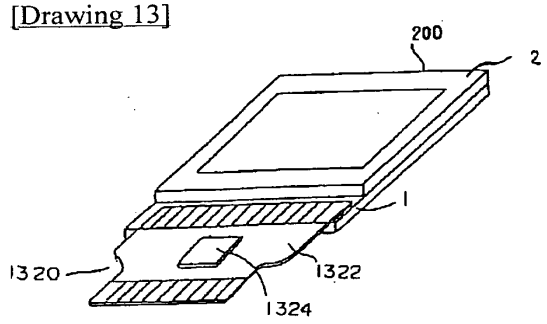
[Drawing 11]



[Drawing 12]



[Drawing 13]



[Translation done.]

PATENT ABSTRACTS OF JAPAN

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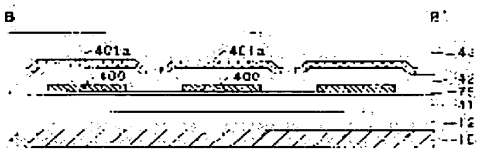
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G02F 1/1368
G09F 9/00
G09F 9/30
// G09G 3/20
G09G 3/36

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(71)Applicant : SEIKO EPSON CORP
(72)Inventor : MURAIDE MASAO

(54) ELECTROOPTICAL DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To display a high quality picture in an electrooptical device such as a liquid crystal device by reducing noise in signals on a signal line arranged on a peripheral region of a substrate with relatively simple construction of the device.
SOLUTION: The electrooptical device is provided with a pixel electrode (9a), a TFT(thin film transistor 30) connected thereto and a capacitive line (300) on a picture display region of a TFT array substrate (10) and further is provided with a data line (6a) and a scanning line (3a) connected to the TFT. In the peripheral region a peripheral circuit including a circuit related to data line driving, a signal line (400) connected thereto and composed of the same film as the capacitive line, and a shield (401a) electrically screening the line (400) from at least a direction and composed of the same film as the data line are provided.



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	1/1368		Ｇ０９Ｆ	9/00	３０９Ｚ	５Ｃ００６
Ｇ０９Ｆ	9/00	３０９			３４８Ｃ	５Ｃ０８０
		３４８		9/30	３３０Ｚ	５Ｃ０９４

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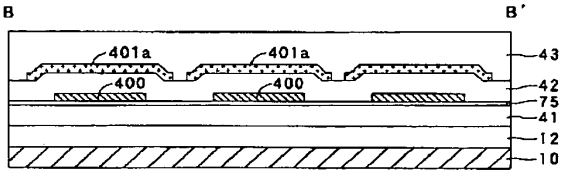
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最終頁に続く

(54)【発明の名称】　電気光学装置

(57)【要約】
【課題】　液晶装置等の電気光学装置において、比較的簡単な装置構成により、基板上の周辺領域に設けられた信号線上の信号におけるノイズを低減し、高品位の画像表示を行なう。
【解決手段】　電気光学装置は、ＴＦＴアレイ基板（１０）上の画像表示領域に、画素電極（９ａ）と、これに接続されたＴＦＴ（３０）及び容量線（３００）を備え、更にＴＦＴに接続されたデータ線（６ａ）及び走査線（３ａ）を備える。周辺領域に、データ線の駆動に係る回路を含む周辺回路と、これに接続されており容量線と同一膜からなる信号線（４００）と、これを少なくとも一方向から電気遮蔽するデータ線と同一膜からなるシールド（４０１ａ）を備える。



(2)

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【特許請求の範囲】

【請求項１】　基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導電膜からなる容量線と、該第１導電膜上に層間絶縁膜を介して積層された第２導電膜からなるデータ線とを備え、前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路と、該周辺回路に接続されており前記第１導電膜及び前記第２導電膜の一方からなる信号線と、該信号線を少なくとも一方向から電気遮蔽する前記第１導電膜及び前記第２導電膜の他方からなるシールドとを備えたことを特徴とする電気光学装置。

【請求項２】　前記シールドは、前記第２導電膜からなり、前記第１導電膜からなる前記信号線を上方から電気遮蔽することを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記シールドは、前記信号線を上方から電気遮蔽する本線部と該本線部から延設されて少なくとも前記層間絶縁膜に掘られた溝内に埋め込まれる側壁部分を更に有し、前記本線部及び前記側壁部分により前記信号線の断面上で見て前記信号線を三方から電気遮蔽することを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記シールドは、前記信号線の下方に他の層間絶縁膜を介して積層された他の導電膜からなる底壁部分を更に有し、前記本線部、前記側壁部分及び前記底壁部分により前記信号線を前記信号線の断面上で見て四方から電気遮蔽することを特徴とする請求項３に記載の電気光学装置。

【請求項５】　前記シールドは、前記第１導電膜からなり、前記第２導電膜からなる前記信号線を下方から電気遮蔽することを特徴とする請求項１に記載の電気光学装置。

【請求項６】　前記信号線は、画像信号を供給する画像信号線を含むことを特徴とする請求項１から５のいずれか一項に記載の電気光学装置。

【請求項７】　前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、

前記信号線は、前記画像信号を供給する画像信号線と前記サンプリング回路とを中継接続する中継配線を含むことを特徴とする請求項１から６のいずれか一項に記載の電気光学装置。

【請求項８】　前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、

前記信号線は、前記サンプリング回路のゲート信号線を含むことを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記信号線は、クロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線を含むことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。

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【請求項１０】　前記信号線は、画像信号を供給する画像信号線とクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線とを含み、

前記シールドは、前記画像信号線を電気遮蔽する第１部分と、前記制御信号線を電気遮蔽する第２部分とを含み、

前記第１部分は第１定電位に固定され且つ前記第２部分は前記第１定電位とは異なる第２定電位に固定されることを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記シールドは、１本の信号線毎に分断されていることを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項１２】　前記シールドは、複数の信号線毎に分断されていることを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項１３】　前記第１導電膜及び前記第２導電膜のうち少なくとも一方は、金属を含有する膜から形成されたことを特徴とする請求項１から１２のいずれか一項に記載の電気光学装置。

【請求項１４】　前記画像表示領域に、前記基板上において前記第１導電膜よりも下方に積層された第３導電膜からなる走査線を更に備え、

前記周辺領域に、前記信号線を下方から電気遮蔽する前記第３導電膜からなる他のシールドを更に備えたことを特徴とする請求項１から１３のいずれか一項に記載の電気光学装置。

【請求項１５】　前記画像表示領域に、前記データ線と前記画素電極との間に接続された薄膜トランジスタと、該薄膜トランジスタの少なくともチャネル領域を遮光する前記基板上において前記第１導電膜及び前記薄膜トランジスタよりも下方に積層された導電性の遮光膜とを更に備え、

前記周辺領域に、前記信号線を下方から電気遮蔽する前記遮光膜からなる他のシールドを更に備えたことを特徴とする請求項１から１４に記載の電気光学装置。

【請求項１６】　前記基板に電気光学物質を介して対向する対向基板上に、前記複数の画素電極に対向する対向電極を更に備えており、

前記シールドは、前記信号線のうち前記対向電極に対向する一部と前記対向電極との間において前記信号線の一部を上方から電気遮蔽する部分を含むことを特徴とする請求項１から１５のいずれか一項に記載の電気光学装置。

【請求項１７】　前記シールドは、電源配線の本線又は分岐配線からなることを特徴とする請求項１から１６のいずれか一項に記載の電気光学装置。

【請求項１８】　基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導

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電膜からなる容量線と、該第１導電膜上に層間絶縁膜を介して積層された第２導電膜からなるデータ線とを備え、

前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路と、該周辺回路に画像信号を供給すると共に前記第１導電膜及び前記第２導電膜の一方からなる画像信号線と、該周辺回路にクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給すると共に前記第１導電膜及び前記第２導電膜の他方からなる制御信号線とを備えたことを特徴とする電気光学装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、液晶装置等の電気光学装置の技術分野に属し、特に、ＴＦＴアレイ基板上の周辺領域に設けられたデータ線駆動回路、サンプリング回路等の周辺回路により画像信号、クロック信号等に応じてデータ線を駆動する形式の電気光学装置の技術分野に属する。

【０００２】

【背景技術】ＴＦＴ駆動によるアクティブマトリクス駆動方式の電気光学装置においては、縦横に夫々配列された多数の走査線及びデータ線並びにこれらの各交点に対応して多数の画素電極がＴＦＴアレイ基板上に設けられている。そして、これらに加えて、データ線駆動回路、サンプリング回路、走査線駆動回路等の周辺回路、更にこのような周辺回路に接続された画像信号線や制御信号線（例えば、クロック信号線や波形選択信号線）などの信号線が、係るＴＦＴアレイ基板上の周辺領域に設けられる場合がある。

【０００３】この場合、データ線駆動回路には、画像信号の供給タイミングの基準となる基準クロック（以下、Ｘ側基準クロックと称す）や所謂ゴーストの発生を防ぐための波形選択信号などの制御信号、表示すべき画像の内容に対応する画像信号、正や負の定電位電源等が、ＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して夫々供給される。他方、走査線駆動回路には、走査信号の供給タイミングの基準となる基準クロック（以下、Ｙ側基準クロックと称す）、正や負の定電位電源等が、やはりＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して供給される。そして例えば、走査線駆動回路により、Ｙ側基準クロックに基づくタイミングで走査信号を走査線に線順次で供給する。これに対応してデータ線駆動回路が、入力された画像信号をサンプリングするサンプリング回路を、Ｘ側基準クロックに基づくタイミングで順次駆動して、サンプリング回路から画像信号がデータ線に供給される。これらの結果、走査線にゲート接続された各ＴＦＴは、走査信号の供給に応じて導通状態とされ、画像信号がデータ線及び当該ＴＦＴを介して画素電極に供給されて各画素における画像表示が

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行われる。

【０００４】近年特に、表示画像の高解像度化に伴って、非常に高い周波数のシリアルな画像信号が入力されるようになってきている。例えば、画像信号のドット周波数は、近時の高解像度のパソコン画面において使用されるＸＧＡ表示モードでは約６５ＭＨｚであり、ＳＸＧＡ表示モードでは約１３５ＭＨｚであり、従来のＶＧＡ表示モードにおけるドット周波数（約３０ＭＨｚ）を遥かに上回る。これに対応すべく、特にデータ線駆動回路に供給されるＸ側基準クロックの周波数も非常に高くなる。更に、このように高い画像信号の周波数を、サンプリング回路でサンプリング可能な程度の周波数に落とすために、電気光学装置に入力される前段階で、高周波数のシリアルな画像信号を複数のパラレルな画像信号にシリアルーパラレル変換する処理が行われている。例えば、前述のＶＧＡ表示モードでは、６個程度のパラレルな画像信号への変換が行われており、ＸＧＡ表示モードやＳＸＧＡ表示モードでは、サンプリング回路の性能に応じて、例えば１２個或いは２４個程度のパラレルな画像信号への変換が必要となる。

【０００５】

【発明が解決しようとする課題】しかしながら、近年の表示画像の高品位化の要請の下では、このように基準クロックの周波数を高くすることによる、高周波のクロックノイズの発生が無視し得ないようになる。即ち、例えば従来の比較的周波数の低いＸ側基準クロックをデータ線駆動回路に供給してサンプリング回路を駆動する構成において、そのままクロック信号の周波数を上げたのでは、サンプリング回路に入力される画像信号中やサンプリング回路から出力される画像信号中に高周波のクロックノイズが発生して、データ線に供給すべき画像信号が変化してしまう。このように変化した画像信号の供給を受けたのでは、各画素電極により表示される画像もやはり変化してしまうという問題点がある。例えば、各画素において中間レベルの階調表示を行う時に、数ｍＶ～数十ｍＶ程度の微少なノイズが画像信号中に飛び込んだだけでも、表示画像中に視認可能な程度のノイズとして現れてしまう。これは、最高又は最低の液晶駆動電圧（例えば、０～５Ｖ間の電圧）に対応する白又は黒レベルの表示を行っている場合と比べて、中間レベルにおける液晶駆動電圧の変化に対する液晶の透過率の変化が急峻だからである。このように高精度の多階調表示を実現するためには、高周波のクロックノイズの問題は重大である。

【０００６】他方で、前述のようにシリアルーパラレル変換によるパラレルな画像信号の個数を増やすことによりサンプリング回路に供給される画像信号の周波数を下げることはできるが、電気光学装置の基板に設けねばならない画像信号入力用の外部入力端子の数や画像信号線の数は、このパラレルな画像信号の個数の増加に対応し

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て増やさねばならない。従って、限られた基板上の周辺領域に多数の信号線を極めて近接配置せねばならず、結果として、近接配置された一の信号線（例えば、クロック信号線）をノイズ源として他の信号線（例えば、画像信号線）上の信号中に飛び込むノイズが増大してしまうという問題点が生ずる。しかも、シリアルーパラレル変換によるパラレルな画像信号の個数を増やす程、画素電極への書き込み能力不足に起因して発生するブロックゴースト（即ち、パラレルな画像信号が供給される複数のデータ線に対応する画素電極群を一纏めとして発生するブロック状のゴースト）が画像表示領域内に占める面積が増加する。この結果、ブロックゴーストが視覚上目立つようになるという深刻な問題も生じる。

【０００７】本発明は上述の問題点に鑑みなされたものであり、基板上の周辺領域に設けられた信号線上の信号におけるノイズが低減されており、高品位の画像表示が可能な電気光学装置を提供することを課題とする。

【０００８】

【課題を解決するための手段】本発明の電気光学装置は上記課題を解決するために、基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導電膜からなる容量線と、該第１導電膜上に層間絶線膜を介して積層された第２導電膜からなるデータ線とを備え、前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路と、該周辺回路に接続されており前記第１導電膜及び前記第２導電膜の一方からなる信号線と、該信号線を少なくとも一方向から電気遮蔽する前記第１導電膜及び前記第２導電膜の他方からなるシールドとを備える。

【０００９】本発明の電気光学装置によれば、画像表示領域では、容量線をなす第１導電膜上に、データ線をなす第２導電膜が層間絶線膜を介して積層されている。周辺領域では、これら第１導電膜及び第２導電膜の一方から、周辺回路に接続された信号線が形成されており、これら第１導電膜及び第２導電膜の他方から、信号線を少なくとも一方向（例えば、上方や下方）から電気遮蔽するシールドが形成されている。従って、容量線をなす第１導電膜を利用して周辺領域における信号線を形成しつつ、データ線をなす第２導電膜を利用して係る信号線を電気遮蔽することにより、信号線上の信号への電磁ノイズの飛び込みを効果的に低減でき、又は信号線からの電磁ノイズの発生を効果的に低減できる。或いは、信号線をなす第２導電膜を利用して周辺領域における信号線を形成しつつ、容量線をなす第１導電膜を利用して係る信号線を電気遮蔽することにより、信号線上の信号への電磁ノイズの飛び込みを効果的に低減でき、又は信号線からの電磁ノイズの発生を効果的に低減できる。しかも、いずれの場合にも、周辺領域に信号線やシールドを形成するために専用の膜を別途形成しないで済むので、装置

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構成及び製造工程を簡略化する上でも有利である。特に、画像品位の向上のために画素ピッチを微細化し駆動周波数を高めた場合に、一般にこのような信号線に係るノイズは相対的に増加する。従って、本発明のように周辺領域に配線された画像信号線、制御信号線等の信号線を電気遮蔽する構成は、画素ピッチを微細化し或いは駆動周波数を高める上で大変有利である。

【００１０】尚、本発明における周辺回路のうち「データ線の駆動に係る回路」とは、例えばデータ線を駆動するデータ線駆動回路の他、データ線駆動回路からのサンプリング回路駆動信号による制御を受けて複数のデータ線に画像信号を所定のタイミングで印加するサンプリング回路、複数のデータ線に所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路等を含む、データ線の駆動或いはデータ線への画像信号の供給に関連する回路を全て含む広い意味である。また、「周辺回路」とは、このようなデータ線の駆動に係る回路以外に、例えば走査線の駆動に係る回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等の周辺領域に作りこまれる任意の回路をいう。

【００１１】以上の結果、比較的簡単な装置構成により、画像信号等におけるノイズが低減されており、高品位の画像表示が可能な電気光学装置を実現できる。

【００１２】本発明の電気光学装置の一態様では、前記シールドは、前記第２導電膜からなり、前記第１導電膜からなる前記信号線を上方から電気遮蔽する。

【００１３】この態様によれば、第１導電膜からなる画像信号線等の信号線は、第２導電膜からなるシールドにより上方から電気遮蔽される。従って、各信号線の主に上方や側方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを効果的に低減できる。

【００１４】この態様では、前記シールドは、前記信号線を上方から電気遮蔽する本線部と該本線部から延設されて少なくとも前記層間絶縁膜に掘られた溝内に埋め込まれる側壁部分を更に有し、前記本線部及び前記側壁部分により前記信号線の断面上で見て前記信号線を三方から電気遮蔽するように構成してもよい。

【００１５】このように構成すれば、第１導電膜からなる画像信号線等の信号線は、第２導電膜からなるシールドにより上方及び側方の三方から電気遮蔽される。従って、各信号線の主に上方や側方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを一層効果的に低減できる。

【００１６】この場合更に、前記シールドは、前記信号線の下方に他の層間絶線膜を介して積層された他の導電膜からなる底壁部分を更に有し、前記本線部、前記側壁部分及び前記底壁部分により前記信号線を前記信号線の断面上で見て四方から電気遮蔽するように構成してもよ

い。

【００１７】このように構成すれば、第１導電膜からなる画像信号線等の信号線は、第２導電膜及び他の導電膜からなるシールドにより上方、側方及び下方の四方から電気遮蔽される。従って、各信号線の四方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを非常に効果的に低減できる。

【００１８】本発明の電気光学装置の他の態様では、前記シールドは、前記第１導電膜からなり、前記第２導電膜からなる前記信号線を下方から電気遮蔽する。

【００１９】この態様によれば、第２導電膜からなる画像信号線等の信号線は、第１導電膜からなるシールドにより下方から電気遮蔽される。従って、各信号線の主に下方や側方に位置するノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを効果的に低減できる。

【００２０】本発明の電気光学装置の他の態様では、前記信号線は、画像信号を供給する画像信号線を含む。

【００２１】この態様によれば、周辺領域において、画像信号線は電気遮蔽されているので、ノイズ源としての他の信号線や配線或いは回路や素子からの画像信号線上の画像信号への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的に高いＳ／Ｎを持つ画像信号に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００２２】本発明の電気光学装置の他の態様では、前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、前記信号線は、前記画像信号を供給する画像信号線と前記サンプリング回路とを中継接続する中継配線を含む。

【００２３】この態様によれば、周辺領域において、中継配線はシールドされているので、ノイズ源としての他の信号線や配線或いは回路や素子からの中継配線上の画像信号への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的に高いＳ／Ｎを持つ画像信号に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。特に、対向基板に設けられる対向電極に対向する中継配線部分については、当該中継配線部分と対向電極との寄生容量を低減する観点から、両者間に配置される上方シールドにより電気遮蔽すると効果的である。

【００２４】本発明の電気光学装置の他の態様では、前記周辺回路は、画像信号をサンプリングするサンプリング回路を含み、前記信号線は、前記サンプリング回路のゲート信号線を含む。

【００２５】この態様によれば、周辺領域において、サンプリング回路のゲート信号線はシールドされているので、ノイズ源としての他の信号線や配線或いは回路や素子からのゲート信号線上の制御信号（例えば、データ線駆動回路から出力されるサンプリング回路駆動信号）への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的にサンプリング回路における高精度のサンプリング動作により、画像表示領域において高品位の画像表示を行うことが可能となる。特に、対向基板に設けられる対向電極に対向するゲート信号線部分については、当該ゲート信号線部分と対向電極との寄生容量を低減する観点から、両者間に配置される上方シールドにより電気遮蔽すると効果的である。

【００２６】本発明の電気光学装置の他の態様では、前記信号線は、クロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線を含む。

【００２７】この態様によれば、周辺領域において、制御信号線は電気遮蔽されているので、ノイズ源としての他の信号線や配線或いは回路や素子からの制御信号線上の制御信号への電磁ノイズの飛び込みを効果的に低減できる。更に、一般に高周波数や高電位である制御信号は画像信号に対するノイズ源となり易い。従って、このように制御信号線を電気遮蔽することにより、ノイズ源としての当該制御信号線からの、他の信号線たる画像信号線等に供給される画像信号等への電磁ノイズの飛び込みを効果的に低減できる。よって、最終的に高いＳ／Ｎを持つ制御信号や画像信号等に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００２８】尚、以上説明した本発明の電気光学装置（各実施形態を含む）では、シールドは、好ましくは接地電位や他の定電位に固定される。

【００２９】本発明の電気光学装置の他の態様では、前記信号線は、画像信号を供給する画像信号線とクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給する制御信号線とを含み、前記シールドは、前記画像信号線を電気遮蔽する第１部分と、前記制御信号線を電気遮蔽する第２部分とを含み、前記第１部分は第１定電位に固定され且つ前記第２部分は前記第１定電位とは異なる第２定電位に固定される。

【００３０】この態様によれば、周辺領域において、画像信号線はシールドの第１部分により電気遮蔽されており、制御信号線はシールドの第２部分により電気遮蔽されているので、ノイズ源としての他の信号線や配線或いは回路や素子からの、画像信号線上の画像信号及び制御信号線上の制御信号への電磁ノイズの飛び込みを夫々効果的に低減できる。そして特に、シールドの第１部分と第２部分とは、相異なる定電位に固定されているので、同一の定電位配線を介して両信号線間でそれらの電位変動が相互に影響を及ぼす事態を未然防止できる。従って、最終的に高いＳ／Ｎを持つ画像信号や制御信号等に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００３１】本発明の電気光学装置の他の態様では、前記シールドは、１本の信号線毎に分断されている。

【００３２】この態様によれば、信号線は、１本毎に別個に電気遮蔽されているので、各信号線を他の全ての信号線から電気遮蔽できる。即ち、複数の信号線相互間の電磁波による悪影響を極力低減できる。

【００３３】本発明の電気光学装置の他の態様では、前記シールドは、複数の信号線毎に分断されている。

【００３４】この態様によれば、信号線は、複数の信号線毎に別個に電気遮蔽されているので、１本の信号線毎にシールドを設ける場合と比較して、容易にシールドを形成できる。この際、例えば複数の画素信号線など、相互に電磁波が及ぼす影響が基本的に小さい複数の信号線を同一シールドにより纏めて電気遮蔽するようにし、他方で、例えば画像信号線とクロック信号線など、相互に電磁波が及ぼす影響が基本的に大きい信号線を相互に別個のシールドにより電気遮蔽するようにすれば、このように複数の信号線を纏めて電気遮蔽する際の不利益（即ち、同一シールドで電気遮蔽される複数の信号線相互間におけるノイズの飛び込み）を抑えることができる。

【００３５】本発明の電気光学装置の他の態様では、前記第１導電膜及び前記第２導電膜のうち少なくとも一方は、金属を含有する膜から形成される。

【００３６】この態様によれば、例えば、Ａｌ（アルミニウム）膜、Ｃｒ（クロム）等の金属を含有する膜から第１導電膜や第２導電膜を形成することにより、これらの導電膜の低抵抗化を容易に図ることができる。

【００３７】本発明の電気光学装置の他の態様では、前記画像表示領域に、前記基板上において前記第１導電膜よりも下方に積層された第３導電膜からなる走査線を更に備え、前記周辺領域に、前記信号線を下方から電気遮蔽する前記第３導電膜からなる他のシールドを更に備える。

【００３８】この態様によれば、画像表示領域では、走査線をなす第３導電膜が、容量線をなす第１導電膜よりも下方に積層されている。周辺領域では、この第３導電膜から、信号線を下方から電気遮蔽する他のシールドが形成されている。従って、第１導電膜及び第２導電膜の一方からなる画像信号線等の信号線は、第１導電膜及び第２導電膜の他方からなるシールドと、第３導電膜からなるシールドとにより上下から或いは下方から冗長的に電気遮蔽される。従って、ノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを一層効果的に低減できる。尚、画像表示領域では、走査線及びデータ線によるアクティブマトリクス駆動或いはパッシブマトリクス駆動が可能となる。

【００３９】本発明の電気光学装置の他の態様では、前記画像表示領域に、前記データ線と前記画素電極との間に接続された薄膜トランジスタと、該薄膜トランジスタの少なくともチャネル領域を遮光する前記基板上において前記第１導電膜及び前記薄膜トランジスタよりも下方に積層された導電性の遮光膜とを更に備え、前記周辺領域に、前記信号線を下方から電気遮蔽する前記遮光膜からなる他のシールドを更に備える。

【００４０】この態様によれば、画像表示領域では、薄膜トランジスタの少なくともチャネル領域を遮光する遮光膜が、容量線をなす第１導電膜よりも下方に積層されている。周辺領域では、この遮光膜から、信号線を下方から電気遮蔽する他のシールドが形成されている。従って、第１導電膜及び第２導電膜の一方からなる画像信号線等の信号線は、第１導電膜及び第２導電膜の他方からなるシールドと、遮光膜からなるシールドとにより上下から或いは下方から冗長的に電気遮蔽される。従って、ノイズ源としての他の信号線や配線或いは回路や素子からの電磁ノイズの飛び込みを一層効果的に低減できる。尚、画像表示領域では、データ線及び薄膜トランジスタによるアクティブマトリクス駆動が可能となる。

【００４１】本発明の電気光学装置の他の態様では、前記基板に電気光学物質を介して対向する対向基板上に、前記複数の画素電極に対向する対向電極を更に備えており、前記シールドは、前記信号線のうち前記対向電極に対向する一部と前記対向電極との間において前記信号線の一部を上方から電気遮蔽する部分を含む。

【００４２】この態様によれば、対向基板に設けられる対向電極とこれに対向する信号線の一部との間に上方シールドが存在するので、当該信号線の一部と対向電極との間における寄生容量を低減できる。即ち、ノイズ源としての対向電極からの信号線上の画像信号等への電磁ノイズの飛び込みや、ノイズ源としての信号線からの対向電極上の定電位信号（例えば、反転しない定電位の信号、フレームやフィールド毎に反転する定電位の信号など）等への電磁ノイズの飛び込みを効果的に低減できる。

【００４３】本発明の電気光学装置の他の態様では、前記シールドは、電源配線の本線又は分岐配線からなる。

【００４４】この態様によれば、シールドは、電源配線の本線又は分岐配線からなるので、シールドを定電位に固定できる。しかも、周辺領域におけるシールドが占める領域を電源配線に割り当てることになるので、電源配線を比較的容易に幅広に構成することができ、安定した定電位を供給することも可能となる。またシールドと電源配線とを共用することで、装置構成及び製造工程の簡略化を図ることも可能となる。更に、シールドをこのように安定した定電位に固定することにより、電気遮蔽の性能も向上するので一層有利である。

【００４５】本発明の他の電気光学装置は上記課題を解決するために、基板上の画像表示領域に、複数の画素電極と、該画素電極に蓄積容量を付加するための第１導電膜からなる容量線と、該第１導電膜上に層間絶縁膜を介して積層された第２導電膜からなるデータ線とを備え、前記基板上の前記画像表示領域の周辺に位置する周辺領域に、前記データ線の駆動に係る回路を含む周辺回路

と、該周辺回路に画像信号を供給すると共に前記第１導電膜及び前記第２導電膜の一方からなる画像信号線と、該周辺回路にクロック信号及び波形選択信号のうち少なくとも一方を含む制御信号を供給すると共に前記第１導電膜及び前記第２導電膜の他方からなる制御信号線とを備える。

【００４６】本発明の他の電気光学装置によれば、画像表示領域では、容量線をなす第１導電膜上に、データ線をなす第２導電膜が層間絶縁膜を介して積層されている。周辺領域では、これら第１導電膜及び第２導電膜の一方から、画像信号線が形成されており、これら第１導電膜及び第２導電膜の他方から、制御信号線が形成されている。従って、周辺領域において、同一導電膜をパターニングすることにより同一平面内に画像信号線と制御信号線とを形成する場合と比べると、画像信号線と制御信号線とを形成する二つの導電膜が基板に垂直な方向に離間した分だけ両者間における寄生容量は低減されたことになる。即ち、二つの信号線間の距離が大きくなるに連れて小さくなるノイズ源としての制御信号線からの画像信号線上の画像信号への電磁ノイズの飛び込み（或いはノイズ源としての画像信号線からの制御信号線上の制御信号への電磁ノイズの飛び込み）を低減できる。尚、このような構成を持つ電気光学装置に対して、上述した本発明に係る各種のシールドを設けてもよい。このように構成すれば、画送信号線と制御信号線とが基板に垂直な方向に離間したことによる電磁ノイズを低減する効果と、画像信号と制御信号線との間のシールドによる電磁ノイズを低減する効果との両者を享受できる。

【００４７】以上の結果、比較的簡単な装置構成により、画像信号等におけるノイズが低減されており、高品位の画像表示が可能な電気光学装置を実現できる。

【００４８】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにされる。

【００４９】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。以下の実施形態は、本発明の電気光学装置を液晶装置に適用したものである。

【００５０】先ず本発明の実施形態における電気光学装置の構成について、図１から図３を参照して説明する。図１は、電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。図２は、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。図３は、図２のＡ－Ａ’断面図である。尚、図３においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００５１】図１において、本実施形態における電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素には夫々、画素電極９ａと当該画素電極９ａをスイッチング制御するためのＴＦＴ３０とが形成されており、画像信号が供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されている。データ線６ａに書き込む画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給しても構わないし、相隣接する複数のデータ線６ａ同士に対して、グループ毎に供給するようにしても良い。また、ＴＦＴ３０のゲートに走査線３ａが電気的に接続されており、所定のタイミングで、走査線３ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。画素電極９ａを介して電気光学物質の一例としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板（後述する）に形成された対向電極（後述する）との間で一定期間保持される。液晶は、印加される電位レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能にする。ノーマリーホワイトモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が減少し、ノーマリーブラックモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が増加され、全体として電気光学装置からは画像信号に応じたコントラストを持つ光が出射する。ここで、保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極との間に形成される液晶容量と並列に蓄積容量７０を付加する。走査線３ａに並んで、蓄積容量７０の固定電位側容量電極を含むと共に定電位に固定された容量線３００が設けられている。

【００５２】図２において、電気光学装置のＴＦＴアレイ基板上には、マトリクス状に複数の透明な画素電極９ａ（点線部９ａ’により輪郭が示されている）が設けられており、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ及び走査線３ａが設けられている。

【００５３】また、半導体層１ａのうち図中右上がりの斜線領域で示したチャネル領域１ａ’に対向するように走査線３ａが配置されており、走査線３ａはゲート電極として機能する（特に、本実施形態では、走査線３ａは、当該ゲート電極となる部分において幅広に形成されている）。このように、走査線３ａとデータ線６ａとの交差する個所には夫々、チャネル領域１ａ’に走査線３ａがゲート電極として対向配置された画素スイッチング用のＴＦＴ３０が設けられている。

【００５４】図２及び図３に示すように、蓄積容量７０は、ＴＦＴ３０の高濃度ドレイン領域１ｅ（及び画素電極９ａ）に接続された画素電位側容量電極としての中継層７１と、固定電位側容量電極としての容量線３００の一部とが、誘電体膜７５を介して対向配置されることに

より形成されている。

【００５５】中継層７１は、蓄積容量７０の画素電位側容量電極としての機能の他、コンタクトホール８３及び８５を介して、画素電極９ａとＴＦＴ３０の高濃度ドレイン領域１ｅとを中継接続する中間導電層としての機能を持つ。

【００５６】容量線３００は平面的に見て、走査線３ａに沿ってストライプ状に伸びており、ＴＦＴ３０に重なる個所が図２中上下に突出している。このような容量線３００は好ましくは、膜厚５０ｎｍ程度の導電性のポリシリコン膜等からなる第１膜と、膜厚１５０ｎｍ程度の高融点金属を含む金属シリサイド膜等からなる第２膜とが積層された多層構造を持つように構成される。このように構成すれば、第２膜は、容量線３００或いは蓄積容量７０の固定電位側容量電極としての機能の他、ＴＦＴ３０の上側において入射光からＴＦＴ３０を遮光する遮光層としての機能を持つ。

【００５７】他方、ＴＦＴアレイ基板１０上におけるＴＦＴ３０の下側には、下側遮光膜１１ａが格子状に設けられている。下側遮光膜１１ａは、例えば、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）、Ｐｂ（鉛）等の高融点金属のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等からなる。

【００５８】そして、図２中縦方向に夫々伸びるデータ線６ａと図２中横方向に夫々伸びる容量線３００とが相交差して形成されること及び格子状に形成された下側遮光膜１１ａにより、ＴＦＴアレイ基板１０上におけるＴＦＴ３０の上側及び下側には夫々、平面的に見て格子状に遮光領域が構成されており、各画素の開口領域を規定している。

【００５９】また図３において、容量電極としての中継層７１と容量線３００との間に配置される誘電体膜７５は、例えば膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ膜、ＬＴＯ膜等の酸化シリコン膜、あるいは窒化シリコン膜等から構成される。蓄積容量７０を増大させる観点からは、膜の信頼性が十分に得られる限りにおいて、誘電体膜７５は薄い程良い。

【００６０】図２及び図３に示すように、データ線６ａは、コンタクトホール８１を介して、例えばポリシリコン膜からなる半導体層１ａのうち高濃度ソース領域１ｄに電気的に接続されている。尚、上述した中継層７１と同一膜からなる中継層を形成して、当該中継層及び２つのコンタクトホールを介してデータ線６ａと高濃度ソース領域１ｄとを電気的に接続してもよい。

【００６１】また容量線３００は、画素電極９ａが配置された画像表示領域からその周囲に延設され、定電位源と電気的に接続されて、固定電位とされる。このような定電位源としては、ＴＦＴ３０を駆動するための走査信号を走査線３ａに供給するための走査線駆動回路（後述する）や画像信号をデータ線６ａに供給するサンプリング回路を制御するデータ線駆動回路（後述する）に供給される正電源や負電源の定電位源でもよいし、対向基板２０の対向電極２１に供給される定電位でも構わない。更に、ＴＦＴ３０の下側に設けられる下側遮光膜１１ａについても、その電位変動がＴＦＴ３０に対して悪影響を及ぼすことを避けるために、容量線３００と同様に、画像表示領域からその周囲に延設して定電位源に接続するとよい。

【００６２】画素電極９ａは、中継層７１を中継することにより、コンタクトホール８３及び８５を介して半導体層１ａのうち高濃度ドレイン領域１ｅに電気的に接続されている。即ち、本実施形態では、中継層７１は、蓄積容量７０の画素電位側容量電極としての機能に加えて、画素電極９ａをＴＦＴ３０へ中継接続する機能を果たす。このように中継層７１は、層間距離が例えば１０００ｎｍ程度に長くても、両者間を一つのコンタクトホールで接続する技術的困難性を回避しつつ比較的小径の二つ以上の直列なコンタクトホールで両者間を良好に接続でき、画素開口率を高めることが可能となり、コンタクトホール開孔時におけるエッチングの突き抜け防止にも役立つ。

【００６３】図２及び図３において、電気光学装置は、ＴＦＴアレイ基板１０と、これに対向配置される透明な対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば石英基板、ガラス基板、シリコン基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。

【００６４】図３に示すように、ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９ａは例えば、ＩＴＯ（Indium Tin Oxide）膜などの透明導電性薄膜からなる。また配向膜１６は例えば、ポリイミド薄膜などの有機薄膜からなる。

【００６５】他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜２２は、ポリイミド薄膜などの有機薄膜からなる。

【００６６】対向基板２０には、格子状又はストライプ状の遮光膜を設けるようにしてもよい。このような構成を採ることで、前述の如く遮光領域を構成する容量線３００及びデータ線６ａと共に当該対向基板２０上の遮光膜により、対向基板２０側からの入射光がチャネル領域１ａ’や低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに侵入するのを、より確実に阻止できる。更に、このような対向基板２０上の遮光膜は、少なくとも入射光

が照射される面を高反射な膜で形成することにより、電気光学装置の温度上昇を防ぐ働きをする。

【００６７】このように構成された、画素電極９ａと対向電極２１とが対面するように配置されたＴＦＴアレイ基板１０と対向基板２０との間には、後述のシール材により囲まれた空間に電気光学物質の一例である液晶が封入され、液晶層５０が形成される。液晶層５０は、画素電極９ａと対向電極２１との間に電圧が生じていない状態で配向膜１６及び２２により所定の配向状態をとる。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、ＴＦＴアレイ基板１０及び対向基板２０をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのグラスファイバー或いはガラスビーズ等のギャップ材が混入されている。

【００６８】更に、画素スイッチング用のＴＦＴ３０下には、下地絶縁膜１２が設けられている。下地絶縁膜１２は、下側遮光膜１１ａからＴＦＴ３０を層間絶縁する機能の他、ＴＦＴアレイ基板１０の全面に形成されることにより、ＴＦＴアレイ基板１０の表面の研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用のＴＦＴ３０の特性の変化を防止する機能を有する。

【００６９】図３において、画素スイッチング用のＴＦＴ３０は、ＬＤＤ（Lightly DopedDrain）構造を有しており、走査線３ａ、当該走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ’、走査線３ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁薄膜２、半導体層１ａの低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ、半導体層１ａの高濃度ソース領域１ｄ並びに高濃度ドレイン領域１ｅを備えている。

【００７０】走査線３ａ上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８３が各々開孔された第１層間絶縁膜４１が形成されている。

【００７１】第１層間絶縁膜４１上には中継層７１及び容量線３００が形成されており、これらの上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び中継層７１へ通じるコンタクトホール８５が各々開孔された第２層間絶縁膜４２が形成されている。

【００７２】尚、本実施形態では、第１層間絶縁膜４１に対しては、１０００℃の焼成を行うことにより、半導体層１ａや走査線３ａを構成するポリシリコン膜に注入したイオンの活性化を図ってもよい。他方、第２層間絶縁膜４２に対しては、このような焼成を行わないことにより、容量線３００の界面付近に生じるストレスの緩和を図るようにしてもよい。

【００７３】第２層間絶縁膜４２上にはデータ線６ａが形成されており、これらの上には、中継層７１へ通じるコンタクトホール８５が形成された平坦化した第３層間絶縁膜４３が形成されている。画素電極９ａは、このように構成された第３層間絶縁膜４３の上面に設けられている。

【００７４】本実施形態では、第３層間絶縁膜４３の表面は、ＣＭＰ（Chemical Mechanical Polishing：化学的機械研磨）処理等により平坦化されており、その下方に存在する各種配線や素子による段差に起因する液晶層５０における液晶の配向不良を低減する。

【００７５】以上のように構成された本実施形態によれば、対向基板２０側からＴＦＴ３０のチャネル領域１ａ’及びその付近に入射光が入射しようとすると、データ線６ａ及び容量線３００からなる格子状の遮光層で遮光を行う。他方、ＴＦＴアレイ基板１０側から、ＴＦＴ３０のチャネル領域１ａ’及びその付近に戻り光が入射しようとすると、下側遮光膜１１ａで遮光を行う（特に、複板式のカラー表示用のプロジェクタ等で複数の電気光学装置をプリズム等を介して組み合わせて一つの光学系を構成する場合には、他の電気光学装置からプリズム等を突き抜けて来る投射光部分からなる戻り光は強力であるので、有効である。）。これらの結果、ＴＦＴ３０の特性が光リークにより変化することは殆ど無くなり、当該電気光学装置では、非常に高い耐光性が得られる。また、データ線６ａ及び走査線３ａが形成された各画素の非開口領域を利用して大きな蓄積容量７０を構築できる。

【００７６】次に、図４を参照して、本実施形態における周辺領域における配線及びシールドについて説明する。ここに、図４は、本実施形態におけるＴＦＴアレイ基板上に設けられたシールドを含む各種配線、周辺回路等の構成を示す図式的な平面図である。

【００７７】図５から図１０は夫々、シールド線、画像信号線及びクロック信号線等の配線の各種具体例を示す図４のＢ－Ｂ’断面図である。

【００７８】図４において、液晶装置のＴＦＴアレイ基板上における画像表示領域の周辺に位置する周辺領域には、周辺回路の一例として、データ線駆動回路１０１、走査線駆動回路１０４及びサンプリング回路３０１が形成されている。

【００７９】以下図４の説明において、ＴＦＴアレイ基板１の下辺に沿って複数設けられた外部入力端子１０２を介して入力される信号の配線４００は、説明の容易化のために信号名称と同一のアルファベット記号を配線４００の後に夫々括弧で付加して参照する（例えば、“クロック信号ＣＬＸ”の信号配線を“配線４００（ＣＬＸ）”と呼ぶ）ことにする。走査線駆動回路１０４は、外部制御回路から外部入力端子１０２並びに配線４００（ＶＳＳＹ）及び配線４００（ＶＤＤＹ）を介して供給される、走査線駆動回路１０４用の負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用いて、スタート信号ＳＰ

Ｙの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線４００（ＣＬＹ）及び配線４００（ＣＬＹ’）を介して供給される、走査線駆動回路１０４の内蔵シフトレジスタ回路用の基準クロック信号ＣＬＹ及びその反転クロック信号ＣＬＹ’に基づく所定タイミングで、走査線３ａに走査信号をパルス的に線順次で印加する。

【００８０】データ線駆動回路１０１は、外部制御回路から外部入力端子１０２並びに信号配線４００（ＶＳＳＸ）及び配線４００（ＶＤＤＸ）を介して供給される、データ線駆動回路１０１用の負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用いて、スタート信号ＳＰＸの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線４００（ＣＬＸ）及び配線４００（ＣＬＸ’）を介して供給される、データ線駆動回路１０１の内蔵シフトレジスタ回路用の基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＸ’に基づき、走査線駆動回路１０４が走査信号を印加するタイミングに合わせて、外部入力端子１０２及び配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）を介して供給される例えば１２個のパラレル信号にシリアル－パラレル変換された画像信号ＶＩＤ１～ＶＩＤ１２夫々について、データ線６ａ毎にサンプリング回路駆動信号Ｑｍ（ｍ＝１、２、…）をサンプリング回路３０１にサンプリング回路駆動信号線３０６を介して所定タイミングで供給する。

【００８１】サンプリング回路３０１は、ＴＦＴ３０２を各データ線６ａ毎に備えており、配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）が中継配線３０５を経由して、ＴＦＴ３０２のソース電極に接続されており、サンプリング回路駆動信号線３０６がＴＦＴ３０２のゲート電極に接続されている。そして、画像信号ＶＩＤ１～ＶＩＤ１２が入力されると、これらの画像信号をサンプリングする。また、サンプリング回路駆動信号線３０６を介して、データ線駆動回路１０１からサンプリング回路駆動信号Ｑｍが入力されると、画像信号ＶＩＤ１～ＶＩＤ１２夫々についてサンプリングされた画像信号を、１２本の隣接するデータ線６ａからなるグループ毎に順次印加する。

【００８２】以上のように、データ線駆動回路１０１とサンプリング回路３０１とは、１２個のパラレル信号に変換された画像信号ＶＩＤ１～ＶＩＤ１２をデータ線６ａに画像信号Ｓ１、Ｓ２、…として供給するように構成されている。本実施の形態では隣接する１２本のデータ線６ａに接続されるサンプリング回路３０１を同時に選択し、１２本のデータ線６ａからなるグループ毎に順次転送していく方式を述べたが、データ線６ａを６本毎に選択してもよいし、２４本毎に選択してもよい。或いは、２本以上の任意の本数を同時に選択してもよい。この際、少なくともパラレルな画像信号の個数だけ、画像信号用の外部入力端子１０２及び画像信号線が必要なことは言うまでもない。尚、パラレルな画像信号の個数とサンプリング回路３０１を同時に選択する数が相等しくなるように構成してもよいし、前者が後者よりも多くなるように構成してもよい。

【００８３】更に図４に示すように、データ線駆動回路１０１は、スタート信号ＳＰＸが入力されると、基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＫ’に基づく転送信号の順次生成を開始するシフトレジスタ回路１０１ａと、シフトレジスタ回路１０１ａからの転送信号を波形整形した後、サンプリング回路駆動信号線３０６を介してサンプリング回路３０１に供給する波形制御回路１０１ｂ及びバッファ回路１０１ｃとを備えている。また、サンプリング回路３０１は、１２個にシリアル－パラレル変換された画像信号ＶＩＤ１～ＶＩＤ１２に対応してＴＦＴ３０２が１２個ずつパラレルに各サンプリング回路駆動信号線３０６に接続されている。即ち、ＴＦＴ３０２から構成されるスイッチＳ１～Ｓ１２が左から１本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳ１３～Ｓ２４が左から２本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳｎ-11～Ｓｎが右端のサンプリング回路駆動信号線３０６に接続されている。

【００８４】制御信号の一つである波形選択信号としてのイネーブル信号ＥＮＢ１及びＥＮＢ２は、波形制御回路１０１ｂに入力される。この波形制御回路１０１ｂでは、シフトレジスタ回路１０１ａから順次出力されるパルスの幅を、イネーブル信号ＥＮＢ１及びＥＮＢ２のパルス幅に制限することにより、サンプリング回路３０１の選択期間を（相前後するサンプリング回路駆動信号Ｑ１、Ｑ２、…がハイレベルとなる期間が相互に重ならないように）制御する。これにより、同一の配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）から画像信号を受けるデータ線６ａ間におけるブロックゴーストの発生を防止する。従って、イネーブル信号ＥＮＢ１及びＥＮＢ２は、クロック信号ＣＬＸ及びＣＬＸ’と同じく、水平走査期間よりも短い周期を持つ高周波の制御信号である。

【００８５】尚、本実施形態では、画像表示領域の四隅には、ＴＦＴアレイ基板１と対向基板２０側の対向電極２１（図３参照）との間で電気的な導通をとるための上下導通端子１０６が設けられている（但し、図４では、そのうち２隅が図示されている）。上下導通端子１０６には、外部入力端子１０２並びに配線４００（ＬＣＣＯＭ）を介して供給される。

【００８６】次に、本実施形態の電気光学装置で採用可能なシールドの各種具体例を図５から図１０に夫々示す。ここに、図５から図１０は夫々、シールドの各種具体例の、図４のＢ－Ｂ’断面における構造を夫々示す断面図である。

【００８７】図５から図１０において、各具体例では夫々、画像信号線である配線４００（ＶＩＤ１）～配線４００（ＶＩＤ１２）は、画像表示領域における容量線３００と同一の導電膜（例えば、導電性のポリシリコン膜と導電性の金属シリサイド膜とを含む多層膜）から構成されており、これらの配線４００は少なくとも、画像表示領域におけるデータ線６ａと同一膜（例えば、Ａｌ膜）からなるシールドにより電気遮蔽されている。

【００８８】即ち、図５の具体例では、容量線３００と同一導電膜からなる配線４００は、その上方から各配線４００に沿って且つ各配線４００を覆う領域に形成されたデータ線６ａと同一導電膜からなる上方シールド４０１ａにより、電気遮蔽されている。特にこの具体例では、上方シールド４０１ａは、１本の配線４００毎に分断されているので、各配線４００を他の全ての配線４００から相互に電気遮蔽できる。

【００８９】図６の具体例では、容量線３００と同一導電膜からなる配線４００は、その上方から複数の配線４００に沿って且つ複数の配線４００を纏めて覆う領域に形成されたデータ線６ａと同一導電膜からなる上方シールド４０１ｂにより、電気遮蔽されている。特にこの具体例では、上方シールド４０１ｂは、複数の信号線毎に分断されている。従って、１本の信号線毎に上方シールド４０１ａを設ける図５の具体例の場合と比較して、比較的容易に上方シールド４０１ｂを形成できる。この際、複数の画素信号線など、相互に電磁波が及ぼす影響が基本的に小さい複数の信号線を一つの上方シールド４０１ｂにより纏めて電気遮蔽するようにし、他方で、例えば画像信号線とクロック信号線など、相互に電磁波が及ぼす影響が基本的に大きい信号線を相互に別個の上方シールド４０１ｂにより電気遮蔽するとよい。即ち、これにより、複数の信号線を纏めて電気遮蔽する際の不利益を最小限に抑えることができる。

【００９０】図７の具体例では、図５に示した上方シールド４０１ａに加えて、画像表示領域における下側遮光膜１１ａと同一導電膜からなる下方シールド１１ｂより、配線４００は上下方向から電気遮蔽されている。

【００９１】図８の具体例では、図５に示した上方シールド４０１ａに加えて、画像表示領域における走査線３ａと同一導電膜からなる下方シールド４０２より、配線４００は上下方向から電気遮蔽されている。

【００９２】図９の具体例では、図７と同様の上方シールド４０１ｃ及び下方シールド１１ｂに加えて、上方シールド４０１ｃと同一導電膜から延設されてなり、下地絶縁膜１２、第１層間絶縁膜４１、誘電体膜７５及び第２層間絶縁膜４２に配線４００に沿って溝状に掘られた穴に埋め込まれた側方シールド４０１ｄにより、配線４００は上下左右方向から電気遮蔽されている。特にこの具体例では、シールドは、１本の配線４００毎に全周を電気遮蔽しているので、複数の配線４００相互間の電磁波による悪影響を極力低減できる。

【００９３】図１０の具体例では、図８と同様の上方シールド４０１ｃ及び下方シールド４０２に加えて、上方シールド４０１ｃと同一導電膜から延設されてなり且つ第１層間絶縁膜４１、誘電体膜７５及び第２層間絶縁膜４２に配線４００に沿って溝状に掘られた穴に埋め込まれた側方シールド４０１ｅにより、配線４００は上下左右方向から電気遮蔽されている。特にこの具体例では、シールドは、１本の配線４００毎に全周を電気遮蔽しているので、複数の配線４００相互間の電磁波による悪影響を極力低減できる。以上説明したように本実施形態の電気光学装置によれば、画像表示領域では、容量線３００をなす第１導電膜上に、データ線６ａをなす第２導電膜が層間絶縁膜を介して積層されている。周辺領域では、これら第１導電膜及び第２導電膜の一方から、周辺回路に接続された配線４００が形成されており、これら第１導電膜及び第２導電膜の他方から、配線４００を少なくとも一方向（例えば、上方や下方）から電気遮蔽するシールドが形成されている。従って、画像信号線等の配線４００上の画像信号等への電磁ノイズの飛び込みを効果的に低減できる。しかも、周辺領域に配線４００やシールドを形成するために専用の膜を別途形成しないで済むので、装置構成及び製造工程を簡略化する上でも有利である。特に、画像品位の向上のために画素ピッチを微細化し駆動周波数を高めた場合に、一般にこのような信号線に係るノイズ（例えば、クロック信号線や波形選択信号線等の制御信号線から画像信号線上の画像信号への電磁ノイズ、外部装置や他の回路等からの画像信号線上の画像信号への電磁ノイズ、クロック信号線や波形選択信号線等の制御信号線から外部装置や他の回路等への電磁ノイズなど）は相対的に増加する（即ち、Ｓ／Ｎは低下する）。従って、本実施形態のように周辺領域に配線された画像信号線、制御信号線等の配線４００を、上方シールド４０１ａ、４０１ｂ又は４０１ｃ、下方シールド１１ｂ又は４０２、側方シールド４０１ｄ又は４０１ｅ等のシールドにより電気遮蔽する構成は、画素ピッチを微細化し或いは駆動周波数を高める上で大変有利である。

【００９４】また本実施形態では特に配線４００として画像信号線を電気遮蔽するので、ノイズ源としての他の信号線や配線或いは回路や素子からの画像信号線上の画像信号Ｓ１、Ｓ２、…への電磁ノイズの飛び込みを効果的に低減できる。従って、最終的に高いＳ／Ｎを持つ画像信号Ｓ１、Ｓ２、…に基づいて、画像表示領域において高品位の画像表示を行うことが可能となる。

【００９５】また以上説明した実施形態では、図４に示した画像信号線とサンプリング回路３０１とを中継接続する中継配線３０５やサンプリング回路駆動信号線３０６を、図５から図１０に示したように上方、下方或いは側方から電気遮蔽してもよい。このようにすれば、中継

配線３０５上の画像信号Ｓ１、Ｓ２、…への電磁ノイズの飛び込みや、サンプリング回路駆動信号線３０６上のサンプリング回路駆動信号Ｑ１、Ｑ２、…への電磁ノイズの飛込みを効果的に低減できる。これらの中継配線３０５やサンプリング回路駆動信号線３０６は、対向基板２０に設けられる対向電極２１に対向する部分を含むので、これらの配線と対向電極２１との寄生容量を低減する観点から、両者間に配置される上方シールドにより電気遮蔽すると特に効果的である。

【００９６】更に以上説明した実施形態では、クロック信号線としての配線４００（ＣＬＸ）、配線４００（ＣＬＸ’）や、波形選択信号線としての配線４００（ＥＮＢ１）、配線４００（ＥＮＢ２）を図５から図１０に示したように上方、下方或いは側方から電気遮蔽してもよい。このように構成すれば、これらの制御信号線上にあり、一般には画像信号に対するノイズ源となり易い高周波数で高電位である制御信号に起因する高周波で強力な電磁ノイズが、画像信号線等上の画像信号に飛び込むことを効果的に阻止できる。

【００９７】以上説明した本発明の電気光学装置（各実施形態を含む）では、シールドは、好ましくは接地電位や他の定電位に固定される。この際特に、画像信号線（配線４００（ＶＩＤ１）、配線４００（ＶＩＤ２）、…など）と制御信号線（配線４００（ＣＬＸ）、配線４００（ＣＬＸ’）、…など）とを別々に電気遮蔽すると共に相互に異なる定電位に固定するのがより好ましい。このように構成すれば、同一の定電位配線を介して両信号線間でそれらの電位変動が相互に影響を及ぼす事態を未然防止できる。例えば、画像信号線を低電位（接地電位或いは数ボルト程度）の第１定電位の定電位線に接続することにより低電位で電気遮蔽し、制御信号線を高電位（十数ボルト程度）の第２定電位の定電位線に接続することにより高電位で電気遮蔽すればよい。

【００９８】加えて本実施形態では、シールドと電源配線の本線又は分岐配線とを共用するのが好ましい。このように構成すれば、装置構成及び製造工程の簡略化を図りつつ、シールドを定電位に固定できる。しかも、周辺領域におけるシールドが占める領域を電源配線に割り当てることになるので、電源配線を比較的容易に幅広に構成することができる。更に、シールドを幅広に形成することにより、シールドの性能も向上するので一層有利である。

【００９９】また図５から図１０に示した各種具体例では、配線４００を容量線３００と同一導電膜から形成し且つシールドを容量線３００と異なる導電層から形成したが、配線４００をデータ線６ａと同一導電膜から形成し且つシールドをデータ線６ａと異なる導電層から形成してもよいし、配線４００を走査線３ａと同一導電膜から形成し且つシールドを走査線３ａと異なる導電層から形成してもよいし、配線４００を下側遮光膜１１ａと同一導電膜から形成し且つシールドを下側遮光膜１１ａと異なる導電層から形成してもよい。

【０１００】更に、シールドの一部を、配線と同一膜から形成することも可能であり、この場合には主に側方から電気遮蔽することが可能である。本実施形態では、図４に示したように、同一平面内で、負電源ＶＳＳＹを供給する配線４００（ＶＳＳＹ）及び負電源ＶＳＳＸを供給する配線４００（ＶＳＳＸ）は、画像信号線たる配線４００（ＶＩＤ２）、配線４００（ＶＩＤ４）、配線４００（ＶＩＤ６）、…を囲んでおり、画像信号シールド線として機能している。同様に同一平面内で、正電源ＶＤＤＹを供給する配線４００（ＶＤＤＹ）及び負電源ＶＳＳＸを供給する配線４００（ＶＳＳＸ）は、画像信号線たる配線４００（ＶＩＤ１）、配線４００（ＶＩＤ３）、配線４００（ＶＩＤ５）、…を囲んでおり、画像信号シールド線として機能している。更に、正電源ＶＤＤＸを供給する配線４００（ＶＤＤＸ）は、やはり同一平面内で、クロック信号線たる配線４００（ＣＬＸ）、配線４００（ＣＬＸ’）等の制御信号線を囲んでおり、制御信号シールド線として機能している。同様に正電源ＶＤＤＹを供給する配線４００（ＶＤＤＹ）は、やはり同一平面内で、クロック信号線たる配線４００（ＣＬＹ）、配線４００（ＣＬＹ’）等の制御信号を囲んでおり、制御信号シールド線として機能している。特に図４中で、破線で示したように、制御信号シールド線としての配線４００（ＶＤＤＸ）の２つの先端は、接続部９３により相互に接続されてもよいし、同様に画像信号シールド線としての配線４００（ＶＳＳＸ）の２つの先端は、接続部９１により相互に接続されてもよい。

【０１０１】更にまた、積層された２つの導電膜を共に低抵抗のＡｌ膜から構成することも可能であり、これにより、低抵抗の配線を低抵抗の導電膜で電気遮蔽することが可能となり、非常に電磁ノイズが飛び込み難い構成が得られる。

【０１０２】以上説明した実施形態では、図３に示したように多数の導電層を積層することにより、画素電極９ａの下地面（即ち、第３層間絶縁膜４３の表面）におけるデータ線６ａや走査線３ａに沿った領域に段差が生じるのを、第３層間絶縁膜４３の表面を平坦化することで緩和しているが、これに代えて或いは加えて、ＴＦＴアレイ基板１０、下地絶縁膜１２、第１層間絶縁膜４１、第２層間絶縁膜４２或いは第３層間絶縁膜４３に溝を掘って、データ線６ａ等の配線やＴＦＴ３０等を埋め込むことにより平坦化処理を行ってもよいし、第２層間絶縁膜４２の上面の段差をＣＭＰ（Chemical Mechanical Polishing）処理等で研磨することにより、或いは有機ＳＯＧを用いて平らに形成することにより、当該平坦化処理を行ってもよい。

【０１０３】尚、以上説明した実施形態では、画素スイッチング用ＴＦＴ３０は、好ましくは図３に示したよう

にＬＤＤ構造を持つが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物の打ち込みを行わないオフセット構造を持ってよいし、走査線３ａの一部からなるゲート電極をマスクとして高濃度で不純物を打ち込み、自己整合的に高濃度ソース及びドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。また本実施形態では、画素スイッチング用ＴＦＴ３０のゲート電極を高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。このようにデュアルゲート或いはトリプルゲート以上でＴＦＴを構成すれば、チャネルとソース及びドレイン領域との接合部のリーク電流を防止でき、オフ時の電流を低減することができる。

【０１０４】加えて、以上説明した本発明の実施形態の変形として、周辺領域で配線４００に対して、図５から図１０に示した如き各種シールドを設けるのに代えて又は加えて、容量線３００、データ線６ａ、走査線３ａ及び下側遮光膜１１ａの４つの導電膜のうちの一つから、制御信号線たる配線４００（ＣＬＸ）、配線４００（ＣＬＹ）、…を形成すると共に、これら４つの導電膜の他の一つから、画像信号線たる配線４００（ＶＩＤ１）、配線４００（ＶＩＤ２）、…を形成してもよい。このように構成すれば、同一導電膜をパターニングすることにより同一平面内にこれら２種類の配線を形成する場合と比べると、両信号線は基板に垂直な方向に離間し且つ両信号線間に層間絶縁膜が配置されている分だけ、両信号線間におけるノイズの飛び込みを低減できるので有利である。即ち、シールドがなくとも、このように基板に垂直な方向に離間するように、これら２種類の信号線を形成することにより、ノイズを低減することが可能となるのである。更に、このような構成と上述した各種シールドとを組み合わせることにより、電磁ノイズを低減する効果を一層高めることができる。

【０１０５】（電気光学装置の全体構成）以上のように構成された各実施形態における電気光学装置の全体構成を図１１及び図１２を参照して説明する。尚、図１１は、ＴＦＴアレイ基板１０をその上に形成された各構成要素と共に対向基板２０の側から見た平面図であり、図１２は、図１１のＨ－Ｈ’断面図である。

【０１０６】図１２において、ＴＦＴアレイ基板１０の上には、シール材５２がその縁に沿って設けられており、その内側に並行して、画像表示領域１０ａの周辺を規定する額縁としての遮光膜５３が設けられている。シール材５２の外側の領域には、データ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、走査線駆動回路１０４が、この一辺に隣接する２辺に沿って設けられている。走査線３ａに供給される走査信号遅延が問題にならないのならば、走査線駆動回路１０４は片側だけでも良いことは言うまでもない。また、データ線駆動回路１０１を画像表示領域１０ａの辺に沿って両側に配列してもよい。更にＴＦＴアレイ基板１０の残る一辺には、画像表示領域１０ａの両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられている。また、対向基板２０のコーナー部の少なくとも１箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的に導通をとるための上下導通材１０６が設けられている。また図４に示したサンプリング回路３０１が額縁領域に設けられている。そして、図１２に示すように、図１１に示したシール材５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材５２によりＴＦＴアレイ基板１０に固着されている。

【０１０７】尚、ＴＦＴアレイ基板１０上には、これらのデータ線駆動回路１０１、走査線駆動回路１０４、サンプリング回路３０１等に加えて、複数のデータ線６ａに所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等を形成してもよい。

【０１０８】以上図１から図１２を参照して説明した実施形態では、データ線駆動回路１０１及び走査線駆動回路１０４をＴＦＴアレイ基板１０の上に設ける代わりに、例えばＴＡＢ（Tape Automated bonding)基板上に実装された駆動用ＬＳＩに、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して電気的及び機械的に接続するようにしてもよい。また、対向基板２０の投射光が入射する側及びＴＦＴアレイ基板１０の出射光が出射する側には各々、例えば、ＴＮモード、ＶＡ（Vertically Aligned）モード、ＰＤＬＣ(Polymer Dispersed LiquidCrystal)モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【０１０９】以上説明した実施形態における電気光学装置は、プロジェクタに適用されるため、３枚の電気光学装置がＲＧＢ用のライトバルブとして各々用いられ、各ライトバルブには各々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が投射光として各々入射されることになる。従って、各実施形態では、対向基板２０に、カラーフィルタは設けられていない。しかしながら、画素電極９ａに対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２０上に形成してもよい。このようにすれば、プロジェクタ以外の直視型や反射型のカラー電気光学装置について、各実施形態における電気光学装置を適用できる。また、対向基板２０上に１画素１個対応するようにマイクロレンズを形成してもよい。あるいは、ＴＦＴアレイ基板１０上のＲＧＢに対向する画素電極９ａ下にカラーレジスト等でカラーフィルタ層を形成することも可能である。この

ようにすれば、入射光の集光効率を向上することで、明るい電気光学装置が実現できる。更にまた、対向基板２０上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー電気光学装置が実現できる。

【０１１０】本発明は、上述した実施形態に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨或いは思想に反しない範囲で適宜変更可能であり、そのような変更を伴なう電気光学装置及びその製造方法もまた本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【図１】本発明の実施形態の電気光学装置における画像表示領域を構成するマトリクス状の複数の画素に設けられた各種素子、配線等の等価回路である。

【図２】実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。

【図３】図２のＡ－Ａ’断面図である。

【図４】本実施形態におけるＴＦＴアレイ基板上に設けられたシールドを含む各種配線、周辺回路等の構成を示す図式的な平面図である。

【図５】本実施形態で採用可能なシールドの一具体例に係る図４のＢ－Ｂ’断面図である。

【図６】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図７】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図８】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図９】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

【図１０】本実施形態で採用可能なシールドの他の具体例に係る図４のＢ－Ｂ’断面図である。

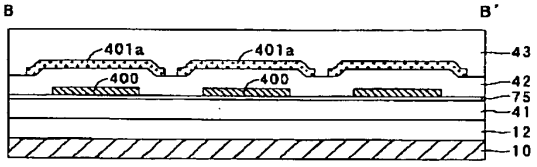
【図１１】実施形態の電気光学装置におけるＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図である。

【図１２】図１１のＨ－Ｈ’断面図である。

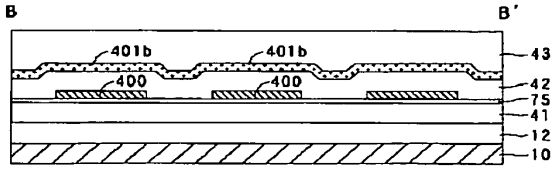
【符号の説明】

１ａ…半導体層
１ａ’…チャネル領域
１ｂ…低濃度ソース領域
１ｃ…低濃度ドレイン領域
１ｄ…高濃度ソース領域
１ｅ…高濃度ドレイン領域
２…絶縁薄膜
３ａ…走査線
６ａ…データ線
９ａ…画素電極
１０…ＴＦＴアレイ基板
１１ａ…下側遮光膜
１２…下地絶縁膜
１６…配向膜
２０…対向基板
２１…対向電極
２２…配向膜
３０…ＴＦＴ
５０…液晶層
７０…蓄積容量
７１…中継層
７５…誘電体膜
８１、８３、８５…コンタクトホール
１０１…データ線駆動回路
１０１ａ…シフトレジスタ回路
１０１ｂ…波形制御回路
１０１ｃ…バッファ回路
１０４…走査線駆動回路
３００…容量線
３０１…サンプリング回路
３０２…サンプリング回路のＴＦＴ
３０５…中継配線
３０６…サンプリング回路駆動信号線
４００…配線
４０１ａ、４０１ｂ、４０１ｃ…上方シールド
４０１ｄ、４０１ｅ…側方シールド
４０２…下方シールド

【図５】

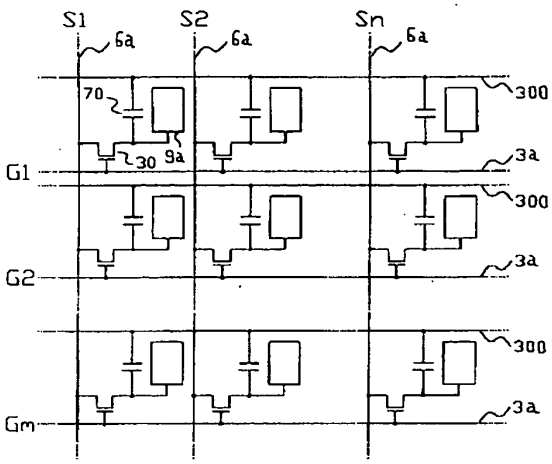


【図６】

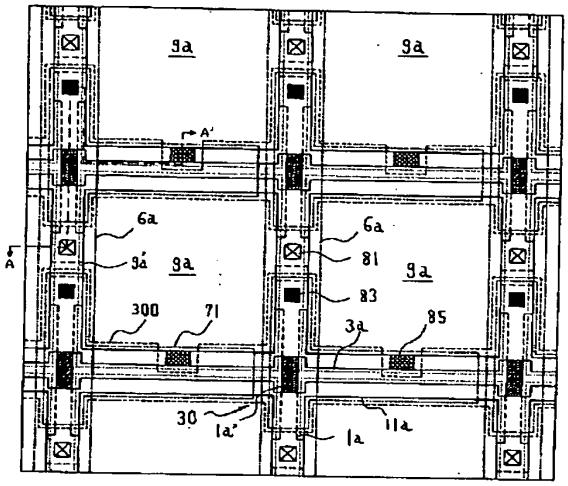


(15)

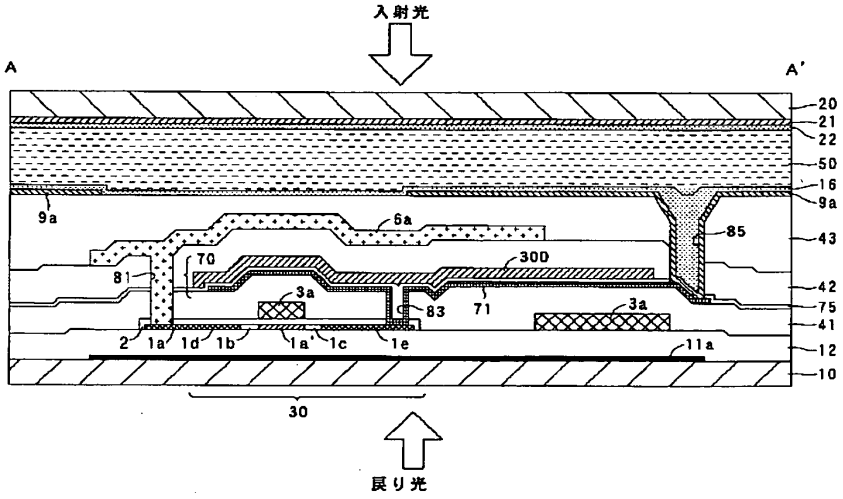
【図１】



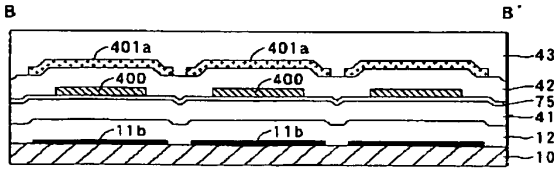
【図２】



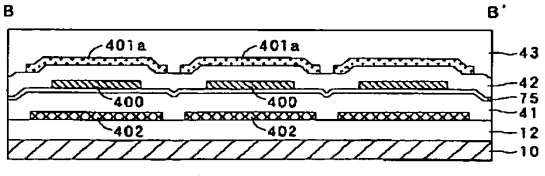
【図３】



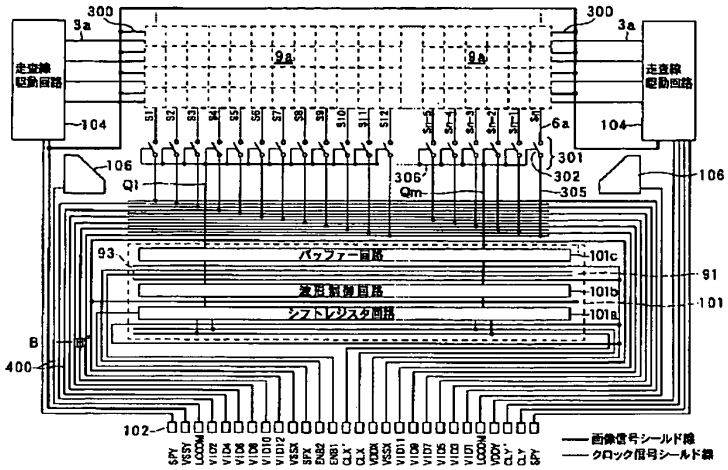
【図７】



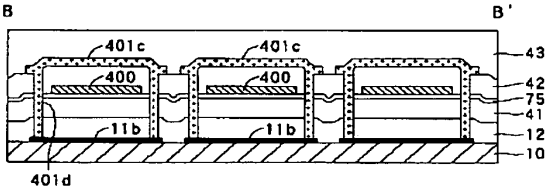
【図８】



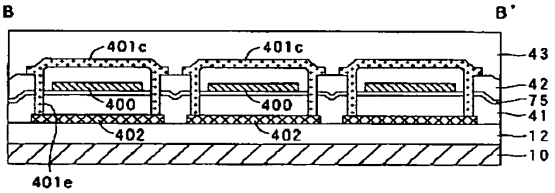
【図４】



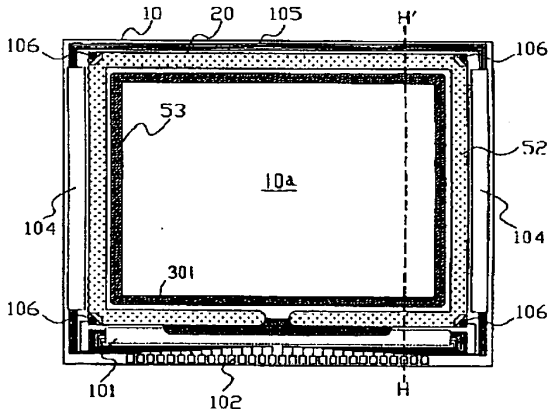
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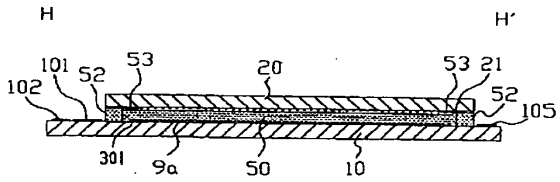
【図１０】



【図１１】



【図１２】



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JJ06
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HH14

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CLAIMS

[Claim(s)]
[Claim 1] The capacity line which becomes two or more pixel electrodes and these pixel electrodes from the 1st electric conduction film for adding storage capacitance to the image display field on a substrate, A circumference circuit including the circuit which starts the drive of said data line in the boundary region which is equipped with the data line which consists of the 2nd electric conduction film by which the laminating was carried out through ********** on this 1st electric conduction film, and is located around said image display field on said substrate, The electro-optic device characterized by having the signal line which is connected to this circumference circuit and consists of either said 1st electric conduction film or said 2nd electric conduction film, and shielding which consists of another side of said 1st electric conduction film which carries out electric screening of this signal line from an one direction at least, and said 2nd electric conduction film.
[Claim 2] Said shielding is an electro-optic device according to claim 1 characterized by carrying out electric screening of said signal line which consists of said 2nd electric conduction film, and consists of said 1st electric conduction film from the upper part.
[Claim 3] Said shielding is an electro-optic device according to claim 2 characterized by having further the side-attachment-wall part embedded at Mizouchi who was installed from the main track section and this main track section which carry out electric screening of said signal line from the upper part, and was dug in said interlayer insulation film at least, seeing on the cross section of said signal line by said main track section and said side-attachment-wall part, and carrying out electric screening of said signal line from Mikata.
[Claim 4] Said shielding is an electro-optic device according to claim 3 characterized by having further the bottom wall part which consists of other electric conduction film by which the laminating was caudad carried out through other ********** of said signal line, seeing said signal line on the cross section of said signal line by said main track section, said side-attachment-wall part, and said bottom wall part, and carrying out electric screening from a four way type.
[Claim 5] Said shielding is an electro-optic device according to claim 1 characterized by carrying out electric screening of said signal line which consists of said 1st electric conduction film, and consists of said 2nd electric conduction film from a lower part.
[Claim 6] Said signal line is an electro-optic device given in any 1 term of claims 1-5 characterized by including the picture signal line which supplies a picture signal.
[Claim 7] Said signal line is an electro-optic device given in any 1 term of claims 1-6 characterized by including junction wiring which carries out trunk connection of the picture signal line which supplies said picture signal, and said sampling circuit including the sampling circuit where said circumference circuit samples a picture signal.
[Claim 8] Said signal line is an electro-optic device given in any 1 term of claims 1-7 characterized by including the gate signal line of said sampling circuit including the sampling circuit where said circumference circuit samples a picture signal.
[Claim 9] Said signal line is an electro-optic device given in any 1 term of claims 1-8 characterized by

including the control signal line which supplies the control signal which contains at least one side among a clock signal and a wave-selection signal.
[Claim 10] Said signal line contains the control signal line which supplies the control signal which contains at least one side among the picture signal line which supplies a picture signal, a clock signal, and a wave-selection signal. Said shielding A part for a part for part I which carries out electric screening of said picture signal line, and part II which carries out electric screening of said control signal line is included. It is an electro-optic device given in any 1 term of claims 1-9 to which a part for said part I is fixed to potential the 1st law, and a part for said part II is characterized by said thing [being fixed to potential the 2nd law] from which potential differs the 1st law.
[Claim 11] Said shielding is an electro-optic device given in any 1 term of claims 1-10 characterized by being divided for every one signal line.
[Claim 12] Said shielding is an electro-optic device given in any 1 term of claims 1-10 characterized by being divided for two or more signal lines of every.
[Claim 13] It is an electro-optic device given in any 1 term of claims 1-12 characterized by forming at least one side from the film containing a metal among said 1st electric conduction film and said 2nd electric conduction film.
[Claim 14] An electro-optic device given in any 1 term of claims 1-13 characterized by having equipped said image display field with the scanning line which consists of the 3rd electric conduction film by which the laminating was carried out more nearly caudad than said 1st electric conduction film on said substrate further, and having further other shielding which consists of said 3rd electric conduction film which carries out electric screening of said signal line to said boundary region from a lower part.
[Claim 15] The thin film transistor connected to said image display field between said data lines and said pixel electrodes, It has further the conductive light-shielding film by which the laminating was carried out more nearly caudad than said 1st electric conduction film and said thin film transistor on said substrate of this thin film transistor which shades a channel field at least. An electro-optic device given in claims 1-14 characterized by equipping said boundary region with other shielding which consists of said light-shielding film which carries out electric screening of said signal line from a lower part further.

[Claim 16] It is an electro-optic device given in any 1 term of claims 1-15 which are further equipped with the counterelectrode which counters said two or more pixel electrodes on the opposite substrate which counters said substrate through electrooptic material, and are characterized by said shielding containing the part which carries out electric screening of said some of signal lines from the upper part between the part which counters said counterelectrode among said signal lines, and said counterelectrode.
[Claim 17] Said shielding is an electro-optic device given in any 1 term of claims 1-16 characterized by consisting of a main track of power-source wiring, or branching wiring.
[Claim 18] The capacity line which becomes two or more pixel electrodes and these pixel electrodes from the 1st electric conduction film for adding storage capacitance to the image display field on a substrate, A circumference circuit including the circuit which starts the drive of said data line in the boundary region which is equipped with the data line which consists of the 2nd electric conduction film by which the laminating was carried out through ********** on this 1st electric conduction film, and is located around said image display field on said substrate, The picture signal line which consists of either said 1st electric conduction film or said 2nd electric conduction film while supplying a picture signal to this circumference circuit, The electro-optic device characterized by having the control signal line which consists of another side of said 1st electric conduction film and said 2nd electric conduction film while supplying the control signal which contains at least one side among a clock signal and a wave-selection signal to this circumference circuit.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of electro-optic devices, such as liquid crystal equipment, and belongs to the technical field of the electro-optic device of a format which drives the data line according to a picture signal, a clock signal, etc. by circumference circuits especially established in the boundary region on a TFT array substrate, such as a data-line drive circuit and a sampling circuit.
[0002]
[Background of the Invention] In the electro-optic device of the active-matrix drive method by TFT drive, many pixel electrodes are prepared on the TFT array substrate at many the scanning lines and the data-line lists which were arranged in all directions, respectively corresponding to each of these intersections. And in addition to these, signal lines connected to circumference circuits, such as a data-line drive circuit, a sampling circuit, and a scanning-line drive circuit, and still such a circumference circuit, such as a picture signal line and a control signal line (for example, a clock signal line and a wave-selection signal line), may be prepared in the boundary region on the TFT array substrate to apply.

[0003] In this case, control signals, such as a wave-selection signal for preventing the so-called generating of the reference clock (the X side reference clock is called hereafter) used as the criteria of the supply timing of a picture signal or a ghost, the picture signal corresponding to the contents of the image which should be displayed, forward, a negative constant potential power source, etc. are supplied to a data-line drive circuit through the external input terminal and wiring which were prepared in the TFT array substrate, respectively. On the other hand, forward [used as the criteria of the supply timing of a scan signal / the reference clock (the Y side reference clock is called hereafter) and forward], a negative constant potential power source, etc. are supplied to a scanning-line drive circuit through the external input terminal and wiring which were too prepared in the TFT array substrate. And for example, a scan signal is supplied to the scanning line to the timing based on the Y side reference clock by the scanning-line drive circuit line sequential. Corresponding to this, a data-line drive circuit carries out the sequential drive of the sampling circuit which samples the inputted picture signal to the timing based on the X side reference clock, and a picture signal is supplied to the data line from a sampling circuit. These results, each TFT by which gate connection was made is made into switch-on at the scanning line according to supply of a scan signal, a picture signal is supplied to a pixel electrode through the data line and the TFT concerned, and image display in each pixel is performed.
[0004] A picture signal with a serial, very high frequency is increasingly inputted with high-resolution-izing of a display image especially in recent years. For example, with the XGA display mode used in the personal computer screen of the latest high resolution, the dot frequency of a picture signal is about 65MHz, with a SXGA display mode, is about 135MHz and easily exceeds the dot frequency (about 30MHz) in the conventional VGA display mode. The frequency of the X side reference clock supplied to especially a data-line drive circuit also becomes very high that it should correspond to this.

Furthermore, in order to drop the frequency of a picture signal high in this way on the frequency of extent which can be sampled in a sampling circuit, processing which carries out serial-parallel conversion of the picture signal with serial high frequency at two or more parallel picture signals is performed on the preceding paragraph story inputted into an electro-optic device. For example, conversion to about six parallel picture signals is performed, and conversion to 12 pieces or about 24 parallel picture signals is needed with an XGA display mode or a SXGA display mode with the above-mentioned VGA display mode, corresponding to the engine performance of a sampling circuit.
[0005]
[Problem(s) to be Solved by the Invention] However, under the request of high-definition-izing of a display image in recent years, generating of the clock noise of a RF by making the frequency of a reference clock high in this way cannot ignore now. That is, in the configuration which supplies the conventional X side reference clock with a comparatively low frequency to a data-line drive circuit, for example, and drives a sampling circuit, by having raised the frequency of a clock signal as it was, the clock noise of high frequency will occur in the picture signal outputted from the inside of the picture signal inputted into a sampling circuit, or a sampling circuit, and the picture signal which should be supplied at the data line will change. Thus, in having received supply of the picture signal which changed, there is a trouble displayed with each pixel electrode of carrying out image mist beam change. For example, when performing the gradation display of middle level in each pixel, it will also appear that the several mV - about dozens of mV very small noise jumped in into the picture signal as a noise of extent which can be checked by looking in a display image. This is because change of the permeability of the liquid crystal to change of the liquid crystal driver voltage in middle level is steep compared with the case where the display of the white corresponding to the highest or minimum liquid crystal driver voltage (for example, electrical potential difference between 0 - 5V) or black level is being performed. Thus, in order to realize a highly precise multi-gradation display, the problem of the clock noise of a RF is serious.
[0006] Although the frequency of the picture signal supplied to a sampling circuit by increasing the number of the parallel picture signal by serial-parallel conversion as mentioned above on the other hand can be lowered, the number of the external input terminals for a picture signal input and the number of picture signal lines which must be formed in the substrate of an electro-optic device must be increased corresponding to the increment in the number of this parallel picture signal. Therefore, contiguity arrangement of many signal lines must be carried out extremely in the boundary region on the limited substrate, and the trouble that the noise which jumps in as a result into the signal on other signal lines (for example, picture signal line) by making into a noise source the signal line (for example, clock signal line) of 1 by which contiguity arrangement was carried out will increase arises. And the area which the block ghost (namely, ghost of the letter of a block which generates as a bundle the pixel electrode group corresponding to two or more data lines with which a parallel picture signal is supplied) who originates insufficient [the write-in capacity to a pixel electrode], and is generated occupies in an image display field increases, so that the number of the parallel picture signal by serial-parallel conversion is increased. Consequently, the serious problem that a block ghost comes to be conspicuous on vision is also produced.
[0007] This invention is made in view of an above-mentioned trouble, and the noise in the signal on the signal line prepared in the boundary region on a substrate is reduced, and let it be a technical problem to offer the electro-optic device in which high-definition image display is possible.
[0008]
[Means for Solving the Problem] In order that the electro-optic device of this invention may solve the above-mentioned technical problem, to the image display field on a substrate Two or more pixel electrodes, The capacity line which consists of the 1st electric conduction film for adding storage capacitance to this pixel electrode, A circumference circuit including the circuit which starts the drive of said data line in the boundary region which is equipped with the data line which consists of the 2nd electric conduction film by which the laminating was carried out through ********** on this 1st electric conduction film, and is located around said image display field on said substrate, It has the

signal line which is connected to this circumference circuit and consists of either said 1st electric conduction film or said 2nd electric conduction film, and shielding which consists of another side of said 1st electric conduction film which carries out electric screening of this signal line from an one direction at least, and said 2nd electric conduction film.
[0009] According to the electro-optic device of this invention, in the image display field, the laminating of the 2nd electric conduction film which makes the data line is carried out through ********** on the 1st electric conduction film which makes a capacity line. In the boundary region, the signal line connected to the circumference circuit is formed from either these 1st electric conduction film or the 2nd electric conduction film, and shielding which carries out electric screening of the signal line from an one direction (for example, the upper part and a lower part) at least is formed from another side of these 1st electric conduction film and the 2nd electric conduction film. therefore, the thing done for the electric screening of the signal line applied using the 2nd electric conduction film which makes the data line, forming the signal line in a boundary region using the 1st electric conduction film which makes a capacity line -- the electromagnetism to the signal on a signal line -- the diving of a noise -- effective -- it can decrease -- or the electromagnetism from a signal line -- generating of a noise can be reduced effectively. or the thing done for the electric screening of the signal line applied using the 1st electric conduction film which makes a capacity line, forming the signal line in a boundary region using the 2nd electric conduction film which forms a signal line -- the electromagnetism to the signal on a signal line -- the diving of a noise -- effective -- it can decrease -- or the electromagnetism from a signal line -- generating of a noise can be reduced effectively. And in any case, since it is not necessary to form the film of dedication separately in order to form a signal line and shielding in a boundary region, it is advantageous also when simplifying an equipment configuration and a production process. When a pixel pitch is made detailed and drive frequency is especially raised for improvement in image grace, the noise which generally starts such a signal line increases relatively. Therefore, the configuration which carries out electric screening of the signal lines wired like this invention in the boundary region, such as a picture signal line and a control signal line, is very advantageous, when making a pixel pitch detailed or raising drive frequency.
[0010] Among the circumference circuits in this invention, in addition, with "the circuit concerning the drive of the data line" For example, the sampling circuit which impresses a picture signal to two or more data lines to predetermined timing in response to control by the sampling circuit driving signal from a data-line drive circuit besides [which drives the data line] a data-line drive circuit, It is large semantics including all the circuits relevant to supply of the picture signal to the drive of the data line or the data line including the precharge circuit which precedes the precharge signal of a predetermined voltage level with a picture signal, and supplies it to two or more data lines respectively. Moreover, the circuit of the arbitration made and crowded in boundary regions, such as an inspection circuit for inspecting the circuit concerning the drive of the scanning line, the quality of the electro-optic device concerned at the manufacture middle or the time of shipment, a defect, etc., in addition to the circuit which a "circumference circuit" requires for the drive of such the data line is said.
[0011] The above result, the noise in a picture signal etc. is reduced by the comparatively easy equipment configuration, and the electro-optic device in which high-definition image display is possible can be realized.
[0012] In one mode of the electro-optic device of this invention, said shielding carries out electric screening of said signal line which consists of said 2nd electric conduction film, and consists of said 1st electric conduction film from the upper part.
[0013] According to this mode, electric screening of the signal lines, such as a picture signal line which consists of the 1st electric conduction film, is carried out from the upper part with shielding which consists of the 2nd electric conduction film. therefore, the electromagnetism from other signal lines, wiring or circuits, and components as a noise source of each signal line mainly located in the upper part or the side -- the diving of a noise can be reduced effectively.
[0014] Said shielding has further the side-attachment-wall part embedded at Mizouchi who was installed from the main track section and this main track section which carry out electric screening of said signal

line from the upper part, and was dug in said interlayer insulation film at least, and it may constitute it from this mode so that it may see on the cross section of said signal line by said main track section and said side-attachment-wall part and electric screening of said signal line may be carried out from Mikata.
[0015] Thus, if constituted, electric screening of the signal lines, such as a picture signal line which consists of the 1st electric conduction film, will be carried out from Mikata, the upper part and the side, with shielding which consists of the 2nd electric conduction film. therefore, the electromagnetism from other signal lines, wiring or circuits, and components as a noise source of each signal line mainly located in the upper part or the side -- the diving of a noise can be reduced much more effectively.
[0016] In this case, further, said shielding has further the bottom wall part which consists of other electric conduction film by which the laminating was caudad carried out through other ********** of said signal line, and it may constitute it so that said signal line may be seen on the cross section of said signal line by said main track section, said side-attachment-wall part, and said bottom wall part and electric screening may be carried out from a four way type.
[0017] Thus, if constituted, electric screening of the signal lines, such as a picture signal line which consists of the 1st electric conduction film, will be carried out from the four way type of the upper part, the side, and a lower part with shielding which consists of the 2nd electric conduction film and other electric conduction film. therefore, the electromagnetism from other signal lines, wiring or circuits, and components as a noise source located in the four way type of each signal line -- the diving of a noise can be reduced very effectively.
[0018] In other modes of the electro-optic device of this invention, said shielding carries out electric screening of said signal line which consists of said 1st electric conduction film, and consists of said 2nd electric conduction film from a lower part.
[0019] According to this mode, electric screening of the signal lines, such as a picture signal line which consists of the 2nd electric conduction film, is carried out from a lower part with shielding which consists of the 1st electric conduction film. therefore, the electromagnetism from other signal lines, wiring or circuits, and components as a noise source located in a lower part or the side at the Lord of each signal line -- the diving of a noise can be reduced effectively.
[0020] In other modes of the electro-optic device of this invention, said signal line contains the picture signal line which supplies a picture signal.
[0021] this voice -- if it depends like, since electric screening of the picture signal line is carried out in the boundary region -- the electromagnetism to the picture signal on the picture signal line from other signal lines and wiring, or the circuit as a noise source, or a component -- the diving of a noise can be reduced effectively. Therefore, based on the picture signal which finally has high S/N, it becomes possible to perform high-definition image display in an image display field.
[0022] In other modes of the electro-optic device of this invention, said signal line includes junction wiring which carries out trunk connection of the picture signal line which supplies said picture signal, and said sampling circuit including the sampling circuit where said circumference circuit samples a picture signal.
[0023] this voice -- if it depends like, since junction wiring is shielded in the boundary region -- the electromagnetism to the picture signal on other signal lines and wiring as a noise source, or junction wiring from a circuit or a component -- the diving of a noise can be reduced effectively. Therefore, based on the picture signal which finally has high S/N, it becomes possible to perform high-definition image display in an image display field. About especially the junction wiring part that counters the counterelectrode prepared in an opposite substrate, if electric screening is carried out with upper part shielding arranged among both from a viewpoint which reduces the parasitic capacitance of the junction wiring part and a counterelectrode concerned, it is effective.
[0024] In other modes of the electro-optic device of this invention, said signal line contains the gate signal line of said sampling circuit including the sampling circuit where said circumference circuit samples a picture signal.
[0025] this voice -- if it depends like, since the gate signal line of a sampling circuit is shielded in the boundary region -- the electromagnetism to the control signal on the gate signal line from other signal

lines and wiring, or the circuit as a noise source, or a component (for example, sampling circuit driving signal outputted from a data-line drive circuit) -- the diving of a noise can be reduced effectively. Therefore, finally the highly precise sampling action in a sampling circuit enables it to perform high-definition image display in an image display field. About a part especially for the gate signal line part which counters the counterelectrode prepared in an opposite substrate, if electric screening is carried out with upper part shielding arranged among both from a viewpoint which reduces the parasitic capacitance of a part for the gate signal line part concerned, and a counterelectrode, it is effective.

[0026] In other modes of the electro-optic device of this invention, said signal line contains the control signal line which supplies the control signal which contains at least one side among a clock signal and a wave-selection signal.

[0027] this voice -- if it depends like, since electric screening of the control signal line is carried out in the boundary region -- the electromagnetism to the control signal on the control signal line from other signal lines and wiring, or the circuit as a noise source, or a component -- the diving of a noise can be reduced effectively. Furthermore, the control signal which are generally high frequency and high potential tends to serve as a noise source over a picture signal. therefore, the thing done for the electric screening of the control signal line in this way -- the others from the control signal line concerned as a noise source -- a signal line -- the electromagnetism to the picture signal supplied to a picture signal line etc. -- the diving of a noise can be reduced effectively. Therefore, based on a control signal, a picture signal, etc. which finally have high S/N, it becomes possible to perform high-definition image display in an image display field.

[0028] In addition, in the electro-optic device (each operation gestalt is included) of this invention explained above, shielding is preferably fixed to touch-down potential or other constant potentials.

[0029] In other modes of the electro-optic device of this invention, said signal line The control signal line which supplies the control signal which contains at least one side among the picture signal line which supplies a picture signal, a clock signal, and a wave-selection signal is included. Said shielding a part for said part I is fixed to potential the 1st law including a part for a part for part I which carries out electric screening of said picture signal line, and part II which carries out electric screening of said control signal line -- having -- a part for and said part II -- said -- it differs from potential the 1st law -- it is fixed to potential the 2nd law.

[0030] this voice -- if it depends like, since electric screening of the picture signal line is carried out by the amount of [of shielding] part I and electric screening of the control signal line is carried out by the amount of [of shielding] part II in the boundary region -- the electromagnetism to the picture signal on a picture signal line from other signal lines, wiring or circuits, and components as a noise source, and the control signal on a control signal line -- the diving of a noise can be reduced effectively, respectively. And since it is fixed to the constant potential which is different from each other, especially a part for a part for part I of shielding and part II can carry out before-it-happens prevention of the situation where those potential fluctuation does effect mutually among both signal lines through the same constant potential wiring. Therefore, based on a picture signal, a control signal, etc. which finally have high S/N, it becomes possible to perform high-definition image display in an image display field.

[0031] In other modes of the electro-optic device of this invention, said shielding is divided for every one signal line.

[0032] According to this mode, since electric screening of the signal line is separately carried out for [every], it can carry out electric screening of each signal line from all other signal lines. That is, the bad influence by two or more electromagnetic waves between signal lines can be reduced as much as possible.

[0033] In other modes of the electro-optic device of this invention, said shielding is divided for two or more signal lines of every.

[0034] According to this mode, since electric screening is separately carried out for two or more signal lines of every, a signal line can form shielding easily as compared with the case where shielding is prepared for every one signal line. Fundamentally, the effect which an electromagnetic wave does packs two or more small signal lines mutually with the same shielding, and is made to carry out electric

screening of in this case, for example, two or more pixel signal lines etc., to it. On the other hand For example, if the effect which an electromagnetic wave does mutually is made to carry out electric screening of the large signal line mutually with separate shielding fundamentally, a picture signal line, a clock signal line, etc. thus, the time of carrying out electric screening of two or more signal lines collectively -- being disadvantageous (namely, diving of the noise signal-line mutual [two or more] by which electric screening is carried out with the same shielding) -- it can stop.
[0035] In other modes of the electro-optic device of this invention, at least one side is formed from the film containing a metal among said 1st electric conduction film and said 2nd electric conduction film.
[0036] According to this mode, low resistance-ization of these electric conduction film can be easily attained by, for example, forming the 1st electric conduction film and the 2nd electric conduction film from the film containing metals, such as aluminum (aluminum) film and Cr (chromium).
[0037] In other modes of the electro-optic device of this invention, said image display field is further equipped with the scanning line which consists of the 3rd electric conduction film by which the laminating was carried out more nearly caudad than said 1st electric conduction film on said substrate, and it has further other shielding which consists of said 3rd electric conduction film which carries out electric screening of said signal line to said boundary region from a lower part.
[0038] According to this mode, in the image display field, the laminating of the 3rd electric conduction film which makes the scanning line is carried out more nearly caudad than the 1st electric conduction film which makes a capacity line. In the boundary region, other shielding which carries out electric screening of the signal line from a lower part is formed from this 3rd electric conduction film. Therefore, electric screening of the signal lines, such as a picture signal line which consists of either the 1st electric conduction film or the 2nd electric conduction film, is carried out in redundancy from a lower part from the upper and lower sides with shielding which consists of another side of the 1st electric conduction film and the 2nd electric conduction film, and shielding which consists of the 3rd electric conduction film. therefore, the electromagnetism from other signal lines, wiring or circuits, and components as a noise source -- the diving of a noise can be reduced much more effectively. In addition, in an image display field, the active-matrix drive or passive matrix drive by the scanning line and the data line is attained.
[0039] In other modes of the electro-optic device of this invention, it has further the conductive light-shielding film by which the laminating was carried out more nearly caudad than said 1st electric conduction film and said thin film transistor to said image display field on the thin film transistor connected between said data lines and said pixel electrodes, and said substrate of this thin film transistor which shades a channel field at least, and has further other shielding which consists of said light-shielding film which carries out electric screening of said signal line to said boundary region from a lower part.
[0040] According to this mode, in the image display field, the laminating of the light-shielding film of a thin film transistor which shades a channel field at least is carried out more nearly caudad than the 1st electric conduction film which makes a capacity line. In the boundary region, other shielding which carries out electric screening of the signal line from a lower part is formed from this light-shielding film. Therefore, electric screening of the signal lines, such as a picture signal line which consists of either the 1st electric conduction film or the 2nd electric conduction film, is carried out in redundancy from a lower part from the upper and lower sides with shielding which consists of another side of the 1st electric conduction film and the 2nd electric conduction film, and shielding which consists of a light-shielding film. therefore, the electromagnetism from other signal lines, wiring or circuits, and components as a noise source -- the diving of a noise can be reduced much more effectively. In addition, in an image display field, the active-matrix drive by the data line and the thin film transistor is attained.
[0041] In other modes of the electro-optic device of this invention, it has further the counterelectrode which counters said two or more pixel electrodes on the opposite substrate which counters said substrate through electrooptic material, and said shielding contains the part which carries out electric screening of said some of signal lines from the upper part between the part which counters said counterelectrode among said signal lines, and said counterelectrode.

[0042] Since upper part shielding exists between [some] the counterelectrode prepared in an opposite substrate, and the signal line which counters this according to this mode, the parasitic capacitance between some of signal lines concerned and a counterelectrode can be reduced. namely, the electromagnetism to the picture signal on the signal line from the counterelectrode as a noise source etc. -- the electromagnetism to the diving of a noise, the constant potential signals on the counterelectrode from the signal line as a noise source (for example, the signal of the constant potential which is not reversed, the signal of the constant potential reversed for every frame or field, etc.), etc. -- the diving of a noise can be reduced effectively.
[0043] Said shielding consists of a main track of power-source wiring, or branching wiring in other modes of the electro-optic device of this invention.
[0044] According to this mode, since shielding consists of a main track of power-source wiring, or branching wiring, it can fix shielding to constant potential. And since the field which shielding in a boundary region occupies will be assigned to power-source wiring, power-source wiring can be constituted broadly comparatively easily, and it also becomes possible to supply the stable constant potential. Moreover, by sharing shielding and power-source wiring, it also becomes possible to attain simplification of an equipment configuration and a production process. Furthermore, by fixing shielding to the constant potential stabilized in this way, since the engine performance of electric screening also improves, it is much more advantageous.
[0045] In order that other electro-optic devices of this invention may solve the above-mentioned technical problem, to the image display field on a substrate Two or more pixel electrodes, The capacity line which consists of the 1st electric conduction film for adding storage capacitance to this pixel electrode, A circumference circuit including the circuit which starts the drive of said data line in the boundary region which is equipped with the data line which consists of the 2nd electric conduction film by which the laminating was carried out through ********** on this 1st electric conduction film, and is located around said image display field on said substrate, The picture signal line which consists of either said 1st electric conduction film or said 2nd electric conduction film while supplying a picture signal to this circumference circuit, While supplying the control signal which contains at least one side among a clock signal and a wave-selection signal to this circumference circuit, it has the control signal line which consists of another side of said 1st electric conduction film and said 2nd electric conduction film.
[0046] According to other electro-optic devices of this invention, in the image display field, the laminating of the 2nd electric conduction film which makes the data line is carried out through ********** on the 1st electric conduction film which makes a capacity line. In the boundary region, the picture signal line is formed from either these 1st electric conduction film or the 2nd electric conduction film, and the control signal line is formed from another side of these 1st electric conduction film and the 2nd electric conduction film. Therefore, it means that the parasitic capacitance [part / to have estranged in the direction where two electric conduction film which forms a picture signal line and a control signal line compared with the case where a picture signal line and a control signal line are formed in the same flat surface is perpendicular to a substrate] between both was reduced by carrying out patterning of the same electric conduction film in the boundary region. namely, the electromagnetism to the picture signal on the picture signal line from the control signal line as a noise source by which the distance between two signal lines takes for becoming large, and becomes small -- the diving (or electromagnetism to the control signal on the control signal line from the picture signal line as a noise source diving of a noise) of a noise can be reduced. In addition, various kinds of shielding concerning this invention mentioned above may be prepared to an electro-optic device with such a configuration. thus, the electromagnetism by having estranged in the direction where drawing transmitting **** and a control signal line are perpendicular to a substrate, when constituted -- electromagnetism with shielding between the effectiveness of reducing a noise, and a picture signal and a control signal line -- both with the effectiveness of reducing a noise are enjoyable.
[0047] The above result, the noise in a picture signal etc. is reduced by the comparatively easy equipment configuration, and the electro-optic device in which high-definition image display is possible can be realized.

[0048] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.
[0049]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing. The following operation gestalten apply the electro-optic device of this invention to liquid crystal equipment.
[0050] The configuration of the electro-optic device in the operation gestalt of this invention is first explained with reference to drawing 3 from drawing 1 . Drawing 1 is equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of an electro-optic device] a matrix, and wiring. Drawing 2 is a top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other. Drawing 3 is the A-A' sectional view of drawing 2 . In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 3 .
[0051] In drawing 1 , TFT30 for carrying out switching control of pixel electrode 9a and the pixel electrode 9a concerned, respectively is formed in two or more pixels formed in the shape of [which constitutes the image display field of the electro-optic device in this operation gestalt] a matrix, and data-line 6a to which a picture signal is supplied is electrically connected to the source concerned of TFT30. The picture signals S1, S2, --, Sn written in data-line 6a may be supplied to line sequential, and you may make it supply them to this order for every group to two or more data-line 6a which adjoin each other. Moreover, scanning-line 3a is electrically connected to the gate of TFT30, and it consists of predetermined timing so that the scan signals G1, G2, --, Gm may be impressed to scanning-line 3a in pulse line sequential at this order. It connects with the drain of TFT30 electrically, and pixel electrode 9a writes in the picture signals S1, S2, --, Sn supplied from data-line 6a in TFT30 which is a switching element when only a fixed period closes the switch to predetermined timing. Fixed period maintenance of the picture signals S1, S2, --, Sn of the predetermined level written in the liquid crystal as an example of electrooptic material through pixel electrode 9a is carried out between the counterelectrodes (it mentions later) formed in the opposite substrate (it mentions later). When the orientation and order of molecular association change with the potential level impressed, liquid crystal modulates light and enables a gradation display. The transmission to incident light decreases according to the electrical potential difference impressed in the unit of each pixel when it was in no MARI White mode, if it is in NOMA reeve rack mode, the transmission to incident light will be increased according to the electrical potential difference impressed in the unit of each pixel, and light with the contrast according to a picture signal will carry out outgoing radiation from an electro-optic device as a whole. Here, in order to prevent the held picture signal leaking, storage capacitance 70 is added to the liquid crystal capacity and juxtaposition which are formed between pixel electrode 9a and a counterelectrode. It ranks with scanning-line 3a, and while the fixed potential side capacity electrode of storage capacitance 70 is included, the capacity line 300 fixed to constant potential is formed.
[0052] In drawing 2 , on the TFT array substrate of an electro-optic device, two or more transparent pixel electrode 9a (the profile is shown by dotted-line section 9a') is prepared in the shape of a matrix, and data-line 6a and scanning-line 3a are prepared respectively along the boundary of pixel electrode 9a in every direction.
[0053] Moreover, scanning-line 3a is arranged so that channel field 1a' shown in the slash field of a Fig. Nakamigi riser among semi-conductor layer 1a may be countered, and scanning-line 3a functions as a gate electrode (with this operation gestalt, especially scanning-line 3a is broadly formed in the part used as the gate electrode concerned). Thus, TFT30 for pixel switching by which opposite arrangement of the scanning-line 3a was carried out as a gate electrode is formed in the crossing part of scanning-line 3a and data-line 6a at channel field 1a', respectively.
[0054] As shown in drawing 2 and drawing 3 , storage capacitance 70 is formed by carrying out opposite arrangement of the junction layer 71 as a pixel potential side capacity electrode connected to high concentration drain field 1e (and pixel electrode 9a) of TFT30, and a part of capacity line 300 as a

fixed potential side capacity electrode through a dielectric film 75.
[0055] The junction layer 71 has a function as a middle conductive layer which carries out trunk connection of pixel electrode 9a and the high concentration drain field 1e of TFT30 through the contact holes 83 and 85 besides the function as a pixel potential side capacity electrode of storage capacitance 70.
[0056] The capacity line 300 was seen superficially, and is extended in the shape of a stripe along with scanning-line 3a, and the part which laps with TFT30 has projected it under drawing 2 Nakagami. Such a capacity line 300 is constituted so that the 1st film which consists of conductive polish recon film of about 50nm of thickness etc., and the 2nd film which consists of metal silicide film containing the refractory metal of about 150nm of thickness etc. may have preferably the multilayer structure by which the laminating was carried out. Thus, if constituted, the 2nd film has a function as a protection-from-light layer which shades TFT30 from incident light in a TFT [besides the function as the capacity line 300 or a fixed potential side capacity electrode of storage capacitance 70]30 top.
[0057] On the other hand, bottom light-shielding film 11a is prepared in the TFT30 bottom on the TFT array substrate 10 in the shape of a grid. Bottom light-shielding film 11a consists of the metal simple substance containing at least one of refractory metals, such as Ti (titanium), Cr (chromium), W (tungsten), Ta (tantalum), Mo (molybdenum), and Pb (lead), an alloy, metal silicide, a polysilicon side, a thing that carried out the laminating of these.
[0058] And to the top and the bottom of TFT30 on the TFT array substrate 10, it sees superficially, respectively, the protection-from-light field is constituted in the shape of a grid by bottom light-shielding film 11a formed in the lengthwise direction in drawing 2 that the capacity line 300 extended, respectively carries out a phase crossover, and is formed in data-line 6a extended, respectively and the longitudinal direction in drawing 2 , and in the shape of a grid, and the opening field which is each pixel is specified.
[0059] Moreover, in drawing 3 , the dielectric film 75 arranged between the junction layer 71 as a capacity electrode and the capacity line 300 consists of silicon oxide film, such as comparatively thin HTO film of about 5-200nm of thickness, and LTO film, or a silicon nitride film. As long as membranous dependability is fully acquired from a viewpoint which increases storage capacitance 70, a dielectric film 75 is so good that it is thin.
[0060] As shown in drawing 2 and drawing 3 , data-line 6a is electrically connected to 1d of high concentration source fields through the contact hole 81 among semi-conductor layer 1a which consists of polish recon film. In addition, the junction layer which consists of the same film as the junction layer 71 mentioned above may be formed, and 1d of high concentration source fields may be electrically connected with data-line 6a through the junction layer concerned and two contact holes.
[0061] Moreover, it is installed in the perimeter from the image display field where pixel electrode 9a has been arranged, it connects with the constant source of potential electrically, and let the capacity line 300 be fixed potential. The constant source of potential of a positive supply or a negative supply supplied to the data-line drive circuit (it mentions later) which controls the sampling circuit which supplies the scanning-line drive circuit (it mentions later) and picture signal for supplying the scan signal for driving TFT30 to scanning-line 3a as such a constant source of potential to data-line 6a is sufficient, and the constant potential supplied to the counterelectrode 21 of the opposite substrate 20 is also available. Furthermore, in order to avoid that the potential fluctuation does a bad influence to TFT30 also about bottom light-shielding film 11a prepared in the TFT30 bottom, it is good to install in the perimeter from an image display field, and to connect with the constant source of potential like the capacity line 300.
[0062] Pixel electrode 9a is electrically connected to high concentration drain field 1e among semi-conductor layer 1a through contact holes 83 and 85 by relaying the junction layer 71. namely, -- this operation gestalt -- the junction layer 71 -- the function as a pixel potential side capacity electrode of storage capacitance 70 -- in addition, the function which carries out trunk connection of the pixel electrode 9a to TFT30 is achieved. Thus, even if the distance between layers is long to about 1000nm, the junction layer 71 can connect between both good comparatively in two or more in-series contact

holes of a minor diameter, avoiding the technical difficulty which connects between both in one contact hole, and becomes possible [raising a pixel numerical aperture], and etching at the time of contact hole puncturing runs through it, and it is useful also to prevention.
[0063] The electro-optic device is equipped with the TFT array substrate 10 and the transparent opposite substrate 20 by which opposite arrangement is carried out at this in drawing 2 and drawing 3 . The TFT array substrate 10 consists of for example, a quartz substrate, a glass substrate, and a silicon substrate, and the opposite substrate 20 consists of a glass substrate or a quartz substrate.
[0064] As shown in drawing 3 , pixel electrode 9a is prepared in the TFT array substrate 10, and the orientation film 16 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. Pixel electrode 9a consists of transparent conductive thin films, such as for example, ITO (Indium Tin Oxide) film. Moreover, the orientation film 16 consists of organic thin films, such as for example, a polyimide thin film.
[0065] On the other hand, it crosses to the opposite substrate 20 all over the, the counterelectrode 21 is formed, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 22 consists of organic thin films, such as a polyimide thin film.
[0066] You may make it prepare the light-shielding film of the shape of the shape of a grid, and a stripe in the opposite substrate 20. It can prevent more certainly that the incident light from the opposite substrate 20 side invades into channel field 1a', low concentration source field 1b, and low concentration drain field 1c by the light-shielding film on the opposite substrate 20 concerned with the capacity line 300 and data-line 6a which constitute a protection-from-light field from taking such a configuration like the above-mentioned. furthermore, the field where incident light is irradiated to the light-shielding film on such an opposite substrate 20 at least -- high -- it serves to prevent the temperature rise of an electro-optic device by forming by the film [****].
[0067] Thus, between the TFT array substrates 10 and the opposite substrates 20 which have been arranged so that pixel electrode 9a and the counterelectrode 21 which were constituted may meet, the liquid crystal which is an example of electrooptic material is enclosed with the space surrounded by the below-mentioned sealant, and the liquid crystal layer 50 is formed. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 16 and 22 in the condition that the electrical potential difference has not arisen between pixel electrode 9a and a counterelectrode 21. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant 52 may stick the TFT array substrate 10 and the opposite substrate 20 around those, and gap material, such as glass fiber for making distance between both substrates into a predetermined value or a glass bead, is mixed.
[0068] Furthermore, the substrate insulator layer 12 is formed in the bottom of TFT30 for pixel switching. The substrate insulator layer 12 has the function to prevent change of the property of TFT30 for pixel switching with the dry area at the time of polish of the front face of the TFT array substrate 10, the dirt which remains after washing, by being formed all over the TFT array substrate 10 besides the function which carries out layer insulation of TFT30 from bottom light-shielding film 11a.
[0069] In drawing 3 TFT30 for pixel switching It has LDD (Lightly DopedDrain) structure. Channel field 1a' of semi-conductor layer 1a in which a channel is formed of the electric field from scanning-line 3a and concerned scanning-line 3a, 1d list of high concentration source fields of low concentration source field 1b of the insulating thin film 2 containing the gate dielectric film with which scanning-line 3a and semi-conductor layer 1a are insulated, and semi-conductor layer 1a and low concentration drain field 1c, and semi-conductor layer 1a is equipped with high concentration drain field 1e.
[0070] On scanning-line 3a, the 1st interlayer insulation film 41 with which the contact hole 83 which leads to the contact hole 81 and high concentration drain field 1e which lead to 1d of high concentration source fields was punctured respectively is formed.
[0071] On the 1st interlayer insulation film 41, the junction layer 71 and the capacity line 300 are

formed, and the 2nd interlayer insulation film 42 with which the contact hole 85 which leads to the contact hole 81 and the junction layer 71 which lead to 1d of high concentration source fields was punctured respectively is formed on these.
[0072] In addition, with this operation gestalt, activation of the ion poured into the polish recon film which constitutes semi-conductor layer 1a and scanning-line 3a may be attained by performing 1000-degree C baking to the 1st interlayer insulation film 41. On the other hand, you may make it aim at relaxation of the stress produced near the interface of the capacity line 300 by not performing such baking to the 2nd interlayer insulation film 42.
[0073] Data-line 6a is formed on the 2nd interlayer insulation film 42, and the 3rd interlayer insulation film 43 with which the contact hole 85 which leads to the junction layer 71 was formed and which carried out flattening is formed on these. Pixel electrode 9a is prepared in the top face of the 3rd interlayer insulation film 43 constituted in this way.
[0074] With this operation gestalt, flattening of the front face of the 3rd interlayer insulation film 43 is carried out by CMP (Chemical Mechanical Polishing: chemical mechanical polishing) processing etc., and it reduces the poor orientation of the liquid crystal in the liquid crystal layer 50 resulting from the level difference by the various wiring and component which exist caudad.
[0075] According to this operation gestalt constituted as mentioned above, if incident light tends to carry out incidence channel field 1a' of TFT30, and near the from the opposite substrate 20 side, it will shade in the protection-from-light layer of the shape of a grid which consists of data-line 6a and a capacity line 300. On the other hand, from the TFT array substrate 10 side, if return light tends to carry out incidence channel field 1a' of TFT30, and near the It shades by bottom light-shielding film 11a (in combining two or more electro-optic devices by the projector for the color displays of a double plate type etc. through prism etc. and constituting one optical system especially). since the return light which consists of an incident light part which runs through prism etc. from other electro-optic devices is powerful, it is effective. . These results, most things which the property of TFT30 changes with optical leaks are lost, and very high lightfastness is acquired with the electro-optic device concerned. Moreover, the big storage capacitance 70 can be built using the non-opening field in which data-line 6a and scanning-line 3a were formed and which is each pixel.
[0076] Next, with reference to drawing 4 , wiring and shielding in the boundary region in this operation gestalt are explained. Drawing 4 is the graph-top view showing the configuration of various wiring including shielding prepared at the TFT array substrate [in / here / this operation gestalt] top, a circumference circuit, etc.
[0077] Drawing 5 to drawing 10 is the B-B' sectional view of drawing 4 showing the various examples of wiring of shielding wire, a picture signal line, a clock signal line, etc., respectively.
[0078] It sets to drawing 4 and the data-line drive circuit 101, the scanning-line drive circuit 104, and the sampling circuit 301 are formed in the boundary region located around the image display field on the TFT array substrate of liquid crystal equipment as an example of a circumference circuit.
[0079] Wiring 400 of a signal inputted through the external input terminal 102 prepared along the lower side of the TFT array substrate 1 in explanation of drawing 4 is made into what (for example, the signal wiring of "a clock signal CLX" is called "wiring 400 (CLX)") the alphabet notation same for easy-izing of explanation as a signal name is added and referred to for in a parenthesis after wiring 400, respectively below. [two or more] The scanning-line drive circuit 104 starts a built-in shift register circuit by the input of a start signal SPY, using the negative supply VSSY and positive supply VDDY for scanning-line drive circuit 104 which are supplied to external input terminal 102 list through wiring 400 (VSSY) and wiring 400 (VDDY) from an external control circuit as a power source. And a scan signal is impressed to scanning-line 3a by line sequential in pulse to the reference clock signal CLY for the built-in shift register circuits of the scanning-line drive circuit 104 supplied to external input terminal 102 list through wiring 400 (CLY) and wiring 400 (CLY'), and the predetermined timing based on the reversal clock signal CLY'.
[0080] The data-line drive circuit 101 starts a built-in shift register circuit by the input of start signal SPX, using the negative supply VSSX and positive supply VDDX for data-line drive circuit 101 which

are supplied to external input terminal 102 list through signal wiring 400 (VSSX) and wiring 400 (VDDX) from an external control circuit as a power source. And external input terminal 102 list is supplied through wiring 400 (CLX) and wiring 400 (CLX'). It is based on the reference clock signal CLX for the built-in shift register circuits of the data-line drive circuit 101, and its reversal clock signal CLX'. It doubles with the timing to which the scanning-line drive circuit 104 impresses a scan signal. About picture signal [which is supplied through the external input terminal 102 and wiring 400 (VID1) - wiring 400 (VID12) / by which serial-parallel conversion was carried out] VID1 - VID12 each, for example to 12 parallel signals The sampling circuit driving signal Qm (m= 1, 2, --) is data-line 6 minded [every], the sampling circuit drive signal line 306 is minded [301], and it supplies to predetermined timing.

[0081] The sampling circuit 301 equips each data-line 6a of every with TFT302, wiring 400 (VID1) - wiring 400 (VID12) are connected to the source electrode of TFT302 via the junction wiring 305, and the sampling circuit drive signal line 306 is connected to the gate electrode of TFT302. And an input of picture signals VID1-VID12 samples these picture signals. Moreover, if the sampling circuit driving signal Qm is inputted from the data-line drive circuit 101 through the sampling circuit drive signal line 306, sequential impression of the picture signal sampled about picture signal VID1 - VID12 each will be carried out for every group who consists of 12 adjoining data-lines 6a.

[0082] As mentioned above, the data-line drive circuit 101 and the sampling circuit 301 are constituted so that the picture signals VID1-VID12 changed into 12 parallel signals may be supplied to data-line 6a as picture signals S1 and S2 and --. Although the gestalt of this operation described the method which chooses as coincidence the sampling circuit 301 connected to adjoining 12 data-lines 6a, and consists of 12 data-lines 6a and which carries out the sequential transfer for every group, data-line 6a may be chosen every six, and you may choose every 24. Or the number of two or more arbitration may be chosen as coincidence. Under the present circumstances, it cannot be overemphasized that the external input terminal 102 and picture signal line for picture signals only of the number of a picture signal parallel at least are the need. In addition, you may constitute so that the number of a parallel picture signal and the number which chooses a sampling circuit 301 as coincidence may spread a phase etc. and it may become, and you may constitute so that the former may increase more than the latter. [0083] Furthermore, as shown in drawing 4 , if start signal SPX is inputted, after the data-line drive circuit 101 will shape in waveform the transfer signal from shift-register-circuit 101a which starts sequential generation of the reference clock signal CLX and the transfer signal based on the reversal clock signal CLK', and shift-register-circuit 101a, it is equipped with wave control circuit 101b and buffer circuit 101c which are supplied to a sampling circuit 301 through the sampling circuit drive signal line 306. Moreover, corresponding to the picture signals VID1-VID12 with which serial-parallel conversion of the sampling circuit 301 was carried out at 12 pieces, 12 TFT(s)302 are connected at a time to each sampling circuit drive signal line 306 at parallel. That is, the switches S1-S12 which consist of TFT(s) 302 are connected to 1 Motome's sampling circuit drive signal line 306 from the left, switches S13-S24 are connected to 2 Motome's sampling circuit drive signal line 306 from the left, and switch Sn-11 - Sn are connected to the right end sampling circuit drive signal line 306.

[0084] The enable signals ENB1 and ENB2 as a wave-selection signal which is one of the control signals are inputted into wave control circuit 101b. The selection period of a sampling circuit 301 is controlled by this wave control circuit 101b by restricting the width of face of the pulse by which a sequential output is carried out from shift-register-circuit 101a to the pulse width of enable signals ENB1 and ENB2 (it does not lap mutually like [the sampling circuit driving signals Q1 and Q2 which get mixed up, and the period when -- becomes high-level]). Generating of the block ghost between data-line 6a which receive a picture signal from the same wiring 400 (VID1) - wiring 400 (VID12) by this is prevented. Therefore, enable signals ENB1 and ENB2 are control signals of the RF which has a period shorter than a horizontal scanning period as well as a clock signal CLX and CLX'.

[0085] In addition, with this operation gestalt, the vertical flow terminal 106 for taking an electric flow between the counterelectrodes 21 (referring to drawing 3) by the side of the TFT array substrate 1 and the opposite substrate 20 is formed in the four corners of an image display field (however, in drawing 4 ,

two corners are illustrated among those). The vertical flow terminal 106 is supplied through wiring 400 (LCCOM) at external input terminal 102 list.
[0086] Next, the various examples of shielding employable [with the electro-optic device of this operation gestalt] are shown in drawing 10 from drawing 5 , respectively. Drawing 5 to drawing 10 is the sectional view showing structure [in / here / the B-B' cross section of drawing 4 of the various examples of shielding], respectively, respectively.
[0087] In drawing 10 , the wiring 400 (VID1) which is a picture signal line - wiring 400 (VID12) by each example, respectively from drawing 5 It consists of same electric conduction film (for example, multilayers containing the conductive polish recon film and the conductive metal silicide film) as the capacity line 300 in an image display field. Electric screening of these wiring 400 is carried out with shielding which consists of the same film (for example, aluminum film) as data-line 6a in an image display field at least.
[0088] That is, by the example of drawing 5 , electric screening of the wiring 400 which consists of same electric conduction film as the capacity line 300 is carried out by upper part shielding 401a which consists of same electric conduction film as data-line 6a formed in the wrap field in each wiring 400 along with each wiring 400 from the upper part. By this example, since especially upper part shielding 401a is divided every wiring 400 of one, it can carry out electric screening of each wiring 400 mutually from other the wiring 400 of all.
[0089] By the example of drawing 6 , electric screening of the wiring 400 which consists of same electric conduction film as the capacity line 300 is carried out by upper part shielding 401b which consists of same electric conduction film as data-line 6a which met two or more wiring 400 from the upper part, and packed two or more wiring 400, and was formed in the wrap field. By this example, especially upper part shielding 401b is divided for two or more signal lines of every. Therefore, as compared with the case of the example of drawing 5 which prepares upper part shielding 401a for every one signal line, upper part shielding 401b can be formed comparatively easily. Under the present circumstances, it is good for the effect which an electromagnetic wave does to pack two or more small signal lines mutually by one upper part shielding 401b, to be made to carry out electric screening of two or more pixel signal lines etc. to it fundamentally, and for the effect is another side, for example, an electromagnetic wave affects mutual [, such as a picture signal line and a clock signal line,] to carry out electric screening of the large signal line mutually by separate upper part shielding 401b fundamentally. That is, thereby, the disadvantageous profit at the time of carrying out electric screening of two or more signal lines collectively can be suppressed to the minimum.
[0090] In addition to upper part shielding 401a shown in drawing 5 , by the example of drawing 7 , electric screening of the wiring 400 is carried out from the upper and lower sides from lower part shielding 11b which consists of same electric conduction film as bottom light-shielding film 11a in an image display field.
[0091] In addition to upper part shielding 401a shown in drawing 5 , by the example of drawing 8 , electric screening of the wiring 400 is carried out from the upper and lower sides from the lower part shielding 402 which consists of same electric conduction film as scanning-line 3a in an image display field.
[0092] In addition to the same upper part shielding 401c as drawing 7 , and lower part shielding 11b, by the example of drawing 9 , electric screening of the wiring 400 is carried out from four directions by side shielding 401d embedded in the hole which it came to install from the same electric conduction film as upper part shielding 401c, and was dug in the substrate insulator layer 12, ****** 41 between the 1st layer, a dielectric film 75, and the 2nd interlayer insulation film 42 by the groove along with wiring 400. By this example, since especially shielding is carrying out electric screening of the perimeter every wiring 400 of one, it can reduce the bad influence by two or more electromagnetic waves between wiring 400 as much as possible.
[0093] By the example of drawing 10 , electric screening of the wiring 400 is carried out from four directions by side shielding 401e embedded in the hole which in addition to the same upper part shielding 401c as drawing 8 , and the lower part shielding 402 was installed from the same electric

conduction film as upper part shielding 401c, and became, and was dug in ****** 41 between the 1st layer, a dielectric film 75, and the 2nd interlayer insulation film 42 by the groove along with wiring 400. By this example, since especially shielding is carrying out electric screening of the perimeter every wiring 400 of one, it can reduce the bad influence by two or more electromagnetic waves between wiring 400 as much as possible. As explained above, according to the electro-optic device of this operation gestalt, in the image display field, the laminating of the 2nd electric conduction film which makes data-line 6a is carried out through ********** on the 1st electric conduction film which makes the capacity line 300. In the boundary region, the wiring 400 connected to the circumference circuit is formed from either these 1st electric conduction film or the 2nd electric conduction film, and shielding which carries out electric screening of the wiring 400 from an one direction (for example, the upper part and a lower part) at least is formed from another side of these 1st electric conduction film and the 2nd electric conduction film. therefore, the electromagnetism to the picture signal on the wiring 400 of a picture signal line etc. -- the diving of a noise can be reduced effectively. And since it is not necessary to form the film of dedication separately in order to form wiring 400 and shielding in a boundary region, it is advantageous also when simplifying an equipment configuration and a production process. When a pixel pitch is made detailed and drive frequency is especially raised for improvement in image grace the noise (for example, the electromagnetism from control signal lines, such as a clock signal line and a wave-selection signal line, to the picture signal on a picture signal line -- a noise --) which generally starts such a signal line the electromagnetism to the picture signal on the picture signal line from an external device, other circuits, etc. -- the electromagnetism to the external devices from a control signal line, other circuits, etc., such as a noise, a clock signal line, and a wave-selection signal line, -- a noise etc. increases relatively (that is, S/N falls). Therefore, the configuration which carries out electric screening of the wiring 400 of the picture signal line wired like this operation gestalt in the boundary region, a control signal line, etc. with shielding, such as upper part shieldinga [401] and 401b or 401c, lower part shielding 11b or 402, and side shielding 401d or 401e, is very advantageous, when making a pixel pitch detailed or raising drive frequency.

[0094] moreover -- since electric screening of the picture signal line is carried out as wiring 400 especially with this operation gestalt -- the picture signals S1 and S2 on the picture signal line from signal lines and wiring, or the circuit as a noise source, or a component, and the electromagnetism to -- the diving of a noise can be reduced effectively. Therefore, based on the picture signals S1 and S2 which finally have high S/N, and --, it becomes possible to perform high-definition image display in an image display field.

[0095] Moreover, with the operation gestalt explained above, as shown in drawing 10 from drawing 5 , electric screening of the junction wiring 305 and the sampling circuit drive signal line 306 which carry out trunk connection of the picture signal line shown in drawing 4 and the sampling circuit 301 may be carried out from the upper part, a lower part, or the side. thus -- if it carries out -- the picture signals S1 and S2 on the junction wiring 305, and the electromagnetism to -- the diving of a noise, and the sampling circuit driving signals Q1 and Q2 on the sampling circuit drive signal line 306 and the electromagnetism to -- a dive of a noise can be reduced effectively. Since the part which counters the counterelectrode 21 prepared in the opposite substrate 20 is included, especially if electric screening of these junction wiring 305 or the sampling circuit drive signal line 306 is carried out with upper part shielding arranged among both from a viewpoint which reduces the parasitic capacitance of these wiring and counterelectrodes 21, they are effective.

[0096] Furthermore, with the operation gestalt explained above, as shown in drawing 10 from drawing 5 , electric screening of the wiring 400 (CLX) as a clock signal line, wiring 400 (CLX'), and the wiring 400 (ENB1) as a wave-selection signal line and wiring 400 (ENB2) may be carried out from the upper part, a lower part, or the side. thus, electromagnetism powerful at the RF which originates in the control signal which is high potential with the high frequency which is on these control signal lines and is generally easy to serve as a noise source over a picture signal if constituted -- a noise can prevent effectively jumping into the upper picture signals, such as a picture signal line.

[0097] In the electro-optic device (each operation gestalt is included) of this invention explained above,

shielding is preferably fixed to touch-down potential or other constant potentials. Under the present circumstances, while carrying out electric screening of picture signal lines (wiring 400 (VID1), wiring 400 (VID2), --, etc.) and the control signal lines (wiring 400 (CLX), wiring 400 (CLX'), --, etc.) separately especially, it is more desirable to fix to constant potential which is mutually different. Thus, if constituted, the before-it-happens prevention of the situation where those potential fluctuation does effect mutually among both signal lines through the same constant potential wiring can be carried out. For example, what is necessary is to carry out electric screening of the picture signal line by low voltage by [of low voltage (touch-down potential or about several volts)] connecting with the constant potential line of potential the 1st law, and just to carry out electric screening of the control signal line with high potential by [of high potential (about about ten volts)] connecting with the constant potential line of potential the 2nd law.

[0098] In addition, it is desirable to share the main track of shielding and power-source wiring or branching wiring with this operation gestalt. Thus, shielding is fixable to constant potential, attaining simplification of an equipment configuration and a production process, if constituted. And since the which shielding in a boundary region occupies will be assigned to power-source wiring, power-source wiring can be constituted broadly comparatively easily. Furthermore, by forming shielding broadly, since the engine performance of shielding also improves, it is much more advantageous.

[0099] Moreover, although wiring 400 was formed from the same electric conduction film as the capacity line 300 and shielding was formed from a different conductive layer from the capacity line 300 by the various examples shown in drawing 10 from drawing 5 Form wiring 400 from the same electric conduction film as data-line 6a, and may form shielding from a different conductive layer from data-line 6a, and Wiring 400 may be formed from the same electric conduction film as scanning-line 3a, and shielding may be formed from a different conductive layer from scanning-line 3a, and wiring 400 may be formed from the same electric conduction film as bottom light-shielding film 11a, and shielding may be formed from a different conductive layer from bottom light-shielding film 11a.

[0100] Furthermore, it is also possible to form some shielding from the same film as wiring, and it is possible to mainly carry out electric screening from the side in this case. the wiring 400 (VSSX) which supplies the wiring 400 (VSSY) which supplies a negative supply VSSY, and a negative supply VSSX in the same flat surface with this operation gestalt as shown in drawing 4 -- a picture signal -- a line -- wiring 400 (VID2), wiring 400 (VID4), wiring 400 (VID6), and -- are surrounded, and it is functioning as a picture signal shielding wire. the wiring 400 (VSSX) which supplies similarly the wiring 400 (VDDY) which supplies a positive supply VDDY, and a negative supply VSSX in the same flat surface -- a picture signal -- a line -- wiring 400 (VID1), wiring 400 (VID3), wiring 400 (VID5), and -- are surrounded, and it is functioning as a picture signal shielding wire. Furthermore, too, in the same flat surface, the wiring 400 (VDDX) which supplies a positive supply VDDX has surrounded control signal lines, such as the clock signal line slack wiring 400 (CLX) and wiring 400 (CLX'), and is functioning as a control signal shielding wire. Too, in the same flat surface, the wiring 400 (VDDY) which supplies a positive supply VDDY similarly has surrounded the control signal of the clock signal line slack wiring 400 (CLY), wiring 400 (CLY'), etc., and is functioning as a control signal shielding wire. As the broken line showed especially in drawing 4 , two tips of wiring 400 (VDDX) as a control signal shielding wire may be mutually connected by the connection 93, and two tips of wiring 400 (VSSX) as a picture signal shielding wire may be similarly connected mutually by the connection 91.

[0101] furthermore -- it is also possible to constitute two electric conduction film by which the laminating was carried out from aluminum film of both low resistance again, and it is possible to carry out electric screening of the wiring of low resistance by the electric conduction film of low resistance by this -- becoming -- very much -- electromagnetism -- the configuration into which a noise cannot jump easily is obtained.

[0102] By carrying out the laminating of many conductive layers with the operation gestalt explained above, as shown in drawing 3 Although it is easing by carrying out flattening of the front face of the 3rd interlayer insulation film 43, that a level difference arises to the field in alignment with data-line 6a and scanning-line 3a in the substrate side (namely, front face of the 3rd interlayer insulation film 43) of pixel

electrode 9a Replace with this or, in addition, the TFT array substrate 10, the substrate insulator layer 12, the 1st interlayer insulation film 41, the 2nd interlayer insulation film 42, or the 3rd interlayer insulation film 43 is trenched. By embedding wiring and the TFT30 grade of data-line 6a etc., may perform flattening processing and grinding the level difference of the top face of the 2nd interlayer insulation film 42 by CMP (Chemical Mechanical Polishing) processing etc. -- or the flattening processing concerned may be performed by forming in Taira and others using organic [SOG].
[0103] With the operation gestalt explained above, in addition, TFT30 for pixel switching Although it has LDD structure as preferably shown in drawing 3 , may have the offset structure which does not drive an impurity into low concentration source field 1b and low concentration drain field 1c, and You may be TFT of the self aryne mold which drives in an impurity by high concentration by using as a mask the gate electrode which consists of a part of scanning-line 3a, and forms the high concentration source and a drain field in self align. Moreover, although considered as the single gate structure which has arranged one gate electrode of TFT30 for pixel switching among 1d [of high concentration source fields], and high concentration drain field 1e with this operation gestalt, two or more gate electrodes may be arranged among these. Thus, if TFT is constituted above the dual gate or the triple gate, the leakage current of a joint with a channel, the source, and a drain field can be prevented, and the current at the time of OFF can be reduced.
[0104] In addition, wiring 400 is received as deformation of the operation gestalt of this invention explained above in a boundary region. It replaces with or adds to preparing **** various shielding shown in drawing 10 from drawing 5 . From one of four electric conduction film of the capacity line 300, data-line 6a, scanning-line 3a, and bottom light-shielding film 11a, while forming the control signal line slack wiring 400 (CLX), wiring 400 (CLY), and -- The picture signal line slack wiring 400 (VID1), wiring 400 (VID2), and -- may be formed from other one of the four electric conduction film of these. Thus, if constituted, since only the part which estranges both signal lines in the direction perpendicular to a substrate and by which the interlayer insulation film is arranged among both signal lines compared with the case where these two kinds of wiring is formed in the same flat surface by carrying out patterning of the same electric conduction film can reduce the diving of the noise between both signal lines, it is advantageous. That is, even if there is no shielding, it becomes possible by forming these two kinds of signal lines to reduce a noise so that it may estrange in the direction perpendicular to a substrate in this way. furthermore, the thing for which such a configuration and various shielding mentioned above are combined -- electromagnetism -- the effectiveness of reducing a noise can be heightened further.
[0105] (The whole electro-optic device configuration) The whole electro-optic device configuration in each operation gestalt constituted as mentioned above is explained with reference to drawing 11 and drawing 12 . In addition, drawing 11 is the top view which looked at the TFT array substrate 10 from the opposite substrate 20 side with each component formed on it, and drawing 12 is the H-H' sectional view of drawing 11 .
[0106] In drawing 12 , on the TFT array substrate 10, the sealant 52 is formed along the edge and the light-shielding film 53 as a frame which specifies the circumference of image display field 10a is formed in parallel to the inside. The data-line drive circuit 101 and the external circuit connection terminal 102 are formed in the field of the outside of a sealant 52 along with one side of the TFT array substrate 10, and the scanning-line drive circuit 104 is established in it along with two sides which adjoin this one side. If the scan signal delay supplied to scanning-line 3a does not become a problem, the thing only with one side sufficient [the scanning-line drive circuit 104] cannot be overemphasized. Moreover, the data-line drive circuit 101 may be arranged on both sides along the side of image display field 10a. Furthermore, two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of image display field 10a is formed in one side in which the TFT array substrate 10 remains. Moreover, in at least one place of the corner section of the opposite substrate 20, the vertical flow material 106 for taking a flow electrically between the TFT array substrate 10 and the opposite substrate 20 is formed. Moreover, the sampling circuit 301 shown in drawing 4 is established in the frame field. And as shown in drawing 12 , the opposite substrate 20 with the almost same profile as

the sealant 52 shown in drawing 11 has fixed to the TFT array substrate 10 by the sealant 52 concerned.
[0107] In addition, on the TFT array substrate 10, the inspection circuit for inspecting the precharge circuit which precedes the precharge signal of a predetermined voltage level with a picture signal, and supplies it to two or more data-line 6a respectively, the quality of the electro-optic device concerned at the manufacture middle or the time of shipment, a defect, etc. in addition to these data-line drive circuits 101, the scanning-line drive circuit 104, and sampling circuit 301 grade etc. may be formed.
[0108] You may make it connect with LSI for a drive mounted on the TAB (Tape Automated bonding) substrate instead of forming the data-line drive circuit 101 and the scanning-line drive circuit 104 on the TFT array substrate 10 electrically and mechanically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10 with the operation gestalt explained with reference to drawing 12 from drawing 1 above. Moreover, according to the exception of modes of operation, such as TN mode, VA (Vertically Aligned) mode, and PDLC (Polymer Dispersed LiquidCrystal) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, a polarizing plate, etc. are respectively arranged in a predetermined direction at the side in which the outgoing radiation light of the side in which the incident light of the opposite substrate 20 carries out incidence, and the TFT array substrate 10 carries out outgoing radiation.
[0109] Since the electro-optic device in the operation gestalt explained above is applied to a projector, the electro-optic device of three sheets will be respectively used as a light valve for RGB, and incidence of the light of each color respectively decomposed through the dichroic mirror for RGB color separation will be respectively carried out to each light valve as incident light. Therefore, with each operation gestalt, the color filter is not prepared in the opposite substrate 20. However, the color filter of RGB may be formed in the predetermined field which counters pixel electrode 9a on the opposite substrate 20 with the protective coat. If it does in this way, the electro-optic device in each operation gestalt is applicable about the color electro-optic device of direct viewing types other than a projector, or a reflective mold. Moreover, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 20. Or it is also possible to form a color filter layer in the bottom of pixel electrode 9a which counters RGB on the TFT array substrate 10 by a color resist etc. If it does in this way, a bright electro-optic device is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 20 again may be formed. According to this opposite substrate with a die clo IKKU filter, a brighter color electro-optic device is realizable.
[0110] This invention is not restricted to the operation gestalt mentioned above, and can be suitably changed in the range which is not contrary to the summary or thought of invention which can be read in a claim and the whole specification, and the electro-optic device accompanied by such modification and its manufacture approach are also included in the technical range of this invention.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] They are equal circuits established in two or more pixels of the shape of a matrix which constitutes the image display field in the electro-optic device of the operation gestalt of this invention, such as various components and wiring.
[Drawing 2] It is the top view of two or more pixel groups where the TFT array substrate with which the data line in the electro-optic device of an operation gestalt, the scanning line, a pixel electrode, etc. were formed adjoins each other.
[Drawing 3] It is the A-A' sectional view of drawing 2 .
[Drawing 4] It is the graph-top view showing the configuration of various wiring including shielding prepared on the TFT array substrate in this operation gestalt, a circumference circuit, etc.
[Drawing 5] It is the B-B' sectional view of drawing 4 concerning one example of shielding employable with this operation gestalt.
[Drawing 6] It is the B-B' sectional view of drawing 4 concerning other examples of shielding employable with this operation gestalt.
[Drawing 7] It is the B-B' sectional view of drawing 4 concerning other examples of shielding employable with this operation gestalt.
[Drawing 8] It is the B-B' sectional view of drawing 4 concerning other examples of shielding employable with this operation gestalt.
[Drawing 9] It is the B-B' sectional view of drawing 4 concerning other examples of shielding employable with this operation gestalt.
[Drawing 10] It is the B-B' sectional view of drawing 4 concerning other examples of shielding employable with this operation gestalt.
[Drawing 11] It is the top view which looked at the TFT array substrate in the electro-optic device of an operation gestalt from the opposite substrate side with each component formed on it.
[Drawing 12] It is the H-H' sectional view of drawing 11 .
[Description of Notations]
1a -- Semi-conductor layer
1a' -- Channel field
1b -- Low concentration source field
1c -- Low concentration drain field
1d -- High concentration source field
1e -- High concentration drain field
2 -- Insulating thin film
3a -- Scanning line
6a -- Data line
9a -- Pixel electrode
10 -- TFT array substrate
11a -- Bottom light-shielding film

12 -- Substrate insulator layer
16 -- Orientation film
20 -- Opposite substrate
21 -- Counterelectrode
22 -- Orientation film
30 -- TFT
50 -- Liquid crystal layer
70 -- Storage capacitance
71 -- Junction layer
75 -- Dielectric film
81, 83, 85 -- Contact hole
101 -- Data-line drive circuit
101a -- Shift register circuit
101b -- Wave control circuit
101c -- Buffer circuit
104 -- Scanning-line drive circuit
300 -- Capacity line
301 -- Sampling circuit
302 -- TFT of a sampling circuit
305 -- Junction wiring
306 -- Sampling circuit drive signal line
400 -- Wiring
401a, 401b, 401c -- Upper part shielding
401d, 401e -- Side shielding
402 -- Lower part shielding

[Translation done.]

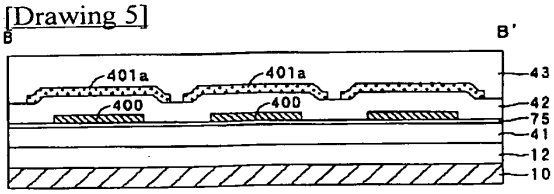
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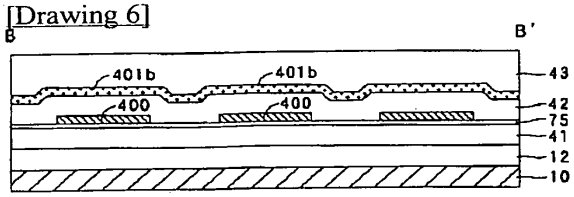
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DRAWINGS

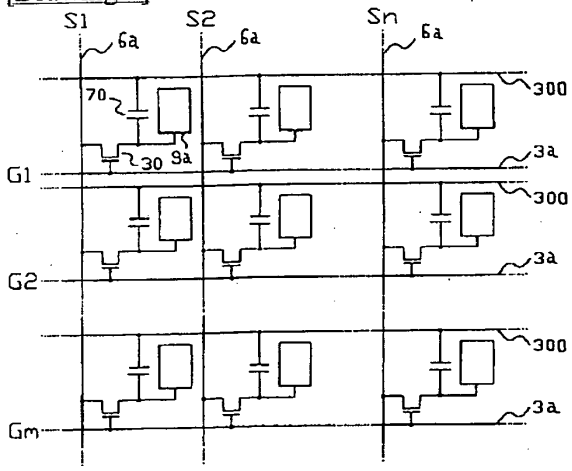
[Drawing 5]



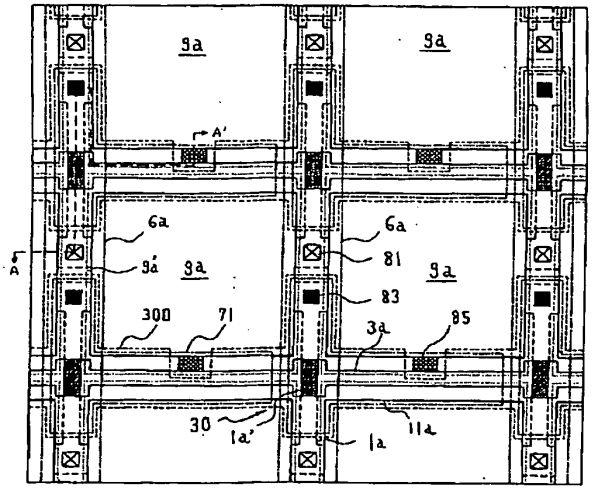
[Drawing 6]



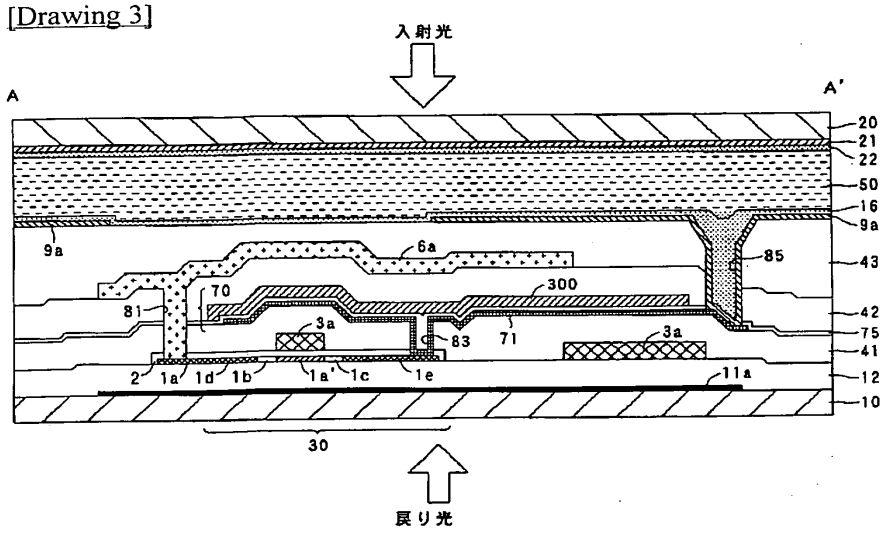
[Drawing 1]



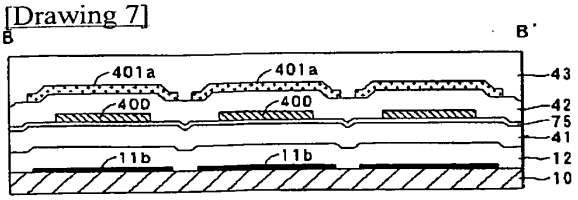
[Drawing 2]



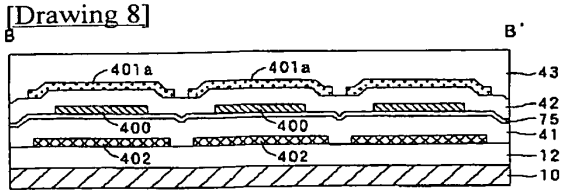
[Drawing 3]



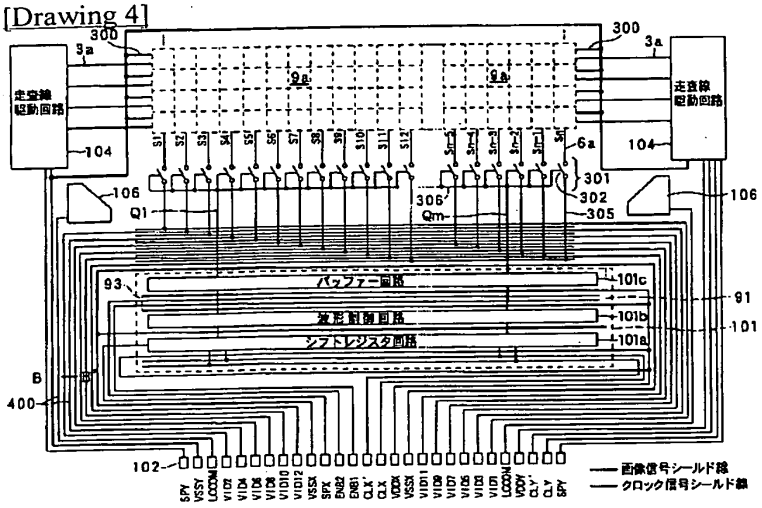
[Drawing 7]



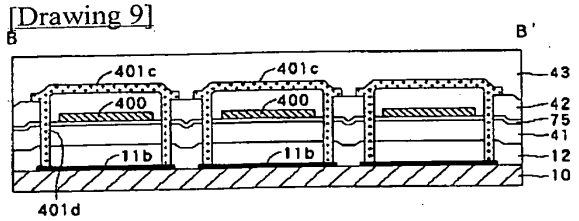
[Drawing 8]



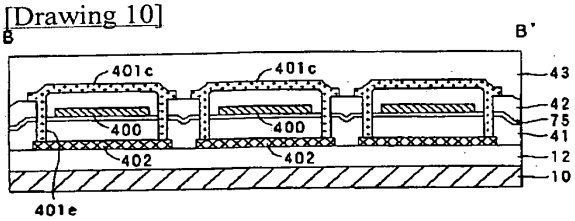
[Drawing 4]



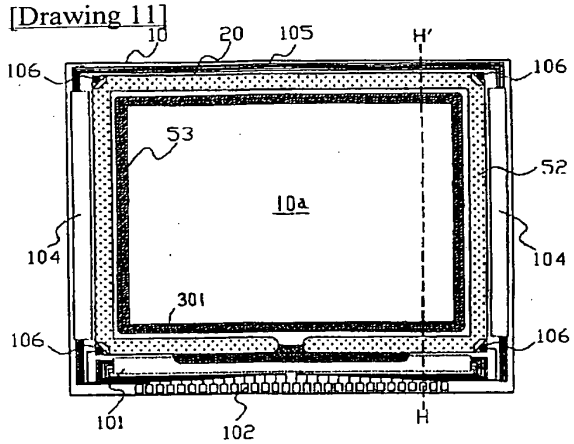
[Drawing 9]



[Drawing 10]

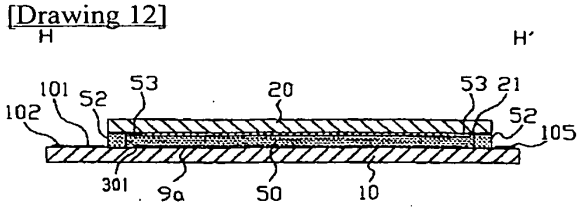


[Drawing 11]



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[Drawing 12]



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出願人 Applicant(s):	セイコーエプソン株式会社

２００４年　４月１２日

特許庁長官
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Japan Patent Office

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出証特２００４－３０３０２７３

【書類名】　明細書

【発明の名称】　電気光学装置及びこれを備えた電子機器

【特許請求の範囲】

【請求項１】　素子基板上における画像表示領域に複数の画素部を備えており、

前記素子基板上における前記画像表示領域の周辺に位置する周辺領域に、複数の外部回路接続端子と、該複数の外部回路接続端子に夫々一端が接続された複数の主配線と、該主配線の他端に接続されており前記外部回路接続端子から前記主配線を介して供給される電気信号に基づいて前記画素部を駆動するための周辺駆動回路とを備えており、

前記複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように前記周辺領域内に平面レイアウトされていることを特徴とする電気光学装置。

【請求項２】　前記周辺駆動回路の内部配線、前記周辺駆動回路から前記画素部に向けて引き出された引出配線、及び前記主配線から分岐した分岐配線のうち少なくとも一つを含んでなる副配線は、その第１部分において前記同一導電膜とは異なる他の導電膜から形成されて前記主配線と層間絶縁膜を介して交差するように且つその第２部分において前記同一導電膜から形成されて前記主配線と交差しないように前記周辺領域内に平面レイアウトされていることを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記第１部分及び前記第２部分の間は、前記層間絶縁膜に開孔されたコンタクトホールを介して電気的に接続されていることを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、

前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、

前記対向電極電位線は、前記周辺領域において、前記複数の主配線中で前記素子基板の縁寄りに位置し、

前記周辺駆動回路は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに位置することを特徴とする請求項１から３のいずれか一項に記載の電気光学装置。

【請求項５】　前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、

前記複数の外部回路接続端子のうち前記対向電極電位線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置することを特徴とする請求項４に記載の電気光学装置。

【請求項６】　前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、

前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、

前記対向電極電位線は、前記周辺領域において、前記対向電極電位線を除く一又は複数の主配線よりも前記素子基板の縁寄りに位置し、前記対向電極電位線を除く他の一又は複数の主配線よりも前記素子基板の中央寄りに位置し、

前記周辺駆動回路の一部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに部分的に位置し、前記周辺駆動回路の他部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の縁寄りに部分的に位置することを特徴とする請求項１から３のいずれか一項に記載の電気光学装置。

【請求項７】　前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、

前記複数の外部回路接続端子のうち前記他の一又は複数の主配線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置することを特徴とする請求項６に記載の電気光学装置。

【請求項８】　前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を夫々供給すると共に前記対向電極電位線と交差しない一対のクロック信号線を含むことを特徴とする請求項４から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を供給するための一対のクロック信号線と、前記電気信号として電源信号を供給するための電源配線とを含み、

前記一対の信号線と前記電源配線とは交差しないことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。

【請求項１０】　前記複数の主配線は、相互に交差することを避けて蛇行するように平面レイアウトされていることを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記複数の主配線は少なくとも部分的に、前記同一導電膜と別層に形成された他の導電膜からなる冗長配線を含むことを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項１２】　請求項１から１１のいずれか一項に記載の電気光学装置を具備してなることを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】

本発明は、例えば素子基板上に周辺駆動回路が作り込まれてなる駆動回路内蔵型の液晶装置等の電気光学装置及該電気光学装置を具備してなる電子機器の技術分野に属する。

【０００２】

【背景技術】

この種の液晶装置等の電気光学装置では、その画像表示領域に、画像表示用に駆動される複数の画素部がマトリクス状に配列されている。各画素部には、例えば、画素電極と各画素電極をスイッチング制御する薄膜トランジスタ（Thin Film Transistor；以下、適宜「ＴＦＴ」という。）とが配置されており、縦横に相

隣接する画素電極間の間隙に沿って走査線、データ線、容量線等の配線が設けられている。特に、駆動回路内蔵型の場合には、走査線やデータ線を駆動するための走査線駆動回路やデータ線駆動回路が、同一素子基板上における周辺領域に作り込まれている。このため、通常は、素子基板の一辺に沿って配列された複数の外部回路接続端子から周辺駆動回路に至る、電源信号線、クロック信号線、画像信号線、制御信号線等の各種配線が、周辺領域内に平面レイアウトされている。

【０００３】

ここで、電気光学装置或いは素子基板の小型化の要請に沿って、限られた周辺領域内に外部回路接続端子から周辺回路に至る多数本の各種配線が収まるように、或いは限られた周辺領域内で近接配置される各種配線間における相互ノイズが低減されるように、当該各種配線の平面レイアウトを工夫する技術も提案されている（特許文献１及び２参照）

【特許文献１】

特開平１１－２０２３６７号公報

【特許文献２】

特開平１１－２２３８３２号公報

【０００４】

【発明が解決しようとする課題】

この種の電気光学装置では、装置或いは素子基板の小型化を図りつつも、駆動周波数向上や精細度向上による画像の高品位化の要請は、実践上極めて強い。

【０００５】

しかしながら、上述した従来の周辺領域に各種配線を設ける技術によれば、限られた周辺領域内には、複数の外部回路接続端子に一端が夫々接続された複数の配線（本願明細書では適宜「主配線」と称する）が存在している。しかも主配線の本数或いは外部回路接続端子の個数は、駆動方式の複雑高度化に伴い増大傾向にある。このため、少なくとも何本かの主配線については、その他端が周辺駆動回路や上下導通端子に至る途中で、他の主配線と交差せざるを得ない。この交差する個所では、素子基板上に構築された積層構造において当該少なくとも一つの主配線を構成する導電膜よりも下側又上側に積層された他の導電膜からなる中継

配線部分を経由しなければならない。そして、通常例えばアルミニウム等の素子基板上に構築された積層構造中で最も低抵抗の導電膜から主配線は形成されることに鑑みれば、このように他の導電膜から、即ち最も低抵抗ではない導電膜から中継配線部分を形成することは、主配線における配線抵抗の増大を顕著に招くという技術的問題点がある。そして、係る主配線における配線抵抗の増大は、その主配線の用途に応じて各種の画質低下を招きかねない。

【０００６】

このように周辺領域を狭めることによる装置の小型化と画素ピッチ或いは配線ピッチの微細化による画質向上とを両立させることは、実践上極めて困難である。加えて、上述の如き中継配線部分を作ると、接触抵抗やコンタクトホール抵抗による抵抗増加、更に素子基板上における積層構造及び製造プロセスの複雑化を招き、最終的に装置歩留まりの低下や信頼性の低下を招きかねないという技術的問題点もある。

【０００７】

本発明は、例えば上記問題点に鑑みてなされたものであり、主配線を効率的に低抵抗化できると共に主配線間における信号の相互干渉を抑制でき、これらにより高品位な画像表示が可能である電気光学装置及びこのような電気光学装置を具備する電子機器を提供することを課題とする。

【０００８】

【課題を解決するための手段】

本発明の電気光学装置は上記課題を解決するために、素子基板上における画像表示領域に複数の画素部を備えており、前記素子基板上における前記画像表示領域の周辺に位置する周辺領域に、複数の外部回路接続端子と、該複数の外部回路接続端子に夫々一端が接続された複数の主配線と、該主配線の他端に接続されており前記外部回路接続端子から前記主配線を介して供給される電気信号に基づいて前記画素部を駆動するための周辺駆動回路とを備えており、前記複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように前記周辺領域内に平面レイアウトされている。

【０００９】

本発明の電気光学装置によれば、その動作時には、外部回路接続端子及びこれに一端が接続された主配線を介して、例えば画像信号、クロック信号、その反転信号、電源信号、制御信号等の各種電気信号が夫々、主配線の他端に接続された周辺駆動回路に供給される。或いは、外部回路接続端子及びこれに一端が接続された主配線を介して例えば、対向電極電位が、周辺領域に設けられた上下導通端子に供給され、更に該上下導通材を介して対向基板側に設けられた対向電極へと供給される。このような主配線は例えば、走査線駆動回路、データ線駆動回路等である周辺駆動回路によって、上述の如く供給される各種電気信号に基づいて走査線及びデータ線が駆動されることで、所定方式による画像表示が行われる。例えば、複数の画素部がアクティブマトリクス駆動される。

【００１０】

ここで本発明の電気光学装置では特に、複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように周辺領域に平面レイアウトされている。このため、導電性に優れた導電膜を、素子基板上に構築される積層構造中に含めておき、上述した同一導電膜として採用すれば、或いは、素子基板上に構築される積層構造中で最も導電性に優れた導電膜を上述の同一導電膜として採用すれば、複数の主配線を導電性に優れた配線として構築できる。更に、主配線の本数或いは外部回路接続端子の個数が、駆動方式の複雑高度化に伴い増大しても、複数の主配線は相互に交差しないように平面レイアウトされているので、交差する個所で中継配線部分を経由させる必要性はない。そして、通常例えばアルミニウム等の素子基板上に構築された積層構造中で最も低抵抗の導電膜から主配線を形成すれば、これよりも低抵抗ではない積層構造中の他の導電膜から形成された中継配線部分を利用する場合と比較して、主配線における配線抵抗を顕著に低減できる。従って、主配線の配線抵抗の増加に起因した各種の画質低下を効果的に未然防止できる。言い換えれば、周辺領域を狭めての装置の小型化と、画素ピッチ或いは配線ピッチの微細化による画質向上とを、両立させることが可能となる。加えて、上述の如く主配線中に中継配線部分を作らないので済むので、主配線における接触抵抗やコンタクトホール抵抗による抵抗増加を回避でき、更に素子基板上における積層構造及び製造プロセスを単純化できる。従って、最終的に装置

歩留まりの低下や信頼性の向上が可能となる。しかも、例えば二つの主配線が薄い層間絶縁膜を介して交差する場合に見られるような該二つの主配線間における二種類の電気信号の相互干渉を、複数の主配線を相互に交差しないように平面レイアウトすることで顕著に低減することも可能となる。

【００１１】

以上の結果、本発明の電気光学装置によれば、主配線を効率的に低抵抗化できると共に主配線間における信号の相互干渉を抑制でき、これらにより高品位な画像表示が可能となる。

【００１２】

本発明の電気光学装置の一態様では、前記周辺駆動回路の内部配線、前記周辺駆動回路から前記画素部に向けて引き出された引出配線、及び前記主配線から分岐した分岐配線のうち少なくとも一つを含んでなる副配線は、その第１部分において前記同一導電膜とは異なる他の導電膜から形成されて前記主配線と層間絶縁膜を介して交差するように且つその第２部分において前記同一導電膜から形成されて前記主配線と交差しないように前記周辺領域内に平面レイアウトされている。

【００１３】

この態様によれば、周辺領域には、内部配線、引出配線、分岐配線等の副配線が設けられている。これらのうち、周辺駆動回路の内部配線は、周辺駆動回路内の例えばシフトレジスタを構成する複数配列された回路間をつなぐ配線である。引出配線は、走査線、データ線、容量線等を画像表示領域から周辺領域へ引き出すための配線である。分岐配線は、例えば電源信号やクロック信号など、周辺駆動回路の複数箇所で共通に使用する各種電気信号を供給するための配線である。このような副配線は、その第１部において、例えば最も導電性に優れた導電膜に対して層間絶縁膜を介して積層された二番目、三番目等に導電性に優れた金属膜或いは導電性ポリシリコン膜等からなり、主配線と交するように平面レイアウトされている。更に、このような副配線は、その第２部において、例えば主配線と同様に最も導電性に優れた導電膜からなり、主配線と交しないように平面レイアウトされている。従って、副配線についても主配線と抵触しない限りにおいて、

その導電性を向上させることが可能である。

【００１４】

この態様では、前記第１部分及び前記第２部分の間は、前記層間絶縁膜に開孔されたコンタクトホールを介して電気的に接続されてもよい。

【００１５】

このように構成すれば、副配線は、主配線を避けるようにコンタクトホールを介して交差して延びる、第１部分及び第２部分を含んでなる１本の配線として機能し得る。尚、コンタクトホール以外の方式で、これら第１部分及び第２部分の間を接続してもよい。

【００１６】

本発明の電気光学装置の他の態様では、前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、前記対向電極電位線は、前記周辺領域において、前記複数の主配線中で前記素子基板の縁寄りに位置し、前記周辺駆動回路は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに位置する。

【００１７】

この態様によれば、その動作時には、外部回路接続端子及びこれに一端が接続された主配線を介して例えば、対向電極電位が、周辺領域に設けられた上下導通端子に供給され、更に該上下導通材を介して対向基板側に設けられた対向電極へと供給される。これにより、対向電極と、例えば画素部に設けられた画素電極との間で縦電界を発生させることで、例えば両基板間に挟持された液晶等の電気光学物質を駆動できる。ここで特に、周辺領域において、対向電極電位線は、複数の主配線中で素子基板の縁寄りに位置する。例えば、対向電極電位線は外部接続端子から素子基板の縁に沿って延びる。これに対して、周辺駆動回路は上下導通端子及び対向電極電位線よりも素子基板の中央寄りに位置するので、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単

に得られる。

【００１８】

尚、好ましくは、対向電極電位線は、周辺領域において、複数の主配線中で最も素子基板の縁寄りに位置する。これにより、対向電極電位線を除く全ての主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００１９】

この態様では、前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、前記複数の外部回路接続端子のうち前記対向電極電位線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置するように構成してもよい。

【００２０】

このように構成すれば、周辺領域において、対向電極電位線は、縁寄りの外部回路接続端子から延びて、素子基板の縁寄りに位置する。従って、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが非常に簡単に得られる。

【００２１】

尚、好ましくは、対向電極電位線の一端が接続される外部回路接続端子は、周辺領域において、複数の外部回路接続端子の配列中で最も端に位置する。例えば、複数の外部回路接続端子が配列された辺から見て、右端の外部回路接続端子には、素子基板の右縁に沿って延びる対向電極電位線の先端が接続され、例えば、左端の外部回路接続端子には、素子基板の左縁に沿って延びる対向電極電位線の先端が接続される。これにより、外部回路接続端子の付近の周辺領域においても、対向電極電位線を除く全ての主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００２２】

或いは本発明の電気光学装置の他の態様では、前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間におけ

る上下導通をとるための上下導通端子を更に備えており、前記対向電極電位線は、前記周辺領域において、前記対向電極電位線を除く一又は複数の主配線よりも前記素子基板の縁寄りに位置し、前記対向電極電位線を除く他の一又は複数の主配線よりも前記素子基板の中央寄りに位置し、前記周辺駆動回路の一部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに部分的に位置し、前記周辺駆動回路の他部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の縁寄りに部分的に位置する。

【００２３】

この態様によれば、その動作時には、外部回路接続端子及びこれに一端が接続された主配線を介して例えば、対向電極電位が、周辺領域に設けられた上下導通端子に供給され、更に該上下導通材を介して対向基板側に設けられた対向電極へと供給される。ここで特に、周辺領域において、対向電極電位線は、対向電極電位線を除く一又は複数の主配線よりも素子基板の縁寄りに位置する。他方、周辺領域において、対向電極電位線は、対向電極電位線を除く他の一又は複数の主配線よりも素子基板の中央寄りに位置する。従って、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００２４】

この態様では、前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、前記複数の外部回路接続端子のうち、対向電極電位線を除く他の一又は複数の主配線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置するように構成してもよい。

【００２５】

このように構成すれば、周辺領域において、対向電極電位線を除く他の一又は複数の主配線は、縁寄りの外部回路接続端子から延びて、素子基板の縁寄りに位置する。他方、対向電極電位線を除く一又は複数の主配線は、中央寄りの外部回路接続端子から延びて、素子基板の中央寄りに位置する。従って、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが簡単に得られる。

【００２６】

上述した対向電極を備えた各種態様では、前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を夫々供給すると共に前記対向電極電位線と交差しない一対のクロック信号線を含むように構成してもよい。

【００２７】

このように構成すれば、仮に交差させると相互干渉が顕著であるクロック信号線と対向電極電位線とが、交差していないので、クロック信号の電位が対向電極電位の変動に応じて変動したり、対向電極電位がクロック信号の電位の変動に応じて変動することを効果的に回避できる。これらにより、高品位の画像表示画可能となる。

【００２８】

本発明の電気光学装置の他の態様では、前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を供給するための一対のクロック信号線と、前記電気信号として電源信号を供給するための電源配線とを含み、前記一対の信号線と前記電源配線とは交差しない。

【００２９】

この態様によれば、仮に交差させると相互干渉が顕著であるクロック信号線と電源配線とが、交差していないので、クロック信号の電位が電源信号の電位の変動に応じて変動したり、電源信号の電位がクロック信号の電位の変動に応じて変動することを効果的に回避できる。これらにより、高品位の画像表示画可能となる。

【００３０】

本発明の電気光学装置の他の態様では、前記複数の主配線は、相互に交差することを避けて蛇行するように平面レイアウトされている。

【００３１】

この態様によれば、主配線については蛇行することで、その配線長が長くなることを犠牲にしつつ、主配線が交差する事態を避ける。ここで主配線を構成する同一導電膜の抵抗を低くすることで、配線長に応じた配線抵抗は、低く抑えることが可能であり、他方、交差する際に必要な中継配線を利用しないことによる利

益を享受できる。

【００３２】

尚、この態様では好ましくは、数学的或いは幾何学的に、交差個所が極力減るように平面レイアウトし、蛇行してでも交差個所を少なくする。他方で、上述の副配線については、交差してもよいとすることで、配線ピッチを高めつつ且つ主配線についての交差を避けつつ、主配線及び副配線を周辺領域に平面レイアウトできる。

【００３３】

本発明の電気光学装置の他の態様では、前記複数の主配線は少なくとも部分的に、前記同一導電膜と別層に形成された他の導電膜からなる冗長配線を含む。

【００３４】

この態様によれば、主配線は、同一導電膜からなる配線部に加えてこれと別層に形成された他の導電膜からなる冗長配線を含むという冗長構造の採用によって、主配線の配線抵抗を、より一層低めることが可能となる。加えて、冗長構造をなす二つの配線部分のうち一方が仮に断線しても、配線としての機能を果たし得る可能性が残るので、当該電気光学装置における信頼性を向上させることも可能である。

【００３５】

本発明の電子機器は上記課題を解決するために、上述した本発明の電気光学装置（但し、その各種態様を含む）を具備してなる。

【００３６】

本発明の電子機器は、上述した本発明の電気光学装置を具備してなるので、主配線により各種電気信号が適切に供給されることで高品位の画像表示画可能である、テレビ、携帯電話、電子手帳、ワードプロセッサ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルなどの各種電子機器を実現できる。また、本発明の電子機器として、例えば電子ペーパなどの電気泳動装置を実現することも可能である。

【００３７】

本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかに

される。

【００３８】

【発明の実施の形態】

以下、本発明の実施形態を図面に基づいて説明する。以下の実施形態は、本発明の電気光学装置をＴＦＴアクティブマトリクス駆動方式の液晶装置に適用したものである。

【００３９】

（電気光学装置の全体構成）

先ず、本実施形態に係る電気光学装置の全体構成について、図１及び図２を参照して説明する。ここに、図１は、本実施形態に係る電気光学装置の全体構成を示す平面図であり、図２は、図１のＨ－Ｈ’断面図である。ここでは、電気光学装置の一例である駆動回路内蔵型のＴＦＴアクティブマトリクス駆動方式の液晶装置を例にとる。

【００４０】

図１及び図２において、本実施形態に係る電気光学装置では、ＴＦＴアレイ基板１０と対向基板２０とが対向配置されている。ＴＦＴアレイ基板１０と対向基板２０との間に液晶層５０が封入されており、ＴＦＴアレイ基板１０と対向基板２０とは、画像表示領域１０ａの周囲に位置するシール領域５２ａに設けられたシール材５２により相互に接着されている。

【００４１】

シール材５２は、両基板を貼り合わせるための、例えば光硬化性樹脂、熱硬化樹脂等からなり、製造プロセスにおいてＴＦＴアレイ基板１０上に塗布された後、紫外線照射、加熱等により硬化させられたものである。また、シール材５２中には、ＴＦＴアレイ基板１０と対向基板２０との間隔（基板間ギャップ）を所定値とするためのグラスファイバー或いはガラスビーズ等のギャップ材が散布されている。但し、このようにシール材５２中に散布するのに代えて又は加えて、特に大型の電気光学装置であれば、ギャップ材を液晶層５０中に散布してもよい。

【００４２】

シール材５２が配置されたシール領域５２ａの内側に並行して、画像表示領域

１０ａの額縁領域を規定する遮光性の額縁遮光膜５３が、対向基板２０側に設けられている。但し、このような額縁遮光膜５３の一部又は全部は、ＴＦＴアレイ基板１０側に内蔵遮光膜として設けられてもよい。

【００４３】

本実施形態においては、画像表示領域１０ａの周辺に、周辺領域が規定されている。即ち、ＴＦＴアレイ基板１０の中央から見て、額縁遮光膜５３より縁寄りが周辺領域として規定されている。

【００４４】

周辺領域のうち、シール領域５２ａの外側に位置する領域には、データ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺（即ち、図１中で下辺）に沿って設けられている。また、走査線駆動回路１０４は、この一辺に隣接する二辺（即ち、図１中で左右両辺）に沿い、且つ、額縁遮光膜５３に覆われるようにして設けられている。更に、このように画像表示領域１０ａの両側に設けられた二つの走査線駆動回路１０４間をつなぐため、ＴＦＴアレイ基板１０の残る一辺（即ち、図１中で上辺）に沿い、且つ、額縁遮光膜５３に覆われるようにして複数の配線１０５が設けられている。本実施形態では特に、周辺領域には、外部回路接続端子１０２に一端が夫々接続された複数の主配線１０８が配線されている。主配線１０８は、他端がデータ線駆動回路１０１、走査線駆動回路１０４等に接続されている。尚、これらのＴＦＴアレイ基板１０上の回路構成及びその動作、並びに主配線１０８の平面レイアウトについては後で詳述する。

【００４５】

図２において、ＴＦＴアレイ基板１０上には、画素スイッチング用のＴＦＴや走査線、データ線等の配線が形成された後の画素電極９ａ上に、配向膜が形成されている。他方、対向基板２０上には、対向電極２１の他、格子状又はストライプ状の遮光膜２３、更には最上層部分に配向膜が形成されている。また、液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなり、これら一対の配向膜間で、所定の配向状態をとる。

【００４６】

図１において、ＴＦＴアレイ基板１０の４つのコーナー付近には、ＴＦＴアレイ基板１０上に平面レイアウトされた主配線１０８のうちの１本である対向電極電位線に接続された上下導通端子１０６ｔが設けられている。これらの上下導通端子１０６ｔ上に夫々、上下導通材１０６が配置されている。上下導通材１０６は、対向電極２１の四隅に面接触しており、外部回路接続端子１０２からの対向電極電位を、主配線１０８を介して対向電極２１に供給するように構成されている。

【００４７】

（画素部の構成）

次に、本実施形態における電気光学装置の画素部における構成について、図３を参照して説明する。ここに、図３は、電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。

【００４８】

図３において、本実施形態における電気光学装置の画像表示領域１０ａ（図１参照）内にマトリクス状に形成された複数の画素部には夫々、画素電極９ａと当該画素電極９ａをスイッチング制御するためのＴＦＴ３０とが形成されており、後で詳述する画像信号Ｓ１、Ｓ２、…、Ｓｎが供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されている。

【００４９】

また、ＴＦＴ３０のゲートに走査線３ａが電気的に接続されており、所定のタイミングで、走査線３ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。

【００５０】

画素電極９ａを介して電気光学物質の一例としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板に形成された対向電極２１と

の間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能とする。ノーマリーホワイトモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が減少し、ノーマリーブラックモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が増加され、全体として電気光学装置からは画像信号に応じたコントラストをもつ光が出射する。

【００５１】

ここで保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極２１（図１及び図２参照）との間に形成される液晶容量と並列に蓄積容量７０を付加する。この蓄積容量７０は、走査線３ａに並んで設けられ、固定電位側容量電極を含むと共に所定電位とされた容量線３００を含んでいる。この蓄積容量７０によって、各画素電極における電荷保持特性は向上されている。尚、容量線３００の電位は、一つの電圧値に常時固定してもよいし、複数の電圧値に所定周期で振りつつ固定してもよい。

【００５２】

続いて、本実施形態に係る電気光学装置のＴＦＴアレイ基板上の回路構成及び主配線の平面レイアウトについて、図４を参照して説明する。ここに図４は、ＴＦＴアレイ基板上に形成された各種駆動回路、及び各種信号配線の構成を示す等価回路図である。尚、以下の説明において、外部回路接続端子１０２を介してＴＦＴアレイ基板１０内に入力される信号名称と、その信号配線とは、同一のアルファベット記号を信号及び配線Ｌの後に夫々付与して称する。即ち、例えば、信号名称である“クロック信号ＣＬＸ”に対して、その信号配線を“クロック信号線ＬＣＬＸ”と呼称することとする。

【００５３】

図４に示すように、ＴＦＴアレイ基板１０上には、電気光学装置の駆動回路として、データ線６ａに画像信号を供給する手段の一例を構成するデータ線駆動回路１０１及びサンプリング回路３０１と、走査線３ａに走査信号を供給する手段の一例を構成する走査線駆動回路１０４とが形成されている。また、これらの各駆動回路に供給される各種信号を、外部制御回路から入力するための複数の端子

を含む外部回路接続端子１０２が、ＴＦＴアレイ基板１０の一辺に沿って形成されている（図１参照）。

【００５４】

データ線駆動回路１０１は、主な構成要素として、シフトレジスタ回路１０１ａ、波形選択回路１０１ｂ及びバッファー回路１０１ｃを備える。

【００５５】

シフトレジスタ回路１０１ａは、外部制御回路から外部回路接続端子１０２並びに、主配線１０８のうち配線ＬＶＳＳＸ及び配線ＬＶＤＤＸを介して供給される負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用い、同じく外部制御回路から供給されるスタート信号ＳＰＸに応じて転送動作を開始する。続いて、外部回路接続端子１０２並びに、主配線１０８のうちクロック信号線ＬＣＬＸ及び逆位相クロック信号線ＬＣＬＸ$_{INV}$を介して供給される、シフトレジスタ回路１０１ａ用のクロック信号ＣＬＸ及び逆位相クロック信号ＣＬＸ$_{INV}$に基づき、転送信号を順次、所定タイミングで波形選択回路１０１ｂへ出力する。

【００５６】

波形選択回路１０１ｂは、“イネーブル回路”とも称され、シフトレジスタ回路１０１ａから順次出力される転送信号のパルス幅を、外部制御回路から外部回路接続端子１０２を介して入力されるイネーブル信号ＥＮＢ１～ＥＮＢ４のパルス幅に制限することにより、後述のサンプリング回路３０１における、各サンプリング期間を規定する。より具体的には、波形選択回路１０１ｂは、上述のシフトレジスタ回路１０１ａの各段に対応して設けられている、例えば、ＮＡＮＤ回路及びインバータ等により構成されており、シフトレジスタ回路１０１ａより順次出力される転送信号がハイレベルとされており、且つ、イネーブル信号ＥＮＢ１～ＥＮＢ４のいずれかがハイレベルとされているときにのみデータ線１１４が駆動されるように、時間軸上における波形の選択制御を行う。

【００５７】

バッファー回路１０１ｃは、このように波形の選択が行われた転送信号をバッファリングした後、サンプリング回路駆動信号として、サンプリング回路駆動信号線１１４を介してサンプリング回路３０１に供給する。バッファー回路１０１

ｃは、レベルシフト処理、インバーティング処理等の信号処理を行ってもよい。

【００５８】

サンプリング回路３０１は、画像信号をサンプリングするためのスイッチング回路素子の一例であるＴＦＴ２０２を複数備えて構成されている。但し、このスイッチング用回路素子としては、図に示すようにｎチャネル型のＴＦＴでもよいし、ｐチャネル型のＴＦＴでもよい。更に、相補型等のＴＦＴ等によって構成することも可能である。ＴＦＴ２０２のドレインには、上述のデータ線６ａの図３中下端が接続され、該ＴＦＴ２０２のソースには、引き出し配線１１６を介して画像信号線１１５が接続されるとともに、該ＴＦＴ２０２のゲートには、データ線駆動回路１０１に接続されたサンプリング回路駆動信号線１１４が接続されている。そして、画像信号線１１５上の画像信号ＶＩＤ１～ＶＩＤ６は、データ線駆動回路１０１からサンプリング回路駆動信号線１１４を通じてサンプリング回路駆動信号が供給されるのに応じ、サンプリング回路３０１によりサンプリングされて、各データ線６ａに供給されるように構成されている。

【００５９】

外部回路接続端子１０２から主配線１０８を経て供給され且つ上述の如くサンプリング回路３０１によりデータ線６ａに書き込まれる画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給されても構わないが、本実施形態においては、画像信号Ｓ１、Ｓ２、…、Ｓｎは、６相にシリアル－パラレル展開された画像信号ＶＩＤ１～ＶＩＤ６の夫々に対応して、６本のデータ線６ａの組に対してグループ毎に供給されるよう構成されている。尚、画像信号の相展開数に関しては、６相に限られるものでなく、例えば、９相、１２相、２４相など、複数相に展開された画像信号が、その展開数に対応した数を一組としたデータ線６ａの組に対して供給されるよう構成してもよい。

【００６０】

走査線駆動回路１０４は、構成要素としてシフトレジスタ回路（図示省略）を備える。そして、外部制御回路から外部回路接続端子１０２並びに、主配線１０８のうち配線ＬＶＳＳＹ及び配線ＬＶＤＤＹを介して供給される負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用い、同じく外部制御回路から供給されるスタ

ート信号ＳＰＹに応じて、その内蔵シフトレジスタ回路の転送動作を開始する。続いて、外部回路接続端子１０２並びに、主配線１０８のうちクロック信号線ＬＣＬＹ及び逆位相クロック信号線ＬＣＬＹ$_{INV}$を介して供給される、内蔵シフトレジスタ回路用のクロック信号ＣＬＹ及び逆位相クロック信号ＣＬＹ$_{INV}$に基づき、所定タイミングで上述の走査線３ａに走査信号をパルス的に線順次で印加する。

【００６１】

また、ＴＦＴアレイ基板１０上には、上下導通端子１０６ｔに接続され、ＴＦＴアレイ基板１０上の４つのコーナー部を通過するように、主配線１０８のうちの１本である対向電極電位線ＬＬＣＣＯＭが配線されている。そして、上下動通材１０６、上下導通端子１０６ｔ及び対向電極電位線ＬＬＣＣＯＭを介して、対向電極２１に対して所定電位が供給される。これらの電位供給によって、上述のような、画素電極９ａ及び対向電極２１の両電極間に挟持された液晶の駆動が可能となっている。

【００６２】

本実施形態では特に、走査線駆動回路１０４は、図１に示したシール領域５２ａよりも内側に配置されている。即ち、図４において４つの上下導通端子１０６ｔを通過し、画像表示領域１０ａや各種駆動回路を囲むようにＴＦＴアレイ基板１０の縁に沿って配線された対向電極電位線ＬＬＣＣＯＭよりも、ＴＦＴアレイ基板１０の中央寄りに配置されている。このように配置されることにより、走査線駆動回路１０４が、周辺領域のうちシール領域５２ａよりも外側に配置される場合と比較してＴＦＴアレイ基板１０上における周辺領域のスペースが削減され且つ装置全体の小型化を図ることとなっており、しかも対向電極電位線ＬＬＣＣＯＭ並びに走査線駆動回路１０４及びデータ線駆動回路１０１に至る各種信号配線を含む複数の主配線１０８が、相互に交差することなく平面レイアウト可能とされている。

【００６３】

（外部回路接続端子及び信号配線の配置構成）

次に、引き続き図４を参照しながら、外部回路接続端子１０２及び外部回路接

続端子１０２に接続された各種信号配線の詳細構成について以下に説明する。尚、以下の説明において、外部回路接続端子１０２を介してＴＦＴアレイ基板１０内に入力される信号名称と、その入力端子とは、同一のアルファベット記号を信号及び端子Ｔの後に夫々付与して称する。即ち、例えば、信号名称である“クロック信号ＣＬＸ”に対して、その入力端子を“端子ＴＣＬＸ”と呼称することとする。

【００６４】

上述のようにＴＦＴアレイ基板１０の一辺に沿って設けられた外部回路接続端子１０２は、対向電極電位線用、走査線駆動回路用、画像信号用、及びデータ線駆動回路用の４つの用途に大きく分類される複数の端子群を備えて構成されている。より具体的には、外部回路接続端子１０２は、対向電極電位線ＬＬＣＣＯＭ用として端子ＴＬＣＣＯＭ、走査線駆動回路１０４用として端子ＴＳＰＹ、端子ＴＶＳＳＹ、端子ＴＶＤＤＹ、端子ＴＣＬＸ及び端子ＴＣＬＸ$_{INV}$、画像信号ＶＩＤ１～ＶＩＤ６用として端子ＴＶＩＤ１～ＴＶＩＤ６、並びにデータ線駆動回路１０１用として端子ＴＶＳＳＸ、端子ＴＳＰＸ、端子ＴＶＤＤＸ、端子ＴＣＬＸ、端子ＴＣＬＸ$_{INV}$、端子ＴＥＮＢ１～ＴＥＮＢ４、及び端子ＴＶＳＳＸを備えて構成されている。

【００６５】

ここで本実施形態では特に、図４に示すように、外部回路接続端子１０２のうち、対向電極電位ＬＣＣＯＭを供給するための２つの端子ＴＬＣＣＯＭは、右端及び左端の両端に配置されている。そして、この２つの端子ＴＬＣＣＯＭに両端を接続された対向電極電位線ＬＬＣＣＯＭは、上述のように４つの上下導通端子１０６ｔに接続されて、シール領域５２ａの外周を囲むように配線されている。

【００６６】

次に、両端に配置された端子ＴＬＣＣＯＭに続いて右側から、走査線駆動回路１０４を駆動するための端子ＴＣＬＹ、端子ＴＣＬＹ$_{INV}$、端子ＴＶＤＤＹ、及び端子ＴＳＰＹが、この順に並んで配置されている。一方、左側から、同じく走査線駆動回路１０４を駆動するための端子ＴＳＰＹ及び端子ＴＶＳＳＹが、この順に並んで配置されている。

【００６７】

対向電極電位線用の端子ＴＬＣＣＯＭと走査線駆動回路１０４用の端子群とがこのような位置関係で配置構成されることにより、走査線駆動回路１０４用の端子群に接続された複数の主配線１０８、即ち、走査線駆動回路１０４を駆動するための複数の信号配線は全て、端子ＴＬＣＣＯＭに接続された対向電極電位線ＬＬＣＣＯＭよりも内側（即ち、ＴＦＴアレイ基板１０の中央寄り）を配線させることが可能となっている。即ち、本実施形態のように走査線駆動回路１０４が、シール領域５２ａよりも内側に配置されている場合において、対向電極電位線ＬＬＣＣＯＭと、上述の走査線駆動回路１０４を駆動するための信号配線群とは、基板平面上で交差することが無い。従って、対向電極電位線ＬＬＣＣＯＭと、走査線駆動回路１０４を駆動するための信号配線群とは、これらの製造工程段階において同時に形成される同一配線層として形成することが可能となっている。

【００６８】

仮に、対向電極電位線ＬＬＣＣＯＭと、走査線駆動回路１０４用の信号配線群とを、層間絶縁膜等を挟んで別々の配線層で形成することによって、平面的に見て交差させるよう構成する方法を採った場合には、特にその交差部分において夫々の信号配線から生じる信号のノイズによって互いに干渉し合う等の不具合を生じる可能性が考えられる。これに対して、上述のように本実施形態では、対向電極電位線ＬＬＣＣＯＭと走査線駆動回路１０４用の信号配線群とが、平面的に見て交差することなく、同一配線層にて形成されているため、このような不具合は未然に防止されていることとなる。

【００６９】

加えて、仮に、対向電極電位ＬＣＣＯＭを供給する外部回路接続端子１０２である端子ＴＬＣＣＯＭと走査線駆動回路１０４を駆動するための端子群とが図４に示したものと逆の位置関係に配置されていると、即ち、端子ＴＬＣＣＯＭが中央寄りであるとすると、夫々の端子に接続された配線同士を基板平面上で互いに交差させることが必要となり、いずれかの主配線１０８を、途中で別の配線層につなぎ替える等の手段を採る必要が生じる。この場合には、別々の配線層を互いに、例えば層間絶縁膜に穿設されたコンタクトホール等を介して接続するので、

製造工程の複雑化を招き、更には、このような接続箇所において特に配線抵抗が増大してしまう等の不具合が生じる可能性が高い。これに対して、本実施形態の如く図４に示したような外部回路接続端子１０２の配置構成を採ることにより、即ち、端子ＴＬＣＣＯＭを端寄りに配置することにより、対向電極電位線ＬＬＣＣＯＭ及び走査線駆動回路１０４を駆動するための複数の主配線１０８に関して、製造工程において比較的容易に形成することが可能であり、且つ、配線抵抗に起因した信号遅延等の不具合は好適に防止されていることとなる。

【００７０】

尚、走査線駆動回路１０４がシール領域５２ａよりも外側の領域に形成される場合においては、対向電極電位を供給する端子ＴＬＣＣＯＭと、走査線駆動回路１０４用の端子群とを、上述の例に対して逆に配置し、基板平面上で両者が互いに交差しないよう構成すればよい。このように構成されることにより、上述の場合と同様に、基板平面上で主配線１０８が互いに交差することが無く、つなぎ替えによる配線抵抗の増大を防止することが可能であることは言うまでも無い。

【００７１】

ここで本実施形態では好ましくは、対向電極電位線ＬＬＣＣＯＭ、及び走査線駆動回路１０４の駆動用の各主配線１０８は、アルミニウム等を含む低抵抗の金属膜或いは合金膜から構成されている。このように構成することにより、これらの信号配線の時定数を下げることができ、配線の引き廻しによる信号遅延を防止することが可能となる。加えて、主配線１０８を低抵抗の金属膜或いは合金膜から形成すれば、対向電極電位線ＬＬＣＣＯＭを含む複数或いは多数の主配線１０８を、相互に交差しないように蛇行させる構成を採ることも容易となる。即ち、蛇行により配線長が増大して、これに伴い配線抵抗は増大するが、低抵抗の金属膜或いは合金膜から形成することで、蛇行による不利益は殆ど又は全く顕在化しないで済む。逆に、蛇行させることで主配線１０８の交差を回避可能となるので、より多数の主配線１０８を限られた周辺領域内に平面レイアウトすることが可能となる。

【００７２】

更に、外部回路接続端子１０２において、走査線駆動回路１０４用の端子ＴＳ

ＰＹ及び端子ＴＶＳＳＹに続いて左側から、画像信号用の端子ＴＶＩＤ１～ＴＶＩＤ６、データ線駆動回路１０１用の端子ＴＶＳＳＸ、端子ＴＳＰＸ、端子ＴＶＤＤＸ、端子ＴＣＬＸ、端子ＴＣＬＸ$_{INV}$、端子ＴＥＮＢ１～ＴＥＮＢ４、及び端子ＴＶＳＳＸが、この順に並んで配置されている。

【００７３】

ここで、端子ＴＶＩＤ１～ＴＶＩＤ６に接続された主配線の他の一例である６本の画像信号線１１５は、夫々が互いに基板平面上で交差することなく、且つ、外部回路接続端子１０２に接続された他のいずれの信号配線とも、互いに基板平面上で交差することなく、サンプリング回路３０１とデータ線駆動回路１０１との間の領域まで配線されている。また、データ線駆動回路用の各端子に接続された複数の主配線１０８、即ち、定電位線ＶＳＳＸ及び定電位線ＶＤＤＸ、スタート信号線ＬＳＰＸ、クロック信号線ＬＣＬＸ及び逆位相クロック信号線ＬＣＬＸＩＮＶ，並びに、イネーブル信号線ＬＥＮＢ１～ＬＥＮＢ４についても、夫々が互いに基板平面上で交差することなく、且つ、外部回路接続端子１０２に接続された他のいずれの主配線１０８とも、互いに基板平面上で交差することなく、データ線駆動回路１０１へ到達するよう配線されている。

【００７４】

以上のように外部回路接続端子１０２が配置されているため、本実施形態によれば、夫々の端子に接続された複数の主配線１０８が、基板平面上で交差されること無く配線されることにより、外部回路接続端子１０２に接続された全ての主配線１０８は、これらの製造工程段階において同時に形成される同一配線層として形成することが可能となっている。このため、製造工程の簡略化を図ることが可能となる。しかも既に述べたように、交差する主配線１０８間の干渉等の不具合を未然防止することも可能であり、配線途中のコンタクトホール等で生じる接触抵抗や配線抵抗に起因した信号遅延等の不具合を未然防止することも可能である。

【００７５】

本実施形態では好ましくは、画像信号用の端子ＴＶＩＤ１～ＴＶＩＤ６は、その両側を定電位線用、或いは、低周波制御信号に属する信号配線用の端子に挟ま

れるように配置され、且つ、高周波制御信号に属する信号配線用の端子から、可能な限り離れた位置に配置される。より具体的には、図４に示すように、画像信号用の端子ＴＶＩＤ１～ＴＶＩＤ６は、定電位線用の端子ＴＶＳＳＹ及び端子ＴＶＳＳＸに挟まれるように配置されており、且つ、データ線駆動回路１０１を駆動するための高周波制御信号に属する配線用の端子ＴＣＬＸＩＮＶ、端子ＴＣＬＸ、及び端子ＴＥＮＢ１～ＴＥＮＢ４から離れた位置に配置されている。一般に、距離及び障害物の介在に応じて電磁波は減少するので、本実施形態のように配置されることにより、画像信号線１１５に対する高周波のクロックノイズ等の飛び込みを低減することが可能となる。即ち、画像信号線１１５は、高周波制御信号用の配線群から距離を離して配置されることによりノイズの影響が低減され、且つ、定電位線の介在によって高周波制御信号用配線から電気的にシールドされる形となっている。従って、ノイズの影響により画質が劣化することなく高品位な画像表示を維持することが可能となっている。

【００７６】

（画素部の詳細構成）

以下では、データ線６ａ、走査線３ａ、ＴＦＴ３０等による、上述のような回路動作が実現される電気光学装置の画素部に係る実際の構成について、図５及び図６を参照して説明する。ここに図５は、本実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であり、図６は、そのＡ－Ａ´断面図である。

【００７７】

図５において、画素電極９ａは、ＴＦＴアレイ基板１０上に、マトリクス状に複数設けられており（点線部９ａ´により輪郭が示されている）、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ及び走査線３ａが設けられている。データ線６ａは、例えばアルミニウム膜等の金属膜あるいは合金膜からなり、走査線３ａは、例えば導電性のポリシリコン膜等からなる。また、走査線３ａは、半導体層１ａのうち図中右上がりの斜線領域で示したチャネル領域１ａ´に対向するように配置されており、該走査線３ａはゲート電極として機能する。すなわち、走査線３ａとデータ線６ａとの交差する箇所にはそれぞれ、チャネル領域１ａ´

に走査線３ａの本線部がゲート電極として対向配置された画素スイッチング用のＴＦＴ３０が設けられている。

【００７８】

図６に示すように、電気光学装置は、透明なＴＦＴアレイ基板１０と、これに対向配置される透明な対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば、石英基板、ガラス基板、シリコン基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。このうち画素電極９ａは、例えばＩＴＯ（Indium Tin Oxide）膜等の透明導電性膜からなる。他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。このうち対向電極２１は、上述の画素電極９ａと同様に、例えばＩＴＯ膜等の透明導電性膜からなり、配向膜１６及び２２は、例えば、ポリイミド膜等の透明な有機膜からなる。液晶層５０は、画素電極９ａからの電界が印加されていない状態で配向膜１６及び２２により所定の配向状態をとる。

【００７９】

ＴＦＴ３０は、図６に示すように、ＬＤＤ（Lightly Doped Drain）構造を有しており、その構成要素としては、上述したようにゲート電極として機能する走査線３ａ、例えばポリシリコン膜からなり走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ´、走査線３ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁膜２、半導体層１ａにおける低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを備えている。

【００８０】

尚、ＴＦＴ３０は、好ましくは図６に示したようにＬＤＤ構造をもつが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物の打ち込みを行わないオフセット構造をもってよいし、走査線３ａの一部からなるゲート電極をマスクとして高濃度で不純物を打ち込み、自己整合的に高濃度ソース領域及び高濃度ドレ

イン領域を形成するセルフアライン型のＴＦＴであってもよい。また、本実施形態では、画素スイッチング用ＴＦＴ３０のゲート電極を、高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。このようにデュアルゲート、あるいはトリプルゲート以上でＴＦＴを構成すれば、チャネルとソース及びドレイン領域との接合部のリーク電流を防止でき、オフ時の電流を低減することができる。さらに、ＴＦＴ３０を構成する半導体層１ａは非単結晶層でも単結晶層でも構わない。単結晶層の形成には、貼り合わせ法等の公知の方法を用いることができる。半導体層１ａを単結晶層とすることで、特に周辺回路の高性能化を図ることができる。

【００８１】

一方、図６においては、蓄積容量７０が、ＴＦＴ３０の高濃度ドレイン領域１ｅ及び画素電極９ａに接続された画素電位側容量電極としての中継層７１と、固定電位側容量電極としての容量線３００の一部とが、誘電体膜７５を介して対向配置されることにより形成されている。

【００８２】

容量線３００は、例えば、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）等の高融点金属のうち少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等からなる。或いは、Ａｌ（アルミニウム）膜から形成することも可能である。

【００８３】

中継層７１は、例えば導電性のポリシリコン膜からなり画素電位側容量電極として機能する。ただし、中継層７１は、後に述べる容量線３００と同様に、金属又は合金を含む単一層膜又は多層膜から構成してもよい。中継層７１は、画素電位側容量電極としての機能のほか、コンタクトホール８３及び８５を介して、画素電極９ａとＴＦＴ３０の高濃度ドレイン領域１ｅとを中継接続する機能をもつ。

【００８４】

容量線３００は、中継層７１と対向配置された固定電位側容量電極として機能する。この容量線３００は、平面的に見ると、図５に示すように、走査線３ａの形成領域に重ねて形成されている。より具体的には容量線３００は、走査線３ａに沿って延びる本線部と、図中、データ線６ａと交差する各個所からデータ線６ａに沿って上方に夫々突出した突出部と、コンタクトホール８５に対応する個所が僅かに括れた括れ部とを備えている。このうち突出部は、走査線３ａ上の領域及びデータ線６ａ下の領域を利用して、蓄積容量７０の形成領域の増大に貢献する。また、容量線３００は、好ましくは、画素電極９ａが配置された画像表示領域１０ａからその周囲に延設され、定電位源と電気的に接続されて、固定電位とされる。このような定電位源としては、例えば、上述のようにデータ線駆動回路１０１に供給される正電源ＶＤＤＸや負電源ＶＳＳＸ等の定電位源でもよいし、対向基板２０の対向電極２１に供給される対向電極電位ＬＣＣＯＭでも構わない。

【００８５】

誘電体膜７５は、図６に示すように、例えば膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ（High Temperature Oxide）膜、ＬＴＯ（Low Temperature Oxide）膜等の酸化シリコン膜、あるいは窒化シリコン膜等から構成される。蓄積容量７０を増大させる観点からは、膜の信頼性が十分に得られる限りにおいて、誘電体膜７５は薄いほどよい。

【００８６】

図５及び図６においては、上記のほか、ＴＦＴ３０の下側に、下側遮光膜１１ａが設けられている。下側遮光膜１１ａは、格子状にパターニングされており、これにより各画素の開口領域を規定している。下側遮光膜１１ａは、前述の容量線３００と同様に、金属又は合金を含む単一層膜又は多層膜から構成される。尚、開口領域の規定は、図５中のデータ線６ａと、これに交差するよう形成された容量線３００とによっても、なされている。また、下側遮光膜１１ａについても、前述の容量線３００の場合と同様に、その電位変動がＴＦＴ３０に対して悪影響を及ぼすことを避けるために、画像表示領域からその周囲に延設して定電位源に接続するとよい。

【００８７】

また、ＴＦＴ３０下には、下地絶縁膜１２が設けられている。下地絶縁膜１２は、下側遮光膜１１ａからＴＦＴ３０を層間絶縁する機能のほか、ＴＦＴアレイ基板１０の全面に形成されることにより、ＴＦＴアレイ基板１０の表面研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用のＴＦＴ３０の特性変化を防止する機能を有する。

【００８８】

加えて、走査線３ａ上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８３がそれぞれ開孔された第１層間絶縁膜４１が形成されている。

【００８９】

第１層間絶縁膜４１上には、中継層７１、及び容量線３００が形成されており、これらの上には高濃度ソース領域１ｄへ通じるコンタクトホール８１及び中継層７１へ通じるコンタクトホール８５がそれぞれ開孔された第２層間絶縁膜４２が形成されている。

【００９０】

加えて更に、第２層間絶縁膜４２上には、データ線６ａが形成されており、これらの上には中継層７１へ通じるコンタクトホール８５が形成された第３層間絶縁膜４３が形成されている。

【００９１】

（信号配線の断面構成）

次に、図６を参照して説明した画素部の断面構造に対応させて、特に本実施形態に係る、外部回路接続端子に接続された各種信号配線の断面構成について以下に説明する。ここに、図７は、図４のＢ－Ｂ´断面図であり、図８は、図４のＣ－Ｃ´断面図である。

【００９２】

図７に示すように、外部回路接続端子１０２の複数の端子のうち、図４に示した右側半数分にあたる端子ＴＣＬＶＩＮＶ～端子ＴＬＣＣＯＭに接続された主配線１０８は全て、図６に示した第２層間絶縁膜４２上に、夫々が互いに製造工程

段階で同時に形成される同一配線層として構成されている。一方、図８に示すように、外部回路接続端子１０２の複数の端子のうち、図４に示した残りの左側半数分にあたる端子ＴＶＤＤＸ～端子ＴＬＣＣＯＭに接続された主配線１０８についても、図６に示した第２層間絶縁膜４２上に、夫々が互いに製造工程段階で同時に形成される同一配線層として構成されている。即ち、外部回路接続端子１０２に接続された全ての主配線１０８は、図６を参照して上述した第２相間絶縁膜上に形成されるデータ線６ａの配線層と、同時に形成される同一配線層として構成されている。このことは、図４に示したような順序で外部回路接続端子１０２の各端子が配列され、これらの端子に接続された主配線１０８が、基板平面上で互いに交差することなく配線されることによって実現されている。

【００９３】

以上のように、外部回路接続端子１０２に接続された各種の主配線１０８が、互いに同一配線層として構成できることにより、これらの製造工程において比較的容易に形成することが可能であり、更には、データ線６ａと同一配線層として構成できることにより、製造工程を更に簡略化させることが可能となっている。加えて、データ線６ａは、上述のように例えばアルミニウム膜等の低抵抗の金属膜あるいは合金膜からなるため、これと同時に形成される外部回路接続端子１０２に接続された各種の主配線１０８についても、低抵抗の信号配線として構成することができ、信号遅延等の不具合を防止することが可能となっている。

【００９４】

（変形形態）

次に図９及び図１０を参照して、上述した実施形態の変形形態について説明する。ここに図９及び図１０は夫々、変形形態に係る主配線及び冗長配線の断面図であり、図９は、それらの伸延方向に垂直な断面で、即ち図８と同じく図４のＣ－Ｃ’断面に対応する個所で切った断面図であり、図１０は、それらの伸延方向に沿った断面で切った断面図である。

【００９５】

図９及び図１０に示すように、変形形態では、図８と同じくアルミニウム膜等から夫々形成された複数の主配線１０８である配線ＬＶＤＤＸ、ＬＳＰＸ、ＬＶ

ＳＳＸ等は、冗長配線６００を夫々有する。冗長配線６００は、主配線１０８と別層であり、例えば高融点金属膜等の容量線３００と同一の導電膜から形成されている。また、各冗長配線６００は、平面的に見て対応する主配線１０８と重なって延びており、冗長構造をなす領域においては、主配線１０８とほぼ同様の平面レイアウトを有するように形成されている。更に、冗長配線６００は夫々、複数のコンタクトホール６０１を介して、対応する主配線１０８と電気的に接続されており、該接続された主配線１０８の冗長配線として機能する。その他の構成については、図１から図８を参照して説明した上述の実施形態と同様である。

【００９６】

従って、本変形形態によれば、冗長構造の採用によって、主配線１０８の配線抵抗を、より一層低めることが可能となる。加えて、冗長構造をなす主配線１０８と冗長配線とのうち一方が仮に断線しても、配線としての機能を果たし得る可能性が残るので、装置が欠陥品化する可能性を低減でき、製造歩留まりを向上させることも可能となる。

【００９７】

（電子機器）

次に、以上詳細に説明した電気光学装置をライトバルブとして用いた電子機器の一例たる投射型カラー表示装置の実施形態について、その全体構成、特に光学的な構成について説明する。ここに、図１１は、投射型カラー表示装置の図式的断面図である。

【００９８】

図１１において、本実施形態における投射型カラー表示装置の一例たる液晶プロジェクタ１１００は、駆動回路がＴＦＴアレイ基板上に搭載された液晶装置を含む液晶モジュールを３個用意し、それぞれＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロックミラー１１０８によって、ＲＧＢの三原色に対応する光成分Ｒ、Ｇ及びＢに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにそれ

ぞれ導かれる。この際特に、Ｂ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂによりそれぞれ変調された三原色に対応する光成分は、ダイクロックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【００９９】

本発明は、上述した実施形態に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨或いは思想に反しない範囲で適宜変更可能であり、そのような変更を伴なう電気光学装置及び電子機器もまた本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【図１】　本実施形態における電気光学装置の全体構成を示す平面図である。

【図２】　図１のＨ－Ｈ’断面図である。

【図３】　電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路図である。

【図４】　ＴＦＴアレイ基板上に形成された各種駆動回路、及び各種信号配線の構成を示す等価回路図である。

【図５】　本発明の実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。

【図６】　図５のＡ－Ａ´断面図である。

【図７】　図４のＢ－Ｂ´断面図である。

【図８】　図４のＣ－Ｃ´断面図である。

【図９】　変形形態に係る主配線及び冗長配線の一の断面図である。

【図１０】　変形形態に係る主配線及び冗長配線の他の断面図である。

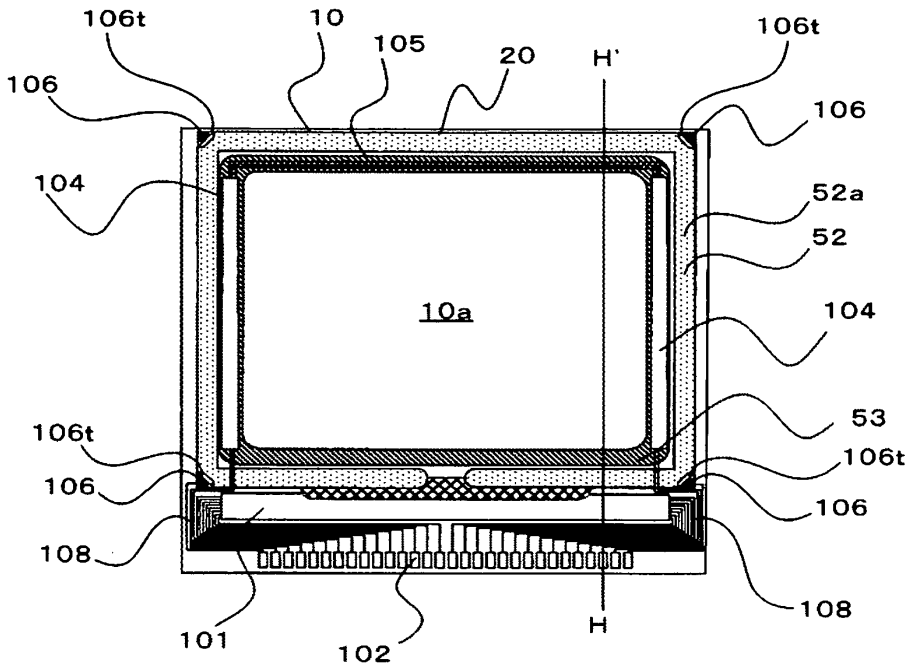
【図１１】　本発明の電子機器の実施形態である投射型カラー表示装置の一例たるカラー液晶プロジェクタを示す図式的断面図である。

【符号の説明】

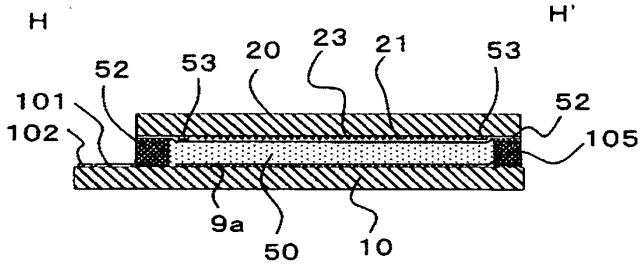
１０･･･ＴＦＴアレイ基板、１０ａ･･･画像表示領域、２０･･･対向基板、２１･･･対向電極、５０･･･液晶層、５２･･･シール材、５２ａ･･･シール領域、７０･･･蓄積容量、１０１･･･データ線駆動回路、１０２･･･外部回路接続端子、１０４･･･走査線駆動回路、１０６･･･上下導通材、１０６ｔ･･･上下導通端子、１０８･･･主配線、３００･･･容量線

【書類名】　図面

【図１】

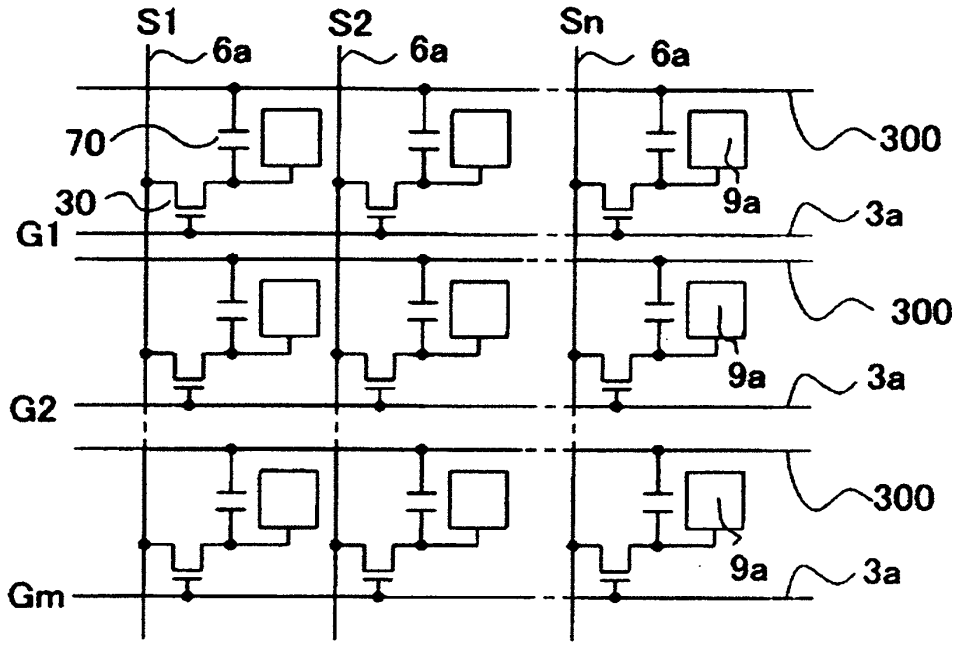


【図２】

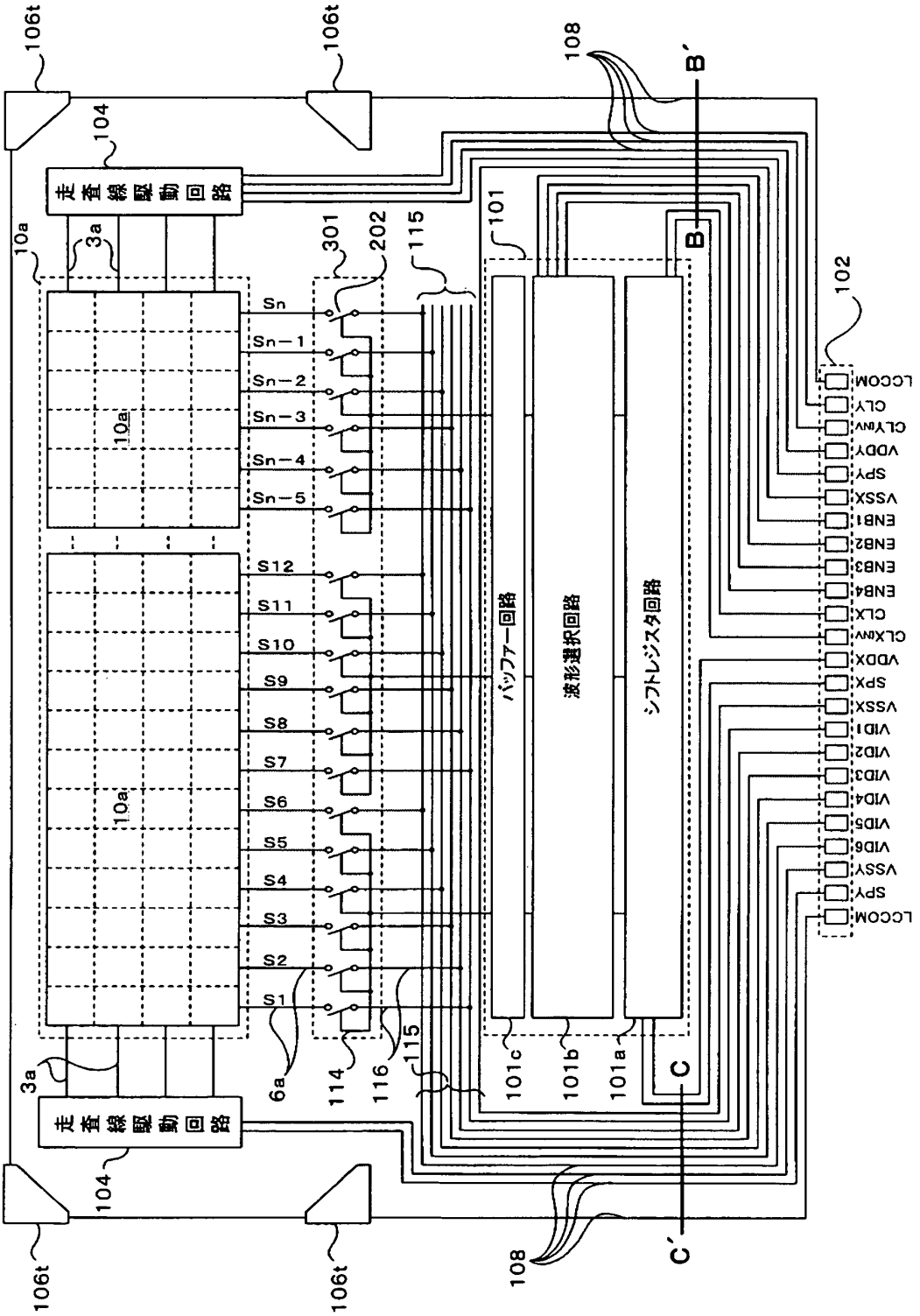


出証特２００４－３０３０２７３

【図３】

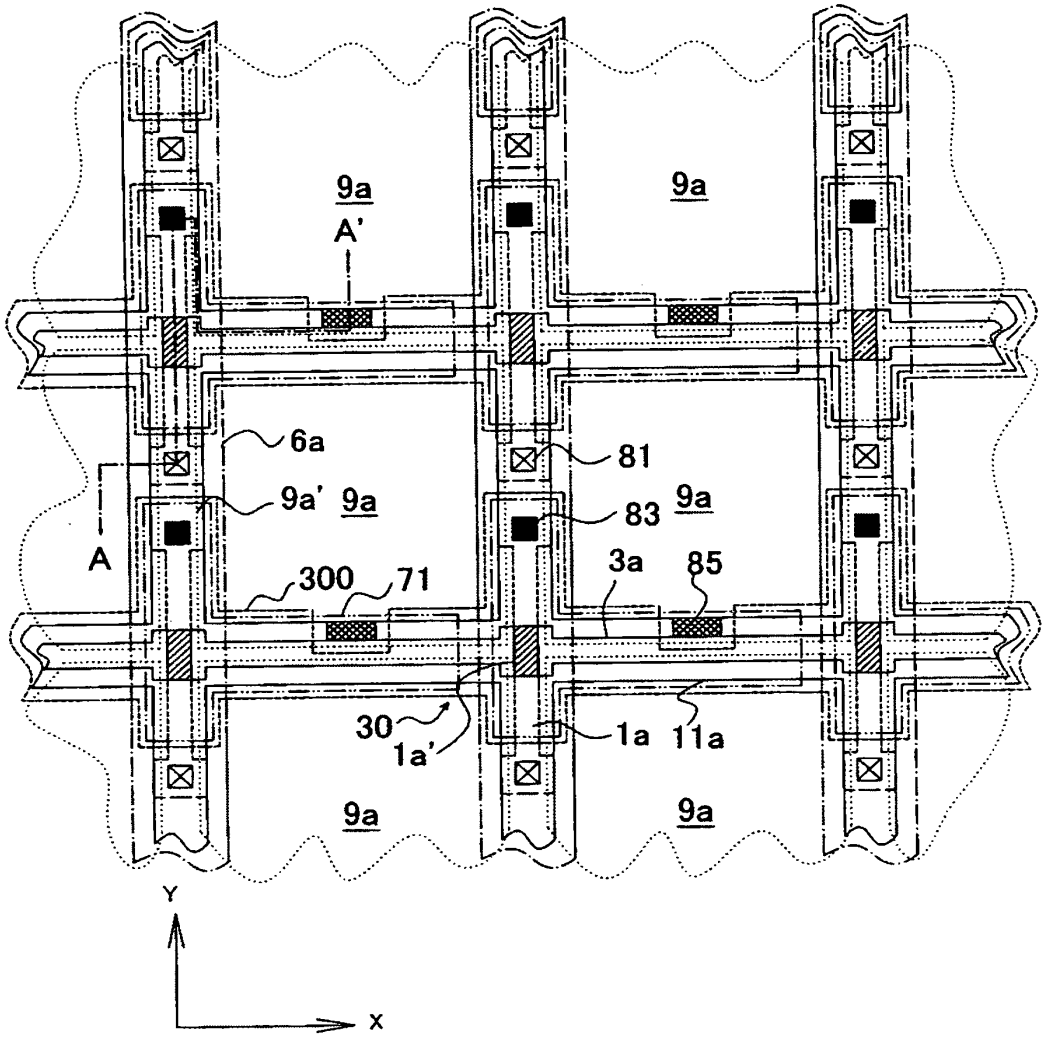


【図４】

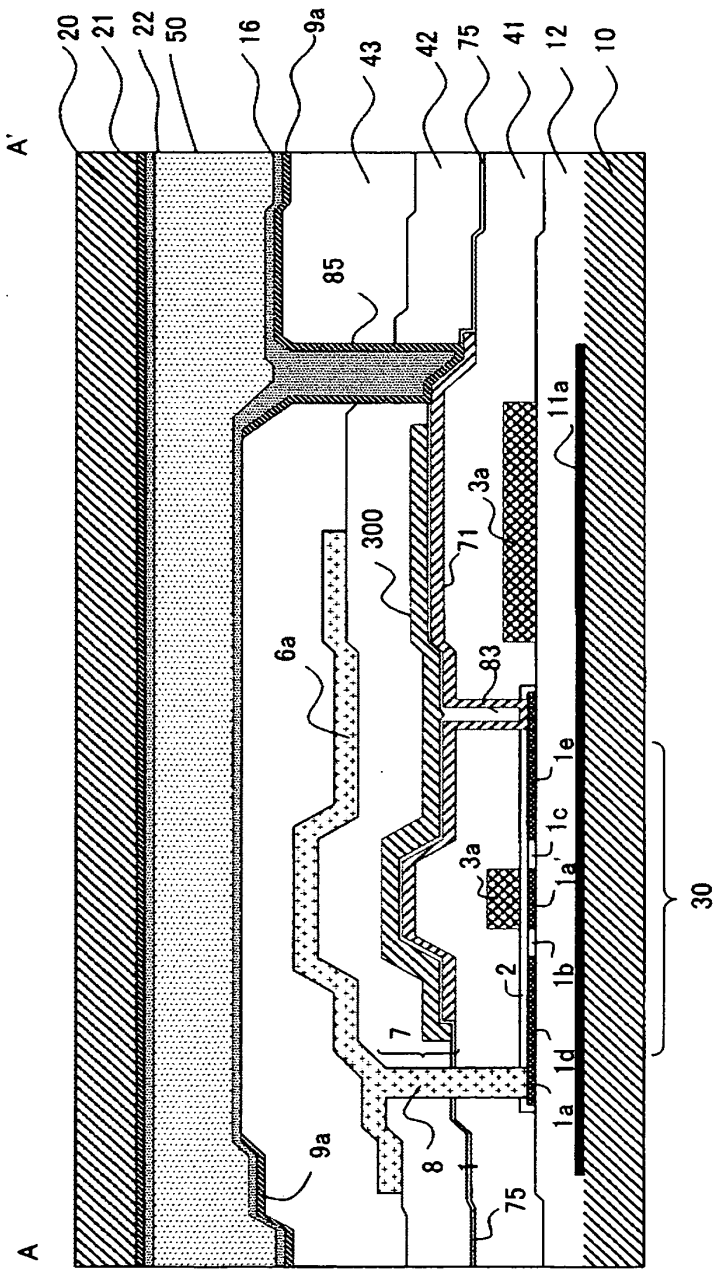


出証特２００４－３０３０２７３

【図５】

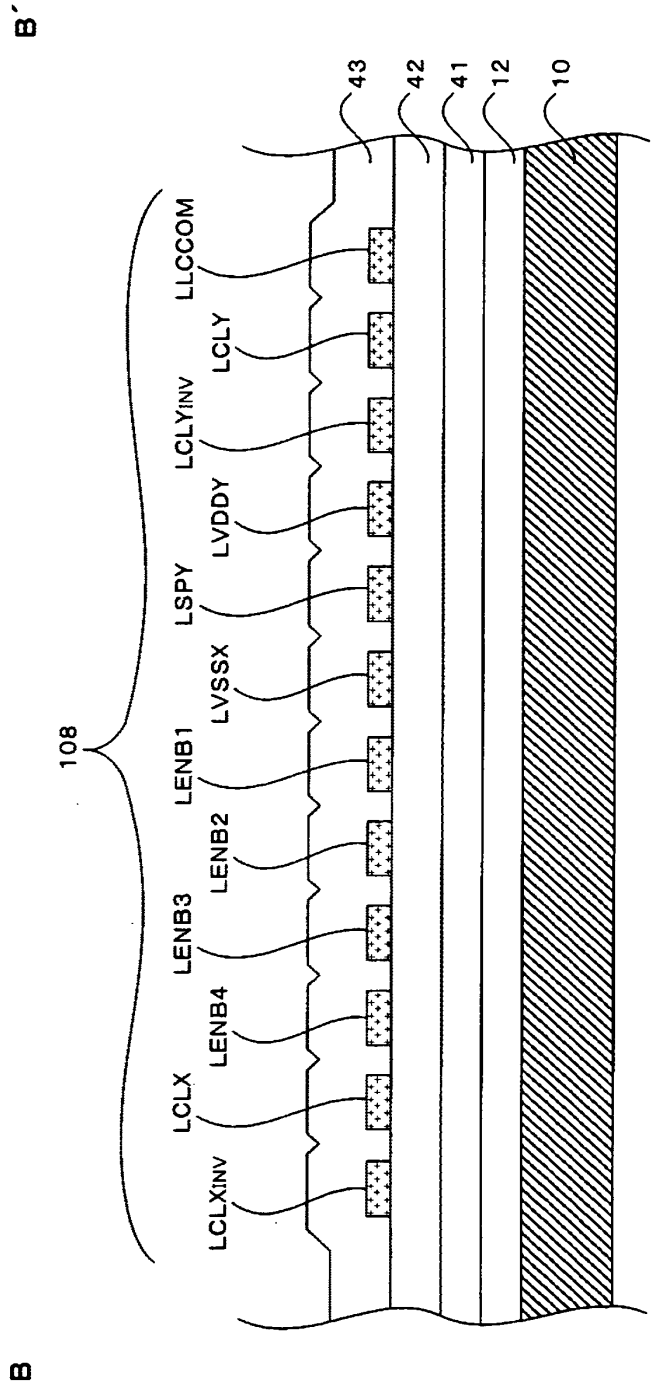


【図６】

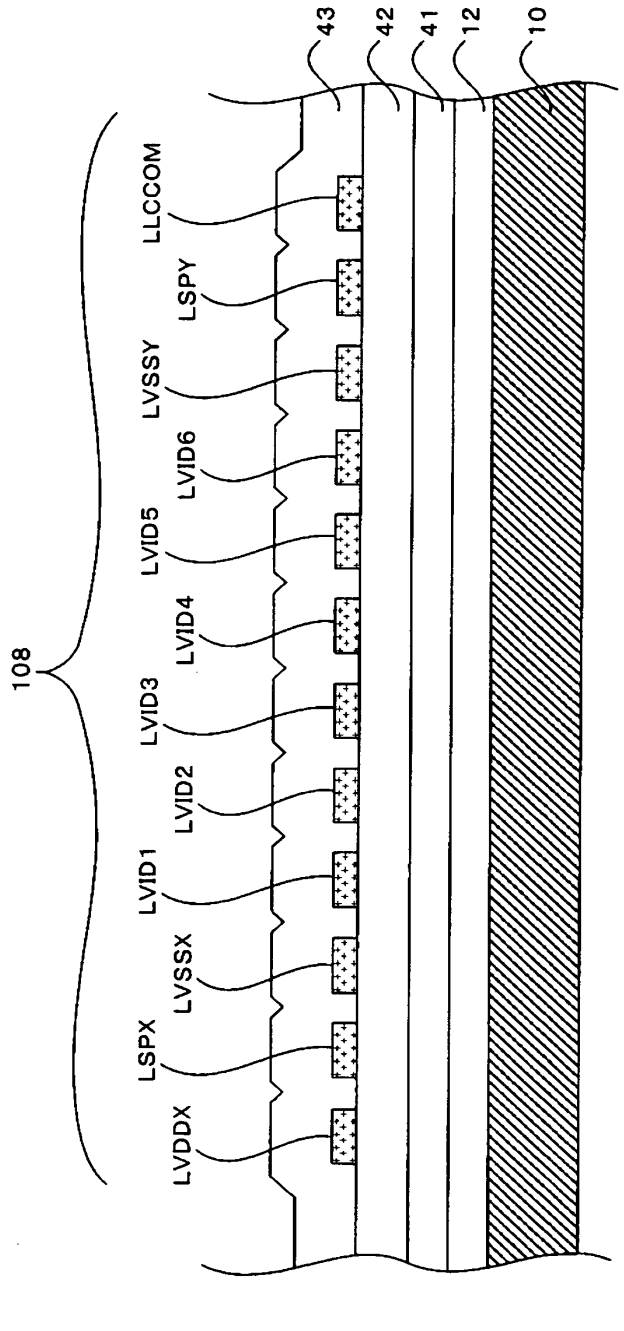


出証特２００４－３０３０２７３

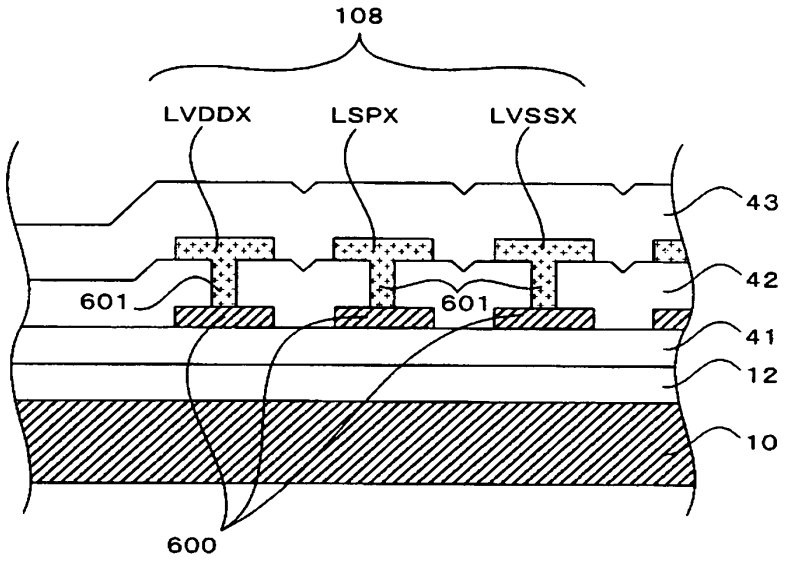
【図７】


B'
43
42
41
12
10
LLCCOM
LCLY
LCLYINV
LVDDY
LSPY
LVSSX
LENB1
LENB2
LENB3
LENB4
LCLX
LCLXINV
108
B

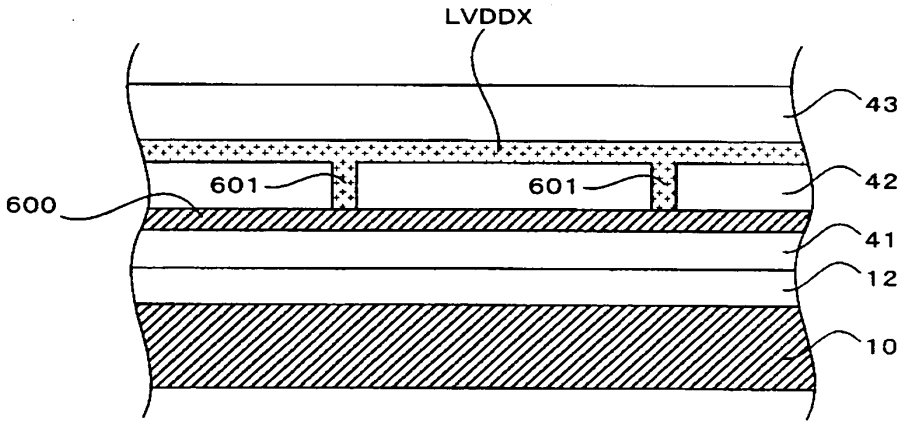
【図８】


C'
C
43
42
41
12
10
108
LLCCOM
LSPY
LVSSY
LVID6
LVID5
LVID4
LVID3
LVID2
LVID1
LVSSX
LSPX
LVDDX

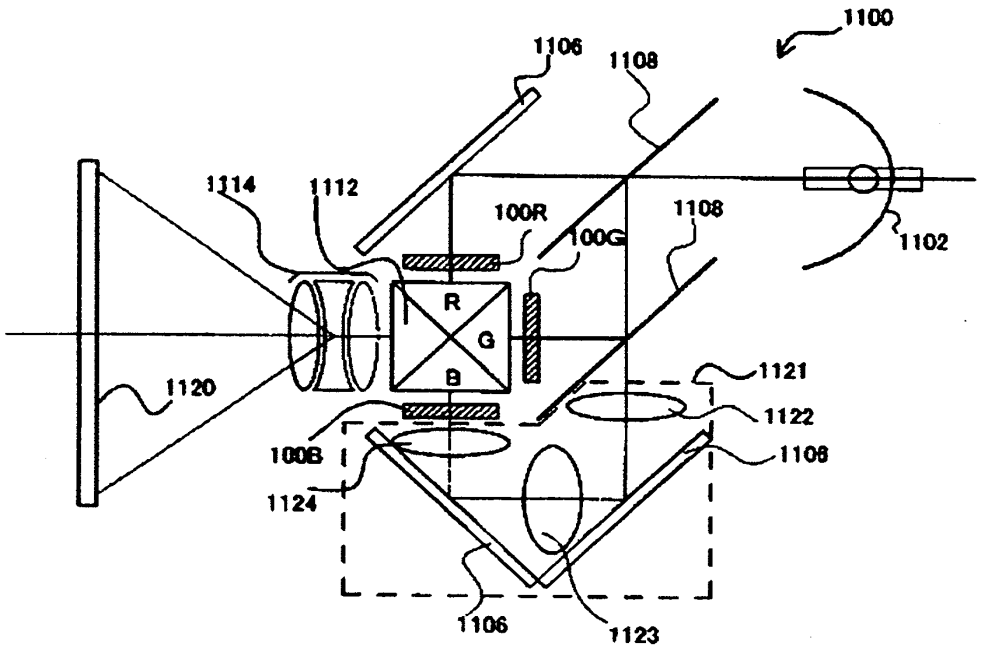
【図９】


108
LVDDX
LSPX
LVSSX
43
42
601
601
41
12
10
600

【図１０】


LVDDX
43
601
601
42
600
41
12
10

【図１１】



出証特２００４－３０３０２７３

【書類名】　　要約書

【要約】

【課題】　液晶装置等において、主配線を効率的に低抵抗化し、主配線間における信号の相互干渉を抑制することで、高品位な画像表示を行う。

【解決手段】　基板（１０）上における画像表示領域（１０ａ）の周辺に位置する周辺領域に、複数の外部回路接続端子（１０２）と、これらに夫々一端が接続された複数の主配線（１０８）と、該主配線の他端に接続されており外部回路接続端子から主配線を介して供給される電気信号に基づいて画素部を駆動するための周辺駆動回路（１０１、１０４）とを備える。複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように周辺領域内に平面レイアウトされている。

【選択図】　図４

出証特２００４－３０３０２７３

認定・付加情報

特許出願の番号	特願２００３－１５６８３２
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書類名	特許願
担当官	第四担当上席　　００９３
作成日	平成１５年　６月　３日

＜認定情報・付加情報＞

【提出日】　平成15年 6月 2日

次頁無

出証特２００４－３０３０２７３

特願２００３－１５６８３２

出　願　人　履　歴　情　報

識別番号　［０００００２３６９］

１．変更年月日　１９９０年　８月２０日
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出証番号　出証特２００４－３０３０２７３

日本国特許庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００４年　３月１９日
出願番号 Application Number: [ST. 10/C]:	特願２００４－０８１５３２ [ＪＰ２００４－０８１５３２]
出願人 Applicant(s):	セイコーエプソン株式会社

２００４年　４月１２日

特許庁長官
Commissioner,
Japan Patent Office　今井康夫

出証番号　出証特２００４－３０３０３１８

【書類名】　特許願
【整理番号】　J0108463
【提出日】　平成16年 3月19日
【あて先】　特許庁長官殿
【国際特許分類】　G09F 9/30 308
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　【氏名又は名称】　須澤　修
【先の出願に基づく優先権主張】
　【出願番号】　特願2003-156832
　【出願日】　平成15年 6月 2日
【手数料の表示】
　【予納台帳番号】　013044
　【納付金額】　21,000円
【提出物件の目録】
　【物件名】　特許請求の範囲　1
　【物件名】　明細書　1
　【物件名】　図面　1
　【物件名】　要約書　1
　【包括委任状番号】　0109826

出証特２００４－３０３０３１８

【書類名】特許請求の範囲
【請求項１】
素子基板上における画像表示領域に備えられた複数の画素部と、
前記素子基板上における前記画像表示領域の周辺に位置する周辺領域に、複数の外部回路接続端子と、該複数の外部回路接続端子に夫々一端が接続された複数の主配線と、該主配線の他端に接続されており前記外部回路接続端子から前記主配線を介して供給される電気信号に基づいて前記画素部を駆動するための周辺駆動回路とを備えており、
前記複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように前記周辺領域内に平面レイアウトされていることを特徴とする電気光学装置。
【請求項２】
前記周辺駆動回路の内部配線、前記周辺駆動回路から前記画素部に向けて引き出された引出配線、及び前記主配線から分岐した分岐配線のうち少なくとも一つを含んでなる副配線は、その第１部分において前記同一導電膜とは異なる他の導電膜から形成されて前記主配線と層間絶縁膜を介して交差するように且つその第２部分において前記同一導電膜から形成されて前記主配線と交差しないように前記周辺領域内に平面レイアウトされていることを特徴とする請求項１に記載の電気光学装置。
【請求項３】
前記第１部分及び前記第２部分の間は、前記層間絶縁膜に開孔されたコンタクトホールを介して電気的に接続されていることを特徴とする請求項２に記載の電気光学装置。
【請求項４】
前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、
前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、
前記対向電極電位線は、前記周辺領域において、前記複数の主配線中で前記素子基板の縁寄りに位置し、
前記周辺駆動回路は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに位置することを特徴とする請求項１から３のいずれか一項に記載の電気光学装置。
【請求項５】
前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、
前記複数の外部回路接続端子のうち前記対向電極電位線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置することを特徴とする請求項４に記載の電気光学装置。
【請求項６】
前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、
前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、
前記対向電極電位線は、前記周辺領域において、前記対向電極電位線を除く一又は複数の主配線よりも前記素子基板の縁寄りに位置し、前記対向電極電位線を除く他の一又は複数の主配線よりも前記素子基板の中央寄りに位置し、
前記周辺駆動回路の一部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに部分的に位置し、前記周辺駆動回路の他部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の縁寄りに部分的に位置することを特徴とする請求項１から３のいずれか一項に記載の電気光学装置。
【請求項７】

前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、
前記複数の外部回路接続端子のうち前記他の一又は複数の主配線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置することを特徴とする請求項６に記載の電気光学装置。
【請求項８】
前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を夫々供給すると共に前記対向電極電位線と交差しない一対のクロック信号線を含むことを特徴とする請求項４から７のいずれか一項に記載の電気光学装置。
【請求項９】
前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を供給するための一対のクロック信号線と、前記電気信号として電源信号を供給するための電源配線とを含み、
前記一対の信号線と前記電源配線とは交差しないことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。
【請求項１０】
前記複数の主配線は、相互に交差することを避けて蛇行するように平面レイアウトされていることを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。
【請求項１１】
前記複数の主配線は少なくとも部分的に、前記同一導電膜と別層に形成された他の導電膜からなる冗長配線を含むことを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。
【請求項１２】
素子基板上における画像表示領域に備えた複数の画素部と、
前記素子基板上における前記画像表示領域の周辺に位置する周辺領域に、複数の外部回路接続端子と、
走査線駆動回路と、
データ線駆動回路と、
前記外部回路接続端子に一端が接続され他端が前記走査線駆動回路に接続される走査線駆動回路用配線と、
前記外部回路接続端子に一端が接続され他端が前記データ線駆動回路に接続されるデータ線駆動回路用配線と、
前記外部回路接続端子に一端が接続され前記複数の画素部の画像信号を供給するための画像信号配線とを備え、
前記走査線駆動回路用配線と、前記データ線駆動回路用配線と、前記画像信号配線は、相互に交差しないように前記周辺領域内に平面レイアウトされていることを特徴とする電気光学装置。
【請求項１３】
前記画像信号配線は、前記走査線駆動回路用配線と前記データ線駆動回路用配線との間に配置されることを特徴とする請求項１２に記載の電気光学装置。
【請求項１４】
更に、前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極と、前記外部回路接続端子に一端が接続され他端が前記対向電極に対向電位を供給するための対向電極電位線とを備え、
前記対向電極電位線は、前記走査線駆動回路用配線を囲むように配置されることを特徴とする請求項１２または請求項１３に記載の電気光学装置。
【請求項１５】
請求項１から１４のいずれか一項に記載の電気光学装置を具備してなることを特徴とする電子機器。

【書類名】明細書
【発明の名称】電気光学装置及びこれを備えた電子機器
【技術分野】
【０００１】
本発明は、例えば素子基板上に周辺駆動回路が作り込まれてなる駆動回路内蔵型の液晶装置等の電気光学装置及該電気光学装置を具備してなる電子機器の技術分野に属する。
【背景技術】
【０００２】
この種の液晶装置等の電気光学装置では、その画像表示領域に、画像表示用に駆動される複数の画素部がマトリクス状に配列されている。各画素部には、例えば、画素電極と各画素電極をスイッチング制御する薄膜トランジスタ（Thin Film Transistor；以下、適宜「ＴＦＴ」という。）とが配置されており、縦横に相隣接する画素電極間の間隙に沿って走査線、データ線、容量線等の配線が設けられている。特に、駆動回路内蔵型の場合には、走査線やデータ線を駆動するための走査線駆動回路やデータ線駆動回路が、同一素子基板上における周辺領域に作り込まれている。このため、通常は、素子基板の一辺に沿って配列された複数の外部回路接続端子から周辺駆動回路に至る、電源信号線、クロック信号線、画像信号線、制御信号線等の各種配線が、周辺領域内に平面レイアウトされている。
【０００３】
ここで、電気光学装置或いは素子基板の小型化の要請に沿って、限られた周辺領域内に外部回路接続端子から周辺回路に至る多数本の各種配線が収まるように、或いは限られた周辺領域内で近接配置される各種配線間における相互ノイズが低減されるように、当該各種配線の平面レイアウトを工夫する技術も提案されている（特許文献１及び２参照）。
【０００４】
【特許文献１】特開平１１－２０２３６７号公報
【特許文献２】特開平１１－２２３８３２号公報
【発明の開示】
【発明が解決しようとする課題】
【０００５】
この種の電気光学装置では、装置或いは素子基板の小型化を図りつつも、駆動周波数向上や精細度向上による画像の高品位化の要請は、実践上極めて強い。
【０００６】
しかしながら、上述した従来の周辺領域に各種配線を設ける技術によれば、限られた周辺領域内には、複数の外部回路接続端子に一端が夫々接続された複数の配線（本願明細書では適宜「主配線」と称する）が存在している。しかも主配線の本数或いは外部回路接続端子の個数は、駆動方式の複雑高度化に伴い増大傾向にある。このため、少なくとも何本かの主配線については、その他端が周辺駆動回路や上下導通端子に至る途中で、他の主配線と交差せざるを得ない。この交差する個所では、素子基板上に構築された積層構造において当該少なくとも一つの主配線を構成する導電膜よりも下側又上側に積層された他の導電膜からなる中継配線部分を経由しなければならない。そして、通常例えばアルミニウム等の素子基板上に構築された積層構造中で最も低抵抗の導電膜から主配線は形成されることに鑑みれば、このように他の導電膜から、即ち最も低抵抗ではない導電膜から中継配線部分を形成することは、主配線における配線抵抗の増大を顕著に招くという技術的問題点がある。そして、係る主配線における配線抵抗の増大は、その主配線の用途に応じて各種の画質低下を招きかねない。
【０００７】
このように周辺領域を狭めることによる装置の小型化と画素ピッチ或いは配線ピッチの微細化による画質向上とを両立させることは、実践上極めて困難である。加えて、上述の如き中継配線部分を作ると、接触抵抗やコンタクトホール抵抗による抵抗増加、更に素子基板上における積層構造及び製造プロセスの複雑化を招き、最終的に装置歩留まりの低下や信頼性の低下を招きかねないという技術的問題点もある。

【０００８】
本発明は、例えば上記問題点に鑑みてなされたものであり、主配線を効率的に低抵抗化できると共に主配線間における信号の相互干渉を抑制でき、これらにより高品位な画像表示が可能である電気光学装置及びこのような電気光学装置を具備する電子機器を提供することを課題とする。
【課題を解決するための手段】
【０００９】
本発明の電気光学装置は上記課題を解決するために、素子基板上における画像表示領域に備えられた複数の画素部と、前記素子基板上における前記画像表示領域の周辺に位置する周辺領域に、複数の外部回路接続端子と、該複数の外部回路接続端子に夫々一端が接続された複数の主配線と、該主配線の他端に接続されており前記外部回路接続端子から前記主配線を介して供給される電気信号に基づいて前記画素部を駆動するための周辺駆動回路とを備えており、前記複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように前記周辺領域内に平面レイアウトされている。
【００１０】
本発明の電気光学装置によれば、その動作時には、外部回路接続端子及びこれに一端が接続された主配線を介して、例えば画像信号、クロック信号、その反転信号、電源信号、制御信号等の各種電気信号が夫々、主配線の他端に接続された周辺駆動回路に供給される。或いは、外部回路接続端子及びこれに一端が接続された主配線を介して例えば、対向電極電位が、周辺領域に設けられた上下導通端子に供給され、更に該上下導通材を介して対向基板側に設けられた対向電極へと供給される。このような主配線は例えば、走査線駆動回路、データ線駆動回路等である周辺駆動回路によって、上述の如く供給される各種電気信号に基づいて走査線及びデータ線が駆動されることで、所定方式による画像表示が行われる。例えば、複数の画素部がアクティブマトリクス駆動される。
【００１１】
ここで本発明の電気光学装置では特に、複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように周辺領域に平面レイアウトされている。このため、導電性に優れた導電膜を、素子基板上に構築される積層構造中に含めておき、上述した同一導電膜として採用すれば、或いは、素子基板上に構築される積層構造中で最も導電性に優れた導電膜を上述の同一導電膜として採用すれば、複数の主配線を導電性に優れた配線として構築できる。更に、主配線の本数或いは外部回路接続端子の個数が、駆動方式の複雑高度化に伴い増大しても、複数の主配線は相互に交差しないように平面レイアウトされているので、交差する個所で中継配線部分を経由させる必要性はない。そして、通常例えばアルミニウム等の素子基板上に構築された積層構造中で最も低抵抗の導電膜から主配線を形成すれば、これよりも低抵抗ではない積層構造中の他の導電膜から形成された中継配線部分を利用する場合と比較して、主配線における配線抵抗を顕著に低減できる。従って、主配線の配線抵抗の増加に起因した各種の画質低下を効果的に未然防止できる。言い換えれば、周辺領域を狭めての装置の小型化と、画素ピッチ或いは配線ピッチの微細化による画質向上とを、両立させることが可能となる。
【００１２】
加えて、上述の如く主配線中に中継配線部分を作らないので済むので、主配線における接触抵抗やコンタクトホール抵抗による抵抗増加を回避でき、更に素子基板上における積層構造及び製造プロセスを単純化できる。従って、最終的に装置歩留まりの低下や信頼性の向上が可能となる。しかも、例えば二つの主配線が薄い層間絶縁膜を介して交差する場合に見られるような該二つの主配線間における二種類の電気信号の相互干渉を、複数の主配線を相互に交差しないように平面レイアウトすることで顕著に低減することも可能となる。
【００１３】
以上の結果、本発明の電気光学装置によれば、主配線を効率的に低抵抗化できると共に主配線間における信号の相互干渉を抑制でき、これらにより高品位な画像表示が可能とな

る。

【００１４】

本発明の電気光学装置の一態様では、前記周辺駆動回路の内部配線、前記周辺駆動回路から前記画素部に向けて引き出された引出配線、及び前記主配線から分岐した分岐配線のうち少なくとも一つを含んでなる副配線は、その第１部分において前記同一導電膜とは異なる他の導電膜から形成されて前記主配線と層間絶縁膜を介して交差するように且つその第２部分において前記同一導電膜から形成されて前記主配線と交差しないように前記周辺領域内に平面レイアウトされている。

【００１５】

この態様によれば、周辺領域には、内部配線、引出配線、分岐配線等の副配線が設けられている。これらのうち、周辺駆動回路の内部配線は、周辺駆動回路内の例えばシフトレジスタを構成する複数配列された回路間をつなぐ配線である。

【００１６】

引出配線は、走査線、データ線、容量線等を画像表示領域から周辺領域へ引き出すための配線である。分岐配線は、例えば電源信号やクロック信号など、周辺駆動回路の複数箇所で共通に使用する各種電気信号を供給するための配線である。

【００１７】

このような副配線は、その第１部において、例えば最も導電性に優れた導電膜に対して層間絶縁膜を介して積層された二番目、三番目等に導電性に優れた金属膜或いは導電性ポリシリコン膜等からなり、主配線と交するように平面レイアウトされている。更に、このような副配線は、その第２部において、例えば主配線と同様に最も導電性に優れた導電膜からなり、主配線と交しないように平面レイアウトされている。従って、副配線についても主配線と抵触しない限りにおいて、その導電性を向上させることが可能である。

【００１８】

この態様では、前記第１部分及び前記第２部分の間は、前記層間絶縁膜に開孔されたコンタクトホールを介して電気的に接続されてもよい。

【００１９】

このように構成すれば、副配線は、主配線を避けるようにコンタクトホールを介して交差して延びる、第１部分及び第２部分を含んでなる１本の配線として機能し得る。尚、コンタクトホール以外の方式で、これら第１部分及び第２部分の間を接続してもよい。

【００２０】

本発明の電気光学装置の他の態様では、前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、前記対向電極電位線は、前記周辺領域において、前記複数の主配線中で前記素子基板の縁寄りに位置し、前記周辺駆動回路は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに位置する。

【００２１】

この態様によれば、その動作時には、外部回路接続端子及びこれに一端が接続された主配線を介して例えば、対向電極電位が、周辺領域に設けられた上下導通端子に供給され、更に該上下導通材を介して対向基板側に設けられた対向電極へと供給される。これにより、対向電極と、例えば画素部に設けられた画素電極との間で縦電界を発生させることで、例えば両基板間に挟持された液晶等の電気光学物質を駆動できる。ここで特に、周辺領域において、対向電極電位線は、複数の主配線中で素子基板の縁寄りに位置する。例えば、対向電極電位線は外部接続端子から素子基板の縁に沿って延びる。これに対して、周辺駆動回路は上下導通端子及び対向電極電位線よりも素子基板の中央寄りに位置するので、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００２２】

尚、好ましくは、対向電極電位線は、周辺領域において、複数の主配線中で最も素子基板の縁寄りに位置する。これにより、対向電極電位線を除く全ての主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００２３】

この態様では、前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、前記複数の外部回路接続端子のうち前記対向電極電位線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置するように構成してもよい。

【００２４】

このように構成すれば、周辺領域において、対向電極電位線は、縁寄りの外部回路接続端子から延びて、素子基板の縁寄りに位置する。従って、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが非常に簡単に得られる。

【００２５】

尚、好ましくは、対向電極電位線の一端が接続される外部回路接続端子は、周辺領域において、複数の外部回路接続端子の配列中で最も端に位置する。例えば、複数の外部回路接続端子が配列された辺から見て、右端の外部回路接続端子には、素子基板の右縁に沿って延びる対向電極電位線の先端が接続され、例えば、左端の外部回路接続端子には、素子基板の左縁に沿って延びる対向電極電位線の先端が接続される。これにより、外部回路接続端子の付近の周辺領域においても、対向電極電位線を除く全ての主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００２６】

或いは本発明の電気光学装置の他の態様では、前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極を更に備え、前記素子基板上における前記周辺領域に、前記複数の主配線のうちの少なくとも一つである前記対向電極に対向電極電位を供給するための対向電極電位線と前記対向電極との間における上下導通をとるための上下導通端子を更に備えており、前記対向電極電位線は、前記周辺領域において、前記対向電極電位線を除く一又は複数の主配線よりも前記素子基板の縁寄りに位置し、前記対向電極電位線を除く他の一又は複数の主配線よりも前記素子基板の中央寄りに位置し、前記周辺駆動回路の一部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の中央寄りに部分的に位置し、前記周辺駆動回路の他部は、前記周辺領域において、前記上下導通端子及び前記対向電極電位線よりも前記素子基板の縁寄りに部分的に位置する。

【００２７】

この態様によれば、その動作時には、外部回路接続端子及びこれに一端が接続された主配線を介して例えば、対向電極電位が、周辺領域に設けられた上下導通端子に供給され、更に該上下導通材を介して対向基板側に設けられた対向電極へと供給される。ここで特に、周辺領域において、対向電極電位線は、対向電極電位線を除く一又は複数の主配線よりも素子基板の縁寄りに位置する。他方、周辺領域において、対向電極電位線は、対向電極電位線を除く他の一又は複数の主配線よりも素子基板の中央寄りに位置する。従って、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが比較的簡単に得られる。

【００２８】

この態様では、前記複数の外部回路接続端子は、前記素子基板の一辺に沿って配列されており、前記複数の外部回路接続端子のうち、対向電極電位線を除く他の一又は複数の主配線の一端が接続される外部回路接続端子は、前記複数の外部回路接続端子の配列中で、端寄りに位置するように構成してもよい。

【００２９】

このように構成すれば、周辺領域において、対向電極電位線を除く他の一又は複数の主配線は、縁寄りの外部回路接続端子から延びて、素子基板の縁寄りに位置する。他方、対向電極電位線を除く一又は複数の主配線は、中央寄りの外部回路接続端子から延びて、素

子基板の中央寄りに位置する。従って、対向電極電位線を除く主配線と対向電極電位線とが交差しない平面レイアウトが簡単に得られる。

【００３０】

上述した対向電極を備えた各種態様では、前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を夫々供給すると共に前記対向電極電位線と交差しない一対のクロック信号線を含むように構成してもよい。

【００３１】

このように構成すれば、仮に交差させると相互干渉が顕著であるクロック信号線と対向電極電位線とが、交差していないので、クロック信号の電位が対向電極電位の変動に応じて変動したり、対向電極電位がクロック信号の電位の変動に応じて変動することを効果的に回避できる。これらにより、高品位の画像表示画可能となる。

【００３２】

本発明の電気光学装置の他の態様では、前記複数の主配線は、前記電気信号としてクロック信号及びその反転信号を供給するための一対のクロック信号線と、前記電気信号として電源信号を供給するための電源配線とを含み、前記一対の信号線と前記電源配線とは交差しない。

【００３３】

この態様によれば、仮に交差させると相互干渉が顕著であるクロック信号線と電源配線とが、交差していないので、クロック信号の電位が電源信号の電位の変動に応じて変動したり、電源信号の電位がクロック信号の電位の変動に応じて変動することを効果的に回避できる。これらにより、高品位の画像表示画可能となる。

【００３４】

本発明の電気光学装置の他の態様では、前記複数の主配線は、相互に交差することを避けて蛇行するように平面レイアウトされている。

【００３５】

この態様によれば、主配線については蛇行することで、その配線長が長くなることを犠牲にしつつ、主配線が交差する事態を避ける。ここで主配線を構成する同一導電膜の抵抗を低くすることで、配線長に応じた配線抵抗は、低く抑えることが可能であり、他方、交差する際に必要な中継配線を利用しないことによる利益を享受できる。

【００３６】

尚、この態様では好ましくは、数学的或いは幾何学的に、交差個所が極力減るように平面レイアウトし、蛇行してでも交差個所を少なくする。他方で、上述の副配線については、交差してもよいとすることで、配線ピッチを高めつつ且つ主配線についての交差を避けつつ、主配線及び副配線を周辺領域に平面レイアウトできる。

【００３７】

本発明の電気光学装置の他の態様では、前記複数の主配線は少なくとも部分的に、前記同一導電膜と別層に形成された他の導電膜からなる冗長配線を含む。

【００３８】

この態様によれば、主配線は、同一導電膜からなる配線部に加えてこれと別層に形成された他の導電膜からなる冗長配線を含むという冗長構造の採用によって、主配線の配線抵抗を、より一層低めることが可能となる。加えて、冗長構造をなす二つの配線部分のうち一方が仮に断線しても、配線としての機能を果たし得る可能性が残るので、当該電気光学装置における信頼性を向上させることも可能である。

【００３９】

また、本発明の電気光学装置は、素子基板上における画像表示領域に備えた複数の画素部と、前記素子基板上における前記画像表示領域の周辺に位置する周辺領域に、複数の外部回路接続端子と、走査線駆動回路と、データ線駆動回路と、前記外部回路接続端子に一端が接続され他端が前記走査線駆動回路に接続される走査線駆動回路用配線と、前記外部回路接続端子に一端が接続され他端が前記データ線駆動回路に接続されるデータ線駆動回路用配線と、前記外部回路接続端子に一端が接続され前記複数の画素部の画像信号を供給

するための画像信号配線とを備え、前記走査線駆動回路用配線と、前記データ線駆動回路用配線と、前記画像信号配線は、相互に交差しないように前記周辺領域内に平面レイアウトされている。

【００４０】

また、本発明の電気光学装置の一態様では、前記画像信号配線は、前記走査線駆動回路用配線と前記データ線駆動回路用配線との間に配置されるとよい。

【００４１】

また、本発明の電気光学装置の他の態様では、更に、前記素子基板に対向配置された対向基板上における前記周辺領域に対向電極と、前記外部回路接続端子に一端が接続され他端が前記対向電極に対向電位を供給するための対向電極電位線とを備え、前記対向電極電位線は、前記走査線駆動回路用配線を囲むように配置されるとよい。

【００４２】

本発明の電子機器は上記課題を解決するために、上述した本発明の電気光学装置（但し、その各種態様を含む）を具備してなる。

【００４３】

本発明の電子機器は、上述した本発明の電気光学装置を具備してなるので、主配線により各種電気信号が適切に供給されることで高品位の画像表示画可能である、テレビ、携帯電話、電子手帳、ワードプロセッサ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルなどの各種電子機器を実現できる。また、本発明の電子機器として、例えば電子ペーパなどの電気泳動装置を実現することも可能である。

【００４４】

本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにされる。

【発明を実施するための最良の形態】

【００４５】

以下、本発明の実施形態を図面に基づいて説明する。以下の実施形態は、本発明の電気光学装置をＴＦＴアクティブマトリクス駆動方式の液晶装置に適用したものである。

【００４６】

（電気光学装置の全体構成）

先ず、本実施形態に係る電気光学装置の全体構成について、図１及び図２を参照して説明する。ここに、図１は、本実施形態に係る電気光学装置の全体構成を示す平面図であり、図２は、図１のＨ－Ｈ’断面図である。ここでは、電気光学装置の一例である駆動回路内蔵型のＴＦＴアクティブマトリクス駆動方式の液晶装置を例にとる。

【００４７】

図１及び図２において、本実施形態に係る電気光学装置では、ＴＦＴアレイ基板１０と対向基板２０とが対向配置されている。ＴＦＴアレイ基板１０と対向基板２０との間に液晶層５０が封入されており、ＴＦＴアレイ基板１０と対向基板２０とは、画像表示領域１０ａの周囲に位置するシール領域５２ａに設けられたシール材５２により相互に接着されている。

【００４８】

シール材５２は、両基板を貼り合わせるための、例えば光硬化性樹脂、熱硬化樹脂等からなり、製造プロセスにおいてＴＦＴアレイ基板１０上に塗布された後、紫外線照射、加熱等により硬化させられたものである。また、シール材５２中には、ＴＦＴアレイ基板１０と対向基板２０との間隔（基板間ギャップ）を所定値とするためのグラスファイバー或いはガラスビーズ等のギャップ材が散布されている。但し、このようにシール材５２中に散布するのに代えて又は加えて、特に大型の電気光学装置であれば、ギャップ材を液晶層５０中に散布してもよい。

【００４９】

シール材５２が配置されたシール領域５２ａの内側に並行して、画像表示領域１０ａの額縁領域を規定する遮光性の額縁遮光膜５３が、対向基板２０側に設けられている。但し

、このような額縁遮光膜５３の一部又は全部は、ＴＦＴアレイ基板１０側に内蔵遮光膜として設けられてもよい。

【００５０】

本実施形態においては、画像表示領域１０ａの周辺に、周辺領域が規定されている。即ち、ＴＦＴアレイ基板１０の中央から見て、額縁遮光膜５３より縁寄りが周辺領域として規定されている。

【００５１】

周辺領域のうち、シール領域５２ａの外側に位置する領域には、データ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺（即ち、図１中で下辺）に沿って設けられている。また、走査線駆動回路１０４は、この一辺に隣接する二辺（即ち、図１中で左右両辺）に沿い、且つ、額縁遮光膜５３に覆われるようにして設けられている。更に、このように画像表示領域１０ａの両側に設けられた二つの走査線駆動回路１０４間をつなぐため、ＴＦＴアレイ基板１０の残る一辺（即ち、図１中で上辺）に沿い、且つ、額縁遮光膜５３に覆われるようにして複数の配線１０５が設けられている。本実施形態では特に、周辺領域には、外部回路接続端子１０２に一端が夫々接続された複数の主配線１０８が配線されている。主配線１０８は、他端がデータ線駆動回路１０１、走査線駆動回路１０４等に接続されている。尚、これらのＴＦＴアレイ基板１０上の回路構成及びその動作、並びに主配線１０８の平面レイアウトについては後で詳述する。

【００５２】

図２において、ＴＦＴアレイ基板１０上には、画素スイッチング用のＴＦＴや走査線、データ線等の配線が形成された後の画素電極９ａ上に、配向膜が形成されている。他方、対向基板２０上には、対向電極２１の他、格子状又はストライプ状の遮光膜２３、更には最上層部分に配向膜が形成されている。また、液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなり、これら一対の配向膜間で、所定の配向状態をとる。

【００５３】

図１において、ＴＦＴアレイ基板１０の４つのコーナー付近には、ＴＦＴアレイ基板１０上に平面レイアウトされた主配線１０８のうちの１本である対向電極電位線に接続された上下導通端子１０６ｔが設けられている。これらの上下導通端子１０６ｔ上に夫々、上下導通材１０６が配置されている。上下導通材１０６は、対向電極２１の四隅に面接触しており、外部回路接続端子１０２からの対向電極電位を、主配線１０８を介して対向電極２１に供給するように構成されている。

【００５４】

（画素部の構成）

次に、本実施形態における電気光学装置の画素部における構成について、図３を参照して説明する。ここに、図３は、電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。

【００５５】

図３において、本実施形態における電気光学装置の画像表示領域１０ａ（図１参照）内にマトリクス状に形成された複数の画素部には夫々、画素電極９ａと当該画素電極９ａをスイッチング制御するためのＴＦＴ３０とが形成されており、後で詳述する画像信号Ｓ１、Ｓ２、…、Ｓｎが供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されている。

【００５６】

また、ＴＦＴ３０のゲートに走査線３ａが電気的に接続されており、所定のタイミングで、走査線３ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを所定のタイミングで書き込む。

【００５７】
画素電極９ａを介して電気光学物質の一例としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、対向基板に形成された対向電極２１との間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能とする。ノーマリーホワイトモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が減少し、ノーマリーブラックモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が増加され、全体として電気光学装置からは画像信号に応じたコントラストをもつ光が出射する。
【００５８】
ここで保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極２１（図１及び図２参照）との間に形成される液晶容量と並列に蓄積容量７０を付加する。この蓄積容量７０は、走査線３ａに並んで設けられ、固定電位側容量電極を含むと共に所定電位とされた容量線３００を含んでいる。この蓄積容量７０によって、各画素電極における電荷保持特性は向上されている。尚、容量線３００の電位は、一つの電圧値に常時固定してもよいし、複数の電圧値に所定周期で振りつつ固定してもよい。
【００５９】
続いて、本実施形態に係る電気光学装置のＴＦＴアレイ基板上の回路構成及び主配線の平面レイアウトについて、図４及び図５を参照して説明する。ここに図４は、ＴＦＴアレイ基板上に形成された各種駆動回路、及び各種信号配線の構成を示す等価回路図である。図５は図４をさらに具体的に明示した各種駆動回路、及び各種信号配線の構成を示す等価回路図である。尚、以下の説明において、外部回路接続端子１０２を介してＴＦＴアレイ基板１０内に入力される信号名称と、その信号配線とは、同一のアルファベット記号を信号及び配線Ｌの後に夫々付与して称する。即ち、例えば、信号名称である“クロック信号ＣＬＸ”に対して、その信号配線を“クロック信号線ＬＣＬＸ”と呼称することとする。
【００６０】
図４及び図５に示すように、ＴＦＴアレイ基板１０上には、電気光学装置の駆動回路として、データ線６ａに画像信号を供給する手段の一例を構成するデータ線駆動回路１０１及びサンプリング回路３０１と、走査線３ａに走査信号を供給する手段の一例を構成する走査線駆動回路１０４とが形成されている。また、これらの各駆動回路に供給される各種信号を、外部制御回路から入力するための複数の端子を含む外部回路接続端子１０２が、ＴＦＴアレイ基板１０の一辺に沿って形成されている（図１参照）。外部回路接続端子１０２からは主配線１０８が配設される。
【００６１】
データ線駆動回路１０１は、主な構成要素として、シフトレジスタ回路１０１ａ、波形選択回路１０１ｂ及びバッファー回路１０１ｃを備える。
【００６２】
シフトレジスタ回路１０１ａは、外部制御回路から外部回路接続端子１０２並びに、主配線１０８のうち配線ＬＶＳＳＸ及び配線ＬＶＤＤＸを介して供給される負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用い、同じく外部制御回路から供給されるスタート信号ＳＰＸに応じて転送動作を開始する。続いて、外部回路接続端子１０２並びに、主配線１０８のうちクロック信号線ＬＣＬＸ及び逆位相クロック信号線$LCLX_{INV}$を介して供給される、シフトレジスタ回路１０１ａ用のクロック信号ＣＬＸ及び逆位相クロック信号CLX_{INV}に基づき、転送信号を順次、所定タイミングで波形選択回路１０１ｂへ出力する。
【００６３】
波形選択回路１０１ｂは、“イネーブル回路”とも称され、シフトレジスタ回路１０１ａから順次出力される転送信号のパルス幅を、外部制御回路から外部回路接続端子１０２を介して入力されるイネーブル信号ＥＮＢ１～ＥＮＢ４のパルス幅に制限することにより、後述のサンプリング回路３０１における、各サンプリング期間を規定する。より具体的には、波形選択回路１０１ｂは、上述のシフトレジスタ回路１０１ａの各段に対応して設

けられている、例えば、ＮＡＮＤ回路及びインバータ等により構成されており、シフトレジスタ回路１０１ａより順次出力される転送信号がハイレベルとされており、且つ、イネーブル信号ＥＮＢ１～ＥＮＢ４のいずれかがハイレベルとされているときにのみデータ線１１４が駆動されるように、時間軸上における波形の選択制御を行う。

【００６４】

バッファー回路１０１ｃは、このように波形の選択が行われた転送信号をバッファリングした後、サンプリング回路駆動信号として、サンプリング回路駆動信号線１１４を介してサンプリング回路３０１に供給する。バッファー回路１０１ｃは、レベルシフト処理、インバーティング処理等の信号処理を行ってもよい。

【００６５】

サンプリング回路３０１は、画像信号をサンプリングするためのスイッチング回路素子の一例であるＴＦＴ２０２を複数備えて構成されている。但し、このスイッチング用回路素子としては、図に示すように第１導電チャネル型のＴＦＴであり、ｎチャネル型のＴＦＴでもよいし、ｐチャネル型のＴＦＴでもよい。更に、相補型等のＴＦＴ等によって構成することも可能である。ＴＦＴ２０２のドレインには、上述のデータ線６ａの図３中下端が接続され、該ＴＦＴ２０２のソースには、引き出し配線１１６を介して画像信号線１１５が接続されるとともに、該ＴＦＴ２０２のゲートには、データ線駆動回路１０１に接続されたサンプリング回路駆動信号線１１４が接続されている。そして、画像信号線１１５上の画像信号ＶＩＤ１～ＶＩＤ６は、データ線駆動回路１０１からサンプリング回路駆動信号線１１４を通じてサンプリング回路駆動信号が供給されるのに応じ、サンプリング回路３０１によりサンプリングされて、各データ線６ａに供給されるように構成されている。

【００６６】

外部回路接続端子１０２から主配線１０８を経て供給され且つ上述の如くサンプリング回路３０１によりデータ線６ａに書き込まれる画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給されても構わないが、本実施形態においては、画像信号Ｓ１、Ｓ２、…、Ｓｎは、６相にシリアルーパラレル展開された画像信号ＶＩＤ１～ＶＩＤ６の夫々に対応して、６本のデータ線６ａの組に対してグループ毎に供給されるよう構成されている。尚、画像信号の相展開数に関しては、６相に限られるものでなく、例えば、９相、１２相、２４相など、複数相に展開された画像信号が、その展開数に対応した数を一組としたデータ線６ａの組に対して供給されるよう構成してもよい。

【００６７】

走査線駆動回路１０４は、構成要素としてシフトレジスタ回路及びバッファー回路を備える。そして、外部制御回路から外部回路接続端子１０２並びに、主配線１０８のうち配線ＬＶＳＳＹ及び配線ＬＶＤＤＹを介して供給される負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用い、同じく外部制御回路から供給されるスタート信号ＳＰＹに応じて、その内蔵シフトレジスタ回路の転送動作を開始する。続いて、外部回路接続端子１０２並びに、主配線１０８のうちクロック信号線ＬＣＬＹ及び逆位相クロック信号線$ＬＣＬＹ_{INV}$を介して供給される、内蔵シフトレジスタ回路用のクロック信号ＣＬＹ及び逆位相クロック信号$ＣＬＹ_{INV}$に基づき、所定タイミングで上述の走査線３ａに走査信号をパルス的に線順次で印加する。

【００６８】

また、ＴＦＴアレイ基板１０上には、上下導通端子１０６ｔに接続され、ＴＦＴアレイ基板１０上の４つのコーナー部を通過するように、主配線１０８のうちの１本である対向電極電位線ＬＬＣＣＯＭが配線されている。そして、上下導通材１０６、上下導通端子１０６ｔ及び対向電極電位線ＬＬＣＣＯＭを介して、対向電極２１に対して所定電位が供給される。これらの電位供給によって、上述のような、画素電極９ａ及び対向電極２１の両電極間に挟持された液晶の駆動が可能となっている。

【００６９】

本実施形態では特に、走査線駆動回路１０４は、図１に示したシール領域５２ａよりも

内側に配置されている。即ち、図４及び図５において４つの上下導通端子１０６ｔを通過し、画像表示領域１０ａや各種駆動回路を囲むようにＴＦＴアレイ基板１０の縁に沿って配線された対向電極電位線ＬＬＣＣＯＭよりも、ＴＦＴアレイ基板１０の中央寄りに配置されている。このように配置されることにより、走査線駆動回路１０４が、周辺領域のうちシール領域５２ａよりも外側に配置される場合と比較してＴＦＴアレイ基板１０上における周辺領域のスペースが削減され且つ装置全体の小型化を図ることとなっており、しかも対向電極電位線ＬＬＣＣＯＭ並びに走査線駆動回路１０４に至る各種信号配線を含む複数の主配線１０８ａの群及びデータ線駆動回路１０１に至る各種信号配線を含む複数の主配線１０８ｂの群が、相互に交差することなく平面レイアウト可能とされている。そして、走査線駆動回路１０４に至る主配線１０８ａに群の間でも相互に交差することなく平面レイアウト可能とされている。また、データ線駆動回路１０１に至る主配線１０８ｂの群の間でも、シフトレジスタ１０１ａや、波形整形回路１０１ｂ、バッファー回路１０１ｃに接続するために必要な交差部を除いて、相互に交差することなく平面レイアウト可能とされている。また、サンプリング回路３０１に至る主配線１０８ｃ、すなわち画像信号線１１５は、サンプリング回路３０１に接続するために必要な交差部を除いて、相互に交差することなく平面レイアウト可能とされている。

【００７０】

（外部回路接続端子及び信号配線の配置構成）

次に、引き続き図４及び図５を参照しながら、外部回路接続端子１０２及び外部回路接続端子１０２に接続された各種信号配線の詳細構成について以下に説明する。尚、以下の説明において、外部回路接続端子１０２を介してＴＦＴアレイ基板１０内に入力される信号名称と、その入力端子とは、同一のアルファベット記号を信号及び端子Ｔの後に夫々付与して称する。即ち、例えば、信号名称である“クロック信号ＣＬＸ”に対して、その入力端子を“端子ＴＣＬＸ”と呼称することとする。

【００７１】

上述のようにＴＦＴアレイ基板１０の一辺に沿って設けられた外部回路接続端子１０２は、対向電極電位線用、走査線駆動回路用、画像信号用、及びデータ線駆動回路用の４つの用途に大きく分類される複数の端子群を備えて構成されている。より具体的には、外部回路接続端子１０２は、対向電極電位線ＬＬＣＣＯＭ用として端子ＴＬＣＣＯＭ、走査線駆動回路１０４用として端子ＴＳＰＹ、端子ＴＶＳＳＹ、端子ＴＶＤＤＹ、端子ＴＣＬＸ及び端子ＴＣＬＸ$_{INV}$、画像信号ＶＩＤ１～ＶＩＤ６用として端子ＴＶＩＤ１～ＴＶＩＤ６、並びにデータ線駆動回路１０１用として端子ＴＶＳＳＸ、端子ＴＳＰＸ、端子ＴＶＤＤＸ、端子ＴＣＬＸ、端子ＴＣＬＸ$_{INV}$、端子ＴＥＮＢ１～ＴＥＮＢ４、及び端子ＴＶＳＳＸを備えて構成されている。

【００７２】

ここで本実施形態では特に、図４及び図５に示すように、外部回路接続端子１０２のうち、対向電極電位ＬＣＣＯＭを供給するための２つの端子ＴＬＣＣＯＭは、右端及び左端の両端に配置されている。そして、この２つの端子ＴＬＣＣＯＭに両端を接続された対向電極電位線ＬＬＣＣＯＭは、上述のように４つの上下導通端子１０６ｔに接続されて、シール領域５２ａの外周を囲むように配線されている。なお、上下導通端子１０６ｔは１つでも良い。

【００７３】

次に、両端に配置された端子ＴＬＣＣＯＭに続いて右側から、走査線駆動回路１０４を駆動するための端子ＴＣＬＹ、端子ＴＣＬＹ$_{INV}$、端子ＴＶＤＤＹ、及び端子ＴＳＰＹが、この順に並んで配置されている。一方、左側から、同じく走査線駆動回路１０４を駆動するための端子ＴＳＰＹ及び端子ＴＶＳＳＹが、この順に並んで配置されている。

【００７４】

対向電極電位線用の端子ＴＬＣＣＯＭと走査線駆動回路１０４用の端子群とがこのような位置関係で配置構成されることにより、走査線駆動回路１０４用の端子群に接続された複数の主配線１０８ａ、即ち、走査線駆動回路１０４を駆動するための複数の信号配線は

全て、端子ＴＬＣＣＯＭに接続された対向電極電位線ＬＬＣＣＯＭよりも内側（即ち、ＴＦＴアレイ基板１０の中央寄り）を配線させることが可能となっている。そして、図５に示すように、クロック信号線ＬＣＬＹ、逆位相クロック信号線ＬＣＬＹＩＮＶ、定電位線である配線ＬＶＤＤＹは、図上、右側より、左右の走査線駆動回路１０４に電気的に接続されるように、右側の走査線駆動回路１０４及び左側の走査線駆動回路１０４の外側で、かつ対向電極電位線ＬＬＣＣＯＭの内側に沿って配置されている。即ち、本実施形態のように走査線駆動回路１０４が、シール領域５２ａよりも内側に配置されている場合において、対向電極電位線ＬＬＣＣＯＭと、上述の走査線駆動回路１０４を駆動するための信号配線群とは、基板平面上で交差することが無い。従って、対向電極電位線ＬＬＣＣＯＭと、走査線駆動回路１０４を駆動するための信号配線群１０８ａとは、これらの製造工程段階において同時に形成される同一配線層として形成することが可能となっている。

【００７５】

仮に、対向電極電位線ＬＬＣＣＯＭと、走査線駆動回路１０４用の信号配線群とを、層間絶縁膜等を挟んで別々の配線層で形成することによって、平面的に見て交差させるよう構成する方法を採った場合には、特にその交差部分において夫々の信号配線から生じる信号のノイズによって互いに干渉し合う等の不具合を生じる可能性が考えられる。これに対して、上述のように本実施形態では、対向電極電位線ＬＬＣＣＯＭと走査線駆動回路１０４用の信号配線群とが、平面的に見て交差することなく、同一配線層にて形成されているため、このような不具合は未然に防止されていることとなる。

【００７６】

加えて、仮に、対向電極電位ＬＣＣＯＭを供給する外部回路接続端子１０２である端子ＴＬＣＣＯＭと走査線駆動回路１０４を駆動するための端子群とが図４または図５に示したものと逆の位置関係に配置されていると、即ち、端子ＴＬＣＣＯＭが中央寄りであるとすると、夫々の端子に接続された配線同士を基板平面上で互いに交差させることが必要となり、いずれかの主配線１０８を、途中で別の配線層につなぎ替える等の手段を採る必要が生じる。この場合には、別々の配線層を互いに、例えば層間絶縁膜に穿設されたコンタクトホール等を介して接続するので、製造工程の複雑化を招き、更には、このような接続箇所において特に配線抵抗が増大してしまう等の不具合が生じる可能性が高い。これに対して、本実施形態の如く図４及び図５に示したような外部回路接続端子１０２の配置構成を採ることにより、即ち、端子ＴＬＣＣＯＭを端寄りに配置することにより、対向電極電位線ＬＬＣＣＯＭ及び走査線駆動回路１０４を駆動するための複数の主配線１０８ａに関して、製造工程において比較的容易に形成することが可能であり、且つ、配線抵抗に起因した信号遅延等の不具合は好適に防止されていることとなる。

【００７７】

尚、走査線駆動回路１０４がシール領域５２ａよりも外側の領域に形成される場合においては、対向電極電位を供給する端子ＴＬＣＣＯＭと、走査線駆動回路１０４用の端子群とを、上述の例に対して逆に配置し、基板平面上で両者が互いに交差しないよう構成すればよい。このように構成されることにより、上述の場合と同様に、基板平面上で主配線１０８が互いに交差することが無く、つなぎ替えによる配線抵抗の増大を防止することが可能であることは言うまでも無い。

【００７８】

ここで本実施形態では好ましくは、対向電極電位線ＬＬＣＣＯＭ、及び走査線駆動回路１０４の駆動用の各主配線１０８ａは、アルミニウム等を含む低抵抗の金属膜或いは合金膜から構成されている。このように構成することにより、これらの信号配線の時定数を下げることができ、配線の引き廻しによる信号遅延を防止することが可能となる。加えて、主配線１０８ａを低抵抗の金属膜或いは合金膜から形成すれば、対向電極電位線ＬＬＣＣＯＭを含む複数或いは多数の主配線１０８を、相互に交差しないように蛇行させる構成を採ることも容易となる。即ち、蛇行により配線長が増大して、これに伴い配線抵抗は増大するが、低抵抗の金属膜或いは合金膜から形成することで、蛇行による不利益は殆ど又は全く顕在化しないで済む。逆に、蛇行させることで主配線１０８の交差を回避可能となる

ので、より多数の主配線１０８を限られた周辺領域内に平面レイアウトすることが可能となる。

【００７９】

更に、外部回路接続端子１０２において、走査線駆動回路１０４用の端子ＴＳＰＹ及び端子ＴＶＳＳＹに続いて左側から、画像信号用の端子ＴＶＩＤ１～ＴＶＩＤ６、データ線駆動回路１０１用の端子ＴＶＳＳＸ、端子ＴＳＰＸ、端子ＴＶＤＤＸ、端子ＴＣＬＸ、端子ＴＣＬＸ$_{INV}$、端子ＴＥＮＢ１～ＴＥＮＢ４、及び端子ＴＶＳＳＸが、この順に並んで配置されている。

【００８０】

ここで、端子ＴＶＩＤ１～ＴＶＩＤ６に接続された主配線１０８ｃである６本の画像信号線１１５は、夫々が互いに基板平面上で交差することなく、且つ、外部回路接続端子１０２に接続された他のいずれの信号配線とも、互いに基板平面上で交差することなく、サンプリング回路３０１とデータ線駆動回路１０１との間の領域まで配線されている。具体的には、画像信号線１１５は、走査線駆動回路１０４の駆動用の主配線１０８ａの配線ＬＶＳＳＹとデータ線駆動回路１０１の駆動用の主配線１０８ｂの配線ＬＶＳＳＸとの間に配置されている。そして、各画像信号線１１５は各サンプリング回路３０１に電気的に接続するために、引き出し配線１１６と図示しないコンタクトホールを介して接続される。そして、引き出し配線１１６は他の画像信号線１１５と相互に交差して配置される。

【００８１】

また、データ線駆動回路用の各端子に接続された複数の主配線１０８ｂ、即ち、定電位線である配線ＬＶＳＳＸ及び定電位線である配線ＬＶＤＤＸ、スタート信号線ＬＳＰＸ、クロック信号線ＬＣＬＸ及び逆位相クロック信号線ＬＣＬＸ$_{INV}$，並びに、イネーブル信号線ＬＥＮＢ１～ＬＥＮＢ４についても、夫々が互いに基板平面上で交差することなく、且つ、外部回路接続端子１０２に接続された他のいずれの主配線１０８とも、互いに基板平面上で交差することなく、データ線駆動回路１０１へ到達するよう配線されている。具体的には、配線ＬＶＳＳＸは、主配線１０８ａ及び主配線１０８ｃの内側で、かつデータ線駆動回路１０１を囲むように配置される。そして、他の主配線１０８ｂであるスタート信号線ＬＳＰＸ、クロック信号線ＬＣＬＸ及び逆位相クロック信号線ＬＣＬＸ$_{INV}$，並びに、イネーブル信号線ＬＥＮＢ１～ＬＥＮＢ４は、配線ＬＶＳＳＸの内側に配置されている。そして、データ線駆動回路１０１のシフトレジスタ１０１ａ、波形整形回路１０１ｂ、バッファー回路１０１ｃに電気的な接続のためにコンタクトホールを介して引き出し配線と接続される。そして、引き出し配線は他の主配線１０８ｂと相互に交差して配置される。

【００８２】

以上のように外部回路接続端子１０２が配置されているため、本実施形態によれば、夫々の端子に接続された複数の主配線１０８が、基板平面上で交差されること無く配線されることにより、外部回路接続端子１０２に接続された全ての主配線１０８は、これらの製造工程段階において同時に形成される同一配線層として形成することが可能となっている。このため、製造工程の簡略化を図ることが可能となる。しかも既に述べたように、交差する主配線１０８間の干渉等の不具合を未然防止することも可能であり、配線途中のコンタクトホール等で生じる接触抵抗や配線抵抗に起因した信号遅延等の不具合を未然防止することも可能である。

【００８３】

本実施形態では好ましくは、画像信号用の端子ＴＶＩＤ１～ＴＶＩＤ６は、その両側を定電位線用、或いは、低周波制御信号に属する信号配線用の端子に挟まれるように配置され、且つ、高周波制御信号に属する信号配線用の端子から、可能な限り離れた位置に配置される。より具体的には、図４又は図５に示すように、画像信号用の端子ＴＶＩＤ１～ＴＶＩＤ６は、定電位線用の端子ＴＶＳＳＹ及び端子ＴＶＳＳＸに挟まれるように配置されており、且つ、データ線駆動回路１０１を駆動するための高周波制御信号に属する配線用の端子ＴＣＬＸ$_{INV}$、端子ＴＣＬＸ、及び端子ＴＥＮＢ１～ＴＥＮＢ４から離れた位置

に配置されている。一般に、距離及び障害物の介在に応じて電磁波は減少するので、本実施形態のように配置されることにより、画像信号線１１５に対する高周波のクロックノイズ等の飛び込みを低減することが可能となる。即ち、画像信号線１１５は、高周波制御信号用の配線群から距離を離して配置されることによりノイズの影響が低減され、且つ、定電位線の介在によって高周波制御信号用配線から電気的にシールドされる形となっている。従って、ノイズの影響により画質が劣化することなく高品位な画像表示を維持することが可能となっている。

【００８４】

（画素部の詳細構成）

以下では、データ線６ａ、走査線３ａ、ＴＦＴ３０等による、上述のような回路動作が実現される電気光学装置の画素部に係る実際の構成について、図６及び図７を参照して説明する。ここに図６は、本実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であり、図７は、そのＡ－Ａ´断面図である。

【００８５】

図６において、画素電極９ａは、ＴＦＴアレイ基板１０上に、マトリクス状に複数設けられており（点線部９ａ´により輪郭が示されている）、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ及び走査線３ａが設けられている。データ線６ａは、例えばアルミニウム膜等の金属膜あるいは合金膜からなり、走査線３ａは、例えば導電性のポリシリコン膜等からなる。また、走査線３ａは、半導体層１ａのうち図中右上がりの斜線領域で示したチャネル領域１ａ´に対向するように配置されており、該走査線３ａはゲート電極として機能する。すなわち、走査線３ａとデータ線６ａとの交差する箇所にはそれぞれ、チャネル領域１ａ´に走査線３ａの本線部がゲート電極として対向配置された画素スイッチング用のＴＦＴ３０が設けられている。

【００８６】

図７に示すように、電気光学装置は、透明なＴＦＴアレイ基板１０と、これに対向配置される透明な対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば、石英基板、ガラス基板、シリコン基板からなり、対向基板２０は、例えばガラス基板や石英基板からなる。ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。このうち画素電極９ａは、例えばＩＴＯ（Indium Tin Oxide）膜等の透明導電性膜からなる。他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。このうち対向電極２１は、上述の画素電極９ａと同様に、例えばＩＴＯ膜等の透明導電性膜からなり、配向膜１６及び２２は、例えば、ポリイミド膜等の透明な有機膜からなる。液晶層５０は、画素電極９ａからの電界が印加されていない状態で配向膜１６及び２２により所定の配向状態をとる。

【００８７】

ＴＦＴ３０は、図７に示すように、ＬＤＤ（Lightly Doped Drain）構造を有しており、その構成要素としては、上述したようにゲート電極として機能する走査線３ａ、例えばポリシリコン膜からなり走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ´、走査線３ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁膜２、半導体層１ａにおける低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを備えている。

【００８８】

尚、ＴＦＴ３０は、好ましくは図７に示したようにＬＤＤ構造をもつが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物の打ち込みを行わないオフセット構造をもってよいし、走査線３ａの一部からなるゲート電極をマスクとして高濃度で不純物を打ち込み、自己整合的に高濃度ソース領域及び高濃度ドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。また、本実施形態では、画素スイッチング用ＴＦＴ３０のゲ

ート電極を、高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。このようにデュアルゲート、あるいはトリプルゲート以上でＴＦＴを構成すれば、チャネルとソース及びドレイン領域との接合部のリーク電流を防止でき、オフ時の電流を低減することができる。さらに、ＴＦＴ３０を構成する半導体層１ａは非単結晶層でも単結晶層でも構わない。単結晶層の形成には、貼り合わせ法等の公知の方法を用いることができる。半導体層１ａを単結晶層とすることで、特に周辺回路の高性能化を図ることができる。

【００８９】

一方、図７においては、蓄積容量７０が、ＴＦＴ３０の高濃度ドレイン領域１ｅ及び画素電極９ａに接続された画素電位側容量電極としての中継層７１と、固定電位側容量電極としての容量線３００の一部とが、誘電体膜７５を介して対向配置されることにより形成されている。

【００９０】

容量線３００は、例えば、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）等の高融点金属のうち少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等からなる。或いは、Ａｌ（アルミニウム）膜から形成することも可能である。

【００９１】

中継層７１は、例えば導電性のポリシリコン膜からなり画素電位側容量電極として機能する。ただし、中継層７１は、後に述べる容量線３００と同様に、金属又は合金を含む単一層膜又は多層膜から構成してもよい。中継層７１は、画素電位側容量電極としての機能のほか、コンタクトホール８３及び８５を介して、画素電極９ａとＴＦＴ３０の高濃度ドレイン領域１ｅとを中継接続する機能をもつ。

【００９２】

容量線３００は、中継層７１と対向配置された固定電位側容量電極として機能する。この容量線３００は、平面的に見ると、図６に示すように、走査線３ａの形成領域に重ねて形成されている。より具体的には容量線３００は、走査線３ａに沿って延びる本線部と、図中、データ線６ａと交差する各個所からデータ線６ａに沿って上方に夫々突出した突出部と、コンタクトホール８５に対応する個所が僅かに括れた括れ部とを備えている。このうち突出部は、走査線３ａ上の領域及びデータ線６ａ下の領域を利用して、蓄積容量７０の形成領域の増大に貢献する。また、容量線３００は、好ましくは、画素電極９ａが配置された画像表示領域１０ａからその周囲に延設され、定電位源と電気的に接続されて、固定電位とされる。このような定電位源としては、例えば、上述のようにデータ線駆動回路１０１に供給される正電源ＶＤＤＸや負電源ＶＳＳＸ等の定電位源でもよいし、対向基板２０の対向電極２１に供給される対向電極電位ＬＣＣＯＭでも構わない。

【００９３】

誘電体膜７５は、図７に示すように、例えば膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ（High Temperature Oxide）膜、ＬＴＯ（Low Temperature Oxide）膜等の酸化シリコン膜、あるいは窒化シリコン膜等から構成される。蓄積容量７０を増大させる観点からは、膜の信頼性が十分に得られる限りにおいて、誘電体膜７５は薄いほどよい。

【００９４】

図６及び図７においては、上記のほか、ＴＦＴ３０の下側に、下側遮光膜１１ａが設けられている。下側遮光膜１１ａは、格子状にパターニングされており、これにより各画素の開口領域を規定している。下側遮光膜１１ａは、前述の容量線３００と同様に、金属又は合金を含む単一層膜又は多層膜から構成される。尚、開口領域の規定は、図６中のデータ線６ａと、これに交差するよう形成された容量線３００とによっても、なされている。また、下側遮光膜１１ａについても、前述の容量線３００の場合と同様に、その電位変動がＴＦＴ３０に対して悪影響を及ぼすことを避けるために、画像表示領域からその周囲に延設して定電位源に接続するとよい。

【００９５】

また、ＴＦＴ３０下には、下地絶縁膜１２が設けられている。下地絶縁膜１２は、下側遮光膜１１ａからＴＦＴ３０を層間絶縁する機能のほか、ＴＦＴアレイ基板１０の全面に形成されることにより、ＴＦＴアレイ基板１０の表面研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用のＴＦＴ３０の特性変化を防止する機能を有する。

【００９６】

加えて、走査線３ａ上には、高濃度ソース領域１ｄへ通じるコンタクトホール８１及び高濃度ドレイン領域１ｅへ通じるコンタクトホール８３がそれぞれ開孔された第１層間絶縁膜４１が形成されている。

【００９７】

第１層間絶縁膜４１上には、中継層７１、及び容量線３００が形成されており、これらの上には高濃度ソース領域１ｄへ通じるコンタクトホール８１及び中継層７１へ通じるコンタクトホール８５がそれぞれ開孔された第２層間絶縁膜４２が形成されている。

【００９８】

加えて更に、第２層間絶縁膜４２上には、データ線６ａが形成されており、これらの上には中継層７１へ通じるコンタクトホール８５が形成された第３層間絶縁膜４３が形成されている。

【００９９】

（信号配線の断面構成）

次に、図７を参照して説明した画素部の断面構造に対応させて、特に本実施形態に係る、外部回路接続端子に接続された各種信号配線の断面構成について以下に説明する。ここに、図８は、図４または図５のＢ－Ｂ´断面図であり、図９は、図４または図５のＣ－Ｃ´断面図である。

【０１００】

図８に示すように、外部回路接続端子１０２の複数の端子のうち、図４または図５に示した右側半数分にあたる端子ＴＣＬＶ$_{INV}$～端子ＴＬＣＣＯＭに接続された主配線１０８は全て、図７に示した第２層間絶縁膜４２上に、夫々が互いに製造工程段階で同時に形成される同一配線層として構成されている。一方、図９に示すように、外部回路接続端子１０２の複数の端子のうち、図４または図５に示した残りの左側半数分にあたる端子ＴＶＤＤＸ～端子ＴＬＣＣＯＭに接続された主配線１０８についても、図７に示した第２層間絶縁膜４２上に、夫々が互いに製造工程段階で同時に形成される同一配線層として構成されている。即ち、外部回路接続端子１０２に接続された全ての主配線１０８は、図７を参照して上述した第２層間絶縁膜上に形成されるデータ線６ａの配線層と、同時に形成される同一配線層として構成されている。このことは、図４または図５に示したような順序で外部回路接続端子１０２の各端子が配列され、これらの端子に接続された主配線１０８が、基板平面上で互いに交差することなく配線されることによって実現されている。

【０１０１】

以上のように、外部回路接続端子１０２に接続された各種の主配線１０８が、互いに同一配線層として構成できることにより、これらの製造工程において比較的容易に形成することが可能であり、更には、データ線６ａと同一配線層として構成できることにより、製造工程を更に簡略化させることが可能となっている。加えて、データ線６ａは、上述のように例えばアルミニウム膜等の低抵抗の金属膜あるいは合金膜からなるため、これと同時に形成される外部回路接続端子１０２に接続された各種の主配線１０８についても、低抵抗の信号配線として構成することができ、信号遅延等の不具合を防止することが可能となっている。

【０１０２】

（変形形態）

次に図１０及び図１１を参照して、上述した実施形態の変形形態について説明する。ここに図１０及び図１１は夫々、変形形態に係る主配線及び冗長配線の断面図であり、図１０は、それらの伸延方向に垂直な断面で、即ち図９と同じく図４または図５のＣ－Ｃ’断面に対応する個所で切った断面図であり、図１１は、それらの伸延方向に沿った断面で切

った断面図である。

【０１０３】

図１０及び図１１に示すように、変形形態では、図９と同じくアルミニウム膜等から夫々形成された複数の主配線１０８である配線ＬＶＤＤＸ、ＬＳＰＸ、ＬＶＳＳＸ等は、冗長配線６００を夫々有する。冗長配線６００は、主配線１０８と別層であり、例えば高融点金属膜等の容量線３００と同一の導電膜から形成されている。また、各冗長配線６００は、平面的に見て対応する主配線１０８と重なって延びており、冗長構造をなす領域においては、主配線１０８とほぼ同様の平面レイアウトを有するように形成されている。更に、冗長配線６００は夫々、複数のコンタクトホール６０１を介して、対応する主配線１０８と電気的に接続されており、該接続された主配線１０８の冗長配線として機能する。その他の構成については、図１から図９を参照して説明した上述の実施形態と同様である。

【０１０４】

従って、本変形形態によれば、冗長構造の採用によって、主配線１０８の配線抵抗を、より一層低めることが可能となる。加えて、冗長構造をなす主配線１０８と冗長配線とのうち一方が仮に断線しても、配線としての機能を果たし得る可能性が残るので、装置が欠陥品化する可能性を低減でき、製造歩留まりを向上させることも可能となる。

【０１０５】

（電子機器）

次に、以上詳細に説明した電気光学装置をライトバルブとして用いた電子機器の一例たる投射型カラー表示装置の実施形態について、その全体構成、特に光学的な構成について説明する。ここに、図１２は、投射型カラー表示装置の図式的断面図である。

【０１０６】

図１２において、本実施形態における投射型カラー表示装置の一例たる液晶プロジェクタ１１００は、駆動回路がＴＦＴアレイ基板上に搭載された液晶装置を含む液晶モジュールを３個用意し、それぞれＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロックミラー１１０８によって、ＲＧＢの三原色に対応する光成分Ｒ、Ｇ及びＢに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにそれぞれ導かれる。この際特に、Ｂ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂによりそれぞれ変調された三原色に対応する光成分は、ダイクロックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１０７】

本発明は、上述した実施形態に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨或いは思想に反しない範囲で適宜変更可能であり、そのような変更を伴なう電気光学装置及び電子機器もまた本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【０１０８】

【図１】本実施形態における電気光学装置の全体構成を示す平面図である。

【図２】図１のＨ－Ｈ’断面図である。

【図３】電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路図である。

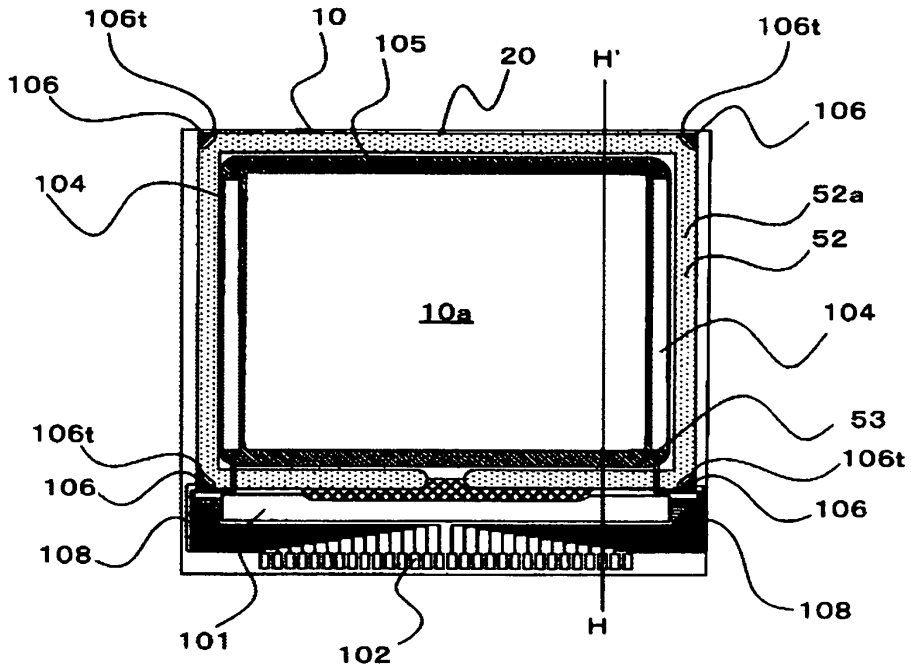
【図４】ＴＦＴアレイ基板上に形成された各種駆動回路、及び各種信号配線の構成を示す等価回路図である。

【図５】ＴＦＴアレイ基板上に形成された各種駆動回路、及び各種信号配線の構成を示す等価回路図である。

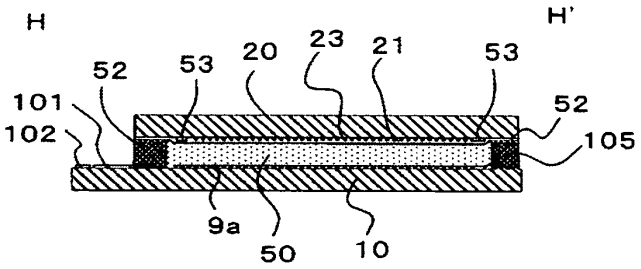
【図６】本発明の実施形態の電気光学装置におけるデータ線、走査線、画素電極等が

形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。
【図７】図６のＡ－Ａ´断面図である。
【図８】図４または図５のＢ－Ｂ´断面図である。
【図９】図４または図５のＣ－Ｃ´断面図である。
【図１０】変形形態に係る主配線及び冗長配線の一の断面図である。
【図１１】変形形態に係る主配線及び冗長配線の他の断面図である。
【図１２】本発明の電子機器の実施形態である投射型カラー表示装置の一例たるカラー液晶プロジェクタを示す図式的断面図である。
【符号の説明】
【０１０９】
１０…ＴＦＴアレイ基板、１０ａ…画像表示領域、２０…対向基板、２１…対向電極、５０…液晶層、５２…シール材、５２ａ…シール領域、７０…蓄積容量、１０１…データ線駆動回路、１０２…外部回路接続端子、１０４…走査線駆動回路、１０６…上下導通材、１０６ｔ…上下導通端子、１０８…主配線、３００…容量線。

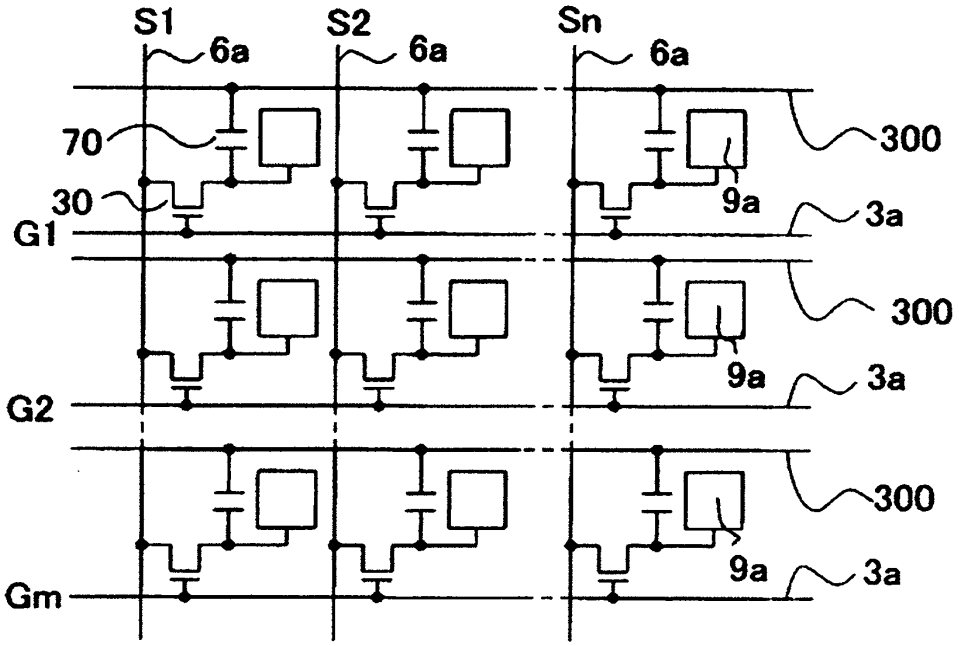
【書類名】図面
【図１】


106t
10
105
20
H'
106t
106
106
104
52a
52
10a
104
53
106t
106t
106
106
108
108
101
102
H

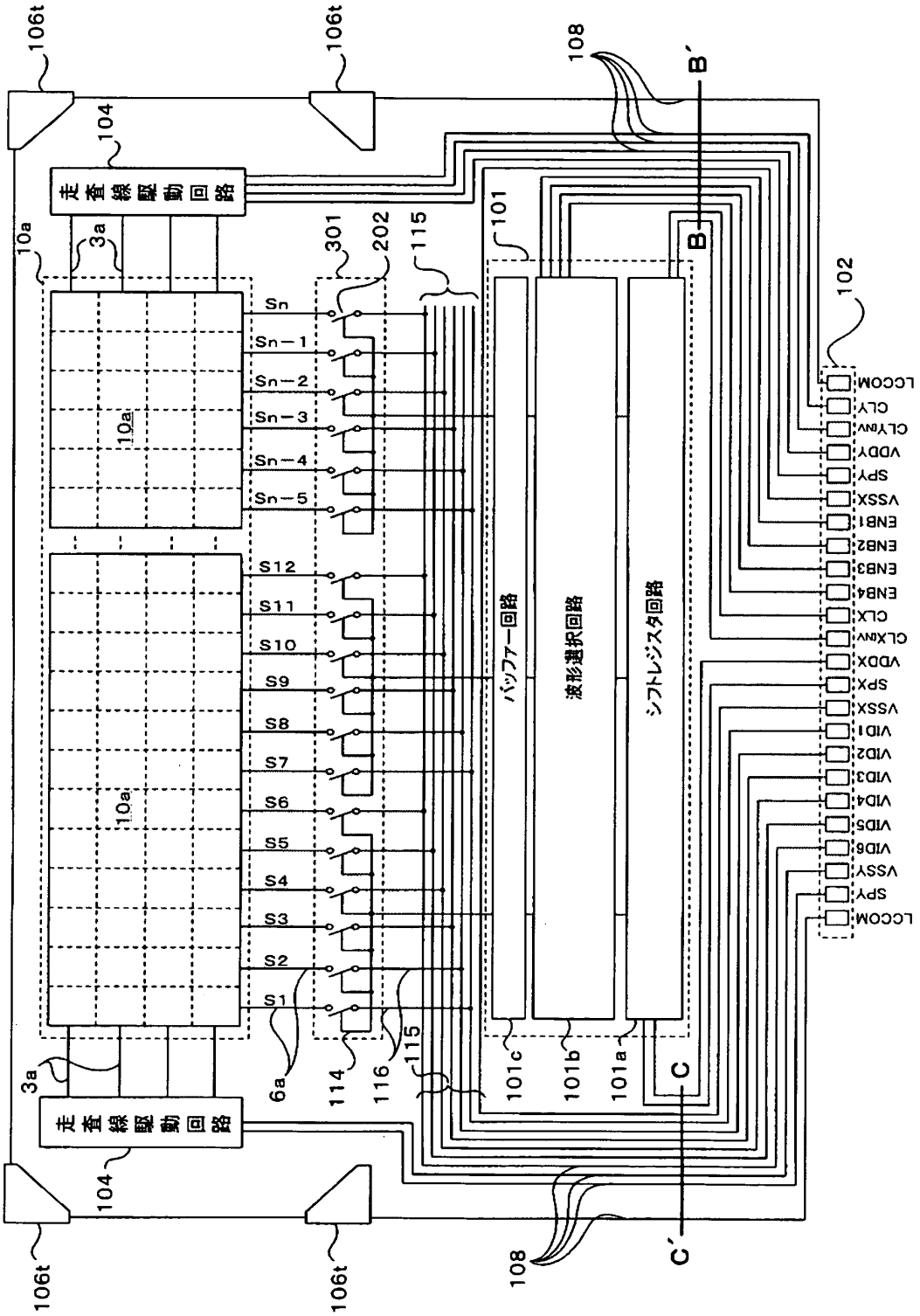
【図２】


H
H'
52
53
20
23
21
53
101
102
52
105
9a
50
10

【図３】

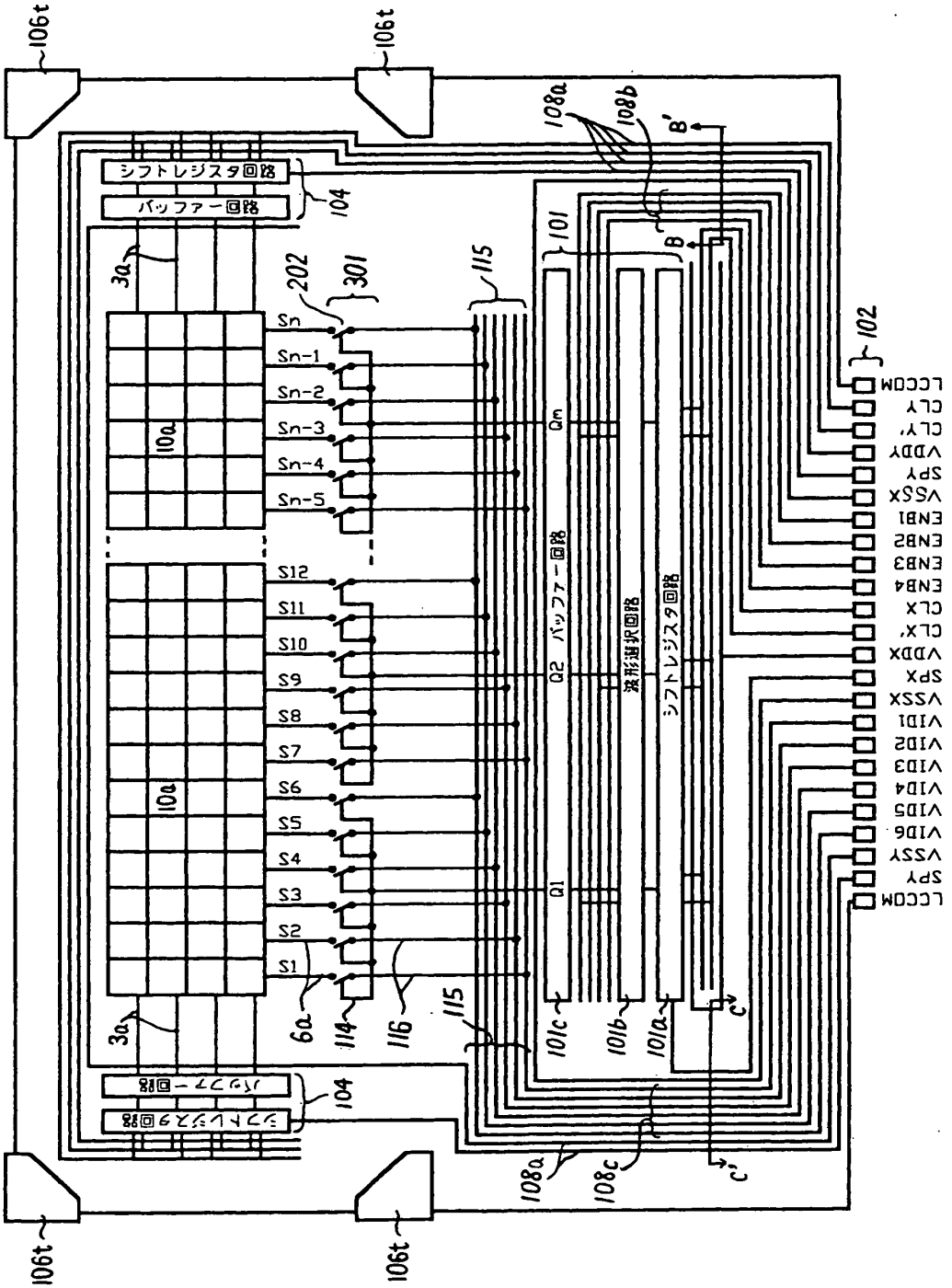


【図４】



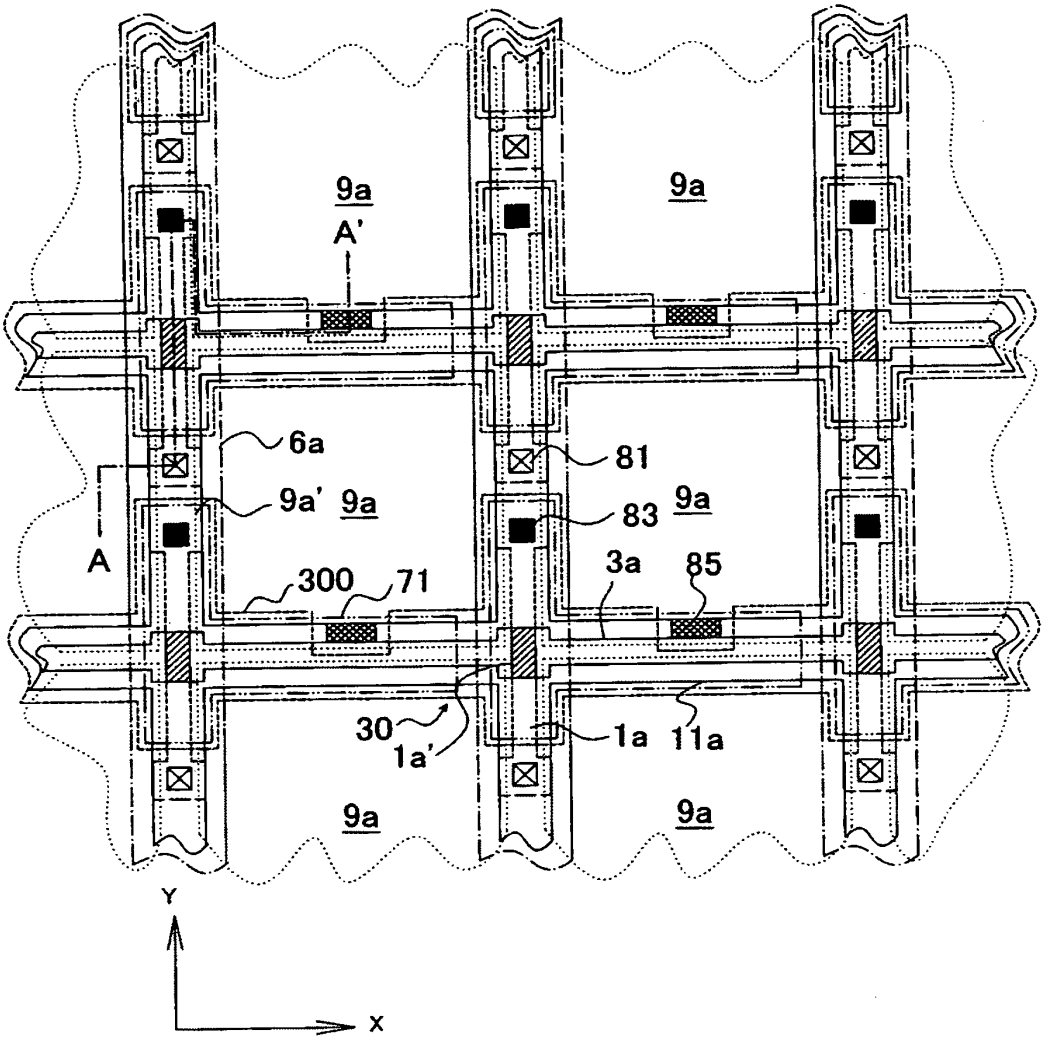
出証特２００４－３０３０３１８

【図５】

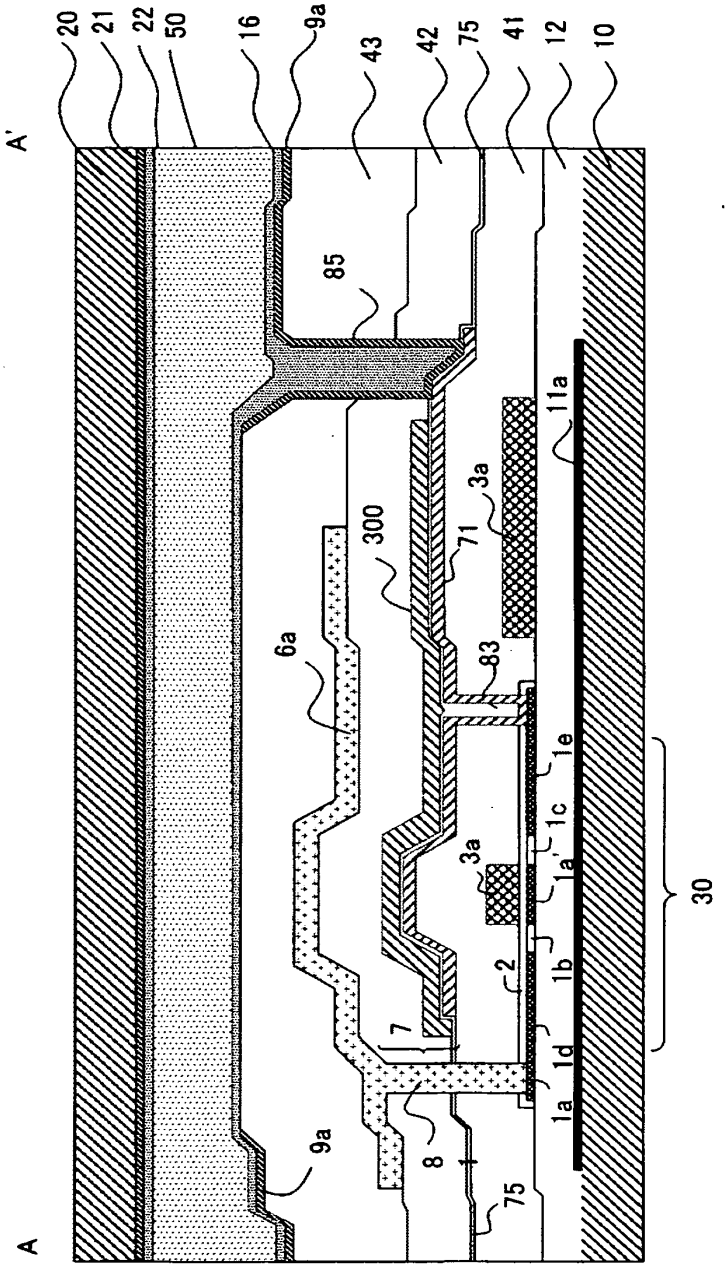


出証特２００４－３０３０３１８

【図６】

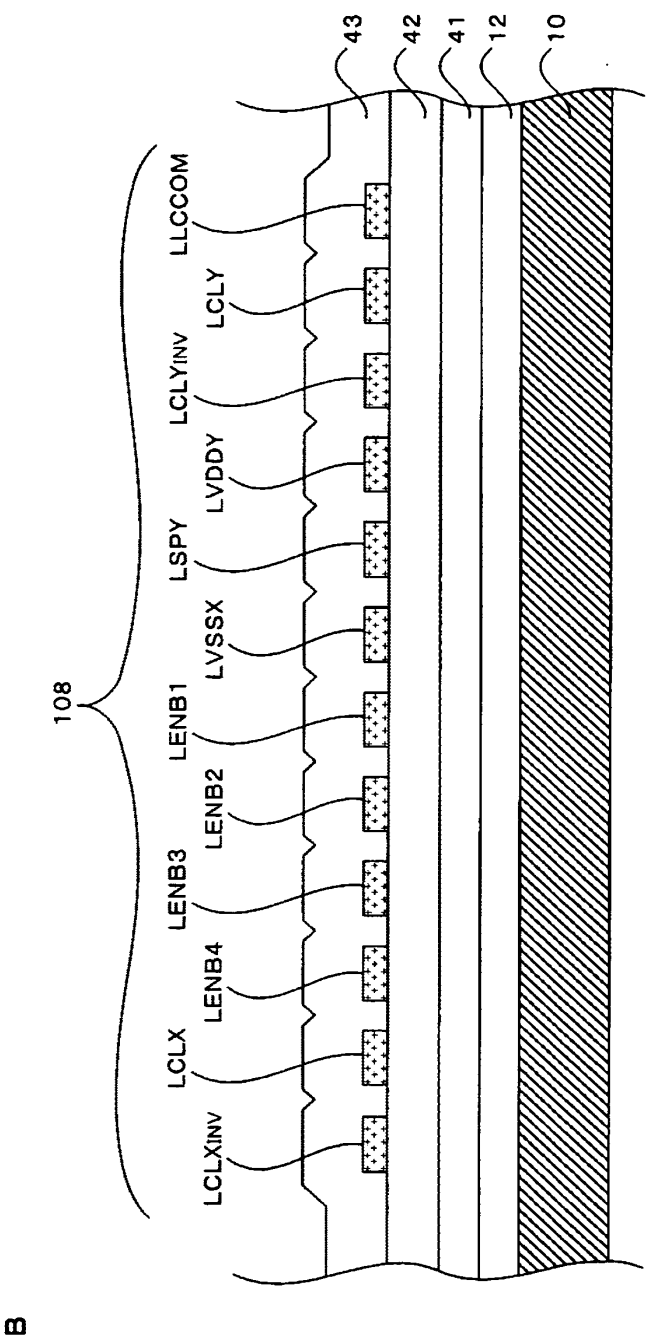


【図７】

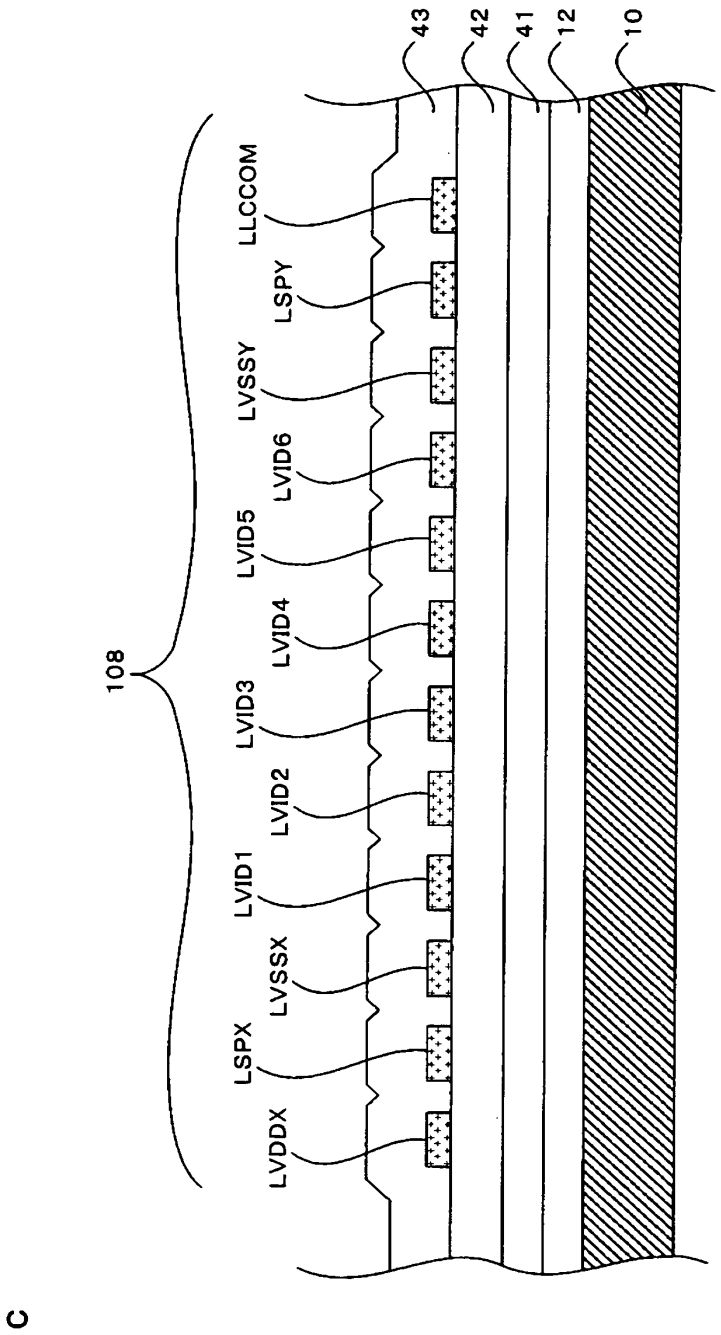


出証特２００４－３０３０３１８

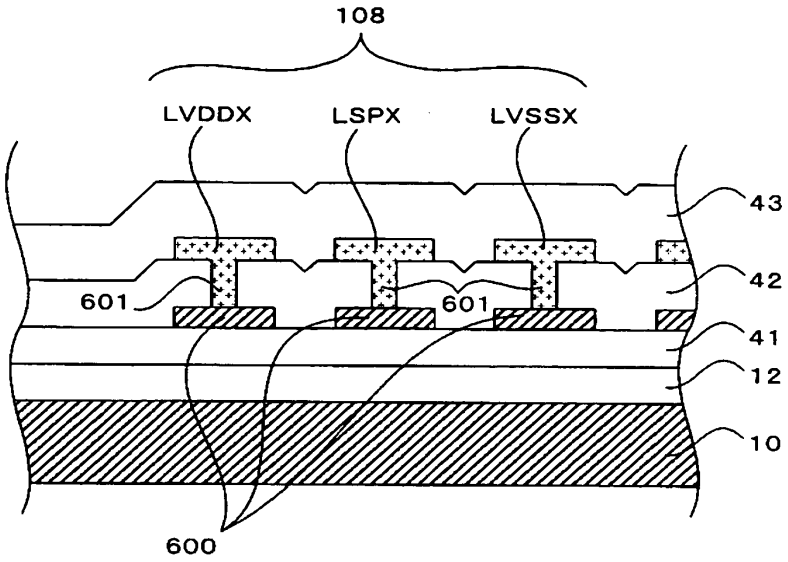
【図８】


B'
43
42
41
12
10
LLCCOM
LCLY
LCLYINV
LVDDY
LSPY
LVSSX
LENB1
LENB2
LENB3
LENB4
LCLX
LCLXINV
108
B

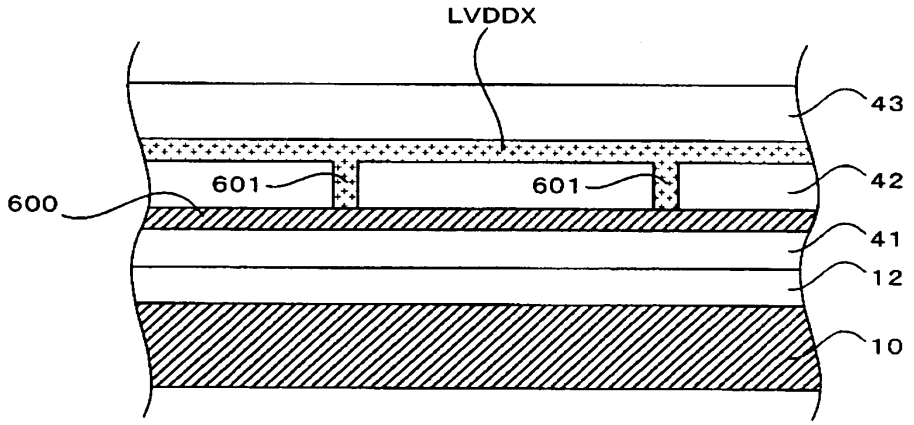
【図９】


C'
C
43
42
41
12
10
108
LLCCOM
LSPY
LVSSY
LVID6
LVID5
LVID4
LVID3
LVID2
LVID1
LVSSX
LSPX
LVDDX

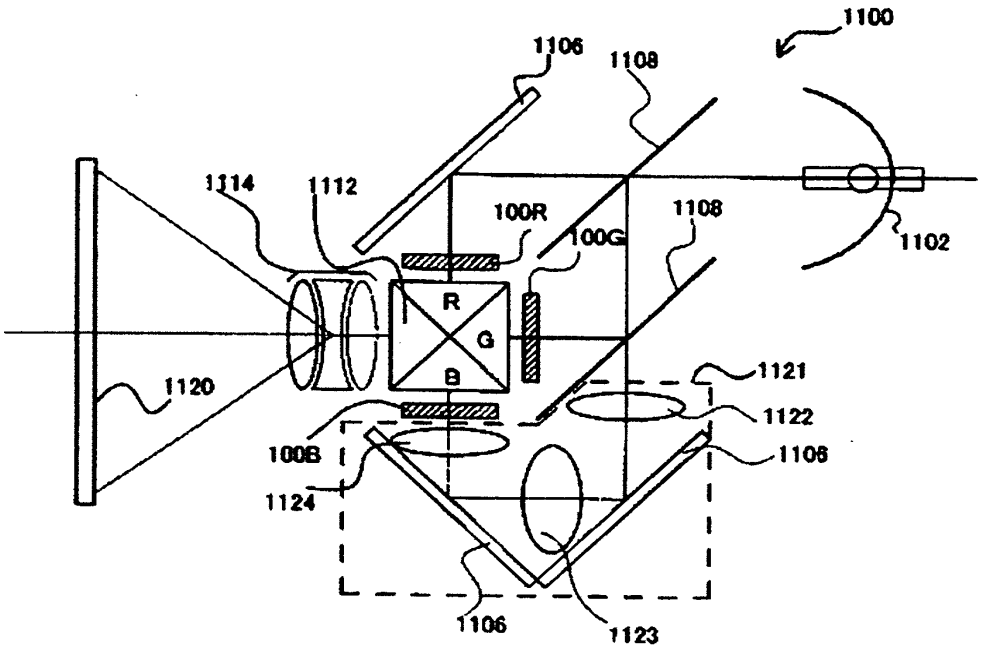
【図１０】


108
LVDDX
LSPX
LVSSX
43
42
601
601
41
12
10
600

【図１１】


LVDDX
43
601
601
42
600
41
12
10

【図１２】



出証特２００４－３０３０３１８

【書類名】要約書
【要約】
【課題】　液晶装置等において、主配線を効率的に低抵抗化し、主配線間における信号の相互干渉を抑制することで、高品位な画像表示を行う。
【解決手段】　基板（１０）上における画像表示領域（１０ａ）の周辺に位置する周辺領域に、複数の外部回路接続端子（１０２）と、これらに夫々一端が接続された複数の主配線（１０８）と、該主配線の他端に接続されており外部回路接続端子から主配線を介して供給される電気信号に基づいて画素部を駆動するための周辺駆動回路（１０１、１０４）とを備える。複数の主配線は、同一導電膜から形成されていると共に相互に交差しないように周辺領域内に平面レイアウトされている。
【選択図】　図５

認定・付加情報

特許出願の番号	特願２００４－０８１５３２
受付番号	５０４００４６３１１３
書類名	特許願
担当官	第四担当上席　　００９３
作成日	平成１６年　３月２４日

＜認定情報・付加情報＞

【特許出願人】

【識別番号】　000002369

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【代理人】　申請人

【識別番号】　100095728

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【氏名又は名称】　上柳　雅誉

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【氏名又は名称】　藤綱　英吉

【選任した代理人】

【識別番号】　100107261

【住所又は居所】　長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社　知的財産本部内

【氏名又は名称】　須澤　修

出証特２００４－３０３０３１８

特願２００４－０８１５３２

出　願　人　履　歴　情　報

識別番号　　［０００００２３６９］

１．変更年月日　　１９９０年　８月２０日
［変更理由］　　新規登録
住　所　　東京都新宿区西新宿２丁目４番１号
氏　名　　セイコーエプソン株式会社

出証番号　出証特２００４－３０３０３１８

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/26/2004 STEUMEL1 00000100 10852255
01 FC:1001 770.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10852255

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	16	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	16 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	0
X43=		OR	X86=	0
+145=		OR	+290=	0
TOTAL		OR	TOTAL	770

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev 10/03)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

NONPROVISIONAL PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400
Facsimile: (703) 836-2787

Attorney Docket No.: 119570

Date: May 25, 2004

16018 U.S. PTO 10/852255 052504

MAIL STOP PATENT APPLICATION

Customer Number: 25944

NONPROVISIONAL APPLICATION TRANSMITTAL
RULE §1.53(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the nonprovisional patent application

For (Title): ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS COMPRISING THE SAME

By (Inventor): Masao MURADE

☒ Formal drawings (Figs. 1-12; 10 sheets) are attached.
☐ Use Figure _____ for front page of Publication.
☐ A Declaration and Power of Attorney is filed herewith.
☐ This application claims benefit of Provisional Application No. _____ filed _____.
(A Preliminary Amendment is attached to reflect this claim in the Specification if not already present.)
☒ This patent application is assigned to SEIKO EPSON CORPORATION.
☐ The executed Assignment is filed herewith.
☒ An Information Disclosure Statement is filed herewith.
☐ Entitlement to small entity status is hereby asserted.
☐ A Preliminary Amendment is filed herewith.
☒ Priority of foreign applications No. 2003-156832 filed June 2, 2003 in Japan and No. 2004-081532 filed March 19, 2004 in Japan is claimed (35 U.S.C. §119).
☒ A certified copy of the above corresponding foreign applications is filed herewith.
☐ This application is NOT to be published under 35 U.S.C. 122(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing.
☒ The filing fee is calculated below:

CLAIMS IN THE APPLICATION AFTER ENTRY OF ANY PRELIMINARY AMENDMENT NOTED ABOVE

			SMALL ENTITY			OTHER THAN A SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$ 385	OR		$ 770
TOTAL CLAIMS	16 - 20	= 0	x 9 =	$	OR	x 18	$
INDEP CLAIMS	2 - 3	= 0	x 43 =	$	OR	x 86	$
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+ 145 =	$	OR	+ 290	$
			TOTAL	$	OR	TOTAL	$ 770

* If the difference is less than zero, enter "0".

☒ Check No. 154404 in the amount of $770.00 to cover the filing fee is attached. Except as otherwise noted herein, the Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

John S. Kern
Registration No. 42,719

JAO:JSK/mxm