

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CHONGQING HKC OPTOELECTRONICS TECHNOLOGY CO., LTD.,
Petitioner,

v.

138 EAST LCD ADVANCEMENTS LIMITED,
Patent Owner.

Case IPR2023-00475
U.S. Patent No. 7,116,390

PATENT OWNER'S PRELIMINARY RESPONSE

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Number	Description
2001	Declaration of Michael Lebby, Ph.D.

I. PRELIMINARY STATEMENT

Pursuant to 37 C.F.R. § 42.107, Patent Owner 138 East LCD Advancements Limited submits this Preliminary Response to the Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 7,116,390 (the “’390 patent” or “’390”). Paper 1, Petition (“Petition” or “Pet.”). Petitioner Chongqing HKC Optoelectronics Technology Co., Ltd. challenges the validity of all ’390 claims 1-13.

The Petition has not established any likelihood that the asserted references render any of claims 1-13 unpatentable. The references presented, alone or in combination as presented in the asserted Grounds, do not disclose all limitations of any ’390 claim. Michael Lebby, Ph.D., a veteran of the optoelectronics industry with extensive LCD research and design work during the relevant time period confirms that the Petition and its supporting expert declaration do not disclose evidence or analysis establishing the presence of all elements of any ’390 claim for any Ground.

Indeed, the Office already considered the teachings relied on by the Petition during prosecution of the ’390 application. The Examiner allowed the ’390 claims over *Muraide*, which the Petition relies on for Grounds 1 and 2, and over a reference, *Kaito*, that discloses substantially the same material relied on by the Petition from *Sunao* (Grounds 1, 2, 4, and 5), *Komeno* (same), and *Fujikawa*

(Ground 3). *Murade II*, which the Petition relies on for Grounds 4 and 5, contains the same material teachings as *Muraide*, considered during prosecution.

The Examiner thus considered all material presented by the Petition and allowed the '390 claims. As shown below, this conclusion follows from the absence of claim limitations from the references presented in each Ground.

The Board therefore should deny institution under 35 U.S.C. § 314(a) for failure to present a likelihood that the Petitioner will prevail on any Ground, or in the alternative under 35 U.S.C. § 325(d) because the Office already considered either the same art (*Muraide*) or substantially the same art (*Kaito*, compared to *Sunao*, *Komeno*, and *Fujikawa*, and *Muraide* compared to *Murade II*) and allowed the claims. Both the teachings of the references presented during prosecution and the teachings of the references presented in the Petition do not disclose all elements of any challenged claim.

II. THE '390 PATENT

A. Inventions Described and Claimed in the '390 Patent

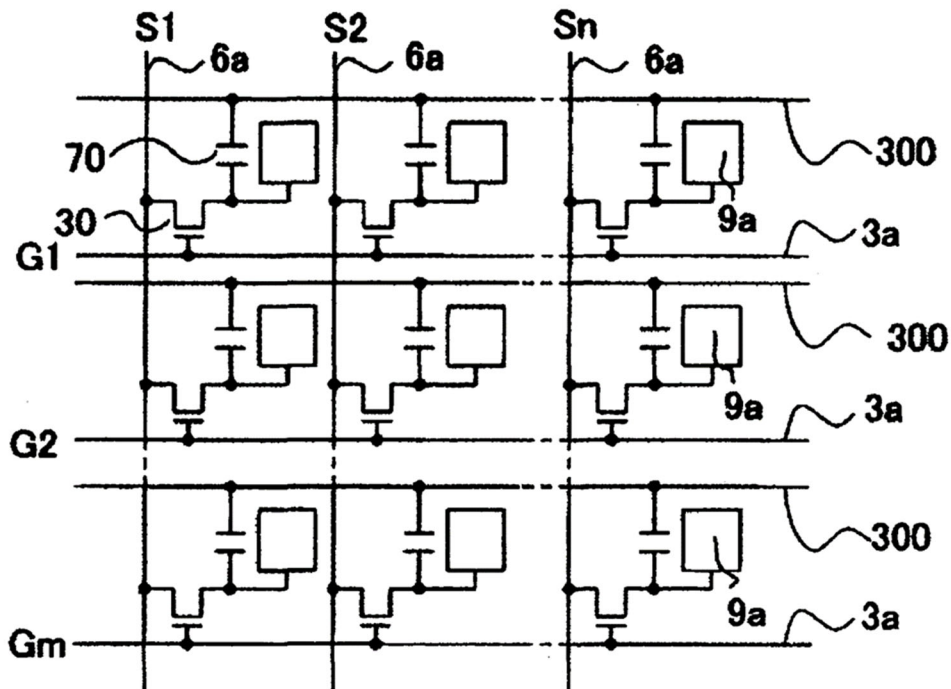
The '390 inventions improve the picture quality of LCD displays while reducing the size of the peripheral region outside the display area and simplifying the manufacturing process. Ex. 1001, 1:33-2:35; Ex. 2001, ¶46. The '390 inventions achieve these benefits with a novel layout of circuits and wires in an LCD device. Ex. 1001, 1:33-2:35, 13:6-39, 14:18-15:31, 16:36-51; Ex. 2001, ¶46.

LCD devices typically have several fundamental components, described here to provide context for the '390 inventions. LCD displays produce images by transmitting light through liquid crystal (LC) molecules controlled by an array of thin film transistors (TFTs) that supply voltages to pixel electrodes. Ex. 1001, 1:14-32, 10:33-65, 12:61-13:5; Ex. 2001, ¶47. The liquid crystal molecules are sealed in an area between two substrates. *Id.*

One substrate, called the “element substrate” or “TFT array substrate” in the '390 patent, includes the TFTs and the circuitry and wiring needed to control those TFTs to supply voltages to the pixel electrodes and produce images. Ex. 1001, 1:14-32, 9:13-20, Fig. 1, Fig. 2; Ex. 2001, ¶48. The second substrate, called the “counter substrate” in the '390 patent, Ex. 1001, 9:13-20, includes a “counter electrode” supplied with a predetermined electrical potential, called a “counter potential” or “counter electrode potential.” *Id.*, 4:23-38, 10:3-25, 12:61-13:5, Fig. 1, Fig. 2; Ex. 2001, ¶48. The counter potential creates an electric field between the pixel electrodes supplied by the TFTs and the counter substrate that causes the liquid crystal molecules to rotate and change the direction of light passed through them to create different levels of brightness. Ex. 1001, 4:39-52, 10:50-65; Ex. 2001, ¶48.

The image display region of an LCD device contains an array of many TFTs to control individual pixels or sub-pixels in the display. Ex. 1001, 9:13-20, 10:33-

40, Fig. 1, Fig. 3; Ex. 2001, ¶49. The TFTs are controlled by voltages supplied on “data lines” that supply image signals and “scanning lines” that control the gates of the TFTs. Ex. 1001, 10:26-49; Ex. 2001, ¶49. Figure 3 of the '390 patent illustrates “data lines 6a,” which provide “image signals S1, S2, . . . , and Sn” to an array of “TFTs 30,” and also “scanning lines 3a,” which provide “scanning signals G1, G2, . . . , and Gn”:

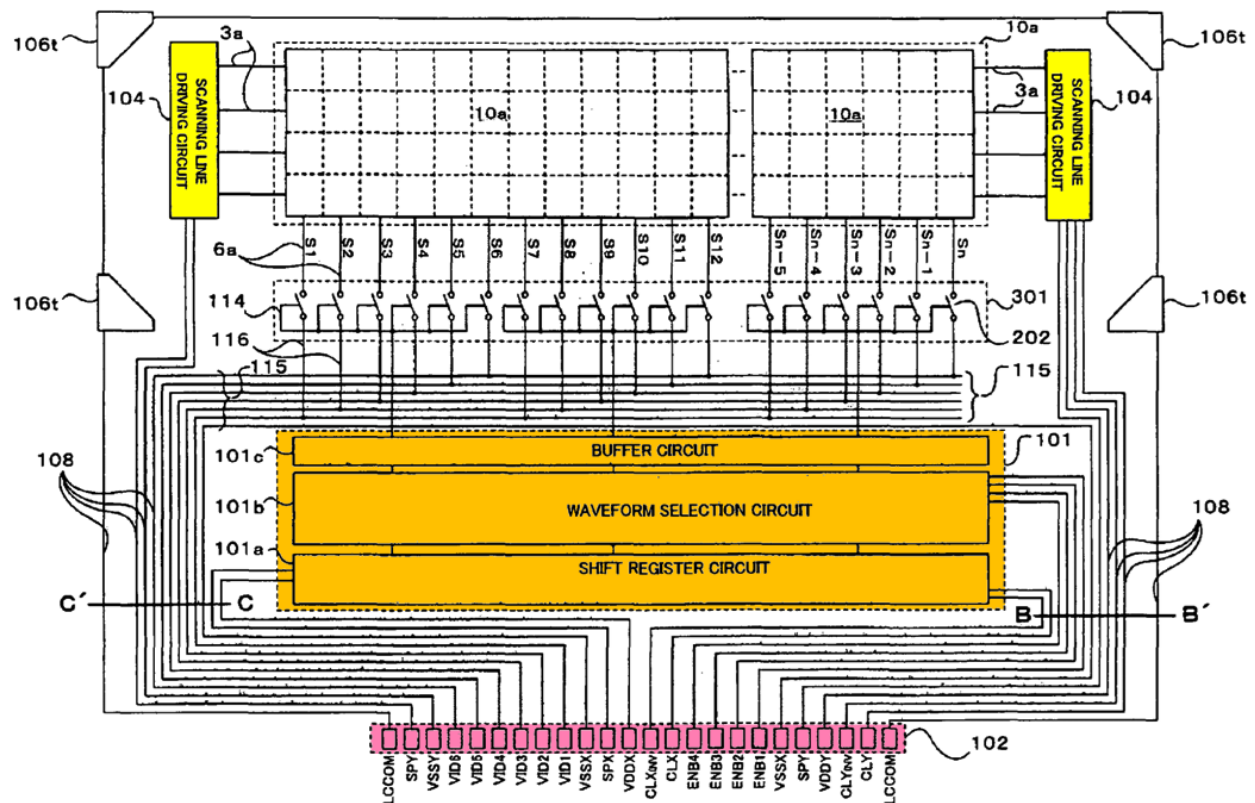


Ex. 1001, Fig. 3, 8:27-30, 10:26-49; Ex. 2001, ¶49.

Circuits control the TFTs in the array: “a data line driving circuit” for providing the image signals, and “scanning line driving circuits” for the scanning signals. Ex. 1001, 1:14-32, 9:47-60; Ex. 2001, ¶50. Figure 4 illustrates “data line driving circuit 101” (highlighted below in orange) connected to “data lines 6a” and

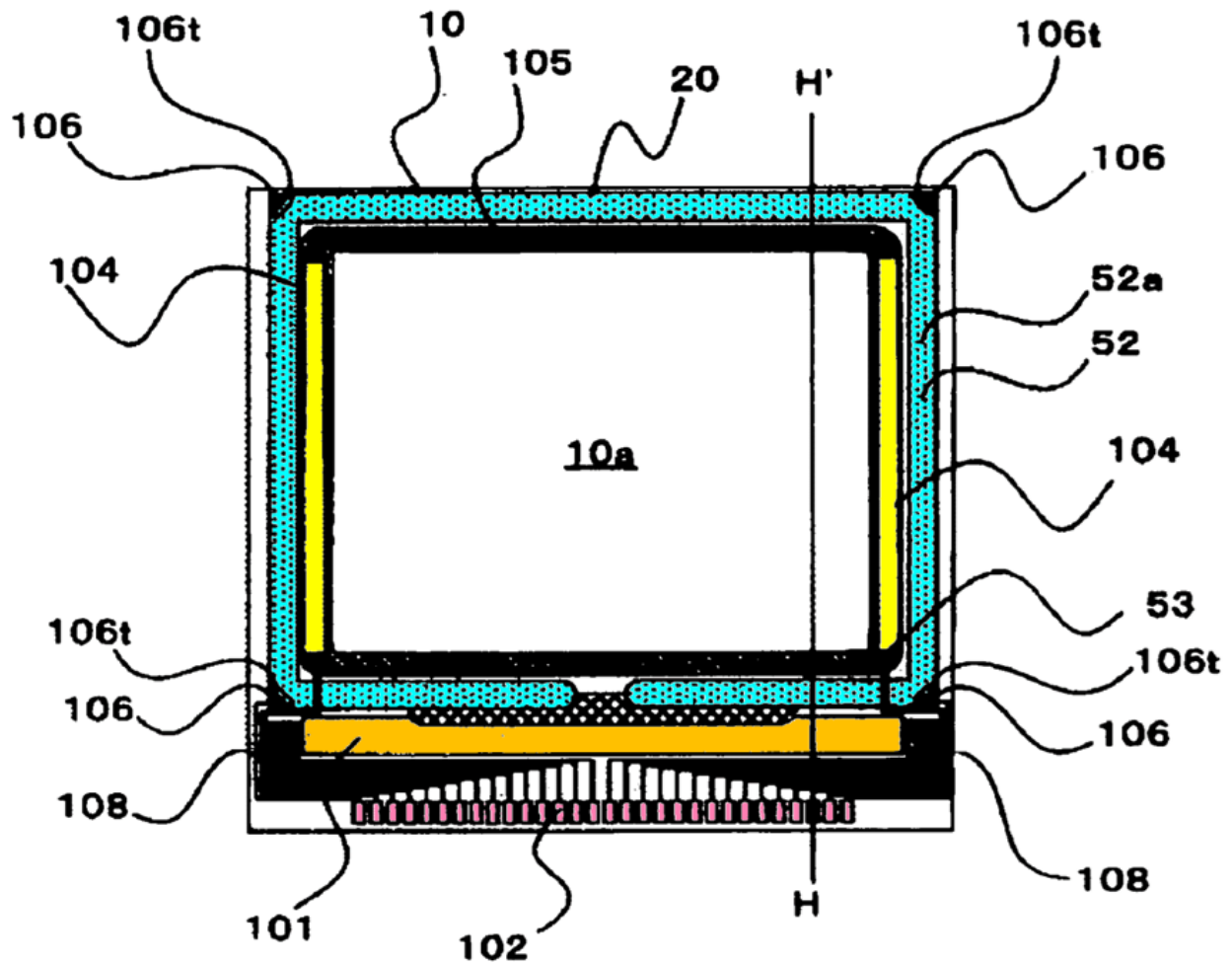
“scanning line driving circuits 104” (highlighted in yellow) connected to “scanning lines 3a” that provide signals to “image display region 10a” where the TFTs reside.

Ex. 1001, Fig. 4, 11:29-40, 10:33-49; Ex. 2001, ¶50. The “data line driving circuit 101” and “scanning line driving circuits 104” are supplied from external sources via “external circuit connection terminals 102” (highlighted in pink) and “main wiring lines 108” (not highlighted). Ex. 1001, 9:47-10:2, 11:29-40; Ex. 2001, ¶50.



Ex. 1001, Fig. 4 (emphasis added), 11:29-40; Ex. 2001, ¶50.

Figure 1 illustrates these circuits at a less granular level of detail. It also illustrates “seal material 52,” (highlighted in blue) which encloses the liquid crystal material between the substrates:

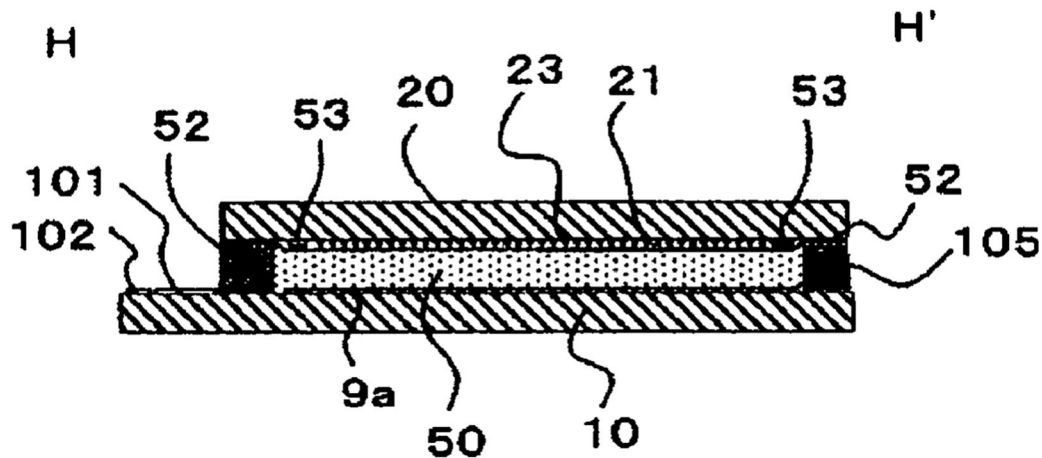


Ex. 1001, Fig. 1 (emphasis added), 9:47-10:2; Ex. 2001, ¶51.

Figure 2 provides a cross-section across the line H—H' shown in Figure 1.

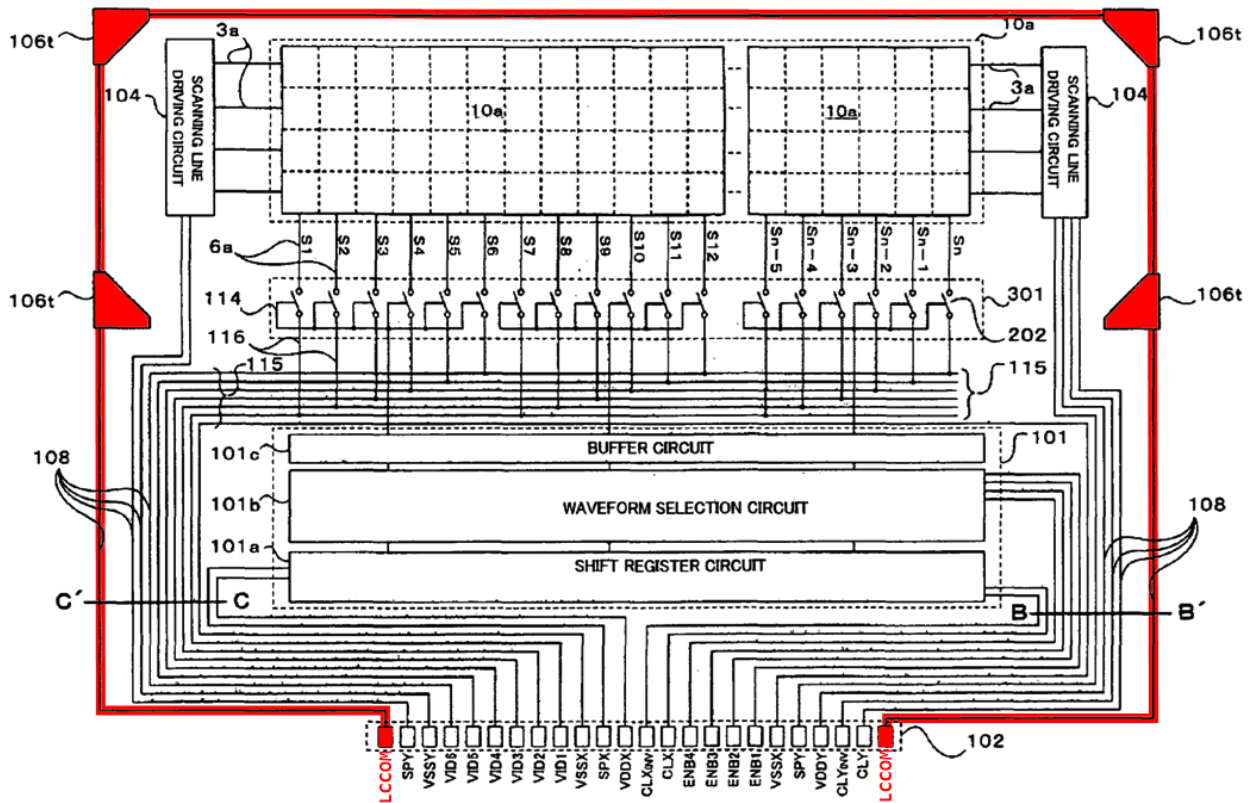
Ex. 1001, 9:8-10; Ex. 2001, ¶52. Figure 2 illustrates “liquid crystal layer 50”

between “TFT array substrate 10” and “counter substrate 20” and sealed in by “seal material 52”:



Ex. 1001, Fig. 2, 9:13-20; Ex. 2001, ¶52.

The “TFT array substrate 10” and “counter substrate 20” are electrically connected by “conduction terminals 106t,” as shown in Figures 1 and 4. Ex. 1001, Fig. 1, Fig. 4, 10:14-25, 12:61-13:5; Ex. 2001, ¶53. The terminals provide a “counter electrode potential LCCOM” to the counter substrate via “counter electrode potential line LLCCOM” and its corresponding external terminal “TLCCOM” on the element substrate. Ex. 1001, 12:61-15:31; Ex. 2001, ¶53. The items highlighted in red below illustrate the electrical counter potential path on the element substrate:



Ex. 1001, Fig. 4 (emphasis added), 12:61-14:9; Ex. 2001, ¶53.

The '390 inventions relate to the layout and fabrication of these components.

Ex. 2001, ¶54. The inventions provide a layout of circuits, terminals, and main wiring lines that improve upon the prior art by reducing the area occupied by circuits and wiring while improving image quality and simplifying manufacturing.

Id. Three particular characteristics of the inventive layout frame the issues presented by the Petition and distinguish all the references it presents. *Id.*

First, the '390 inventions locate the counter electrode potential line and corresponding terminal nearer the edge of the element substrate than a plurality of other main wiring lines 108 coupled to the peripheral driving circuits 101 and 104,

as shown in the annotated Figure 4 above. Ex. 1001, 13:6-39; Ex. 2001, ¶55. This allows a reduction in size of the element substrate and a decrease in resistance in the wiring lines in conjunction with the second and third aspects of the inventions discussed below. Ex. 1001, 13:6-39, 14:18-15:54, 16:36-51; Ex. 2001, ¶55.

Second, the '390 inventions provide a layout of main wiring lines 108 such that those lines do not intersect. Ex. 1001, 13:6-39, 14:18-15:54; Ex. 2001, ¶56.

The '390 patent explains an example way of achieving this layout by locating the “scanning line driving circuits 104” within the seal region 52a (as illustrated in Figure 1, above) instead of outside that region. Ex. 1001, 13:6-39; Ex. 2001, ¶56.

The specification explains:

According to the present embodiment, in particular, the scanning line driving circuits 104 are arranged further inside than the seal region 52a illustrated in FIG. 1. That is, in FIGS. 4 and 5, the scanning line driving circuits 104 are arranged to be closer to the center of the TFT array substrate 10 than the counter electrode potential lines LLCCOM provided along the edges of the TFT array substrate 10 so as to pass through the four upper and lower conduction terminals 106t and to surround the image display region 10a and various driving circuits.

Therefore, compared with the case in which the scanning line driving circuits 104 are arranged outside the seal region 52a in the peripheral region, it is possible to reduce the space of the peripheral region in the TFT array substrate 10 and to miniaturize the entire device.

Furthermore, it is possible to lay out the group of the plurality of main wiring lines 108a including the counter electrode potential lines LLCCOM and the various signal wiring lines that reach the scanning line driving circuits 104 and the group of the plurality of main wiring lines 108b including the various signal wiring lines that reach the data line driving circuit 101 in plan view without intersecting each other.

Ex. 1001, 13:6-39. That is, the arrangement of seal and scanning line driving circuits allows locating the counter electrode potential line near the edge of the element substrate without crossing any other main wiring lines. *Id.*; Ex. 2001, ¶56.

Third, the '390 inventions fabricate all main wiring lines, including the counter electrode potential line, from the same conductive material. Ex. 1001, 14:18-15:31, 16:36-51; Ex. 2001, ¶57. The '390 inventions achieve this by eliminating intersections of any main wiring lines, including the counter electrode

potential line. *Id.* When lines intersect, they require separate wiring line layers, separated by an insulating film, at the intersections. *Id.* Because the '390 inventions avoid intersections, they allow fabricating the main wiring lines from the same conductive film, which decreases resistance and simplifies the manufacturing process. *Id.*

Claim 1 recites these elements of the '390 invention. Ex. 1001, 21:52-22:12 (claim 1). It recites (1) a counter electrode potential line located nearest the edge of the substrate among a plurality of main wiring lines, including lines coupled to peripheral driving circuits; (2) a layout of main wiring lines such that they do not intersect; and (3) main wiring lines made out of the same conductive film:

1. An electro-optical device, comprising:

a plurality of pixel portions provided in an image display

region on an element substrate;

in a peripheral region of the image display region on the

element substrate, a plurality of external circuit

connection terminals, **a plurality of main wiring**

lines each having one end coupled to each of the

plurality of external circuit connection

terminals, and peripheral driving circuits

coupled to the other ends of the main wiring

lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines,

a counter electrode provided in the peripheral region on a counter substrate that is arranged to face the element substrate;

a counter electrode potential line that supplies counter electrode potential to the counter electrode, which is at least one of the plurality of main wiring lines, upper and lower conduction terminals that are provided in the peripheral region on the element substrate, and that are connected to the counter electrode potential line,

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

**the counter electrode potential line being closest to
edges of the element substrate, among the
plurality of main wiring lines.**

Id. (emphasis added).

None of the references or combinations asserted in the Petition disclose this combination of elements that deliver the benefits of the '390 inventions.

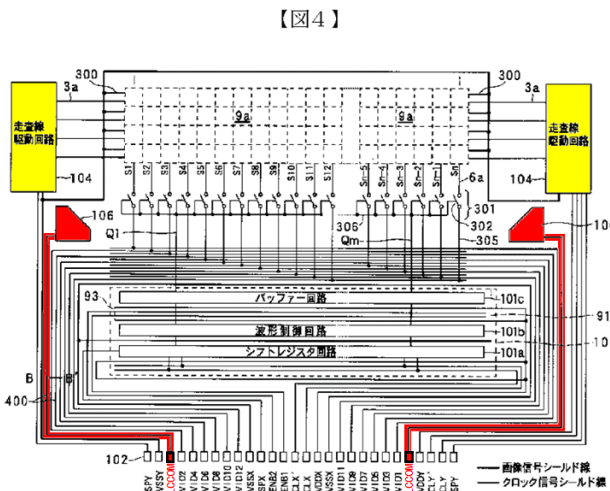
B. Art Addressed During Prosecution of the '390 Patent

During prosecution, the '390 applicant disclosed prior art references that included teachings identical in relevant part to those relied on in the Petition. The applicant disclosed these references before receiving an Office Action. First, the '390 applicant disclosed *Muraide*, with a Japanese original and English translation, in an IDS with the initial '390 application on May 25, 2004. Ex. 1004, 295-296 (IDS), 404-448 (original and translation). Second, the applicant disclosed *Kaito* (JP10-253984, Ex. 1004, 224-241) in a second IDS dated September 14, 2005, *id.*, 103-114, and provided the Examiner with an original (in Japanese) and an English translation. Ex. 1004, 126-127 (IDS), 224-231 (translation), 232-241 (original).

The Petition relies upon *Muraide* as the primary reference for Grounds 1 and 2. For Grounds 4 and 5, the Petition relies upon teachings from *Murade II* that are substantially the same as teachings from *Muraide*. For example (discussed further in §V.D.iii):

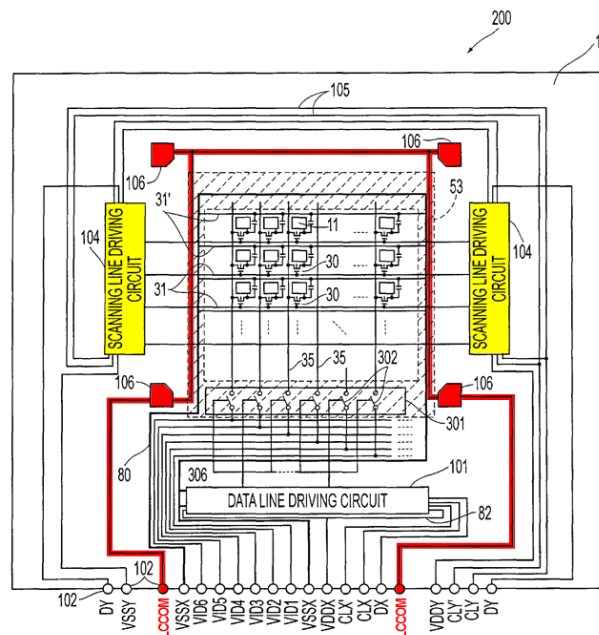
***Muraide*, Fig. 4 (Ex. 1005)**

(considered during prosecution;
asserted in Grounds 1, 2)



***Murade II*, Fig. 1 (Ex. 1008)**

(asserted in Grounds 4, 5)

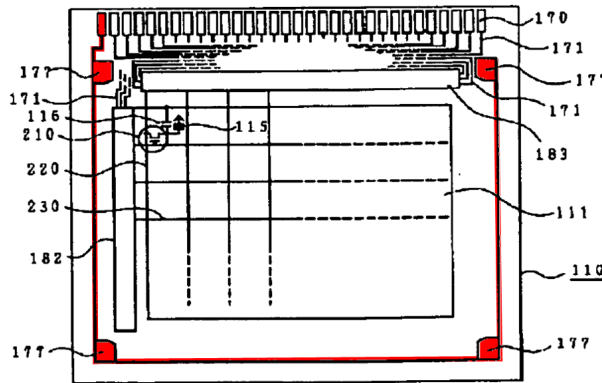


Ex. 1005, Fig. 4 (emphasis added); Ex. 1008, Fig. 1 (emphasis added).

For all Grounds, 1-5, the Petition relies upon alleged teachings from *Sunao*, *Komeno*, and *Fujikawa* relating to placement of a counter potential line near the edge of the LCD substrate—*Kaito* contains a substantially identical teaching. For example (discussed further in §V.A.vi, §V.C.iii, and §V.D.iii):

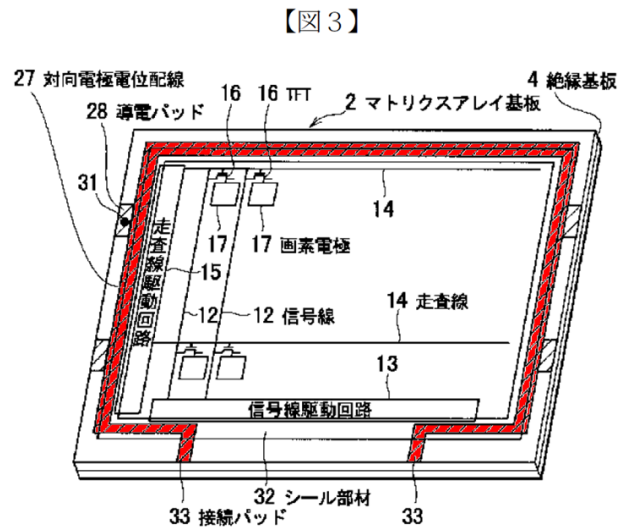
Kaito, Fig. 3 (Ex. 1004, 237)

(considered during prosecution)



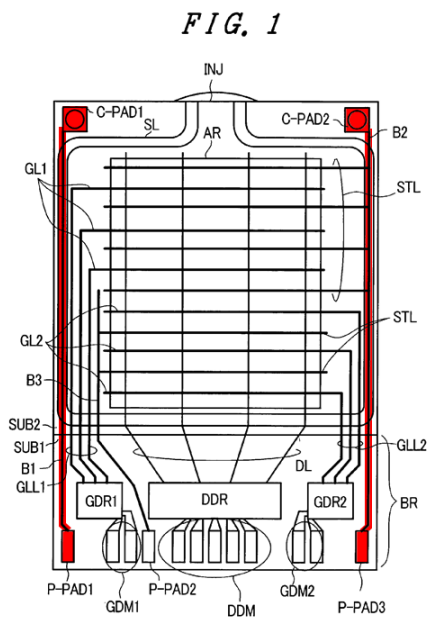
Sunao, Fig. 3 (Ex. 1006)

(asserted in Grounds 1, 2, 4, 5)



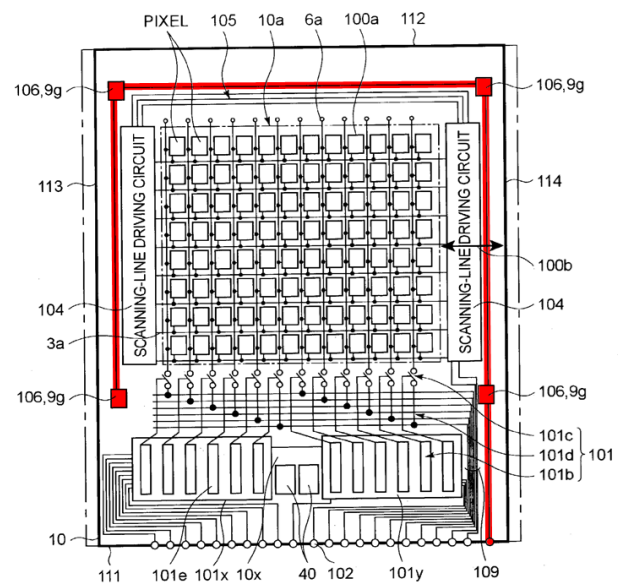
Komeno, Fig. 1 (Ex. 1009)

(asserted in Grounds 1, 2, 4, 5)



Fujikawa, Fig. 2 (Ex. 1007)

(asserted in Ground 3)



Ex. 1004, 237 (Fig. 3 (emphasis added)); Ex. 1006, Fig. 3 (emphasis added); Ex. 1009, Fig. 1 (emphasis added); Ex. 1007, Fig. 2 (emphasis added).

The Examiner considered both *Muraide* and *Kaito*. The Examiner applied *Muraide* in the '390 prosecution's sole Office Action, asserting that *Muraide* anticipated some '390 application claims and rendered others obvious. Ex. 1004, 103-113 (Office Action, Nov. 15, 2005). The Examiner also initialed the IDS to indicate consideration of *Kaito*, *id.*, 116, and did not apply *Kaito* in the Office Action.

In response to the Office Action, the applicant amended the proposed claims to include limitations relating to “a counter electrode line,” including the limitations “a counter electrode potential . . . is at least one of the plurality of main wiring lines” and “the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.” Ex. 1004, 39 (Amendment, Feb. 15, 2006).

After the amendment, the Examiner allowed the claims. Ex. 1004, 5-9 (Notice of Allowability, June 12, 2006). The Examiner explained that “there is no prior art of record that teaches or suggests an electro-optical device comprising a relationship of various elements as claimed with the specific allowable subject matter cited in the following claim,” and emphasized the following limitations from '390 claim 1:

in a peripheral region of the image display region on the element substrate, a plurality of external circuit connection terminals, a plurality of main wiring lines each having one end coupled to each of the plurality of external circuit connection terminals, and peripheral driving circuits coupled to the other ends of the main wiring lines, the peripheral driving circuits driving the pixel portions based on electric signals supplied from the external circuit connection terminals through the main wiring lines

* * *

the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region; and

the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.

Id., 7-8.

As shown below, the references asserted in the Petition do not disclose this relationship of elements in the '390 claims, as the Examiner determined for *Muraide* and *Kaito*.

III. CLAIM CONSTRUCTION

No claim terms require express construction to determine that the Petition does not establish any evidence of several claim limitations and thus deny institution. For purposes of this Preliminary Response, Patent Owner contends that the claims should be given their ordinary and customary meaning in light of the specification and prosecution history, as understood by a person of ordinary skill in the art. 37 C.F.R. § 100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

IV. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this Preliminary Response only, Patent Owner does not dispute the level of skill for a person of ordinary skill in the art (“POSITA”) set forth in the Petition. Pet., 8. The level of skill in the art does not affect whether to deny institution, because the Petition and its expert do not address certain claim limitations and disclosures from the applied references at all. Patent Owner does not waive, however, any argument regarding the proper level of skill and reserves the right to later advance additional arguments.

**V. THE PETITION DOES NOT ESTABLISH A REASONABLE
LIKELIHOOD THAT THE APPLIED REFERENCES RENDER THE
CHALLENGED CLAIMS UNPATENTABLE OR THAT THE
OFFICE ERRED IN ITS ANALYSIS OF SUBSTANTIALLY THE
SAME ART DURING PROSECUTION.**

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3), requiring IPR petitions to identify “with particularity . . . the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim”). That requirement compels the Petition to explain *how* an individual reference renders a challenged claim unpatentable. *Id.*

The Petition does not satisfy this fundamental requirement for any Ground, because it does not explain how the asserted references disclose certain limitations of ’390 claim 1, from which all other claims depend. It relies instead on conclusory assertions about cited disclosures without explaining how or why those disclosures teach what the Petition asserts. The Petition also does not address express teachings in the asserted references that contradict the Petition’s conclusory assertions as to what the references disclose.

The Petition also does not address art considered during prosecution that includes disclosures substantially the same as those relied on in the Petition, and it does not assert that the Office erred in its consideration of such art.

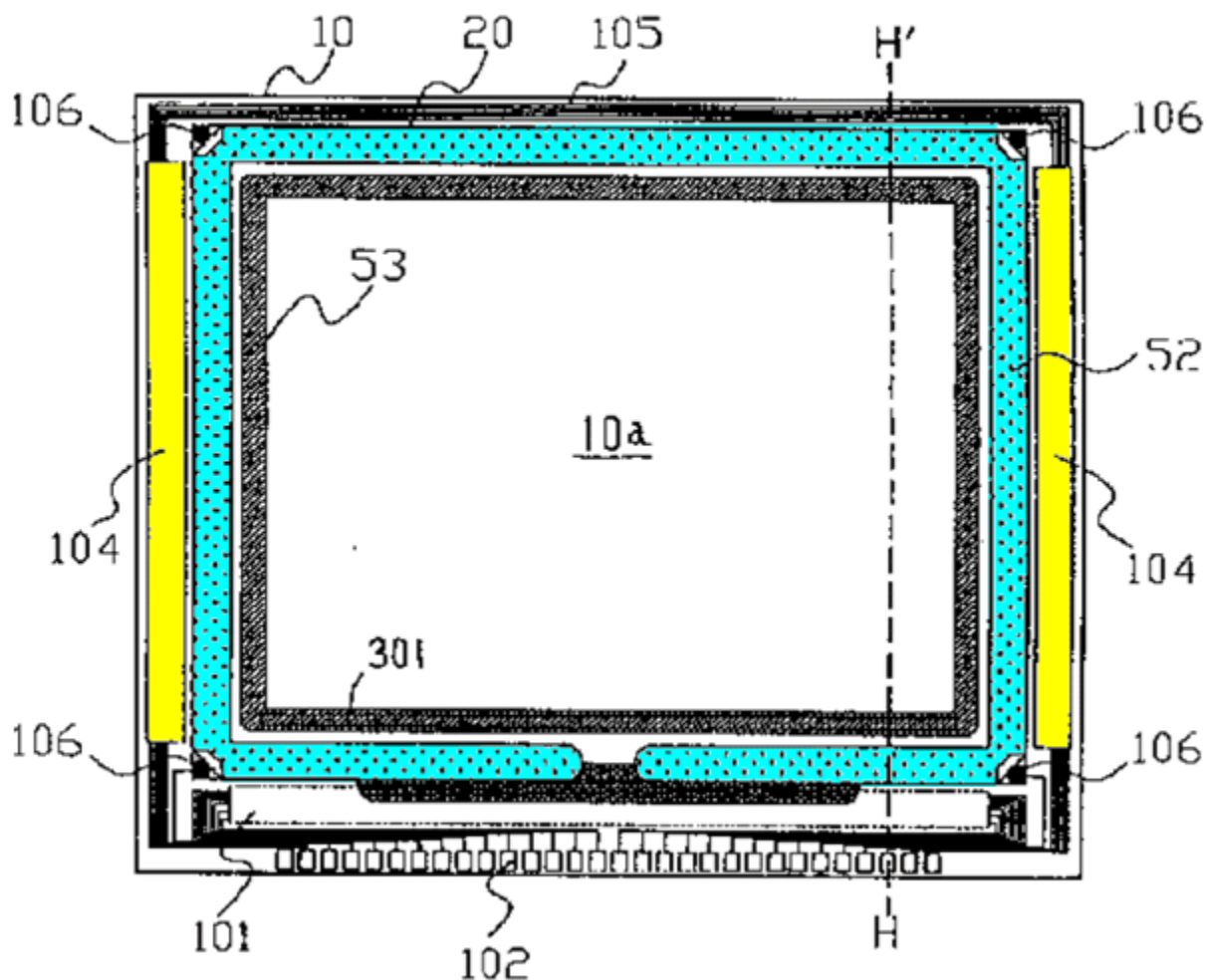
The Petition therefore has not carried its burden to establish a reasonable likelihood of success under § 314(a), and it has not addressed that “the same or substantially the same prior art . . . previously were presented to the Office” under § 325(d). The Board should deny institution.

A. Ground 1: The Petition Does Not Establish a Reasonable Likelihood that *Muraide* in Combination with *Sunao* or *Komeno* Renders Unpatentable Claims 1-11 and 13 or that the Office Erred in Its Consideration of *Muraide* and Art Substantially the Same as *Sunao* and *Komeno* During Prosecution.

i. Overview of *Muraide*

Muraide describes an LCD layout in which the counter potential line does not reside nearer the edge of the substrate than wiring lines supplying scanning line driving circuits. Ex. 1005, ¶¶[0076]-[0078], ¶[0085], ¶¶[0105]-[0106], Fig. 4, Fig. 11, Fig. 12; Ex. 2001, ¶71. *Muraide*’s placement of scanning line driving circuits relative to the LCD seal and counter substrate, and its fabrication process to achieve its noise-shielding goals, dictate this layout. *Id.*

Unlike the '390 patent, *Muraide* locates its scanning line driving circuits outside the LCD seal, as illustrated in Figure 11 with “sealing material 52” highlighted in blue and “scanning line driving circuit 104” highlighted in yellow:



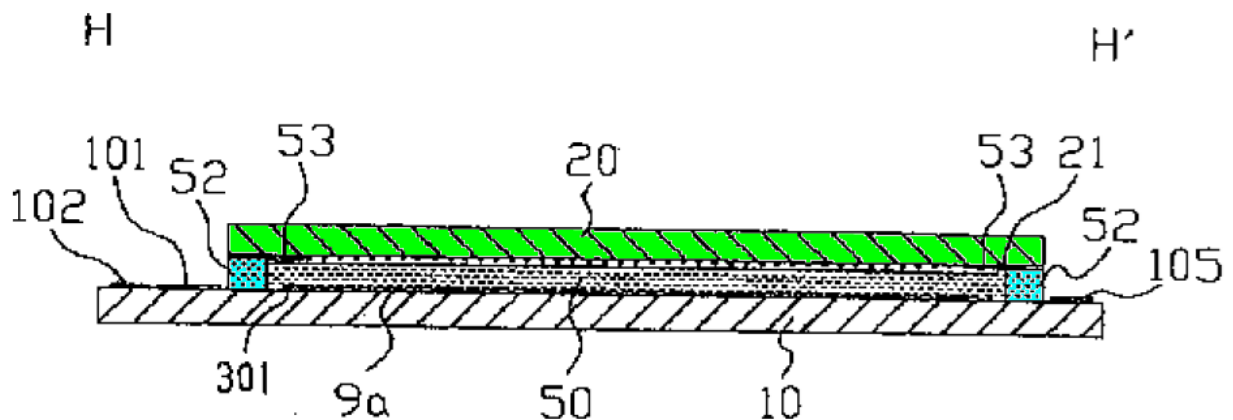
Ex. 1005, ¶[0106], Fig. 11 (emphasis added); Ex. 2001, ¶72.

Muraide’s Figure 11 also illustrates “vertical conductive terminals 106,” which supply a counter potential from “TFT array substrate 10” to a “counter substrate 20” at the corners of the LCD seal, farther from the edge than scanning

line driving circuit 104. Ex. 1005, ¶[0106], Fig. 11; Ex. 2001, ¶73. *Muraide* explains that the vertical conductive terminals reside “in at least one position of a corner portion of the counter substrate 20.” *Id.*

Muraide’s Figure 12 illustrates, in a cross-sectional view, that “counter substrate 20” (highlighted green, below) extends only to the “sealing material 52” (highlighted blue):

【図 12】

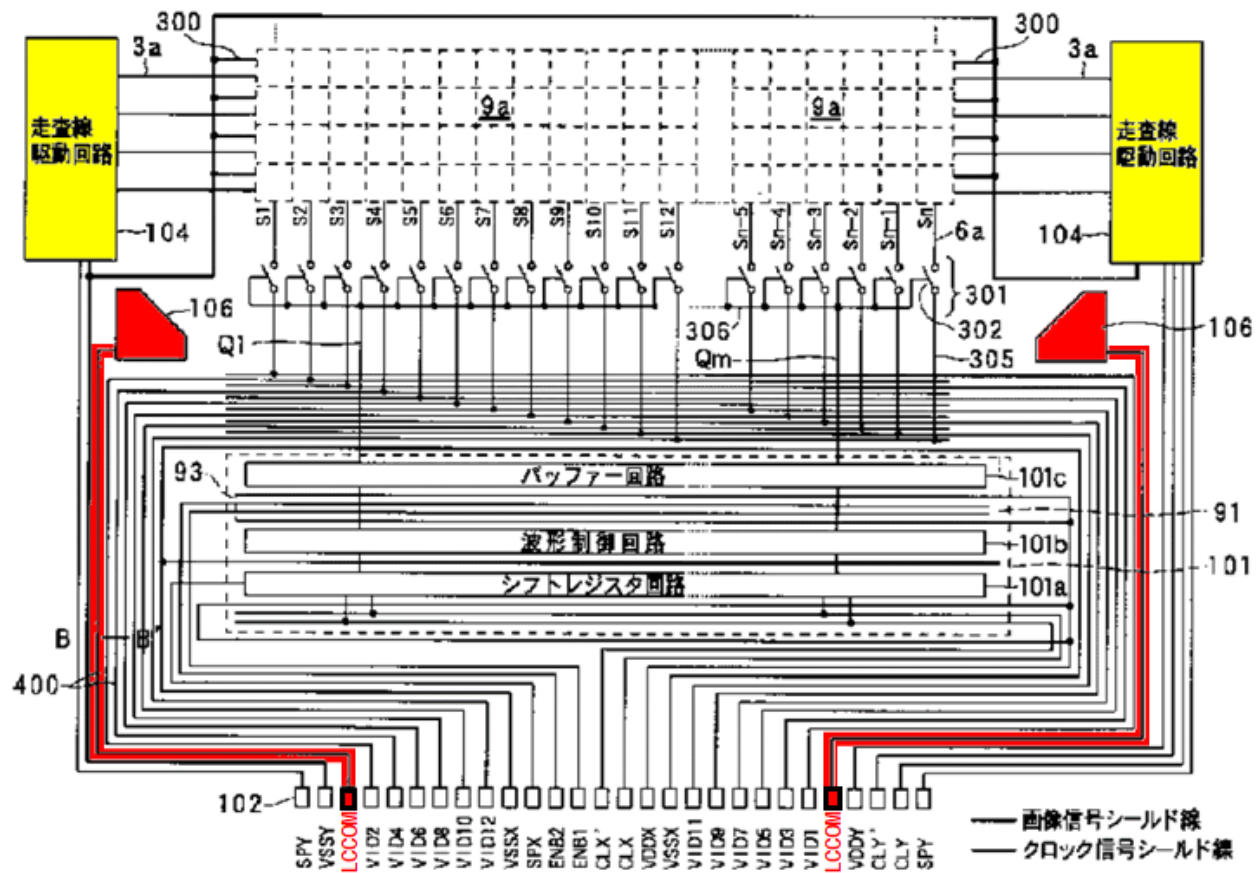


Ex. 1005, Fig. 12 (emphasis added), ¶[0106]; Ex. 2001, ¶74.

As a result of this design, *Muraide*’s scanning line driving circuit 104 (highlighted yellow, below) resides nearer the edge of TFT array substrate 10 than vertical conductive terminals 106 (highlighted red, below). Ex. 1005, ¶[0085], ¶[0106], Fig. 4, Fig. 11; Ex. 2001, ¶75. *Muraide*’s Figure 4 illustrates the wiring layout corresponding to this circuit and substrate layout. *Muraide*’s layout places the external terminals 102 and wiring lines 400 supplying scanning line driving

circuit 104 nearer the edge of TFT array substrate 10 than the terminal and line LCCOM (also highlighted red), which supplies a counter potential to vertical conductive terminals 106:

【図4】



Id. (emphasis added).

Muraide's layout and the fabrication of its wiring lines attempts to reduce noise from control signal lines (such as clock signals CLX, CLX', CLY, and CLY') interfering with image signal lines (VID1 to VID12). Ex. 1005, ¶¶[0005]-[0008],

¶¶[0086]-[0087], ¶[0100]; Ex. 2001, ¶76. *Muraide* attempts to achieve this goal in two ways. *Id.* First, it provides a shield, such as an aluminum film, around the image signal lines VID1 to VID12. Ex. 1005, ¶¶[0086]-[0087]; Ex. 2001, ¶76. Second, it arranges its wiring lines to provide voltage supply lines between the clock signal lines (CLX, CLX', CLY, and CLY') and the image signal lines (VID1 to VID12). Ex. 1005, ¶[0100]; Ex. 2001, ¶76.

In sum, *Muraide* teaches a specific layout of substrates, driving circuits, external terminals, and wiring lines—and a fabrication process tailored to that specific layout—to achieve its goals. *Muraide*'s layout does not allow reconfiguring its wiring layout without also reconfiguring its entire circuit layout and fabrication process. Ex. 2001, ¶77.

ii. Overview of *Sunao*

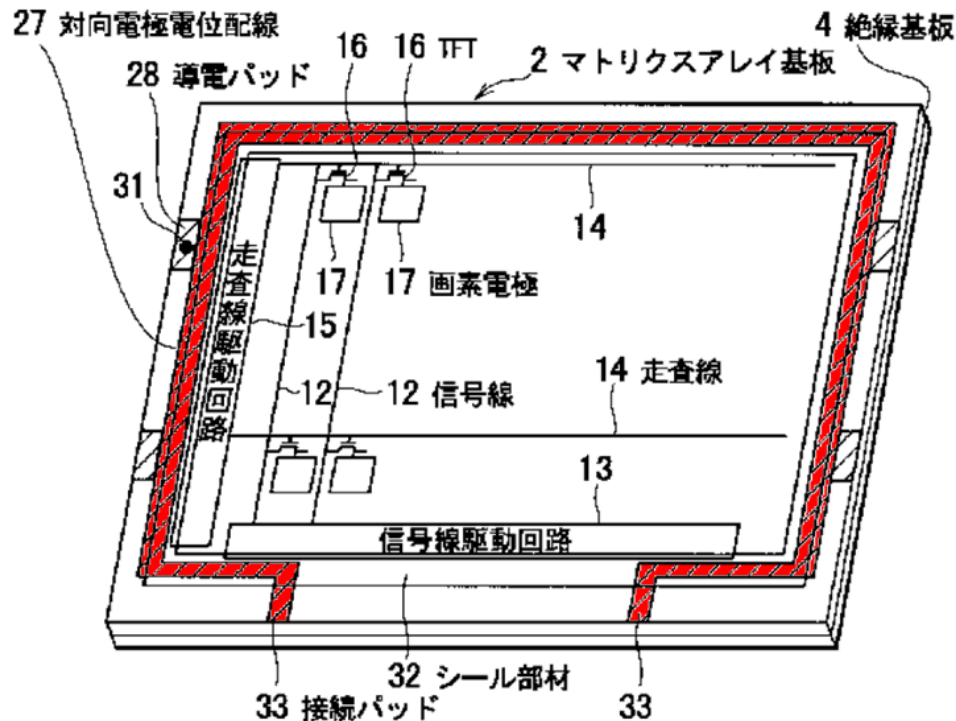
Sunao relates to providing an electrical potential to a counter electrode and to a metal frame surrounding an LCD device. Ex. 1006, Abstract, ¶¶[0007]-[0010]; Ex. 2001, ¶78. *Sunao* does not relate to the layout of wiring lines connected to terminals on the substrate of an LCD device, and therefore does not describe that layout. Ex. 2001, ¶78. *Sunao* explains that prior devices supplied different potentials to a counter electrode and metal frame, and if the two short-circuited, the difference in potential could flow through the counter electrode wiring and damage other components. Ex. 1006, ¶[0005]; Ex. 2001, ¶78. To avoid this issue, prior

devices placed an insulating spacer between the counter electrode and the metal frame, which increased the area of the device in a peripheral region. Ex. 1006, ¶[0006], Fig. 5 (illustrating “insulating spacer 8” between “counter electrode 7” and “metal cover frame 6”); Ex. 2001, ¶78.

Sunao says it solves this problem by supplying the same electrical potential to the frame and the counter electrode instead of different potentials. Ex. 1006, ¶¶[0007]-[0010]; Ex. 2001, ¶79. As a result, *Sunao*’s device can eliminate the insulating spacers present in prior devices and reduce the size of the LCD peripheral region. *Id.*

Sunao thus omits nearly all detail of its wiring layout, because its invention does not relate to that layout. Ex. 2001, ¶80. *Sunao* illustrates only a single wiring line, “counter electrode potential wirings 27,” highlighted in red below, supplied by “connection pad 33,” and does not illustrate any other wiring lines supplying “signal line driving circuit 13” or “scanning line drive circuit 15” or terminals to supply such lines:

【図 3】



Ex. 1006, Fig. 3 (emphasis added), ¶[0014], ¶[0018]; Ex. 2001, ¶80.

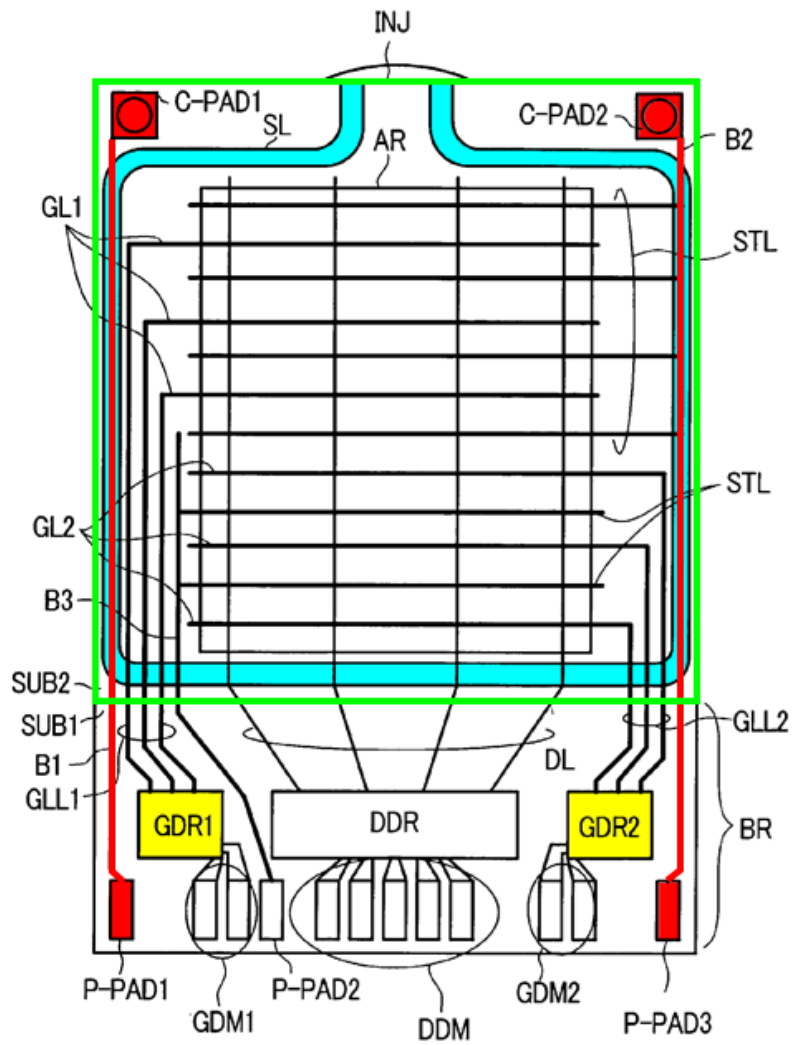
Sunao thus does not disclose where “counter electrode potential wirings 27” or “connection pad 33” reside relative to any other terminals or wiring lines that supply scanning line or data line driving circuits. Ex. 2001, ¶81. It describes only one line outside the display region. Ex. 1006, Fig. 3, ¶[0014], ¶[0018]; Ex. 2001, ¶81.

iii. Overview of *Komeno*

Komeno describes an LCD device in which scanning line driving circuits and data line driving circuits all reside in the peripheral region on the same side (the bottom side) of the substrate. Ex. 1009, ¶¶[0103]-[0104], Fig. 1; Ex. 2001,

¶82. *Komeno*, like *Muraide*, places its scanning line driving circuits (“gate line driving circuits” “GDR1” and “GDR2,” highlighted in yellow, below) outside the LCD seal (“sealing member SL,” highlighted in blue). *Id.* *Komeno*’s counter substrate (“second substrate SUB2,” outlined in green) aligns with its sealing member. *Id.* As a result, *Komeno*’s vertical conductive terminals (“counter electrode connection pads C-PAD1, C-PAD2,” highlighted in red) must reside in the same planar region as the seal to connect to the counter substrate. Ex. 1009, ¶[0108], ¶[0110], Fig. 1; Ex. 2001, ¶82. *Komeno* provides “common lines B1, B2” (also red) to carry an electrical potential from “feeding pads P-PAD1, P-PAD3” (red) to “counter electrode connection pads C-PAD1, C-PAD2.” *Id.*

FIG. 1



Ex. 1009, ¶¶[0103]-[0104], ¶[0108], ¶[0110], Fig. 1 (emphasis added); Ex. 2001, ¶82.

- iv. **The Petition does not establish any likelihood that *Muraide*, *Sunao*, or *Komeno* teach “the plurality of main wiring lines being made of a same conductive film,” as recited in ’390 claim 1.**

Muraide does not teach “the plurality of main wiring lines being made of a same conductive film,” as recited in ’390 claim 1. Claim 1 recites “a counter electrode potential line . . . , which is at least one of the plurality of main wiring lines” and “the plurality of main wiring lines being made of a same conductive film.”

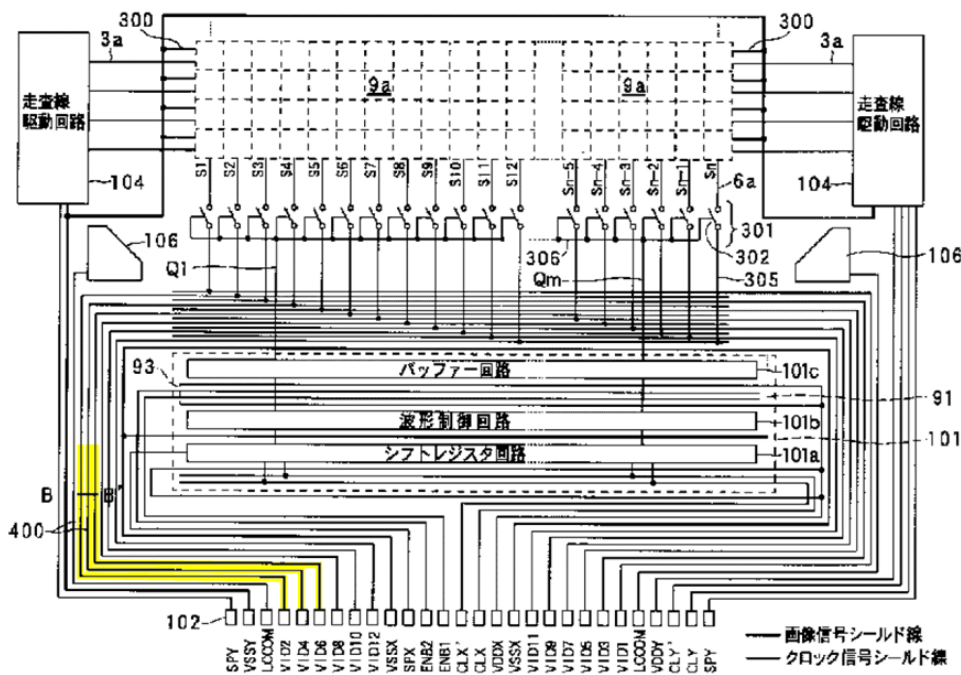
Muraide does not teach the material used for “wiring 400 (LCCOM),” which the Petition identifies as the claimed “counter electrode potential line.” Pet., 18; Ex. 1005, ¶[0085]; Ex. 2001, ¶¶88-95. It also does not teach that “wiring 400 (LCCOM)” is made of the same material as image signal lines “wirings 400 (VID1) to 400 (VID12),” which the Petition relies on as the other “main wiring lines” allegedly satisfying the “plurality of main wiring lines” in claim 1. Pet., 18; Ex. 1005, ¶[0087]; Ex. 2001, ¶¶88-93.

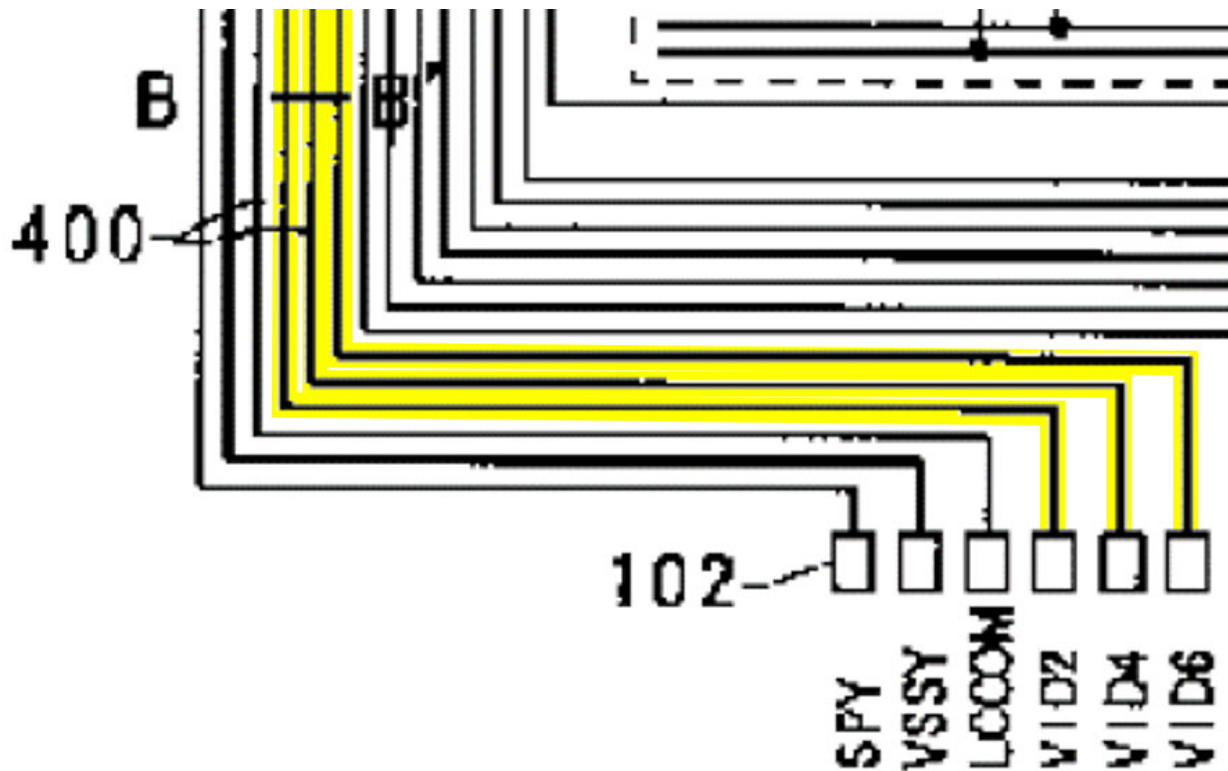
Muraide instead specifies only that certain “wirings 400”—the image signal lines—are made of the same film: “the wirings 400 (VID1) to 400 (VID12) that are image signal lines are made of the same conductive film (for example, a multilayer film including a conductive polysilicon film and a conductive metal silicide film)

as the capacitance lines 300 in the image display region.” Ex. 1005, ¶[0087]; Ex. 2001, ¶88-93.

Muraide remains silent as to the material used for the alleged “counter electrode potential line,” “wiring 400 (LCCOM).” Ex. 1005, ¶¶[0085], [0087]; Ex. 2001, ¶94. None of the cross-sections in Figures 5-10 illustrate “wiring 400 (LCCOM)” —they illustrate only “wirings 400 (VID1) to 400 (VID12).” Ex. 1005, ¶[0087], Figs. 5-10; Ex. 2001, ¶91. *Muraide*’s “FIGS. 5 to 10 are cross-sectional views taken along line B-B’ of FIG. 4,” Ex. 1005, ¶[0077], and line B-B’ crosses only lines VID2, VID4, and VID6 (partially highlighted in yellow to show the scope of line B-B’) and does not cross LCCOM:

【図4】





Id., Fig. 4 (emphasis added); Ex. 2001, ¶91.

The Petition does not assert that a POSITA would necessarily infer that the common nomenclature “wiring(s) 400” means all such wirings are made of the same conductive film. Pet., 17. Petitioner’s expert mimics the Petition and thus also does not provide any evidence of such necessary inference. Ex. 1002, ¶68. Without such evidence, the Petition cannot establish any likelihood of success. *See Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192 (Fed. Cir. 2003) (“A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present.”).

A POSITA could not draw such an inference by necessity because *Muraide* teaches making different “wiring(s) 400” from different materials. Ex. 1005, ¶[0104], Ex. 2001, ¶¶88-93. For example, *Muraide* contemplates forming “the wiring 400 (CLX), [and] the wiring 400 (CLY) . . . from one of the four conductive films” and forming “the wiring 400 (VID 1), [and] the wiring 400 (VID 2) . . . from another one of the four conductive films.” Ex. 1005, ¶[0104], Ex. 2001, ¶92.

Muraide’s silence as to “wiring 400 (LCCOM),” its suggestion of making different “wiring(s) 400” from different materials, and the Petition’s corresponding lack of evidence as to the material used for “wiring 400 (LCCOM)” demonstrate that the Petition does not establish any likelihood that *Muraide* teaches “the plurality of main wiring lines being made of a same conductive film,” as recited in ’390 claim 1. Ex. 2001, ¶¶88-95. All other ’390 claims depend from claim 1. The Petition does not rely on any other reference to supply this missing element, and therefore it has not established any likelihood of success for any claim under Ground 1.

- v. **The Petition does not establish any likelihood that *Muraide* in combination with *Sunao* or *Komeno* teach “the plurality of main wiring lines . . . being planarly laid out so as not to intersect each other in the peripheral region; and the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines,” as recited in ’390 claim 1.**

Combining *Muraide* with the teachings of *Sunao* or *Komeno* would not produce the wiring layout recited in ’390 claim 1. Claim 1’s layout requires at least two elements. First, “the plurality of main wiring lines,” including “a counter electrode potential line,” must be “planarly laid out so as not to intersect each other in the peripheral region.” Ex. 1001, 22:1-12. Second, “the counter electrode potential line” must be “closest to edges of the element substrate, among the plurality of main wiring lines.” *Id.*

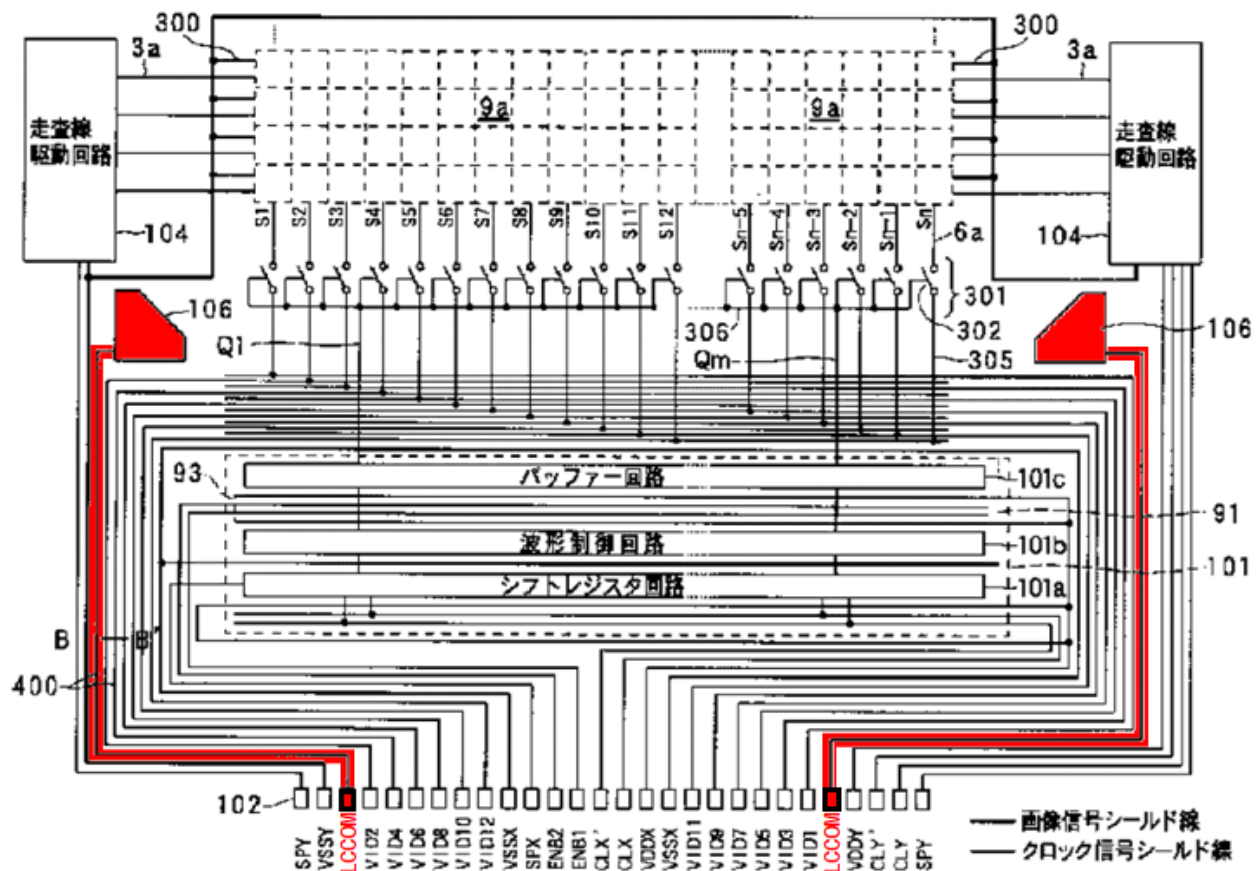
Modifying *Muraide*’s layout based on *Sunao* or *Komeno* would not satisfy both of these limitations.

First, *Muraide*’s deficiencies. As the Petition concedes, *Muraide* does not teach “the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines.” Pet., 19. Instead, *Muraide* teaches placing all wiring lines that supply scanning line driving circuit 104 closer to the edge of its substrate than “wiring 400 (LCCOM),” the alleged “counter

electrode potential line.” Pet., 17; Ex. 1005, Fig. 4, ¶[0085]; Ex. 2001, ¶¶103-110.

Muraide’s Figure 4 illustrates LCCOM, highlighted here in red:

【図4】



Ex. 1005, Fig. 4 (emphasis added), ¶[0085]; Ex. 2001, ¶75. All of the wirings that supply “scanning line driving circuit 104”—SPY, VSSY, VDDY, CLY’, and CLY—reside closer to the edge of “TFT array substrate 1” than LCCOM. Ex. 1005, Fig. 4, ¶[0085]; Ex. 2001, ¶107. *Muraide* thus does not disclose “the counter electrode potential line being closest to edges of the element substrate, among the

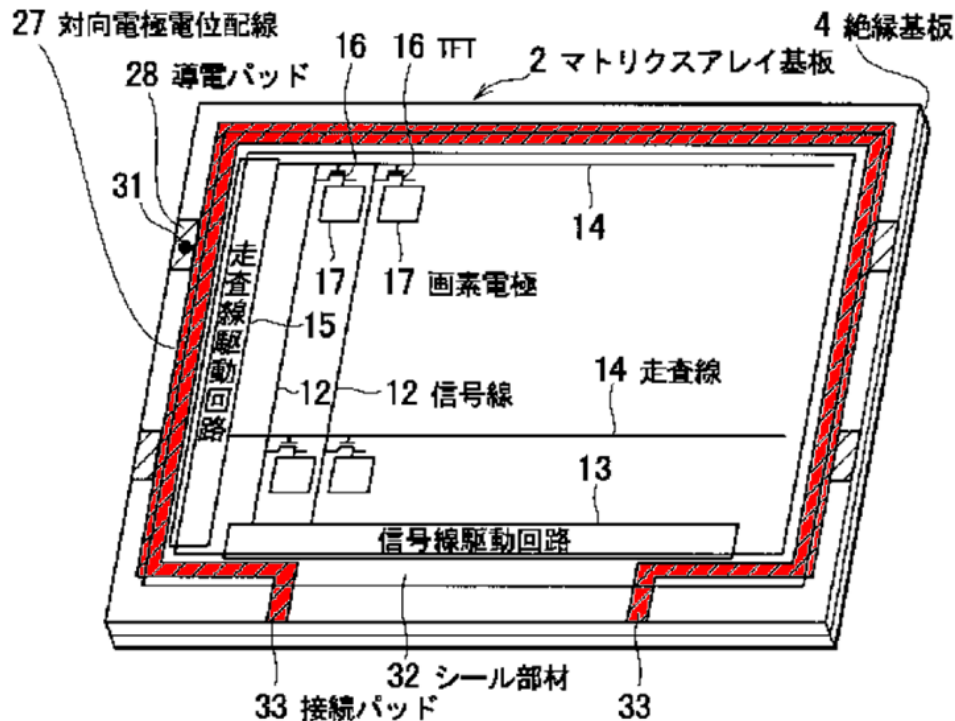
plurality of main wiring lines” that include wiring lines with “peripheral driving circuits coupled to” their ends. Ex. 2001, ¶¶103-110.

The Petition thus relies on *Sunao* or *Komeno*, alternatively, to supply this (and only this) element. Pet., 19-24. But neither reference cures *Muraide*’s deficiency.

Sunao

Sunao does not supply this missing element. Ex. 2001, ¶111. It does not teach “the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines,” because *Sunao* does not describe the layout of any line in a peripheral region except the alleged counter electrode potential line. Ex. 1006, Fig. 3, ¶[0014], ¶[0018]; Ex. 2001, ¶111. The Petition contends that *Sunao*’s “counter electrode potential wirings 27” discloses the claimed “counter electrode potential line,” relying on *Sunao*’s Figure 3. Pet., 20. The Petition omits that Figure 3 illustrates *only* that line (highlighted below in red) and not its position relative to any other wiring lines:

【図 3】



Ex. 1006, Fig. 3 (emphasis added), ¶[0014], ¶[0018]; Ex. 2001, ¶¶80-81, ¶111.

Illustrating a single line does not disclose a “line closest to edges . . . among the plurality of main wiring lines.” Ex. 2001, ¶¶80-81, ¶111. The Petition provides no evidence to address this absence from *Sunao*. Pet., 20-22. It does not describe any other alleged “main wiring lines” in *Sunao* or their layout relative to “counter electrode potential wirings 27.” *Id.* Instead the Petition relies only on an assumption, without any cited evidence, that “Figure 3 of *Sunao* teaches a counter electrode potential line 27 that is nearest to the edges of the element substrate of the main wiring lines.” *Id.*, 21. As shown above, *Sunao*’s Figure 3 does not illustrate any other wiring lines and thus does not teach “wirings 27” nearer the

edge of the substrate than any other lines. Ex. 1006, Fig. 3, ¶¶[0014], ¶¶[0018]; Ex. 2001, ¶¶80-81, ¶111.

The Petition also describes *Sunao*'s "scanning lines 14" and "signal lines 12," but it does not assert that those satisfy the '390 claims' "main wiring lines." Pet., 20. They cannot, because they reside only in *Sunao*'s image display region and have no connection to external terminals. Ex. 1006, ¶¶[0013]-[0015]. Thus, they do not satisfy '390 claim 1's requirements that the "main wiring lines" reside "in a peripheral region of the image display region on the element substrate" and "each hav[e] one end coupled to each of [a] plurality of external circuit connection terminals." Ex. 1001, 21:55-64.

Sunao therefore does not cure *Muraide*'s lack of a "counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Ex. 2001, ¶111. The Petition has not provided evidence that the combination of *Muraide* and *Sunao* renders obvious '390 claim 2 or its dependent claim 3.

Komeno

The Petition also relies, in the alternative, on *Komeno* to fill the gap in *Muraide*. Pet., 22-24. The Petition does not, however, provide any evidence or analysis that the proposed combination of *Muraide* and *Komeno* would provide "the plurality of main wiring lines . . . planarly laid out so as not to intersect each

other in the peripheral region.” *Id.* Patent Owner assumes, for purposes of this POPR only, that *Komeno* teaches “the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines,” as the Petition asserts. *Id.* Even so, the Petition does not explain how modifying *Muraide* to incorporate that teaching from *Komeno* would result in wiring lines that do not intersect. *Id.* It would not. Ex. 2001, ¶¶103-110.

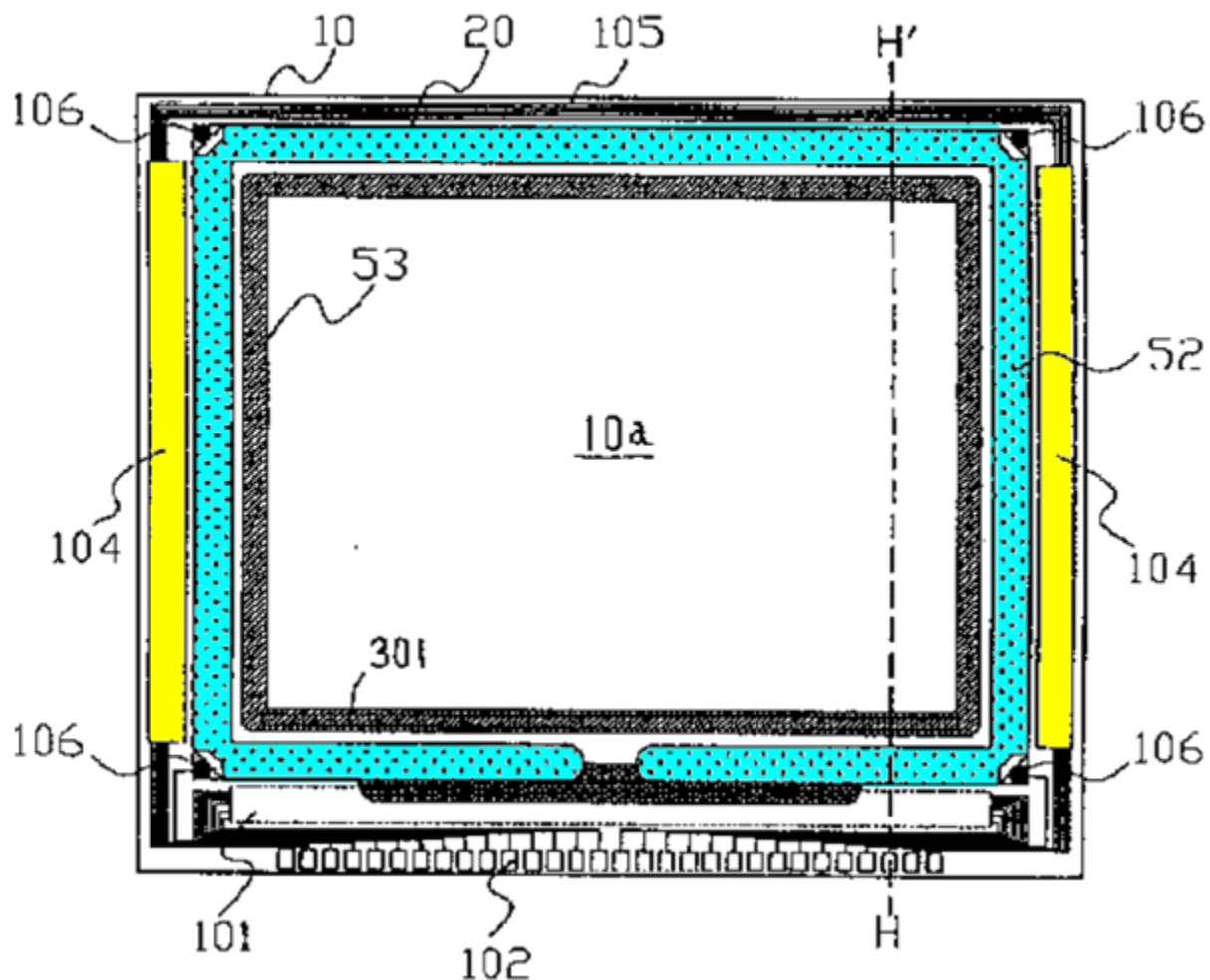
Both *Muraide* and *Komeno* include a critical teaching that the Petition does not address. Their circuits for driving the scanning lines in the LCD display area reside *outside* the seal region and corresponding area of the counter electrode that the counter potential line supplies with a counter potential. Ex. 1005, ¶¶[0076]-[0078], ¶[0085], ¶¶[0105]-[0106], Fig. 4, Fig. 11, Fig. 12; Ex. 1009, ¶¶[0103]-[0104], ¶[0108], ¶[0110], Fig. 1; Ex. 2001, ¶¶71-75, ¶82, ¶¶104-106, ¶112.

Accordingly, the conductive terminals that connect the substrates—the terminals that connect to the counter electrode potential line on one substrate to supply a counter potential to the counter substrate—also must reside closer to the pixel region than the scanning line driving circuits. *Id.*

As a result of this layout, modifying *Muraide* as the Petition suggests—by moving the counter potential line to the position nearest the edge of the substrate—results in intersecting lines and thus does not satisfy “the plurality of main wiring

lines . . . being planarly laid out so as not to intersect each other in the peripheral region,” as claimed. Ex. 2001, ¶¶103-113.

Muraide’s Figure 11 illustrates the relevant arrangement of circuits, lines, and terminals. Its “sealing material 52, highlighted below in blue, lies “along an edge of the TFT array substrate 10.” Ex. 1005, ¶[0106], Fig. 11; Ex. 2001, ¶72, ¶107. Its “scanning line driving circuit 104,” highlighted in yellow, lies “[i]n a region outside the sealing material 52.” Ex. 1005, ¶[0106], Fig. 11; Ex. 2001, ¶72. *Muraide*’s “vertical conductive material 106” that supplies a counter potential to the counter substrate—and thus must connect to the counter potential line, LCCOM—lies “in at least one position of a corner portion of the counter substrate 20.” Ex. 1005, ¶[0106], Fig. 11; Ex. 2001, ¶73.

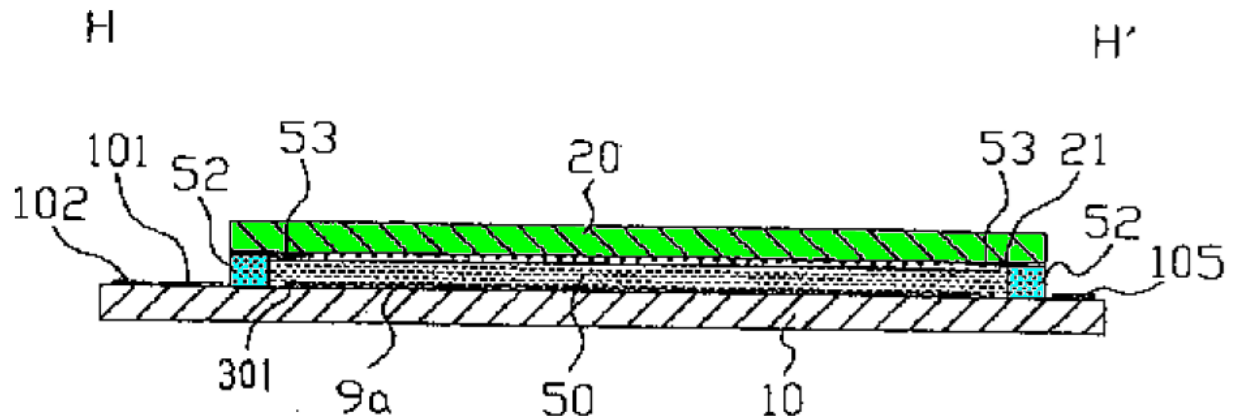


Ex. 1005, ¶[0106], Fig. 11 (emphasis added).

Muraide's "counter substrate 20" extends only to "substantially a same contour as the sealing material 52." Ex. 1005, ¶[0106]. This means *Muraide*'s vertical conductive terminals must reside closer to the TFT array than its "scanning line driving circuit 104." *Id.*; Ex. 2001, ¶¶104-107. The counter substrate does not extend any further in plan view. Ex. 1005, ¶[0106]; Ex. 2001, ¶¶104-107. *Muraide* provides a cross-sectional view in Figure 12 that shows the alignment of the edge

of “counter substrate 20” (highlighted in green) and “sealing material 52” (highlighted in blue):

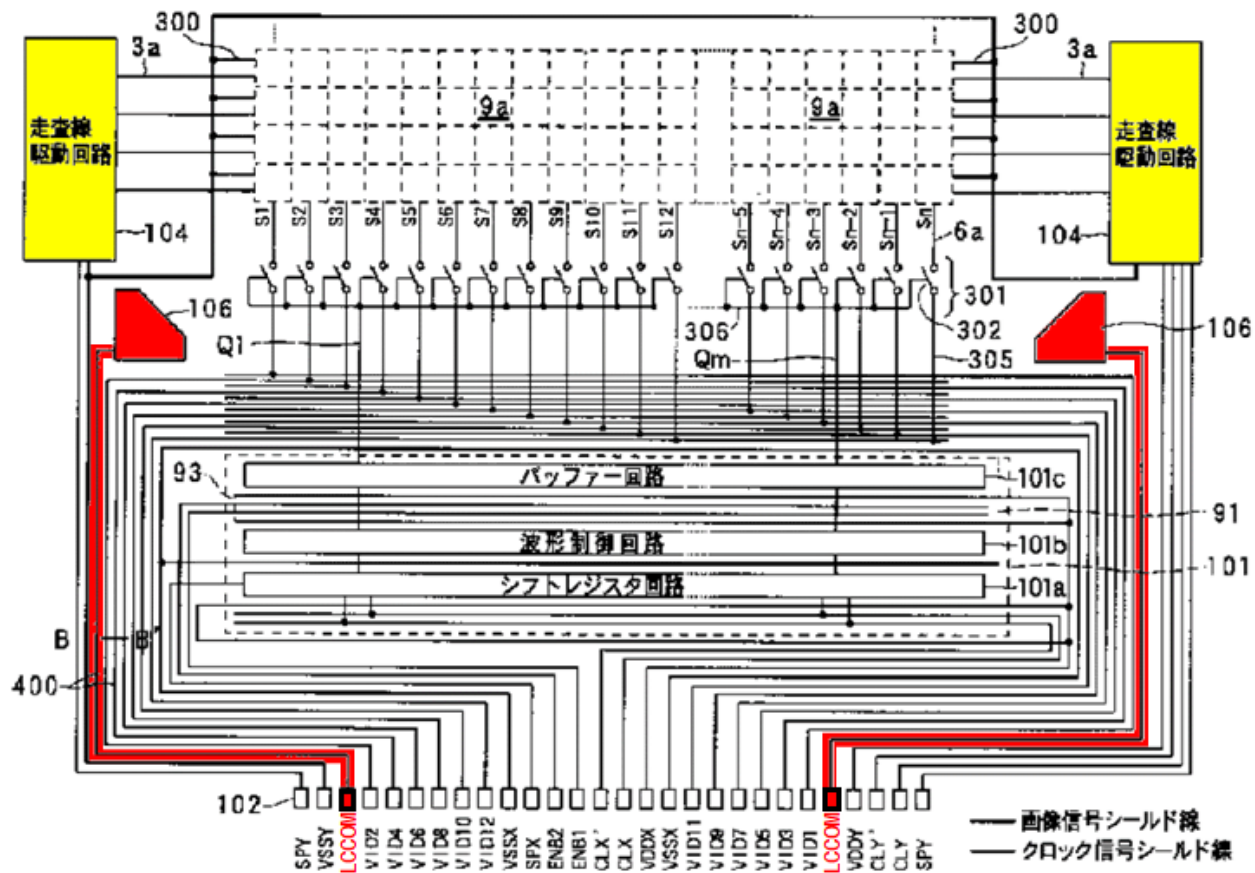
【図 1 2】



Ex. 1005, Fig. 12 (emphasis added), ¶[0106]; Ex. 2001, ¶74, ¶106.

Muraide’s Figure 4 likewise illustrates “scanning line driving circuit[s] 104,” highlighted in yellow, closer to the edge of the element substrate than “vertical conductive terminals 106,” which LCCOM supplies with a constant electric potential (highlighted in red). Ex. 1005, ¶[0085], ¶[0106], Fig. 4, Fig. 11; Ex. 2001, ¶75.

【図4】

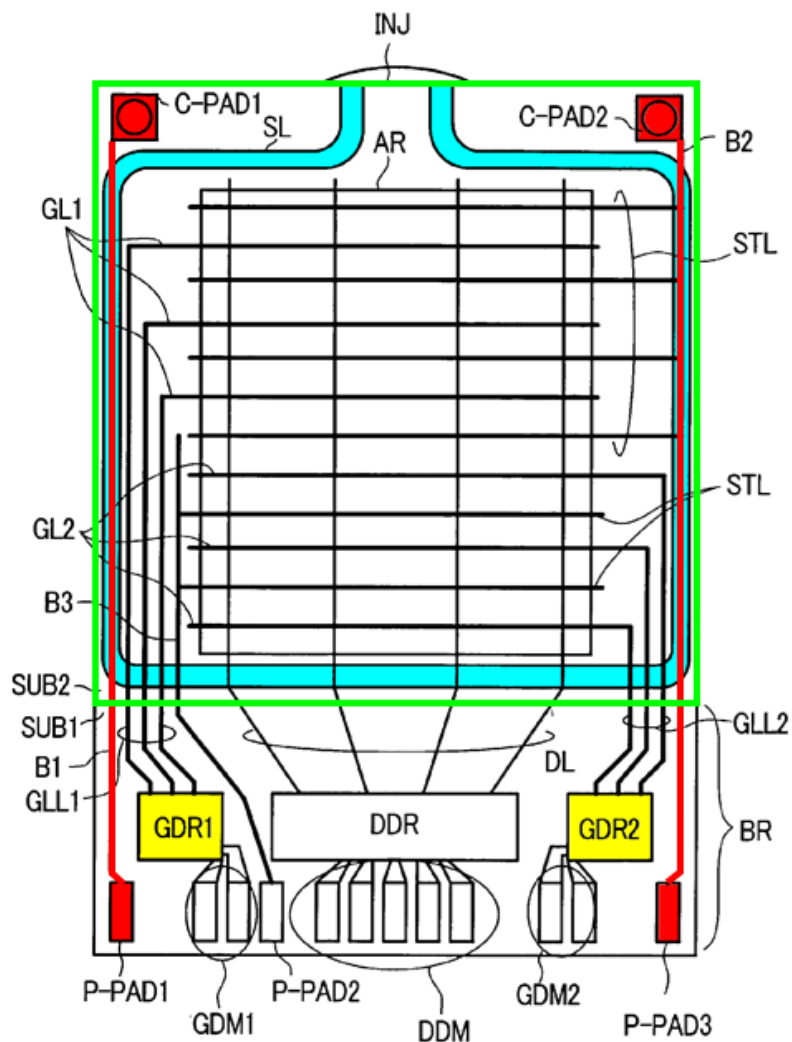


Ex. 1005, Fig. 4 (emphasis added).

Komeno has the same relative layout of scanning line driving circuits, counter substrate, sealing material, and conductive terminals as *Muraide*. *Komeno*, like *Muraide*, places its scanning line driving circuits (which *Komeno* calls “gate line driving circuits” “GDR1” and “GDR2,” highlighted in yellow, below) outside its “sealing member” (“SL,” highlighted in blue). Ex. 1009, ¶[0103]-[0104], Fig. 1; Ex. 2001, ¶82, ¶112. *Komeno* locates these circuits at the bottom of the substrate,

instead of at the sides as in *Muraide*. *Id.* Komeno also aligns the edges of its counter substrate (“second substrate SUB2,” outlined in green) with its sealing member, so its vertical conductive terminals (“counter electrode connection pads C-PAD1, C-PAD2,” highlighted in red) must reside in the same planar region as the seal to connect to the counter substrate. Ex. 1009, ¶[0108], ¶[0110], Fig. 1; Ex. 2001, ¶82. *Komeno* provides “common lines B1, B2” (also red) to carry a potential from “feeding pads P-PAD1, P-PAD3” (red) to “counter electrode connection pads C-PAD1, C-PAD2.” *Id.*

FIG. 1



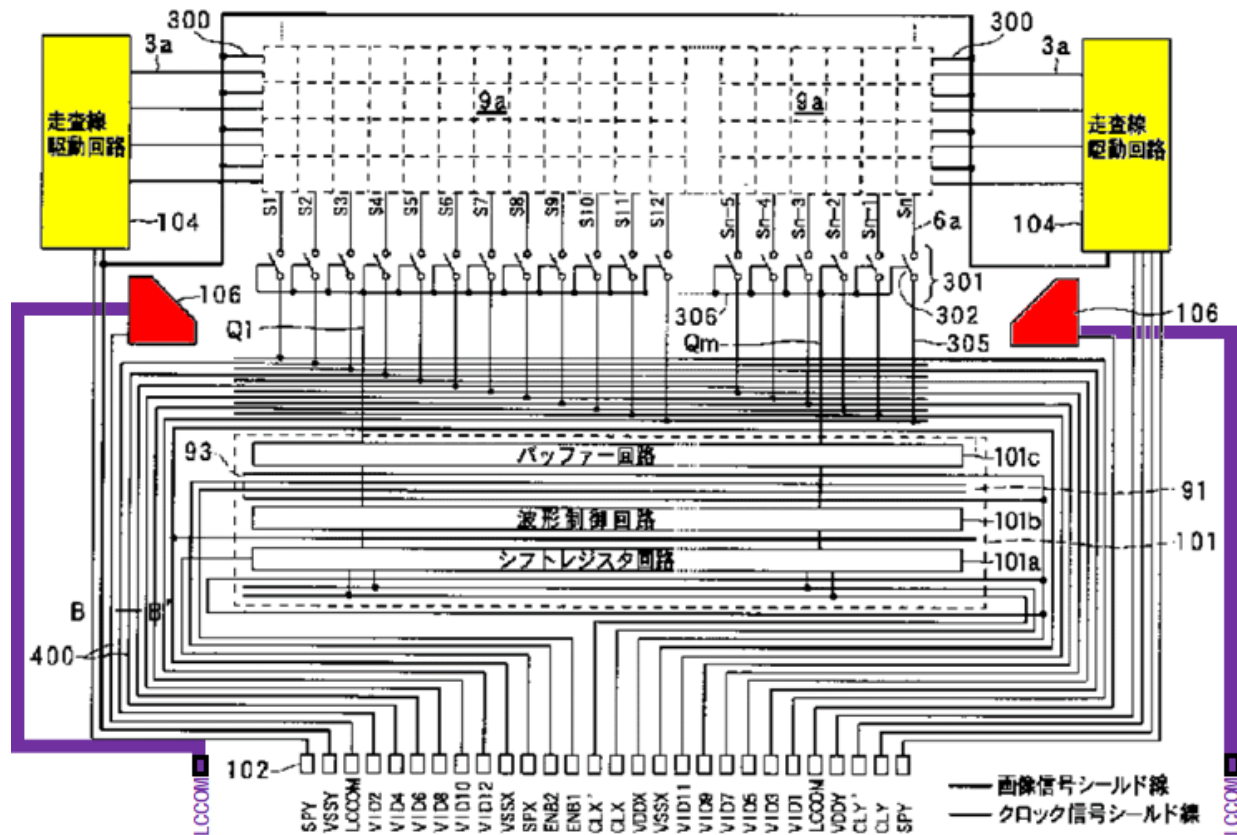
Ex. 1009, Fig. 1 (emphasis added); Ex. 2001, ¶82, ¶112.

Both *Muraide* and *Komeno* therefore locate the scanning line driving circuits *outside* the area of the counter substrate. A POSITA integrating the teachings of *Muraide* and *Komeno* would have no basis (and the Petition asserts none) to relocate the scanning line driving circuits within the area of the counter substrate. Ex. 2001, ¶113. These teachings from both references mean that rearranging

Muraide's external terminals to place the counter electrode potential line nearest the edge, as the Petition alleges *Komeno* teaches, would result in intersecting lines. Ex. 2001, ¶¶103-113.

Relocating *Muraide*'s LCCOM terminals to place them nearer the edge of the substrate than the terminals supplying the scanning line driving circuits 104 would necessarily require the LCCOM lines to intersect with at least the SPY, VSSY, VDDY, CLY, and CLY' lines supplying those circuits due to the placement of those circuits outside the vertical conductive terminals 106 supplying the counter substrate. Ex. 1005, Fig. 4; Ex. 2001, ¶107. Patent Owner has illustrated that necessary outcome here, showing hypothetical relocated LCCOM terminals and lines in purple, with the disclosed vertical conductive terminals 106 remaining in red and the scanning line driving circuits 104 in yellow:

【図4】



Ex. 1005, Fig. 4 (yellow and red emphasis added; purple modifications added); Ex. 2001, ¶107. Even if LCCOM was placed closer to the edge of the substrate than one of the supply lines for the scanning line driving circuit, such as VSSY, LCCOM would still have to cross that line to reach the vertical conductive terminal 106. *Id.*

The combination of *Muraide* and *Komeno* thus does not disclose “the plurality of main wiring lines . . . being planarly laid out so as not to intersect each other in the peripheral region,” as claimed. Ex. 2001, ¶¶103-113. Although an

obviousness analysis does not require bodily incorporation of references, the Petition must explain, with evidentiary support, “*how* or *why*” the proposed combination would arrive at the claimed invention without improper hindsight. *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016) (emphasis original; quotations omitted); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“The petitioner must . . . articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”). The Petition does not explain or provide evidentiary support for “*how* or *why*” the combination of *Muraide* with a counter potential line nearest the edge of the substrate—as a “design choice” or as allegedly disclosed in *Sunao* or *Komeno*—would satisfy all elements of ’390 claim 1. The Petition’s mere suggestion to move the counter potential line does not explain or provide evidence how or why the modification would satisfy the other elements of the ’390 claims.

Nowhere does the Petition suggest modifying *Muraide* based on *Sunao* or *Komeno* except for the alleged “design choice” of relocating the counter electrode potential line relative to the other wiring lines. Pet., 19 (describing alleged “design choice”), 20-22 (addressing *Sunao*), 22-24 (addressing *Komeno*). The Petition contains no analysis or evidence suggesting modifying the layout of *Muraide* in any other way, based on *Sunao*, *Komeno* or otherwise, any motivation to do so, or how a POSITA would reasonably expect success in such modifications. *Cf.*

Personal Web Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (finding obviousness analysis deficient for absence of explanation or evidence of *how* a combination would work).

This omission from the Petition’s analysis of *Muraide* and *Komeno* demonstrates that the location of the counter electrode potential line is not a “mere design choice.” The Petition provides no evidence for this alleged “design choice” except its expert’s conclusory opinion, unsupported by evidence and mirroring the Petition. Pet., 19 (citing Ex. 1002, ¶70); Ex. 1002, ¶70 (repeating language from Pet., 19). Such testimony, which “offer[s] conclusory assertions without underlying factual support and repeat[s]” the Petition’s arguments, carries “little weight.” *ByteMark, Inc. v. Xerox Corp.*, IPR2022-00624, Paper 12, at 5 (PTAB Feb. 10, 2023) (citing *In re Ethicon, Inc.*, 844 F.3d 1344, 1348, 1352 (Fed. Cir. 2017); *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019)); 37 C.F.R. § 42.65(a).

The evidence from the asserted *Muraide* and *Komeno* references discussed above—and not addressed by the Petition—indicates that the placement of the counter potential line is not a “mere design choice” and instead consists of only one part of an integrated novel and non-obvious layout recited in ’390 claim 1. Even if the Petition had introduced evidence establishing the location of the counter potential line as a “mere design choice,” the Petition has not addressed any

of the other design modifications necessary to transform *Muraide* or *Komeno* into the layout recited in '390 claim 1 or cited any evidence indicating how a POSITA would have chosen to make such modifications without using '390 claim 1 as a guide.

The combinations alleged in Ground 1 do not disclose “the plurality of main wiring lines . . . being planarly laid out so as not to intersect each other in the peripheral region,” as recited in '390 claim 1. Ex. 2001, ¶¶103-113. All other '390 claims depend from claim 1. The Petition does not rely on any other reference to supply this missing element, and therefore it has not established any likelihood of success for any claim under Ground 1.

- vi. The Petition does not establish that the Office erred, during prosecution, in evaluating and allowing the claims in view of *Muraide* and a reference, *Kaito*, that contains substantially the same disclosure as the Petition relies on from *Sunao* and *Komeno*.**

The Board may deny institution under § 325(d) because during prosecution the Office considered *Muraide* and the *Kaito* reference (JP10-253984, Ex. 1004, 224-241) that contains the same disclosure the Petition relies on as the sole teaching necessary to render the '390 claims obvious in view of *Muraide*: a counter potential line nearest the edge of the substrate. Pet., 2 (“For example, *Sunao*,

Fujikawa and *Komeno* all disclose a counter electrode potential line being closest to the edges of an element substrate.”).

The Director may elect not to institute if the Petition depends on matters previously presented to the Office. 35 U.S.C. § 325(d); *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, at 7-11 (PTAB Feb. 13, 2020) (precedential) (“*Advanced Bionics*”). “Previously presented art includes art made of record by the Examiner, and art provided to the Office by an applicant, such as on an Information Disclosure Statement (IDS), in the prosecution history of the challenged patent.” *Id.* at 7-8.

In particular, *Advanced Bionics* provides that the Board should consider, in determining whether to exercise discretion to deny institution:

- (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and
- (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Id. at 8. Under Part 1, the Board evaluates *Becton, Dickinson* factors (a), (c) and (d), and under Part 2, the Board evaluates factors (c), (e), and (f):

(a) the similarities and material differences between the asserted art and the prior art involved during examination;

(b) the cumulative nature of the asserted art and the prior art evaluated during examination;

(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;

(d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;

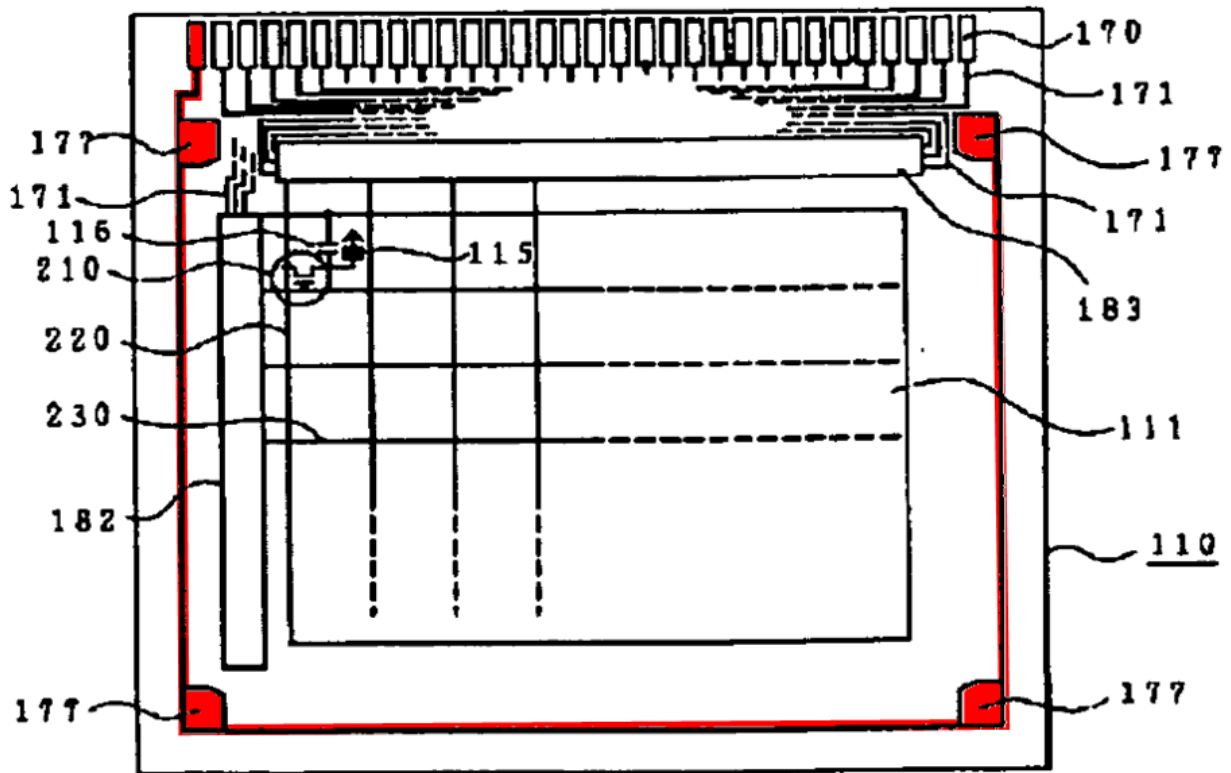
(e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and

(f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of prior art or arguments.

Id. at 10 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, at 17-18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) (“*Becton, Dickinson*”).

The Petition has not established or even asserted that the Office erred in its examination of the ’390 claims. Rather, the Petition asserts that the Office did not have *Sunao* or *Komeno* and thus did not address the Petition’s arguments. Pet., 6-7, 13. The Petition implies that the Office did not consider art teaching a counter potential line nearest the edge of the substrate. *Id.*

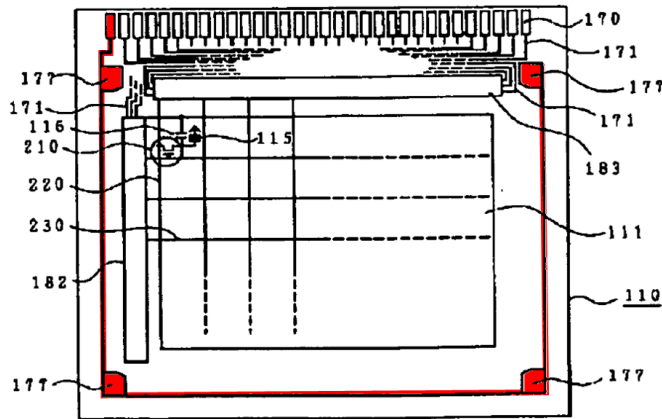
But the Petition does not address *Kaito*, which the Office considered and which discloses a counter potential line nearest the edge of the substrate. *Kaito* locates its vertical conductive terminals, counter potential line, and counter potential conductive terminal nearer the edge of the TFT substrate than any other lines or circuits. Ex. 1004, 227-228 (¶¶[0022]-[0025]), 237 (Figs. 2, 3); Ex. 2001, ¶¶66-68. *Kaito* describes a “contact section 177” for providing electrical contact from a “connection terminal block 170” on a “TFT substrate 110” to a “common electrode 121” on an opposite substrate 120. *Id.* *Kaito*’s Figure 3 illustrates the counter potential path, highlighted in red:



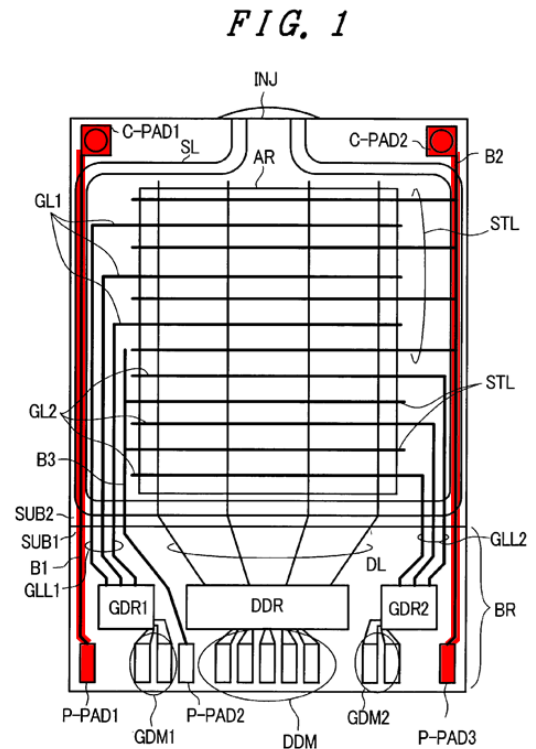
Ex. 1004, 237 (Fig. 3 (emphasis added)), 227-228 (¶¶[0022]-[0025]); Ex. 2001, ¶67.

Kaito's disclosure thus does not differ from *Komeno*'s Figure 1 illustrating a counter potential terminal and line nearer the edge of the TFT substrate than other wires and circuits:

Kaito, Fig. 3 (Ex. 1004, 237)



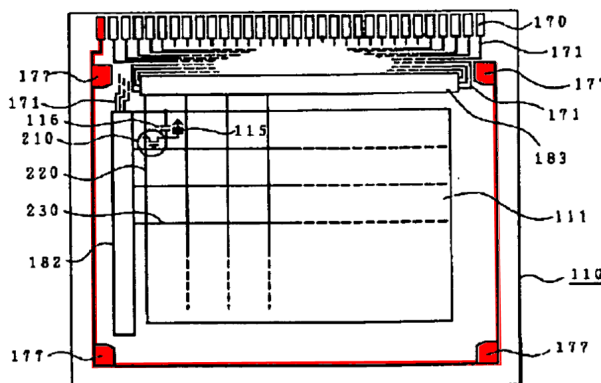
Komeno, Fig. 1 (Ex. 1009)



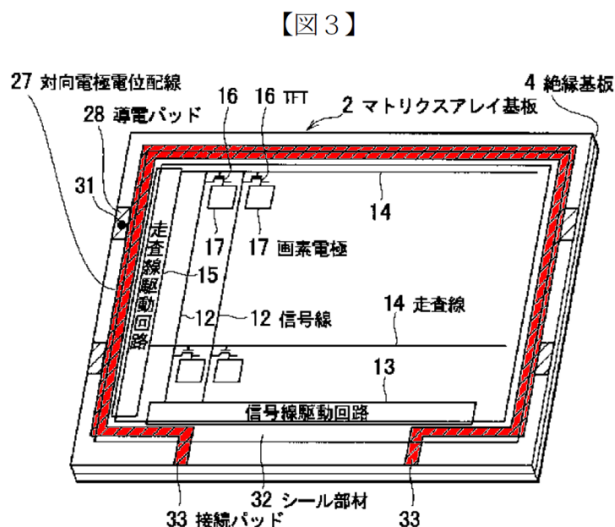
Ex. 1004, 237 (Fig. 3 (emphasis added)); Ex. 1009, Fig. 1 (emphasis added); Ex. 2001, ¶68.

Kaito's disclosure also does not differ from *Sunao*'s (alleged) disclosure of a counter potential line near the edge of the substrate (setting aside that *Sunao* does not disclose the location of any other wiring lines, as discussed above):

Kaito, Fig. 3 (Ex. 1004, 237)



Sunao, Fig. 3 (Ex. 1006)



Ex. 1004, 237 (Fig. 3 (emphasis added)); Ex. 1006, Fig. 3 (emphasis added); Ex. 2001, ¶68.

The '390 applicant disclosed *Kaito*, and the Office considered it. The '390 applicant disclosed *Kaito* in an IDS dated September 14, 2005, *id.*, 103-114, and provided the Examiner with an original (in Japanese) and an English translation. Ex. 1004, 126-127 (IDS), 224-231 (translation), 232-241 (original). The applicant previously had disclosed *Muraide*, with a Japanese original and English translation, in an IDS with the initial '390 application on May 25, 2004. *Id.*, 295-296 (IDS), 404-448 (original and translation).

The Examiner considered *Kaito* and initialed the IDS on November 11, 2005. Ex. 1004, 116. The Examiner then issued a non-final Office Action on November 15, 2005, not relying on *Kaito* but stating that “[t]he prior art made of

record and not relied upon is considered pertinent to applicant's disclosure." *Id.*, 112.

In allowing the claims, the Examiner emphasized the same combination of '390 claim 1 limitations discussed above that any combination of *Muraide*, *Sunao*, and *Komeno* lacks: "the plurality of main wiring lines being made of a same conductive film and being planarly laid out so as not to intersect each other in the peripheral region" and "the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines." Ex. 1004, 8. In short, the Office allowed the claims for the same reasons presented above as to why the Petition has not shown any likelihood of success for Ground 1.

The Office therefore considered both *Muraide* (as the Petition concedes) and a reference that discloses the precise teaching that the Petition contends that *Muraide* lacks: a counter potential line nearest the edge of the substrate. *Muraide* is the same art the Office considered, and *Kaito* is substantially the same as *Sunao* and *Komeno* for purposes of the Petition's arguments because it contains the same teaching that the Petition relies on from those references—there are no material differences. Because the Office previously considered the same and substantially the same art presented in the Petition, and the Petition has not asserted that the Office erred in its evaluation of that art, the Board may deny institution under

§ 325(d). *Advanced Bionics*, IPR2019-01469, Paper 6 at 7-11; *Becton, Dickinson*, IPR2017-01586, Paper 8, at 17-18.

B. Ground 2: The Petition Does Not Establish a Reasonable Likelihood that *Muraide* in View of *Sunao* or *Komeno* and in Further Combination with *Murade III* Renders Unpatentable Claims 2-3 and 12 or that the Office Erred in Its Consideration of *Muraide* and Art Substantially the Same as *Sunao* and *Komeno* During Prosecution.

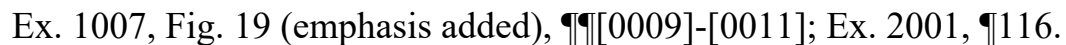
Muraide in combination with *Sunao* or *Komeno* and in further combination with *Murade III* does not render obvious claims 2-3 and 12, which depend from claim 1, for at least the reasons that *Muraide* in combination with *Sunao* or *Komeno* does not disclose all elements of claim 1, as described for Ground 1. The Petition does not assert in Ground 2 that *Murade III* satisfies any limitation of claim 1, Pet. 40-44, and therefore *Murade III* does not cure any of the Petition's deficiencies for claim 1, as discussed above for Ground 1. §V.A.

C. Ground 3: The Petition Does Not Establish a Reasonable Likelihood that *Fujikawa* Anticipates Claims 1-5, 7, 8, 11, and 13 or that the Office Erred in Its Consideration of Art Substantially the Same as *Fujikawa* During Prosecution.

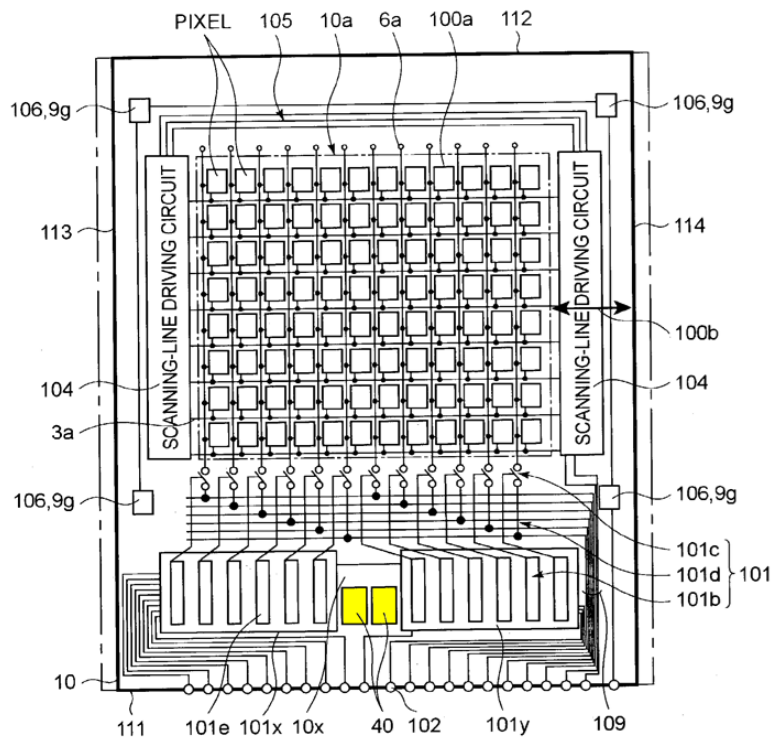
i. Overview of *Fujikawa*

Fujikawa relates to the layout of an LCD device to facilitate the placement of “identification marks” indicating the part numbers of the device and used for quality control during production. Ex. 1007, ¶¶[0009]-[0011]; Ex. 2001, ¶116.

Fujikawa's Figure 19 illustrates "identification marks 40" (highlighted yellow) requiring space in the peripheral region:



58



Ex. 1007, Fig. 2 (emphasis added), ¶¶[0081]-[0083]; Ex. 2001, ¶117.

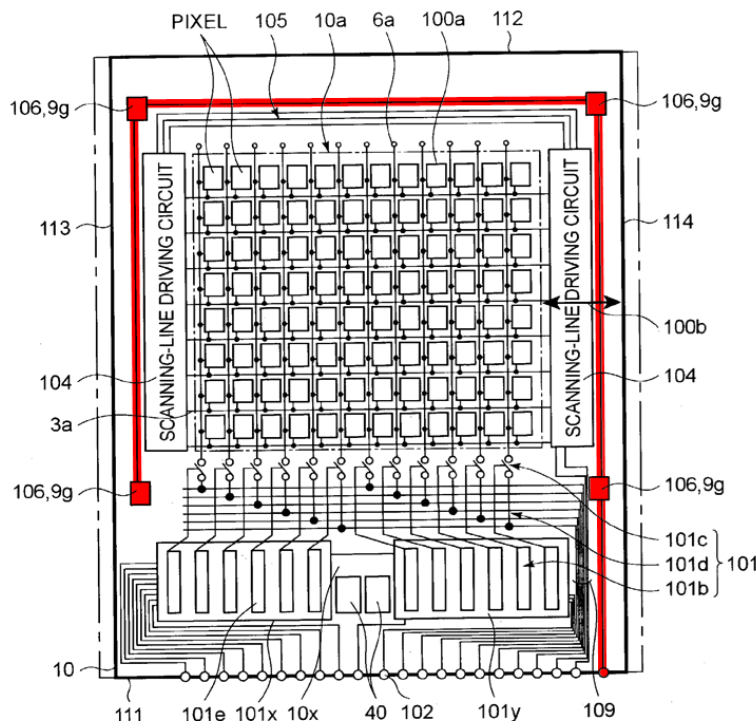
- ii. **The Petition does not establish any likelihood that *Fujikawa* teaches “the plurality of main wiring lines being made of a same conductive film,” as recited in ’390 claim 1.**

Fujikawa, like *Muraide*, does not teach “the plurality of main wiring lines being made of a same conductive film,” as recited in ’390 claim 1. Claim 1 recites “a counter electrode potential line . . . , which is at least one of the plurality of main wiring lines” and “the plurality of main wiring lines being made of a same conductive film.” Ex. 1001, 22:1-12.

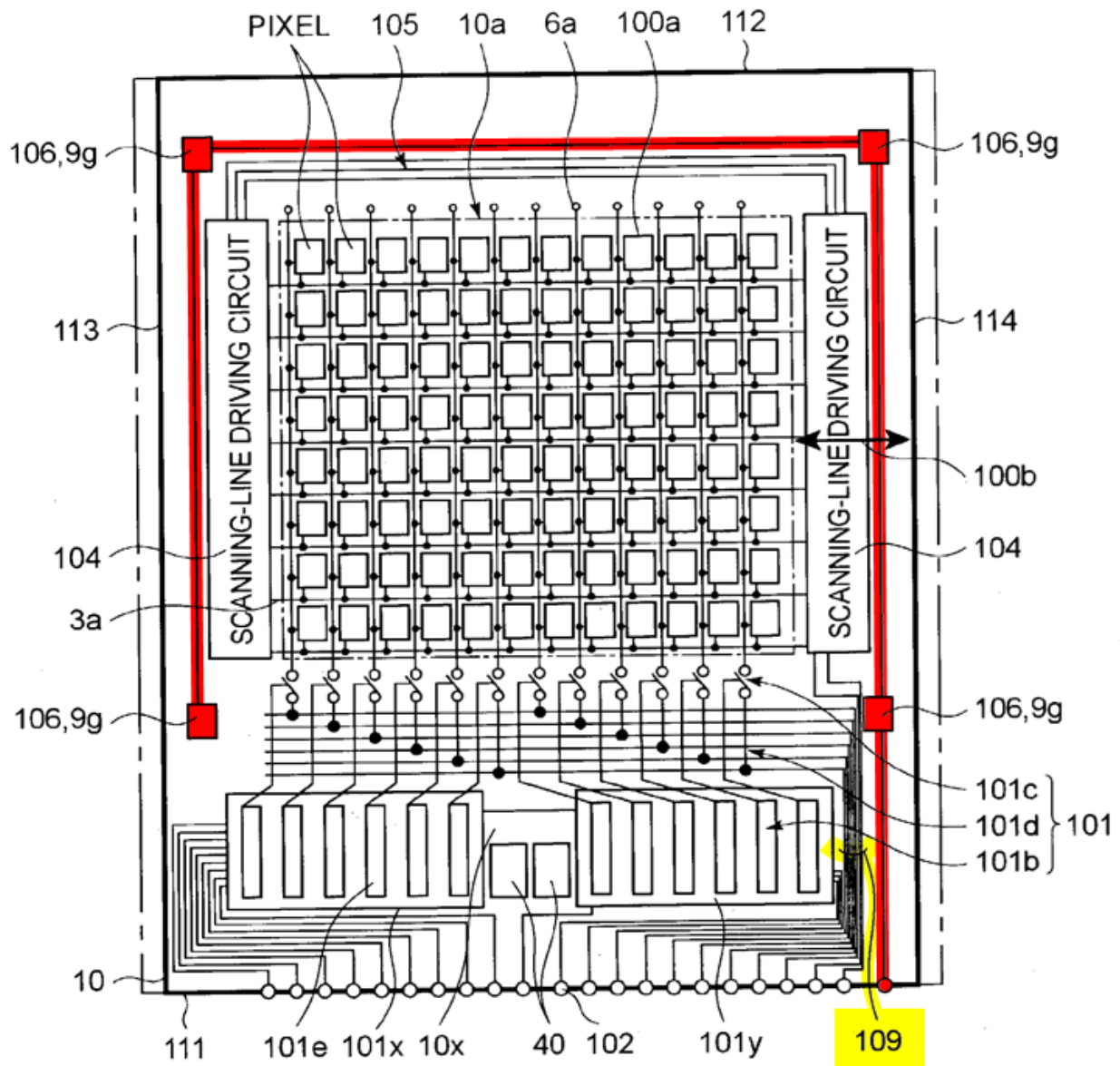
Fujikawa does not teach the material used for the line that provides DCCOM to conductive electrodes 9g and conductive terminals 106, which the Petition identifies as the claimed “counter electrode potential line.” Pet., 47-49; Ex. 1007,

¶¶[0007]-[0008], ¶¶[0079] (describing DCCOM, without reference to material); Ex. 2001, ¶¶122-129. It also does not teach that the line providing DCCOM is made of the same material as the “lines 109” that “transfer voltage and signals from the terminals 102 to a data-line driving circuit 101 and a scanning-line driving circuits 104,” as the Petition asserts. Pet., 45; Ex. 1007, ¶¶[0055]; Ex. 2001, ¶¶122-129.

For the claimed “counter electrode potential line,” the Petition relies on a line that provides “a constant voltage (DCCOM)” through “[c]onductive electrodes 9g” and “conductive materials 106” to a “counter substrate.” Pet., 47-51, 52; Ex. 1007, ¶¶[0009]. *Fujikawa*’s Figure 2, for example, illustrates “[c]onductive electrodes 9g” and “conductive materials 106” and the line connected to them, all highlighted in red:



Ex. 1007, Fig. 2 (emphasis added), ¶¶[0008]-[0009]. For the other claimed “main wiring lines,” the Petition relies on “lines 109 . . . for driving a scanning-line driving circuit 101 and data-line driving circuits 104.” Pet., 45-46; Ex. 1007, ¶[0055]. *Fujikawa*’s Figure 2 identifies these “lines 109” separate from the DCCOM line, as shown with yellow highlighting for the “lines 109” label:



Ex. 1007, Fig. 2 (emphasis added), ¶[0055] (“A plurality of lines 109 made of, for example, a low-resistance metal film, such as an aluminum film, for driving a scanning-line driving circuit 101 and data-line driving circuits 104, are routed from these terminals 102.”); Ex. 2001, ¶124.

Fujikawa, like *Muraide*, remains silent as to the material for the alleged counter potential line supplying DCCOM. Ex. 2001, ¶¶122-127. Both references teach using the same material only for wiring lines supplying the scanning-line and data-line circuits driving the pixel array, and not for a counter potential line. Ex. 1007, ¶[0055]. *Fujikawa* describes only the lines driving those circuits as made of a common film:

A plurality of lines 109 made of, for example, a low-resistance metal film, such as an aluminum film, **for driving a scanning-line driving circuit 101 and data-line driving circuits 104**, are routed from these terminals 102.

Id. (emphasis added); Ex. 2001, ¶122.

This statement describes Figure 2, in which “lines 109” do not include DCCOM, as shown above. Ex. 1007, Fig. 2, ¶[0055]; Ex. 2001, ¶124. In Figure 2, “lines 109” include only lines connected to data line driving circuit 101 and scanning line driving circuits 103. *Id.* The express written disclosure that does not

describe DCCOM and the exclusion of DCCOM from “lines 109” in Figure 2 demonstrate that *Fujikawa* intended to describe only the scanning-line and data-line driving circuit supply lines as made of the same material, and not the DCCOM line. Ex. 1007, Fig. 2, ¶[0055]; Ex. 2001, ¶125.

The Petition does not identify in *Fujikawa* anything except the quote above for *Fujikawa*’s alleged disclosure of ’390 claim limitation “the plurality of main wiring lines being made of a same conductive film.” Pet., 51-52 (citing Ex. 1007, ¶[0055]). The Petition does not explain how or why *Fujikawa*’s description of “lines 109 . . . for driving a scanning-line driving circuit 101 and data-line driving circuits 104” also describes a different line for DCCOM. *Id.*

The Petition also does not identify anything in *Fujikawa* that describes the makeup of the DCCOM line. *Id.* And the Petition omits *Fujikawa*’s statement expressly tying a common material, such as an aluminum film, only to the lines 109 supplying voltages and signals to the circuits driving the pixel array. *Id.*, 51-52 (paraphrasing Ex. 1007, ¶[0055] to omit “for driving a scanning-line driving circuit 101 and data-line driving circuits 104”).

Fujikawa does not teach that the line providing DCCOM constitutes one of “lines 109.” For example, when describing Figures 18 and 19, *Fujikawa* also defines “lines 109” as those that supply the scanning-line and data-line driving circuits:

[0007] As shown in Figs. 18 and 19, scanning-line driving circuits 104 are formed on the periphery of the image display region 10a so that they are connected to the scanning lines 3a, and **a plurality of lines 109 are routed from terminals 102 so as to supply signals to the scanning-line driving circuits 104 and the data-line driving circuit 101.**

Ex. 1007, ¶[0007] (emphasis added). *Fujikawa* then separately, in the next paragraph, describes the line providing DCCOM without calling it a “line 109”:

[0008] Conductive electrodes 9g are formed in the regions on the periphery of the image display region 10a that overlap with the counter substrate 20, and are electrically connected to the counter electrodes of the counter substrate 20 through conductive materials 106 held between the substrates. Therefore, a constant voltage (DCCOM) supplied to the terminals 102 of the TFT array substrate 10 can be supplied to the counter electrodes of the counter substrate 20.

Id., ¶[0008].

This separation of “lines 109” and the line providing DCCOM further indicates that *Fujikawa* does not consider the DCCOM line as one of “lines 109.” In the one other place *Fujikawa* describes DCCOM, it again does not refer to the DCCOM line as one of “lines 109.” Ex. 1007, ¶[0079]. That paragraph describes materials used to make “conductive material 106” (“epoxy resin adhesive component mixed with conductive particles”) and “conductive electrodes 9g” (“ITO film”), but does not describe any material for the DCCOM line. *Id.* A POSITA could not infer that *Fujikawa*’s disclosure necessarily teaches making the line providing DCCOM to terminals 9g with the same material used for “lines 109” supplying the scanning-line and data-line driving circuits. Ex. 2001, ¶¶122-127; *Akamai*, 344 F.3d at 1192 (finding that a possibility or probability of a claim element does not establish inherency).

Fujikawa’s other figures confirm that the description of material used for “lines 109 . . . for driving a scanning-line driving circuit 101 and data-line driving circuits 104” applies only to those specific lines and not DCCOM. Ex. 1007, ¶[0055]. Figures 13, 14, and 15 identify, as “109,” only lines connected to the data-line driving circuit 101 and scanning-line driving circuits 104. Ex. 1007, Figs. 13, 14, 15; Ex. 2001, ¶127.

Fujikawa’s Figures 19 and 12 do not expand the written description of “lines 109” to the DCCOM line. Ex. 2001, ¶126. The label “109” in *Fujikawa*’s Figure

19 may appear to encompass DCCOM, but *Fujikawa* describes Figure 19 as prior art, so the description of the materials used to make “lines 109” in the description of the invention would not apply to Figure 19. Ex. 1007, ¶¶[0003]-[0095] (describing prior art allegedly improved by the invention); Ex. 2001, ¶126. The label “109” in Figure 12 may appear to touch DCCOM at its edge, but *Fujikawa*’s written description of Figure 12 does not describe any material used to make any of the wiring lines. Ex. 1007, ¶¶[0087]-[0091]; Ex. 2001, ¶126.

As a whole, *Fujikawa*’s specification provides no indication that these labels alone intend to extend its express description of the material for the scanning-line and data-line driving circuit “lines 109” to DCCOM as well, and *Fujikawa*’s express written disclosure indicates that “lines 109” do *not* include DCCOM. Ex. 1007, ¶¶[0007]-[0008], [0055]; Ex. 2001, ¶¶122-129.

The Petition does not address any of *Fujikawa*’s teachings indicating that it does not include the DCCOM line in the “lines 109” made of “aluminum film.” Pet., 51-52. It does not explain or provide evidentiary support to establish how a teaching about one set of lines could also describe a different line. *Id.* The Petition therefore has not established any likelihood of prevailing on its assertion that *Fujikawa* anticipates ’390 claim 1 and its dependents. *Fujikawa* does not expressly teach the material used to make its DCCOM line, it does not imply by necessity using the same material to make the DCCOM line and the “lines 109” supplying

the scanning-line and data-line driving circuits, and its teachings indicate that it does not intend to specify the material used for the DCCOM line. Ex. 2001, ¶¶122-129.

The Petition has not established any likelihood that *Fujikawa* discloses the limitation “the plurality of main wiring lines being made of a same conductive film,” as recited in ’390 claim 1. Ex. 2001, ¶¶122-129. All other ’390 claims depend from claim 1. The Petition therefore has not established any likelihood of success for any claim under Ground 3.

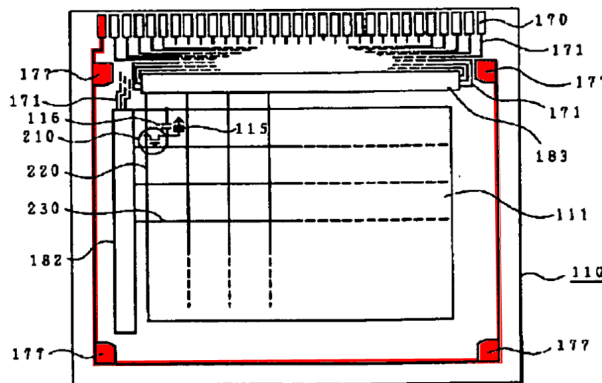
iii. The Petition does not establish that the Office erred, during prosecution, in evaluating a reference *Kaito* that contains the same disclosure as the Petition relies on from *Fujikawa*.

During prosecution, the Examiner considered *Kaito*, which contains the same material disclosure the Petition relies on from *Fujikawa*: a counter potential line nearer the edge of a TFT substrate than other wiring lines. The Board may deny the Petition pursuant to § 325(d).

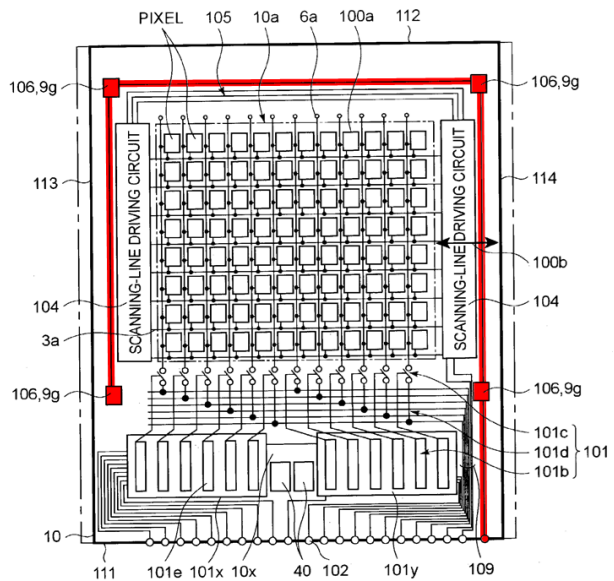
Kaito (discussed above at §V.A.vi) discloses the same layout as *Fujikawa* with respect to the counter potential terminal and counter potential wiring line

placed nearer the edge of the substrate than other wiring lines, as highlighted in red here:

***Kaito*, Fig. 3 (Ex. 1004, 237)**



***Fujikawa*, Fig. 2 (Ex. 1007)**



Ex. 1004, 237 (Fig. 3 (emphasis added)); Ex. 1007, Fig. 2 (emphasis added); Ex. 2001, ¶¶67-68.

Kaito also lacks the same disclosure that *Fujikawa* lacks: *Kaito*, like *Fujikawa*, does not teach the material used to make the counter potential line. The references differ in that *Kaito* does not describe the material used to make any wiring lines, while *Fujikawa* describes using a common film for “a plurality of lines 109 . . . for driving a scanning-line driving circuit 101 and data-line driving circuits 104.” Ex. 1007, ¶[0055].

This distinction does not constitute a material difference between *Kaito* and *Fujikawa* because disclosing what is used to make *other* lines is not material to the patentability of the '390 claims that recite using a particular film to make the *counter potential* line. The Petition does not contain any evidence or argument explaining how *Fujikawa*'s disclosure of the film used to make the scanning-line driving circuit and data-line driving circuit supply lines teaches what is used to make the counter potential line. §V.C.ii. The Petition therefore does not establish that this distinction between *Kaito* and *Fujikawa* is material to patentability for purposes of evaluating § 325(d).

Consistent with these deficiencies, the Examiner emphasized the limitation **“the plurality of main wiring lines being made of a same conductive film** and being planarly laid out so as not to intersect each other in the peripheral region” in allowing the '390 claims. Ex. 1004, 8. The Office considered *Kaito*, and its deficiencies, and emphasized the limitation missing from both *Kaito* and *Fujikawa* to allow the claims.

The Petition also does not argue that the Office erred in its consideration of *Kaito* and allowance of the claims. It does not address the issue at all. The Board therefore may deny the Petition under § 325(d) because the Office already considered art—*Kaito*—substantially the same as *Fujikawa*, it allowed the claims over that art based on the same deficiencies as in *Fujikawa*, and the Petition makes

no attempt to demonstrate the Office erred. *Advanced Bionics*, IPR2019-01469, Paper 6 at 8-11.

D. Ground 4: The Petition Does Not Establish a Reasonable Likelihood that *Murade II* in Combination with *Sunao* or *Komeno* Renders Obvious Claims 1, 4-11 and 13 or that the Office Erred in Its Consideration of Art Substantially the Same as *Murade II*, *Sunao*, and *Komeno* During Prosecution.

i. Overview of *Murade II*

Murade II describes an LCD layout substantially the same as *Muraide* in relevant components. Ex. 2001, ¶133. Like *Muraide*, *Murade II* locates its scanning line driving circuits nearer the edge of the substrate than the LCD seal and the vertical conductive terminals supplying a counter potential to a counter substrate. Ex. 1008, Fig. 1, Fig. 12, Fig. 13, 14:38-39, 30:64-31:15, 31:39-58; Ex. 1005, Fig. 4, Fig. 11, Fig. 12, ¶[0106]; Ex. 2001, ¶133.

Like *Muraide*, the edge of *Murade II*'s counter substrate aligns with the edge of the LCD seal, and so the vertical conductive terminals must reside nearer the pixel display region than the scanning line driving circuits outside the seal. Ex. 1008, Fig. 1, Fig. 13, 14:38-39, 30:64-31:15, 31:39-58; Ex. 1005, Fig. 4, Fig. 12, ¶[0106]; Ex. 2001, ¶¶134-135. Accordingly, like *Muraide*, *Murade II* locates its counter potential terminal LCCOM and corresponding wiring line farther from the

edge of the substrate than the lines supplying the scanning line driving circuits, including DY, VSSY, VDDY, CLY', and CLY. *Id.*

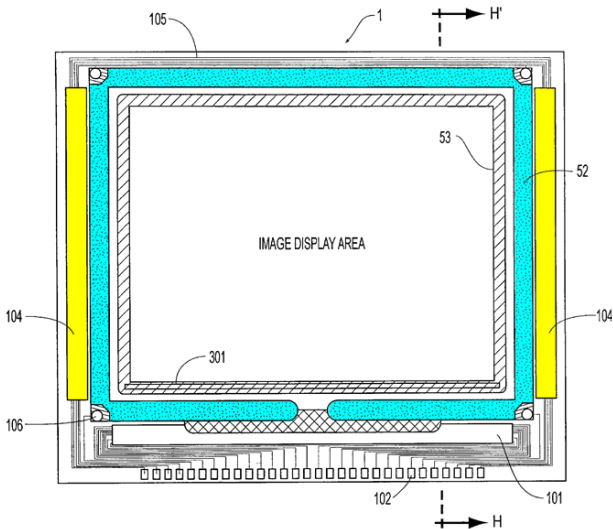
- ii. **The Petition does not establish any likelihood that *Murade II* in combination with *Sunao* or *Komeno* teach “the plurality of main wiring lines . . . being planarly laid out so as not to intersect each other in the peripheral region; and the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines,” as recited in ’390 claim 1.**

The combinations of *Murade II* with *Sunao* or *Komeno* do not disclose all elements of the ’390 claims due to the same deficiencies as the combinations of *Muraide* with *Sunao* or *Komeno* in Ground 1. Ex. 2001, ¶¶137-152. *Murade II* and *Muraide* describe identical layouts of the relevant components. *Id.*, ¶¶133-135. Thus, just like *Muraide*, modifying the layout of *Murade II* based on *Sunao* or *Komeno* cannot result in “the plurality of main wiring lines . . . being planarly laid out so as not to intersect each other in the peripheral region; and the counter electrode potential line being closest to edges of the element substrate, among the plurality of main wiring lines,” as recited in ’390 claim 1. *Id.*, ¶¶137-152.

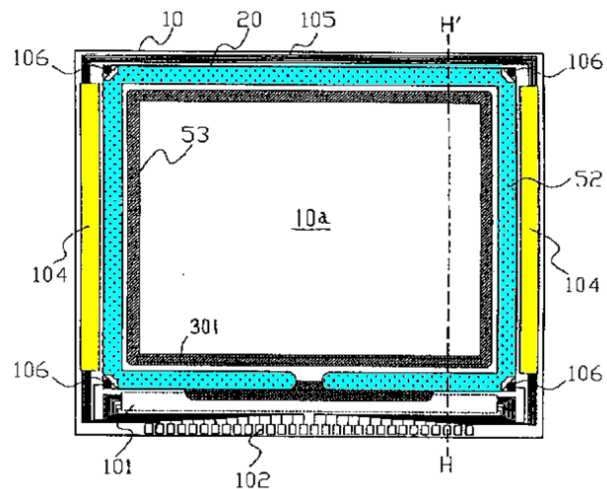
Murade II describes the same layout as *Muraide* with respect to the terminals, wiring lines, scanning line driving circuits, and counter substrate. Ex.

2001, ¶¶63-65. ¶¶133-135. Both *Murade II* and *Muraide* teach placing the scanning line driving circuits (highlighted in yellow) outside the LCD seal (blue):

***Murade II*, Fig. 12 (Ex. 1008)**



***Muraide*, Fig. 11 (Ex. 1005)**



Ex. 1008, Fig. 12 (emphasis added); Ex. 1005, Fig. 11 (emphasis added); Ex. 2001, ¶¶63, ¶133.

Both references also teach aligning the counter substrate (highlighted in green, called “opposite substrate” in *Murade II*) with the edge of the LCD seal:

***Murade II*, Fig. 13 (Ex. 1008)**

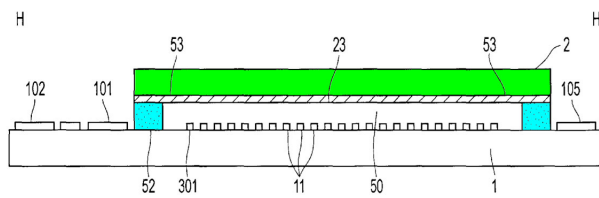
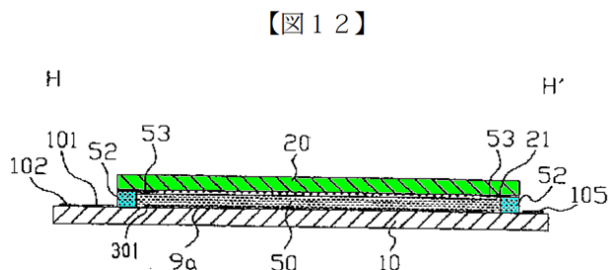


FIG. 13

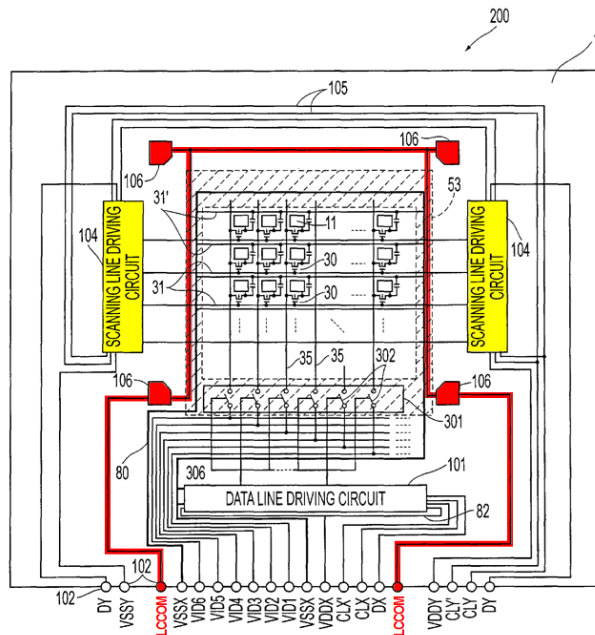
***Muraide*, Fig. 12 (Ex. 1005)**



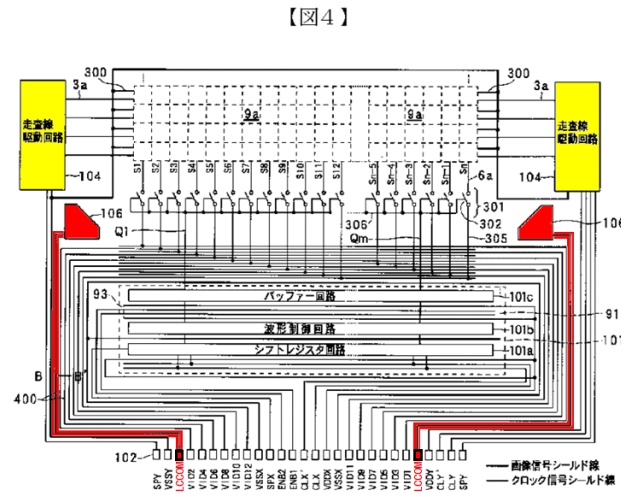
Ex. 1008, Fig. 13 (emphasis added), 14:38-39, 30:64-31:15, 31:39-58; Ex. 1005, Fig. 12 (emphasis added), ¶[0106]; Ex. 2001, ¶64, ¶134.

As a result of this arrangement of counter substrate and scanning line driving circuits, the scanning line driving circuits (yellow) reside nearer the edge of the LCD substrate than the vertical conductive terminals (red) between the substrates to which the counter potential line (red) must run:

Muraide II, Fig. 1 (Ex. 1008)



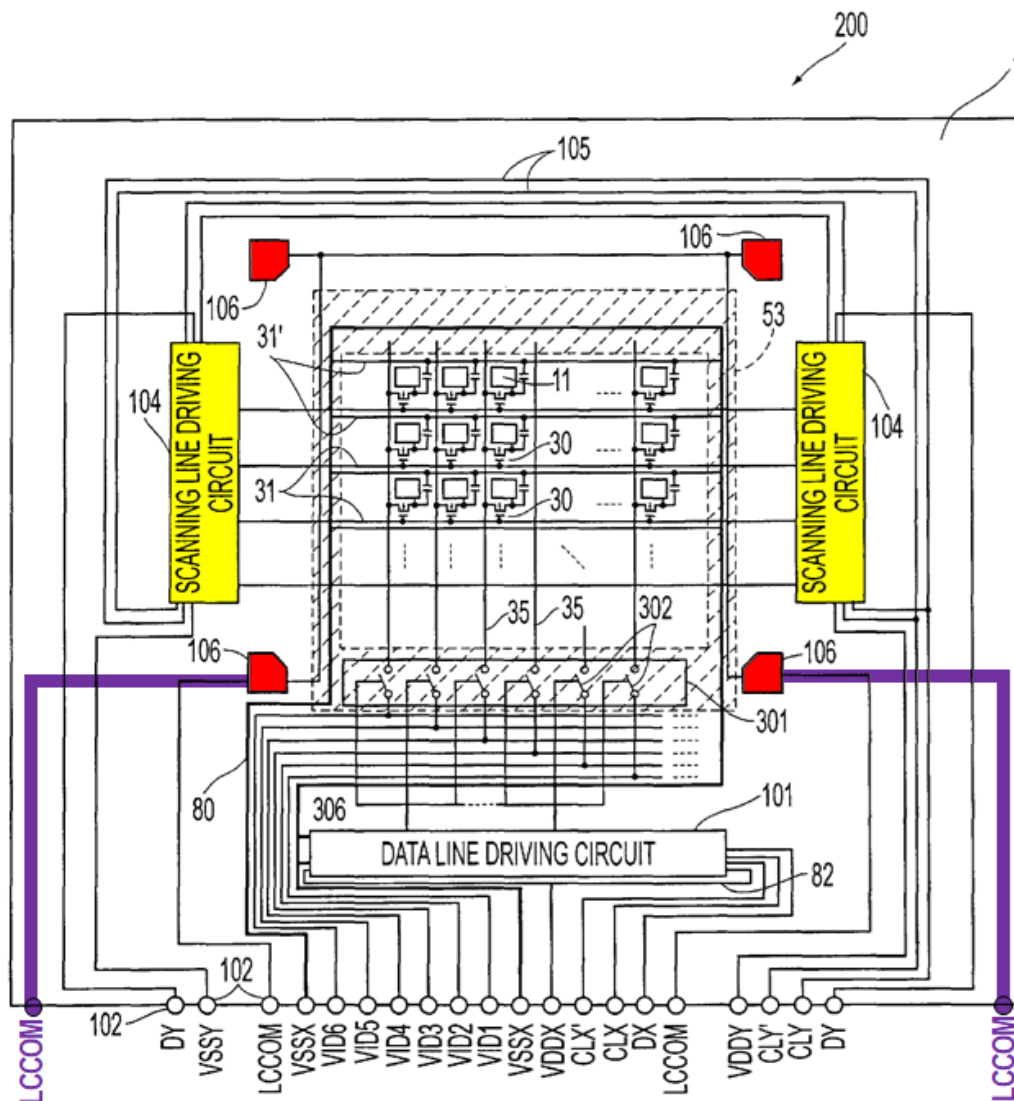
Muraide, Fig. 4 (Ex. 1005)



Ex. 1008, Fig. 1 (emphasis added); Ex. 1005, Fig. 4 (emphasis added); Ex. 2001, ¶65, ¶135.

The identical teachings in *Murade II* and *Muraide* mean that combining *Murade II* with *Sunao* or *Komeno* cannot satisfy the '390 claim limitations for the same reasons discussed for Ground 1, above. §V.A.v. Ex. 2001, ¶137.

As in *Muraide*, relocating *Murade II*'s LCCOM terminals to place them nearer the edge of the substrate than the terminals supplying the scanning line driving circuits 104 would necessarily require the LCCOM lines to intersect with lines supplying those circuits—at least DY, VSSY, VDDY, CLY', and CLY—due to the placement of those circuits outside the vertical conductive terminals 106 supplying the counter substrate. Ex. 1008, Fig. 1; Ex. 2001, ¶¶137-146. Patent Owner has illustrated that necessary outcome here, showing hypothetical relocated LCCOM terminals and lines in purple, with the disclosed vertical conductive terminals 106 remaining in red and the scanning line driving circuits 104 in yellow:



Ex. 1008, Fig. 1 (yellow and red emphasis added; purple modifications added); Ex. 2001, ¶146.

As in Ground 1, the Petition does not explain or provide evidentiary support for “*how or why*” the combination of *Murade II* with a counter potential line nearest the edge of the substrate—as a “design choice” or as allegedly disclosed in *Sunao* or *Komeno*—would satisfy all elements of ’390 claim 1. *TriVascular*, 812

F.3d at 1066. The Petition’s mere suggestion to move the counter potential line does not explain or provide evidence how or why the modification would satisfy the other elements of the ’390 claims.

As in Ground 1, the Petition does not suggest modifying *Murade II* based on *Sunao* or *Komeno* except for the alleged “design choice” of relocating the counter electrode potential line relative to the other wiring lines. Pet., 68 (describing alleged “design choice”), 68-69 (addressing *Sunao*), 69-70 (addressing *Komeno*). The Petition contains no analysis or evidence suggesting modifying the layout of *Murade II* in any other way, based on *Sunao*, *Komeno* or otherwise, any motivation to do so, or how a POSITA would reasonably expect success in such modifications. *Cf. Personal Web Techs.*, 848 F.3d at 994 (finding obviousness analysis deficient for absence of explanation or evidence of *how* a combination would work).

As in Ground 1, and for the reasons set forth in §V.A.v, the combinations alleged in Ground 4 do not disclose “the plurality of main wiring lines . . . being planarly laid out so as not to intersect each other in the peripheral region,” as recited in ’390 claim 1. Ex. 2001, ¶¶137-152. All other ’390 claims depend from claim 1. The Petition does not rely on any other reference to supply this missing element, and therefore it has not established any likelihood of success for any claim under Ground 4.

- iii. **The Petition does not establish that the Office erred, during prosecution, in evaluating and allowing the claims in view of *Muraide*, which contains the same disclosure as the Petition relies on from *Murade II*, and *Kaito*, which contains the same disclosure as the Petition relies on from *Sunao* and *Komeno*.**

The identical teachings relied upon by the Petition from *Murade II* and *Muraide* also mean that the Board may deny institution under § 325(d) for Grounds 4 and 5 that combine *Murade II* with *Sunao* or *Komeno*, for the same reasons discussed for Grounds 1 and 2 (*Muraide* combined with *Sunao* or *Komeno*). §V.A.vi. *Murade II* does not differ in material part from *Muraide*, which the Examiner considered and distinguished. *Sunao* and *Komeno* are substantially the same in material part as *Kaito*, discussed above, which the Examiner also considered and found did not, in conjunction with *Muraide*, teach or suggest the relationship of elements in the '390 claims. *Id.*; Ex. 1004, 7-8 (Notice of Allowability).

The Petition makes no attempt to establish that the Office erred in its decision to allow the '390 claims over the disclosures in *Muraide*, identical in relevant part to *Murade II*, and *Kaito*, identical in relevant part to *Sunao* and *Komeno*. Because the Office previously considered the same and substantially the same art presented in the Petition, and the Petition has not asserted that the Office erred in its evaluation of that art, the Board may deny institution under § 325(d).

Advanced Bionics, IPR2019-01469, Paper 6 at 7-11; *Becton, Dickinson*, IPR2017-01586, Paper 8, at 17-18.

E. Ground 5: The Petition Does Not Establish a Reasonable Likelihood that *Murade II* in Combination with *Sunao* or *Komeno* and in Further Combination with *Murade III* Renders Obvious Claims 2, 3 and 12 or that the Office Erred in Its Consideration of Art Substantially the Same as *Murade II*, *Sunao*, and *Komeno* During Prosecution.

Murade II in combination with *Sunao* or *Komeno* and in further combination with *Murade III* does not render obvious claims 2-3 and 12, which depend from claim 1, for at least the reasons that *Murade II* in combination with *Sunao* or *Komeno* does not disclose all elements of claim 1, as described for Ground 4. The Petition does not assert in Ground 5 that *Murade III* satisfies any limitation of claim 1, Pet. 40-44, and therefore *Murade III* does not cure any of the Petition's deficiencies for claim 1, as discussed above for Ground 4. §V.D.

VI. CONCLUSION

The Petition does not establish a reasonable likelihood that the art and arguments presented in any of the Grounds render any challenged claim unpatentable, because for every Ground the Petition provides no evidence to satisfy one or more limitations of '390 independent claim 1. The Office also already considered all material teachings of the references presented in the

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Petition, and the Petition has not argued in error in that analysis. The Board should deny institution under either § 314(a) or § 325(d).

Date: June 7, 2023

Respectfully submitted,

s/ Cyrus A. Morton

Cyrus A. Morton (Reg. No. 44,954)

CMorton@RobinsKaplan.com

Lead Counsel

Jessica L. Gutierrez (Reg. No. 75,094)

JGutierrez@RobinsKaplan.com

Back-Up Counsel

Robins Kaplan LLP

800 LaSalle Avenue, Suite 2800

Minneapolis, MN 55402

Direct Line: 612-349-8722

Fax: 612-339-4181

Attorneys for Patent Owner

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

I certify that this Patent Owner's Preliminary Response complies with the word count limit and contains 12,210 words in 14-point Times New Roman font as calculated by the word count feature of Microsoft Office, in compliance with 37 C.F.R. § 42.24(a)(1)(i). This word count is inclusive of all text and footnotes but does not include the table of contents, table of authorities, certificate of service or word count, or appendix of exhibits or claim listing.

Date: June 7, 2023

Respectfully submitted,

s/ Cyrus A. Morton

Cyrus A. Morton (Reg. No. 44,954)
CMorton@RobinsKaplan.com
Lead Counsel
Jessica L. Gutierrez (Reg. No. 75,094)
JGutierrez@RobinsKaplan.com
Back-Up Counsel
Robins Kaplan LLP
800 LaSalle Avenue, Suite 2800
Minneapolis, MN 55402
Direct Line: 612-349-8722
Fax: 612-339-4181

Attorneys for Patent Owner

CERTIFICATE OF SERVICE

I certify that on June 7, 2023, a copy of Patent Owner's Preliminary Response, including exhibits, was served in its entirety by electronic mail to Petitioner's counsel at the following addresses indicated in Petitioner's Mandatory Notices:

Wenye Tan
wtan@anovalaw.com

Li Jiang
li.jiang@anovalaw.com

Date: June 7, 2023

Respectfully submitted,

s/ Cyrus A. Morton

Cyrus A. Morton (Reg. No. 44,954)
CMorton@RobinsKaplan.com
Lead Counsel
Jessica L. Gutierrez (Reg. No. 75,094)
JGutierrez@RobinsKaplan.com
Back-Up Counsel
Robins Kaplan LLP
800 LaSalle Avenue, Suite 2800
Minneapolis, MN 55402
Direct Line: 612-349-8722
Fax: 612-339-4181

Attorneys for Patent Owner