AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-382	9/30/2022	Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
CRYSTAL LEAP ZRT	HKC CORP. LTD.; CHONGQING HKC OPTOELECTRONICS TECHNOLOGY CO., LTD.; HKC OVERSEAS LTD.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,116,390	10/3/2006	Crystal Leap Zrt
2	7,335,913	2/26/2008	Crystal Leap Zrt
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

HKC EXHIBIT 1004

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	02/26/2008	7335913	125312	9022

25944 7590 02/06/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 106 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Masao Murade, Suwa-shi, JAPAN;

PART B - FEE TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 10/30/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	09/13/2005	Masao Murade	125312	9022

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	01/30/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-059000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Oliff & Berridge, PLC
2
3 00000070 11223919

12/11/2007 JADD02
01 FC:1501 1440.00 OP
02 FC:1504 300.00 OP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Seiko Epson Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Tokyo, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☒ A check is enclosed. ck# 200107 ($1740)
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 15-0461 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date December 10, 2007

Typed or printed name Christopher J. Wheeler Registration No. 60,738

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25944 7590 10/30/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/30/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	09/13/2005	Masao Murade	125312	9022

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	01/30/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25944 7590 10/30/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	09/13/2005	Masao Murade	125312	9022

TITLE OF INVENTION: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	01/30/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-059000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	09/13/2005	Masao Murade	125312	9022

25944 7590 10/30/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/30/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 106 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 106 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/223,919	MURADE, MASAO	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment dated 08/07/07*.

2. ☒ The allowed claim(s) is/are *1-11*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Long Pham/
Primary Examiner, Art Unit 2814

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11223919	MURADE, MASAO
	Examiner	**Art Unit**
	Long Pham	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/09/2007								
1	1	=								
2	2	=								
3	3	=								
4	4	=								
5	5	=								
6	6	=								
7	7	=								
8	8	=								
9	9	=								
10	10	=								
11	11	=								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11223919	MURADE, MASAO
	Examiner	Art Unit
	Long Pham	2814

SEARCHED			
Class	Subclass	Date	Examiner
257	59, 57, 66, 79	10/09/07	LP

SEARCH NOTES		
Search Notes	Date	Examiner
Updated text or interference searches	10/09/07	LP

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	59	10/09/07	LP

Form PTO-1449 (REV. 8-83) US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 125312	APPLICATION NO. New U.S. Patent Application 11/223,919
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Masao MURADE	
	FILING DATE September 13, 2005	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 09-113906 with abstract and translation.	05/02/1997	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	/Long Pham/ (10/20/2007)	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./ (10/20/2007)

Date: September 13, 2005

OIPE IAP38 JAN 24 2007 PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 1/06) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 125312	APPLICATION NO. 11/223,919
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Masao MURADE	
	FILING DATE September 13, 2005	GROUP 2811

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	JP-A-2004-354969	12/16/2004	JAPAN	X	X
	2	KR 10-2004-0094339 A	11/09/2004	KOREA		
	3	KR 1999-009398 A	02/05/1999	KOREA	X	

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	/Long Pham/ (10/27/2007)	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 24, 2007 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11223919	MURADE, MASAO
	Examiner	Art Unit
	Long Pham	2814

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
257	59	H	0	1	L	29 / 04 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	57	79	66		

NONE (Assistant Examiner) (Date)		Total Claims Allowed: 11	
(Legal Instruments Examiner) (Date)	/Long Pham/ 10/09/07 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1,2

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 9022

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/223,919	09/13/2005	257	2814	125312

APPLICANTS
Masao Murade, Suwa-shi, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
JAPAN 2004-328982 11/12/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
09/29/2005

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /LONG PHAM/ Examiner's Signature	☐ Met after Allowance LP Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	13	9	2

ADDRESS

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320
UNITED STATES

TITLE

Electro-optical device and electronic apparatus

FILING FEE RECEIVED		
1000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2814

Application No.: 11/223,919 — Examiner: L. PHAM

Filed: September 13, 2005 — Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the June 14, 2007 Office Action, please consider the following:

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates including an extending portion that extends from the other substrate on ~~at least~~ one side in plan view;

display electrodes that are provided on the one substrate;

a circuit unit that is provided on the one substrate so as to drive the display electrodes;

wiring lines for driving the circuit unit and the display electrodes;

a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines ~~for driving the circuit unit and the display electrodes~~ to ~~an~~ the extending ~~portion extending on the one side of one substrate;~~ portion; and

a plurality of external connecting terminals ~~that are correspondingly connected to the plurality of lead wiring lines and are~~ provided on ~~a surface of~~ the extending ~~portion facing the other substrate so as to at least partially overlap~~ portion, each of the external connecting terminals overlapping with the plurality of lead wiring lines in plan view.

2. (Currently Amended) The electro-optical device according to Claim 1,

wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween, each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.

~~the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and~~

~~the lead wiring lines have the same film as a second conductive film constituting the circuit unit.~~

3. (Original) The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

4. (Original) The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

5. (Currently Amended) An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates <u>including an</u> extending <u>portion that extends</u> from the other substrate on ~~at least~~ one side in plan view;

display electrodes that are provided on <u>the</u> one substrate;

a circuit unit that is provided on <u>the</u> one substrate so as to drive the display electrodes;

<u>wiring lines for driving the circuit unit and the display electrodes;</u>

a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines ~~for driving the circuit unit and the display electrodes~~ to ~~an~~ the extending ~~portion extending on the one side of one substrate;~~portion; and

a plurality of external connecting terminals ~~that are correspondingly connected to the plurality of lead wiring lines and are~~ provided on ~~a surface of~~ the extending ~~portion facing the other substrate so as to at least partially overlap~~ portion, each of the external connecting terminals overlapping with the circuit unit in plan view.

6. (Original) The electro-optical device according to Claim 5,

wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and

at least a part of the driving circuit overlaps the external connecting terminals in plan view.

7. (Currently Amended) The electro-optical device according to Claim 5,

wherein the external connecting terminals and the part of the circuit unit are laminated with an interlayer insulating film interposed therebetween, ~~and~~each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.

~~the external connecting terminals have the same film as a first conductive film constituting the circuit unit.~~

8. (Original) The electro-optical device according to Claim 1, further comprising:

a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and

an electro-optical material that is held in the internal space,

wherein the display electrodes and a part of the circuit unit are disposed to face the internal space.

9. (Original) An electronic apparatus comprising the electro-optical device according to Claim 1.

10. (New) The electro-optical device according to Claim 2, the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit, and the lead wiring lines being formed from the same film as a second conductive film constituting the circuit unit.

11. (New) The electro-optical device according to Claim 7, the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit.

REMARKS

Claims 1-11 are pending in this application. By this Amendment, claims 1, 2, 5 and 7 are amended and claims 10 and 11 are added. The amendments and added claims introduce no new matter. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The Office Action, on page 2, withdraws from consideration claims 6 and 7 as drawn to non-elected subject matter, and makes final the February 27, 2007 Election of Species Requirement. In reply to the Election of Species Requirement, Applicant provisionally elected species 1, Fig. 1, claims 1-5, 8 and 9, with traverse. Applicant further asserted that at least claims 1-4, 8 and 9 are generic to all species. The non-elected claims are subject to rejoinder, as discussed below.

Applicant respectfully submits that claims 1-4, 8 and 9 are generic to all species. As such, Applicant respectfully requests rejoinder of claims 6 and 7 upon allowance of any one or more of generic claims 1-4, 8 and 9. Further, Applicant requests rejoinder of claims 6 and 7 based on their respective dependencies on an allowable independent claim 5.

The Office Action, on pages 2-4, rejects claims 1, 5, 8 and 9 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication No. 2003/0122979 A1 to Morimitsu. This rejection is respectfully traversed.

The Office Action, on pages 2-4, asserts that Morimitsu teaches a liquid crystal display device with features that are alleged to correspond to the combinations of all of the features recited in independent claims 1 and 5. This assertion is incorrect for at least the following reasons.

Morimitsu teaches a liquid crystal display device including electric power supply paths to supply electric power from connecting pads on a circuit array substrate to a counter electrode of a counter substrate (Abstract).

Morimitsu, however, does not teach, nor can it reasonably be considered to have suggested, a plurality of external connecting terminals provided on the extending portion, each of the external connecting terminals overlapping with a plurality of lead wiring lines in plan view, as positively recited in claims 1. Claim 5 recites similar features with regard to the claimed circuit unit.

The Office Action, at the bottom of page 2 and at the top of page 3, alleges that elements 12 and 13 of Morimitsu can be considered to correspond to a plurality of lead wiring lines, as recited in claims 1 and 5. The Office Action, on the top of page 3, further alleges that pad ITO films 52 correspond to external connecting terminals, as recited in claims 1 and 5. However, with reference to Figs. 4 and 5 of Morimitsu and the relevant portions of the disclosure, Morimitsu does not disclose each of the external connecting terminals overlapping with the plurality of lead wiring lines, or circuit unit, in plan view. At best, Morimitsu suggests that pad ITO film 52 overlaps a single power supply pad 13. As such, it is unreasonable to assert that Morimitsu teaches at least the combinations of all the features recited in claims 1 and 5.

For at least the foregoing reasons, the applied reference does not teach the combinations of all the features positively recited in independent claims 1 and 5. Additionally, claims 2-4, 8 and 9 are also not taught by the applied reference for at least the respective dependence of these claims, directly or indirectly, on an allowable base claim, as well as for the separately patentable subject matter each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-5, 8 and 9 under 35 U.S.C. §102(b) as being anticipated by the applied reference are respectfully requested.

Added claims 10 and 11 are also allowable at least for the respective dependence of these claims, directly or indirectly, on an allowable base claim, as well as for the separately patentable subject matter that each of these claims recites.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-5, and 8-11, and rejoinder of claims 6 and 7, upon at least the allowance of independent claim 5, are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Christopher J. Wheeler
Registration No. 60,738

JAO:CJW/clf

Date: August 7, 2007

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	09/13/2005	Masao Murade	125312	9022

25944 7590 06/14/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	
MAIL DATE	**DELIVERY MODE**
06/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/223,919	MURADE, MASAO	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/13/05,01/24/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-5, 8, and 9 in the reply filed on 03/26/07 is acknowledged. The traversal is on the ground(s) that see election of 03/26/07. This is not found persuasive because the searches for the patentably distinct species are not co-extensive.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Morimitsu (US pub 20030122979).

With respect to claim 1; Morimitsu teaches an electro-optical device, comprising (see figs. 1-7 and associated text):

a pair of substrates 10, 20 that are disposed to face each other with a predetermined gap therebetween, one substrate 10 of the pair of substrates extending from the other substrate on at least one side in plan view (see figs. 1 and 2);

display (pixel) electrodes (see claim 1) that are provided on one substrate;

a circuit unit (see claim 1 and para [0035] that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines 12, 13 that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals 52 (see figs. 2 and 5 and associated text) that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

With respect to claim 2, Morimitsu further teaches the external connecting terminals 52 and the lead wiring lines 12,13 are laminated with an interlayer insulating film 15 interposed therebetween (see fig. 2), the external connecting terminals 52 have the same film as a first conductive film constituting the circuit unit (see bottom and top right portions of fig. 5), and the lead wiring lines 12, 13 have the same film as a conductive film constituting the circuit unit (see para [0036]).

With respect to claim 3, Morimitsu further teaches the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side. See fig. 1 and 5.

With respect to claim 4 Morimitsu further teaches the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view. See fig. 2.

With respect to claim 8, Morimitsu further teaches a sealant 62 that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and an electro-optical material that is held in the internal space, wherein the display electrodes and a part of the circuit unit are disposed to face the internal space. See figs. 1-7 and associated text.

With respect to claim 9, Morimitsu further teaches n electronic apparatus comprising the above electro-optical device. See figs. 1-7 and associated text.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Morimitsu (US pub 20030122979).

With respect to claim 5, Morimitsu teaches an electro-optical device, comprising (see figs. 1-7 and associated text):

a pair of substrates 10, 20 that are disposed to face each other with a predetermined gap therebetween, one substrate 10 of the pair of substrates extending from the other substrate on at least one side in plan view (see figs. 1 and 2);

display (pixel) electrodes (see claim 1) that are provided on one substrate;

a circuit unit (see claim 1 and para [0035] that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines 12, 13 that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals 52 (see figs. 2 and 5 and associated text) that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit (11b scanning line) in plan view. See figs. 4 and 5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP

Sheet 1 of 1

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 125312	APPLICATION NO. New U.S. Patent Application
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANTS Masao MURADE	
		FILING DATE September 13, 2005	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
LP						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 09-113906 with abstract and translation.	05/02/1997	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER L. Pham	DATE CONSIDERED 6/8/07

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 13, 2005

OIPE IAP38 JAN 24 2007 PATENT & TRADEMARK OFFICE

Sheet 1 of 1

Form PTO-1449 (REV. 1/06) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 125312	APPLICATION NO. 11/223,919
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Masao MURADE	
	FILING DATE September 13, 2005	GROUP 2811

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	JP-A-2004-354969	12/16/2004	JAPAN	X	X
	2	KR 10-2004-0094339 A	11/09/2004	KOREA		
	3	KR 1999-009398 A	02/05/1999	KOREA	X	

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER L. Pham	DATE CONSIDERED 6/8/07

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 24, 2007

Notice of References Cited	Application/Control No. 11/223,919	Applicant(s)/Patent Under Reexamination MURADE, MASAO	
	Examiner Long Pham	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0122979	07-2003	Morimitsu, Atsushi	349/42
*	B	US-2005/0105036	05-2005	Murakami, Masahiro	349/150
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
11/223,919	MURADE, MASAO
Examiner	**Art Unit**
Long Pham	2814

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date								
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	Type	Hits	Search Text
1	BRS	0	("2003/0122979").URPN.
2	BRS	0	("2004/0036941").URPN.
3	BRS	4426	counter adj2 substrate
4	BRS	0	("2003/0122979").URPN.
5	BRS	15692	S2 near10 (extension or extending or extended or larger or bigger)
6	BRS	0	("2005/0105036").URPN.
7	BRS	23770	counter adj2 electrode
8	BRS	41676	(pixel or display) near2 electrode
9	BRS	1325	S3 same S4
10	BRS	294391	substrate near3 (device or semiconductor or array or tft)
11	BRS	19	S4 same S9
12	BRS	794	S5 same S6
13	BRS	3	("5155612" | "6097467" | "6166848").PN.
14	BRS	0	("2005/0105036").URPN.
15	BRS	101	S1 same S8
16	BRS	2385	S1 same S2
17	IS&R	1	("20030122979").PN.
18	BRS	1	S18 and S17
19	BRS	41676	electrode near2 (pixel or display)

	DBs
1	USPAT
2	USPAT
3	US-PGPUB; USPAT
4	USPAT
5	US-PGPUB; USPAT
6	USPAT
7	US-PGPUB; USPAT
8	US-PGPUB; USPAT
9	US-PGPUB; USPAT
10	US-PGPUB; USPAT
11	US-PGPUB; USPAT
12	US-PGPUB; USPAT
13	US-PGPUB; USPAT; USOCR
14	USPAT
15	US-PGPUB; USPAT
16	US-PGPUB; USPAT
17	US-PGPUB; USPAT
18	US-PGPUB; USPAT
19	US-PGPUB; USPAT



IFW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE — Group Art Unit: 2814

Application No.: 11/223,919 — Examiner: L. PHAM

Filed: September 13, 2005 — Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

RESPONSE TO ELECTION OF SPECIES REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the February 27, 2007 Election of Species Requirement, Applicant provisionally elects Species 1, Figure 1, with traverse. Claims 1-5, 8 and 9 read on elected Species 1. Claims 1-4, 8 and 9 are generic to all species.

It is also respectfully submitted that the subject matter of all species is sufficiently related that a thorough search for the subject matter of any one species would encompass a search for the subject matter of the remaining species. Thus, it is respectfully submitted that the search and examination of the entire application could be made without serious burden. See MPEP §803 in which it is stated that "if the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions" (emphasis added). It is respectfully submitted that this policy should apply in the present application in order to avoid unnecessary delay and expense to Applicants and duplicative examination by the Patent Office.

Thus, withdrawal of the Election of Species Requirement is respectfully requested.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Daniel A. Tanner, III
Registration No. 54,734

JAO:CJW/axl

Date: March 26, 2007

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/223,919	09/13/2005	Masao Murade	125312	9022

25944 7590 02/27/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
31 DAYS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	11/223,919	MURADE, MASAO	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1-9 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species: species 1: embodiment of fig. 1 and species 2: embodiment of fig. 11. The species are independent or distinct because they are nonobvious variants.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim appears generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

A telephone call was made to -- on -- to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If

the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicant traverse on the ground that the inventions or species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103(a) of the other invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham

Primary Examiner

Art Unit 2814

LP

Index of Claims

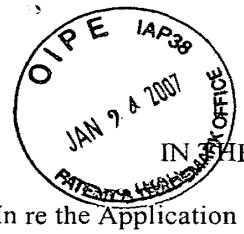
Application/Control No.	Applicant(s)/Patent under Reexamination
11/223,919	MURADE, MASAO
Examiner	**Art Unit**
Long Pham	2814

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Group Art Unit: 2811

Application No.: 11/223,919

Filed: September 13, 2005

Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. An English language Abstract of one or more non-English language reference is attached hereto. See References 1 and 3.

☒ 3. A computer-generated English language translation of one or more Japanese Patent Publication cited herein has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See Reference 1.

☒ 4. Reference 1 corresponds to reference 2.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Joel S. Armstrong
Registration No. 36,430

JAO:JSA/mch

Date: January 24, 2007

OLIFF & BERRIDGE, PLC
P.O. Box 19928
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OIPE IAP38
JAN 24 2007
PATENT & TRADEMARK OFFICE

Form PTO-1449 (REV. 1/06) U.S. Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 125312	APPLICATION NO. 11/223,919
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT Masao MURADE	
	FILING DATE September 13, 2005	GROUP 2811

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	1	JP-A-2004-354969	12/16/2004	JAPAN	X	X
	2	KR 10-2004-0094339 A	11/09/2004	KOREA		
	3	KR 1999-009398 A	02/05/1999	KOREA	X	

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 24, 2007

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-354969
(43)Date of publication of application : 16.12.2004

51)Int.Cl. G09F 9/30
G02F 1/1345
G02F 1/1368
G02F 1/167
// H05B 33/06
H05B 33/14

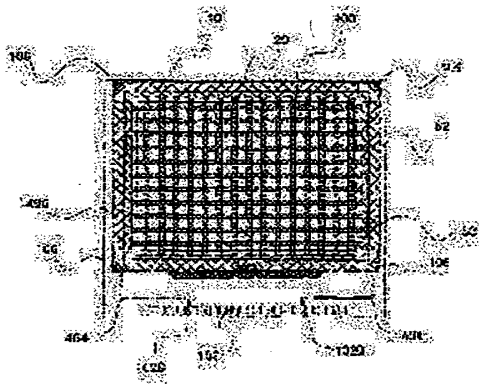
21)Application number : **2004-054200**
22)Date of filing : **27.02.2004**

(71)Applicant : SEIKO EPSON CORP
(72)Inventor : MURADE MASAO

30)Priority
riority number : **2003127309** Priority date : **02.05.2003** Priority country : JP

54) ELECTRO-OPTICAL APPARATUS AND ELECTRONIC EQUIPMENT

57)Abstract:
ROBLEM TO BE SOLVED: To provide an electro-optical apparatus apable of enhancing image quality by preventing the appearance of mages due to light leakage around an image to the utmost in the lectro-optical apparatus such as liquid crystal display apparatus.
OLUTION: The electro-optical apparatus is provided with data lines, canning lines, TFTs (thin film transistors) and pixel electrodes on a TFT rray substrate 10. The substrate has an image display region 10a pecified as a formation region of the TFT and pixel electrode and a eripheral region specifying the periphery of the image display region. urther, the electro-optical apparatus is provided with storage apacitances which retain the potential in the pixel electrodes for a rescribed time and capacitance wires 400 connected to capacitance lectrodes constituting the storage capacitances on the picture display egion. Furthermore, the electro-optical apparatus is provided with a rame (frame-shaped pattern) 406 which is formed as the same film as he capacitance wire and constitutes one part of a frame region 53 ividing the picture display region and the peripheral region. Therein, the rame pattern is formed as the same film as a wire 404 connected to an utside circuit connecting terminal 102Q, too.



EGAL STATUS

Date of request for examination]	27.02.2004
Date of sending the examiner's decision of rejection]	
Kind of final disposal of application other than the xaminer's decision of rejection or application onverted registration]	
Date of final disposal for application]	
Patent number]	3772888
Date of registration]	24.02.2006
Number of appeal against examiner's decision of	

ejection]
Date of requesting appeal against examiner's decision
f rejection]
Date of extinction of right]

(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2004-354969
(P2004-354969A)
(43)公開日　平成16年12月16日(2004.12.16)

(51)Int.Cl.[7]		F I			テーマコード（参考）
G09F	9/30	G09F	9/30	349C	2H092
G02F	1/1345	G09F	9/30	330Z	3K007
G02F	1/1368	G09F	9/30	338	5C094
G02F	1/167	G02F	1/1345		
// H05B	33/06	G02F	1/1368		

審査請求 有　請求項の数 21　ＯＬ　（全 34 頁）　最終頁に続く

(21)出願番号　特願2004-54200 (P2004-54200)
(22)出願日　平成16年2月27日 (2004.2.27)
(31)優先権主張番号　特願2003-127309 (P2003-127309)
(32)優先日　平成15年5月2日 (2003.5.2)
(33)優先権主張国　日本国 (JP)

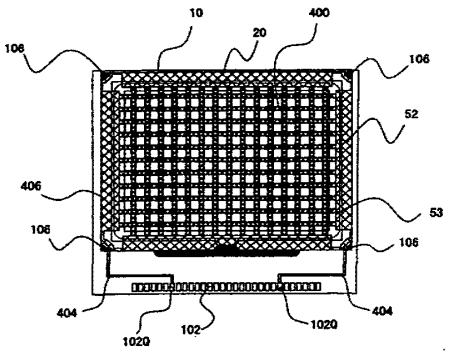
(71)出願人　000002369
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(74)代理人　100095728
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(74)代理人　100107261
弁理士　須澤　修
(72)発明者　村出　正夫
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

Ｆターム(参考)　2H092 GA35 JA24 JA46 JB23 JB24 JB32 JB33 JB66 JB69 MA13 NA01 NA28 PA09

最終頁に続く

(54)【発明の名称】電気光学装置及び電子機器

(57)【要約】
【課題】　電気光学装置において、画像の周囲に光漏れに起因する像が現れるということを極力防止等することで、画質を高める。
【解決手段】　ＴＦＴアレイ基板（１０）上に、データ線、走査線、ＴＦＴ及び画素電極を備えている。前記基板は、ＴＦＴ及び画素電極の形成領域として規定される画像表示領域（１０ａ）と、該画像表示領域の周辺を規定する周辺領域とを有する。画像表示領域上には、画素電極における電位を所定期間保持する蓄積容量と、該蓄積容量を構成する容量電極に接続される容量配線（４００）とを備え、前記画像表示領域及び前記周辺領域間を画する額縁領域（５３）上には、容量配線と同一膜として形成され、且つ、当該額縁領域の少なくとも一部に形成された額縁パターン（４０６）を備えている。この額縁パターンは、外部回路接続端子（１０２Ｑ）に接続された配線（４０４）とも同一膜として形成されている。
【選択図】　図８



【特許請求の範囲】
【請求項１】
基板上に、
一定の方向に延びるデータ線及び該データ線に交差する方向に延びる走査線と、
前記走査線により走査信号が供給されるスイッチング素子と、
前記データ線により前記スイッチング素子を介して画像信号が供給される画素電極とを備えてなり、
前記基板は、前記画素電極及び前記スイッチング素子の形成領域として規定される画像表示領域と、該画像表示領域の周辺を規定する周辺領域とを有し、
前記画像表示領域上に、
前記画素電極における電位を所定期間保持する蓄積容量と、
該蓄積容量を構成する容量電極に所定電位を供給する第１配線とを備え、
前記第１配線と同一膜として形成され、前記画像表示領域と前記周辺領域とを画する額縁領域の少なくとも一部を構成する額縁パターンとを備えたことを特徴とする電気光学装置。
【請求項２】
前記額縁パターンは、データ線に画像信号を供給するためのサンプリング回路を少なくとも覆うように形成されていることを特徴とする請求項１に記載の電気光学装置。
【請求項３】
前記第１配線は、前記所定電位が供給される側の容量電極と同一膜として、前記容量電極が延長されて形成されたことを特徴とする請求項１に記載の電気光学装置。
【請求項４】
前記額縁パターンの少なくとも一部は、短冊状に分断されて形成され、浮遊電位とされることを特徴とする請求項１に記載の電気光学装置。
【請求項５】
前記基板に対向配置される対向基板と、前記基板及び前記対向基板を接着するシール材とを更に備えてなり、
前記額縁パターンは、前記シール材が形成されるシール領域の少なくとも一部に形成されていることを特徴とする請求項１に記載の電気光学装置。
【請求項６】
前記基板に対向配置される対向基板と、該対向基板上に形成される対向電極とを更に備えてなり、
前記額縁パターンは、前記対向電極と電気的に接続されている接続部分を有することを特徴とする請求項１に記載の電気光学装置。
【請求項７】
前記額縁パターンは、前記第１配線と電気的に接続するように形成されていることを特徴とする請求項１に記載の電気光学装置。
【請求項８】
前記接続部分は、前記対向基板のコーナー部に対応して設けられていることを特徴とする請求項６又は７に記載の電気光学装置。
【請求項９】
前記額縁パターンは、前記画像表示領域の周囲すべてを囲むように形成されていることを特徴とする請求項１に記載の電気光学装置。
【請求項１０】
前記画像表示領域は平面視して矩形状を有し、
前記額縁パターンは、前記矩形状の三辺に沿って連続して形成された第1のパターンと、残る一辺に沿って形成されるとともに前記第1のパターンと分断して形成された第２のパターンとを含み、
前記接続部分は、前記第1のパターン上に存在することを特徴とする請求項６乃至８のいずれか一項に記載の電気光学装置。

【請求項１１】
前記画像表示領域は平面視して矩形状を有し、
前記額縁パターンは、前記矩形状の対向する二辺に沿って形成された第３のパターンと、残る二辺に沿って形成されるとともに前記第３のパターンと分断して形成された第４のパターンとを含み、
前記接続部分は、前記第３のパターン上に存在することを特徴とする請求項６乃至８のいずれか一項に記載の電気光学装置。
【請求項１２】
前記画像表示領域は平面視して矩形状を有し、
前記額縁パターンは、前記矩形状の一つの角部に対応する部分を除いて連続して形成された第５のパターンと、前記一つの角部に対応する部分に形成されるとともに前記第５のパターンと分断して形成された第６のパターンとを含み、
前記接続部分は、前記第５のパターン及び前記第６のパターンの少なくとも一方の上に存在することを特徴とする請求項６乃至８のいずれか一項に記載の電気光学装置。
【請求項１３】
前記周辺領域上に、
前記基板の辺縁部に沿って形成された外部回路接続端子と、該外部回路接続端子に延設された第２配線とを更に備え、
該第２配線の少なくとも一部は、前記第１配線と同一膜として、且つ、該第１配線と電気的に接続されて形成されていることを特徴とする請求項１乃至１２のいずれか一項に記載の電気光学装置。
【請求項１４】
前記第１配線は、前記データ線の上に層間絶縁膜を介して形成されていることを特徴とする請求項１３に記載の電気光学装置。
【請求項１５】
前記第１配線は、前記画素電極を含む層の直下の層に形成されていることを特徴とする請求項１３又は１４に記載の電気光学装置。
【請求項１６】
前記第１配線及び前記額縁パターンは電気的に接続されて形成されておらず、且つ、
前記第２配線の第１部分及び前記第１配線が電気的に接続され、
前記第２配線の第２部分及び前記額縁パターンが電気的に接続されており、
前記第１部分は前記外部回路接続端子の第１部分に、
前記第２部分は前記外部回路接続端子の第２部分にそれぞれ接続されていることを特徴とする請求項１３乃至１５のいずれか一項に記載の電気光学装置。
【請求項１７】
前記第１配線は、遮光性材料から構成されていることを特徴とする請求項１乃至１６のいずれか一項に記載の電気光学装置。
【請求項１８】
前記第１配線は、相異なる材料からなる積層構造を有することを特徴とする請求項１乃至１７のいずれか一項に記載の電気光学装置。
【請求項１９】
前記基板に対向配置される対向基板と、該対向基板上に形成された遮光膜を更に備えてなり、
前記額縁パターンは、前記遮光膜と重なるように形成されていることを特徴とする請求項１乃至１８のいずれか一項に記載の電気光学装置。
【請求項２０】
前記遮光膜は、前記対向基板の辺縁部に沿うように形成された額縁遮光膜を含むことを特徴とする請求項１９に記載の電気光学装置。
【請求項２１】
請求項１乃至２０のいずれか一項に記載の電気光学装置を具備してなることを特徴とする

電子機器。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、例えばアクティブマトリクス駆動の液晶装置、電子ペーパなどの電気泳動装置、ＥＬ（Electro-Luminescence）表示装置等の電気光学装置の技術分野に属する。また、本発明は、このような電気光学装置を具備してなる電子機器の技術分野にも属する。
【背景技術】
【０００２】
従来、基板上に、マトリクス状に配列された画素電極及び該電極の各々に接続された薄膜トランジスタ（Thin Film Transistor；以下適宜、「ＴＦＴ」という。）、該ＴＦＴの各々に接続され、行及び列方向それぞれに平行に設けられたデータ線及び走査線等を備えることで、いわゆるアクティブマトリクス駆動が可能な電気光学装置が知られている。
【０００３】
このような電気光学装置では、上記に加えて、前記基板に対向配置される対向基板を備えるとともに、該対向基板上に、画素電極に対向する対向電極等を備え、更には、画素電極及び対向電極間に挟持される液晶層等を備えることで、画像表示が可能となる。すなわち、液晶層内の液晶分子は、画素電極及び対向電極間に設定された所定の電位差によって、その配向状態が適当に変更され、これにより、当該液晶層を透過する光の透過率が変化することによって画像の表示が可能になるのである。
【０００４】
また、前述の電気光学装置における前記基板は、走査線、データ線及び画素電極等が設けられる画像表示領域と、走査線駆動回路、データ線駆動回路、これら回路に所定信号を供給するための外部回路接続端子等が設けられる周辺領域とを有する。このような電気光学装置の一典型例としては、例えば特許文献１に記載されているものを挙げることができる。
【０００５】
【特許文献１】特開平１１－２２３８３２号公報
【発明の開示】
【発明が解決しようとする課題】
【０００６】
しかしながら、従来における電気光学装置においては、次のような問題点がある。すなわち、前記の周辺領域においては、通常、基板及び対向基板を接着するためのシール材が設けられる。このシール材としては、取り扱いが容易であること、比較的強力な接着力が得られること等から、光硬化性樹脂が好ましく用いられている。この場合、シール材を硬化するためには、基板及び対向基板間に挟まれて存在する当該シール材に対して光を照射する必要がある。他方、画像表示領域及び周辺領域には、前述した走査線及びデータ線と走査線駆動回路及びデータ線駆動回路とを接続するための配線や、データ線に画像信号を好適に供給するためのサンプリング回路、該画像信号それ自体を供給する画像信号線等各種の配線が形成される必要がある。これらによると、周辺領域上の所定の領域においては、前記シール材と前記各種の配線等が併せて形成される必要があることになるが、当該領域では、シール材硬化のために、所定の隙間を設けておく等によって光の通り道を確保しておくことが行われる。
【０００７】
しかしながら、これによると、完成後の電気光学装置を実地に使用している際に、光の通り道として設けられた前記の所定の隙間等を介して光が漏れてしまうという問題が生じることになる。すなわち、当該電気光学装置を、例えば液晶プロジェクタ等の投射型表示装置のライトバルブとして用いる場合においては、このライトバルブに対して光を投射するとともに、該ライトバルブを通り抜けた光をスクリーン上に拡大投射することで、画像表示を行うことになるが、前記所定の隙間等が存在すると、ライトバルブの通り抜けた光

に、該隙間から漏れ出た光が混入してしまうのである。このような場合、スクリーン上の画像の周囲には、前記各種の配線等のパターンの像が映り込むなどの事態が生じ、画像の品質を貶める結果となってしまう。

【０００８】

また、従来の電気光学装置においては、画像表示領域に、画素電極における電位保持特性を高めるために蓄積容量が形成される場合がある。この蓄積容量を構成する一方の電極（以下、「容量電極」ということがある。）は、一定の電位に維持することが好ましいため、周辺領域に形成される外部回路接続端子に接続されることが行われている。しかしながら、この場合、両者間をコンタクトホールを介して接続する態様が採用されると、該コンタクトホールに起因する高抵抗化がもたらされるおそれが大きいこと、また、コンタクトホール毎に特性が異なるという事態が生じ得ること等から、容量電極、或いはこれから延びる配線の時定数が大きくなり、結果、画像上にクロストークを発生させる等という不具合が生じることがあったのである。なお、前記の配線が、画像表示領域を横切るように形成されている場合には、いわゆる横クロストークとして観察されることになる。

【０００９】

本発明は、上記問題点に鑑みてなされたものであり、画像の周囲に光漏れに起因する像が現れるということを極力防止し、或いは容量電極に所定電位を好適に供給することによって、高品質な画像を表示することの可能な電気光学装置を提供することを課題とする。また、本発明は、そのような電気光学装置を具備する電子機器を提供することをも課題とする。

【課題を解決するための手段】

【００１０】

本発明の電気光学装置は、上記課題を解決するため、基板上に、一定の方向に延びるデータ線及び該データ線に交差する方向に延びる走査線と、前記走査線により走査信号が供給されるスイッチング素子と、前記データ線により前記スイッチング素子を介して画像信号が供給される画素電極とを備えてなり、前記基板は、前記画素電極及び前記スイッチング素子の形成領域として規定される画像表示領域と、該画像表示領域の周辺を規定する周辺領域とを有し、前記画像表示領域上に、前記画素電極における電位を所定期間保持する蓄積容量と、該蓄積容量を構成する容量電極に所定電位を供給する第１配線とを備え、前記第１配線と同一膜として形成され、前記画像表示領域と前記周辺領域とを画する額縁領域の少なくとも一部を構成する額縁パターンとを備えている。

【００１１】

本発明の電気光学装置によれば、スイッチング素子の一例たる薄膜トランジスタに対し走査線を通じて走査信号が供給されることで、そのＯＮ・ＯＦＦが制御される。他方、画素電極に対しては、データ線を通じて画像信号が供給されることで、前記薄膜トランジスタのＯＮ・ＯＦＦに応じて、画素電極に当該画像信号の印加・非印加が行われる。これにより、本発明に係る電気光学装置は、いわゆるアクティブマトリクス駆動が可能とされている。また、本発明においては、画素電極における電位の所定期間保持する蓄積容量が形成されていることにより、該画素電極の電位保持特性が向上されている。

【００１２】

そして、本発明では特に、前記基板は、画像表示領域及び周辺領域を有し、このうちの前者には前記の画素電極、スイッチング素子、蓄積容量及び第１配線が形成されている。更に、本発明では、周辺領域又は画像表示領域及び周辺領域間を画する額縁領域の少なくとも一部に、前記第１配線と同一膜として形成された額縁パターンを備えている。ここで額縁領域とは、例えば、画像表示領域が矩形状である場合には、この矩形状の周囲を所定の幅でもって縁取った領域として規定される。したがって、この場合における額縁領域は、平面視して、ロの字状を有することになる。また、周辺領域は、画像表示領域の中心から見て、このロの字状となる額縁領域の外縁から以遠の領域として規定されることになる。また、「同一膜として形成」されているとは、当該電気光学装置の製造工程において、額縁パターン及び第１配線の前駆膜が同一の機会に成膜され、且つ、この前駆膜に対して

同時に所定のパターニング処理（例えば、フォトリソグラフィ及びエッチング工程等）が実施されることを意味する。

【００１３】

そして、前記額縁パターンは、前記のような額縁領域の少なくとも一部に形成されている。これにより、額縁領域を透過しようとする光は、額縁パターンによって、その進行が遮られることになる。したがって、本発明によれば、額縁パターンが形成されている領域に対応する分、背景技術で説明したような光漏れが生じることを未然に防止することが可能となり、もって、画像の周囲に各種の配線等のパターンの像が映り込むなどといったことを防止することが可能となるから、より品質の高い画像を表示することが可能となる。

【００１４】

なお、本発明において、額縁パターンは、画像表示領域に形成される第１配線と電気的に接続されているように形成されてもよいし、又は両者間はパターニング上分断されるように形成されてもよい。

【００１５】

また、本発明において、第１配線が容量電極に所定電位を供給する役割を果たすための構成としては、例えば、該第１配線が、容量電極に接続又は延設されるような構成を採用するとよい。ここに、「容量電極に接続」されるとは、例えば、容量電極及び第１配線が基板上に構築される積層構造中別々の層に形成されている場合において、両者間にコンタクトホールを介することで、これらを電気的に接続する等という場合を含む。他方、第１配線が、「容量電極に・・・延設」されるとは、例えば、該容量電極と平面的に連続する形状を有するパターン（即ち、このパターンにおいては、該パターンが形作られる平面内において第１配線と呼べる部分と容量電極と呼べる部分の双方を含むことになる。）が同一層に形成される等という場合を含む。

【００１６】

さらに、念のため、本発明にいう「額縁パターン」は、額縁領域上に形成されているがゆえに、その名が与えられているというにとどまり、該額縁パターンが、額縁のような形状を有しているということを必ずしも意味しない（額縁パターンが、「額縁領域の少なくとも一部」に形成されているということは、そのような趣旨を含む。）。また、このような額縁パターンは、額縁領域を越えて、周辺領域上に至るように形成されてもよい。

【００１７】

本発明の電気光学装置の他の態様では、前記基板に対向配置される対向基板と、前記基板及び前記対向基板を接着するシール材とを更に備えてなり、前記額縁パターンは、前記シール材が形成されるシール領域の少なくとも一部に形成されている。

【００１８】

この態様によれば、基板及び対向基板が、例えば光硬化性樹脂等からなるシール材により接着されている。この場合、額縁領域が、仮に前記のようなロの字状を有するものとすると、シール材が形成されるシール領域は、該額縁領域のロの字状の全部若しくは一部を含み又は含まずに該額縁領域の外縁以遠に位置し、且つ、該ロの字状よりも若干大きいロの字状を有するものと想定することができる（したがって、このシール領域の少なくとも一部は、前記周辺領域に含まれる領域である。）。

【００１９】

本態様によれば、このように、額縁領域以遠においても、前記額縁パターンが形成されていることにより、シール領域を透過しようとする光もまた、額縁パターンによって、その進行が遮られることになる。したがって、本発明によれば、画像の周囲に各種の配線等のパターンの像が映り込むなどといったことをより効果的に防止することが可能となるから、より品質の高い画像を表示することが可能となる。

【００２０】

本発明の電気光学装置の他の態様では、前記基板に対向配置される対向基板と、該対向基板上に形成される対向電極とを更に備えてなり、前記額縁パターンは、前記対向電極と電気的に接続されている接続部分を有する。

【００２１】
この態様によれば、額縁パターンは、対向電極と電気的に接続された接続部分を有する、すなわち対向電極及び額縁パターンは電気的に接続された状態となり、両者は常に同電位にあることになる。これによると、額縁パターンは、前述した光漏れ防止の機能と対向電極への電位供給機能という二つの機能を同時に果たすことになり、その分、装置構成の簡略化が図れることになる。
【００２２】
本発明の電気光学装置の他の態様では、前記額縁パターンは、前記第１配線と電気的に接続するように形成されている。
【００２３】
この態様によれば、額縁パターン及び第１配線は、常に同電位にあることになる。これによると、額縁パターンは、前述した光漏れ防止の機能と第１配線への電位供給機能という二つの機能を同時に果たすことになり、その分、装置構成の簡略化が図れることになる。ちなみに、額縁パターンと第１配線とは、上述のように同一膜として形成されていることから、両者を「電気的に接続するように形成」するとは、典型的には、額縁遮光膜及び第１配線に共通の前駆膜において両者を分断することなくパターニング処理する場合（すなわち、この場合においては、平面的に連続するパターン上、額縁パターンといえる部分と第１配線といえる部分の双方が存在する。）が想定されることになる。
【００２４】
また、本態様に併せて、前述した額縁パターン及び対向電極間の電気的接続が図られた態様を併せもてば、額縁パターン、対向電極及び第１配線の三者は、常に同電位にあることになる。これによると、装置構成の簡略化はより好適に達成されることになるのは言うまでもない。
【００２５】
接続部分を備える態様では、前記接続部分は、前記対向基板のコーナー部に対応して設けられているように構成してもよい。
【００２６】
このような構成によれば、例えば、画像表示領域が矩形状である場合には、該画像表示領域の四隅に対応するように、或いは該画像表示領域を縁取る額縁領域、或いはそれ以遠のシール領域の四隅に対応するように、接続部分を配置するなどということが可能となる。この場合、額縁パターン及び対向電極間の電気的接続を好適に図りつつ、画像表示を妨げないという作用効果が得られる。
【００２７】
なお、本態様にいう「コーナー部」とは、対向基板自体の四隅の部分を含むのは勿論、これら各隅から一定の平面的な広がり（例えば、当該隅の部分を中心とした同心円的な広がり）を有する部分をも含む概念である。また、接続部分が「コーナー部に対応して設けられている」ということには、該接続部分が前記したような四隅全部に設けられている場合の他、画像表示領域の三隅以下に対応するように設けられているなどという場合も含む。
【００２８】
本発明の電気光学装置の他の態様では、前記額縁パターンは、前記画像表示領域の周囲すべてを囲むように形成されている。
【００２９】
この態様によれば、額縁パターンが、前記画像表示領域の周囲すべてを囲むように形成されていることから、原理上は、額縁領域、或いはシール領域を透過する光を完全に遮断することも可能である。したがって、前記した光漏れの作用はより効果的に発揮されることになり、もってより高品質な画像を表示することが可能となる。
【００３０】
また、この態様において、前記画像表示領域の周囲すべてを囲むように形成された額縁パターンに、前記した対向電極との「接続部分」が存在する場合にあっては、この額縁パ

ターンと対向電極との電気的接続をより確実になすことができる。というのも、額縁パターンは、そのあらゆる部分が電気的に接続されている（換言すれば、間断なきパターンとして形成されている）こと、また、前記接続部分は、上述の例のように、画像表示領域の四隅、即ち額縁パターン、或いはシール領域の四隅に対応するように複数形成可能であることから、たとえ額縁パターンの一部、或いは接続部分のいずれかが何らかの事情により電気的に導通不能となった場合であっても、他の部分によって電気的導通を滞りなく実現することが可能だからである（言い換えれば、額縁パターン、或いは該額縁パターン上の接続部分について冗長的な構造がとられているということができる。）。これにより、このような態様においては、対向電極の電位を極めて安定に維持することが可能となり、該対向電極及び画素電極間に挟持される電気光学物質の一例たる液晶分子の配向状態の調整を好適に行うことができるから、より高品質な画像を表示することが可能となる。

【００３１】

他方、前述した額縁パターンが対向電極と電気的に接続されている接続部分を有する態様では、前記画像表示領域は平面視して矩形状を有し、前記額縁パターンは、前記矩形状の三辺に沿って連続して形成された第1のパターンと、残る一辺に沿って形成されるとともに前記第1のパターンと分断して形成された第２のパターンとを含み、前記接続部分は、前記第1のパターン上に存在するようにしてもよい。

【００３２】

このような構成によれば、まず、額縁パターンが矩形状を有する画像表示領域の三辺に沿って連続して形成された第1のパターンを含み、且つ、前記接続部分はこの第1のパターン上に存在するから、前述の画像表示領域の周囲すべてを囲むように額縁パターンが形成されている態様と同様、額縁パターン及び対向電極間の電気的接続をより確実になすことができ、対向電極の電位を極めて安定に維持することが可能となる。

【００３３】

また、本態様においては、この第1のパターンに加えて、前記矩形状の残る一辺に沿って形成されるとともに前記第1のパターンと分断して形成された第２のパターンを含むことから、次のような作用効果が得られる。すなわち、この第２のパターンの形成される領域が、例えばデータ線駆動回路が形成される領域に対応する場合においては、当該データ線駆動回路により制御されるサンプリング回路に引き回される画像信号線と、対向基板上の対向電極との間で容量カップリングが発生するおそれがある。この容量カップリングが発生すると、一方に対する通電によって、他方における電位に変動を与えてしまうため、所望どおりの画像の表示が困難となることになる。しかるに、本態様によれば、当該領域には、前記の第２のパターンが形成されていることから、画像信号線及び対向電極間には該第２のパターンが存在することになり、前記の容量カップリングの発生を抑制することができるのである。したがって、本態様によれば、所望どおりの画像を好適に表示することができる。

【００３４】

なお、このような作用効果は、前述した、額縁パターンを画像表示領域の周囲すべてを囲むように形成する態様においても、全く同様に享受できることは言うまでもない。

【００３５】

また、本態様にいう「第1のパターン」及び「第２のパターン」、更には以下に後述する態様にいう「第３のパターン」ないし「第６のパターン」という用語は、単に、それぞれが個別の概念で規定される半導体プロセス上のパターンであるということを表しているに過ぎない（換言すれば、「Ａ」乃至「Ｆ」というのは、単なる「名前」に過ぎない。）。

【００３６】

あるいは、前記画像表示領域は平面視して矩形状を有し、前記額縁パターンは、前記矩形状の対向する二辺に沿って形成された第３のパターンと、残る二辺に沿って形成されるとともに前記第３のパターンと分断して形成された第４のパターンとを含み、前記接続部分は、前記第３のパターン上に存在するようにしてもよい。

【００３７】
このような構成によれば、まず、額縁パターンが矩形状を有する画像表示領域の対向する二辺に沿って形成された第３のパターンを含み、且つ、前記接続部分はこの第３のパターン上に存在する。この第３のパターンは、前記の定義上、分断して形成される二本の直線状の配線が含まれることが一般的に想定される。この態様によれば、当該二本の直線状の配線それぞれには、前記接続部分が少なくとも二個存在し得る。したがって、対向電極及び額縁パターン間の電気的接続をより確実になすことができる。
【００３８】
また、本態様においては、この第３のパターンに加えて、前記矩形状の残る二辺に沿って形成されるとともに、前記第３のパターンと分断して形成された第４のパターンを含む。これにより、前記の第２のパターンと同様に、第４のパターンの形成される領域が、例えばデータ線駆動回路が形成される領域に対応する場合においては、画像信号線及び対向電極間の容量カップリングの発生を防止することができる。
【００３９】
さらには、前記画像表示領域は平面視して矩形状を有し、前記額縁パターンは、前記矩形状の一つの角部に対応する部分を除いて連続して形成された第５のパターンと、前記一つの角部に対応する部分に形成されるとともに前記第５のパターンと分断して形成された第６のパターンとを含み、前記接続部分は、前記第５のパターン及び前記第６のパターンの少なくとも一方の上に存在するようにしてもよい。
【００４０】
このような構成によれば、まず、額縁パターンが矩形状を有する画像表示領域の一つの角部に対応する部分を除いて連続して形成された第５のパターンを含み、且つ、該第５のパターン上に前記接続部分が存在し得る。したがって、典型的には、接続部分は、この第５のパターン上に三個存在することが考えられる。
【００４１】
また、本態様においては、この第５のパターンに加えて、前記一つの角部に対応する部分に形成されるとともに前記第５のパターンと分断して形成された第６のパターンを含み、且つ、該第６のパターン上に前記接続部分が存在し得る。したがって、典型的には、接続部分は、この第６のパターン上に一個存在することが考えられる。
【００４２】
以上により、本態様によれば、前述した額縁パターン及び対向電極間の電気的接続の確実性、或いは画像信号線及び対向電極間の容量カップリングの発生抑止等の作用効果が略同様に得られる。
【００４３】
なお、本態様に係る額縁パターンの態様、或いは前述した額縁パターンに関する各種の態様は、額縁パターンの形成態様のバリエーションを増加させる意義を有することは言うまでもない。これにより、外部回路接続端子から、データ線駆動回路、走査線駆動回路、或いは前記接続部分へ引き回す各種配線の配置（ないしはパターニング）を、より容易になすこと等も可能となる。
【００４４】
本発明の電気光学装置の他の態様では、前記周辺領域上に、前記基板の辺縁部に沿って形成された外部回路接続端子と、該外部回路接続端子に延設された第２配線とを更に備え、該第２配線の少なくとも一部は、前記第１配線と同一膜として、且つ、該第１配線と電気的に接続されて形成されている。
【００４５】
この態様によれば、周辺領域には外部回路接続端子及び第２配線が形成されており、このうちの第２配線の少なくとも一部が、第１配線と同一膜として、且つ、該第１配線と電気的に接続されて形成されている。ここで「同一膜として形成されている」とは、額縁パターン及び第１配線に関して既に述べたとおりの意義を有する。これによれば、第２配線の少なくとも一部及び第１配線は、データ線、走査線及び画素電極等が構成する積層構造

中同一の層に形成されることになり、また、両者は同一の材料から構成されることとなる。ちなみに、本発明においては第１配線と額縁パターンとが同一膜として形成されることから、本態様によれば結局、第１配線、額縁パターン及び第２配線のいずれもが同一膜として形成されるということになる。

【００４６】

これによれば、第一に、外部回路接続端子、第２配線及び第１配線を、同一層に形成することが可能となるから、これら各要素間における電気抵抗値を低下せしめることができる。

【００４７】

ちなみに、従来においては、前述のような各要素は別々の層に形成されることが行われており、これにより、該各要素間の電気的接続にはコンタクトホール等が利用されることがあった。しかしながら、コンタクトホールを利用してしまうと、該コンタクトホールに起因する高抵抗化がもたらされるおそれが大きいこと、また、コンタクトホール毎に特性が異なるという事態が生じ得ること等から、容量電極、或いはこれから延びる配線の時定数が大きくなり、結果、画像上にクロストークを発生させる等という不具合が生じることがあったのである。なお、前記の配線が、画像表示領域を横切るように形成されている場合には、いわゆる横クロストークとして観察されることになる。

【００４８】

しかるに、本態様においては、既に述べたように、外部回路接続端子、第２配線及び第１配線を同一層に形成することが可能であるから、上述のような不具合を被らなくて済むのである。

【００４９】

また第二に、本態様と、前記した額縁パターンに接続部分を有する態様、或いは画像表示領域の周囲すべてを囲むように額縁パターンが形成される態様、更には前記の第1のパターン、第２のパターン、第３のパターン、第４のパターン、第５のパターン及び第６のパターンを含む額縁パターンを備えた態様とを併せもった電気光学装置（以下、当該電気光学装置の態様を「併用態様」という。）に関しては特に、次のような特有の作用効果を奏することになる。すなわち、この併用態様に係る電気光学装置では、額縁パターンには、これと対向電極との間の接続部分が存在しているから、該額縁パターンは、前記の光漏れ防止の作用効果等に併せて、対向電極に所定の電位を供給する配線としての機能も有している。ここで、この併用態様では、この額縁パターンとともに、第２配線、第１配線もまた、同一膜として形成されているから、これら各要素及び外部回路接続端子間の電気抵抗値は低下せしめることが可能となっているのである。

【００５０】

このようなことから、前記併用態様においては、外部回路接続端子から、第２配線、そして額縁パターンに至るまでの電気抵抗値は低く抑えられることになるから、該額縁パターンの電位は安定した状態を維持することが可能となり、もって対向電極の電位も安定した状態に維持することが可能となるのである。さらに、額縁パターンには、第１配線が電気的に接続され得るから、該第１配線の電位、ひいてはこれに接続又は延設される容量電極の電位もまた、安定した状態に維持することが可能となる。

【００５１】

このように、併用態様によれば、額縁パターン、第２配線及び第１配線が同一膜且つ電気的に接続された状態で形成され、且つ、該額縁パターンに前記接続部分が存在することから、本態様に係る作用効果（低抵抗化）、及び接続部分を有することによる作用効果（対向電極に対する電位供給機能）の双方について、これをより効果的に享受することが可能となるのである。

【００５２】

この態様では、前記第１配線は、前記データ線の上に第１の層間絶縁膜を介して形成されているようにしてもよい。

【００５３】

このような構成によれば、基板上に構築される走査線、データ線、画素電極及び外部回路接続端子等からなる積層構造を好適に構成することが可能となる。

【００５４】

すなわち、まず、外部回路接続端子は、外部に曝される電極を備えなければならないことから、前記の積層構造中、比較的上層に形成されることが好ましい。さもなければ、積層構造の最上層部分から前記電極に通ずるような比較的深いコンタクトホール等を開孔しなければならないからである。他方、本態様によれば、第１配線は、データ線の上に形成されていることから、該第１配線と同一膜として形成され、外部回路接続端子に接続又は延設される第２配線もまた、データ線の上に形成されることになる。したがって、第２配線は、前記の積層構造中、比較的上層に形成されることになる。

【００５５】

以上により、本態様では、外部回路接続端子を比較的上層に形成するとしても、これに接続又は延設される第２配線もまた比較的上層に形成されることにより、両者間の電気的接続を無理なく実現することが可能となる。このように、本態様によれば、前記の積層構造を好適に形成することが可能となるのである。

【００５６】

或いは、前記第１配線は、前記画素電極を含む層の直下の層に形成されているようにしてもよい。

【００５７】

このような構成によれば、外部回路接続端子及び第２配線間の電気的接続を更に無理なく実現することが可能である。すなわち、画素電極が電気光学物質に対向する必要があることからすると、第１配線が画素電極を含む層の直下の層に形成されているということは、該第１配線が、電気光学物質の層からみて、画素電極との間に一層の絶縁膜を挟むのみで形成されているという場合が典型的には想定されることになる。そして、この場合、第１配線と同一膜として形成される第２配線もまた、画素電極を含む層の直下の層に形成されていることになるから、該第２配線の上には、通常、前記絶縁膜が存在するのみということになる。これは、周辺領域においては、画素電極の直下に形成される絶縁膜の表面が、外部に曝されることとなるのが通常だからである。

【００５８】

したがって、本態様によれば、外部回路接続端子を構成する電極を外部に曝すことは極めて容易となる。また、第２配線との電気的な接続は、前記の電極から該第２配線を延設することによればよい。

【００５９】

このように、本態様によれば、外部回路接続端子及び第２配線間の電気的接続を無理なく実現することが可能となるのである。

【００６０】

また、第２配線を備える電気光学装置の他の態様では、前記第１配線及び前記額縁パターンは電気的に接続されて形成されておらず、且つ、前記第２配線の第１部分及び前記第１配線が電気的に接続され、前記第２配線の第２部分及び前記額縁パターンが電気的に接続されており、前記第１部分は前記外部回路接続端子の第１部分に、前記第２部分は前記外部回路接続端子の第２部分にそれぞれ接続されているようにしてもよい。

【００６１】

このような構成によれば、額縁パターン及び第１配線のそれぞれを異なる電位に維持することができる。この場合、第１配線が容量電極に所定電位を供給するためのものであることに注意するとともに、額縁パターンに対向電極が接続されているという前提を置けば、額縁パターン及び第１配線のそれぞれを異なる電位に維持することができるということは、容量電極及び対向電極のそれぞれを異なる電位に維持することができるということに同義になる。これは、外部回路接続端子の第１部分にある電位を供給すれば、当該第１部分が、第２配線の第１部分、第１配線及び容量電極に接続されていることから、容量電極は当該電位に維持される一方、外部回路接続端子の第２部分に前記ある電位とは異なる電

位を供給すれば、当該第２部分が、第２配線の第２部分、額縁パターン及び対向電極に接続されていることから、対向電極は当該電位に維持されることとなるからである。これをまとめれば、以下の表１のようになる。なお、これら各概念を具体化したものについては、後に説明する発明の実施の形態において、〔第５実施形態〕として説明されている。

【００６２】

【表１】

	電気の流れは左欄から右欄へ（上欄と下欄とは各々独立の電気の流れを表している）			
容量電極への電気の流れ	外部回路接続端子の第１部分	第２配線の第１部分	第１配線	容量電極
対向電極への電気の流れ	外部回路接続端子の第２部分	第２配線の第２部分	額縁パターン	対向電極

【００６３】

これにより、本態様によれば、当該電気光学装置内で発生する各種の電気作用を好適に調整すること等ができる。

【００６４】

本発明の電気光学装置の他の態様では、第１配線は、遮光性材料から構成されている。

【００６５】

この態様によれば、第１配線は容量電極に接続又は延設される配線であって画像表示領域内に形成されるものであるから、画像表示領域内において、当該第１配線が形成されている領域に対応した遮光を実現することができる。これにより、前記スイッチング素子の一例たる薄膜トランジスタを構成する半導体層（活性層）に、みだりに光が入射するという事態を未然に防止することが可能となるから、該半導体層における光リーク電流の発生を抑制することができ、したがって、画像上にフリッカ等が発生することを未然に防止することが可能となる。

【００６６】

また、本態様によれば、該第１配線と同一膜として形成される第２配線もまた、遮光性材料から構成されることになる。したがって、周辺領域上に形成されるスイッチング素子としての薄膜トランジスタについても、前記と同様な作用効果を得ることができ、もって、当該薄膜トランジスタの正確な動作を期することができる。

【００６７】

そしてさらに、本態様によれば、前記第１配線と同一膜として形成される額縁パターンもまた、遮光性材料から構成されることになる。したがって、前記の光漏れ防止の作用効果は、より効果的に享受されることになる。

【００６８】

なお、本態様にいう「遮光性材料」としては、例えば、光反射率が比較的大きいＡｌ（アルミニウム）等を含むほか、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）等の高融点金属のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの等も含む。

【００６９】

本発明の電気光学装置の他の態様では、前記第１配線は、相異なる材料からなる積層構造を有する。

【００７０】

この態様によれば、例えば、第１配線の下層にアルミニウムからなる層、その上層に窒

化チタンからなる層等といった二層構造として構成される。この場合、下層のアルミニウム層によれば、高い電気伝導性能及び光反射率が比較的高いことによる遮光性能を享受することができると同時に、上層の窒化チタン層によれば、第１配線上に形成される層間絶縁膜等の前駆膜をパターニング処理する際、或いは該層間絶縁膜等にコンタクトホールを形成する際に、いわゆる突き抜けの発生を防止する機能を享受すること（即ち、該窒化チタンからなる層は、いわゆるエッチストップとして機能する）が可能となる。

【００７１】

このように、本態様によれば、第１配線が「積層構造」を有するものとして構成されることにより、該第１配線に、容量電極に電位を供給するという機能を担わせるのに加えて、新たな機能を付与することが可能であり、その高機能化を図ることができる。

【００７２】

なお、本態様にいう「積層構造」としては、上述の他、種々の構成を採用することが可能であることは言うまでもない。

【００７３】

また、本態様によれば、第１配線と同一膜として形成される第２配線及び額縁パターンもまた、相異なる材料からなる積層構造を有することになるが、この積層構造を構成する各材料の選択は、該第２配線及び該額縁パターンの担う機能（即ち、外部回路接続端子と走査線駆動回路及びデータ線駆動回路の接続（第２配線）や、第２配線から第１配線への電位供給の橋渡し（額縁パターン）等）に考慮した上で、新たな機能を付与するという観点から行うとよい。なお、低抵抗材料の一例たるアルミニウムを含む前記の二層構造は、このような観点からも好ましいということが言える。

【００７４】

本発明の電気光学装置の他の態様では、前記基板に対向配置される対向基板と、該対向基板上に形成された遮光膜を更に備えてなり、前記額縁パターンは、前記遮光膜と重なるように形成されている。

【００７５】

この態様によれば、例えば、対向基板から基板へ向けて光を投射する場合において、額縁領域では、まず、前記遮光膜による遮光が行われ、続いて、額縁パターンによる遮光が行われる。このように、本態様によれば、二重の遮光が実現されることにより、前述した光漏れ防止の作用効果は、より効果的に奏されることになる。

【００７６】

この態様では、前記遮光膜は、前記対向基板の辺縁部に沿うように形成された額縁遮光膜を含むようにしてもよい。

【００７７】

このような構成によれば、遮光膜が額縁遮光膜を含むことから、前述の二重の遮光は、よりよく実現されることになる。

【００７８】

本発明の電子機器は、上記課題を解決するために、上述の本発明の電気光学装置（ただし、その各種態様を含む。）を具備してなる。

【００７９】

本発明の電子機器によれば、上述した本発明の電気光学装置を具備してなるので、画像の周囲に各種の配線等のパターンの像が映り込むなどといったことが未然に防止されることにより、高品質な画像が表示可能な、プロジェクタ、液晶テレビ、携帯電話、電子手帳、ワードプロセッサ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルなどの各種電子機器を実現できる。

【００８０】

本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにされる。

【発明を実施するための最良の形態】

【００８１】

以下では、本発明の実施の形態について図を参照しつつ説明する。以下の実施形態は、本発明の電気光学装置を液晶装置に適用したものである。

【００８２】

〔第１実施形態〕

〔電気光学装置の全体構成〕

まず、本発明の電気光学装置に係る第１実施形態の全体構成について、図１及び図２を参照して説明する。ここに、図１は、ＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た電気光学装置の平面図であり、図２は、図１のＨ－Ｈ’断面図である。ここでは、電気光学装置の一例である駆動回路内蔵型のＴＦＴアクティブマトリクス駆動方式の液晶装置を例にとる。

【００８３】

図１及び図２において、第１実施形態に係る電気光学装置では、ＴＦＴアレイ基板１０と対向基板２０とが対向配置されている。ＴＦＴアレイ基板１０と対向基板２０との間に液晶層５０が封入されており、ＴＦＴアレイ基板１０と対向基板２０とは、画像表示領域１０ａの周囲に位置するシール領域に設けられたシール材５２により相互に接着されている。

【００８４】

シール材５２は、両基板を貼り合わせるための、例えば紫外線硬化樹脂、熱硬化樹脂等からなり、製造プロセスにおいてＴＦＴアレイ基板１０上に塗布された後、紫外線照射、加熱等により硬化させられたものである。また、シール材５２中には、ＴＦＴアレイ基板１０と対向基板２０との間隔（基板間ギャップ）を所定値とするためのグラスファイバ或いはガラスビーズ等のギャップ材が散布されている。即ち、第１実施形態の電気光学装置は、プロジェクタのライトバルブ用として小型で拡大表示を行うのに適している。

【００８５】

シール材５２が配置されたシール領域の内側に並行して、画像表示領域１０ａの額縁領域を規定する遮光性の額縁遮光膜５３が、対向基板２０側に設けられている。但し、このような額縁遮光膜５３の一部又は全部は、ＴＦＴアレイ基板１０側に内蔵遮光膜として設けられてもよい。なお、第１実施形態においては、前記の画像表示領域１０ａの周辺を規定する周辺領域が存在する。言い換えれば、第１実施形態においては特に、ＴＦＴアレイ基板１０の中心から見て、この額縁遮光膜５３より以遠が周辺領域として規定されている。

【００８６】

周辺領域のうち、シール材５２が配置されたシール領域の外側に位置する領域には、データ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられている。また、走査線駆動回路１０４は、この一辺に隣接する２辺に沿い、且つ、前記額縁遮光膜５３に覆われるようにして設けられている。更に、このように画像表示領域１０ａの両側に設けられた二つの走査線駆動回路１０４間をつなぐため、ＴＦＴアレイ基板１０の残る一辺に沿い、且つ、前記額縁遮光膜５３に覆われるようにして複数の配線１０５が設けられている。このうちデータ線駆動回路１０１及び走査線駆動回路１０４は、外部回路接続端子１０２と配線４０４を介して接続されている。

【００８７】

また、対向基板２０の４つのコーナー部には、両基板間の上下導通端子として機能する上下導通材１０６が配置されている。この上下導通材１０６は、銀粉等の導電性粒子が固められた構成等からなる。他方、ＴＦＴアレイ基板１０にはこれらのコーナー部に対向する領域において上下導通端子が設けられている。これらにより、ＴＦＴアレイ基板１０と対向基板２０との間で電気的な導通をとることができる。

【００８８】

図２において、ＴＦＴアレイ基板１０上には、画素スイッチング用のＴＦＴや走査線、データ線等の配線が形成された後の画素電極９ａ上に、配向膜が形成されている。他方、対向基板２０上には、対向電極２１の他、格子状又はストライプ状の遮光膜２３、更には

最上層部分に配向膜が形成されている。また、液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなり、これら一対の配向膜間で、所定の配向状態をとる。

【００８９】

以上のような全体構成を有する第１実施形態の電気光学装置においては、上述した各種要素のうち、配線４０４、上下導通材１０６等に関する具体的構成について特徴があるが、その点については、図７等を参照しながら後に詳述する。

【００９０】

なお、図１及び図２に示したＴＦＴアレイ基板１０上には、これらのデータ線駆動回路１０１、走査線駆動回路１０４等に加えて、画像信号線上の画像信号をサンプリングしてデータ線に供給するサンプリング回路、複数のデータ線に所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等を形成してもよい。

【００９１】

〔画素部における構成〕

以下では、本発明の第１実施形態における電気光学装置の画素部における構成について、図３から図７を参照して説明する。ここに図３は、電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路であり、図４及び図５は、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。なお、図４及び図５は、それぞれ、後述する積層構造のうち下層部分（図４）と上層部分（図５）とを分かって図示している。

【００９２】

また、図６は、図４及び図５を重ね合わせた場合のＡ－Ａ´断面図であり、図７（ａ）及び図７（ｂ）は、それぞれ、図２における符号Ｚを付した円内部分の拡大図及び図１における上下導通材１０６が存在する部分に関する断面図であって、いずれも図６に示す積層構造に対応する断面図である。なお、図６及び図７においては、各層・各部材を図面上で認識可能な程度の大きさとするため、該各層・各部材ごとに縮尺を異ならしめてある。

【００９３】

（画素部の回路構成）

図３において、第１実施形態における電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素には、それぞれ、画素電極９ａと当該画素電極９ａをスイッチング制御するためのＴＦＴ３０とが形成されており、画像信号が供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されている。データ線６ａに書き込む画像信号Ｓ１、Ｓ２、・・・、Ｓｎは、この順に線順次に供給しても構わないし、相隣接する複数のデータ線６ａ同士に対して、グループ毎に供給するようにしてもよい。

【００９４】

また、ＴＦＴ３０のゲートにゲート電極３ａが電気的に接続されており、所定のタイミングで、走査線１１ａ及びゲート電極３ａにパルス的に走査信号Ｇ１、Ｇ２、・・・、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、・・・、Ｓｎを所定のタイミングで書き込む。

【００９５】

画素電極９ａを介して電気光学物質の一例としての液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、・・・、Ｓｎは、対向基板に形成された対向電極との間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能とする。ノーマリーホワイトモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が減少し、ノーマリーブラックモードであれば、各画素の単位で印加された電圧に応じて入射光に対する透過率が増加され、全体として電気光学装置からは画像信号に応じたコントラストをもつ光が出射する。

【００９６】
ここで保持された画像信号がリークするのを防ぐために、画素電極９ａと対向電極との間に形成される液晶容量と並列に蓄積容量７０を付加する。この蓄積容量７０は、走査線１１ａに並んで設けられ、固定電位側容量電極を含むとともに定電位に固定された容量電極３００を含んでいる。
【００９７】
〔画素部の具体的構成〕
以下では、上記データ線６ａ、走査線１１ａ及びゲート電極３ａ、ＴＦＴ３０等による、上述のような回路動作が実現される電気光学装置の、具体的の構成について、図４乃至図７を参照して説明する。
【００９８】
まず、図４及び図５において、画素電極９ａは、ＴＦＴアレイ基板１０上に、マトリクス状に複数設けられており（点線部により輪郭が示されている）、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ及び走査線１１ａが設けられている。データ線６ａは、後述するようにアルミニウム膜等を含む積層構造からなり、走査線１１ａは、例えば導電性のポリシリコン膜等からなる。また、走査線１１ａは、半導体層１ａのうち図中右上がりの斜線領域で示したチャネル領域１ａ´に対向するゲート電極３ａにコンタクトホール１２ｃｖを介して電気的に接続されており、該ゲート電極３ａは該走査線１１ａに含まれる形となっている。
【００９９】
すなわち、ゲート電極３ａとデータ線６ａとの交差する箇所にはそれぞれ、チャネル領域１ａ´に、走査線１１ａに含まれるゲート電極３ａが対向配置された画素スイッチング用のＴＦＴ３０が設けられている。これによりＴＦＴ３０（ゲート電極を除く。）は、ゲート電極３ａと走査線１１ａとの間に存在するような形態となっている。
【０１００】
次に、電気光学装置は、図４及び図５のＡ－Ａ´線断面図たる図６に示すように、例えば、石英基板、ガラス基板、シリコン基板からなるＴＦＴアレイ基板１０と、これに対向配置される、例えばガラス基板や石英基板からなる対向基板２０とを備えている。
【０１０１】
ＴＦＴアレイ基板１０の側には、図６に示すように、前記の画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９ａは、例えばＩＴＯ膜等の透明導電性膜からなる。他方、対向基板２０の側には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は、上述の画素電極９ａと同様に、例えばＩＴＯ膜等の透明導電性膜からなる。
【０１０２】
このように対向配置されたＴＦＴアレイ基板１０及び対向基板２０間には、前述のシール材５２（図１及び図２参照）により囲まれた空間に液晶等の電気光学物質が封入され、液晶層５０が形成される。液晶層５０は、画素電極９ａからの電界が印加されていない状態で配向膜１６及び２２により所定の配向状態をとる。
【０１０３】
一方、ＴＦＴアレイ基板１０上には、前記の画素電極９ａ及び配向膜１６の他、これらを含む各種の構成が積層構造をなして備えられている。この積層構造は、図６に示すように、下から順に、走査線１１ａを含む第１層、ゲート電極３ａを含むＴＦＴ３０等を含む第２層、蓄積容量７０を含む第３層、データ線６ａ等を含む第４層、本発明にいう「第１配線」の一例たる容量配線４００等を含む第５層、前記の画素電極９ａ及び配向膜１６等を含む第６層（最上層）からなる。
【０１０４】
また、第１層及び第２層間には下地絶縁膜１２が、第２層及び第３層間には第１層間絶縁膜４１が、第３層及び第４層間には第２層間絶縁膜４２が、第４層及び第５層間には第

３層間絶縁膜４３が、第５層及び第６層間には第４層間絶縁膜４４が、それぞれ設けられており、前述の各要素間が短絡することを防止している。また、これら各種の絶縁膜１２、４１、４２、４３及び４４には、例えば、ＴＦＴ３０の半導体層１ａ中の高濃度ソース領域１ｄとデータ線６ａとを電気的に接続するコンタクトホール等もまた設けられている。以下では、これらの各要素について、下から順に説明を行う。なお、前述のうち第１層から第３層までが、下層部分として図４に図示されており、第４層から第６層までが上層部分として図５に図示されている。

【０１０５】

（積層構造・第１層の構成-走査線等-）

まず、第１層には、例えば、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ等の高融点金属のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの、或いは導電性ポリシリコン等からなる走査線１１ａが設けられている。この走査線１１ａは、平面的にみて、図４のＸ方向に沿うように、ストライプ状にパターニングされている。より詳しく見ると、ストライプ状の走査線１１ａは、図４のＸ方向に沿うように延びる本線部と、データ線６ａ或いは容量配線４００が延在する図４のＹ方向に延びる突出部とを備えている。なお、隣接する走査線１１ａから延びる突出部は相互に接続されることはなく、したがって、該走査線１１ａは１本１本分断された形となっている。

【０１０６】

（積層構造・第２層の構成-ＴＦＴ等-）

次に、第２層として、ゲート電極３ａを含むＴＦＴ３０が設けられている。ＴＦＴ３０は、図６に示すように、ＬＤＤ（Lightly Doped Drain）構造を有しており、その構成要素としては、上述したゲート電極３ａ、例えばポリシリコン膜からなりゲート電極３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１ａ´、ゲート電極３ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁膜２、半導体層１ａにおける低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを備えている。

【０１０７】

また、第１実施形態では、この第２層に、上述のゲート電極３ａと同一膜として中継電極７１９が形成されている。この中継電極７１９は、平面的に見て、図４に示すように、各画素電極９ａのＸ方向に延びる一辺の略中央に位置するように、島状に形成されている。中継電極７１９とゲート電極３ａとは同一膜として形成されているから、後者が例えば導電性ポリシリコン膜等からなる場合においては、前者もまた、導電性ポリシリコン膜等からなる。

【０１０８】

（積層構造・第１層及び第２層間の構成-下地絶縁膜-）

図６に示すように、以上説明した走査線１１ａの上、かつ、ＴＦＴ３０の下には、例えばシリコン酸化膜等からなる下地絶縁膜１２が設けられている。下地絶縁膜１２は、走査線１１ａからＴＦＴ３０を層間絶縁する機能のほか、ＴＦＴアレイ基板１０の全面に形成されることにより、ＴＦＴアレイ基板１０の表面研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用のＴＦＴ３０の特性変化を防止する機能を有する。

【０１０９】

この下地絶縁膜１２には、平面的にみて半導体層１ａの両脇に、後述するデータ線６ａに沿って延びる半導体層１ａのチャネル長の方向に沿った溝状のコンタクトホール１２ｃｖが掘られており、このコンタクトホール１２ｃｖに対応して、その上方に積層されるゲート電極３ａは下側に凹状に形成された部分を含んでいる。また、このコンタクトホール１２ｃｖ全体を埋めるようにして、ゲート電極３ａが形成されていることにより、該ゲート電極３ａには、これと一体的に形成された側壁部３ｂが延設されるようになっている。これにより、ＴＦＴ３０の半導体層１ａは、図４によく示されているように、平面的にみて側方から覆われるようになっており、少なくともこの部分からの光の入射が抑制されるようになっている。

【０１１０】
また、この側壁部３ｂは、図４に示すように、前記のコンタクトホール１２ｃｖを埋めるように形成されているとともに、その下端が前記の走査線１１ａと接するようにされている。ここで走査線１１ａは、上述のようにストライプ状に形成されていることから、ある行に存在するゲート電極３ａ及び走査線１１ａは、当該行に着目する限り、常に同電位となる。
【０１１１】
（積層構造・第３層の構成-蓄積容量等-）
さて、図６に示すように、前述の第２層に続けて第３層には、蓄積容量７０が設けられている。蓄積容量７０は、ＴＦＴ３０の高濃度ドレイン領域１ｅ及び画素電極９ａに接続された画素電位側容量電極としての下部電極７１と、固定電位側容量電極としての容量電極３００とが、誘電体膜７５を介して対向配置されることにより形成されている。この蓄積容量７０によれば、画素電極９ａにおける電位保持特性を顕著に高めることが可能となる。また、第１実施形態に係る蓄積容量７０は、図４の平面図を見るとわかるように、画素電極９ａの形成領域にほぼ対応する光透過領域には至らないように形成されているため（換言すれば、遮光領域内に収まるように形成されているため）、電気光学装置全体の画素開口率は比較的大きく維持され、これにより、より明るい画像を表示することが可能となる。
【０１１２】
ここで、上記画素電位側容量電極としての電極が下部電極７１とは逆に蓄積容量７０の上部に設けられる構成でもよい。この場合、当然のことながら固定電位側容量電極としての容量電極３００は蓄積容量７０の下部に設けられることとなる。好適な例としては、画素電位側容量電極がＴＦＴ３０の高濃度ドレイン領域１ｅの延長された高濃度ドレイン領域１ｅと同一膜であり、固定電位側容量電極としての容量電極３００は、ＴＦＴ３０よりさらに下方にあり、ＴＦＴ３０に下方から侵入する入射光を遮光するための遮光層と同一層であってもよい。この場合の後述する容量配線４００は、固定電位側容量電極としての容量電極３００と同一層の膜であることが構造が簡単になり好ましいが、これに限定するものではない。
【０１１３】
より詳細には、下部電極７１は、例えば導電性のポリシリコン膜からなり画素電位側容量電極として機能する。ただし、下部電極７１は、金属又は合金を含む単一層膜又は多層膜から構成してもよい。また、この下部電極７１は、画素電位側容量電極としての機能のほか、画素電極９ａとＴＦＴ３０の高濃度ドレイン領域１ｅとを中継接続する機能をもつ。ちなみに、ここにいう中継接続は、前記の中継電極７１９を介して行われている。
【０１１４】
容量電極３００は、蓄積容量７０の固定電位側容量電極として機能する。第１実施形態において、容量電極３００を固定電位とするためには、固定電位とされた容量配線４００（後述する。）と電気的接続が図られることによりなされている。ここでは、容量電極３００を固定電位とするための接続において、容量配線４００を中継しているが、例えば容量配線４００を容量電極３００と同一膜として延長して形成してもよい。かかる構成により、容量配線４００を別層として必要とせず、接続抵抗による配線抵抗増大もなくなり、容量配線４００としての層を別に設ける必要も無いためプロセスも簡単になる。
【０１１５】
また、容量電極３００は、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ等の高融点金属のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド、ポリシリサイド、これらを積層したもの、或いは好ましくはタングステンシリサイドからなる。
【０１１６】
これにより、容量電極３００は、ＴＦＴ３０に上側から入射しようとする光を遮る機能を有している。
【０１１７】

誘電体膜７５は、図６に示すように、例えば膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ（High Temperature Oxide）膜、ＬＴＯ（Low Temperature Oxide）膜等の酸化シリコン膜、あるいは窒化シリコン膜等から構成される。蓄積容量７０を増大させる観点からは、膜の信頼性が十分に得られる限りにおいて、誘電体膜７５は薄いほどよい。

【０１１８】

第１実施形態において、この誘電体膜７５は、図６に示すように、下層に酸化シリコン膜７５ａ、上層に窒化シリコン膜７５ｂというように二層構造を有するものとなっている。上層の窒化シリコン膜７５ｂは画素電位側容量電極の下部電極７１より少し大きなサイズにパターニングされ、遮光領域（非開口領域）内で収まるように形成されている。

【０１１９】

（積層構造、第２層及び第３層間の構成-第１層間絶縁膜-）

以上説明したＴＦＴ３０ないしゲート電極３ａ及び中継電極７１９の上、かつ、蓄積容量７０の下には、例えば、ＮＳＧ（ノンシリケートガラス）、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）等のシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等、あるいは好ましくはＮＳＧからなる第１層間絶縁膜４１が形成されている。

【０１２０】

そして、この第１層間絶縁膜４１には、ＴＦＴ３０の高濃度ソース領域１ｄと後述するデータ線６ａとを電気的に接続するコンタクトホール８１が、後記第２層間絶縁膜４２を貫通しつつ開孔されている。また、第１層間絶縁膜４１には、ＴＦＴ３０の高濃度ドレイン領域１ｅと蓄積容量７０を構成する下部電極７１とを電気的に接続するコンタクトホール８３が開孔されている。さらに、この第１層間絶縁膜４１には、蓄積容量７０を構成する画素電位側容量電極としての下部電極７１と中継電極７１９とを電気的に接続するためのコンタクトホール８８１が開孔されている。更に加えて、第１層間絶縁膜４１には、中継電極７１９と後述する第２中継電極６ａ２とを電気的に接続するためのコンタクトホール８８２が、後記第２層間絶縁膜を貫通しつつ開孔されている。

【０１２１】

（積層構造・第４層の構成-データ線等-）

さて、前述の第３層に続けて第４層には、データ線６ａが設けられている。このデータ線６ａは、図６に示すように、下層より順に、アルミニウムからなる層（図６における符号４１Ａ参照）、窒化チタンからなる層（図６における符号４１ＴＮ参照）、窒化シリコン膜からなる層（図６における符号４０１参照）の三層構造を有する膜として形成されている。窒化シリコン膜は、その下層のアルミニウム層と窒化チタン層を覆うように少し大きなサイズにパターニングされている。

【０１２２】

また、この第４層には、データ線６ａと同一膜として、容量配線用中継層６ａ１及び第２中継電極６ａ２が形成されている。これらは、図５に示すように、平面的に見ると、データ線６ａと連続した平面形状を有するように形成されているのではなく、各者間はパターニング上分断されるように形成されている。例えば図５中最左方に位置するデータ線６ａに着目すると、その直右方に略四辺形状を有する容量配線用中継層６ａ１、更にその右方に容量配線用中継層６ａ１よりも若干大きめの面積をもつ略四辺形状を有する第２中継電極６ａ２が形成されている。

【０１２３】

（積層構造・第３層及び第４層間の構成-第２層間絶縁膜-）

以上説明した蓄積容量７０の上、かつ、データ線６ａの下には、例えばＮＳＧ、ＰＳＧ，ＢＳＧ、ＢＰＳＧ等のシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等、あるいは好ましくはＴＥＯＳガスを用いたプラズマＣＶＤ法によって形成された第２層間絶縁膜４２が形成されている。この第２層間絶縁膜４２には、ＴＦＴ３０の高濃度ソース領域１ｄとデータ線６ａとを電気的に接続する、前記のコンタクトホール８１が開孔されているとともに、前記容量配線用中継層６ａ１と蓄積容量７０の上部電極たる容量電極３００

とを電気的に接続するコンタクトホール８０１が開孔されている。さらに、第２層間絶縁膜４２には、第２中継電極６ａ２と中継電極７１９とを電気的に接続するための、前記のコンタクトホール８８２が形成されている。

【０１２４】

（積層構造・第５層の構成-容量配線等-）

さて、前述の第４層に続けて第５層には、容量配線４００が形成されている。この容量配線４００は、平面的にみると、図５に示すように、図中Ｘ方向及びＹ方向それぞれに延在するように、格子状に形成されている。該容量配線４００のうち図中Ｙ方向に延在する部分については特に、データ線６ａを覆うように、且つ、該データ線６ａよりも幅広に形成されている。また、図中Ｘ方向に延在する部分については、後述の第３中継電極４０２を形成する領域を確保するために、各画素電極９ａの一辺の中央付近に切り欠き部を有している。

【０１２５】

さらには、図５中、ＸＹ方向それぞれに延在する容量配線４００の交差部分の隅部においては、該隅部を埋めるようにして、略三角形状の部分が設けられている。容量配線４００に、この略三角形状の部分が設けられていることにより、ＴＦＴ３０の半導体層１ａに対する光の遮蔽を効果的に行うことができる。すなわち、半導体層１ａに対して、斜め上から進入しようとする光は、この三角形状の部分で反射又は吸収されることになり半導体層１ａには至らないことになる。したがって、光リーク電流の発生を抑制的にし、フリッカ等のない高品質な画像を表示することが可能となる。

【０１２６】

この容量配線４００は、画素電極９ａが配置された画像表示領域１０ａからその周囲に延設され、対向電極電位や、駆動回路やその他周辺回路の定電位源と電気的に接続されることで、固定電位とされている（後の配線４０４に関する説明参照）。

【０１２７】

このように、データ線６ａの全体を覆うように形成されているとともに、固定電位とされた容量配線４００の存在によれば、該データ線６ａ及び画素電極９ａ間に生じる容量カップリングの影響を排除することが可能となる。すなわち、データ線６ａへの通電に応じて、画素電極９ａの電位が変動するという事態を未然に回避することが可能となり、画像上に該データ線６ａに沿った表示ムラ等を発生させる可能性を低減することができる。第１実施形態においては特に、容量配線４００は格子状に形成されているから、走査線１１ａが延在する部分についても無用な容量カップリングが生じないように、これを抑制することが可能となっている。

【０１２８】

また、第５層には、このような容量配線４００と同一膜として、第３中継電極４０２が形成されている。この第３中継電極４０２は、後述のコンタクトホール８０４及び８９を介して、第２中継電極６ａ２及び画素電極９ａ間の電気的接続を中継する機能を有する。なお、これら容量配線４００及び第３中継電極４０２間は、平面形状的に連続して形成されているのではなく、両者間はパターニング上分断されるように形成されている。

【０１２９】

他方、上述の容量配線４００及び第３中継電極４０２は、下層にアルミニウムからなる層、上層に窒化チタンからなる層の二層構造を有している。このように容量配線４００及び第３中継電極４０２は、光反射性能に比較的優れたアルミニウムを含み、且つ、光吸収性能に比較的優れた窒化チタンを含むことから、該容量配線４００及び該第３中継層４０２は遮光層として機能し得る。すなわち、これらによれば、ＴＦＴ３０の半導体層１ａに対する入射光（図６参照）の進行を、その上側でさえぎることが可能である。

【０１３０】

そして、第１実施形態においては特に、画像表示領域１０ａ以外の領域に、図７（ａ）及び図７（ｂ）に示すように、上述の容量配線４００に延設された引き回し配線、より詳しくは、配線４０４（本発明にいう「第２配線」の一例に該当する。）及び額縁パターン

４０６からなる引き回し配線が形成されている。以下では、この引き回し配線の構成について、前述までに触れた各図及び図８を参照しながら説明する。ここに図８は、図１と同趣旨の図であって、特に配線４０４及び額縁パターン４０６からなる引き回し配線と容量配線４００との配置関係を明瞭に図示するための図である。なお、図８においては、前記の目的のため、特に配線４０４の縮尺、或いは額縁パターン４０６の縮尺、平面形状及び配列ピッチ等について適宜視認可能なように変更を加えており、また、図１等に示された要素のうちの幾つか（例えば、図１のデータ線駆動回路１０１、或いは図５の第３中継電極４０２等）の図示が適宜省略されている。

【０１３１】

まず、周辺領域には、図７（ａ）及び図８に示すように、容量配線４００に額縁パターン４０６を介して延設された配線４０４が形成されている。すなわち、この配線４０４は、第３層間絶縁膜４３上で、容量配線４００及び第３中継電極４０２（以下、「容量配線４００等」ということがある。）と同一膜として形成されている。これにより、配線４０４は、前述の容量配線４００及び第３中継電極４０２と同様に、下層にアルミニウムからなる層、上層に窒化チタンからなる層という二層構造を有している。

【０１３２】

この配線４０４の一部は、図１及び図２を参照して説明した外部回路接続端子１０２Ｑを構成する。具体的には、配線４０４上に形成された第４層間絶縁膜４４に、該配線４０４へ通ずるコンタクトホール４４Ｈ１が形成されることにより、該配線４０４の上面が外部へ露出することによって、外部回路接続端子１０２Ｑが形成されるようになっている。

【０１３３】

なお、この際、コンタクトホール４４Ｈ１の開口時、配線４０４の上層の窒化チタンからなる膜を取り除いてもよい。これにより、該配線４０４と外部回路とを電気的に接続する際、該外部回路は、下層のアルミニウムからなる膜と直接接続されることになるため、接続面で低抵抗化を実現できる。また、配線４０４の上層の窒化チタンからなる膜を残存させたままであると、当該外部回路接続端子１０２Ｑを介して当該電気光学装置の検査を実施する際に、該窒化チタンからなる膜が硬質の膜であるため、検査端子が滑り検査しにくいという不具合の生じることが懸念されるが、該窒化チタンからなる膜を取り除けば、そのような不具合を被らなくて済む。

【０１３４】

ちなみに、図７（ａ）に示すような配線４０４は、図１に示す外部回路接続端子１０２のすべてについて同様に形成されているが、それらのうち容量配線４００に延設されているもの、即ち該容量配線４００と電気的な連絡が図られているものは、当該それらのうちの一部である。すなわち、図８又は図１に示すように、外部回路接続端子１０２のうち、特定の外部回路接続端子１０２Ｑに対応する配線４０４のみが容量配線４００と延設されて形成されるようになっており、残りの外部回路接続端子１０２に対応する配線４０４については、容量配線４００等と同一膜として形成されているものの、両者は、パターニング上分断されるように形成されている。

【０１３５】

他方、第１実施形態においては更に、図７（ｂ）及び図８に示すように、前記の容量配線４００等、更には上述した配線４０４に延設された額縁パターン４０６が形成されている。すなわち、この額縁パターン４０６は、第３層間絶縁膜４３上で、容量配線４００等及び額縁パターン４０６と同一膜として形成されている。これにより、額縁パターン４０６もまた、前述の容量配線４００等と同様に、下層にアルミニウムからなる層、上層に窒化チタンからなる層という二層構造を有している。

【０１３６】

額縁パターン４０６は、図８に示すように、平面視して画像表示領域１０ａと周辺領域とを画する額縁領域（即ち、額縁遮光膜５３の形成領域に対応する領域）及び該額縁領域の周囲のシール材５２の形成領域を埋めるように、或いは画像表示領域１０ａの周囲すべてを囲むように形成されており、全体として略ロの字状を有している。この額縁パターン

４０６は、図８中下方に示すように、前記の特定の外部回路接続端子１０２Ｑに接続された配線４０４に延設されているから、額縁パターン４０６及び特定の外部回路接続端子１０２Ｑは、相互に電気的に接続されている。また、額縁パターン４０６は容量配線４００に延設されていることにより、該容量配線４００及び特定の外部回路接続端子１０２Ｑもまた、相互に電気的に接続されている。以上により、結局、特定の外部回路接続端子１０２Ｑに接続された配線４０４、額縁パターン４０６及び容量配線４００は、常に同電位になる。

【０１３７】

また、額縁パターン４０６の一部は、図７（ｂ）に示すように、コンタクトホール４４Ｈ２によって外部に曝された後、上下導通材１０６を含むシール材５２が充填されることにより、額縁パターン４０６及び対向電極２１間にも電気的接続が実現されるようになっている（なお、額縁パターン４０６上、上下導通材１０６と接触する部分を、接続部分４０６Ｃということとする。）。この接続部分４０６Ｃは、図１を参照して説明したように上下導通材１０６が対向基板２０の四つのコーナー部に配置されていることに応じて、当該四つのコーナー部に設けられることになる。

【０１３８】

以上により、第１実施形態においては、特定の外部回路接続端子１０２Ｑに接続された配線４０４、額縁パターン４０６、容量配線４００及び対向電極２１は、常に同じ電位となることになる。

【０１３９】

なお、コンタクトホール４４Ｈ２の開口時には、額縁パターン４０６の上層の窒化チタンからなる膜を取り除いてもよい。これにより、上下導通材１０６は、該額縁パターン４０６の下層のアルミニウムからなる膜と直接接続されることになるため、接続面で低抵抗化を実現できる。また、窒化チタンからなる膜が存在すると、該窒化チタンからなる膜は硬質の膜であるため、上下導通材１０６が埋め込まれるようにならず、接触面積が小さくなって抵抗値が大きくなるという不具合の生じることが懸念されるが、該窒化チタンからなる膜を取り除けば、そのような不具合を被らなくて済む。

【０１４０】

なお、図７においては、画像表示領域に形成される走査線１１ａと同一膜として、段差調整膜１１ａＰが形成され、また、ゲート電極３ａ及び中継電極７１９と同一膜として、段差調整膜３ａＰが形成されている。これら段差調整膜１１ａＰ及び３ａＰの存在により、画像表示領域と周辺領域とにおける積層構造の全体の高さをほぼ同一とする等の調整を行うことができる。

【０１４１】

（積層構造・第４層及び第５層間の構成-第３層間絶縁膜-）

図６に示すように、データ線６ａの上、かつ、容量配線４００の下には、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等、あるいは好ましくは、ＴＥＯＳガスを用いたプラズマＣＶＤ法で形成された第３層間絶縁膜４３が形成されている。この第３層間絶縁膜４３には、前記の容量配線４００と容量配線用中継層６ａ１とを電気的に接続するためのコンタクトホール８０３、及び、第３中継電極４０２と第２中継電極６ａ２とを電気的に接続するためのコンタクトホール８０４がそれぞれ開孔されている。

【０１４２】

（積層構造・第６層並びに第５層及び第６層間の構成-画素電極等-）

最後に、第６層には、上述したように画素電極９ａがマトリクス状に形成され、該画素電極９ａ上に配向膜１６が形成されている。そして、この画素電極９ａ下には、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等、あるいは好ましくはＮＳＧからなる第４層間絶縁膜４４が形成されている。この第４層間絶縁膜４４には、画素電極９ａ及び前記の第３中継電極４０２間を電気的に接続するためのコンタクトホール８９が開孔されている。画素電極９ａとＴＦＴ３０との間は、この

コンタクトホール８９及び第３中継層４０２並びに前述したコンタクトホール８０４、第２中継層６ａ２、コンタクトホール８８２、中継電極７１９、コンタクトホール８８１、下部電極７１及びコンタクトホール８３を介して、電気的に接続されることとなる。

【０１４３】

また、第１実施形態では、第４層間絶縁膜４４の表面は、ＣＭＰ（Chemical Mechanical Polishing）処理等により平坦化されており、その下方に存在する各種配線や素子等による段差に起因する液晶層５０の配向不良を低減する。ただし、このように第４層間絶縁膜４４に平坦化処理を施すのに代えて、又は加えて、ＴＦＴアレイ基板１０、下地絶縁膜１２、第１層間絶縁膜４１、第２層間絶縁膜４２及び第３層間絶縁膜４３のうち少なくとも一つに溝を掘って、データ線６ａ等の配線やＴＦＴ３０等を埋め込むことにより、平坦化処理を行ってもよい。

【０１４４】

〔当該電気光学装置の作用効果〕

以上のような構成となる第１実施形態の電気光学装置によれば、特に第５層の構成として説明した配線４０４及び額縁パターン４０６からなる引き回し配線が形成されていることから、次のような作用効果が奏されることになる。

【０１４５】

まず第一に、第１実施形態においては、額縁パターン４０６が額縁領域及びシール領域に形成されていることにより、この額縁パターン４０６が形成されている領域においては、図７（ｂ）の矢印Ｌ１に示すように、光漏れが生じることを未然に防止することが可能であるから、画像の周囲に各種の配線等のパターンの像が映り込むなどといったことを防止することが可能となる。したがって、第１実施形態によれば、より品質の高い画像を表示することが可能となる。

【０１４６】

特に、第１実施形態に係る額縁パターン４０６は、画像表示領域１０ａの周囲すべてを囲むように形成されているから、原理上は、額縁領域、或いはシール領域を透過する光を完全に遮断することも可能である。また、額縁パターン４０６は、下層にアルミニウムからなる層、上層に窒化チタンからなる層（いずれも本発明にいう「遮光性材料」の一例に該当する。）という二層構造を有していることから、前記の光遮蔽作用は、より確実に発揮される。さらに、額縁パターン４０６は、図８から明らかなように、画像表示領域１０ａに重ならないように形成されているから、該額縁パターン４０６が、画像表示領域１０ａを透過する光の邪魔になるようなことがない。つまり、画像は所望どおり表示することが可能である。なお、シール材５２が光硬化性樹脂等からなる場合においては、その硬化の際に必要となる光照射は、図７（ｂ）の上方から、即ち対向基板２０側から行うようにすればよい。

【０１４７】

また、これに関連して、第１実施形態においては、対向基板２０上に、額縁遮光膜５３が形成されていることにより、図７（ｂ）の矢印Ｌ２に示すような遮光も実現されることになる。この場合、仮に、額縁遮光膜５３を透過する光があったとしても、その光は、次に控える額縁パターン４０６によって反射又は吸収されることになる。このように、第１実施形態によれば、いわば二重の遮光を実現することができる。

【０１４８】

また第二に、第１実施形態に係る額縁パターン４０６は、上下導通材１０６を介して対向電極２１と電気的接続が図られているとともに、容量配線４００とも電気的接続が図られていることから、該額縁パターン４０６は、前述した光漏れ防止作用の機能に併せて、対向電極２１への電位供給、及び容量配線４００、ひいては容量電極３００への電位供給（この電位供給は、コンタクトホール８０１及び８０３並びに容量配線用中継層６ａ１を介して行われる。図６参照）の機能をももっている。これによって、装置構成の簡略化が実現されることになる。

【０１４９】

これに関連して、上下導通材１０６の配置箇所は、図８及び図１に示すように、画像表示領域１０ａの四隅に対応するようにされているから、額縁パターン４０６及び対向電極２１間の電気的接続を好適に実現しつつも、このことが画像表示の妨げになるようなことがない。加えて、額縁パターン４０６は、画像表示領域１０ａの周囲すべてを囲むように形成されているから、該額縁パターン４０６と対向電極２１との電気的接続をより確実になすことができる。これは、額縁パターン４０６のあらゆる部分が電気的に接続されている（換言すれば、間断なきパターンとして形成されている）こと、また、接続部分４０６Ｃは、画像表示領域１０ａの四隅、即ち額縁パターン４０６の四隅に対応するように複数形成されていることから、たとえ額縁パターン４０６の一部、或いは四つの上下導通材１０６のいずれかが何らかの事情により電気的に導通不能となった場合であっても、他の部分によって電気的導通を滞りなく実現することが可能だからである。

【０１５０】

以上のことにより、第１実施形態によれば、対向電極２１の電位を極めて安定に維持することが可能となり、該対向電極２１及び画素電極９ａ間に挟持される液晶層５０内の液晶分子の配向状態の調整を好適に行うことができるから、より高品質な画像を表示することが可能となる。

【０１５１】

なお、第１実施形態においては、図８に示したように、額縁パターン４０６に接続される外部回路接続端子１０２Ｑは、図中左右に二つ設けられるようになっているが、本発明は、このような形態に限定されない。例えば、図中左及び右のいずれか一方にのみ、額縁パターン４０６に接続される外部回路接続端子１０２Ｑが設けられるような形態を採用してもよい。

【０１５２】

他方、第１実施形態においては、前記のように対向電極２１及び容量配線４００への電位供給機能を有する額縁パターン４０６は、配線４０４の一部、即ち特定の外部回路接続端子１０２Ｑと接続された配線４０４と同一膜として、且つ、電気的に接続されるように形成されていることから、これら各要素が、例えば別々の層に形成され且つコンタクトホール等によって電気的な接続が図られているというような場合に比べて、該各要素間の電気抵抗値を低下せしめることができる。したがって、対向電極２１への安定した電位の供給が実現されるのに加えて、容量配線４００等の高抵抗化を起因とするクロストークの発生等を防止することができる。

【０１５３】

これに関連して、第１実施形態においては、配線４０４及び容量配線４００は、データ線６ａの上に、第３層間絶縁膜４３を介して形成されている。これにより、配線４０４及び容量配線４００を同一膜として形成するということと、外部回路接続端子１０２は外部に曝されなければならないという要請、更には配線４０４及び外部回路接続端子１０２間で電気的連絡を図らなければならないという要請とを比較的容易に達成することが可能となる（図７（ａ）参照）。また、第１実施形態では特に、配線４０４及び容量配線４００は、共に画素電極９ａを含む第６層の直下、即ち該画素電極９ａとの間に第４層間絶縁膜４４のみを介して形成されていることから、前述の作用効果はより効果的に奏されることになる。

【０１５４】

すなわち、このような構成により、外部回路接続端子１０２を構成するためのコンタクトホール４４Ｈ１は、図７（ａ）に示すように第４層間絶縁膜４４についてのみ形成すればよいから、その深度は比較的浅く、該コンタクトホール４４Ｈ１の形成は比較的容易となるのである。

【０１５５】

〔第２実施形態〕

以下では、本発明の第２の実施形態について、図９乃至図１１を参照しながら説明する。ここに図９は、図８と同趣旨の図であって、額縁パターンの形成態様が異なるものであ

る。ただし、図９においては、図８とは異なり、容量配線４００についての図示も省略している。また、図１０及び図１１は、図９に示す符号Ｄ付近を拡大し且つ当該部分における回路構成等を併せて示す説明図である。なお、第２実施形態では、前述した第１実施形態の電気光学装置の全体構成、画素部の構成等の殆どの部分については全く同様である。したがって、以下では、第１実施形態と同様な部分についての説明は省略し、主に、第２実施形態に特徴的な構成についてのみ説明を加えることとする。

【０１５６】

図９においては、額縁パターン４６１Ａ及び４６１Ｂからなる額縁パターン４６１が形成されている。このうち額縁パターン４６１Ａは、本発明にいう「第1のパターン」の一例に該当し、図９に示すように、矩形状を有する画像表示領域１０ａの三辺（図中上辺並びに左辺及び右辺）に沿って連続して形成されている。また、額縁パターン４６１Ｂは、本発明にいう「第２のパターン」の一例に該当し、画像表示領域１０ａの残る一辺（図中下辺）に沿って形成されるとともに前記の額縁パターン４６１Ａと分断して形成されている（図中符号４６１Ｇ参照。）。そして、上下導通材１０６は、これらのうち額縁パターン４６１Ａ上に存在する。

【０１５７】

このような形態によれば、前述の第１実施形態と同様、額縁パターン４６１Ａ及びその上の四つの上下導通材１０６について冗長的な構造がとられていることにより、額縁パターン４６１及び対向電極２１間の電気的接続をより確実になすことができ、対向電極２１の電位を極めて安定に維持することが可能となる。また、額縁パターン４６１Ａ及び４６１Ｂの存在によって、光漏れ防止の作用効果が得られることも、前述の第１実施形態と同様である。

【０１５８】

また、第２実施形態においては特に、額縁パターン４６１Ｂによって次のような作用効果が得られる。すなわち、第２実施形態では、額縁パターン４６１Ｂは、図９において図示が省略されているデータ線駆動回路１０１（図１参照）が形成される領域に対応して形成されている。

【０１５９】

このデータ線駆動回路１０１付近の構成は、図１０に示すようになっている。

すなわち、データ線駆動回路１０１から引き出された制御線１１４は、サンプリング回路１１８を構成するスイッチング素子２０２のゲートに接続されている。

【０１６０】

他方、スイッチング素子２０２のソースには、引き出し配線１１６を介して画像信号線１１５が接続されており、そのドレインにはデータ線６ａが接続されている。これにより、データ線駆動回路１０１によってスイッチング素子２０２のＯＮ・ＯＦＦが制御されることで、画像信号線１１５からデータ線６ａへの画像信号の供給の有無が制御されるようになっている。

【０１６１】

しかしながら、このような構成を備えているデータ線駆動回路１０１付近の構成では、前記の引き出し配線１１６と、対向基板２０上の対向電極２１との間で容量カップリングが発生するおそれがあるのである。この容量カップリングが発生すると、一方に対する通電によって、他方における電位に変動を与えてしまうため、所望どおりの画像の表示が困難となることになる。

【０１６２】

しかるに、第２実施形態によれば、当該領域には、図１０に示すように、前記の額縁パターン４６１Ｂが形成されていることから、画像信号線１１５及び対向電極２１間には該額縁パターン４６１Ｂが存在することになり、前記の容量カップリングの発生を抑制することができるのである。したがって、第２実施形態によれば、所望どおりの画像を好適に表示することができる。ちなみに、このような作用をより効果的に得るためには、額縁パターン４６１Ｂを固定電位に維持しておくことが好ましい。そのためには、例えば該額縁

パターン４６１Ｂを、図９において図示されない容量配線４００（図８参照）に接続しておくようにしておくとよい。

【０１６３】

なお、このような作用効果は、前述した第１実施形態のように、額縁パターン４０６を画像表示領域１０ａの周囲すべてを囲むように形成する態様においても、同様に享受できる。

【０１６４】

また、上記第２実施形態においては、額縁パターン４６１Ｂが、サンプリング回路１１８及び該サンプリング回路１１８から延びる引き出し配線１１６をほぼ全部覆うように形成されているが、本発明は、このような形態に限定されない。

【０１６５】

例えば、図１１に示すように、短冊状に分断された額縁パターン４６１ＢＢを形成するようにしてもよい。ちなみに、このような構成を採用する場合においては、図１０とは異なり、これら短冊状の額縁パターン４６１ＢＢを固定電位に維持する必要はなく、フローティング（浮遊電位）にしておいてよい。

【０１６６】

〔第３実施形態〕

以下では、本発明の第３の実施形態について、図１２を参照しながら説明する。ここに図１２は、図８と同趣旨の図であって、額縁パターンの形成態様が異なるものである。ただし、図１２においては、図８とは異なり、容量配線４００についての図示も省略している。なお、第３実施形態では、前述した第１実施形態の電気光学装置の全体構成、画素部の構成等の殆どの部分については全く同様である。したがって、以下では、第１実施形態と同様な部分についての説明は省略し、主に、第３実施形態に特徴的な構成についてのみ説明を加えることとする。

【０１６７】

図１２においては、額縁パターン４６２Ｃ及び４６２Ｄからなる額縁パターン４６２が形成されている。このうち額縁パターン４６２Ｃは、本発明にいう「第３のパターン」の一例に該当し、図１２に示すように、矩形状を有する画像表示領域１０ａの対応する二辺（図中左辺及び右辺）に沿って形成されている。また、額縁パターン４６２Ｄは、本発明にいう「第４のパターン」の一例に該当し、画像表示領域１０ａの残る二辺（図中上辺及び下辺）に沿って形成されるとともに前記の額縁パターン４６２Ｃと分断して形成されている（図中符号４６２Ｇ参照）。

【０１６８】

そして、上下導通材１０６は、これらのうち額縁パターン４６２Ｃ上に存在する。

【０１６９】

このような形態によれば、図１２中、画像表示領域１０ａの左辺及び右辺に沿って、二本の直線状パターンとして形成された額縁パターン４６２Ｃには、それぞれ、上下導通材１０６が二個ずつ存在している。したがって、この点に関しては、第１実施形態と同様、冗長的な構造がとられているということができるから、額縁パターン４６２及び対向電極２１間の電気的接続をより確実になすことができる。

【０１７０】

また、額縁パターン４６２Ｄによれば、前記第２実施形態の額縁パターン４６１Ｂと同様に、引き出し配線１１６及び対向電極２１間における容量カップリングの発生を極力防止することができる。

【０１７１】

むろん、額縁パターン４６２Ｃ及び４６２Ｄの存在によって、光漏れ防止の作用効果が得られることも、前述の第１実施形態と同様である。

【０１７２】

〔第４実施形態〕

以下では、本発明の第４の実施形態について、図１３を参照しながら説明する。ここに

図１３は、図８と同趣旨の図であって、額縁パターンの形成態様が異なるものである。ただし、図１３においては、図８とは異なり、容量配線４００についての図示も省略している。なお、第４実施形態では、前述した第１実施形態の電気光学装置の全体構成、画素部の構成等の殆どの部分については全く同様である。したがって、以下では、第１実施形態と同様な部分についての説明は省略し、主に、第４実施形態に特徴的な構成についてのみ説明を加えることとする。

【０１７３】

図１３においては、額縁パターン４６３Ｅ及び４６３Ｆからなる額縁パターン４６３が形成されている。このうち額縁パターン４６３Ｅは、本発明にいう「第５のパターン」の一例に該当し、図１３に示すように、矩形状を有する画像表示領域１０ａの一つの角部に対応する部分を除いて連続して形成されている。また、額縁パターン４６３Ｆは、本発明にいう「第６のパターン」の一例に該当し、前記一つの角部に対応する部分に形成されるとともに前記額縁パターン４６３Ｅと分断して形成されている（図中符号４６３Ｇ参照）。そして、上下導通材１０６は、これらのうち額縁パターン４６３Ｅ及び４６３Ｆのいずれの上にも存在する。

【０１７４】

このような形態によれば、前記第１から第３実施形態と略同様な作用効果、すなわち額縁パターン４６３及び対向電極２１間の電気的接続の確実性、或いは引き出し配線１１６及び対向電極２１間の容量カップリングの発生抑止、更には、光漏れ防止等の作用効果が略同様に得られることが明白である。

【０１７５】

〔第５実施形態〕

以下では、本発明の第５の実施形態について、図１４を参照しながら説明する。ここに図１４は、図８と同趣旨の図であって、額縁パターンの形成態様等が異なるものである。なお、第５実施形態では、前述した第１実施形態の電気光学装置の全体構成、画素部の構成等の殆どの部分については全く同様である。したがって、以下では、第１実施形態と同様な部分についての説明は省略し、主に、第５実施形態に特徴的な構成についてのみ説明を加えることとする。

【０１７６】

まず、図１４においては、上記第４実施形態と略同様なパターン形状を有する額縁パターン４６４が形成されている。すなわち、額縁パターン４６４は、画像表示領域１０ａの一つの角部を除いて連続に形成された額縁パターン４６４Ｅ及び前記一つの角部に対応する部分に形成された額縁パターン４６４Ｆからなる。

【０１７７】

また、これらの額縁パターン４６４Ｅ及び４６４Ｆには、それぞれ、三つ及び一つの上下導通材１０６が形成されていること、該上下導通材１０６に電位を供給するための配線４０４が形成されていること、及び該配線４０４の一部は特定の外部回路接続端子１０２Ｑに接続されていることも、上記第４実施形態と同様である。ただし、第５実施形態に係る配線４０４は特に、本発明にいう「第２配線の第１部分」の一例に該当し、特定の外部回路接続端子１０２Ｑは、本発明にいう「外部回路接続端子の第１部分」の一例に該当する。

【０１７８】

そして、第５実施形態において、この額縁パターン４６４Ｅ及び４６４Ｆは、容量配線と電気的に接続されていない。すなわち、額縁パターン４６４と容量配線４００´とは、同一膜として形成されてはいるものの、パターニング上分断されるように形成されているのである（図中符号４６Ｇ参照）。そして、このように額縁パターン４６４から電位の供給を受けることのできない容量配線４００´には、配線４０８が延設されるようになっている。この配線４０８は、本発明にいう「第２配線の第２部分」の一例に該当し、額縁パターン４６４Ｅ及び４６４Ｆを分ける間隙４６４Ｇ間を抜けて、特定の外部回路接続端子１０２Ｒ（本発明にいう「外部回路接続端子の第２部分」の一例に該当する。）に接続さ

れている。

【０１７９】

以上をまとめると、第５実施形態では、配線４０４、額縁パターン４６４、配線４０８及び容量配線４００´は、すべて同一膜として形成されているが（第３中継電極４０２を勿論含む。）、配線４０４と額縁パターン４６４との間、及び、配線４０８と容量配線４００´との間のそれぞれについては電気的接続が図られているものの、前者及び後者間には電気的な連絡がなされていないのである。

【０１８０】

このような形態によれば、対向電極２１と、容量配線４００´ひいては容量電極３００とに与える電位を異ならせることができる。すなわち、対向電極２１は、上下導通材１０６を介して額縁パターン４６４、配線４０４、特定の外部回路接続端子１０２Ｑに接続されているから、該外部回路接続端子１０２Ｑに対向電極２１用の電位を供給すれば、対向電極２１を当該電位に維持することができる。一方、容量配線４００´、ひいてはこれに電気的に接続されている容量電極３００（図６参照）は、配線４０８、特定の外部回路接続端子１０２Ｒに接続されているから、該外部回路接続端子１０２Ｒに、前記対向電極２１用の電位とは異なる容量電極３００用の電位を供給すれば、該容量電極３００を当該電位に維持することができるのである。このように、第５実施形態によれば、対向電極２１及び容量電極３００それぞれを異なる電位に維持することができることから、当該電気光学装置内で発生する各種の電気作用を好適に調整すること等ができる。

【０１８１】

なお、第５実施形態においても、上記第１から第４実施形態と同様に、額縁パターン４６４及び対向電極２１間の確実な電気的接続の確保、或いは画像信号線１１５及び対向電極２１間の容量カップリング発生の抑制、更には光漏れ防止等が可能であることに変わりない。

【０１８２】

なお、上記第２から第４実施形態においては、額縁パターン４６１、４６２及び４６３には、上下導通材１０６及び対向電極２１並びに容量配線４００が電気的に接続されていることから、特定の外部回路接続端子１０２Ｑには、対向電極２１及び容量配線４００或いは容量電極３００に共通の電位を供給する必要がある。ただし、本発明は、このような形態に限定されない。すなわち、第５実施形態として述べたように、上記第２から第４実施形態においても、額縁パターン４６１、４６２及び４６３を構成する間隙４６１Ｇ、４６２Ｇ及び４６３Ｇを利用して、容量配線４００或いは容量電極３００用の電位を、対向電極２１用の電位とは別個に供給するようにしてもよい。

【０１８３】

また、上記第１から第５実施形態においては、特定の外部回路接続端子１０２Ｑ又は１０２Ｒに供給される電位を、走査線駆動回路１０４に供給される低電位側の定電位として利用してもよい。これによると、対向電極２１、容量電極３００の電位は、当該定電位と同じになる。或いはまた、上述のような構成に代えて、外部回路接続端子１０２Ｑ又は１０２Ｒに供給される電位を、データ線駆動回路１０１に供給される定電位として使用しても構わない。

【０１８４】

（電子機器）

次に、以上詳細に説明した電気光学装置をライトバルブとして用いた電子機器の一例たる投射型カラー表示装置の実施形態について、その全体構成、特に光学的な構成について説明する。ここに、図１５は、投射型カラー表示装置の図式的断面図である。

【０１８５】

図１５において、本実施形態における投射型カラー表示装置の一例たる液晶プロジェクタ１１００は、駆動回路がＴＦＴアレイ基板上に搭載された液晶装置を含む液晶モジュールを３個用意し、それぞれＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハ

ライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロックミラー１１０８によって、ＲＧＢの三原色に対応する光成分Ｒ、Ｇ及びＢに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにそれぞれ導かれる。この際特に、Ｂ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂによりそれぞれ変調された三原色に対応する光成分は、ダイクロックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１８６】

本発明は、上述した実施形態に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨、あるいは思想に反しない範囲で適宜変更可能であり、そのような変更を伴う電気光学装置及び電子機器もまた、本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【０１８７】

【図１】ＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た電気光学装置の平面図である。

【図２】図１のＨ－Ｈ’断面図である。

【図３】電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路である。

【図４】データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であって、下層部分（図６における符号７０（蓄積容量）までの下層の部分）に係る構成のみを示すものである。

【図５】データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であって、上層部分（図６における符号７０（蓄積容量）を越えて上層の部分）に係る構成のみを示すものである。

【図６】図４及び図５を重ね合わせた場合のＡ－Ａ´断面図である。

【図７】図６に示す積層構造に対応する断面図であって、（ａ）は図２における符号Ｚを付した円内部分の拡大図、（ｂ）は図２における符号Ｓを付した円内部分の拡大図である。

【図８】図１と同趣旨の図であって、特に額縁パターン及び容量配線等の構成を説明するため両要素の配置関係を明瞭に図示するものである。

【図９】図８と同趣旨の図であって、本発明の第２実施形態の電気光学装置に係る額縁パターンの態様を示すものである。

【図１０】図９に示す符号Ｄ付近を拡大し且つ当該部分における回路構成等を併せて示す説明図である。

【図１１】図１０と同趣旨の図であって、額縁パターンの形成態様が異なるものを示すものである。

【図１２】図８と同趣旨の図であって、本発明の第３実施形態の電気光学装置に係る額縁パターンの態様を示すものである。

【図１３】図８と同趣旨の図であって、本発明の第４実施形態の電気光学装置に係る額縁パターンの態様を示すものである。

【図１４】図８と同趣旨の図であって、本発明の第５実施形態の電気光学装置に係る額縁パターンの態様を示すものである。

【図１５】本発明の各実施形態に係る投射型液晶装置の平面図である。

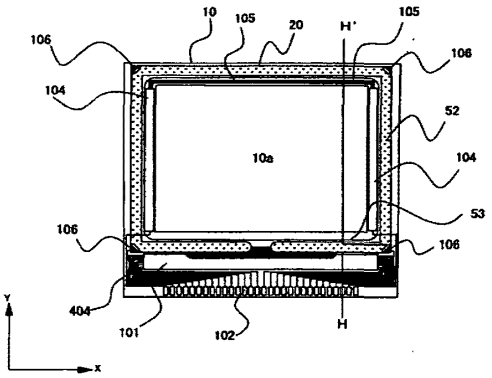
【符号の説明】

【０１８８】

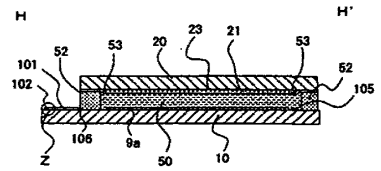
１０・・・ＴＦＴアレイ基板、１０ａ・・・画像表示領域、３ａ・・・走査線、６ａ・・・データ線、３０・・・ＴＦＴ、９ａ・・・画素電極、７０・・・蓄積容量、３００・

・・容量電極、４００・・・容量配線（第１配線）、４０６、４６１、４６２、４６３、４６４・・・額縁パターン、４０４、４０８・・・配線（第２配線）、１０１・・・データ線駆動回路、１０４・・・走査線駆動回路、１０２・・・外部回路接続端子、１０６・・・上下導通材、２０・・・対向基板、２１・・・対向電極、５３・・・額縁遮光膜。

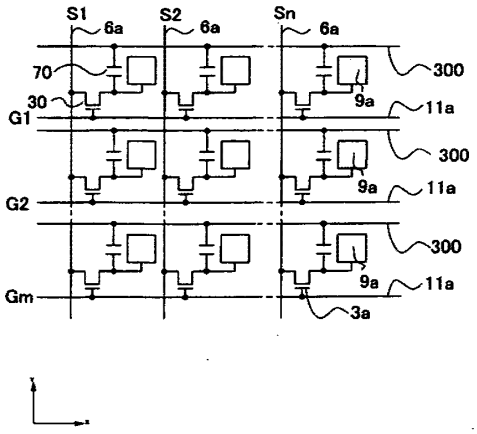
【図１】



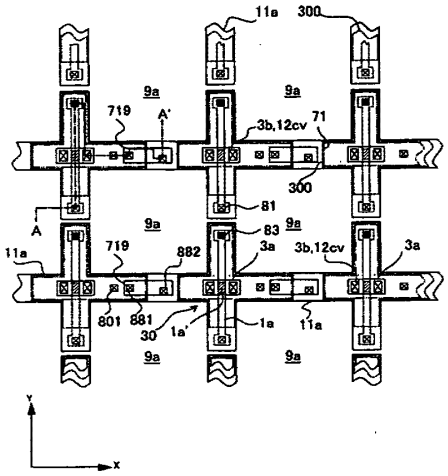
【図２】



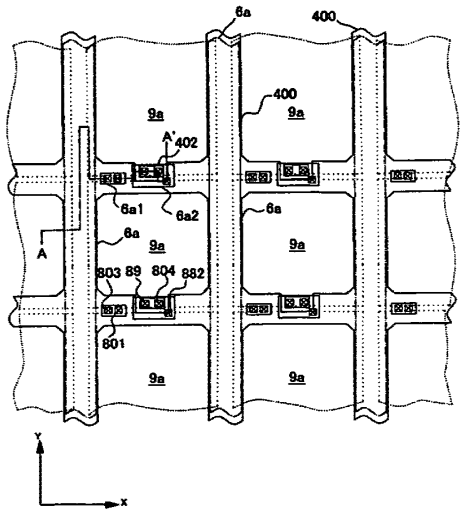
【図３】



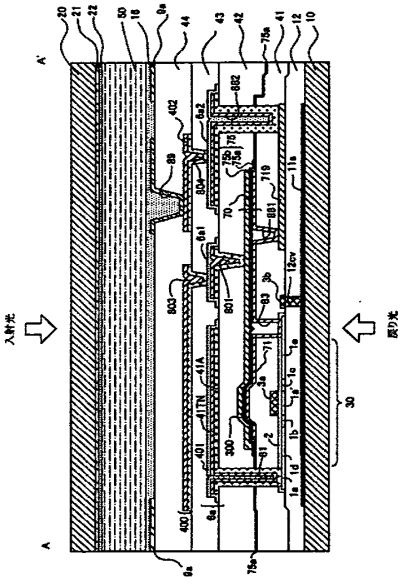
【図４】


11a
300
9a
719
A'
3b,12cv
71
300
81
A
83
3a
882
801
881
30
1a'
1a

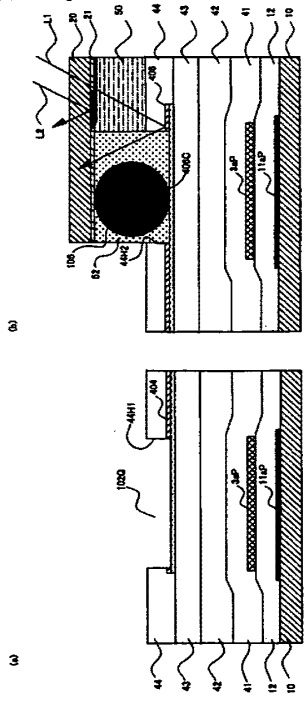
【図５】


6a
400
9a
A'
402
6a1
6a2
A
803
89
804
882
801

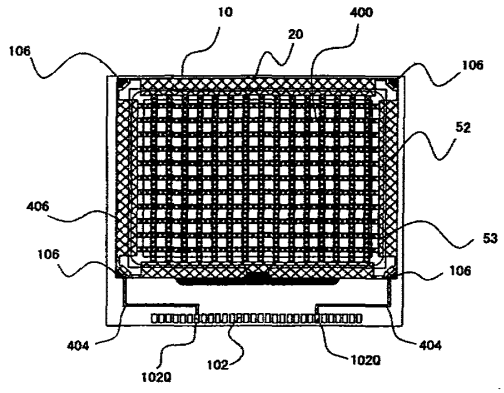
【図６】


入射光
射出光
30

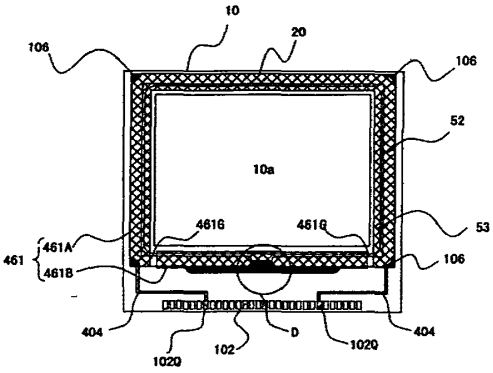
【図７】



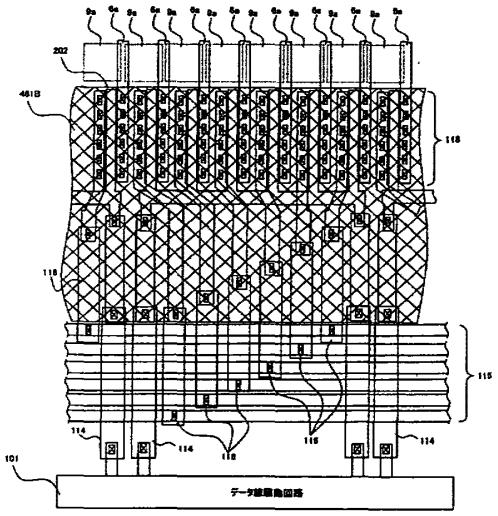
【図８】


10
400
20
106
106
52
406
53
106
106
404
404
1020
102
1020

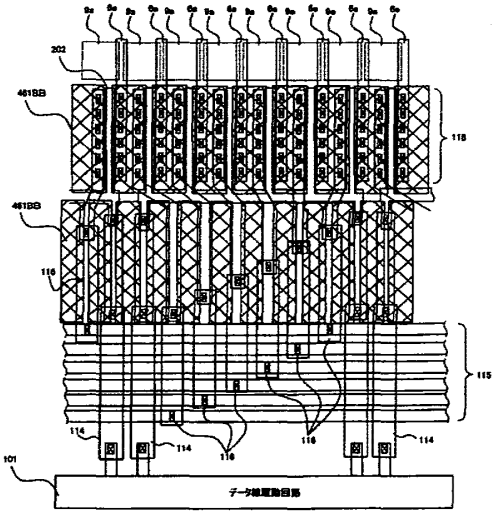
【図９】


10
106
20
106
52
10a
4616
4618
53
461
461A
461B
106
404
404
1020
102
D
1020

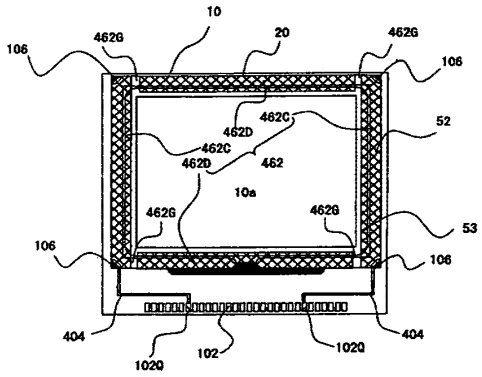
【図１０】


202
461B
118
118
115
114
114
116
116
101

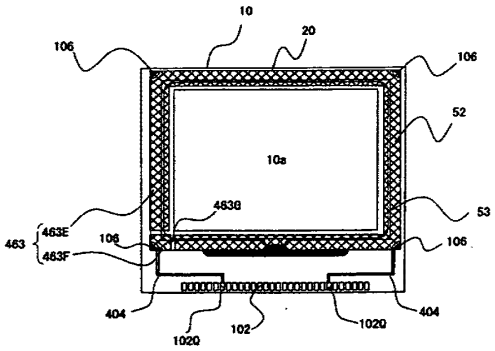
【図１１】


202
461BB
118
461BB
118
115
114
114
116
116
101

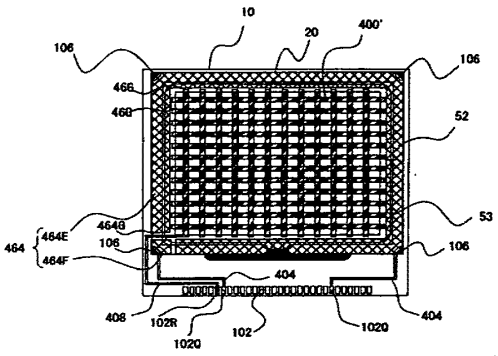
【図１２】



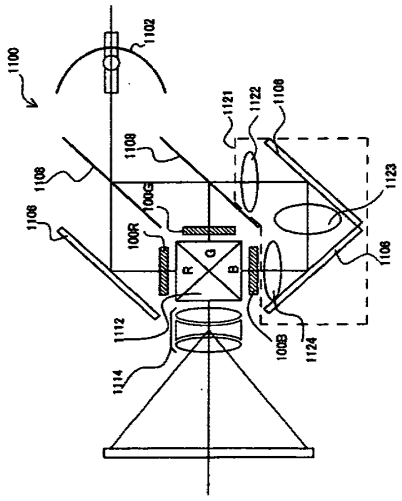
【図１３】



【図１４】



【図１５】



フロントページの続き

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	H05B 33/06		
	H05B 33/14	A	

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5C094 AA03 AA16 AA21 AA23 BA43 CA19 DA20 ED14

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CLAIMS

[Claim(s)]
[Claim 1]
On a substrate,
The scanning line prolonged in the direction which intersects the data line and this data line which are prolonged in the fixed direction,
The switching element to which a scan signal is supplied by said scanning line,
It comes to have the pixel electrode to which a picture signal is supplied through said switching element by said data line,
Said substrate has the image display field specified as said pixel electrode and a formation field of said switching element, and the boundary region which specifies the circumference of this image display field,
On said image display field,
Storage capacitance which carries out predetermined period maintenance of the potential in said pixel electrode,
The capacity electrode which constitutes this storage capacitance is equipped with the 1st wiring which supplies predetermined potential,
The electro-optic device characterized by having the frame pattern which constitutes a part of frame field [at least] which is formed as the same film as said 1st wiring, and demarcates said image display field and said boundary region.
[Claim 2]
Said frame pattern is an electro-optic device according to claim 1 characterized by being formed so that the sampling circuit for supplying a picture signal to the data line may be covered at least.
[Claim 3]
Said 1st wiring is an electro-optic device according to claim 1 characterized by having extended said capacity electrode and being formed as the same film as the near capacity electrode with which said predetermined potential is supplied.
[Claim 4]
Said some of frame patterns [at least] are the electro-optic devices according to claim 1 characterized by being divided in the shape of a strip of paper, being formed, and considering as floating potential.
[Claim 5]
It comes further to have the sealant which pastes up the opposite substrate by which opposite arrangement is carried out, and said substrate and said opposite substrate on said substrate,
Said frame pattern is an electro-optic device according to claim 1 characterized by being formed in a part of seal field [at least] in which said sealant is formed.
[Claim 6]
It comes further to prepare for said substrate the opposite substrate by which opposite arrangement is carried out, and the counterelectrode formed on this opposite substrate,
Said frame pattern is an electro-optic device according to claim 1 characterized by having a part for the

connection connected to said counterelectrode and electric target.
[Claim 7]
Said frame pattern is an electro-optic device according to claim 1 characterized by being formed so that it may connect with said 1st wiring and electric target.
[Claim 8]
A part for said connection is an electro-optic device according to claim 6 or 7 characterized by being prepared corresponding to the corner section of said opposite substrate.
[Claim 9]
Said frame pattern is an electro-optic device according to claim 1 characterized by being formed so that all the perimeters of said image display field may be surrounded.
[Claim 10]
Plane view of said image display field is carried out, and it has the shape of a rectangle,
Said frame pattern contains the 1st pattern continuously formed along with three sides of the shape of said rectangle, and the 2nd pattern which divided with said 1st pattern and was formed while being formed along with one side which remains,
A part for said connection is an electro-optic device given in claim 6 characterized by existing on said 1st pattern thru/or any 1 term of 8.
[Claim 11]
Plane view of said image display field is carried out, and it has the shape of a rectangle,
Said frame pattern contains the 3rd pattern formed along with two sides which the shape of said rectangle counters, and the 4th pattern which divided with said 3rd pattern and was formed while being formed along with two sides which remain,
A part for said connection is an electro-optic device given in claim 6 characterized by existing on said 3rd pattern thru/or any 1 term of 8.
[Claim 12]
Plane view of said image display field is carried out, and it has the shape of a rectangle,
Said frame pattern contains the 5th pattern continuously formed except for the part corresponding to one corner of the shape of said rectangle, and the 6th pattern which divided with said 5th pattern and was formed while being formed in the part corresponding to said one corner,
A part for said connection is an electro-optic device given in claim 6 characterized by existing on [one / at least] said 5th pattern and said 6th pattern thru/or any 1 term of 8.
[Claim 13]
On said boundary region,
It has further the external circuit connection terminal formed along the side edge of said substrate, and the 2nd wiring installed by this external circuit connection terminal,
This a part of 2nd wiring [at least] is an electro-optic device given in claim 1 characterized by connecting and being formed in this 1st wiring and an electric target as the same film as said 1st wiring thru/or any 1 term of 12.
[Claim 14]
Said 1st wiring is an electro-optic device according to claim 13 characterized by being formed through an interlayer insulation film on said data line.
[Claim 15]
Said 1st wiring is an electro-optic device according to claim 13 or 14 characterized by being formed in the layer [directly under] of the layer containing said pixel electrode.
[Claim 16]
it connects electrically and said 1st wiring and said frame pattern are formed -- not having -- and
A part for part I and said 1st wiring of said 2nd wiring are connected electrically,
A part for part II and said frame pattern of said 2nd wiring are connected electrically,
A part for said part I is a part for part I of said external circuit connection terminal,
A part for said part II is an electro-optic device given in claim 13 characterized by connecting with a part for part II of said external circuit connection terminal, respectively thru/or any 1 term of 15.

[Claim 17]
Said 1st wiring is an electro-optic device given in claim 1 characterized by consisting of protection-from-light nature ingredients thru/or any 1 term of 16.
[Claim 18]
Said 1st wiring is an electro-optic device given in claim 1 characterized by having the laminated structure which consists of an ingredient which is different from each other thru/or any 1 term of 17.
[Claim 19]
It comes further to prepare for said substrate the light-shielding film formed on the opposite substrate by which opposite arrangement is carried out, and this opposite substrate,
Said frame pattern is an electro-optic device given in claim 1 characterized by being formed so that it may lap with said light-shielding film thru/or any 1 term of 18.
[Claim 20]
Said light-shielding film is an electro-optic device according to claim 19 characterized by including the frame light-shielding film formed so that the side edge of said opposite substrate might be met.
[Claim 21]
Electronic equipment characterized by coming to provide the electro-optic device of a publication in claim 1 thru/or any 1 term of 20.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
This invention belongs to the technical field of electro-optic devices, such as electrophoresis apparatus, such as liquid crystal equipment of active-matrix actuation for example, and an electronic paper, and EL (Electro-Luminescence) display. Moreover, this invention belongs also to the technical field of electronic equipment which comes to provide such an electro-optic device.
[Background of the Invention]
[0002]
The electro-optic device in which the so-called active-matrix actuation is possible is known for having conventionally the data line, the scanning line, etc. which were connected to the thin film transistor (it is suitably called "TFT" below Thin Film Transistor;.) connected to each of the pixel electrode arranged in the shape of a matrix, and this electrode, and this each of TFT, and were formed in a line and each direction of a train on the substrate at parallel.
[0003]
With such an electro-optic device, while equipping said substrate with the opposite substrate by which opposite arrangement is carried out in addition to the above, image display becomes possible by having the counterelectrode which counters a pixel electrode on this opposite substrate, and having further the liquid crystal layer pinched between a pixel electrode and a counterelectrode. That is, the display of an image is attained when the permeability of the light in which the orientation condition is suitably changed into and penetrates the liquid crystal layer concerned by this according to the predetermined potential difference by which the liquid crystal molecule in a liquid crystal layer was set up between the pixel electrode and the counterelectrode changes.
[0004]
Moreover, said substrate in the above-mentioned electro-optic device has the image display field in which the scanning line, the data line, a pixel electrode, etc. are prepared, and the boundary region in which the external circuit connection terminal for supplying a Sadanobu Tokoro number to a scanning-line actuation circuit, a data-line actuation circuit, and these circuits etc. is prepared. As an example of 1 type of such an electro-optic device, what is indicated by the patent reference 1, for example can be mentioned.
[0005]
[Patent reference 1] JP,11-223832,A
[Description of the Invention]
[Problem(s) to be Solved by the Invention]
[0006]
However, there are the following troubles in the electro-optic device in the former. That is, in the aforementioned boundary region, the sealant for pasting up a substrate and an opposite substrate is usually prepared. Since handling being easy and comparatively powerful adhesive strength are obtained

as this sealant, the photo-setting resin is used preferably. In this case, in order to harden a sealant, it is necessary to irradiate light to the sealant concerned which is inserted between a substrate and an opposite substrate and exists. On the other hand, various kinds of wiring, such as wiring for connecting the scanning line and the data line which were mentioned above, a scanning-line actuation circuit, and a data-line actuation circuit, and a sampling circuit for supplying a picture signal to the data line suitably, a picture signal line which supplies this picture signal itself, needs to be formed in an image display field and a boundary region. According to these, in the predetermined field on a boundary region, they need to be collectively formed by said sealant, said various kinds of wiring, etc., but in the field concerned, securing a path by preparing a predetermined clearance for sealant hardening etc. as light is performed.

[0007]

However, according to this, when using the electro-optic device after completion practically, the problem that light will leak through the aforementioned predetermined clearance prepared as a path as light will arise. That is, when using the electro-optic device concerned as a light valve of projection mold indicating equipments, such as a liquid crystal projector, while projecting light to this light valve, it is carrying out amplification projection of the light which passed through this light valve on a screen, and image display will be performed, but if said predetermined clearance etc. exists, the light which leaked and appeared from this clearance in the light through which the light valve passed will mix. In such a case, around the image on a screen, the situations, like the image of patterns, such as said various kinds of wiring, is reflected will arise, and it will result in looking down upon the quality of an image in it.

[0008]

Moreover, in the conventional electro-optic device, in order to raise the potential maintenance property in a pixel electrode, storage capacitance may be formed in an image display field. While constitutes this storage capacitance, and since maintaining to fixed potential is desirable as for an electrode (it may be hereafter called a "capacity electrode"), connecting with the external circuit connection terminal formed in a boundary region is performed. However, since a possibility that high resistance-ization resulting from this contact hole may be brought about being large, and the situation where properties differed for every contact hole might arise when the mode which connects between both through a contact hole in this case was adopted, the time constant of a capacity electrode or wiring prolonged from now on might become large, and the nonconformity of generating a cross talk on a result and an image etc. might arise. In addition, when the aforementioned wiring is formed so that an image display field may be crossed, it will be observed as the so-called horizontal cross talk.

[0009]

This invention makes it a technical problem to offer the possible electro-optic device of displaying a quality image by being made in view of the above-mentioned trouble, and preventing that the image which originates in optical leakage around an image appears as much as possible, or supplying predetermined potential to a capacity electrode suitably. Moreover, this invention also makes it a technical problem to offer the electronic equipment possessing such an electro-optic device.

[Means for Solving the Problem]

[0010]

The scanning line prolonged in the direction which intersects the data line and this data line which are prolonged in the fixed direction on a substrate in order that the electro-optic device of this invention may solve the above-mentioned technical problem, It comes to have the switching element to which a scan signal is supplied by said scanning line, and the pixel electrode to which a picture signal is supplied through said switching element by said data line. Said substrate The image display field specified as said pixel electrode and a formation field of said switching element, The storage capacitance which has the boundary region which specifies the circumference of this image display field, and carries out predetermined period maintenance of the potential in said pixel electrode on said image display field, The capacity electrode which constitutes this storage capacitance was equipped with the 1st wiring which supplies predetermined potential, and it was formed as the same film as said 1st wiring, and has the frame pattern which constitutes a part of frame field [at least] which demarcates said image display

field and said boundary region.
[0011]
According to the electro-optic device of this invention, the ON-OFF is controlled by a scan signal being supplied through the scanning line to an example slack thin film transistor of a switching element. On the other hand, to a pixel electrode, it is that a picture signal is supplied through the data line, and impression and un-impressing are performed to a pixel electrode according to ON-OFF of said thin film transistor. [of the picture signal concerned] Thereby, the so-called active-matrix actuation of the electro-optic device concerning this invention is enabled. Moreover, in this invention, the potential maintenance property of this pixel electrode is improving by forming the storage capacitance the potential in a pixel electrode carries out [storage capacitance] predetermined period maintenance.
[0012]
And especially in this invention, said substrate has an image display field and a boundary region, and the aforementioned pixel electrode, a switching element, storage capacitance, and the 1st wiring are formed in the former of these. Furthermore, in this invention, it has the frame pattern formed in a part of frame field [at least] which demarcates between a boundary region or an image display field, and a boundary region as the same film as said 1st wiring. A frame field is specified here as a field bordered as it is also at predetermined width of face about the perimeter of the shape of this rectangle, when for example, an image display field is a rectangle-like. Therefore, plane view of the frame field which can be set in this case will be carried out, and it will have a hollow square shape. Moreover, a boundary region will be seen from the core of an image display field, and it will be specified as a beyond field from the rim of the frame field used as this hollow square shape. Moreover, it means that membranes are formed in the production process of the electro-optic device concerned by the opportunity for a frame pattern and the precursive film of the 1st wiring to be the same as "forming as the same film" is carried out, and predetermined patterning processings (for example, a photolithography, an etching process, etc.) are simultaneously carried out to this precursive film.
[0013]
And said frame pattern is formed in a part of above frame fields [at least]. By this, as for the light which is going to penetrate a frame field, the progress will be interrupted with a frame pattern. Therefore, it becomes possible to prevent beforehand and has that optical leakage which was explained with the part corresponding to the field in which the frame pattern is formed, and the background technique arises according to this invention, and since it becomes possible to prevent that the image of patterns, such as various kinds of wiring, is reflected in the perimeter of an image etc., it becomes possible to display an image with more high quality.
[0014]
In addition, in this invention, a frame pattern may be formed as it connects with the 1st wiring and the electric target which are formed in an image display field, or between both, it may be formed so that it may be divided on patterning.
[0015]
Moreover, in this invention, it is good for this 1st wiring to adopt a configuration which is connected or installed by the capacity electrode, for example as a configuration for playing the role by which the 1st wiring supplies predetermined potential to a capacity electrode. The case where it is said by minding a contact hole among both when being formed here at the separate layer among the laminated structure by which for example, a capacity electrode and the 1st wiring are built on a substrate as "connecting with a capacity electrode" is carried out that these are connected electrically etc. is included. on the other hand, the 1st wiring -- "-- a capacity electrode ... installation" -- the case where it is said that the pattern (that is, the both sides of the part which can be called the part which can be called the 1st wiring in the flat surface where this pattern is formed, and a capacity electrode will be included in this pattern.) which has the configuration which follows for example, this capacity electrode and a flat-surface target as being carried out is formed in the same layer etc. is included.
[0016]
Furthermore, the "frame pattern" said to this invention remains by way of precaution for saying that the

name is given although formed on the frame field therefore, and this frame pattern does not necessarily mean having a configuration like a frame (it includes such the meaning that the frame pattern is formed in "a part of frame field [at least]".). Moreover, across a frame field, such a frame pattern may be formed so that it may result on a boundary region.

[0017]

In other modes of the electro-optic device of this invention, it comes further to have the sealant which pastes up the opposite substrate by which opposite arrangement is carried out, and said substrate and said opposite substrate on said substrate, and said frame pattern is formed in a part of seal field [at least] in which said sealant is formed.

[0018]

According to this mode, it has pasted up by the sealant which a substrate and an opposite substrate become from a photo-setting resin etc. In this case, if a frame field shall have the above hollow square shapes, it can be assumed that the seal field in which a sealant is formed is located in the rim beyond of this frame field, without including or including this all or some of hollow square-shaped frame field, and has a larger hollow square shape a little than this hollow square shape (therefore, a part of this seal field [at least] is a field included in said boundary region.).

[0019]

According to this mode, the progress will be interrupted also for the light which is going to penetrate a seal field with a frame pattern by forming said frame pattern also in frame field beyond in this way. Therefore, according to this invention, since it becomes possible about the image of patterns, such as various kinds of wiring, being reflected in the perimeter of an image etc. to prevent more effectively, it becomes possible to display an image with more high quality.

[0020]

In other modes of the electro-optic device of this invention, it comes further to prepare for said substrate the opposite substrate by which opposite arrangement is carried out, and the counterelectrode formed on this opposite substrate, and said frame pattern has a part for the connection connected to said counterelectrode and electric target.

[0021]

According to this mode, a frame pattern has a part for the connection connected to the counterelectrode and the electric target, namely, a counterelectrode and a frame pattern will be in the condition of having connected electrically, and both will always be in same electric potential. According to this, a frame pattern will achieve simultaneously the function of the optical leakage prevention mentioned above, and two functions of the potential supply function to a counterelectrode, and can attain simplification of the part and an equipment configuration.

[0022]

In other modes of the electro-optic device of this invention, said frame pattern is formed so that it may connect with said 1st wiring and electric target.

[0023]

According to this mode, same electric potential will always have a frame pattern and the 1st wiring. According to this, a frame pattern will achieve simultaneously the function of the optical leakage prevention mentioned above, and two functions of the potential supply function to the 1st wiring, and can attain simplification of the part and an equipment configuration. incidentally, both as carrying out "forming so that it may connect electrically", since a frame pattern and the 1st wiring are formed as the same film as mentioned above When carrying out patterning processing, without dividing both typically in a frame light-shielding film and the precursive film common to the 1st wiring (that is, the both sides of the part which can be called frame pattern, and the part which can be called 1st wiring exist on the pattern which continues superficially in this case.) It will be assumed.

[0024]

Moreover, if it has the mode by which electrical installation between the frame pattern which combined with this mode and was mentioned above, and a counterelectrode was planned, three persons of a frame pattern, a counterelectrode, and the 1st wiring will always be in same electric potential. According to

this, it cannot be overemphasized that simplification of an equipment configuration will be attained more suitably.

[0025]

A part for said connection may consist of modes equipped with a part for a connection as prepared corresponding to the corner section of said opposite substrate.

[0026]

According to such a configuration, when an image display field is a rectangle-like, it becomes possible to arrange a part for a connection etc., for example so that it may correspond to the four corners of this image display field, or so that it may correspond to the four corners of the frame field which borders this image display field, or the seal field of it beyond. In this case, the operation effectiveness of not barring image display is acquired, planning suitably electrical installation between a frame pattern and a counterelectrode.

[0027]

In addition, it is a concept also containing the part which, of course, has superficial fixed breadth (for example, concentric circle-breadth centering on the part of the corner concerned) from each [these] corner that the "corner section" said to this mode contains the part of the four corners of the opposite substrate itself. Moreover, a part for a connection contains in "being prepared corresponding to the corner section", also when saying that it is prepared so that it may correspond to below Misumi of an image display field besides in the case of being prepared in all four corners that the amount of this connection described above etc.

[0028]

In other modes of the electro-optic device of this invention, said frame pattern is formed so that all the perimeters of said image display field may be surrounded.

[0029]

Since according to this mode the frame pattern is formed so that all the perimeters of said image display field may be surrounded, a principle top can also intercept thoroughly the light which penetrates a frame field or a seal field. Therefore, it becomes possible to demonstrate an operation of the above mentioned optical leakage more effectively, to have it, and to display a more nearly quality image.

[0030]

Moreover, in this mode, if it is when the amount of [with a counterelectrode / "the amount of"] connection exists in the frame pattern formed so that all the perimeters of said image display field might be surrounded said bottom, the electrical installation of this frame pattern and counterelectrode can be made more certainly. That is, a part for the thing for which, as for the frame pattern, all the parts are connected electrically (formed as a pattern without an intermission if it puts in another way), and said connection From two or more formation being possible like an above-mentioned example, so that it may correspond to the four corners of the four corners of an image display field, i.e., a frame pattern, and a seal field Even if it is the case where it becomes impossible electrically flowing either for some frame patterns or a connection according to a certain situation even if It is because it is possible to realize an electric flow duly by other parts (in other words, it can be said that redundancy-[part / for the connection on a frame pattern or this frame pattern] structure is taken.). . Thereby, it becomes possible to maintain the potential of a counterelectrode to stability extremely in such a mode, and since the orientation condition of an example slack liquid crystal molecule of the electrooptic material pinched by this counterelectrode and pixel inter-electrode can be adjusted suitably, it becomes possible to display a more nearly quality image.

[0031]

on the other hand, in the mode which has a part for the connection by which the frame pattern mentioned above is connected to the counterelectrode and the electric target Plane view of said image display field is carried out, and it has the shape of a rectangle. Said frame pattern You may make it the amount of said connection exist on said 1st pattern including the 1st pattern continuously formed along with three sides of the shape of said rectangle, and the 2nd pattern which divided with said 1st pattern and was formed while being formed along with one side which remains.

[0032]
According to such a configuration, the 1st pattern with which the frame pattern was first formed continuously along with three sides of an image display field which have the shape of a rectangle is included. and a part for said connection like [since it exists on this 1st pattern] the mode in which the frame pattern is formed so that all the perimeters of the above-mentioned image display field may be surrounded The electrical installation between a frame pattern and a counterelectrode can be made more certainly, and it becomes possible to maintain the potential of a counterelectrode to stability extremely.
[0033]
Moreover, in this mode, since the 2nd pattern which divided with said 1st pattern and was formed is included while being formed along with one side in which the shape of said rectangle remains in addition to this 1st pattern, the following operation effectiveness is acquired. That is, when the field in which this 2nd pattern is formed is equivalent to the field in which for example, a data-line actuation circuit is formed, there is a possibility that capacity coupling may occur between the picture signal line taken about in the sampling circuit controlled by the data-line actuation circuit concerned and the counterelectrode on an opposite substrate. If this capacity coupling occurs, in order to give fluctuation to the potential in another side by energization to one side, the display of the image as a request will be difficult. However, according to this mode, since the 2nd aforementioned pattern is formed in the field concerned, this 2nd pattern will exist between a picture signal line and a counterelectrode, and generating of the aforementioned capacity coupling can be controlled. Therefore, according to this mode, the image as a request can be displayed suitably.
[0034]
In addition, it cannot be overemphasized that the frame pattern which mentioned such operation effectiveness above is completely similarly enjoyable in the mode formed so that all the perimeters of an image display field may be surrounded.
[0035]
moreover, the "1st pattern" said to this mode and the "2nd pattern", and the voice mentioned further later below -- vocabulary called the "3rd pattern" thru/or the "6th pattern" said like Each only expresses that it is a pattern on the semi-conductor process specified with the concept according to individual (if it puts in another way, "A" thru/or "F" will be mere "only identifiers".). .
[0036]
Or plane view of said image display field is carried out, it has the shape of a rectangle, and you may make it the amount of said connection exist on said 3rd pattern including the 3rd pattern with which said frame pattern was formed along with two sides which the shape of said rectangle counters, and the 4th pattern which divided with said 3rd pattern and was formed while being formed along with two sides which remain.
[0037]
According to such a configuration, the amount of said connection exists on this 3rd pattern, including the 3rd pattern with which the frame pattern was first formed along with two sides which the image display field which has the shape of a rectangle counters. Generally it is assumed that wiring of the shape of two straight lines which divides this 3rd pattern on the aforementioned definition, and is formed is included. According to this mode, the amount of [at least two] said connection may exist in each wiring of the shape of two straight lines concerned. Therefore, the electrical installation between a counterelectrode and a frame pattern can be made more certainly.
[0038]
Moreover, in this mode, while being formed along with two sides in which the shape of said rectangle remains in addition to this 3rd pattern, the 4th pattern which divided with said 3rd pattern and was formed is included. Thereby, like the 2nd aforementioned pattern, when the field in which the 4th pattern is formed is equivalent to the field in which for example, a data-line actuation circuit is formed, it can prevent generating of capacity coupling between a picture signal line and a counterelectrode.
[0039]
Plane view of said image display field is carried out, and it has the shape of a rectangle. Furthermore,

said frame pattern The 5th pattern continuously formed except for the part corresponding to one corner of the shape of said rectangle, While being formed in the part corresponding to said one corner, you may make it the amount of said connection exist including the 6th pattern which divided with said 5th pattern and was formed on [one / at least] said 5th pattern and said 6th pattern.
[0040]
the 5th pattern with which the frame pattern was first formed continuously except for the part corresponding to one corner of an image display field which has the shape of a rectangle according to such a configuration -- containing -- and -- this -- the amount of said connection may exist on the 5th pattern. Therefore, typically, it is [the amount of connection] possible to exist on [three] this 5th pattern.
[0041]
moreover, this mode -- setting -- this 5th pattern -- in addition, the 6th pattern which divided with said 5th pattern and was formed while being formed in the part corresponding to said one corner -- containing -- and -- this -- the amount of said connection may exist on the 6th pattern. Therefore, typically, the amount of connection is possible [it] on this 6th pattern to recognize piece existence.
[0042]
According to this mode, the operation effectiveness, such as generating suppression of capacity coupling between the soundness of the electrical installation between the frame pattern mentioned above and a counterelectrode or a picture signal line, and a counterelectrode, is acquired like abbreviation by the above.
[0043]
In addition, it cannot be overemphasized that various kinds of modes about the mode of the frame pattern concerning this mode or the frame pattern mentioned above have the meaning to which the variation of the formation mode of a frame pattern is made to increase. Thereby, it becomes possible from an external circuit connection terminal to arrange more easily various wiring taken about to a part for a data-line actuation circuit, a scanning-line actuation circuit, or said connection (or patterning) etc.
[0044]
In other modes of the electro-optic device of this invention, it has further the external circuit connection terminal formed along the side edge of said substrate on said boundary region, and the 2nd wiring installed by this external circuit connection terminal, and this a part of 2nd wiring [at least] is connected and formed in this 1st wiring and an electric target as the same film as said 1st wiring.
[0045]
According to this mode, an external circuit connection terminal and the 2nd wiring are formed in the boundary region, and a part of 2nd wiring [at least] of these is connected and formed in this 1st wiring and an electric target as the same film as the 1st wiring. It has meaning as a frame pattern and the 1st wiring were already described ["it is formed as the same film", and] here. According to this, the 1st wiring will be formed in the same layer by the 2nd wiring reaching in part at least among the laminated structure which the data line, the scanning line, a pixel electrode, etc. constitute, and both will consist of same ingredients. according to a book mode since the 1st wiring and a frame pattern are incidentally formed as the same film in this invention -- after all -- both the 1st wiring a frame pattern and the 2nd wiring -- although -- it will be said that it is formed as the same film.
[0046]
Since it becomes possible to form an external circuit connection terminal, the 2nd wiring, and the 1st wiring in the same layer, the electric resistance value between each [these] element can be made to fall in the first place according to this.
[0047]
Incidentally, in the former, it is performed that each above element is formed in a separate layer, and, thereby, the contact hole etc. might be used for the electrical installation between this each element. However, since a possibility that high resistance-ization resulting from this contact hole may be brought about being large, and the situation where properties differed for every contact hole might arise after using the contact hole, the time constant of a capacity electrode or wiring prolonged from now on might

become large, and the nonconformity of generating a cross talk on a result and an image etc. might arise. In addition, when the aforementioned wiring is formed so that an image display field may be crossed, it will be observed as the so-called horizontal cross talk.

[0048]

However, in this mode, since it is possible to form an external circuit connection terminal, the 2nd wiring, and the 1st wiring in the same layer as already stated, it is not necessary to wear the above nonconformities.

[0049]

Moreover, the mode which has a part for a connection to the above mentioned frame pattern with this mode the second, Or the mode in which a frame pattern is formed so that all the perimeters of an image display field may be surrounded, Furthermore, the electro-optic device having the mode equipped with the frame pattern containing the 1st pattern, 2nd pattern, 3rd pattern, 4th pattern, 5th aforementioned pattern, and 6th aforementioned pattern (the mode of the electro-optic device concerned is hereafter called "concomitant use mode".) It will be related and the following characteristic operation effectiveness will be especially done so. That is, in the electro-optic device concerning this concomitant use mode, to the frame pattern, since the amount of [between this and a counterelectrode] connection exists, this frame pattern is combined with the operation effectiveness of the aforementioned optical leakage prevention etc., and it also has the function as wiring which supplies predetermined potential to a counterelectrode. Here, in this concomitant use mode, it is possible for the electric resistance value between each [these] element and an external circuit connection terminal to make them fall with this frame pattern, since the 2nd wiring and the 1st wiring are also formed as the same film.

[0050]

It becomes possible to maintain in the condition that the potential of this frame pattern became possible [maintaining the condition of having been stabilized], and had and the potential of a counterelectrode was also stabilized since an electric resistance value until it results [from an external circuit connection terminal] in the 2nd wiring and a frame pattern in said concomitant use mode, since it is such would be held down low. Furthermore, since the 1st wiring may be electrically connected to a frame pattern, the potential of this 1st wiring, as a result the potential of the capacity electrode connected or installed in this also become possible [maintaining in the condition of having been stabilized].

[0051]

Thus, according to the concomitant use mode, a frame pattern, the 2nd wiring, and the 1st wiring are formed in the same film and the condition of having connected electrically. And since the amount of said connection exists in this frame pattern, it becomes possible about the both sides of the operation effectiveness (reduction in resistance) concerning this mode, and the operation effectiveness (potential supply function to a counterelectrode) by having a part for a connection to enjoy this more effectively.

[0052]

In this mode, said 1st wiring may be made to be formed on said data line through the 1st interlayer insulation film.

[0053]

According to such a configuration, it becomes possible to constitute suitably the laminated structure which consists of the scanning line built on a substrate, the data line, a pixel electrode, an external circuit connection terminal, etc.

[0054]

That is, as for an external circuit connection terminal, it is desirable first to be comparatively formed in the upper layer among the aforementioned laminated structure from it having to have the electrode put outside.

Otherwise, it is because a comparatively deep contact hole which passes to said electrode from a part for the management of the maximum of a laminated structure must be punctured. On the other hand, according to this mode, it will be formed as the film as this 1st wiring with it, and the 2nd wiring connected or installed by the external circuit connection terminal will also be formed on the data line. [same since the 1st wiring is formed on the data line] Therefore, the 2nd wiring will be comparatively

formed in the upper layer among the aforementioned laminated structure.
[0055]
By the above, in this mode, though an external circuit connection terminal is comparatively formed in the upper layer, the 2nd wiring connected or installed in this also becomes possible [realizing electrical installation between both reasonable] by being comparatively formed in the upper layer. Thus, according to this mode, it becomes possible to form the aforementioned laminated structure suitably.
[0056]
Or said 1st wiring may be made to be formed in the layer [directly under] of the layer containing said pixel electrode.
[0057]
According to such a configuration, it is possible to realize electrical installation between an external circuit connection terminal and the 2nd wiring still more reasonable. That is, the case where being formed in the layer [directly under] of the layer in which the 1st wiring contains a pixel electrode says that this 1st wiring is formed only by inserting much more insulator layer between pixel electrodes, in view of the layer of electrooptic material will be assumed typically, considering a pixel electrode countering electrooptic material. And since the 2nd wiring formed as the same film as the 1st wiring in this case will also be formed in the layer [directly under] of the layer containing a pixel electrode, it will only be said that it is usually that said insulator layer exists after this 2nd wiring. This is because it is usual that the front face of the insulator layer formed directly under a pixel electrode will be put outside in a boundary region.
[0058]
Therefore, according to this mode, it becomes very easy to put outside the electrode which constitutes an external circuit connection terminal. Moreover, the electric connection with the 2nd wiring should just be because this 2nd wiring is installed from the aforementioned electrode.
[0059]
Thus, according to this mode, it becomes possible to realize electrical installation between an external circuit connection terminal and the 2nd wiring reasonable.
[0060]
moreover, in other modes of an electro-optic device equipped with the 2nd wiring Connect electrically and said 1st wiring and said frame pattern are not formed. And a part for part I and said 1st wiring of said 2nd wiring are connected electrically. A part for part II and said frame pattern of said 2nd wiring are connected electrically, a part for said part I may be connected to a part for part I of said external circuit connection terminal, and a part for said part II may be made to be connected to a part for part II of said external circuit connection terminal, respectively.
[0061]
According to such a configuration, each of a frame pattern and the 1st wiring is maintainable to different potential. In this case, that each of a frame pattern and the 1st wiring is maintainable to different potential if the premise that the counterelectrode is connected to a frame pattern is placed while it is cautious of it being for the 1st wiring supplying predetermined potential to a capacity electrode turns into that each of a capacity electrode and a counterelectrode is maintainable to different potential to homonymy. If the potential in a part for part I of an external circuit connection terminal is supplied, this the amount of part I concerned If different potential from said a certain potential is supplied to a part for part II of an external circuit connection terminal while a capacity electrode is maintained by the potential concerned, since it connects with a part for part I, the 1st wiring, and the capacity electrode of the 2nd wiring Since it connects with a part for part II, frame pattern, and counterelectrode of the 2nd wiring, the amount of part II concerned is because a counterelectrode will be maintained by the potential concerned. If this is summarized, it will become as it is shown in the following table 1. In addition, what materialized each [these] concept is explained as the [5th operation gestalt] in the gestalt of implementation of invention explained later.
[0062]
[A table 1]

	電気の流れは左欄から右欄へ （上欄と下欄とは各々独立の電気の流れを表している）			
容量電極への電気の流れ	外部回路接続端子の第１部分	第２配線の第１部分	第１配線	容量電極
対向電極への電気の流れ	外部回路接続端子の第２部分	第２配線の第２部分	額縁パターン	対向電極

[0063]
Thereby, according to this mode, it can perform adjusting suitably various kinds of electric operations generated within the electro-optic device concerned etc.
[0064]
In other modes of the electro-optic device of this invention, the 1st wiring consists of protection-from-light nature ingredients.
[0065]
According to this mode, the 1st wiring is wiring connected or installed by the capacity electrode, and since it is formed in an image display field, it can realize protection from light corresponding to the field to which the 1st wiring concerned is formed in the image display field. Since it becomes possible to prevent beforehand the situation where light carries out incidence to the semi-conductor layer (barrier layer) which constitutes an example slack thin film transistor of said switching element indiscriminately by this, it becomes possible about being able to control generating of the optical leakage current in this semi-conductor layer, therefore a flicker etc. occurring on an image to prevent beforehand.
[0066]
Moreover, according to this mode, the 2nd wiring formed as the same film as this 1st wiring will also consist of protection-from-light nature ingredients. Therefore, also about the thin film transistor as a switching element formed on a boundary region, the same operation effectiveness as the above can be acquired, it can have, and exact actuation of the thin film transistor concerned can be expected.
[0067]
And according to this mode, the frame pattern formed as the same film as said 1st wiring will also consist of protection-from-light nature ingredients further. Therefore, the operation effectiveness of the aforementioned optical leakage prevention will be enjoyed more effectively.
[0068]
In addition, as a "protection-from-light nature ingredient" said to this mode, for example, aluminum (aluminum) with the comparatively large rate of a light reflex etc. is included, and also the metal simple substance containing at least one of refractory metals, such as Ti (titanium), Cr (chromium), W (tungsten), Ta (tantalum), and Mo (molybdenum), an alloy, metal silicide, a polysilicon side, the thing that carried out the laminating of these are included.
[0069]
In other modes of the electro-optic device of this invention, said 1st wiring has the laminated structure which consists of an ingredient which is different from each other.
[0070]
According to this mode, it is constituted as the two-layer structure, such as a layer which turns into a lower layer of the 1st wiring from aluminum, and a layer which turns into that upper layer from titanium nitride, for example. In this case, according to the upper titanium nitride layer, at the same time the high

electric conduction engine performance and the protection-from-light engine performance by the rate of a light reflex being comparatively high are enjoyable according to the lower layer aluminum layer When carrying out patterning processing of the precursive film, such as an interlayer insulation film formed on the 1st wiring, Or in case a contact hole is formed in this interlayer insulation film etc., it becomes possible to enjoy the function to prevent the so-called generating through which it runs (that is, for the layer which consists of this titanium nitride to function as the so-called dirty stop).

[0071]

Thus, according to this mode, by constituting the 1st wiring as what has a "laminated structure", it is possible to give a new function to this 1st wiring in addition to making a capacity electrode bear the function to supply potential, and the advanced features can be attained.

[0072]

In addition, it cannot be overemphasized that it is possible to adopt various configurations besides a **** as a "laminated structure" said to this mode.

[0073]

Moreover, according to this mode, will have the laminated structure which the 2nd wiring and the frame pattern which are formed as the same film as the 1st wiring also become from the ingredient which is different from each other, but The function in which this 2nd wiring and this frame pattern bear selection of each ingredient which constitutes this laminated structure It is good to carry out from a viewpoint of giving a new function after (namely, taking into consideration to connection (the 2nd wiring) of an external circuit connection terminal, a scanning-line actuation circuit, and a data-line actuation circuit, mediation (frame pattern) of the potential supply to the 1st wiring from the 2nd wiring, etc.). In addition, the aforementioned two-layer structure containing example slack aluminum of low electrical resistance materials can say that it is desirable also from such a viewpoint.

[0074]

In other modes of the electro-optic device of this invention, it comes further to prepare for said substrate the light-shielding film formed on the opposite substrate by which opposite arrangement is carried out, and this opposite substrate, and said frame pattern is formed so that it may lap with said light-shielding film.

[0075]

According to this mode, when projecting light towards a substrate from an opposite substrate, in a frame field, first, protection from light by said light-shielding film is performed, then protection from light by the frame pattern is performed, for example. Thus, according to this mode, the operation effectiveness of the optical leakage prevention mentioned above will be more effectively done so by realizing protection from light of a duplex.

[0076]

You may make it said light-shielding film contain the frame light-shielding film formed so that the side edge of said opposite substrate might be met in this mode.

[0077]

According to such a configuration, protection from light of the above-mentioned duplex will be better realized from a light-shielding film containing a frame light-shielding film.

[0078]

The electronic equipment of this invention comes to provide the electro-optic device (however, for the various modes to be included.) of above-mentioned this invention, in order to solve the above-mentioned technical problem.

[0079]

Since it comes to provide the electro-optic device of this invention mentioned above according to the electronic equipment of this invention, that the image of patterns, such as various kinds of wiring, is reflected in the perimeter of an image etc. can realize various electronic equipment, such as a video tape recorder of the projector and liquid crystal television which can display a quality image, a cellular phone, an electronic notebook, a word processor, a viewfinder mold, or a monitor direct viewing type, a workstation, a TV phone, a POS terminal, and a touch panel, by being prevented beforehand.

[0080]
Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.
[Best Mode of Carrying Out the Invention]
[0081]
Below, it explains, referring to drawing about the gestalt of operation of this invention. The following operation gestalten apply the electro-optic device of this invention to liquid crystal equipment.
[0082]
[The 1st operation gestalt]
[The whole electro-optic device configuration]
First, the whole 1st operation gestalt configuration concerning the electro-optic device of this invention is explained with reference to drawing 1 and drawing 2 . It is the top view of the electro-optic device seen from the opposite substrate side with each component with which drawing 1 was formed on it in the TFT array substrate here, and drawing 2 is the H-H' sectional view of drawing 1 . Here, the liquid crystal equipment of the actuation circuit built-in TFT active-matrix actuation method which is an example of an electro-optic device is taken for an example.
[0083]
In drawing 1 and drawing 2 , opposite arrangement of the TFT array substrate 10 and the opposite substrate 20 is carried out with the electro-optic device concerning the 1st operation gestalt. The liquid crystal layer 50 is enclosed between the TFT array substrate 10 and the opposite substrate 20, and the TFT array substrate 10 and the opposite substrate 20 are mutually pasted up by the sealant 52 prepared in the seal field located in the perimeter of image display field 10a.
[0084]
After it consists of ultraviolet-rays hardening resin, heat-curing resin, etc. in order to stick both substrates, and a sealant 52 is applied on the TFT array substrate 10 in a manufacture process, it is stiffened by UV irradiation, heating, etc. Moreover, in the sealant 52, gap material, such as a glass fiber for making spacing (gap between substrates) of the TFT array substrate 10 and the opposite substrate 20 into a predetermined value or a glass bead, is sprinkled. That is, the electro-optic device of the 1st operation gestalt is small as an object for the light valves of a projector, and suitable for performing an enlarged display.
[0085]
In parallel to the inside of the seal field where the sealant 52 has been arranged, the frame light-shielding film 53 of the protection-from-light nature which specifies the frame field of image display field 10a is formed in the opposite substrate 20 side. However, a part or all of such a frame light-shielding film 53 may be prepared in the TFT array substrate 10 side as a built-in light-shielding film. In addition, in the 1st operation gestalt, the boundary region which specifies the circumference of the aforementioned image display field 10a exists. In other words, especially in the 1st operation gestalt, it sees from the core of the TFT array substrate 10, and beyond is specified as a boundary region from this frame light-shielding film 53.
[0086]
The data-line actuation circuit 101 and the external circuit connection terminal 102 are formed in the field located in the outside of the seal field where the sealant 52 has been arranged among boundary regions along with one side of the TFT array substrate 10. Moreover, along with two sides which adjoin this one side, the scanning-line actuation circuit 104 is covered with said frame light-shielding film 53, and is made and prepared. Furthermore, in order to connect between two scanning-line actuation circuits 104 established in the both sides of image display field 10a in this way, as it is covered with said frame light-shielding film 53, two or more wiring 105 is formed along with one side in which the TFT array substrate 10 remains. Among these, the data-line actuation circuit 101 and the scanning-line actuation circuit 104 are connected with the external circuit connection terminal 102 through wiring 404.
[0087]
Moreover, the vertical flow material 106 which functions as a vertical flow terminal between both

substrates is arranged at the four corner sections of the opposite substrate 20. The flow-under besides material 106 consists of a configuration that conductive particles, such as silver dust, were hardened etc. On the other hand, in the field which counters these corner sections, the vertical flow terminal is prepared in the TFT array substrate 10. By these, an electric flow can be taken between the TFT array substrate 10 and the opposite substrate 20.

[0088]

In drawing 2 , the orientation film is formed on pixel electrode 9a after wiring of TFT for pixel switching, the scanning line, the data line, etc., etc. was formed on the TFT array substrate 10. On the other hand, on the opposite substrate 20, the orientation film is formed at a part for the light-shielding film 23 of the shape of the shape of others and a grid, and a stripe, and also the management of the maximum. [counterelectrode / 21] Moreover, the liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds, and takes a predetermined orientation condition between the orientation film of these couples.

[0089]

In the electro-optic device of the 1st operation gestalt which has the above whole configurations, although it is characteristic among the various elements mentioned above about the concrete configuration about wiring 404 and vertical flow material 106 grade, the point is explained in full detail behind, referring to drawing 7 etc.

[0090]

In addition, on the TFT array substrate 10 shown in drawing 1 and drawing 2 , the inspection circuit for inspecting the sampling circuit which samples the picture signal on a picture signal line, and is supplied to the data line, the precharge circuit which precedes the precharge signal of a predetermined voltage level with a picture signal, and supplies it to two or more data lines respectively, the quality of the electro-optic device concerned at the manufacture middle or the time of shipment, a defect, etc. in addition to these data-line actuation circuits 101 and scanning-line actuation circuit 104 grade etc. may be formed.

[0091]

[The configuration in a picture element part]

Below, the configuration in the picture element part of the electro-optic device in the 1st operation gestalt of this invention is explained with reference to drawing 7 from drawing 3 . Drawing 4 and drawing 5 are top views of two or more pixel groups where the TFT array substrate with which drawing 3 is equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of an electro-optic device] a matrix, and wiring, and the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other here. In addition, drawing 4 and drawing 5 are understanding and illustrating a part for a lower layer part (drawing 4) and a management (drawing 5) among the laminated structures mentioned later, respectively.

[0092]

Moreover, drawing 6 is an A-A'sectional view at the time of piling up drawing 4 and drawing 5 , and drawing 7 (a) and drawing 7 (b) are the sectional views about the part in which the vertical flow material 106 in the enlarged drawing and drawing 1 for the interior of a circle which attached the sign Z in drawing 2 exists, respectively, and it is a sectional view corresponding to the laminated structure which all show to drawing 6 . In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, contraction scales are made to have differed for every each class and each part material of this in drawing 6 and drawing 7 .

[0093]

(Circuitry of a picture element part)

In drawing 3 , TFT30 for carrying out switching control of pixel electrode 9a and the pixel electrode 9a concerned is formed in two or more pixels formed in the shape of [which constitutes the image display field of the electro-optic device in the 1st operation gestalt] a matrix, respectively, and data-line 6a to which a picture signal is supplied is electrically connected to the source concerned of TFT30. The picture signals S1, S2, ..., Sn written in data-line 6a may be supplied to line sequential, and you may

make it supply them to this order for every group to two or more data-line 6a which adjoin each other.
[0094]
Moreover, gate electrode 3a is electrically connected to the gate of TFT30, and it consists of predetermined timing so that the scan signals G1, G2, ..., Gm may be impressed to scanning-line 11a and gate electrode 3a in pulse line sequential at this order. It connects with the drain of TFT30 electrically, and pixel electrode 9a writes in the picture signals S1, S2, ..., Sn supplied from data-line 6a in TFT30 which is a switching element when only a fixed period closes the switch to predetermined timing.
[0095]
Fixed period maintenance of the picture signals S1, S2, ..., Sn of the predetermined level written in the liquid crystal as an example of electrooptic material through pixel electrode 9a is carried out between the counterelectrodes formed in the opposite substrate. When the orientation and order of molecular association change with the voltage levels impressed, liquid crystal modulates light and enables a gradation display. The transmission to incident light decreases according to the electrical potential difference impressed in the unit of each pixel when it was in no MARI White mode, if it is in NOMA reeve rack mode, the transmission to incident light will be increased according to the electrical potential difference impressed in the unit of each pixel, and light with the contrast according to a picture signal will carry out outgoing radiation from an electro-optic device as a whole.
[0096]
In order to prevent the picture signal held here leaking, storage capacitance 70 is added to the liquid crystal capacity and juxtaposition which are formed between pixel electrode 9a and a counterelectrode. This storage capacitance 70 is formed together with scanning-line 11a, and it contains the capacity electrode 300 fixed to constant potential while it contains a fixed potential side capacity electrode.
[0097]
[The concrete configuration of a picture element part]
Below, the concrete configuration of the electro-optic device with which the above circuit actuation by above-mentioned data-line 6a, scanning-line 11a and gate electrode 3a, and TFT30 grade is realized is explained with reference to drawing 4 thru/or drawing 7 .
[0098]
First, in drawing 4 and drawing 5 , two or more pixel electrode 9a is prepared in the shape of a matrix on the TFT array substrate 10 (the profile is shown by the dotted-line section), and data-line 6a and scanning-line 11a are prepared respectively along the boundary of pixel electrode 9a in every direction. Data-line 6a consists of a laminated structure containing the aluminum film etc. so that it may mention later, and scanning-line 11a consists of conductive polish recon film etc. moreover -- the scanning line -- 11 -- a -- a semi-conductor -- a layer -- one -- a -- inside -- drawing -- inside -- an upward slant to the right -- a slash -- a field -- having been shown -- a channel -- a field -- one -- a -- ' -- countering -- the gate -- an electrode -- three -- a -- a contact hole -- 12 -- cv -- minding -- electric -- connecting -- having -- **** -- this -- the gate -- an electrode -- three -- a -- this -- the scanning line -- 11 -- a -- containing -- having -- a form -- becoming -- **** .
[0099]
That is, TFT30 for pixel switching by which opposite arrangement of the gate electrode 3a contained in scanning-line 11a at channel field 1a' was carried out is formed in the crossing part of gate electrode 3a and data-line 6a, respectively. Thereby, TFT30 (except for a gate electrode) serves as a gestalt which exists between gate electrode 3a and scanning-line 11a.
[0100]
Next, the electro-optic device is equipped with the quartz substrate, the glass substrate, the TFT array substrate 10 that consists of a silicon substrate, and the opposite substrate 20 which opposite arrangement is carried out at this, for example, consists of a glass substrate or a quartz substrate as shown in A-A'line sectional view slack drawing 6 of drawing 4 and drawing 5 .
[0101]
As shown in drawing 6 , the aforementioned pixel electrode 9a is prepared and the orientation film 16

with which predetermined orientation processing of rubbing processing etc. was performed is formed in the upside at the TFT array substrate 10 side. Pixel electrode 9a consists of transparent conductive film, such as for example, ITO film. On the other hand, it crosses all over the, the counterelectrode 21 is formed in the opposite substrate 20 side, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductive film, such as ITO film, like above-mentioned pixel electrode 9a.

[0102]

Thus, between the TFT array substrate 10 by which opposite arrangement was carried out, and the opposite substrate 20, electrooptic material, such as liquid crystal, is enclosed with the space surrounded by the above-mentioned sealant 52 (refer to drawing 1 and drawing 2), and the liquid crystal layer 50 is formed. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 16 and 22 in the condition that the electric field from pixel electrode 9a are not impressed.

[0103]

On the other hand, on the TFT array substrate 10, various kinds of configurations containing these besides the aforementioned pixel electrode 9a and the orientation film 16 make a laminated structure, and it has them. The 1st layer in which this laminated structure contains scanning-line 11a sequentially from the bottom as shown in drawing 6 , It consists of the 6th layer (the maximum upper layer) containing the 4th layer containing the 2nd layer containing the TFT30 grade containing gate electrode 3a, the 3rd layer containing storage capacitance 70, data-line 6a, etc., the 5th layer containing the example slack capacity wiring 400 grade of the "1st wiring" said to this invention, above pixel electrode 9a, and orientation film 16 grade.

[0104]

Moreover, between the 1st layer and the 2nd layer, between the 2nd layer and the 3rd layer, between the 3rd layer and the 4th layer, the 3rd interlayer insulation film 43 is formed between the 4th layer and the 5th layer, the 4th interlayer insulation film 44 is formed for the 2nd interlayer insulation film 42 between the 5th layer and the 6th layer, respectively, and the 1st interlayer insulation film 41 has prevented [the substrate insulator layer 12] that between each above-mentioned element connects too hastily. Moreover, the contact hole which connects electrically 1d of high concentration source fields in semi-conductor layer 1a of TFT30 and data-line 6a is established in the insulator layers 12, 41, 42, 43, and 44 of these various kinds. Below, each of these elements are explained sequentially from the bottom. In addition, from the 1st layer to the 3rd layer of the above-mentioned is illustrated by drawing 4 as a lower layer part, and from the 4th layer to the 6th layer is illustrated by drawing 5 as a part for a management.

[0105]

(-, such as a laminated structure and the configuration-scanning line of the 1st layer)

First, scanning-line 11a which consists of the metal simple substance containing at least one of refractory metals, such as Ti, Cr, W, Ta, and Mo, an alloy, metal silicide, a polysilicon side, a thing that carried out the laminating of these, or conductive polish recon is prepared in the 1st layer. This scanning-line 11a is seen superficially, and patterning is carried out to the shape of a stripe so that it may meet in the direction of X of drawing 4 . If it sees in more detail, stripe-like scanning-line 11a is equipped with the main track section prolonged so that it may meet in the direction of X of drawing 4 , and the lobe prolonged in the direction of Y of drawing 4 in which data-line 6a or the capacity wiring 400 extends. In addition, the lobe prolonged from adjoining scanning-line 11a is not connected mutually, therefore this scanning-line 11a has a form divided respectively.

[0106]

(A laminated structure, the 2nd-layer configuration - -, such as TFT)

Next, TFT30 containing gate electrode 3a is formed as the 2nd layer. TFT30 has LDD (Lightly Doped Drain) structure, as shown in drawing 6 . As the component gate electrode 3a mentioned above, for example, channel field 1of semi-conductor layer 1a in which it becomes from polish recon film and channel is formed of electric field from gate electrode 3a a, -- ' -- Low concentration source field 1b in the insulator layer 2 containing the gate dielectric film with which gate electrode 3a and semi-conductor

layer 1a are insulated, and semi-conductor layer 1a, and a low concentration drain field 1c list are equipped with 1d of high concentration source fields, and high concentration drain field 1e.
[0107]
Moreover, with the 1st operation gestalt, the junction electrode 719 is formed in this 2nd layer as the same film as above-mentioned gate electrode 3a. This junction electrode 719 is seen superficially, and as shown in drawing 4 , it is formed in island shape so that it may be located in the center of abbreviation of one side which extends in the direction of X of each pixel electrode 9a. Since the junction electrode 719 and gate electrode 3a are formed as the same film, when the latter consists for example, of conductive polish recon film etc., the former also consists of conductive polish recon film etc.
[0108]
(Configuration-substrate insulator layer - between a laminated structure, the 1st layer, and the 2nd layer)

As shown in drawing 6 , on scanning-line 11a explained above and in the bottom of TFT30, the substrate insulator layer 12 which consists of silicon oxide etc. is formed. The substrate insulator layer 12 has the function to prevent property change of TFT30 for pixel switching with the dry area at the time of surface polish of the TFT array substrate 10, the dirt which remains after washing, by being formed all over the TFT array substrate 10 besides the function which carries out layer insulation of TFT30 from scanning-line 11a.
[0109]
Groove contact hole 12cv which met in the direction of the channel length of semi-conductor layer 1a prolonged along with data-line 6a which sees superficially and is later mentioned by both side of semi-conductor layer 1a is dug in this substrate insulator layer 12, and gate electrode 3a by which a laminating is carried out to that upper part contains the part formed in the bottom at the concave corresponding to this contact hole 12cv. Moreover, this and side-attachment-wall section 3b formed in one are installed in this gate electrode 3a by forming gate electrode 3a, as this whole contact hole 12cv is buried. Thereby, it sees superficially, and is covered from the side and the incidence of the light from this part is controlled at least as semi-conductor layer 1a of TFT30 is well shown in drawing 4 .
[0110]
Moreover, while this side-attachment-wall section 3b is formed so that above contact hole 12cv may be buried as shown in drawing 4 , he is trying to touch it with scanning-line 11a of the above [that soffit]. Since scanning-line 11a is formed in the shape of a stripe as mentioned above, gate electrode 3a and scanning-line 11a which exist in a certain line always become same electric potential here, as long as its attention is paid to the line concerned.
[0111]
(-, such as a laminated structure and configuration-storage capacitance of the 3rd layer)
Now, as shown in drawing 6 , storage capacitance 70 is formed in the 3rd layer after the 2nd above-mentioned layer. Storage capacitance 70 is formed by carrying out opposite arrangement of the lower electrode 71 as a pixel potential side capacity electrode connected to high concentration drain field 1e of TFT30, and pixel electrode 9a, and the capacity electrode 300 as a fixed potential side capacity electrode through a dielectric film 75. According to this storage capacitance 70, it becomes possible to raise notably the potential maintenance property in pixel electrode 9a. Moreover, since the storage capacitance 70 concerning the 1st operation gestalt is formed so that it may turn out that the top view of drawing 4 is seen, and the light transmission field corresponding to the formation field of pixel electrode 9a may not be reached mostly, the pixel numerical aperture of the whole electro-optic device is maintained comparatively greatly (since it is formed so that it may be settled in a protection-from-light field, if it puts in another way), and it becomes possible [displaying a thereby more bright image].
[0112]
Here, the configuration of being prepared in the upper part of storage capacitance 70 at reverse is sufficient as the electrode as the above-mentioned pixel potential side capacity electrode in the lower electrode 71. In this case, the capacity electrode 300 as a fixed potential side capacity electrode will be formed in the lower part of storage capacitance 70 with a natural thing. As a suitable example, a pixel

potential side capacity electrode may be the same film as high concentration drain field 1e by which high concentration drain field 1e of TFT30 was extended, and the capacity electrode 300 as a fixed potential side capacity electrode may be the same layer as the protection-from-light layer for shading the incident light which exists further caudad and invades into TFT30 from a lower part from TFT30. Although it becomes easy and has desirable structure that it is the film of the same layer as the capacity electrode 300 as a fixed potential side capacity electrode, it does not limit the capacity wiring 400 later mentioned in this case to this.

[0113]

More, the lower electrode 71 becomes a detail from the conductive polish recon film, and functions on it as a pixel potential side capacity electrode. However, the lower electrode 71 may consist of the monolayer film or multilayers containing a metal or an alloy. Moreover, this lower electrode 71 has the function which carries out trunk connection of pixel electrode 9a besides the function as a pixel potential side capacity electrode, and the high concentration drain field 1e of TFT30. Incidentally, trunk connection said here is performed through the aforementioned junction electrode 719.

[0114]

The capacity electrode 300 functions as a fixed potential side capacity electrode of storage capacitance 70. In the 1st operation gestalt, in order to make the capacity electrode 300 into fixed potential, it is made by planning the capacity wiring 400 (it mentioning later.) and electrical installation which were made into fixed potential. Here, in the connection for making the capacity electrode 300 into fixed potential, although the capacity wiring 400 is relayed, the capacity wiring 400 may be extended as the same film as the capacity electrode 300, and may be formed, for example. By this configuration, the capacity wiring 400 is not needed as another layer, but the wiring resistance buildup by connection resistance is also lost, and a process also becomes easy in order for there to be also no need of preparing the layer as capacity wiring 400 independently.

[0115]

moreover, the metal simple substance with which the capacity electrode 300 contains at least one of refractory metals, such as Ti, Cr, W, Ta, and Mo, an alloy, metal silicide, a polysilicon side, and the thing that carried out the laminating of these -- or it consists of tungsten silicide preferably.

[0116]

Thereby, the capacity electrode 300 has the function which interrupts the light which is going to carry out incidence to TFT30 from an upside.

[0117]

A dielectric film 75 consists of oxidation silicone films, such as comparatively thin HTO (High Temperature Oxide) film of about 5-200nm of thickness, and LTO (Low Temperature Oxide) film, or a silicon nitride film, as shown in drawing 6 . As long as membranous dependability is fully acquired from a viewpoint which increases storage capacitance 70, a dielectric film 75 is so good that it is thin.

[0118]

In the 1st operation gestalt, it has oxidation silicone film 75a in a lower layer, and this dielectric film 75 has the two-layer structure like silicon nitride film 75b in the upper layer, as shown in drawing 6 . Patterning of the upper silicon nitride film 75b is carried out to big size for a while than the lower electrode 71 of a pixel potential side capacity electrode, and it is formed so that it may be settled in a protection-from-light field (non-opening field).

[0119]

(Configuration-1st interlayer insulation film - between a laminated structure, the 2nd layer, and the 3rd layer)

The 1st interlayer insulation film 41 which consists of NSG preferably, such as silicate glass film, such as NSG (non silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (boron phosphorus silicate glass), a silicon nitride film, and an oxidation silicone film, is formed on TFT30 thru/or gate electrode 3a, and the junction electrode 719 which were explained above, and in the bottom of storage capacitance 70.

[0120]

And it is punctured, the contact hole 81 which connects electrically to this 1st interlayer insulation film 41 1d of high concentration source fields of TFT30 and data-line 6a mentioned later penetrating the 2nd interlayer insulation film 42 of a postscript. Moreover, the contact hole 83 which connects electrically to the 1st interlayer insulation film 41 high concentration drain field 1e of TFT30 and the lower electrode 71 which constitutes storage capacitance 70 is punctured. Furthermore, the contact hole 881 for connecting electrically to this 1st interlayer insulation film 41 the lower electrode 71 and the junction electrode 719 as a pixel potential side capacity electrode which constitute storage capacitance 70 is punctured. It is punctured the contact hole 882 for furthermore, connecting electrically to the 1st interlayer insulation film 41 the junction electrode 719 and the 2nd junction electrode six a2 mentioned later in addition penetrating the 2nd interlayer insulation film of a postscript.

[0121]

(-, such as a laminated structure and the configuration-data line of the 4th layer)

Now, data-line 6a is prepared in the 4th layer after the 3rd above-mentioned layer. This data-line 6a is formed from the lower layer as film which has three layer systems of the layer (refer to sign 41A in drawing 6) which becomes order from aluminum, the layer (refer to sign 41TN in drawing 6) which consists of titanium nitride, and the layer (sign 401 reference in drawing 6) which consists of a silicon nitride film, as shown in drawing 6 . Patterning of the silicon nitride film is carried out to big size for a while so that the lower layer aluminum layer and titanium nitride layer may be covered.

[0122]

Moreover, the junction layer six a1 for capacity wiring and the 2nd junction electrode six a2 are formed in this 4th layer as the same film as data-line 6a. If it sees superficially as these show drawing 5 , it is not formed so that it may have the flat-surface configuration which followed data-line 6a, and it is formed between each ** so that it may be divided on patterning. For example, if its attention is paid to data-line 6a located in the method of the leftmost in drawing 5 , the 2nd junction electrode six a2 which has the shape of the junction layer six a1 for capacity wiring which has the shape of an abbreviation quadrilateral in the method of the ****, and an abbreviation quadrilateral which has a larger area a little than the junction layer six a1 for capacity wiring further at the method of the right is formed.

[0123]

(Configuration-2nd interlayer insulation film - between a laminated structure, the 3rd layer, and the 4th layer)

The 2nd interlayer insulation film 42 preferably formed by the plasma-CVD method using TEOS gas, such as silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, and an oxidation silicone film, is formed on the storage capacitance 70 explained above and in the bottom of data-line 6a. While the aforementioned contact hole 81 which connects electrically 1d of high concentration source fields of TFT30 and data-line 6a to this 2nd interlayer insulation film 42 is punctured, the contact hole 801 which connects electrically said junction layer six a1 for capacity wiring and up electrode slack capacity electrode 300 of storage capacitance 70 is punctured. Furthermore, the aforementioned contact hole 882 for connecting electrically the 2nd junction electrode six a2 and the junction electrode 719 to the 2nd interlayer insulation film 42 is formed.

[0124]

(-, such as a laminated structure and the 5th-layer configuration-capacity wiring)

Now, the capacity wiring 400 is formed in the 5th layer after the 4th above-mentioned layer.

If it sees superficially, this capacity wiring 400 is formed in the shape of a grid so that it may extend in the direction of X in drawing, and each direction of Y, as shown in drawing 5 . It is formed more broadly than this data-line 6a so that data-line 6a may be covered especially about the part which extends in the direction of Y in drawing among these capacity wiring 400. Moreover, about the part which extends in the direction of X in drawing, in order to secure the field which forms the below-mentioned 3rd junction electrode 402, it has the notching section near [central / of one side] each pixel electrode 9a.

[0125]

Furthermore, among drawing 5 , in the corner for an intersection of the capacity wiring 400 which

extends in each XY direction, as this corner is filled, the abbreviation triangle-like part is prepared. Light to semi-conductor layer 1a of TFT30 can be effectively covered by preparing the part of the shape of this abbreviation triangle in the capacity wiring 400. That is, to semi-conductor layer 1a, the light which is going to advance from slant will be reflected or absorbed in the part of the shape of this triangle, and will not result in semi-conductor layer 1a. Therefore, generating of optical leakage current is made in control, and it becomes possible to display a quality image without a flicker etc.

[0126]

This capacity wiring 400 is installed in that perimeter from image display field 10a by which pixel electrode 9a has been arranged, and it is counterelectrode potential, an actuation circuit, and connecting with the constant source of potential and the electric target of a circumference circuit in addition to this, and let it be fixed potential (refer to explanation about the next wiring 404).

[0127]

Thus, while being formed so that the whole data-line 6a may be covered, according to existence of the capacity wiring 400 made into fixed potential, it becomes possible to eliminate the effect of capacity coupling produced between this data-line 6a and pixel electrode 9a. That is, it becomes possible to avoid beforehand the situation of changing the potential of pixel electrode 9a, according to the energization to data-line 6a, and possibility of generating the display nonuniformity which met on the image at this data-line 6a can be reduced. Since the capacity wiring 400 is formed in the shape of a grid especially in the 1st operation gestalt, it is possible to control this so that capacity coupling unnecessary about the part into which scanning-line 11a extends may not arise.

[0128]

Moreover, the 3rd junction electrode 402 is formed in the 5th layer as the same film as such capacity wiring 400. This 3rd junction electrode 402 has the function to relay the electrical installation between 2nd junction electrode six a2 and pixel electrode 9a, through the below-mentioned contact holes 804 and 89. In addition, a flat-surface configuration target is followed between these capacity wiring 400 and the 3rd junction electrode 402, and it is not formed, and between both, it is formed so that it may be divided on patterning.

[0129]

On the other hand, the above-mentioned capacity wiring 400 and the 3rd junction electrode 402 have the two-layer structure of the layer which turns into a lower layer from aluminum, and the layer which turns into the upper layer from titanium nitride. Thus, since the capacity wiring 400 and the 3rd junction electrode 402 contain the titanium nitride which was comparatively excellent in the optical absorption engine performance, including the aluminum which was comparatively excellent in the light reflex engine performance, this capacity wiring 400 and this 3rd junction layer 402 may function as protection-from-light layers. That is, according to these, it is possible to interrupt progress of the incident light (refer to drawing 6) to semi-conductor layer 1a of TFT30 with the up side.

[0130]

And especially in the 1st operation gestalt, as shown in drawing 7 (a) and drawing 7 (b), leading-about wiring installed by the above-mentioned capacity wiring 400 and leading-about wiring which consists of wiring 404 (it corresponds to an example of the "2nd wiring" said to this invention.) and a frame pattern 406 in more detail are formed in fields other than image display field 10a. Below, it explains, referring to each drawing and drawing 8 which touched by the above-mentioned about the configuration of this leading-about wiring. It is drawing for illustrating clearly the arrangement relation of leading-about wiring and the capacity wiring 400 which drawing 8 is drawing of drawing 1 and this meaning, and consist of wiring 404 and a frame pattern 406 especially here. In addition, especially in drawing 8 , some (for example, the data-line actuation circuit 101 of drawing 1 or the 3rd junction electrode 402 grade of drawing 5) graphic displays of the elements which are adding modification so that it can check by looking suitably about the contraction scale of wiring 404 or the contraction scale of the frame pattern 406, a flat-surface configuration, an array pitch, etc., and were shown in drawing 1 etc. are suitably omitted for the aforementioned object.

[0131]

First, as shown in drawing 7 (a) and drawing 8 , the wiring 404 installed by the capacity wiring 400 through the frame pattern 406 is formed in the boundary region. That is, this wiring 404 is formed on the 3rd interlayer insulation film 43 as the same film as the capacity wiring 400 and the 3rd junction electrode 402 (it may be hereafter called "capacity wiring 400 grade"). Thereby, wiring 404 has the two-layer structure of the layer which turns into a lower layer from aluminum, and the layer which turns into the upper layer from titanium nitride like the above-mentioned capacity wiring 400 and the 3rd junction electrode 402.

[0132]

A part of this wiring 404 constitutes external circuit connection terminal 102Q explained with reference to drawing 1 and drawing 2 . By forming contact hole 44H1 which passes to this wiring 404, when the top face of this wiring 404 is exposed to the exterior, specifically, external circuit connection terminal 102Q is formed in the 4th interlayer insulation film 44 formed on wiring 404.

[0133]

In addition, the film which consists of titanium nitride of the upper layer of wiring 404 may be removed at the time of opening of contact hole 44H1 in this case. Thereby, in case this wiring 404 and an external circuit are connected electrically, since direct continuation of this external circuit will be carried out to the film which consists of lower layer aluminum, it can realize low resistance-ization in respect of connection. Moreover, since the film which consists of this titanium nitride is hard film in case the electro-optic device concerned is inspected [having made freely the film which consists of titanium nitride of the upper layer of wiring 404 remain, and] through the external circuit connection terminal 102Q concerned, we are anxious about the nonconformity of being hard to carry out slipping inspection of the inspection terminal arising, but if the film which consists of this titanium nitride is removed, it is not necessary to wear such nonconformity.

[0134]

Incidentally, although the wiring 404 as shown in drawing 7 (a) is similarly formed about all the external circuit connection terminals 102 shown in drawing 1 , what is installed by the capacity wiring 400, i.e., this capacity wiring 400 and the thing by which electric communication is achieved, is a part of the them concerned. That is, although only the wiring 404 corresponding to specific external circuit connection terminal 102Q is installed with the capacity wiring 400 among the external circuit connection terminals 102, it is formed and it is formed as the same film as capacity wiring 400 grade about the wiring 404 corresponding to the remaining external circuit connection terminal 102 as shown in drawing 8 or drawing 1 , both are formed so that it may be divided on patterning.

[0135]

On the other hand, in the 1st operation gestalt, further, as shown in drawing 7 (b) and drawing 8 , the aforementioned capacity wiring 400 grade and the frame pattern 406 installed by the wiring 404 further mentioned above are formed. That is, this frame pattern 406 is formed on the 3rd interlayer insulation film 43 as the same film as capacity wiring 400 grade and the frame pattern 406. This has the two-layer structure of the layer which turns into a lower layer from aluminum like the capacity wiring 400 grade of the above-mentioned [the frame pattern 406], and the layer which turns into the upper layer from titanium nitride.

[0136]

As shown in drawing 8 , the frame pattern 406 is formed so that all the perimeters of image display field 10a may be surrounded, and has the abbreviation hollow square shape as a whole so that the formation field of the sealant 52 around the frame field (namely, field corresponding to the formation field of the frame light-shielding film 53) which carries out plane view and demarcates image display field 10a and a boundary region, and this frame field may be filled. Since it is installed by the wiring 404 connected to the aforementioned specific external circuit connection terminal 102Q as this frame pattern 406 is shown in the method of drawing 8 Nakashita, the frame pattern 406 and specific external circuit connection terminal 102Q are connected mutually electrically. Moreover, when the frame pattern 406 is installed by the capacity wiring 400, this capacity wiring 400 and specific external circuit connection terminal 102Q are also connected mutually electrically. By the above, wiring 404, the frame pattern 406, and the

capacity wiring 400 which were connected to specific external circuit connection terminal 102Q always become same electric potential after all.

[0137]

Moreover, as some frame patterns 406 are shown in drawing 7 (b), after being put outside by contact hole 44H2, electrical installation is realized also between the frame pattern 406 and a counterelectrode 21 by filling up with the sealant 52 containing the vertical flow material 106 (in addition, the part in contact with the vertical flow material 106 is set to connection part 406C on the frame pattern 406.). This connection part 406C will be prepared in the four corner sections concerned according to the vertical flow material 106 being arranged at the four corner sections of the opposite substrate 20, as explained with reference to drawing 1 .

[0138]

The wiring 404 connected to specific external circuit connection terminal 102Q in the 1st operation gestalt by the above, the frame pattern 406, the capacity wiring 400, and a counterelectrode 21 will serve as the always same potential.

[0139]

In addition, at the time of opening of contact hole 44H2, the film which consists of titanium nitride of the upper layer of the frame pattern 406 may be removed. Thereby, since direct continuation of the vertical flow material 106 will be carried out to the film which consists of lower layer aluminum of this frame pattern 406, it can realize low resistance-ization in respect of connection. Moreover, since the film which consists of this titanium nitride is hard film when the film which consists of titanium nitride exists, we are anxious about the nonconformity that the vertical flow material 106 does not come to be embedded, a touch area becomes small, and resistance becomes large arising, but if the film which consists of this titanium nitride is removed, it is not necessary to wear such nonconformity.

[0140]

In addition, in drawing 7 , as the same film as scanning-line 11a formed in an image display field, level difference adjustment film 11aP is formed, and level difference adjustment film 3aP is formed as the same film as gate electrode 3a and the junction electrode 719. Existence of these level difference adjustment film 11aP and 3aP(s) can adjust making almost the same the height of the whole laminated structure in an image display field and a boundary region etc.

[0141]

(Configuration-3rd interlayer insulation film - between a laminated structure, the 4th layer, and the 5th layer)

As shown in drawing 6 , the 3rd interlayer insulation film 43 preferably formed by the plasma-CVD method using TEOS gas, such as silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, and an oxidation silicone film, is formed on data-line 6a and in the bottom of the capacity wiring 400. The contact hole 804 for connecting electrically the contact hole 803, and the 3rd junction electrode 402 and the 2nd junction electrode six a2 for connecting electrically the aforementioned capacity wiring 400 and the junction layer six a1 for capacity wiring to this 3rd interlayer insulation film 43 is punctured, respectively.

[0142]

(They are -, such as a configuration-pixel electrode between the 5th layer and the 6th layer, to a laminated structure and the 6th layer list)

Finally, as mentioned above to the 6th layer, pixel electrode 9a is formed in the shape of a matrix, and the orientation film 16 is formed on this pixel electrode 9a. And the 4th interlayer insulation film 44 which consists of NSG preferably, such as silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, and an oxidation silicone film, is formed in the bottom of this pixel electrode 9a. The contact hole 89 for connecting electrically between pixel electrode 9a and the aforementioned 3rd junction electrode 402 to this 4th interlayer insulation film 44 is punctured. Between pixel electrode 9a and TFT30, it will connect electrically through the contact hole 804 mentioned above in this contact hole 89 and 3rd junction layer 402 list, the 2nd junction layer six a2, a contact hole 882, the junction electrode 719, a contact hole 881, the lower electrode 71, and a contact hole 83.

[0143]
Moreover, with the 1st operation gestalt, flattening of the front face of the 4th interlayer insulation film 44 is carried out by CMP (Chemical Mechanical Polishing) processing etc., and it reduces the poor orientation of the liquid crystal layer 50 resulting from the level difference by the various wiring, component, etc. which exist caudad. However, it may replace with the 4th interlayer insulation film 44 in this way performing flattening processing, or, in addition, flattening processing may be performed by trenching at least one of the TFT array substrate 10, the substrate insulator layer 12, the 1st interlayer insulation film 41, the 2nd interlayer insulation film 42, and the 3rd interlayer insulation films 43, and embedding wiring and the TFT30 grade of data-line 6a etc.
[0144]
[The operation effectiveness of the electro-optic device concerned]
According to the electro-optic device of the 1st operation gestalt used as the above configurations, since leading-about wiring which consists of wiring 404 and the frame pattern 406 which were especially explained as the 5th-layer configuration is formed, the following operation effectiveness will be done so.

[0145]
In the field to which this frame pattern 406 is first formed in the first place in the 1st operation gestalt by forming the frame pattern 406 in the frame field and the seal field Since it is possible to prevent beforehand that optical leakage arises as shown in the arrow head L1 of drawing 7 (b), it becomes possible to prevent that the image of patterns, such as various kinds of wiring, is reflected in the perimeter of an image etc. Therefore, according to the 1st operation gestalt, it becomes possible to display an image with more high quality.
[0146]
Since especially the frame pattern 406 concerning the 1st operation gestalt is formed so that all the perimeters of image display field 10a may be surrounded, it is possible also for intercepting thoroughly the light which penetrates a frame field or a seal field. [of a principle top] Moreover, the aforementioned optical screening is more certainly demonstrated from the frame pattern 406 having the two-layer structure of the layer which turns into a lower layer from aluminum, and the layer (it corresponding to an example of the "protection-from-light nature ingredient" with which all are said to this invention.) which turns into the upper layer from titanium nitride. This frame pattern 406 seems furthermore, not to become the obstacle of the light which penetrates image display field 10a, since it is formed by the frame pattern 406 so that from drawing 8 , and it may not lap with image display field 10a. That is, an image can be displayed as a request. In addition, what is necessary is just made to perform the optical exposure which is needed in the case of the hardening when a sealant 52 consists of a photo-setting resin etc. from the upper part of drawing 7 (b), i.e., the opposite substrate 20 side.
[0147]
Moreover, in relation to this, protection from light as shown in the arrow head L2 of drawing 7 (b) will also be realized in the 1st operation gestalt by forming the frame light-shielding film 53 on the opposite substrate 20. In this case, even if there is light which penetrates the frame light-shielding film 53, that light will be reflected or absorbed with the frame pattern 406 which is in a degree. Thus, according to the 1st operation gestalt, so to speak, protection from light of a duplex is realizable.
[0148]
Moreover, the frame pattern 406 applied to the 1st operation gestalt the second While a counterelectrode 21 and electrical installation are planned through the vertical flow material 106, since electrical installation is planned, the capacity wiring 400 this frame pattern 406 It combines with the function of the optical leakage prevention operation mentioned above, and is potential supply (this potential supply is performed in a contact hole 801 and 803 lists through the junction layer six a1 for capacity wiring.) to the potential supply to a counterelectrode 21 and the capacity wiring 400, as a result the capacity electrode 300. A peach requires the function of refer to drawing 6 . Simplification of an equipment configuration will be realized by this.
[0149]

This seems not to become the hindrance of image display, although electrical installation between the frame pattern 406 and a counterelectrode 21 is suitably realized since he is trying to correspond to the four corners of image display field 10a as the arrangement part of the vertical flow material 106 is shown in drawing 8 and drawing 1 in relation to this. In addition, since the frame pattern 406 is formed so that all the perimeters of image display field 10a may be surrounded, it can make more certainly the electrical installation of this frame pattern 406 and a counterelectrode 21. The thing for which, as for this, all the parts of the frame pattern 406 are connected electrically (formed as a pattern without an intermission if it puts in another way), and connection part 406C From two or more formation being carried out so that it may correspond to the four corners of image display field 10a, i.e., the four corners of the frame pattern 406 Even if it is the case where it becomes impossible electrically flowing either some frame patterns 406 or four vertical flow material 106 according to a certain situation even if, it is because it is possible to realize an electric flow duly by other parts.

[0150]

According to the 1st operation gestalt, the above thing enables it to maintain the potential of a counterelectrode 21 to stability extremely, and since the orientation condition of the liquid crystal molecule in the liquid crystal layer 50 pinched among this counterelectrode 21 and pixel electrode 9a can be adjusted suitably, it becomes possible to display a more nearly quality image.

[0151]

In addition, in the 1st operation gestalt, although external circuit connection terminal 102Q connected to the frame pattern 406 is prepared in two right and left among drawing as shown in drawing 8 , this invention is not limited to such a gestalt. For example, a gestalt with which external circuit connection terminal 102Q connected to the frame pattern 406 is prepared in either ****** and the right may be adopted.

[0152]

In the 1st operation gestalt, on the other hand, the frame pattern 406 which has a potential supply function to a counterelectrode 21 and the capacity wiring 400 as mentioned above As the same film as the wiring 404 connected to some wiring 404, i.e., specific external circuit connection terminal 102Q And since it is formed so that it may connect electrically, each [these] element is formed in a separate layer, for example, and can make the electric resistance value between this each element fall compared with a case so that it may say that electric connection is achieved by the contact hole etc. Therefore, in addition to supply of the stable potential to a counterelectrode 21 being realized, generating of the cross talk which considers high resistance-ization of capacity wiring 400 grade as a reason etc. can be prevented.

[0153]

In relation to this, wiring 404 and the capacity wiring 400 are formed through the 3rd interlayer insulation film 43 on data-line 6a in the 1st operation gestalt. Thereby, forming wiring 404 and the capacity wiring 400 as the same film and the external circuit connection terminal 102 become possible [attaining comparatively easily the request that it must be put outside, and the request that electric communication must be further aimed at between wiring 404 and the external circuit connection terminal 102] (refer to drawing 7 (a)). Moreover, especially with both the 1st operation gestalten, the above-mentioned operation effectiveness will be more effectively done so from wiring 404 and the capacity wiring 400 being formed only through the 4th interlayer insulation film 44 between directly under [containing pixel electrode 9a / of the 6th layer], i.e., this pixel electrode 9a.

[0154]

namely, -- since contact hole 44H1 for constituting the external circuit connection terminal 102 should form only about the 4th interlayer insulation film 44 by such configuration as shown in drawing 7 (a) -- the depth -- comparatively -- shallow -- this -- formation of contact hole 44H1 becomes comparatively easy.

[0155]

[The 2nd operation gestalt]

Below, the 2nd operation gestalt of this invention is explained, referring to drawing 9 thru/or drawing

11 . Drawing 9 is drawing of drawing 8 and this meaning, and the formation modes of a frame pattern differ here. However, unlike drawing 8 , in drawing 9 , the graphic display about the capacity wiring 400 is also omitted. Moreover, drawing 10 and drawing 11 are the explanatory views in which expanding near sign D shown in drawing 9 , and showing the circuitry in the part concerned etc. collectively. In addition, about almost all parts, such as the whole electro-optic device configuration of the 1st operation gestalt mentioned above with the 2nd operation gestalt, and a configuration of a picture element part, it is completely the same. Therefore, below, the explanation about the same part as the 1st operation gestalt is omitted, and suppose that explanation is mainly added only about a configuration characteristic of the 2nd operation gestalt.

[0156]

In drawing 9 , the frame pattern 461 which consists of frame patterns 461A and 461B is formed. Among these, frame pattern 461A corresponds to an example of the "1st pattern" said to this invention, and as shown in drawing 9 , it is continuously formed along with three sides (they are left part and the right-hand side to a drawing Nakagami side list) of image display field 10a which has the shape of a rectangle. Moreover, frame pattern 461B corresponds to an example of the "2nd pattern" said to this invention, and it divides with the aforementioned frame pattern 461A, and it is formed while being formed along with one side (drawing Nakashita side) in which image display field 10a remains (sign 461G in drawing reference.). And the vertical flow material 106 exists on frame pattern 461A among these.

[0157]

Like the above-mentioned 1st operation gestalt, by taking redundancy-[material / 106 / frame pattern 461A and / on it / four / vertical flow] structure, the electrical installation between the frame pattern 461 and a counterelectrode 21 can be made more certainly, and, according to such a gestalt, it becomes possible to maintain the potential of a counterelectrode 21 to stability extremely. Moreover, it is the same as that of the above-mentioned 1st operation gestalt that the operation effectiveness of optical leakage prevention is acquired by existence of the frame patterns 461A and 461B.

[0158]

Moreover, the following operation effectiveness is acquired by frame pattern 461B especially in the 2nd operation gestalt. That is, with the 2nd operation gestalt, frame pattern 461B is formed corresponding to the field in which the data-line actuation circuit 101 (refer to drawing 1) where the graphic display is omitted in drawing 9 is formed.

[0159]

The configuration of this data-line actuation circuit 101 neighborhood is shown in drawing 10 .
That is, the control line 114 pulled out from the data-line actuation circuit 101 is connected to the gate of the switching element 202 which constitutes a sampling circuit 118.

[0160]

On the other hand, the picture signal line 115 is connected to the source of a switching element 202 through the drawer wiring 116, and data-line 6a is connected to the drain. Thereby, the existence of supply of the picture signal from the picture signal line 115 to data-line 6a is controlled by ON-OFF of a switching element 202 being controlled by the data-line actuation circuit 101.

[0161]

However, with the configuration of the data-line actuation circuit 101 neighborhood equipped with such a configuration, there is a possibility that capacity coupling may occur between the aforementioned drawer wiring 116 and the counterelectrode 21 on the opposite substrate 20. If this capacity coupling occurs, in order to give fluctuation to the potential in another side by energization to one side, the display of the image as a request will be difficult.

[0162]

However, according to the 2nd operation gestalt, since the aforementioned frame pattern 461B is formed in the field concerned as shown in drawing 10 , this frame pattern 461B will exist between the picture signal line 115 and a counterelectrode 21, and generating of the aforementioned capacity coupling can be controlled. Therefore, according to the 2nd operation gestalt, the image as a request can be displayed suitably. In order to acquire such an operation more effectively incidentally, it is desirable to maintain

frame pattern 461B to fixed potential. For that purpose, it is good to connect this frame pattern 461B to the capacity wiring 400 (to refer to drawing 8) which is not illustrated in drawing 9 , for example.
[0163]
In addition, such operation effectiveness can enjoy the frame pattern 406 similarly like the 1st operation gestalt mentioned above in the mode formed so that all the perimeters of image display field 10a may be surrounded.
[0164]
Moreover, in the above-mentioned 2nd operation gestalt, although frame pattern 461B is formed so that the drawer wiring 116 prolonged from a sampling circuit 118 and this sampling circuit 118 may all be covered mostly, this invention is not limited to such a gestalt.
[0165]
For example, you may make it form frame pattern 461BB divided in the shape of a strip of paper, as shown in drawing 11 . When adopting such a configuration incidentally, it is not necessary to maintain these strips-of-paper-like frame pattern 461BB to fixed potential, and, unlike drawing 10 , you may make it floating (floating potential).
[0166]
[The 3rd operation gestalt]
Below, the 3rd operation gestalt of this invention is explained, referring to drawing 12 . Drawing 12 is drawing of drawing 8 and this meaning, and the formation modes of a frame pattern differ here. However, unlike drawing 8 , in drawing 12 , the graphic display about the capacity wiring 400 is also omitted. In addition, about almost all parts, such as the whole electro-optic device configuration of the 1st operation gestalt mentioned above with the 3rd operation gestalt, and a configuration of a picture element part, it is completely the same. Therefore, below, the explanation about the same part as the 1st operation gestalt is omitted, and suppose that explanation is mainly added only about a configuration characteristic of the 3rd operation gestalt.
[0167]
In drawing 12 , the frame pattern 462 which consists of frame patterns 462C and 462D is formed. Among these, frame pattern 462C corresponds to an example of the "3rd pattern" said to this invention, and as shown in drawing 12 , it is formed along with two sides (left part in drawing, and right-hand side) to which image display field 10a which has the shape of a rectangle corresponds. Moreover, frame pattern 462D corresponds to an example of the "4th pattern" said to this invention, and it divides with aforementioned frame pattern 462C, and it is formed while being formed along with two sides (drawing Nakagami side and lower side) in which image display field 10a remains (sign 462G in drawing reference).
[0168]
And the vertical flow material 106 exists on frame pattern 462C among these.
[0169]
According to such a gestalt, along with the left part and the right-hand side of image display field 10a, two vertical flow material 106 exists at a time in frame pattern 462C formed as a two straight-lines-like pattern among drawing 12 , respectively. Therefore, since it can say that redundancy-structure is taken like the 1st operation gestalt about this point, the electrical installation between the frame pattern 462 and a counterelectrode 21 can be made more certainly.
[0170]
Moreover, according to frame pattern 462D, generating of capacity coupling between the drawer wiring 116 and a counterelectrode 21 can be prevented as much as possible like frame pattern 461B of said 2nd operation gestalt.
[0171]
Of course, it is the same as that of the above-mentioned 1st operation gestalt that the operation effectiveness of optical leakage prevention is acquired by existence of the frame patterns 462C and 462D.
[0172]

[The 4th operation gestalt]
Below, the 4th operation gestalt of this invention is explained, referring to drawing 13 . Drawing 13 is drawing of drawing 8 and this meaning, and the formation modes of a frame pattern differ here. However, unlike drawing 8 , in drawing 13 , the graphic display about the capacity wiring 400 is also omitted. In addition, about almost all parts, such as the whole electro-optic device configuration of the 1st operation gestalt mentioned above with the 4th operation gestalt, and a configuration of a picture element part, it is completely the same. Therefore, below, the explanation about the same part as the 1st operation gestalt is omitted, and suppose that explanation is mainly added only about a configuration characteristic of the 4th operation gestalt.
[0173]
In drawing 13 , the frame pattern 463 which consists of frame patterns 463E and 463F is formed. Among these, frame pattern 463E corresponds to an example of the "5th pattern" said to this invention, and as shown in drawing 13 , it is continuously formed except for the part corresponding to one corner of image display field 10a which has the shape of a rectangle. Moreover, frame pattern 463F correspond to an example of the "6th pattern" said to this invention, and it divides with said frame pattern 463E, and they are formed while being formed in the part corresponding to said one corner (sign 463G in drawing reference). And the vertical flow material 106 exists in any [of the frame patterns 463E and 463F] top among these.
[0174]
According to such a gestalt, it is clear generating suppression of capacity coupling between the soundness of the electrical installation between the said 1st [the] to 3rd operation gestalt and the same operation effectiveness 463 as abbreviation, i.e., a frame pattern, and a counterelectrode 21 or the drawer wiring 116, and a counterelectrode 21 and to be obtained still like abbreviation of the operation effectiveness, such as optical leakage prevention.
[0175]
[The 5th operation gestalt]
Below, the 5th operation gestalt of this invention is explained, referring to drawing 14 . Drawing 14 is drawing of drawing 8 and this meaning, and the formation modes of a frame pattern etc. differ here. In addition, about almost all parts, such as the whole electro-optic device configuration of the 1st operation gestalt mentioned above with the 5th operation gestalt, and a configuration of a picture element part, it is completely the same. Therefore, below, the explanation about the same part as the 1st operation gestalt is omitted, and suppose that explanation is mainly added only about a configuration characteristic of the 5th operation gestalt.
[0176]
First, in drawing 14 , the frame pattern 464 which has the above-mentioned 4th operation gestalt and the same pattern configuration as abbreviation is formed. That is, the frame pattern 464 consists of frame pattern 464F formed in the part corresponding to frame pattern 464E formed in continuation except for one corner of image display field 10a, and said one corner.
[0177]
Moreover, it is the same as that of the above-mentioned 4th operation gestalt to connect with specific external circuit connection terminal 102Q of some of that the wiring 404 for supplying potential to that three and one vertical flow material 106 are formed and this vertical flow material 106, respectively is formed in these frame patterns 464E and 464F and these wiring 404. However, especially the wiring 404 concerning the 5th operation gestalt corresponds to an example "for part I of the 2nd wiring said to this invention", and specific external circuit connection terminal 102Q corresponds to an example "for part I of an external circuit connection terminal said to this invention."
[0178]
And in the 5th operation gestalt, these frame patterns 464E and 464F are not connected to capacity wiring and an electric target. That is, although formed as the same film, the frame pattern 464 and capacity wiring 400' are formed so that it may be divided on patterning (sign 46G in drawing reference). And wiring 408 is installed in capacity wiring 400' which cannot receive supply of potential from the

frame pattern 464 in this way. This wiring 408 corresponds to an example "for part II of the 2nd wiring said to this invention", escapes from between gap 464G which divide the frame patterns 464E and 464F, and is connected to specific external circuit connection terminal 102R (it corresponds to an example "for part II of an external circuit connection terminal said to this invention".).

[0179]

When the above is summarized, with the 5th operation gestalt wiring 404, the frame pattern 464, wiring 408, and capacity wiring 400' Although all are formed as the same film (the 3rd junction electrode 402 is included, of course.) Although electrical installation is planned about each between wiring 404 and the frame pattern 464 and between wiring 408 and capacity wiring 400', electric communication is not made between the former and the latter.

[0180]

According to such a gestalt, the potential given to a counterelectrode 21, and capacity wiring 400', as a result the capacity electrode 300 can be changed. That is, since it connects with the frame pattern 464, wiring 404, and specific external circuit connection terminal 102Q through the vertical flow material 106, a counterelectrode 21 can maintain a counterelectrode 21 to the potential concerned, if the potential for counterelectrode 21 is supplied to this external circuit connection terminal 102Q. Since it connects with wiring 408 and specific external circuit connection terminal 102R, the capacity electrode 300 (refer to drawing 6) electrically connected to capacity wiring 400', as a result this on the other hand can maintain this capacity electrode 300 to the potential concerned, if different potential for capacity electrode 300 from the potential for said counterelectrode 21 is supplied to this external circuit connection terminal 102R. thus -- according to the 5th operation gestalt -- a counterelectrode 21 and the capacity electrode 300 -- since each is maintainable to different potential, it can perform adjusting suitably various kinds of electric operations generated within the electro-optic device concerned etc.

[0181]

In addition, also in the 5th operation gestalt, it is unchanging from the above 1st like the 4th operation gestalt to being [of capacity coupling generating between reservation of the positive electrical installation between the frame pattern 464 and a counterelectrode 21 or the picture signal line 115, and a counterelectrode 21] control, and optical leakage prevention etc. being still more possible.

[0182]

In addition, it is necessary to supply potential common to a counterelectrode 21 and the capacity wiring 400, or the capacity electrode 300 to specific external circuit connection terminal 102Q from the capacity wiring 400 being electrically connected to the frame patterns 461, 462, and 463 in the 4th operation gestalt at the vertical flow material 106 and counterelectrode 21 list from the above 2nd. However, this invention is not limited to such a gestalt. That is, you may make it supply separately from the potential for counterelectrode 21 the potential the capacity wiring 400 or for capacity electrode 300 using the gaps 461G, 462G, and 463G which constitute the frame patterns 461, 462, and 463 from the above 2nd also in the 4th operation gestalt, as stated as the 5th operation gestalt.

[0183]

Moreover, the potential supplied to specific external circuit connection terminal 102Q or 102R in the 5th operation gestalt from the above 1st may be used as constant potential by the side of the low voltage supplied by the scanning-line actuation circuit 104. According to this, the potential of a counterelectrode 21 and the capacity electrode 300 becomes the same as the constant potential concerned. Or it may replace with the above configurations again and the potential supplied to external circuit connection terminal 102Q or 102R may be used as constant potential supplied by the data-line actuation circuit 101.

[0184]

(Electronic equipment)

Next, the whole configuration and especially an optical configuration are explained about the operation gestalt of an example slack projection mold electrochromatic display of electronic equipment using the electro-optic device explained to the detail above as a light valve. Drawing 15 is the diagrammatic sectional view of a projection mold electrochromatic display here.

[0185]
In drawing 15 , an example slack liquid crystal projector 1100 of the projection mold electrochromatic display in this operation gestalt prepares three liquid crystal modules containing the liquid crystal equipment with which the actuation circuit was carried on the TFT array substrate, and is constituted as a projector used as light valves 100R, 100G, and 100B for RGB, respectively. In a liquid crystal projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB by three mirrors 1106 and two impounding basin lock mirrors 1108, and will be led to the light valves 100R, 100G, and 100B corresponding to each color, respectively. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors modulated with light valves 100R, 100G, and 100B, respectively is again compounded by the impounding basin lock prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.
[0186]
This invention is not restricted to the operation gestalt mentioned above, and can be suitably changed in the range which is not contrary to the summary of invention which can be read in a claim and the whole description, or thought, and the electro-optic device and electronic equipment accompanied by such modification are also contained in the technical range of this invention.
[Brief Description of the Drawings]
[0187]
[Drawing 1] It is the top view of the electro-optic device which looked at the TFT array substrate from the opposite substrate side with each component formed on it.
[Drawing 2] It is the H-H' sectional view of drawing 1 .
[Drawing 3] They are equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of an electro-optic device] a matrix, and wiring.
[Drawing 4] It is the top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other, and only the configuration concerning a lower layer part (lower layer part to the sign 70 (storage capacitance) in drawing 6) is shown.
[Drawing 5] It is the top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other, and only the configuration concerning a part for a management (the sign 70 (storage capacitance) in drawing 6 is exceeded, and it is the upper part) is shown.
[Drawing 6] It is an A-A'sectional view at the time of piling up drawing 4 and drawing 5.
[Drawing 7] It is a sectional view corresponding to the laminated structure shown in drawing 6, and the enlarged drawing for the interior of a circle to which (a) gave the sign Z in drawing 2, and (b) are the enlarged drawings for the interior of a circle which attached the sign S in drawing 2.
[Drawing 8] It is drawing of drawing 1 and this meaning, and in order to explain the configuration of a frame pattern, capacity wiring, etc. especially, the arrangement relation of both elements is illustrated clearly.
[Drawing 9] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 2nd operation gestalt of this invention is shown.
[Drawing 10] It is the explanatory view in which expanding near sign D shown in drawing 9, and showing the circuitry in the part concerned etc. collectively.
[Drawing 11] It is drawing of drawing 10 and this meaning, and that from which the formation mode of a frame pattern differs is shown.
[Drawing 12] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 3rd operation gestalt of this invention is shown.
[Drawing 13] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning

the electro-optic device of the 4th operation gestalt of this invention is shown.
[Drawing 14] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 5th operation gestalt of this invention is shown.
[Drawing 15] It is the top view of the projection mold liquid crystal equipment concerning each operation gestalt of this invention.
[Description of Notations]
[0188]
10 ... A TFT array substrate, 10a ... An image display field, 3a ... Scanning line, 6a [... Storage capacitance,] ... The data line, 30 ... TFT, 9a ... A pixel electrode, 70 300 ... A capacity electrode, 400 ... Capacity wiring (the 1st wiring), 406, 461, 462, 463, 464 ... Frame pattern, 404 408 [... An external circuit connection terminal, 106 / ... Vertical flow material, 20 / ... An opposite substrate, 21 / ... A counterelectrode, 53 / ... Frame light-shielding film.] ... Wiring (the 2nd wiring), 101 ... A data-line actuation circuit, 104 ... A scanning-line actuation circuit, 102

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[0187]
[Drawing 1] It is the top view of the electro-optic device which looked at the TFT array substrate from the opposite substrate side with each component formed on it.
[Drawing 2] It is the H-H' sectional view of drawing 1 .
[Drawing 3] They are equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of an electro-optic device] a matrix, and wiring.
[Drawing 4] It is the top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other, and only the configuration concerning a lower layer part (lower layer part to the sign 70 (storage capacitance) in drawing 6) is shown.
[Drawing 5] It is the top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other, and only the configuration concerning a part for a management (the sign 70 (storage capacitance) in drawing 6 is exceeded, and it is the upper part) is shown.
[Drawing 6] It is an A-A'sectional view at the time of piling up drawing 4 and drawing 5 .
[Drawing 7] It is a sectional view corresponding to the laminated structure shown in drawing 6 , and the enlarged drawing for the interior of a circle to which (a) gave the sign Z in drawing 2 , and (b) are the enlarged drawings for the interior of a circle which attached the sign S in drawing 2 .
[Drawing 8] It is drawing of drawing 1 and this meaning, and in order to explain the configuration of a frame pattern, capacity wiring, etc. especially, the arrangement relation of both elements is illustrated clearly.
[Drawing 9] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 2nd operation gestalt of this invention is shown.
[Drawing 10] It is the explanatory view in which expanding near sign D shown in drawing 9 , and showing the circuitry in the part concerned etc. collectively.
[Drawing 11] It is drawing of drawing 10 and this meaning, and that from which the formation mode of a frame pattern differs is shown.
[Drawing 12] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 3rd operation gestalt of this invention is shown.
[Drawing 13] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 4th operation gestalt of this invention is shown.
[Drawing 14] It is drawing of drawing 8 and this meaning, and the mode of the frame pattern concerning the electro-optic device of the 5th operation gestalt of this invention is shown.
[Drawing 15] It is the top view of the projection mold liquid crystal equipment concerning each operation gestalt of this invention.

[Translation done.]

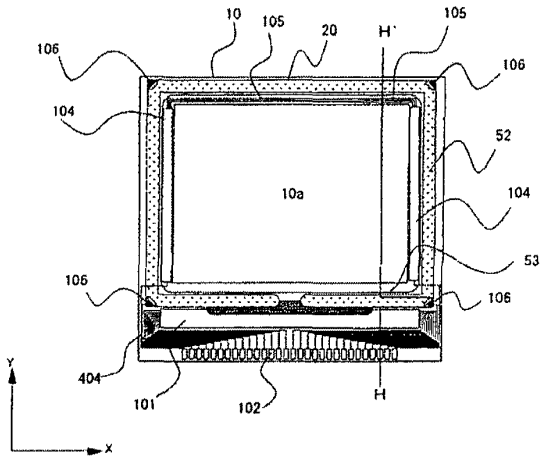
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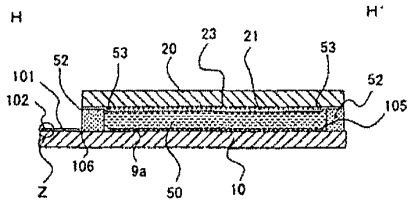
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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

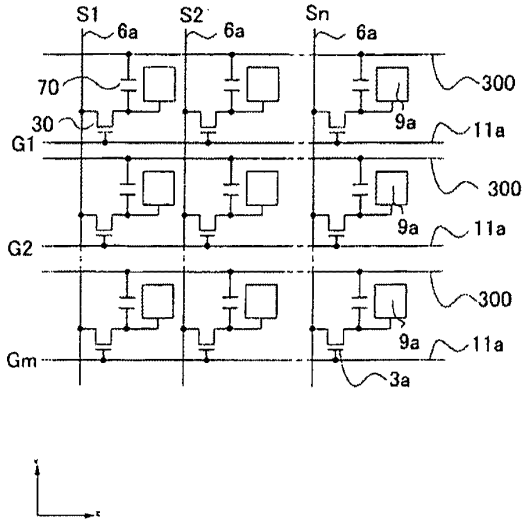
[Drawing 1]



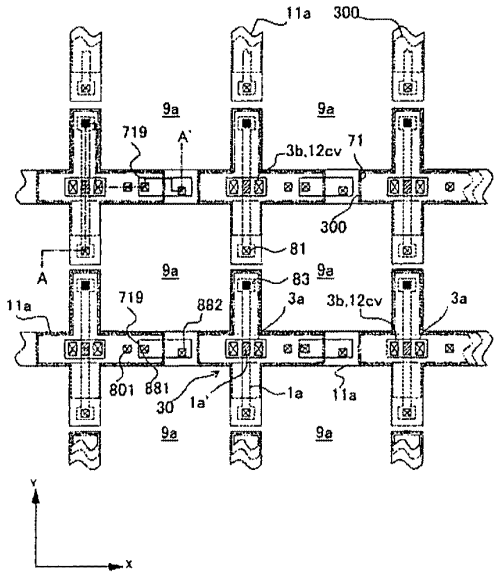
[Drawing 2]



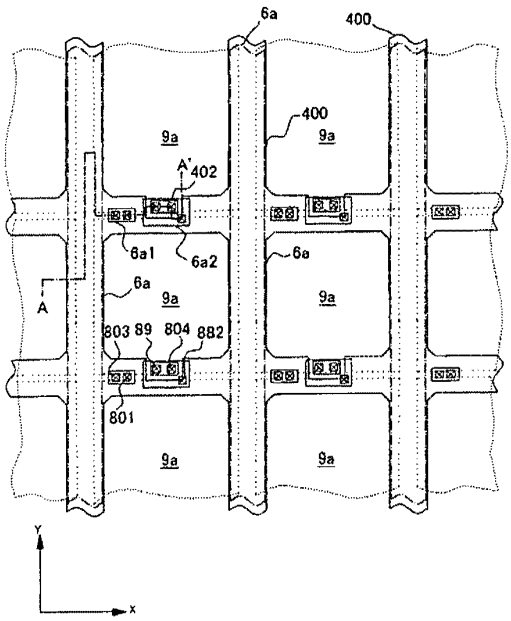
[Drawing 3]



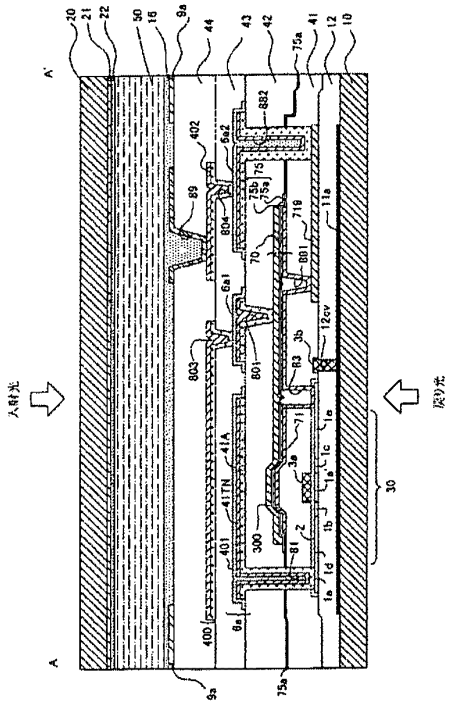
[Drawing 4]



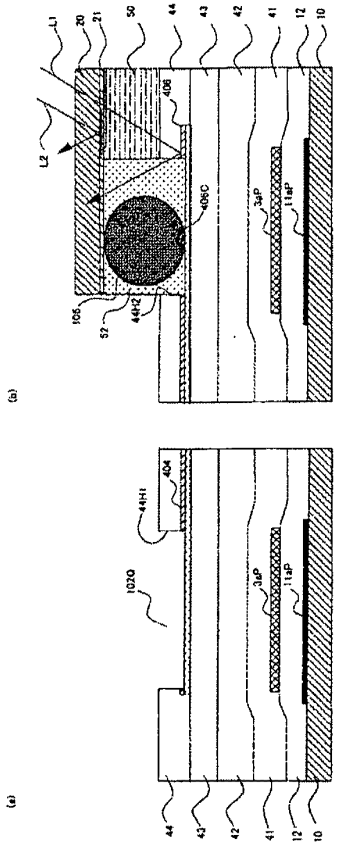
[Drawing 5]



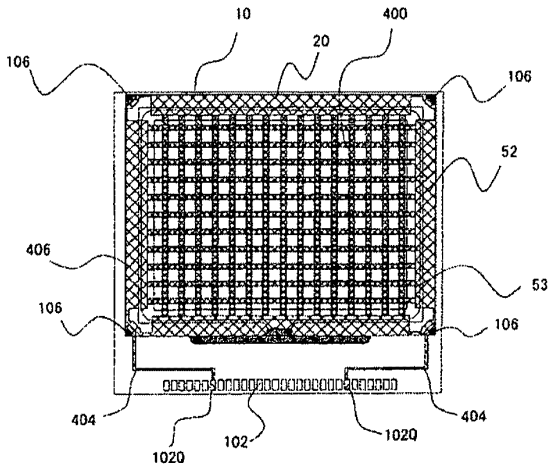
[Drawing 6]



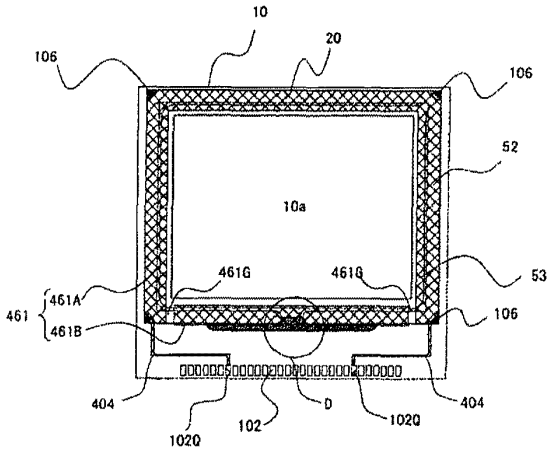
[Drawing 7]



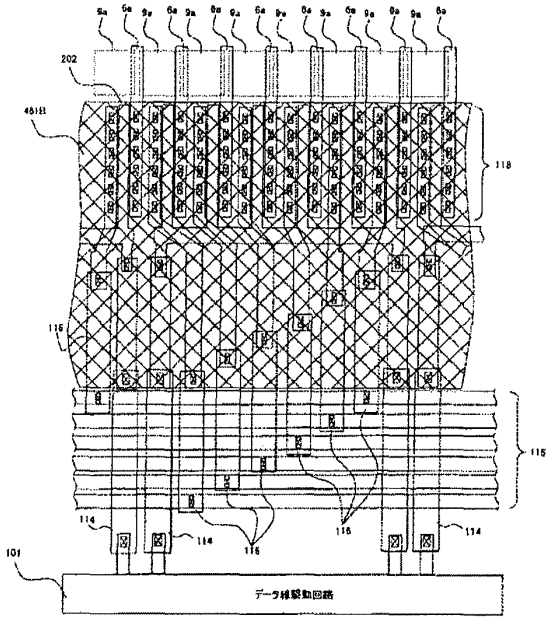
[Drawing 8]



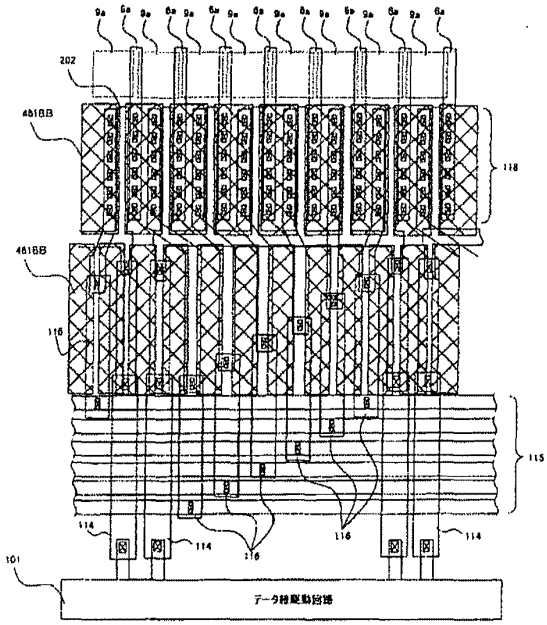
[Drawing 9]



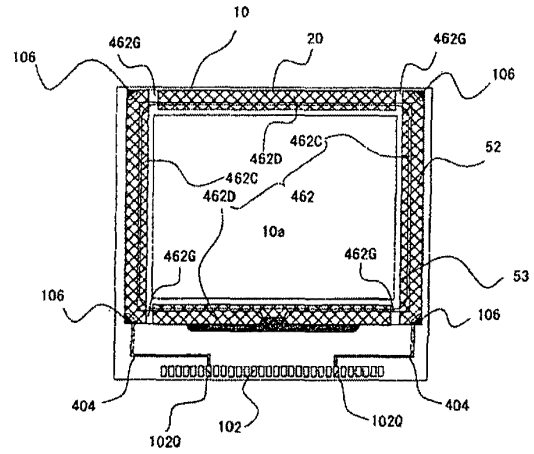
[Drawing 10]



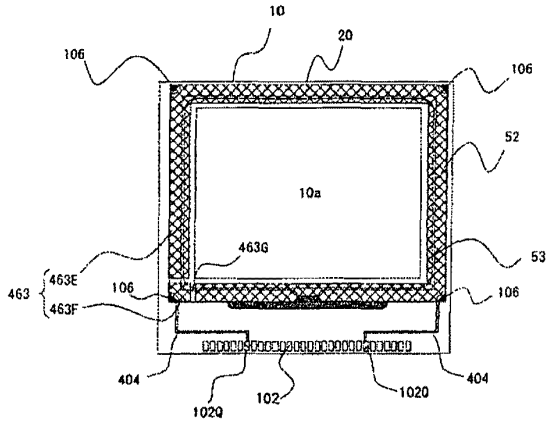
[Drawing 11]



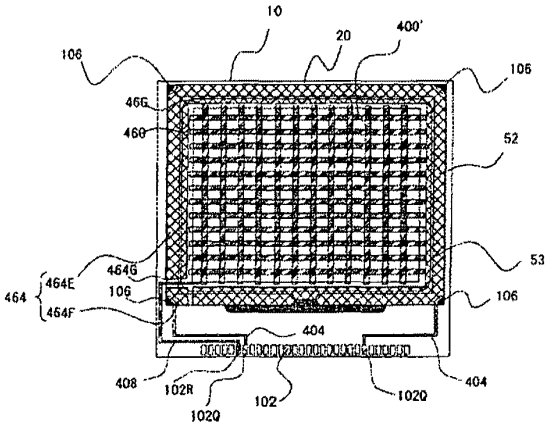
[Drawing 12]



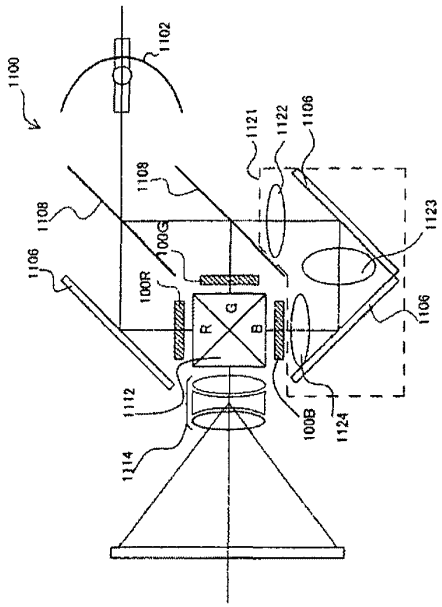
[Drawing 13]



[Drawing 14]



[Drawing 15]



[Translation done.]

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OIPE IAP38 JAN 24 2007 PATENT & TRADEMARK OFFICE

English Translation of Abctract of Korean Patent Laid-Open No. 1999-009398

Abstract

The present invention relates to a liquid crystal display (LCD) device wherein, in case of a COG (Chip On Glass)-type LCD device, an input line, which is connected to a driving IC, is directly mounted to a bottom plate.

The unit cost of production of a LCD device used to be expensive since the input lines were formed in FPC. For this reason, the above LCD device wherein the input line is directly mounted to a bottom plate was invented, wherein the input line and said driving IC were connected by a draw out line.

However, in the LCD device wherein the input line is directly mounted to the bottom plate, the signal is delayed due to the capacitance on the insulating film, which is formed in the layer between the the input line and the draw out line.

The present invention can prevent the delay of the signal by insulating the layer between the input line and the draw out line with an organic insulating film, which has a low dielectric constant, and reducing the capacitance.

In the present invention, the unit cost of production of a LCD device is reduced since the above-mentioned FPC is less more used, and a high quality LCD device is realized since the delay of the signal is reduced when compared to that of a LCD device wherein the layer between an input line and a draw out line is insulated by an inorganic layer, due to the reduction of capacitance between the input line and the draw out line.

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심사청구 : 있음

(54) 액정표시장치의 테이터 연가부의 구조

요약

본 발명은 COB(Chip On Glass)방식의 액정표시장치에서 구동IC에 연결되는 입력배선을 하판에 직접 실장시킨 액정표시장치에 관한 것이다.

종래에는 상기 입력배선이 FPC에 형성되어 액정표시장치의 제조시, 제조단가가 높았다. 그래서, 상기 입력배선이 하판에 직접 실장된 액정표시장치를 개발했었다. 그리고, 상기 입력배선과 구동IC 사이를 인출선으로 연결했었다.

그러나, 상기 입력배선이 하판에 직접 실장된 액정표시장치는 상기 입력배선과 인출선 사이의 층에 형성된 절연막에 발생하는 기생용량으로 인해 신호의 지연현상이 일어나는 문제점이 있었다.

본 발명은 상기 입력배선과 인출선 사이의 층을 유전율이 낮은 유기절연막으로 절연시킴으로써 상기 기생용량을 줄여 신호의 지연현상을 방지할 수 있다.

본 발명은 상기 FPC의 사용량이 줄어 종래의 액정표시장치보다 제조단가가 낮아지고, 상기 입력배선과 인출선 사이의 기생용량이 줄어 입력배선과 인출선 사이를 무기막으로 절연시킨 경우의 액정표시장치보다 신호의 지연현상이 줄어드므로, 고화질의 액정표시장치를 구현할 수 있다.

대표도

도3a

명세서

도면의 간단한 설명

도 1은 일반적인 COB(Chip On Glass) 방식의 액정표시장치를 나타낸 것이다.

도 2는 구동IC의 입력배선이 형성된 FPC를 나타낸 것이다.

도 3은 L자형의 FPC를 나타낸 것이다.

도 4는 구동IC의 입력배선이 하판에 직접 실장된 종래의 COB방식의 액정표시장치를 나타낸 것이다.

도 5는 도 4의 액정표시장치의 입력배선과 인출선 사이의 단면을 나타낸 것이다.

도 6은 입력배선과 인출선 사이가 유기절연막으로 코팅된 본 발명의 액정표시장치의 일부 단면을 나타낸 것이다.

도 7은 본 발명의 액정표시장치의 개략적인 구조를 나타낸 평면도이다.

도 8은 본 발명의 액정표시장치의 신호선입력배선과 신호인출선이 형성된 부분의 단면을 참조로 본 발명의 액정표시장치를 제조하는 방법을 나타낸 것이다.

도 9는 본 발명의 액정표시장치의 주사선입력배선과 주사인출선이 형성된 부분의 단면을 참조로 본 발명의 액정표시장치를 제조하는 방법을 나타낸 것이다.

도 10은 본 발명의 실시예 2의 제조방법을 나타낸 단면도이다.

도 11은 본 발명의 실시예 2의 제조방법을 나타낸 평면도이다.

도 12는 본 발명의 실시예 3의 제조방법을 나타낸 단면도이다.

도 13은 본 발명의 실시예 3의 제조방법을 나타낸 평면도이다.

도면의 기호설명

10 : 상판11 : 하판12 : 제1영역

13 : 제2영역14 : 주사선구동IC15 : 신호선구동IC

16 : 입력배선17 : 입력단자18 : 출력단자

19 : 회로기판20 : 데이터전송선21 : FPC

22 : 주사선23 : 신호선30 : L자형의 FPC

31 : 직사각형의 FPC40 : ITO(인출선)50 : 게이트금속(추가배선)

51 : 게이트절연막52 : 소스, 드레인금속(인출선)

53 : 보호막55 : 구동IC패드56 : 추가배선

100: 신호선구동입력배선110 : 신호입력추가배선(게이트금속)

120 : 게이트출선130 : 유기절연막(BCB)140 : 신호입력전극

150 : 신호인출선160 : 접촉홀(contact hole)

200 : PCB기판210 : 데이터전송선230 : 하판

240 : 신호선구동IC250 : 표시영역

300 : 주사선310 : 신호선320 : 화소

400 : 주사선구동입력배선 410 : 주사입력추가배선(게이트금속)

440 : 주사선구동IC450 : 주사인출선470 : 주사입력전극

500 : 기판510 : 입력배선

520 : 접촉구멍(contact hole)

530 : 인출선540 : 절연막

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 COB(Chip On Blass) 방식의 액정표시장치에서 신호선구동입력배선과 신호선구동IC의 인출입력선 사이에 유기막을 형성시켜 상기 신호선구동입력배선과 상기 인출입력선 사이에 형성되는 기생용량(Capacitance)에 의한 신호지연을 감소시키는 데에 그 특징이 있다.

일반적인 표시장치로서 사용되는 CRT브라운관은 RGB 전자총에 의해 영상을 표시하는 방법을 사용한다. 그러나, CRT브라운관은 표시영역을 크게하려면 필연적으로 두께를 증가시켜야 한다는 단점이 있다. 그 이유는 전자총과 브라운관의 표면 사이의 거리가 충분히 확보되어야만 화면에 영상을 표시할 수 있기 때문이다.

그래서, 이러한 CRT브라운관을 대체하는 표시장치들이 개발 중에 있는데, 그중 액정표시장치는 CRT브라운관을 대체하는 표시장치로서 가장 가까이 실용화단계에 접근해 있다.

액정표시장치는 액정패널과 구동IC의 접착방법에 따라 TAB방식의 액정표시장치와 COB방식의 액정표시장치로 구분지을 수 있다. 종래에는 TAB방식의 액정표시장치가 주류를 이루었으나, 제작기술의 발달에 따라 COB방식의 액정표시장치도 많이 개발되고 있다.

일반적인 COB방식의 액정표시장치는 도 1에 나타낸 것과 같이 투명기판으로 형성된 상판(10)과 하판(11)으로 구성되어 있다. 도면에는 도시되지 않았지만, 상기 상판은 한쪽면에 편광판이 부착되어 있고, 반대면에는 칼라필터와 공통전극이 형성되어 있다. 그리고, 상기 하판은 도면에는 도시되지 않았지만, 한쪽면에 편광판이 부착되어 있고, 상기 상판보다 조금 더 넓다. 상기 하판은 편광판이 부착되지 않은 면이 상기 상판의 공통전극과 대향하도록 맞붙어 있다.

상기 하판은 상기 상판에 대응하는 제1영역(12)과 상판에 대응하지 않는 제2영역(13)으로 구분지을 수 있다. 상기 제1영역에는 주사선(22)과 신호선(23)이 서로 직교하며 형성되어 있다. 그리고, 상기 제2영역(13)에는 상기 주사선(22)에 연결된 주사선구동IC(14)와 상기 신호선(23)에 연결된 신호선구동IC(15)가 부착되어 있다.

상기 신호선구동IC(15)는 입력단자(17)와 출력단자(18)로 구성되어 있다. 상기 입력단자는 R(Red)단자 6개와, G(Green)단자 6개, 및 B(Blue)단자 6개와, SSC(Shift Start Clock)단자와, SSP(Shift Start Pulse)단자와 LP(Latch Pulse)단자와, 감마(Gamma) 입력선 9개와, 아날로그 접지단자와, 디지탈 접지단자와,

디지탈 전압의 3.3V 전원단자와, 아날로그 전압의 4.2V 전원단자와, 공통전압단자(Vcom)와 음전전압단자(Vst)와, 데이터입력단자(Din)단자 등으로 구성되어 있다. 상기 각 단자들은 때에 따라 개수의 증감이 있을 수 있다. 그리고, 상기 출력단자(18)는 상기 신호선(23)에 하나씩 연결되어 있다. 일반적으로 하나의 신호선구동IC(15)에 약 80개~100개의 출력단자가 있다.

그리고, 상기 액정표시장치는 하판의 외부에 따라 설치된 PCB 회로기판(19)과 상기 입력단자를 연결하기 위하여 데이터전송선(connection cable)(20)과 FPC(Flexible Printed Circuit)(21)를 이용하였다. 상기 FPC(21)에는 신호선구동IC와 주사선구동IC의 입력단자에 연결되는 입력배선(16)이 형성되어 있다. 도 1은 PCB기판(19)과 FPC(21)가 데이터전송선(20)으로 연결되어 있고, 상기 FPC(21)와 신호선구동IC의 입력단자(17)가 연결된 액정표시장치를 나타낸 것이다.

설명이 어루고자 하는 기술적 과제

그런데, 도 1에 나타낸 액정표시장치는 제작시 상당한 양의 FPC가 필요하다. 왜냐하면, 도 2에 나타낸 것과 같이 상기 신호선구동IC의 입력단자에 각각 연결되는 입력배선(16)이 서로 단락되지 않으려면, 상기 FPC(21)의 폭이 넓어야 하기 때문이다.

그래서, 도 4에 나타낸 것과 같이 상기 FPC에 형성되었던 입력배선이 상기 하판의 제2영역에 형성된 액정표시장치가 고안되었다.

그런데, 상기 도 4의 액정표시장치는 입력배선(16)에 IC를 연결하기 위한 인출선(40)과 상기 입력배선(16)이 중첩되므로, 상기 중첩되는 부위는 반드시 절연막으로 분리되어야 한다. 이 때, 상기 중첩되는 부위의 단면은 도 5a, 도 5b와 같다. 상기 도 5a는 신호선입력배선과 신호인출선 사이의 단면을 나타낸 것이고, 도 5b는 주사선입력배선과 주사인출선 사이의 단면을 나타낸 것이다. 상기 중첩되는 부위는 상기 입력배선(16)의 게이트금속(50)과 인출선(52, 40) 사이에 절연막(51)이 끼워진 모양이 된다. 이 때, 상기 입력배선(16, 50)과 인출선(52)은 캐패시터(capacitor)의 전극에 대응되고, 상기 절연막(51)은 유전체에 대응되는 기생용량(capacitance)이 발생된다. 상기 기생용량은 상기 입력배선에 인가되는 신호의 지연 현상을 일으키게 되고, 상기 지연 현상에 의해 신호의 왜곡이 발생된다.

그러므로, 상기 입력배선을 하판에 직접 설장하였을 때, 입력배선과 인출선 사이의 기생용량을 줄일 수 있어야 한다.

발명의 구성 및 작용

본 발명은 도 4에 나타낸 액정표시장치에서 발생하는 신호의 지연현상을 감소시키기 위해 도 6에 나타낸 것과 같이 입력배선(100)과 인출선(150) 사이를 유기재료(130)로 절연시킨 액정표시장치이다. 도 6a는 신호선입력배선과 신호인출선 사이의 단면을 나타낸 것이고, 도 6b는 주사선입력배선과 주사인출선 사이의 단면을 나타낸 것이다.

도 7을 참조로 본 발명의 액정표시장치의 구조를 설명하면 다음과 같다. 본 발명의 액정표시장치는 열(列 : row)방향으로 연속하여 형성된 복수개의 주사선(300)과, 행(行 : column)방향으로 연속하여 형성된 복수개의 신호선(310)이 직교하고, 그 교차부에 화소(畵素 : pixel)(320)가 형성된 표시영역과; 상기 주사선과 평행하게 형성되고, 한쪽 끝단은 외부 데이터전송선(210)에 연결되고, 상기 데이터전송선으로부터 신호선구동입력신호를 인가받는 신호선구동입력배선(100)과; 상기 신호선구동입력배선의 일부에 적층된 유기절연막(도 8의 130)과; 상기 유기절연막 위에 형성되어 상기 신호선의 한쪽 끝단에 연결된 출력전극과 상기 신호선구동입력배선에서 분기된 신호인출선(150)과; 상기 신호인출선에 연결된 입력전극(140)으로 구성된 신호선구동IC(240)와; 상기 신호선과 평행하게 형성되고, 한쪽 끝단은 외부 데이터전송선(210)에 연결되고, 상기 데이터전송선으로부터 주사선구동입력신호를 인가받는 주사선구동입력배선(400)과; 상기 주사선구동입력배선의 일부에 적층된 유기절연막(도 9의 130)과; 상기 유기절연막 위에 형성되어 상기 신호선의 한쪽 끝단에 연결된 출력전극과 상기 주사선구동입력배선에서 분기된 주사인출선(450)과; 상기 주사인출선에 연결된 입력전극(470)으로 구성된 주사선구동IC(440)를 구비하여 형성되어 있다. 이때, 상기 유기절연막은 상기 주사선구동입력배선과 주사인출선과의 교차부 및 상기 신호선구동입력배선과 신호인출선과의 교차부에 형성된다. 상기 유기절연막의 재료로는 BCB(Benzo Cyclo Butene)와 같은 감광물을 사용할 수 있다. 본 발명의 제조방법은 다음과 같다.

[실시예 1]

상기 도 7의 A-A'부분의 단면을 참조로 본 실시예는 도 8에 나타낸 것과 같다. 하판 위에 복수개의 신호선구동입력배선(100)과 신호입력추가배선(110)이 차례로 적층되고 그 위에 게이트절연막(120)이 증착된다(도 8a). 그리고, 상기 게이트절연막(120) 위에 신호선구동IC의 입력전극에 연결되는 신호입력패드(140)가 형성된다. 상기 신호입력패드(140)와 상기 게이트절연막(120) 위의 전부에 유기절연막(130)이 코팅되어 평평한 표면을 형성한다(도 8b). 그리고, 상기 신호선구동입력배선 중, 신호선구동IC의 입력전극에 연결되는 신호선구동입력배선 위의 게이트절연막(120)과 유기절연막(130)을 에칭하여 접속홀(contact hole)(160)을 뚫는다. 동시에 상기 신호입력 패드의 유기절연막도 에칭하여 접속홀(contact hole)(160)을 뚫는다(도 8c). 그리고, 상기 유기절연막 위에 금속이나, ITO를 증착하고, 상기 신호입력패드와 상기 접속홀로 인해 노출된 신호선구동입력배선이 연결되도록 상기 신호인출선(150)을 패터닝한다(도 8d). 그래서, 상기 신호선구동IC의 입력전극과 상기 접속홀을 통해 신호선구동입력배선(100)이 연결되도록 한다.

상기 도 7의 B-B'의 단면도를 참조로 본 발명의 제조방법을 나타내면 도 9에 나타낸 것과 같다. 하판 위에 복수개의 주사선구동입력배선(400)과 주사입력추가배선(140)이 차례로 형성되고, 동시에 주사선구동IC의 입력전극에 연결되는 주사입력패드(470)가 형성된다. 그리고, 상기 주사선구동입력배선과 주사입력패드 위에 게이트절연막(120)이 증착된다(도 9a). 상기 게이트절연막 위에 유기절연막(130)이 코팅되어 평평하게 된다(도 9b). 그리고, 상기 주사선구동입력배선 중, 주사선구동IC의 입력전극에 연결되는 주사선구동입력배선(140)과 상기 주사입력패드 위의 게이트절연막(120)과 유기절연막(130)을 에칭하여 접속홀(contact hole)(160)을 뚫는다(도 9c). 그리고, 상기 유기절연막 위에 금속이나, ITO를 증착하고, 상기

주사입력패드(140)와 상기 접촉홀을 통해 주사선구동입력배선(400)이 연결되도록 상기 주사인출선(450)을 형성하도록 패터닝한다(도 9d). 그러서, 상기 주사선구동IC의 입력전극과 상기 접촉홀을 통해 주사선구동입력배선(400)이 연결되도록 한다.

[실시예 2]

본 발명은 입력배선(510)과 인출선(530) 및 유기절연막(540)을 형성하는 단계의 순서에 따라 여러 방법으로 제조될 수 있다. 도 11은 상기 입력배선이 형성되는 하판의 평면도이고, 도 10은 상기 도 11의 A-A'을 자른 단면도이다. 먼저 하판(500) 위에 게이트금속으로 입력배선(510)을 형성한다(도 10a, 도 11a). 그리고, 상기 입력배선(510) 위에 BCB로 된 유기절연막(540)을 입고, 상기 입력배선(510)에서 인출선(530)이 형성될 부분에 접촉홀(contact hole)(520)을 형성한다.(도 10b, 도 11b) 그리고, 상기 접촉홀(520)에 의해 노출된 입력배선(510)의 일부분과 상기 유기절연막(540) 위에 인출선(530)을 형성한다.(도 10c, 도 11c) 상기 입력배선은 액정패널의 주사선과 동시에 형성될 수 있도록 게이트금속을 사용해도 되나, 신호선과 동시에 형성될 수 있도록 소스, 드레인 금속 혹은, ITO로 형성해도 된다.

상기 공정은 액정패널의 박막트랜지스터 공정과 동시에 진행될 수 있으므로, 유기절연막을 증착하기 전에, 게이트절연막이 먼저 증착될 수 있다. 그리고, 상기 게이트절연막 위에 IC의 입력전극과 연결되는 패드가 형성된다.

[실시예 3]

상기 실시예 1과 2는 입력배선이 먼저 형성되고, 나중에 인출선이 형성되었으나, 인출선이 먼저 형성될 수도 있다. 도 12은 상기 인출선이 형성되는 하판의 평면도이고, 도 13은 상기 하판의 B-B'을 자른 단면도이다. 먼저 하판에 금속으로 인출선(530)을 형성한다.(도 12a, 도 13a) 그리고, 상기 인출선(530) 위에 BCB로 된 유기절연막(540)을 적층하고, 인출선에서 추후 입력배선과 연결될 부분에 접촉홀(520)을 형성한다.(도 12b, 도 13b) 그리고, 상기 접촉홀에 의해 노출된 인출선의 일부분과 상기 유기절연막(540) 위에 입력배선(510)을 형성한다(도 12c, 도 13c).

상기 공정은 액정패널의 박막트랜지스터 공정과 동시에 진행될 수 있으므로, 유기절연막을 증착하기 전에, 게이트절연막이 먼저 증착될 수 있다. 그리고, 상기 게이트절연막 위에 IC의 입력전극과 연결되는 패드가 형성된다.

발명의 효과

종래의 액정표시장치는 주사선구동IC와 신호선구동IC의 입력배선이 FPC에 형성됨으로 인해 상당한 양의 FPC가 필요하여 제조비용이 높았었다. 그래서, 상기 FPC의 사용량을 줄이는 노력의 일환으로 상기 입력배선이 하판에 직접 실장된 액정표시장치를 개발했다. 그러나, 상기 입력배선이 하판에 직접 실장된 액정표시장치는 FPC의 사용이 줄어들어 단가는 낮출 수 있으나, 상기 입력배선과 인출선 사이의 절연막에 존재하는 기생용량으로 인하여 신호지연이 일어나는 단점이 있었다.

본 발명은 입력배선과 인출선의 교차부에 유전율이 낮은 유기재료로 절연막을 형성함으로써 상기 기생용량을 줄일 수 있다. 그래서, 신호지연이 종래보다 줄어든다는 장점이 있다. 그리고, 구동IC의 입력배선이 하판에 직접 실장됨으로 인해 FPC의 사용량이 줄어들어 액정표시장치의 제조비용이 낮아지는 장점도 있다. 뿐만 아니라, 유기절연막이 평평하게 코팅되므로, 하판에 형성된 배선의 표면 굴곡이 제거되어 배선의 손상을 방지할 수도 있다.

(57) 청구의 범위

청구항 1

열(列 : row)방향으로 연속하여 형성된 복수개의 주사선과, 행(行 : column)방향으로 연속하여 형성된 복수개의 신호선이 직교하고, 그 교차부에 화소(畫素 : pixel)가 형성된 표시영역과;

상기 주사선과 평행하게 형성되고, 한쪽 끝단은 외부 데이터전송선에 연결되고, 상기 데이터전송선으로부터 신호선구동입력신호를 인가받는 신호선구동입력배선과;

상기 신호선과 평행하게 형성되고, 한쪽 끝단은 외부 데이터전송선에 연결되고, 상기 데이터전송선으로부터 주사선구동입력신호를 인가받는 주사선구동입력배선과;

상기 주사선의 한쪽 끝단에 연결된 출력전극과 상기 주사선구동입력배선에서 분기된 주사인출선에 연결된 입력전극으로 구성된 주사선구동IC와;

상기 신호선의 한쪽 끝단에 연결된 출력전극과 상기 신호선구동입력배선에서 분기된 신호인출선에 연결된 입력전극으로 구성된 신호선구동IC로 구성된 액정패널에 있어서,

상기 주사선구동입력배선과 상기 주사인출선의 교차부가 유기절연막으로 절연되고, 상기 신호선구동입력배선과 상기 신호인출선의 교차부가 유기절연막으로 절연된 액정패널.

청구항 2

제1항에 있어서, 상기 유기절연막이 BCB인 것을 특징으로 하는 액정패널.

청구항 3

열(列 : row)방향으로 연속하여 형성된 복수개의 주사선과, 행(行 : column)방향으로 연속하여 형성된 복수개의 신호선이 직교하고, 그 교차부에 화소(畫素 : pixel)가 형성된 표시영역과;

상기 주사선과 평행하게 형성되고, 한쪽 끝단은 외부 데이터전송선에 연결되고, 상기 데이터전송선으로부

터 신호선구동입력신호를 인가받는 신호선구동입력배선과;

상기 신호선구동입력배선의 일부에 적층된 유기절연막과;

상기 유기절연막 위에 형성되어 상기 신호선의 한쪽 끝단에 연결된 출력전극과 상기 신호선구동입력배선에서 분기된 신호인출선과;

상기 신호인출선에 연결된 입력전극으로 구성된 신호선구동IC와;

상기 신호선과 평행하게 형성되고, 한쪽 끝단은 외부 데이터전송선에 연결되고, 상기 데이터전송선으로부터 주사선구동입력신호를 인가받는 주사선구동입력배선과;

상기 주사선구동입력배선의 일부에 적층된 유기절연막과;

상기 유기절연막 위에 형성되어 상기 신호선의 한쪽 끝단에 연결된 출력전극과 상기 주사선구동입력배선에서 분기된 주사인출선과;

상기 주사인출선에 연결된 입력전극으로 구성된 주사선구동IC로 구성된 액정패널.

청구항 4

제3항에 있어서, 상기 유기절연막은 BCB인 것을 특징으로 하는 액정패널.

청구항 5

기판과;

상기 기판 위에 섬 형상으로 형성된 복수개의 제1입력배선과;

상기 제1입력배선 위의 일부분에 증착된 제1절연막과;

상기 제1절연막 위 중, 상기 제1입력배선에 겹치지 않는 부분에 형성된 IC패드와;

상기 IC패드의 일부분과 상기 제1절연막 위의 일부분에 코팅된 유기절연막과;

상기 입력배선 중, 어느 하나의 위의 상기 제1절연막과 유기절연막을 제거하여 접촉홀(contact hole)을 뚫고, 상기 접촉홀을 통해 상기 IC패드와 상기 접촉홀이 뚫린 제1입력배선을 연결한 인출선을 포함하여 이루어진 액정패널.

청구항 6

제5항에 있어서, 상기 유기절연막은 상기 제1입력배선 위의 제1절연막 위와 상기 인출선 사이의 층에 형성된 것을 특징으로 하는 액정패널.

청구항 7

제5항 또는, 제6항에 있어서, 상기 유기절연막은 BCB인 것을 특징으로 하는 액정패널.

청구항 8

기판 위에 복수개의 입력배선을 형성하는 단계와;

상기 입력배선을 덮는 제1절연막을 도포하는 단계와;

상기 제1절연막 위 일부에 IC패드를 형성하는 단계와;

상기 IC패드와 상기 제1절연막 위에 유기절연막을 코팅하는 단계와;

상기 복수개의 입력배선 중, 어느 하나의 위에 도포된 제1절연막과 유기절연막을 제거하여 접촉홀을 뚫고, 동시에 상기 IC패드의 일부의 유기절연막을 제거하여 접촉홀을 뚫는 단계와;

상기 IC패드의 접촉홀과 상기 입력배선 위의 접촉홀을 연결하도록 상기 유기절연막 위에 인출선을 형성하는 단계를 포함하는 액정패널의 제조방법.

청구항 9

기판 위에 복수개의 인출선을 형성하는 단계와;

상기 인출선을 덮는 제1절연막을 도포하는 단계와;

상기 제1절연막 위 일부에 IC패드를 형성하는 단계와;

상기 IC패드와 상기 제1절연막 위에 유기절연막을 코팅하는 단계와;

상기 복수개의 인출선에 도포된 제1절연막과 유기절연막의 일부를 제거하여 접촉홀을 뚫고, 동시에 상기 IC패드의 유기절연막의 일부를 제거하여 접촉홀을 뚫는 단계와;

상기 IC패드의 접촉홀과 상기 인출선의 접촉홀을 연결하도록 상기 유기절연막 위에 입력배선을 형성하는 단계를 포함하는 액정패널의 제조방법.

도면

図1

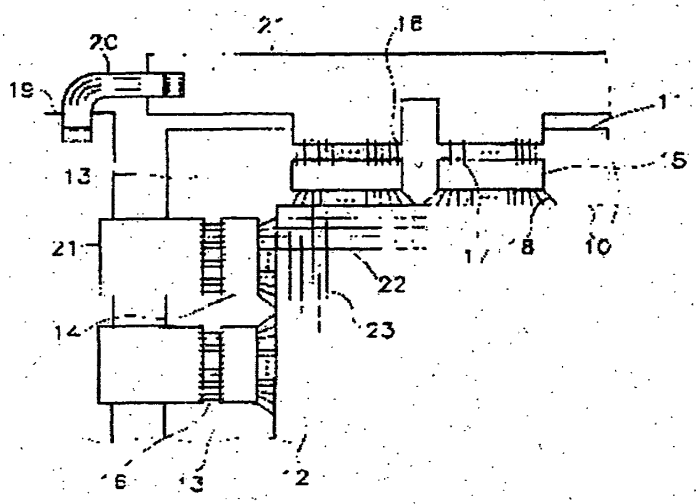
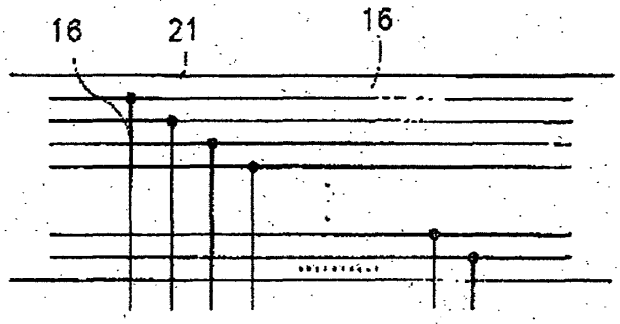
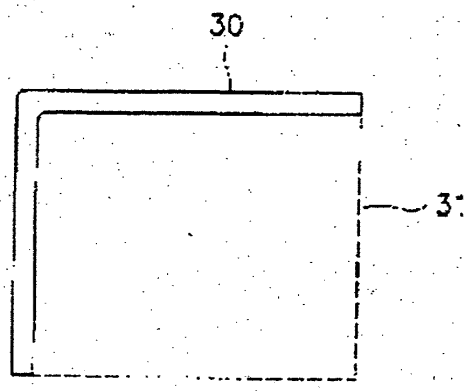


図2

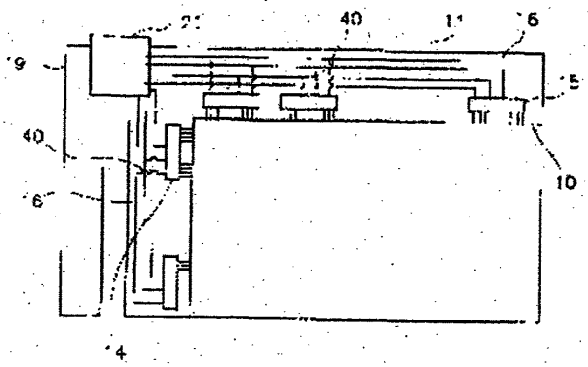


15-6

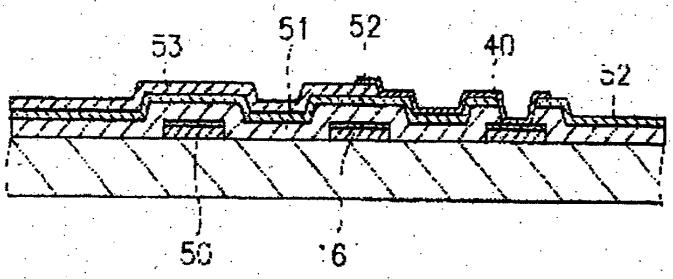
도면8



도면4

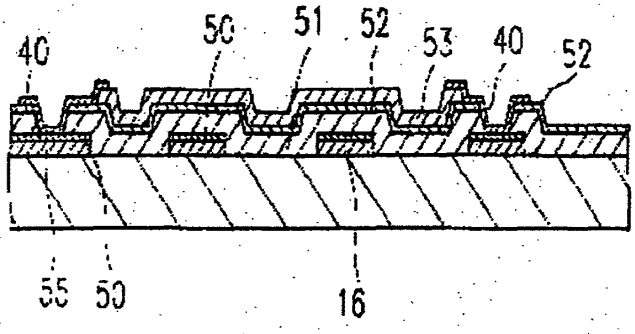


도면5a

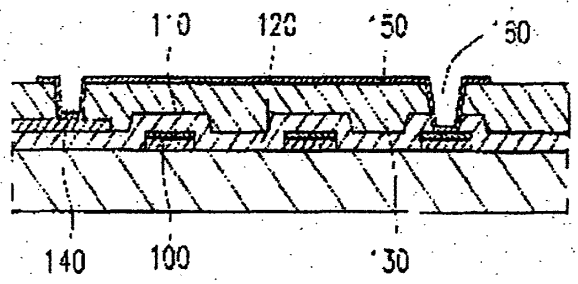


15-7

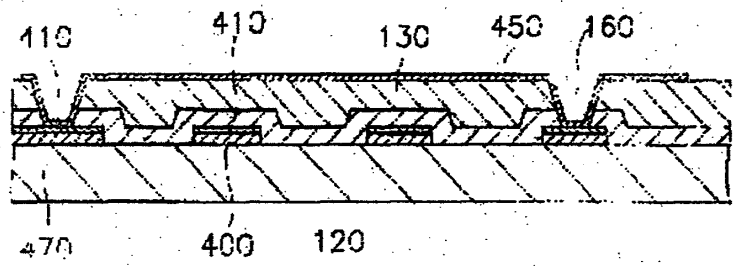
도면5b



도면6a

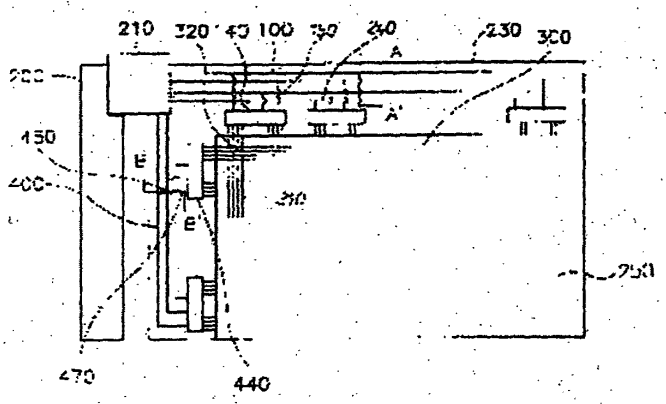


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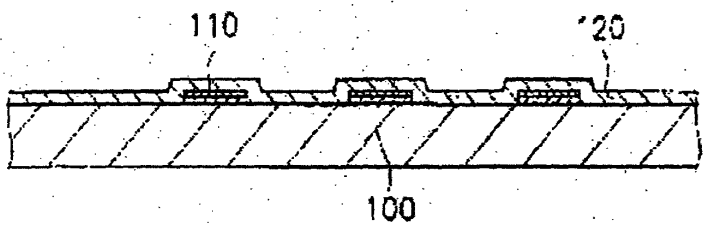


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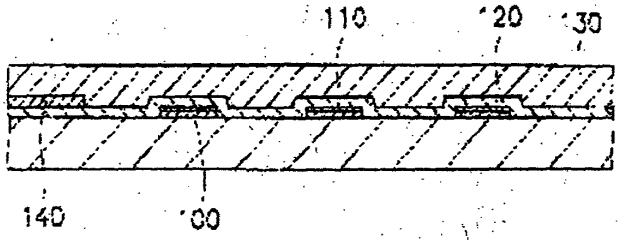
도면7



도면8a

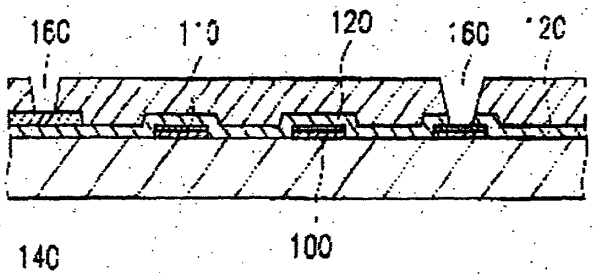


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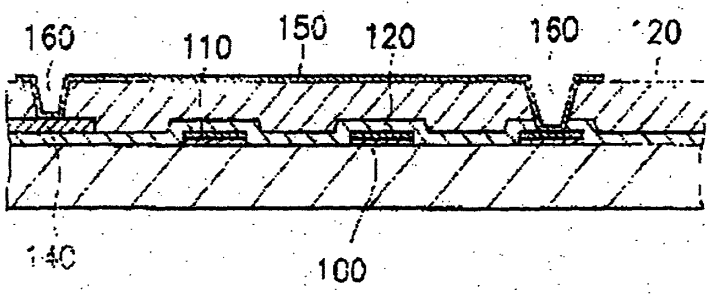


15-9

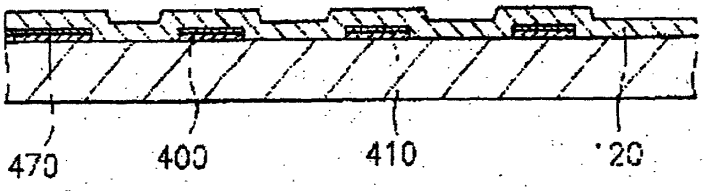
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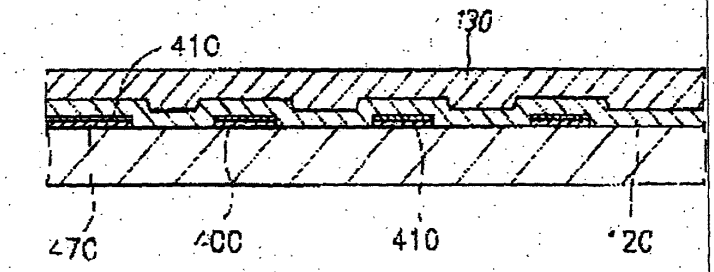
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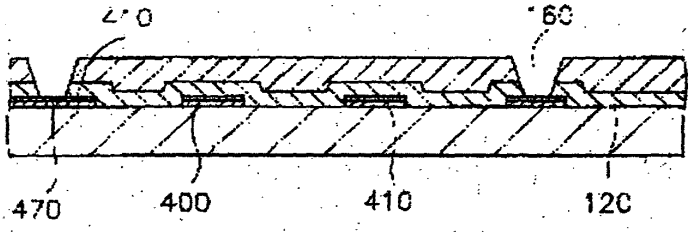
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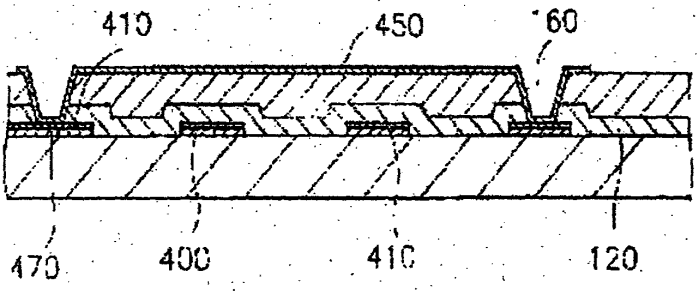
도면6b



도면6c

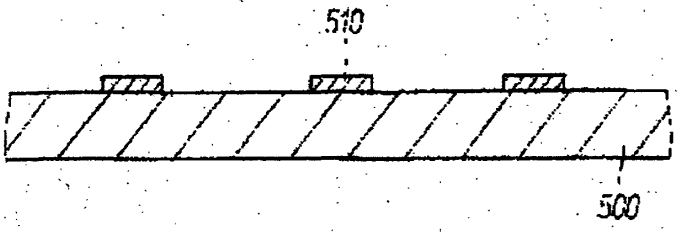


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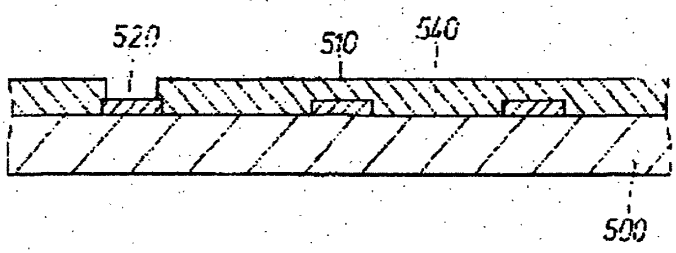


15-11

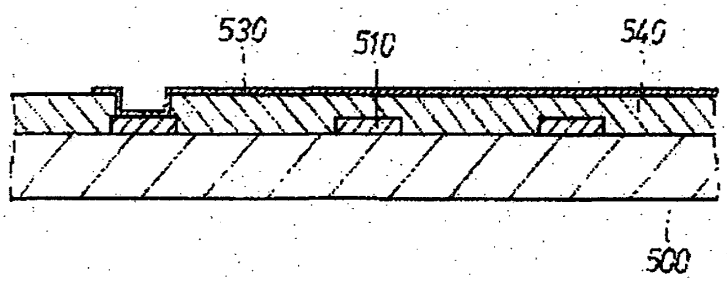
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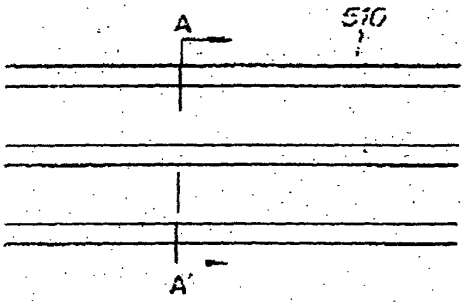
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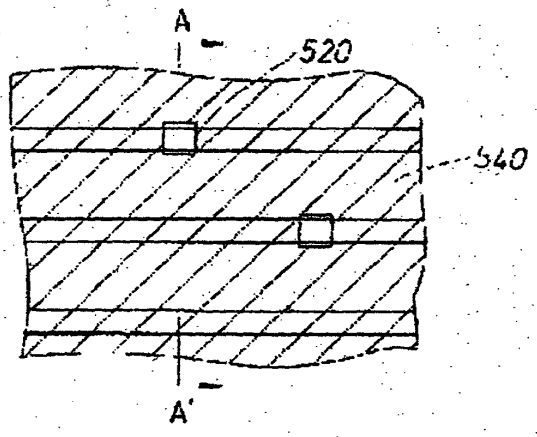
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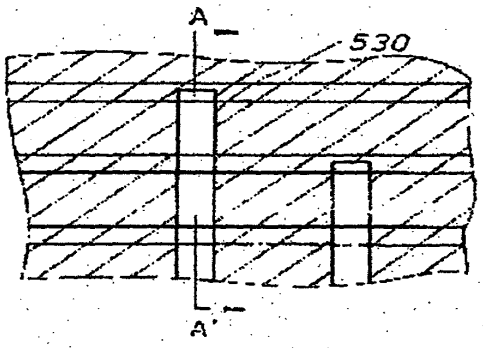
도면11a



도면11b

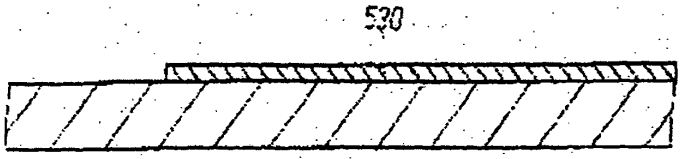


도면11c

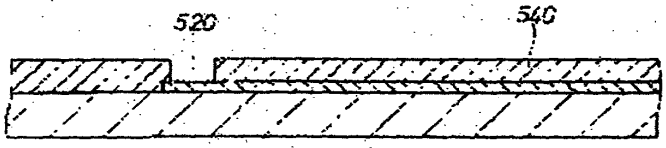


15-13

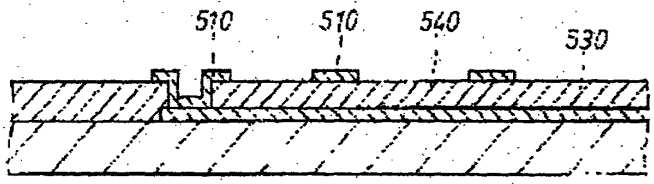
도면12a



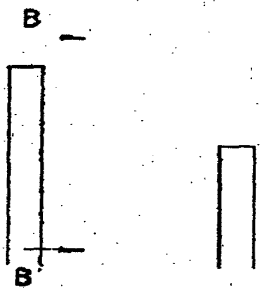
도면12b



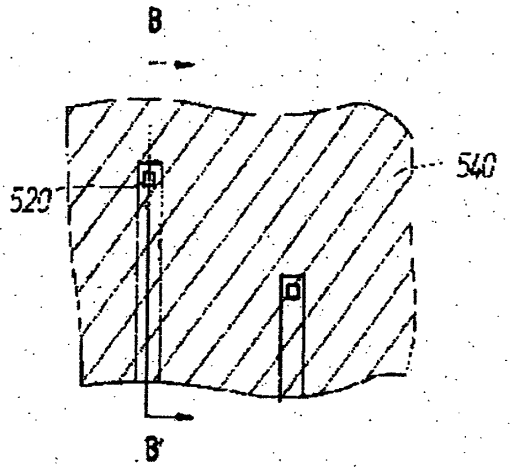
도면12c



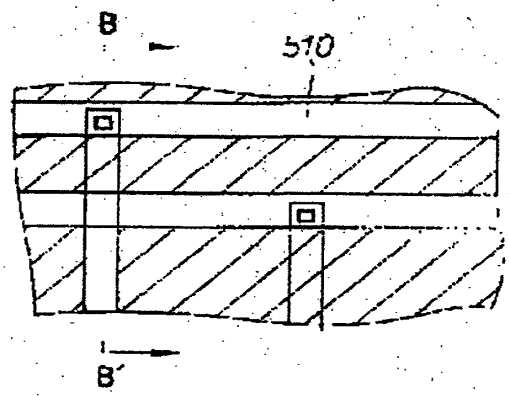
도면13a



도면13b



도면13c



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요약

TFT 어레이기판상에 있어서, 화상표시영역 및 주변영역 사이를 구획하는 프레임영역상에는, 용량배선과 동일막으로 형성되며 해당 프레임영역의 적어도 일부에 형성된 프레임패턴을 구비하고 있다. 이 프레임패턴은, 외부회로 접속단자에 접속된 배선과도 동일막으로 형성되어 있다.

이에 의해, 화상의 주위에 광누설에 기인하는 이미지가 나타난다는 것을 최대한 방지하는 등의 방법으로 화질을 높이는 것이다.

대표도

도1

색인어

전기광학장치, 전자기기, 프레임패턴

명세서

도면의 간단한 설명

도 1은 TFT 어레이기판을 그 위에 형성된 각 구성요소와 함께 대향기판측에서 본 전기광학장치의 평면도.

도 2는 도 1의 H-H' 단면도.

도 3은 전기광학장치의 화상표시영역을 구성하는 매트릭스형으로 형성된 복수의 화소에서의 각종 소자, 배선 등의 등가회로도.

도 4는 데이터선, 주사선, 화소전극 등이 형성된 TFT 어레이기판의 서로 인접하는 복수의 화소군의 평면도이고, 하층부분(도 6에서의 부호 70(축적용량)까지의 하층부분)에 관한 구성만을 나타내는 도면.

도 5는 데이터선, 주사선, 화소전극 등이 형성된 TFT 어레이기판의 서로 인접하는 복수의 화소군의 평면도이고, 상층부분(도 6에서의 부호70(축적용량)을 넘어 상층부분)에 관한 구성만을 나타내는 도면.

도 6은 도 4 및 도 5를 겹치게 한 경우의 A-A' 단면도.

도 7은 도 6에 나타내는 적층구조에 대응하는 단면도로서, (a)는 도 2에서의 부호 Z로 나타낸 원내부분의 확대도, (b)는 도 1 에서의 상하도통재가 존재하는 부분의 단면도.

도 8은 도 1과 등일한 취지의 도면으로서, 특히 프레임패턴 및 용량배선 등의 구성을 설명하기 위해 두 요소의 배치관계를 명료하게 나타내는 도면.

도 9는 도 8과 등일한 취지의 도면으로서, 본 발명의 제 2 실시 형태의 전기광학장치에 관한 프레임패턴의 태양을 나타내는 도면.

도 10은 도 9에 나타내는 부호 D 부근을 확대하고, 또한 해당 부분에서의 회로구성 등을 함께 나타내는 설명도.

도 11은 도 10과 등일한 취지의 도면으로서, 프레임패턴의 형성태양이 다른 것을 나타내는 도면.

도 12는 도 8과 동일한 취지의 도면으로서, 본 발명의 제 3 실시 형태의 전기광학장치에 관한 프레임패턴의 태양을 나타내는 도면.

도 13은 도 8과 동일한 취지의 도면으로서, 본 발명의 제 4 실시 형태의 전기광학장치에 관한 프레임패턴의 태양을 나타내는 도면.

도 14는 도 8과 동일한 취지의 도면으로서, 본 발명의 제 5 실시 형태의 전기광학장치에 관한 프레임패턴의 태양을 나타내는 도면.

도 15는 본 발명의 각 실시 형태에 관한 투사형 액정장치의 평면도.

※도면의 주요부분에 대한 부호의 설명※

3a: 게이트 전극 6a: 데이터선

9a: 화소전극 10: TFT 어레이기판

10a: 화상표시영역 11a : 주사선

20: 대향기판21: 대향전극

30: TFT53: 프레임차광막

70: 축적용량101: 데이터선 구동회로

104: 주사선 구동회로102: 외부회로 접속단자

106: 상하도통재300: 용량전극

400: 용량배선(제 1 배선)406,451,452,453,454: 프레임패턴

404,408: 배선(제 2 배선)

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은, 예컨대 액티브 매트릭스 구동의 액정장치, 전자 페이퍼 등의 전기영동장치, EL(Electro-Luminescence)표시장치 등의 전기광학장치의 기술분야에 속한다. 또한, 본 발명은 이러한 전기광학장치를 구비하여 이루어진 전자기기의 기술분야에도 속한다.

종래, 기판상에 매트릭스형으로 배열된 화소전극 및 그 전극 각각에 접속된 박막 트랜지스터(Thin Film Transistor; 이하 적절히 「TFT」라 함), 그 TFT 각각에 접속되고 행 및 열방향 각각에 평행하게 형성된 데이터선 및 주사선 등을 구비함으로써, 소위 액티브 매트릭스 구동이 가능한 전기광학장치가 알려져 있다.

이러한 전기광학장치에서는, 상기에 더해, 상기 기판에 대향배치되는 대향기판을 구비함과 동시에, 그 대향기판상에 화소전극에 대향하는 대향전극 등을 구비하고, 또한 화소전극 및 대향전극 사이에 협지되는 액정층 등을 구비함으로써 화상표시가 가능해진다. 즉, 액정층내의 액정분자는, 화소전극 및 대향전극 사이에 설정된 소정의 전위차에 의해 그 배향상태가 적당히 변경되고, 이에 의해, 해당 액정층을 투과하는 광의 투과율이 변화함으로써 화상표시가 가능해지는 것이다.

또한, 상기 기술한 전기광학장치에서의 상기 기판은, 주사선, 데이터선 및 화소전극 등이 형성되는 화상표시영역과, 주사선 구동회로, 데이터선 구동회로, 이들 회로에 소정 신호를 공급하기 위한 외부회로 접속단자 등이 형성되는 주변영역을 갖는다.

발명이 이루고자 하는 기술적 과제

그러나, 종래의 전기광학장치에서는 다음과 같은 문제점이 있다. 즉, 상기 주변영역에서는 통상, 기판 및 대향기판을 접착하기 위한 시일(seal)재가 형성된다. 이 시일재로는, 취급이 용이하다는 점, 비교적 강력한 접착력이 얻어진다는 점 등 때문에 광경화성 수지가 바람직하게 사용되고 있다. 이 경우, 시일재를 경화하기 위해서는, 기판 및 대향기판 사이에 끼워져 존재하는 해당 시일재에 대하여 광을 조사할 필요가 있다. 한편, 화상표시영역 및 주변영역에는, 상기 기술한 주사선 및 데이터선과 주사선 구동회로 및 데이터선 구동회로를 접속하기 위한 배선이나, 데이터선에 화상신호를 적절히 공급하기 위한 샘플링회로, 그 화상신호 자체를 공급하는 화상신호선 등 각종 배선이 형성될 필요가 있다. 이들에 의하면, 주변영역상의 소정 영역에서는, 상기 시일재와 상기 각종 배선 등이 함께 형성될 필요가 있게 되는데, 해당 영역에서는, 시일재 경화를 위해 소정 간극을 형성해 두는 등에 의해 광의 통로를 확보해 두는 것이 행해진다.

그러나, 이에 의하면, 완성 후의 전기광학장치를 실제로 사용할 때, 광의 통로로서 형성된 상기 소정의 간극 등을 통해 광이 누설되는 문제가 발생하게 된다. 즉, 해당 전기광학장치를, 예컨대 액정프로젝터 등의 투사형 표시장치의 라이트밸브로서 사용하는 경우에는, 이 라이트밸브에 대하여 광을 투사함과 동시에, 그 라이트밸브를 빠져나간 광을 스크린상에 확대투사함으로써 화상표시를 행하게 되는데, 상기 소정 간극 등이 존재하면, 라이트밸브를 빠져나간 광에 상기 간극으로부터 누설된 광이 혼입되어 버리는 것이다. 이러한 경우, 스크린상의 화상 주위에는 상기 각종 배선 등의 패턴 이미지가 비치는 등의 사태가 발생하여 화상의 품위를 떨어뜨리는 결과가 되어 버린다.

또한, 종래의 전기광학장치에 있어서는, 화상표시영역에 화소전극에서의 전위유지특성을 높이기 위해 축적용량이 형성되는 경우가 있다. 이 축적용량은 구성하는 한쪽 전극(이하, 「용량전극」이라 하는 경우가 있음)은, 일정한 전위로 유지하는 것이 바람직하므로, 주변영역에 형성되는 외부회로 접속단자에 접속되는 것이 행해지고 있다. 그러나, 이 경우, 양자간을 콘택트 홀을 통해 접속하는 데에 채택되면, 그 콘택트 홀에 기인하는 고저항화가 초래될 우려가 크다는 점, 또한 콘택트 홀마다 특성이 달라지는 경우가 발생할 수 있는 점 등으로 인해, 용량전극 또는 이로부터 연장되는 배선의 저항수가 커져, 그 결과 화상상에 크로스토크를 발생시키는 등의 문제가 발생하는 경우가 있었다. 상기 배선이 화상표시영역을 가로질러 형성되어 있는 경우에는, 소위 횡크로스토크로서 관찰되게 된다.

본 발명은, 상기 문제점을 감안하여 이루어진 것으로, 화상의 주위에 광누설에 기인한 이미지가 나타나는 것을 최대한 방지하고, 또는 용량전극에 소정 전위를 적절하게 공급함으로써, 고품위의 화상을 표시하는 것이 가능한 전기광학장치를 제공하는 것을 과제로 한다. 또한, 본 발명은, 그와 같은 전기광학장치를 구비하는 전자기기를 제공하는 것도 과제로 한다.

발명의 구성 및 작용

본 발명의 전기광학장치는, 상기 과제를 해결하기 위해, 기판상에 임의한 방향으로 연장되는 데이터선 및 상기 데이터선에 교차하는 방향으로 연장되는 주사선과, 상기 주사선에 의해 주사신호가 공급되는 스위칭소자와, 상기 데이터선에 의해 상기 스위칭소자를 통해 화상신호가 공급되는 화소전극을 구비하여 이루어지고, 상기 기판은 상기 화소전극 및 상기 스위칭소자의 형성영역으로서 규정되는 화상표시영역과, 상기 화상표시영역의 주변을 규정하는 주변영역을 가지며, 상기 화상표시영역상에 상기 화소전극에서의 전위를 소정 기간 유지하는 축적용량과, 상기 축적용량을 구성하는 용량전극에 소정 전위를 공급하는 제 1 배선을 구비하고, 상기 제 1 배선과 동일막으로 형성되고, 상기 화상표시영역과 상기 주변영역을 구획하는 프레임영역의 적어도 일부를 구성하는 프레임패턴을 구비하고 있다.

본 발명의 전기광학장치에 의하면, 스위칭소자의 일례인 박막 트랜지스터에 대해 주사선을 통해 주사신호가 공급됨으로써 그 ON·OFF가 제어된다. 한편, 화소전극에 대해서는, 데이터선을 통해 화상신호가 공급됨으로써, 상기 박막 트랜지스터의 ON·OFF에 따라 화소전극에 해당 화상신호의 입가·비인가가 이루어진다. 이에 의해, 본 발명에 관한 전기광학장치는 소위 액티브 매트릭스 구동이 가능해졌다. 또한, 본 발명에 있어서는, 화소전극에서의 전위를 소정 기간 유지하는 축적용량이 형성되어 있음으로써, 그 화소전극의 전위유지특성이 향상되었다.

그리고, 본 발명에서는 특히, 상기 기판은 화상표시영역 및 주변영역을 가지며, 이 중 전자에는 상기 화소전극, 스위칭소자, 축적용량 및 제 1 배선이 형성되어 있다. 또한, 본 발명에서는, 주변영역 또는 화상표시영역 및 주변영역 사이를 구획하는 프레임영역의 적어도 일부에, 상기 제 1 배선과 동일막으로 형성된 프레임패턴을 구비하고 있다. 여기서 프레임영역이란, 예컨대 화상표시영역이 직사각형상인 경우에는, 이 직사각형상의 주위를 소정 폭의 프레임을 설정한 영역으로 규정된다. 따라서, 이 경우의 프레임영역은, 평면으로 볼 때 ㅁ 자 형상을 갖게 된다. 또한, 주변영역은, 화상표시영역의 중심에서 봤을 때 이 ㅁ 자 형상이 되는 프레임영역의 외연으로부터 바깥영역으로서 규정되게 된다. 또한, 「동일막으로 형성」되어 있다는 것은, 해당 전기광학장치의 제조공정에서, 프레임패턴 및 제 1 배선의 전구막이 동일한 기회에 형성되고, 이 전구막에 대해 동시에 소정의 패터닝 처리(예컨대, 포토리소그래피 및 에칭공정 등)가 실시되는 것을 의미한다.

그리고, 상기 프레임패턴은, 상기와 같은 프레임영역의 적어도 일부에 형성되어 있다. 이에 의해, 프레임영역을 투과하고자 하는 광은 프레임패턴에 의해 그 진행이 차단되게 된다. 따라서, 본 발명에 의하면, 프레임패턴이 형성되어 있는 영역에 대응하는 만큼, 배광기술에서 설명한 광누설이 발생하는 것을 미연에 방지할 수 있게 됨으로써, 화상의 주위에 각종 배선 등의 패턴 이미지가 비치는 것 등을 방지하는 것이 가능해지므로 보다 고품질의 화상을 표시하는 것이 가능해진다.

또한, 본 발명에 있어서, 프레임패턴은, 화상표시영역에 형성되는 제 1 배선과 전기적으로 접속되어 있도록 형성되어도 되고, 또는 양자간은 패터닝상 분단되도록 형성되어도 된다.

또한, 본 발명에 있어서, 제 1 배선이 용량전극에 소정 전위를 공급하는 역할을 하기 위한 구성으로는, 예컨대, 그 제 1 배선이 용량전극에 접속 또는 연장형성되는 구성을 채택하면 된다. 여기서, 「용량전극에 접속」된다는 것은, 예컨대, 용량전극 및 제 1 배선이 기판상에 구축되는 적층구조 중 각각 다른 층에 형성되어 있는 경우에 있어서, 양자간에 콘택트 홀을 통함으로써 이들간 전기적으로 접속하는 등의 경우를 포함한다. 한편, 제 1 배선이 「용량전극에 ... 연장형성」된다는 것은, 예컨대, 그 용량전극과 평면적으로 연속하는 형상을 갖는 패턴(즉, 이 패턴에 있어서는, 그 패턴이 형성되는 평면 내에서 제 1 배선이라 부를 수 있는 부분과 용량전극이라 부를 수 있는 부분의 쌍방을 포함하게 됨)이 동일층에 형성되는 등의 경우를 포함한다.

또한, 본 발명에서 말하는 「프레임패턴」은 프레임영역상에 형성되어 있기 때문에 그 이름이 부여되어 있을 뿐, 그 프레임패턴이 프레임과 같은 형상을 갖고 있다는 것을 의미하는 것은 아님을 덧붙여둔다(프레임패턴이, 「프레임영역의 적어도 일부」에 형성되어 있다는 것은, 그러한 취지를 포함함). 또한, 이러한 프레임패턴은, 프레임영역을 넘어 주변영역상에 이르도록 형성되어도 된다.

본 발명의 전기광학장치의 다른 태양에서는, 상기 기판에 대향배치되는 대향기판과, 상기 기판 및 상기 대향기판을 협력하는 시일재를 더 구비하며 이루어지고, 상기 프레임패턴은 상기 시일재가 형성되는 시일영역의 적어도 일부에 형성되어 있다.

이 태양에 의하면, 기판 및 대향기판이 예컨대 광경화성 수지 등으로 이루어진 시일재에 의해 접착되어 있다. 이 경우, 프레임영역이, 가령 상기와 같은 ㅁ 자 형상을 갖는 것이라 한다면, 시일재가 형성되는 시일영역은, 그 프레임영역의 ㅁ 자 형상의 전부 또는 일부를 포함하거나, 또는 포함하지 않고 그 프레임영역의 외연 바깥에 위치하며, 또한 그 ㅁ 자 형상보다도 약간 큰 ㅁ 자 형상을 갖는 것으로 상정할 수 있다(따라서, 이 시일영역의 적어도 일부는, 상기 주변영역에 포함되는 영역임).

본 태양에 의하면, 이와 같이, 프레임영역 바깥에서도 상기 프레임패턴이 형성되어 있음으로써, 시험영역을 투과하고자 하는 광 또한 프레임패턴에 의해 그 전영에 차단되게 된다. 따라서, 본 발명에 의하면, 화상의 주위에 각종 배선 등의 패턴 이미지가 비치는 것 등을 보다 효과적으로 방지하는 것이 가능해지므로, 보다 고품질의 화상을 표시하는 것이 가능해진다.

본 발명의 전기광학장치의 다른 태양에서는, 상기 기판에 대향배치되는 대향기판과 그 대향기판상에 형성되는 대향전극을 더 구비하여 이루어지고, 상기 프레임패턴은, 상기 대향전극과 전기적으로 접속되어 있는 접속부분을 갖는다.

이 태양에 의하면, 프레임패턴은 대향전극과 전기적으로 접속된 접속부분을 갖는, 즉 대향전극 및 프레임패턴은 전기적으로 접속된 상태가 되어, 양자는 항상 등전위 전위에 있게 된다. 이에 의하면, 프레임패턴은 상기 기술한 광누설 방지의 기능과 대향전극에의 전위공급기능이라는 두가지 기능을 동시에 하게 되어, 그만큼 장치 구성의 간략화가 도모된다. 덧붙이면, 프레임패턴과 제 1 배선은, 상기 기술한 바와 같이 동일막으로 형성되어 있기 때문에, 양자를 「전기적으로 접속하도록 형성」하는 것은, 전형적으로는 프레임차광막 및 제 1 배선에 공통의 전구막에 있어서 양자를 분단하지 않고 패터닝 처리하는 경우(즉, 이 경우에는 평면적으로 연속하는 패턴상, 프레임패턴이라 할 수 있는 부분과 제 1 배선이라 할 수 있는 부분의 쌍방이 존재함)가 상정되게 된다.

또한, 본 태양과 더불어, 상기 기술한 프레임패턴 및 대향전극 사이의 전기적 접속이 도모된 태양을 경비하면, 프레임패턴, 대향전극 및 제 1 배선 상자는 항상 동일 전위에 있게 된다. 이에 의하면, 장치 구성의 간략화는 더욱 바람직하게 달성되게 되는 것은 말할 필요도 없다.

접속부분을 구비하는 태양에서는, 상기 접속부분은, 상기 대향기판의 코너부에 대응하여 형성되도록 구성해도 된다.

이러한 구성에 의하면, 예컨대, 화상표시영역이 직사각형상인 경우에는, 그 화상표시영역의 네 모퉁이에 대응하도록, 또는 그 화상표시영역에 프레임을 설정한 프레임영역 또는 그 바깥의 시험영역의 네 모퉁이에 대응하도록 접속부분을 배치하는 것 등이 가능해진다. 이 경우, 프레임패턴 및 대향전극 사이의 전기적 접속을 적절히 도모하면서, 화상표시를 방해하지 않는다는 작용효과가 얻어진다.

또, 본 태양에서 말하는 「코너부」는, 대향기판 자체의 네 모퉁이 부분을 포함하는 것은 물론, 이들 각 모퉁이로부터 일정한 평면적인 확장(예컨대, 해당 모퉁이 부분을 중심으로 한 등설원적인 확장)을 갖는 부분도 포함하는 개념이다. 또한, 접속부분이 「코너부에 대응하여 형성되어 있다」는 것에는, 그 접속부분이 상기 네 모퉁이 전부에 형성되어 있는 경우 외에, 화상표시영역의 세 모퉁이 이하에 대응하도록 형성되어 있는 등의 경우도 포함한다.

본 발명의 전기광학장치의 다른 태양에서는, 상기 프레임패턴은 상기 화상표시영역의 주위 전부를 둘러싸도록 형성되어 있다.

이 태양에 의하면, 프레임패턴이 상기 화상표시영역의 주위 전부를 둘러싸도록 형성되어 있기 때문에, 원리상으로는 프레임영역 또는 시험영역을 투과하는 광을 완전히 차단하는 것도 가능해다. 따라서, 상기 광누설의 작용은 보다 효과적으로 방지되게 되어, 보다 고품질의 화상을 표시하는 것이 가능해진다.

또한, 이 태양에 있어서, 상기 화상표시영역의 주위 전부를 둘러싸도록 형성된 프레임패턴에 상기 대향전극과의 「접속부분」이 존재하는 경우에 있어서는, 이 프레임패턴과 대향전극과의 전기적 접속을 보다 확실하게 이룰 수 있다. 그 이유는, 프레임패턴은 그 모든 부분이 전기적으로 접속되어 있는(바꾸어 말하면, 연속적인 패턴으로 형성되어 있음) 것, 그리고 상기 접속부분은 상기 기술한 예와 같이, 화상표시영역의 네 모퉁이, 즉 프레임패턴 또는 시험영역의 네 모퉁이에 대응하도록 다수형성 가능하므로, 설령 프레임패턴의 일부 또는 접속부분의 어느 부분이 임의의 사정에 의해 전기적으로 도통 (導通) 불능이 된 경우라 하더라도, 다른 부분에 의해 전기적 도통을 지체없이 실현하는 것이 가능하기 때문이다 (바꾸어 말하면, 프레임패턴 또는 그 프레임패턴상의 접속부분에 대해 용장 (冗長) 적인 구조가 채택될 수 있음). 이에 의해, 이와 같은 태양에 있어서는, 대향전극의 전위를 매우 안정적으로 유지하는 것이 가능해져, 그 대향전극 및 화소전극 사이에 협지되는 전기광학물질의 배향상태의 조정을 적절하게 행할 수 있기 때문에, 보다 고품질의 화상을 표시하는 것이 가능해진다.

한편, 상기 기술한 프레임패턴이 대향전극과 전기적으로 접속되어 있는 접속부분을 갖는 태양에서는, 상기 화상표시영역은 평면으로 볼 때 직사각형한 가지며, 상기 프레임패턴은, 상기 직사각형의 3변을 따라 연속하여 형성된 제 1 패턴과, 나머지 1변을 따라 형성됨과 동시에 상기 제 1 패턴과 분단되어 형성된 제 2 패턴을 포함하고, 상기 접속부분은 상기 제 1 패턴상에 존재하도록 해도 된다.

이러한 구성에 의하면, 우선, 프레임패턴이 직사각형을 갖는 화상표시영역의 3변을 따라 연속하여 형성된 제 1 패턴을 포함하고, 또한 상기 접속부분은 이 제 1 패턴상에 존재하므로, 상기 기술한 화상표시영역의 주위 전부를 둘러싸도록 프레임패턴이 형성되어 있는 태양과 마찬가지로, 프레임패턴 및 대향전극 사이의 전기적 접속을 보다 확실하게 이룰 수 있어, 대향전극의 전위를 매우 안정적으로 유지하는 것이 가능해진다.

또한, 본 태양에 있어서는, 이 제 1 패턴에 더하여, 상기 직사각형의 나머지 1변을 따라 형성됨과 동시에 상기 제 1 패턴과 분단되어 형성된 제 2 패턴을 포함하므로, 다음과 같은 작용효과가 얻어진다. 즉, 이 제 2 패턴이 형성되는 영역이, 예컨대 데이터선 구동회로가 형성되는 영역에 대응하는 경우에 있어서는, 해당 데이터선 구동회로에 의해 제어되는 샘플링회로에 둘러쳐지는 화상신호선과, 대향기판상의 대향

전극과의 사이에서 용량커플링이 발생할 우려가 있다. 이 용량커플링이 발생하면, 입력에 대한 응답에 의해 타측에서의 전위에 변동을 주게 되므로, 원하는 화상표시가 어려워지게 된다. 그런데, 본 태양에 의하면, 해당 영역에는 상기 제 2 패턴이 형성되어 있기 때문에, 화상신호선 및 대향전극 사이에는 그 제 2 패턴이 존재하게 되어, 상기 용량커플링의 발생을 억제할 수 있는 것이다. 따라서, 본 태양에 의하면 원하는 화상을 적절하게 표시할 수 있다.

또, 이러한 작용효과는, 상기 기술한 프레임패턴을 화상표시영역의 주위 전부를 둘러싸도록 형성하는 태양에 있어서도, 완전히 동일하게 누릴수 있음은 말할 필요도 없다.

또한, 본 태양에서 말하는 「제 1 패턴」 및 「제 2 패턴」, 나아가 이하에 후술하는 태양에서 말하는 「제 3 패턴」 내지 「제 6 패턴」이란 용어는, 단순히 각각이 별개의 개념으로 규정되는 반도체 프로세스상의 패턴이라는 것을 나타내는 것에 불과하다(바꾸어 말하면, 「A」 내지 「F」는 단순한 「이름」에 불과함).

또는, 상기 화상표시영역은 평면으로 볼 때 직사각형을 가지며, 상기 프레임패턴은, 상기 직사각형의 대향하는 2변을 따라 형성된 제 5 패턴과, 나머지 2변을 따라 형성됨과 동시에 상기 제 3 패턴과 분단되어 형성된 제 4 패턴을 포함하고, 상기 접속부분은 상기 제 3 패턴상에 존재하도록 해도 된다.

이러한 구성에 의하면, 우선, 프레임패턴이 직사각형을 갖는 화상표시영역의 대향하는 2변을 따라 형성된 제 3 패턴을 포함하고, 또한 상기 접속부분은 이 제 3 패턴상에 존재한다. 이 제 3 패턴은, 상기 정의상 분단되어 형성되는 2개의 직선형 배선이 포함되는 것이 전반적으로 상정된다. 이 태양에 의하면, 해당 2개의 직선형 배선에는 각각 상기 접속부분이 적어도 2개 존재할 수 있다. 따라서, 대향전극 및 프레임패턴 사이의 전기적 접속을 보다 확실하게 이룰 수 있다.

또한, 본 태양에 있어서는, 이 제 3 패턴에 더하여, 상기 직사각형이 나머지 2변을 따라 형성됨과 동시에, 상기 제 3 패턴과 분단되어 형성된 제 4 패턴을 포함한다.

이에 의해, 상기 제 2 패턴과 마찬가지로, 제 4 패턴이 형성되는 영역이, 예컨대 데이터선 구동회로가 형성되는 영역에 대응하는 경우에는, 화상신호선 및 대향전극 사이의 용량커플링의 발생을 방지할 수 있다.

또한, 상기 화상표시영역은 평면으로 볼 때 직사각형을 가지며, 상기 프레임패턴은, 상기 직사각형상의 하나의 모서리부에 대응하는 부분을 제외하고 연속하여 형성된 제 5 패턴과, 상기 하나의 모서리부에 대응하는 부분에 형성됨과 동시에 상기 제 5 패턴과 분단되어 형성된 제 6 패턴을 포함하고, 상기 접속부분은 상기 제 5 패턴 및 상기 제 6 패턴의 적어도 일측상에 존재하도록 해도 된다.

이러한 구성에 의하면, 우선, 프레임패턴이 직사각형상을 갖는 화상표시영역의 하나의 모서리부에 대응하는 부분을 제외하고 연속하여 형성된 제 5 패턴을 포함하고, 또한 그 제 5 패턴상에 상기 접속부분이 존재할 수 있다. 따라서, 전형적으로는, 접속부분은 이 제 5 패턴상에 3개 존재하는 것을 생각할 수 있다.

또한, 본 태양에 있어서는, 이 제 5 패턴에 더하여, 상기 하나의 모서리부에 대응하는 부분에 형성됨과 동시에 상기 제 5 패턴과 분단되어 형성된 제 6 패턴을 포함하고, 또한 그 제 6 패턴상에 상기 접속부분이 존재할 수 있다. 따라서, 전형적으로는, 접속부분은 이 제 6 패턴상에 1개 존재하는 것을 생각할 수 있다.

이상으로부터, 본 태양에 의하면, 상기 기술한 프레임패턴 및 대향전극 사이의 전기적 접속의 확실성 또는 화상신호선 및 대향전극 사이의 용량커플링의 발생억제 등의 작용효과가 거의 동일하게 얻어진다.

또, 본 태양에 관한 프레임패턴의 태양, 또는 상기 기술한 프레임패턴에 관한 각종 태양은, 프레임패턴의 형성태양의 변형을 증가시키는 의미를 갖는 것은 말할 필요도 없다. 이에 의해, 외부회로 접속단자로부터, 데이터선 구동회로, 주사선 구동회로, 또는 상기 접속부분으로 끌어치는 각종 배선의 배치(내지는 패터닝)를 보다 용이하게 이루는 것 등도 가능해진다.

본 발명의 전기광학장치의 다른 태양에서는, 상기 주변영역상에 상기 기판의 변 가장자리부를 따라 형성된 외부회로 접속단자와, 그 외부회로 접속단자에 연장형성된 제 2 배선을 더 구비하고, 그 제 2 배선의 적어도 일부가 상기 제 1 배선과 층간막으로, 또한 그 제 1 배선과 전기적으로 접속되어 형성되어 있다.

이 태양에 의하면, 주변영역에는 외부회로 접속단자 및 제 2 배선이 형성되어 있고, 이 중 제 2 배선의 적어도 일부가 제 1 배선과 층간막으로, 또한 그 제 1 배선과 전기적으로 접속되어 형성되어 있다. 여기서 「층간막으로 형성되어 있다」는, 프레임패턴 및 제 1 배선에 관하여 이미 서술한 바와 같은 의의를 갖는다. 이에 의하면, 제 2 배선의 적어도 일부 및 제 1 배선은, 데이터선, 주사선 및 화소전극 등이 구성하는 적층구조 중 동일한 층에 형성되게 되고, 또한 양자는 동일한 재료로 구성되게 된다. 덧붙이면, 본 발명에 있어서는 제 1 배선과 프레임패턴이 층간막으로 형성되므로, 본 태양에 의하면 결국, 제 1 배선, 프레임패턴 및 제 2 배선이 모두 층간막으로 형성되게 된다.

이에 의하면, 첫째로, 외부회로 접속단자, 제 2 배선 및 제 1 배선을 동일층에 형성하는 것이 가능해지므로, 이들 각 요소간의 전기저항치를 저하시킬 수 있다.

덧붙이면, 종래에 있어서는, 상기 기술한 바와 같은 각 요소는 각각 별도의 층에 형성되어 있고, 이에 의해, 그 각 요소간의 전기적 접속에는 콘택트 홀 등이 이용되는 경우가 있었다. 그러나, 콘택트 홀을 이용하면 그 콘택트 홀에 기인하는 고저항화가 초래될 우려가 크다는 점, 또한 콘택트 홀마다 특성이 달라지는 사태가 발생할 수 있다는 점에서 보면, 용량커플 또는 이로부터 연장되는 배선의 시정수가 커져, 그 결과 화상상에 크로스토크를 발생시키는 등의 문제점이 발생하는 경우가 있었다. 상기 배선이 화상표시영역을 가로질러 형성되어 있는 경우에는, 소위 횡 크로스토크로서 관찰되게 된다.

그런데, 본 태양에 있어서는, 이미 서술한 바와 같이, 외부회로 접속단자, 제 2 배선 및 제 1 배선을 동일층에 형성하는 것이 가능하므로, 상기와 같은 문제없이 끝난다.

둘째로, 본 태양과, 상기 프레임패턴에 접속부분을 갖는 태양, 또는 화상표시영역의 주위 전부를 둘러싸도록 프레임패턴이 형성되는 태양, 나아가 상기 제 1 패턴, 제 2 패턴, 제 3 패턴, 제 4 패턴, 제 5 패턴

및 제 6 패턴을 포함하는 프레임패턴을 구비한 태양전지 겸비한 전기광학장치(이하, 해당 전기광학장치의 태양전지를 「병용 (併用) 태양전지」이라 함)에 관해서는 그에 더하여, 다음과 같은 다양의 작용효과를 나타내게 된다. 즉, 이 병용태양전지에 관한 전기광학장치에서는, 프레임패턴에는 이것과 대향전극 사이의 접속부분이 존재하므로, 그 프레임패턴은 상기 광누설 방지의 작용효과 등과 함께, 대향전극에 소정 전위를 공급하는 배선으로서의 기능도 갖고 있다. 여기서, 이 병용태양전지에서는, 이 프레임패턴과 함께, 제 2 배선, 제 1 배선 또한 투명막으로 형성되어 있으므로, 이들 각 요소 및 외부회로 접속단자 사이의 전기저항치는 저하시키는 것이 가능해진 것이다.

여러한 점에서, 상기 병용태양전지에 있어서는, 외부회로 접속단자로부터, 제 2 배선, 그리고 프레임패턴에 이르기까지의 전기저항치는 낮게 억제되게 되므로, 그 프레임패턴의 전위는 안정된 상태를 유지하는 것이 가능해져, 대향전극의 전위도 안정한 상태로 유지하는 것이 가능해지는 것이다. 또한, 프레임패턴에는 제 1 배선이 전기적으로 접속될 수 있으므로, 그 제 1 배선의 전위, 나아가 여기에 접속 또는 연장형성되는 용량전극의 전위 또한 안정한 상태로 유지하는 것이 가능해진다.

이와 같이 병용태양전지에 의하면, 프레임패턴, 제 2 배선 및 제 1 배선이 투명막으로 그리고 전기적으로 접속된 상태로 형성되며, 또한 그 프레임패턴에 상기 접속부분이 존재하므로, 본 태양전지에 관한 작용효과(저저항화) 및 접속부분을 갖는 것에 의한 작용효과(대향전극에 대한 전위공급가능)의 쌍방에 대해, 이것을 보다 효과적으로 누리는 것이 가능해지는 것이다.

이 태양전지에서는, 상기 제 1 배선은 상기 데이터선상에 제 1 층간절연막을 개재하여 형성되도록 해도 된다.

이러한 구성에 의하면, 기판상에 구축되는 주사선, 데이터선, 화소전극 및 외부회로 접속단자 등으로 이루어진 적층구조를 적절하게 구성하는 것이 가능해진다.

즉, 우선, 외부회로 접속단자는 외부로 노출되는 전극을 구비해야 하므로, 상기 적층구조 중 비교적 상층에 형성되는 것이 바람직하다.

그렇지 않으면, 적층구조의 최상층부분으로부터 상기 전극에 대하는 비교적 깊은 콘택트 홀 등을 개공해야 하기 때문이다. 한편, 본 태양전지에 의하면, 제 1 배선은 데이터선상에 형성되어 있으므로, 그 제 1 배선과 투명막으로 형성되고, 외부회로 접속단자에 접속 또는 연장형성되는 제 2 배선도 역시 데이터선상에 형성되게 된다. 따라서, 제 2 배선은 상기 적층구조 중 비교적 상층에 형성되게 된다.

이상으로부터, 본 태양전지에서는, 외부회로 접속단자를 비교적 상층에 형성한다 하더라도, 여기에 접속 또는 연장형성되는 제 2 배선도 역시 비교적 상층에 형성됨으로써 양자간의 전기적 접속을 무리없이 실현하는 것이 가능해진다. 이와 같이, 본 태양전지에 의하면, 상기 적층구조를 적절하게 형성하는 것이 가능해지는 것이다.

또는, 상기 제 1 배선은 상기 화소전극을 포함하는 층의 바로 아래층에 형성되어 있도록 해도 된다.

이러한 구성에 의하면, 외부회로 접속단자 및 제 2 배선 사이의 전기적 접속을 더욱 무리없이 실현하는 것이 가능하다. 즉, 화소전극이 전기광학특성에 대향할 필요가 있다는 점에서, 제 1 배선이 화소전극을 포함하는 층의 바로 아래층에 형성되어 있다는 것은, 그 제 1 배선이 전기광학특성의 층에서 본 때, 화소전극과의 사이에 1층의 절연막을 끼우는 것만으로 형성되어 있는 경우가 전형적으로는 상정되게 된다. 그리고, 이 경우, 제 1 배선과 투명막으로 형성되는 제 2 배선도 역시 화소전극을 포함하는 층의 바로 아래층에 형성되게 되므로, 그 제 2 배선 위에는 통상 상기 절연막이 존재할 뿐이다. 이는, 주변영역에 있어서는, 화소전극의 바로 아래에 형성되는 절연막의 표면이 외부로 노출되게 되는 것이 통상이기 때문이다.

따라서, 본 태양전지에 의하면, 외부회로 접속단자를 구성하는 전극을 외부로 노출시키는 것은 매우 용이해진다. 또한, 제 2 배선과의 전기적인 접속은 상기 전극으로부터 그 제 2 배선을 연장형성하는 것에 의하면 된다.

이와 같이, 본 태양전지에 의하면, 외부회로 접속단자 및 제 2 배선 사이의 전기적 접속을 무리없이 실현하는 것이 가능해지는 것이다.

또한, 제 2 배선을 구비하는 전기광학장치의 다른 태양에서는, 상기 제 1 배선 및 상기 프레임패턴은 전기적으로 접속되어 형성되어 있지 않고, 또한 상기 제 2 배선의 제 1 부분 및 상기 제 1 배선이 전기적으로 접속되고, 상기 제 2 배선의 제 2 부분 및 상기 프레임패턴이 전기적으로 접속되어 있고, 상기 제 1 부분은 상기 외부회로 접속단자의 제 1 부분에, 상기 제 2 부분은 상기 외부회로 접속단자의 제 2 부분에 각각 접속되도록 해도 된다.

이러한 구성에 의하면, 프레임패턴 및 제 1 배선을 각각 서로 다른 전위로 유지할 수 있다. 이 경우, 제 1 배선이 용량전극에 소정 전위를 공급하기 위한 것이라는 점에 주의함과 동시에, 프레임패턴에 대향전극이 접속되어 있다는 전제를 두면, 프레임패턴 및 제 1 배선을 각각 다른 전위로 유지할 수 있다는 것은, 용량전극 및 대향전극을 각각 다른 전위로 유지할 수 있다는 것과 같은 의미가 된다. 이는, 외부회로 접속단자의 제 1 부분에 있는 전위를 공급하면, 해당 제 1 부분이, 제 2 배선의 제 1 부분, 제 1 배선 및 용량전극에 접속되어 있으므로, 용량전극은 해당 전위로 유지되는 한편, 외부회로 접속단자의 제 2 부분에 상기 어떤 전위와는 다른 전위를 공급하면, 해당 제 2 부분이, 제 2 배선의 제 2 부분, 프레임패턴 및 대향전극에 접속되어 있으므로, 대향전극은 해당 전위로 유지되게 되기 때문이다. 이들 각 개념을 구체화한 것에 관해서는, 후에 설명하는 실시의 실시 형태에 있어서, [제 5 실시 형태] 로서 설명되어 있다.

이에 의해, 본 태양에 의하면, 해당 전기광학장치내에서 발생하는 각종 전기작용을 적절하게 조정하는 것 등이 가능하다.

본 발명의 전기광학장치의 다른 태양에서는, 제 1 배선은 차광성 재료로 구성되어 있다.

이 태양에 의하면, 제 1 배선은 용량전극에 접속 또는 연장형성되는 배선으로서 화상표시영역내에 형성되

는 것이므로, 화상표시영역내에 있어서 해당 제 1 배선이 형성되어 있는 영역에 대응한 차광을 실현할 수 있다. 이에 의해, 상기 스위칭소자의 일례인 박막 트랜지스터를 구성하는 반도체층(한성층)에 광이 함부로 입사되는 사태를 미연에 방지하는 것이 가능해지므로, 이 반도체층에서의 광리크전류의 발생을 억제할 수 있고, 따라서 화상상에 플리커 등이 발생하는 것을 미연에 방지하는 것이 가능해진다.

또한, 본 태양에 의하면, 그 제 1 배선과 동일막으로 형성되는 제 2 배선 또한 차광성 재료로 구성되게 된다. 따라서, 주변영역상에 형성되는 스위칭소자로서의 박막 트랜지스터에 관해서도, 상기와 동일한 작용효과를 얻을 수 있어 해당 박막 트랜지스터의 정확한 동작을 기대할 수 있다.

그리고 또한, 본 태양에 의하면, 상기 제 1 배선과 동일막으로 형성되는 프레임패턴 또한 차광성 재료로 구성되게 된다. 따라서, 상기 광누설 방지의 작용효과를 보다 효과적으로 얻게 된다.

본 태양에서 말하는 「차광성 재료」로는, 예컨대 광반사율이 비교적 큰 Al(알루미늄) 등을 포함하는 외에, Ti(티탄), Cr(크롬), W(텅스텐), Ta(탄탈), Mo(몰리브덴) 등의 고융점 금속 등의 적어도 하나를 포함하는, 금속 단체, 합금, 금속실리사이드, 폴리실리사이드, 이들을 적층한 것 등도 포함한다.

본 발명의 전기광학장치의 다른 태양에서는, 상기 제 1 배선은 상이한 재료로 이루어진 적층구조를 갖는다.

이 태양에 의하면, 예컨대, 제 1 배선의 하층에 알루미늄으로 이루어진 층, 그 상층에 질화 티탄으로 이루어진 층 등의 2층 구조로 구성된다. 이 경우, 하층의 알루미늄층에 의하면, 높은 전기전도성능 및 광반사율이 비교적 높은 것에 의한 차광성능을 누릴 수 있음과 동시에, 상층의 질화 티탄층에 의하면, 제 1 배선상에 형성되는 층간절연막 등의 전구막을 패터닝 처리할 때, 또는 그 층간절연막 등에 콘택트 홀을 형성할 때, 활용되는 것의 발생을 방지하는 기능을 누리는 것(즉, 그 질화 티탄으로 이루어진 층은, 소위 에치스톱으로서 기능함)이 가능해진다.

이와 같이, 본 태양에 의하면, 제 1 배선이 「적층구조」를 갖는 것으로서 구성됨으로써, 그 제 1 배선에 용량전극에 전위를 공급하는 기능을 담당하게 하는 것에 더하여, 새로운 기능을 부여하는 것이 가능하여 그 고기능화를 도모할 수 있다.

또, 본 태양에서 말하는 「적층구조」로는, 상기 기술한 것 외에, 여러 가지 구성을 채택하는 것이 가능한 것은 말할 필요도 없다.

또한, 본 태양에 의하면, 제 1 배선과 동일막으로 형성되는 제 2 배선 및 프레임패턴 또한 상이한 재료로 이루어진 적층구조를 갖게 되는데, 이 적층구조를 구성하는 각 재료의 선택은, 그 제 2 배선 및 그 프레임패턴이 담당하는 기능(즉, 외부회로 접속단자와 주사선 구동회로 및 데이터선 구동회로의 접속(제 2 배선)이나, 제 2 배선으로부터 제 1 배선에의 전위공급의 용개(프레임패턴) 등)을 고려하여 새로운 기능을 부여한다는 관점에서 행하면 된다. 또, 저저항재료의 일례인 알루미늄을 포함하는 상기 2층 구조는, 이러한 관점에서도 바람직하다고 할 수 있다.

본 발명의 전기광학장치의 다른 태양에서는, 상기 기판에 대향배치되는 대향기판과, 그 대향기판상에 형성된 차광막을 더 구비하여 이루어지고, 상기 프레임패턴은 상기 차광막과 겸치도록 형성되어 있다.

이 태양에 의하면, 예컨대, 대향기판으로부터 기판을 향하여 광을 투사하는 경우에 있어서, 프레임영역에서는 우선, 상기 차광막에 의한 차광이 행해지고, 계속해서 프레임패턴에 의한 차광이 행해진다. 이와 같이, 본 태양에 의하면 이중 차광이 삼현됨으로써, 상기 기술한 광누설 방지의 작용효과는 보다 효과적으로 나타나게 된다.

이 태양에서는, 상기 차광막은 상기 대향기판의 변 가장자리부를 따르도록 형성된 프레임차광막을 포함하도록 해도 된다.

이러한 구성에 의하면, 차광막이 프레임차광막을 포함하므로, 상기 기술한 이중차광은 보다 양호하게 실현되게 된다.

본 발명의 전자기기는 상기 과제를 해결하기 위해, 상기 기술한 본 발명의 전기광학장치(단, 그 각종 태양을 포함함)를 구비하여 이루어진다.

본 발명의 전자기기에 의하면, 상기 기술한 본 발명의 전기광학장치를 구비하여 이루어지므로, 화상의 주위에 각종 배선 등의 패턴 이미지가 비치는 것 등이 미연에 방지됨으로써, 고품질의 화상이 표시가능한 프로젝터, 액정 TV, 휴대전화, 전자수첩, 워드 프로세서, 뷰파인더형 또는 모니터 직시형의 비디오테이프 레코더, 워크스테이션, TV 전화, POS 단말기, 터치패널 등의 각종 전자기기를 실현할 수 있다.

본 발명의 이러한 작용 및 다른 이득은 다음에 설명하는 실시 형태로부터 명확해진다.

이하에서는, 본 발명의 실시 형태에 대해 도면을 참조하면서 설명한다. 이하의 실시 형태는 본 발명의 전기광학장치를 액정장치에 적용한 것이다.

[제 1 실시 형태]

[전기광학장치의 전체 구성]

우선, 본 발명의 전기광학장치에 관한 제 1 실시 형태의 전체 구성에 대해 도 1 및 도 2를 참조하여 설명한다. 여기서, 도 1은, TFT 어레이기판과 그 위에 형성된 각 구성요소와 함께 대향기판을 포함한 전기광학장치의 평면도이고, 도 2는 도 1의 H-H' 단면도이다. 여기서는, 전기광학장치의 일례인 구동회로 내장형의 TFT 액티브 매트릭스 구동방식의 액정장치를 예로 든다.

도 1 및 도 2에 있어서, 제 1 실시 형태에 관한 전기광학장치에서는, TFT 어레이기판(10)과 대향기판(20)이 대향배치되어 있다. TFT 어레이기판(10)과 대향기판(20) 사이에 액정층(50)이 봉입되어 있고, TFT 어레이기판(10)과 대향기판(20)은, 화상표시영역(10a)의 주위에 위치하는 시일영역에 형성된 시일재

(52)에 의해 상호 접력되며 있다.

시일재(52)는, 두 기판을 접합하기 위한, 예컨대, 자외선 경화수지, 열경화 수지 등으로 이루어지며, 제조 프로세스에 있어서 TFT 어레이기판(10)상에 도포된 후, 자외선 조사, 가열 등에 의해 경화된 것이다. 또한, 시일재(52) 중에는, TFT 어레이기판(10)과 대향기판(20)과의 간격(기판간 갭)을 소정치로 하기 위한 유리섬유 또는 유리비드 등의 갭재가 살포되어 있다. 특, 제 1 실시 형태의 전기광학장치는 프로젝터의 라이트밸브용으로서 소형으로 확대표시를 행하는 데 적합하다.

시일재(52)가 배치된 시일영역의 내측에 병행하여, 화상표시영역(10a)의 프레임영역을 규정하는 차광성의 프레임차광막(53)이 대향기판(20)측에 형성되어 있다. 단, 이러한 프레임차광막(53)의 일부 또는 전부는 TFT 어레이기판(10) 측에 내장 차광막으로 형성되어도 된다. 제 1 실시 형태에 있어서는, 상기 화상표시영역(10a)의 주변을 규정하는 주변영역이 존재한다. 바꿔 말하면, 제 1 실시 형태에 있어서는 특히, TFT 어레이기판(10)의 용성에서 볼 때, 이 프레임차광막(53)보다 바깥이 주변영역으로 규정되어 있다.

주변영역 중, 시일재(52)가 배치된 시일영역의 외측에 위치하는 영역에는, 데이터선 구동회로(101) 및 외부회로 접속단자(102)가 TFT 어레이기판(10)의 1변을 따라 형성되어 있다. 또한, 주사선 구동회로(104)는, 이 1변에 인접하는 2변을 따라, 또한 상기 프레임차광막(53)에 덮이도록 형성되어 있다. 또한, 이와 같이 화상표시영역(10a)의 양측에 형성된 2개의 주사선 구동회로(104) 사이를 연결하므로, TFT 어레이기판(10)의 나머지 1변을 따라, 그리고 상기 프레임차광막(53)에 덮이도록 복수의 배선(105)이 형성되어 있다. 이 중 데이터선 구동회로(101) 및 주사선 구동회로(104)는, 외부회로 접속단자(102)와 배선(404)을 통해 접속되어 있다.

또한, 대향기판(20)의 4개의 코너부에는, 두 기판 사이의 상하도통단자로서 기능하는 상하도통재(106)가 배치되어 있다. 이 상하도통재(106)는, 은가루 등의 도전성 입자가 굳어진 구성 등으로 이루어진다. 한편, TFT 어레이기판(10)에는 이들의 코너부에 대향하는 영역에 상하도통단자가 형성되어 있다. 이들에 의해, TFT 어레이기판(10)과 대향기판(20) 사이에서 전기적인 도통을 취할 수 있다.

도 2에 있어서, TFT 어레이기판(10)상에는, 화소 스위칭용의 TFT나 주사선, 데이터선 등의 배선이 형성된 후의 화소전극(9a)상에 배향막이 형성되어 있다. 한편, 대향기판(20)상에는, 대향전극(21) 외에, 격자형 또는 스트라이프형의 차광막(23), 나아가 최상층부분에 배향막이 형성되어 있다. 또한, 액정층(50)은, 예컨대 1종 또는 여러 종류의 네마틱 액정을 혼합한 액정으로 이루어지며, 이들 한 쌍의 배향막 사이에서 소정의 배향상태를 갖는다.

이상과 같은 전체 구성을 갖는 제 1 실시 형태의 전기광학장치에 있어서는, 상기 기술한 각종 요소 중, 배선(404), 상하도통재(105) 등에 관한 구체적 구성에 대해 특징이 있지만, 그 점에 대해서는 도 7 등을 참조하면서 후에 상세히 서술한다.

도 1 및 도 2에 나타낸 TFT 어레이기판(10)상에는, 이들의 데이터선 구동회로(101), 주사선 구동회로(104) 등에 더하여, 화상신호선상의 화상신호를 샘플링하여 데이터선에 공급하는 샘플링회로, 복수의 데이터선에 소정 전압레벨의 프리차지신호를 화상신호에 선행하여 각각 공급하는 프리차지회로, 제조 도중이나 출하시의 해당 전기광학장치의 품질, 결함 등을 검사하기 위한 검사회로 등을 형성해도 된다.

[화소부에서의 구성]

이하에서는, 본 발명의 제 1 실시 형태에서의 전기광학장치의 화소부에서의 구성에 대해 도 3 내지 도 7을 참조하여 설명한다. 여기서 도 3은, 전기광학장치의 화상표시영역을 구성하는 매트릭스형으로 형성된 복수의 화소에서의 각종 소자, 배선 등의 등가회로이고, 도 4 및 도 5는, 데이터선, 주사선, 화소전극 등이 형성된 TFT 어레이기판의 서로 인접하는 복수의 화소군의 평면도이다. 도 4 및 도 5는, 각각 후술하는 적층구조 중 하층부분(도 4)과 상층부분(도 5)을 나누어 도시하고 있다.

또한, 도 6은 도 4 및 도 5를 겸한 경우의 A-A' 단면도이고, 도 7(a) 및 도 7(b)는 각각 도 2에서의 부호 Z로 나타낸 원내부분의 확대도 및 도 1에서의 상하도통재(106)가 존재하는 부분에 관한 단면도로서, 모두 도 6에 나타내는 적층구조에 대응하는 단면도이다. 도 6 및 도 7에 있어서는, 각 층·각 부재를 도면상에서 인식가능한 정도의 크기로 하기 위해 그 각 층·각 부재마다 축척을 다르게 하고 있다.

(화소부의 회로구성)

도 3에 있어서, 제 1 실시 형태에서의 전기광학장치의 화상표시영역을 구성하는 매트릭스형으로 형성된 복수의 화소에는, 각각 화소전극(9a)과 해당 화소전극(9a)을 스위칭제어하기 위한 TFT(30)가 형성되어 있고, 화상신호가 공급되는 데이터선(6a)이 해당 TFT(30)의 소스에 전기적으로 접속되어 있다. 데이터선(6a)에 기록하는 화상신호(S1, S2,..., Sn)는 이 순서로 선순차로 공급해도 관계없고, 서로 인접하는 복수의 데이터선(6a)끼리에 대해 그룹마다 공급하도록 해도 된다.

또한, TFT(30)의 게이트에 게이트전극(3a)이 전기적으로 접속되어 있고, 소정의 타이밍으로 주사선(11a) 및 게이트전극(3a)에 펄스적으로 주사신호(G1, G2,..., Gm)를 이 순서로 선순차로 인가하도록 구성되어 있다. 화소전극(9a)은 TFT(30)의 드레인에 전기적으로 접속되어 있고, 스위칭소자인 TFT(30)를 일정 기간만큼 그 스위치를 닫음으로써, 데이터선(6a)으로부터 공급되는 화상신호(S1, S2,..., Sn)를 소정 타이밍으로 기록한다.

화소전극(9a)을 통해 전기광학장치의 일례로서의 액정에 기록된 소정 레벨의 화상신호(S1, S2,..., Sn)는, 대향기판에 형성된 대향전극과의 사이에서 일정 기간 유지된다. 액정은, 인가되는 전압레벨에 따라 분자집합의 배향이나 질서가 변화함으로써, 광을 변조하여 계조표시를 가능하게 한다. 노멀리 화이트 모드이면, 각 화소의 단위로 인가된 전압에 따라 입사광에 대한 투과율이 감소하고, 노멀리 블랙 모드이면, 각 화소의 단위로 인가된 전압에 따라 입사광에 대한 투과율이 증가되어, 전체적으로 전기광학장치로부터는 화상신호에 따른 콘트라스트를 갖는 광이 출사된다.

여기서 유지된 화상신호가 누설되는 것을 방지하기 위해, 화소전극(9a)과 대향전극 사이에 형성되는 액정

용량과 병렬로 축적용량(70)을 부가한다. 이 축적용량(70)은, 주사선(11a)에 나란히 형성되고, 고정 전위측 용량전극을 포함함과 동시에 정전위에 고정된 용량전극(300)을 포함하고 있다.

[화소부의 구체적 구성]

이하에서는, 상기 데이터선(6a), 주사선(11a) 및 게이트전극(3a), TFT(30) 등에 의한 상기 기술한 회로 동작이 실현되는 전기광학장치의 구체적인 구성에 대해 도 4 내지 도 7을 참조하며 설명한다.

우선, 도 4 및 도 5에 있어서, 화소전극(9a)은, TFT 어레이기판(10)상에 매트릭스형으로 다수 형성되어 있고(점선부에 의한 윤곽이 나타나 있음), 화소전극(9a)의 종횡의 경계 각각을 따라 데이터선(6a) 및 주사선(11a)이 형성되어 있다. 데이터선(6a)은, 후술하는 바와 같이 알루미늄막 등을 포함하는 적층구조로 이루어지고, 주사선(11a)은 예컨대 도전성의 폴리규소막 등으로 이루어진다. 또한, 주사선(11a)은 반도체층(1a) 중 도면 중 사선영역으로 나타낸 채널영역(1a')에 대향하는 게이트전극(3a)에 콘택트홀(12cv)을 통해 전기적으로 접속되어 있고, 상기 게이트전극(3a)은 상기 주사선(11a)에 포함되는 형으로 되어 있다.

즉, 게이트전극(3a)과 데이터선(6a)이 교차하는 곳에는 각각, 주사선(11a) 에 포함되는 게이트전극(3a)이 채널영역(1a')에 대향하도록 배치된 화소 스위칭용의 TFT(30)가 형성되어 있다. 이에 의해 TFT(30: 게이트전극 제외)는, 게이트전극(3a)과 주사선(11a) 사이에 존재하는 형태로 되어 있다.

다음으로, 전기광학장치는 도 4 및 도 5의 A-A' 선 단면도인 도 6에 나타내는 바와 같이, 예컨대 석영기판, 유리기판, 규소기판으로 이루어진 TFT 어레이기판(10)과, 이에 대향배치되는 예컨대 유리기판이나 석영기판으로 이루어진 대향기판(20)을 구비하고 있다.

TFT 어레이기판(10)측에는 도 6에 나타내는 바와 같이 상기 화소전극(9a)이 형성되어 있고, 그 상측에는 러빙처리 등의 소정의 배향처리가 실시된 배향막(16)이 형성되어 있다. 화소전극(9a)은 예컨대 ITO막 등의 투명 도전성막으로 이루어진다. 한편, 대향기판(20)측에는 그 전체면에 걸쳐 대향전극(21)이 형성되어 있고, 그 하측에는 러빙처리 등의 소정의 배향처리가 실시된 배향막(22)이 형성되어 있다. 대향전극(21)은, 상기 기술한 화소전극(9a)과 마찬가지로, 예컨대 ITO막 등의 투명 도전성막으로 이루어진다.

이와 같이 대향배치된 TFT 어레이기판(10) 및 대향기판(20) 사이에는, 상기 기술한 씰재(52: 도 1 및 도 2 참조)에 의해 둘러싸인 공간에 액정 등의 전기광학물질이 봉입되고 액정층(50)이 형성된다. 액정층(50)은, 화소전극(9a)으로부터의 전계가 인가되지 않은 상태로 배향막(16 및 22)에 의해 소정의 배향상태를 갖는다.

한편, TFT 어레이기판(10)상에는, 상기 화소전극(9a) 및 배향막(16) 외에, 이들을 포함하는 각종 구성의 적층구조를 이루어 구비되어 있다. 이 적층구조는 도 6에 나타내는 바와 같이, 밑에서부터 순서대로 주사선(11a)을 포함하는 제 1 층, 게이트전극(3a)을 포함하는 TFT(30) 등을 포함하는 제 2 층, 축적용량(70)을 포함하는 제 3 층, 데이터선(6a) 등을 포함하는 제 4 층, 본 발명에 말하는 '제 1 배선'의 일례인 용량배선(400) 등을 포함하는 제 5 층, 상기 화소전극(9a) 및 배향막(16) 등을 포함하는 제 6 층(최상층)으로 이루어진다.

또한, 제 1 층 및 제 2 층 사이에는 하지절연막(12)이, 제 2 층 및 제 3 층 사이에는 제 1 층간절연막(41)이, 제 3 층 및 제 4 층 사이에는 제 2 층간절연막(42)이, 제 4 층 및 제 5 층 사이에는 제 3 층간절연막(43)이, 제 5 층 및 제 6 층 사이에는 제 4 층간절연막(44)이 각각 형성되어 있고, 상기 기술한 각 요소간이 단락되는 것을 방지하고 있다. 또한, 이들 각종 절연막(12,41,42,43 및 44)에는, 예컨대 TFT(30)의 반도체층(1a) 중의 고농도 소스영역(1d)과 데이터선(6a)을 전기적으로 접속하는 콘택트 홀 등 또한 형성되어 있다. 이하에서는, 이들 각 요소에 대해 밑에서부터 순서대로 설명한다. 상기 기술한 것 중 제 1 층부터 제 3 층까지가 하층부분으로서 도 4에 도시되어 있고, 제 4 층부터 제 6 층까지가 상층부분으로서 도 5에 도시되어 있다.

(적층구조 - 제 1 층의 구성 -주사선 등-)

우선, 제 1 층에는, 예컨대, Ti, Cr, W, Ta, Mo 등의 고융점 금속 중의 적어도 하나를 포함하는, 금속 단체, 합금, 금속실리사이드, 폴리실리사이드, 이들을 적층한 것, 또는 도전성 폴리규소 등으로 이루어진 주사선(11a)이 형성되어 있다. 이 주사선(11a)은, 평면적으로 볼 때 도 4의 X 방향을 따르도록 스트라이프형으로 패터닝되어 있다. 더 상세히 보면, 스트라이프형의 주사선(11a)은 도 4의 X 방향을 따르도록 연장되는 본선부와, 데이터선(6a) 또는 용량배선(400)이 연장된 도 4의 Y 방향으로 연장되는 돌출부를 구비하고 있다. 인접하는 주사선(11a)으로부터 연장되는 돌출부는 서로 접속되지 않고, 따라서 그 주사선(11a)은 1개 1개 분단된 형으로 되어 있다.

(적층구조 - 제 2 층의 구성 -TFT 등-)

다음, 제 2 층으로서 게이트전극(3a)을 포함하는 TFT(30)가 형성되어 있다. TFT(30)는 도 6에 나타내는 바와 같이, LDD(Lightly Doped Drain)구조를 갖고 있고, 그 구성요소로는 상기 기술한 게이트전극(3a), 예컨대 폴리규소막으로 이루어지며 게이트전극(3a)으로부터의 전계에 의해 채널이 형성되는 반도체층(1a)의 채널영역(1a'), 게이트전극(3a)과 반도체층(1a)을 절연하는 게이트절연막을 포함하는 절연막(2), 반도체층(1a)에서의 저농도 소스영역(1b) 및 저농도 드레인영역(1c) 및 고농도 소스영역(1d) 및 고농도 드레인영역(1e)을 구비하고 있다.

또한, 제 1 실시 형태에서는, 이 제 2 층에 상기 기술한 게이트전극(3a)과 동일막으로 중계전극(719)이 형성되어 있다. 이 중계전극(719)은 평면적으로 볼 때, 도 6에 나타내는 바와 같이 각 화소전극(9a)의 X 방향으로 연장되는 1변의 거의 절반에 위치하도록 섬형상으로 형성되어 있다. 중계전극(719)과 게이트전극(3a)은 동일막으로 형성되어 있으므로, 후자가 예컨대 도전성 폴리규소막 등으로 이루어진 경우에는, 전자 또한 도전성 폴리규소막 등으로 이루어진다.

(적층구조 : 제 1 층 및 제 2 층 사이의 구성 -하지절연막-)

도 6에 나타내는 바와 같이, 이상 설명한 주사선(11a)의 위, 그리고 TFT(30)의 아래에는, 예컨대 규소산화막 등으로 이루어진 하지절연막(12)이 형성되어 있다. 하지절연막(12)은, 주사선(11a)으로부터 TFT(30)를 층간절연하는 기능 외에, TFT 어레이기판(10)의 전체면에 형성됨으로써, TFT 어레이기판(10)의 표면연마에 의한 거칠어짐이나, 세정후에 남는 더러움 등에 의한 화소스위칭용 TFT(30)의 특성변화를 방지하는 기능을 갖는다.

이 하지절연막(12)에는 평면적으로 볼 때 반도체층(1a)의 양측에, 후술하는 데이터선(6a)을 따라 연장되는 반도체층(1a)의 채널폭이의 방향을 따른 공형상의 콘택트 홀(12cv)이 관련 있고, 이 콘택트 홀(12cv)에 대응하여, 그 상측에 적층되는 게이트전극(3a)은 하측에 오목하게 형성된 부분을 포함하고 있다. 또한, 이 콘택트 홀(12cv) 전체를 메우도록 게이트전극(3a)이 형성됨으로써, 그 게이트 전극(3a)에는 이것과 일체적으로 형성된 측벽부(3b)가 연장형성되어 있다. 이에 의해, TFT(30)의 반도체층(1a)은 도 4에 잘 나타나 있는 바와 같이, 평면적으로 볼 때 측방으로부터 덮이도록 되어 있고, 적어도 이 부분으로부터의 광의 입사가 억제되게 되어 있다.

또한, 이 측벽부(3b)는 도 4에 나타내는 바와 같이, 상기 콘택트 홀(12cv)을 메우도록 형성되어 있을과 동시에, 그 하단이 상기 주사선(11a)과 접속되도록 되어 있다. 여기서 주사선(11a)은, 상기 기술한 바와 같이 스트라이프형으로 형성되어 있기 때문에, 등연 행에 존재하는 게이트전극(3a) 및 주사선(11a)은, 해당 행에 유의하는 한 항상 등일 전위가 된다.

(적층구조 : 제 3 층의 구성 -축적용량 등-)

도 6에 나타내는 바와 같이, 상기 기술한 제 2 층에 계속하여 제 3 층에는 축적용량(70)이 형성되어 있다. 축적용량(70)은, TFT(30)의 고농도 드레인영역(1e) 및 화소전극(9a)에 접속된 화소전위측 용량전극으로서의 하부전극(71)과, 고정전위측 용량전극으로서의 용량전극(300)이, 유전체막(75)을 통해 대향 배치됨으로써 형성되어 있다. 이 축적용량(70)에 의하면, 화소전극(9a)에서의 전위유지특성을 현저히 높이는 것이 가능해진다. 또한, 제 1 실시 형태에 관한 축적용량(70)은, 도 4의 평면도를 보면 알 수 있듯이, 화소전극(9a)의 형성영역에 거의 대응하는 광투과영역에는 이르지 않도록 형성되어 있으므로(바꾸어 말하면, 차광영역내에 수용되도록 형성되어 있으므로), 전기광학장치 전체의 화소 개구율은 비교적 크게 유지되고, 이에 의해 보다 밝은 화상을 표시하는 것이 가능해진다.

여기서, 상기 화소전위측 용량전극으로서의 전극이 하부전극(71)과는 반대로 축적용량(70)의 상부에 형성되는 구성이어도 된다. 이 경우, 당연한 원이지만 고정전위측 용량전극으로서의 용량전극(300)은 축적용량(70)의 하부에 형성되게 된다. 바람직한 예로는, 화소전위측 용량전극이 TFT(30)의 고농도 드레인영역 (1e)의 연장된 고농도 드레인영역(1e)과 등일막이고, 고정전위측 용량전극으로서의 용량전극(300)은, TFT(30)보다 더 하측에 있고, TFT(30)에 하측으로부터 혐입하는 입사광을 차광하기 위한 차광층과 등일층이어도 된다. 이 경우의 후술하는 용량배선(400)은, 고정전위측 용량전극으로서의 용량전극(300)과 등일층의 막인 것이 구조가 간단해져 바람직하지만, 이에 한정되는 것은 아니다.

보다 상세하게는, 하부전극(71)은, 예컨대 도전성의 폴리규소막으로 이루어져 화소전위측 용량전극으로서 기능한다. 단, 하부전극(71)은, 금속 또는 합금을 포함하는 단일층막 또는 다층막으로 구성해도 된다. 또한, 이 하부전극(71)은, 화소전위측 용량전극으로서의 기능 외에, 화소전극(9a)과 TFT(30)의 고농도 드레인영역(1e)을 중계접속하는 기능을 갖는다. 이와 관련하여, 여기서 말하는 중계접속은 상기 중계전극(719)을 통해 행해지고 있다.

용량전극(300)은 축적용량(70)의 고정전위측 용량전극으로서 기능한다. 제 1 실시 형태에 있어서, 용량전극(300)을 고정전위로 하기 위해서는, 고정전위로 된 용량배선(400; 후술)과 전기적 접속이 도모됨으로써 이루어지고 있다. 여기서는, 용량전극(300)을 고정전위로 하기 위한 접속에 있어서 용량배선(400)을 중계하고 있는데, 예컨대 용량배선(400)을 용량전극(300)과 등일막으로 연장하여 형성해도 된다. 이러한 구성에 의해, 용량배선(400)을 별층으로 필요로 하지 않아, 접속저항에 의한 배선저항 증대도 없어지고, 용량배선(400)으로서의 층을 별도로 형성할 필요도 없기 때문에 프로세스도 간단해진다.

또한, 용량전극(300)은 Ti, Cr, W, Ta, Mo 등의 고융점 금속 중의 적어도 하나를 포함하는, 금속 단체, 합금, 금속실리사이드, 폴리실리사이드, 이들을 적층한 것, 또는 바람직하게는 텅스텐 실리사이드로 이루어진다.

이에 의해, 용량전극(300)은 TFT(30)에 상측으로부터 입사하고자 하는 광을 차단하는 기능을 갖고 있다.

유전체막(75)은 도 6에 나타내는 바와 같이, 예컨대 막두께 5~200㎚ 정도의 비교적 얇은 HTO(High Temperature Oxide)막, LTO(Low Temperature Oxide)막 등의 산화 규소막 또는 질화 규소막 등으로 구성된다. 축적용량(70)을 증대시키는 관점에서는, 막의 신뢰성이 충분히 얻어지는 한, 유전체막(75)은 얇을수록 좋다.

제 1 실시 형태에 있어서, 이 유전체막(75)은 도 6에 나타내는 바와 같이, 하층의 산화 규소막(75a), 상층의 질화 규소막(75b)의 2층 구조를 갖는 것으로 되어 있다. 상층의 질화 규소막(75b)은 화소전위측 용량전극의 하부전극(71)보다 조금 큰 크기로 패터닝되어, 차광영역(비개구영역)내에서 수용되도록 형성되어 있다.

(적층구조, 제 2 층 및 제 3 층 사이의 구성 -제 1 층간절연막-)

이상 설명한 TFT(30) 내지 게이트전극(3a) 및 중계전극(719)의 위, 또한 축적용량(70)의 아래에는, 예컨대 NSG(non-실리케이트 유리), PSG(인 실리케이트 유리), BSG(붕소 인 실리케이트 유리) 등의 실리케이트 유리막, 질화 규소막이나 산화 규소막 등, 또는 바람직하게는 NSG로 이루어진 제 1 층간절연막(41)이 형성되어 있다.

그리고, 이 제 1 층간절연막(41)에는, TFT(30)의 고농도 소스영역(1d)과 후술하는 데이터선(6a)을 전기적

으로 접속하는 콘택트 홀(81)이, 후술하는 제 2 층간절연막(42)을 관통하면서 개공되어 있다. 또한, 제 1 층간절연막(41)에는, TFT(30)의 고농도 드레인영역(1e)과 축적용량(70)을 구성하는 하부전극(71)을 전기적으로 접속하는 콘택트 홀(83)이 개공되어 있다. 또한, 이 제 1 층간절연막(41)에는, 축적용량(70)을 구성하는 화소전위측 용량전극으로서의 하부전극(71)과 용계전극(719)을 전기적으로 접속하기 위한 콘택트 홀(881)이 개공되어 있다. 또한, 제 1 층간절연막(41)에는 용계전극(719)과 후술하는 제 2 용계전극(6a2)을 전기적으로 접속하기 위한 콘택트 홀(882)이, 후술하는 제 2 층간절연막을 관통하면서 개공되어 있다.

(적층구조 · 제 4 층의 구성 -데이터선 등-)

상기 기술한 제 3 층에 계속하여 제 4 층에는 데이터선(6a)이 형성되어 있다. 이 데이터선(6a)은 도 6에 나타내는 바와 같이, 하층으로부터 순서대로, 알루미늄으로 이루어진 층(도 6의 부호 41A 참조), 질화 티탄으로 이루어진 층(도 6의 부호 41TN 참조), 질화 규소막으로 이루어진 층(도 6의 부호 401 참조)의 3층 구조를 갖는 막으로 형성되어 있다. 질화 규소막은, 그 하층의 알루미늄층과 질화 티탄층을 덮도록 조금 큰 크기로 패터닝되어 있다.

또한, 이 제 4 층에는 데이터선(6a)과 동일막으로 용량배선용 용계층(6a1) 및 제 2 용계전극(6a2)이 형성되어 있다. 이들은 도 6에 나타내는 바와 같이, 평면적으로 볼 때, 데이터선(6a)과 연속한 평면형상을 갖도록 형성되어 있는 것은 아니라, 각각의 사이는 패터닝상 분단되도록 형성되어 있다. 예컨대 도 5 중 가장 좌측에 위치하는 데이터선(6a)에 유의하면, 그 바로 우측에 대략 사변형상을 갖는 용량배선용 용계층(6a1), 그 우측에 용량배선용 용계층(6a1)보다도 약간 큰 면적을 갖는 대략 사변형상을 갖는 제 2 용계전극(6a2)이 형성되어 있다.

(적층구조 · 제 3 층 및 제 4 층 사이의 구성 -제 2 층간절연막-)

이상 설명한 축적용량(70)의 위, 그리고 데이터선(6a)의 아래에는, 예컨대 NSG, PSG, BSG, BPSG 등의 실리케이트 유리막, 질화 규소막이나 산화 규소막 등, 또는 바람직하게는 TEOS 가스를 사용한 플라즈마 CVD법에 의해 형성된 제 2 층간절연막(42)이 형성되어 있다. 이 제 2 층간절연막(42)에는, TFT(30)의 고농도 소스영역(1d)과 데이터선(6a)을 전기적으로 접속하는 상기 콘택트 홀(81)이 개공되어 있음과 동시에, 상기 용량배선용 용계층(6a1)과 축적용량(70)의 상부전극인 용량전극(300)을 전기적으로 접속하는 콘택트 홀(801)이 개공되어 있다. 또한, 제 2 층간절연막(42)에는, 제 2 용계전극(6a2)과 용계전극(719)을 전기적으로 접속하기 위한 상기 콘택트 홀(882)이 형성되어 있다.

(적층구조 · 제 5 층의 구성 -용량배선 등-)

상기 기술한 제 4 층에 계속하여 제 5 층에는 용량배선(400)이 형성되어 있다.

이 용량배선(400)은 평면적으로 보면, 도 5에 나타내는 바와 같이 도면 중 X 방향 및 Y 방향으로 각각 연장되도록 격자형으로 형성되어 있다. 그 용량배선(400)중 도면 중 Y 방향으로 연장된 부분에 대해서는 특히, 데이터선(6a)을 덮도록, 또한 그 데이터선(6a)보다도 크게 형성되어 있다. 또한, 도면 중 X 방향으로 연장된 부분에 대해서는, 후술하는 제 3 용계전극(402)을 형성하는 영역을 확보하기 위해, 각 화소전극(9a)의 1변의 중앙부근에 노치부를 가지고 있다.

나아가, 도 5 중 XV 방향으로 각각 연장된 용량배선(400)의 교차부분의 모퉁이부에 있어서는, 그 모퉁이부를 에우도록 하여 대략 삼각형의 부분이 형성되어 있다. 용량배선(400)에, 이 대략 삼각형의 부분이 형성되어 있음으로써, TFT(30)의 반도체층(1a)에 대한 광의 차폐가 효과적으로 행할 수 있다. 즉, 반도체층(1a)에 대해 비스듬하게 위로부터 진입하고자 하는 광은, 이 삼각형 부분에서 반사 또는 흡수되어 반도체층(1a)에는 이르지 않게 된다. 따라서, 광리크전류의 발생을 억제하여, 플리커 등이 없는 고품질 화상을 표시하는 것이 가능해진다.

이 용량배선(400)은, 화소전극(9a)이 배치된 화상표시영역(10a)으로부터 그 주위로 연장형성되어, 대향전극전위나 구동회로 또는 기타 주변회로의 정전위원과 전기적으로 접속됨으로써 고정전위로 되어 있다 (후술하는 배선(404)에 관한 설명 참조).

이와 같이, 데이터선(6a) 전체를 덮도록 형성되어 있음과 동시에, 고정전위로 된 용량배선(400)의 존재에 의하면, 그 데이터선(6a) 및 화소전극(9a) 사이에 발생하는 용량커플링의 영향을 배제하는 것이 가능해진다. 즉, 데이터선(6a)에으로 인가된 전기에 반응하여 화소전극(9a)의 전위가 변동하는 사태를 미연에 회피하는 것이 가능해져, 화상상에 그 데이터선(6a)을 따른 표시편차 등을 발생시킬 가능성을 저감할 수 있다. 제 1 실시 형태에서는 더하, 용량배선(400)은 격자형으로 형성되어 있으므로, 주사선(11a)이 연장된 부분에 대해서도 필요없는 용량커플링이 생기지 않도록 이것을 억제하는 것이 가능해졌다.

또한, 제 5 층에는 이러한 용량배선(400)과 동일막으로 제 3 용계전극(402)이 형성되어 있다. 이 제 3 용계전극(402)은, 후술하는 콘택트 홀(804 및 89)을 통해, 제 2 용계전극(6a2) 및 화소전극(9a) 사이의 전기적 접속을 용계하는 기능을 갖는다. 또, 이들 용량배선(400) 및 제 3 용계전극(402) 사이는, 평면형상적으로 연속하여 형성되어 있는 것은 아니고, 양자간은 패터닝상 분단되도록 형성되어 있다.

한편, 상기 기술한 용량배선(400) 및 제 3 용계전극(402)은, 하층에 알루미늄으로 이루어진 층, 상층에 질화 티탄으로 이루어진 층의 2층 구조를 갖고 있다. 이와 같이 용량배선(400) 및 제 3 용계전극(402)은, 광반사성능이 비교적 뛰어난 알루미늄을 포함하고, 또한 광흡수성능이 비교적 뛰어난 질화 티탄을 포함하기 때문에, 그 용량배선(400) 및 그 제 3 용계층(402)은 차광층으로서 기능할 수 있다. 즉, 이들에 의하면, TFT(30)의 반도체층(1a)에 대한 입사광(도 6참조)의 진행을 그 상층에서 차단하는 것이 가능하다.

그리고, 제 1 실시 형태에 있어서는 특히, 화상표시영역(10a) 이외의 영역에, 도 7(a) 및 도 7(b)에 나타내는 바와 같이, 상기 기술한 용량배선(400)에 연장형성된 플러스측 배선, 보다 상세하게는, 배선(404; 본 명세서에서 말하는 「제 2 배선」의 일례에 해당함) 및 프레임패턴(405)으로 이루어진 회전배선이 형성되어 있다. 이하에서는, 이 회전배선의 구성에 대해 상기까지 언급했던 각 도면 및 도 8을 참조하면

서 설명한다. 여기서 도 8은, 도 1과 동일한 취지의 도면으로서, 특히 배선(404) 및 프레임패턴(405)으로 이루어진 회절배선과 용량배선(400)과의 배치관계를 명료하게 도시하기 위한 도면이다. 또, 도 8에 있어서는, 상기 목적을 위하여, 특히 배선(404)의 윤곽 또는 프레임패턴(405)의 윤곽, 평면형상 및 배열피치 등에 대해 적절히 시인가능하도록 변경하였고, 또한 도 1 등에 나타난 요소 중의 몇가지(예컨대, 도 1의 데이터선 구동회로(101), 또는 도 9의 제 3 용계전극(402) 등) 도시가 적절히 생략되어 있다.

우선, 주변영역에는 도 7(a) 및 도 8에 나타내는 바와 같이, 용량배선(400)에 프레임패턴(405)을 통해 연장형성된 배선(404)이 형성되어 있다. 즉, 이 배선(404)은, 제 3 층간절연막(43)상에서, 용량배선(400) 및 제 3 용계전극(402: 이하, 「용량배선(400) 등」이라 하는 경우가 있음)과 동일막으로 형성되어 있다. 이에 의해, 배선(404)은 상기 기술한 용량배선(400) 및 제 3 용계전극(402)과 마찬가지로, 하층에 알루미늄으로 이루어진 층, 상층에 질화 티탄으로 이루어진 층의 2층 구조를 갖고 있다.

이 배선(404)의 일부는, 도 1 및 도 2를 참조하여 설명한 외부회로 접속단자(1020)를 구성한다. 구체적으로는, 배선(404)상에 형성된 제 4 층간절연막(44)에 그 배선(404)으로 달하는 콘택트 홀(44H1)이 형성됨으로써, 그 배선(404)의 상부면이 외부로 노출됨으로써 외부회로 접속단자(1020)가 형성된다.

또, 이 때, 콘택트 홀(44H1)의 개구시, 배선(404)의 상층의 질화 티탄으로 이루어진 막을 제거하도 된다. 이에 의해, 그 배선(404)과 외부회로를 전기적으로 접속할 때, 그 외부회로는 하층의 알루미늄으로 이루어진 막과 직접 접속되게 되므로, 접속면에서 저저항화를 실현할 수 있다. 또한, 배선(404) 상층의 질화 티탄으로 이루어진 막을 잔존시킨 채이면, 해당 외부회로 접속단자(1020)를 통해 해당 전기광학장치의 검사를 실시할 때, 그 질화 티탄으로 이루어진 막이 경질의 막이므로, 검사단자가 마모되기 검사하기 어렵다는 문제가 발생하는 것이 우려되지만, 그 질화 티탄으로 이루어진 막을 제거하면 그와 같은 문제없이 끝난다.

덧붙이면, 도 7(a)에 나타내는 배선(404)은, 도 1에 나타내는 외부회로 접속단자(102)의 전부에 대해 동일하게 형성되어 있지만, 그들 중 용량배선(400)에 연장형성되어 있는 것, 즉 그 용량배선(400)과 전기적인 연락이 도모되고 있는 것은 그들 중의 일부이다. 즉, 도 8 또는 도 1에 나타내는 바와 같이, 외부회로 접속단자(102) 중 특정한 외부회로 접속단자(1020)에 대응하는 배선(404)만이 용량배선(400)과 연장되어 형성되게 되어 있고, 나머지 외부회로 접속단자(102)에 대응하는 배선(404)에 대해서는, 용량배선(400) 등과 동일막으로 형성되어 있지만, 양자는 패터닝상 분단되도록 형성되어 있다.

한편, 제 1 실시 형태에 있어서는 또한, 도 7(b) 및 도 8에 나타내는 바와 같이, 상기 용량배선(400) 등, 그리고 상기 기술한 배선(404)에 연장형성된 프레임패턴(405)이 형성되어 있다. 즉, 이 프레임패턴(406)은, 제 3 층간절연막(43)상에서, 용량배선(400) 등 및 프레임패턴(405)과 동일막으로 형성되어 있다. 이에 의해, 프레임패턴(406) 또한 상기 기술한 용량배선(400) 등과 마찬가지로, 하층에 알루미늄으로 이루어진 층, 상층에 질화 티탄으로 이루어진 층의 2층 구조를 갖고 있다.

프레임패턴(405)은 도 8에 나타내는 바와 같이, 평면으로 볼 때 화상표시영역(10a)과 주변영역(특히 구체적으로는 프레임영역(즉, 프레임차광막(53)의 형성영역에 대응하는 영역) 및 그 프레임영역 주위의 시험재(52)의 형성영역을 메우도록, 또는 화상표시영역(10a)의 주위 전부를 둘러싸도록 형성되어 있어, 전체적으로 대략 ㅁ 자 형상을 가지고 있다. 이 프레임패턴(406)은 도 8 중 하층에 나타내는 바와 같이, 상기 특정한 외부회로 접속단자(1020)에 접속된 배선(404)에 연장형성되어 있으므로, 프레임패턴(405) 및 특정한 외부회로 접속단자(1020)는 서로 전기적으로 접속되어 있다. 또한, 프레임패턴(405)은 용량배선(400)에 연장형성됨으로써, 그 용량배선(400) 및 특정한 외부회로 접속단자(1020) 또한 서로 전기적으로 접속되어 있다. 이상에 의해, 결국 특정한 외부회로 접속단자(1020)에 접속된 배선(404), 프레임패턴(406) 및 용량배선(400)은 항상 등전위가 된다.

또한, 프레임패턴(406)의 일부는 도 7(b)에 나타내는 바와 같이, 콘택트 홀(44H2)에 의해 외부로 노출된 후, 상하도통재(106)를 포함하는 시험재(52)가 올려짐으로써, 프레임패턴(405) 및 대향전극(21) 사이에도 전기적 접속이 실현되게 되었다(프레임패턴(406)상, 상하도통재(106)와 접속하는 부분을 접속부분(406C)으로 하기로 함). 이 접속부분(406C)은 도 1을 참조하여 설명했듯이, 상하도통재(106)가 대향기판(20)의 4개의 코너부에 배치됨에 따라, 해당 4개의 코너부에 형성되게 된다.

이상에 의해, 제 1 실시 형태에 있어서는, 특정한 외부회로 접속단자(1020)에 접속된 배선(404), 프레임패턴(406), 용량배선(400) 및 대향전극(21)은 항상 등전위가 된다.

또, 콘택트 홀(44H2)의 개구시에는, 프레임패턴(406)의 상층의 질화 티탄으로 이루어진 막을 제거하도 된다. 이에 의해, 상하도통재(106)는, 그 프레임패턴(406)의 하층의 알루미늄으로 이루어진 막과 직접 접속되게 되므로, 접속면에서 저저항화를 실현할 수 있다. 또한, 질화 티탄으로 이루어진 막이 존재하면, 그 질화 티탄으로 이루어진 막은 경질의 막이므로 상하도통재(106)가 매립되지 않고, 접속면적이 작아져 저항치가 커진다는 문제가 발생하는 것이 우려되지만, 그 질화 티탄으로 이루어진 막을 제거하면 그와 같은 문제없이 끝난다.

또, 도 7에 있어서는, 화상표시영역에 형성되는 주사선(11a)과 동일막으로 단차조정막(11aP)이 형성되고, 또한 게이트전극(3a) 및 용계전극(719)과 동일막으로 단차조정막(3aP)이 형성되어 있다. 이들 단차조정막(11aP 및 3aP)의 존재에 의해, 화상표시영역과 주변영역에서의 적층구조의 전체 높이를 거의 동일하게 하는 등의 조정을 행할 수 있다.

(적층구조 -제 4 층 및 제 5 층 사이의 구성 -제 3 층간절연막-)

도 6에 나타내는 바와 같이, 데이터선(6a)의 위, 그리고 용량배선(400) 아래에는, NSG, PSG, BSG, BPSG 등의 실리케이트 유리막, 질화 규소막이나 산화 규소막 등, 또는 바람직하게는, TEOS 가스를 사용한 플라즈마 CVD법으로 형성된 제 3 층간절연막(43)이 형성되어 있다. 여 제 3 층간절연막(43)에는, 상기 용량배선(400)과 용량배선용 용계층(6a1)을 전기적으로 접속하기 위한 콘택트 홀(803) 및 제 3 용계전극(402)과 제 2 용계전극(6a2)을 전기적으로 접속하기 위한 콘택트 홀(804)이 각각 개공되어 있다.

(적층구조 : 제 6 층 및 제 5 층 및 제 6 층 사이의 구성 -화소전극 등-)

마지막으로 제 6 층에는, 상기 기술한 바와 같이 화소전극(9a)이 매트릭스형으로 형성되고, 그 화소전극(9a)상에 배향막(16)이 형성되어 있다. 그리고, 이 화소전극(9a) 아래에는, NSG, PSG, BSG, BPSG 등의 실리케이트 유리막, 질화 규소막이나 산화 규소막 등, 또는 바람직하게는 NSG로 이루어진 제 4 층간절연막(44)이 형성되어 있다. 이 제 4 층간절연막(44)에는, 화소전극(9a) 및 상기 제 3 층계전극(402) 사이를 전기적으로 접속하기 위한 콘택트 홀(89)이 개공되어 있다. 화소전극(9a)과 TFT(30) 사이는, 이 콘택트 홀(89) 및 제 3 중계층(402) 및 상기 기술한 콘택트 홀(804), 제 2 중계층(6a2), 콘택트 홀(882), 중계전극(719), 콘택트 홀(881), 하부전극(71) 및 콘택트 홀(83)을 통해 전기적으로 접속되게 된다.

또한, 제 1 실시 형태에서는, 제 4 층간절연막(44)의 표면은, CMP(Chemical Mechanical Polishing)처리 등에 의해 평탄화되어 있고, 그 하층에 존재하는 각종 배선이나 소자 등에 의한 단차에 기인하는 액정층(50)의 배향 불량을 저감한다. 단, 이와 같이 제 4 층간절연막(44)에 평탄화처리를 실시하는 대신, 또는 그에 더하여 TFT 어레이기판(10), 하지절연막(12), 제 1 층간절연막(41), 제 2 층간절연막(42) 및 제 3 층간절연막(43) 중 적어도 하나에 홈을 만들고 데이터선(6a) 등의 배선이나 TFT(30) 등을 매몰으로써 평탄화처리를 해도 된다.

(해당 전기광학장치의 작용효과)

이상과 같은 구성이 되는 제 1 실시 형태의 전기광학장치에 의하면, 특히 제 5 층의 구성으로서 설명한 배선(404) 및 프레임패턴(405)으로 이루어진 화전배선이 형성되어 있으므로, 다음과 같은 작용효과가 나타나게 된다.

먼저 첫째로, 제 1 실시 형태에 있어서는, 프레임패턴(406)이 프레임영역 및 시현영역에 형성되어 있으므로, 이 프레임패턴(406)이 형성되어 있는 영역에 있어서는, 도 7(b)의 화살표 L1로 나타내는 바와 같이, 광누설이 생기는 것을 미연에 방지하는 것이 가능하므로, 화상의 주위에 각종 배선 등의 패턴 이미지가 비치는 것 등을 방지하는 것이 가능해진다. 따라서, 제 1 실시 형태에 의하면, 보다 고품질의 화상을 표시하는 것이 가능해진다.

특히, 제 1 실시 형태에 관한 프레임패턴(406)은, 화상표시영역(10a)의 주위 전부를 둘러싸도록 형성되어 있으므로, 원리상으로는, 프레임영역 또는 시현영역을 투과하는 광을 완전히 차단하는 것도 가능하다. 또한, 프레임패턴(406)은, 하층에 알루미늄으로 이루어진 층, 상층에 흑화 티탄으로 이루어진 층(모두 본 발명에서 말하는 「차광성 재료」의 일례에 해당함)의 2층 구조를 갖는 점에서, 상기 광차폐작용은 보다 확실하게 발휘된다. 또한, 프레임패턴(406)은, 도 8에서 명확하듯이, 화상표시영역(10a)에 겹치지 않게 형성되어 있으므로, 그 프레임패턴(406)이 화상표시영역(10a)을 투과하는 광의 방해가 되는 경우가 없다. 요컨대, 화상은 원하는대로 표시하는 것이 가능하다. 또, 시일재(52)가 광경화성 수지 등으로 이루어진 경우에 있어서는, 그 경화시에 필요한 광조사는, 도 7(b)의 상측으로부터, 즉 대향기판(20) 측으로부터 행하도록 하면 된다.

또한, 이와 관련하여 제 1 실시 형태에 있어서는, 대향기판(20)상에 프레임차광막(53)이 형성됨으로써 도 7(b)의 화살표 L2에 나타내는 차광도 실현되게 된다. 이 경우, 가령 프레임차광막(53)을 투과하는 광이 있다 하더라도, 그 광은 다음에 대기하는 프레임패턴(406)에 의해 반사 또는 흡수되게 된다. 이와 같이 제 1 실시 형태에 의하면 이른바 2중 차광을 실현할 수 있다.

또한 둘째로, 제 1 실시 형태에 관한 프레임패턴(406)은, 상하도통재(106)를 통해 대향전극(21)과 전기적 접속이 도모됨과 동시에, 용량배선(400)과도 전기적 접속이 도모되고 있으므로, 그 프레임패턴(406)은 상기 기술한 광누설 방지작용의 기능과 더불어, 대향전극(21)에의 전위공급, 및 용량배선(400), 나아가 용량전극(300)에의 전위공급(이 전위공급은, 콘택트 홀(80)및 803) 및 용량배선용 중계층(6a1)을 통해 실시됨, 도 6참조)의 기능도 가지고 있다. 이에 의해, 장치구성의 간략화가 실현된다.

이와 관련하여, 상하도통재(106)의 배치 개소(箇所)는, 도 8 및 도 10에 나타내는 바와 같이 화상표시영역(10a)의 네 모퉁이에 대응하도록 되어 있으므로, 프레임패턴(405) 및 대향전극(21)사이의 전기적 접속을 적절하게 실현하면서도, 이것이 화상표시를 방해하는 경우가 없다. 게다가, 프레임패턴(405)은, 화상표시영역(10a)의 주위 전부를 둘러싸도록 형성되어 있으므로, 그 프레임패턴(406)과 대향전극(21)과의 전기적 접속을 보다 확실하게 이룰 수 있다. 이것은, 프레임패턴(406)의 모든 부분이 전기적으로 접속되어 있는(바꾸어 말하면, 연속적인 패턴으로 형성되어 있는) 것, 또한 접속부분(406C)은, 화상표시영역(10a)의 네 모퉁이, 즉 프레임패턴(406)의 네 모퉁이에 대응하도록 복수 형성되어 있으므로, 설령 프레임패턴(406)의 일부, 또는 4개의 상하도통재(106) 중 어느 하나가 임의의 사정에 의해 전기적으로 도통불능이 된 경우라 하더라도, 다른 부분에 의해 전기적 도통을 지체없이 실현하는 것이 가능하기 때문이다.

이상으로부터, 제 1 실시 형태에 의하면, 대향전극(21)의 전위를 매우 안정적으로 유지하는 것이 가능해지고, 그 대향전극(21) 및 화소전극(9a) 사이에 협지되는 액정층(50)내의 액정분자의 배향상태의 조정을 적절히 행할 수 있으므로, 보다 고품질의 화상을 표시하는 것이 가능해진다.

또, 제 1 실시 형태에 있어서는 도 8에 나타낸 바와 같이, 프레임패턴(406)에 접속되는 외부회로 접속단자(1020)는 도면 중 좌우에 2개 형성되게 되어 있지만 본 발명은 이러한 형태에 한정되지 않는다. 예컨대, 도면 중 좌 및 우 중 어느 한쪽에만 프레임패턴(406)에 접속되는 외부회로 접속단자(1020)가 형성되는 형태를 채택해도 된다.

한편, 제 1 실시 형태에 있어서는, 상기와 같이 대향전극(21) 및 용량배선(400)에의 전위공급기능을 갖는 프레임패턴(405)은, 배선(404)의 일부, 즉 측정한 외부회로 접속단자(1020)와 접속된 배선(404)과 동일막으로, 또한 전기적으로 접속되도록 형성되어 있으므로, 이들 각 요소가, 예컨대 각각 별도의 층으로 형성되며 콘택트 홀 등에 의해 전기적인 접속이 도모되고 있는 경우에 비해, 그 각 요소간의 전기저항치를 저하시킬 수 있다. 따라서, 대향전극(21)에의 안정된 전위의 공급이 실현될 뿐 아니라, 용량배선(400)

등의 고저항화에 기인하는 크로스토크의 발생 등을 방지할 수 있다.

이와 관련하여, 제 1 실시 형태에 있어서는, 배선(404) 및 용량배선(400)은 데이터선(6a) 위에 제 3 층간 절연막(43)을 통해 형성되어 있다. 이에 의해, 배선(404) 및 용량배선(400)을 동일막으로 형성한다는 것과, 외부회로 접속단자(102)는 외부로 노출되어야 한다는 요청, 및 배선(404) 및 외부회로 접속단자(102)사이에서 전기적 연락을 도모해야 한다는 요청을 비교적 용이하게 달성하는 것이 가능해진다(도 7(a)참조). 또한, 제 1 실시 형태에서는 특히, 배선(404) 및 용량배선(400)은, 모두 화소전극(9a)을 포함하는 제 6 층의 바로 아래, 즉 그 화소전극(9a)과의 사이에 제 4 층간절연막(44)만을 통해 형성되어 있으므로, 상기 기술한 작용효과는 보다 효과적으로 나타나게 된다.

즉, 이러한 구성에 의해, 외부회로 접속단자(102)를 구성하기 위한 콘택트 홀(44H1)은, 도 7(a)에 나타내는 바와 같이 제 4 층간절연막(44)에 대해서만 형성하면 되므로, 그 심도는 비교적 얕고, 그 콘택트 홀(44H1)의 형성은 비교적 용이해지는 것이다.

[제 2 실시 형태]

이하에서는, 본 발명의 제 2 실시 형태에 대해 도 9 내지 도 11을 참조하면서 설명한다. 여기서 도 9는, 도 8과 동일한 취지의 도면으로서, 프레임패턴의 형성태양에 다른 것이다. 단, 도 9에 있어서는 도 8과는 달리, 용량배선(400)에 관한 도시도 생략하고 있다. 또한, 도 10 및 도 11은, 도 9에 나타내는 부호 D 부근을 확대하고, 또한 해당 부분에서의 회로구성 등을 함께 나타내는 설명도이다. 또, 제 2 실시 형태에서는, 상기 기술한 제 1 실시 형태의 전기광학장치의 전체 구성, 화소부의 구성 등의 거의 모든 부분에 대해서는 완전히 동일하다. 따라서, 이하에서는 제 1 실시 형태와 동일한 부분에 대한 설명은 생략하고, 주로, 제 2 실시 형태에 특징적인 구성에 대해서만 설명을 추가하기로 한다.

도 9에 있어서는, 프레임패턴(461A 및 461B)으로 이루어진 프레임패턴(461)이 형성되어 있다. 이 중 프레임패턴(461A)은, 본 발명에서 말하는 「제 1 패턴」의 일례에 해당하고, 도 9에 나타내는 바와 같이, 직사각형을 갖는 화상표시영역(10a)의 3변(도면 중, 상변 및 좌변 및 우변)을 따라 연속하여 형성되어 있다. 또한, 프레임패턴(461B)은, 본 발명에서 말하는 「제 2 패턴」의 일례에 해당하고, 화상표시영역(10a)의 나머지 1변(도면 중 하변)을 따라 형성됨과 동시에 상기 프레임패턴(461A)과 분단되어 형성되어 있다(도면 중 부호 461B 참조). 그리고, 상하도통재(106)는 이들 중 프레임패턴(461A)상에 존재한다.

이러한 형태에 의하면, 상기 기술한 제 1 실시 형태와 마찬가지로, 프레임패턴(461A) 및 그 위의 4개의 상하도통재(106)에 대해 용장적인 구조가 채택됨으로써, 프레임패턴(461) 및 대향전극(21) 사이의 전기적 접속을 보다 확실하게 이룰 수 있고, 대향전극(21)의 전위를 매우 안정적으로 유지하는 것이 가능해진다. 또한, 프레임패턴(461A 및 461B)의 존재에 의해, 광누설 방지의 작용효과가 얻어지는 것도 상기 기술한 제 1 실시 형태와 동일하다.

또한, 제 2 실시 형태에 있어서는 특히, 프레임패턴(461B)에 의해 다음과 같은 작용효과가 얻어진다. 즉, 제 2 실시 형태에서는, 프레임패턴(461B)은 도 9에 있어서 도시가 생략되어 있는 데이터선 구동회로(101; 도 1참조)가 형성되는 영역에 대응하여 형성되어 있다.

이 데이터선 구동회로(101) 부근의 구성은 도 10에 나타내는 바와 같이 되어 있다.

즉, 데이터선 구동회로(101)로부터 인출된 제어선(114)은, 샘플링회로(118)를 구성하는 스위칭소자(202)의 게이트에 접속되어 있다.

한편, 스위칭소자(202)의 소스에는, 인출배선(116)을 통해 화상신호선(115)이 접속되어 있고, 그 드레인에는 데이터선(6a)이 접속되어 있다. 이에 의해, 데이터선 구동회로(101)에 의해 스위칭소자(202)의 ON·OFF가 제어됨으로써, 화상신호선(115)으로부터 데이터선(6a)에의 화상신호의 공급의 유무가 제어된다.

그러나, 이러한 구성을 구비하고 있는 데이터선 구동회로(101)부근의 구성에서는, 상기 인출배선(116)과, 대향기판(20)상의 대향전극(21) 사이에서 용량커플링이 발생할 우려가 있는 것이다. 이 용량커플링이 발생하면, 일례에 대한 D전에 의해 타측에서의 전위에 변동을 주기 때문에 희망하는 화상표시가 어려워진다.

그런데, 제 2 실시 형태에 의하면, 해당 영역에는 도 10에 나타내는 바와 같이 상기 프레임패턴(461B)이 형성되어 있으므로, 화상신호선(115) 및 대향전극(21) 사이에는 그 프레임패턴(461B)이 존재하게 되어, 상기 용량커플링의 발생을 억제할 수 있는 것이다. 따라서, 제 2 실시 형태에 의하면, 희망하는 화상을 적절하게 표시할 수 있다. 덧붙이면, 이러한 작용을 보다 효과적으로 얻기 위해서는, 프레임패턴(461B)을 고정전위에 유지해 두는 것이 바람직하다. 그것을 위해서는, 예컨대 그 프레임패턴(461B)을, 도 9에 있어서 도시되지 않은 용량배선(400; 도 8참조)에 접속해 두면 된다.

또, 이러한 작용효과는, 상기 기술한 제 1 실시 형태와 같이, 프레임패턴(406)을 화상표시영역(10a)의 주위 전부를 둘러싸도록 형성하는 태양에 있어서도 동일하게 누릴 수 있다.

또한, 상기 제 2 실시 형태에 있어서는, 프레임패턴(461B)이, 샘플링회로(118) 및 그 샘플링회로(118)로부터 연장되는 인출배선(116)을 거의 전부 덮도록 형성되어 있는데, 본 발명은 여러한 형태에 한정되지 않는다.

예컨대, 도 11에 나타내는 바와 같이, 직사각형으로 분단된 프레임패턴 (461BB)을 형성하도록 해도 된다. 덧붙이면, 이러한 구성을 채택하는 경우에 있어서는, 도 10과는 달리 이들 직사각형의 프레임패턴(461BB)을 고정전위로 유지할 필요는 없고, 플로팅(부유 전위)으로 해 두면 된다.

[제 3 실시 형태]

이하에서는, 본 발명의 제 3 실시 형태에 대해 도 12를 참조하면서 설명한다. 여기서 도 12는 도 8과 동일한 취지의 도면으로서, 프레임패턴의 형성태양이 다른 것이다. 단, 도 12에 있어서는 도 8과는 달리 용량배선(400)에 대한 도시도 생략하고 있다. 제 3 실시 형태에서는, 상기 기술한 제 1 실시 형

태의 전기광학장치의 전체 구성, 화소부의 구성 등의 대부분에 대해서는 완전히 동일하다. 따라서, 이하에서는 제 1 실시 형태와 동일한 부분에 대한 설명은 생략하고, 주로 제 3 실시 형태에 특징적인 구성에 대해서만 설명을 추가하기로 한다.

도 12에 있어서는, 프레임패턴(452C 및 452D)으로 이루어진 프레임패턴(462)이 형성되어 있다. 이 중 프레임패턴(462C)은 본 발명에서 말하는 「제 3 패턴」의 일례에 해당하고, 도 12에 나타내는 바와 같이, 직사각형을 갖는 화상표시영역(10a)의 대응하는 2변(도면 중 좌변 및 우변)을 따라 형성되어 있다. 또한, 프레임패턴(462D)은 본 발명에서 말하는 「제 4 패턴」의 일례에 해당하고, 화상표시영역(10a)의 나머지 2변(도면 중 상변 및 하변)을 따라 형성됨과 동시에 상기 프레임패턴(462C)과 분단되어 형성되어 있다(도면 중 부호 462B 참조).

그리고, 상하도통재(106)는, 이들 중 프레임패턴(462C)상에 존재한다.

이러한 형태에 의하면, 도 12중 화상표시영역(10a)의 좌변 및 우변을 따라, 2개의 직선형 패턴으로 형성된 프레임패턴(462C)에는, 각각 상하도통재(106)가 2개씩 존재하고 있다. 따라서, 이 점에 관해서는 제 1 실시 형태와 마찬가지로, 용장적인 구조가 채택될 수 있다는 점에서, 프리임패턴(462) 및 대향전극(21) 사이의 전기적 접속을 보다 확실하게 이룰 수 있다.

또한, 프레임패턴(462D)에 의하면, 상기 제 2 실시 형태의 프레임패턴(461B)과 마찬가지로, 인출배선(116) 및 대향전극(21) 사이에서의 용량커플링의 발생을 최대한 방지할 수 있다.

물론, 프레임패턴(462C 및 462D)의 존재에 의해, 광누설 방지의 작용효과가 얻어지는 것도 상기 기술한 제 1 실시 형태와 마찬가지이다.

[제 4 실시 형태]

이하에서는, 본 발명의 제 4 실시 형태에 대해 도 13을 참조하면서 설명한다. 여기서 도 13은 도 8과 동일한 취지의 도면으로서, 프레임패턴의 형성태양이 다른 것이다. 단, 도 13에 있어서는 도 8과는 달리 용량배선(400)에 대한 도시도 생략하고 있다. 또, 제 4 실시 형태에서는, 상기 기술한 제 1 실시 형태의 전기광학장치의 전체 구성, 화소부의 구성 등의 거의 모든 부분에 대해서는 완전히 동일하다. 따라서, 이하에서는 제 1 실시 형태와 동일한 부분에 대한 설명은 생략하고, 주로 제 4 실시 형태의 특징적인 구성에 대해서만 설명을 추가하기로 한다.

도 13에 있어서는, 프레임패턴(463E 및 463F)으로 이루어진 프레임패턴(463)이 형성되어 있다. 이 중 프레임패턴(463E)은 본 발명에서 말하는 「제 5 패턴」의 일례에 해당하고, 도 13에 나타내는 바와 같이, 직사각형을 갖는 화상표시영역(10a)의 하나의 모서리부에 대응하는 부분을 제외하고 연속하여 형성되어 있다. 또한, 프레임패턴(463F)은, 본 발명에서 말하는 「제 6 패턴」의 일례에 해당하고 상기 하나의 모서리부에 대응하는 부분에 형성됨과 동시에 상기 프레임패턴(463E)과 분단되어 형성되어 있다(도면 중 부호 463B 참조). 그리고, 상하도통재(105)는, 이들 중 프레임패턴(463E 및 463F) 의 어느 것의 위에도 존재한다.

이러한 형태에 의하면, 상기 제 1 내지 제 3 실시 형태와 거의 동일한 작용효과, 즉 프레임패턴(463) 및 대향전극(21) 사이의 전기적 접속의 확실성, 또는 인출배선(116) 및 대향전극(21) 사이의 용량커플링의 발생억제, 나아가 광누설 방지 등의 작용효과가 거의 동일하게 얻어지는 것이 명백하다.

[제 5 실시 형태]

이하에서는, 본 발명의 제 5 실시 형태에 대해 도 14를 참조하면서 설명한다. 여기서 도 14는 도 8과 동일한 취지의 도면으로서, 프레임패턴의 형성태양 등이 다른 것이다. 또, 제 5 실시 형태에서는, 상기 기술한 제 1 실시 형태의 전기광학장치의 전체 구성, 화소부의 구성 등의 거의 모든 부분에 대해서는 완전히 동일하다. 따라서, 이하에서는 제 1 실시 형태와 동일한 부분에 대한 설명은 생략하고, 주로 제 5 실시 형태의 특징적인 구성에 대해서만 설명을 추가하기로 한다.

우선, 도 14에 있어서는 상기 제 4 실시 형태와 거의 동일한 패턴형상을 갖는 프레임패턴(464)이 형성되어 있다. 즉, 프레임패턴(464)은, 화상표시영역 (10a)의 하나의 모서리부를 제외하고 연속하여 형성된 프레임패턴(464E) 및 상기 하나의 모서리부에 대응하는 부분에 형성된 프레임패턴(464F)으로 이루어진다.

또한, 이들 프레임패턴(464E 및 464F)에는 각각 3개 및 1개의 상하도통재 (105)가 형성되어 있는 것, 그 상하도통재(106)에 전위를 공급하기 위한 배선(404)이 형성되어 있는 것, 및 그 배선(404)의 일부는 특정한 외부회로 접속단자(1020)에 접속되어 있는 것도 상기 제 4 실시 형태와 마찬가지이다. 단, 제 5 실시 형태에 관한 배선(404)은 특히, 본 발명에서 말하는 「제 2 배선의 제 1 부분」의 일례에 해당하고, 특정한 외부회로 접속단자(1020)는, 본 발명에서 말하는 「외부회로 접속단자의 제 1 부분」의 일례에 해당한다.

그리고, 제 5 실시 형태에 있어서, 이 프레임패턴(464E 및 464F)은 용량배선과 전기적으로 접속되어 있지 않다. 즉, 프레임패턴(464)과 용량배선(400')은 동일막으로 형성되어 있기는 하지만, 패터닝상 분단되도록 형성되어 있는 것이다(도면 중 부호 469 참조). 그리고, 이와 같이 프레임패턴(464)으로부터 전위의 공급을 받을 수 없는 용량배선(400')에는 배선(408)이 연장형성되게 되어 있다. 이 배선(408)은, 본 발명에서 말하는 「제 2 배선의 제 2 부분」의 일례에 해당하고, 프리임패턴(464E 및 464F)을 나누는 간극(4648) 사이를 跨재, 특정한 외부회로 접속단자(102R: 본 발명에서 말하는 「외부회로 접속단자의 제 2 부분」의 일례에 해당함)에 접속되어 있다.

이상을 정리하면, 제 5 실시 형태에서는, 배선(404), 프레임패턴(464), 배선(408) 및 용량배선(400')은 모두 동일막으로 형성되어 있는데(제 3 중계전극(402)을 포함함), 배선(404)과 프레임패턴(464) 사이 및 배선(408)과 용량배선(400') 사이 각각에 대해서는 전기적 접속이 도모되고 있지만, 전자 및 후자 사이에는 전기적인 연락이 이루어지지 않는다.

이러한 형태에 의하면, 대향전극(21)과, 용량배선(400'), 나아가 용량전극(300)에 부여하는 전위를 다르게 할 수 있다. 즉, 대향전극(21)은, 상하도통재(106)를 통해 프레임패턴(464), 배선(404), 특정한 외부회로 접속단자 (1020)에 접속되어 있으므로, 그 외부회로 접속단자(1020)에 대향전극(21)용 전위를 공급하면, 대향전극(21)을 해당 전위로 유지할 수 있다. 한편, 용량배선(400'), 나아가 여기에 전기적으로 접속되어 있는 용량전극(300; 도 6참조)은, 배선(408), 특정한 외부회로 접속단자(102R)에 접속되어 있으므로, 그 외부회로 접속단자(102R)에, 상기 대향전극(21)용 전위와는 다른 용량전극(300)용 전위를 공급하면, 그 용량전극(300)을 해당 전위로 유지할 수 있는 것이다. 이와 같이, 제 5 실시 형태에 의하면, 대향전극(21) 및 용량전극(300)을 각각 다른 전위로 유지할 수 있기 때문에, 해당 전기광학장치 내에서 발생하는 각종 전기작용을 적절히 조정하는 것 등이 가능하다.

또, 제 5 실시 형태에 있어서도, 상기 제 1 내지 제 4 실시 형태와 마찬가지로, 프레임패턴(464) 및 대향전극(21) 사이의 확실한 전기적 접속의 확보, 또는 화상선호선(115) 및 대향전극(21) 사이의 용량커플링 발생의 억제, 나아가 광누설 방지 등이 가능한 것에 변함은 없다.

또, 상기 제 2 내지 제 4 실시 형태에 있어서는, 프레임패턴(461, 462 및 463)에는, 상하도통재(106) 및 대향전극(21) 및 용량배선(400)이 전기적으로 접속되어 있으므로, 특정한 외부회로 접속단자(1020)에는, 대향전극(21) 및 용량배선(400) 또는 용량전극(300)에 공통의 전위를 공급할 필요가 있다. 단, 본 발명은 이러한 형태에 한정되지 않는다. 즉, 제 5 실시 형태로서 서술한 바와 같이, 상기 제 2 내지 제 4 실시 형태에 있어서도, 프레임패턴(461, 462 및 463)을 구성하는 간극(4618, 4628 및 4638)을 이용하여, 용량배선(400) 또는 용량전극(300)용 전위를, 대향전극(21)용 전위와는 별개로 공급하도록 해도 된다.

또한, 상기 제 1 내지 제 5 실시 형태에 있어서는, 특정한 외부회로 접속단자(1020 또는 102R)에 공급되는 전위를, 주사선 구동회로(104)에 공급되는 저전위측 정전위로서 이용해도 된다. 이에 의하면, 대향전극(21), 용량전극(300)의 전위는, 해당 정전위와 동일해진다. 또는, 상기 기술한 구성 대신, 외부회로 접속단자(1020 또는 102R)에 공급되는 전위를, 데이터선 구동회로(101)에 공급되는 정전위로서 사용해도 관계없다.

(전자기기)

다음에, 이상 상세히 설명한 전기광학장치를 라이트벌브로 사용한 전자기기의 일례인 투사형 컬러표시장치의 실시 형태에 대하, 그 전체 구성, 특히 광학적인 구성에 대해 설명한다. 여기서 도 15는, 투사형 컬러표시장치의 도식적 단면도이다.

도 15에 있어서, 본 실시 형태에서의 투사형 컬러표시장치의 일례인 액정프로젝터(1100)는, 구동회로가 TFT 어레이기판상에 탑재된 액정장치를 포함하는 액정모듈을 3개 준비하여, 각각 RGB용 라이트벌브(100R, 100G 및 100B)로 사용한 프로젝터로서 구성되어 있다. 액정프로젝터(1100)에서는, 메탈할로겐 램프 등의 백색 광원의 램프유닛(1102)으로부터 투사광이 발생하면, 3장의 미러(1106) 및 2장의 다이크로익 미러(1108)에 의해, RGB의 삼원색에 대응하는 광성분 R, G 및 B로 나누어지고, 각 색에 대응하는 라이트벌브(100R, 100G 및 100B)로 각각 안내된다. 이 때 특히, B광은 긴 광로에 의한 광손실을 방지하기 위해, 입사렌즈(1122), 릴레이렌즈(1123) 및 출사렌즈(1124)로 이루어진 릴레이렌즈계(1121)를 통해 안내된다. 그리고, 라이트벌브(100R, 100G 및 100B)에 의해 각각 변조된 삼원색에 대응하는 광성분은, 다이크로익 프리즘(1112)에 의해 다시 합성된 후, 투사렌즈 (1114)를 통해 스크린(1120)에 컬러화상으로 투사된다.

본 발명은 상기 기술한 실시 형태에 한정되는 것은 아니고, 청구범위 및 명세서 전체로부터 파악할 수 있는 발명의 요지, 또는 사상에 반하지 않는 범위에서 적절히 변경가능하며, 그와 같은 변경을 수반하는 전기광학장치 및 전자기기 또한 본 발명의 기술적 범위에 포함되는 것이다.

발명의 효과

용량커플링의 발생을 억제하여 화상에 플리커 등이 발생하는 것을 미연에 방지하여 원하는 화상을 적절하게 표시할 수 있으며, 프레임패턴은 광누설 방지 기능이 있고, 대향전극에의 전위공급, 및 용량배선, 나아가 용량전극에의 전위공급의 기능도 가지고 있어 장치구성이 간략해진다. 또한 대향전극에의 안정된 전위의 공급이 실현될 뿐 아니라, 용량배선 등의 고저항화에 기인하는 크로스토크의 발생 등을 방지할 수 있다.

화상의 주위에 각종 배선 등의 패턴 이미지가 비치는 것 등이 미연에 방지됨으로써, 고품질의 화상에 표시가능한 각종 전자기기를 실현할 수 있다.

[57] 청구의 범위

청구항 1

기판 위에,

임장한 방향으로 연장되는 데이터선 및 상기 데이터선에 교차하는 방향으로 연장되는 주사선;

상기 주사선에 의해 주사신호가 공급되는 스위칭소자;

상기 데이터선에 의해 상기 스위칭소자를 통해 화상신호가 공급되는 화소전극;

상기 기판에 있어서, 상기 화소전극 및 상기 스위칭소자의 형성영역으로서 규정되는 화상표시영역;

상기 화상표시영역의 주변을 규정하는 주변영역;,

상기 화상표시영역 위에,

상기 화소전극에서의 전위를 소정 기간 유지하는 축적용량;

상기 축적용량을 구성하는 용량전극에 소정 전위를 공급하는 제 1 배선; 및

상기 제 1 배선과 동일막으로 형성되고, 상기 화상표시영역과 상기 주변영역을 구획하는 프레임영역의 적어도 일부를 구성하는 프레임패턴을 구비한 것을 특징으로 하는 전기광학장치.

청구항 2

제 1 항에 있어서,

상기 프레임패턴은 데이터선에 화상신호를 공급하기 위한 샘플링회로를 적어도 덮도록 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 3

제 1 항에 있어서,

상기 제 1 배선은 상기 소정 전위가 공급되는 복수의 용량전극과 동일막으로서, 상기 용량전극이 연장되어 형성된 것을 특징으로 하는 전기광학장치.

청구항 4

제 1 항에 있어서,

상기 프레임패턴의 적어도 일부는 직사각형상으로 분단되어 형성되어 부유 전위로 되는 것을 특징으로 하는 전기광학장치.

청구항 5

제 1 항에 있어서,

상기 기판에 대향배치되는 대향기판; 및

상기 기판과 상기 대향기판을 접착하는 시일재를 더 구비하고,

상기 프레임패턴은 상기 시일재가 형성되는 시일영역의 적어도 일부에 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 6

제 1 항에 있어서,

상기 기판에 대향배치되는 대향기판; 및

상기 대향기판 위에 형성되는 대향전극을 더 구비하고,

상기 프레임패턴은 상기 대향전극과 전기적으로 접속되어 있는 접속부분을 가지는 것을 특징으로 하는 전기광학장치.

청구항 7

제 1 항에 있어서,

상기 프레임패턴은 상기 제 1 배선과 전기적으로 접속하도록 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 8

제 6 항에 있어서,

상기 접속부분은 상기 대향기판의 코너부에 대응하여 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 9

제 1 항에 있어서,

상기 프레임패턴은 상기 화상표시영역의 주위 전부를 둘러싸도록 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 10

제 6 항에 있어서,

상기 화상표시영역은 평면으로 볼 때 직사각형상을 가지며,

상기 프레임패턴은, 상기 직사각형상의 3변을 따라서 연속하여 형성된 제 1 패턴과, 나머지 1변을 따라서 형성됨과 동시에 상기 제 1 패턴과 분단되어 형성된 제 2 패턴을 포함하고,

상기 접속부분은 상기 제 1 패턴 상에 존재하는 것을 특징으로 하는 전기광학장치.

청구항 11

제 6 항에 있어서,

상기 화상표시영역은 평면으로 볼 때 직사각형상을 가지며,

상기 프레임패턴은, 상기 직사각형상의 대향하는 2 변을 따라서 형성된 제 3 패턴과 나머지 2 변을 따라 형성됨과 동시에 상기 제 3 패턴과 분단되어 형성된 제 4 패턴을 포함하고,

상기 접속부분은 상기 제 3 패턴 상에 존재하는 것을 특징으로 하는 전기광학장치.

청구항 12

제 6 항에 있어서,

상기 화상표시영역은 평면으로 볼 때 직사각형상을 가지며,

상기 프레임패턴은, 상기 직사각형상의 하나의 모서리부에 대응하는 부분을 제외하고 연속하여 형성된 제 5 패턴과, 상기 하나의 모서리부에 대응하는 부분에 형성됨과 동시에 상기 제 5 패턴과 분단되어 형성된 제 6 패턴을 포함하고,

상기 접속부분은 상기 제 5 패턴 및 상기 제 6 패턴의 적어도 일측 상에 존재하는 것을 특징으로 하는 전기광학장치.

청구항 13

제 1 항에 있어서,

상기 주변영역 위에,

상기 기판의 변 가장자리부를 따라서 형성된 외부회로 접속단자와 상기 외부회로 접속단자에 연장형성된 제 2 배선을 더 구비하고,

상기 제 2 배선의 적어도 일부는 상기 제 1 배선과 동일막으로 형성되고, 상기 제 1 배선과 전기적으로 접속되어 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 14

제 13 항에 있어서,

상기 제 1 배선은 상기 데이터선 위에 층간절연막을 개재하여 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 15

제 13 항에 있어서,

상기 제 1 배선은 상기 화소전극을 포함하는 층의 바로 아래층에 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 16

제 13 항에 있어서,

상기 제 1 배선과 상기 프레임패턴은 전기적으로 접속되어 형성되어 있지 않고,

상기 제 2 배선의 제 1 부분과 상기 제 1 배선이 전기적으로 접속되고,

상기 제 2 배선의 제 2 부분과 상기 프레임패턴이 전기적으로 접속되어 있고,

상기 제 1 부분은 상기 외부회로 접속단자의 제 1 부분에,

상기 제 2 부분은 상기 외부회로 접속단자의 제 2 부분에 각각 접속되어 있는 것을 특징으로 하는 전기광학장치.

청구항 17

제 1 항에 있어서,

상기 제 1 배선은 차광성 재료로 구성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 18

제 1 항에 있어서,

상기 제 1 배선은 상이한 재료로 이루어진 적층구조를 갖는 것을 특징으로 하는 전기광학장치.

청구항 19

제 1 항에 있어서,

상기 기판에 대향배치되는 대향기판; 및

상기 대향기판 위에 형성된 차광막을 더 구비하여 이루어지고,

상기 프레임패턴은, 상기 차광막과 겹치도록 형성되어 있는 것을 특징으로 하는 전기광학장치.

청구항 20

제 19 항에 있어서,

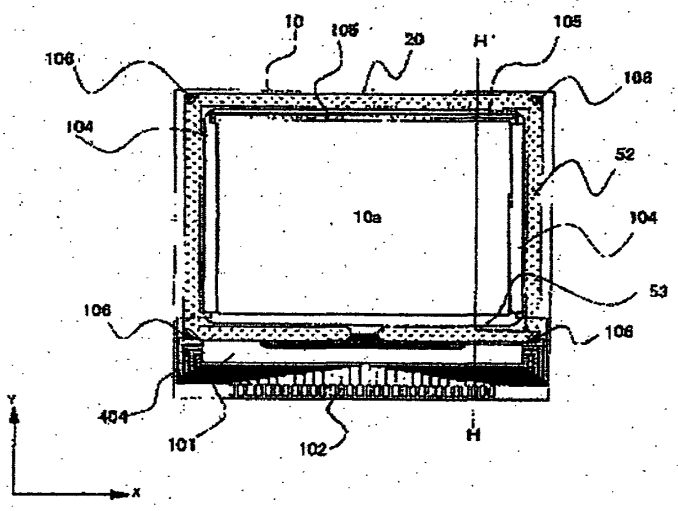
상기 차광막은 상기 대향기판의 변 가장자리부를 따라서 형성된 프레임차광막을 포함하는 것을 특징으로 하는 전기광학장치.

청구항 21

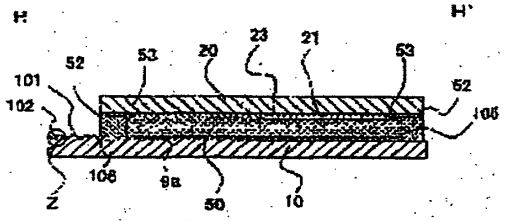
제 1 항 내지 제 20 항 중 어느 한 항에 기재된 전기광학장치를 구비하여 이루어진 것을 특징으로 하는 전자기기.

도면

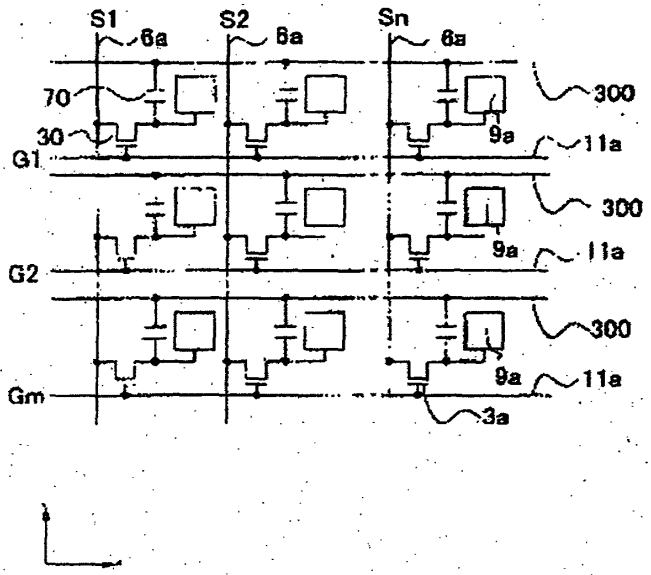
도면1



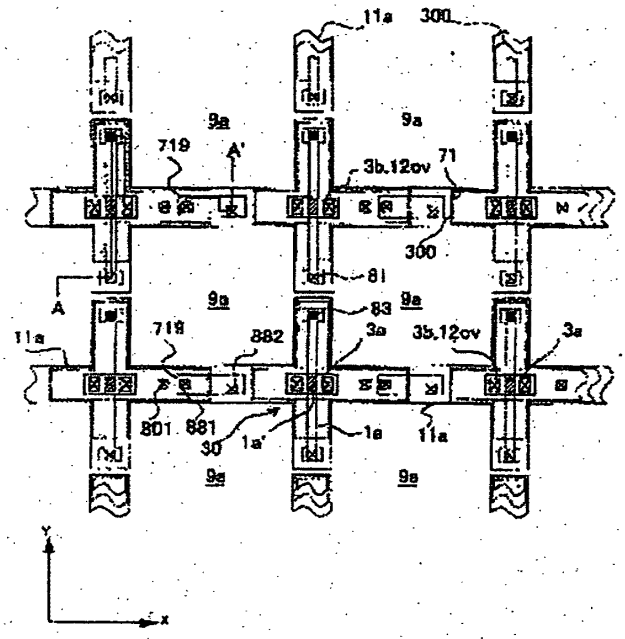
도면2



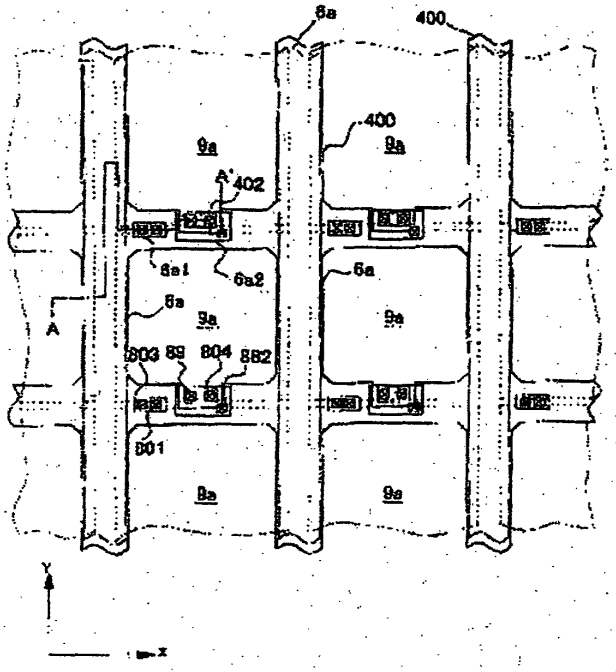
도면3



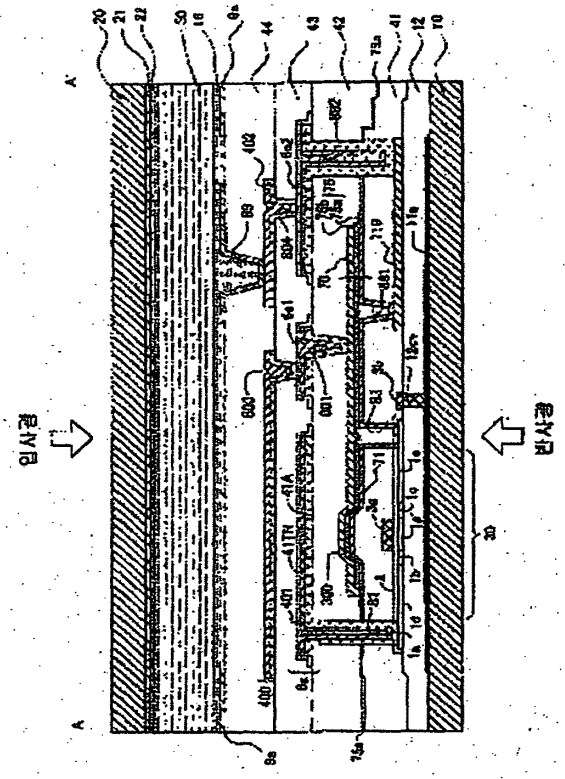
도면4


11a
300
9a
719
A'
3b,12ov
71
300
81
A
9a
83
9a
719
882
3a
35,12ov
3a
11a
801
681
30
1a'
1a
11a
9a
9a
Y
X

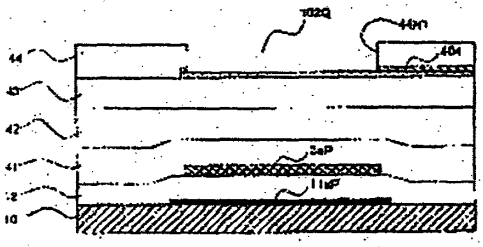
도면5


6a
400
400
9a
9a
A'
402
6a1
6a2
6a
6a
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9a
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803
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804
882
801
9a
9a
Y
X

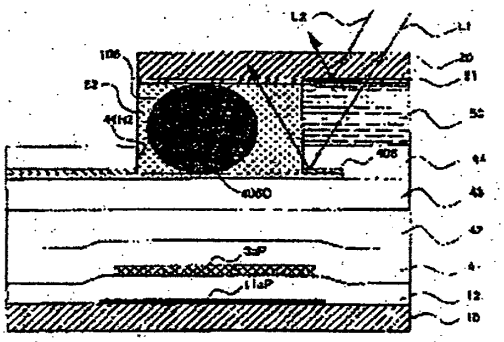
도면6



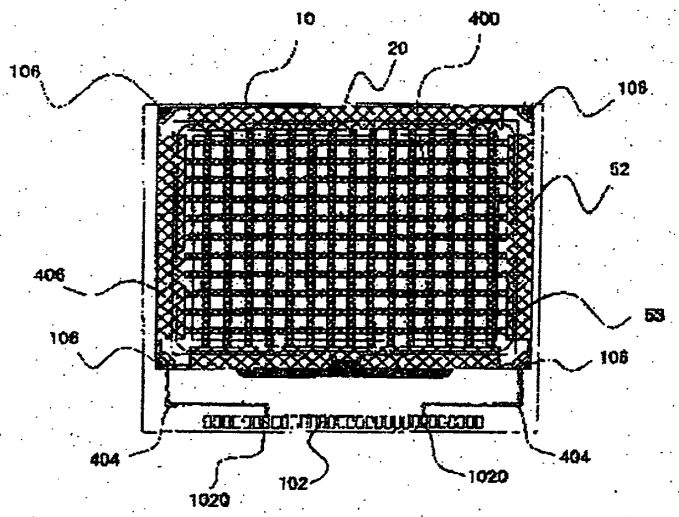
도면7a



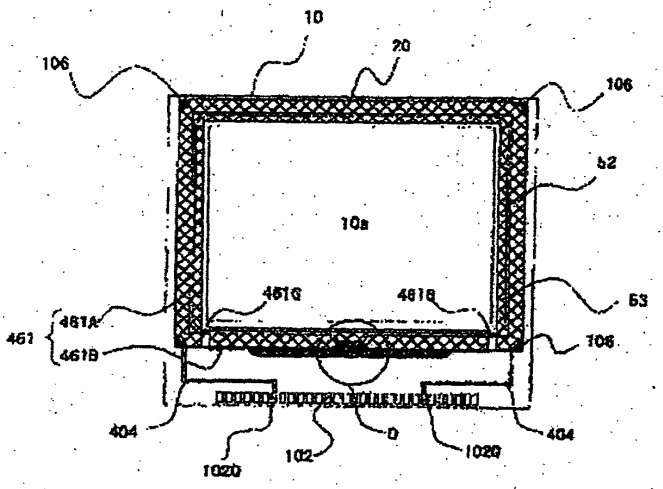
도면7b



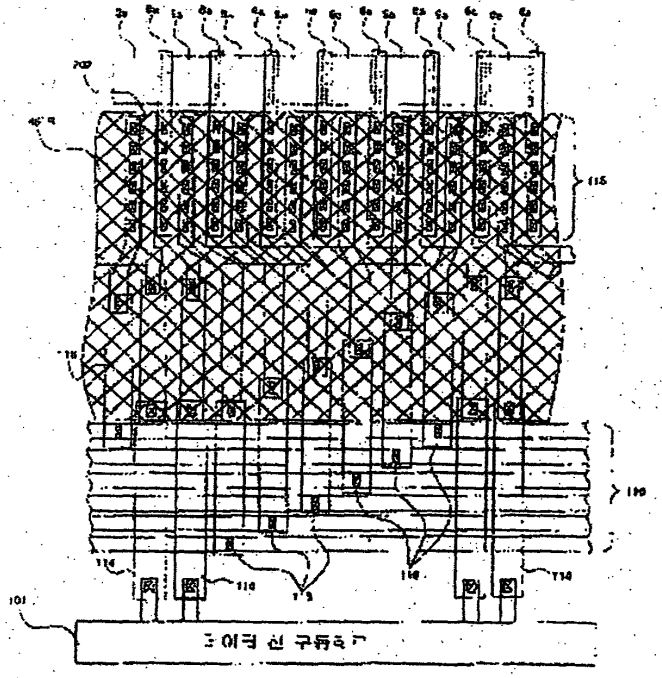
도면8



도면9

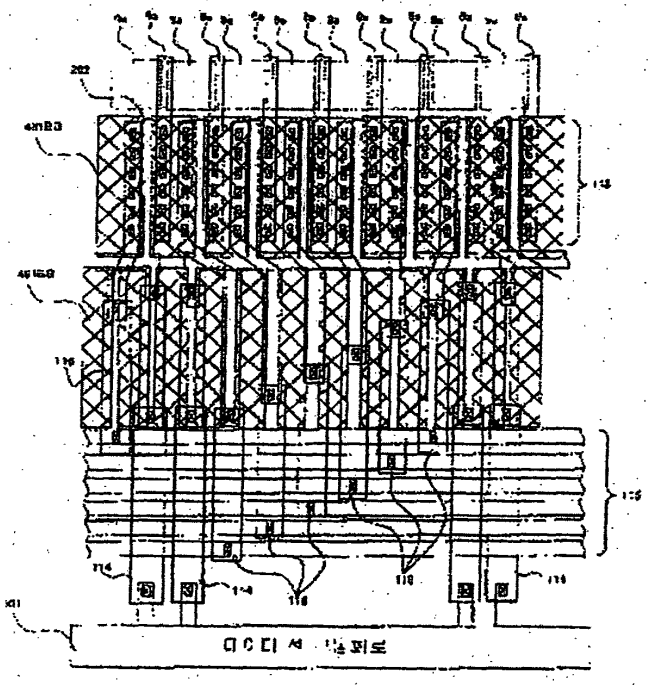


도면10

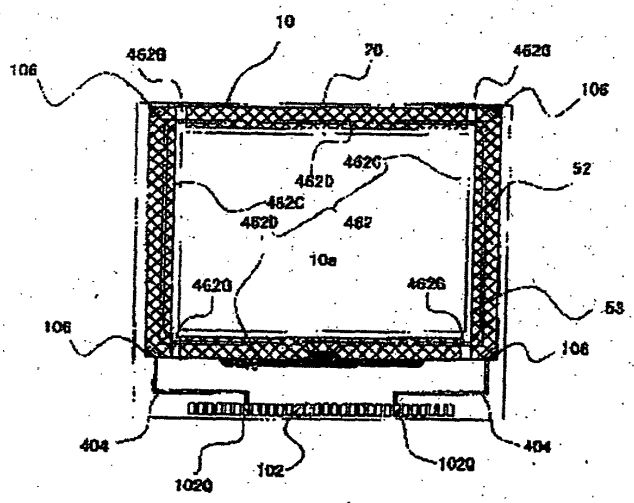


28-25

도면11

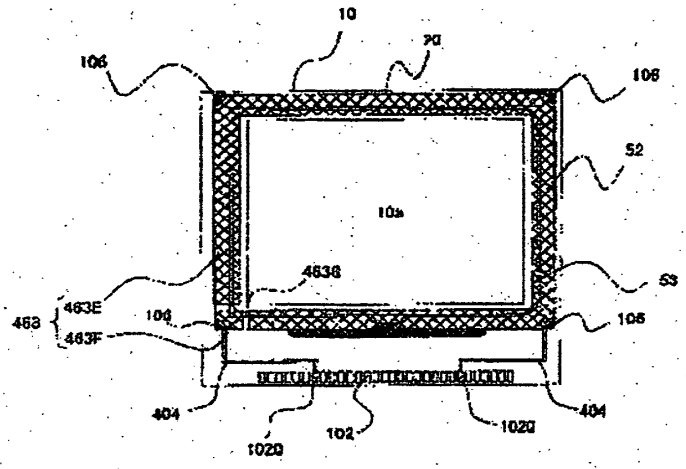


도면12

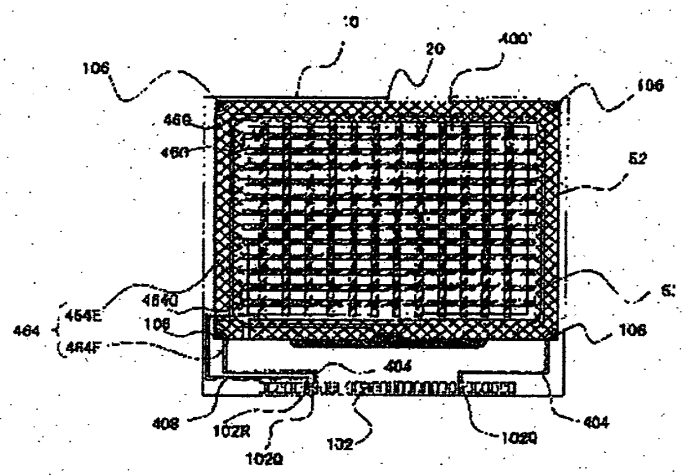


28-26

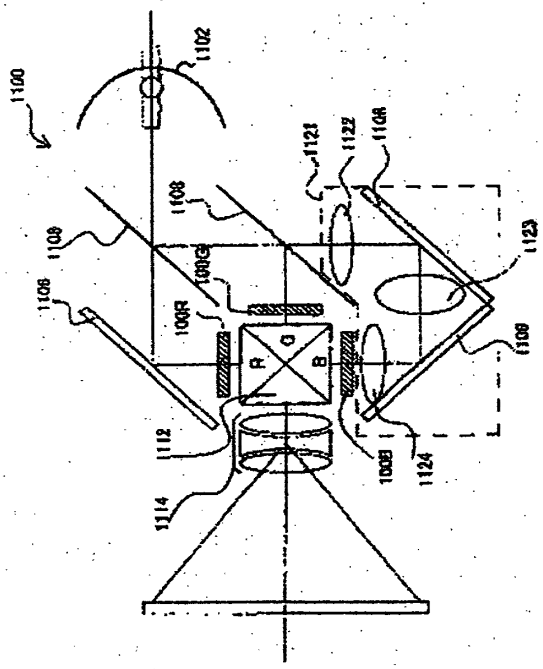
도면13


10
20
106
106
52
10a
463G
53
463
463E
463F
106
106
404
404
1020
102
1020

도면14


10
20
400'
106
106
466
460
52
464G
464
464E
464F
106
106
404
408
102R
102
1020
1020
404

도면15


1100
1102
1121
1122
1104
1103
1123
1105
1106
100R
100B
R
G
B
1109
1112
1114
1124

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: 11/223,919

Filed: September 13, 2005



Group Art Unit: 2811

Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

CLAIM FOR PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested for the above-identified patent application and the priority provided in 35 U.S.C. §119 is hereby claimed:

Japanese Patent Application No. 2004-328982 filed November 12, 2004.

In support of this claim, a certified copy of said original foreign application:

☒ is filed herewith.

It is requested that the file of this application be marked to indicate that the requirements of 35 U.S.C. §119 have been fulfilled and that the Patent and Trademark Office kindly acknowledge receipt of this document.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Philip A. Caramanica, Jr.
Registration No. 51,528

JAO:PAC/yxm

Date: November 3, 2005

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００４年１１月１２日
出願番号 Application Number:	特願２００４－３２８９８２
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００４－３２８９８２
出願人 Applicant(s):	セイコーエプソン株式会社

CERTIFIED COPY OF PRIORITY DOCUMENT

２００５年　８月１０日

特許庁長官
Commissioner,
Japan Patent Office

小川洋

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G02F　1/1333
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【電話番号】　03-5524-2323
【手数料の表示】
【予納台帳番号】　131946
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【物件名】　明細書　1
【物件名】　図面　1
【物件名】　要約書　1
【包括委任状番号】　0401860

出証特２００５－３０６７３９０

【書類名】特許請求の範囲
【請求項１】
所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、
前記一方の基板に設けられた表示用電極と、
前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、
前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、
該複数の引き出し配線に夫々接続され、平面的に見て前記複数の引き出し配線と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子と
を備えたことを特徴とする電気光学装置。
【請求項２】
前記外部接続端子及び前記引出し配線は、層間絶縁膜を介して積層され、
前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含み、
前記引き出し配線は、前記回路部を構成する第２導電膜と同一膜を含むことを特徴とする請求項１に記載の電気光学装置。
【請求項３】
前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に前記外部接続端子のうち前記一辺に沿った方向と交差する方向における縁部と接続されていることを特徴とする請求項１又は２に記載の電気光学装置。
【請求項４】
前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に平面的に見て前記外部接続端子と交差する領域において前記外部接続端子と接続されていることを特徴とする請求項１又は２に記載の電気光学装置。
【請求項５】
所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、
前記一方の基板に設けられた表示用電極と、
前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、
前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、
該複数の引き出し配線に夫々接続され、平面的に見て前記回路部と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子と
を備えたことを特徴とする電気光学装置。
【請求項６】
前記回路部は、前記複数の外部接続端子のうち画像信号を供給する端子と電気的に接続されると共に前記画像信号の供給を受けて駆動される駆動回路を含んでおり、該駆動回路の少なくとも一部は平面的に見て前記外部接続端子と重畳するように設けられていることを特徴とする請求項５に記載の電気光学装置。
【請求項７】
前記外部接続端子と前記回路部の一部とは層間絶縁膜を介して積層され、前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含むことを特徴とする請求項５又は６に記載の電気光学装置。
【請求項８】

前記一対の基板間に内部空間を形成するように前記一対の基板における相対向する面の周縁を貼り合わせるシール材と、前記内部空間に収容された電気光学物質とを更に備え、前記表示用電極及び前記回路部の一部は、前記内部空間に面して配置されることを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】

請求項１から８のいずれか一項に記載の電気光学装置を具備することを特徴とする電子機器。

【書類名】明細書
【発明の名称】電気光学装置及び電子機器
【技術分野】
【０００１】
本発明は、例えば液晶装置等の電気光学装置、及び、該電気光学装置を備えた、例えば液晶プロジェクタ等の電子機器の技術分野に関する。
【背景技術】
【０００２】
この種の電気光学装置では、表示用電極及びこれを駆動するための回路部が設けられた基板と対向基板とが、液晶等の電気光学物質を挟んで対向配置されている。具体的には、これらの基板を所定間隔で対向させ、その対向面の周縁をシール材で貼り合わせることで形成された内部空間に、電気光学物質が封入されている。
【０００３】
表示用電極が設けられた方の基板は、平面的に見て一辺において対向基板より張り出しており、この張り出した部分（以下、張り出し部という）に、外部接続端子が設けられている。外部接続端子は、回路部等から引き出された配線と接続される一方で、信号や電源が外部入力されるように表面が外部に露出するように設けられる。その他、画像信号供給用の外部接続端子と接続される駆動回路もまた、通常はこの張り出し部に設けられる。
【０００４】
これに対し、例えば特許文献１に記載されているように、駆動回路を内部空間に配置し、張り出し部には外部接続端子しか設けない装置構成を採れば、張り出し部の幅が短縮され、基板サイズの縮小を図ることができるとされている。
【０００５】
【特許文献１】特開平９－１１３９０６号公報
【発明の開示】
【発明が解決しようとする課題】
【０００６】
しかしながら、実際の電気光学装置において、駆動回路を配置し、駆動回路から配線を引き出すだけのスペースを内部空間に設けるのは困難である。また、仮に張り出し部に外部接続端子しか設けない場合であっても、外部接続端子に接続される引出し配線の少なくとも一部は張り出し部に配置されるわけで、張り出し部の幅を縮小するためには、これら外部接続端子と引出し配線とのレイアウトを考慮する余地がある。
【０００７】
本発明は上記問題点に鑑みてなされたものであり、基板サイズの縮小が可能な電気光学装置、及び、そのような電気光学装置を具備してなる電子機器を提供することを課題とする。
【課題を解決するための手段】
【０００８】
本発明の第１電気光学装置は、上記課題を解決するために、所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、前記一方の基板に設けられた表示用電極と、前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、該複数の引き出し配線に夫々接続され、平面的に見て前記複数の引き出し配線と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子とを備える。
【０００９】
本発明の第１電気光学装置によれば、少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板を所定間隔で相対向している。一対の基板のうち、他方よ

り張り出す基板には、例えば、走査線、データ線等の配線や薄膜トランジスタ（Thin Film Transistor：以下適宜“ＴＦＴ”と呼ぶ）等の電子素子、データ線駆動回路や走査線駆動回路等によって表示用電極を駆動する回路部が構成されており、その上層側に表示用電極が形成されている。

【００１０】

そして、この基板のうち、上記一辺において他方の基板より張り出してなる張り出し部に、回路部と電気的に接続される外部接続端子が設けられている。外部接続端子は、例えば張り出し部の外縁に沿って複数配列されており、回路部或いは表示用電極から引き出された引出し配線に夫々接続されている。引出し配線は通常、外部接続端子が配列された領域以外の領域に引き回されている。

【００１１】

これに対し、本発明に係る張り出し部では、平面的に見て、外部接続端子と引き出し配線とが少なくとも部分的に重なり合うように（即ち、張り出し部において立体的に）配置されている。そのような構成は、例えば、引出し配線及び外部接続端子の少なくとも一部を、コンタクトホール等を介して導通させつつ層間絶縁膜を介して積層させることで実現できる。この場合、配線や端子となる導電膜は、２層或いはそれ以上に積層されてよく、各層の導電膜は単層膜又は多層膜のいずれであってもよい。

【００１２】

このようにレイアウトを工夫することで、張り出し部の、張り出した方向における幅を短縮することができる。従って、基板サイズの縮小により、電気光学装置の省スペース化が実現可能である。また特に、基板サイズの縮小により、ウェハ一枚当たりから製造される電気光学装置の個数を増やすことができ、製造コストの低減、及び製造効率の向上に対して多大な効果を発揮する。例えば、一枚についての縮小量が１ｍｍ程度の比較的少量であっても、これが数枚から数十枚分或いは数百枚分だけ、同一ウェハ上に配列されるのであれば、同一ウェハ上に一行或いは複数行分だけ余計に電気光学装置を作り込める場合もあり得る。従って、実践上は顕著に有利となる。

【００１３】

本発明の第１電気光学装置の一態様では、前記外部接続端子及び前記引出し配線は、層間絶縁膜を介して積層され、前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含み、前記引き出し配線は、前記回路部を構成する第２導電膜と同一膜を含む。

【００１４】

この態様によれば、外部接続端子と引出し配線とは、層間絶縁膜を介して積層された、相異なる導電膜により形成されることで、平面的に見て互いに重なり合いつつも、コンタクトホール等によって接続される部位以外では電気的に導通しないように構成することができる。

【００１５】

また、外部接続端子と引出し配線とは、回路部を構成する導電膜と同一膜として、或いはそのような導電膜の同一膜を含んで形成されることから、外部接続端子及び引出し配線の積層構造を回路部とは別に設けずに済む。よって、基板上の構造が簡素化でき、比較的容易に形成することが可能である。尚、導電膜の材料としては、例えば低抵抗のアルミニウム（Ａｌ）が好適に用いられる。

【００１６】

本発明の第１電気光学装置の他の態様では、前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に前記外部接続端子のうち前記一辺に沿った方向と交差する方向における縁部と接続されている。

【００１７】

この態様によれば、複数の外部接続端子の配列方向に複数の引出し配線が張り出すことで、外部接続端子と引出し配線とが立体交差している。両者は、外部接続端子のうち上記一辺に沿った方向と交差する方向における縁部（即ち、外部接続端子のうち外縁側ないし

内縁側の縁部）において、例えばコンタクトホールを介して接続されている。このようなレイアウトでは、外部接続端子の形成領域内に引出し配線を効率よく配置できる。また、引出し配線は、自身が延在する領域からそれた領域で外部接続端子と接続されることから、例えばコンタクトホールの形成位置の誤差等により、外部接続端子に、接続対象とする配線と隣接する配線が誤って導通することが防止できる。よって、本態様に係る電気光学装置は、信頼性高く製造することができる。

【００１８】

或いは、他の態様では、前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に平面的に見て前記外部接続端子と交差する領域において前記外部接続端子と接続されている。

【００１９】

この態様によれば、複数の外部接続端子と複数の引出し配線とは、平面的に見て互いに交差する領域において、例えばコンタクトホールを介して接続されている。このようなレイアウトでは、外部接続端子の形成領域内に引出し配線を効率よく配置できると共に、引出し配線は自身が延在する領域で外部接続端子と接続されることから、コンタクトホールを形成するための領域を別途設けずに済み、引出し配線及び外部接続端子の配置スペースを小さくすることが可能である。よって、本態様に係る電気光学装置は、張り出し部が張り出した方向における幅が更に短縮され、基板サイズを更に縮小することが可能である。

【００２０】

本発明の第２電気光学装置は、上記課題を解決するために、所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、前記一方の基板に設けられた表示用電極と、前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、該複数の引き出し配線に夫々接続され、平面的に見て前記回路部と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子とを備える。

【００２１】

本発明の第２電気光学装置によれば、張り出し部に、回路部と外部接続端子とが、平面的に見て少なくとも部分的に重なり合うように配置されている。このような構成は、例えば、回路部及び外部接続端子の少なくとも一部を、層間絶縁膜を介して積層させることで実現できる。この場合、回路部や端子を構成する導電膜は、２層或いはそれ以上に積層されてよく、各層の導電膜は単層膜又は多層膜のいずれであってもよい。

【００２２】

このようにレイアウトを工夫することで、張り出し部の張り出し方向における幅を短縮することができ、基板サイズの縮小により、上記第１電気光学装置と同様の効果を奏する。

【００２３】

本発明の第２電気光学装置の一態様では、前記回路部は、前記複数の外部接続端子のうち画像信号を供給する端子と電気的に接続されると共に前記画像信号の供給を受けて駆動される駆動回路を含んでおり、前記外部接続端子は、前記駆動回路と少なくとも部分的に重畳する。

【００２４】

この態様によれば、駆動回路、即ち、所謂データ線駆動回路が、平面的に見て外部接続端子と少なくとも部分的に重なり合うように配置されている。データ線駆動回路は一般に、上記一辺に沿って延在するように設けられ、両端において画像信号入力のために多数の外部接続端子と引出し配線を介して接続される。そのため、周辺に多数の引出し配線を引き回すだけの領域が必要とされることから、データ線駆動回路は、外部接続端子と共に、空間的制約の少ない張り出し部に設けられることが多い。その場合、通常は外部接続端子とデータ線駆動回路とは同一平面上に設けられるために、張り出し部の幅は、データ線駆

動回路のサイズ形状等に応じて拡張されることになる。

【００２５】

これに対し、本態様では、張り出し部に設けられるデータ線駆動回路の全体又は少なくとも一部が外部接続端子と同じスペースに設けられているので、その分だけ張り出し部の幅が短縮され、電気光学装置の省スペース化或いは小型化を効果的に実現可能となる。

【００２６】

本発明の第２電気光学装置の他の態様では、前記外部接続端子と前記回路部の一部とは層間絶縁膜を介して積層され、前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含む。

【００２７】

この態様によれば、外部接続端子と回路部とは夫々、層間絶縁膜を介して積層されることで、平面的に見て互いに重なり合いつつも電気的に導通しないように構成できる。また、外部接続端子は、回路部を構成する導電膜と同一膜として、或いはそのような導電膜の同一膜を含んで形成されることから、基板上の構造が簡素化でき、比較的容易に形成することが可能である。尚、導電膜の材料としては、例えば低抵抗のアルミニウム（Ａｌ）が好適に用いられる。

【００２８】

本発明の第１及び第２電気光学装置における他の態様では、前記一対の基板間に内部空間を形成するように前記一対の基板における相対向する面の周縁を貼り合わせるシール材と、前記内部空間に収容された電気光学物質とを更に備え、前記表示用電極及び前記回路部の一部は、前記内部空間に面して配置される。

【００２９】

この態様によれば、電気光学装置を構成する一対の基板の間には、両基板における相対向する面の周縁をシール材で封止することによって内部空間が構成されており、その周縁から張り出し部が張り出している。内部空間には液晶等の電気光学物質が封入される。表示用電極は、電気光学物質を動作させるために、内部空間に面して配置される。また、回路部の一部、例えば、走査線、データ線及びＴＦＴ等の配線や素子、走査線駆動回路等の一部の駆動回路は、表示用電極と共に内部空間に面した領域に設けられている。よって、張り出し部の殆ど全域を、外部接続端子を形成するための領域として利用できる。

【００３０】

本発明の電子機器は上記課題を解決するために、上述した本発明の電気光学装置（但し、その各種態様を含む）を備える。

【００３１】

本発明の電子機器によれば、上述した本発明の電気光学装置を備えるので、省スペース化或いは小型化された、投射型表示装置、液晶テレビ、携帯電話、電子手帳、ワードプロセッサ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルなどの各種電子機器を実現できる。また、本発明の電子機器として、例えば電子ペーパなどの電気泳動装置等も実現可能である。

【００３２】

本発明のこのような作用及び他の利得は、次に説明する実施の形態から明らかにされる。

【発明を実施するための最良の形態】

【００３３】

以下、本発明の実施形態を図面に基づいて説明する。

【００３４】

＜１：電気光学装置の実施形態＞

図１から図１３を参照して、本発明の電気光学装置に係る実施形態について説明する。尚、以下の実施形態は、本発明の電気光学装置を液晶装置に適用したものである。

【００３５】

＜１－１：第１実施形態＞

図１から図７を参照して、本発明の第１実施形態に係る液晶装置について説明する。

【００３６】

＜１－１－１：液晶装置の概略構成＞

先ず、図１から図３を参照して、この液晶装置の概略構成について説明する。図１は、本実施形態に係る液晶装置の構成を示す平面図であり、図２は、図１のＩ－Ｉ’線断面を示している。図３は、本実施形態に係る液晶装置の比較例を示している。

【００３７】

図１及び図２において、液晶装置１００では、ＴＦＴアレイ基板１０に対向基板２０を所定間隔で対向させ、両基板の相対向する面の周縁をシール材５２ａで貼り合わせることによって、内部空間が形成されている。ＴＦＴアレイ基板１０には、平面的に見て対向基板２０より張り出してなる張り出し部２０１が存在し、シール材５２ａは、この張り出し部２０１が延在する辺における所定箇所（ここでは、この辺の両端）に対して、内部空間に通じる開口を規定している。そして、開口から内部空間に注入された液晶によって液晶層５０が構成され、開口は、封止モールド材１５１ａ及び１５１ｂによって夫々、封止されている。シール材５２ａの内縁に沿って設けられた額縁遮光膜５３は、画像が表示される画像表示領域１０ａを規定している。

【００３８】

ＴＦＴアレイ基板１０の対向面（図２中、上面）のうち、画像表示領域１０ａには、画素スイッチング用ＴＦＴや走査線、データ線等の配線の上層に、本発明の「表示用電極」の一例たる画素電極９ａが設けられている。そして、画素電極９ａの直上に配向膜が形成されている。対向基板２０の対向面（図２中、下面）には、ストライプ状の遮光膜２３を介して対向電極２１が形成されており、その上層に配向膜が形成されている。また、対向基板２０の角部の少なくとも１箇所（ここでは４箇所全部）には、ＴＦＴアレイ基板１０との間を電気的に導通させる上下導通端子１０６が設けられている。液晶層５０の液晶の配向状態は、画素電極９ａと対向電極２１との間に印加される電界に応じて変化するが、電界が印加されていない状態では、配向膜によって規定される初期配向をとる。

【００３９】

ＴＦＴアレイ基板１０の対向面のうち、額縁遮光膜５３の形成領域には、走査線を駆動する走査線駆動回路１０４と配線１０５とが設けられている。図１において、走査線駆動回路１０４は、額縁遮光膜５３の左右の辺に一つずつ設けられ、配線１０５は、これら２つの走査線駆動回路１０４の相互間を接続すべく、額縁遮光膜５３の上辺に引き回されている。

【００４０】

ＴＦＴアレイ基板１０の張り出し部２０１には、本発明の「駆動回路」の一具体例として、データ線を駆動するデータ線駆動回路１０１ａが、図１において、シール材５２ａの下辺に沿って配置されている。但し、平面的に見て、データ線駆動回路１０１ａの上半分は、シール材５２ａと重なるように設けられている。また、その下半分は、両端に封止モールド材１５１ａ及び１５１ｂの開口からはみ出した部分が夫々重なっている。

【００４１】

尚、本実施形態においては、ＴＦＴ等の電子素子や走査線、データ線等の配線、走査線駆動回路１０４やデータ線駆動回路１０１ａを含むＴＦＴアレイ基板１０上の回路全般が、本発明の「回路部」の具体例に対応している。また、張り出し部２０１には、データ線駆動回路１０１に加えて、複数のデータ線に画像信号を所定のタイミングで印加するサンプリング回路、複数のデータ線に所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の液晶装置１００の品質、欠陥等を検査するための検査回路等が形成されていてもよい。

【００４２】

更に、本実施形態では、張り出し部２０１において複数の引出し配線１０３ａの少なくとも一部が、平面的に見て、外部接続端子１０２ａと重畳するように設けられている。具体的には後述するが、この液晶装置１００では、外部接続端子１０２ａが形成されている

層と引出し配線１０３ａが形成されている層とは、例えば層間絶縁膜を介して積層され、外部接続端子１０２ａの形成領域と引出し配線１０３ａの形成領域とは少なくとも一部が重なり合っている。配線や端子となる導電膜は、２層或いはそれ以上に積層されてよく、各層の導電膜は単層膜又は多層膜のいずれであってもよい。

【００４３】

これら外部接続端子１０２ａは、ＦＰＣ１１０を介して接続された外部回路から液晶装置１００内に電源や信号を供給するために設けられており、夫々、引出し配線１０３ａを介して走査線駆動回路１０４やデータ線駆動回路１０１ａ等の駆動回路と適宜に接続されている。液晶装置１００では、これら外部接続端子１０２ａに外部入力された信号に応じて画素電極９ａが駆動され、画像が表示される。ここでデータ線駆動回路１０１ａは、張り出し部２０１側の両端において、引出し配線１０３ａを介して複数の外部接続端子１０２ａと接続されている。

【００４４】

図３に示したように、本実施形態の比較例に係る液晶装置においては、外部接続端子１０２と引出し配線１０３とは、平面的に見て互いに重なり合わないように、例えば同一平面上に配置される。外部接続端子１０２はまた、ＦＰＣ１１０と接続されなければならないので、その上に封止モールド材１５０が重なるのを防ぐために、ある程度、封止モールド材１５０から離しておく必要がある。結果的に、張り出し部２００は所定の幅Ｌ0を有し、データ線駆動回路１０１全体を配置できるだけのスペースが生じる。

【００４５】

これに対し、本実施形態の液晶装置１００では、以上に説明したように、外部接続端子１０２ａと引出し配線１０３ａの少なくとも一部とを、平面的に見て重畳するように配置したので、省スペース化が実現できる。特に、ここでは、外部接続端子１０２ａが張り出し部２０１の外縁に沿って配列されていることから、張り出し部２０１の、張り出し方向における幅Ｌ11を、通常より短縮することができる。

【００４６】

尚且つ、ここでは、封止モールド材１５１ａと封止モールド材１５１ｂとの間の領域に外部接続端子１０２ａを配置するようにしたので、外部接続端子１０２ａは封止モールド材１５１ａ及び１５１ｂに対して間隔をとらずに済む。更に、図１において、データ線駆動回路１０１ａの上半分をシール材５２ａが配置される領域に設けることで、外部接続端子１０２ａの位置を上側に押し上げることができる。以上の結果、張り出し部２０１の幅Ｌ11は、比較例における張り出し部２００の幅Ｌ0よりも短縮できる。

【００４７】

従って、本実施形態における液晶装置１００は省スペース化が可能であり、これを適用する電子機器に高い設計自由度を与えることができる。また、ウェハ一枚当たりから製造される液晶装置の個数を増やすことができ、製造効率の向上及び製造コスト低減に対して大きな効果を発揮する。即ち、１つの液晶装置１００における張り出し部２０１の縮小幅は、たとえ僅かであっても、ウェハ上には通常、上記ＴＦＴアレイ基板１０に対応する領域が数百ないし数千単位で形成され、更にそのようなウェハが多数生産されることから、製造上極めて有効である。

【００４８】

更に、ここでは、図１におけるシール材５２ａないし対向基板２０の下辺において、開口及び封止モールド材１５０ａ及び１５０ｂの夫々を両端部に配置し、外部接続端子１０２ａを中央部に配置するようにしたので、引出し配線１０３ａは、中央部から左右に分かれて引き回しても左右で配線長をほぼ等しくすることができ、左右における信号遅延等の不具合が生じずに済む。また、開口が左右両端に規定されていることから、内部空間に液晶を効率よく且つ均一に注入することができる。

【００４９】

＜１－１－２：張り出し部の構成＞

次に、図４から図７を参照して、液晶装置１００における張り出し部２０１の具体的構

成について、詳細に説明する。図４は、本実施形態に係る液晶装置の張り出し部における主要部分を拡大して表しており、図５は、図４のＡ－Ａ’線断面を表している。図６は、本実施形態に係る液晶装置の画像表示領域において、画素部が構成する等価回路を表している。図７及び図８は、画素部の構造を表す平面図と断面図である。尚、図８の（ａ）は、図７のＩＩ－ＩＩ’線断面を表しており、（ｂ）は、図７のＩＩＩ－ＩＩＩ’線断面を表している。また、図８においては、各層・各部材を図面上で認識可能な程度の大きさとするため、該各層・各部材の縮尺比率を適宜に変えてある。

【００５０】

図４において、複数の外部接続端子１０２ａは一方向に配列されており、複数の引出し配線１０３ａの夫々は、外部接続端子１０２ａの配列方向に延びると共に、外部接続端子１０２ａとコンタクトホール２０ａを介して接続されている。コンタクトホール２０ａは、各外部接続端子１０２ａの外縁に複数設けられている。尚、こうしたコンタクトホールの全部又は一部は、各外部接続端子１０２ａの内縁側に設けられていてもよい。

【００５１】

このようなレイアウトでは、引出し配線１０３ａは、自身が延在する領域からそれた領域で外部接続端子１０２ａと接続されることから、例えばコンタクトホール２０ａの形成位置の誤差等によって、外部接続端子１０２ａと、接続対象の引出し配線１０３ａと隣接して延びる引出し配線１０３ａとが誤って導通することが防止できる。よって、この液晶装置１００は、信頼性高く製造することができる。

【００５２】

図５において、このような外部接続端子１０２ａと引出し配線１０３ａとは、層間絶縁膜４３を介して積層されている。また、コンタクトホール２０ａは、この層間絶縁膜４３を貫通するように形成されている。引出し配線１０３ａは、このように所望の外部接続端子１０２ａとコンタクトホール２０ａを介して接続されつつも、それ以外の外部接続端子１０２ａとは層間絶縁膜４３によって絶縁されることによって、平面的に見て外部接続端子１０２ａと重ね合わせられている。

【００５３】

ここで、ＴＦＴアレイ基板１０上には、下地絶縁膜１２、層間絶縁膜４１～４４が順に積層されており、層間絶縁膜４２上に引出し配線１０３ａが設けられ、その上の層間絶縁膜４３上に外部接続端子１０２ａが設けられている。ここで、引出し配線１０３ａ及び外部接続端子１０２ａは共にアルミニウム層４０Ａ、窒化チタン層４０ＴＮの２層からなり、外部接続端子１０２ａの露出面Ｄ（図４中、外部接続端子１０２ａの斜線領域）層間絶縁膜４４及び窒化チタン層４０ＴＮを部分的に除去して形成された開口から外表に対して露出している。このような積層構造は、ＴＦＴアレイ基板１０上の画像表示領域１０ａにおける積層構造を準用して構成されている。そこで次に、画像表示領域１０ａにおける積層構造の構成について説明する。

【００５４】

＜１－１－３：画像表示領域の構成＞

図６において、画像表示領域１０ａには、複数の走査線１１ａ及び複数のデータ線６ａが相交差して配列しており、その線間に、走査線１１ａ，データ線６ａの各一によって選択される画素部が構成されている。各画素部は、ＴＦＴ３０、画素電極９ａ及び蓄積容量７０を含む。ＴＦＴ３０は、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを選択画素に印加するために設けられ、ゲートが走査線１１ａに接続され、ソースがデータ線６ａに接続され、ドレインが画素電極９ａに接続されている。画素電極９ａは、後述の対向電極２１との間で液晶容量を形成し、入力される画像信号Ｓ１、Ｓ２、…、Ｓｎを一定期間保持するようになっている。即ち、画素電極９ａによって画素部毎の開口領域が画定される。蓄積容量７０の一方の電極は、画素電極９ａと並列にＴＦＴ３０のドレインと接続され、他方の電極は、定電位となるように電位固定の容量配線４００に接続されている。

【００５５】

液晶装置１００は、例えばＴＦＴアクティブマトリクス駆動方式を採り、走査線駆動回路１０４（図１参照）から各走査線１１ａに走査信号Ｇ１、Ｇ２、…、Ｇｍが線順次に印加されると共に、それによってＴＦＴ３０がオン状態となる水平方向の選択画素部の列に対し、データ線駆動回路１０１（図１参照）からの画像信号Ｓ１、Ｓ２、…、Ｓｎを、データ線６ａを通じて印加される。その結果、選択画素に対応する画素電極９ａに画像信号が供給される。ＴＦＴアレイ基板１０は、液晶層５０を介して対向基板２０と対向配置されているので（図２参照）、こうして画素部毎に液晶層５０に電界を印加することにより、両基板間の透過光量が画素毎に制御され、画像が階調表示される。このとき各画素部に保持された画像信号は、蓄積容量７０によりリークが防止される。

【００５６】

図７及び図８においては、上述した画素部の各回路要素がパターン化され、積層された導電膜としてＴＦＴアレイ基板１０上に構築されている。本実施形態のＴＦＴアレイ基板１０は、石英基板からなり、ガラス基板や石英基板等からなる対向基板２０と対向配置されている。また、各回路要素は、下から順に、走査線１１ａを含む第１層、ゲート電極３ａを含む第２層、蓄積容量７０の固定電位側容量電極を含む第３層、データ線６ａ等を含む第４層、容量配線４００等を含む第５層、画素電極９ａ等を含む第６層からなる。また、第１層－第２層間には下地絶縁膜１２、第２層－第３層間には第１層間絶縁膜４１、第３層－第４層間には第２層間絶縁膜４２、第４層－第５層間には第３層間絶縁膜４３、第５層－第６層間には第４層間絶縁膜４４が夫々設けられ、前述の各要素間の短絡が防止されている。

【００５７】

（第１層の構成―走査線等―）

第１層は、走査線１１ａで構成される。走査線１１ａは、図７のＸ方向に沿って延びる本線部と、データ線６ａ或いは容量配線４００が延在する図７のＹ方向に延びる突出部とからなる形状にパターニングされている。このような走査線１１ａは、例えば導電性ポリシリコンからなり、その他にもチタン（Ｔｉ）、クロム（Ｃｒ）、タングステン（Ｗ）、タンタル（Ｔａ）、モリブデン（Ｍｏ）等の高融点金属のうちの少なくとも一つを含む金属単体、合金、金属シリサイド、ポリシリサイド又はこれらの積層体等により形成することができる。即ち、本実施形態における走査線１１ａは、できるだけ開口領域の間の領域を覆うことで、ＴＦＴ３０を下側から遮光する遮光膜としても機能する。

【００５８】

（第２層の構成―ＴＦＴ等―）

第２層は、ＴＦＴ３０及び中継電極７１９で構成されている。ＴＦＴ３０は、例えばＬＤＤ（Lightly Doped Drain）構造とされ、ゲート電極３ａ、半導体層１ａ、ゲート電極３ａと半導体層１ａを絶縁するゲート絶縁膜２を備えている。ゲート絶縁膜２は、例えば、ＨＴＯ（High Temperature Oxide）や熱酸化されたシリコン酸化膜からなる。ゲート電極３ａは、例えば導電性ポリシリコンで形成される。半導体層１ａは、例えばポリシリコンからなり、チャネル領域１ａ’、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ、並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅからなる。中継電極７１９は、例えばゲート電極３ａと同一膜として形成される。

【００５９】

ＴＦＴ３０のゲート電極３ａは、下地絶縁膜１２に形成されたコンタクトホール１２ｃｖを介して走査線１１ａに電気的に接続されている。下地絶縁膜１２は、例えば、ＨＴＯ等のシリコン酸化膜、或いはＮＳＧ（ノンシリケートガラス）膜からなり、第１層と第２層との層間を絶縁する他、ＴＦＴアレイ基板１０の全面に形成されることで、基板表面の研磨による荒れや汚れ等が惹き起こすＴＦＴ３０の素子特性の変化を防止する機能を有している。

【００６０】

（第３層の構成―蓄積容量等―）

第３層は、蓄積容量７０で構成されている。蓄積容量７０は、容量電極３００と下部電

極７１とが誘電体膜７５を介して対向配置された構成となっている。このうち、容量電極３００は、コンタクトホール８０１、８０３及び容量配線用中継層６ａ１を介して容量配線４００と電気的に接続されている。下部電極７１と高濃度ドレイン領域１ｅとは、第１層間絶縁膜４１に開孔されたコンタクトホール８３を介して接続されている。また、下部電極７１と画素電極９ａとは、コンタクトホール８８１、８８２、８０４及び中継電極７１９、第２中継電極６ａ２、第３中継電極４０２により各層を中継し、コンタクトホール８９において電気的に接続されている。

【００６１】

容量電極３００は、例えば、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ等の高融点金属のうちの少なくとも一つを含む金属単体、合金、金属シリサイド、ポリシリサイドからなる単層ないし多層膜、好ましくはタングステンシリサイドからなり、ＴＦＴ３０に図８の上側から入射しようとする光を遮る機能を有している。下部電極７１には、例えば導電性のポリシリコンが用いられる。誘電体膜７５は、例えば、膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ膜、ＬＴＯ（Low Temperature Oxide）膜等の酸化シリコン膜、或いは窒化シリコン膜等からなる。

【００６２】

また、第１層間絶縁膜４１は、例えば、ＮＳＧによって形成されている。その他、第１層間絶縁膜４１には、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）等のシリケートガラス、窒化シリコンや酸化シリコン等を用いることができる。

【００６３】

（第４層の構成―データ線等―）

第４層は、データ線６ａ、容量配線用中継層６ａ１及び第２中継電極６ａ２で構成されている。データ線６ａは、アルミニウム膜、窒化チタン膜の２層からなり、窒化シリコン膜によって表面を被覆されている。データ線６ａは、第１層間絶縁膜４１及び第２層間絶縁膜４２を貫通するコンタクトホール８１を介して、ＴＦＴ３０の高濃度ソース領域１ｄと電気的に接続されている。更に、データ線６ａと同一膜として、容量配線用中継層６ａ１及び第２中継電極６ａ２が形成されている。

【００６４】

また、第２層間絶縁膜４２は、例えばＮＳＧからなり、その他、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス、窒化シリコンや酸化シリコン等によって形成することができる。

【００６５】

（第５層の構成―容量配線等―）

第５層は、容量配線４００及び第３中継電極４０２により構成されている。容量配線４００は、画像表示領域１０ａの周囲にまで延設され、周辺駆動回路に供給される電源や上下導通端子を介して対向基板に供給される対向電極電位等の定電位源と電気的に接続されることで、固定電位とされている。また、容量配線４００は、第３層間絶縁膜４３に開孔されたコンタクトホール８０３を介して、容量配線用中継層６ａ１と電気的に接続されている。このような容量配線４００は、例えばアルミニウム膜、窒化チタン膜を積層した二層構造となっている。

【００６６】

容量配線４００は、図７に示すように、Ｘ方向、Ｙ方向に延在する格子状に形成され、Ｘ方向に延在する部分には、第３中継電極４０２の形成領域を確保するために切り欠きが設けられている。更に、容量配線４００は、遮光膜としても機能し、下層のデータ線６ａ、走査線１１ａ、ＴＦＴ３０等を覆うように、これらの回路要素よりも幅広に形成され、非開口領域を最終的に規定する形状となっている。更に、第５層には、容量配線４００と同一膜として、第３中継電極４０２が形成されている。

【００６７】

第５層の下には、全面に第３層間絶縁膜４３が形成されている。第３層間絶縁膜４３は

、例えばＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス、窒化シリコンや酸化シリコン等によって形成することができる。また、第３層間絶縁膜４３の表面を平坦化するためにＣＭＰ（Chemical Mechanical Polishing）等により研磨しても良いし、ＳＯＧ（Spin On Glass）等により平坦化膜を形成しても良い。平坦化により、配線間の段差等によるクラック発生を防止することができる。

【００６８】

（第６層の構成―画素電極等―）

第５層の全面には第４層間絶縁膜４４が形成され、更にその上に、第６層として画素電極９ａが形成されている。第４層間絶縁膜４４には、画素電極９ａ－第３中継電極４０２間を電気的に接続するためのコンタクトホール８９が開孔されている。このような第４層間絶縁膜４４は、例えばＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス、窒化シリコンや酸化シリコン等によって形成することができる。また、第４層間絶縁膜４４の表面を平坦化するためにＣＭＰ等により研磨しても良いし、ＳＯＧ等により平坦化膜を形成しても良い。平坦化により、配線間の段差等によるクラック発生を防止する事ができる。

【００６９】

画素電極９ａ（図７中、破線９ａ’で輪郭が示されている）は、縦横に区画配列された画素領域の各々と略対応して配置されている。このような画素電極９ａは、例えばＩＴＯ（Indium Tin Oxide）等の透明導電膜からなる。更に、画素電極９ａ上には、配向膜１６が形成されている。以上が、ＴＦＴアレイ基板１０側の画素部の構成である。

【００７０】

因みに、対向基板２０には、その対向面の全面に対向電極２１が設けられており、更にその上（図８では対向電極２１の下側）に配向膜２２が設けられている。対向電極２１は、画素電極９ａと同様、例えばＩＴＯ膜等の透明導電性膜からなる。対向基板２０と対向電極２１の間には、ＴＦＴ３０における光リーク電流の発生等を防止するため、少なくともＴＦＴ３０と正対する領域を覆うように遮光膜２３が設けられている。

【００７１】

本実施形態においては、このような画像表示領域１０ａの積層構造の延長上に、張り出し部２０１が形成されている。即ち、張り出し部２０１では、引出し配線１０３ａがデータ線６ａ等の同一膜として第４層に形成され、外部接続端子１０２ａが容量配線４００等と同一膜として第５層に形成されている（図５及び図８を参照）。そのため、図５に示したような引出し配線１０３ａと外部接続端子１０２ａとが層間絶縁膜を介して積層された構造を、画像表示領域１０ａの積層構造とは別に設けずに済む。よって、ＴＦＴアレイ基板１０上の構造が簡素化でき、比較的容易に形成することが可能である。

【００７２】

また、ここでは、第４層と第５層とが共にアルミニウムを含むことから、データ線６ａ、容量配線４００は勿論のこと、引出し配線１０３ａ及び外部接続端子１０２ａもまた、低抵抗に構成される。因みに、第４層及び第５層は、熱処理が必要な蓄積容量７０やＴＦＴ３０の上層に位置することにより、耐熱性の低いアルミニウムを用いることが可能となっている。ここでは、画像表示領域１０ａにおける積層構造のうち、第４層及び第５層に引出し配線１０３ａ及び外部接続端子１０２ａの夫々を設けることで、配線の低抵抗化と、外部接続端子１０２ａの露出面Ｄを容易に形成することが可能となる。

【００７３】

＜１－２：変形例＞

次に、図９及び図１０を参照して、第１実施形態の変形例に係る液晶装置について説明する。図９は、第１実施形態の変形例に係る液晶装置のうち、張り出し部における主要部分を拡大して表しており、図１０は、図９のＢ－Ｂ’線断面を表している。

【００７４】

本発明に係る外部接続端子及び引出し配線は、平面的に見て、少なくとも部分的に重畳するように配置されていればよく、そのレイアウトは、上記第１実施形態に説明した場合

以外にも種々の変形実施が可能である。

【００７５】

図９においては、そのような一例として、複数の外部接続端子１０２ｂは一方向に配列されており、引出し配線１０３ｂとコンタクトホール２０ｂを介して接続されている。コンタクトホール２０ｂは、平面的に見て、複数の引出し配線１０３ｂが複数の外部接続端子１０２ｂと交差する領域の夫々に設けられている。

【００７６】

このようなレイアウトでは、引出し配線１０３ｂは、自身が延在する領域で外部接続端子１０２ｂと接続されることから、コンタクトホールを形成するための領域を別途設けずに済み、引出し配線及び外部接続端子の配置スペースを、例えば第１実施形態に比べて小さくすることが可能である（図５及び図１０を参照）。よって、本変形例では、張り出し部の幅がより短縮され、ＴＦＴアレイ基板のサイズを更に縮小することが可能である。

【００７７】

＜１－３：第２実施形態＞

次に、図１１から図１３を参照して、第２実施形態に係る液晶装置について説明する。ここに、図１１は、本実施形態に係る液晶装置の概略構成を表している。図１２は、第２実施形態に係る液晶装置のうち、張り出し部における主要部分を拡大して表しており、図１３は、図１２のＣ－Ｃ’線断面を表している。尚、本実施形態の液晶装置１００Ａは、張り出し部内のレイアウトが異なることを除けば、液晶装置１００と同様に構成されていることから、液晶装置１００と同様の構成要素については、同一の符号を付して、その説明を適宜省略する。

【００７８】

図１１において、液晶装置１００Ａでは、張り出し部２０２の外縁に沿って配列された複数の外部接続端子１０２ｃに対し、データ線駆動回路１０１ｃ及び引出し配線１０３ｃの夫々が、平面的に見て部分的に重畳された状態で配置されている。このように張り出し部２０２のレイアウトを工夫することで、張り出し部２０２の幅Ｌ12を短縮することができ、ＴＦＴアレイ基板１０のサイズの縮小によって上記第１実施形態と同様の効果を奏する。

【００７９】

図１２及び図１３には、その様子が拡大表示されている。引出し配線１０３ｃは、第１実施形態の変形例と同様、外部接続端子１０２ｃと交差する領域に設けられたコンタクトホール２０ｃによって外部接続端子１０２ｃと接続されている。その一方、引出し配線１０３ｃは、自身が延在する領域に設けられたコンタクトホール２１ｃによってデータ線駆動回路１０１ｃと接続されている。

【００８０】

ここでは、ＴＦＴアレイ基板１０上の積層構造のうち、引出し配線１０３ｃは第４層に、外部接続端子１０２ｃは第５層に設けられており、コンタクトホール２０ｃは層間絶縁膜４３を貫通するように設けられている。データ線駆動回路１０１ｃは、第１層から第５層の少なくともいずれか（図示した範囲では第２層と第４層）に設けられており、コンタクトホール２１ｃは層間絶縁膜４１及び４２を貫通するように設けられている。

【００８１】

このように本実施形態においては、外部接続端子１０２ｃと引出し配線１０３ｃの夫々が、データ線駆動回路１０１ｃや画像表示領域１０ａにおける回路部分を構成する導電膜と同一膜として、或いはそのような導電膜の同一膜を含んで形成されることから、ＴＦＴアレイ基板１０上の構造が簡素化でき、比較的容易に形成することが可能である。その他の作用及び効果は上記第１実施形態と同様であり、第２実施形態に対しても第１実施形態に対する変形と同様の変形実施が可能である。

【００８２】

また、上記第２実施形態では、外部接続端子１０２ｃと引出し配線１０３ｃ、外部接続端子１０２ｃとデータ線駆動回路１０１ｃの夫々が平面的に見て重畳するようにしたが、

図１４に示したように、外部接続端子に対してデータ線駆動回路のみが重畳されるようなレイアウトにおいても張り出し部の幅が短縮され、本発明の効果を得ることができる。

【００８３】

＜２：電子機器＞

次に、図１５を参照して、以上に説明した液晶装置を電子機器に適用する場合について説明する。ここでは、本発明に係る電子機器の一例として、上述の液晶装置をライトバルブとして用いたプロジェクタについて説明する。図１５は、このプロジェクタの構成例を示している。

【００８４】

図１５において、プロジェクタ１１００内部には、ハロゲンランプ等の白色光源からなるランプユニット１１０２が設けられている。このランプユニット１１０２から射出された投射光は、ライトガイド内に配置された４枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によってＲＧＢの３原色に分離され、各原色に対応するライトバルブとしての液晶装置１００Ｒ、１００Ｂ及び１００Ｇに入射される。液晶装置１００Ｒ、１００Ｂ及び１００Ｇの構成は上述した液晶装置と同等であり、夫々において画像信号処理回路から供給されるＲ、Ｇ、Ｂの原色信号が変調される。液晶装置１００Ｒ、１００Ｂ及び１００Ｇによって変調された光は、ダイクロイックプリズム１１１２に３方向から入射される。これにより各色の画像が合成され、投射レンズ１１１４を介して、スクリーン１１２０等にカラー画像が投写される。

【００８５】

尚、本発明の電気光学装置は、上述の液晶装置以外に、例えば有機ＥＬ装置、電子ペーパ等の電気泳動装置、電子放出素子を利用した表示装置（Field Emission Display及びSurface-Conduction Electron-Emitter Display）等の各種装置として実現可能である。

【００８６】

また、このような本発明の電気光学装置は、先に説明したプロジェクタ以外にも、テレビジョン受像機や、ビューファインダ型或いはモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、ページャ、電子手帳、電卓、ワードプロセッサ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等の、各種の電子機器に対して適用可能である。

【００８７】

本発明は、上述した実施形態及び実施例に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨或いは思想に反しない範囲で適宜変更可能であり、そのような変更を伴う電気光学装置及びこれを備えた電子機器もまた、本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【００８８】

【図１】本発明の第１実施形態に係る液晶装置の構成を示す平面図である。

【図２】図１に示した液晶装置のＩ－Ｉ’線における断面図である。

【図３】第１実施形態に係る液晶装置の比較例を示す平面図である。

【図４】第１実施形態に係る液晶装置の主要部分の構成を示す平面図である。

【図５】図４に示した張り出し部のＡ－Ａ’線における断面図である。

【図６】第１実施形態に係る液晶装置の画像表示領域における等価回路を示す模式図である。

【図７】第１実施形態に係る液晶装置の画像表示領域の構成を示す平面図である。

【図８】第１実施形態に係る液晶装置の画像表示領域の構成を示す断面図であり、（ａ）は図７のＩＩ－ＩＩ’線における断面図、（ｂ）は図７のＩＩＩ－ＩＩＩ’線における断面図である。

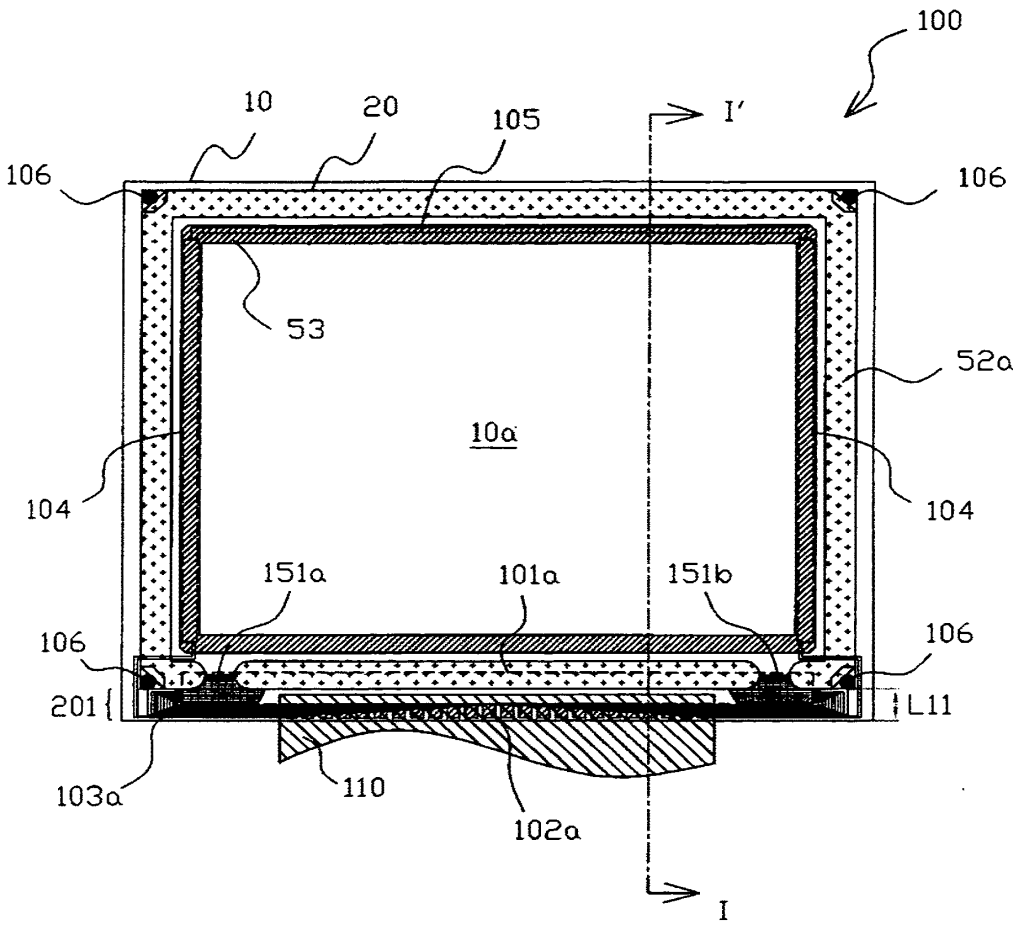
【図９】第１実施形態に係る液晶装置の変形例を示す平面図である。

【図１０】図９に示した張り出し部のＢ－Ｂ’線における断面図である。

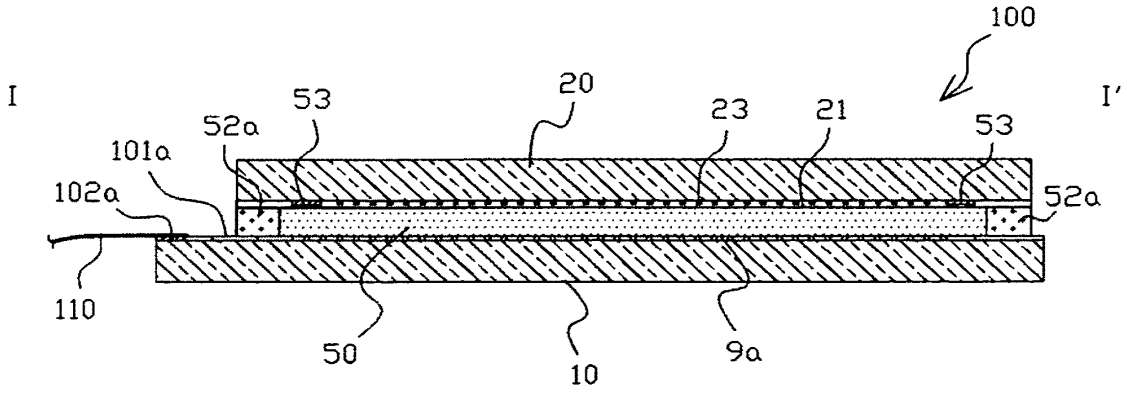
【図１１】第２実施形態に係る液晶装置の構成を示す平面図である。

【図１２】第２実施形態に係る液晶装置における主要部分の構成を示す平面図である。
【図１３】図１２に示した張り出し部のＣ－Ｃ’線における断面図である。
【図１４】第２実施形態に係る液晶装置の変形例を示す平面図である。
【図１５】本発明の電子機器の実施形態に係る液晶プロジェクタの構成を表す断面図である。
【符号の説明】
【００８９】
１０…ＴＦＴアレイ基板、９ａ…画素電極、１０ａ…画像表示領域、２０…対向基板、２１…対向電極、５０…液晶層、５２、５２ａ…シール材、５３…額縁遮光膜、１０１、１０１ａ～１０１ｄ…データ線駆動回路、１０２、１０２ａ～１０２ｄ…外部接続端子、１０３ａ～１０３ｄ…配線、１０４…走査線駆動回路、１０５…配線、１０６…上下導通端子、１１０…フレキシブルプリント回路（ＦＰＣ）、２００～２０２…張り出し部、１５０～１５３…封止モールド材、Ｌ0、Ｌ11、Ｌ12…（張り出し部の）幅。

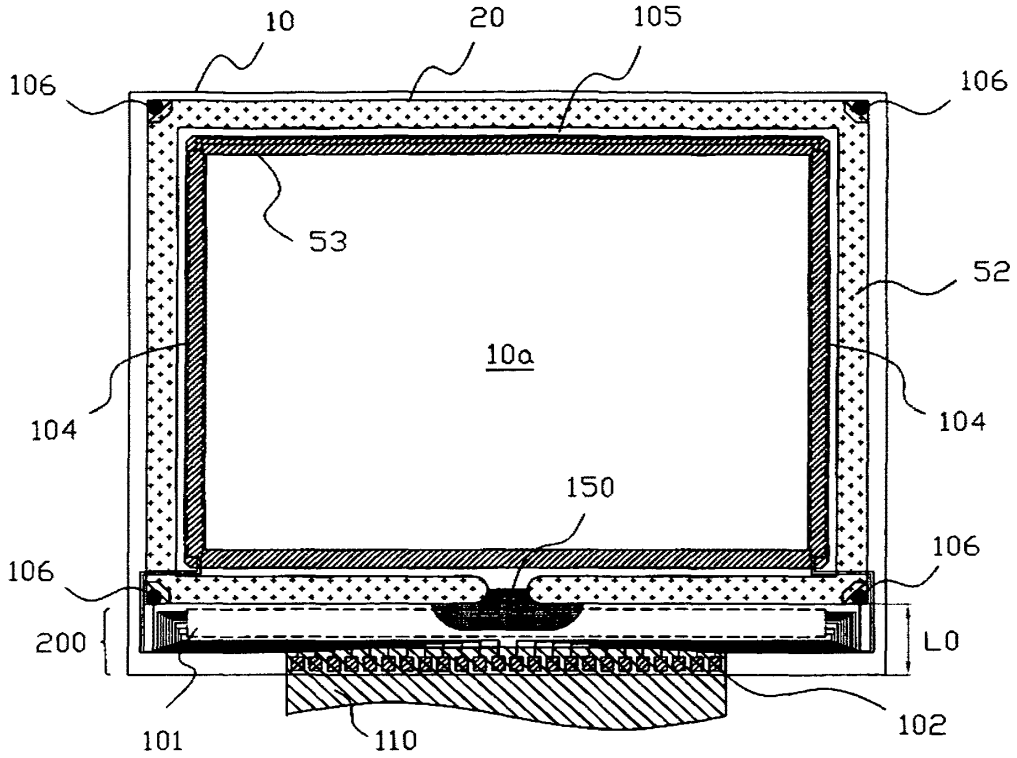
【書類名】図面
【図１】


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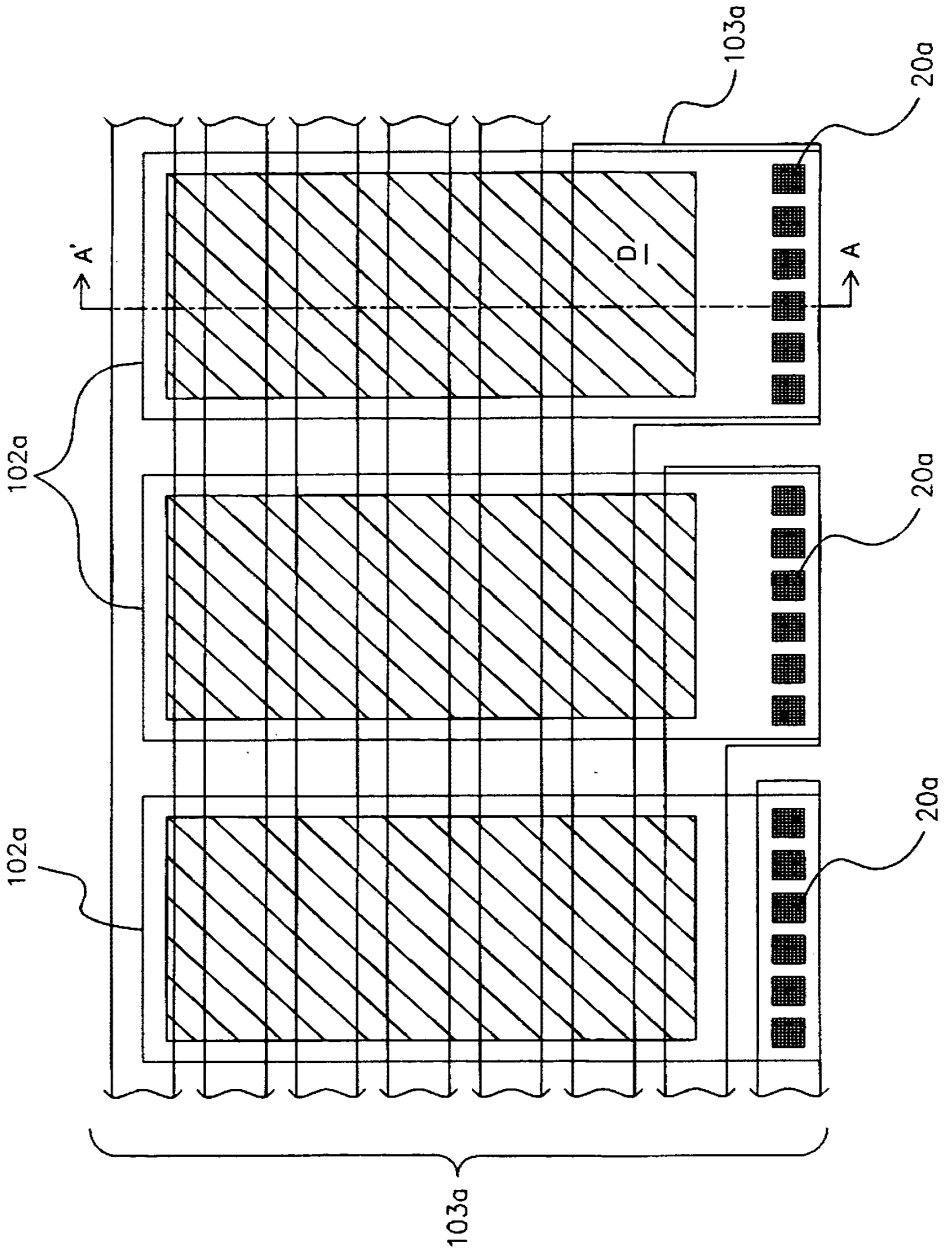
【図２】


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50
10
9a

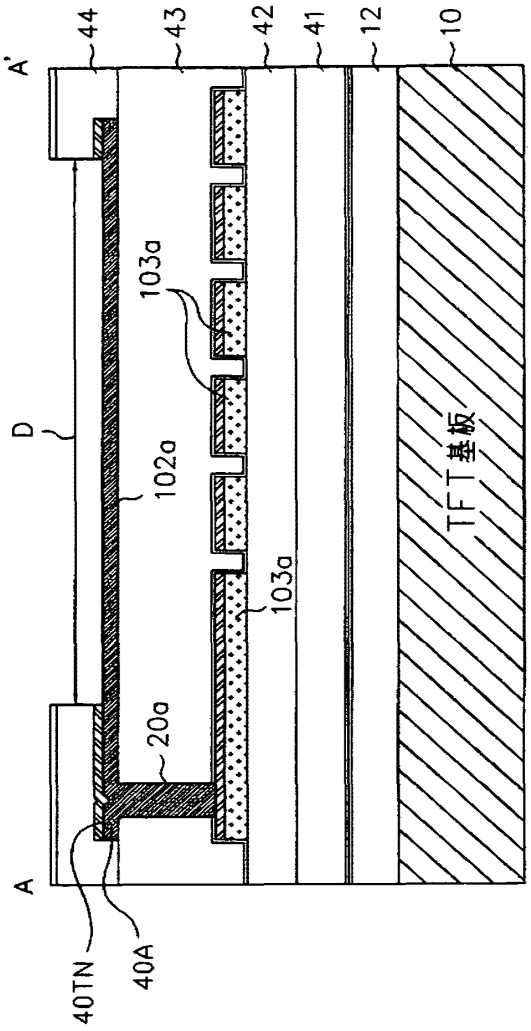
【図３】



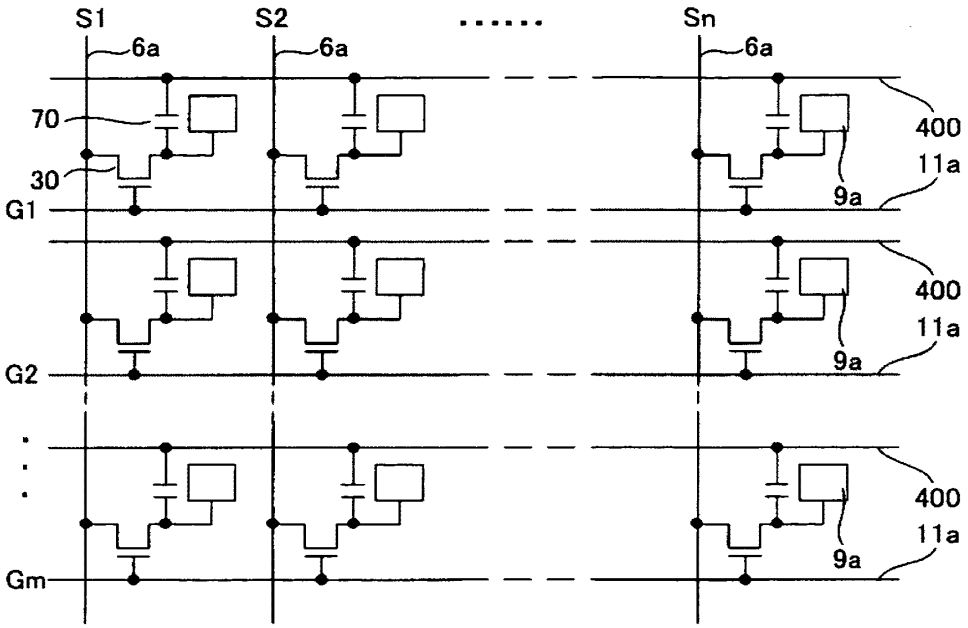
【図４】



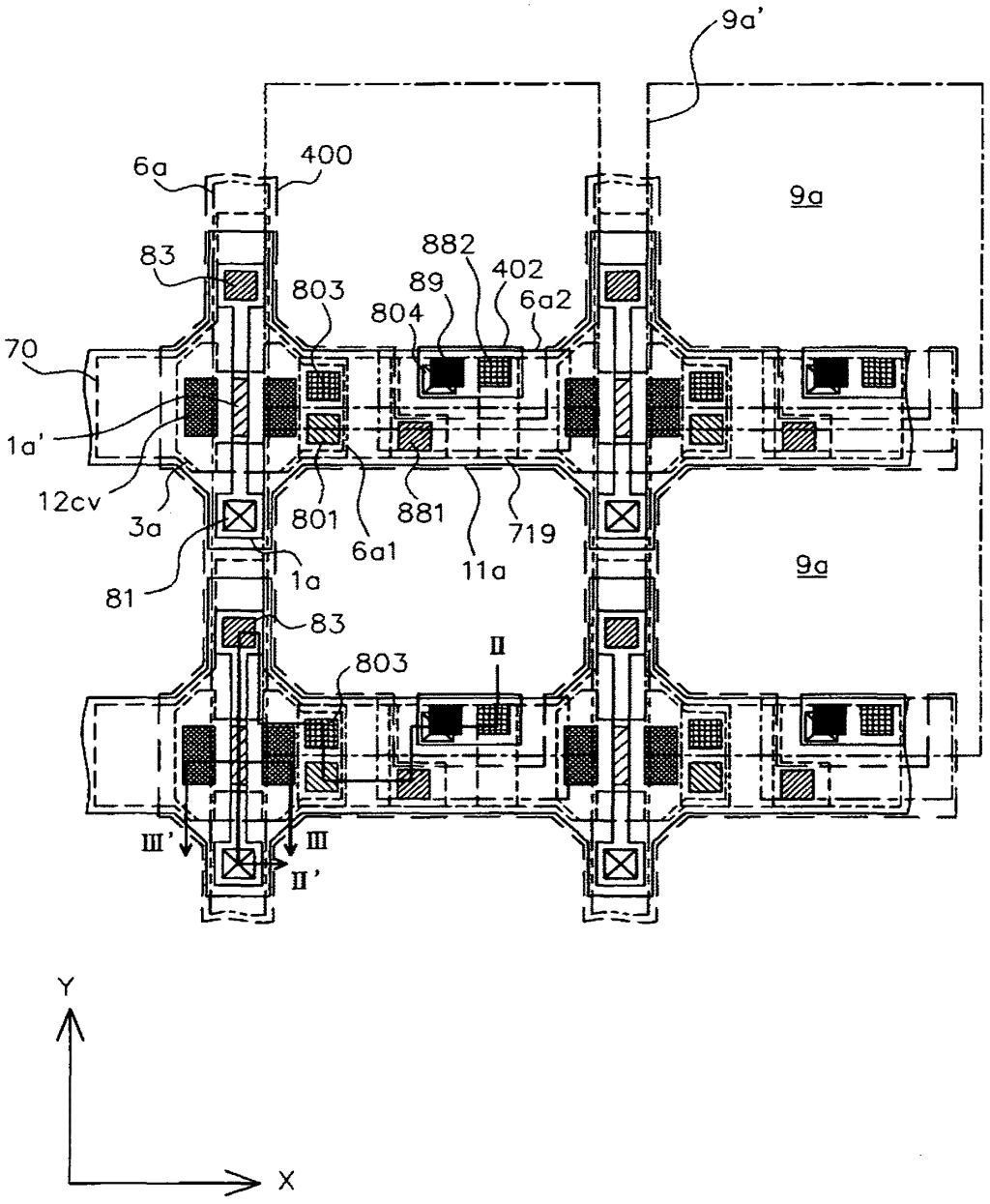
【図５】



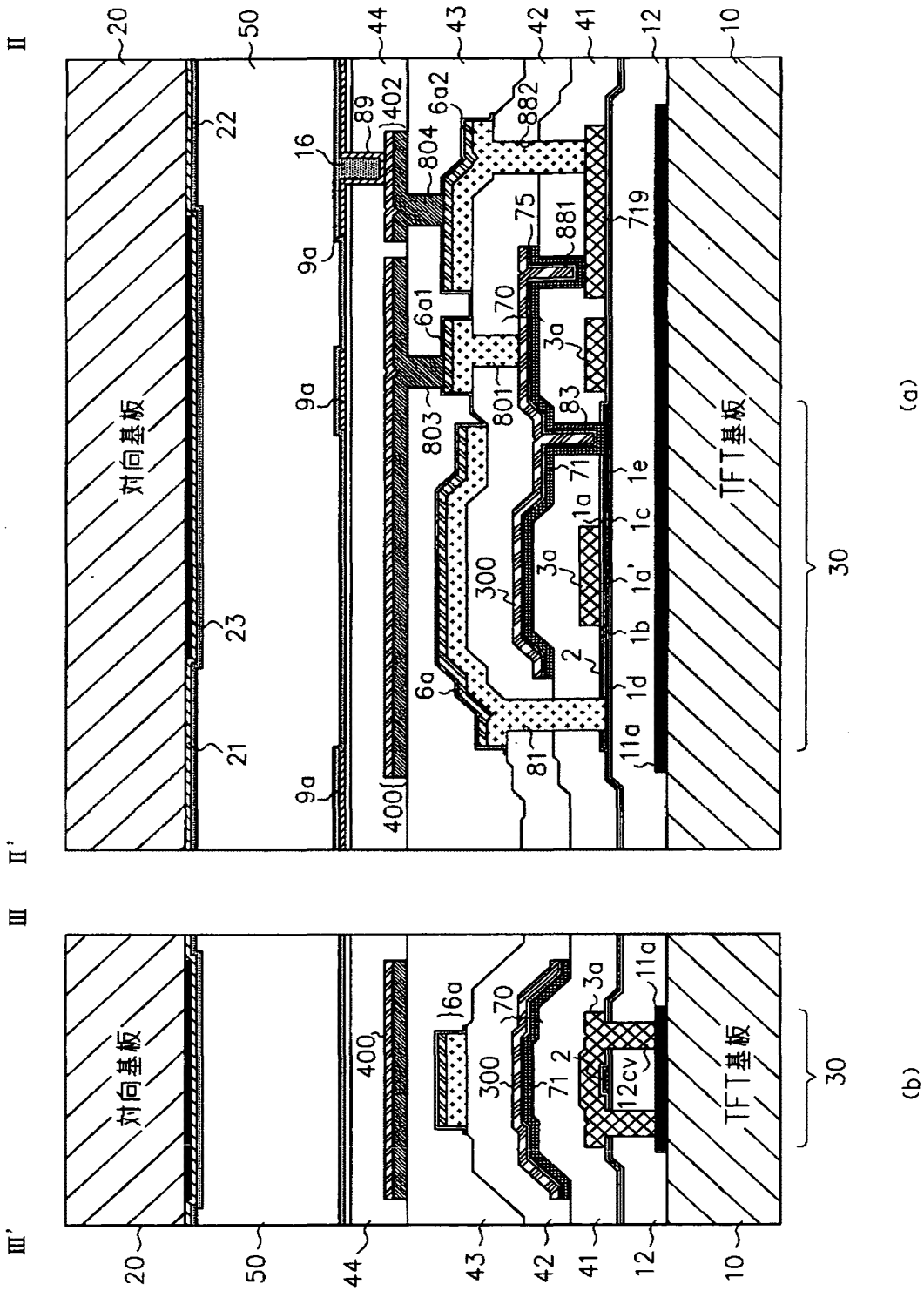
【図６】



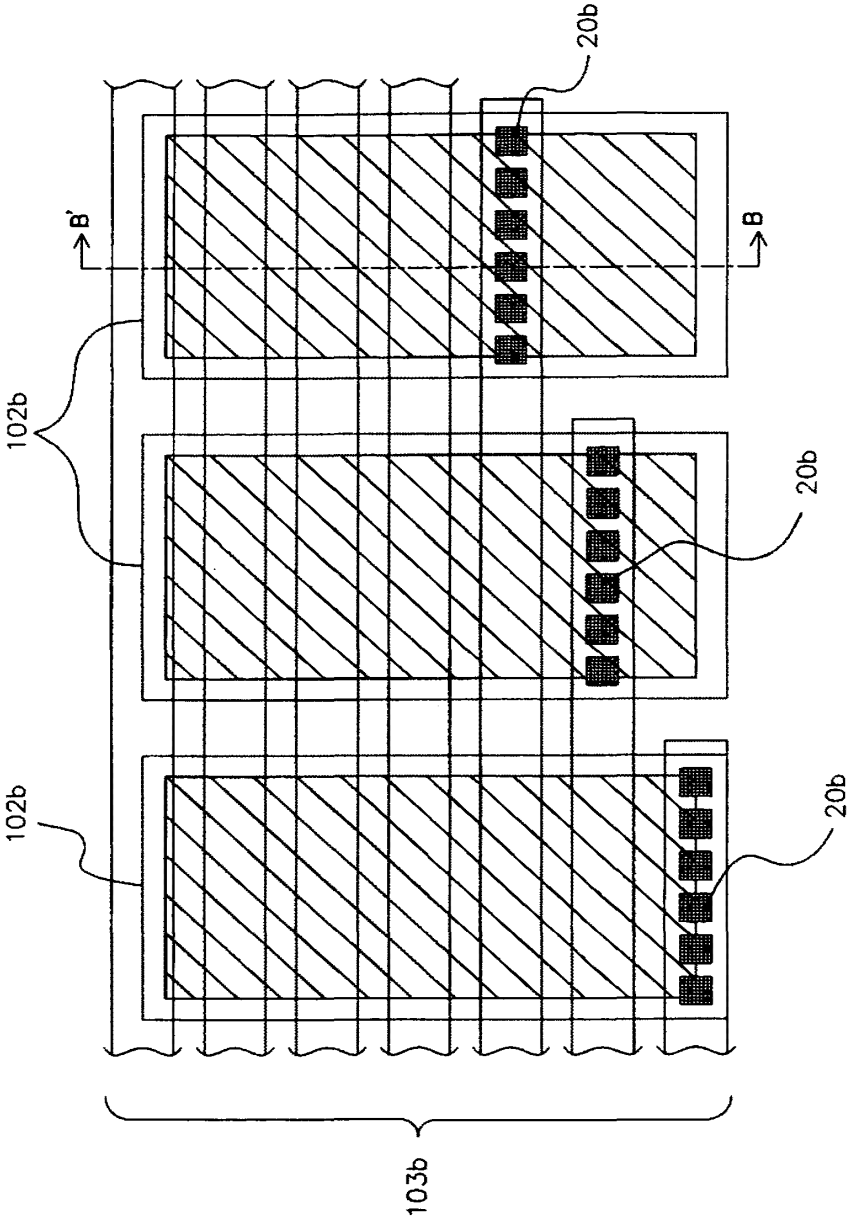
【図７】


9a'
6a
400
9a
83
882
402
89
803
804
6a2
70
1a'
12cv
3a
801
881
719
6a1
11a
9a
81
1a
83
803
II
III'
III
II'
Y
X

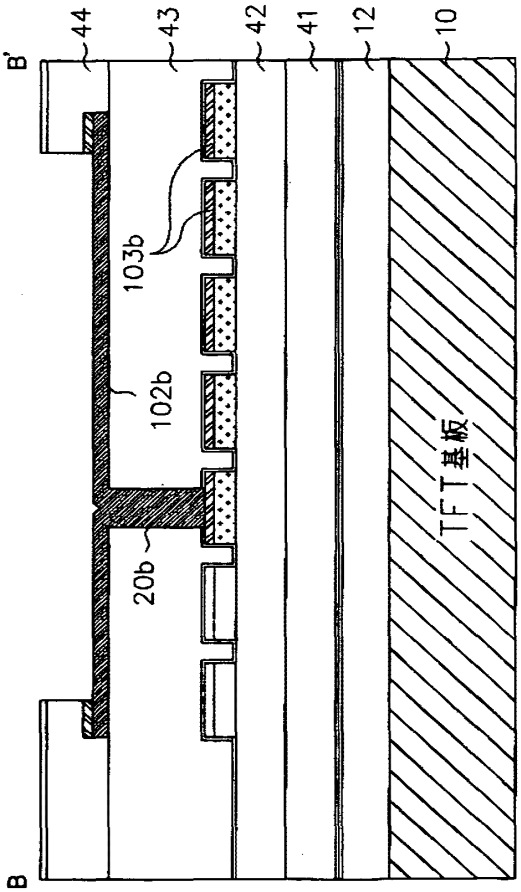
【図８】


II
II'
III
III'
20
50
44
43
42
41
12
10
対向基板
TFT基板
22
23
21
16
89
402
804
6a2
882
9a
6a1
75
881
719
70
3a
801
803
83
71
1e
1a
1c
1a'
1b
1d
300
2
6a
81
11a
400
12cv
30
(a)
(b)

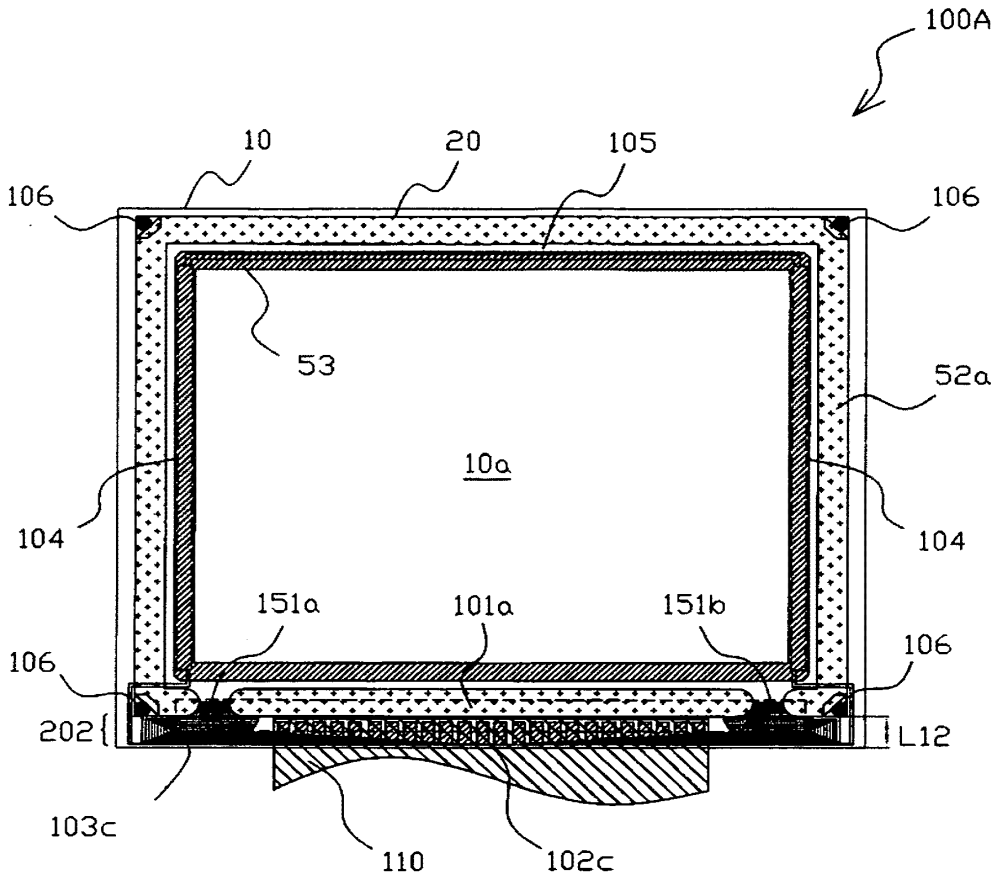
【図９】



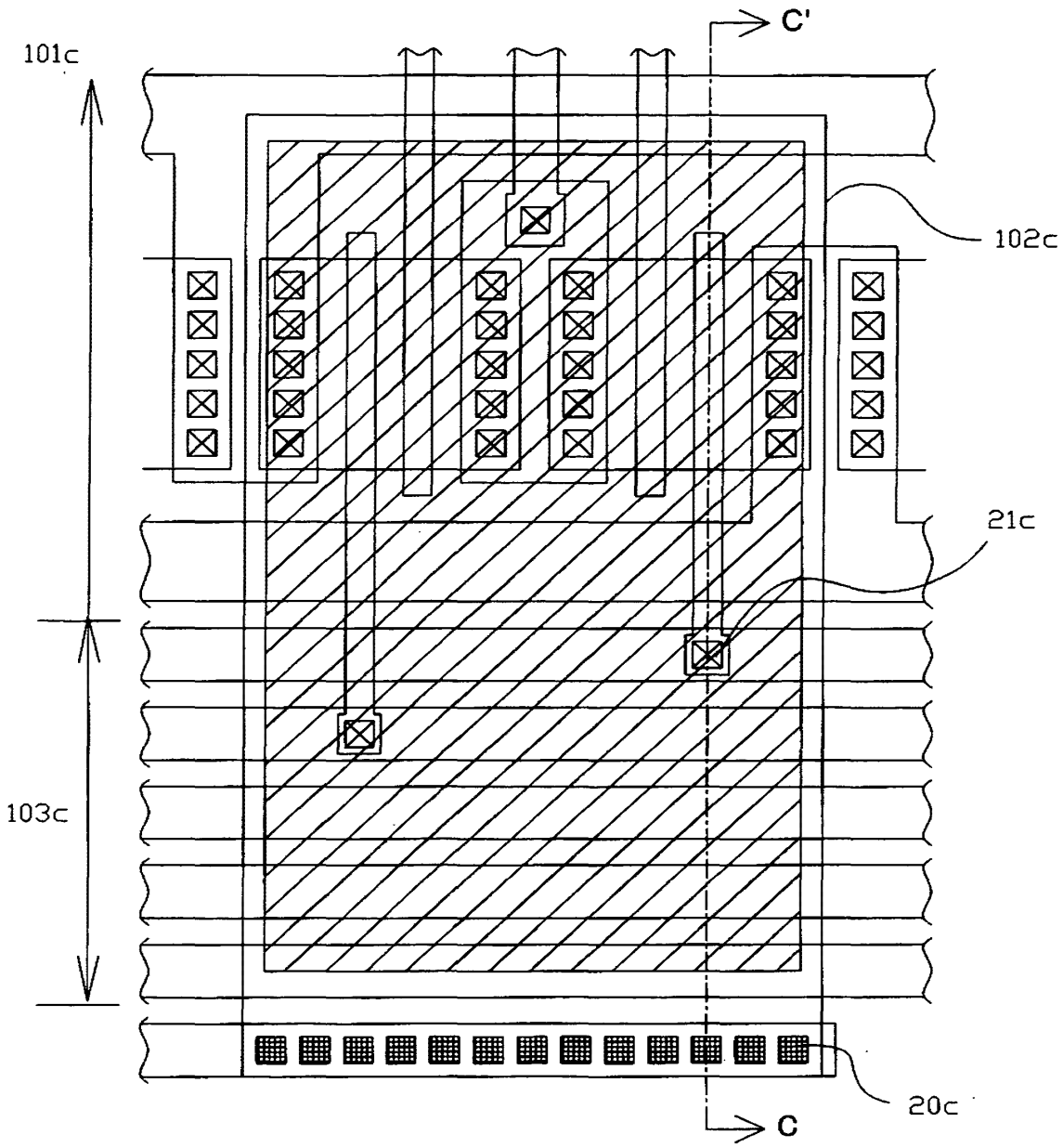
【図１０】



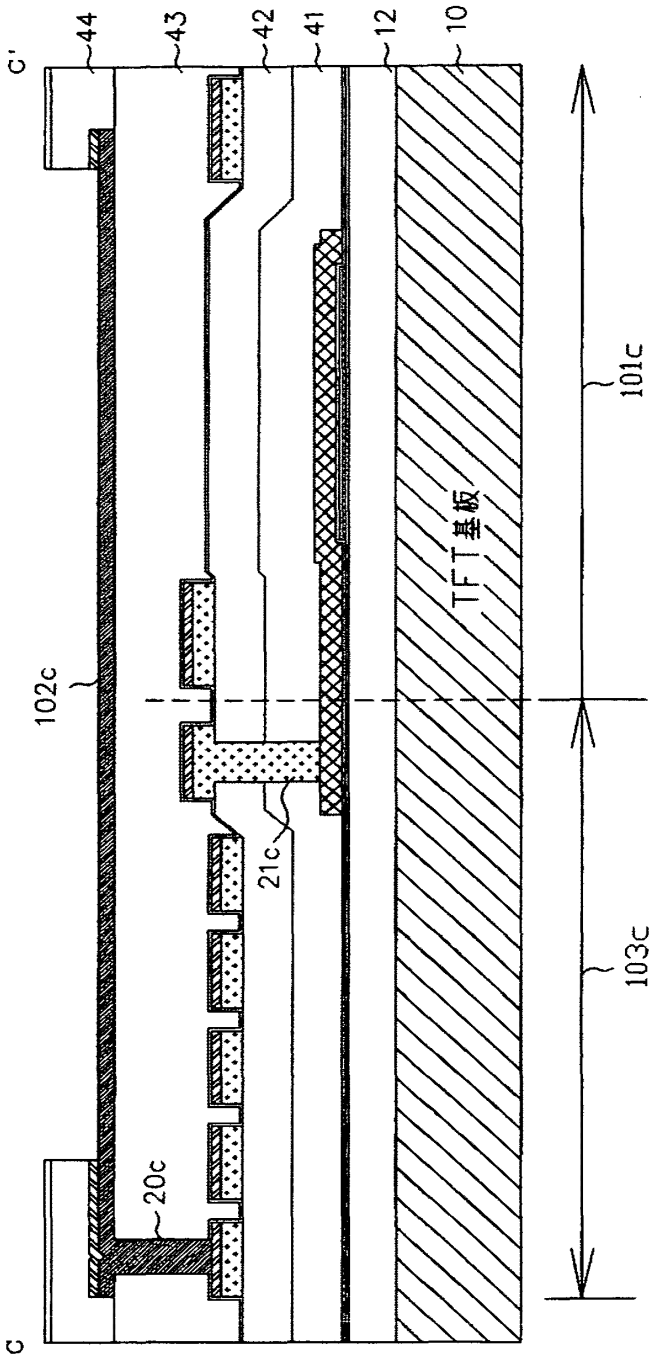
【図１１】


100A
10
20
105
106
106
53
52a
10a
104
104
151a
101a
151b
106
106
202
L12
103c
110
102c

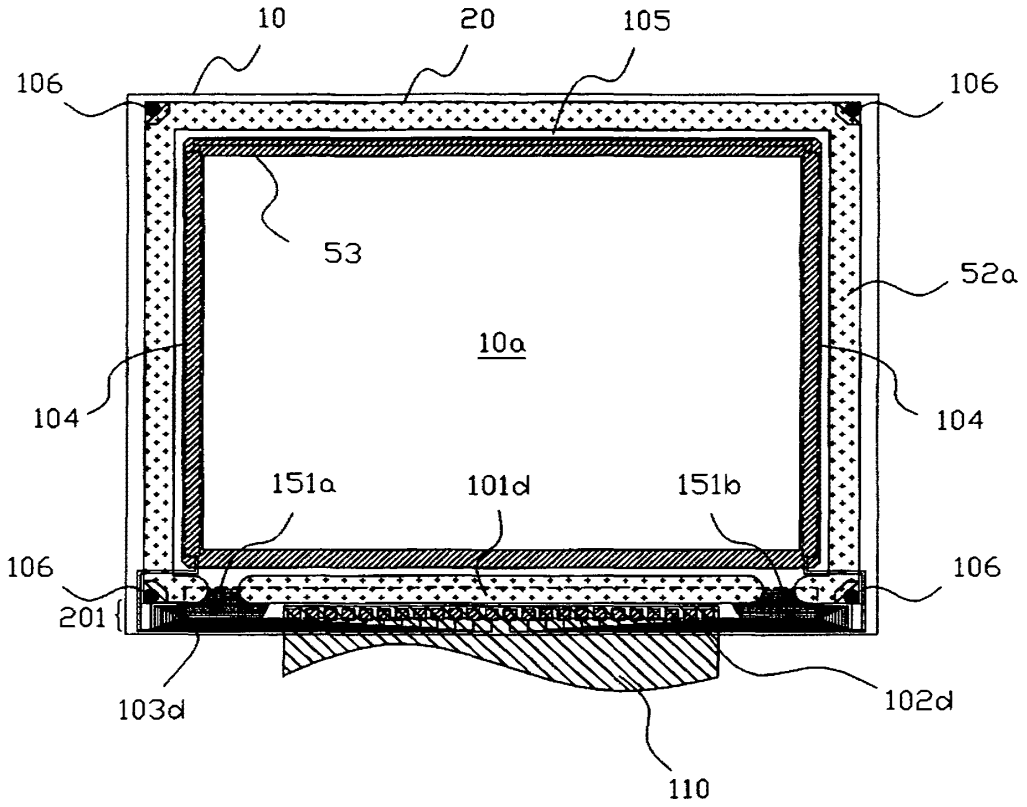
【図１２】



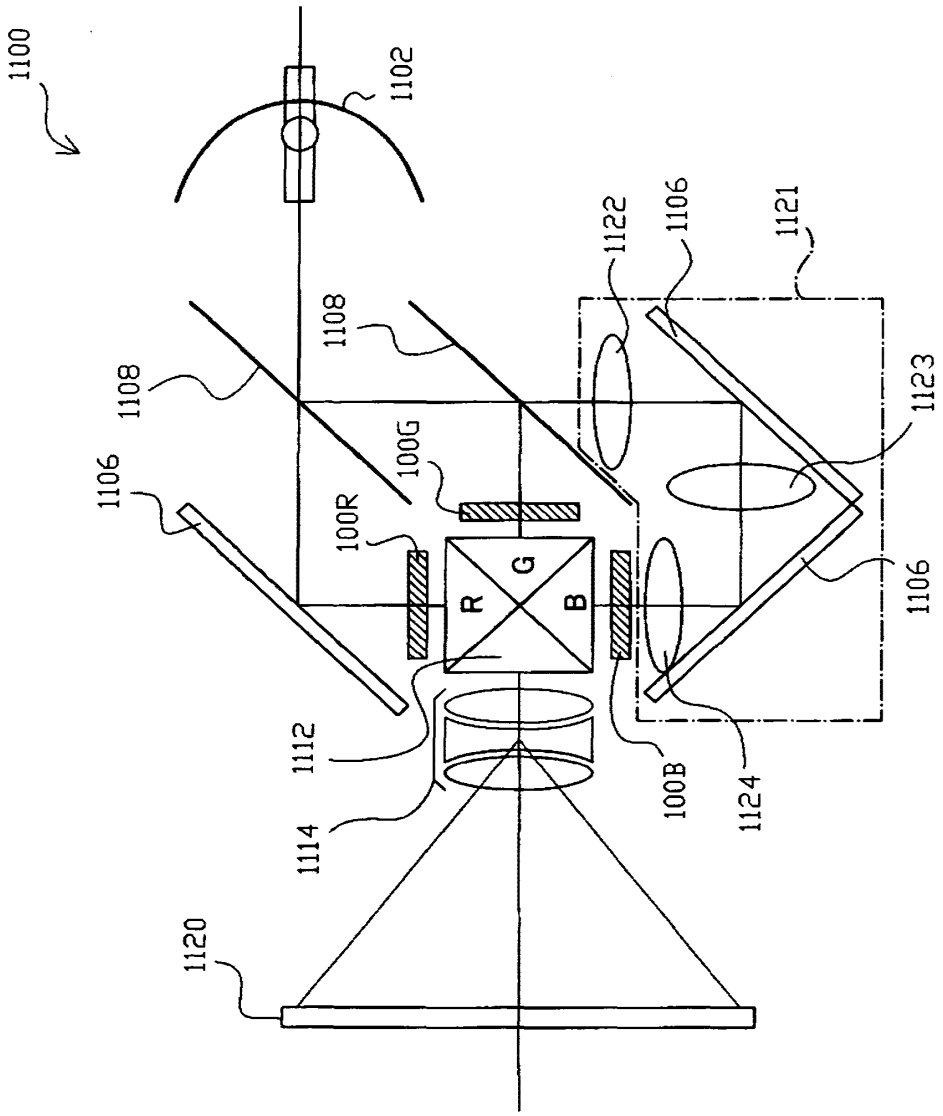
【図１３】



【図１４】


10
20
105
106
106
53
52a
10a
104
104
151a
101d
151b
106
106
201
103d
102d
110

【図１５】


1100
1102
1122
1106
1121
1108
1108
1123
100G
1106
100R
G
R
B
1106
1112
100B
1124
1114
1120

【書類名】要約書
【要約】
【課題】　液晶装置等の電気光学装置における基板サイズを縮小する。
【解決手段】
所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板（１０）が他方の基板（２０）より張り出している一対の基板を備える。一方の基板には、表示用電極を駆動する回路部が設けられ、前記一辺において張り出してなる張り出し部（２０１）における他方の基板と対向する側の面には、回路部と引出し配線（１０３ａ）によって電気的に接続された複数の外部接続端子（１０２ａ）が設けられている。外部接続端子は、平面的に見て、引き出し配線と少なくとも部分的に重畳するように設けられる。
【選択図】　図１

認定・付加情報

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＜認定情報・付加情報＞

【提出日】　平成16年11月12日

出証特２００５－３０６７３９０

特願２００４－３２８９８２

出　願　人　履　歴　情　報

識別番号　［０００００２３６９］

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出証番号　出証特２００５－３０６７３９０

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: 11/223,919

Filed: September 13, 2005



Group Art Unit: 2811

Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

CLAIM FOR PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested for the above-identified patent application and the priority provided in 35 U.S.C. §119 is hereby claimed:

Japanese Patent Application No. 2004-328982 filed November 12, 2004.

In support of this claim, a certified copy of said original foreign application:

☒ is filed herewith.

It is requested that the file of this application be marked to indicate that the requirements of 35 U.S.C. §119 have been fulfilled and that the Patent and Trademark Office kindly acknowledge receipt of this document.

Respectfully submitted,

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Date: November 3, 2005

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日 Date of Application:	２００４年１１月１２日
出願番号 Application Number:	特願２００４－３２８９８２
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００４－３２８９８２
出願人 Applicant(s):	セイコーエプソン株式会社

CERTIFIED COPY OF PRIORITY DOCUMENT

２００５年　８月１０日

特許庁長官
Commissioner,
Japan Patent Office

小川洋

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【国際特許分類】　G09F　9/00
G02F　1/13
G02F　1/1333
G03B 21/00
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【電話番号】　03-5524-2323
【手数料の表示】
【予納台帳番号】　131946
【納付金額】　16,000円
【提出物件の目録】
【物件名】　特許請求の範囲　1
【物件名】　明細書　1
【物件名】　図面　1
【物件名】　要約書　1
【包括委任状番号】　0401860

【書類名】特許請求の範囲
【請求項１】
所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、
前記一方の基板に設けられた表示用電極と、
前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、
前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、
該複数の引き出し配線に夫々接続され、平面的に見て前記複数の引き出し配線と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子と
を備えたことを特徴とする電気光学装置。
【請求項２】
前記外部接続端子及び前記引出し配線は、層間絶縁膜を介して積層され、
前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含み、
前記引き出し配線は、前記回路部を構成する第２導電膜と同一膜を含むことを特徴とする請求項１に記載の電気光学装置。
【請求項３】
前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に前記外部接続端子のうち前記一辺に沿った方向と交差する方向における縁部と接続されていることを特徴とする請求項１又は２に記載の電気光学装置。
【請求項４】
前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に平面的に見て前記外部接続端子と交差する領域において前記外部接続端子と接続されていることを特徴とする請求項１又は２に記載の電気光学装置。
【請求項５】
所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、
前記一方の基板に設けられた表示用電極と、
前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、
前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、
該複数の引き出し配線に夫々接続され、平面的に見て前記回路部と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子と
を備えたことを特徴とする電気光学装置。
【請求項６】
前記回路部は、前記複数の外部接続端子のうち画像信号を供給する端子と電気的に接続されると共に前記画像信号の供給を受けて駆動される駆動回路を含んでおり、該駆動回路の少なくとも一部は平面的に見て前記外部接続端子と重畳するように設けられていることを特徴とする請求項５に記載の電気光学装置。
【請求項７】
前記外部接続端子と前記回路部の一部とは層間絶縁膜を介して積層され、前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含むことを特徴とする請求項５又は６に記載の電気光学装置。
【請求項８】

前記一対の基板間に内部空間を形成するように前記一対の基板における相対向する面の周縁を貼り合わせるシール材と、前記内部空間に収容された電気光学物質とを更に備え、前記表示用電極及び前記回路部の一部は、前記内部空間に面して配置されることを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】

請求項１から８のいずれか一項に記載の電気光学装置を具備することを特徴とする電子機器。

【書類名】明細書
【発明の名称】電気光学装置及び電子機器
【技術分野】
【０００１】
本発明は、例えば液晶装置等の電気光学装置、及び、該電気光学装置を備えた、例えば液晶プロジェクタ等の電子機器の技術分野に関する。
【背景技術】
【０００２】
この種の電気光学装置では、表示用電極及びこれを駆動するための回路部が設けられた基板と対向基板とが、液晶等の電気光学物質を挟んで対向配置されている。具体的には、これらの基板を所定間隔で対向させ、その対向面の周縁をシール材で貼り合わせることで形成された内部空間に、電気光学物質が封入されている。
【０００３】
表示用電極が設けられた方の基板は、平面的に見て一辺において対向基板より張り出しており、この張り出した部分（以下、張り出し部という）に、外部接続端子が設けられている。外部接続端子は、回路部等から引き出された配線と接続される一方で、信号や電源が外部入力されるように表面が外部に露出するように設けられる。その他、画像信号供給用の外部接続端子と接続される駆動回路もまた、通常はこの張り出し部に設けられる。
【０００４】
これに対し、例えば特許文献１に記載されているように、駆動回路を内部空間に配置し、張り出し部には外部接続端子しか設けない装置構成を採れば、張り出し部の幅が短縮され、基板サイズの縮小を図ることができるとされている。
【０００５】
【特許文献１】特開平９－１１３９０６号公報
【発明の開示】
【発明が解決しようとする課題】
【０００６】
しかしながら、実際の電気光学装置において、駆動回路を配置し、駆動回路から配線を引き出すだけのスペースを内部空間に設けるのは困難である。また、仮に張り出し部に外部接続端子しか設けない場合であっても、外部接続端子に接続される引出し配線の少なくとも一部は張り出し部に配置されるわけで、張り出し部の幅を縮小するためには、これら外部接続端子と引出し配線とのレイアウトを考慮する余地がある。
【０００７】
本発明は上記問題点に鑑みてなされたものであり、基板サイズの縮小が可能な電気光学装置、及び、そのような電気光学装置を具備してなる電子機器を提供することを課題とする。
【課題を解決するための手段】
【０００８】
本発明の第１電気光学装置は、上記課題を解決するために、所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、前記一方の基板に設けられた表示用電極と、前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、該複数の引き出し配線に夫々接続され、平面的に見て前記複数の引き出し配線と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子とを備える。
【０００９】
本発明の第１電気光学装置によれば、少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板を所定間隔で相対向している。一対の基板のうち、他方よ

り張り出す基板には、例えば、走査線、データ線等の配線や薄膜トランジスタ（Thin Film Transistor：以下適宜“ＴＦＴ”と呼ぶ）等の電子素子、データ線駆動回路や走査線駆動回路等によって表示用電極を駆動する回路部が構成されており、その上層側に表示用電極が形成されている。

【００１０】

そして、この基板のうち、上記一辺において他方の基板より張り出してなる張り出し部に、回路部と電気的に接続される外部接続端子が設けられている。外部接続端子は、例えば張り出し部の外縁に沿って複数配列されており、回路部或いは表示用電極から引き出された引出し配線に夫々接続されている。引出し配線は通常、外部接続端子が配列された領域以外の領域に引き回されている。

【００１１】

これに対し、本発明に係る張り出し部では、平面的に見て、外部接続端子と引き出し配線とが少なくとも部分的に重なり合うように（即ち、張り出し部において立体的に）配置されている。そのような構成は、例えば、引出し配線及び外部接続端子の少なくとも一部を、コンタクトホール等を介して導通させつつ層間絶縁膜を介して積層させることで実現できる。この場合、配線や端子となる導電膜は、２層或いはそれ以上に積層されてよく、各層の導電膜は単層膜又は多層膜のいずれであってもよい。

【００１２】

このようにレイアウトを工夫することで、張り出し部の、張り出した方向における幅を短縮することができる。従って、基板サイズの縮小により、電気光学装置の省スペース化が実現可能である。また特に、基板サイズの縮小により、ウェハ一枚当たりから製造される電気光学装置の個数を増やすことができ、製造コストの低減、及び製造効率の向上に対して多大な効果を発揮する。例えば、一枚についての縮小量が１ｍｍ程度の比較的少量であっても、これが数枚から数十枚分或いは数百枚分だけ、同一ウェハ上に配列されるのであれば、同一ウェハ上に一行或いは複数行分だけ余計に電気光学装置を作り込める場合もあり得る。従って、実践上は顕著に有利となる。

【００１３】

本発明の第１電気光学装置の一態様では、前記外部接続端子及び前記引出し配線は、層間絶縁膜を介して積層され、前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含み、前記引き出し配線は、前記回路部を構成する第２導電膜と同一膜を含む。

【００１４】

この態様によれば、外部接続端子と引出し配線とは、層間絶縁膜を介して積層された、相異なる導電膜により形成されることで、平面的に見て互いに重なり合いつつも、コンタクトホール等によって接続される部位以外では電気的に導通しないように構成することができる。

【００１５】

また、外部接続端子と引出し配線とは、回路部を構成する導電膜と同一膜として、或いはそのような導電膜の同一膜を含んで形成されることから、外部接続端子及び引出し配線の積層構造を回路部とは別に設けずに済む。よって、基板上の構造が簡素化でき、比較的容易に形成することが可能である。尚、導電膜の材料としては、例えば低抵抗のアルミニウム（Ａｌ）が好適に用いられる。

【００１６】

本発明の第１電気光学装置の他の態様では、前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に前記外部接続端子のうち前記一辺に沿った方向と交差する方向における縁部と接続されている。

【００１７】

この態様によれば、複数の外部接続端子の配列方向に複数の引出し配線が張り出すことで、外部接続端子と引出し配線とが立体交差している。両者は、外部接続端子のうち上記一辺に沿った方向と交差する方向における縁部（即ち、外部接続端子のうち外縁側ないし

内縁側の縁部）において、例えばコンタクトホールを介して接続されている。このようなレイアウトでは、外部接続端子の形成領域内に引出し配線を効率よく配置できる。また、引出し配線は、自身が延在する領域からそれた領域で外部接続端子と接続されることから、例えばコンタクトホールの形成位置の誤差等により、外部接続端子に、接続対象とする配線と隣接する配線が誤って導通することが防止できる。よって、本態様に係る電気光学装置は、信頼性高く製造することができる。

【００１８】

或いは、他の態様では、前記複数の外部接続端子は、前記一辺に沿った方向に配列され、前記複数の引出し配線は夫々、前記一辺に沿った方向に延びると共に平面的に見て前記外部接続端子と交差する領域において前記外部接続端子と接続されている。

【００１９】

この態様によれば、複数の外部接続端子と複数の引出し配線とは、平面的に見て互いに交差する領域において、例えばコンタクトホールを介して接続されている。このようなレイアウトでは、外部接続端子の形成領域内に引出し配線を効率よく配置できると共に、引出し配線は自身が延在する領域で外部接続端子と接続されることから、コンタクトホールを形成するための領域を別途設けずに済み、引出し配線及び外部接続端子の配置スペースを小さくすることが可能である。よって、本態様に係る電気光学装置は、張り出し部が張り出した方向における幅が更に短縮され、基板サイズを更に縮小することが可能である。

【００２０】

本発明の第２電気光学装置は、上記課題を解決するために、所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板が他方の基板より張り出している一対の基板と、前記一方の基板に設けられた表示用電極と、前記表示用電極を駆動するために前記一方の基板に設けられた回路部と、前記回路部及び前記表示用電極を駆動するための配線のうち少なくとも一方から、前記一方の基板のうち前記一辺において張り出してなる張り出し部に夫々引き出された複数の引出し配線と、該複数の引き出し配線に夫々接続され、平面的に見て前記回路部と少なくとも部分的に重畳するように、前記張り出し部における前記他方の基板と対向する側の面に設けられた複数の外部接続端子とを備える。

【００２１】

本発明の第２電気光学装置によれば、張り出し部に、回路部と外部接続端子とが、平面的に見て少なくとも部分的に重なり合うように配置されている。このような構成は、例えば、回路部及び外部接続端子の少なくとも一部を、層間絶縁膜を介して積層させることで実現できる。この場合、回路部や端子を構成する導電膜は、２層或いはそれ以上に積層されてよく、各層の導電膜は単層膜又は多層膜のいずれであってもよい。

【００２２】

このようにレイアウトを工夫することで、張り出し部の張り出し方向における幅を短縮することができ、基板サイズの縮小により、上記第１電気光学装置と同様の効果を奏する。

【００２３】

本発明の第２電気光学装置の一態様では、前記回路部は、前記複数の外部接続端子のうち画像信号を供給する端子と電気的に接続されると共に前記画像信号の供給を受けて駆動される駆動回路を含んでおり、前記外部接続端子は、前記駆動回路と少なくとも部分的に重畳する。

【００２４】

この態様によれば、駆動回路、即ち、所謂データ線駆動回路が、平面的に見て外部接続端子と少なくとも部分的に重なり合うように配置されている。データ線駆動回路は一般に、上記一辺に沿って延在するように設けられ、両端において画像信号入力のために多数の外部接続端子と引出し配線を介して接続される。そのため、周辺に多数の引出し配線を引き回すだけの領域が必要とされることから、データ線駆動回路は、外部接続端子と共に、空間的制約の少ない張り出し部に設けられることが多い。その場合、通常は外部接続端子とデータ線駆動回路とは同一平面上に設けられるために、張り出し部の幅は、データ線駆

動回路のサイズ形状等に応じて拡張されることになる。

【００２５】

これに対し、本態様では、張り出し部に設けられるデータ線駆動回路の全体又は少なくとも一部が外部接続端子と同じスペースに設けられているので、その分だけ張り出し部の幅が短縮され、電気光学装置の省スペース化或いは小型化を効果的に実現可能となる。

【００２６】

本発明の第２電気光学装置の他の態様では、前記外部接続端子と前記回路部の一部とは層間絶縁膜を介して積層され、前記外部接続端子は、前記回路部を構成する第１導電膜と同一膜を含む。

【００２７】

この態様によれば、外部接続端子と回路部とは夫々、層間絶縁膜を介して積層されることで、平面的に見て互いに重なり合いつつも電気的に導通しないように構成できる。また、外部接続端子は、回路部を構成する導電膜と同一膜として、或いはそのような導電膜の同一膜を含んで形成されることから、基板上の構造が簡素化でき、比較的容易に形成することが可能である。尚、導電膜の材料としては、例えば低抵抗のアルミニウム（Ａｌ）が好適に用いられる。

【００２８】

本発明の第１及び第２電気光学装置における他の態様では、前記一対の基板間に内部空間を形成するように前記一対の基板における相対向する面の周縁を貼り合わせるシール材と、前記内部空間に収容された電気光学物質とを更に備え、前記表示用電極及び前記回路部の一部は、前記内部空間に面して配置される。

【００２９】

この態様によれば、電気光学装置を構成する一対の基板の間には、両基板における相対向する面の周縁をシール材で封止することによって内部空間が構成されており、その周縁から張り出し部が張り出している。内部空間には液晶等の電気光学物質が封入される。表示用電極は、電気光学物質を動作させるために、内部空間に面して配置される。また、回路部の一部、例えば、走査線、データ線及びＴＦＴ等の配線や素子、走査線駆動回路等の一部の駆動回路は、表示用電極と共に内部空間に面した領域に設けられている。よって、張り出し部の殆ど全域を、外部接続端子を形成するための領域として利用できる。

【００３０】

本発明の電子機器は上記課題を解決するために、上述した本発明の電気光学装置（但し、その各種態様を含む）を備える。

【００３１】

本発明の電子機器によれば、上述した本発明の電気光学装置を備えるので、省スペース化或いは小型化された、投射型表示装置、液晶テレビ、携帯電話、電子手帳、ワードプロセッサ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルなどの各種電子機器を実現できる。また、本発明の電子機器として、例えば電子ペーパなどの電気泳動装置等も実現可能である。

【００３２】

本発明のこのような作用及び他の利得は、次に説明する実施の形態から明らかにされる。

【発明を実施するための最良の形態】

【００３３】

以下、本発明の実施形態を図面に基づいて説明する。

【００３４】

＜１：電気光学装置の実施形態＞

図１から図１３を参照して、本発明の電気光学装置に係る実施形態について説明する。尚、以下の実施形態は、本発明の電気光学装置を液晶装置に適用したものである。

【００３５】

＜１－１：第１実施形態＞

図１から図７を参照して、本発明の第１実施形態に係る液晶装置について説明する。

【００３６】

＜１－１－１：液晶装置の概略構成＞

先ず、図１から図３を参照して、この液晶装置の概略構成について説明する。図１は、本実施形態に係る液晶装置の構成を示す平面図であり、図２は、図１のＩ－Ｉ’線断面を示している。図３は、本実施形態に係る液晶装置の比較例を示している。

【００３７】

図１及び図２において、液晶装置１００では、ＴＦＴアレイ基板１０に対向基板２０を所定間隔で対向させ、両基板の相対向する面の周縁をシール材５２ａで貼り合わせることによって、内部空間が形成されている。ＴＦＴアレイ基板１０には、平面的に見て対向基板２０より張り出してなる張り出し部２０１が存在し、シール材５２ａは、この張り出し部２０１が延在する辺における所定箇所（ここでは、この辺の両端）に対して、内部空間に通じる開口を規定している。そして、開口から内部空間に注入された液晶によって液晶層５０が構成され、開口は、封止モールド材１５１ａ及び１５１ｂによって夫々、封止されている。シール材５２ａの内縁に沿って設けられた額縁遮光膜５３は、画像が表示される画像表示領域１０ａを規定している。

【００３８】

ＴＦＴアレイ基板１０の対向面（図２中、上面）のうち、画像表示領域１０ａには、画素スイッチング用ＴＦＴや走査線、データ線等の配線の上層に、本発明の「表示用電極」の一例たる画素電極９ａが設けられている。そして、画素電極９ａの直上に配向膜が形成されている。対向基板２０の対向面（図２中、下面）には、ストライプ状の遮光膜２３を介して対向電極２１が形成されており、その上層に配向膜が形成されている。また、対向基板２０の角部の少なくとも１箇所（ここでは４箇所全部）には、ＴＦＴアレイ基板１０との間を電気的に導通させる上下導通端子１０６が設けられている。液晶層５０の液晶の配向状態は、画素電極９ａと対向電極２１との間に印加される電界に応じて変化するが、電界が印加されていない状態では、配向膜によって規定される初期配向をとる。

【００３９】

ＴＦＴアレイ基板１０の対向面のうち、額縁遮光膜５３の形成領域には、走査線を駆動する走査線駆動回路１０４と配線１０５とが設けられている。図１において、走査線駆動回路１０４は、額縁遮光膜５３の左右の辺に一つずつ設けられ、配線１０５は、これら２つの走査線駆動回路１０４の相互間を接続すべく、額縁遮光膜５３の上辺に引き回されている。

【００４０】

ＴＦＴアレイ基板１０の張り出し部２０１には、本発明の「駆動回路」の一具体例として、データ線を駆動するデータ線駆動回路１０１ａが、図１において、シール材５２ａの下辺に沿って配置されている。但し、平面的に見て、データ線駆動回路１０１ａの上半分は、シール材５２ａと重なるように設けられている。また、その下半分は、両端に封止モールド材１５１ａ及び１５１ｂの開口からはみ出した部分が夫々重なっている。

【００４１】

尚、本実施形態においては、ＴＦＴ等の電子素子や走査線、データ線等の配線、走査線駆動回路１０４やデータ線駆動回路１０１ａを含むＴＦＴアレイ基板１０上の回路全般が、本発明の「回路部」の具体例に対応している。また、張り出し部２０１には、データ線駆動回路１０１に加えて、複数のデータ線に画像信号を所定のタイミングで印加するサンプリング回路、複数のデータ線に所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の液晶装置１００の品質、欠陥等を検査するための検査回路等が形成されていてもよい。

【００４２】

更に、本実施形態では、張り出し部２０１において複数の引出し配線１０３ａの少なくとも一部が、平面的に見て、外部接続端子１０２ａと重畳するように設けられている。具体的には後述するが、この液晶装置１００では、外部接続端子１０２ａが形成されている

層と引出し配線１０３ａが形成されている層とは、例えば層間絶縁膜を介して積層され、外部接続端子１０２ａの形成領域と引出し配線１０３ａの形成領域とは少なくとも一部が重なり合っている。配線や端子となる導電膜は、２層或いはそれ以上に積層されてよく、各層の導電膜は単層膜又は多層膜のいずれであってもよい。

【００４３】

これら外部接続端子１０２ａは、ＦＰＣ１１０を介して接続された外部回路から液晶装置１００内に電源や信号を供給するために設けられており、夫々、引出し配線１０３ａを介して走査線駆動回路１０４やデータ線駆動回路１０１ａ等の駆動回路と適宜に接続されている。液晶装置１００では、これら外部接続端子１０２ａに外部入力された信号に応じて画素電極９ａが駆動され、画像が表示される。ここでデータ線駆動回路１０１ａは、張り出し部２０１側の両端において、引出し配線１０３ａを介して複数の外部接続端子１０２ａと接続されている。

【００４４】

図３に示したように、本実施形態の比較例に係る液晶装置においては、外部接続端子１０２と引出し配線１０３とは、平面的に見て互いに重なり合わないように、例えば同一平面上に配置される。外部接続端子１０２はまた、ＦＰＣ１１０と接続されなければならないので、その上に封止モールド材１５０が重なるのを防ぐために、ある程度、封止モールド材１５０から離しておく必要がある。結果的に、張り出し部２００は所定の幅Ｌ0を有し、データ線駆動回路１０１全体を配置できるだけのスペースが生じる。

【００４５】

これに対し、本実施形態の液晶装置１００では、以上に説明したように、外部接続端子１０２ａと引出し配線１０３ａの少なくとも一部とを、平面的に見て重畳するように配置したので、省スペース化が実現できる。特に、ここでは、外部接続端子１０２ａが張り出し部２０１の外縁に沿って配列されていることから、張り出し部２０１の、張り出し方向における幅Ｌ11を、通常より短縮することができる。

【００４６】

尚且つ、ここでは、封止モールド材１５１ａと封止モールド材１５１ｂとの間の領域に外部接続端子１０２ａを配置するようにしたので、外部接続端子１０２ａは封止モールド材１５１ａ及び１５１ｂに対して間隔をとらずに済む。更に、図１において、データ線駆動回路１０１ａの上半分をシール材５２ａが配置される領域に設けることで、外部接続端子１０２ａの位置を上側に押し上げることができる。以上の結果、張り出し部２０１の幅Ｌ11は、比較例における張り出し部２００の幅Ｌ0よりも短縮できる。

【００４７】

従って、本実施形態における液晶装置１００は省スペース化が可能であり、これを適用する電子機器に高い設計自由度を与えることができる。また、ウェハ一枚当たりから製造される液晶装置の個数を増やすことができ、製造効率の向上及び製造コスト低減に対して大きな効果を発揮する。即ち、１つの液晶装置１００における張り出し部２０１の縮小幅は、たとえ僅かであっても、ウェハ上には通常、上記ＴＦＴアレイ基板１０に対応する領域が数百ないし数千単位で形成され、更にそのようなウェハが多数生産されることから、製造上極めて有効である。

【００４８】

更に、ここでは、図１におけるシール材５２ａないし対向基板２０の下辺において、開口及び封止モールド材１５０ａ及び１５０ｂの夫々を両端部に配置し、外部接続端子１０２ａを中央部に配置するようにしたので、引出し配線１０３ａは、中央部から左右に分かれて引き回しても左右で配線長をほぼ等しくすることができ、左右における信号遅延等の不具合が生じずに済む。また、開口が左右両端に規定されていることから、内部空間に液晶を効率よく且つ均一に注入することができる。

【００４９】

＜１－１－２：張り出し部の構成＞

次に、図４から図７を参照して、液晶装置１００における張り出し部２０１の具体的構

成について、詳細に説明する。図４は、本実施形態に係る液晶装置の張り出し部における主要部分を拡大して表しており、図５は、図４のＡ－Ａ’線断面を表している。図６は、本実施形態に係る液晶装置の画像表示領域において、画素部が構成する等価回路を表している。図７及び図８は、画素部の構造を表す平面図と断面図である。尚、図８の（ａ）は、図７のＩＩ－ＩＩ’線断面を表しており、（ｂ）は、図７のＩＩＩ－ＩＩＩ’線断面を表している。また、図８においては、各層・各部材を図面上で認識可能な程度の大きさとするため、該各層・各部材の縮尺比率を適宜に変えてある。

【００５０】

図４において、複数の外部接続端子１０２ａは一方向に配列されており、複数の引出し配線１０３ａの夫々は、外部接続端子１０２ａの配列方向に延びると共に、外部接続端子１０２ａとコンタクトホール２０ａを介して接続されている。コンタクトホール２０ａは、各外部接続端子１０２ａの外縁に複数設けられている。尚、こうしたコンタクトホールの全部又は一部は、各外部接続端子１０２ａの内縁側に設けられていてもよい。

【００５１】

このようなレイアウトでは、引出し配線１０３ａは、自身が延在する領域からそれた領域で外部接続端子１０２ａと接続されることから、例えばコンタクトホール２０ａの形成位置の誤差等によって、外部接続端子１０２ａと、接続対象の引出し配線１０３ａと隣接して延びる引出し配線１０３ａとが誤って導通することが防止できる。よって、この液晶装置１００は、信頼性高く製造することができる。

【００５２】

図５において、このような外部接続端子１０２ａと引出し配線１０３ａとは、層間絶縁膜４３を介して積層されている。また、コンタクトホール２０ａは、この層間絶縁膜４３を貫通するように形成されている。引出し配線１０３ａは、このように所望の外部接続端子１０２ａとコンタクトホール２０ａを介して接続されつつも、それ以外の外部接続端子１０２ａとは層間絶縁膜４３によって絶縁されることによって、平面的に見て外部接続端子１０２ａと重ね合わせられている。

【００５３】

ここで、ＴＦＴアレイ基板１０上には、下地絶縁膜１２、層間絶縁膜４１～４４が順に積層されており、層間絶縁膜４２上に引出し配線１０３ａが設けられ、その上の層間絶縁膜４３上に外部接続端子１０２ａが設けられている。ここで、引出し配線１０３ａ及び外部接続端子１０２ａは共にアルミニウム層４０Ａ、窒化チタン層４０ＴＮの２層からなり、外部接続端子１０２ａの露出面Ｄ（図４中、外部接続端子１０２ａの斜線領域）層間絶縁膜４４及び窒化チタン層４０ＴＮを部分的に除去して形成された開口から外表に対して露出している。このような積層構造は、ＴＦＴアレイ基板１０上の画像表示領域１０ａにおける積層構造を準用して構成されている。そこで次に、画像表示領域１０ａにおける積層構造の構成について説明する。

【００５４】

＜１－１－３：画像表示領域の構成＞

図６において、画像表示領域１０ａには、複数の走査線１１ａ及び複数のデータ線６ａが相交差して配列しており、その線間に、走査線１１ａ，データ線６ａの各一によって選択される画素部が構成されている。各画素部は、ＴＦＴ３０、画素電極９ａ及び蓄積容量７０を含む。ＴＦＴ３０は、データ線６ａから供給される画像信号Ｓ１、Ｓ２、…、Ｓｎを選択画素に印加するために設けられ、ゲートが走査線１１ａに接続され、ソースがデータ線６ａに接続され、ドレインが画素電極９ａに接続されている。画素電極９ａは、後述の対向電極２１との間で液晶容量を形成し、入力される画像信号Ｓ１、Ｓ２、…、Ｓｎを一定期間保持するようになっている。即ち、画素電極９ａによって画素部毎の開口領域が画定される。蓄積容量７０の一方の電極は、画素電極９ａと並列にＴＦＴ３０のドレインと接続され、他方の電極は、定電位となるように電位固定の容量配線４００に接続されている。

【００５５】

液晶装置１００は、例えばＴＦＴアクティブマトリクス駆動方式を採り、走査線駆動回路１０４（図１参照）から各走査線１１ａに走査信号Ｇ１、Ｇ２、…、Ｇｍが線順次に印加されると共に、それによってＴＦＴ３０がオン状態となる水平方向の選択画素部の列に対し、データ線駆動回路１０１（図１参照）からの画像信号Ｓ１、Ｓ２、…、Ｓｎを、データ線６ａを通じて印加される。その結果、選択画素に対応する画素電極９ａに画像信号が供給される。ＴＦＴアレイ基板１０は、液晶層５０を介して対向基板２０と対向配置されているので（図２参照）、こうして画素部毎に液晶層５０に電界を印加することにより、両基板間の透過光量が画素毎に制御され、画像が階調表示される。このとき各画素部に保持された画像信号は、蓄積容量７０によりリークが防止される。

【００５６】

図７及び図８においては、上述した画素部の各回路要素がパターン化され、積層された導電膜としてＴＦＴアレイ基板１０上に構築されている。本実施形態のＴＦＴアレイ基板１０は、石英基板からなり、ガラス基板や石英基板等からなる対向基板２０と対向配置されている。また、各回路要素は、下から順に、走査線１１ａを含む第１層、ゲート電極３ａを含む第２層、蓄積容量７０の固定電位側容量電極を含む第３層、データ線６ａ等を含む第４層、容量配線４００等を含む第５層、画素電極９ａ等を含む第６層からなる。また、第１層－第２層間には下地絶縁膜１２、第２層－第３層間には第１層間絶縁膜４１、第３層－第４層間には第２層間絶縁膜４２、第４層－第５層間には第３層間絶縁膜４３、第５層－第６層間には第４層間絶縁膜４４が夫々設けられ、前述の各要素間の短絡が防止されている。

【００５７】

（第１層の構成―走査線等―）

第１層は、走査線１１ａで構成される。走査線１１ａは、図７のＸ方向に沿って延びる本線部と、データ線６ａ或いは容量配線４００が延在する図７のＹ方向に延びる突出部とからなる形状にパターニングされている。このような走査線１１ａは、例えば導電性ポリシリコンからなり、その他にもチタン（Ｔｉ）、クロム（Ｃｒ）、タングステン（Ｗ）、タンタル（Ｔａ）、モリブデン（Ｍｏ）等の高融点金属のうちの少なくとも一つを含む金属単体、合金、金属シリサイド、ポリシリサイド又はこれらの積層体等により形成することができる。即ち、本実施形態における走査線１１ａは、できるだけ開口領域の間の領域を覆うことで、ＴＦＴ３０を下側から遮光する遮光膜としても機能する。

【００５８】

（第２層の構成―ＴＦＴ等―）

第２層は、ＴＦＴ３０及び中継電極７１９で構成されている。ＴＦＴ３０は、例えばＬＤＤ（Lightly Doped Drain）構造とされ、ゲート電極３ａ、半導体層１ａ、ゲート電極３ａと半導体層１ａを絶縁するゲート絶縁膜２を備えている。ゲート絶縁膜２は、例えば、ＨＴＯ（High Temperature Oxide）や熱酸化されたシリコン酸化膜からなる。ゲート電極３ａは、例えば導電性ポリシリコンで形成される。半導体層１ａは、例えばポリシリコンからなり、チャネル領域１ａ’、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ、並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅからなる。中継電極７１９は、例えばゲート電極３ａと同一膜として形成される。

【００５９】

ＴＦＴ３０のゲート電極３ａは、下地絶縁膜１２に形成されたコンタクトホール１２ｃｖを介して走査線１１ａに電気的に接続されている。下地絶縁膜１２は、例えば、ＨＴＯ等のシリコン酸化膜、或いはＮＳＧ（ノンシリケートガラス）膜からなり、第１層と第２層との層間を絶縁する他、ＴＦＴアレイ基板１０の全面に形成されることで、基板表面の研磨による荒れや汚れ等が惹き起こすＴＦＴ３０の素子特性の変化を防止する機能を有している。

【００６０】

（第３層の構成―蓄積容量等―）

第３層は、蓄積容量７０で構成されている。蓄積容量７０は、容量電極３００と下部電

極７１とが誘電体膜７５を介して対向配置された構成となっている。このうち、容量電極３００は、コンタクトホール８０１、８０３及び容量配線用中継層６ａ１を介して容量配線４００と電気的に接続されている。下部電極７１と高濃度ドレイン領域１ｅとは、第１層間絶縁膜４１に開孔されたコンタクトホール８３を介して接続されている。また、下部電極７１と画素電極９ａとは、コンタクトホール８８１、８８２、８０４及び中継電極７１９、第２中継電極６ａ２、第３中継電極４０２により各層を中継し、コンタクトホール８９において電気的に接続されている。

【００６１】

容量電極３００は、例えば、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ等の高融点金属のうちの少なくとも一つを含む金属単体、合金、金属シリサイド、ポリシリサイドからなる単層ないし多層膜、好ましくはタングステンシリサイドからなり、ＴＦＴ３０に図８の上側から入射しようとする光を遮る機能を有している。下部電極７１には、例えば導電性のポリシリコンが用いられる。誘電体膜７５は、例えば、膜厚５～２００ｎｍ程度の比較的薄いＨＴＯ膜、ＬＴＯ（Low Temperature Oxide）膜等の酸化シリコン膜、或いは窒化シリコン膜等からなる。

【００６２】

また、第１層間絶縁膜４１は、例えば、ＮＳＧによって形成されている。その他、第１層間絶縁膜４１には、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）等のシリケートガラス、窒化シリコンや酸化シリコン等を用いることができる。

【００６３】

（第４層の構成―データ線等―）

第４層は、データ線６ａ、容量配線用中継層６ａ１及び第２中継電極６ａ２で構成されている。データ線６ａは、アルミニウム膜、窒化チタン膜の２層からなり、窒化シリコン膜によって表面を被覆されている。データ線６ａは、第１層間絶縁膜４１及び第２層間絶縁膜４２を貫通するコンタクトホール８１を介して、ＴＦＴ３０の高濃度ソース領域１ｄと電気的に接続されている。更に、データ線６ａと同一膜として、容量配線用中継層６ａ１及び第２中継電極６ａ２が形成されている。

【００６４】

また、第２層間絶縁膜４２は、例えばＮＳＧからなり、その他、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス、窒化シリコンや酸化シリコン等によって形成することができる。

【００６５】

（第５層の構成―容量配線等―）

第５層は、容量配線４００及び第３中継電極４０２により構成されている。容量配線４００は、画像表示領域１０ａの周囲にまで延設され、周辺駆動回路に供給される電源や上下導通端子を介して対向基板に供給される対向電極電位等の定電位源と電気的に接続されることで、固定電位とされている。また、容量配線４００は、第３層間絶縁膜４３に開孔されたコンタクトホール８０３を介して、容量配線用中継層６ａ１と電気的に接続されている。このような容量配線４００は、例えばアルミニウム膜、窒化チタン膜を積層した二層構造となっている。

【００６６】

容量配線４００は、図７に示すように、Ｘ方向、Ｙ方向に延在する格子状に形成され、Ｘ方向に延在する部分には、第３中継電極４０２の形成領域を確保するために切り欠きが設けられている。更に、容量配線４００は、遮光膜としても機能し、下層のデータ線６ａ、走査線１１ａ、ＴＦＴ３０等を覆うように、これらの回路要素よりも幅広に形成され、非開口領域を最終的に規定する形状となっている。更に、第５層には、容量配線４００と同一膜として、第３中継電極４０２が形成されている。

【００６７】

第５層の下には、全面に第３層間絶縁膜４３が形成されている。第３層間絶縁膜４３は

、例えばＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス、窒化シリコンや酸化シリコン等によって形成することができる。また、第３層間絶縁膜４３の表面を平坦化するためにＣＭＰ（Chemical Mechanical Polishing）等により研磨しても良いし、ＳＯＧ（Spin On Glass）等により平坦化膜を形成しても良い。平坦化により、配線間の段差等によるクラック発生を防止することができる。

【００６８】

（第６層の構成―画素電極等―）

第５層の全面には第４層間絶縁膜４４が形成され、更にその上に、第６層として画素電極９ａが形成されている。第４層間絶縁膜４４には、画素電極９ａ－第３中継電極４０２間を電気的に接続するためのコンタクトホール８９が開孔されている。このような第４層間絶縁膜４４は、例えばＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧ等のシリケートガラス、窒化シリコンや酸化シリコン等によって形成することができる。また、第４層間絶縁膜４４の表面を平坦化するためにＣＭＰ等により研磨しても良いし、ＳＯＧ等により平坦化膜を形成しても良い。平坦化により、配線間の段差等によるクラック発生を防止する事ができる。

【００６９】

画素電極９ａ（図７中、破線９ａ’で輪郭が示されている）は、縦横に区画配列された画素領域の各々と略対応して配置されている。このような画素電極９ａは、例えばＩＴＯ（Indium Tin Oxide）等の透明導電膜からなる。更に、画素電極９ａ上には、配向膜１６が形成されている。以上が、ＴＦＴアレイ基板１０側の画素部の構成である。

【００７０】

因みに、対向基板２０には、その対向面の全面に対向電極２１が設けられており、更にその上（図８では対向電極２１の下側）に配向膜２２が設けられている。対向電極２１は、画素電極９ａと同様、例えばＩＴＯ膜等の透明導電性膜からなる。対向基板２０と対向電極２１の間には、ＴＦＴ３０における光リーク電流の発生等を防止するため、少なくともＴＦＴ３０と正対する領域を覆うように遮光膜２３が設けられている。

【００７１】

本実施形態においては、このような画像表示領域１０ａの積層構造の延長上に、張り出し部２０１が形成されている。即ち、張り出し部２０１では、引出し配線１０３ａがデータ線６ａ等の同一膜として第４層に形成され、外部接続端子１０２ａが容量配線４００等と同一膜として第５層に形成されている（図５及び図８を参照）。そのため、図５に示したような引出し配線１０３ａと外部接続端子１０２ａとが層間絶縁膜を介して積層された構造を、画像表示領域１０ａの積層構造とは別に設けずに済む。よって、ＴＦＴアレイ基板１０上の構造が簡素化でき、比較的容易に形成することが可能である。

【００７２】

また、ここでは、第４層と第５層とが共にアルミニウムを含むことから、データ線６ａ、容量配線４００は勿論のこと、引出し配線１０３ａ及び外部接続端子１０２ａもまた、低抵抗に構成される。因みに、第４層及び第５層は、熱処理が必要な蓄積容量７０やＴＦＴ３０の上層に位置することにより、耐熱性の低いアルミニウムを用いることが可能となっている。ここでは、画像表示領域１０ａにおける積層構造のうち、第４層及び第５層に引出し配線１０３ａ及び外部接続端子１０２ａの夫々を設けることで、配線の低抵抗化と、外部接続端子１０２ａの露出面Ｄを容易に形成することが可能となる。

【００７３】

＜１－２：変形例＞

次に、図９及び図１０を参照して、第１実施形態の変形例に係る液晶装置について説明する。図９は、第１実施形態の変形例に係る液晶装置のうち、張り出し部における主要部分を拡大して表しており、図１０は、図９のＢ－Ｂ’線断面を表している。

【００７４】

本発明に係る外部接続端子及び引出し配線は、平面的に見て、少なくとも部分的に重畳するように配置されていればよく、そのレイアウトは、上記第１実施形態に説明した場合

以外にも種々の変形実施が可能である。

【００７５】

図９においては、そのような一例として、複数の外部接続端子１０２ｂは一方向に配列されており、引出し配線１０３ｂとコンタクトホール２０ｂを介して接続されている。コンタクトホール２０ｂは、平面的に見て、複数の引出し配線１０３ｂが複数の外部接続端子１０２ｂと交差する領域の夫々に設けられている。

【００７６】

このようなレイアウトでは、引出し配線１０３ｂは、自身が延在する領域で外部接続端子１０２ｂと接続されることから、コンタクトホールを形成するための領域を別途設けずに済み、引出し配線及び外部接続端子の配置スペースを、例えば第１実施形態に比べて小さくすることが可能である（図５及び図１０を参照）。よって、本変形例では、張り出し部の幅がより短縮され、ＴＦＴアレイ基板のサイズを更に縮小することが可能である。

【００７７】

＜１－３：第２実施形態＞

次に、図１１から図１３を参照して、第２実施形態に係る液晶装置について説明する。ここに、図１１は、本実施形態に係る液晶装置の概略構成を表している。図１２は、第２実施形態に係る液晶装置のうち、張り出し部における主要部分を拡大して表しており、図１３は、図１２のＣ－Ｃ’線断面を表している。尚、本実施形態の液晶装置１００Ａは、張り出し部内のレイアウトが異なることを除けば、液晶装置１００と同様に構成されていることから、液晶装置１００と同様の構成要素については、同一の符号を付して、その説明を適宜省略する。

【００７８】

図１１において、液晶装置１００Ａでは、張り出し部２０２の外縁に沿って配列された複数の外部接続端子１０２ｃに対し、データ線駆動回路１０１ｃ及び引出し配線１０３ｃの夫々が、平面的に見て部分的に重畳された状態で配置されている。このように張り出し部２０２のレイアウトを工夫することで、張り出し部２０２の幅Ｌ12を短縮することができ、ＴＦＴアレイ基板１０のサイズの縮小によって上記第１実施形態と同様の効果を奏する。

【００７９】

図１２及び図１３には、その様子が拡大表示されている。引出し配線１０３ｃは、第１実施形態の変形例と同様、外部接続端子１０２ｃと交差する領域に設けられたコンタクトホール２０ｃによって外部接続端子１０２ｃと接続されている。その一方、引出し配線１０３ｃは、自身が延在する領域に設けられたコンタクトホール２１ｃによってデータ線駆動回路１０１ｃと接続されている。

【００８０】

ここでは、ＴＦＴアレイ基板１０上の積層構造のうち、引出し配線１０３ｃは第４層に、外部接続端子１０２ｃは第５層に設けられており、コンタクトホール２０ｃは層間絶縁膜４３を貫通するように設けられている。データ線駆動回路１０１ｃは、第１層から第５層の少なくともいずれか（図示した範囲では第２層と第４層）に設けられており、コンタクトホール２１ｃは層間絶縁膜４１及び４２を貫通するように設けられている。

【００８１】

このように本実施形態においては、外部接続端子１０２ｃと引出し配線１０３ｃの夫々が、データ線駆動回路１０１ｃや画像表示領域１０ａにおける回路部分を構成する導電膜と同一膜として、或いはそのような導電膜の同一膜を含んで形成されることから、ＴＦＴアレイ基板１０上の構造が簡素化でき、比較的容易に形成することが可能である。その他の作用及び効果は上記第１実施形態と同様であり、第２実施形態に対しても第１実施形態に対する変形と同様の変形実施が可能である。

【００８２】

また、上記第２実施形態では、外部接続端子１０２ｃと引出し配線１０３ｃ、外部接続端子１０２ｃとデータ線駆動回路１０１ｃの夫々が平面的に見て重畳するようにしたが、

図１４に示したように、外部接続端子に対してデータ線駆動回路のみが重畳されるようなレイアウトにおいても張り出し部の幅が短縮され、本発明の効果を得ることができる。

【００８３】

＜２：電子機器＞

次に、図１５を参照して、以上に説明した液晶装置を電子機器に適用する場合について説明する。ここでは、本発明に係る電子機器の一例として、上述の液晶装置をライトバルブとして用いたプロジェクタについて説明する。図１５は、このプロジェクタの構成例を示している。

【００８４】

図１５において、プロジェクタ１１００内部には、ハロゲンランプ等の白色光源からなるランプユニット１１０２が設けられている。このランプユニット１１０２から射出された投射光は、ライトガイド内に配置された４枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によってＲＧＢの３原色に分離され、各原色に対応するライトバルブとしての液晶装置１００Ｒ、１００Ｂ及び１００Ｇに入射される。液晶装置１００Ｒ、１００Ｂ及び１００Ｇの構成は上述した液晶装置と同等であり、夫々において画像信号処理回路から供給されるＲ、Ｇ、Ｂの原色信号が変調される。液晶装置１００Ｒ、１００Ｂ及び１００Ｇによって変調された光は、ダイクロイックプリズム１１１２に３方向から入射される。これにより各色の画像が合成され、投射レンズ１１１４を介して、スクリーン１１２０等にカラー画像が投写される。

【００８５】

尚、本発明の電気光学装置は、上述の液晶装置以外に、例えば有機ＥＬ装置、電子ペーパ等の電気泳動装置、電子放出素子を利用した表示装置（Field Emission Display及びSurface-Conduction Electron-Emitter Display）等の各種装置として実現可能である。

【００８６】

また、このような本発明の電気光学装置は、先に説明したプロジェクタ以外にも、テレビジョン受像機や、ビューファインダ型或いはモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、ページャ、電子手帳、電卓、ワードプロセッサ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等の、各種の電子機器に対して適用可能である。

【００８７】

本発明は、上述した実施形態及び実施例に限られるものではなく、請求の範囲及び明細書全体から読み取れる発明の要旨或いは思想に反しない範囲で適宜変更可能であり、そのような変更を伴う電気光学装置及びこれを備えた電子機器もまた、本発明の技術的範囲に含まれるものである。

【図面の簡単な説明】

【００８８】

【図１】本発明の第１実施形態に係る液晶装置の構成を示す平面図である。

【図２】図１に示した液晶装置のＩ－Ｉ’線における断面図である。

【図３】第１実施形態に係る液晶装置の比較例を示す平面図である。

【図４】第１実施形態に係る液晶装置の主要部分の構成を示す平面図である。

【図５】図４に示した張り出し部のＡ－Ａ’線における断面図である。

【図６】第１実施形態に係る液晶装置の画像表示領域における等価回路を示す模式図である。

【図７】第１実施形態に係る液晶装置の画像表示領域の構成を示す平面図である。

【図８】第１実施形態に係る液晶装置の画像表示領域の構成を示す断面図であり、（ａ）は図７のＩＩ－ＩＩ’線における断面図、（ｂ）は図７のＩＩＩ－ＩＩＩ’線における断面図である。

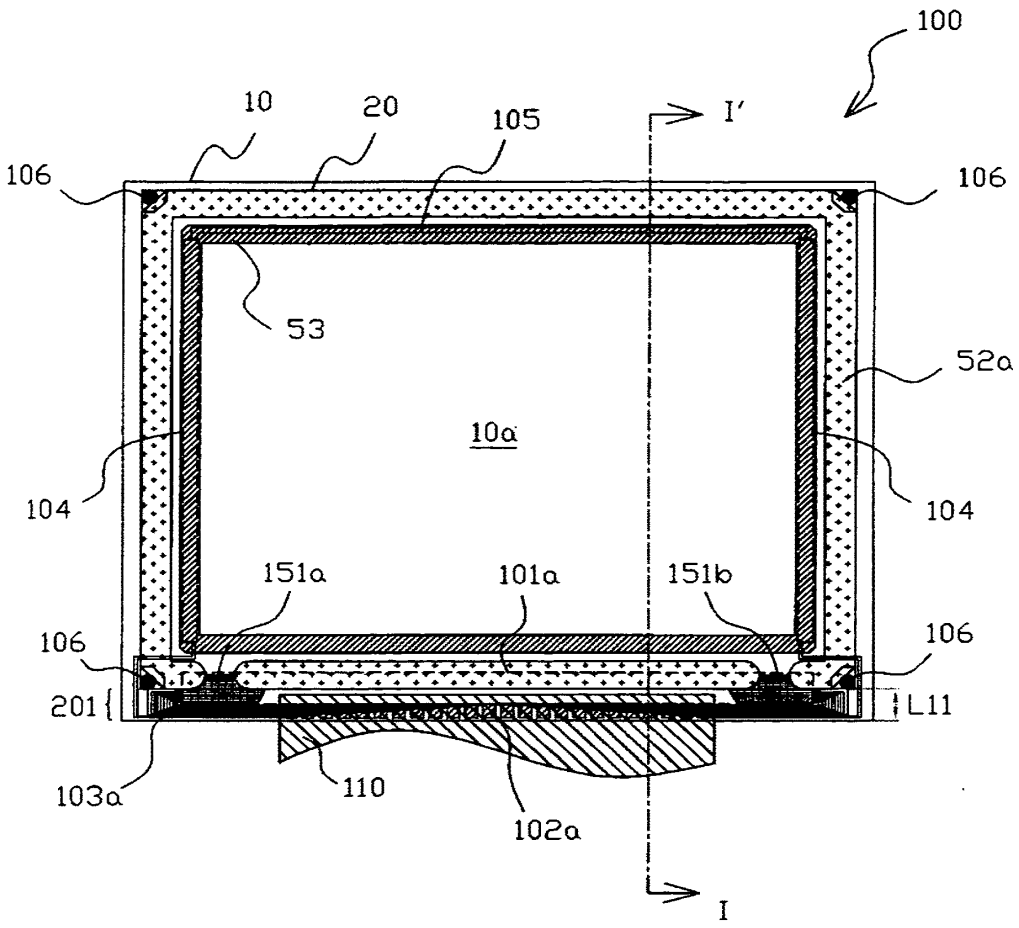
【図９】第１実施形態に係る液晶装置の変形例を示す平面図である。

【図１０】図９に示した張り出し部のＢ－Ｂ’線における断面図である。

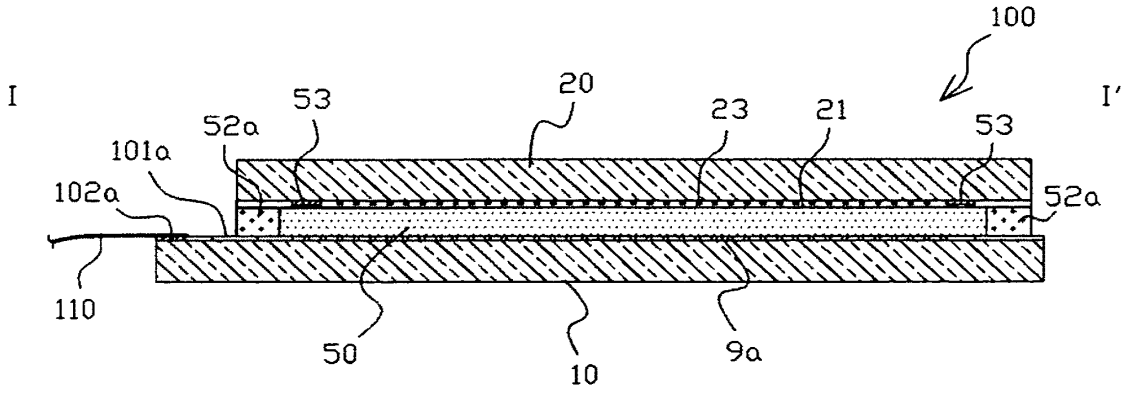
【図１１】第２実施形態に係る液晶装置の構成を示す平面図である。

【図１２】第２実施形態に係る液晶装置における主要部分の構成を示す平面図である。
【図１３】図１２に示した張り出し部のＣ－Ｃ’線における断面図である。
【図１４】第２実施形態に係る液晶装置の変形例を示す平面図である。
【図１５】本発明の電子機器の実施形態に係る液晶プロジェクタの構成を表す断面図である。
【符号の説明】
【００８９】
１０…ＴＦＴアレイ基板、９ａ…画素電極、１０ａ…画像表示領域、２０…対向基板、２１…対向電極、５０…液晶層、５２、５２ａ…シール材、５３…額縁遮光膜、１０１、１０１ａ～１０１ｄ…データ線駆動回路、１０２、１０２ａ～１０２ｄ…外部接続端子、１０３ａ～１０３ｄ…配線、１０４…走査線駆動回路、１０５…配線、１０６…上下導通端子、１１０…フレキシブルプリント回路（ＦＰＣ）、２００～２０２…張り出し部、１５０～１５３…封止モールド材、Ｌ0、Ｌ11、Ｌ12…（張り出し部の）幅。

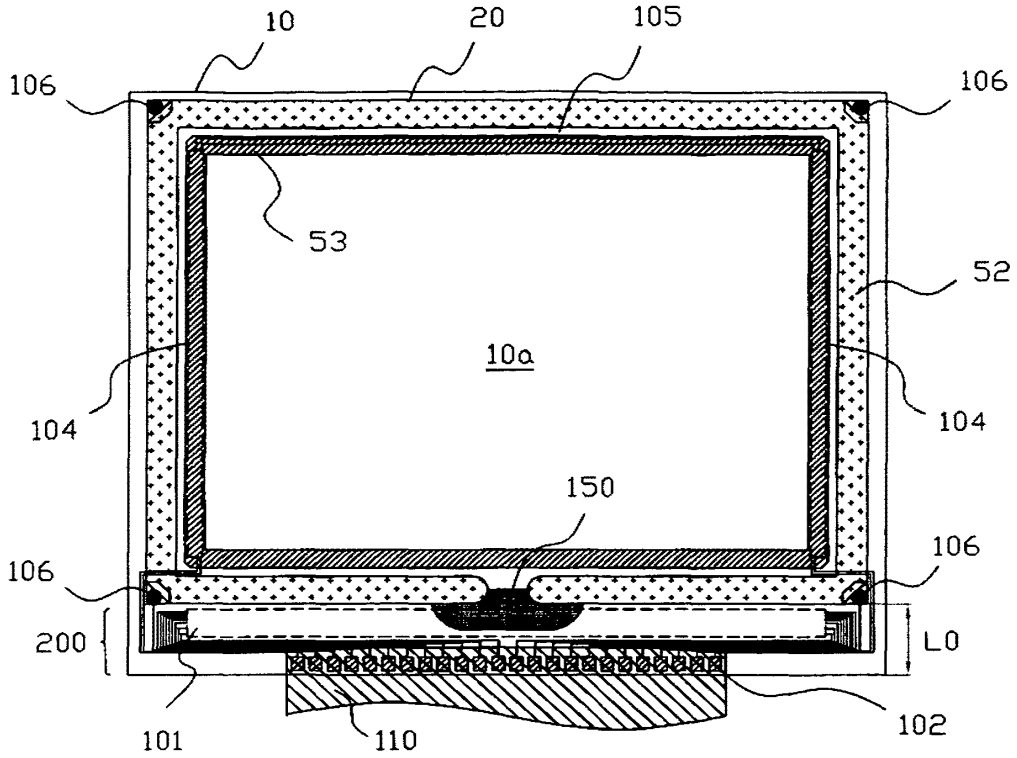
【書類名】図面
【図１】


100
10
20
105
I'
106
106
53
52a
10a
104
104
151a
101a
151b
106
106
201
L11
103a
110
102a
I

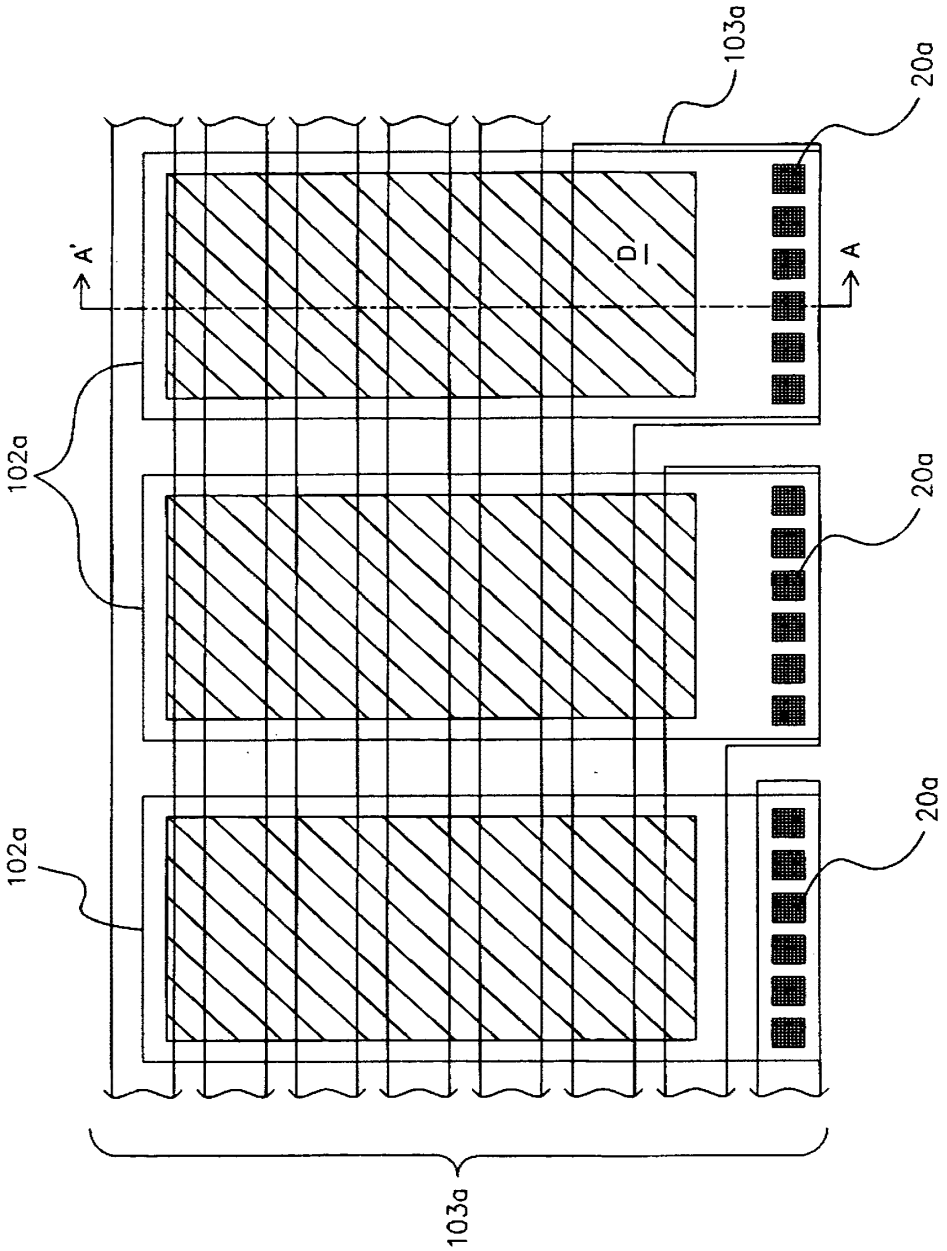
【図２】


100
I
I'
53
20
23
21
53
52a
101a
102a
52a
110
50
10
9a

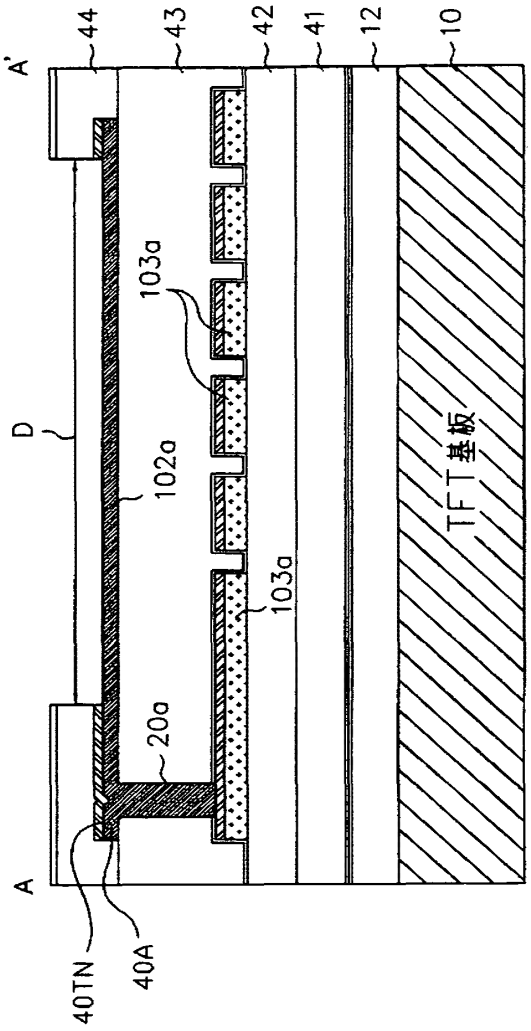
【図３】



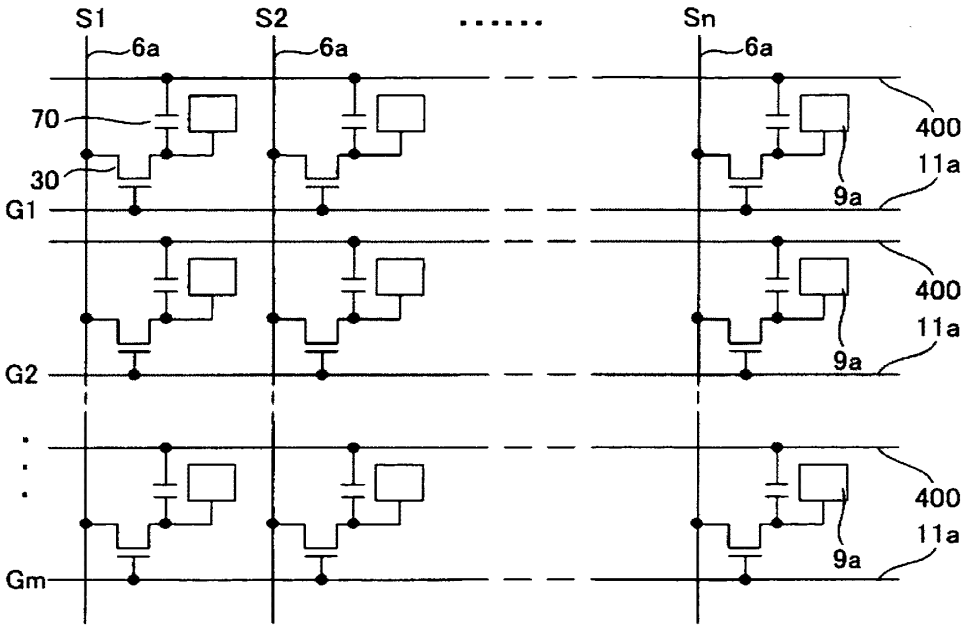
【図４】



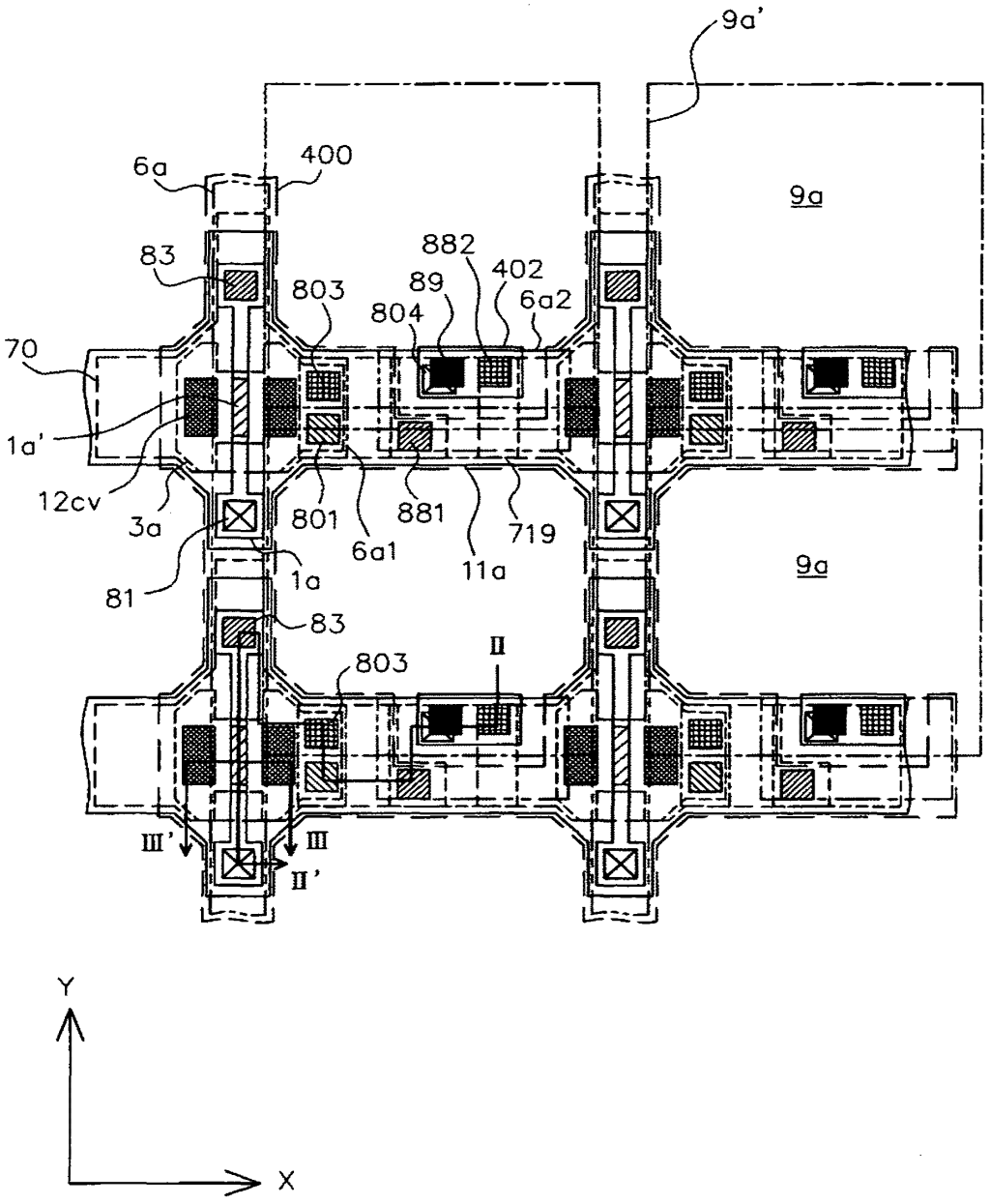
【図５】



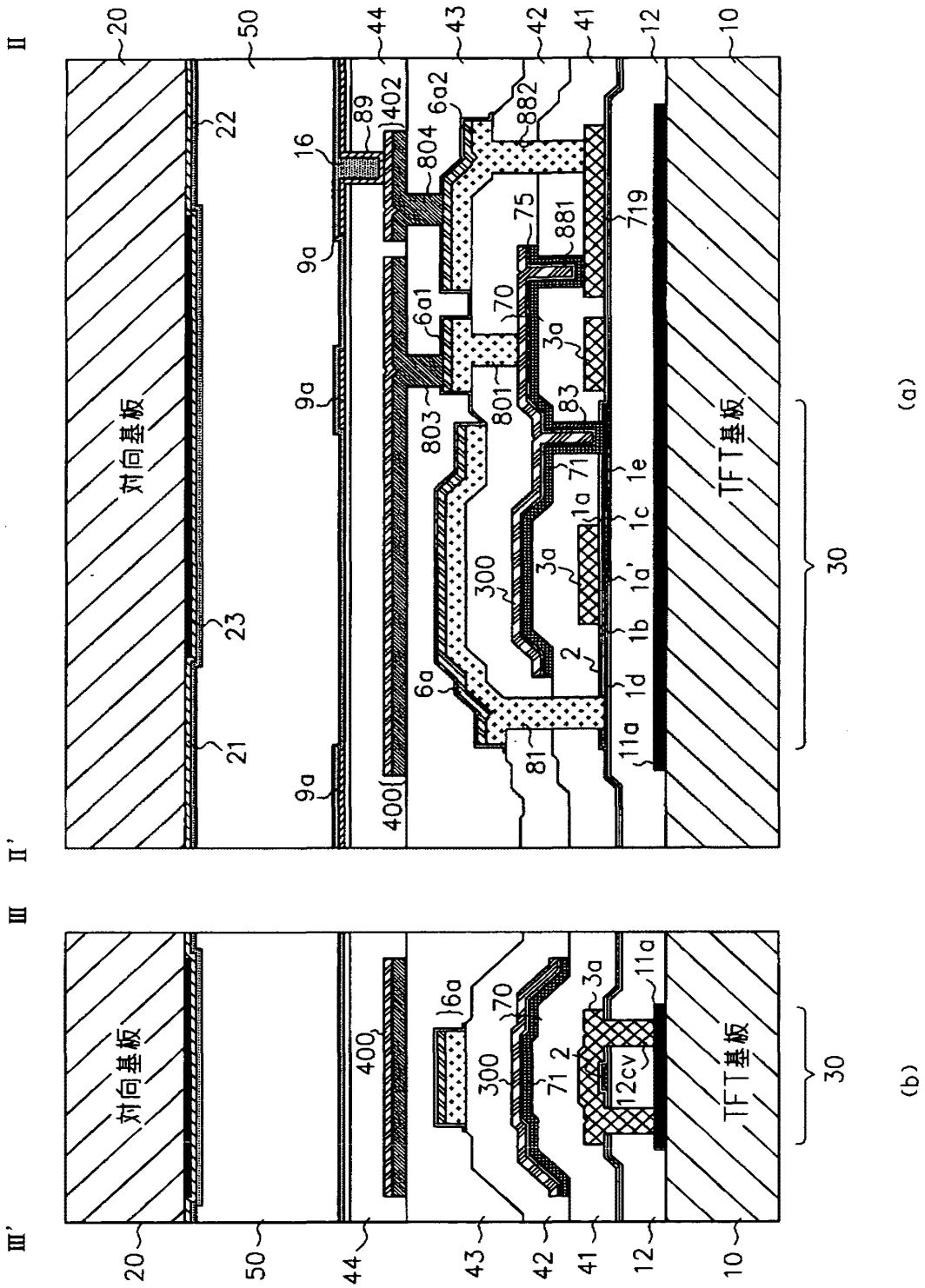
【図６】



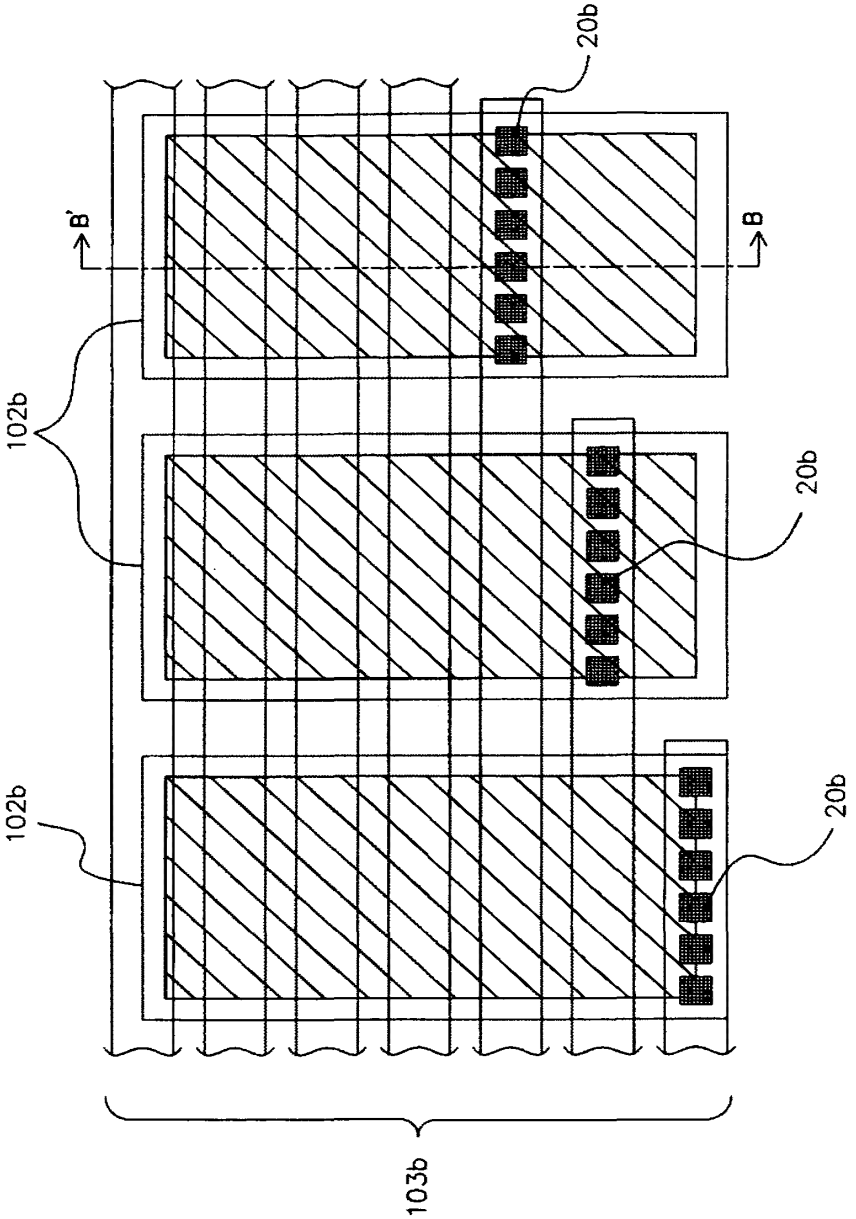
【図７】


9a'
6a
400
9a
83
882
402
89
803
804
6a2
70
1a'
12cv
3a
801
881
719
6a1
11a
9a
81
1a
83
803
II
III'
III
II'
Y
X

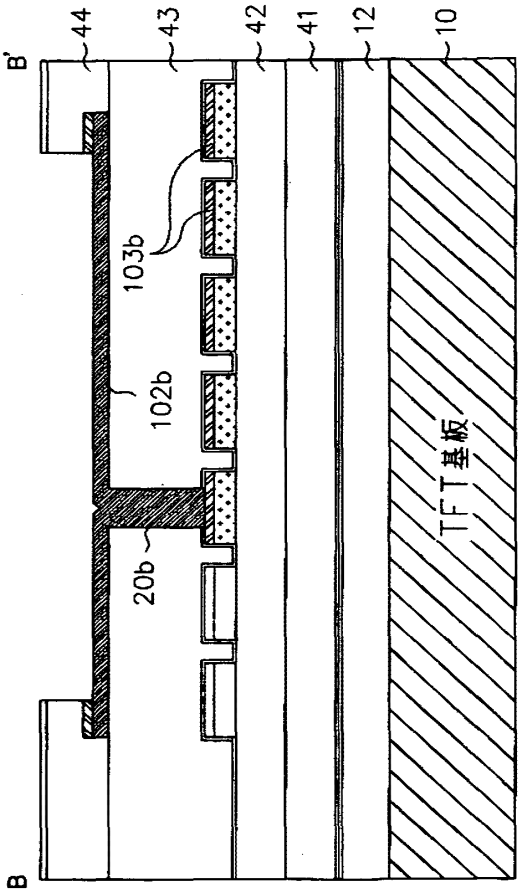
【図８】


II
II'
III
III'
対向基板
TFT基板
20
50
44
43
42
41
12
10
22
16
89
402
804
6a2
882
9a
75
881
719
6a1
70
3a
801
83
803
71
1e
1a
1c
300
1a'
1b
2
1d
6a
11a
81
400
30
(a)
(b)
12cv

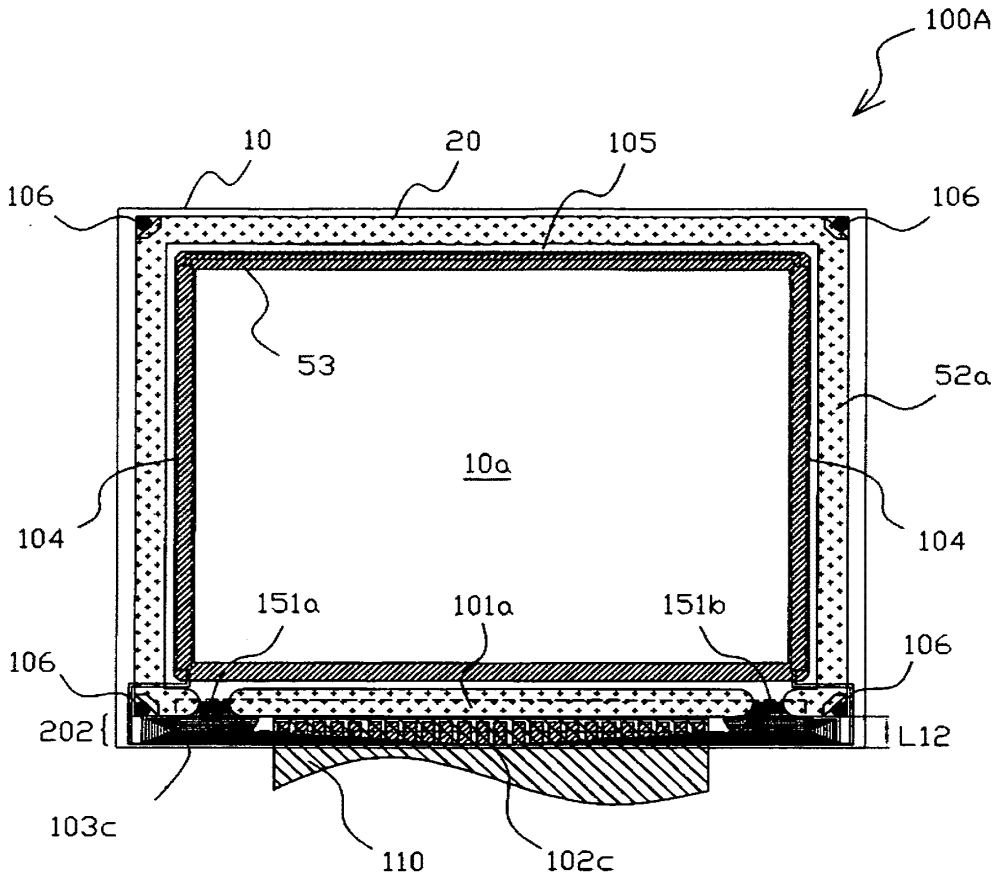
【図９】



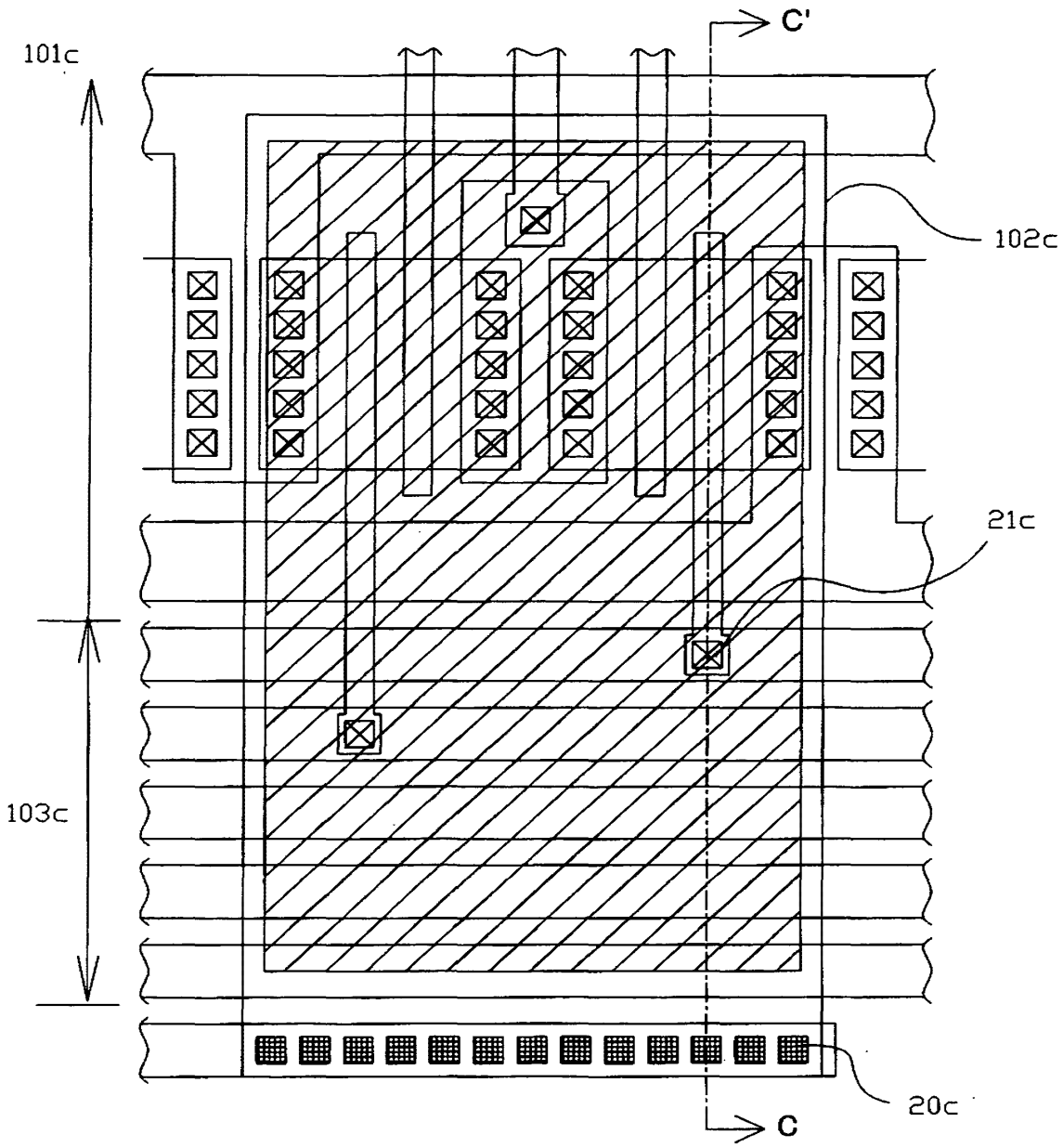
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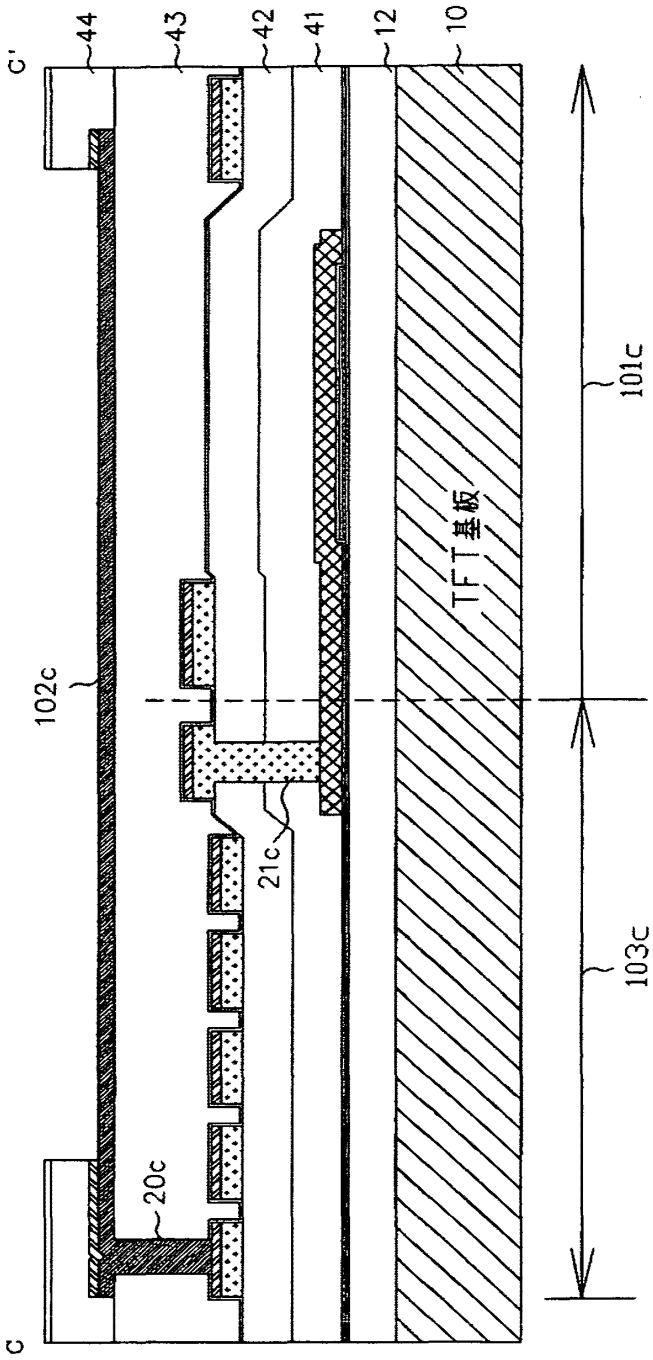
【図１１】


100A
10
20
105
106
106
53
52a
10a
104
104
151a
101a
151b
106
106
202
L12
103c
110
102c

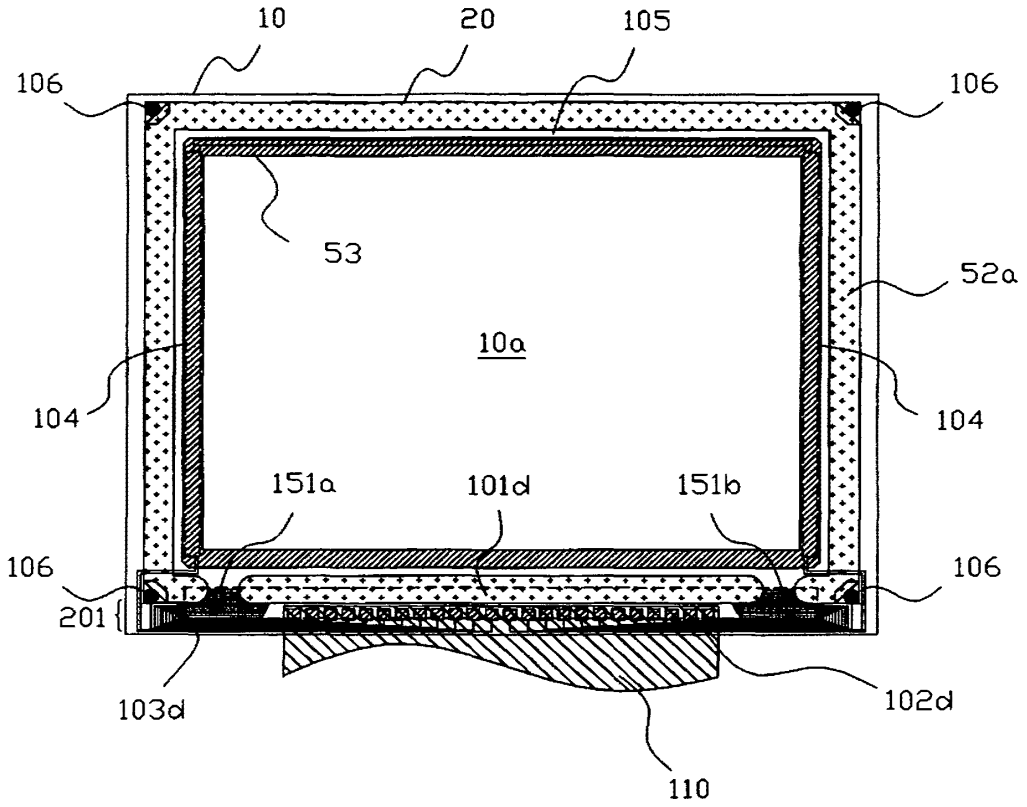
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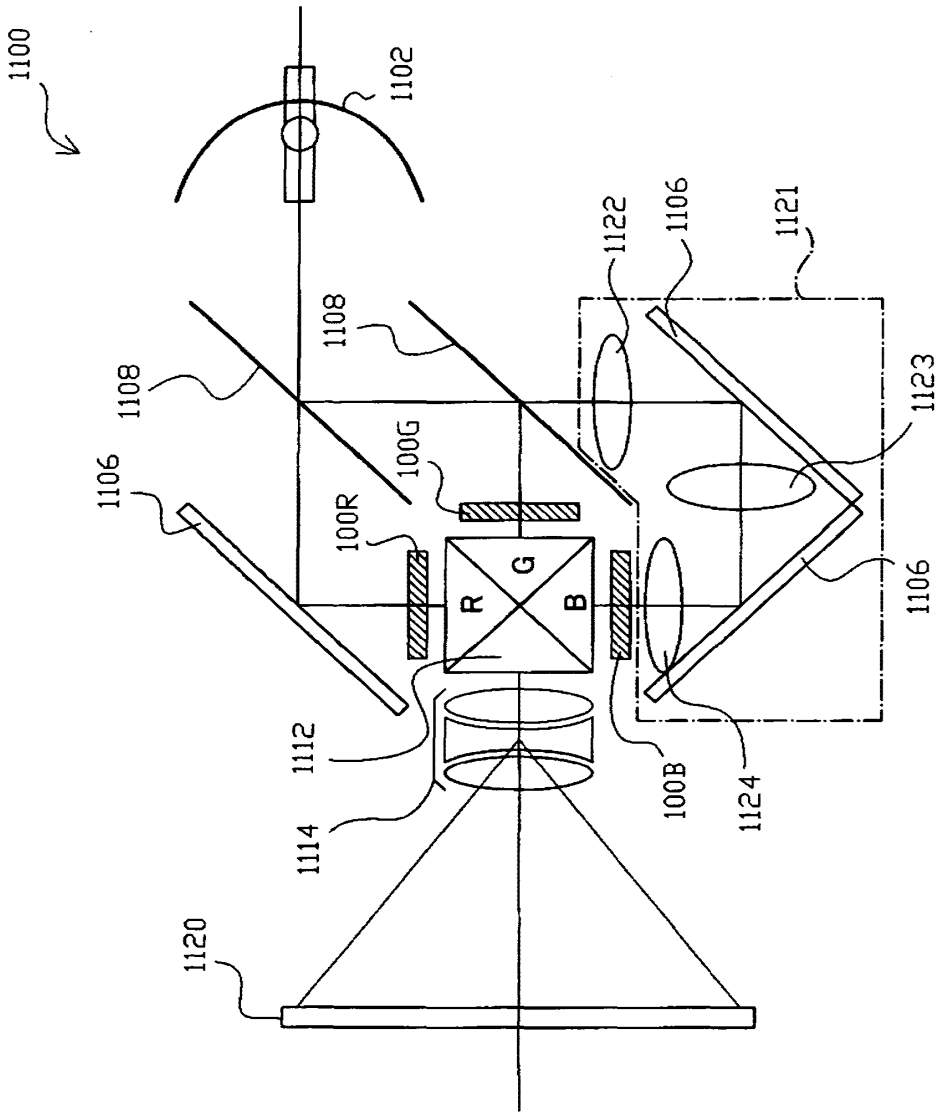
【図１３】



【図１４】


10
20
105
106
106
53
52a
10a
104
104
151a
101d
151b
106
106
201
103d
102d
110

【図１５】


1100
1102
1122
1106
1121
1108
1108
1123
100G
1106
100R
G
R
B
1106
1112
100B
1124
1114
1120

【書類名】要約書
【要約】
【課題】　液晶装置等の電気光学装置における基板サイズを縮小する。
【解決手段】
所定間隔で相対向すると共に平面的に見て少なくとも一辺において一方の基板（１０）が他方の基板（２０）より張り出している一対の基板を備える。一方の基板には、表示用電極を駆動する回路部が設けられ、前記一辺において張り出してなる張り出し部（２０１）における他方の基板と対向する側の面には、回路部と引出し配線（１０３ａ）によって電気的に接続された複数の外部接続端子（１０２ａ）が設けられている。外部接続端子は、平面的に見て、引き出し配線と少なくとも部分的に重畳するように設けられる。
【選択図】　図１

認定・付加情報

特許出願の番号	特願２００４－３２８９８２
受付番号	５０４０１９３７６８６
書類名	特許願
担当官	第四担当上席　００９３
作成日	平成１６年１１月１５日

＜認定情報・付加情報＞

【提出日】　平成16年11月12日

出証特２００５－３０６７３９０

特願２００４－３２８９８２

出　願　人　履　歴　情　報

識別番号　［０００００２３６９］

１．変更年月日　１９９０年　８月２０日
［変更理由］　新規登録
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出証番号　出証特２００５－３０６７３９０

13281 U.S.PTO 091305

NONPROVISIONAL PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Attorney Docket No.: 125312

Date: September 13, 2005

113277 U.S.PTO 11/223919 091305

MAIL STOP PATENT APPLICATION

Customer Number: 25944

NONPROVISIONAL APPLICATION TRANSMITTAL
RULE §1.53(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the nonprovisional patent application

For (Title): ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

By (Inventor): Masao MURADE

☒ Formal drawings (Figs. 1-15; 13 sheets) are attached.
☐ Use Figure _____ for front page of Publication.

☒ A Declaration of the inventor is filed herewith.

☒ A Power of Attorney is filed herewith.
☐ The Power of Attorney is a General Power of Attorney.
A Transmittal of Power of Attorney and Statement Under 37 C.F.R. §3.73(b) is attached, and
A copy of the Assignment ☐ is attached to the Transmittal or ☐ was recorded at Reel _____ Frame _____.
☐ The Power of Attorney is a Specific Power of Attorney for this application (must be filed with or after an Assignment if assigned). A Transmittal of Power of Attorney and Statement Under 37 C.F.R. §3.73(b) is attached.
☒ The Power of Attorney is in a combined Declaration/Power of Attorney.
☒ The Power of Attorney identifies no more than ten attorneys.
☐ The Power of Attorney identifies more than ten attorneys, and a separate Designation of Ten Attorneys for Power of Attorney is filed herewith.

☐ This application claims benefit of Provisional Application No. _____ filed _____.
(A Preliminary Amendment is attached to reflect this claim in the Specification if not already present.)

☐ This patent application is assigned to _____.
☐ The executed Assignment is filed herewith.

☒ An Information Disclosure Statement is filed herewith.

☐ Entitlement to small entity status is hereby asserted.

☒ A Preliminary Amendment is filed herewith.

☒ Priority of foreign application No. 2004-328982 filed November 12, 2004 in Japan is claimed (35 U.S.C. §119).
☐ A certified copy of the above corresponding foreign application(s) is filed herewith.

☐ This application is NOT to be published under 35 U.S.C. 122(b). The undersigned attorney or agent hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing.

☒ The fees due upon filing are calculated below:

CLAIMS IN THE APPLICATION AFTER ENTRY OF
ANY PRELIMINARY AMENDMENT NOTED BELOW

FOR:	NO. FILED	NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
BASIC FEE				$ 150	OR		$ 300
EXAMINATION FEE				$ 100	OR		$ 200
SEARCH FEE				$ 250	OR		$ 500
TOTAL PAGES OF APPLICATION OVER 100 (54 - 100)	0 ÷ 50	= †0	x 125 =	$		x 250 =	$0
TOTAL CLAIMS	9 - 20	= *0	x 25 =	$	OR	x 50 =	$0
INDEP CLAIMS	2 - 3	= *0	x 100 =	$	OR	x 200 =	$0
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+ 180 =	$	OR	+ 360 =	$0
			TOTAL	$	OR	TOTAL	$1000

*If the difference is less than zero, enter "0".
†round up to next integer

☒ Check No. 170682 in the amount of $1000 to cover the fees due upon filing is attached. Except as otherwise noted herein, the Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/yxm

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

BACKGROUND

This application claims the benefit of Japanese Patent Application No. 2004-328982 filed November 12, 2004. The entire disclosure of the prior application is hereby incorporated by reference herein its entirety.

1. Technical Field

[0001]The present invention relates to an electro-optical device, such as a liquid crystal device or the like, and to an electronic apparatus, such as a liquid crystal projector or the like, having such an electro-optical device.

2. Related Art

[0002]In such an electro-optical device, a substrate, on which display electrodes and a circuit unit for driving the display electrodes are provided, and a counter substrate are disposed to face each other with an electro-optical material, such as liquid crystal, interposed therebetween. More specifically, the substrates are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of the substrates are bonded to each other by a sealant so as to form an internal space, and the electro-optical material is sealed in the internal space.

[0003]The substrate provided with the display electrodes extends from the counter substrate on one side in plan view, and external connecting

terminals are provided in a portion extending on one side (hereinafter, referred to as an extending portion). The external connecting terminals are connected to wiring lines led from a circuit unit and the like, and are provided such that surfaces thereof are exposed to the outside so as to be supplied with signals or power from the outside. In addition, a driving circuit, which is connected to the external connecting terminals for supplying image signals, is generally provided in the extending portion.

[0004]In contrast, for example, as disclosed in JP-A-9-113906, according to a configuration in which a driving circuit is disposed in the internal space and only external connecting terminals are provided in the extending portion, the width of the extending portion can be made narrow, and thus the size of the substrate can be reduced.

[0005]However, in an actual electro-optical device, it is difficult to provide a space sufficient to dispose the driving circuit and to lead the wiring lines from the driving circuit in the internal space. Further, even when only the external connecting terminals are provided in the extending portion, at least some of the lead wiring lines connected to the external connecting terminals is substantially disposed in the extending portion. For this reason, in order to reduce the width of the extending portion, the layout of the external connecting terminals and the lead wiring lines needs to be considered.

SUMMARY

[0006]An advantage of some aspects of the invention is that it provides an electro-optical device which can reduce the size of a substrate and an electronic apparatus having such an electro-optical device.

[0007]According to a first aspect of the invention, an electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit or the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

[0008]In accordance with the first aspect of the invention, the pair of substrates are disposed to face each other with a predetermined gap therebetween and one substrate extends from the other substrate on at least one side. On one substrate extending from the other substrate of the pair of substrates, for example, wiring lines, such as scanning lines, data lines, and the like, electronic elements, such as thin film transistors (hereinafter, referred to as a "TFTs") and the like, and the circuit unit that drives display electrodes by means of a data line

driving circuit or a scanning line driving circuit are provided. The display electrodes are formed on an upper layer of one substrate.

[0009] Further, in the extending portion extending the other substrate on the one side, the external connecting terminals, which are electrically connected to the circuit unit, are provided. A plurality of external connecting terminals are arranged, for example, along an outer edge of the extending portion, and are correspondingly connected to the lead wiring lines, which are led from the circuit unit or the display electrodes. The lead wiring lines are generally relayed in a region other than a region where the external connecting terminals are arranged.

[0010] In the extending portion of the first aspect of the invention, the external connecting terminals and the lead wiring lines are arranged to at least partially overlap each other in plan view (that is, in a three-dimensional manner in the extending portion). Such a configuration is implemented by electrically connecting at least some of the lead wiring lines and the external connecting terminals to each other via contact holes or the like, for example, and by laminating them with an interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0011] As such, with the design of the layout, the width of the extending portion in the extension direction thereof can be reduced. As a result, with the reduced size of the substrate, the space of the electro-optical

device can be saved. In particular, the number of electro-optical devices which can be manufactured per one wafer can be increased, such that considerable effects for reduction of manufacturing costs and enhancement of manufacturing efficiency are shown. For example, even when the reduced size for one substrate is relatively small, for example, 1 mm or so, if several substrates to several tens or hundreds of substrates are arranged on the same wafer, there is a case in which one row or a plurality of rows of electro-optical devices can be further manufactured on the same wafer. Therefore, it is markedly advantageous in practice.

[0012]In the electro-optical device of the first aspect of the invention, it is preferable that the external connecting terminals and the lead wiring lines be laminated with an interlayer insulating film interposed therebetween, the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and the lead wiring lines have the same film as a second conductive film constituting the circuit unit.

[0013]According to this configuration, the external connecting terminals and the lead wiring lines are formed with different conductive films laminated with an interlayer insulating film interposed therebetween. Therefore, the external connecting terminals and the lead wiring lines can be constituted so as to overlap in plan view but not to be electrically connected to each other in portions other than portions where connected each other via contact holes or the like.

[0014]Further, the external connecting terminals and the lead wiring

lines are formed as the same film as a conductive film constituting the circuit unit or to include the same film as such a conductive film, such that the laminate structure of the external connecting terminals and the lead wiring lines does not need to be prepared separately from the circuit unit. Therefore, the structure on the substrate can be simplified and be relatively easily formed. Moreover, as a material of the conductive film, for example, aluminum (Al) having low resistance is suitably used.

[0015]Further, in the electro-optical device of the first aspect of the invention, it is preferable that the plurality of external connecting terminals be arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and be connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

[0016]According to this configuration, the plurality of lead wiring lines extend in the direction in which the plurality of external connecting terminals are arranged, such that the external connecting terminals and the lead wiring lines intersect each other in a three-dimensional manner. The external connecting terminals and the lead wiring lines are connected, for example, via contact holes at the edges of the external connecting terminals (that is, the edges of the external connecting terminals on an outer edge side and an inner edge side) in the direction intersecting the direction along the one side. According to such a layout, the lead wiring lines can be efficiently arranged in a region where the external connecting terminals are formed. Further,

since the lead wiring lines are connected to the external connecting terminals in a region distant from the region where the lead wiring lines extend, such that the external connecting terminals and other lead wiring lines adjacent to the lead wiring lines to be originally connected to the external connecting terminals can be prevented from being electrically connected to each other due to an error in formation location of the contact hole, for example. Therefore, the liquid crystal device according to the above-described configuration can be manufactured with high reliability.

[0017]Further, in the electro-optical device of the first aspect of the invention, it is preferable that the plurality of external connecting terminals be arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and be correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

[0018]According to this configuration, the external connecting terminals and the lead wiring lines are correspondingly connected to each other via contact holes, for example, in the region where they intersect each other in plan view. With such a layout, the lead wiring lines can be efficiently arranged in the region where the external connecting terminals are formed, and the lead wiring lines are correspondingly connected to the external connecting terminals in the region where the lead wiring lines extend. Therefore, the regions for forming the contact holes do not need to be separately prepared, and thus the

arrangement space of the lead wiring lines and the external connecting terminals can be made small. As a result, according to the above-described configuration, the width in the direction in which the extending portion extends can be further reduced, and thus the size of the substrate can be further reduced.

[0019]Further, according to a second aspect of the invention, an electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

[0020]In accordance with the second aspect of the invention, in the extending portion, the circuit unit and the external connecting terminals are disposed to at least partially overlap each other in plan view. Such a configuration can be implemented by laminating the circuit unit and at least some of the external connecting terminals with an interlayer insulating film interposed therebetween. In this case, two

or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0021]As such, with the design of the layout, the width of the extending portion in the extending direction thereof can be reduced. As a result, with the reduced size of the substrate, the same effects as those in the electro-optical device according to the first aspect of the invention can be obtained.

[0022]In the electro-optical device of the second aspect of the invention, it is preferable that the circuit unit be electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and have a driving circuit, which is driven by the supplied image signal, and at least a part of the driving circuit overlap the external connecting terminals in plan view.

[0023]According to this configuration, the driving circuit, that is, a so-called data line driving circuit is disposed to at least partially overlap the external connecting terminals in plan view. In general, the data line driving circuit is provided to extend along the one side and is connected to the external connecting terminals via the lead wiring lines, such that image signals can be supplied to both ends thereof. For this reason, since a region sufficient to arrange the plurality of lead wiring lines around the data line driving circuit is required, there are many cases in which the data line driving circuit is provided in the extending portion having little spatial restriction, together with the external connecting terminals. In this case, the external

connecting terminals and the data line driving circuit are generally provided on the same plane, so that the width of the extending portion becomes large according to the size, the shape, and the like of the data line driving circuit.

[0024] In contrast, in the invention, since the entire data line driving circuit provided in the extending portion or at least a part thereof, and the external connecting terminals are provided in the same space, the width of the extending portion can be reduced, and thus the space of the electro-optical device can be effectively saved or the size of the electro-optical device can be effectively reduced.

[0025] Further, in the electro-optical device of the second aspect of the invention, it is preferable that the external connecting terminals and the part of the circuit unit be laminated with an interlayer insulating film interposed therebetween, and the external connecting terminals have the same film as a first conductive film constituting the circuit unit.

[0026] According to this configuration, since the external connecting terminals and the circuit unit are laminated with the interlayer insulating film interposed therebetween, the external connecting terminals and the circuit unit can overlap in plan view but can not be electrically connected to each other. In addition, the external connecting terminals are formed as the same film as the conductive film constituting the circuit unit or to include the same film as the conductive film, so that the structure on the substrate can be simplified and relatively easily formed. Moreover, as a material of the conductive film, for example, aluminum (Al) having low resistance is

suitably used.

[0027]The electro-optical device of the first aspect of the invention may further include a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates, and an electro-optical material that is held in the internal space. In addition, it is preferable that the display electrodes and the part of the circuit unit be disposed to face the internal space.

[0028]According to this configuration, the edges of the opposite surfaces of the pair of substrates are bonded to each other by the sealant so as to form the internal space therebetween, and the extending portion extends from the edges. The electro-optical material, such as liquid crystal, is sealed into the internal space. The display electrodes are disposed to face the internal space. Further, a part of the circuit unit, for example, wiring lines or elements, such as scanning lines, data lines, TFTs, and the like, and a driving circuit, such as a scanning line driving circuit or the like, is provided in the region facing the internal space, together with the display electrodes. Therefore, almost the entire area of the extending portion can be used for forming the external connecting terminals.

[0029]According to a third aspect of the invention, an electronic apparatus includes the above-described electro-optical device (including various configurations).

[0030]According to this configuration, since the electronic apparatus includes the above-described electro-optical device, various electronic

apparatuses, such as a projection type display device, a liquid crystal television, a cellular phone, an electronic organizer, a word processor, a viewfinder-type or monitor-direct-view-type video tape recorder, a workstation, a video phone, a POS terminal, a touch panel, and the like, which are saved in space and reduced in size, can be implemented. In addition, for example, an electrophoretic device, such as an electronic paper, can be implemented as the electronic apparatus according to the third aspect of the invention.

[0031]Such effects and other advantages of the invention will be apparent from the following embodiments to be described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]The invention will be described with reference to the accompanying drawings, wherein like numbers reference like elements.

[0033]Fig. 1 is a plan view showing a configuration of a liquid crystal device according to a first embodiment of the invention.

[0034]Fig. 2 is a cross-sectional view showing the liquid crystal device taken along the line II-II of Fig. 1.

[0035]Fig. 3 is a plan view showing a comparative example of the liquid crystal device according to the first embodiment.

[0036]Fig. 4 is a plan view showing a configuration of main parts of the liquid crystal device according to the first embodiment.

[0037]Fig. 5 is a cross-sectional view showing an extending portion taken along the line V-V of Fig. 4.

[0038]Fig. 6 is a schematic view showing an equivalent circuit in an image display region of the liquid crystal device according to the first embodiment.

[0039]Fig. 7 is a plan view showing a configuration of the image display region of the liquid crystal device according to the first embodiment.

[0040]Fig. 8A is a cross-sectional view showing the configuration of the image display region of the liquid crystal device according to the first embodiment taken along the line VIIIA-VIIIA of Fig. 7.

[0041]Fig. 8B is a cross-sectional view showing the configuration of the image display region of the liquid crystal device according to the first embodiment taken along the line VIIIB-VIIIB of Fig. 7.

[0042]Fig. 9 is a plan view showing a modification of the liquid crystal device according to the first embodiment.

[0043]Fig. 10 is a cross-sectional view showing the extending portion taken along the line X-X of Fig. 9.

[0044]Fig. 11 is a plan view showing a configuration of a liquid crystal device according to a second embodiment.

[0045]Fig. 12 is a plan view showing a configuration of main parts of the liquid crystal device according to the second embodiment.

[0046]Fig. 13 is a cross-sectional view showing an extending portion taken along the line XIII-XIII of Fig. 12.

[0047]Fig. 14 is a plan view showing a modification of the liquid crystal device according to the second embodiment.

[0048]Fig. 15 is a cross-sectional view showing a configuration of a liquid crystal projector according to an embodiment of an electronic

apparatus of the invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0049]Hereinafter, embodiments of the invention will be described with reference to the drawings.

Embodiments of Electro-Optical Device

[0050]The embodiments of the invention will be described with reference to Figs. 1 to 13. In the embodiments to be described below, the electro-optical device of the invention is applied to a liquid crystal device.

First Embodiment

[0051]A liquid crystal device according to a first embodiment of the invention will be described with reference to Figs. 1 to 7.

Schematic Configuration of Liquid Crystal Device

[0052]First, the schematic configuration of a liquid crystal device will be described with reference to Figs. 1 to 3. Fig. 1 is a plan view showing the configuration of a liquid crystal device according to the present embodiment, and Fig. 2 is a cross-sectional view taken along the line II-II of Fig. 1. Fig. 3 shows a comparative example of the liquid crystal device according to the present embodiment.

[0053]Referring to Figs. 1 and 2, in the liquid crystal device 100, a

TFT array substrate 10 and a counter substrate 20 are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of both substrates are bonded to each other by a sealant 52a so as to form an internal space. The TFT array substrate 10 has an extending portion 201 which extends from the counter substrate 20 on one side in plan view, and the sealant 52a defines openings which lead to the internal space at predetermined places of a side where the extending portion 201 extends (here, both ends of the side). Further, a liquid crystal layer 50 is formed by injecting liquid crystal into the internal space through the openings, and the openings are sealed with sealing mold materials 151a and 151b. A frame light-shielding film 53, which is provided along an inner edge of the sealant 52a, defines an image display region 10a on which images are displayed.

[0054]On the image display region 10a of a surface (top surface in Fig. 2) of the TFT array substrate 10 facing the counter substrate 20, pixel electrodes 9a, which are examples of 'display electrodes' of the invention, are provided on switching TFTs or wiring lines, such as scanning lines, data lines, and the like. In addition, an alignment film is formed just above the pixel electrodes 9a. On a surface (bottom surface in Fig. 2) of the counter substrate 20 facing the TFT array substrate 10, a counter electrode 21 is formed via a stripe-shaped light-shielding film 23, and an alignment film is formed on the counter electrode 21. Further, in at least one corner portion (here, all of four corner portions) of the counter substrate 20, vertical connecting terminals 106 for electrically connecting the counter substrate 20 and

the TFT array substrate 10 are provided. The alignment state of liquid crystal of the liquid crystal layer 50 changes according to the electric field applied between the pixel electrodes 9a and the counter electrode 21, but liquid crystal of the liquid crystal layer 50 maintains an initial alignment state defined by the alignment films when the electric field is not applied.

[0055]In a region of the surface of the TFT array substrate 10 facing the counter substrate 20 which corresponds to a region where the frame light-shielding film 53 is formed, scanning line driving circuits 104 for driving scanning lines, and wiring lines 105 are provided. In Fig. 1, two scanning line driving circuits 104 are provided on left and right sides the frame light-shielding film 53. The wiring lines 105 are relayed on the upper side of the frame light-shielding film 53 so as to connect the two scanning line driving circuits 104.

[0056]The extending portion 201 of the TFT array substrate 10 is provided with a data line driving circuit 101a for driving data lines, which is a specified example of 'driving circuit' of the invention, along a lower side of the sealant 52a in Fig. 1. The upper half of the data line driving circuit 101a overlaps the sealant 52a in plan view. Further, the lower half of the data line driving circuit 101a overlaps portions pushed from the openings of the sealing mold materials 151a and 151b at both ends thereof.

[0057]Moreover, in the present embodiment, all of electronic elements, such as TFTs or the like, the wiring lines, such as scanning lines, data lines, and the like, and circuits on the TFT array substrate 10

including the scanning line driving circuits 104 and the data line driving circuit 101a correspond to a specified example of 'circuit unit' of the invention. Further, the extending portion 201 may be further provided with a sampling circuit that applies image signals to a plurality of data lines with a predetermined timing, a precharge circuit that supplies a precharge signal having a predetermined voltage level to the plurality of data lines prior to the image signals, and a test circuit that tests quality, defects, or the like of the liquid crystal device 100 during manufacture or at the time of shipping.

[0058]Further, in the present embodiment, at least some of a plurality of lead wiring lines 103a in the extending portion 201 is provided to overlap external connecting terminals 102a in plan view. Specifically, in the liquid crystal device 100, a layer where the external connecting terminals 102a are formed and a layer where the lead wiring lines 103a are formed are laminated with, for example, an interlayer insulating film interposed therebetween, and the formation region of the external connecting terminals 102a and the formation region of the lead wiring lines 103a at least partially overlap each other. Two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0059]The external connecting terminals 102a are provided so as to supply power or signals to the liquid crystal device 100 from an external circuit, which is connected thereto via an FPC 110. The external connecting terminals 102a are properly connected to the driving

circuit, such as the scanning circuit driving circuits 104 or the data line driving circuit 101a, via the lead wiring lines 103a. In the liquid crystal device 100, the pixel electrodes 9a are driven by signals inputted to the external connecting terminals 102a from the outside, such that images are displayed. Here, the data line driving circuit 101a is connected to the plurality of external connecting terminals 102a through the lead wiring lines 103a at both ends of the extending portion 201.

[0060]As shown in Fig. 3, in a liquid crystal device according to a comparative example of the present embodiment, external connecting terminals 102 and lead wiring lines 103 are disposed on the same plane so as not to overlap each other in plan view. In addition, the external connecting terminals 102 must be connected to the FPC 110, and thus a sealant 150 does not overlap the external connecting terminals 102. Accordingly, the external connecting terminals 102a need to be disposed away from the sealant 150 to some extent. As a result, an extending portion 200 has a predetermined width L0 and has a space, such that a space for disposing the entire data line driving circuit 101 is generated.

[0061]In contrast, in the liquid crystal device 100 of the present embodiment, as described above, at least some of the plurality of lead wiring lines 103a are disposed to overlap the external connecting terminals 102a in plan view, so that a space can be saved. In particular, since the external connecting terminals 102a are arranged along an outer edge of the extending portion 201, the width L11 of the

extending portion 201 in the extending direction can be reduced further than the related art.

[0062]Further, in the liquid crystal device 100 of the present embodiment, since the external connecting terminals 102a are arranged in a region between the sealing mold materials 151a and 151b, the external connecting terminals 102a do not need to be provided distant from and the sealing mold materials 151a and 151b. In addition, in Fig. 1, the positions of the external connecting terminals 102a can be moved upward by disposing the upper half of the data line driving circuit 101a in a region where the sealant 52a is provided. As a result, the width L11 of the extending portion 201 can be further reduced than the width L0 of the extending portion 200 in the comparative example.

[0063]As such, the space can be saved in the liquid crystal device 100 of the present embodiment, and thus an electronic apparatus, to which the liquid crystal device 100 is applied, can have a high degree of freedom in terms of design. Further, the number of liquid crystal devices which can be manufactured per one wafer can be increased, and considerable effects for reduction of manufacturing costs and enhancement of manufacturing efficiency are shown. That is, even though the reduced width of the extending portion 201 in one liquid crystal device 100 is small, several hundreds or thousands of regions, each corresponding to the TFT array substrate 10, are generally formed on the wafer and a large number of such wafers are manufactured. Therefore, it is very effective for manufacture.

[0064]Here, on the lower side of the sealant 52a or the lower side of

the counter substrate 20, the openings and the sealing mold materials 150a and 150b are disposed at the ends thereof and the external connecting terminals 102a are arranged at a central portion thereof. Therefore, even when the lead wiring lines 103a are divided into the left and right sides, the lengths of the lead wiring lines 103a can be approximately equal one left and right sides, such that a failure, such as a signal delay between the left and right sides, does not occur. Further, the openings are disposed at the left and right ends, so that liquid crystal can be injected into the internal space efficiently and uniformly.

Configuration of Extending Portion

[0065]Next, referring to Figs. 4 to 7, a specified configuration of the extending portion 201 in the liquid crystal device 100 will be described in detail. Fig. 4 shows main parts of the extending portion in the liquid crystal device according to the present embodiment on a magnified scale. Fig. 5 is a cross-sectional view taken along the line V-V of Fig. 4. Fig. 6 shows an equivalent circuit constituted by a pixel unit in an image display region of the liquid crystal device according to the present embodiment. Fig. 7 is a plan view showing the configuration of the pixel unit. Figs. 8A and 8B are cross-sectional views showing the configuration of the pixel unit. Specifically, Fig. 8A is a cross-sectional view taken along the line VIIIA-VIIIA of Fig. 7, and Fig. 8B is a cross-sectional view taken along the line VIIIB-VIIIB of Fig. 7. In Figs. 8A and 8B, the scale of each layer or each member has been

adjusted in order to have a recognizable size.

[0066]In Fig. 4, the plurality of external connecting terminals 102a are arranged in one direction, and the plurality of lead wiring lines 103a extend in the direction in which the external connecting terminals 102a are arranged and are connected to the external connecting terminals 102a via contact holes 20a. The plurality of contact holes 20a are provided at the outer edges of the plurality of external connecting terminals 102a. Alternatively, all or some of the contact holes 20a may be provided at the inner edges of the plurality of external connecting terminals 102a.

[0067]According to such a layout, the lead wiring lines 103a are connected to the external connecting terminals 102a in a region distant from a region where the lead wiring lines 103a extend, so that the external connecting terminals 102a and other lead wiring lines 103a adjacent to the lead wiring lines 103a to be originally connected to the external connecting terminals 102a can be prevented from being electrically connected to each other due to an error in formation location of the contact hole 20a, for example. Therefore, the liquid crystal device 100 can be manufactured with high reliability.

[0068]In Fig. 5, the external connecting terminals 102a and the lead wiring lines 103 are laminated with an interlayer insulating film 43 interposed therebetween. Further, the contact holes 20a are formed to pass through the interlayer insulating film 43. Each of the lead wiring lines 103a is connected to a desired external connecting terminal 102a via the contact hole 20a but is electrically isolated from other

external connecting terminals 102a by means of the interlayer insulating film 43, so that the lead wiring lines 103a overlap the external connecting terminals 102a in plan view.

[0069] Here, a base insulating film 12 and interlayer insulating films 41, 42, 43, and 44 are laminated on the TFT array substrate 10 in that order, and the lead wiring lines 103a are provided on the interlayer insulating film 43. Here, the lead wiring line 103a and the external connecting terminal 102a each has a two-layered structure made of an aluminum layer 40A, a titanium nitride film 40TN, and an exposed surface D of each of the external connecting terminals 102a (a hatched region of each of the external connecting terminals 102a in Fig. 4) is exposed to the outside from an opening which is formed by partially removing the interlayer insulating film 44 and the titanium nitride film 40TN. A laminated structure in the image display region 10a on the TFT array substrate 10 is constituted based on the above-described laminated structure. Next, the configuration of the laminated structure in the image display region 10a will be described below.

Configuration of Image Display Region

[0070] In Fig. 6, a plurality of scanning lines 11a and a plurality of data lines 6a are arranged to intersect each other in the image display region 10a, and pixel units, each being selected by one of the plurality of scanning lines 11a and one of the plurality of data lines 6a, are formed between these lines. Each of the pixel units has a TFT 30, a pixel electrode 9a, and a storage capacitor 70. The TFT 30 is provided

to apply image signals S1, S2, …, and Sn supplied from the data lines 6a to the selected pixels. A gate of the TFT 30 is connected to the scanning line 11a, a source thereof is connected to the data line 6a, and a drain thereof is connected to the pixel electrode 9a. A liquid crystal capacitor is formed between the pixel electrode 9a and a counter electrode 21 to be described below, and the respective pixel electrodes 9a hold the input image signals S1, S2, …, and Sn for a predetermined period of time. That is, an opening region for each pixel unit is divided by each of the pixel electrodes 9a. One electrode of the storage capacitor 70 is connected to the drain of the TFT 30 in parallel with the pixel electrode 9a, and the other electrode thereof is connected to a fixed-potential capacitor wiring line 400, such that the electric potential on the other electrode can be made constant.

[0071]The liquid crystal device 100 uses a TFT active matrix driving method, for example. Specifically, in the liquid crystal device 100, scanning signals G1, G2, …, Gm are line-sequentially applied to the respective scanning lines 11a from the scanning line driving circuit 104 (see Fig. 1), and simultaneously the image signals S1, S2, …, and Sn supplied from the data line driving circuit 101 (see Fig. 1) are applied through the data lines 6a to a selected row of horizontally-arrayed pixel units in which the TFTs 30 are turned on. As a result, the image signals are supplied to the pixel electrodes 9a corresponding to the selected pixels. Since the TFT array substrate 10 is disposed to face the counter substrate 20 with the liquid crystal layer 50 interposed therebetween (see Fig. 2), the amount of transmitted light between the

substrates is controlled for each pixel by applying an electric field to the liquid crystal layer 50 for each pixel unit in such a manner, such that gray-scale display of an image is performed. At this time, the image signal held in each pixel unit is prevented from leaking by means of the storage capacitor 70.

[0072]In Figs. 7 and 8, circuit elements of the above-described pixel unit are patterned to be formed on the TFT array substrate 10 as laminated conductive films. The TFT array substrate 10 of the present embodiment is made of a quartz substrate and is disposed to face the counter substrate 20 made of a glass substrate, a quartz substrate, or the like. Further, each of the circuit elements has a first layer including the scanning line 11a, a second layer including the gate electrode 3a, a third layer including the fixed-potential capacitor electrode of the storage capacitor 70, a fourth layer including the data line 6a, a fifth layer including the capacitor wiring line 400, and a sixth layer including the pixel electrode 9a from the bottom. In addition, the base insulating film 12 is provided between the first and second layers, the first interlayer insulating film 41 is provided between the second and third layers, the second interlayer insulating film 42 is provided between the third and fourth layers, the third interlayer insulating film 43 is provided between the fourth and fifth layers, and the fourth interlayer insulating film 44 is provided between the fifth and sixth layers, such that the above-described elements can be prevented from being short-circuited.

Configuration of First Layer - Scanning Line and the like

[0073]The first layer has the scanning lines 11a. Each of the scanning lines 11a is patterned to have a main line part extending in an X direction of Fig. 7 and a protruding part extending in a Y direction of Fig. 7 in which the data lines 6a or the capacitor wiring lines 400 extend. The scanning line 11a is made of, for example, conductive polysilicon. Alternatively, the scanning line 11a may be made of a metal simplex of at least one high-melting-point metal selected from a group of titanium (Ti), chromium (Cr), tungsten (W), tantalum (Ta), molybdenum (Mo), and the like, an alloy thereof, metal silicide, polysilicide, or a laminate thereof. That is, the scanning line 11a of the present embodiment covers a region between the openings as much as possible, thereby serving as a light-shielding film which shields the TFT 30 from the lower side.

Configuration of Second Layer - TFT and the like

[0074]The second layer has the TFTs 30 and relay electrodes 719. Each of the TFTs 30 has an LDD (Lightly Doped Drain) structure, for example, and includes a gate electrode 3a, a semiconductor layer 1a, and a gate insulating film 2 for electrically isolating the gate electrode 3a from the semiconductor layer 1a. The gate insulating film 2 is made of, for example, an HTO (High Temperature Oxide) or a thermally-oxidized silicon oxide. The gate electrode 3a is made of, for example, conductive polysilicon. The semiconductor layer 1a is made of, for example, polysilicon, and has a lightly-doped source region 1b, a lightly-doped

drain region 1c, a heavily-doped source region 1d, and a heavily-doped drain region 1e. In addition, on the second layer, the relay electrodes 719 are formed as the same film as that of the gate electrode 3a.

[0075] The gate electrode 3a of the TFT 30 is electrically connected to the scanning line 11a via a contact hole 12cv formed in the base insulating film 12. The base insulating film 12 is made of a silicon oxide film, such as an HTO film or an NSG (non-silicate glass) film, electrically isolates the first layer from the second layer, and is formed on the entire surface of the TFT array substrate 10 so as to prevent element characteristics of the TFT 30 from changing due to roughness or contamination caused by the abrasion of a substrate surface.

Configuration of Third Layer - Storage Capacitor and the like

[0076] The third layer has the storage capacitors 70. Each of the storage capacitors 70 is configured such that a capacitor electrode 300 and a lower electrode 71 are disposed to face each other with a dielectric film 75 interposed therebetween. The capacitor electrode 300 is electrically connected to the capacitor wiring line 400 via contact holes 801 and 803 and a relay layer 6a1 for a capacitor wiring line. The lower electrode 71 and the heavily-doped drain region 1e are connected via a contact hole 83 formed in the first interlayer insulating film 41. Further, the lower electrode 71 and the pixel electrode 9a relay the respective layers by means of contact holes 881, 882, and 804, the relay electrode 719, a second relay electrode 6a2, and

a third relay electrode 402, and are electrically connected via a contact hole 89.

[0077]The capacitor electrode 300 has a single layer made of a metal simplex of at least one high-melting-point metal selected from a group of Ti, Cr, W, Ta, Mo, and the like, an alloy thereof, metal silicide, polysilicide, or a laminate. Preferably, the capacitor electrode 300 is made of tungsten silicide, and has a function of blocking light incident on the TFT 30 from the top in Fig. 8. The lower electrode 71 is made of conductive polysilicon, for example. The dielectric film 75 is made of, for example, a silicon oxide film, such as an HTO film or an LTO (Low Temperature Oxide) film, or a silicon nitride film, to have a relatively small thickness of approximately 5 to 200 nm.

[0078]Further, the first interlayer insulating film 41 is made of, for example, NSG. Alternatively, the first interlayer insulating film 41 may be made of silicate glass, such as PSG (phosphorus silicate glass), BSG (boron silicate glass), BPSG (boron phosphorus silicate glass), a silicon nitride, a silicon oxide, or the like.

Configuration of Fourth Layer - Data Line and the like

[0079]The fourth layer has the data lines 6a, the relay layer 6a1 for a capacitor wiring line, and the second relay electrode 6a2. Each of the data lines 6a has a two-layered structure of an aluminum film and a titanium nitride film, and the surface thereof is covered with a silicon nitride film. The data line 6a is electrically connected to the heavily-doped source region 1d of the TFT 30 via a contact hole 81

passing through the first and second interlayer insulating films 41 and 42. In addition, on the fourth layer, the relay layer 6a1 for a capacitor wiring line and the second relay electrode 6a2 are formed as the same film as that of the data line 6a.

[0080]Further, the second interlayer insulating film 42 is made of, for example, NSG. Alternatively, the second interlayer insulating film 42 may be made of silicate glass, such as PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like.

Configuration of Fifth Layer - Capacitor Wiring Line and the like

[0081]The fifth layer has the capacitor wiring lines 400 and the third relay electrode 402. Each of the capacitor wiring lines 400 extends to reach the periphery of the image display region 10a, and is electrically connected to a constant voltage source, from which power is supplied to a peripheral driving circuit or a counter electrode potential is supplied to a counter substrate via the vertical connecting terminal, such that the capacitor wiring line 400 has a constant potential. Further, the capacitor wiring line 400 is electrically connected to the relay layer 6a1 for a capacitor wiring line via the contact hole 803 formed in the third interlayer insulating film 43. The capacitor wiring line 400 has a two-layered structure of, for example, an aluminum film and a titanium nitride film.

[0082]The capacitor wiring line 400 has a lattice pattern extending in the X and Y directions, as shown in Fig. 7. A part of the capacitor wiring line 400 extending in the X direction is provided with a notch

portion in order to ensure a region for forming the third relay electrode 402. Further, the capacitor wiring line 400 has a width larger than those of the lower data line 6a, the scanning line 11a, and the TFT 30, such that the capacitor wiring line 400 can function as a light-shielding film and cover those circuit elements, thereby finally defining a non-opening region. In addition, on the fifth layer, the third relay electrode 402 is formed as the same film as that of the data line 6a.

[0083]Below the fifth layer, the third interlayer insulating film 43 is formed over the entire surface thereof. The third interlayer insulating film 43 is made of, for example, silicate glass, such as NSG, PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like. Further, the surface of the third interlayer insulating film 43 may be planarized by a CMP (Chemical Mechanical Polishing) treatment or a planarizing film formed by an SOG (Spin On Glass) treatment. With the planarization, cracks caused by a step difference between wiring lines can be prevented.

Configuration of Sixth Layer - Pixel Electrode and the like

[0084]The fourth interlayer insulating film 44 is formed on the entire surface of the fifth layer, and the pixel electrodes 9a are formed thereon as the sixth layer. In the fourth interlayer insulating film 44, a contact hole 89 is formed to electrically connect the pixel electrode 9a and the third relay electrode 402. The fourth interlayer insulating film 43 is made of, for example, silicate glass, such as NSG,

PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like. Further, the surface of the fourth interlayer insulating film 44 may be planarized by the CMP treatment or a planarizing film formed by the SOG treatment. With the planarization, cracks caused by a step difference between wiring lines can be prevented.

[0085]Each of the pixel electrodes 9a (indicated by a dotted line 9a' in Fig. 7) is disposed to approximately correspond to each of the pixel regions partitioned vertically and horizontally. The pixel electrode 9a is made of, for example, a transparent conductive film, such as ITO (Indium Tin Oxide). Further, an alignment film 16 is formed on the pixel electrode 9a. Until now, the configuration of the pixel unit on the TFT array substrate 10 has been described.

[0086]Further, with respect to the counter substrate 20, the counter electrode 21 is provided on the entire surface thereof facing the TFT array substrate 10, and an alignment film 22 is formed thereon (below the counter electrode 21 in Fig. 8). The counter electrode 21 is made of, for example, a transparent conductive film, such as ITO, in the same manner as the pixel electrode 9a. Between the counter substrate 20 and the counter electrode 21, a light-shielding film 23 for covering at least a region facing the TFT 30 is provided to prevent optical leakage current from being generated.

[0087]In the present embodiment, the extending portion 201 is formed on the extension of such a laminated structure constituting the image display region 10a. That is, in the extending portion 201, the lead wiring lines 103a are formed in the fourth layer as the same film as

that of the data line 6a, and the external connecting terminals 102a are formed in the fifth layer as the same film as that of the capacitor wiring line 400. For this reason, a laminated structure shown in Fig. 5, in which the lead wiring lines 103a and the external connecting terminals 102a are laminated with the interlayer insulating film interposed therebetween, does not need to be provided separately from the laminated structure constituting the image display region 10a. Therefore, the structure on the TFT array substrate 10 can be simplified and relatively easily formed.

[0088] In addition, in the present embodiment, since both the fourth and fifth layers contain aluminum, the data lines 6a and the capacitor wiring lines 400 have low resistance, and the lead wiring lines 103a and the external connecting terminals 102a have low resistance. Since the fourth and fifth layers are disposed above the storage capacitor 70 or the TFT 30, which requires a heat treatment, aluminum having low thermal resistance can be used. Here, by providing the lead wiring lines 103a and the external connecting terminals 102a in the fourth and fifth layers of the laminated structure constituting the image display region 10a, the wiring lines can have low resistance and the exposed surface D of each of the external connecting terminals 102a can be easily formed.

Modification

[0089] Next, a liquid crystal device according to a modification of the first embodiment will be described with reference to Figs. 9 and 10. Fig. 9 shows main parts of the extending portion in the liquid crystal

device according to the modification of the first embodiment on a magnified scale. Fig. 10 is a cross-sectional view taken along the line X-X of Fig. 9.

[0090]Preferably, the lead wiring lines and the external connecting terminals according to the invention are arranged to partially overlap each other in plan view, and various modifications can be made, in addition to the arrangement of the first embodiment.

[0091]Fig. 9 shows an example of such modifications. In Fig. 9, a plurality of external connecting terminals 102b are arranged in one direction and are connected to external connecting terminals 103b via contact holes 20b. Each of the contact holes 20b is provided in each of the regions where the plurality of lead wiring lines 103b and the plurality of external connecting terminals 102b intersect each other in plan view.

[0092]With such an arrangement, since the lead wiring lines 103a are connected to the external connecting terminals 102a in the regions where the lead wiring lines 103a extend, separate regions for forming contact holes do not need to be prepared, such that a space where the lead wiring lines and the external connecting terminals are arranged can be made smaller than that in the first embodiment (see Figs. 5 and 10). Therefore, in the modification, the width of the extending portion can be further reduced, so that the size of the TFT array substrate 10 can be further reduced.

Second Embodiment

[0093]Next, a liquid crystal device according to a second embodiment will be described with reference to Figs. 11 to 13. Fig. 11 shows the schematic configuration of the liquid crystal device according to the present embodiment, Fig. 12 shows main parts of an extending portion in the liquid crystal device according to the second embodiment on a magnified scale, and Fig. 13 is a cross-sectional view taken along the line XIII-XIII of Fig. 12. In addition, the liquid crystal device 100A has the same configuration as the liquid crystal device 100, except that the arrangement within the extending portion is different. Therefore, the same parts as those in the liquid crystal device 100 are denoted by the same reference numerals and the detailed descriptions thereof will be omitted.

[0094]In Fig. 11, in the liquid crystal device 100A, a data line driving circuit 101c and lead wiring lines 103c are disposed to overlap a plurality of external connecting terminals 102c, which are arranged along the outer edge of an extending portion 202, in plan view. With the design of the layout of the extending portion 202, the width L12 of the extending portion 202 can be made narrow to thereby reduce the size of the TFT array substrate 10, such that the same effects as those in the first embodiment can be obtained.

[0095]Figs. 12 and 13 show that mode on a magnified scale. The lead wiring lines 103c are connected to the external connecting terminals 102c via contact holes 20c provided in regions where the lead wiring lines 103c and the external connecting terminals 102c intersect each other, in the same manner as that in the modification of the first

embodiment. On the other hand, each of the lead wiring lines 103c is connected to the data line driving circuit 101c via the contact hole 21c provided in a region where each of the lead wiring lines 103c extends.

[0096] Here, in a structure laminated on the TFT array substrate 10, the lead wiring lines 103c are provided in the fourth layer, the external connecting terminals 102c are provided in the fifth layer, and the contact holes 20c are provided to pass through the interlayer insulating film 43. The data line driving circuit 101c is provided in at least one (second and fourth layers in the range shown in the drawing) of the first to fifth layers, and the contact holes 20c are provided to pass through the interlayer insulating films 41 and 42.

[0097] In the present embodiment, the external connecting terminals 102c and the lead wiring lines 103c are formed as the same film as the conductive film for the data line driving circuit 101c or a circuit unit in the image display region 10a or are formed as a part of the same film as the conductive film, so that the structure on the TFT array substrate 10 can be simplified and relatively easily formed. Other advantages and effects of the second embodiment are the same as those of the first embodiment, and the modification of the first embodiment can also be made in the present embodiment.

[0098] Further, though the external connecting terminals 102c and the lead wiring lines 103c overlap each other in plan view and the external connecting terminals 102c and the data line driving circuit 101c overlap each other in plan view in the second embodiment, the width of the extending portion can be reduced in a layout in which only the data line

driving circuit overlaps the external connecting terminals, as shown in Fig. 14, and thus the effects of the invention can be obtained.

Electronic Apparatus

[0099]Next, a case in which the above-described liquid crystal device is applied to an electronic apparatus will be described with reference to Fig. 15. Here, a projector which uses the liquid crystal device 100 as a light valve will be described as an example of the electronic apparatus according to the invention. Fig. 15 shows an example of a configuration of the projector.

[00100] In Fig. 15, a liquid crystal projector 1100 includes a lamp unit 1102 having a white light source, such as a halogen lamp. Projection light emitted from the lamp unit 1102 is separated into light components of three primary colors of R (red), G (green), and B (blue) by three mirrors 1106 and two dichroic mirrors 1108, and the light components of three primary colors are incident on liquid crystal devices 100R, 100G, and 100B, serving as light valves, corresponding to the respective colors of R, G, and B. The configurations of each of the liquid crystal devices 100R, 100G, and 100B is the same as that of the above-described liquid crystal device, and three primary color signals supplied from an image signal processing circuit are modulated by the liquid crystal devices 100R, 100G, and 100B, respectively. The light components of three primary colors modulated by the liquid crystal devices 100R, 100G, and 100B are incident on a dichroic prism 1112 from three directions. Then, images, each having one of the light components

for three primary colors, are synthesized, such that a color image is projected onto a screen 1120 through a projection lens 1114.

[00101] In addition, the electro-optical device according to the invention may be implemented as an organic EL device, an electrophoretic device, such as an electronic paper or the like, a display device using an electron emission element (Field Emission Display and Surface-Conduction Electron-Emitter Display), and the like, in addition to the above-described liquid crystal device.

[00102] Further, the electro-optical device according to the invention can be applied to various electronic apparatuses, such as a television receiver, a viewfinder-type or monitor-direct-view-type video tape recorder, a car navigation device, a pager, an electronic organizer, an electronic calculator, a word processor, a workstation, a video phone, a POS terminal, a device having a touch panel, and the like, in addition to the above-described projector.

[00103] It should be understood that the invention is not limited to the above-described embodiments and examples, but various modifications can be made within the scope without departing from the subject matter or spirit of the invention defined by the appended claims and the entire specification. Therefore, an electro-optical device and an electronic apparatus having such an electro-optical device that accompany such modifications still fall within the technical scope of the invention.

What is claimed is:

1. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

2. The electro-optical device according to Claim 1,

wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween,

the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and

the lead wiring lines have the same film as a second conductive

film constituting the circuit unit.

3. The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

4. The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

5. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

6. The electro-optical device according to Claim 5,

wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and

at least a part of the driving circuit overlaps the external connecting terminals in plan view.

7. The electro-optical device according to Claim 5,

wherein the external connecting terminals and the part of the circuit unit are laminated with an interlayer insulating film interposed therebetween, and

the external connecting terminals have the same film as a first conductive film constituting the circuit unit.

8. The electro-optical device according to Claim 1, further

comprising:

a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and

an electro-optical material that is held in the internal space,

wherein the display electrodes and a part of the circuit unit are disposed to face the internal space.

9. An electronic apparatus comprising the electro-optical device according to Claim 1.

ABSTRACT

An electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit or the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

FIG. 1

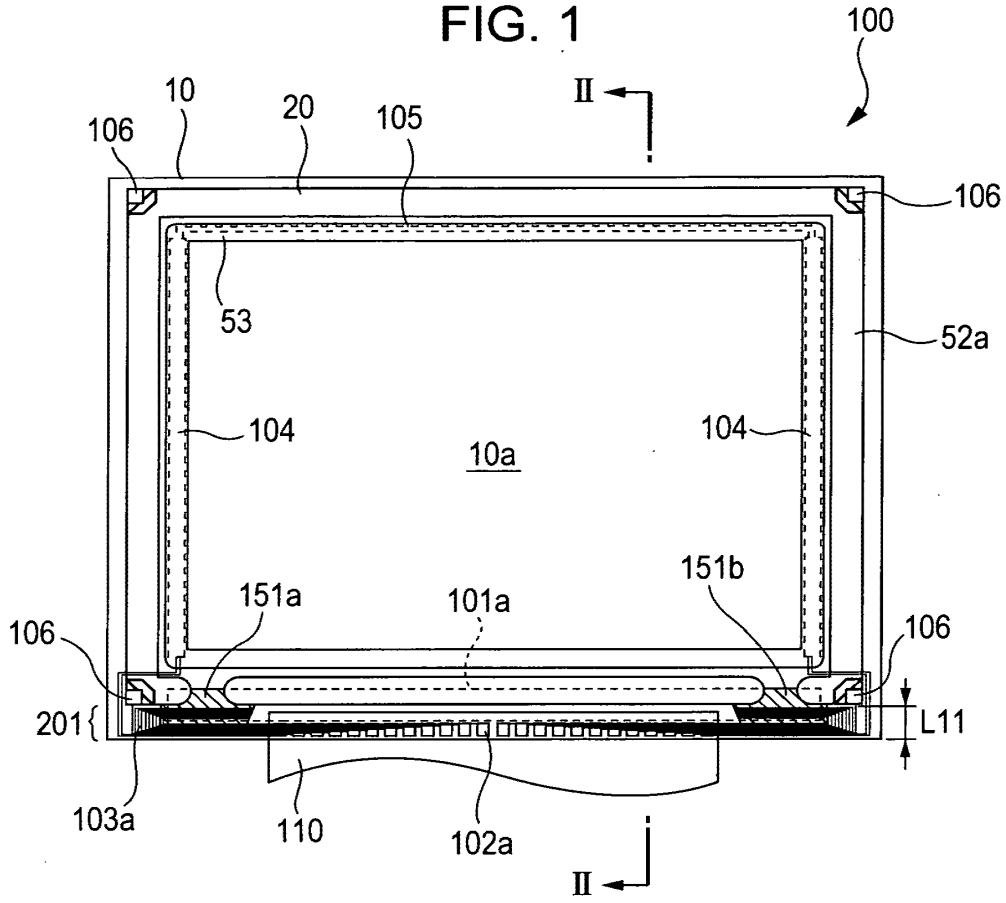

100
10
20
105
II
106
106
53
52a
104
104
10a
151b
151a
101a
106
106
201
L11
103a
110
102a
II

FIG. 2

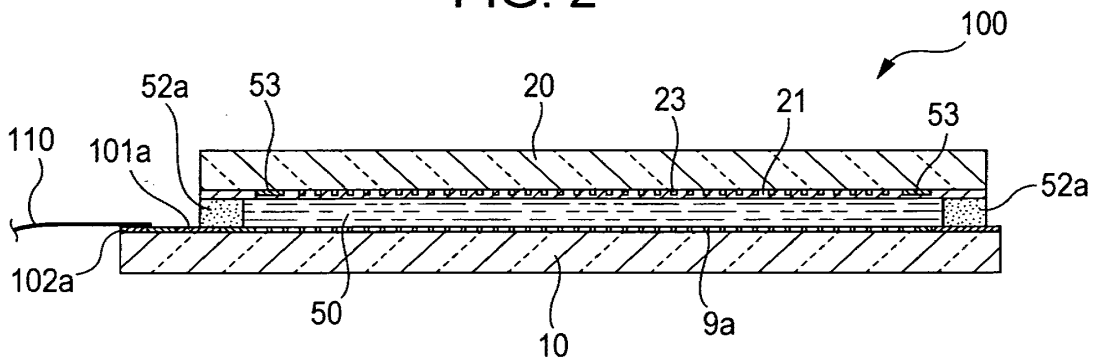

100
52a
53
20
23
21
53
110
101a
52a
102a
50
10
9a

FIG. 3

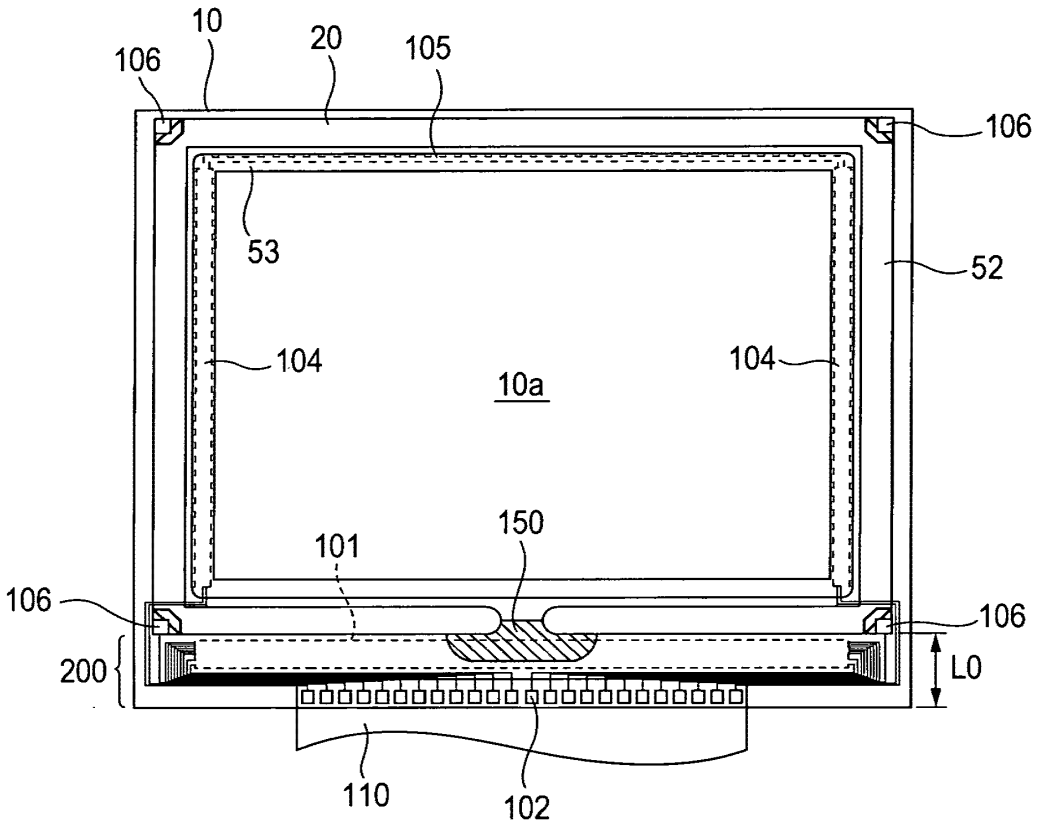


FIG. 4

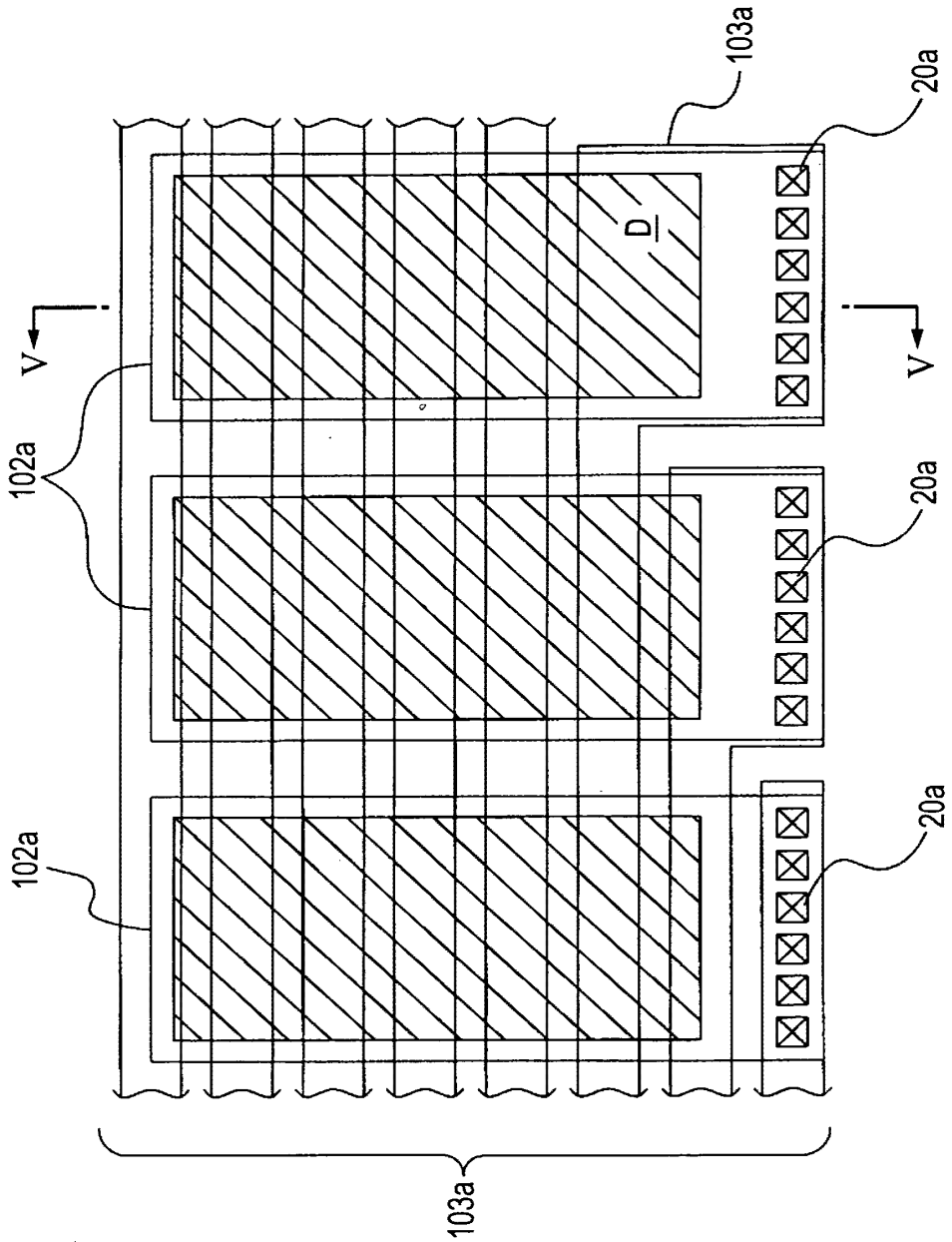


FIG. 5

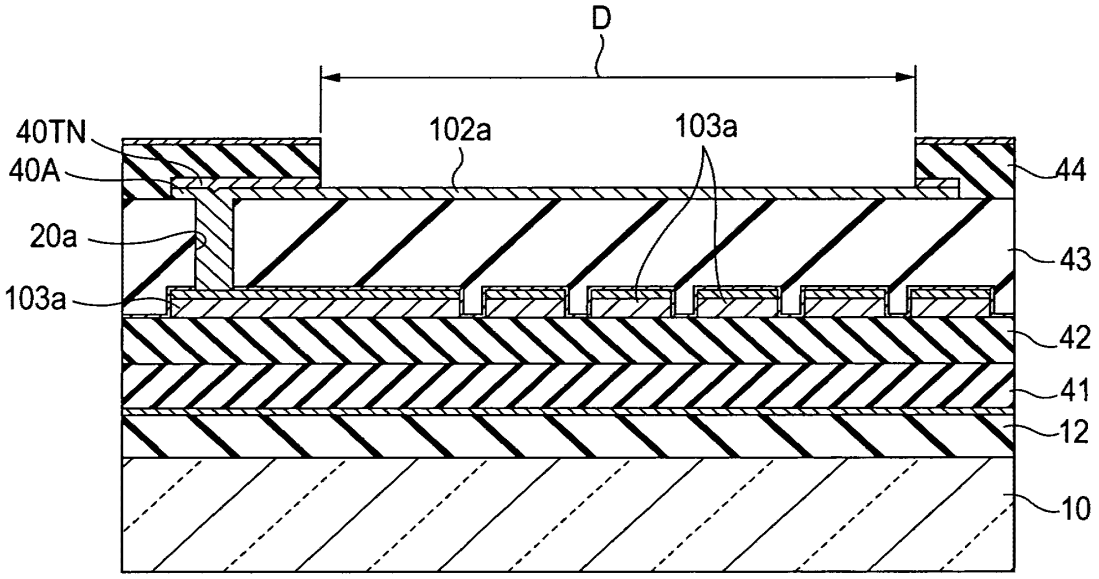


FIG. 6

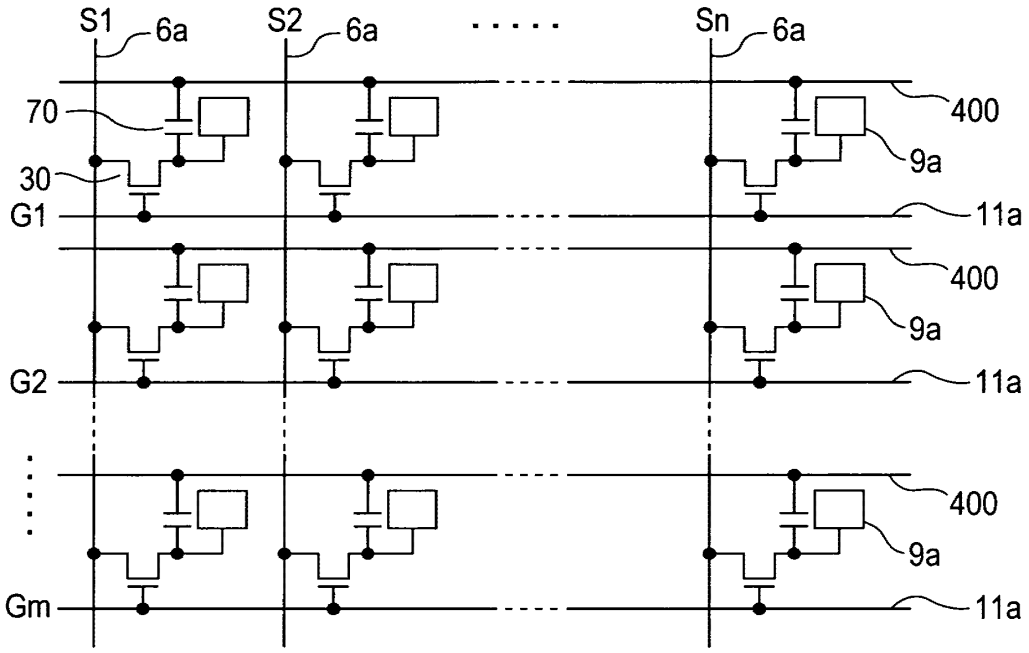


FIG. 7

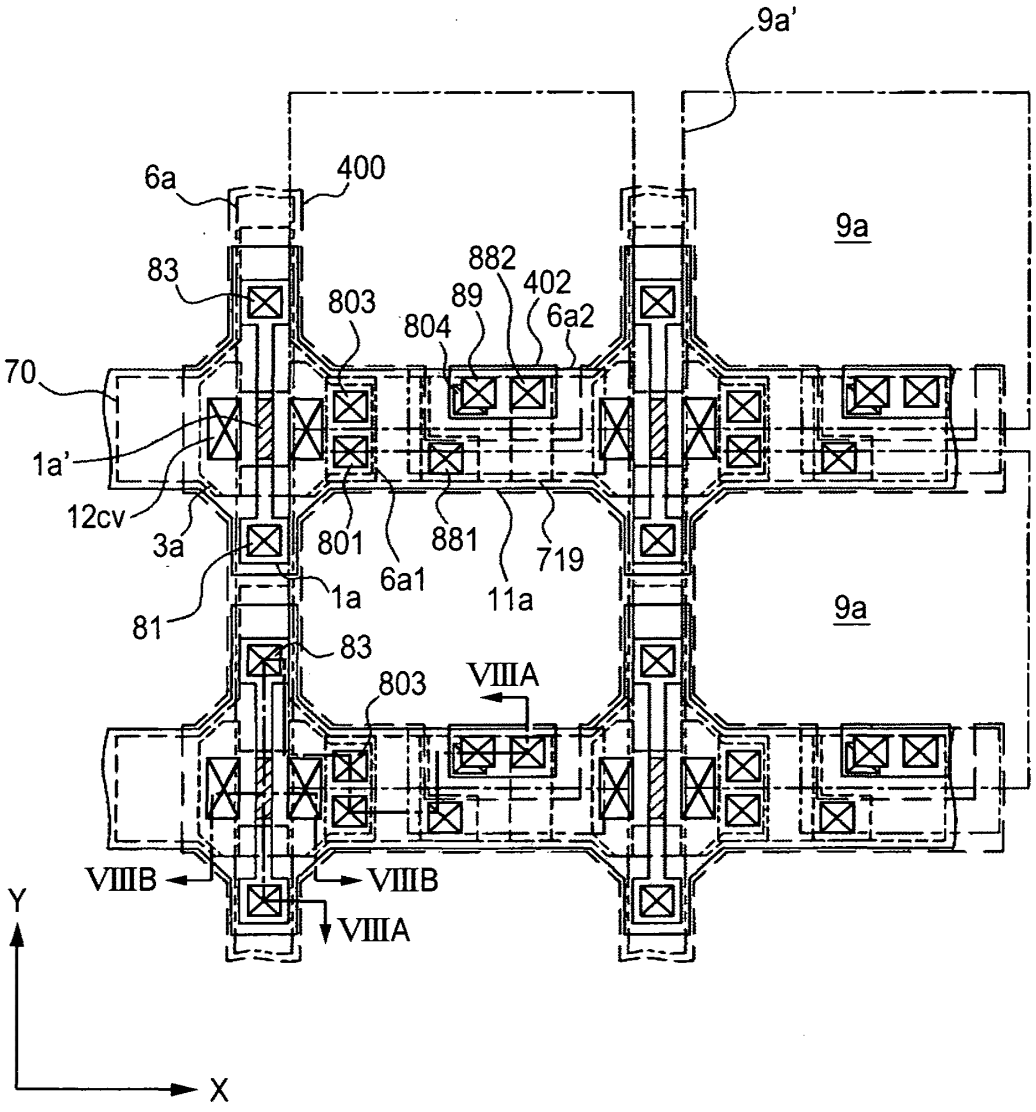

9a'
6a
400
9a
83
882
402
89
803
804
6a2
70
1a'
12cv
3a
801
881
719
6a1
11a
1a
81
83
803
VIIIA
9a
VIIIB
VIIIB
VIIIA
Y
X

FIG. 8B

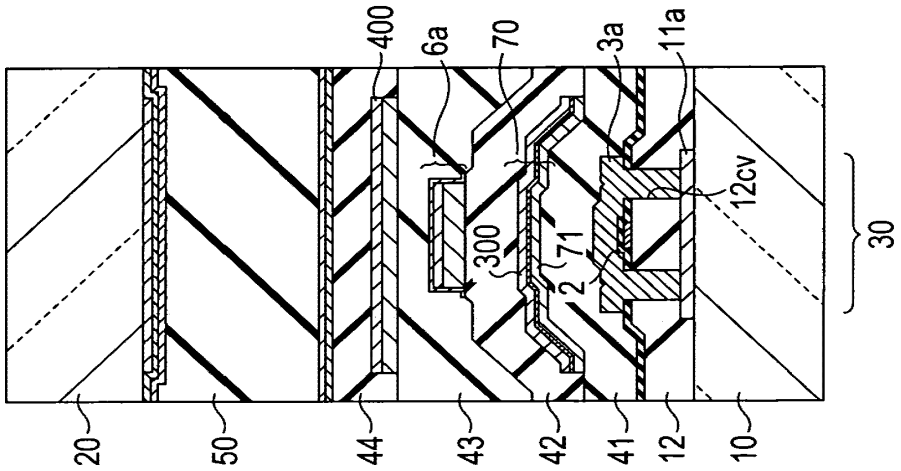

400
6a
70
3a
11a
12cv
30
300
71
2
20
50
44
43
42
41
12
10

FIG. 8A

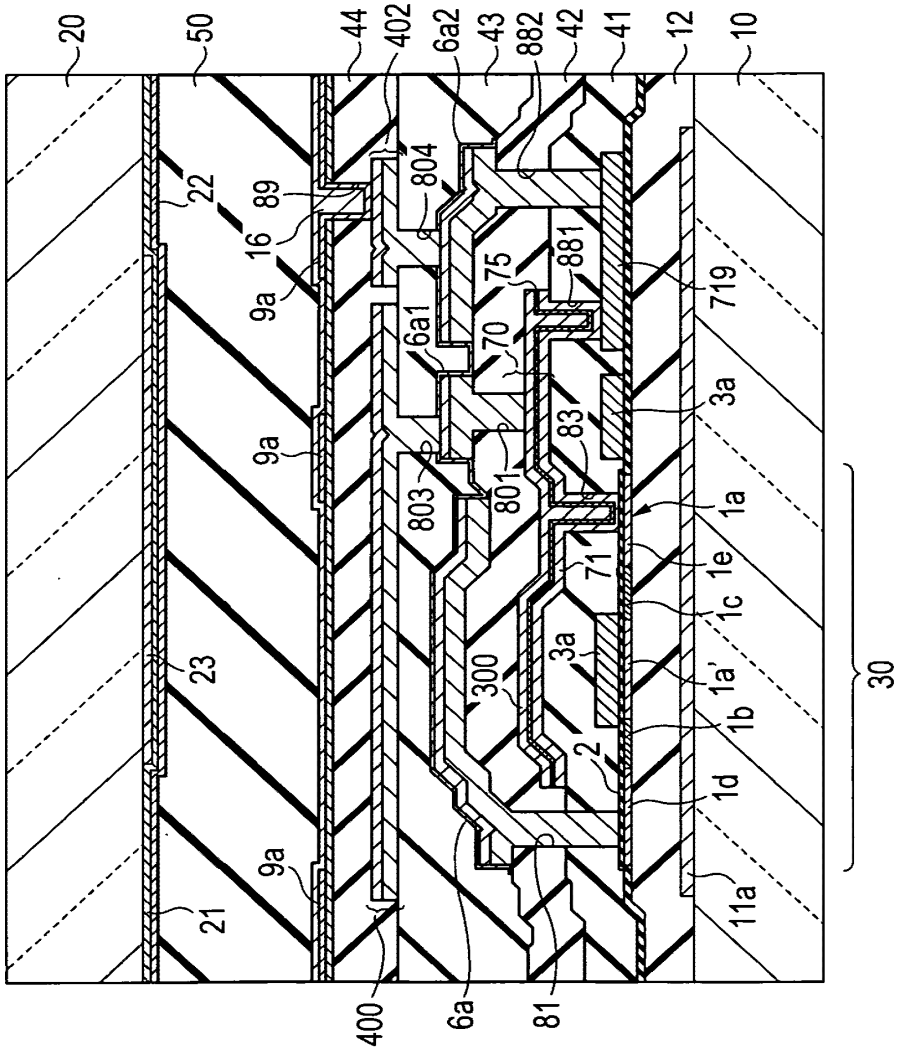

20
50
44
402
6a2
43
882
42
41
12
10
22
89
804
16
9a
881
75
719
6a1
70
3a
83
801
803
1a
71
1e
1c
1a'
1b
1d
300
2
23
21
11a
400
6a
81
30

FIG. 9

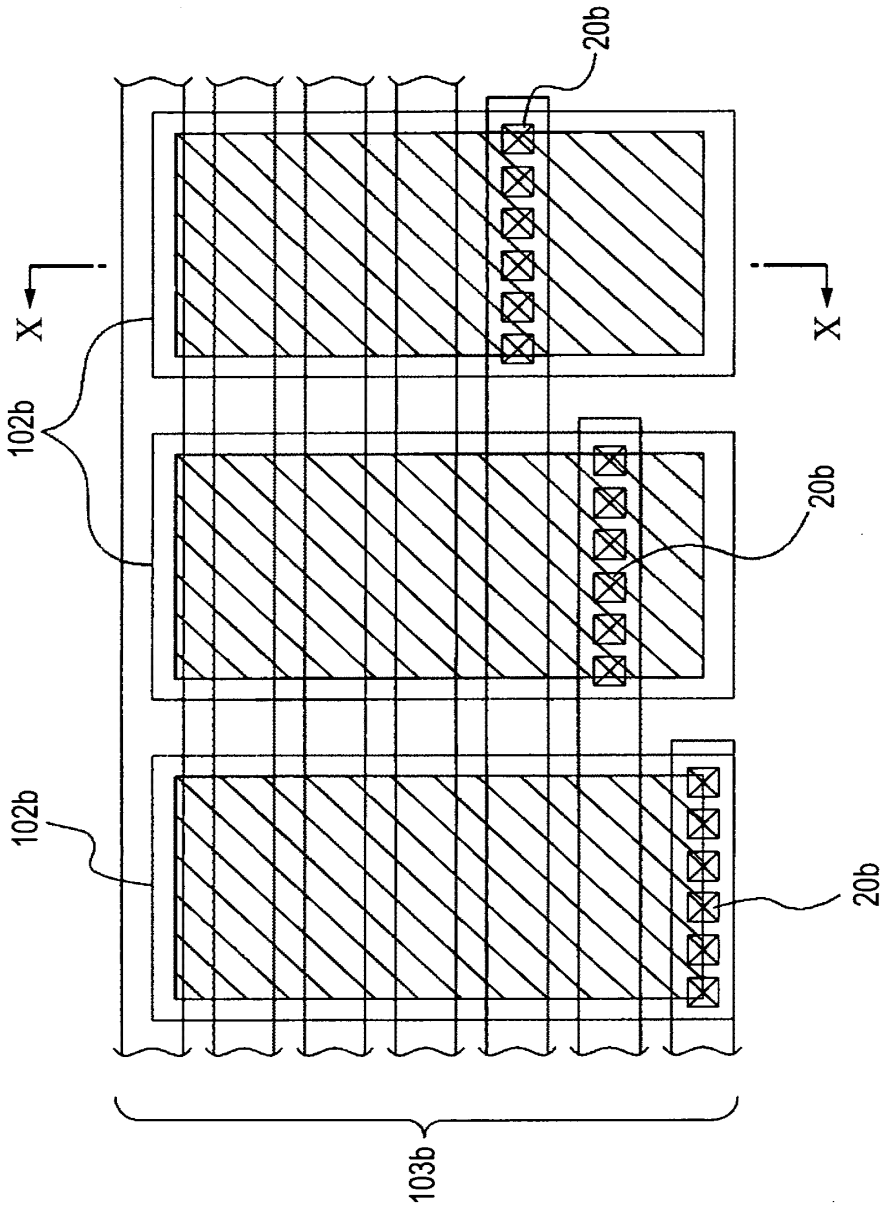


FIG. 10

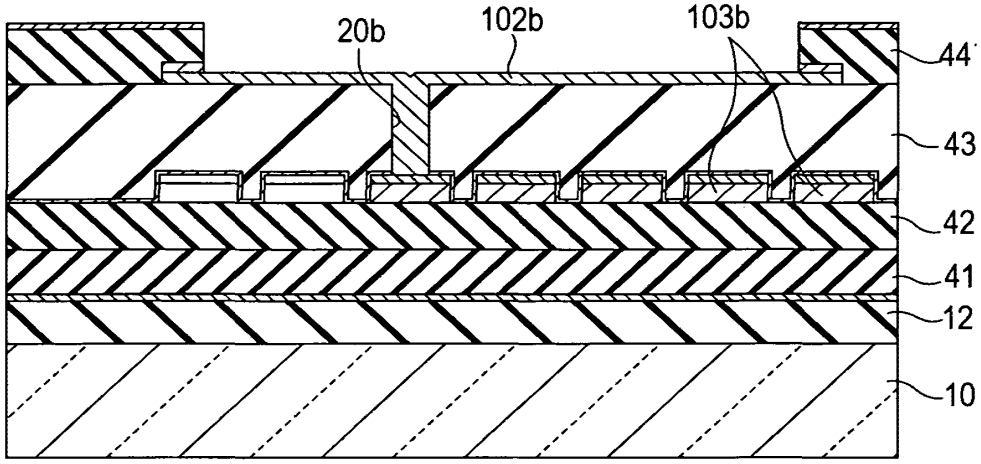

20b
102b
103b
44
43
42
41
12
10

FIG. 11

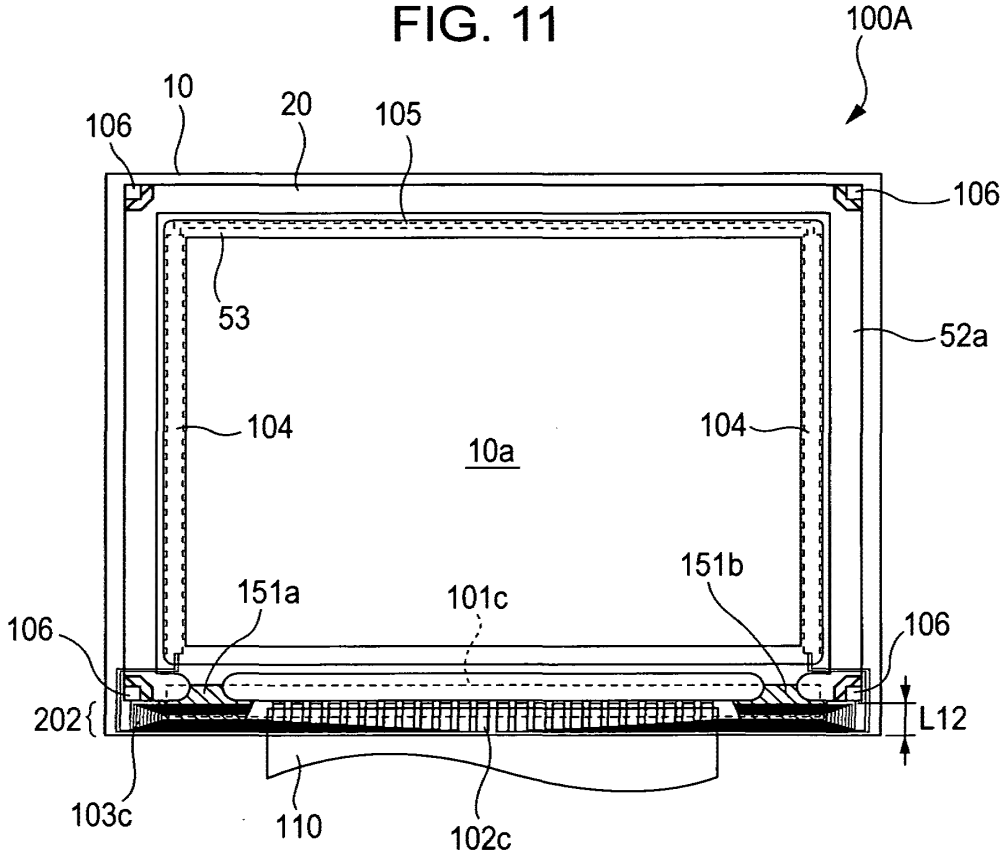

100A
10
106
20
105
106
53
52a
104
104
10a
151a
101c
151b
106
106
202
L12
103c
110
102c

FIG. 12

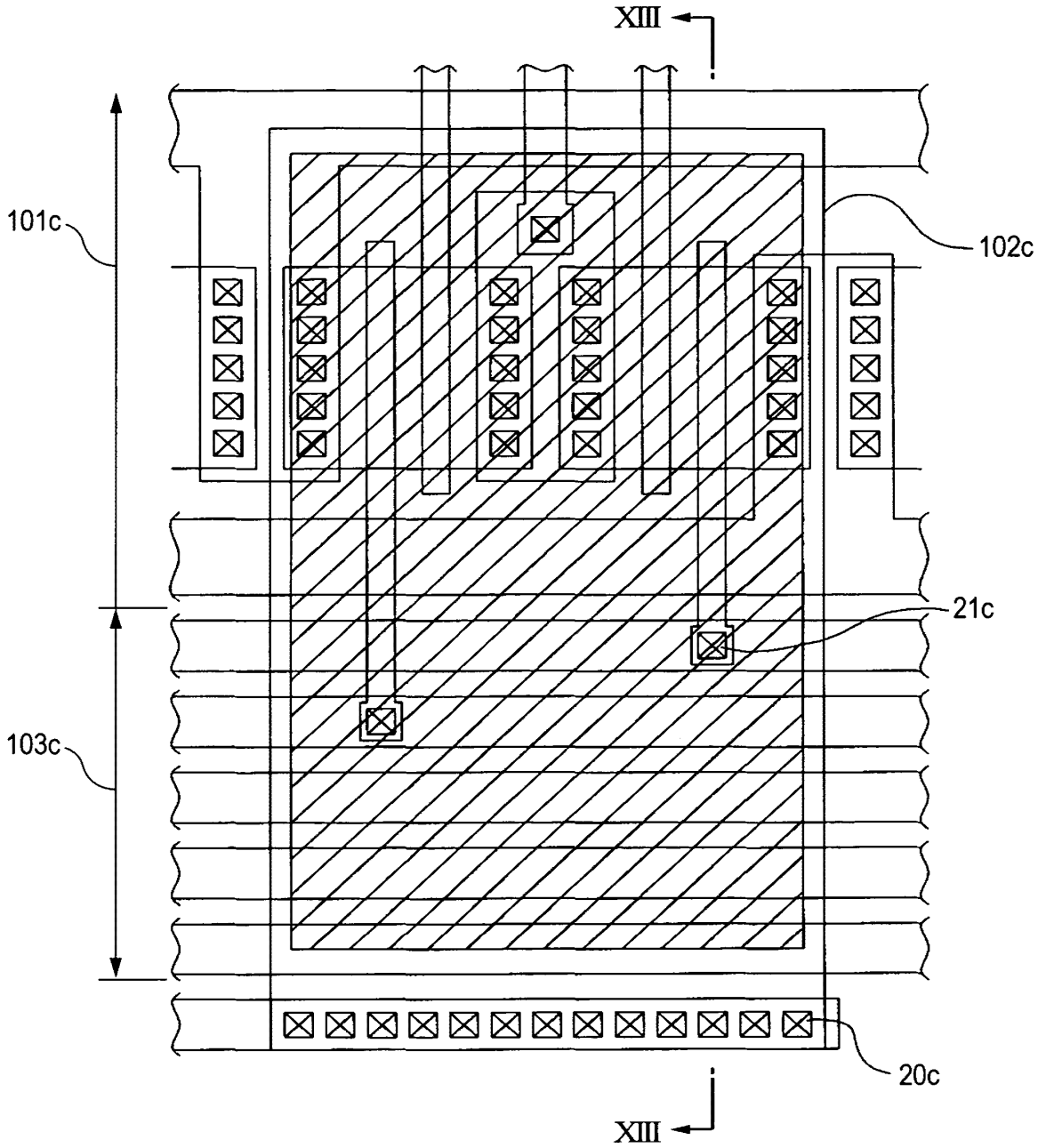


FIG. 13

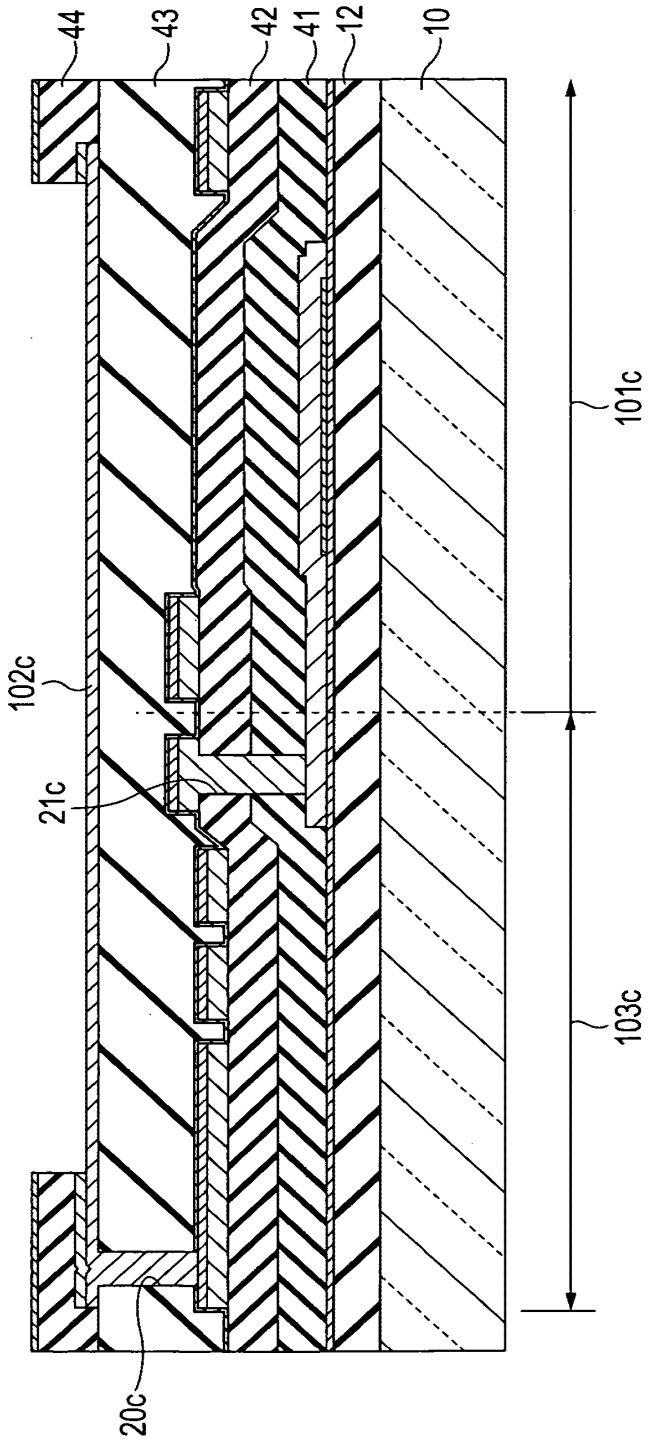


FIG. 14

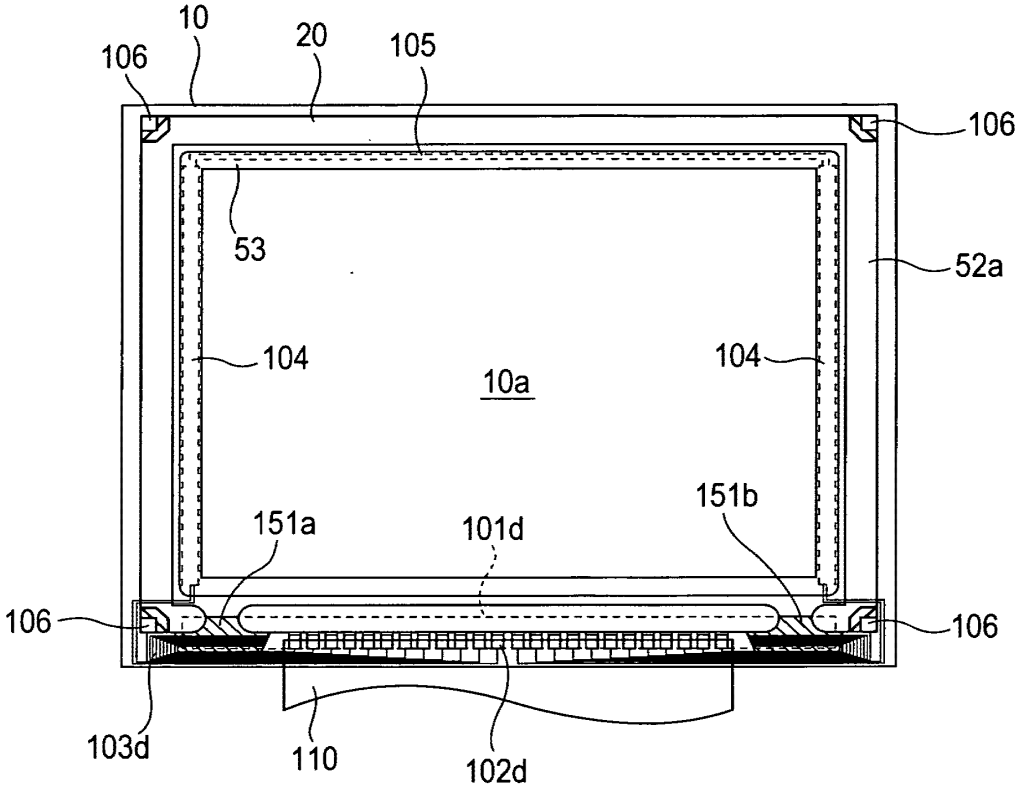
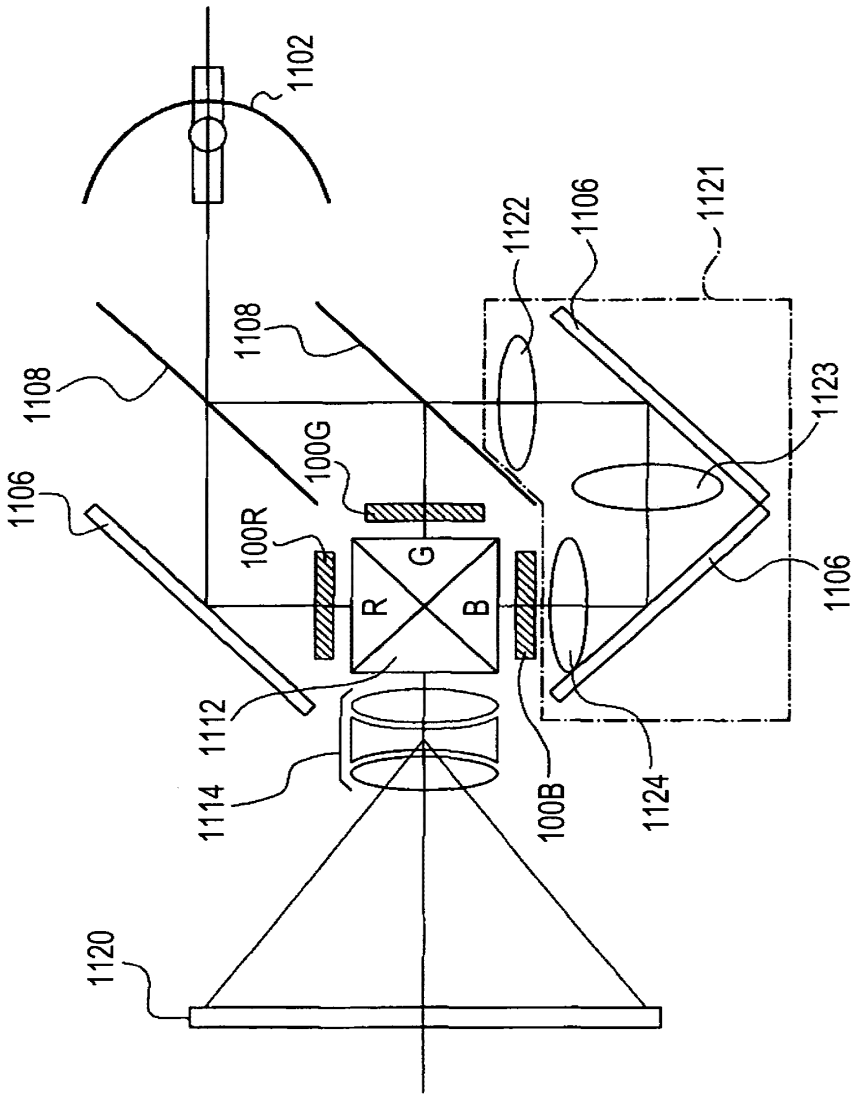

10
20
105
106
106
53
52a
104
104
10a
151b
151a
101d
106
106
103d
110
102d

FIG. 15


1100
1102
1122
1106
1121
1108
1108
1123
100G
1106
100R
G
R
B
1106
1112
1114
100B
1124
1120

PTO/SB/106 (8-98)
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Seiko Epson Ref. No.: J0113435US01 Attorney's Ref. No.: 125312

Declaration and Power of Attorney For Patent Application

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Japanese Language Declaration

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As a below named inventor, I hereby declare that:

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My residence, post office address and citizenship are as stated next to my name.

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

電気光学装置及び電子機器

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ _____に提出され、米国出願番号または特許協定条約 国際出願番号を _____ とし、（該当する場合） _____ に訂正されました。

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
2004-328982 (Number) (番号)	Japan (Country) (国名)	12/November/2004 (Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)

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(703) 836-6400

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Full name of sole or first inventor
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発明者の署名　日付
村出 正夫　2005年8月29日

Inventor's signature　Date
Masao Murade　Aug. 29, 2005

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国籍
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Full name of second joint inventor, if any

第二共同発明者の署名　日付

Second inventor's signature　Date

住所
日本国、＿＿＿＿＿＿、＿＿＿＿＿＿

Residence
＿＿＿＿＿＿、＿＿＿＿＿＿, Japan

国籍

Citizenship

私書箱

Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

BACKGROUND

1. Technical Field

[0001] The present invention relates to an electro-optical device, such as a liquid crystal device or the like, and to an electronic apparatus, such as a liquid crystal projector or the like, having such an electro-optical device.

2. Related Art

[0002] In such an electro-optical device, a substrate, on which display electrodes and a circuit unit for driving the display electrodes are provided, and a counter substrate are disposed to face each other with an electro-optical material, such as liquid crystal, interposed therebetween. More specifically, the substrates are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of the substrates are bonded to each other by a sealant so as to form an internal space, and the electro-optical material is sealed in the internal space.

[0003] The substrate provided with the display electrodes extends from the counter substrate on one side in plan view, and external connecting terminals are provided in a portion extending on one side (hereinafter, referred to as an extending portion). The external connecting terminals are connected to wiring lines led from a circuit unit and the like, and are provided such that surfaces thereof are exposed to the outside so as

to be supplied with signals or power from the outside. In addition, a driving circuit, which is connected to the external connecting terminals for supplying image signals, is generally provided in the extending portion.

[0004] In contrast, for example, as disclosed in JP-A-9-113906, according to a configuration in which a driving circuit is disposed in the internal space and only external connecting terminals are provided in the extending portion, the width of the extending portion can be made narrow, and thus the size of the substrate can be reduced.

[0005] However, in an actual electro-optical device, it is difficult to provide a space sufficient to dispose the driving circuit and to lead the wiring lines from the driving circuit in the internal space. Further, even when only the external connecting terminals are provided in the extending portion, at least some of the lead wiring lines connected to the external connecting terminals is substantially disposed in the extending portion. For this reason, in order to reduce the width of the extending portion, the layout of the external connecting terminals and the lead wiring lines needs to be considered.

SUMMARY

[0006] An advantage of some aspects of the invention is that it provides an electro-optical device which can reduce the size of a substrate and an electronic apparatus having such an electro-optical device.

[0007] According to a first aspect of the invention, an electro-optical

device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit or the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

[0008] In accordance with the first aspect of the invention, the pair of substrates are disposed to face each other with a predetermined gap therebetween and one substrate extends from the other substrate on at least one side. On one substrate extending from the other substrate of the pair of substrates, for example, wiring lines, such as scanning lines, data lines, and the like, electronic elements, such as thin film transistors (hereinafter, referred to as a "TFTs") and the like, and the circuit unit that drives display electrodes by means of a data line driving circuit or a scanning line driving circuit are provided. The display electrodes are formed on an upper layer of one substrate.

[0009] Further, in the extending portion extending the other substrate on the one side, the external connecting terminals, which are electrically

connected to the circuit unit, are provided. A plurality of external connecting terminals are arranged, for example, along an outer edge of the extending portion, and are correspondingly connected to the lead wiring lines, which are led from the circuit unit or the display electrodes. The lead wiring lines are generally relayed in a region other than a region where the external connecting terminals are arranged.

[0010] In the extending portion of the first aspect of the invention, the external connecting terminals and the lead wiring lines are arranged to at least partially overlap each other in plan view (that is, in a three-dimensional manner in the extending portion). Such a configuration is implemented by electrically connecting at least some of the lead wiring lines and the external connecting terminals to each other via contact holes or the like, for example, and by laminating them with an interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0011] As such, with the design of the layout, the width of the extending portion in the extension direction thereof can be reduced. As a result, with the reduced size of the substrate, the space of the electro-optical device can be saved. In particular, the number of electro-optical devices which can be manufactured per one wafer can be increased, such that considerable effects for reduction of manufacturing costs and enhancement of manufacturing efficiency are shown. For example, even

when the reduced size for one substrate is relatively small, for example, 1 mm or so, if several substrates to several tens or hundreds of substrates are arranged on the same wafer, there is a case in which one row or a plurality of rows of electro-optical devices can be further manufactured on the same wafer. Therefore, it is markedly advantageous in practice.

[0012] In the electro-optical device of the first aspect of the invention, it is preferable that the external connecting terminals and the lead wiring lines be laminated with an interlayer insulating film interposed therebetween, the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and the lead wiring lines have the same film as a second conductive film constituting the circuit unit.

[0013] According to this configuration, the external connecting terminals and the lead wiring lines are formed with different conductive films laminated with an interlayer insulating film interposed therebetween. Therefore, the external connecting terminals and the lead wiring lines can be constituted so as to overlap in plan view but not to be electrically connected to each other in portions other than portions where connected each other via contact holes or the like.

[0014] Further, the external connecting terminals and the lead wiring lines are formed as the same film as a conductive film constituting the circuit unit or to include the same film as such a conductive film, such that the laminate structure of the external connecting terminals and the lead wiring lines does not need to be prepared separately from the

circuit unit. Therefore, the structure on the substrate can be simplified and be relatively easily formed. Moreover, as a material of the conductive film, for example, aluminum (Al) having low resistance is suitably used.

[0015] Further, in the electro-optical device of the first aspect of the invention, it is preferable that the plurality of external connecting terminals be arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and be connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

[0016] According to this configuration, the plurality of lead wiring lines extend in the direction in which the plurality of external connecting terminals are arranged, such that the external connecting terminals and the lead wiring lines intersect each other in a three-dimensional manner. The external connecting terminals and the lead wiring lines are connected, for example, via contact holes at the edges of the external connecting terminals (that is, the edges of the external connecting terminals on an outer edge side and an inner edge side) in the direction intersecting the direction along the one side. According to such a layout, the lead wiring lines can be efficiently arranged in a region where the external connecting terminals are formed. Further, since the lead wiring lines are connected to the external connecting terminals in a region distant from the region where the lead wiring lines extend, such that the external connecting terminals and other lead wiring lines adjacent to the lead wiring lines to be originally

connected to the external connecting terminals can be prevented from being electrically connected to each other due to an error in formation location of the contact hole, for example. Therefore, the liquid crystal device according to the above-described configuration can be manufactured with high reliability.

[0017] Further, in the electro-optical device of the first aspect of the invention, it is preferable that the plurality of external connecting terminals be arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and be correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

[0018] According to this configuration, the external connecting terminals and the lead wiring lines are correspondingly connected to each other via contact holes, for example, in the region where they intersect each other in plan view. With such a layout, the lead wiring lines can be efficiently arranged in the region where the external connecting terminals are formed, and the lead wiring lines are correspondingly connected to the external connecting terminals in the region where the lead wiring lines extend. Therefore, the regions for forming the contact holes do not need to be separately prepared, and thus the arrangement space of the lead wiring lines and the external connecting terminals can be made small. As a result, according to the above-described configuration, the width in the direction in which the extending portion extends can be further reduced, and thus the size of

the substrate can be further reduced.

[0019] Further, according to a second aspect of the invention, an electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

[0020] In accordance with the second aspect of the invention, in the extending portion, the circuit unit and the external connecting terminals are disposed to at least partially overlap each other in plan view. Such a configuration can be implemented by laminating the circuit unit and at least some of the external connecting terminals with an interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0021] As such, with the design of the layout, the width of the extending

portion in the extending direction thereof can be reduced. As a result, with the reduced size of the substrate, the same effects as those in the electro-optical device according to the first aspect of the invention can be obtained.

[0022] In the electro-optical device of the second aspect of the invention, it is preferable that the circuit unit be electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and have a driving circuit, which is driven by the supplied image signal, and at least a part of the driving circuit overlap the external connecting terminals in plan view.

[0023] According to this configuration, the driving circuit, that is, a so-called data line driving circuit is disposed to at least partially overlap the external connecting terminals in plan view. In general, the data line driving circuit is provided to extend along the one side and is connected to the external connecting terminals via the lead wiring lines, such that image signals can be supplied to both ends thereof. For this reason, since a region sufficient to arrange the plurality of lead wiring lines around the data line driving circuit is required, there are many cases in which the data line driving circuit is provided in the extending portion having little spatial restriction, together with the external connecting terminals. In this case, the external connecting terminals and the data line driving circuit are generally provided on the same plane, so that the width of the extending portion becomes large according to the size, the shape, and the like of the data line driving circuit.

[0024]In contrast, in the invention, since the entire data line driving circuit provided in the extending portion or at least a part thereof, and the external connecting terminals are provided in the same space, the width of the extending portion can be reduced, and thus the space of the electro-optical device can be effectively saved or the size of the electro-optical device can be effectively reduced.

[0025]Further, in the electro-optical device of the second aspect of the invention, it is preferable that the external connecting terminals and the part of the circuit unit be laminated with an interlayer insulating film interposed therebetween, and the external connecting terminals have the same film as a first conductive film constituting the circuit unit.

[0026]According to this configuration, since the external connecting terminals and the circuit unit are laminated with the interlayer insulating film interposed therebetween, the external connecting terminals and the circuit unit can overlap in plan view but can not be electrically connected to each other. In addition, the external connecting terminals are formed as the same film as the conductive film constituting the circuit unit or to include the same film as the conductive film, so that the structure on the substrate can be simplified and relatively easily formed. Moreover, as a material of the conductive film, for example, aluminum (Al) having low resistance is suitably used.

[0027]The electro-optical device of the first aspect of the invention may further include a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space

between the pair of substrates, and an electro-optical material that is held in the internal space. In addition, it is preferable that the display electrodes and the part of the circuit unit be disposed to face the internal space.

[0028]According to this configuration, the edges of the opposite surfaces of the pair of substrates are bonded to each other by the sealant so as to form the internal space therebetween, and the extending portion extends from the edges. The electro-optical material, such as liquid crystal, is sealed into the internal space. The display electrodes are disposed to face the internal space. Further, a part of the circuit unit, for example, wiring lines or elements, such as scanning lines, data lines, TFTs, and the like, and a driving circuit, such as a scanning line driving circuit or the like, is provided in the region facing the internal space, together with the display electrodes. Therefore, almost the entire area of the extending portion can be used for forming the external connecting terminals.

[0029]According to a third aspect of the invention, an electronic apparatus includes the above-described electro-optical device (including various configurations).

[0030]According to this configuration, since the electronic apparatus includes the above-described electro-optical device, various electronic apparatuses, such as a projection type display device, a liquid crystal television, a cellular phone, an electronic organizer, a word processor, a viewfinder-type or monitor-direct-view-type video tape recorder, a workstation, a video phone, a POS terminal, a touch panel, and the like,

which are saved in space and reduced in size, can be implemented. In addition, for example, an electrophoretic device, such as an electronic paper, can be implemented as the electronic apparatus according to the third aspect of the invention.

[0031] Such effects and other advantages of the invention will be apparent from the following embodiments to be described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The invention will be described with reference to the accompanying drawings, wherein like numbers reference like elements.

[0033] Fig. 1 is a plan view showing a configuration of a liquid crystal device according to a first embodiment of the invention.

[0034] Fig. 2 is a cross-sectional view showing the liquid crystal device taken along the line II-II of Fig. 1.

[0035] Fig. 3 is a plan view showing a comparative example of the liquid crystal device according to the first embodiment.

[0036] Fig. 4 is a plan view showing a configuration of main parts of the liquid crystal device according to the first embodiment.

[0037] Fig. 5 is a cross-sectional view showing an extending portion taken along the line V-V of Fig. 4.

[0038] Fig. 6 is a schematic view showing an equivalent circuit in an image display region of the liquid crystal device according to the first embodiment.

[0039] Fig. 7 is a plan view showing a configuration of the image display

region of the liquid crystal device according to the first embodiment.

[0040]Fig. 8A is a cross-sectional view showing the configuration of the image display region of the liquid crystal device according to the first embodiment taken along the line VIIIA-VIIIA of Fig. 7.

[0041]Fig. 8B is a cross-sectional view showing the configuration of the image display region of the liquid crystal device according to the first embodiment taken along the line VIIIB-VIIIB of Fig. 7.

[0042]Fig. 9 is a plan view showing a modification of the liquid crystal device according to the first embodiment.

[0043]Fig. 10 is a cross-sectional view showing the extending portion taken along the line X-X of Fig. 9.

[0044]Fig. 11 is a plan view showing a configuration of a liquid crystal device according to a second embodiment.

[0045]Fig. 12 is a plan view showing a configuration of main parts of the liquid crystal device according to the second embodiment.

[0046]Fig. 13 is a cross-sectional view showing an extending portion taken along the line XIII-XIII of Fig. 12.

[0047]Fig. 14 is a plan view showing a modification of the liquid crystal device according to the second embodiment.

[0048]Fig. 15 is a cross-sectional view showing a configuration of a liquid crystal projector according to an embodiment of an electronic apparatus of the invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0049]Hereinafter, embodiments of the invention will be described with reference to the drawings.

Embodiments of Electro-Optical Device

[0050]The embodiments of the invention will be described with reference to Figs. 1 to 13. In the embodiments to be described below, the electro-optical device of the invention is applied to a liquid crystal device.

First Embodiment

[0051]A liquid crystal device according to a first embodiment of the invention will be described with reference to Figs. 1 to 7.

Schematic Configuration of Liquid Crystal Device

[0052]First, the schematic configuration of a liquid crystal device will be described with reference to Figs. 1 to 3. Fig. 1 is a plan view showing the configuration of a liquid crystal device according to the present embodiment, and Fig. 2 is a cross-sectional view taken along the line II-II of Fig. 1. Fig. 3 shows a comparative example of the liquid crystal device according to the present embodiment.

[0053]Referring to Figs. 1 and 2, in the liquid crystal device 100, a TFT array substrate 10 and a counter substrate 20 are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of both substrates are bonded to each other by a sealant 52a so as to form an internal space. The TFT array substrate 10 has an

extending portion 201 which extends from the counter substrate 20 on one side in plan view, and the sealant 52a defines openings which lead to the internal space at predetermined places of a side where the extending portion 201 extends (here, both ends of the side). Further, a liquid crystal layer 50 is formed by injecting liquid crystal into the internal space through the openings, and the openings are sealed with sealing mold materials 151a and 151b. A frame light-shielding film 53, which is provided along an inner edge of the sealant 52a, defines an image display region 10a on which images are displayed.

[0054]On the image display region 10a of a surface (top surface in Fig. 2) of the TFT array substrate 10 facing the counter substrate 20, pixel electrodes 9a, which are examples of 'display electrodes' of the invention, are provided on switching TFTs or wiring lines, such as scanning lines, data lines, and the like. In addition, an alignment film is formed just above the pixel electrodes 9a. On a surface (bottom surface in Fig. 2) of the counter substrate 20 facing the TFT array substrate 10, a counter electrode 21 is formed via a stripe-shaped light-shielding film 23, and an alignment film is formed on the counter electrode 21. Further, in at least one corner portion (here, all of four corner portions) of the counter substrate 20, vertical connecting terminals 106 for electrically connecting the counter substrate 20 and the TFT array substrate 10 are provided. The alignment state of liquid crystal of the liquid crystal layer 50 changes according to the electric field applied between the pixel electrodes 9a and the counter electrode 21, but liquid crystal of the liquid crystal layer 50 maintains an

initial alignment state defined by the alignment films when the electric field is not applied.

[0055] In a region of the surface of the TFT array substrate 10 facing the counter substrate 20 which corresponds to a region where the frame light-shielding film 53 is formed, scanning line driving circuits 104 for driving scanning lines, and wiring lines 105 are provided. In Fig. 1, two scanning line driving circuits 104 are provided on left and right sides the frame light-shielding film 53. The wiring lines 105 are relayed on the upper side of the frame light-shielding film 53 so as to connect the two scanning line driving circuits 104.

[0056] The extending portion 201 of the TFT array substrate 10 is provided with a data line driving circuit 101a for driving data lines, which is a specified example of 'driving circuit' of the invention, along a lower side of the sealant 52a in Fig. 1. The upper half of the data line driving circuit 101a overlaps the sealant 52a in plan view. Further, the lower half of the data line driving circuit 101a overlaps portions pushed from the openings of the sealing mold materials 151a and 151b at both ends thereof.

[0057] Moreover, in the present embodiment, all of electronic elements, such as TFTs or the like, the wiring lines, such as scanning lines, data lines, and the like, and circuits on the TFT array substrate 10 including the scanning line driving circuits 104 and the data line driving circuit 101a correspond to a specified example of 'circuit unit' of the invention. Further, the extending portion 201 may be further provided with a sampling circuit that applies image signals to a

plurality of data lines with a predetermined timing, a precharge circuit that supplies a precharge signal having a predetermined voltage level to the plurality of data lines prior to the image signals, and a test circuit that tests quality, defects, or the like of the liquid crystal device 100 during manufacture or at the time of shipping.

[0058]Further, in the present embodiment, at least some of a plurality of lead wiring lines 103a in the extending portion 201 is provided to overlap external connecting terminals 102a in plan view. Specifically, in the liquid crystal device 100, a layer where the external connecting terminals 102a are formed and a layer where the lead wiring lines 103a are formed are laminated with, for example, an interlayer insulating film interposed therebetween, and the formation region of the external connecting terminals 102a and the formation region of the lead wiring lines 103a at least partially overlap each other. Two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0059]The external connecting terminals 102a are provided so as to supply power or signals to the liquid crystal device 100 from an external circuit, which is connected thereto via an FPC 110. The external connecting terminals 102a are properly connected to the driving circuit, such as the scanning circuit driving circuits 104 or the data line driving circuit 101a, via the lead wiring lines 103a. In the liquid crystal device 100, the pixel electrodes 9a are driven by signals inputted to the external connecting terminals 102a from the outside,

such that images are displayed. Here, the data line driving circuit 101a is connected to the plurality of external connecting terminals 102a through the lead wiring lines 103a at both ends of the extending portion 201.

[0060]As shown in Fig. 3, in a liquid crystal device according to a comparative example of the present embodiment, external connecting terminals 102 and lead wiring lines 103 are disposed on the same plane so as not to overlap each other in plan view. In addition, the external connecting terminals 102 must be connected to the FPC 110, and thus a sealant 150 does not overlap the external connecting terminals 102. Accordingly, the external connecting terminals 102a need to be disposed away from the sealant 150 to some extent. As a result, an extending portion 200 has a predetermined width L0 and has a space, such that a space for disposing the entire data line driving circuit 101 is generated.

[0061]In contrast, in the liquid crystal device 100 of the present embodiment, as described above, at least some of the plurality of lead wiring lines 103a are disposed to overlap the external connecting terminals 102a in plan view, so that a space can be saved. In particular, since the external connecting terminals 102a are arranged along an outer edge of the extending portion 201, the width L11 of the extending portion 201 in the extending direction can be reduced further than the related art.

[0062]Further, in the liquid crystal device 100 of the present embodiment, since the external connecting terminals 102a are arranged in

a region between the sealing mold materials 151a and 151b, the external connecting terminals 102a do not need to be provided distant from and the sealing mold materials 151a and 151b. In addition, in Fig. 1, the positions of the external connecting terminals 102a can be moved upward by disposing the upper half of the data line driving circuit 101a in a region where the sealant 52a is provided. As a result, the width L11 of the extending portion 201 can be further reduced than the width L0 of the extending portion 200 in the comparative example.

[0063]As such, the space can be saved in the liquid crystal device 100 of the present embodiment, and thus an electronic apparatus, to which the liquid crystal device 100 is applied, can have a high degree of freedom in terms of design. Further, the number of liquid crystal devices which can be manufactured per one wafer can be increased, and considerable effects for reduction of manufacturing costs and enhancement of manufacturing efficiency are shown. That is, even though the reduced width of the extending portion 201 in one liquid crystal device 100 is small, several hundreds or thousands of regions, each corresponding to the TFT array substrate 10, are generally formed on the wafer and a large number of such wafers are manufactured. Therefore, it is very effective for manufacture.

[0064]Here, on the lower side of the sealant 52a or the lower side of the counter substrate 20, the openings and the sealing mold materials 150a and 150b are disposed at the ends thereof and the external connecting terminals 102a are arranged at a central portion thereof. Therefore, even when the lead wiring lines 103a are divided into the

left and right sides, the lengths of the lead wiring lines 103a can be approximately equal one left and right sides, such that a failure, such as a signal delay between the left and right sides, does not occur. Further, the openings are disposed at the left and right ends, so that liquid crystal can be injected into the internal space efficiently and uniformly.

Configuration of Extending Portion

[0065]Next, referring to Figs. 4 to 7, a specified configuration of the extending portion 201 in the liquid crystal device 100 will be described in detail. Fig. 4 shows main parts of the extending portion in the liquid crystal device according to the present embodiment on a magnified scale. Fig. 5 is a cross-sectional view taken along the line V-V of Fig. 4. Fig. 6 shows an equivalent circuit constituted by a pixel unit in an image display region of the liquid crystal device according to the present embodiment. Fig. 7 is a plan view showing the configuration of the pixel unit. Figs. 8A and 8B are cross-sectional views showing the configuration of the pixel unit. Specifically, Fig. 8A is a cross-sectional view taken along the line VIIIA-VIIIA of Fig. 7, and Fig. 8B is a cross-sectional view taken along the line VIIIB-VIIIB of Fig. 7. In Figs. 8A and 8B, the scale of each layer or each member has been adjusted in order to have a recognizable size.

[0066]In Fig. 4, the plurality of external connecting terminals 102a are arranged in one direction, and the plurality of lead wiring lines 103a extend in the direction in which the external connecting terminals 102a

are arranged and are connected to the external connecting terminals 102a via contact holes 20a. The plurality of contact holes 20a are provided at the outer edges of the plurality of external connecting terminals 102a. Alternatively, all or some of the contact holes 20a may be provided at the inner edges of the plurality of external connecting terminals 102a.

[0067]According to such a layout, the lead wiring lines 103a are connected to the external connecting terminals 102a in a region distant from a region where the lead wiring lines 103a extend, so that the external connecting terminals 102a and other lead wiring lines 103a adjacent to the lead wiring lines 103a to be originally connected to the external connecting terminals 102a can be prevented from being electrically connected to each other due to an error in formation location of the contact hole 20a, for example. Therefore, the liquid crystal device 100 can be manufactured with high reliability.

[0068]In Fig. 5, the external connecting terminals 102a and the lead wiring lines 103 are laminated with an interlayer insulating film 43 interposed therebetween. Further, the contact holes 20a are formed to pass through the interlayer insulating film 43. Each of the lead wiring lines 103a is connected to a desired external connecting terminal 102a via the contact hole 20a but is electrically isolated from other external connecting terminals 102a by means of the interlayer insulating film 43, so that the lead wiring lines 103a overlap the external connecting terminals 102a in plan view.

[0069]Here, a base insulating film 12 and interlayer insulating films

41, 42, 43, and 44 are laminated on the TFT array substrate 10 in that order, and the lead wiring lines 103a are provided on the interlayer insulating film 43. Here, the lead wiring line 103a and the external connecting terminal 102a each has a two-layered structure made of an aluminum layer 40A, a titanium nitride film 40TN, and an exposed surface D of each of the external connecting terminals 102a (a hatched region of each of the external connecting terminals 102a in Fig. 4) is exposed to the outside from an opening which is formed by partially removing the interlayer insulating film 44 and the titanium nitride film 40TN. A laminated structure in the image display region 10a on the TFT array substrate 10 is constituted based on the above-described laminated structure. Next, the configuration of the laminated structure in the image display region 10a will be described below.

Configuration of Image Display Region

[0070] In Fig. 6, a plurality of scanning lines 11a and a plurality of data lines 6a are arranged to intersect each other in the image display region 10a, and pixel units, each being selected by one of the plurality of scanning lines 11a and one of the plurality of data lines 6a, are formed between these lines. Each of the pixel units has a TFT 30, a pixel electrode 9a, and a storage capacitor 70. The TFT 30 is provided to apply image signals S1, S2, ..., and Sn supplied from the data lines 6a to the selected pixels. A gate of the TFT 30 is connected to the scanning line 11a, a source thereof is connected to the data line 6a, and a drain thereof is connected to the pixel electrode 9a. A liquid

crystal capacitor is formed between the pixel electrode 9a and a counter electrode 21 to be described below, and the respective pixel electrodes 9a hold the input image signals S1, S2, …, and Sn for a predetermined period of time. That is, an opening region for each pixel unit is divided by each of the pixel electrodes 9a. One electrode of the storage capacitor 70 is connected to the drain of the TFT 30 in parallel with the pixel electrode 9a, and the other electrode thereof is connected to a fixed-potential capacitor wiring line 400, such that the electric potential on the other electrode can be made constant.

[0071]The liquid crystal device 100 uses a TFT active matrix driving method, for example. Specifically, in the liquid crystal device 100, scanning signals G1, G2, …, Gm are line-sequentially applied to the respective scanning lines 11a from the scanning line driving circuit 104 (see Fig. 1), and simultaneously the image signals S1, S2, …, and Sn supplied from the data line driving circuit 101 (see Fig. 1) are applied through the data lines 6a to a selected row of horizontally-arrayed pixel units in which the TFTs 30 are turned on. As a result, the image signals are supplied to the pixel electrodes 9a corresponding to the selected pixels. Since the TFT array substrate 10 is disposed to face the counter substrate 20 with the liquid crystal layer 50 interposed therebetween (see Fig. 2), the amount of transmitted light between the substrates is controlled for each pixel by applying an electric field to the liquid crystal layer 50 for each pixel unit in such a manner, such that gray-scale display of an image is performed. At this time, the image signal held in each pixel unit is prevented from leaking by means

of the storage capacitor 70.

[0072]In Figs. 7 and 8, circuit elements of the above-described pixel unit are patterned to be formed on the TFT array substrate 10 as laminated conductive films. The TFT array substrate 10 of the present embodiment is made of a quartz substrate and is disposed to face the counter substrate 20 made of a glass substrate, a quartz substrate, or the like. Further, each of the circuit elements has a first layer including the scanning line 11a, a second layer including the gate electrode 3a, a third layer including the fixed-potential capacitor electrode of the storage capacitor 70, a fourth layer including the data line 6a, a fifth layer including the capacitor wiring line 400, and a sixth layer including the pixel electrode 9a from the bottom. In addition, the base insulating film 12 is provided between the first and second layers, the first interlayer insulating film 41 is provided between the second and third layers, the second interlayer insulating film 42 is provided between the third and fourth layers, the third interlayer insulating film 43 is provided between the fourth and fifth layers, and the fourth interlayer insulating film 44 is provided between the fifth and sixth layers, such that the above-described elements can be prevented from being short-circuited.

Configuration of First Layer - Scanning Line and the like

[0073]The first layer has the scanning lines 11a. Each of the scanning lines 11a is patterned to have a main line part extending in an X direction of Fig. 7 and a protruding part extending in a Y direction of

Fig. 7 in which the data lines 6a or the capacitor wiring lines 400 extend. The scanning line 11a is made of, for example, conductive polysilicon. Alternatively, the scanning line 11a may be made of a metal simplex of at least one high-melting-point metal selected from a group of titanium (Ti), chromium (Cr), tungsten (W), tantalum (Ta), molybdenum (Mo), and the like, an alloy thereof, metal silicide, polysilicide, or a laminate thereof. That is, the scanning line 11a of the present embodiment covers a region between the openings as much as possible, thereby serving as a light-shielding film which shields the TFT 30 from the lower side.

Configuration of Second Layer - TFT and the like

[0074]The second layer has the TFTs 30 and relay electrodes 719. Each of the TFTs 30 has an LDD (Lightly Doped Drain) structure, for example, and includes a gate electrode 3a, a semiconductor layer 1a, and a gate insulating film 2 for electrically isolating the gate electrode 3a from the semiconductor layer 1a. The gate insulating film 2 is made of, for example, an HTO (High Temperature Oxide) or a thermally-oxidized silicon oxide. The gate electrode 3a is made of, for example, conductive polysilicon. The semiconductor layer 1a is made of, for example, polysilicon, and has a lightly-doped source region 1b, a lightly-doped drain region 1c, a heavily-doped source region 1d, and a heavily-doped drain region 1e. In addition, on the second layer, the relay electrodes 719 are formed as the same film as that of the gate electrode 3a.

[0075]The gate electrode 3a of the TFT 30 is electrically connected to

the scanning line 11a via a contact hole 12cv formed in the base insulating film 12. The base insulating film 12 is made of a silicon oxide film, such as an HTO film or an NSG (non-silicate glass) film, electrically isolates the first layer from the second layer, and is formed on the entire surface of the TFT array substrate 10 so as to prevent element characteristics of the TFT 30 from changing due to roughness or contamination caused by the abrasion of a substrate surface.

Configuration of Third Layer - Storage Capacitor and the like

[0076]The third layer has the storage capacitors 70. Each of the storage capacitors 70 is configured such that a capacitor electrode 300 and a lower electrode 71 are disposed to face each other with a dielectric film 75 interposed therebetween. The capacitor electrode 300 is electrically connected to the capacitor wiring line 400 via contact holes 801 and 803 and a relay layer 6a1 for a capacitor wiring line. The lower electrode 71 and the heavily-doped drain region 1e are connected via a contact hole 83 formed in the first interlayer insulating film 41. Further, the lower electrode 71 and the pixel electrode 9a relay the respective layers by means of contact holes 881, 882, and 804, the relay electrode 719, a second relay electrode 6a2, and a third relay electrode 402, and are electrically connected via a contact hole 89.

[0077]The capacitor electrode 300 has a single layer made of a metal simplex of at least one high-melting-point metal selected from a group

of Ti, Cr, W, Ta, Mo, and the like, an alloy thereof, metal silicide, polysilicide, or a laminate. Preferably, the capacitor electrode 300 is made of tungsten silicide, and has a function of blocking light incident on the TFT 30 from the top in Fig. 8. The lower electrode 71 is made of conductive polysilicon, for example. The dielectric film 75 is made of, for example, a silicon oxide film, such as an HTO film or an LTO (Low Temperature Oxide) film, or a silicon nitride film, to have a relatively small thickness of approximately 5 to 200 nm.

[0078]Further, the first interlayer insulating film 41 is made of, for example, NSG. Alternatively, the first interlayer insulating film 41 may be made of silicate glass, such as PSG (phosphorus silicate glass), BSG (boron silicate glass), BPSG (boron phosphorus silicate glass), a silicon nitride, a silicon oxide, or the like.

Configuration of Fourth Layer - Data Line and the like

[0079]The fourth layer has the data lines 6a, the relay layer 6a1 for a capacitor wiring line, and the second relay electrode 6a2. Each of the data lines 6a has a two-layered structure of an aluminum film and a titanium nitride film, and the surface thereof is covered with a silicon nitride film. The data line 6a is electrically connected to the heavily-doped source region 1d of the TFT 30 via a contact hole 81 passing through the first and second interlayer insulating films 41 and 42. In addition, on the fourth layer, the relay layer 6a1 for a capacitor wiring line and the second relay electrode 6a2 are formed as the same film as that of the data line 6a.

[0080]Further, the second interlayer insulating film 42 is made of, for example, NSG. Alternatively, the second interlayer insulating film 42 may be made of silicate glass, such as PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like.

Configuration of Fifth Layer - Capacitor Wiring Line and the like

[0081]The fifth layer has the capacitor wiring lines 400 and the third relay electrode 402. Each of the capacitor wiring lines 400 extends to reach the periphery of the image display region 10a, and is electrically connected to a constant voltage source, from which power is supplied to a peripheral driving circuit or a counter electrode potential is supplied to a counter substrate via the vertical connecting terminal, such that the capacitor wiring line 400 has a constant potential. Further, the capacitor wiring line 400 is electrically connected to the relay layer 6a1 for a capacitor wiring line via the contact hole 803 formed in the third interlayer insulating film 43. The capacitor wiring line 400 has a two-layered structure of, for example, an aluminum film and a titanium nitride film.

[0082]The capacitor wiring line 400 has a lattice pattern extending in the X and Y directions, as shown in Fig. 7. A part of the capacitor wiring line 400 extending in the X direction is provided with a notch portion in order to ensure a region for forming the third relay electrode 402. Further, the capacitor wiring line 400 has a width larger than those of the lower data line 6a, the scanning line 11a, and the TFT 30, such that the capacitor wiring line 400 can function as a

light-shielding film and cover those circuit elements, thereby finally defining a non-opening region. In addition, on the fifth layer, the third relay electrode 402 is formed as the same film as that of the data line 6a.

[0083]Below the fifth layer, the third interlayer insulating film 43 is formed over the entire surface thereof. The third interlayer insulating film 43 is made of, for example, silicate glass, such as NSG, PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like. Further, the surface of the third interlayer insulating film 43 may be planarized by a CMP (Chemical Mechanical Polishing) treatment or a planarizing film formed by an SOG (Spin On Glass) treatment. With the planarization, cracks caused by a step difference between wiring lines can be prevented.

Configuration of Sixth Layer - Pixel Electrode and the like

[0084]The fourth interlayer insulating film 44 is formed on the entire surface of the fifth layer, and the pixel electrodes 9a are formed thereon as the sixth layer. In the fourth interlayer insulating film 44, a contact hole 89 is formed to electrically connect the pixel electrode 9a and the third relay electrode 402. The fourth interlayer insulating film 43 is made of, for example, silicate glass, such as NSG, PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like. Further, the surface of the fourth interlayer insulating film 44 may be planarized by the CMP treatment or a planarizing film formed by the SOG treatment. With the planarization, cracks caused by a step

difference between wiring lines can be prevented.

[0085] Each of the pixel electrodes 9a (indicated by a dotted line 9a' in Fig. 7) is disposed to approximately correspond to each of the pixel regions partitioned vertically and horizontally. The pixel electrode 9a is made of, for example, a transparent conductive film, such as ITO (Indium Tin Oxide). Further, an alignment film 16 is formed on the pixel electrode 9a. Until now, the configuration of the pixel unit on the TFT array substrate 10 has been described.

[0086] Further, with respect to the counter substrate 20, the counter electrode 21 is provided on the entire surface thereof facing the TFT array substrate 10, and an alignment film 22 is formed thereon (below the counter electrode 21 in Fig. 8). The counter electrode 21 is made of, for example, a transparent conductive film, such as ITO, in the same manner as the pixel electrode 9a. Between the counter substrate 20 and the counter electrode 21, a light-shielding film 23 for covering at least a region facing the TFT 30 is provided to prevent optical leakage current from being generated.

[0087] In the present embodiment, the extending portion 201 is formed on the extension of such a laminated structure constituting the image display region 10a. That is, in the extending portion 201, the lead wiring lines 103a are formed in the fourth layer as the same film as that of the data line 6a, and the external connecting terminals 102a are formed in the fifth layer as the same film as that of the capacitor wiring line 400. For this reason, a laminated structure shown in Fig. 5, in which the lead wiring lines 103a and the external connecting

terminals 102a are laminated with the interlayer insulating film interposed therebetween, does not need to be provided separately from the laminated structure constituting the image display region 10a. Therefore, the structure on the TFT array substrate 10 can be simplified and relatively easily formed.

[0088] In addition, in the present embodiment, since both the fourth and fifth layers contain aluminum, the data lines 6a and the capacitor wiring lines 400 have low resistance, and the lead wiring lines 103a and the external connecting terminals 102a have low resistance. Since the fourth and fifth layers are disposed above the storage capacitor 70 or the TFT 30, which requires a heat treatment, aluminum having low thermal resistance can be used. Here, by providing the lead wiring lines 103a and the external connecting terminals 102a in the fourth and fifth layers of the laminated structure constituting the image display region 10a, the wiring lines can have low resistance and the exposed surface D of each of the external connecting terminals 102a can be easily formed.

Modification

[0089] Next, a liquid crystal device according to a modification of the first embodiment will be described with reference to Figs. 9 and 10. Fig. 9 shows main parts of the extending portion in the liquid crystal device according to the modification of the first embodiment on a magnified scale. Fig. 10 is a cross-sectional view taken along the line X-X of Fig. 9.

[0090] Preferably, the lead wiring lines and the external connecting

terminals according to the invention are arranged to partially overlap each other in plan view, and various modifications can be made, in addition to the arrangement of the first embodiment.

[0091]Fig. 9 shows an example of such modifications. In Fig. 9, a plurality of external connecting terminals 102b are arranged in one direction and are connected to external connecting terminals 103b via contact holes 20b. Each of the contact holes 20b is provided in each of the regions where the plurality of lead wiring lines 103b and the plurality of external connecting terminals 102b intersect each other in plan view.

[0092]With such an arrangement, since the lead wiring lines 103a are connected to the external connecting terminals 102a in the regions where the lead wiring lines 103a extend, separate regions for forming contact holes do not need to be prepared, such that a space where the lead wiring lines and the external connecting terminals are arranged can be made smaller than that in the first embodiment (see Figs. 5 and 10). Therefore, in the modification, the width of the extending portion can be further reduced, so that the size of the TFT array substrate 10 can be further reduced.

Second Embodiment

[0093]Next, a liquid crystal device according to a second embodiment will be described with reference to Figs. 11 to 13. Fig. 11 shows the schematic configuration of the liquid crystal device according to the present embodiment, Fig. 12 shows main parts of an extending portion in

the liquid crystal device according to the second embodiment on a magnified scale, and Fig. 13 is a cross-sectional view taken along the line XIII-XIII of Fig. 12. In addition, the liquid crystal device 100A has the same configuration as the liquid crystal device 100, except that the arrangement within the extending portion is different. Therefore, the same parts as those in the liquid crystal device 100 are denoted by the same reference numerals and the detailed descriptions thereof will be omitted.

[0094]In Fig. 11, in the liquid crystal device 100A, a data line driving circuit 101c and lead wiring lines 103c are disposed to overlap a plurality of external connecting terminals 102c, which are arranged along the outer edge of an extending portion 202, in plan view. With the design of the layout of the extending portion 202, the width L12 of the extending portion 202 can be made narrow to thereby reduce the size of the TFT array substrate 10, such that the same effects as those in the first embodiment can be obtained.

[0095]Figs. 12 and 13 show that mode on a magnified scale. The lead wiring lines 103c are connected to the external connecting terminals 102c via contact holes 20c provided in regions where the lead wiring lines 103c and the external connecting terminals 102c intersect each other, in the same manner as that in the modification of the first embodiment. On the other hand, each of the lead wiring lines 103c is connected to the data line driving circuit 101c via the contact hole 21c provided in a region where each of the lead wiring lines 103c extends.

[0096]Here, in a structure laminated on the TFT array substrate 10, the

lead wiring lines 103c are provided in the fourth layer, the external connecting terminals 102c are provided in the fifth layer, and the contact holes 20c are provided to pass through the interlayer insulating film 43. The data line driving circuit 101c is provided in at least one (second and fourth layers in the range shown in the drawing) of the first to fifth layers, and the contact holes 20c are provided to pass through the interlayer insulating films 41 and 42.

[0097] In the present embodiment, the external connecting terminals 102c and the lead wiring lines 103c are formed as the same film as the conductive film for the data line driving circuit 101c or a circuit unit in the image display region 10a or are formed as a part of the same film as the conductive film, so that the structure on the TFT array substrate 10 can be simplified and relatively easily formed. Other advantages and effects of the second embodiment are the same as those of the first embodiment, and the modification of the first embodiment can also be made in the present embodiment.

[0098] Further, though the external connecting terminals 102c and the lead wiring lines 103c overlap each other in plan view and the external connecting terminals 102c and the data line driving circuit 101c overlap each other in plan view in the second embodiment, the width of the extending portion can be reduced in a layout in which only the data line driving circuit overlaps the external connecting terminals, as shown in Fig. 14, and thus the effects of the invention can be obtained.

Electronic Apparatus

[0099]Next, a case in which the above-described liquid crystal device is applied to an electronic apparatus will be described with reference to Fig. 15. Here, a projector which uses the liquid crystal device 100 as a light valve will be described as an example of the electronic apparatus according to the invention. Fig. 15 shows an example of a configuration of the projector.

[00100] In Fig. 15, a liquid crystal projector 1100 includes a lamp unit 1102 having a white light source, such as a halogen lamp. Projection light emitted from the lamp unit 1102 is separated into light components of three primary colors of R (red), G (green), and B (blue) by three mirrors 1106 and two dichroic mirrors 1108, and the light components of three primary colors are incident on liquid crystal devices 100R, 100G, and 100B, serving as light valves, corresponding to the respective colors of R, G, and B. The configurations of each of the liquid crystal devices 100R, 100G, and 100B is the same as that of the above-described liquid crystal device, and three primary color signals supplied from an image signal processing circuit are modulated by the liquid crystal devices 100R, 100G, and 100B, respectively. The light components of three primary colors modulated by the liquid crystal devices 100R, 100G, and 100B are incident on a dichroic prism 1112 from three directions. Then, images, each having one of the light components for three primary colors, are synthesized, such that a color image is projected onto a screen 1120 through a projection lens 1114.

[00101] In addition, the electro-optical device according to the invention may be implemented as an organic EL device, an electrophoretic

device, such as an electronic paper or the like, a display device using an electron emission element (Field Emission Display and Surface-Conduction Electron-Emitter Display), and the like, in addition to the above-described liquid crystal device.

[00102] Further, the electro-optical device according to the invention can be applied to various electronic apparatuses, such as a television receiver, a viewfinder-type or monitor-direct-view-type video tape recorder, a car navigation device, a pager, an electronic organizer, an electronic calculator, a word processor, a workstation, a video phone, a POS terminal, a device having a touch panel, and the like, in addition to the above-described projector.

[00103] It should be understood that the invention is not limited to the above-described embodiments and examples, but various modifications can be made within the scope without departing from the subject matter or spirit of the invention defined by the appended claims and the entire specification. Therefore, an electro-optical device and an electronic apparatus having such an electro-optical device that accompany such modifications still fall within the technical scope of the invention.

What is claimed is:

1. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

2. The electro-optical device according to Claim 1,

wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween,

the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and

the lead wiring lines have the same film as a second conductive

film constituting the circuit unit.

3. The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

4. The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

5. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

6. The electro-optical device according to Claim 5,

wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and

at least a part of the driving circuit overlaps the external connecting terminals in plan view.

7. The electro-optical device according to Claim 5,

wherein the external connecting terminals and the part of the circuit unit are laminated with an interlayer insulating film interposed therebetween, and

the external connecting terminals have the same film as a first conductive film constituting the circuit unit.

8. The electro-optical device according to Claim 1, further

comprising:

a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and

an electro-optical material that is held in the internal space,

wherein the display electrodes and a part of the circuit unit are disposed to face the internal space. .

9. An electronic apparatus comprising the electro-optical device according to Claim 1.

ABSTRACT

An electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit or the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

PATENT APPLICATION SERIAL NO _____

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FEE RECORD SHEET

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APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	9 minus 20 =	* 0	X$ 25 =		OR	X$50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X100 =			X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1000

APPLICATION AS AMENDED – PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: New U.S. Patent Application

Filed: September 13, 2005 Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please consider the following:

Amendments to the Specification;

Remarks.

Amendments to the Specification:

Attached are a marked-up copy of the originally filed specification and a clean substitute specification in accordance with 37 C.F.R. §§1.121(b)(3) and 1.125(c). The substitute specification contains no new matter.

REMARKS

Claims 1 - 9 are pending in this application. By this Amendment, a substitute specification is provided. Prompt and favorable consideration on the merits is respectfully requested.

Respectfully submitted,

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Date: September 13, 2005

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ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

BACKGROUND

This application claims the benefit of Japanese Patent Application No. 2004-328982 filed November 12, 2004. The entire disclosure of the prior application is hereby incorporated by reference herein its entirety.

1. Technical Field

[0001] The present invention relates to an electro-optical device, such as a liquid crystal device or the like, and to an electronic apparatus, such as a liquid crystal projector or the like, having such an electro-optical device.

2. Related Art

[0002] In such an electro-optical device, a substrate, on which display electrodes and a circuit unit for driving the display electrodes are provided, and a counter substrate are disposed to face each other with an electro-optical material, such as liquid crystal, interposed therebetween. More specifically, the substrates are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of the substrates are bonded to each other by a sealant so as to form an internal space, and the electro-optical material is sealed in the internal space.

[0003] The substrate provided with the display electrodes extends from

the counter substrate on one side in plan view, and external connecting terminals are provided in a portion extending on one side (hereinafter, referred to as an extending portion). The external connecting terminals are connected to wiring lines led from a circuit unit and the like, and are provided such that surfaces thereof are exposed to the outside so as to be supplied with signals or power from the outside. In addition, a driving circuit, which is connected to the external connecting terminals for supplying image signals, is generally provided in the extending portion.

[0004]In contrast, for example, as disclosed in JP-A-9-113906, according to a configuration in which a driving circuit is disposed in the internal space and only external connecting terminals are provided in the extending portion, the width of the extending portion can be made narrow, and thus the size of the substrate can be reduced.

[0005]However, in an actual electro-optical device, it is difficult to provide a space sufficient to dispose the driving circuit and to lead the wiring lines from the driving circuit in the internal space. Further, even when only the external connecting terminals are provided in the extending portion, at least some of the lead wiring lines connected to the external connecting terminals is substantially disposed in the extending portion. For this reason, in order to reduce the width of the extending portion, the layout of the external connecting terminals and the lead wiring lines needs to be considered.

SUMMARY

[0006]An advantage of some aspects of the invention is that it provides an electro-optical device which can reduce the size of a substrate and an electronic apparatus having such an electro-optical device.

[0007]According to a first aspect of the invention, an electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit or the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

[0008]In accordance with the first aspect of the invention, the pair of substrates are disposed to face each other with a predetermined gap therebetween and one substrate extends from the other substrate on at least one side. On one substrate extending from the other substrate of the pair of substrates, for example, wiring lines, such as scanning lines, data lines, and the like, electronic elements, such as thin film transistors (hereinafter, referred to as a "TFTs") and the like, and the

circuit unit that drives display electrodes by means of a data line driving circuit or a scanning line driving circuit are provided. The display electrodes are formed on an upper layer of one substrate.

[0009]Further, in the extending portion extending the other substrate on the one side, the external connecting terminals, which are electrically connected to the circuit unit, are provided. A plurality of external connecting terminals are arranged, for example, along an outer edge of the extending portion, and are correspondingly connected to the lead wiring lines, which are led from the circuit unit or the display electrodes. The lead wiring lines are generally relayed in a region other than a region where the external connecting terminals are arranged.

[0010]In the extending portion of the first aspect of the invention, the external connecting terminals and the lead wiring lines are arranged to at least partially overlap each other in plan view (that is, in a three-dimensional manner in the extending portion). Such a configuration is implemented by electrically connecting at least some of the lead wiring lines and the external connecting terminals to each other via contact holes or the like, for example, and by laminating them with an interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0011]As such, with the design of the layout, the width of the extending portion in the extension direction thereof can be reduced. As a result,

with the reduced size of the substrate, the space of the electro-optical device can be saved. In particular, the number of electro-optical devices which can be manufactured per one wafer can be increased, such that considerable effects for reduction of manufacturing costs and enhancement of manufacturing efficiency are shown. For example, even when the reduced size for one substrate is relatively small, for example, 1 mm or so, if several substrates to several tens or hundreds of substrates are arranged on the same wafer, there is a case in which one row or a plurality of rows of electro-optical devices can be further manufactured on the same wafer. Therefore, it is markedly advantageous in practice.

[0012]In the electro-optical device of the first aspect of the invention, it is preferable that the external connecting terminals and the lead wiring lines be laminated with an interlayer insulating film interposed therebetween, the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and the lead wiring lines have the same film as a second conductive film constituting the circuit unit.

[0013]According to this configuration, the external connecting terminals and the lead wiring lines are formed with different conductive films laminated with an interlayer insulating film interposed therebetween. Therefore, the external connecting terminals and the lead wiring lines can be constituted so as to overlap in plan view but not to be electrically connected to each other in portions other than portions where connected each other via contact holes or the like.

[0014]Further, the external connecting terminals and the lead wiring lines are formed as the same film as a conductive film constituting the circuit unit or to include the same film as such a conductive film, such that the laminate structure of the external connecting terminals and the lead wiring lines does not need to be prepared separately from the circuit unit. Therefore, the structure on the substrate can be simplified and be relatively easily formed. Moreover, as a material of the conductive film, for example, aluminum (Al) having low resistance is suitably used.

[0015]Further, in the electro-optical device of the first aspect of the invention, it is preferable that the plurality of external connecting terminals be arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and be connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

[0016]According to this configuration, the plurality of lead wiring lines extend in the direction in which the plurality of external connecting terminals are arranged, such that the external connecting terminals and the lead wiring lines intersect each other in a three-dimensional manner. The external connecting terminals and the lead wiring lines are connected, for example, via contact holes at the edges of the external connecting terminals (that is, the edges of the external connecting terminals on an outer edge side and an inner edge side) in the direction intersecting the direction along the one side. According to such a layout, the lead wiring lines can be efficiently arranged in a

region where the external connecting terminals are formed. Further, since the lead wiring lines are connected to the external connecting terminals in a region distant from the region where the lead wiring lines extend, such that the external connecting terminals and other lead wiring lines adjacent to the lead wiring lines to be originally connected to the external connecting terminals can be prevented from being electrically connected to each other due to an error in formation location of the contact hole, for example. Therefore, the liquid crystal device according to the above-described configuration can be manufactured with high reliability.

[0017]Further, in the electro-optical device of the first aspect of the invention, it is preferable that the plurality of external connecting terminals be arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and be correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

[0018]According to this configuration, the external connecting terminals and the lead wiring lines are correspondingly connected to each other via contact holes, for example, in the region where they intersect each other in plan view. With such a layout, the lead wiring lines can be efficiently arranged in the region where the external connecting terminals are formed, and the lead wiring lines are correspondingly connected to the external connecting terminals in the region where the lead wiring lines extend. Therefore, the regions for forming the

contact holes do not need to be separately prepared, and thus the arrangement space of the lead wiring lines and the external connecting terminals can be made small. As a result, according to the above-described configuration, the width in the direction in which the extending portion extends can be further reduced, and thus the size of the substrate can be further reduced.

[0019]Further, according to a second aspect of the invention, an electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

[0020]In accordance with the second aspect of the invention, in the extending portion, the circuit unit and the external connecting terminals are disposed to at least partially overlap each other in plan view. Such a configuration can be implemented by laminating the circuit unit and at least some of the external connecting terminals with an

interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0021]As such, with the design of the layout, the width of the extending portion in the extending direction thereof can be reduced. As a result, with the reduced size of the substrate, the same effects as those in the electro-optical device according to the first aspect of the invention can be obtained.

[0022]In the electro-optical device of the second aspect of the invention, it is preferable that the circuit unit be electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and have a driving circuit, which is driven by the supplied image signal, and at least a part of the driving circuit overlap the external connecting terminals in plan view.

[0023]According to this configuration, the driving circuit, that is, a so-called data line driving circuit is disposed to at least partially overlap the external connecting terminals in plan view. In general, the data line driving circuit is provided to extend along the one side and is connected to the external connecting terminals via the lead wiring lines, such that image signals can be supplied to both ends thereof. For this reason, since a region sufficient to arrange the plurality of lead wiring lines around the data line driving circuit is required, there are many cases in which the data line driving circuit is provided in the extending portion having little spatial restriction, together

with the external connecting terminals. In this case, the external connecting terminals and the data line driving circuit are generally provided on the same plane, so that the width of the extending portion becomes large according to the size, the shape, and the like of the data line driving circuit.

[0024]In contrast, in the invention, since the entire data line driving circuit provided in the extending portion or at least a part thereof, and the external connecting terminals are provided in the same space, the width of the extending portion can be reduced, and thus the space of the electro-optical device can be effectively saved or the size of the electro-optical device can be effectively reduced.

[0025]Further, in the electro-optical device of the second aspect of the invention, it is preferable that the external connecting terminals and the part of the circuit unit be laminated with an interlayer insulating film interposed therebetween, and the external connecting terminals have the same film as a first conductive film constituting the circuit unit.

[0026]According to this configuration, since the external connecting terminals and the circuit unit are laminated with the interlayer insulating film interposed therebetween, the external connecting terminals and the circuit unit can overlap in plan view but can not be electrically connected to each other. In addition, the external connecting terminals are formed as the same film as the conductive film constituting the circuit unit or to include the same film as the conductive film, so that the structure on the substrate can be simplified and relatively easily formed. Moreover, as a material of the

conductive film, for example, aluminum (Al) having low resistance is suitably used.

[0027]The electro-optical device of the first aspect of the invention may further include a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates, and an electro-optical material that is held in the internal space. In addition, it is preferable that the display electrodes and the part of the circuit unit be disposed to face the internal space.

[0028]According to this configuration, the edges of the opposite surfaces of the pair of substrates are bonded to each other by the sealant so as to form the internal space therebetween, and the extending portion extends from the edges. The electro-optical material, such as liquid crystal, is sealed into the internal space. The display electrodes are disposed to face the internal space. Further, a part of the circuit unit, for example, wiring lines or elements, such as scanning lines, data lines, TFTs, and the like, and a driving circuit, such as a scanning line driving circuit or the like, is provided in the region facing the internal space, together with the display electrodes. Therefore, almost the entire area of the extending portion can be used for forming the external connecting terminals.

[0029]According to a third aspect of the invention, an electronic apparatus includes the above-described electro-optical device (including various configurations).

[0030]According to this configuration, since the electronic apparatus

includes the above-described electro-optical device, various electronic apparatuses, such as a projection type display device, a liquid crystal television, a cellular phone, an electronic organizer, a word processor, a viewfinder-type or monitor-direct-view-type video tape recorder, a workstation, a video phone, a POS terminal, a touch panel, and the like, which are saved in space and reduced in size, can be implemented. In addition, for example, an electrophoretic device, such as an electronic paper, can be implemented as the electronic apparatus according to the third aspect of the invention.

[0031]Such effects and other advantages of the invention will be apparent from the following embodiments to be described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]The invention will be described with reference to the accompanying drawings, wherein like numbers reference like elements.

[0033]Fig. 1 is a plan view showing a configuration of a liquid crystal device according to a first embodiment of the invention.

[0034]Fig. 2 is a cross-sectional view showing the liquid crystal device taken along the line II-II of Fig. 1.

[0035]Fig. 3 is a plan view showing a comparative example of the liquid crystal device according to the first embodiment.

[0036]Fig. 4 is a plan view showing a configuration of main parts of the liquid crystal device according to the first embodiment.

[0037]Fig. 5 is a cross-sectional view showing an extending portion

taken along the line V-V of Fig. 4.

[0038]Fig. 6 is a schematic view showing an equivalent circuit in an image display region of the liquid crystal device according to the first embodiment.

[0039]Fig. 7 is a plan view showing a configuration of the image display region of the liquid crystal device according to the first embodiment.

[0040]Fig. 8A is a cross-sectional view showing the configuration of the image display region of the liquid crystal device according to the first embodiment taken along the line VIIIA-VIIIA of Fig. 7.

[0041]Fig. 8B is a cross-sectional view showing the configuration of the image display region of the liquid crystal device according to the first embodiment taken along the line VIIIB-VIIIB of Fig. 7.

[0042]Fig. 9 is a plan view showing a modification of the liquid crystal device according to the first embodiment.

[0043]Fig. 10 is a cross-sectional view showing the extending portion taken along the line X-X of Fig. 9.

[0044]Fig. 11 is a plan view showing a configuration of a liquid crystal device according to a second embodiment.

[0045]Fig. 12 is a plan view showing a configuration of main parts of the liquid crystal device according to the second embodiment.

[0046]Fig. 13 is a cross-sectional view showing an extending portion taken along the line XIII-XIII of Fig. 12.

[0047]Fig. 14 is a plan view showing a modification of the liquid crystal device according to the second embodiment.

[0048]Fig. 15 is a cross-sectional view showing a configuration of a

liquid crystal projector according to an embodiment of an electronic apparatus of the invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0049]Hereinafter, embodiments of the invention will be described with reference to the drawings.

Embodiments of Electro-Optical Device

[0050]The embodiments of the invention will be described with reference to Figs. 1 to 13. In the embodiments to be described below, the electro-optical device of the invention is applied to a liquid crystal device.

First Embodiment

[0051]A liquid crystal device according to a first embodiment of the invention will be described with reference to Figs. 1 to 7.

Schematic Configuration of Liquid Crystal Device

[0052]First, the schematic configuration of a liquid crystal device will be described with reference to Figs. 1 to 3. Fig. 1 is a plan view showing the configuration of a liquid crystal device according to the present embodiment, and Fig. 2 is a cross-sectional view taken along the line II-II of Fig. 1. Fig. 3 shows a comparative example of the liquid crystal device according to the present embodiment.

[0053]Referring to Figs. 1 and 2, in the liquid crystal device 100, a TFT array substrate 10 and a counter substrate 20 are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of both substrates are bonded to each other by a sealant 52a so as to form an internal space. The TFT array substrate 10 has an extending portion 201 which extends from the counter substrate 20 on one side in plan view, and the sealant 52a defines openings which lead to the internal space at predetermined places of a side where the extending portion 201 extends (here, both ends of the side). Further, a liquid crystal layer 50 is formed by injecting liquid crystal into the internal space through the openings, and the openings are sealed with sealing mold materials 151a and 151b. A frame light-shielding film 53, which is provided along an inner edge of the sealant 52a, defines an image display region 10a on which images are displayed.

[0054]On the image display region 10a of a surface (top surface in Fig. 2) of the TFT array substrate 10 facing the counter substrate 20, pixel electrodes 9a, which are examples of 'display electrodes' of the invention, are provided on switching TFTs or wiring lines, such as scanning lines, data lines, and the like. In addition, an alignment film is formed just above the pixel electrodes 9a. On a surface (bottom surface in Fig. 2) of the counter substrate 20 facing the TFT array substrate 10, a counter electrode 21 is formed via a stripe-shaped light-shielding film 23, and an alignment film is formed on the counter electrode 21. Further, in at least one corner portion (here, all of four corner portions) of the counter substrate 20, vertical connecting

terminals 106 for electrically connecting the counter substrate 20 and the TFT array substrate 10 are provided. The alignment state of liquid crystal of the liquid crystal layer 50 changes according to the electric field applied between the pixel electrodes 9a and the counter electrode 21, but liquid crystal of the liquid crystal layer 50 maintains an initial alignment state defined by the alignment films when the electric field is not applied.

[0055]In a region of the surface of the TFT array substrate 10 facing the counter substrate 20 which corresponds to a region where the frame light-shielding film 53 is formed, scanning line driving circuits 104 for driving scanning lines, and wiring lines 105 are provided. In Fig. 1, two scanning line driving circuits 104 are provided on left and right sides the frame light-shielding film 53. The wiring lines 105 are relayed on the upper side of the frame light-shielding film 53 so as to connect the two scanning line driving circuits 104.

[0056]The extending portion 201 of the TFT array substrate 10 is provided with a data line driving circuit 101a for driving data lines, which is a specified example of 'driving circuit' of the invention, along a lower side of the sealant 52a in Fig. 1. The upper half of the data line driving circuit 101a overlaps the sealant 52a in plan view. Further, the lower half of the data line driving circuit 101a overlaps portions pushed from the openings of the sealing mold materials 151a and 151b at both ends thereof.

[0057]Moreover, in the present embodiment, all of electronic elements, such as TFTs or the like, the wiring lines, such as scanning lines, data

lines, and the like, and circuits on the TFT array substrate 10 including the scanning line driving circuits 104 and the data line driving circuit 101a correspond to a specified example of 'circuit unit' of the invention. Further, the extending portion 201 may be further provided with a sampling circuit that applies image signals to a plurality of data lines with a predetermined timing, a precharge circuit that supplies a precharge signal having a predetermined voltage level to the plurality of data lines prior to the image signals, and a test circuit that tests quality, defects, or the like of the liquid crystal device 100 during manufacture or at the time of shipping.

[0058]Further, in the present embodiment, at least some of a plurality of lead wiring lines 103a in the extending portion 201 is provided to overlap external connecting terminals 102a in plan view. Specifically, in the liquid crystal device 100, a layer where the external connecting terminals 102a are formed and a layer where the lead wiring lines 103a are formed are laminated with, for example, an interlayer insulating film interposed therebetween, and the formation region of the external connecting terminals 102a and the formation region of the lead wiring lines 103a at least partially overlap each other. Two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure.

[0059]The external connecting terminals 102a are provided so as to supply power or signals to the liquid crystal device 100 from an external circuit, which is connected thereto via an FPC 110. The

external connecting terminals 102a are properly connected to the driving circuit, such as the scanning circuit driving circuits 104 or the data line driving circuit 101a, via the lead wiring lines 103a. In the liquid crystal device 100, the pixel electrodes 9a are driven by signals inputted to the external connecting terminals 102a from the outside, such that images are displayed. Here, the data line driving circuit 101a is connected to the plurality of external connecting terminals 102a through the lead wiring lines 103a at both ends of the extending portion 201.

[0060]As shown in Fig. 3, in a liquid crystal device according to a comparative example of the present embodiment, external connecting terminals 102 and lead wiring lines 103 are disposed on the same plane so as not to overlap each other in plan view. In addition, the external connecting terminals 102 must be connected to the FPC 110, and thus a sealant 150 does not overlap the external connecting terminals 102. Accordingly, the external connecting terminals 102a need to be disposed away from the sealant 150 to some extent. As a result, an extending portion 200 has a predetermined width L0 and has a space, such that a space for disposing the entire data line driving circuit 101 is generated.

[0061]In contrast, in the liquid crystal device 100 of the present embodiment, as described above, at least some of the plurality of lead wiring lines 103a are disposed to overlap the external connecting terminals 102a in plan view, so that a space can be saved. In particular, since the external connecting terminals 102a are arranged

along an outer edge of the extending portion 201, the width L11 of the extending portion 201 in the extending direction can be reduced further than the related art.

[0062]Further, in the liquid crystal device 100 of the present embodiment, since the external connecting terminals 102a are arranged in a region between the sealing mold materials 151a and 151b, the external connecting terminals 102a do not need to be provided distant from and the sealing mold materials 151a and 151b. In addition, in Fig. 1, the positions of the external connecting terminals 102a can be moved upward by disposing the upper half of the data line driving circuit 101a in a region where the sealant 52a is provided. As a result, the width L11 of the extending portion 201 can be further reduced than the width L0 of the extending portion 200 in the comparative example.

[0063]As such, the space can be saved in the liquid crystal device 100 of the present embodiment, and thus an electronic apparatus, to which the liquid crystal device 100 is applied, can have a high degree of freedom in terms of design. Further, the number of liquid crystal devices which can be manufactured per one wafer can be increased, and considerable effects for reduction of manufacturing costs and enhancement of manufacturing efficiency are shown. That is, even though the reduced width of the extending portion 201 in one liquid crystal device 100 is small, several hundreds or thousands of regions, each corresponding to the TFT array substrate 10, are generally formed on the wafer and a large number of such wafers are manufactured. Therefore, it is very effective for manufacture.

[0064]Here, on the lower side of the sealant 52a or the lower side of the counter substrate 20, the openings and the sealing mold materials 150a and 150b are disposed at the ends thereof and the external connecting terminals 102a are arranged at a central portion thereof. Therefore, even when the lead wiring lines 103a are divided into the left and right sides, the lengths of the lead wiring lines 103a can be approximately equal one left and right sides, such that a failure, such as a signal delay between the left and right sides, does not occur. Further, the openings are disposed at the left and right ends, so that liquid crystal can be injected into the internal space efficiently and uniformly.

Configuration of Extending Portion

[0065]Next, referring to Figs. 4 to 7, a specified configuration of the extending portion 201 in the liquid crystal device 100 will be described in detail. Fig. 4 shows main parts of the extending portion in the liquid crystal device according to the present embodiment on a magnified scale. Fig. 5 is a cross-sectional view taken along the line V-V of Fig. 4. Fig. 6 shows an equivalent circuit constituted by a pixel unit in an image display region of the liquid crystal device according to the present embodiment. Fig. 7 is a plan view showing the configuration of the pixel unit. Figs. 8A and 8B are cross-sectional views showing the configuration of the pixel unit. Specifically, Fig. 8A is a cross-sectional view taken along the line VIIIA-VIIIA of Fig. 7, and Fig. 8B is a cross-sectional view taken along the line VIIIB-VIIIB of Fig. 7.

In Figs. 8A and 8B, the scale of each layer or each member has been adjusted in order to have a recognizable size.

[0066]In Fig. 4, the plurality of external connecting terminals 102a are arranged in one direction, and the plurality of lead wiring lines 103a extend in the direction in which the external connecting terminals 102a are arranged and are connected to the external connecting terminals 102a via contact holes 20a. The plurality of contact holes 20a are provided at the outer edges of the plurality of external connecting terminals 102a. Alternatively, all or some of the contact holes 20a may be provided at the inner edges of the plurality of external connecting terminals 102a.

[0067]According to such a layout, the lead wiring lines 103a are connected to the external connecting terminals 102a in a region distant from a region where the lead wiring lines 103a extend, so that the external connecting terminals 102a and other lead wiring lines 103a adjacent to the lead wiring lines 103a to be originally connected to the external connecting terminals 102a can be prevented from being electrically connected to each other due to an error in formation location of the contact hole 20a, for example. Therefore, the liquid crystal device 100 can be manufactured with high reliability.

[0068]In Fig. 5, the external connecting terminals 102a and the lead wiring lines 103 are laminated with an interlayer insulating film 43 interposed therebetween. Further, the contact holes 20a are formed to pass through the interlayer insulating film 43. Each of the lead wiring lines 103a is connected to a desired external connecting terminal 102a

via the contact hole 20a but is electrically isolated from other external connecting terminals 102a by means of the interlayer insulating film 43, so that the lead wiring lines 103a overlap the external connecting terminals 102a in plan view.

[0069]Here, a base insulating film 12 and interlayer insulating films 41, 42, 43, and 44 are laminated on the TFT array substrate 10 in that order, and the lead wiring lines 103a are provided on the interlayer insulating film 43. Here, the lead wiring line 103a and the external connecting terminal 102a each has a two-layered structure made of an aluminum layer 40A, a titanium nitride film 40TN, and an exposed surface D of each of the external connecting terminals 102a (a hatched region of each of the external connecting terminals 102a in Fig. 4) is exposed to the outside from an opening which is formed by partially removing the interlayer insulating film 44 and the titanium nitride film 40TN. A laminated structure in the image display region 10a on the TFT array substrate 10 is constituted based on the above-described laminated structure. Next, the configuration of the laminated structure in the image display region 10a will be described below.

Configuration of Image Display Region

[0070]In Fig. 6, a plurality of scanning lines 11a and a plurality of data lines 6a are arranged to intersect each other in the image display region 10a, and pixel units, each being selected by one of the plurality of scanning lines 11a and one of the plurality of data lines 6a, are formed between these lines. Each of the pixel units has a TFT 30, a

pixel electrode 9a, and a storage capacitor 70. The TFT 30 is provided to apply image signals S1, S2, …, and Sn supplied from the data lines 6a to the selected pixels. A gate of the TFT 30 is connected to the scanning line 11a, a source thereof is connected to the data line 6a, and a drain thereof is connected to the pixel electrode 9a. A liquid crystal capacitor is formed between the pixel electrode 9a and a counter electrode 21 to be described below, and the respective pixel electrodes 9a hold the input image signals S1, S2, …, and Sn for a predetermined period of time. That is, an opening region for each pixel unit is divided by each of the pixel electrodes 9a. One electrode of the storage capacitor 70 is connected to the drain of the TFT 30 in parallel with the pixel electrode 9a, and the other electrode thereof is connected to a fixed-potential capacitor wiring line 400, such that the electric potential on the other electrode can be made constant.

[0071]The liquid crystal device 100 uses a TFT active matrix driving method, for example. Specifically, in the liquid crystal device 100, scanning signals G1, G2, …, Gm are line-sequentially applied to the respective scanning lines 11a from the scanning line driving circuit 104 (see Fig. 1), and simultaneously the image signals S1, S2, …, and Sn supplied from the data line driving circuit 101 (see Fig. 1) are applied through the data lines 6a to a selected row of horizontally-arrayed pixel units in which the TFTs 30 are turned on. As a result, the image signals are supplied to the pixel electrodes 9a corresponding to the selected pixels. Since the TFT array substrate 10 is disposed to face the counter substrate 20 with the liquid crystal layer 50 interposed

therebetween (see Fig. 2), the amount of transmitted light between the substrates is controlled for each pixel by applying an electric field to the liquid crystal layer 50 for each pixel unit in such a manner, such that gray-scale display of an image is performed. At this time, the image signal held in each pixel unit is prevented from leaking by means of the storage capacitor 70.

[0072] In Figs. 7 and 8, circuit elements of the above-described pixel unit are patterned to be formed on the TFT array substrate 10 as laminated conductive films. The TFT array substrate 10 of the present embodiment is made of a quartz substrate and is disposed to face the counter substrate 20 made of a glass substrate, a quartz substrate, or the like. Further, each of the circuit elements has a first layer including the scanning line 11a, a second layer including the gate electrode 3a, a third layer including the fixed-potential capacitor electrode of the storage capacitor 70, a fourth layer including the data line 6a, a fifth layer including the capacitor wiring line 400, and a sixth layer including the pixel electrode 9a from the bottom. In addition, the base insulating film 12 is provided between the first and second layers, the first interlayer insulating film 41 is provided between the second and third layers, the second interlayer insulating film 42 is provided between the third and fourth layers, the third interlayer insulating film 43 is provided between the fourth and fifth layers, and the fourth interlayer insulating film 44 is provided between the fifth and sixth layers, such that the above-described elements can be prevented from being short-circuited.

Configuration of First Layer - Scanning Line and the like

[0073]The first layer has the scanning lines 11a. Each of the scanning lines 11a is patterned to have a main line part extending in an X direction of Fig. 7 and a protruding part extending in a Y direction of Fig. 7 in which the data lines 6a or the capacitor wiring lines 400 extend. The scanning line 11a is made of, for example, conductive polysilicon. Alternatively, the scanning line 11a may be made of a metal simplex of at least one high-melting-point metal selected from a group of titanium (Ti), chromium (Cr), tungsten (W), tantalum (Ta), molybdenum (Mo), and the like, an alloy thereof, metal silicide, polysilicide, or a laminate thereof. That is, the scanning line 11a of the present embodiment covers a region between the openings as much as possible, thereby serving as a light-shielding film which shields the TFT 30 from the lower side.

Configuration of Second Layer - TFT and the like

[0074]The second layer has the TFTs 30 and relay electrodes 719. Each of the TFTs 30 has an LDD (Lightly Doped Drain) structure, for example, and includes a gate electrode 3a, a semiconductor layer 1a, and a gate insulating film 2 for electrically isolating the gate electrode 3a from the semiconductor layer 1a. The gate insulating film 2 is made of, for example, an HTO (High Temperature Oxide) or a thermally-oxidized silicon oxide. The gate electrode 3a is made of, for example, conductive polysilicon. The semiconductor layer 1a is made of, for example,

polysilicon, and has a lightly-doped source region 1b, a lightly-doped drain region 1c, a heavily-doped source region 1d, and a heavily-doped drain region 1e. In addition, on the second layer, the relay electrodes 719 are formed as the same film as that of the gate electrode 3a.

[0075]The gate electrode 3a of the TFT 30 is electrically connected to the scanning line 11a via a contact hole 12cv formed in the base insulating film 12. The base insulating film 12 is made of a silicon oxide film, such as an HTO film or an NSG (non-silicate glass) film, electrically isolates the first layer from the second layer, and is formed on the entire surface of the TFT array substrate 10 so as to prevent element characteristics of the TFT 30 from changing due to roughness or contamination caused by the abrasion of a substrate surface.

Configuration of Third Layer - Storage Capacitor and the like

[0076]The third layer has the storage capacitors 70. Each of the storage capacitors 70 is configured such that a capacitor electrode 300 and a lower electrode 71 are disposed to face each other with a dielectric film 75 interposed therebetween. The capacitor electrode 300 is electrically connected to the capacitor wiring line 400 via contact holes 801 and 803 and a relay layer 6a1 for a capacitor wiring line. The lower electrode 71 and the heavily-doped drain region 1e are connected via a contact hole 83 formed in the first interlayer insulating film 41. Further, the lower electrode 71 and the pixel electrode 9a relay the respective layers by means of contact holes 881,

882, and 804, the relay electrode 719, a second relay electrode 6a2, and a third relay electrode 402, and are electrically connected via a contact hole 89.

[0077]The capacitor electrode 300 has a single layer made of a metal simplex of at least one high-melting-point metal selected from a group of Ti, Cr, W, Ta, Mo, and the like, an alloy thereof, metal silicide, polysilicide, or a laminate. Preferably, the capacitor electrode 300 is made of tungsten silicide, and has a function of blocking light incident on the TFT 30 from the top in Fig. 8. The lower electrode 71 is made of conductive polysilicon, for example. The dielectric film 75 is made of, for example, a silicon oxide film, such as an HTO film or an LTO (Low Temperature Oxide) film, or a silicon nitride film, to have a relatively small thickness of approximately 5 to 200 nm.

[0078]Further, the first interlayer insulating film 41 is made of, for example, NSG. Alternatively, the first interlayer insulating film 41 may be made of silicate glass, such as PSG (phosphorus silicate glass), BSG (boron silicate glass), BPSG (boron phosphorus silicate glass), a silicon nitride, a silicon oxide, or the like.

Configuration of Fourth Layer - Data Line and the like

[0079]The fourth layer has the data lines 6a, the relay layer 6a1 for a capacitor wiring line, and the second relay electrode 6a2. Each of the data lines 6a has a two-layered structure of an aluminum film and a titanium nitride film, and the surface thereof is covered with a silicon nitride film. The data line 6a is electrically connected to the

heavily-doped source region 1d of the TFT 30 via a contact hole 81 passing through the first and second interlayer insulating films 41 and 42. In addition, on the fourth layer, the relay layer 6a1 for a capacitor wiring line and the second relay electrode 6a2 are formed as the same film as that of the data line 6a.

[0080]Further, the second interlayer insulating film 42 is made of, for example, NSG. Alternatively, the second interlayer insulating film 42 may be made of silicate glass, such as PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like.

Configuration of Fifth Layer - Capacitor Wiring Line and the like

[0081]The fifth layer has the capacitor wiring lines 400 and the third relay electrode 402. Each of the capacitor wiring lines 400 extends to reach the periphery of the image display region 10a, and is electrically connected to a constant voltage source, from which power is supplied to a peripheral driving circuit or a counter electrode potential is supplied to a counter substrate via the vertical connecting terminal, such that the capacitor wiring line 400 has a constant potential. Further, the capacitor wiring line 400 is electrically connected to the relay layer 6a1 for a capacitor wiring line via the contact hole 803 formed in the third interlayer insulating film 43. The capacitor wiring line 400 has a two-layered structure of, for example, an aluminum film and a titanium nitride film.

[0082]The capacitor wiring line 400 has a lattice pattern extending in the X and Y directions, as shown in Fig. 7. A part of the capacitor

wiring line 400 extending in the X direction is provided with a notch portion in order to ensure a region for forming the third relay electrode 402. Further, the capacitor wiring line 400 has a width larger than those of the lower data line 6a, the scanning line 11a, and the TFT 30, such that the capacitor wiring line 400 can function as a light-shielding film and cover those circuit elements, thereby finally defining a non-opening region. In addition, on the fifth layer, the third relay electrode 402 is formed as the same film as that of the data line 6a.

[0083]Below the fifth layer, the third interlayer insulating film 43 is formed over the entire surface thereof. The third interlayer insulating film 43 is made of, for example, silicate glass, such as NSG, PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like. Further, the surface of the third interlayer insulating film 43 may be planarized by a CMP (Chemical Mechanical Polishing) treatment or a planarizing film formed by an SOG (Spin On Glass) treatment. With the planarization, cracks caused by a step difference between wiring lines can be prevented.

Configuration of Sixth Layer - Pixel Electrode and the like

[0084]The fourth interlayer insulating film 44 is formed on the entire surface of the fifth layer, and the pixel electrodes 9a are formed thereon as the sixth layer. In the fourth interlayer insulating film 44, a contact hole 89 is formed to electrically connect the pixel electrode 9a and the third relay electrode 402. The fourth interlayer

insulating film 43 is made of, for example, silicate glass, such as NSG, PSG, BSG, BPSG, or the like, a silicon nitride, a silicon oxide, or the like. Further, the surface of the fourth interlayer insulating film 44 may be planarized by the CMP treatment or a planarizing film formed by the SOG treatment. With the planarization, cracks caused by a step difference between wiring lines can be prevented.

[0085]Each of the pixel electrodes 9a (indicated by a dotted line 9a' in Fig. 7) is disposed to approximately correspond to each of the pixel regions partitioned vertically and horizontally. The pixel electrode 9a is made of, for example, a transparent conductive film, such as ITO (Indium Tin Oxide). Further, an alignment film 16 is formed on the pixel electrode 9a. Until now, the configuration of the pixel unit on the TFT array substrate 10 has been described.

[0086]Further, with respect to the counter substrate 20, the counter electrode 21 is provided on the entire surface thereof facing the TFT array substrate 10, and an alignment film 22 is formed thereon (below the counter electrode 21 in Fig. 8). The counter electrode 21 is made of, for example, a transparent conductive film, such as ITO, in the same manner as the pixel electrode 9a. Between the counter substrate 20 and the counter electrode 21, a light-shielding film 23 for covering at least a region facing the TFT 30 is provided to prevent optical leakage current from being generated.

[0087]In the present embodiment, the extending portion 201 is formed on the extension of such a laminated structure constituting the image display region 10a. That is, in the extending portion 201, the lead

wiring lines 103a are formed in the fourth layer as the same film as that of the data line 6a, and the external connecting terminals 102a are formed in the fifth layer as the same film as that of the capacitor wiring line 400. For this reason, a laminated structure shown in Fig. 5, in which the lead wiring lines 103a and the external connecting terminals 102a are laminated with the interlayer insulating film interposed therebetween, does not need to be provided separately from the laminated structure constituting the image display region 10a. Therefore, the structure on the TFT array substrate 10 can be simplified and relatively easily formed.

[0088]In addition, in the present embodiment, since both the fourth and fifth layers contain aluminum, the data lines 6a and the capacitor wiring lines 400 have low resistance, and the lead wiring lines 103a and the external connecting terminals 102a have low resistance. Since the fourth and fifth layers are disposed above the storage capacitor 70 or the TFT 30, which requires a heat treatment, aluminum having low thermal resistance can be used. Here, by providing the lead wiring lines 103a and the external connecting terminals 102a in the fourth and fifth layers of the laminated structure constituting the image display region 10a, the wiring lines can have low resistance and the exposed surface D of each of the external connecting terminals 102a can be easily formed.

Modification

[0089]Next, a liquid crystal device according to a modification of the first embodiment will be described with reference to Figs. 9 and 10.

Fig. 9 shows main parts of the extending portion in the liquid crystal device according to the modification of the first embodiment on a magnified scale. Fig. 10 is a cross-sectional view taken along the line X-X of Fig. 9.

[0090]Preferably, the lead wiring lines and the external connecting terminals according to the invention are arranged to partially overlap each other in plan view, and various modifications can be made, in addition to the arrangement of the first embodiment.

[0091]Fig. 9 shows an example of such modifications. In Fig. 9, a plurality of external connecting terminals 102b are arranged in one direction and are connected to external connecting terminals 103b via contact holes 20b. Each of the contact holes 20b is provided in each of the regions where the plurality of lead wiring lines 103b and the plurality of external connecting terminals 102b intersect each other in plan view.

[0092]With such an arrangement, since the lead wiring lines 103a are connected to the external connecting terminals 102a in the regions where the lead wiring lines 103a extend, separate regions for forming contact holes do not need to be prepared, such that a space where the lead wiring lines and the external connecting terminals are arranged can be made smaller than that in the first embodiment (see Figs. 5 and 10). Therefore, in the modification, the width of the extending portion can be further reduced, so that the size of the TFT array substrate 10 can be further reduced.

Second Embodiment

[0093]Next, a liquid crystal device according to a second embodiment will be described with reference to Figs. 11 to 13. Fig. 11 shows the schematic configuration of the liquid crystal device according to the present embodiment, Fig. 12 shows main parts of an extending portion in the liquid crystal device according to the second embodiment on a magnified scale, and Fig. 13 is a cross-sectional view taken along the line XIII-XIII of Fig. 12. In addition, the liquid crystal device 100A has the same configuration as the liquid crystal device 100, except that the arrangement within the extending portion is different. Therefore, the same parts as those in the liquid crystal device 100 are denoted by the same reference numerals and the detailed descriptions thereof will be omitted.

[0094]In Fig. 11, in the liquid crystal device 100A, a data line driving circuit 101c and lead wiring lines 103c are disposed to overlap a plurality of external connecting terminals 102c, which are arranged along the outer edge of an extending portion 202, in plan view. With the design of the layout of the extending portion 202, the width L12 of the extending portion 202 can be made narrow to thereby reduce the size of the TFT array substrate 10, such that the same effects as those in the first embodiment can be obtained.

[0095]Figs. 12 and 13 show that mode on a magnified scale. The lead wiring lines 103c are connected to the external connecting terminals 102c via contact holes 20c provided in regions where the lead wiring lines 103c and the external connecting terminals 102c intersect each

other, in the same manner as that in the modification of the first embodiment. On the other hand, each of the lead wiring lines 103c is connected to the data line driving circuit 101c via the contact hole 21c provided in a region where each of the lead wiring lines 103c extends.

[0096]Here, in a structure laminated on the TFT array substrate 10, the lead wiring lines 103c are provided in the fourth layer, the external connecting terminals 102c are provided in the fifth layer, and the contact holes 20c are provided to pass through the interlayer insulating film 43. The data line driving circuit 101c is provided in at least one (second and fourth layers in the range shown in the drawing) of the first to fifth layers, and the contact holes 20c are provided to pass through the interlayer insulating films 41 and 42.

[0097]In the present embodiment, the external connecting terminals 102c and the lead wiring lines 103c are formed as the same film as the conductive film for the data line driving circuit 101c or a circuit unit in the image display region 10a or are formed as a part of the same film as the conductive film, so that the structure on the TFT array substrate 10 can be simplified and relatively easily formed. Other advantages and effects of the second embodiment are the same as those of the first embodiment, and the modification of the first embodiment can also be made in the present embodiment.

[0098]Further, though the external connecting terminals 102c and the lead wiring lines 103c overlap each other in plan view and the external connecting terminals 102c and the data line driving circuit 101c overlap each other in plan view in the second embodiment, the width of the

extending portion can be reduced in a layout in which only the data line driving circuit overlaps the external connecting terminals, as shown in Fig. 14, and thus the effects of the invention can be obtained.

Electronic Apparatus

[0099]Next, a case in which the above-described liquid crystal device is applied to an electronic apparatus will be described with reference to Fig. 15. Here, a projector which uses the liquid crystal device 100 as a light valve will be described as an example of the electronic apparatus according to the invention. Fig. 15 shows an example of a configuration of the projector.

[00100] In Fig. 15, a liquid crystal projector 1100 includes a lamp unit 1102 having a white light source, such as a halogen lamp. Projection light emitted from the lamp unit 1102 is separated into light components of three primary colors of R (red), G (green), and B (blue) by three mirrors 1106 and two dichroic mirrors 1108, and the light components of three primary colors are incident on liquid crystal devices 100R, 100G, and 100B, serving as light valves, corresponding to the respective colors of R, G, and B. The configurations of each of the liquid crystal devices 100R, 100G, and 100B is the same as that of the above-described liquid crystal device, and three primary color signals supplied from an image signal processing circuit are modulated by the liquid crystal devices 100R, 100G, and 100B, respectively. The light components of three primary colors modulated by the liquid crystal devices 100R, 100G, and 100B are incident on a dichroic prism 1112 from

three directions. Then, images, each having one of the light components for three primary colors, are synthesized, such that a color image is projected onto a screen 1120 through a projection lens 1114.

[00101] In addition, the electro-optical device according to the invention may be implemented as an organic EL device, an electrophoretic device, such as an electronic paper or the like, a display device using an electron emission element (Field Emission Display and Surface-Conduction Electron-Emitter Display), and the like, in addition to the above-described liquid crystal device.

[00102] Further, the electro-optical device according to the invention can be applied to various electronic apparatuses, such as a television receiver, a viewfinder-type or monitor-direct-view-type video tape recorder, a car navigation device, a pager, an electronic organizer, an electronic calculator, a word processor, a workstation, a video phone, a POS terminal, a device having a touch panel, and the like, in addition to the above-described projector.

[00103] It should be understood that the invention is not limited to the above-described embodiments and examples, but various modifications can be made within the scope without departing from the subject matter or spirit of the invention defined by the appended claims and the entire specification. Therefore, an electro-optical device and an electronic apparatus having such an electro-optical device that accompany such modifications still fall within the technical scope of the invention.

What is claimed is:

1. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

2. The electro-optical device according to Claim 1,

wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween,

the external connecting terminals have the same film as a first conductive film constituting the circuit unit, and

the lead wiring lines have the same film as a second conductive

film constituting the circuit unit.

3. The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.

4. The electro-optical device according to Claim 1,

wherein the plurality of external connecting terminals are arranged in a direction along the one side, and

the plurality of lead wiring lines extend in the direction along the one side and are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

5. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

6. The electro-optical device according to Claim 5,

wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and

at least a part of the driving circuit overlaps the external connecting terminals in plan view.

7. The electro-optical device according to Claim 5,

wherein the external connecting terminals and the part of the circuit unit are laminated with an interlayer insulating film interposed therebetween, and

the external connecting terminals have the same film as a first conductive film constituting the circuit unit.

8. The electro-optical device according to Claim 1, further

comprising:

a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and

an electro-optical material that is held in the internal space,

wherein the display electrodes and a part of the circuit unit are disposed to face the internal space.

9. An electronic apparatus comprising the electro-optical device according to Claim 1.

ABSTRACT

An electro-optical device includes a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view, display electrodes that are provided on one substrate, a circuit unit that is provided on one substrate so as to drive the display electrodes, a plurality of lead wiring lines that are led from one of the sides of wiring lines for driving the circuit unit or the display electrodes to an extending portion extending on the one side of one substrate, and a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the plurality of lead wiring lines in plan view.

OLIFF & BERRIDGE, PLC

ATTORNEYS AT LAW

Application Data Sheet

Applicant Information

Applicant Authority type::	Inventor
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Correspondence Information

Correspondence Customer Number::	25944

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Postal or Zip Code of mailing address::		163-0811	

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masao MURADE

Application No.: New U.S. Patent Application

Filed: September 13, 2005 Docket No.: 125312

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. Relevance of the non-English language references is discussed in the present specification.

☒ 3. An English language Abstract of the non-English language reference is attached hereto.

☒ 4. A computer-generated English language translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See Reference 1.

Respectfully submitted,

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 09-113906 with abstract and translation.	05/02/1997	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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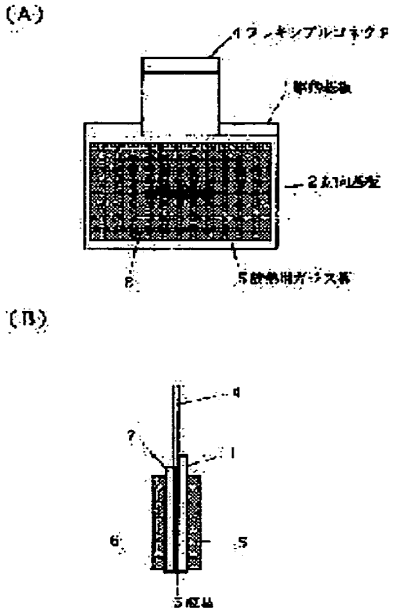
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(54) TRANSMISSION TYPE DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To enhance the cooling effect of a transmission type display device incorporated in a projector.
SOLUTION: This transmission type display device has a panel structure provided with a driving substrate 1 where a pixel electrode and a switching element are formed, a counter substrate 2 where a counter electrode is formed, and liquid crystal 3 held in a gap between both substrates 1 and 2 bonded each other, and is used for the projection display of a picture. A heat radiating glass plate 5 whose heat conductivity is ≥1W/m.K and whose thickness is ≥1mm is attached to the outer surfaces of the respective substrates 1 and 2. The heat radiating glass plate whose heat conductivity is ≥1W/m.K is may be bonded to the outer surfaces of the substrates 1 and 2 through hermetically sealed space whose void dimension is ≤2mm instead of the glass plate 5.



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CLAIMS

[Claim(s)]
[Claim 1] The transparence substrate of another side in which the pixel electrode and the switching element were formed in for while, and the transparence substrate and the counterelectrode were formed, It has the panel structure equipped with the liquid crystal held in the gap of the transparence substrate of this pair joined [each other]. The transparency mold display with which it is the transparency mold display used for the projection display of an image, and thermal conductivity is characterized by thickness pasting up the glass plate for heat dissipation 1mm or more on the external surface of one [at least] transparence substrate by 1 or more W/m-K.
[Claim 2] Said glass plate for heat dissipation is a transparency mold display according to claim 1 characterized by consisting of quartz-glass material or heat-resisting glass material.
[Claim 3] The transparence substrate of another side in which the pixel electrode and the switching element were formed in for while, and the transparence substrate and the counterelectrode were formed, It has the panel structure equipped with the liquid crystal held in the gap of the transparence substrate of this pair joined [each other]. The transparency mold display which is a transparency mold display used for the projection display of an image, and is characterized by for thermal conductivity having minded the glass plate for heat dissipation of 1 or more W/m-K, and for the opening dimension having minded a closed space 2mm or less, and joining to the external surface of one [at least] transparence substrate.
[Claim 4] Said glass plate for heat dissipation is a transparency mold display according to claim 3 characterized by forming the antireflection film in the both sides.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the transparency mold display built into a projector etc. It is related with the cooling structure of a liquid crystal panel in more detail.
[0002]
[Description of the Prior Art] With reference to drawing 4 , the structure of the conventional liquid crystal projector is explained briefly. The liquid crystal projector has the metal halide lamp 202 which is equipped with the light source 201, for example, emits a powerful light source light, and the reflecting mirror 203 of a spheroid mold. Ahead of the light source 201, the heat ray cut-off filter 204, the incidence side polarizing plate 205, and the condenser lens 206 arrange in order. Furthermore, ahead of a condenser lens 206, the liquid crystal panel 207, the outgoing radiation side polarizing plate 208, and the projection lens 209 have arranged. A powerful light source light which carried out outgoing radiation removes unnecessary infrared radiation from a metal halide lamp 202 through the heat ray cut-off filter 204. Furthermore, after passing the incidence side polarizing plate 205, it is condensed with a condenser lens 206, and incidence is carried out to a liquid crystal panel 207. After penetrating the outgoing radiation side polarizing plate 208, expansion projection is carried out with the projection lens 209, and an image copies out on a front screen etc. the light which carried out outgoing radiation from the liquid crystal panel 207. One sheet of this structure is a veneer type using the liquid crystal panel equipped with the color filter. It replaces with a veneer type and the 3 plate type which incorporated the liquid crystal panel of three sheets corresponding to the light source light of RGB three primary colors is also known.
[0003]
[Problem(s) to be Solved by the Invention] The thickness of a liquid crystal panel 207 is about 2mm, and is comparatively thin. For this reason, when nonuniformity is in light source luminous-intensity distribution, light concentrates locally, a liquid crystal panel is heated partially, and the so-called hot spot occurs. Since a perimeter differs from permeability, this hot spot spoils remarkably the grace of the image by which expansion projection was carried out. Moreover, the temperature of a liquid crystal panel rises with the radiant heat from the light source, and property degradation of liquid crystal takes place in connection with it. The liquid crystal panel used by the projector will be heated by powerful light source light, and will become an elevated temperature. It becomes impossible for a liquid crystal panel to achieve the property top display function of liquid crystal.
[0004] For the reason, by the liquid crystal projector, the device which cools a liquid crystal panel from the former is incorporated. As cooling system, the air-cooling mold and the liquid cooling mold are adopted. However, an air-cooling mold has the problem of the noise and dust adhesion. If blast weight is increased in order to acquire sufficient cooling effect, the noise will become intense by high-speed rotation of a fan. It is not suitable for the projector which appreciates a movie etc. in the quiet interior of a room. When only performing air cooling, generally, it is necessary to apply a strong low wind, the fan who uses it inevitably will also become big, and cooling effectiveness is unsuitable to a home theater. Moreover, if cooling by ventilation is performed, dust will dance within equipment, and if it adheres to a liquid crystal panel or a lens, it will become a problem in respect of image quality. On the other hand, about a liquid cooling mold, JP,6-58474,B has an indication. Since the liquid which turns into a heat exchange medium by the liquid cooling method is enclosed, problems various at the point of dependability, such as pressure omission, gassing, a mixing foreign matter, a cooling liquid spill, etc. at the time of a temperature rise, occur. Especially in the case of a water cooling type, the rust

of metal components etc. poses a problem. Moreover, in order to cool, a liquid will be so much needed, and the cooler style itself will become large-scale. Although there is also solid-state cooling system which furthermore attached thermoelectric-cooling equipments, such as a Peltier device, while the cost of the whole projector goes up sharply, it is difficult to acquire sufficient cooling effect.

[0005]

[Means for Solving the Problem] In view of the technical problem of a Prior art mentioned above, this invention aims at offering the cooling structure of a liquid crystal panel where degradation of drawing grace is not caused even if dust adheres while it is easy handling and its dependability is advantageous also in [it is high and] manufacturing cost. In order to attain this purpose, two kinds of following means were provided. According to the 1st means of this invention, as a fundamental configuration, a transparency mold indicating equipment has the panel structure which the pixel electrode and the switching element equipped with the liquid crystal held in the gap of the transparence substrate of another side in which while was formed in and the transparence substrate and the counterelectrode were formed, and the transparence substrate of this pair joined [each other], and is used for the projection display of an image. As a description matter, thickness pastes [thermal conductivity] up the glass plate for heat dissipation 1mm or more on the external surface of one [at least] transparence substrate by 1 or more W/m-K. Said glass plate for heat dissipation consists of quartz-glass material or heat-resisting glass material preferably.

[0006] According to the 2nd means of this invention, a pixel electrode and a switching element have the panel structure equipped with the liquid crystal held in the gap of the transparence substrate of another side in which while was formed in and the transparence substrate and the counterelectrode were formed, and the transparence substrate of this pair joined [each other] as a fundamental configuration, and a transparency mold indicating equipment is used for the projection display of an image. As a description matter, thermal conductivity minds the glass plate for heat dissipation of 1 or more W/m-K, an opening dimension minds a closed space 2mm or less, and it joins to the external surface of one [at least] transparence substrate. As for said glass plate for heat dissipation, the antireflection film is preferably formed in the both sides.

[0007] According to this invention, thermal conductivity carried out the high temperature conduction glass of 1 or more W/m-K to heat dissipation, and the external surface of the transparence substrate of one side or both is pasted. When the transparency mold indicating equipment which has this structure is built into a projector etc., the heat accumulated in the liquid crystal panel is conducted to the glass plate for heat dissipation, and stripping is efficiently carried out from here. Therefore, when it combines with an air-cooled cooler style, it compares with the former and the temperature rise of a liquid crystal panel can be controlled very efficiently. The output of the part and an air cooling fan can be saved. Moreover, on one side face of this invention, thickness has pasted up the thick glass plate 1mm or more on the external surface of a direct transparence substrate. In total, the thickness of a transparence substrate and the glass plate for heat dissipation is set to 2mm or more, and separates greatly the front face of the glass plate for heat dissipation from a liquid crystal layer. Therefore, even if dust adheres to the front face of the glass plate for heat dissipation, it will be in a defocusing condition, and **** which produces degradation of drawing grace decreases. Or even if an opening dimension joins the glass plate of thin meat to the external surface of a transparence substrate through a closed space 2mm or less, while the same air-cooling effectiveness is acquired, degradation of the drawing grace by dust adhesion can also be prevented.

[0008]

[Embodiment of the Invention] With reference to a drawing, an operation gestalt with best this invention is explained to a detail below. Drawing 1 shows the 1st operation gestalt of the transparency mold display concerning this invention. (A) is the top view of a transparency mold display, and, similarly (B) is a sectional view. A transparency mold indicating equipment has the panel structure which the pixel electrode and the switching element equipped with the transparence substrate (opposite substrate) 2 of another side in which while was formed in the viewing area 8 and the transparence substrate (drive substrate) 1 and the counterelectrode were formed, and the liquid crystal 3 held in the gap of both the substrates 1 and 2 joined [each other], and is used for the projection display of images, such as a projector, so that it may illustrate. In addition, the flexible connector 4 for external connection is connected to the upper limit section of the drive substrate 1. As a description matter, thickness pastes [thermal conductivity] up the glass plate 5 for heat dissipation 1mm or more on the external surface of one [at least] transparence substrate directly by 1 or more

W/m-K. In addition, with this operation gestalt, the glass plate 5 for heat dissipation is pasted up on both the drive substrate 1 and the opposite substrate 2. This glass plate 5 for heat dissipation consists of quartz-glass material or heat-resisting glass material. Quartz-glass material has the thermal conductivity of 1.4 W/m-K extent, and is fully high temperature conductivity. Moreover, the thermal conductivity is 1.1 W/m-K extent also in heat-resisting glass material, for example, borosilicate glass. On the other hand, thermal conductivity is 0.5 - 0.7 W/m-K extent, and usual soda glass cannot acquire sufficient cooling effect and the heat dissipation effectiveness.

[0009] With this operation gestalt, thickness has pasted up the glass plate 5 for heat dissipation 1mm or more on the front face of the drive substrate 1 and the opposite substrate 2 at the appearance explained above. It is possible to promote the heat leakage from the whole transparency mold display by making it spread through the glass plate 5 for heat dissipation on which the heat accumulated in the drive substrate 1 and the opposite substrate 2 was pasted up, and performing heat distribution. Moreover, although the board thickness of the drive substrate 1 and the opposite substrate 2 is about 1mm, when thickness pastes up the glass plate 5 for heat dissipation 1mm or more, the distance from the field of liquid crystal 3 to a glass front face is securable 2mm or more. Thereby, the dust adhering to a front face is defocused at the time of a projection, and can mitigate drawing degradation. the temperature rise of the liquid crystal panel according [on the transparency mold display for projectors, and] to the optical incidence of a powerful lamp by this configuration -- mitigating -- in addition -- and it is possible to also mitigate the drawing degradation by the dust adhering to a front face. In addition, the area dimension is specified so that the glass plate 5 for heat dissipation may attain to the viewing area 8 of a transparency mold display at least.

[0010] Drawing 2 shows the 2nd operation gestalt of the transparency mold display concerning this invention. Like drawing 1 , (A) shows a flat-surface configuration and (B) expresses the cross-section configuration. It has the same structure as the 1st operation gestalt fundamentally shown in drawing 1 , and a corresponding reference number is given to a corresponding part, and an understanding is made easy. A different point is thermal conductivity's having minded the glass plate 5 for heat dissipation of 1 or more W/m-K, and the opening dimension's d having minded a closed space 6 2mm or less, and having joined to the external surface of the drive substrate 1 and the opposite substrate 2. That is, unlike the operation gestalt shown in drawing 1 , each glass plate 5 for heat dissipation is thin meat comparatively, and is joined by the external surface of each substrate in the state of sealing through that much heavy-gage jointing material for corrugated fibreboard 7. It is able for thickness to perform heat distribution through the glass plate 5 for heat dissipation of a less than 2mm air space and thin meat, and to promote the heat leakage from the whole transparency mold display with this structure. If the opening dimension d of a closed space 6 exceeds 2mm, loss arises in heat conduction and sufficient cooling effect cannot be acquired. Moreover, it is possible to prevent the drawing degradation by the dust which adhered to the front face of the glass plate 5 for heat dissipation like the 1st operation gestalt shown in drawing 1 . Moreover, as for the glass plate 5 for heat dissipation, the antireflection film is preferably formed in the both sides. As an antireflection film, it is the low refractive-index film SiO2. High refractive-index film TiO2 The multilayers piled up by turns can be used. These multilayers can be formed to both sides of the glass plate 5 for heat dissipation with vacuum deposition etc. Thus, by carrying out the acid-resisting coat of both sides of the glass plate 5 for heat dissipation, loss of the amount of incident light by surface reflection is abolished. Moreover, it has prevented beforehand that the unnecessary light by surface reflection carries out incidence to a liquid crystal panel, and optical leak of a switching element etc. arises.

[0011] Finally with reference to drawing 3 , the concrete example of a configuration of a transparency mold liquid crystal display is explained. This display consists of an opposite substrate 102 which consists of glass etc. as well as the drive substrate 101 which consists of glass etc., and liquid crystal 103 held among both so that it may illustrate. Accumulation formation of the pixel array section (viewing area) 104 and the drive circuit section is carried out at the drive substrate 101. The drive circuit section is divided into the vertical-drive circuit 105 and the level drive circuit 106. Moreover, the terminal area 107 for external connection is formed in the periphery upper limit of the drive substrate 101. The terminal area 107 is connected to the vertical-drive circuit 105 and the level drive circuit 106 through wiring 108. The pixel array section 104 is equipped with the gate line 109 and signal line 110 which crossed mutually. Accumulation formation of the thin film transistor 112 is carried out as the pixel electrode 111 and a switching element which drives this at the intersection of both Rhine 109,110. On the other hand, although not illustrated to the internal surface of the opposite substrate 102, the

color filter is formed depending on the counterelectrode or the case.
[0012] As a description matter of this invention, the glass plate 113 for heat dissipation has joined to the external surface of the opposite substrate 102, and the heat accumulated in liquid crystal 103 is absorbed. The drive substrate 101 has the thickness of about 0.8mm. The opposite substrate 102 has the thickness of about 1.1mm. Doubling both, the thickness of a liquid crystal panel is about 2mm. By pasting up the glass plate 113 for heat dissipation which is the thickness of about 2mm respectively from both sides on this liquid crystal panel, the heat accumulated in the liquid crystal panel can be removed effectively. When a liquid crystal panel is built into a projector, in order to receive the exposure of a powerful light source light, the temperature up of the liquid crystal 103 is carried out to about 100 degrees C only with simple air cooling. The way things stand, the liquefaction temperature of liquid crystal 103 may be exceeded and a display function is lost. Then, the glass plate 113 for heat dissipation is made to unite with a liquid crystal panel, and the request is cooled. According to this, the cooling effect which amounts to 10 degrees C - 20 degrees C is acquired.
[0013]
[Effect of the Invention] According to this invention, thickness has pasted [thermal conductivity] up the glass plate for heat dissipation 1mm or more on the appearance explained above on the external surface of one [at least] transparence substrate by 1 or more W/m-K. Or thermal conductivity minded the glass plate for heat dissipation of 1 or more W/m-K, the opening dimension minded a closed space 2mm or less, and it has joined to the external surface of one [at least] transparence substrate. With this configuration, in the transparency mold display for projections, since heat distribution can be performed through high temperature conduction glass from the panel front face where surface area is the largest, compared with a liquid cooling method etc., it is compact, and reliable cooling can be performed. Moreover, it is possible by securing the distance to a glass front face from a liquid crystal side 2mm or more to mitigate degradation of the drawing grace by adhesion of dust etc.

[Translation done.]

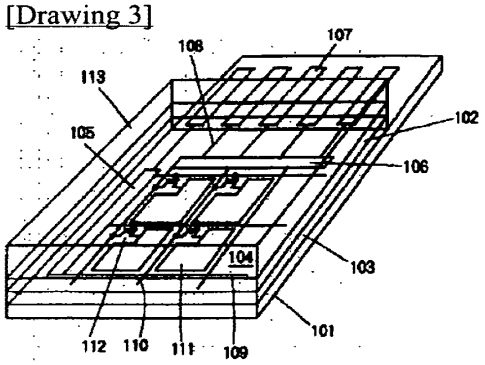
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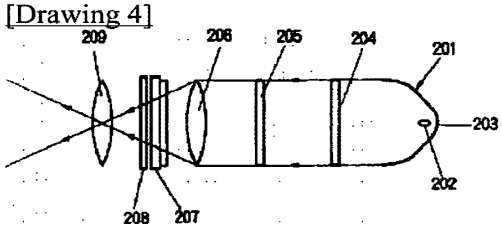
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 3]

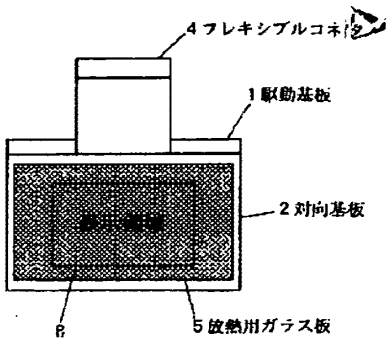


[Drawing 4]

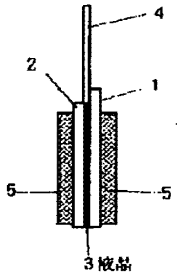


[Drawing 1]

(A)

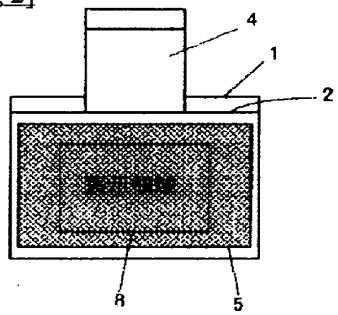


(B)

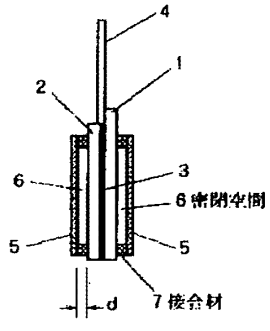


[Drawing 2]

(A)



(B)



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開平9－113906
(43)公開日　平成９年(1997)５月２日

(51)Int.Cl.⁶		識別記号	庁内整理番号	ＦＩ			技術表示箇所
Ｇ０２Ｆ	1/1335	５３０		Ｇ０２Ｆ	1/1335	５３０	
	1/13	５０５			1/13	５０５	

審査請求　未請求　請求項の数４　ＦＤ　（全５頁）

(21)出願番号　特願平7－291792

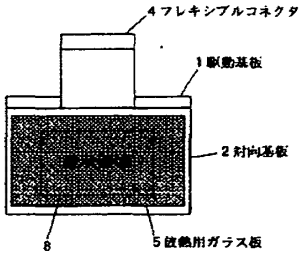
(22)出願日　平成７年(1995)10月13日

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東京都品川区北品川６丁目７番35号
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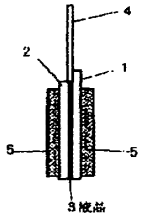
(54)【発明の名称】　透過型表示装置

(57)【要約】
【課題】　プロジェクタに組み込まれる透過型表示装置の冷却構造を改善する。
【解決手段】　透過型表示装置は画素電極及びスイッチング素子が形成された駆動基板１と、対向電極が形成された対向基板２と、互いに接合した両基板１，２の間隙に保持された液晶３とを備えたパネル構造を有し、画像の投影表示に用いられる。熱伝導率が１Ｗ／ｍ・Ｋ以上で厚みが１㎜以上の放熱用ガラス板５を各基板１，２の外面に接着する。あるいはこれに代えて、熱伝導率が１Ｗ／ｍ・Ｋ以上の放熱用ガラス板を空隙寸法が２㎜以下の密閉空間を介して各基板１，２の外面に接合しても良い。

（Ａ）



（Ｂ）



他方の透明基板と、互いに接合した該一対の透明基板の間隙に保持された液晶とを備えたパネル構造を有し、画像の投影表示に用いられる。特徴事項として、熱伝導率が1W／m・K以上の放熱用ガラス板を空隙寸法が2mm以下の密閉空間を介して少なくとも一方の透明基板の外面に接合する。好ましくは前記放熱用ガラス板はその両面に反射防止膜が形成されている。

【0007】本発明によれば熱伝導率が1W／m・K以上の高熱伝導ガラスを放熱用として一方もしくは両方の透明基板の外面に接着している。かかる構造を有する透過型表示装置を例えばプロジェクタ等に組み込んだ場合、液晶パネルに蓄積された熱は放熱用ガラス板に伝導しここから効率良く放散される。従って、空冷式の冷却機構と組み合わせた場合従来に比し極めて効率良く液晶パネルの温度上昇を抑制できる。その分、空冷ファンの出力を節約可能である。又、本発明の一側面では厚みが1mm以上の肉厚ガラス板を直接透明基板の外面に接着している。透明基板と放熱用ガラス板の厚みは合計で2mm以上となり、放熱用ガラス板の表面は液晶層から大きく離れる。従って放熱用ガラス板の表面にダストが付着してもデフォーカス状態となり、画品位の劣化を生じる惧れが少なくなる。あるいは、薄肉のガラス板を空隙寸法が2mm以下の密閉空間を介して透明基板の外面に接合しても同様な空冷効果が得られると共に、ダスト付着による画品位の劣化も防ぐ事ができる。

【0008】

【発明の実施の形態】以下図面を参照して本発明の最良な実施形態を詳細に説明する。図1は本発明にかかる透過型表示装置の第1実施形態を示している。（A）は透過型表示装置の平面図であり、（B）は同じく断面図である。図示する様に、透過型表示装置は画素電極及びスイッチング素子が表示領域8に形成された一方の透明基板（駆動基板）1と、対向電極が形成された他方の透明基板（対向基板）2と、互いに接合した両基板1，2の間隙に保持された液晶3とを備えたパネル構造を有し、プロジェクタ等画像の投影表示に用いられる。なお駆動基板1の上端部には外部接続用のフレキシブルコネクタ4が接続されている。特徴事項として、熱伝導率が1W／m・K以上で厚みが1mm以上の放熱用ガラス板5を少なくとも一方の透明基板の外面に直接接着する。なお本実施形態では駆動基板1及び対向基板2の両方に放熱用ガラス板5を接着している。この放熱用ガラス板5は石英ガラス材又は耐熱ガラス材からなる。石英ガラス材は1．4W／m・K程度の熱伝導率を有しており十分に高熱伝導性である。又、耐熱ガラス材も例えば硼珪酸ガラスではその熱伝導率が1．1W／m・K程度である。これに対し、通常のソーダガラスは熱伝導率が0．5～0．7W／m・K程度であり十分な冷却効果及び放熱効果を得る事はできない。

【0009】以上説明した様に、本実施形態では駆動基板1及び対向基板2の表面に厚さが1mm以上の放熱用ガラス板5を接着している。駆動基板1及び対向基板2に蓄積した熱を接着した放熱用ガラス板5を通して拡散させ、熱分散を行なう事により透過型表示装置全体からの熱放散を促進する事が可能である。又、駆動基板1及び対向基板2の板厚は約1mm程度であるが、厚さが1mm以上の放熱用ガラス板5を接着する事により、液晶3の面からガラス表面までの距離を2mm以上確保する事ができる。これにより、表面に付着したダストがプロジェクション時にデフォーカスされ、画品位低下を軽減する事ができる。かかる構成により、プロジェクタ用の透過型表示装置において、強力なランプの光入射による液晶パネルの温度上昇を軽減し、なお且つ表面に付着するダストによる画品位低下をも軽減する事が可能である。なお、放熱用ガラス板5は少なくとも透過型表示装置の表示領域8に及ぶ様にその面積寸法が規定されている。

【0010】図2は本発明にかかる透過型表示装置の第2実施形態を示している。図1と同様に（A）は平面形状を示し、（B）は断面形状を表わしている。基本的には図1に示した第1実施形態と同一の構造を有しており、対応する部分には対応する参照番号を付して理解を容易にしている。異なる点は、熱伝導率が1W／m・K以上の放熱用ガラス板5を空隙寸法dが2mm以下の密閉空間6を介して駆動基板1及び対向基板2の外面に接合した事である。即ち、各放熱用ガラス板5は図1に示した実施形態と異なり比較的薄肉であり、その分厚肉の接合材7を介して密閉状態で各基板の外面に接合されている。この構造では厚みが2mm以内の空気層及び薄肉の放熱用ガラス板5を通して熱分散を行ない、透過型表示装置全体からの熱放散を促進する事が可能である。密閉空間6の空隙寸法dが2mmを超えると熱伝導に損失が生じ十分な冷却効果を得る事ができない。又、図1に示した第1実施形態と同様に放熱用ガラス板5の表面に付着したダスト等による画品位低下を防ぐ事が可能である。

又、好ましくは放熱用ガラス板5はその両面に反射防止膜が形成されている。反射防止膜としては例えば低屈折率膜SiO_2と高屈折率膜TiO_2を交互に重ねた多層膜を用いる事ができる。この多層膜は真空蒸着等で放熱用ガラス板5の両面に成膜可能である。この様に放熱用ガラス板5の両面を反射防止コートする事により、表面反射による入射光量の損失をなくしている。又、表面反射による不要光が液晶パネルに入射しスイッチング素子の光リーク等が生じる事を未然に防止している。

【0011】最後に図3を参照して、透過型液晶表示装置の具体的な構成例を説明する。図示する様に、本表示装置はガラス等からなる駆動基板101と同じくガラス等からなる対向基板102と両者の間に保持された液晶103とで構成されている。駆動基板101には画素アレイ部（表示領域）104と駆動回路部とが集積形成されている。駆動回路部は垂直駆動回路105と水平駆動

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回路１０６とに分かれている。又、駆動基板１０１の周辺部上端には外部接続用の端子部１０７が形成されている。端子部１０７は配線１０８を介して垂直駆動回路１０５及び水平駆動回路１０６に接続している。画素アレイ部１０４は互いに交差したゲートライン１０９と信号ライン１１０を備えている。両ライン１０９，１１０の交差部には画素電極１１１と、これを駆動するスイッチング素子として薄膜トランジスタ１１２が集積形成されている。一方、対向基板１０２の内表面には図示しないが対向電極や場合によってはカラーフィルタが形成されている。

【００１２】本発明の特徴事項として、例えば対向基板１０２の外面に放熱用ガラス板１１３が接合しており、液晶１０３に蓄積した熱を吸収する。駆動基板１０１は例えば０．８㎜程度の厚みを有する。対向基板１０２は例えば１．１㎜程度の厚みを有する。両者を合わせて液晶パネルの層厚は２㎜程度である。この液晶パネルに両側から例えば各々２㎜程度の厚みの放熱用ガラス板１１３を接着させる事により、液晶パネルに蓄積した熱を効果的に取り除く事ができる。液晶パネルをプロジェクタに組み込んだ場合、強力な光源光の照射を受ける為、単純な空冷だけでは、液晶１０３は例えば１００℃程度まで昇温する。このままでは液晶１０３の液化温度を超える場合があり、表示機能が失われる。そこで放熱用ガラス板１１３を液晶パネルに一体化させ所望の冷却を行なっている。これによれば１０℃～２０℃に及ぶ冷却効果が得られる。

【００１３】

【発明の効果】以上説明した様に、本発明によれば、熱＊

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＊伝導率が１Ｗ／ｍ・Ｋ以上で厚みが１㎜以上の放熱用ガラス板を少なくとも一方の透明基板の外面に接着している。あるいは、熱伝導率が１Ｗ／ｍ・Ｋ以上の放熱用ガラス板を空隙寸法が２㎜以下の密閉空間を介して少なくとも一方の透明基板の外面に接合している。かかる構成ではプロジェクション用透過型表示装置において、最も表面積の大きいパネル表面より高熱伝導ガラスを通して熱分散が行なえる為、液冷方式等に比べコンパクトで信頼性が高い冷却が行なえる。又、液晶面よりガラス表面までの距離を２㎜以上確保する事により、ダスト等の付着による画品位の劣化を軽減する事が可能である。

【図面の簡単な説明】

【図１】本発明にかかる透過型表示装置の第１実施形態を示す平面図及び断面図である。

【図２】本発明にかかる透過型表示装置の第２実施形態を示す平面図及び断面図である。

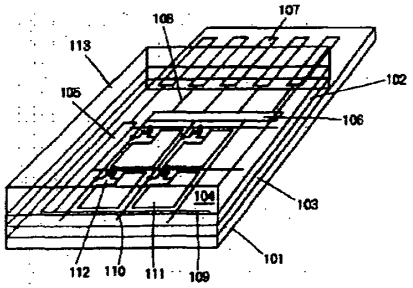
【図３】本発明にかかる透過型表示装置の具体的な構成を示す模式的な斜視図である。

【図４】液晶プロジェクタの一般的な構成を示す模式図である。

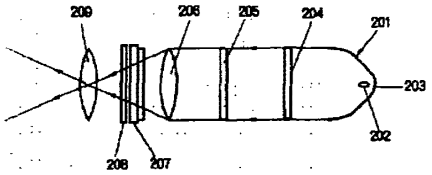
【符号の説明】

1　駆動基板
2　対向基板
3　液晶
4　フレキシブルコネクタ
5　放熱用ガラス板
6　密閉空間
7　接合材
8　表示領域

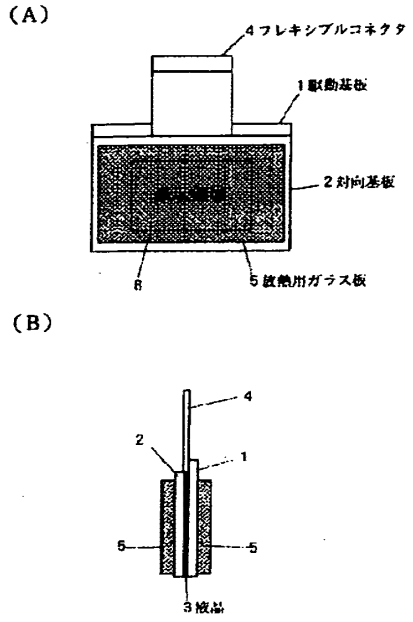
【図３】



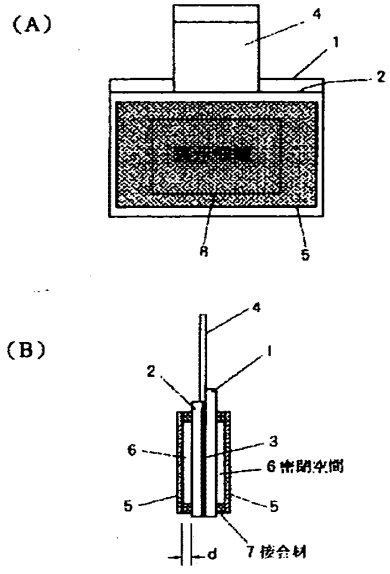
【図４】



【図１】


(A)
4 フレキシブルコネクタ
1 駆動基板
2 対向基板
6
5 放熱用ガラス板
(B)
4
2
1
5
5
3 液晶

【図２】


(A)
4
1
2
6
5
(B)
4
1
2
6
3
6 密閉空間
5
5
d
7 接合材

PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11203919

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	9 minus 20 =	* 0	X$ 25 =		OR	X$50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	X100 =		OR	X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1000

APPLICATION AS AMENDED – PART II

PNA 9-13-05

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 9	Minus	** 20	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NUMBER	

?	Rejected	—	(Through Numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date
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If more than 150 claims or 10 actions staple additional sheet here