

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Chongqing HKC Optoelectronics Technology Co., Ltd.,

Petitioner

v.

138 East LCD Advancements Limited,

Patent Owner

Patent No. 7,335,913

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**Declaration of Carl Sechen, Ph.D.**

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1. I, Professor Carl Sechen, make this declaration in connection with the proceeding identified above.

**I. Introduction**

2. I have been retained by counsel for Petitioner Chongqing HKC Optoelectronics Technology Co., Ltd. (“HKC”), as a technical expert in connection with the proceeding identified above. I submit this declaration in support of HKC.

3. I understand that this proceeding involves U.S. Patent No. 7,335,913 (“the ’913 patent”), and I have been asked to provide my opinions as to the patentability of the claims of the ’913 patent. I have been informed that a copy of the ’913 patent is attached to the petition as Exhibit 1001.

4. This declaration sets forth the opinions that I have formed in this proceeding based on my study of the evidence, my understanding as an expert in the field, and my education, training, research, knowledge, and personal and professional experience.

5. I am being compensated for my time at the rate of \$400 per hour for my work. This compensation is not contingent in any way upon the nature of my findings, the presentation of my findings in testimony, or the outcoming of this proceeding.

6. In forming my opinions, in addition to any materials cited in this report, I have reviewed the following materials:

- U.S. Patent No. 9,335,913, issued to Murade, filed September 13, 200, issued on February 26, 2008 (“‘913 patent”) (Ex. 1001)
- Prosecution History for U.S. Patent No. 7,335,913 (“‘913 FW”) (Ex. 1004)
- Japanese Pub. Patent App. No. JPH10-282522A, filed on April 9, 1997, published on October 23, 1998, and its accompanying translation (“*Adachi*”) (Ex. 1005)
- U.S. Patent Application Pub. No. 2002/0060780, filed on October 15, 2001, published on May 23, 2002 (“*Takezawa*”) (Ex. 1006)
- Japanese Patent No. JP2802156B2, filed on September 21, 1990, published on May 1, 1992 as JPH04130418A, and issued September 24, 1998, and its accompanying translation (“*Sekado*”) (Ex. 1007)
- U.S. Patent No. 6,396,558. filed on August 24, 2000, issued on May 28, 2002 (“*Kim*”) (Ex. 1008)
- U.S. Patent No. 6,501,519, filed on December 15, 2000, published on September 20, 2001 as U.S. Pub. Pat. App. 2001/0022638, issued on December 31, 2002 (“*Ha*”) (Ex. 1009)
- U.S. Patent App. Pub. No. 2002/0135293, filed on February 8, 2002, published on September 26, 2002 (“*Aruga*”) (Ex. 1010)
- Japanese Pub. Patent App. No. JP2000267590A, filed on March 19, 1999, published on September 29, 2000, and its accompanying translation (“*Yoneda*”) (Ex. 1011)
- Japanese Pub. Patent App. No. JP2004094020A, filed on September 2, 2002, published on March 25, 2004, and its accompanying translation (“*Tanaka*”) (Ex. 1012)
- U.S. Pub. Patent Application No. 2003/0189686, filed on April 1, 2003, published October 9, 2003 (“*Hirosue*”) (Ex. 1013)

## II. Expert Qualifications

7. Based upon my educational and work experience, I believe I am well

qualified to serve as a technical expert in this matter.

8. I have been told that my curriculum vitae is attached as Exhibit 1003 to the petition.

9. I expect to testify further, if requested, regarding the subject matter set forth in this declaration.

10. I have been a Professor of Electrical Engineering for 36 years. Since August 15, 2005 to the present, I have been a Professor of Electrical and Computer Engineering at the University of Texas at Dallas. From July 1992 to August 2005, I was a Professor of Electrical Engineering at the University of Washington. From July 1986 through June 1992, I was an Assistant and then Associate Professor of Electrical Engineering at Yale University. Over these years, my research has focused on the design and computer-aided design of digital and analog integrated circuits. I have taught numerous students how to design digital, analog, and mixed signal integrated circuits and printed circuit boards, as part of the design courses that I have offered. More information about my academic work can be found in my curriculum vitae, which I have been told is Exhibit 1003 to the Petition.

11. As a professor, I have developed and taught numerous courses, For example, several courses that teach VLSI integrated circuit design in great detail. I have taught these courses continuously for the past 25 years. I have taught Verilog design to undergraduate and graduate students at the University of Washington and

at the University of Texas at Dallas since 2001.

12. I have also been involved in numerous research projects on digital and analog VLSI design. I have taught numerous graduate researchers how to design digital and analog integrated circuits. My digital and analog VLSI design research has been funded by many companies over the years, including Intel, AMD, Cadence, LSI Logic, and Texas Instruments. Texas Instruments funded my work on H.264 video encoding for more than three years. My VLSI and memory design research has also been supported by governmental agencies such as DARPA and the National Science Foundation. I have authored or coauthored over 200 papers and one book, the majority of which concern digital and analog integrated circuit design, as well as computer-aided design. I have also designed, fabricated and tested numerous integrated circuits. I am a co-inventor on four issued patents directed to transistor and computational logic technologies. Three of the patents concern transistor-level programmable logic.

13. I earned a B.E.E. degree in Electrical Engineering from the University of Minnesota. After that, I went on to the Massachusetts Institute of Technology, where I earned an M.S. degree in Electrical Engineering. I was awarded a Ph.D. in electrical engineering from the University of California at Berkeley in 1986. More details about my education are set forth in my attached curriculum vitae. *See* Exhibit 1003.

14. I was elected a Fellow of the IEEE in 2002 for contributions to placement and routing of ASICs. IEEE stands for Institute of Electrical and Electronics Engineers, which is the leading professional association for electrical engineers. The Board of Directors of the IEEE awards the rank of “Fellow” to individuals with an extraordinary record of accomplishments in any of the IEEE fields of interest. The total number of IEEE members who can be named Fellows in any one year cannot exceed one-tenth of one percent of the total voting IEEE membership.

15. I also received a Distinguished Teaching Award from the University of Texas at Dallas in 2008. I also received a highly unusual *second* Distinguished Teaching Award from the University of Texas at Dallas in 2014. In 2002, I also received the Outstanding Research Advisor Award from the Department of Electrical engineering at the University of Washington and the Best Project Award from the NSF Center for the Design of Digital and Analog ICs. I also received the Semiconductor Research Corporation's Inventor's Recognition Award in 2001 for the development of output prediction logic. I received the 1994 SRC Technical Excellence Award, and I also received the Semiconductor Research Corporation's 1988 SRC Inventor's Award. Additional honors and awards are set forth in my CV. *See* Exhibit 1003.

16. All of the opinions stated in this report are based on my own personal

knowledge and professional judgment.

### **III. Overview of the '913 Patent**

17. I have reviewed the '913 patent and based on my review understand the '913 patent to describe the following.

#### **A. The '913 Patent**

18. The '913 patent is titled "Electro-optical device and electronic apparatus," and issued on February 26, 2008. '913 patent, cover. The patent specifically states that electro-optical devices include liquid crystal displays ("LCDs"). '913 patent, col. 1:12.

19. The '913 patent provides a detailed description of the state-of-the-art devices existing before its alleged invention. In particular, the '913 patent describes the related art as disclosing an electro-optical device, a substrate, on which display electrodes and a circuit unit for driving the display electrodes are provided, and a counter substrate are disposed to face each other with an electro-optical material, such as liquid crystal, interposed therebetween. These substrates are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of the substrates are bonded to each other by a sealant so as to form an internal space, and the electro-optical material is sealed in the internal space. '913 patent, col. 1:15-25.

20. The substrate provided with the display electrodes extends from the

counter substrate on one side in plan view, and external connecting terminals are provided in a portion extending on one side (hereinafter, referred to as an extending portion). The external connecting terminals are connected to wiring lines led from a circuit unit and the like, and are provided such that surfaces thereof are exposed to the outside so as to be supplied with signals or power from the outside. In addition, a driving circuit, which is connected to the external connecting terminals for supplying image signals, is generally provided in the extending portion. '913 patent, col. 1:26-36.

21. The '913 patent asserts that the problem with then-existing devices is that it is difficult to achieve a small enough size for the device, and in particular, for the extending portion. As a solution, the patent states that "in order to reduce the width of the extending portion, the layout of the external connecting terminals and the lead wiring lines needs to be considered." '913 patent, col.1:43-52.

22. The '913 patent describes that on the extending portion are provided external connecting terminals, which are electrically connected to the circuit unit. The '913 patent further describes how a plurality of external connecting terminals are arranged, for example, along an outer edge of the extending portion, and are correspondingly connected to the lead wiring lines, which are led from the circuit unit or the display electrodes. The lead wiring lines are generally relayed in a region other than a region where the external connecting terminals are arranged.

'913 patent, col. 2:21-31.

23. The '913 patent describes that, in a first part of the invention, the external connecting terminals and the lead wiring lines are arranged to at least partially overlap each other in plan view (that is, in a three-dimensional manner in the extending portion). Such a configuration is implemented by electrically connecting at least some of the lead wiring lines and the external connecting terminals to each other via contact holes or the like, for example, and by laminating them with an interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure. '913 patent, col. 2:32-44.

24. The '913 patent describes that, in a second part of the invention, the circuit unit and the external connecting terminals are disposed to at least partially overlap each other in plan view. Such a configuration can be implemented by laminating the circuit unit and at least some of the external connecting terminals with an interlayer insulating film interposed therebetween. In this case, two or more conductive films serving as wiring lines or terminals may be laminated. Further, each conductive film may have a single-layered structure or a multi-layered structure. '913 patent, col. 4:22-31.

25. The claims of the '913 patent mostly recite the basic, well-known

configuration of an electro-optical device that has a pair of substrates that are disposed to face each other with a predetermined gap between them. One of the claimed substrates has an extended portion that extends out from the other substrate in plan view. On this extended substrate, there are display electrodes and circuit units that drive the display electrodes. In addition, there are wiring lines for driving the circuit unit and the display electrodes, and a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion. All of these limitations are a standard description of LCD devices existing at the time of the patent's application. Lastly, the independent claims of the patent recite a final limitation of: a plurality of external connecting terminals provided on the extending portion, each of which overlap in plan view with either the plurality of lead wiring lines (independent claim 1), or the circuit unit (independent claim 5).

26. In particular, claim 1, the first independent claim of the '913 patent recites the following:

1. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;

display electrodes that are provided on the one substrate;

a circuit unit that is provided on the one substrate so as to drive the display electrodes;

wiring lines for driving the circuit unit and the display electrodes;

a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and

a plurality of external connecting terminals provided on the extending portion, each of the external connecting terminals overlapping with the plurality of lead wiring lines in plan view.

27. Similarly, claim 5, the other independent claim of the '913 patent recites the following:

5. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;

display electrodes that are provided on the one substrate;

a circuit unit that is provided on the one substrate so as to drive the display electrodes;

wiring lines for driving the circuit unit and the display electrodes;

a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and

a plurality of external connecting terminals provided on the extending portion, each of the external connecting terminals overlapping with the circuit unit in plan view.

28. As seen from the above, claims 1 and 5 are identical except for the very last limitation. Claim 1 requires “each of the external connecting terminals overlapping with *the plurality of lead wiring lines* in plan view.” Claim 5 differs

only in requiring “each of the external connecting terminals overlapping with *the circuit unit* in plan view.”

**B. Prosecution History**

29. Based on my review of the '913 patent and its prosecution history, I understand the following. The application for the '913 patent was filed on September 13, 2005, as U.S. Patent Application No. 11/223,919. '913 patent, cover. The application claimed priority to Japanese Application No. 2004-328982, dated November 12, 2004. '913 patent, cover.

30. As originally filed, claims 1 and 5 differed from the claims as they issued. As originally filed, claim 1 recited:

(Original) 1. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of the wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to

at least partially overlap the plurality of lead wiring lines in plan view.

'913 FW-0334.

31. As originally filed, claim 5 recited:

(Original) 5. An electro-optical device comprising:

a pair of substrates that are disposed to face each other with a predetermined gap therebetween, one substrate of the pair of substrates extending from the other substrate on at least one side in plan view;

display electrodes that are provided on one substrate;

a circuit unit that is provided on one substrate so as to drive the display electrodes;

a plurality of lead wiring lines that are led from one of the sides of the wiring lines for driving the circuit unit and the display electrodes to an extending portion extending on the one side of one substrate; and

a plurality of external connecting terminals that are correspondingly connected to the plurality of lead wiring lines and are provided on a surface of the extending portion facing the other substrate so as to at least partially overlap the circuit unit in plan view.

'913 FW-0335-0336.

32. During prosecution, the examiner issued a non-final Office Action dated 06/14/2007, in which the examiner rejected pending claims 1-5 and 8-9 under 35 U.S.C. §102 as being unpatentable over U.S. Patent Publication No. US2003-0122979, to *Morimitsu*. '913 FW-0024.

33. In response, the applicant amended the claims to try to distinguish the prior art. Claim 1 was amended to, among other things, recite "each of the external

connecting terminals overlapping with the plurality of lead wiring lines in plan view”; and claim 5 was similarly amended to, among other things, recite “each of the external connecting terminals overlapping with *the circuit unit* in plan view.” ’913 FW-0015-17. In other words, the original claim language of “at least partially overlap” was replaced with “overlapping.” Applicant then argued that “Morimitsu does not disclose each of the external connecting terminals overlapping with the plurality of lead wiring lines, or circuit unit, in plan view. At best, Morimitsu suggests that pad ITO film 52 overlaps a single power supply pad 13.” ’913 FW-0020.

#### **IV. Legal Standards**

34. I have been told that the following legal principles apply to analysis of patentability based on 35 U.S.C. § 103 (pre-America Invents Act (“AIA”)). I also have been told that, in an *inter partes* review proceeding, a patent claim may be deemed unpatentable if it is shown by a preponderance of the evidence that the claim was rendered obvious by one or more prior art patents or publications under § 103.

35. I have been told that under 35 U.S.C. § 103(a) (pre AIA), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have

been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.”

36. When considering the issues of obviousness, I have been told that I am to do the following:

- Determine the scope and content of the prior art;
- Ascertain the differences between the prior art and the claims at issue;
- Resolve the level of ordinary skill in the pertinent art; and
- Consider evidence of secondary indicia of nonobviousness (if available).

37. I also have been advised that, where a party alleges obviousness based on a combination of references, that party must identify a reason why a person skilled in the art would have been motivated to combine the asserted references in the manner recited in the claims and to explain why one skilled in the art would have had a reasonable expectation of success in making such combinations.

38. I have been advised that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine the references as recited in the claims and explain why one would have reasonably expected to succeed in doing so.

39. I have been advised that two references are considered to be in the same field of art when the references are either (1) in the same field of endeavor, regardless of the problems they address, or (2) reasonably pertinent to the particular problem being solved by the inventor in a patent.

40. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

**V. Person of Ordinary Skill in the Art (“POSITA”)**

41. I understand that patentability must be analyzed from the perspective of a hypothetical person of ordinary skill in the art in the same field as the patent at the time of the invention. I understand that "person of ordinary skill in the art" (POSITA), "person of ordinary skill," "skilled artisan," or similar phrase to denote this hypothetical person of ordinary skill.

42. I understand a POSITA is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I further understand that factors that may be considered in determining the level of ordinary skill in the art may include: (1) type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) educational level of active workers in the field. I further

understand that a POSITA is also a person of ordinary creativity, not an automaton.

I understand that a POSITA will be able to fit the teachings of multiple patents together like pieces of a puzzle.

43. Based on my experience in teaching, researching, and consulting, and considering the factors identified in the preceding paragraphs, my opinion is that a person of ordinary skill in the art at the time of the alleged invention of the '913 patent would have either a bachelor's degree in electrical or computer engineering or an equivalent area with three years of experience in the field of display technology or a master's degree with one year of experience in the field of display technology.

44. As of the filing date of the application that led to the '913 patent and its foreign priority application, I was at least a person of ordinary skill in the art.

## **VI. Claim Construction**

45. I have been informed that in an IPR, claim terms should now be construed under the same standard applied in district court cases, which I am told is sometimes referred to as the *Phillips* standard. I have applied that standard here, which I understand involves construing the terms based on how one of ordinary skill in the art would have understood the terms as of the claims' priority date in light of the intrinsic record, including the claim language, patent specification, and prosecution history. I also understand that extrinsic evidence, such as dictionaries,

may be relied on when construing the claims. However, I understand that extrinsic evidence is generally less significant to determining the legally operative meaning of a claim, especially where the intrinsic record demonstrates the scope of the claim.

46. Based on my review of the claims, patent specification, prosecution history, and certain extrinsic evidence discussed in this declaration, I do not see a need to articulate a specific construction for any of the claim terms beyond any discussion that appears in the analysis below. I understand that the Patent Owner has not provided any proposed claim construction for the claims.

## VII. Detailed Analysis

### A. Overview of the Prior Art

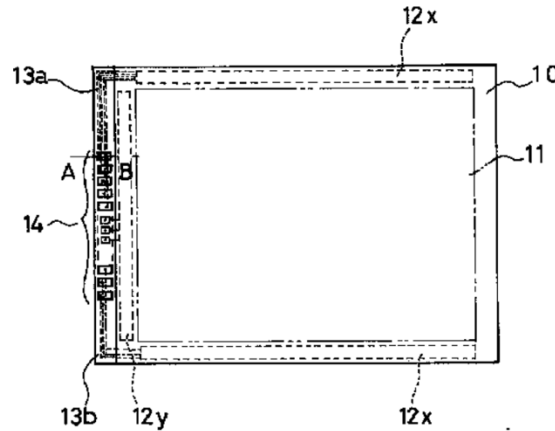
#### 1. *Adachi*

47. *Adachi* relates to a liquid crystal display element 80 including a transparent insulating substrate such as glass that has a rectangular display region 81, and drive circuits 12x and 12y that drive the liquid crystal display element 80, and that are integrated and built in a periphery of the display region 81. *Adachi* Fig. 1 (below). Power or input and output signals supplied to the drive circuits 12x and 12y are connected to an external connection terminal group 83 formed at an end portion of the liquid crystal display element 80 by wiring groups 82a and 82b provided in the liquid crystal display element 80. Further, as shown in *Adachi* Fig. 9 (below), the wiring groups 82a and 82b, as well as the external connection

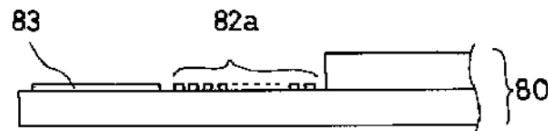
terminal group 83, are patterned in the same conductor layer, and the external connection terminal group 83 is connected to an external circuit not shown.

Adachi, ¶[0004].

【図 1】



【図 9】



As described above, on a side of the liquid crystal display element 80, and needing to be formed on a substrate such as glass, are the external connection terminal group 83 connected to the external circuit, the wiring groups 82a and 82b, and the external connection terminal group 83 for transmitting power or input and output signals to the drive circuits 12x and 12y. In addition, the wiring groups 82a and 82b and the external connection terminal group 83 are formed in the same conductor layer. Thus, the substrate needs a region to dispose the wiring groups 82a and 82b for the drive circuits 12x and 12y to the external connection terminal

group 83 and a region to dispose the external connection terminal group 83.

Therefore, it is difficult to reduce the area to which the external circuit of the liquid crystal display element is connected, and thus it is difficult to reduce the size of the non-display area (frame) of the liquid crystal display device. *Adachi*, ¶[0006].

*Adachi*'s invention was made in view of the above-described conventional example, and its objective was to provide a display device that achieves a narrow frame and an enlarged display region.

## **2.     *Takezawa***

48.     *Takezawa* discloses a projector with a liquid crystal device which modulates light emitted from a light source. The liquid crystal device comprises a base substrate that has a plurality of pixel electrodes disposed in a matrix arrangement and drive elements each provided for a corresponding one of the pixel electrodes and electrically connected thereto, a counter substrate, and liquid crystals provided between the base substrate and the counter substrate. *Takezawa*, ¶[0023].

## **3.     *Sekado***

49.     *Sekado* discloses a liquid crystal display device, with liquid crystals sealed between a pair of substrates, comprising pixel electrodes arranged in a matrix, thin film transistors disposed close to and connected to the pixel electrodes, signal lines connected to source electrodes of the thin film transistors, and scanning

lines connected to gate electrodes of the thin film transistors on one substrate of the substrates. *Sekado* further discloses a driver IC for driving use disposed on the substrate and connected to a COG (chip on glass) so as to supply signals to the signal lines and the scanning lines on the substrate, wherein a plurality of input pads on the driver IC for driving use are arranged in a direction substantially perpendicular to an arrangement direction of a plurality of output pads on the driver IC for driving use. *Sekado*, Claim 1.

**4.     *Kim***

50.     *Kim* relates to a connecting part of an outer circuit in a liquid crystal display panel, including a substrate and a plurality of pads on the substrate, where the pads are connected to an outer circuit. A first connecting wire is connected to one of said pads, the wire being arranged in a first direction. A second connecting wire is connected to another one of said pads, the second connecting wire being arranged in a second direction. *Kim*, Abstract.

**5.     *Ha***

51.     *Ha* relates to an array substrate for a transflective liquid crystal display device and including a pixel electrode, a reflective electrode, and an interposed insulation layer. *Ha*, Abstract.

**6.     *Aruga***

52.     *Aruga* discloses a liquid crystal display comprising a second substrate for carrying a liquid crystal and data lines formed on the surface of the second

substrate, a third insulating layer for covering the data lines are formed on the surface of the second substrate. On the surface of the third insulating layer, chip connecting wiring are formed over a covered region covered with a sealing material 30 and the liquid crystal and the region other than the covered region 61. *Aruga*, abstract.

**7.     *Yoneda***

53.     *Yoneda* discloses a liquid crystal display device, a pixel region, a source driver and a gate driver that are formed on one substrate. An external connecting terminal is formed in a region adjacent to a side of the substrate where the gate driver is formed, and a flexible circuit board is connected to the external connecting terminal. An integrated circuit is disposed on an extension line of the terminal along the side. Thereby, a peripheral region of the substrate can be effectively used, and an outer shape of the liquid crystal module including the substrate and peripheral circuits can be made compact. *Yoneda*, Abstract.

**8.     *Tanaka***

54.     *Tanaka* discloses an external connection terminal that is constituted by successively layering an electrode layer made of a same electrode material as a scanning line electrode, an electrode layer made of a same electrode material as a signal line electrode, an electrode layer made of a same electrode material as a transparent electrode, and an electrode layer made of a same electrode material as a

reflective electrode on a glass substrate. *Tanaka*, Overview.

**9.     *Hirosue***

55.     *Hirosue* discloses a display device that comprises scan lines on an insulating substrate, signal lines intersecting with the scan lines with an insulating film interposed therebetween, a display area comprising pixel electrodes connected to the signal lines, a scan line driver circuit connected to the scan lines, and a signal line driver circuit connected to the signal lines. The scan line driver circuit and the signal line driver circuit are mounted directly on the insulating substrate outside of the display area and close to one side of the display area. Lines connecting the scan line driver circuit and the signal line driver circuit are formed in an area in which the scan line driver circuit and the signal line driver circuit are mounted. *Hirosue*, abstract.

**B.     *Adachi* Anticipates or Renders Obvious in View of a POSITA's General Knowledge Claims 1-4 and 9.**

**1.     Claim 1**

**An electro-optical device comprising:**

56.     A POSITA would understand *Adachi* to teach an electro-optical device. *Adachi* describes a liquid crystal display element 10, which is an electro-optical device. *Adachi*, [0014].

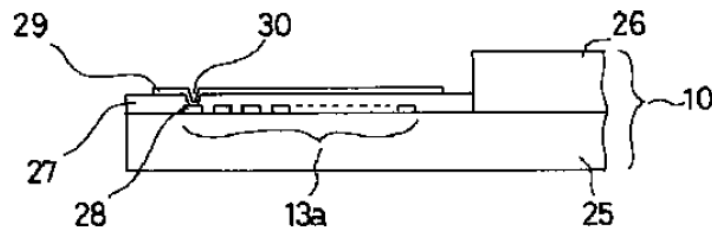
57.     Accordingly, it is my opinion that *Adachi* teaches the preamble of claim 1.

**a pair of substrates that are disposed to face each other with a predetermined gap therebetween,**

58. A POSITA would understand *Adachi* to teach a pair of substrates that are disposed to face each other with a predetermined gap between them.

59. *Adachi* relates to standard liquid crystal devices, such as “a liquid crystal display device (LCD) ... [using] a TFT-LCD that controls on-off operation of liquid crystals by a thin film transistor (TFT) provided in each pixel of a liquid crystal display.” *Adachi*, ¶[0002]. Such LCDs have a pair of substrates that are disposed to face each other with the liquid crystals being in between the two substrates in a display area. For example, *Adachi* Figure 3 (below) illustrates a standard LCD layout showing array substrate 25 and color filter substrate 26 facing each other, with array substrate 25 having an extending portion. *Adachi*, ¶[0035].

【図 3】



60. Thus, *Adachi* teaches a display region 11 where between the two substrates various other components, such as TFT's, are formed on the array substrate 25. *Adachi*, ¶¶[0014]-[0015], [0018]-[0019]; Figs. 1, 2, and 4(e).

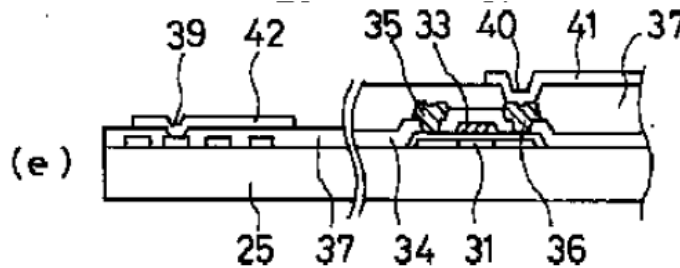
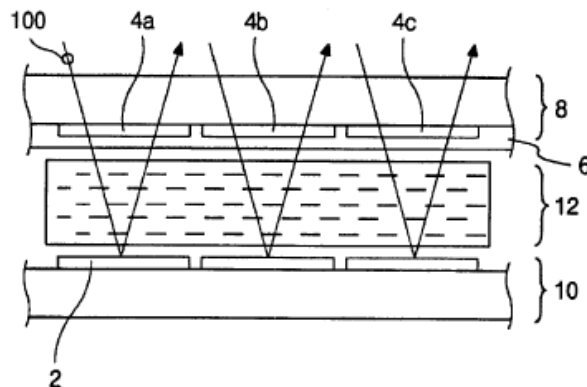


Fig. 4(e) of *Adachi*

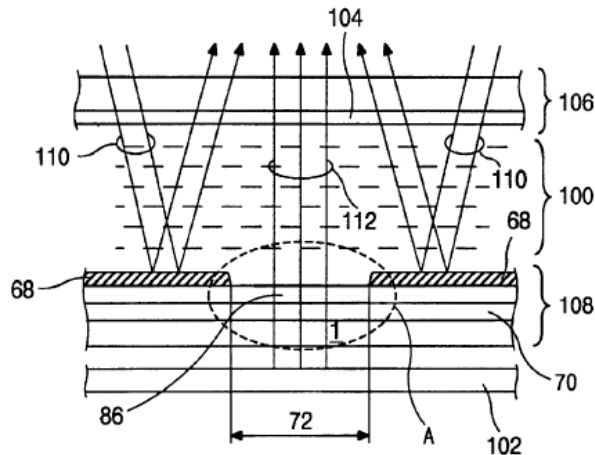
61. Alternatively, a POSITA's general knowledge would include knowing that LCDs necessarily have a gap between the two substrates where the liquid crystals and associated electrical elements are located. For example, the '913 patent itself describes the related art as comprising "a substrate, ... and a counter substrate are disposed to face each other with an electro-optical material, such as liquid crystal, interposed therebetween. More specifically, the substrates are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of the substrates are bonded to each other by a sealant so as to form an internal space, and the electro-optical material is sealed in the internal space." '913 patent, col. 1:16-25.

62. Similarly, *Ha* discloses that "[a] typical transmissive LCD device includes a liquid crystal panel," which "includes upper and lower substrates with a liquid crystal layer interposed therebetween," where "[t]he upper substrate includes a color filter, and the lower substrate includes thin film transistors (TFTs) as switching elements," (*Ha*, col. 1:21-26), and that "a typical reflective LCD device .

. . includes upper and lower substrates 8 and 10 with a liquid crystal layer 12 interposed” where “[t]he upper substrate 8 includes color filter layers 4a, 4b, and 4c . . . [and t]he lower substrate 10 includes a switching element,” (*Ha*, col. 1:49-55). *Ha*, Fig. 2. *Ha* also discloses a transfective LCD device in which color filter 104 is disposed at an upper substrate 106. *Ha*, col. 2:46-54, and Fig. 5. In all these LCD devices, a gap exists between the upper substrate (which includes the color filter) and the lower substrate (which includes TFT’s), where the gap is used to accommodate liquid crystal.



*(related art)*  
**FIG 2**



*(related art)*  
**FIG 5**

63. Therefore, to the extent *Adachi* does not already disclose to a POSITA a predetermined gap between its two substrates, it would be obvious to a POSITA to arrange the color filter substrate 26 of *Adachi* to face the array substrate 25 with a gap therebetween. A POSITA would have found it obvious to combine *Adachi* and their general knowledge that conventional LCDs have two substrates with a predetermined gap between them in which the liquid crystals are. Specifically, a POSITA would have found it obvious to implement their general knowledge of forming the gap between the substrates and structural layout of the pixel electrodes with *Adachi*'s display device. A POSITA would have been motivated to combine their general knowledge of the predetermined gap with *Adachi*'s display device in order to accommodate the liquid crystals such that the liquid crystals in the gap can be controlled by the pixel electrodes to orient as needed and hence the display device can display images. Further, a POSITA would have found it

straightforward to combine their general knowledge of forming the gap between the substrates and structural layout of the pixel electrodes with *Adachi*'s display device. Finally, as both *Adachi* and POSITA's general knowledge (such as that provided by the applicant-admitted prior art in the '913 patent and *Ha*) relate to LCDs and describe similar structures, combining the specific designs of a POSITA's general knowledge with *Adachi*'s display device would have yielded predictable results.

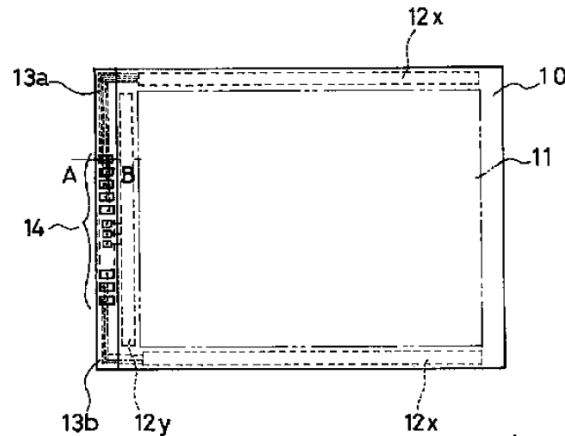
64. Accordingly, it is my opinion that *Adachi* teaches or renders obvious this limitation of claim 1.

**one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;**

65. A POSITA would understand *Adachi* discloses that the array substrate includes an extending portion that extends from the color filter substrate on one side in plan view.

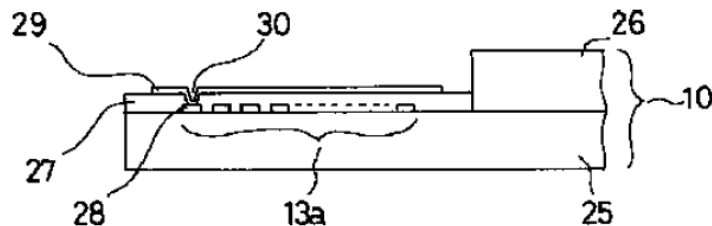
66. *Adachi* Figure 1 (below), which is a plan view, shows the array substrate has an extending portion that extends from the color filter substrate on one side (left side).

【図 1】



67. *Adachi* Figure 3 (below) discloses the extending portion of the array substrate 25 extends out from the color filter substrate 26.

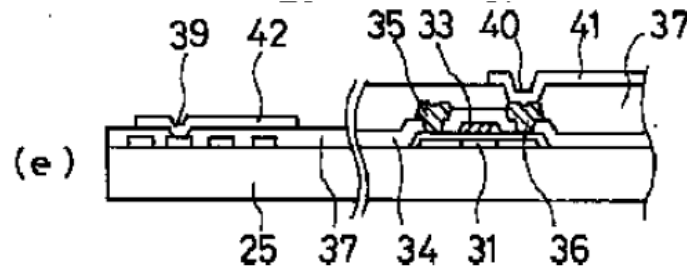
【図 3】



68. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

**display electrodes that are provided on the one substrate;**

69. A POSITA would understand *Adachi* display electrodes provided on an array substrate.



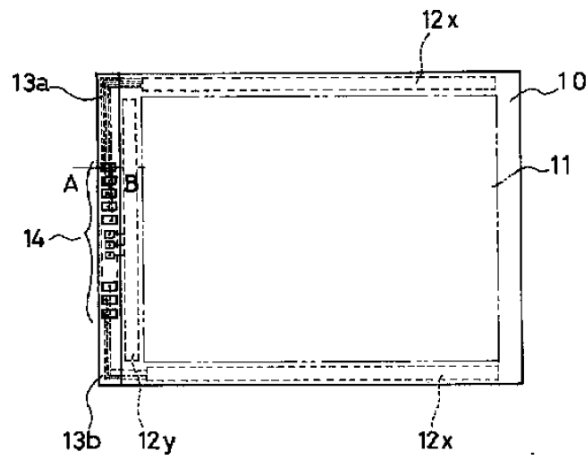
70. *Adachi* Figure 4(e) (above) discloses pixel (display) electrodes 41 that are provided on the array substrate 25. *Adachi*, ¶[0019].

71. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

**a circuit unit that is provided on the one substrate so as to drive the display electrodes;**

72. A POSITA would understand *Adachi* teaches a circuit unit provided on the array substrate that drives the display electrodes.

【图 1】

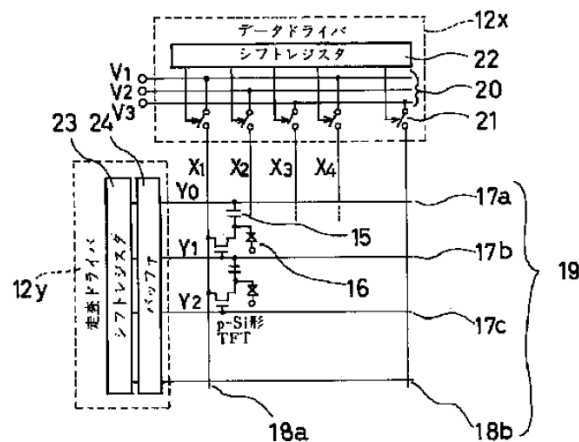


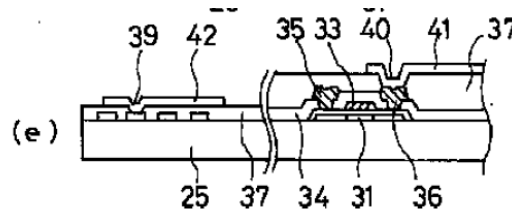
73. *Adachi* Figure 1 (above) depicts “the liquid crystal display element 10

has . . . drive circuits 12x and 12y that drive the liquid crystal display element 10 [and that] are integrated and built in a periphery of the display region 11,” where “the driving circuit 12x supplies image signals to the data lines 18a to 18b, and the driving circuit 12y supplies scanning signals to the scanning lines 17a to 17c.”  
*Adachi*, ¶[0015].

74. *Adachi* further discloses that “pixel TFTs . . . are arranged at intersections of the scanning lines 17a to 17c and the data lines 18a to 18b.”  
*Adachi*, ¶[0015]. *Adachi* Figure 2 (below) shows the drive circuits 12x, 12y supply signals to the TFTs via the scanning lines 17a-17c and the data lines 18a-18b. Further, *Adachi* Figure 4(e) (below) teaches the source electrode 36 of a TFT is electrically connected to the pixel electrode 41. Therefore, *Adachi* teaches drive circuits 12x, 12y (at least part of the circuit unit) drive the pixel electrodes 41 (the display electrodes), via the scanning lines 17a-17c, the data lines 18a-18b, and the TFTs.

【図 2】





75. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

**wiring lines for driving the circuit unit and the display electrodes;**

76. A POSITA would understand *Adachi* teaches wiring lines for driving the circuit unit and display electrodes.

77. *Adachi* teaches a “common wiring for supplying power to the scanning line drive circuit and a common wiring for supplying power to the signal line drive circuit.” *Adachi*, ¶[0007]. The wirings drive the drive circuits, so as to drive the display electrodes.

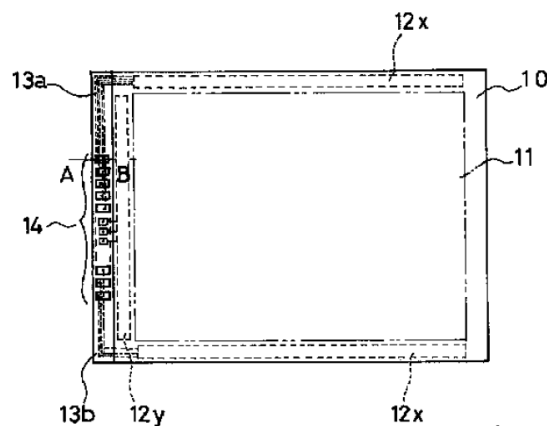
78. *Adachi* discloses a “plurality of common wirings connected to the scanning line drive circuit or the signal line drive circuit.” *Adachi*, ¶[0008]. *Adachi* discloses “wiring group 13a” and “wiring 28.” *Adachi*, ¶[0017], ¶[0035] (13b refers to a wiring group).

79. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

**a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and**

80. A POSITA would understand *Adachi* to teach a plurality of lead wiring lines on the extending portion that lead from one side of the wiring lines to the extending portion.

【図 1】



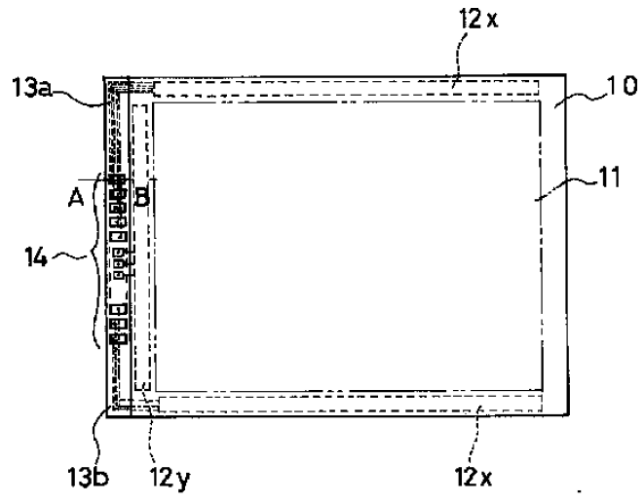
81. A POSITA would understand *Adachi* Figure 1 (above) teaches segments of the wirings in the wiring group 13a/13b are led from one of the sides of the wirings to the extending portion and extend on the extending portion.

82. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

**a plurality of external connecting terminals provided on the extending portion,**

83. A POSITA would understand *Adachi* discloses external connecting terminals.

【図 1】



84. *Adachi* discloses “external connection terminal group 14 including external connection terminals” including terminal 29. *Adachi*, ¶¶[0015], [0020]. *Adachi* Figure 1 (above) shows the plurality of terminals in the external connecting terminal group 14 are provided on the extending portion of the substrate 25.

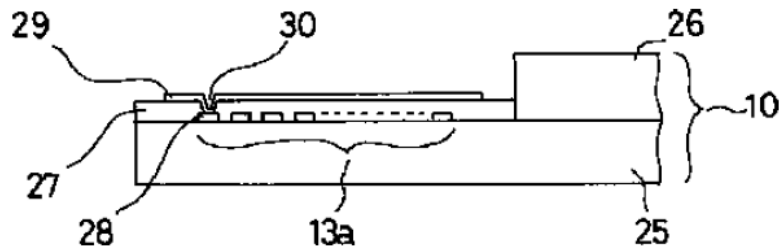
85. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

**each of the external connecting terminals overlapping with the plurality of lead wiring lines in plan view.**

86. A POSITA would understand *Adachi* discloses that the external connecting terminals overlap with the plurality of lead wiring lines in plan view.

87. *Adachi* teaches that “the external connection terminal 29 connected to the wiring 28 is arranged to cover all wirings of the wiring group 13a.” *Adachi*, ¶[0017]. *Adachi* Figure 3 (below) illustrates this teaching:

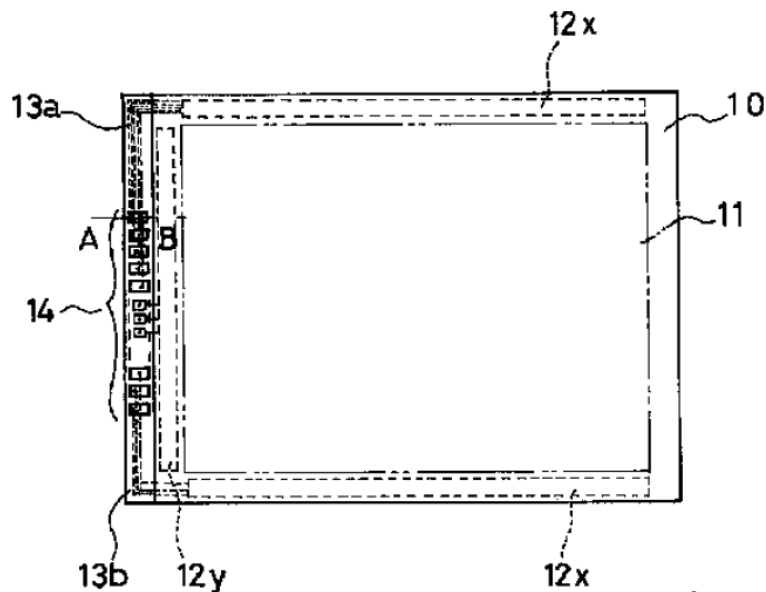
【図 3】



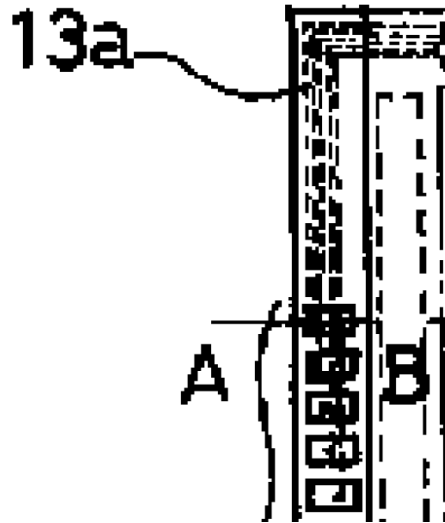
88. Figure 3 clearly shows external connection terminal 29 overlapping with all the lead wirings in the wiring group 13a.

89. In addition, *Adachi* Figure 1 (below) is a plan view that further teaches that the external connection terminals in the external connection terminal group 14 overlap with the lead wiring lines in the wiring group 13a/13b.

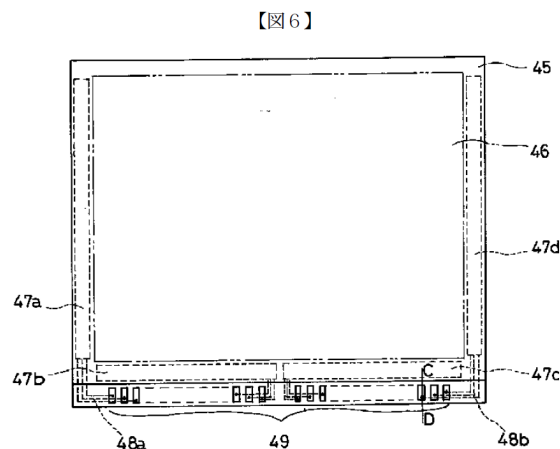
【図 1】



90. The below enlargement of the upper-left corner of Figure 1 clearly shows this arrangement.



91. *Adachi* Figure 6 (below) also teaches that the external connection terminals in the external connection terminal group overlap with the plurality of lead wiring lines in the wiring group 48a/48b. *Adachi*, ¶[0035].



92. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 1.

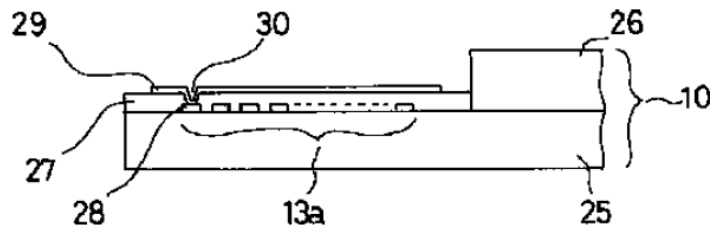
## 2. Claim 2

Claim 2 depends from claim 1 with the further limitation:

**wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween,**

93. A POSITA would understand *Adachi* to teach external connecting terminals and lead wiring lines that are laminated with an interlayer insulating film between them.

【図 3】



94. *Adachi* Figure 3 (above) teaches “the wiring group 13a formed on the array substrate 25 and connected to the drive circuit 12x is covered with the interlayer insulating film 27.” *Adachi*, ¶[0017]. In addition, the external connection terminals 29 are formed on the interlayer insulating film 27. Thus, in the liquid crystal display element 10 of *Adachi*, the external connection terminals 29 and the lead wiring lines (as segments of the wirings in the wiring group 13a/13b) are laminated with the interlayer insulating film 27 interposed therebetween.

95. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 2.

**each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.**

96. A POSITA would understand *Adachi* discloses that each external connecting terminal is electrically connected with a corresponding lead wiring line while being electrically isolated from the other lead wiring lines.

97. *Adachi* teaches that wiring 28 of the wiring group 13a and the external connection terminal 29 are electrically connected to each other via the contact hole 30 and a plurality of terminals each connected to one different wiring. *Adachi*, ¶[0017]. *Adachi* Figure 3 discloses that external connection terminal 29 shown is electrically isolated from others of the wirings in the wiring group 13a/13b by the interlayer insulating film 27.

98. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 2.

### **3. Claim 3**

Claim 3 depends from claim 1 with the further limitation:

**wherein the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and**

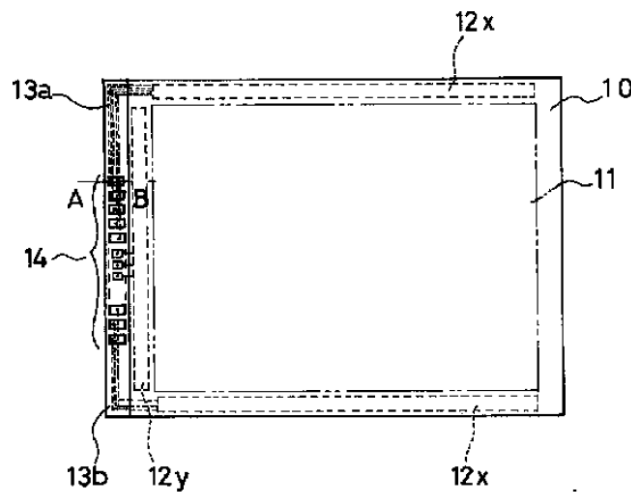
99. A POSITA would understand *Adachi* discloses external connecting terminals and lead wiring lines that are arranged in a direction along one side.

100. *Adachi* Figure 1 discloses the plurality of external connecting

terminals in the external connecting terminal group 14 are arranged along one edge of the extending portion of the substrate (in the up-down direction in the figure).

Further, *Adachi* claim 2 teaches that plurality of external connection terminals are arranged substantially linearly on the side of the insulating substrate.

【図 1】



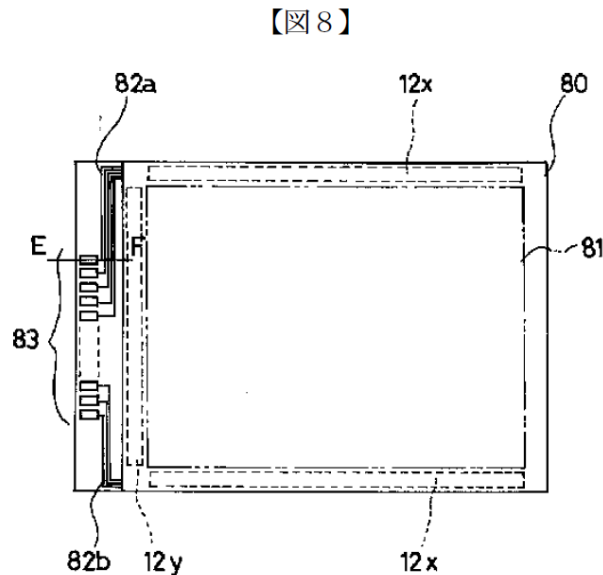
101. *Adachi* Figure 1 teaches the plurality of lead wiring lines (segments of the wirings in the wiring group 13a/13b) also extend in the up-down direction in the figure.

102. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 3.

**are correspondingly connected to edges of the external  
connecting terminals in a direction intersecting the direction  
along the one side.**

103. A POSITA would understand that *Adachi* teaches that the lead wiring lines are connected to the edges of the external connecting terminals in a

perpendicular manner, *i.e.*, in a direction that intersects the direction along the one side. For example, Figure 8 of *Adachi* shows the configuration of another example liquid crystal display element 80. As shown in Figure 8, the segments of wirings in wiring groups 82a and 82b (which correspond to the claimed “lead wiring lines”) extend in the up-down direction and eventually are connected to edges of corresponding external connection terminals in the external connection group 83 in a direction intersecting the up-down direction (the direction along the one side).



104. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 3.

**4. Claim 4**

**Claim 4 depends from claim 1 with the further limitation:**

**wherein the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and**

105. A POSITA would understand *Adachi* discloses this limitation for the reasons set forth in regard to claim 3.

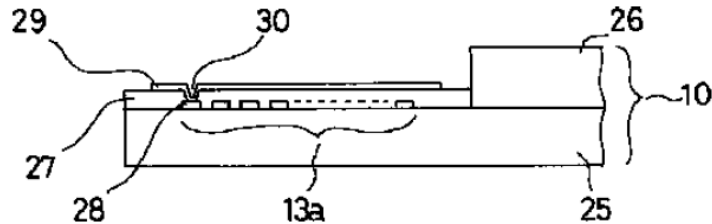
**are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.**

106. A POSITA would understand *Adachi* Figure 1 (enlarged version of which is reproduced below) discloses that the plurality of lead wiring lines (segments of the wirings in the wiring group 13a/13b) are correspondingly connected to the external connection terminals in the external connection terminal group 14 in a region where the segments of the wirings and the external connecting terminals intersect each other in plan view.



107. Further, *Adachi* Figure 3 teaches that the wiring 28 of the wiring group 13a and the external connection terminal 29 are electrically connected to each other via the contact hole 30. *Adachi*, ¶[0017].

【図 3】



108. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 4.

## 5. Claim 9

**An electronic apparatus comprising the electro-optical device according to claim 1.**

109. A POSITA would understand *Adachi* discloses a display device. Display device is an electronic apparatus. The display device of *Adachi* includes the liquid crystal display element 10.

110. Accordingly, it is my opinion that *Adachi* teaches claim 9.

## C. *Adachi* in Combination with *Takezawa* Renders Obvious Claim 8.

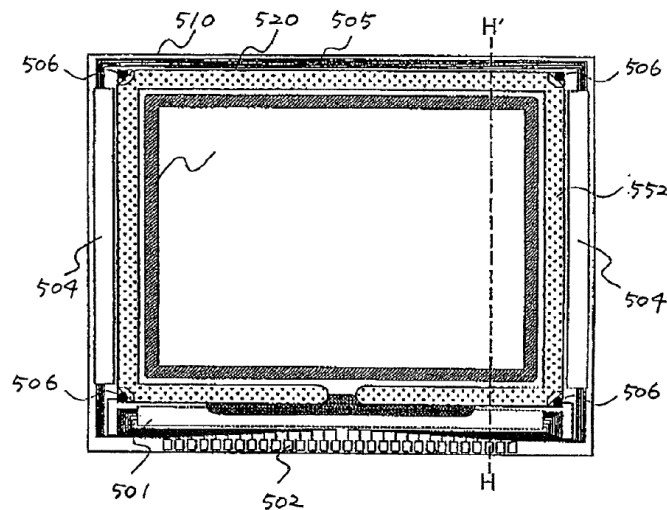
### 1. Claim 8

111. Claim 8 depends from claim 1 with the further limitation:

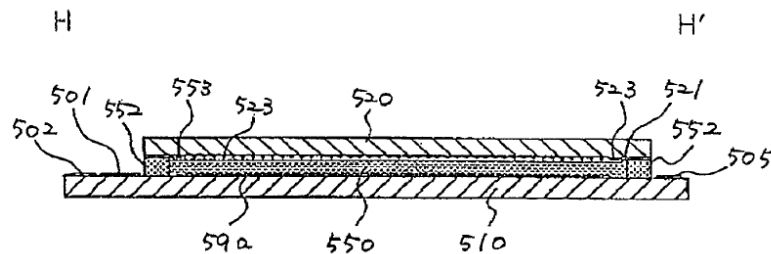
**a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and**

112. A POSITA would understand *Takezawa* teaches two opposing substrates that are sealed together such that an internal space is formed between them.

[FIG. 6]



[FIG. 7]



113. *Takezawa* Figure 7 (above) shows a liquid crystal panel that includes a base substrate 510 and a counter substrate 520. *Takezawa* explains that base and counter substrates are bonded together by a sealant to form a “space surrounded by the base substrate 510, the counter substrate 520, and the sealant 552.” *Takezawa*,

¶[0072]. As shown in FIG. 7, the sealant 552 bonds edges of opposite surfaces of the base substrate 510 and the counter substrate 520, and the internal space is formed between the base substrate 510 and the counter substrate 520. *Takezawa* discloses that the sealant 552 is provided on the base substrate 510 along the edges thereof. *Takezawa*, ¶[0073].

114. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 8.

**an electro-optical material that is held in the internal space,**

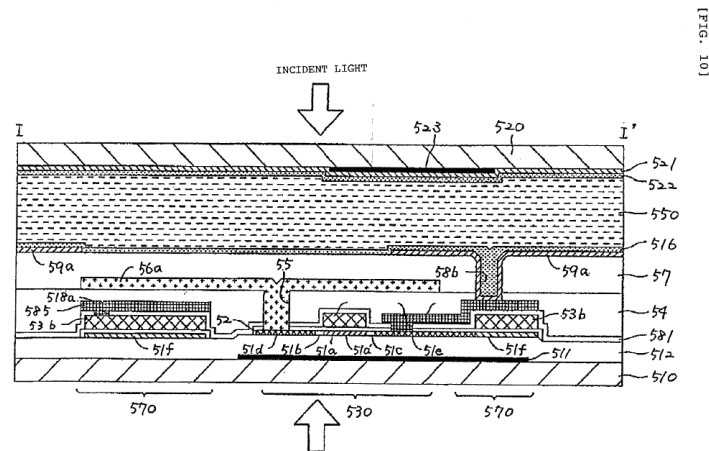
115. A POSITA would understand *Takezawa* discloses that liquid crystals 550 are sealed in the space surrounded by the base substrate 510, the counter substrate 520, and the sealant 552. *Takezawa*, ¶[0072].

116. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 9.

**wherein the display electrodes and a part of the circuit unit are disposed to face the internal space.**

117. A POSITA would understand that *Takezawa* Figure 10 (below) discloses pixel electrode 59a and various components of the circuit unit, such as TFT 530 and data line 56a, are disposed to face the internal space that holds the liquid crystals 550. These are the same components that the '913 patent identifies as part of the circuit unit: "electronic elements, such as TFTs or the like, the wiring lines, such as . . . data lines, and the like. . . correspond to a specified example of

‘circuit unit’.” ’913 patent, col. 7:56-61.



118. A POSITA would have found it obvious to combine *Adachi* and *Takezawa*. Specifically, a POSITA would have found it obvious to implement *Takezawa*’s formation of the gap between the substrates and structural layout of the pixel electrodes and circuit unit with *Adachi*’s display device. A POSITA would have been motivated to combine *Takezawa*’s structure with *Adachi*’s display device in order to accommodate the liquid crystals such that the liquid crystals in the gap can be controlled by the pixel electrodes to orient as needed and hence the display device can display images. Further, as both *Adachi* and *Takezawa* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Takezawa*’s formation of the gap between the substrates and structural layout of the pixel electrodes and circuit unit with *Adachi*’s display device. Finally, as both references relate to LCDs and describe similar structures, combining the specific structures of *Takezawa* with *Adachi*’s

display device would have yielded predictable results.

119. Accordingly, it is my opinion that *Adachi* and *Takezawa* renders obvious claim 8.

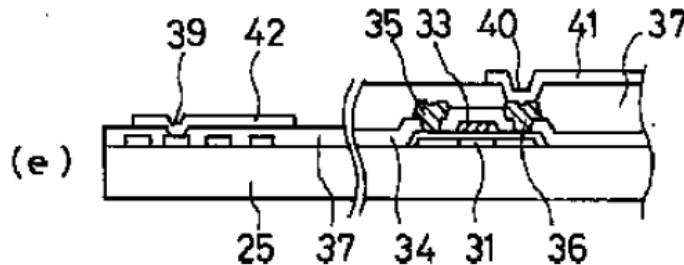
**D. *Adachi* In Combination with *Aruga* Renders Obvious Claim 10.**

**1. Claim 10**

Claim 10 depends from claim 2 with the further limitation:

**the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit,**

120. A POSITA would understand that *Adachi* discloses external connection terminals can be formed from the same film as a conductive film constituting the pixel electrode. For example, *Adachi* teaches that an ITO film can be formed and patterned to form pixel electrodes 41 and terminals 42. *Adachi*, ¶[0019], Fig. 4(e) (below).



121. A POSITA would understand that *Aruga* discloses an electro-optical device. *Aruga*, Title. *Aruga* further discloses that the electro-optical device includes “[a] chip connecting wiring 25 . . . serv[ing] to connect [a] data line 22 to

[an] X driver IC 52.” *Aruga*, ¶[0033]. These are the same components that the ’913 patent identifies as part of the circuit unit: “electronic elements, such as TFTs or the like, the wiring lines, such as . . . data lines, and the like. . . correspond to a specified example of ‘circuit unit’.” ’913 patent, col. 7:56-61. Therefore, the chip connecting wiring 25 can be considered part of the circuit unit.

122. *Aruga* further discloses that “the chip connecting wiring 25 is formed during a step for forming pixel electrodes 23; this step comprises patterning of [an] ITO layer” and “[a]ccordingly, the chip connecting wiring 25 is composed of ITO as is the pixel electrode 23.” *Aruga*, ¶[0033].

123. Thus, as *Adachi* discloses that the external connection terminals can be formed from the same film as the pixel electrode, and *Aruga* discloses that the pixel electrode can be formed from the same film as the chip connecting wiring, which is a conductive film constituting the circuit unit, it would be obvious to a POSITA to modify the teaching of *Adachi* to form the external connection terminals from the same film as a conductive film constituting the circuit unit.

124. A POSITA would have found it obvious to combine *Adachi* and *Aruga*. Specifically, a POSITA would have found it obvious to implement *Aruga*’s chip connecting wiring formed from the same film as a conductive film constituting the pixel electrode with *Adachi*’s display device in which the external connection terminals are formed from the same film as a conductive film

constituting the pixel electrode, resulting in the external connection terminals of *Adachi* being formed from the same film as the conductive film constituting the chip connecting wiring, which is part of the circuit unit. A POSITA would have been motivated to combine *Aruga*'s structure with *Adachi*'s display device in order to reduce the number of layers and processing steps and hence simplify manufacturing and reduce cost. Further, as both *Adachi* and *Aruga* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Aruga*'s structure with *Adachi*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining the specific structures of *Aruga* with *Adachi*'s display device would have yielded predictable results.

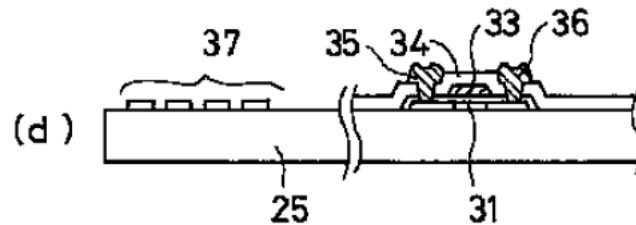
125. Accordingly, it is my opinion that *Adachi* in combination with *Aruga* teaches and render obvious this limitation of claim 10.

**and the lead wiring lines being formed from the same film as a second conductive film constituting the circuit unit.**

126. A POSITA would understand *Adachi* discloses lead wiring lines being made of the same film as a second conductive film constituting the circuit unit.

127. *Adachi* teaches that an aluminum layer can be formed, and patterned to form the drain electrode 35, the source electrode 36, and the wiring group 37 integrated with the signal line in the same process. *Adachi*, ¶[0019]. This is shown in *Adachi* Figure 4(d) below. The drain electrode 35 and the source electrode 36

are each a conductive film constituting the TFT.



128. Accordingly, it is my opinion that *Adachi* teaches this limitation of claim 10.

**E. *Sekado* Anticipates Claims 1-6 and 9.**

**1. Claim 1**

**1. An electro-optical device comprising:**

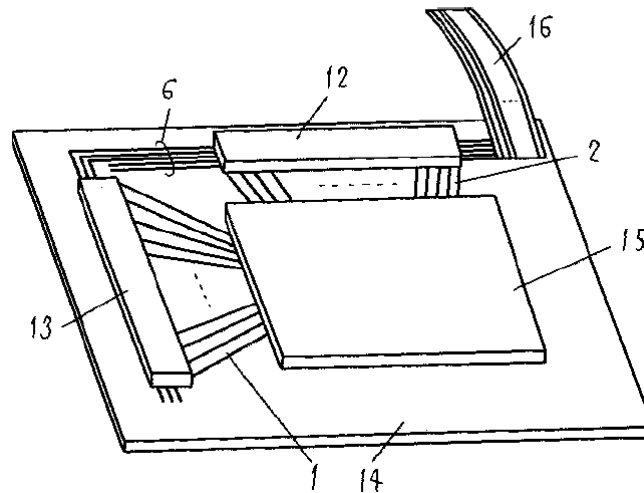
129. A POSITA would understand *Sekado* discloses a liquid crystal display device, which is an electro-optical device. *Sekado*, Title.

**a pair of substrates that are disposed to face each other with a predetermined gap therebetween,**

130. A POSITA would understand *Sekado* teaches a pair of substrates facing each other with a gap between them.

131. *Sekado* discloses an insulating substrate 14 and a color filter 15. *Sekado*, p. 3, l. 7-9; claim 1 (“a pair of substrates”). *Sekado* Figure 5 (below) teaches the insulating substrate 14 and color filter 15 are disposed to face each other. *Sekado* further discloses that “[l]iquid crystals are sealed in to a gap formed by a color filter 15 bonded to the insulating substrate 14.” *Sekado*, p. 3, l. 7-9.

【第5図】

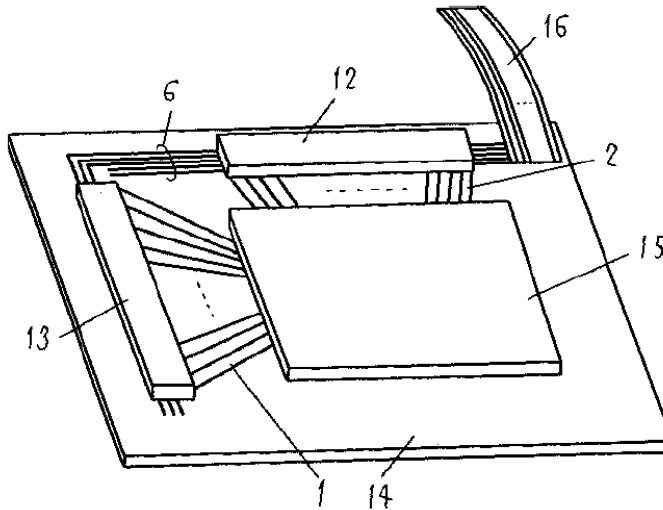


132. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;**

133. A POSITA would understand *Sekado* teaches that one of the substrates extends out on one side from the other substrate, when seen in plan view.

【第5図】



134. *Sekado* Figure 5 (above) discloses insulating substrate 14 has an extending portion that extends from the color filter 15 on one side (upper side).

135. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**display electrodes that are provided on the one substrate;**

136. A POSITA would understand *Sekado* to teach that the one substrate has display electrodes on it.

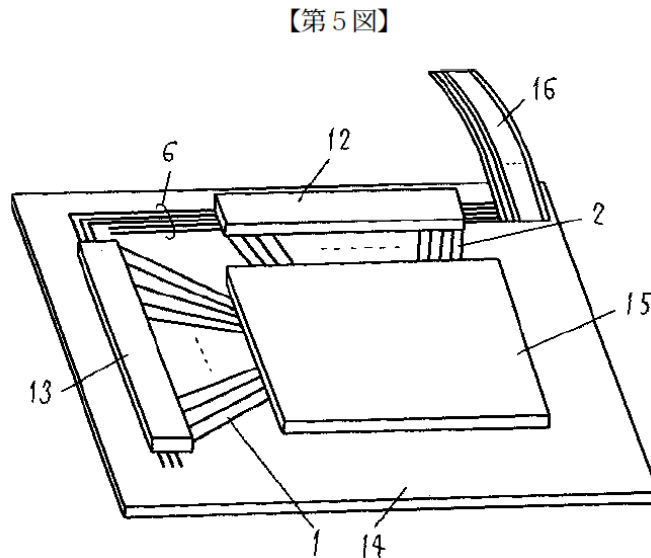
137. *Sekado* discloses an array of pixel electrodes arranged in a matrix, thin film transistors disposed close to and connected to the pixel electrodes, signal lines connected to source electrodes of the thin film transistors, and scanning lines connected to gate electrodes of the thin film transistors on one substrate of the substrates. *Sekado*, claim 1. Further, *Sekado* Figure 4 discloses an active liquid crystal circuit in which a switching element 3 of a field-effect transistor and a

liquid crystal cell 4 are arranged at each intersection of scanning lines 1 and signal lines 2 on an insulating substrate 14. *Sekado*, p. 2, ll. 40-42.

138. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**a circuit unit that is provided on the one substrate so as to drive the display electrodes;**

139. A POSITA would understand *Sekado* teaches that the one substrate has a circuit unit on it that drives the display electrodes.



140. *Sekado* discloses a circuit unit including various circuits/circuit components, such as a scanning line driving driver 13 and a signal line driving driver 12. *Sekado*, p. 2, l. 45. *Sekado* Figure 5 (above) discloses a scanning line driving driver 13 and a signal line driving driver 12 being on the insulating substrate 14.

141. *Sekado* further discloses that “[t]he signal line driving driver IC 12

and the scanning line driving driver IC 13 are respectively mounted and connected to the signal line 2 and the scanning line 1.” *Sekado*, p. 3, ll. 9-10. *Sekado* teaches a switching element 3 of a field-effect transistor and a liquid crystal cell 4 are arranged at each intersection of scanning lines 1 and signal lines 2 on an insulating substrate 14, and that the transistors (switching elements 3) are “connected to the pixel electrodes.” *Sekado*, p. 2, ll. 40-42; claim 1; Fig. 4. *Sekado* teaches driver ICs 12 and 13 “supply signals to the signal lines and the scanning lines on the substrate.” *Sekado*, claim 1. That is, in *Sekado*, the driver ICs 12 and 13 (*i.e.*, the circuit unit or part of the circuit unit) drive the pixel electrodes via the signal lines 2, the scanning lines 1, and the transistors 3.

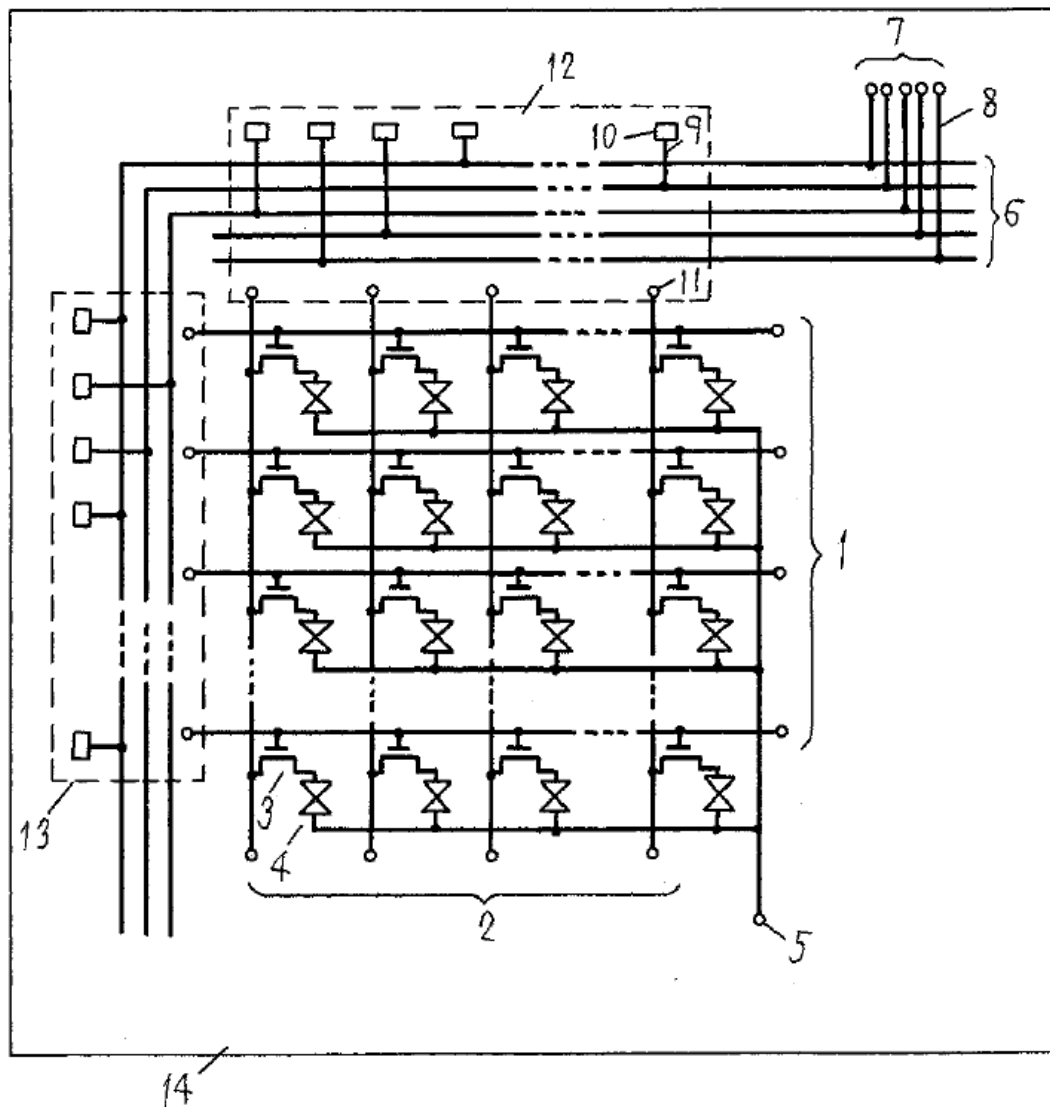
142. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**wiring lines for driving the circuit unit and the display electrodes;**

143. A POSITA would understand *Sekado* teaches wiring lines that are used for driving the circuit unit and display electrodes.

144. *Sekado* Figure 4 (below) discloses wirings 6 which are used to supply driving signals to the scanning line driver 13 and the signal line driver 12. *Sekado*, p. 2, ll. 44-45; Fig. 4. That is, in *Sekado*, the wirings 6 supply driving signals to the driver ICs 12 and 13 (*i.e.*, the circuit unit or part of the circuit unit), and also supply driving signals to the pixel electrodes via the driver ICs 12 and 13.

【第4図】

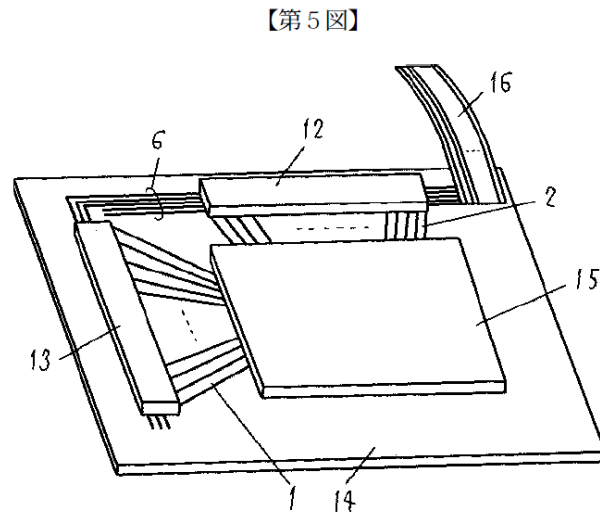
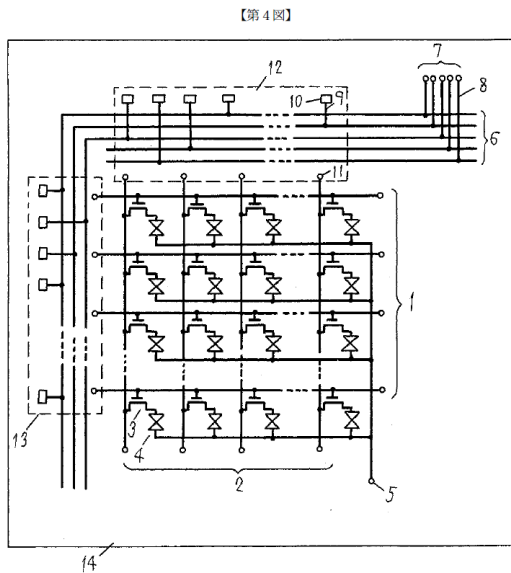


145. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and**

146. A POSITA would understand *Sekado* discloses a plurality of lead wiring lines that are on the extending portion of the one substrate and that led from

one side of the wiring lines to the extending portion.



147. *Sekado* Figures 4 and 5 (above) disclose that segments of wirings 6 that are used to provide driving signals to the drivers are provided on the extending portion and are led from one of the sides of the wirings to the extending portion.

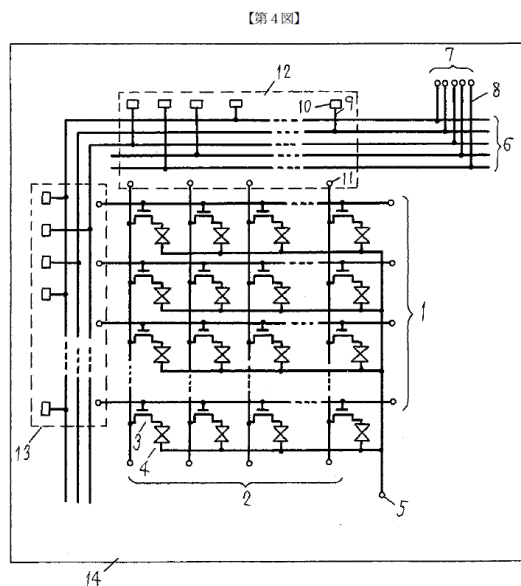
148. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**a plurality of external connecting terminals provided on the extending portion,**

149. A POSITA would understand *Sekado* discloses a plurality of external connecting terminals on an extending portion of one substrate.

150. For example, *Sekado* discloses connection terminals 10 and extraction wirings 9 for connecting the lead line wirings (segments of wirings 6) to the connection terminals 10. A connection terminal 10 and a corresponding extraction wiring 9 form an external connecting terminal.

151. *Sekado* Figure 4 (below) discloses that the location of the connection terminals 10 and the extraction wirings 9 overlaps with the location of the driver IC 12. *Sekado* Figure 4 (below) discloses that the driver IC 12 is provided on the extending portion. Therefore, the connection terminals 10 and the extraction wirings 9 (the external connecting terminals) are provided on the extending portion.



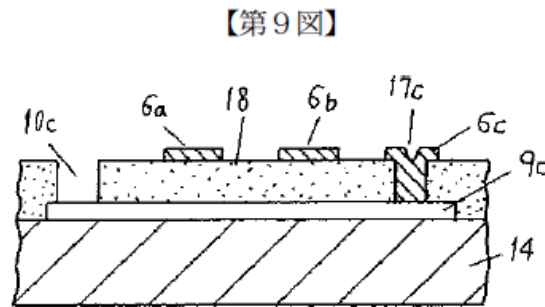
152. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

**each of the external connecting terminals overlapping with the plurality of lead wiring lines in plan view.**

153. A POSITA would understand *Sekado* teaches that each of the external connecting terminals overlap with the plurality of lead wiring lines in plan view.

154. *Sekado* Figure 4 discloses that the external connecting terminals (pairs of connection terminal 10 and extraction wiring 9) overlap with the lead wiring

lines (segments of wirings 6) in plan view. *Sekado* Figure 9 provides a cross-sectional view in which 10c and 9c are an example of the external connecting terminal and 6a-6c are examples of the lead wiring lines. *Sekado*, p. 4, ll. 30-31.



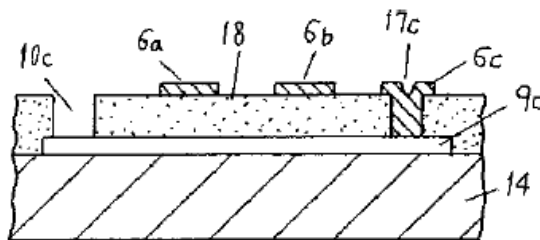
155. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 1.

## 2. Claim 2

**The electro-optical device according to claim 1, wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween,**

156. A POSITA would understand *Sekado* to teach external connecting terminals and lead wiring lines that are laminated with an interlayer insulating film between them.

【第9図】



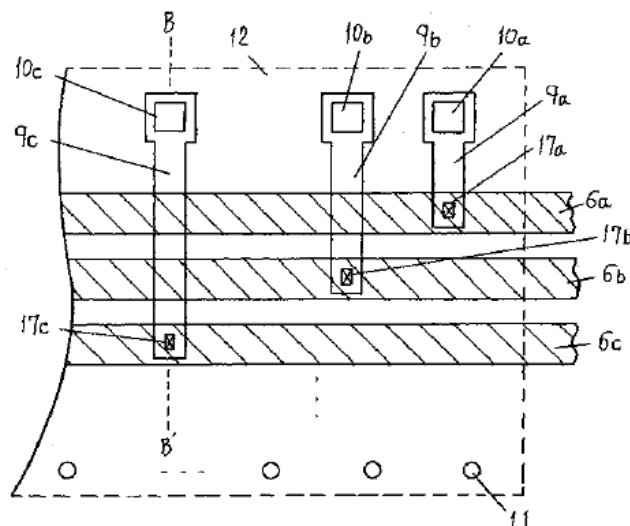
157. *Sekado* Figure 9 (above) discloses the connection terminal 10c/extraction wiring 9c (the external connecting terminal) and the segments of wirings 6a-6c (lead wiring lines) are laminated with an insulating layer 18 interposed therebetween. *Sekado*, p. 3, ll. 21-24.

158. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 2.

**each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.**

159. A POSITA would understand *Sekado* to teach that each external connecting terminal is electrically connected with a corresponding lead wiring line while being electrically isolated from the other lead wiring lines..

【第8図】



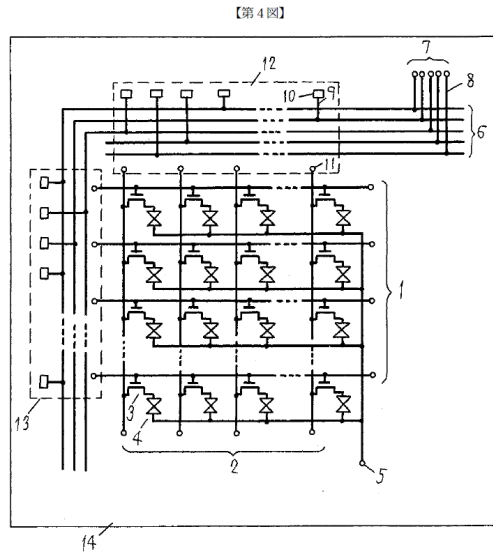
160. *Sekado* Figure 8 (above) discloses that wirings 6-a, b, c and the driver side extraction wirings 9-a, b, c are electrically connected by contacts 17-a, b, c, respectively. *Sekado*, p. 3, ll. 20-21. As set forth above, *Sekado* Figure 9 teaches that the extraction wiring 9c is electrically connected with corresponding wiring 6c and is electrically isolated from wirings 6a and 6b by the insulating layer 18.

161. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 2.

### 3. Claim 3

**The electro-optical device according to claim 1, wherein the plurality of external connecting terminals are arranged in a direction along the one side, and**

162. A POSITA would understand *Sekado* a plurality of external connecting terminals arranged along one side in a direction.



163. *Sekado* Figure 4 discloses a plurality of external connecting terminals (extraction wirings 9/connection terminals 10) are arranged in left-right direction, *i.e.*, a direction along the upper side (the one side).

164. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 3.

**the plurality of lead wiring lines extend in the direction along the one side and**

165. A POSITA would understand *Sekado* Figure 4 to disclose a plurality of lead wiring lines (segments of the wirings 6) that extend in the left-right direction *i.e.*, a direction along the upper side (the one side).

166. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 3.

**are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.**

167. A POSITA would understand *Sekado* Figures 4 and 8 disclose that each lead wiring line (segment of wiring 6) is connected to an edge of a corresponding external connecting terminal (extraction wiring 9/connection terminal 10), where the edge is an edge in an up-down direction i.e., a direction intersecting the left-right direction in FIGs. 4 and 8 (the direction along the one side). *Sekado*, Figs. 4, 8.

168. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 3.

#### **4. Claim 4**

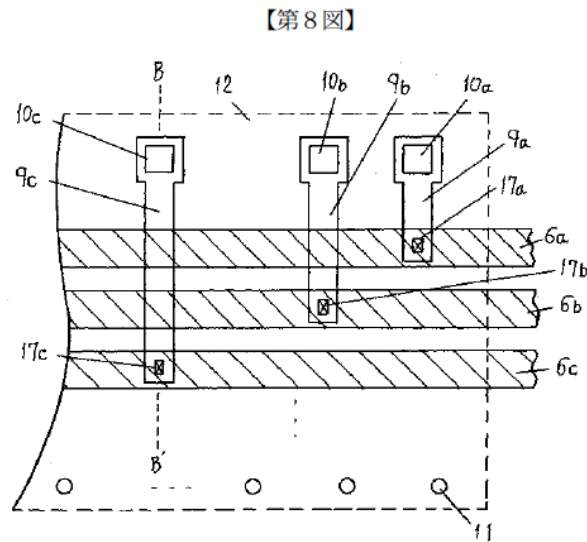
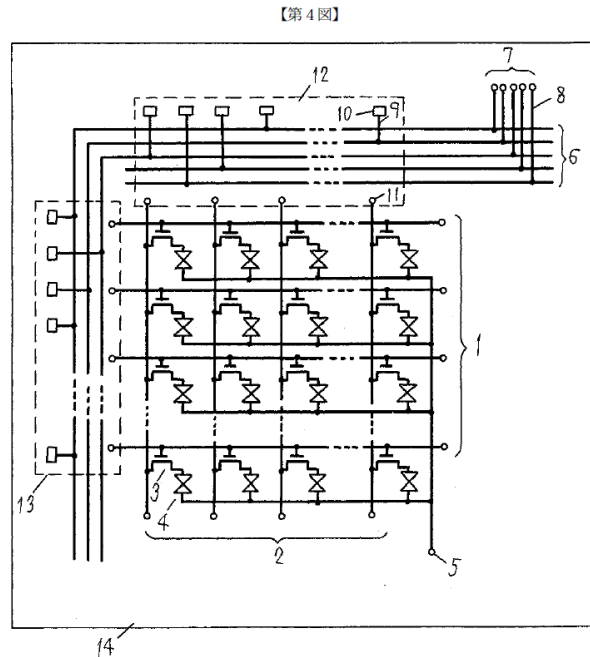
**The electro-optical device according to claim 1, wherein the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and**

169. A POSITA would understand *Sekado* discloses this limitation as set forth above in regard to claim 3.

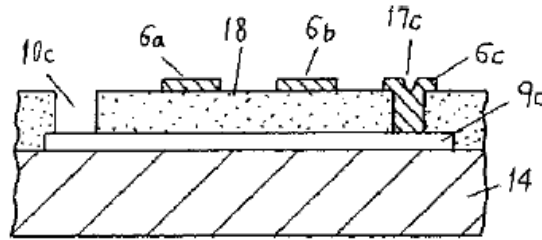
**are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.**

170. A POSITA would understand *Sekado* Figure 8 (below) discloses driver wirings 6-a, b, c and driver side extraction wirings 9-a, b, c that are electrically connected by contacts 17-a, b, c, respectively. *Sekado*, p. 3, ll. 18-21.

*Sekado* Figures 4 and 8 teach that each lead wiring line (segment of wiring 6) is connected to a corresponding external connecting terminal (extraction wiring 9/connection terminal 10) in a region where they intersect each other in plan view. *Sekado*, Figs. 4, 8, 9 (below).



【第9図】



171. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 4.

**5. Claim 5**

**An electro-optical device comprising:**

172. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**a pair of substrates that are disposed to face each other with a predetermined gap therebetween,**

173. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;**

174. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**display electrodes that are provided on the one substrate;**

175. A POSITA would understand *Sekado* discloses this limitation as set

forth in regard to claim 1.

**a circuit unit that is provided on the one substrate so as to drive the display electrodes;**

176. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**wiring lines for driving the circuit unit and the display electrodes;**

177. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and**

178. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**a plurality of external connecting terminals provided on the extending portion,**

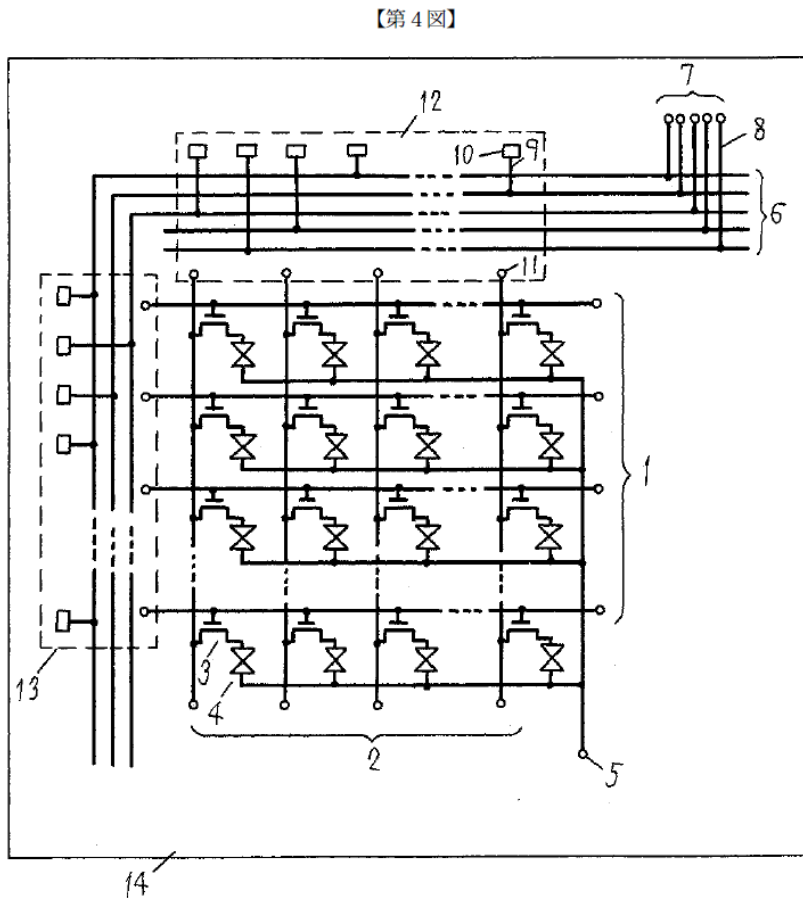
179. A POSITA would understand *Sekado* discloses this limitation as set forth in regard to claim 1.

**each of the external connecting terminals overlapping with the circuit unit in plan view.**

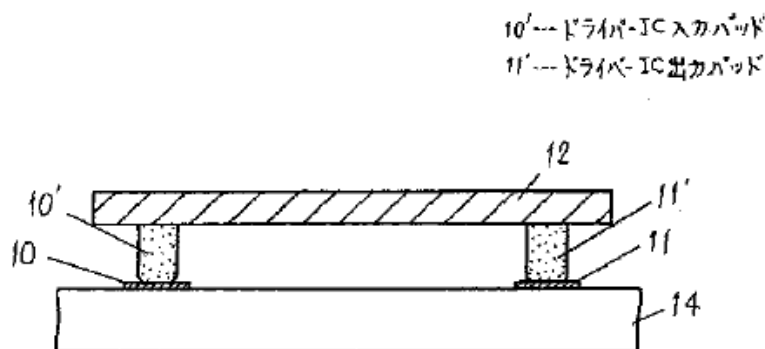
180. A POSITA would understand *Sekado* discloses external connecting terminals that overlap with the circuit unit in plan view.

181. *Sekado* Figure 4 (below) teaches that the external connecting terminals (pairs of connection terminal 10 and extraction wiring 9) overlap with

the circuit unit (e.g., signal line driving driver 12) in plan view. Similarly, *Sekado* Figure 7 (below) discloses the external connecting terminals (pairs of connection terminal 10 and extraction wiring 9) overlapping with the circuit unit.



【第7図】



182. Accordingly, it is my opinion that *Sekado* teaches this limitation of

claim 5.

**6. Claim 6**

**The electro-optical device according to claim 5,**

**wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and**

183. A POSITA would understand *Sekado* discloses a circuit unit which is driven by an image signal that is provided by an electrical connection to terminals for supplying an image signal among a plurality of external connecting terminals.

184. *Sekado* discloses a signal line connected to driver 12, which is a driving circuit. *Sekado*, p. 3, ll. 15-16. *Sekado* Figure 4 teaches that the connection terminals 10 are connected via the extraction wirings 9 to wirings 8, which supply signals to the driver wirings 6. *Sekado*, p. 3, l. 2. Thus, the signals are supplied to the connection terminals 10/extraction wirings 9 via the wirings 8 and 6, and the connection terminals 10/extraction wirings 9 supply the signals to and drive the signal line connected to driver 12.

185. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 6.

**at least a part of the driving circuit overlaps the external connecting terminals in plan view.**

186. A POSITA would understand *Sekado* Figures 4 and 7 disclose a part of the signal line connecting to driver 12 overlaps the connection terminals

10/extraction wirings 9 in plan view.

187. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 6.

**7. Claim 9**

**An electronic apparatus comprising the electro-optical device according to claim 1.**

188. A POSITA would understand *Sekado* discloses using “a liquid crystal display device that can obtain a good television image.” *Sekado*, p. 2, l. 25. Thus, *Sekado* discloses an apparatus (television) that includes the electro-optical device of claim 1.

189. Accordingly, it is my opinion that *Sekado* teaches claim 9.

**F. *Sekado* in Combination with *Aruga* Renders Obvious Claim 7.**

**1. Claim 7**

**The electro-optical device according to claim 5,  
wherein the external connecting terminals and the part of the  
circuit unit are laminated with an interlayer insulating film  
interposed therebetween,**

190. A POSITA would understand *Sekado* in combination with *Aruga* to teach external connecting terminals and a circuit unit being laminated with an interlayer insulating film between them.

191. *Sekado* teaches that:

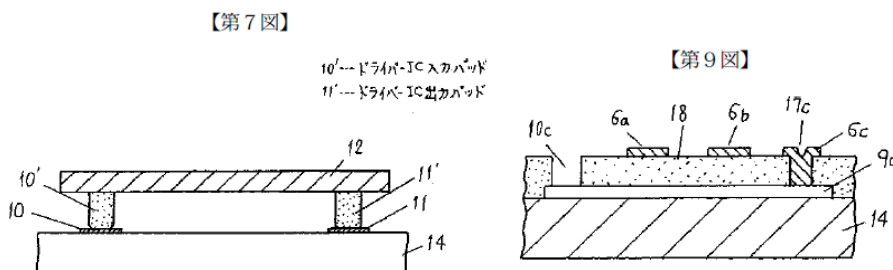
“FIG. 7 is a sectional view of the signal line driving driver 12 of FIG. 6 when mounted on and connected to the insulating substrate

14. Here, the driver IC input pad 10' is mounted and connected to the driver IC input connection terminal 10, and the driver IC output pad 11' is mounted and connected to the driver IC output connection terminal 11.

FIG. 8 shows an actual state of the driver driving wirings 6-a, b, c and the driver driving side extraction wirings 9-a, b, c when the driver IC input pads are arranged as shown in FIG. 6. Here, the driver driving wirings 6-a, b, c and the driver driving side extraction wirings 9-a, b, c are electrically connected by contacts 17-a, b, c, respectively. FIG. 9 is a cross-sectional view taken along line B-B' of FIG. 8. The driver driving side extraction wirings 9-a, b, c are formed on the insulating substrate 14, and the driver driving wirings 6-a, b, c are formed thereon with an insulating layer 18 interposed.

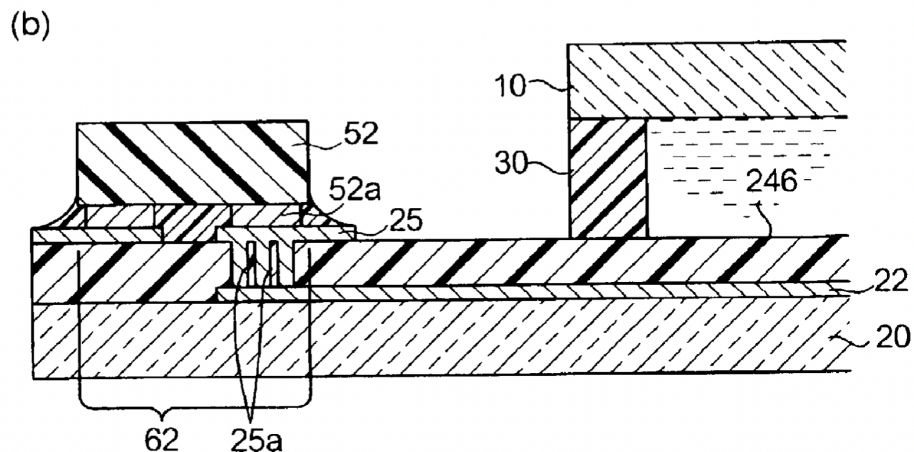
*Sekado*, p. 3, l. 13-24.

192. As seen in *Sekado* Figure 7 (below), a signal line connected to driver 12 is formed over an external connecting terminal. Further, *Sekado* Figure 9 teaches an insulating layer 18 is formed on the external connecting terminal (connection terminal 10/extraction wiring 9).



193. That is, in *Sekado*, an interlayer insulating film (insulating layer 18) is interposed between the external connecting terminals (connection terminals 10/extraction wirings 9) and the part of the circuit unit (signal line connected to driver 12) that overlaps with the external connecting terminals.

194. Further, a POSITA would understand that *Aruga* discloses: “A resin or mold seals the connecting portion between the X driver IC 52 and the chip connecting wiring 25” (para. [0044]), thus “moisture is inhibited from reaching the data lines 22 through the contact holes 25a and corrosion of the data lines 22 can be reliably prevented” (para. [0045]). In *Aruga*, layer 246 is also an insulating layer, similar to layer 18 in *Sekado*. Thus, *Aruga*’s underling conducting layer 22 and IC 52 are laminated with an interlayer insulating film (resin+layer 246) interposed therebetween. *Aruga*, Fig. 7(b) (below).



195. Thus, a POSITA would have found it obvious to combine *Sekado* and *Aruga*. Specifically, a POSITA would have found it obvious to implement *Aruga*’s insulating layer in between *Sekado*’s insulating interlayer 18 and part of the circuit unit 12 of *Sekado*’s display device. A POSITA would have been motivated to combine *Aruga*’s insulating layer into *Sekado*’s display device in order to inhibit moisture and prevent corrosion in the wires, terminals and circuit

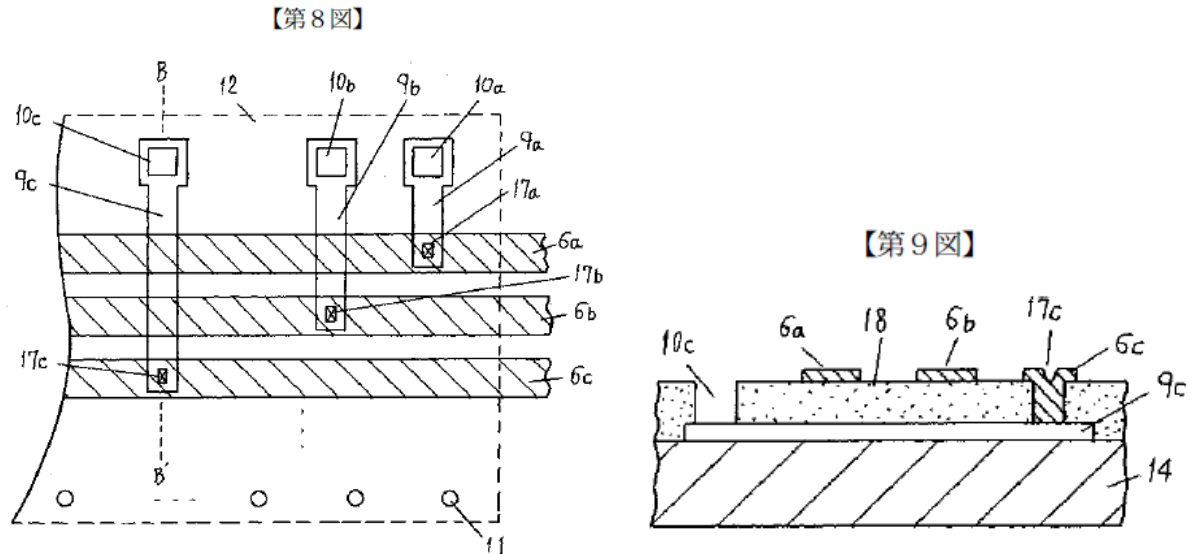
unit as taught by *Aruga*. Further, as both *Sekado* and *Aruga* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Aruga*'s insulating layer in between *Sekado*'s insulating interlayer 18 and part of the circuit unit 12 of *Sekado*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining the specific structures of *Aruga* with *Sekado*'s display device would have yielded predictable results.

196. Accordingly, it is my opinion that *Sekado* in combination with *Aruga* teaches and renders obvious this limitation.

**each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.**

197. A POSITA would understand *Sekado* discloses each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.

198. *Sekado* discloses wirings 6-a, b, c and driver side extraction wirings 9-a, b, c are electrically connected by contacts 17-a, b, c, respectively. *Sekado*, p. 3, ll. 20-21; Fig. 8 (below). *Sekado* Figure 9 (below) teaches that the extraction wiring 9c is electrically connected with corresponding wiring 6c and is electrically isolated from wirings 6a and 6b by the insulating layer 18.



199. Accordingly, it is my opinion that *Sekado* teaches this limitation of claim 7.

**G. *Sekado* Renders Obvious in Combination with *Takezawa* Claim 8.**

**1. Claim 8**

**The electro-optical device according to claim 1, further comprising:**

**a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and**

200. A POSITA would understand that *Sekado* teaches two opposing substrates that are sealed together such that an internal space is formed between them.

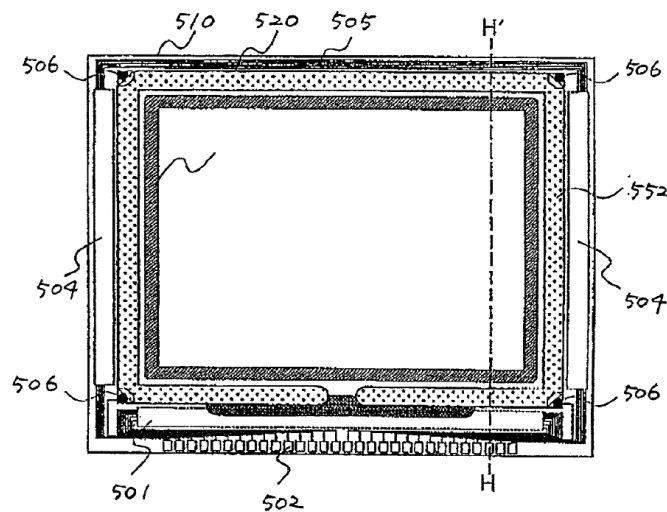
201. *Sekado* teaches that “[l]iquid crystals are sealed in to a gap formed by a color filter 15 bonded to the insulating substrate 14.” *Sekado*, p. 3, ll. 7-8.

Although *Sekado* does not explicitly mention a “sealant,” a POSITA would

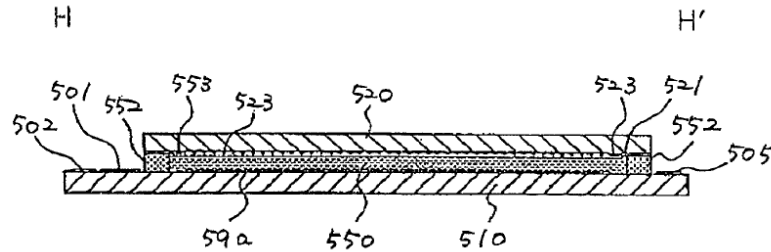
understand “bonded” to mean closed together with a sealant. An internal space between the color filter 15 and the insulating substrate 14 is inherent to accommodate the liquid crystal. Notably, the ’913 patent itself describes the related art as comprising “a substrate, ... and a counter substrate are disposed to face each other with an electro-optical material, such as liquid crystal, interposed therebetween. More specifically, the substrates are disposed to face each other with a predetermined gap therebetween and edges of opposite surfaces of the substrates are bonded to each other by a sealant so as to form an internal space, and the electro-optical material is sealed in the internal space.” ’913 patent, col. 1:16-25.

202. Alternatively, *Takezawa* discloses a liquid crystal panel (an electro-optical device) that includes a pair of substrates and a sealant bonding edges of opposite surfaces of the pair of substrates to form an internal space.

[FIG. 6]



[FIG. 7]



203. *Takezawa* Figure 7 (above) shows a liquid crystal panel that includes a base substrate 510 and a counter substrate 520. *Takezawa* explains that base and counter substrates are bonded together by a sealant to form a “space surrounded by the base substrate 510, the counter substrate 520, and the sealant 552.” *Takezawa*, ¶[0072]. As shown in FIG. 7, the sealant 552 bonds edges of opposite surfaces of the base substrate 510 and the counter substrate 520, and the internal space is formed between the base substrate 510 and the counter substrate 520. *Takezawa* discloses that the sealant 552 is provided on the base substrate 510 along the edges thereof. *Takezawa*, ¶[0073].

204. Accordingly, it is my opinion that *Sekado* discloses this limitation of claim 8. Alternatively, *Sekado* in combination with *Takezawa* renders obvious this limitation of claim 8.

**an electro-optical material that is held in the internal space,**

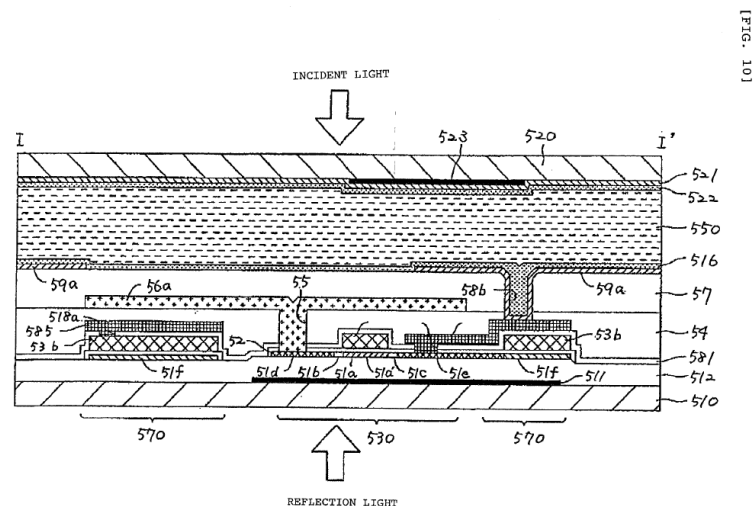
205. A POSITA would understand that *Sekado* alone teaches: “Liquid crystals are sealed in to a gap formed by a color filter 15 bonded to the insulating substrate 14.” *Sekado*, p. 3, ll. 7-8.

206. Similarly, *Takezawa* discloses that liquid crystals 550 are sealed in the space surrounded by the base substrate 510, the counter substrate 520, and the sealant 552. *Takezawa*, ¶[0072].

207. Accordingly, it is my opinion that *Sekado* discloses this limitation of claim 8. Alternatively, *Sekado* in combination with *Takezawa* renders obvious this limitation of claim 8.

**wherein the display electrodes and a part of the circuit unit are disposed to face the internal space.**

208. A POSITA would understand that *Takezawa* Figure 10 (below) discloses pixel electrode 59a and various components of the circuit unit, such as TFT 530 and data line 56a, are disposed to face the internal space that holds the liquid crystals 550. According to the '913 patent, "electronic elements, such as TFTs or the like, the wiring lines, such as . . . data lines, and the like. . . correspond to a specified example of 'circuit unit'." '913 patent, col. 7:56-61.



209. A POSITA would have found it obvious to combine *Sekado* and *Takezawa*. Specifically, a POSITA would have found it obvious to implement *Takezawa*'s sealant to form internal space between the substrates with *Sekado*'s display device. A POSITA would have been motivated to combine *Takezawa*'s structure with *Sekado*'s display device in order to seal the liquid crystals in the internal space. Further, as both *Sekado* and *Takezawa* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Takezawa*'s structure to apply a sealant to bond edges of opposite surfaces of the pair of substrates to each other to form an internal space between the pair of substrates with *Sekado*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining the specific structures of *Takezawa* with *Sekado*'s display device would have yielded predictable results.

210. Accordingly, it is my opinion that *Sekado* in combination with *Takezawa* renders obvious claim 8.

**H. *Sekado* Renders Obvious in Combination with *Kim* Claims 10-11.**

**1. Claim 10**

**The electro-optical device according to claim 2,**

**the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit, and the lead wiring lines being formed from the same film as a second conductive film constituting the circuit unit.**

211. A POSITA would understand that *Kim* discloses a liquid crystal

display device. *Kim*, Title. The liquid crystal display device “ha[s] a driving circuit” and “an outer circuit and the driving circuit are connected to each other by a pad.” *Kim*, col. 1:27-29. The pads of *Kim* are external connecting terminals.

212. *Kim* discloses a plurality of pads 41, and wires 42 connected to each of a plurality of the pads 41, which are formed in a connecting part of outer circuit 40. *Kim*, col. 3:64-67. Further, *Kim* teaches the pads located at the side portions of the connecting part are arranged in a row-like fashion and connected to the driving circuit by the first wire 42 which is bent or angled toward the driving circuit at a certain point or region. *Kim*, col. 4:14-18. *Kim* discloses a first wire 42 that extends in a direction perpendicular to the pad 41. *Kim*, col. 4:67-5:1. At least the segments of the wires 42 connected to the pads 41 constitute lead wiring lines. As shown in, e.g., FIGs. 4 and 5 of *Kim*, which are plan views, the pads 41 overlap with the segments of the plurality of wires 42.

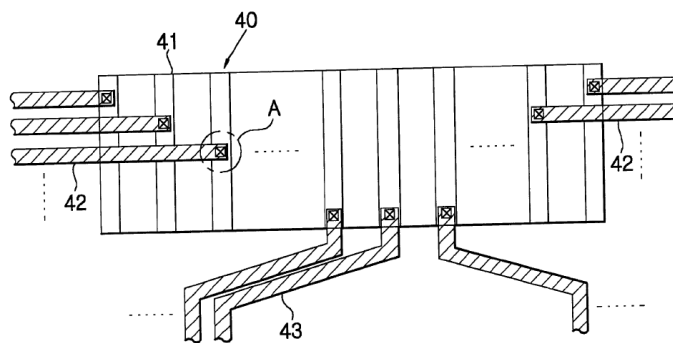


FIG.5

213. That is, *Kim* discloses a configuration similar to that of *Sekado*, in which the external connecting terminals overlap with the lead wiring lines in plan

view.

214. In addition, pad 101 in *Kim* Figures 10 and 11A corresponds to pad 41 in *Kim* Figure 5 and constitutes an external connecting terminal, and wire 105 in Figures 10 and 11A corresponds to wire 42 in Figure 5 and constitutes a lead wiring line. *Kim* Figure 11A discloses the lead wiring line (wire 105) is above the external connecting terminal (pad 101), which is similar to the structure in *Sekado*. *Sekado*, Fig. 9.

215. According to *Kim*, “pad 101 is formed preferably by photolithography after a first conductive layer has been formed,” where “[t]he first conductive layer is used in forming source and drain electrodes or the data line.” *Kim*, col. 6:27-33; claim 5. Further, *Kim* teaches that “first wire 105 is formed preferably by photolithography after a second conductive layer has been formed,” where “[t]he second conductive layer is used in forming the gate electrode or the gate line.” *Kim*, col. 6:37-43; claim 6.

216. A POSITA would have found it obvious to combine *Sekado* and *Kim*. Specifically, a POSITA would have found it obvious to implement *Kim*’s method of using two conductive layers to form the wirings 6 and the connection terminals 10/extraction wirings 9 of *Sekado* from the same films as the two conductive films (first conductive film and second conductive film) constituting the circuit unit, respectively, with *Sekado*’s display device. A POSITA would have been

motivated to combine *Kim*'s method with *Sekado*'s display device in order to reduce the number of layers and processing steps and hence simplify manufacturing and reduce cost. Further, as both *Sekado* and *Kim* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Kim*'s method to create the structure of *Sekado*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining the method of *Kim* with *Sekado*'s display device would have yielded predictable results.

217. Accordingly, it is my opinion that *Sekado* in combination with *Kim* renders obvious claim 10.

## 2. Claim 11

**The electro-optical device according to claim 7,  
the external connecting terminals being formed from the same  
film as a first conductive film constituting the circuit unit.**

218. A POSITA would understand that, as set forth in regard to claim 10, *Kim* discloses a configuration similar to that of *Sekado*, in which the external connecting terminals overlap with the lead wiring lines in plan view.

219. According to *Kim*, "pad 101 is formed preferably by photolithography after a first conductive layer has been formed," where "[t]he first conductive layer is used in forming source and drain electrodes or the data line." *Kim*, col. 6:27-33; claim 5. That is, *Kim* discloses that the pad 101 (external connecting terminal) is formed from the same film as a conductive film constituting the circuit unit.

220. For the reasons set forth in regard to claim 10, a POSITA would have combined the method of *Kim* with *Sekado*'s device.

221. Accordingly, it is my opinion that *Sekado* in combination with *Kim* renders obvious claim 11.

**I. *Takezawa* in Combination with *Kim* Renders Obvious Claims 1-4 and 8-10.**

**1. Claim 1**

**An electro-optical device comprising:**

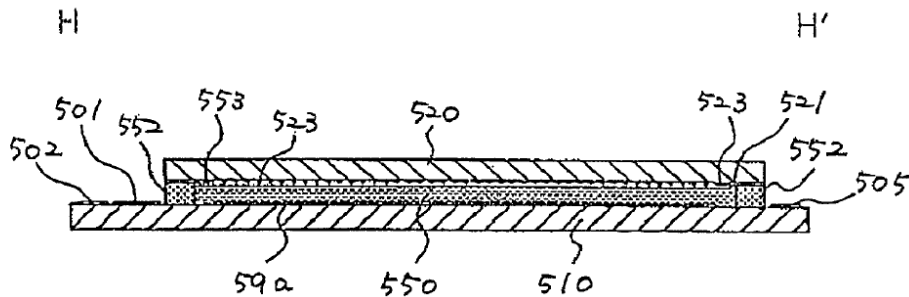
222. A POSITA would understand that *Takezawa* discloses a liquid crystal panel 411, which is an electro-optical device. *Takezawa*, ¶[0071], Figs. 6, 7.

223. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**a pair of substrates that are disposed to face each other with a predetermined gap therebetween,**

224. A POSITA would understand that *Takezawa* teaches two opposing substrates with a predetermined gap between them.

[FIG. 7]



225. *Takezawa* Figure 7 discloses a liquid crystal panel includes a base

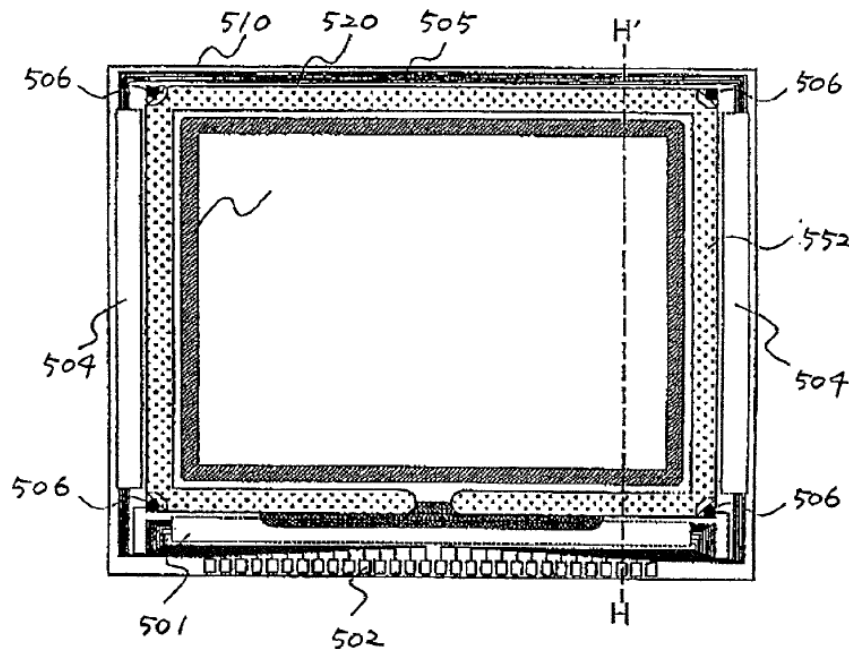
substrate 510 and a counter substrate 520, which are disposed to face each other with a predetermined gap between them. *Takezawa*, ¶[0072].

226. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;**

227. A POSITA would understand that *Takezawa* discloses one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view.

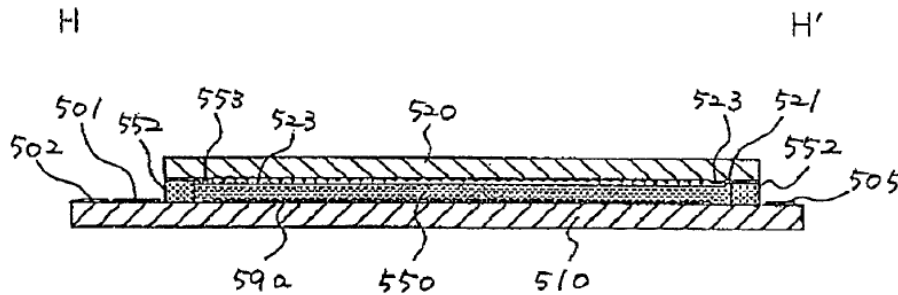
[FIG. 6]



228. *Takezawa* Figure 6 (above), which is a plan view, discloses base substrate 510 with an extending portion that extends from the counter substrate 520

on one side (bottom side). *Takezawa*, Fig. 6. *Takezawa* Figure 7 (below), which is a cross-sectional view, further teaches the same extending portion of the base substrate 510 that extends from the counter substrate 520.

[FIG. 7]



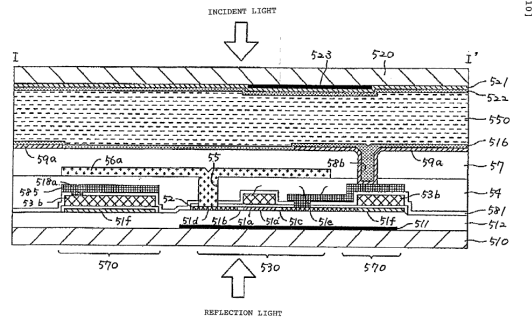
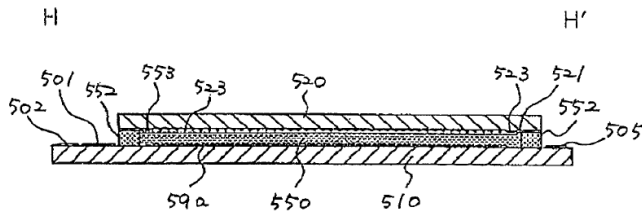
229. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**display electrodes that are provided on the one substrate;**

230. A POSITA would understand that *Takezawa* discloses display electrodes that are provided on the one substrate.

231. *Takezawa* teaches a plurality of pixel electrodes 59a in a matrix arrangement in the image display area of the liquid crystal panel. *Takezawa*, ¶[0076]. *Takezawa* Figures 7 and 10 (below) disclose the pixel electrodes 59a being provided on the base substrate 510.

[FIG. 7]



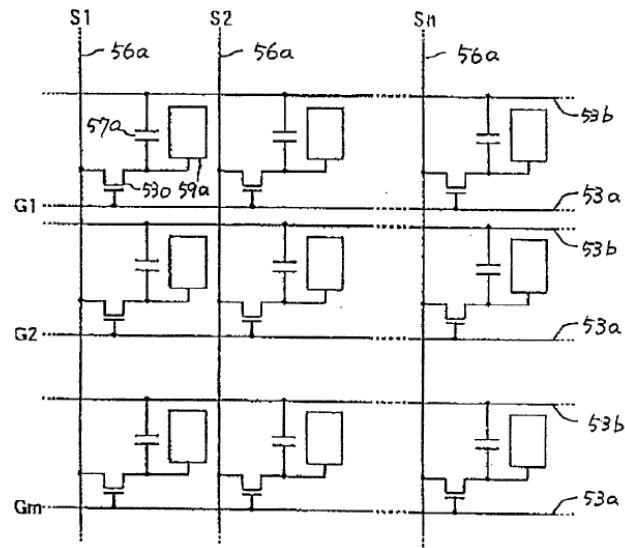
232. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**a circuit unit that is provided on the one substrate so as to drive the display electrodes;**

233. A POSITA would understand that *Takezawa* discloses a circuit unit that is provided on the one substrate so as to drive the display electrodes.

234. *Takezawa* teaches a data line drive circuit 501 that is provided along one side of the base substrate 510. *Takezawa* further teaches that the data line drive circuit 501 drives data lines 56a by supplying image signals to the data lines 56a. *Takezawa*, ¶[0074]; Fig. 6. In particular, *Takezawa* Figure 8 (below) shows that the data lines 56a are coupled to the pixel electrodes 59a via corresponding TFTs 530. Thus, the image signals provided by the data line drive circuit 501 are further provided to drive the pixel electrodes 59a via the data lines 56a and the TFTs 530. *Takezawa*, Fig. 8.

[FIG. 8]



235. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

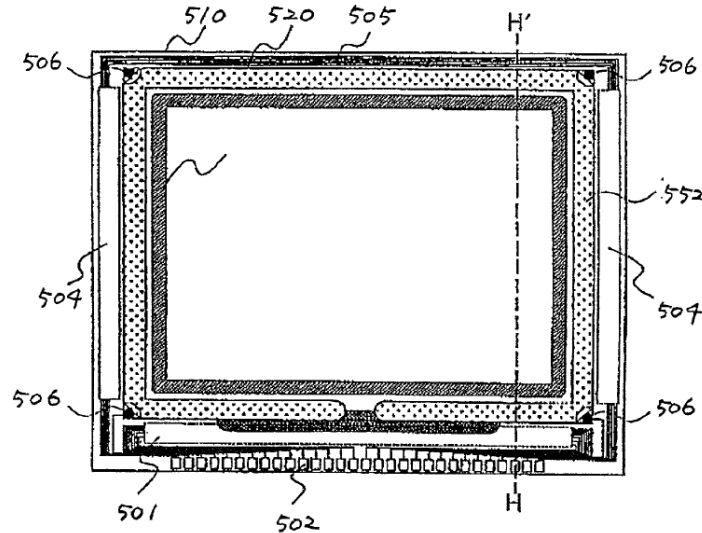
**wiring lines for driving the circuit unit and the display electrodes;**

236. A POSITA would understand that *Takezawa* discloses wiring lines for driving the circuit unit and the display electrodes.

237. *Takezawa* discloses a plurality of data lines 56a for transmitting image signals to the pixel electrodes 59a so as to drive the pixel electrodes 59a.

*Takezawa*, ¶[0074]; Figs. 6, 8. *Takezawa* Figure 6 (below) shows a plurality of wiring lines coupled to the data line drive circuit 501.

[FIG. 6]



238. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and**

239. A POSITA would understand that *Takezawa* teaches a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion.

240. *Takezawa* Figure 6 (above) shows segments of the wiring lines are led from one of the sides of the wirings to the extending portion and extend on the extending portion.

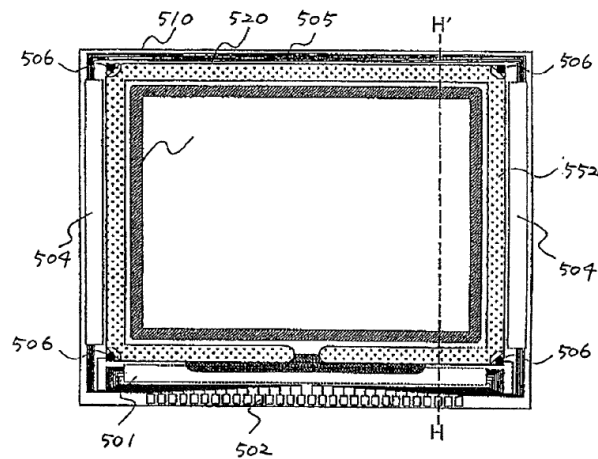
241. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**a plurality of external connecting terminals provided on the extending portion,**

242. A POSITA would understand that *Takezawa* teaches a plurality of external connecting terminals provided on the extending portion.

243. *Takezawa* teaches that “external circuit connection terminal[s] 502 are provided along one side of the base substrate 510.” *Takezawa*, ¶[0074]. *Takezawa* Figure 6 shows the plurality of external circuit connection terminals are provided on the extending portion.

[FIG. 6]



244. Accordingly, it is my opinion that *Takezawa* teaches this limitation of claim 1.

**each of the external connecting terminals overlapping with the plurality of lead wiring lines in plan view.**

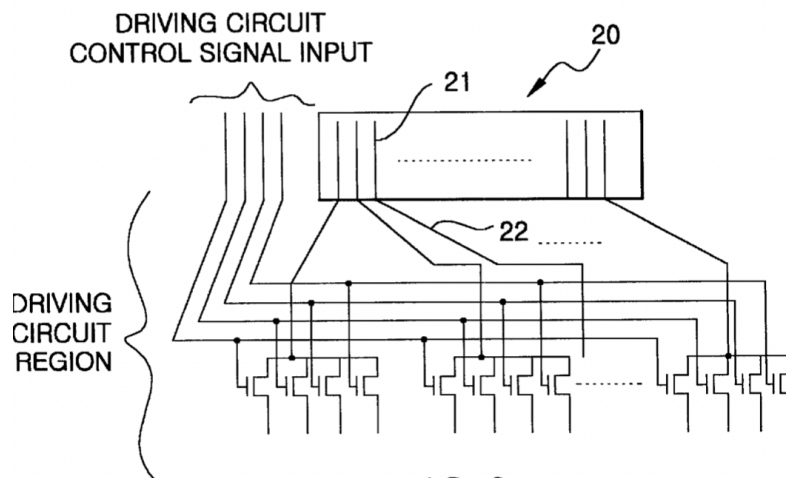
245. A POSITA would understand that *Kim* discloses external connecting terminals that overlap with the plurality of lead wiring lines in plan view.

246. *Kim* discloses a liquid crystal display device. *Kim*, Title. *Kim* teaches

that the liquid crystal display device “ha[s] a driving circuit” and “an outer circuit and the driving circuit are connected to each other by a pad.” *Kim*, col. 1:27-29.

The pads of *Kim* are external connecting terminals.

247. *Kim* teaches a conventional LCD (Figure 2 below) where a “plurality of pads 21 are formed in a connecting part of the outer circuit 20. Each pad 21 is connected to each chip of the driving circuit which is a data outer (output) circuit source (not shown in the drawing) and receives a data driving signal. Each data driving signal diverges at the driver and then carries the data signal to the pixel array.” *Kim*, col. 1:38-48.



248. *Kim* then teaches an LCD with a plurality of pads 41 and wires 42 connected to each of a plurality of the pads 41 in a connecting part of the outer circuit 40. *Kim*, col. 3:64-67. *Kim* further teaches pads located at the side portions of the connecting part are arranged in a row-like fashion and connected to the

driving circuit by the first wire 42. *Kim*, col. 4:14-18. “[T]he first wire 42 extends in a direction perpendicular to the pad 41.” *Kim*, col. 4:67-5:1. The segments of the wires 42 connected to the pads 41 constitute lead wiring lines. *Kim* Figures 4 and 5 (below), which are plan views, teach that pads 41 overlap with the segments of the plurality of wires 42.

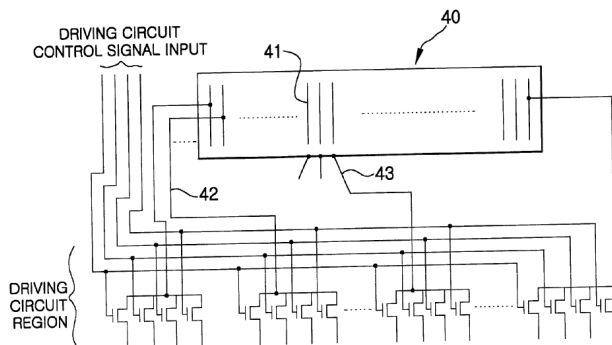


FIG.4

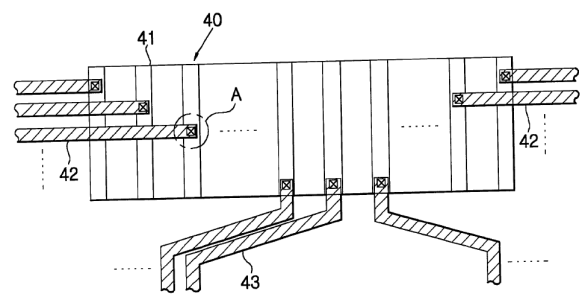


FIG.5

249. A POSITA would have found it obvious to combine *Takezawa* and *Kim*. *Kim* teaches that with its arrangement the wires are not necessarily formed as a long-line type and the space occupied by the wires is reduced as compared to conventional art, and enough space is provided to prevent an electrical short. *Kim*, col. 4:23-26. Therefore, a POSITA would have been motivated to modify the arrangement of the external circuit connection terminals 502 and the lead wiring lines of *Takezawa* according to the disclosure of *Kim*, resulting in overlapping between the external circuit connection terminals 502 and the lead wiring lines in plan view. Further, as both *Takezawa* and *Kim* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Kim*'s structure

as part of *Takezawa*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining the structure of *Kim* with *Takezawa*'s display device would have yielded predictable results.

250. Accordingly, it is my opinion that *Takezawa* in combination with *Kim* teaches and renders obvious this limitation of claim 1.

## **2. Claim 2**

**The electro-optical device according to claim 1,**

**wherein the external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween,**

251. A POSITA would understand that *Kim* discloses external connecting terminals and the lead wiring lines are laminated with an interlayer insulating film interposed therebetween.

252. *Kim* teaches that on the first wire 42 a first insulating layer 44 is formed, and on the insulating layer 44, a pad 41 of the outer circuit connecting part is contacted with and connected to the first wire 42. *Kim*, col. 4:61-65; Fig. 8. *Kim* Figure 8 shows the pad 41 and the first wire 42 are laminated, and the first insulating layer is interposed between the pad 41 and the first wire 42. Figs. 8, 9B (below).

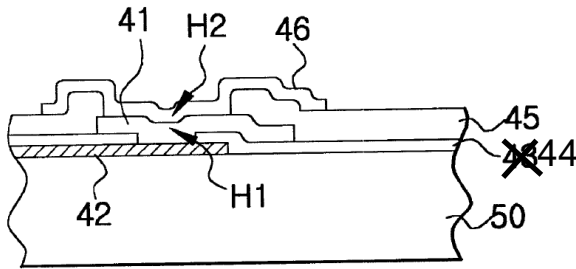


FIG. 8

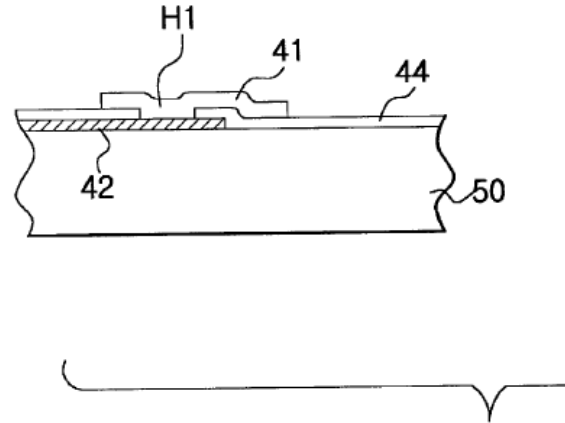


FIG. 9B

253. *Kim* further teaches another embodiment in which a first wire 105 is formed above a pad 101, with a first insulating layer 102 interposed therebetween. *Kim*, col. 6:9-14; Fig. 11A.

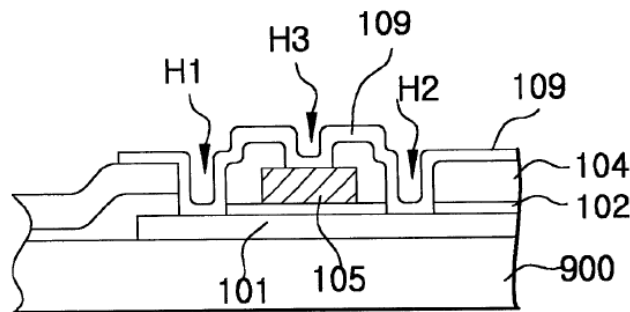


FIG. 11A

254. A POSITA would have found it obvious to combine *Takezawa* and *Kim* for the reasons set forth in regard to the claim limitation below (§260).

255. Accordingly, it is my opinion that the combination of *Takezawa* with *Kim* renders obvious this limitation of claim 2.

**each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.**

256. A POSITA would understand that *Kim* discloses each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.

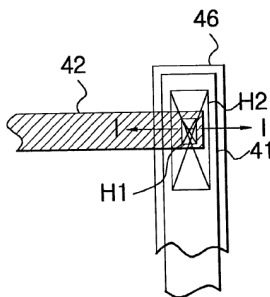


FIG. 7

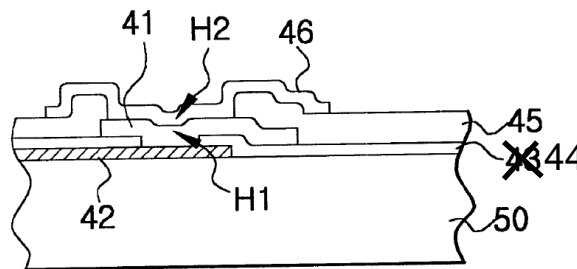


FIG. 8

257. *Kim* Figures 7 and 8 (above) teach that on the first insulating layer 44, a pad 41 of the outer circuit connecting part (an external connecting terminal) is contacted with and connected to the first wire 42 (lead wiring line) via the contact hole H1. Further, *Kim* discloses that on a first wire 42, a first insulating layer 44 is formed with contact hole H1 which exposes a portion of the first wire 42. *Kim*, col. 4:59-65.

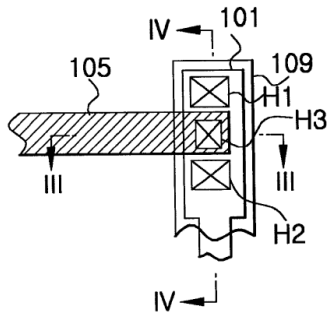


FIG. 10

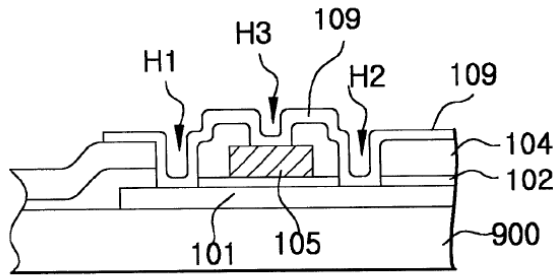


FIG. 11A

258. This limitation is also disclosed in another embodiment of *Kim*. *Kim* Figures 10 and 11A (above) disclose a pad 101 (the external connecting terminal) with a first insulating layer 102 that has contact holes H1 and H2. Further, there is a first wire 105 formed on the first insulating layer 102. There is a second insulating layer 104 that covers the whole surface of the substrate but exposes portions of the pad 101 through a first contact hole H1 and a second contact hole H2 and a portion of the first wire 105 through a third contact hole H3. On the second insulating layer 104, an ITO layer 109 connected to the pad 101 via the first and second contact holes H1 and H2 and connected to the first wire 105 via the third contact hole H3 is formed. *Kim*, col. 6:9-23. Thus, the pad 101 (external connecting terminal) is electrically connected to the corresponding first wire 105 (lead wiring line) via the first and second contact holes H1 and H2, the ITO layer 109, and the third contact hole H3.

259. *Kim* Figures 5, 7, and 8 teach that pads 41 are electrically connected

with a corresponding one of the first wires 42 via a corresponding contact hole H1, with no contact holes between a pad 41 and others of the first wires 42. *Kim*, Figs. 5, 7, 8. As such, *Kim* teaches that the first insulating layer 44 electrically isolates each pad 41 (external connecting terminal) from others of the first wires 42 (lead wiring lines).

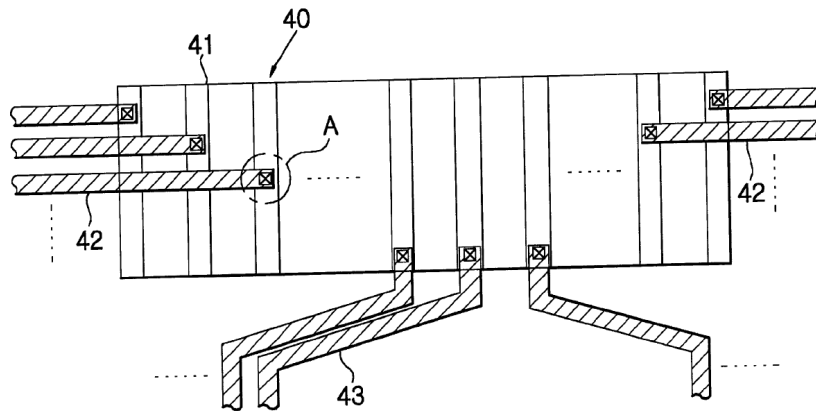


FIG.5

260. A POSITA would have found it obvious to implement *Kim*'s insulating layer in *Takezawa*'s display device. A POSITA would have been motivated to combine *Kim*'s insulating layer into *Takezawa*'s display device once *Kim*'s overlapping structure is adopted in *Takezawa*'s display device, in order to separate overlapping conductive layers that need to be electrically isolated from each other. A POSITA would have also been motivated to apply *Kim*'s contact holes in the insulating layer to provide electrical connection between two conductive layers that need to be electrically connected. Further, as both

*Takezawa* and *Kim* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Kim*'s insulating layer in *Takezawa*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining *Kim*'s insulating layer with *Takezawa*'s display device would have yielded predictable results.

261. Accordingly, it is my opinion that the combination of *Takezawa* with *Kim* renders obvious this limitation of claim 2.

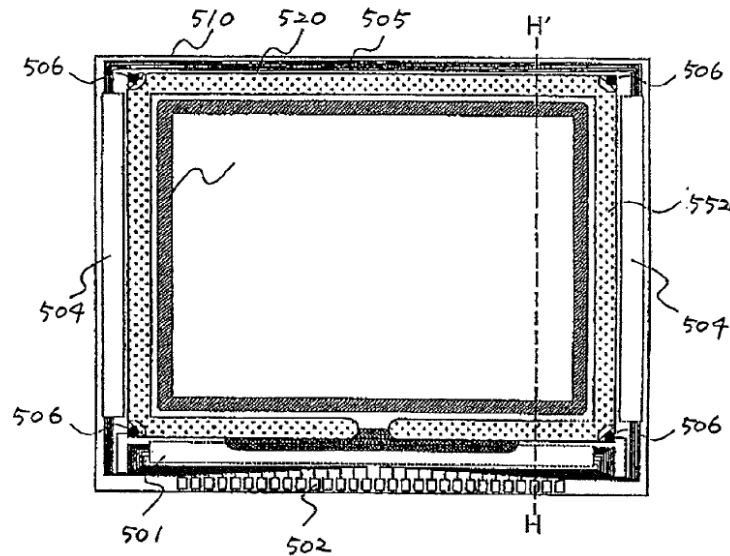
### **3. Claim 3**

**The electro-optical device according to claim 1,**

**wherein the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and**

262. A POSITA would understand that *Takezawa* discloses the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side.

[FIG. 6]



263. *Takezawa* Figure 6 (above) teaches a plurality of external circuit connection terminals 502 are arranged in a left-right direction, *i.e.*, a direction along the bottom side (the one side).

264. *Takezawa* Figure 6 further discloses that the plurality of lead wiring lines (segments of the wirings lines in the extending portion) also extend in the left-right direction, *i.e.*, a direction along the bottom side (the one side).

265. Accordingly, it is my opinion that *Takezawa* discloses this limitation of claim 3.

**are correspondingly connected to edges of the external connecting terminals in a direction intersecting the direction along the one side.**

266. A POSITA would understand that *Takezawa* teaches a plurality of lead wiring lines that are correspondingly connected to edges of the external

connecting terminals in a direction intersecting the direction along the one side.

267. *Takezawa* Figure 6 discloses the lead wiring lines are connected to edges of corresponding external circuit connection terminals 502 in a direction intersecting the left-right direction, *i.e.*, a direction along the bottom side (the one side).

268. Accordingly, it is my opinion that *Takezawa* discloses this limitation of claim 3.

#### 4. Claim 4

**The electro-optical device according to claim 1, wherein the plurality of external connecting terminals are arranged in a direction along the one side, and the plurality of lead wiring lines extend in the direction along the one side and**

269. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 3.

**are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.**

270. A POSITA would understand that *Kim* teaches a plurality of lead wiring lines that are correspondingly connected to the external connecting terminals in a region where the lead wiring lines and the external connecting terminals intersect each other in plan view.

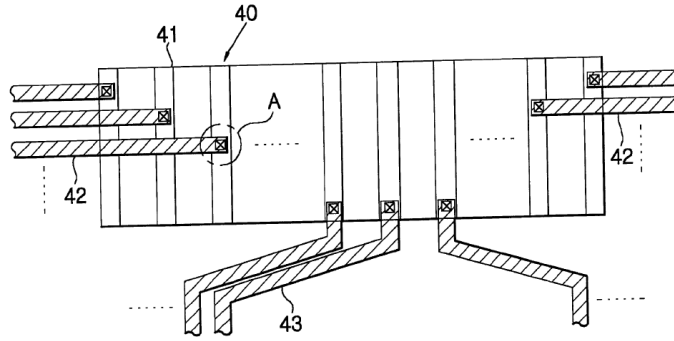


FIG. 5

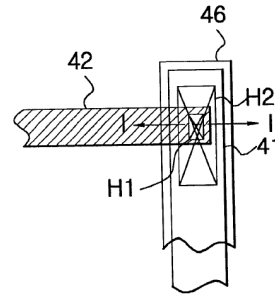


FIG. 7

271. *Kim* Figures 5 and 7 teach a plurality of first wires 42 (lead wiring lines) are correspondingly connected to the pads 41 (external connecting terminals) via contact holes H1 in a region where the first wires 42 and the pads 41 intersect each other in plan view.

272. For the reasons set forth above in regard to claim 1, a POSITA would have been motivated to combine *Takezawa* with *Kim*.

273. Accordingly, it is my opinion that the combination of *Takezawa* with *Kim* renders obvious this limitation of claim 4.

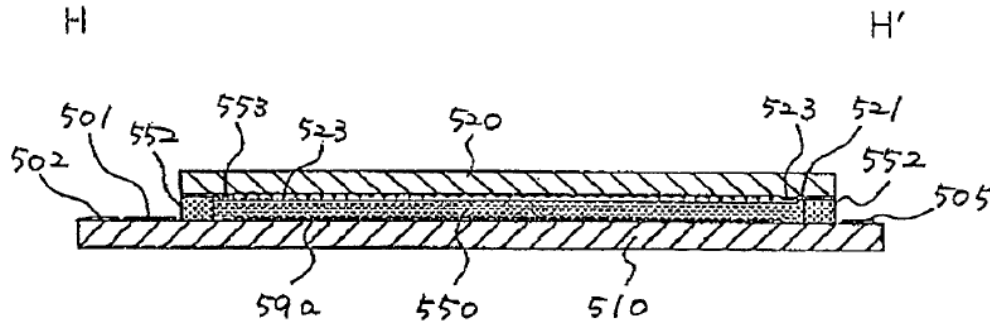
## 5. Claim 8

**The electro-optical device according to claim 1, further comprising:**

**a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates; and**

274. A POSITA would understand that *Takezawa* teaches a sealant that bonds edges of opposite surfaces of the pair of substrates to each other so as to form an internal space between the pair of substrates.

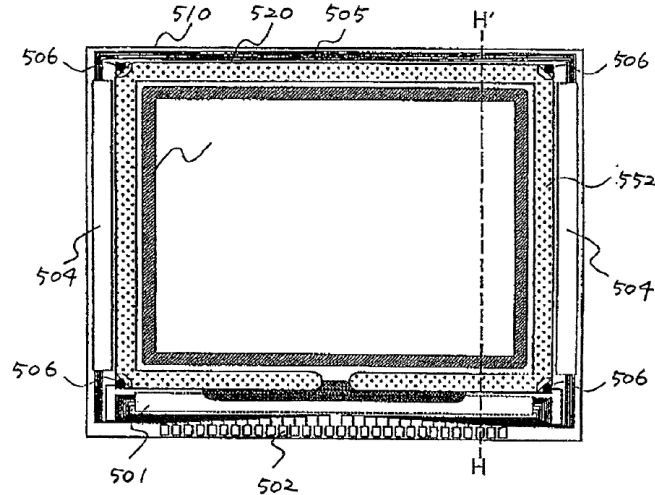
[FIG. 7]



275. *Takezawa* Figure 7 (above) shows a liquid crystal panel that includes a base substrate 510 and the counter substrate 520. *Takezawa* explains that base and counter substrates are bonded together by a sealant 552 to form a “space surrounded by the base substrate 510, the counter substrate 520, and the sealant 552. *Takezawa*, ¶[0072]. As shown in Figure 7, the sealant 552 bonds edges of opposite surfaces of the base substrate 510 and the counter substrate 520, and the internal space is formed between the base substrate 510 and the counter substrate 520. *Takezawa* discloses that the sealant 552 is provided on the base substrate 510 along the edges thereof. *Takezawa*, ¶[0073].

276. *Takezawa* Figure 6 (below) shows that sealed edges surround the internal display region where the liquid crystals are located.

[FIG. 6]



277. Accordingly, it is my opinion that *Takezawa* discloses this limitation of claim 8.

**an electro-optical material that is held in the internal space,**

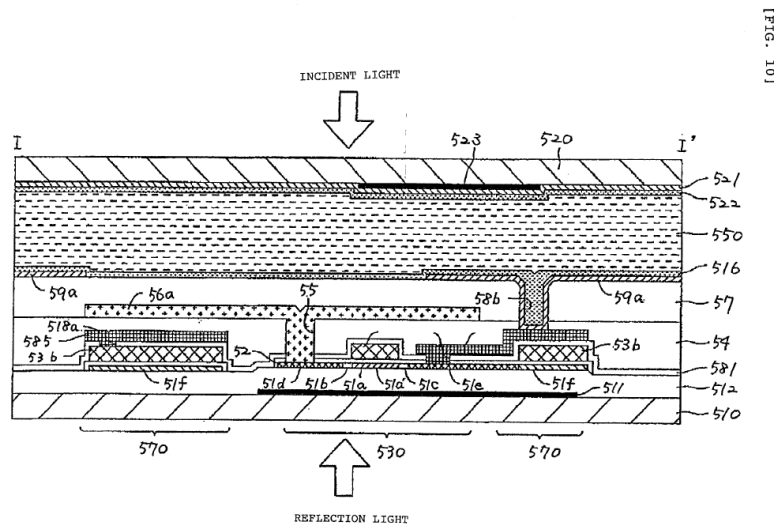
278. A POSITA would understand that *Takezawa* discloses that liquid crystals 550 are sealed in the space surrounded by the base substrate 510, the counter substrate 520, and the sealant 552. *Takezawa*, ¶[0072].

279. Accordingly, it is my opinion that *Takezawa* discloses this limitation of claim 8.

**wherein the display electrodes and a part of the circuit unit are disposed to face the internal space.**

280. A POSITA would understand that *Takezawa* Figure 10 (below) discloses pixel electrode 59a and various components of the circuit unit, such as TFT 530 and data line 56a, are disposed to face the internal space that holds the liquid crystals 550. According to the '913 patent, “electronic elements, such as

TFTs or the like, the wiring lines, such as . . . data lines, and the like. . . correspond to a specified example of ‘circuit unit’.” ’913 patent, col. 7:56-61.



281. Accordingly, it is my opinion that *Takezawa* discloses this limitation of claim 8.

## 6. Claim 9

**An electronic apparatus comprising the electro-optical device according to claim 1.**

282. A POSITA would understand that *Takezawa* discloses a projector. *Takezawa*, Title and Abstract. A projector is an electronic apparatus. ’913 patent, col. 1:12-14 (“an electronic apparatus, such as a liquid crystal projector”). The projector of *Takezawa* includes the liquid crystal panel.

283. Accordingly, it is my opinion that *Takezawa* discloses claim 9.

7. Claim 10

**The electro-optical device according to claim 2, the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit,**

284. A POSITA would understand that *Kim* teaches external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit.

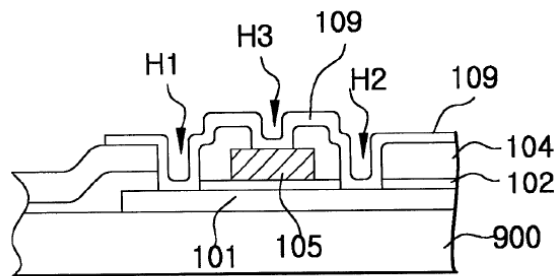


FIG. 11A

285. *Kim* teaches pad 101 is formed preferably by photolithography after a first conductive layer has been formed, where the first conductive layer is used in forming source and drain electrodes or the data line. *Kim*, col. 6:27-33; claim 5.

286. A POSITA would have found it obvious to combine *Takezawa* and *Kim*. Specifically, a POSITA would have found it obvious to implement *Kim*'s method of using two conductive layers to form the wirings and the connection terminals of *Takezawa* from the same films as the two conductive films (first conductive film and second conductive film) constituting the circuit unit, respectively, with *Takezawa*'s display device. A POSITA would have been

motivated to combine *Kim*'s method with *Takezawa*'s display device in order to reduce the number of layers and processing steps and hence simplify manufacturing and reduce cost. Further, as both *Takezawa* and *Kim* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Kim*'s method to create the structure of *Takezawa*'s display device. Finally, as both references relate to LCDs and describe similar structures, combining the method of *Kim* with *Takezawa*'s display device would have yielded predictable results.

287. Accordingly, it is my opinion that the combination of *Takezawa* with *Kim* renders obvious this limitation of claim 10.

**and the lead wiring lines being formed from the same film as a second conductive film constituting the circuit unit.**

288. A POSITA would understand that *Kim* discloses a first wire 105 is formed preferably by photolithography after a second conductive layer has been formed, where the second conductive layer is used in forming the gate electrode or the gate line. *Kim*, col. 6:37-43; claim 6.

289. For the reasons set forth above in the claim limitation above, a POSITA would have been motivated to combine *Takezawa* with *Kim*.

290. Accordingly, it is my opinion that the combination of *Takezawa* with *Kim* renders obvious this limitation of claim 10.

**J.     *Takezawa* Renders Obvious in Combination with *Yoneda* Claims 5 and 6.**

**1.     Claim 5**

**An electro-optical device comprising:**

291. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**a pair of substrates that are disposed to face each other with a predetermined gap therebetween,**

292. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;**

293. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**display electrodes that are provided on the one substrate;**

294. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**a circuit unit that is provided on the one substrate so as to drive the display electrodes;**

295. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**wiring lines for driving the circuit unit and the display electrodes;**

296. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and**

297. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**a plurality of external connecting terminals provided on the extending portion,**

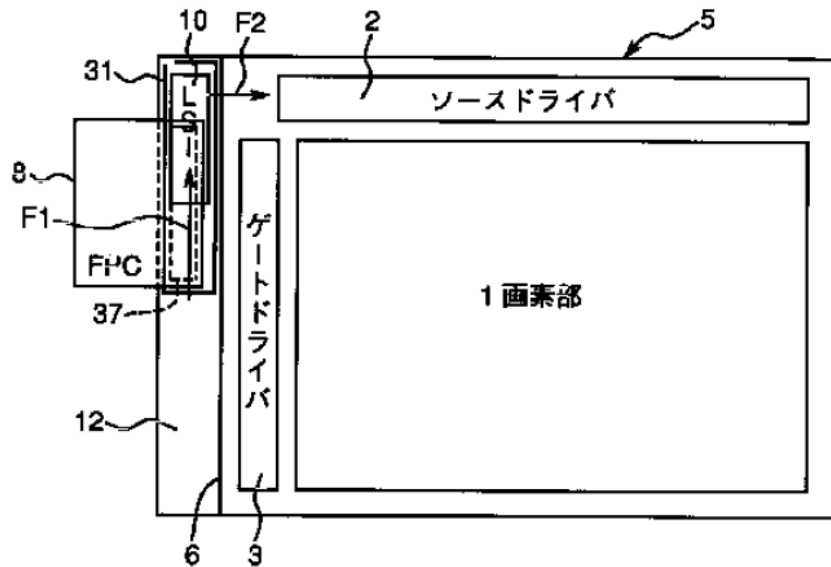
298. A POSITA would understand that *Takezawa* discloses this limitation as set forth in regard to claim 1.

**each of the external connecting terminals overlapping with the circuit unit in plan view.**

299. A POSITA would understand that *Yoneda* teaches each of the external connecting terminals overlapping with the circuit unit in plan view.

300. *Yoneda* discloses an image display device. *Yoneda*, Title and Abstract. *Yoneda* discloses “a polysilicon TFT liquid crystal display device, in which . . . a source driver 2 and a gate driver 3 are formed on a same TFT substrate 5,” where the TFT substrate 5 has an “adjacent region 12 . . . protruding outside the counter substrate (not shown).” *Yoneda*, ¶[0022]. Figure 3 of *Yoneda* is shown below. *Yoneda*’s adjacent region 12 constitutes the claimed extending portion.

【図3】



301. *Yoneda* further teaches external connection terminals 37 formed in the adjacent region 12 (extending portion). *Yoneda*, ¶[0032]; Fig. 3.

302. *Yoneda* discloses a video signal from the outside is transmitted through the flexible wiring board 8, the external connection terminal 7, the integrated circuit 10, and the source driver 2 in this order,” and “[t]he integrated circuit 10 has a circuit for converting a video signal input from the flexible wiring board 8 via the external connection terminal 7 into a signal to be supplied to the source driver (data driver) 2.” *Yoneda*, ¶[0024].

303. A POSITA would have found it obvious to combine *Takezawa* and *Yoneda*. As shown in FIG. 3 of *Yoneda*, the external connecting terminals 37 overlap with the integrated circuit 10 in a plan view. According to *Yoneda*, with

this arrangement, “the flexible wiring board 8, the integrated circuit 10 . . . are arranged in approximately half the area of the adjacent area 12, so that the video signal transmission path can be shortened.” *Yoneda*, ¶[0032].

304. Therefore, a POSITA would have been motivated to modify the arrangement of the external circuit connection terminals 502 and the circuit unit (e.g., data line drive circuit 501) of *Takezawa* according to the disclosure of *Yoneda*, resulting in overlapping between the external circuit connection terminals 502 and the circuit unit in plan view. Specifically, a POSITA would have found it obvious to implement *Yoneda*’s arrangement of the external connecting terminals and circuit unit with *Takezawa*’s display device. A POSITA would have been motivated to combine *Yoneda*’s structure with *Takezawa*’s display device in order to minimize the size of the extending portion of the array substrate. Further, as both *Takezawa* and *Yoneda* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Yoneda*’s arrangement of the external connecting terminals and circuit with *Takezawa*’s display device. Finally, as both references relate to LCDs and describe similar structures, combining the specific structures of *Yoneda* with *Takezawa*’s display device would have yielded predictable results.

305. Accordingly, it is my opinion that the combination of *Takezawa* with *Yoneda* renders obvious this limitation of claim 5.

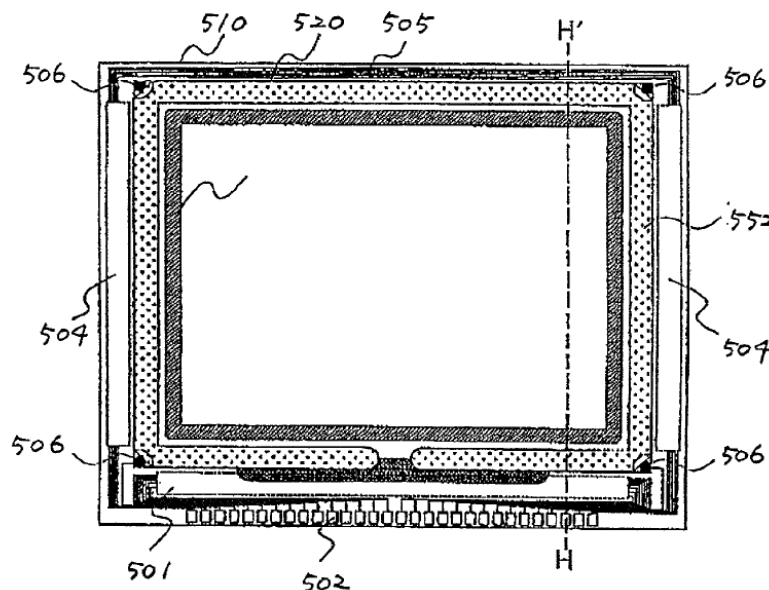
## 2. Claim 6

**The electro-optical device according to claim 5,**

wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and

306. A POSITA would understand that *Takezawa* discloses a circuit unit with data line drive circuit 501. *Takezawa* Figure 6 (below) teaches that among the plurality of external circuit connection terminals 502, some terminals are for the data line drive circuit 501. *Takezawa*, ¶[0074]. In particular, *Takezawa* discloses that: “[The] data line drive circuit 501 . . . drives data lines 56a by supplying image signals to the data lines 56a.” *Takezawa*, ¶[0074].

[FIG. 6]



307. Alternatively, *Yoneda* also discloses that a video signal from the outside is transmitted through flexible wiring board 8, the external connection

terminal 7, the integrated circuit 10, and the source driver 2 in this order. *Yoneda* further discloses that “[t]he integrated circuit 10 has a circuit for converting a video signal input from the flexible wiring board 8 via the external connection terminal 7 into a signal to be supplied to the source driver (data driver) 2.” *Yoneda*, ¶[0024]. Thus, *Yoneda*’s integrated circuit 10 is a driving circuit.

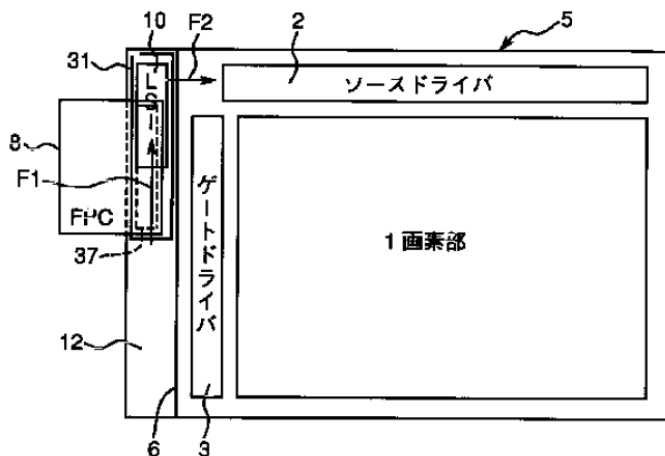
308. Accordingly, it is my opinion that *Takezawa* discloses this limitation of claim 6.

309. Alternatively, it is my opinion that the combination of *Takezawa* with *Yoneda* renders obvious this limitation of claim 6. A POSITA would have been motivated to combine *Takezawa* with *Yoneda* for the reasons set forth in regard to claim 5.

**at least a part of the driving circuit overlaps the external  
connecting terminals in plan view.**

310. A POSITA would understand that *Yoneda* Figure 3 shows that at least a part of the integrated circuit 10 (driving circuit) overlaps the external connection terminals 37 in plan view.

【図3】



311. A POSITA would have been motivated to modify the arrangement of the external circuit connection terminals 502 and the data line drive circuit 501 of *Takezawa* according to the disclosure of *Yoneda*, resulting in overlapping between the external circuit connection terminals 502 and at least a part of the data line drive circuit 501 in plan view. In addition, a POSITA would have been motivated to combine *Takezawa* with *Yoneda* for the reasons set forth in regard to claim 5.

312. Accordingly, it is my opinion that the combination of *Takezawa* with *Yoneda* renders obvious this limitation of claim 6

**K. Takezawa in Combination with Yoneda and Aruga Renders  
Obvious Claim 7.**

**1. Claim 7**

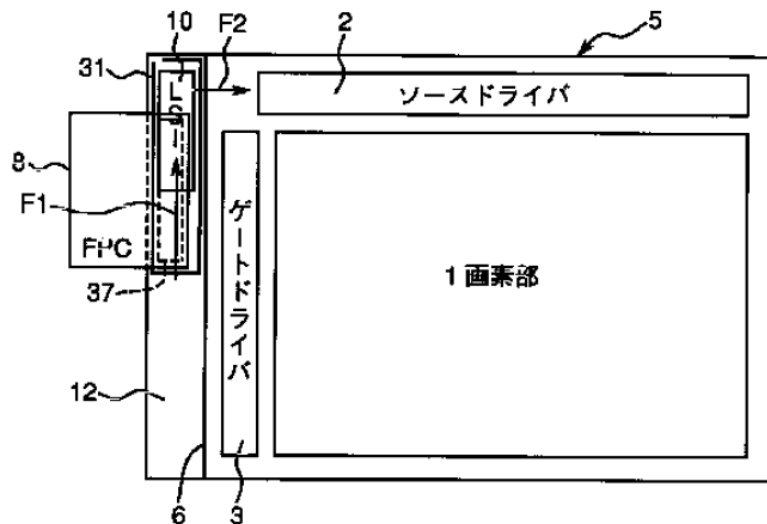
**The electro-optical device according to claim 5,**

**wherein the external connecting terminals and the part of the  
circuit unit are laminated with an interlayer insulating film  
interposed therebetween,**

313. A POSITA would understand that *Yoneda* teaches the external connecting terminals and the part of the circuit unit are laminated with an interlayer insulating film interposed therebetween.

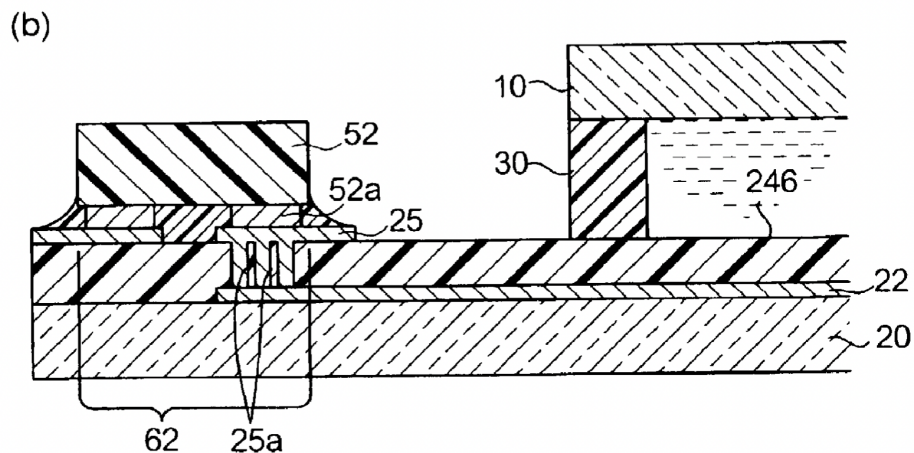
314. As shown in Figure 3 of *Yoneda*, the external connection terminals 37 and the integrated circuit 10 are laminated.

【図3】



315. Further, a POSITA would understand that *Aruga* discloses: “A resin or mold seals the connecting portion between the X driver IC 52 and the chip

connecting wiring 25” (para. [0044]), thus “moisture is inhibited from reaching the data lines 22 through the contact holes 25a and corrosion of the data lines 22 can be reliably prevented” (para. [0045]). Thus, *Aruga*’s underling conducting layer 22 and IC 52 are laminated with an interlayer insulating film (resin+layer 246) interposed therebetween. *Aruga*, Fig. 7(b) (below).



316. A POSITA would have found it obvious to combine *Takezawa* and *Yoneda* with *Aruga*. Specifically, a POSITA would have found it obvious to implement *Aruga*’s insulating layer in between *Yoneda*’s external connection terminals and circuit unit. A POSITA would have been motivated to combine *Aruga*’s insulating layer with *Takazawa*’s and *Yoneda*’s device in order to inhibit moisture and prevent corrosion of at least the terminals as taught by *Aruga*. Further, as *Takezawa*, *Yoneda* and *Aruga* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Aruga*’s insulating layer with *Takazawa*’s and *Yoneda*’s device. Finally, as all references relate to

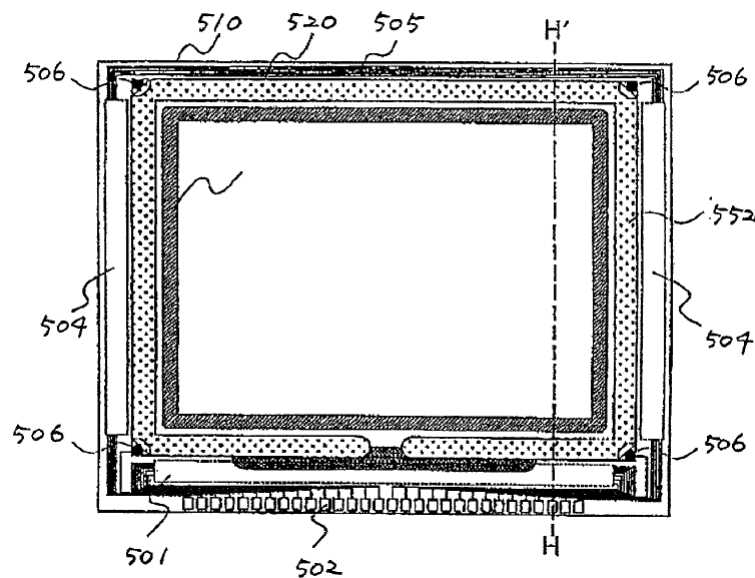
LCDs and describe similar structures, combining the specific structures of *Aruga* with *Takezawa*'s device would have yielded predictable results.

317. Accordingly, it is my opinion that *Takezawa* in combination *Yoneda* and in further combination *Aruga* teaches and renders obvious this limitation of claim 7.

**each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.**

318. A POSITA would understand that *Takezawa* discloses each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.

[FIG. 6]



319. *Takezawa* Figure 6 discloses that each external connecting terminal

(external circuit connection terminal 502) is electrically connected with a corresponding lead wiring line. For the reasons set forth above, a POSITA would have been motivated to combine *Takezawa* with the teachings of *Yoneda* or *Aruga* to laminate the external connection terminals and part of the circuit unit with an interlayer insulating film. As a result, each external connecting terminal would be electrically isolated from other lead wiring lines.

320. Accordingly, it is my opinion that *Takezawa* in combination with *Yoneda* teaches and renders obvious this limitation of claim 7. Alternatively, it is my opinion that *Takezawa* in combination with *Aruga* teaches and renders obvious this limitation of claim 7.

**L. *Takezawa* in Combination with *Tanaka* Renders Obvious Claim 11.**

**1. Claim 11**

**The electro-optical device according to claim 7, the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit.**

321. A POSITA would understand that *Tanaka* discloses a liquid crystal display with external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit.

322. *Tanaka* discloses that the liquid crystal display includes “external connection terminals 6 for inputting signals from an external drive circuit.”

*Tanaka*, ¶[0020]. *Tanaka* teaches that “[t]he external connection terminals 6 are

formed of the same electrode materials when the pixel portion 2, the scanning line driving circuit 3, and the signal line driving circuit 4 are formed.” *Tanaka*, ¶[0020].

323. *Tanaka* teaches that with its method the external connection terminals 6 are more resistive to corrosion and hence disconnection due to corrosion can be prevented so that a liquid crystal display device excellent in reliability and durability can be obtained. *Tanaka*, ¶¶[0031], [0038].

324. A POSITA would have been motivated to apply the terminal structure disclosed in *Tanaka* to the device of *Takezawa*, to form the external circuit connection terminals 502 from the same film as a conductive film constituting the circuit unit, so as to obtain a more reliable and durable liquid crystal display device. Further, as both *Takezawa* and *Tanaka* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine the terminal structure disclosed in *Tanaka* with *Takazawa*’s device. Finally, as both references relate to LCDs and describe similar structures, combining the terminal structure disclosed in *Tanaka* with *Takezawa*’s device would have yielded predictable results.

325. Accordingly, it is my opinion that *Takezawa* in combination with *Tanaka* renders obvious claim 11.

**M. *Hirosue* Anticipates Claims 5 and 6.**

**1. Claim 5**

**An electro-optical device comprising:**

326. A POSITA would understand that *Hirosue* discloses a display device, which is an electro-optical device. *Hirosue*, Title and Abstract.

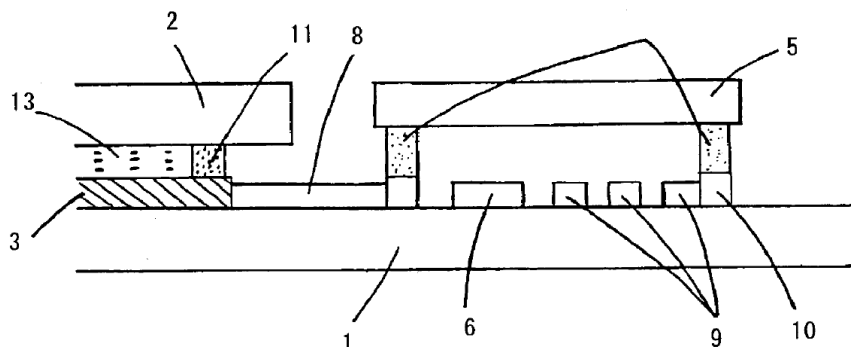
327. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**a pair of substrates that are disposed to face each other with a predetermined gap therebetween,**

328. A POSITA would understand that *Hirosue* discloses that the display device has a pair of substrates that are disposed to face each other with a gap in between.

329. *Hirosue* teaches that in Figures 1 and 2, element “1 denotes an insulating substrate . . . , 2 denotes an opposing substrate.” *Hirosue*, ¶[0035]. As shown in Figure 2 of *Hirosue* (below), the insulating substrate 1 and the opposing substrate 2 are disposed to face each other with a predetermined gap therebetween.

**FIG. 2**



330. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**one substrate of the pair of substrates including an extending portion that extends from the other substrate on one side in plan view;**

331. A POSITA would understand that *Hirosue* discloses that the insulating substrate includes an extending portion that extends from the opposing substrate on one side in plan view.

332. As shown in, Figure 1 of *Hirosue*, which is a plan view, the insulating substrate 1 has an extending portion that extends from the opposing substrate 2 on one side (bottom side). Figure 2 of *Hirosue*, which is a cross-sectional view taken along line A-A in Figure 1, also clearly shows the extending portion of the insulating substrate 1 that extends from the opposing substrate 2.

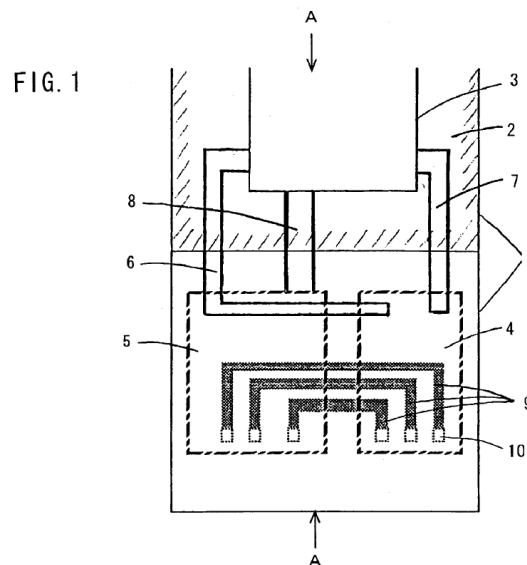
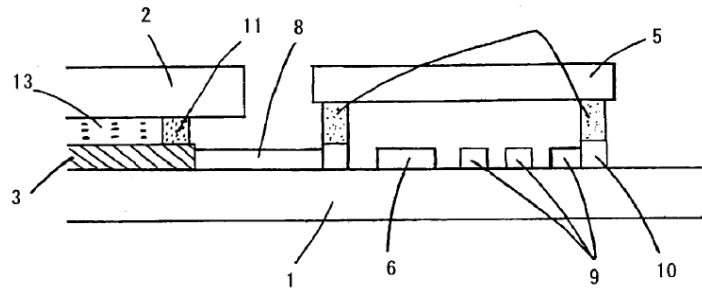


FIG. 2

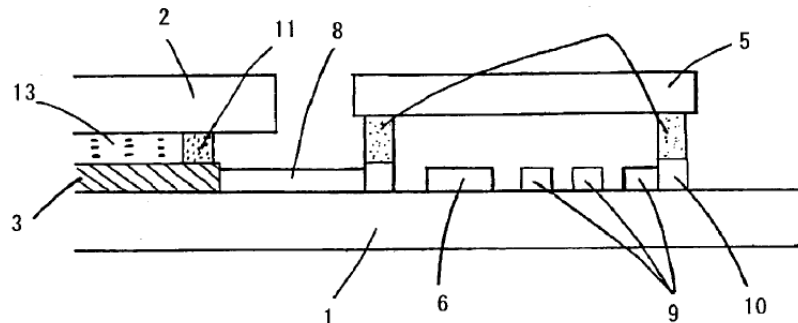


333. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**display electrodes that are provided on the one substrate;**

334. A POSITA would understand that *Hirosue* discloses that the display device includes display electrodes that are provided on the substrate.

FIG. 2



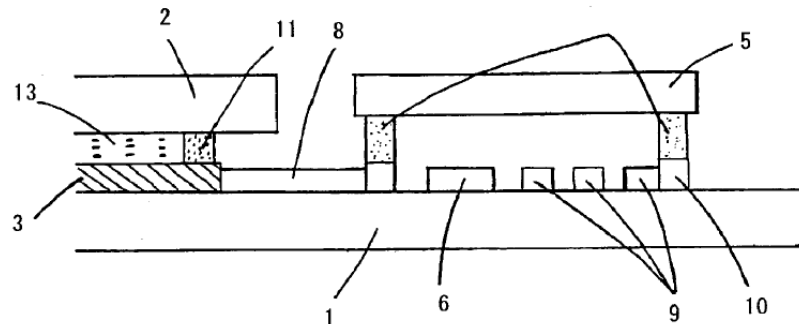
335. *Hirosue* teaches that in Figures 1 and 2, element “3 denotes a display region that comprises pixel electrodes.” *Hirosue*, ¶[0035]. According to the ’913 patent, “pixel electrodes . . . are examples of ‘display electrodes’.” ’913 patent, 7:20-21. As shown in Figure 2 of *Hirosue*, the display region 3 including the pixel electrodes is provided on the insulating substrate 1.

336. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**a circuit unit that is provided on the one substrate so as to drive the display electrodes;**

337. A POSITA would understand that *Hirosue* discloses that the display device includes a circuit unit provided on the insulating substrate to drive the pixel electrodes.

FIG. 2



338. *Hirosue* teaches that in Figures 1 and 2, element “4 denotes a scan line driver circuit, 5 denotes a signal line driver circuit.” *Hirosue*, ¶[0035]. According to the ’913 patent, “all of . . . circuits . . . including the scanning line driving circuits 104 and the data line driving circuit 101a correspond to a specified example of ‘circuit unit’.” ’913 patent, 7:58-61.

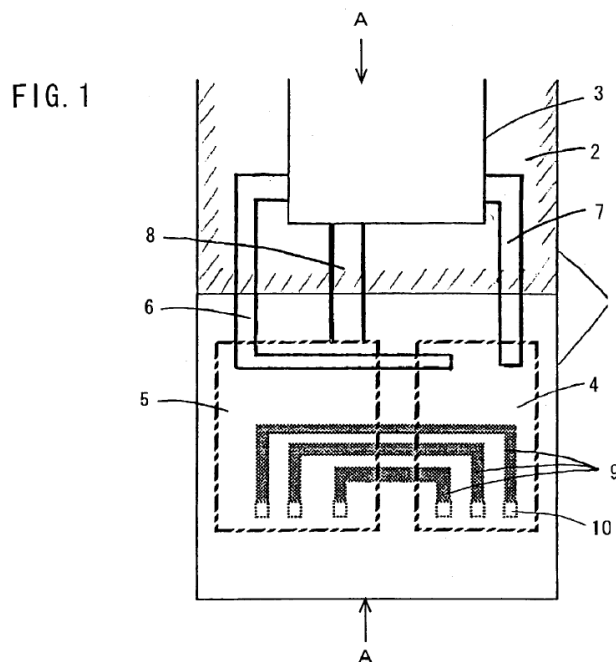
339. As shown in Figure 2 of *Hirosue*, the scan line driver circuit 4 and the signal line driver circuit 5 are provided on the insulating substrate 1.

340. Accordingly, it is my opinion that *Hirosue* discloses this limitation of

claim 5.

**wiring lines for driving the circuit unit and the display electrodes;**

341. A POSITA would understand that *Hirosue* discloses that the display device includes wirings for driving the circuit unit and the display electrodes.



342. *Hirosue* teaches that in Figures 1 and 2, element “6 denotes a group of lines that connects scan lines on one side of the display region and a scan line driver circuit, 7 denotes a group of lines that connects scan lines on a side that lies opposite to the one side of the display region and the scan line driver circuit, 8 denotes a group of lines that connects the signal lines of the display region and the signal line driver circuit; 9 denotes connecting lines that connects the scan line driver circuit and the signal line driver circuit.” *Hirosue*, ¶[0035]. Thus, *Hirosue*

**a plurality of lead wiring lines provided on the extending portion and that are led from one of the sides of the wiring lines to the extending portion; and**

FIG. 1

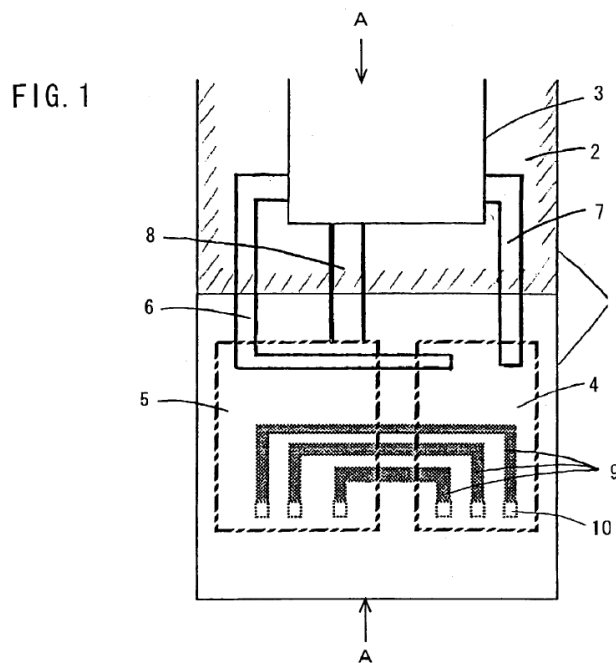
A schematic cross-sectional view of a semiconductor device. The device features a substrate 10 with a patterned conductive layer 9. Above this is a layer 5 containing a complex network of conductive traces 4. A central vertical structure 6 is surrounded by a layer 8. The top of the device is capped by a layer 2, with a central opening 3. A dashed line 7 indicates a boundary or interface. Arrows labeled 'A' indicate the direction of the view from the top and bottom.

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346. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**a plurality of external connecting terminals provided on the  
extending portion,**

347. A POSITA would understand that *Hirosue* discloses a plurality of external connecting terminals provided on the extending portion.



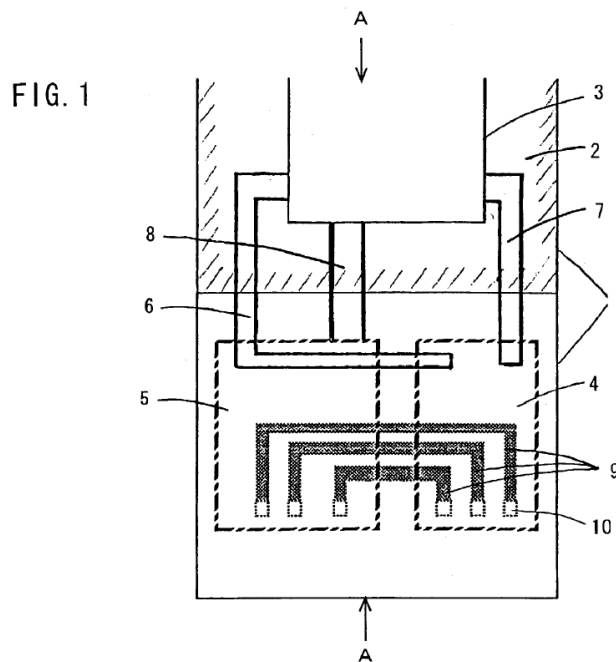
348. *Hirosue* teaches that in Figures 1 and 2, element “10 denotes driver-circuit connecting terminals which are formed on the insulating substrate.”

*Hirosue*, ¶[0035]. As shown in Figure 1 of *Hirosue*, the plurality of connecting terminals 10 are provided on the extending portion.

349. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**each of the external connecting terminals overlapping with the circuit unit in plan view.**

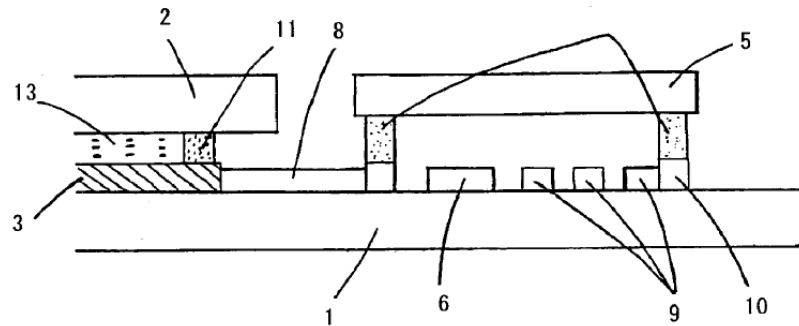
350. A POSITA would understand that *Hirosue* discloses that each of connecting terminals overlap with the circuit unit in plan view.



351. *Hirosue* Figure 1 “is a plan view of a liquid crystal display device.” *Hirosue*, ¶[0021]. As shown in Figure 1 of *Hirosue*, the connecting terminals 10 overlap with the scan line driver circuit 4 and the signal line driver circuit 5.

352. The overlapping relationship between the connecting terminals 10 and, for example, the signal line driver circuit 5 is also shown in Figure 2 of *Hirosue*.

FIG. 2



353. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

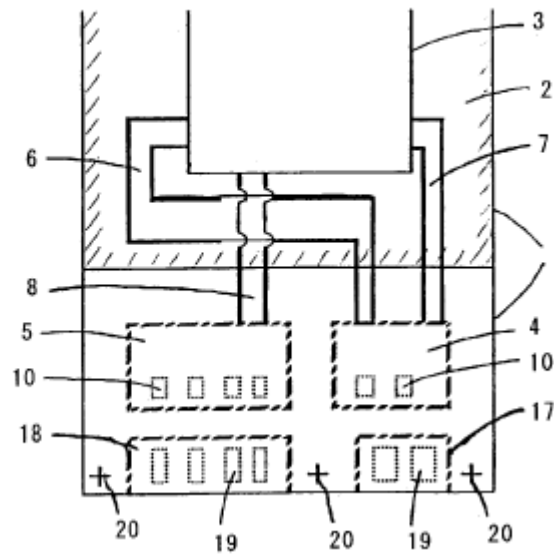
## 2. Claim 6

**The electro-optical device according to claim 5,**

**wherein the circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal, and**

354. A POSITA would understand that *Hirosue* discloses circuit unit is electrically connected to terminals for supplying an image signal among the plurality of external connecting terminals and has a driving circuit, which is driven by the supplied image signal.

FIG. 5

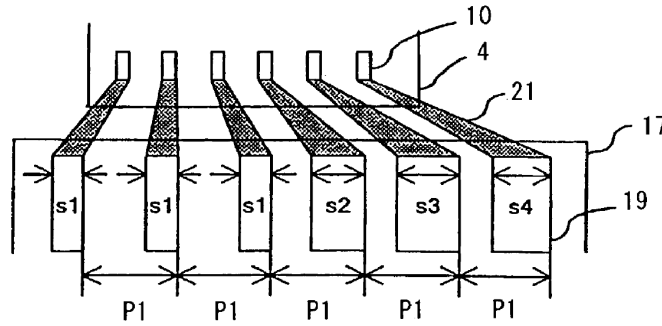


355. The circuit unit in *Hirosue* has the signal line driver circuit 5. As shown above in Figure 5 of *Hirosue*, among the plurality of driver-circuit connecting terminals 10, some terminals are for the signal line driver circuit 5. Corresponding connecting terminals 19 for FPC 18 are also provided on the insulating substrate 1, where FPC 18 “supplies a signal line potential from outside the liquid crystal panel.” *Hirosue*, ¶[0045].

356. *Hirosue* Figures 7-9 (Figure 7 reproduced below as an example), disclose the connection between the scan line driver circuit 4 and an FPC 17 that supplies a scan line potential via FPC connecting terminals 19, connecting lines 21, and driver-circuit connecting terminals 10. *Hirosue*, ¶[0049]. *Hirosue* further states that “the constitution of the present embodiment can be used for either one of: the connecting wiring between the scan line driver circuit and the scan line potential

supply FPC, and the connecting wiring between the signal line driver circuit and the signal line potential supply FPC.” *Hirosue*, ¶[0053].

FIG. 7



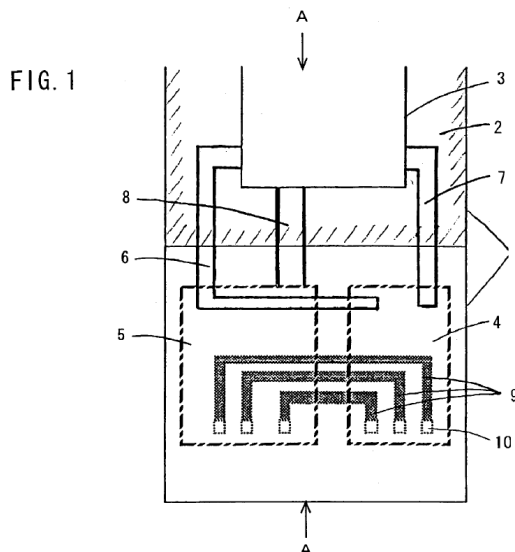
357. That is, in *Hirosue*, the circuit unit has the signal line driver circuit 5 electrically connected to some of the driver-circuit connecting terminals 10, which supply the signal line potential (image signal) received from the signal line potential supply FPC 18 and the signal line potential is for driving the signal line driver circuit 5.

358. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**at least a part of the driving circuit overlaps the external connecting terminals in plan view.**

359. A POSITA would understand that *Hirosue* discloses that at least a part of the driving circuit overlaps the external connecting terminals in plan view.

360. As shown in Figures 1 and 5 of *Hirosue*, a part of the signal line driver circuit 5 overlaps the driver-circuit connecting terminals 10 in plan view.



361. Accordingly, it is my opinion that *Hirosue* discloses this limitation of claim 5.

**N. *Hirosue* in Combination with *Aruga* Renders Obvious Claim 7.**

### 1. Claim 7

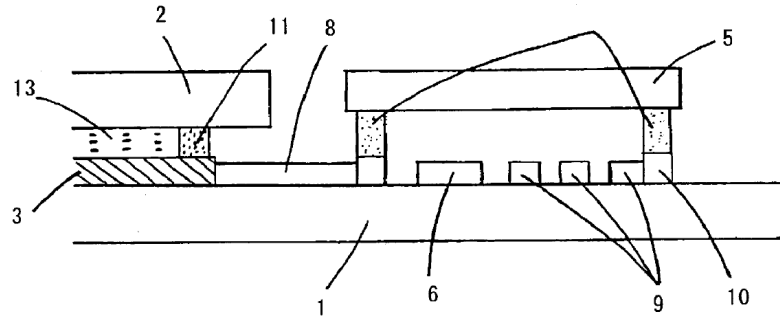
Claim 7 depends from Claim 5 with the further limitation:

**wherein the external connecting terminals and the part of the circuit unit are laminated with an interlayer insulating film interposed therebetween,**

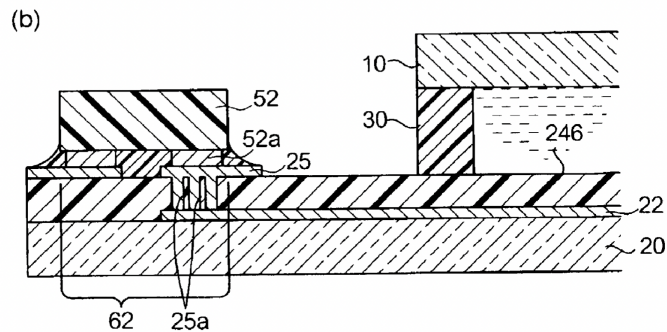
362. A POSITA would understand *Hirosue* to teach external connecting terminals and a part of the circuit unit that are laminated with an interlayer insulating film interposed between them.

363. As shown in Figure 2 of *Hirosue*, the signal line driver circuit 5 is arranged over the external driver-circuit connecting terminals 10.

FIG. 2



364. Further, a POSITA would understand that *Aruga* discloses: "A resin or mold seals the connecting portion between the X driver IC 52 and the chip connecting wiring 25" (para. [0044]), thus "moisture is inhibited from reaching the data lines 22 through the contact holes 25a and corrosion of the data lines 22 can be reliably prevented" (para. [0045]). Thus, *Aruga*'s underling conducting layer 22 and IC 52 are laminated with an interlayer insulating film (resin+layer 246) interposed therebetween. *Aruga*, Fig. 7(b) (below).



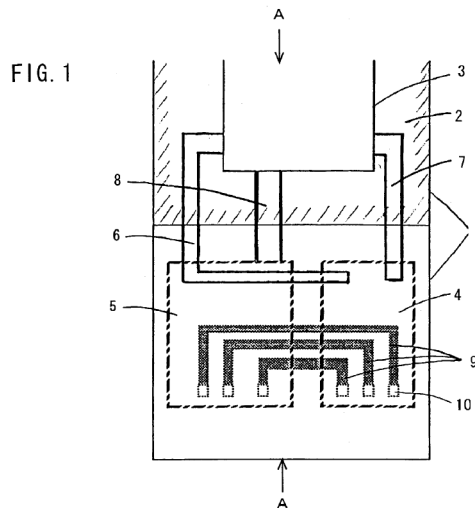
365. A POSITA would have found it obvious to combine *Hirosue* with with *Aruga*. Specifically, a POSITA would have found it obvious to implement *Aruga*'s insulating layer in between *Hirosue*'s external connection terminals and

circuit unit. A POSITA would have been motivated to combine *Aruga*'s insulating layer with *Hirosue*'s device in order to inhibit moisture and prevent corrosion of at least the terminals as taught by *Aruga*. Further, as both *Hirosue* and *Aruga* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine *Aruga*'s insulating layer with *Hirosue*'s device. Finally, as all references relate to LCDs and describe similar structures, combining the specific structures of *Aruga* with *Hirosue*'s device would have yielded predictable results. Therefore, it would be obvious to a POSITA to have the external driver-circuit connecting terminals 10 and the signal line driver circuit 5 of *Hirosue* laminated with each other with an interlayer insulating film interposed therebetween as suggested by *Aruga*.

366. Accordingly, it is my opinion that *Hirosue* in combination with *Aruga* teaches and renders obvious this limitation of claim 7.

**each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.**

367. A POSITA would understand *Hirosue* in combination with *Aruga* to teach each of the external connecting terminals being electrically connected with a corresponding one of the lead wiring lines and being electrically isolated from others of the plurality of lead wiring lines by the interlayer insulating film.



368. As shown in, Figure 1 of *Hirosue*, each external connecting terminal (connecting terminal 10) is electrically connected with a corresponding lead wiring line (segment of line 9 that extends in the up-down direction in Fig. 1). A POSITA would understand that *Hirosue* discloses that each external connecting terminal is electrically isolated from other lead wiring lines. *Hirosue*, Fig. 1. For the reasons set forth above, a POSITA would have been motivated to combine *Hirosue* with the teachings of *Aruga* to laminate the external connection terminals and part of the circuit unit with an interlayer insulating film. As a result, each external connecting terminal would be electrically isolated from other lead wiring lines.

369. Accordingly, it is my opinion that *Hirosue* in combination with *Aruga* teaches and renders obvious this limitation of claim 7.

**O. *Hirosue* in Combination with *Tanaka* Renders Obvious Claim 11.**

**1. Claim 11**

Claim 11 depends from claim 7 with the further limitation:

**the external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit.**

370. A POSITA would understand that *Tanaka* discloses a liquid crystal display with external connecting terminals being formed from the same film as a first conductive film constituting the circuit unit.

371. *Tanaka* discloses that the liquid crystal display includes “external connection terminals 6 for inputting signals from an external drive circuit.” *Tanaka*, ¶[0020]. *Tanaka* teaches that “[t]he external connection terminals 6 are formed of the same electrode materials when the pixel portion 2, the scanning line driving circuit 3, and the signal line driving circuit 4 are formed.” *Tanaka*, ¶[0020].

372. *Tanaka* teaches that with its method the external connection terminals 6 are more resistive to corrosion and hence disconnection due to corrosion can be prevented so that a liquid crystal display device excellent in reliability and durability can be obtained. *Tanaka*, ¶¶[0031], [0038].

373. A POSITA would have been motivated to apply the terminal structure disclosed in *Tanaka* to the device of *Hirosue*, to form the external circuit connection terminals from the same film as a conductive film constituting the circuit unit, so as to obtain a more reliable and durable liquid crystal display

device. Further, as both *Hirosue* and *Tanaka* relate to displays, and specifically LCDs, a POSITA would have found it straightforward to combine the terminal structure disclosed in *Tanaka* with *Hirosue*'s device. Finally, as both references relate to LCDs and describe similar structures, combining the terminal structure disclosed in *Tanaka* with *Hirosue*'s device would have yielded predictable results.

374. Accordingly, it is my opinion that *Hirosue* in combination with *Tanaka* renders obvious claim 11.

#### **VIII. Conclusion**

375. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

376. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 3 February 2023

By: Carl Sechen

Carl Sechen, Ph.D.