

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a Divisional of U.S. application Ser. No. 10/934,915, filed on September 3, 2004, which application is incorporated herein by reference.

FIELD OF INVENTION

[0002] This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND OF INVENTION

[0003] Bipolar Junction transistors (BJT) are minority carrier devices as the principle device conduction mechanism. However, majority carriers also a small yet finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. Carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an 'aiding drift field', to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical

and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the 'uniformly doped epi region' in a IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in the case of an n-channel IGBT) require different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

[0004] 'Retrograde' wells have been attempted, with little success, to help improve soft error immunity in SRAM's and visual quality in imaging circuits. FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3(b), 3(c), and 3(d) illustrate device cross sections, as practiced today.

'Retrograde' and 'halo' wells have also been attempted to improve refresh time in DRAM's (dynamic random access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera Ics. Most of these techniques

either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF DRAWINGS

[0005] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0006] FIGURE 1 illustrates the relative doping profiles of emitter, base, and collector, for the two most popular bipolar junction transistors: namely, A - uniform base, and B - graded base;

[0007] FIGURE 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

[0008] FIGURES 3(a), 3(b), 3(c), 3(d) illustrate cross sections commonly used CMOS silicon substrate with two wells (one n-well in which p-channel transistors are subsequently fabricated, and, one p-well in which n-channel transistors are subsequently fabricated) - typical IC, EEPROM using tunnel insulator, DRAM and NAND flash;

[0009] FIGURE 4 illustrates the cross section of a IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

[0010] FIGURES 5(a), 5(b), 5(c) illustrate the cross sections of a MOS silicon substrate with two wells, and, an underlying layer using embodiments of the invention to improve performance in each application - VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION OF THE INVENTION

[0011] The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, where as the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100X at the emitter-base junction, relative to the base-collector junction (1 X). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

[0012] As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region - n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The 'average' base resistance is optimized, so that conductivity modulation and lifetime (for minority carriers) in base region are not compromised. By sweeping the carriers towards the n^+ buffer region two advantages are obtained - the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. More importantly, during t_{off} , holes can be recombined much quicker at the n^+ buffer layer, compared to a uniformly doped n^- epitaxial drift region by

establishing a different dopant gradient near the n+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Epitaxy enhances lifetime, but, epitaxy is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer. This can improve t(on) and t(off) in the same device.

The following paragraph, beginning on page 5, line 6, and ending on page 11, line 28, is amended as indicated in the marked up version below:

[0013] As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI) - VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC'S. These unwanted carriers can discharge dynamically-held 'actively held high' nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM's is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC's is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC's with the embodiments described here. Creating 'Sub Terrain' recombination centers

underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterranean n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. In nonvolatile memory devices, to decrease programming time, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction field-effect transistors where the "channel pinchoff" is controlled by a graded channel instead of a uniformly doped channel (as practiced in prior art).

[0014] One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface, to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single well, as well triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments, individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below

[0015] Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

[0016] It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device with graded dopant concentration in the active region, to aid carrier movement from emitter to collector.
2. A semiconductor device with graded dopant concentration in the active region, to aid carrier movement from source to drain.
3. A semiconductor device with graded dopant concentration in the well regions, to aid carrier movement away from the active surface regions, towards the substrate.
4. A semiconductor device with graded dopant concentration in the substrate region to aid carrier movement away from the active surface regions, deeper towards the substrate.
5. A semiconductor device with at least one each of dopant concentration of both donor and acceptor, to optimize the operating performance of the device.
6. A semiconductor device with at least one graded dopant concentration fabricated with ion implantation, to provide an aiding or retarding electric field locally in a monolithic integrated circuit.
7. A semiconductor device with at least one graded dopant concentration in an epitaxial layer.
8. A semiconductor device where one layer of dopant from one wafer, is transferred to another wafer having either same polarity or different polarity dopant through wafer bonding or similar processes.

ABSTRACT

[0017] Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICS, improvement in refresh time for DRAM's, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFET's, and a host of other applications.

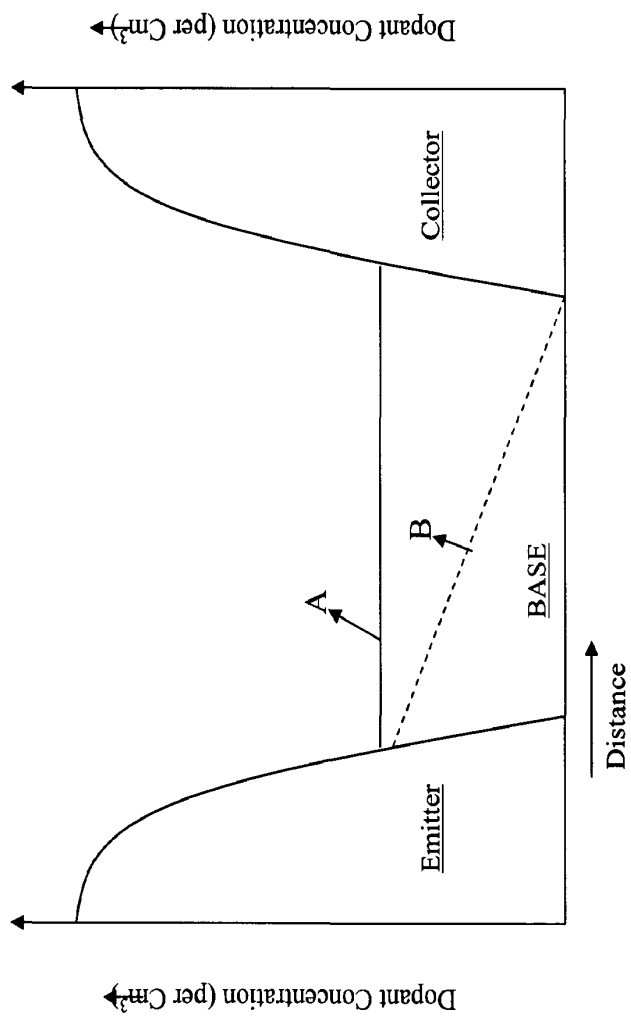


Figure 1 Prior Art

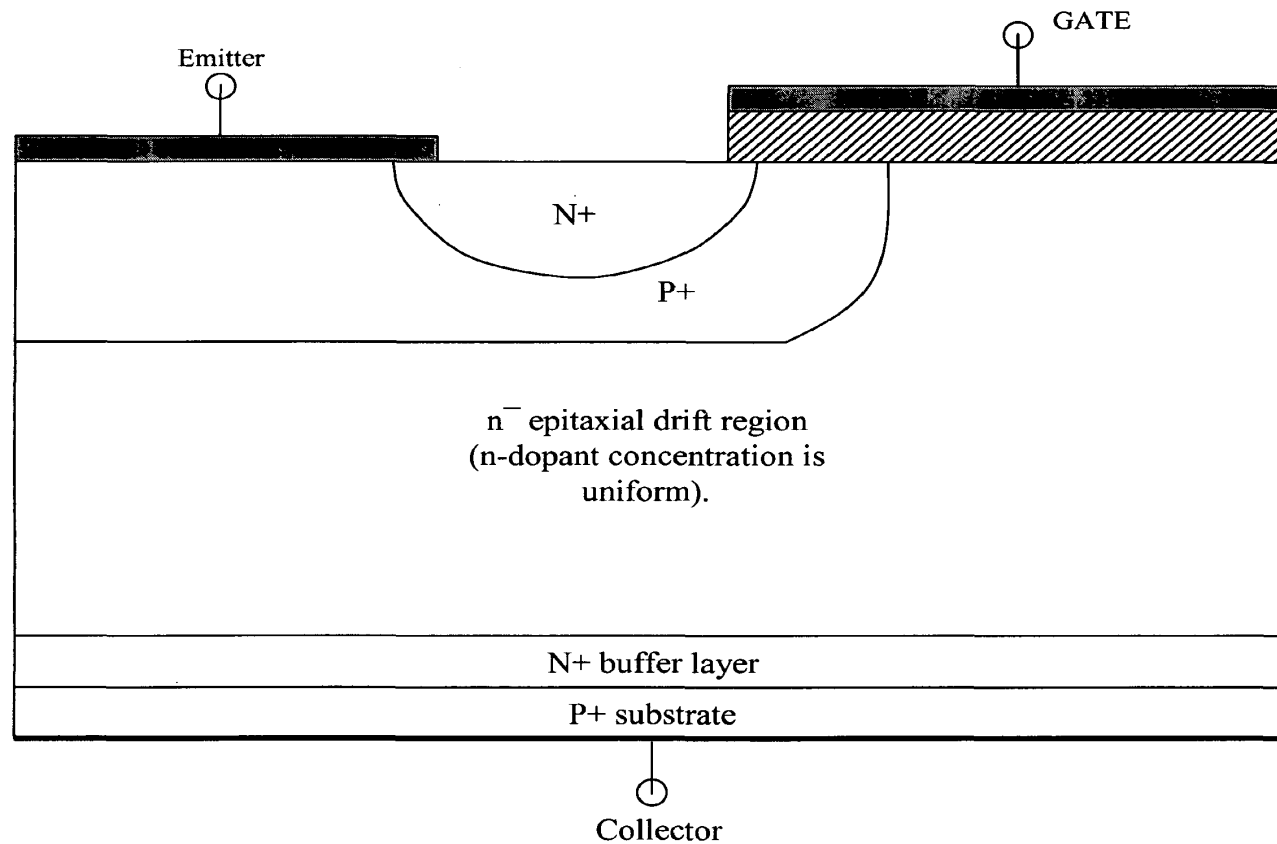


FIGURE 2 Prior art

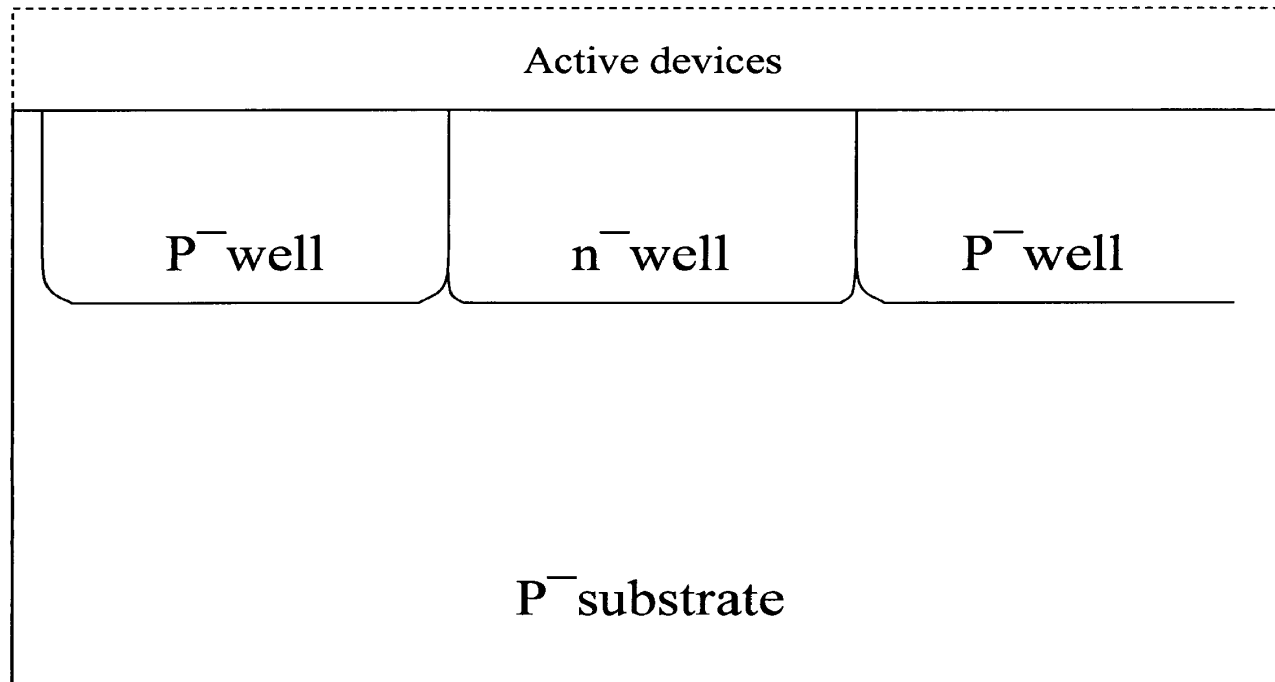


FIGURE 3(a) Prior art (Twin well CMOS) for a CMOS integrated circuit

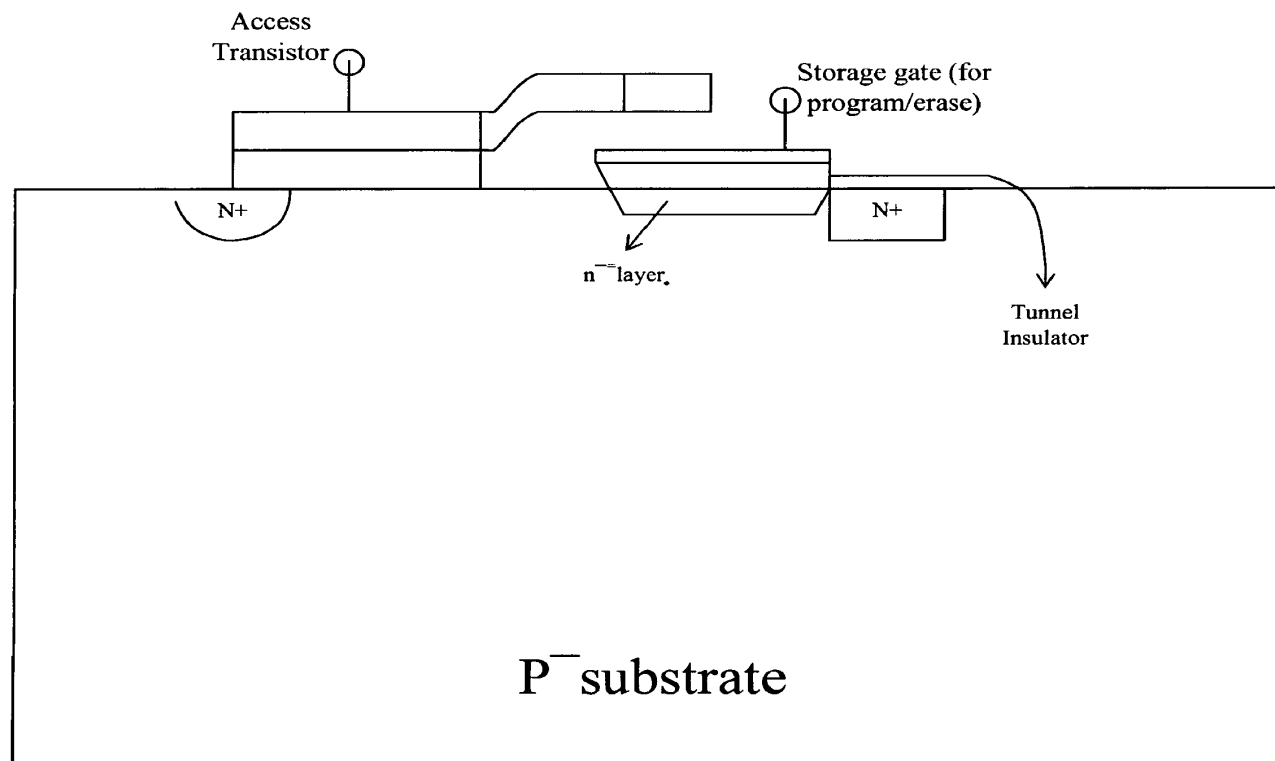


FIGURE 3(b) Prior art for a two-device EEPROM memory cell

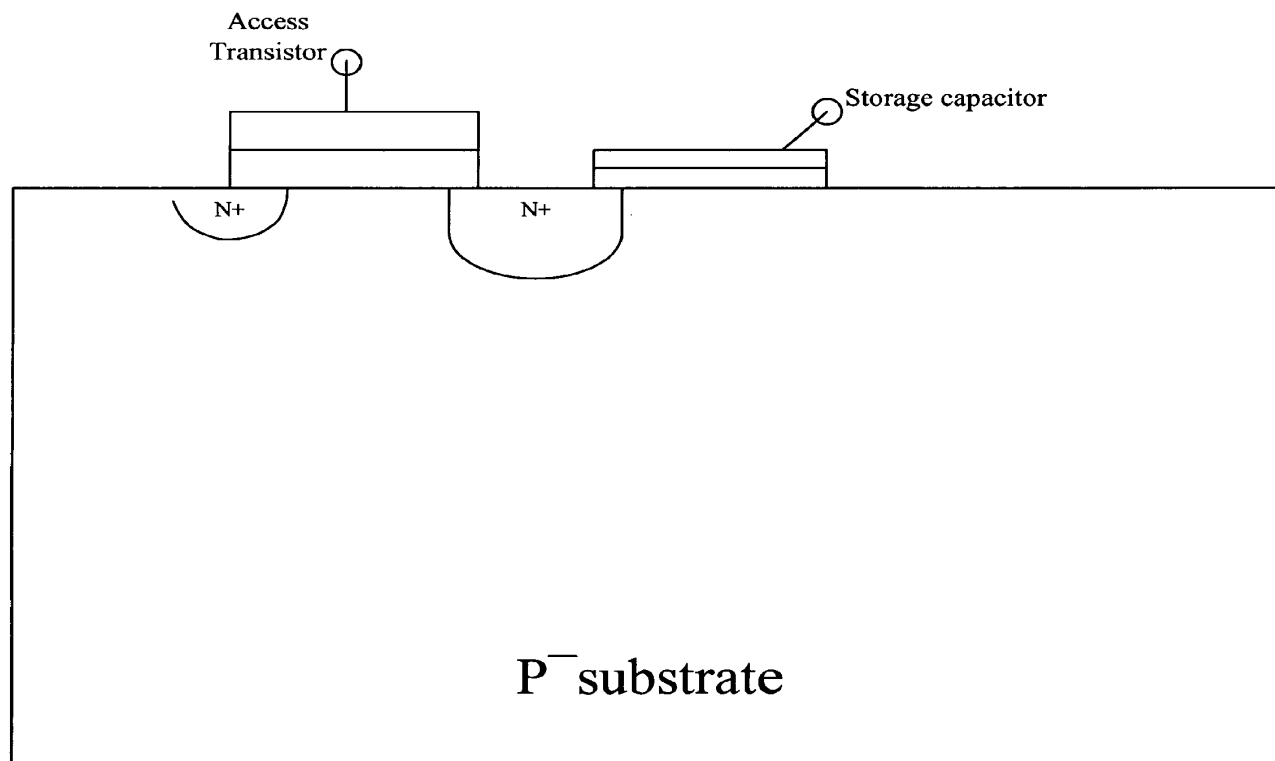


FIGURE 3(c) Prior art for a 1T-1C DRAM memory cell

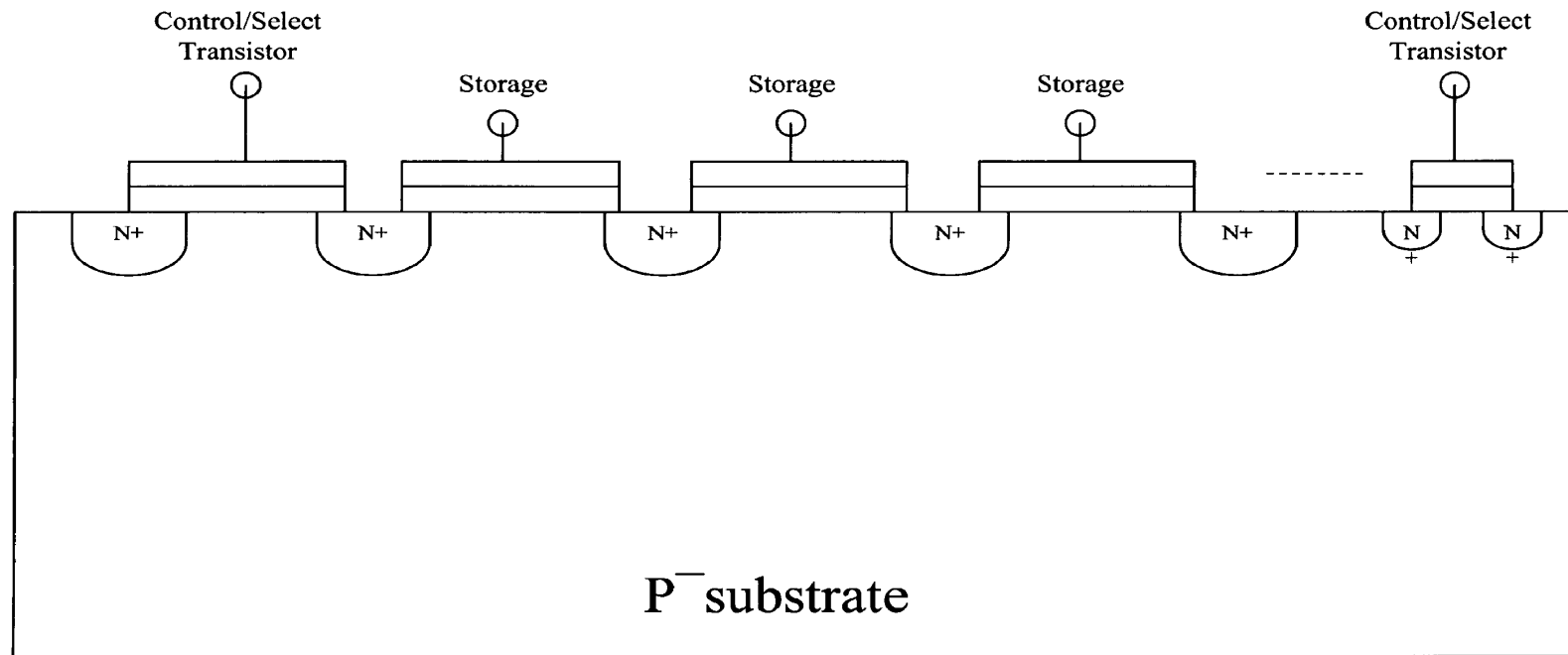


FIGURE 3(d) Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

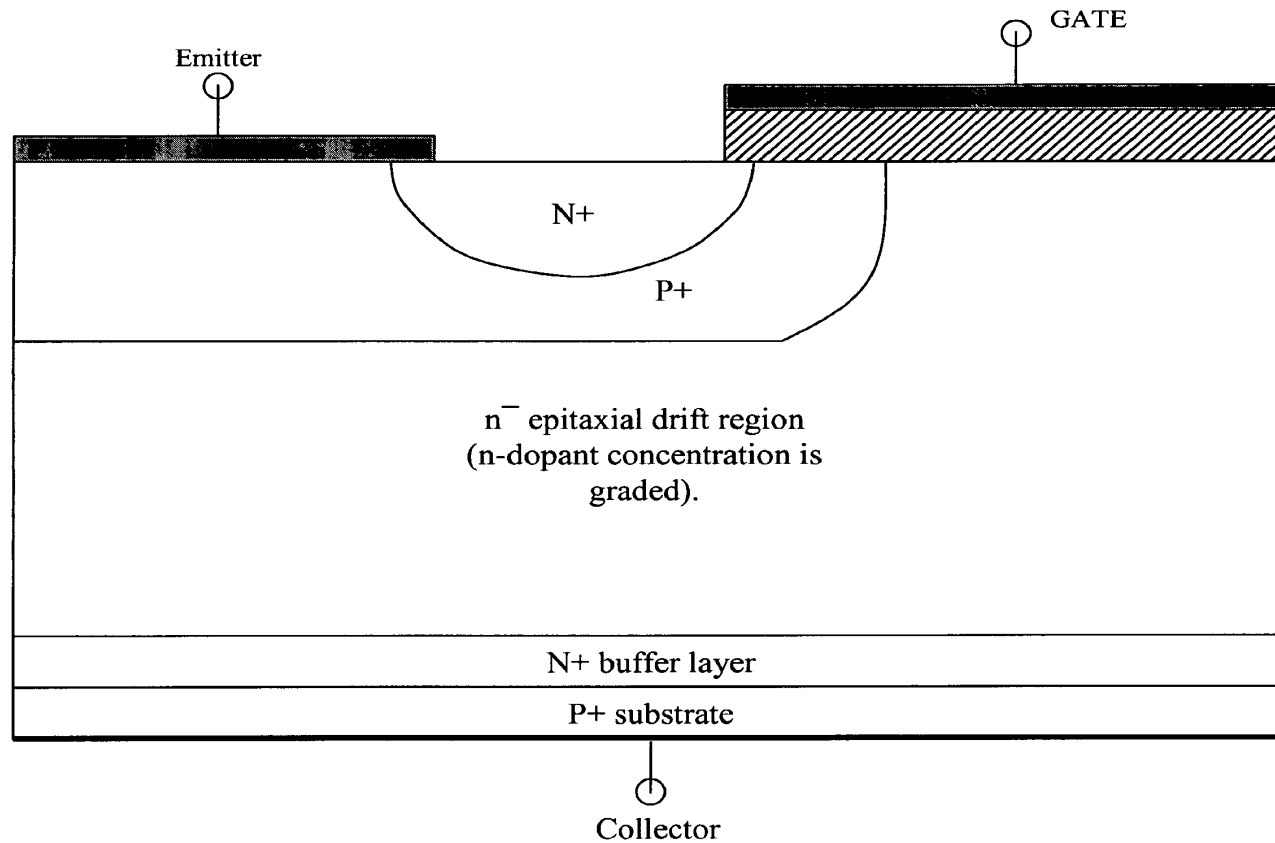


FIGURE 4 A dopant - concentration grinded drift region in a IGBT

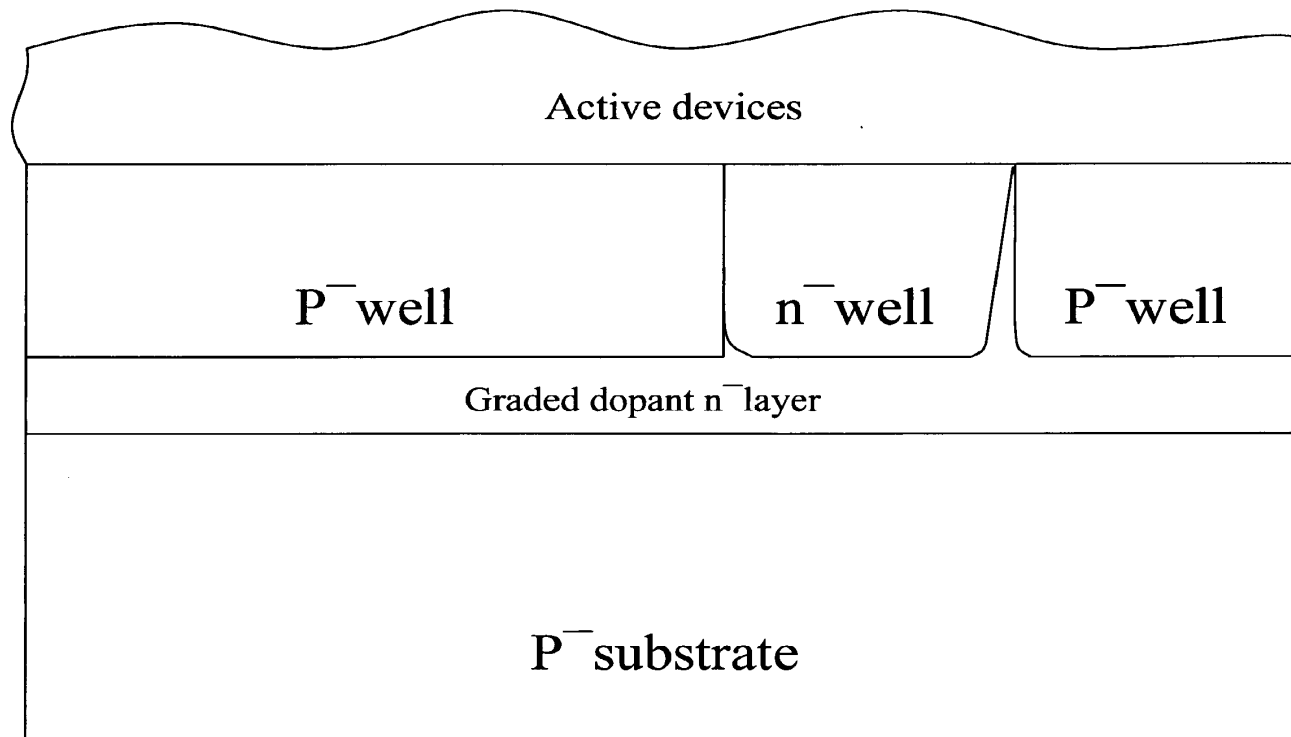


FIGURE 5(a) A CMOS Substrate for digital, mixed, signal, and sensors IC's

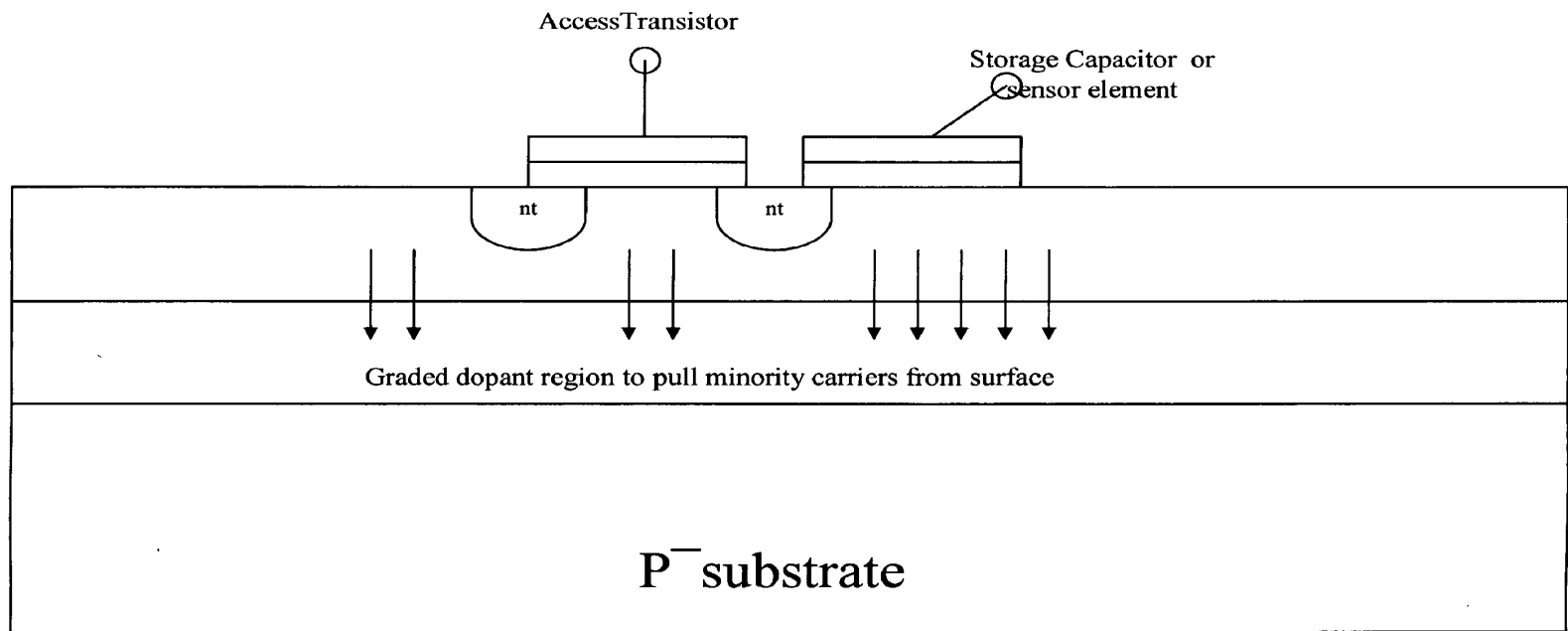


FIGURE 5(b) CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

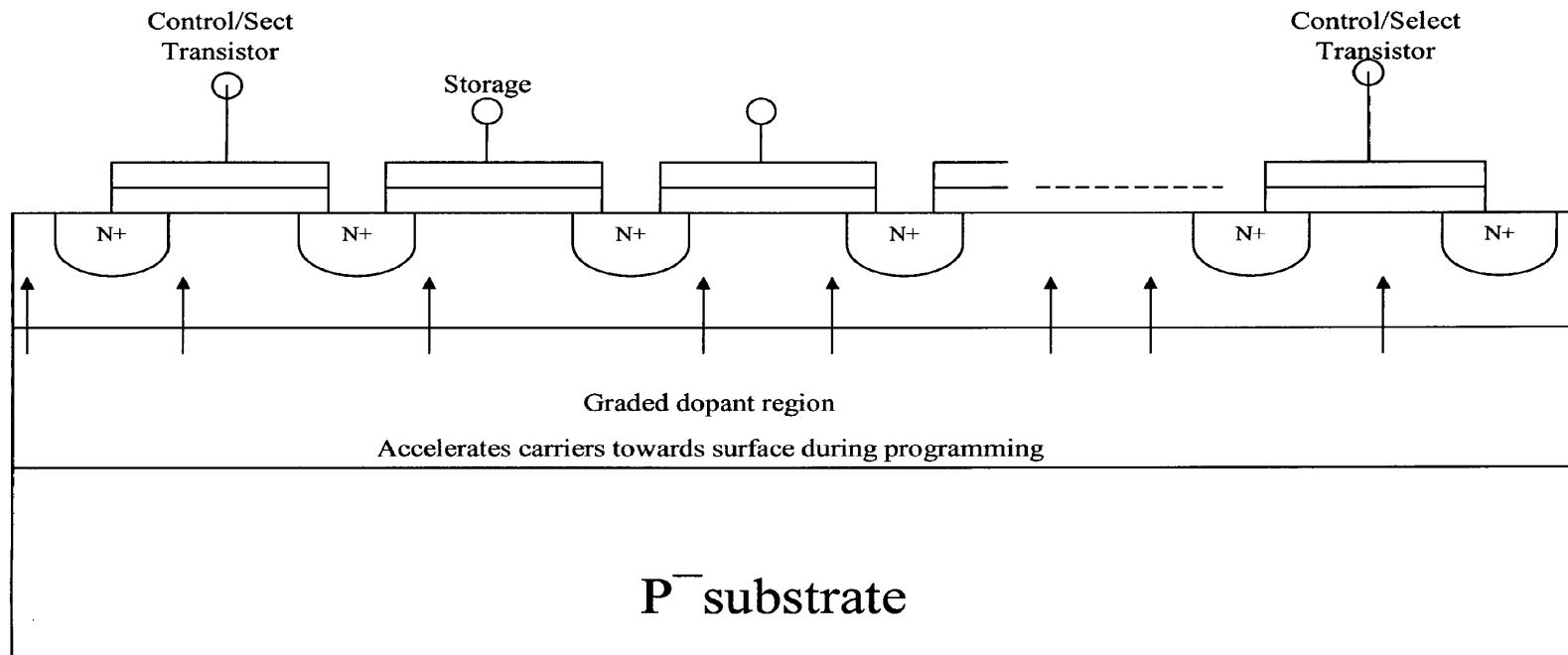


FIGURE 5(c) CMOS Substrate for a NAND flash device to improve programming times

Express Mail Label
No. EV 507 272 815 US

PTO/SB/01 (08-03)

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(37 CFR 1.16 (e))
required)

Attorney Docket Number

43218-P001US

First Named Inventor

G.R. Mohan Rao

COMPLETE IF KNOWN

Application Number

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Art Unit

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Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

(Title of the Invention)

the specification of which



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Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				Yes	No
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

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Given Name (first and middle [if any]) G.R. Mohan		Family Name or Surname Rao	
Inventor's Signature <i>G.R. Mohan Rao</i>		Date <i>September 1, 2004</i>	
Residence: City McKinney	State Texas	Country US	Citizenship US
Mailing Address 1404 Westmont Drive			
City McKinney	State Texas	ZIP 75070	Country US
NAME OF SECOND INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any])		Family Name or Surname	
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☐ Additional inventors or a legal representative are being named on the _____ supplemental sheet(s) PTO/SB/02A or 02LR attached hereto.			

[Page 2 of 2]

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
First Named Inventor/Applicant Name:		G.R. Mohan Rao		
Filer:		Baxter Ward Banowsky.		
Attorney Docket Number:		1388-03		
Filed as Small Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	75	75
Utility Search Fee	2111	1	250	250
Utility Examination Fee	2311	1	100	100
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				425

Electronic Acknowledgement Receipt

EFS ID:	1434580
Application Number:	11622496
International Application Number:	
Confirmation Number:	3086
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
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Receipt Date:	12-JAN-2007
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Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Specification	specification.pdf	83116	no	7
Warnings:					
Information:					
2	Claims	claims.pdf	72618	no	1
Warnings:					
Information:					
3	Abstract	abstract.pdf	72564	no	1
Warnings:					
Information:					
4	Drawings	drawings.pdf	115914	no	10
Warnings:					
Information:					
5	Oath or Declaration filed	Oath.pdf	105074	no	2
Warnings:					
Information:					
6	Fee Worksheet (PTO-06)	fee-info.pdf	8378	no	2
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PATENT APPLICATION FEE DETERMINATION RECORD					Application or Docket Number 11/622,496		
Substitute for Form PTO-875							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))				75		300	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))				250		500	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))				100		200	
TOTAL CLAIMS (37 CFR 1.16(i))	8	minus 20 =		X\$ 25	X\$50	250	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	8	minus 3 =	5	X\$100	X\$200	1200	
APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			180		360		
			TOTAL	925	TOTAL		
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =	
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =	
	Application Size Fee (37 CFR 1.16(s))			180		360	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =	
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =	
	Application Size Fee (37 CFR 1.16(s))			N/A		N/A	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

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11/622,496	01/12/2007	2811	425	43218-P001US	10	8	8

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Applicant(s)

G.R. Mohan Rao, McKinney, TX;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a DIV of 10/934,915 09/03/2004

Foreign Applications

If Required, Foreign Filing License Granted: 02/08/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/622,496**

Projected Publication Date: 05/17/2007

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/622,496	01/12/2007	G.R. Mohan Rao	43218-P001US

Winstead Sechrest & Minick P.C.
P.O. Box 50784
Dallas, TX 75201

CONFIRMATION NO. 3086
FORMALITIES
LETTER

Date Mailed: 02/08/2007

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given TWO MONTHS from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Additional claim fees of \$500 as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$500 for a small entity

- Total additional claim fee(s) for this application is \$500
 - \$500 for 5 independent claims over 3.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.



Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 3 - OFFICE COPY



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

22

ss

2

2

2

2

22

22

2

2

Sir:

1. This transmittal with Certificate of Mailing;
2. Power of Attorney and Correspondence Address Indication Form;
3. Check No. 94, in the amount of \$500.00, to cover the fees associated with the above referenced application for including 5 independent claims over 3; and
4. A return postcard which I would appreciate you date stamping and returning to me.

You are hereby authorized and requested to charge any additional fees or underpayment of fees related to this application to deposit account no. 50-3886. Please credit any over payment of fees to such deposit account as well.

01 FC:2201

1

Hon. Commissioner for Patents
March 20, 2007
Page 2

Attorney Docket No. **1388-03**
Customer No. **61400**

Date: 3/20/07

Respectfully submitted,


Baxter W. Banowsky
Registration No: 58,170

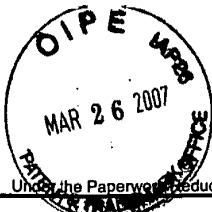
BANOWSKY & LEVINE, P.C.
12001 N. Central Expressway
Suite 790
Dallas, Texas 75243
(214) 871-1300
(214) 871-0038 (facsimile)
Customer No. **61400**

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 3-20-07.

Jackie L. Jenkins
Printed Name

Jackie L. Jenkins
Signature



PTO/SB/81 (01-06)

Approved for use through 12/31/2008. OMB 0651-0035

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**POWER OF ATTORNEY
and
CORRESPONDENCE ADDRESS
INDICATION FORM**

Application Number	11/622,496
Filing Date	01/12/2007
First Named Inventor	ROA, G. R. Mohan
Title	Semiconductor Devices with Graded
Art Unit	
Examiner Name	
Attorney Docket Number	1388-04

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer Number:

61400

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number:

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OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
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Telephone		Email			

I am the:

☒ Applicant/Inventor.☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)**SIGNATURE of Applicant or Assignee of Record**

Signature	<i>G. R. Mohan Rao</i>	Date	<i>March 13, 2007</i>
Name	RAO, G. R. Mohan	Telephone	<i>972-231-4550 ext 1</i>
Title and Company	<i>Green Thread LLC, Dallas, Texas</i>		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/622,496	01/12/2007	G.R. Mohan Rao	1388-04

61400
BANOWSKY & LEVINE, P.C
12001 N. CENTRAL EXPRESSWAY
SUITE 790
DALLAS, TX 75243

CONFIRMATION NO. 3086



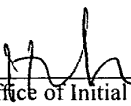
OC000000023487076

Date Mailed: 04/20/2007

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/26/2007.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.


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11/622,496	01/12/2007	G.R. Mohan Rao	1388-04

CONFIRMATION NO. 3086

61400
BANOWSKY & LEVINE, P.C
12001 N. CENTRAL EXPRESSWAY
SUITE 790
DALLAS, TX 75243

Title: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Publication No. US-2007-0158790-A1

Publication Date: 07/12/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Pre-Grant Publication Division, 703-605-4283



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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/622,496	01/12/2007	G.R. Mohan Rao	1388-04

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
11/622,496	01/12/2007	2811	925	1388-04	8	8

CONFIRMATION NO. 3086

UPDATED FILING RECEIPT



OC000000026392551

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12001 N. CENTRAL EXPRESSWAY
SUITE 790
DALLAS, TX 75243

Date Mailed: 10/25/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

G.R. Mohan Rao, McKinney, TX;

Power of Attorney: The patent practitioners associated with Customer Number 61400

Domestic Priority data as claimed by applicant

This application is a DIV of 10/934,915 09/03/2004 ABN

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/622,496	01/12/2007	G.R. Mohan Rao	1388-04	3086

61400 7590 04/15/2008
BANOWSKY &LEVINE, P.C
12001 N. CENTRAL EXPRESSWAY
SUITE 790
DALLAS, TX 75243

EXAMINER

ARORA, AJAY

ART UNIT	PAPER NUMBER
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2892

MAIL DATE	DELIVERY MODE
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04/15/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	11/622,496		RAO, G.R. MOHAN	
	Examiner		Art Unit	
	AJAY K. ARORA		2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 12 January 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) 1-8 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
---	--

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species :

- Embodiment 1 of Figure 4
- Embodiment 2 of Figure 5a
- Embodiment 3 of Figures 5b and 5c

The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election of the species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species.

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./

/Thao X Le/

Application/Control Number: 11/622,496
Art Unit: 2892

Page 5

Examiner, Art Unit 2892

Supervisory Patent Examiner, Art
Unit 2892

<i>Index of Claims</i> 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	04/08/2008								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
	8	÷								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	§	
	§	
RAO, G.R. MOHAN	§	Confirmation No. 3086
	§	
Serial No. 11/622,496	§	Group Art Unit: 2892
	§	
Filed: 12 JANUARY 2007	§	Examiner: AJAY K. ARORA
	§	
For: SEMICONDUCTOR DEVICES	§	
WITH GRADED DOPANT REGIONS	§	

ELECTION UNDER 35 U.S.C. § 121

This paper is in response to the restriction requirement set forth in the Office Action mailed April 15, 2008, having a one month shortened statutory period for response, wherein the Examiner required restriction between the following embodiments:

- Embodiment 1 - Figure 4
- Embodiment 2 - Figure 5(a)
- Embodiment 3 - Figures 5(b) and 5(c)

Applicant elects Embodiment 3 for initial prosecution on the merits. Applicant identifies Claims 3 through 8 as encompassing the elected species.

Applicant notes that the examiner has determined that no claims are generic. Applicant respectfully traverses this finding and asserts that claims 3-8 are generic as to all embodiments. Initially, Applicant notes that this is a division application of Application Serial No. 10/934,915. In Application Serial No. 10/934,915 the Office issued an election/restriction requirement similar to the present office action. In that office action, dated March 28, 2006, the office asserted that claim 8 in the present application (claim 9 in Application Serial No. 10/934,915)

was generic as to all species. Additionally, the office asserted that claim 7 in the present application (claim 8 in Application Serial No. 10/934,915) was generic as to embodiments 1 and 3.

With the exception of Fig. 4 and the references to it in the specification, the balance of the specification and illustrations are of CMOS technology. A CMOS device has both p-ch and n-ch transistors (and both p and n wells). Accordingly, graded dopant concentrations have to be "optimized" for both donors and acceptors. Further, sweeping away minority carriers with donor gradient is generic to all of the embodiments as set forth in paragraph 12 of the specification with respect to IGBT and paragraph 13 with respect to CMOS. Additionally, although the epitaxial layer is only illustrated in Fig. 4, it is referred to in paragraph 13 as being applicable to the CMOS devices of Figs. 5(a), (b) and (c).

To the extent that the examiner agrees with Applicant that claims 3 through 8 are generic, then this election may be considered without traverse.

Applicant reserves the right to file one or more Divisional Applications for the non-elected inventions which the Examiner has indicated are patentably distinct.

Applicant does not believe that any extension of time or any additional fees are necessary for the consideration of the present paper. However, in the event that an extension of time or any additional fees are necessary for consideration of the present paper, I authorize the Commissioner to charge such fees, including fees for extension of time, to Deposit Account No. 50-3886.

Attorney Docket No. **1388-04**
Customer No. **61400**

Respectfully submitted,

Date: May 13, 2008

/s/ Baxter W. Banowsky
Baxter W. Banowsky
Registration No: 58,170

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Customer No. **61400**

Electronic Acknowledgement Receipt

EFS ID:	3293940
Application Number:	11622496
International Application Number:	
Confirmation Number:	3086
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	61400
Filer:	Baxter Ward Banowsky.
Filer Authorized By:	
Attorney Docket Number:	1388-04
Receipt Date:	13-MAY-2008
Filing Date:	12-JAN-2007
Time Stamp:	10:54:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	election.pdf	82764 712fac00bdb00669b974700556a19ee705446d44	no	3

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/622,496	01/12/2007	G.R. Mohan Rao	1388-04	3086
61400 7590 07/28/2008 BANOWSKY &LEVINE, P.C 12001 N. CENTRAL EXPRESSWAY SUITE 790 DALLAS, TX 75243			EXAMINER ARORA, AJAY	
			ART UNIT 2892	PAPER NUMBER
			MAIL DATE 07/28/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/622,496		Applicant(s) RAO, G.R. MOHAN	
	Examiner AJAY K. ARORA		Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 13 May 2008.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) 1 and 2 is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) 3-8 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Election/Restrictions

1. Applicant's election of embodiment 3, claims 3-8 in the reply filed on 05/13/2008 is acknowledged. Because examiner agrees that claims 3-8 are generic to all embodiments as stated by applicant on page 2, lines 12-13 of applicant's response, as a condition for election without traverse, and applicant did not distinctly and specifically point out any additional supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhodes (US 2003/0042511), hereinafter Rhodes.

Regarding claim 3, Rhodes (refer to Figures 5-14) teaches a semiconductor device with graded dopant concentration (page 4, para 0046, 1st sentence) in the well regions (160, 170, 180) to aid carrier movement away from the active surface regions, towards the substrate (page 6, para 0061; page 4, para 0045 & 0049).

Regarding claim 6, Rhodes (US 2003/0042511) (refer to Figures 5-14) teaches a semiconductor device with at least one graded dopant concentration (page 4, para 0046, 1st sentence) fabricated with ion implantation (page 4, para 0047, last sentence), to provide an aiding or retarding electric field locally in a monolithic integrated circuit.

Note that claim 6 is a product claim but recites a method of steps therein, i.e. "fabricated with ion implantation". Therefore, claim 8 amounts to a product by process claim. *"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."* In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

4. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Cathey (US 2002/0093281), hereinafter Cathey.

Regarding claim 4, Cathey teaches a semiconductor device with graded dopant concentration in the substrate (page 2, para 0027) region to aid carrier movement away from the active surface regions, deeper towards the substrate (page 3, claims 1, 5 and 6).

5. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Kane (US 5,029,277), hereinafter Kane.

Regarding claim 5, Kane teaches a semiconductor device with at least one each of dopant concentration of both donor and acceptor, to optimize the operating performance of the device (Col. 5, lines 5-40).

6. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Baliga (US 5,637,898), hereinafter Baliga.

Regarding claim 7, Baliga (US 5,637,898) teaches a semiconductor device with at least one graded dopant concentration in an epitaxial layer (Col. 4, lines 15-21 and Col. 3, lines 45-50).

7. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Macris (US 2002/0134419), hereinafter Macris.

Regarding claim 8, Macris teaches a semiconductor device where one layer of dopant from one wafer, is transferred to another wafer having either same polarity or different polarity dopant through wafer bonding or similar processes (page 4, para 0076).

Note that claim 8 is a product claim but recites a method of steps therein, i.e. "one layer of dopant from one wafer, is transferred to another wafer" and "wafer bonding or similar processes". Therefore, claim 8 amounts to a product by process claim. *"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."* *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

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/A. K. A./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art
Unit 2892

Notice of References Cited	Application/Control No. 11/622,496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner AJAY K. ARORA	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0042511	03-2003	Rhodes, Howard E.	257/232
*	B	US-2002/0093281	07-2002	Cathey, David A.	313/336
*	C	US-5,029,277	07-1991	Kane, Robert C.	250/214C
*	D	US-5,637,898	06-1997	Baliga, Bantval J.	257/330
*	E	US-2002/0134419	09-2002	Macris, Chris	136/204
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	07/24/2008								
	1	N								
	2	N								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								

<i>Search Notes</i> 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
257	655, 269	7/24/2008	AKA

SEARCH NOTES		
Search Notes	Date	Examiner
Refer to EAST search history report	7/24/2008	AKA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner



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BIB DATA SHEET

CONFIRMATION NO. 3086

SERIAL NUMBER 11/622,496	FILING or 371(c) DATE 01/12/2007 RULE	CLASS 257	GROUP ART UNIT 2892	ATTORNEY DOCKET NO. 1388-04	
APPLICANTS G.R. Mohan Rao, McKinney, TX; ** CONTINUING DATA ***** This application is a DIV of 10/934,915 09/03/2004 ABN ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED *** SMALL ENTITY ** 02/08/2007					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /AJAY ARORA/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TX	SHEETS DRAWINGS 10	TOTAL CLAIMS 8 INDEPENDENT CLAIMS 8
ADDRESS BANOWSKY & LEVINE, P.C 12001 N. CENTRAL EXPRESSWAY SUITE 790 DALLAS, TX 75243 UNITED STATES					
TITLE SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS					
FILING FEE RECEIVED 925	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	579	(257/655,269).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/24 09:14
S1	2	("20070158790").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/04/08 11:10
S2	58	("20020074585" "20040063288" "4001864" "4347654" "4866000" "5130262" "5213988" "5329144" "5480816" "5496746" "5569612" "5575862" "5797999" "6211028" "6452086" "6472715" "6670544" "6683343" "6696314" "6706550" "6713813" "6737722" "6744117" "6747883" "6753202" "6754093" "6756616" "RE37441"). PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/08 11:19
S3	1096	(graded OR gradation) WITH (dopant OR doping) WITH concentration	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/08 11:47
S4	805	S3 AND ("257" OR "438").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/08 11:47
S5	253	(graded OR gradation) WITH (dopant OR doping) WITH concentration WITH (semiconductor OR silicon)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/08 11:49

S6	7	S5 SAME (carrier WITH (movement OR mobility))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/08 11:51
S7	48	S5 AND (((carrier OR electron OR hole) WITH (movement OR mobility)) SAME ((emitter WITH collector) OR (source WITH drain)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/08 11:55
S8	58	("20020074585" "20040063288" "4001864" "4347654" "4866000" "5130262" "5213988" "5329144" "5480816" "5496746" "5569612" "5575862" "5797999" "6211028" "6452086" "6472715" "6670544" "6683343" "6696314" "6706550" "6713813" "6737722" "6744117" "6747883" "6753202" "6754093" "6756616" "RE37441"). PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/18 12:16
S9	13	S8 AND ("dopant concentration" OR "concentratio of dopant")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/18 12:16
S10	13	S8 AND ("dopant concentration" OR "concentration of dopant")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/18 12:17
S11	0	S8 AND (dop\$3 WITH (concentrat\$3 OR amount OR quantity) WITH (variable OR varying OR grad\$3)) AND ((doping OR dopant) WITH well) AND ((carrier OR charge) WITH (moving OR movement OR mobile OR mobility))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/18 12:22

S12	1136	(graded OR gradation) WITH (dopant OR doping) WITH concentration	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/18 12:22
S13	86	S12 AND (dop\$3 WITH (concentrat\$3 OR amount OR quantity) WITH (variable OR varying OR grad\$3)) AND ((doping OR dopant) WITH well) AND ((carrier OR charge) WITH (moving OR movement OR mobile OR mobility))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/18 12:22
S14	29	("20020068409" "6303450" "6437406" "6458665" "6483158" "6489223" "6509241"). PN. OR ("6743684"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/18 13:13
S15	34	uniform\$2 WITH dop\$3 WITH drift WITH epitaxial	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:19
S16	2	("5637898").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/23 15:26
S17	0	(non-uniform\$2 OR nonuniform\$2 OR grad43 OR grading OR gradient) WITH (dopant OR doping) WITH well WITH carrier WITH (movement OR mobility) WITH ((away WITH active WITH surface) OR (towards WITH substrate))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:40

S18	4	(non-uniform\$2 OR nonuniform\$2 OR grad\$3 OR grading OR gradient) WITH (dopant OR doping) WITH well WITH carrier WITH (movement OR mobility) WITH ((away WITH active WITH surface) OR (towards WITH substrate))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:40
S19	4	("4001864").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/23 15:43
S20	58	("20020074585" "20040063288" "4001864" "4347654" "4866000" "5130262" "5213988" "5329144" "5480816" "5496746" "5569612" "5575862" "5797999" "6211028" "6452086" "6472715" "6670544" "6683343" "6696314" "6706550" "6713813" "6737722" "6744117" "6747883" "6753202" "6754093" "6756616" "RE37441").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:57
S21	92	S15 S19 S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:58
S22	39	S21 AND ((non-uniform \$2 OR nonuniform\$2 OR grad\$3 OR grading OR gradient) WITH (dopant OR doping))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:58
S23	60	S21 AND well	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:59

S24	39	S22 AND well	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 15:59
S25	2	S22 AND (well WITH carrier WITH (movement OR mobility) WITH ((away WITH active WITH surface) OR (towards WITH substrate)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 16:00
S26	3	S22 AND (well WITH (carrier OR movement OR mobility) WITH ((away WITH active WITH surface) OR (towards WITH substrate)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 16:00
S27	2	("20030042511").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/23 16:05
S28	2	S21 AND (substrate WITH carrier WITH away WITH ((active WITH surface) OR (towards NEAR2 substrate) OR (direction NEAR4 substrate)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 17:17
S29	3	S21 AND (substrate WITH (carrier OR holes OR electron OR majority OR charge) WITH away WITH ((active WITH surface) OR (towards NEAR2 substrate) OR (direction NEAR4 substrate)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 17:18
S30	30	S21 AND ((non-uniform \$2 OR nonuniform\$2 OR grad\$3 OR grading OR gradient) WITH (dopant OR doping) WITH substrate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 17:26

S31	253	(grad\$3 OR grading OR gradient) NEAR2 (dopant OR doping) NEAR4 substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 17:33
S32	5	dopant WITH concentration WITH donor WITH acceptor WITH optimiz\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:02
S33	2	10/182,784	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:06
S34	0	S20 AND (dopant WITH concentration WITH donor WITH acceptor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:22
S35	0	S20 AND (dopant WITH donor WITH acceptor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:22
S36	5	(dopant WITH donor WITH acceptor WITH optimiz\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:26
S37	5	(dopant WITH donor WITH acceptor WITH (optimiz\$ OR optimization OR optimal))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:27
S38	487	(donor WITH acceptor WITH (optimiz\$ OR optimization OR optimal))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:27

S39	14	S38 AND semiconductor. ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:28
S40	0	(layer WITH dopant WITH wafer WITH transfer\$4 WITH ((another OR second OR alternate) NEAR1 wafer)) AND (wafer NEAR1 bond \$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:49
S41	0	(dopant WITH wafer WITH transfer\$4 WITH ((another OR second OR alternate) NEAR1 wafer)) AND (wafer NEAR1 bond \$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:49
S42	0	(dopant WITH transfer\$4 WITH ((another OR second OR alternate) NEAR1 wafer)) AND (wafer NEAR1 bond\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:50
S43	0	(dopant WITH transfer\$4 WITH ((another OR second OR alternate) NEAR1 wafer))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:50
S44	14807	wafer NEAR1 bond\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:51
S45	33	S44 AND (dopant WITH transfer\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/23 18:51

7/ 24/ 2008 9:26:20 AM

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	§	
	§	
RAO, G.R. MOHAN	§	Confirmation No. 3086
	§	
Serial No. 11/622,496	§	Group Art Unit: 2892
	§	
Filed: 12 JANUARY 2007	§	Examiner: ARORA, AJAY
	§	
For: SEMICONDUCTOR DEVICES	§	
WITH GRADED DOPANT REGIONS	§	

**AMENDMENT AND RESPONSE
TO OFFICE ACTION MAILED JULY 28, 2008**

I. INTRODUCTORY COMMENTS:

The present paper is submitted as a complete response to the non-final Office Action mailed July 28, 2008 having a shortened statutory period of response of three months. Applicant does not believe that any extension of time or any additional fees are necessary for the consideration of the present paper. However, in the event that an extension of time or any additional fees are necessary for consideration of the present paper, I authorize the Commissioner to charge such fees, including fees for extension of time, to Deposit Account No. 50-3886.

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

II. AMENDMENTS TO THE CLAIMS:

The text of all claims under examination is submitted, and the status of each is identified.

This listing of claims replaces all prior versions and listings in the application.

Listing of Claims

Claims 1-2 (Cancelled)

3. (currently amended) A VLSI digital semiconductor device with graded dopant concentration in the well regions, to aid carrier movement away from the active surface regions, towards the substrate.
4. (currently amended) A VLSI digital semiconductor device with graded dopant concentration in the substrate region to aid carrier movement away from the active surface regions, deeper towards the substrate.
5. (currently amended) A VLSI digital semiconductor device with at least one each of dopant concentration of both donor and acceptor, to optimize the operating performance of the device.
6. (currently amended) A VLSI digital semiconductor device with at least one graded dopant concentration fabricated with ion implantation, to provide an aiding or retarding electric field locally in a monolithic integrated circuit.
7. (currently amended) A VLSI digital semiconductor device with at least one graded dopant concentration in an epitaxial layer.
8. (currently amended) A VLSI digital semiconductor device where one layer of dopant from one wafer, is transferred to another wafer having either same polarity or different polarity dopant through wafer bonding or similar processes.

III. REMARKS:

Claims 3 through 8 are pending herein.

Claims 1-2 have been cancelled without prejudice or disclaimer. Claims 3-8 have been amended, more particularly, to point out the claimed subject matter. It is respectfully submitted that Claims 3-8 are in full compliance with the broad dictates of 35 U.S.C. § 112. Favorable consideration of Claims 3-8 are respectfully requested.

Claims 3-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by various references more particularly described below. Insofar as these references may be applied against the present claims, this rejection is respectfully traversed.

Each of claims 3-8 have been amended to clarify that the claimed invention relates to the field of VLSI digital semiconductor devices. By definition, a VLSI semiconductor device means a device consisting of at least one million active elements (an active element is a semiconductor transistor or gate consisting of at least two transistors) that can be active when a voltage (or current) is applied. By contrast, SSI (small scale integration) is 1 to 1,000 active elements, MSI (medium scale integration) is up to 100,000 active elements and LSI (large scale integration) is 100,000 to 1,000,000 active elements. As is more fully set forth below, each of the cited references pertains to non-VLSI non-digital technology.

Claims 3 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Rhodes (US 2003/0042511), hereinafter Rhodes. Rhodes discloses a semiconductor based CMOS imaging device. Rhodes does not disclose or anticipate a VLSI digital semiconductor device.

Rhodes describes a CMOS image sensor- but, his sensor elements only uses electrons (a CMOS gate, by strict text book definition has a n-channel transistor that conducts electrons and a p-channel transistor that conducts holes). The "graded dopant" as described by Rhodes, is only in the "sensing element." Rhodes may have one million sensors (he may have a few CMOS trnasistors in periphery on non image sensing function). However, that does not make the device in Rhodes VLSI and certainly not CMOS VLSI.

In the present VLSI digital invention, every one of this 1 million (+) gates, albeit CMOS, has graded dopant for electrons as well as holes. Additionally, the present invention also allows more than one gradient for electrons and more than one gradient for holes. Neither Rhodes nor, for that matter, any of the other cited prior art show this novelty.

Claim 4 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Cathey (US 2002/0093281), hereinafter Cathey. Cathey discloses an electron field emitter for use in computer or other display devices. Cathey does not disclose or anticipate a VLSI digital semiconductor device.

Claim 5 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Kane (US 5,029,277), hereinafter Kane. Kane discloses a method for temperature compensation of a bipolar transistor junction through optically-induced carrier density enhancement. Kane does not disclose or anticipate a VLSI digital semiconductor device.

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Baliga (US 5,637,898), hereinafter Baliga. Baliga discloses a to semiconductor switching device for high power applications. Baliga does not disclose or anticipate a VLSI digital semiconductor device.

Claim 8 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Macris (US 2002/0134419), hereinafter Macris. Macris discloses a heat sink. Macris does not disclose or anticipate a VLSI digital semiconductor device.

Accordingly, for the foregoing reasons, it is respectfully submitted that the cited references do not disclose or suggest the claimed VLSI digital semiconductor device. The rejection of claim 3-8 under 35 U.S.C. §102(b) as anticipated by the cited references should therefore be withdrawn. When read in light of the specification, Applicant submits that none of the foregoing amendments narrow the claims with regard to the claimed semiconductor device.

For all the foregoing reasons, it is respectfully submitted that claims 3-8 are in condition for allowance. Favorable reconsideration and allowance of claims 3-8 is respectfully requested.

Respectfully submitted,

Date: October 28, 2008

/Baxter W. Banowsky/
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Electronic Acknowledgement Receipt

EFS ID:	4187673
Application Number:	11622496
International Application Number:	
Confirmation Number:	3086
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	61400
Filer:	Baxter Ward Banowsky.
Filer Authorized By:	
Attorney Docket Number:	1388-04
Receipt Date:	28-OCT-2008
Filing Date:	12-JAN-2007
Time Stamp:	12:38:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		OA07_28_08_rsp.pdf	95157	yes	5
			946d28a7cd361b68ab61b5db9f538127f395c268		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Extension of Time	1	1
	Claims	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	5
Warnings:			
Information:			
Total Files Size (in bytes):		95157	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/622,496		Filing Date 01/12/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
TOTAL			TOTAL		TOTAL					
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	10/28/2008	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 6	Minus	** 20	= 0	X \$26 =	0	OR	X \$ =	
	Independent (37 CFR 1.16(h))	* 6	Minus	*** 8	= 0	X \$110 =	0	OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE									
TOTAL			TOTAL		TOTAL					
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE									
TOTAL			TOTAL		TOTAL					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/ERIC DANTZLER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/622,496	01/12/2007	G.R. Mohan Rao	1388-04	3086
61400 7590 01/06/2009 BANOWSKY &LEVINE, P.C 12001 N. CENTRAL EXPRESSWAY SUITE 790 DALLAS, TX 75243			EXAMINER ARORA, AJAY	
			ART UNIT 2892	PAPER NUMBER
			MAIL DATE 01/06/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/622,496		Applicant(s) RAO, G.R. MOHAN	
	Examiner AJAY K. ARORA		Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 28 October 2008.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 3-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) 3-8 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 3 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhodes (US 2003/0042511) of prior record, hereinafter Rhodes.

Regarding claim 3, Rhodes (refer to Figures 5-14) teaches a semiconductor device with graded dopant concentration (page 4, para 0046, 1st sentence) in the well regions (160, 170, 180) to aid carrier movement away from the active surface regions, towards the substrate (page 6, para 0061; page 4, para 0045 & 0049).

Regarding claim 6, Rhodes (US 2003/0042511) (refer to Figures 5-14) teaches a semiconductor device with at least one graded dopant concentration (page 4, para 0046, 1st sentence) fabricated with ion implantation (page 4, para 0047, last sentence), to provide an aiding or retarding electric field locally in a monolithic integrated circuit.

Note that claim 6 is a product claim but recites a method of steps therein, i.e. "fabricated with ion implantation". Therefore, claim 8 amounts to a product by process claim. *"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."* In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

3. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Cathey (US 2002/0093281) of prior record, hereinafter Cathey.

Regarding claim 4, Cathey teaches a semiconductor device with graded dopant concentration in the substrate (page 2, para 0027) region to aid carrier movement away from the active surface regions, deeper towards the substrate (page 3, claims 1, 5 and 6).

4. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Kane (US 5,029,277) of prior record, hereinafter Kane.

Regarding claim 5, Kane teaches a semiconductor device with at least one each of dopant concentration of both donor and acceptor, to optimize the operating performance of the device (Col. 5, lines 5-40).

5. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Baliga (US 5,637,898) of prior record, hereinafter Baliga.

Regarding claim 7, Baliga (US 5,637,898) teaches a semiconductor device with at least one graded dopant concentration in an epitaxial layer (Col. 4, lines 15-21 and Col. 3, lines 45-50).

6. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Macris (US 2002/0134419) of prior record, hereinafter Macris.

Regarding claim 8, Macris teaches a semiconductor device where one layer of dopant from one wafer, is transferred to another wafer having either same polarity or different polarity dopant through wafer bonding or similar processes (page 4, para 0076).

Note that claim 8 is a product claim but recites a method of steps therein, i.e. "one layer of dopant from one wafer, is transferred to another wafer" and "wafer bonding or similar processes". Therefore, claim 8 amounts to a product by process claim. *"Even though product-by-process claims are limited by and defined by the process, determination of*

patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

Response to Arguments

7. Applicant's arguments filed 10/28/2008 have been fully considered but they are not persuasive.

8. In response to applicant's arguments, the recitation "A VLSI digital semiconductor device" (see claims 3-8) has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., "every one of this 1 million (+) gates, albeit CMOS, has graded dopant for electrons as well as holes" - see page 4, 2nd paragraph, of applicant's response) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

10. Other arguments presented by the applicant on page 4-5 are similar to the above addressed arguments.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art
Unit 2892

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	539	(257/655). CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/01/02 21:01

1/ 2/ 2009 9:08:30 PM

C:\Documents and Settings\aarora\My Documents\EAST\Workspaces\11622496.
wsp

<i>Index of Claims</i> 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	01/02/2009								
	1	-								
	2	-								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								

Search Notes 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
257	655	1/2/2009	AKA

SEARCH NOTES		
Search Notes	Date	Examiner
Refer to EAST search history report	7/24/2008	AKA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/A. K. A/ Examiner.Art Unit 2892	
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL **(Submitted Only via EFS-Web)**

Application Number	11/622,496	Filing Date	2007-01-12	Docket Number (if applicable)	1388-04	Art Unit	2892
First Named Inventor	RAO, G.R. MOHAN			Examiner Name	ARORA, AJAY		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____.
 (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
 Deposit Account No 503886

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Baxter W. Banowsky/	Date (YYYY-MM-DD)	2009-04-10
Name	Baxter W. Banowsky	Registration Number	58170

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	§	
	§	
RAO, G.R. MOHAN	§	Confirmation No. 3086
	§	
Serial No. 11/622,496	§	Group Art Unit: 2892
	§	
Filed: 12 JANUARY 2007	§	Examiner: ARORA, AJAY
	§	
For: SEMICONDUCTOR DEVICES	§	
WITH GRADED DOPANT REGIONS	§	

AMENDMENT AND RESPONSE
TO OFFICE ACTION MAILED JANUARY 6, 2009

I. INTRODUCTORY COMMENTS:

The present paper is submitted as a complete response to the final Office Action mailed January 6, 2009, having a shortened statutory period of response of three months. Applicant believes that a one month extension of time and the corresponding fees are necessary for the consideration of the present paper, such fees being paid contemporaneously with the filing of this paper. However, in the event that a further extension of time or any additional fees are necessary for consideration of the present paper, I authorize the Commissioner to charge such fees, including fees for extension of time, to Deposit Account No. 50-3886.

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

II. AMENDMENTS TO THE CLAIMS:

The text of all claims under examination is submitted, and the status of each is identified.

This listing of claims replaces all prior versions and listings in the application.

Listing of Claims

Claims 1-2 (Cancelled)

3. (currently amended) A VLSI digital semiconductor device with graded dopant concentration in the well regions and the active channel regions, to aid carrier movement away from the active surface regions, towards the substrate.

4. (currently amended) A VLSI digital semiconductor device with graded dopant concentration in the active channel regions, the well regions and the substrate region to aid carrier movement away from the active surface regions, deeper towards the substrate.

5. (currently amended) A VLSI digital semiconductor device with at least one each of dopant concentration of both donor and acceptor in both the well and channel regions, to optimize the operating performance of the device.

6. (currently amended) A VLSI digital semiconductor device with at least one graded dopant concentration fabricated with ion implantation, to provide an aiding or retarding electric field locally, in both well and channel regions, in a monolithic integrated circuit.

7. (currently amended) A VLSI digital semiconductor device with at least one graded dopant concentration in an epitaxial layer where the epitaxial layer forms the substratum for well and channel regions.

8. (currently amended) A VLSI digital semiconductor device where one layer consisting of dopant gradients in both well and channel regions from one wafer, is transferred to another wafer having either same polarity or different polarity dopant through wafer bonding or similar processes.

III. REMARKS:

Claims 3 through 8 are pending herein.

Claims 1-2 have been cancelled without prejudice or disclaimer. Claims 3-8 have been amended, more particularly, to point out the claimed subject matter. It is respectfully submitted that Claims 3-8 are in full compliance with the broad dictates of 35 U.S.C. § 112. Favorable consideration of Claims 3-8 are respectfully requested.

Claims 3-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by various references more particularly described below. Insofar as these references may be applied against the present claims, this rejection is respectfully traversed.

Each of claims 3-8 have been amended to clarify that the claimed invention relates to the field of VLSI digital semiconductor devices which include graded dopant concentrations in both the active and well regions. By definition, a VLSI semiconductor device means a device consisting of at least one million active elements (an active element is a semiconductor transistor or gate consisting of at least two transistors) that can be active when a voltage (or current) is applied. By contrast, SSI (small scale integration) is 1 to 1,000 active elements, MSI (medium scale integration) is up to 100,000 active elements and LSI (large scale integration) is 100,000 to 1,000,000 active elements. As is more fully set forth below, each of the cited references pertains to non-VLSI non-digital technology.

Claims 3 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Rhodes (US 2003/0042511), hereinafter Rhodes. Rhodes discloses a semiconductor based CMOS imaging device. Rhodes does not disclose or anticipate a VLSI digital semiconductor device.

Rhodes describes a CMOS image sensor- but, his sensor elements only uses electrons (a CMOS gate, by strict text book definition has a n-channel transistor that conducts electrons and a p-channel transistor that conducts holes). The "graded dopant" as described by Rhodes, is only in the "sensing element." Rhodes may have one million sensors (he may have a few CMOS trnasistors in periphery on non image sensing function). However, that does not make the device in Rhodes VLSI and certainly not CMOS VLSI.

Further, Rhodes does not teach a graded dopant layer in both active and well regions.

In the present VLSI digital invention, every one of this 1 million (+) gates, albeit CMOS, has graded dopant for electrons as well as holes. Additionally, the present invention also allows more than one gradient for electrons and more than one gradient for holes. Neither Rhodes nor, for that matter, any of the other cited prior art show this novelty.

Claim 4 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Cathey (US 2002/0093281), hereinafter Cathey. Cathey discloses an electron field emitter for use in computer or other display devices. Cathey does not disclose or anticipate a VLSI digital semiconductor device with graded dopant concentrations in both the active and well regions.

Claim 5 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Kane (US 5,029,277), hereinafter Kane. Kane discloses a method for temperature compensation of a bipolar transistor junction through optically-induced carrier density enhancement. Kane does not disclose or anticipate a VLSI digital semiconductor device with graded dopant concentrations in both the active and well regions.

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Baliga (US 5,637,898), hereinafter Baliga. Baliga discloses a to semiconductor switching device for high power applications. Baliga does not disclose or anticipate a VLSI digital semiconductor device with graded dopant concentrations in both the active and well regions.

Claim 8 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Macris (US 2002/0134419), hereinafter Macris. Macris discloses a heat sink. Macris does not disclose or anticipate a VLSI digital semiconductor device with graded dopant concentrations in both the active and well regions.

Accordingly, for the foregoing reasons, it is respectfully submitted that the cited references do not disclose or suggest the claimed VLSI digital semiconductor device with graded dopant concentrations in both the active and well regions. The rejection of claim 3-8 under 35 U.S.C. §102(b) as anticipated by the cited references should therefore be withdrawn. When read in light of the specification, Applicant submits that none of the foregoing amendments narrow the claims with regard to the claimed semiconductor device.

For all the foregoing reasons, it is respectfully submitted that claims 3-8 are in condition for allowance. Favorable reconsideration and allowance of claims 3-8 is respectfully requested.

Respectfully submitted,

Date: April 10, 2009

/Baxter W. Banowsky/
Baxter W. Banowsky
Registration No: 58,170

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Customer No. **000061400**

Electronic Patent Application Fee Transmittal				
Application Number:		11622496		
Filing Date:		12-Jan-2007		
Title of Invention:		SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
First Named Inventor/Applicant Name:		G.R. Mohan Rao		
Filer:		Baxter Ward Banowsky.		
Attorney Docket Number:		1388-04		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	1	65	

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	2801	1	405	405
Total in USD (\$)				470

Electronic Acknowledgement Receipt	
EFS ID:	5133457
Application Number:	11622496
International Application Number:	
Confirmation Number:	3086
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	61400
Filer:	Baxter Ward Banowsky.
Filer Authorized By:	
Attorney Docket Number:	1388-04
Receipt Date:	10-APR-2009
Filing Date:	12-JAN-2007
Time Stamp:	11:52:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$470
RAM confirmation Number	6840
Deposit Account	503886
Authorized User	BANOWSKY,BAXTER W.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	rce.pdf	625825	no	3
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Warnings:					
Information:					
2		OA_01-06-09_rsp.pdf	78798	yes	7
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Claims		2	3	
	Applicant Arguments/Remarks Made in an Amendment		4	7	
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	32429	no	2
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Warnings:					
Information:					
Total Files Size (in bytes):			737052		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	5133457
Application Number:	11622496
International Application Number:	
Confirmation Number:	3086
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	61400
Filer:	Baxter Ward Banowsky.
Filer Authorized By:	
Attorney Docket Number:	1388-04
Receipt Date:	10-APR-2009
Filing Date:	12-JAN-2007
Time Stamp:	11:52:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$470
RAM confirmation Number	6840
Deposit Account	503886
Authorized User	BANOWSKY,BAXTER W.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	rce.pdf	625825	no	3
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Warnings:					
Information:					
2		OA_01-06-09_rsp.pdf	78798	yes	7
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Claims		2	3	
	Applicant Arguments/Remarks Made in an Amendment		4	7	
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	32429	no	2
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Warnings:					
Information:					
Total Files Size (in bytes):			737052		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/622,496		Filing Date 01/12/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
TOTAL			TOTAL							
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	04/10/2009	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	* 6	Minus	** 20	= 0	X \$26 =	0	OR	X \$ =		
Independent (37 CFR 1.16(h))	* 6	Minus	*** 8	= 0	X \$110 =	0	OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
TOTAL ADD'L FEE					TOTAL ADD'L FEE					
0					0					
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	04/10/2009	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
TOTAL ADD'L FEE					TOTAL ADD'L FEE					
0					0					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/Theresa Dawkins/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/622,496	01/12/2007	G.R. Mohan Rao	1388-04	3086
61400 7590 05/27/2009 BANOWSKY &LEVINE, P.C 12001 N. CENTRAL EXPRESSWAY SUITE 790 DALLAS, TX 75243			EXAMINER ARORA, AJAY	
			ART UNIT 2892	PAPER NUMBER
			MAIL DATE 05/27/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/622,496		Applicant(s) RAO, G.R. MOHAN	
	Examiner AJAY K. ARORA		Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 10 April 2009.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 3-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 3-8 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/10/2009 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Amended claim 5 recites "with at least one each of dopant

concentration of both donor and acceptor in both the well and channel regions”
(emphasis added), which does not comply with the written description requirement.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 3-8 are rejected under 35 U.S.C. 102(a) as being anticipated by Currie (US 6,831,292), hereinafter Currie.

Regarding claim 3, Currie (US 6,831,292) (refer to Figures 1-4 and in particular to Figure 2) teaches a semiconductor device, which may included VLSI (Col. 1, lines 24-27), with graded dopant concentration (Col. 5, lines 36-41 and Col. 6, lines 32-37) in the well regions and the active channel regions (Col. 7, lines 12-13) which can aid carrier movement away from the active surface regions, towards the substrate.

Regarding claim 4, Currie (refer to Figures 1-4 and in particular to Figure 2) teaches a semiconductor device , which may included VLSI (Col. 1, lines 24-27), with graded dopant concentration (Col. 5, lines 36-41 and Col. 6, lines 32-37) in the active channel

regions, the well regions and the substrate region (Col. 7, lines 12-13), which can aid carrier movement away from the active surface regions, deeper towards the substrate.

Regarding claim 5, Currie (refer to Figures 1-4 and in particular to Figure 2) teaches a semiconductor device , which may included VLSI (Col. 1, lines 24-27), with at least one each of dopant concentration (Col. 5, lines 36-41 and Col. 6, lines 32-37) of both donor and acceptor (Col. 6, lines 15-25) in both the well and channel regions (Col. 7, lines 12-13), to optimize the operating performance of the device.

Regarding claim 6, Currie (refer to Figures 1-4 and in particular to Figure 2) teaches a semiconductor device , which may included VLSI (Col. 1, lines 24-27), with at least one graded dopant concentration (Col. 5, lines 36-41 and Col. 6, lines 32-37) fabricated with ion implantation (Col. 6, lines 53-57), which can provide an aiding or retarding electric field locally in both well and channel regions, in a monolithic integrated circuit.

Even though a rejection is provided above, it is noted that claim 6 is a product claim but recites a method of steps therein, i.e. "fabricated with ion implantation". Therefore, claim 8 amounts to a product by process claim. *"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product*

was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

Regarding claim 7, Currie (refer to Figures 1-4 and in particular to Figure 2) teaches a semiconductor device , which may included VLSI (Col. 1, lines 24-27), with at least one graded dopant concentration (Col. 5, lines 36-41 and Col. 6, lines 32-37) in an epitaxial layer (Col. 5, lines 6-12) where the epitaxial layer (124 of Figures 1 and 2) forms the substratum for well and channel regions.

Regarding claim 8, Currie (refer to Figures 1-4 and in particular to Figure 2) teaches a semiconductor device , which may included VLSI (Col. 1, lines 24-27), where one layer consists of dopant gradients in both well and channel regions (Col. 5, lines 36-41 and Col. 6, lines 32-37).

Note that claim 8 is a product claim but recites a method of steps therein, i.e. "one layer of dopant from one wafer, is transferred to another wafer" and "wafer bonding or similar processes". Therefore, claim 8 amounts to a product by process claim. *"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even*

though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

Response to Arguments

6. Applicant's arguments with respect to claims 3-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./
Examiner, Art Unit 2892

/Chuong A Luu/
Primary Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 11/622,496		Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner AJAY K. ARORA		Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,831,292	12-2004	Currie et al.	257/19
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	05/24/2009								
	1	-								
	2	-								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								

Search Notes 	Application/Control No. 11622496	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN
	Examiner AJAY K ARORA	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
257	655	5/24/2009	AKA

SEARCH NOTES		
Search Notes	Date	Examiner
Refer to EAST search history report	5/24/2009	AKA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/A. K. A/ Examiner.Art Unit 2892	
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	551	(257/655).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/24 12:52
L8	2	("5029277").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/24 12:17
L7	2	("6831292").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/24 11:36
L4	4	("4001864").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/05/24 11:10
L3	4	L1 AND (well WITH carrier WITH (movement OR mobility) WITH ((away WITH active WITH surface) OR (towards WITH substrate)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/24 11:06
L2	62	L1 AND (((carrier OR electron OR hole) WITH (movement OR mobility)) SAME ((emitter WITH collector) OR (source WITH drain)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/24 11:05

L1	695	VLSI AND ((graded OR gradation OR gradient) WITH (dopant OR doping OR impurit \$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/05/24 11:04
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5/ 24/ 2009 1:01:49 PM**C:\ Documents and Settings\ aarora\ My Documents\ EAST\ Workspaces\ 11622496.wsp**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	§	
	§	
RAO, G.R. MOHAN	§	Confirmation No. 3086
	§	
Serial No. 11/622,496	§	Group Art Unit: 2892
	§	
Filed: 12 JANUARY 2007	§	Examiner: ARORA, AJAY
	§	
For: SEMICONDUCTOR DEVICES	§	
WITH GRADED DOPANT REGIONS	§	

**AMENDMENT AND RESPONSE
TO OFFICE ACTION MAILED MAY 27, 2009**

I. INTRODUCTORY COMMENTS:

The present paper is submitted as a complete response to the non-final Office Action mailed May 27, 2009, having a shortened statutory period of response of three months. Applicant does not believe that any extension of time or any additional fees are necessary for the consideration of the present paper. However, in the event that an extension of time or any additional fees are necessary for consideration of the present paper, I authorize the Commissioner to charge such fees, including fees for extension of time, to Deposit Account No. 50-3886.

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

II. AMENDMENTS TO THE CLAIMS:

The text of all claims under examination is submitted, and the status of each is identified.
This listing of claims replaces all prior versions and listings in the application.

Listing of Claims

Claims 1-2 (Cancelled)

3. (currently amended) ~~A VLSI digital semiconductor device with graded dopant concentration in the well regions and the active channel regions, to aid carrier movement away from the active surface regions, towards the substrate.~~

A VLSI Digital Semiconductor device comprising:

a surface region;

a substrate;

an active channel region capable of providing a localized drift electric field without the application of an external potential;

an isolation well region capable of providing a localized drift electric field without the application of an external potential; and

a graded dopant concentration in either the channel region or the well region to aid carrier movement away from the surface region towards the substrate.

4. (currently amended) ~~A VLSI digital semiconductor device with graded dopant concentration in the active channel regions, the well regions and the substrate region to aid carrier movement away from the active surface regions, deeper towards the substrate.~~

A VLSI Digital Semiconductor device comprising:

a surface region;

a substrate;

an active channel region capable of providing a localized drift electric field without the application of an external potential;

an isolation well region capable of providing a localized drift electric field without the application of an external potential; and

graded dopant concentrations in the substrate, the channel region and the well region to aid carrier movement away from the active surface region, towards the substrate.

5. (currently amended) ~~A VLSI digital semiconductor device with at least one each of dopant concentration of both donor and acceptor in both the well and channel regions, to optimize the operating performance of the device.~~

A VLSI Digital Semiconductor device comprising:

a surface region;

a substrate;

an active channel region capable of providing a localized drift electric field without the application of an external potential;

an isolation well region capable of providing a localized drift electric field without the application of an external potential; and

a graded dopant concentration of both donor and acceptor in both the channel region and the well region to optimize the operating performance of the device.

6. (currently amended) ~~A VLSI digital semiconductor device with at least one graded dopant concentration fabricated with ion implantation, to provide an aiding or retarding electric field locally, in both well and channel regions, in a monolithic integrated circuit.~~

A VLSI Digital Semiconductor device comprising:

a surface region;

a substrate;

an active channel region capable of providing a localized drift electric field without the application of an external potential;

an isolation well region capable of providing a localized drift electric field without the application of an external potential; and

a graded dopant concentration fabricated with ion implantation in both the channel region and the well region to provide an aiding or retarding electric field locally, in both the well region and the channel region, in a monolithic integrated circuit.

7. (currently amended) ~~A VLSI digital semiconductor device with at least one graded dopant concentration in an epitaxial layer where the epitaxial layer forms the substratum for well and channel regions.~~

A VLSI Digital Semiconductor device comprising:

a surface region;

a substrate;

an active channel region capable of providing a localized drift electric field without the application of an external potential;

an isolation well region capable of providing a localized drift electric field without the application of an external potential; and

wherein said substrate is an epitaxial layer comprising at least one graded dopant concentration.

8. (Cancelled)

9. (New) A VLSI Digital Semiconductor device comprising:

a surface region;

a substrate;

an active channel region capable of providing a localized drift electric field without the application of an external potential;

an isolation well region capable of providing a localized drift electric field without the application of an external potential; and

a graded dopant concentration in either the channel region or the well region to aid carrier movement toward the surface.

III. REMARKS:

Claims 3 through 7 are pending herein.

Claims 1, 2 and 8 have been cancelled without prejudice or disclaimer. Claims 3-7 have been amended, more particularly, to point out the claimed subject matter. Claim 9 is new. It is respectfully submitted that Claims 3-7 and 9 are in full compliance with the broad dictates of 35 U.S.C. § 112. Favorable consideration of Claims 3-7 and 9 is respectfully requested.

Claim 5 stands rejected under 35 U.S.C. § 112 as failing to comply with the written description requirement. Insofar as this reference may be applied against the claim 5 as currently amended, this rejection is respectfully traversed.

The limitation of claim 5, reciting “with at least one each of dopant concentration of both donor and receptor in both the well and channel regions” fully complies with the written description requirement. Paragraph 12 of the specification provides “in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer.”

Likewise, paragraph 4 and figures 3(a), (b), (c) and (d) of the specification describe the prior art, upon which the current invention improves. “FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3(b), 3(c), and 3(d) illustrate device cross sections, as practiced today.” Further, paragraph 8 of the specification provides that “FIGURES 3(a), 3(b), 3(c), 3(d) illustrate cross sections commonly used CMOS silicon substrate with two wells (one n-well in which p-channel transistors are subsequently fabricated, and, one p-well in which n-channel transistors are

subsequently fabricated) - typical IC, EEPROM using tunnel insulator, DRAM and NAND flash.” It is well known in the art that p-ch xstors are in n-well and vice versa in CMOS circuits. These references in the specification clearly show the concept of transistors in wells in connection with the prior art. The embodiments in the specification use the prior art described in paragraphs 4 and 8 and figures 3(a), (b), (c) and (d) and applies graded dopants to produce localized electric fields to improve performance. Accordingly, paragraph 10 of the specification describes Figures 5(a), (b) and (c) which depict how the invention would be applied to the prior art depicted in Figure 3, including the concept of transistors within wells.

It would have been clear to one skilled in the art that the invention described in the specification would be applicable to doped concentrations in both donor and receptor in both the well and channel regions.

Additionally, claims 3-7 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Currie (US 6,831,292). Insofar as this reference may be applied against the present claims, this rejection is respectfully traversed.

Each of claims 3-7 have been amended to clarify that the claimed invention relates to the field of VLSI digital semiconductor devices which include graded dopant concentrations in regions capable of providing a localized drift electric field without the application of an external potential. The Currie reference discloses a strained layer of Si, Ge or SiGe (Column 3, lines 46-58). The Currie reference does not teach a graded dopant concentration in a material capable of providing a localized drift electric field. Silicon and Germanium each have four valence

electrons. Accordingly, a strained SiGe layer, by its physical nature, is not capable of providing a localized electric field without the application of an external potential.

The amendment to claims 3-7 is supported by the description of the invention contained in the specification. Specifically, paragraph 11 of the specification contains a description of the invention including the range of doping concentrations . Additionally, this paragraph discloses that “[t]he relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT.”

Additionally, Figures 5(a), (b) and (c) clearly illustrate how the current invention differs from the prior art, such as Currie.

Accordingly, for the foregoing reasons, it is respectfully submitted that the cited reference does not disclose or suggest the claimed VLSI digital semiconductor device with graded dopant concentrations in regions capable of providing a localized drift electric field without the application of an external potential. The rejection of claims 3-7 under 35 U.S.C. §102(a) as anticipated by the cited reference should therefore be withdrawn. When read in light of the specification, Applicant submits that none of the foregoing amendments narrow the claims with regard to the claimed semiconductor device.

For all the foregoing reasons, it is respectfully submitted that claims 3-7 and 9 are in condition for allowance. Favorable reconsideration and allowance of claims 3-7 and 9 is respectfully requested.

Respectfully submitted,

Date: August 26, 2009

/Baxter W. Banowsky/
Baxter W. Banowsky
Registration No: 58,170

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Electronic Acknowledgement Receipt

EFS ID:	5958155
Application Number:	11622496
International Application Number:	
Confirmation Number:	3086
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	61400
Filer:	Baxter Ward Banowsky.
Filer Authorized By:	
Attorney Docket Number:	1388-04
Receipt Date:	26-AUG-2009
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