UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

GREENTHREAD, LLC Plaintiff, v. INTEL CORPORATION, DELL INC., AND DELL TECHNOLOGIES INC. Defendants.	))))))))))))	Case No. 6:22-cv-105-ADA

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS

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A	U.S. Patent No. 8.421,195
B	U.S. Patent No. 9,190,502
C	U.S. Patent No. 11,121,222
D	U.S. Patent No. 10,510,842
E	U.S. Patent No. 10,734,481
F	U.S. Patent No. 11,316,014
G	File History of U.S. Patent No. 8,421,195
H	U.S. Patent Application No. 13/854,319
I	U.S. Patent No. 4,160,985
J	U.S. Patent No. 4,684,971
K	U.S. Patent Application Publication No. 2003/0183856 A1.
L	U.S. Patent Application Publication No. 2003/0042511 A1.
M	U.S. Patent Application Publication No. 2007/0045682 A1
N	*Silicon Processing for the VLSI Era* (2000) Volumes 1-4
O	Petition for *Inter Partes Review* of United States Patent No. 8,421,195 Pursuant to 35 U.S.C. §§ 311-319, 37 C.F.R. § 42, *Samsung Electronics Co. Ltd., v. Greenthread LLC*, IPR2020-00289
P	Patent Owner Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. §42.107, *Samsung Electronics Co. Ltd., v. Greenthread LLC*, IPR2020-00289
Q	Declaration of Alexander D. Glew, *Samsung Electronics Co. Ltd., v. Greenthread LLC*, IPR2020-00289
R	*McGraw Hill Dictionary of Scientific and Technical Terms*, 6th Ed. (2003)
S	*Microchip Manufacturing*, S. Wolf, (2004)
T	*Semiconductor Devices, Physics and Technology*, S.M. Sze 2nd Ed., (2001)

U	*McGraw-Hill Dictionary of Electrical and Computer Engineering*, 6th Ed., (2003).
V	Declaration of Scott Thompson
W	U.S. Patent No. 8,106,481
X	U.S. Patent No. 6,633,066
Y	U.S. Patent No. 6,930,336
Z	Lin, W., *A Simple Method for Extracting Average Doping Concentration in the Polysilicon and Silicon Surface Layer near the Oxide in Polysilicon-Gate MOS Structures*
AA	Baker, R. J., CMOS Circuit Design, Layout, and Simulation, IEEE (1998)
BB	Chen, J. Y., CMOS Devices and Technology for VLSI, Prentice-Hall (1990)
CC	Webster's Third New International Dictionary of the English Language Unabridged, Merriam-Webster, Inc. (2002),
DD	Weste, N. H. E *et al.*, CMOS VLSI Design: A Circuits and Systems Perspective, Addison-Wesley (2011),
EE	Greenthread's Disclosure of Extrinsic Evidence
FF	U.S. Patent No. 5,536,962
GG	U.S. Patent Application No. 13/854,319
HH	File History of U.S. Patent No. 10,510,842, Office Action, dated July 17, 2018.
II	File History of U.S. Patent No. 10,510,842, Amendment, dated September 16, 2019
JJ	File History of U.S. Patent No. 10,510,842, Amendment, dated January 16, 2019
KK	File History of U.S. Patent No. 10,510,842, Notice of Allowance, dated November 5, 2019
LL	File History of U.S. Patent No. 11,121,222, Notice of Allowance, dated August 11, 2021

MM	File History of U.S. Patent No. 11,316,014, Notice of Allowance, dated August 11, 2021
NN	File History of U.S. Patent No. 10,734,481, Notice of Allowance, dated April 7, 2020
OO	File History of U.S. Patent No. 10,510,842, Office Action, dated August 11, 2021.
PP	File History of U.S. Patent No. 10,510,842, Application, dated May 9, 2017.
QQ	Wang, F., Single Event Upset: An Embedded Tutorial, 21 International Conference on VLSI Design, IEEE (2008)

I. INTRODUCTION

"The [patent] monopoly is a property right; and like any property right, its boundaries should be clear." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 730 (2002). As the Supreme Court has explained, "[t]his clarity is essential to promote progress, because it enables efficient investment in innovation." *Id.* at 730-31. "For this reason, the patent laws require inventors to describe their work in 'full, clear, concise, and exact terms.'" *Id.* (citing 35 U.S.C. § 112). Yet several terms of the Asserted Patents fail to meet this standard, leaving Defendants guessing as to the scope of the claims, and prejudicing Defendants' ability to defend against Greenthread's assertions. The claims that contain these terms are invalid as indefinite.

Even where terms are not so vague as to be indefinite, Greenthread's request that they be given, simply, "plain meaning" is not sufficient. Although certain terms are used according to their ordinary meaning to a person of ordinary skill in the art ("POSITA"), the jurors will almost certainly not be POSITAs, and construction is necessary to ensure that Greenthread is limited to that meaning. Moreover, for other terms the prosecution history—including amendments to overcome prior art and statements to avoid IPR institution—makes clear the meaning intended, and Greenthread should not be permitted to recapture through "plain meaning" a scope it disclaimed to receive and keep its patents.

II. THE ASSERTED PATENTS

Greenthread asserts six patents in this case, all of which share a common, three-column specification.[1] The Asserted Patents describe basic semiconductor devices, such as CMOS transistors, which include conventional structures found in engineering textbooks. The

[1] Greenthread asserts U.S. Patents Nos. 8,421,195 ("the '195 Patent"); 9,190,502 ("the '502 Patent"); 10,510,842 ("the '842 Patent"); 10,734,481 ("the '481 Patent"); 11,121,222 ("the '222 Patent"); and 11,316,014 ("the '014 Patent") (collectively, "the Asserted Patents").

specification states that the claimed devices differ from a conventional device in their use of specific "graded dopant concentrations." Semiconductor devices carry electric charges using either electrons or holes, which together are referred to as charge carriers. *See, e.g.*, Ex. A, '195 Patent at 1:26-27; Ex. V, ¶ 10. Doping is the process of introducing impurities into a semiconductor material, such as silicon, to add surplus carriers. Ex. V, ¶ 11. The relative amount of added dopant is called the dopant concentration. *Id*. The Asserted Patents acknowledge that graded dopant concentrations—where concentration varies at different locations inside the device—were previously known in the art. *See* Ex. A, '195 Patent at 2:13-15. Despite that, the patents purport to claim that specific graded dopant concentrations will "sweep" certain carriers through the device, ostensibly improving performance. *See id*. at 3:30-40, Abstract, 1:32-36. In the claims of the '195 and '502 Patents, the graded dopant concentrations that "aid the movement of minority carriers" are found in a "drift layer" and in a "well region" that is disposed in the drift layer. In the '842, '481, '222, and '014 Patents, the claims require that an "active region" (and for certain patents, additionally a "well region") have a "graded dopant concentration to aid carrier movement."

III. LEGAL STANDARD

35 U.S.C. § 112 ¶ 2 requires that "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the [applicant] regards as his invention." Ordinarily, claim terms are "given their ordinary and customary meaning" as understood by a POSITA unless the patentee has chosen a specific meaning or disclaimed its full scope. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*).

Critically, however, § 112 ¶ 2 demands that patent claims, when read in light of the specification and prosecution history, must inform, "with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). That is, "a patent must be precise enough to afford clear notice of what is claimed, thereby

'apprising the public of what is still open to them,'" and avoiding "a zone of uncertainty which enterprise and experimentation may enter only at the risk of infringement claims." *Id.* at 899. The Supreme Court has noted that patentees benefit from this uncertainty, "fac[ing] powerful incentives to inject ambiguity into their claims," such that it is the responsibility of the patent drafter "to resolve the ambiguity." *Id.* Where a defendant shows by clear and convincing evidence that this ambiguity is not resolved, the patent is invalid for indefiniteness. *Id.* at 912 n. 10.

IV. DISPUTED CLAIM TERMS

A. "surface layer" and related terms

Claim Term	Defendants	Greenthread
"surface layer" / "an active region . . . disposed on one surface of said surface layer" / "a single drift layer disposed between the other surface of said surface layer and [said/the] substrate"	Indefinite	Plain Meaning

Claim 1 of the '195 Patent, Claim 7 of the '502 Patent, and Claim 44 of the '222 Patent each requires a "surface layer," but without anything in the intrinsic evidence to describe what a "surface layer" means—and without any commonly understood meaning to one skilled in the art—the term is indefinite and renders these claims invalid. Not only does the term "surface layer" not appear anywhere in the specification, the specification also does not contain a single example of what would constitute a "surface layer," and no embodiment describes a layer that could plausibly be the claimed "surface layer."[2] Furthermore, "surface layer" is not a term of art having a commonly accepted definition, as discussed below.

[2] Defendants are concurrently filing a Motion for Summary Judgment of Invalidity for Lack of Written Description on this issue.

While the words "surface" and "layer" are generally known and each have an understandable meaning on their own, the dispute is not what "surface layer" might mean in isolation, but rather, its meaning in the context of the entirety of each claim. Here, the term must be considered in the context of its spatial relationship with other recited structural elements. *See Infinity Computer Prod., Inc. v. Oki Data Americas, Inc.*, 987 F.3d 1053, 1062 (Fed. Cir. 2021), *cert. denied*, 142 S. Ct. 585 (2021) ("We recognize that, in a vacuum, it might seem odd to hold 'computer' indefinite. . . . Yet the indefiniteness here does not reside in the term 'passive link' or 'computer' on its own but rather in the relationship between the two in the context of these claims."). The unambiguous claim language requires a "surface layer" with two "surfaces," an "active region" that is "disposed ***on one surface***" of the claimed "surface layer," and a "single drift layer" that is "disposed between the ***other surface***" of the surface layer and a "substrate." A separate "well region" is "disposed ***in***" the "single drift layer." Claim 1 of the '195 Patent, excerpted below, is representative:

1. A CMOS Semiconductor device comprising:

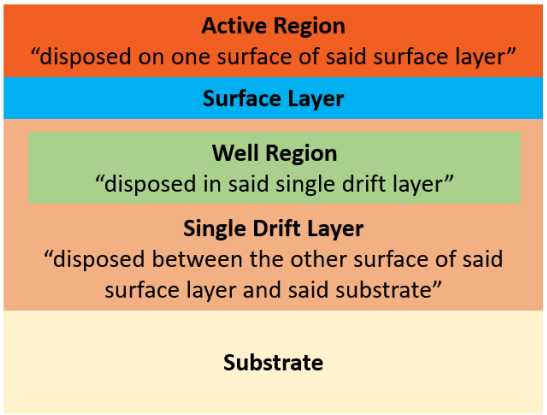
a surface layer;

a substrate;

an active region including a source and a drain, ***disposed on one surface of said surface layer;***

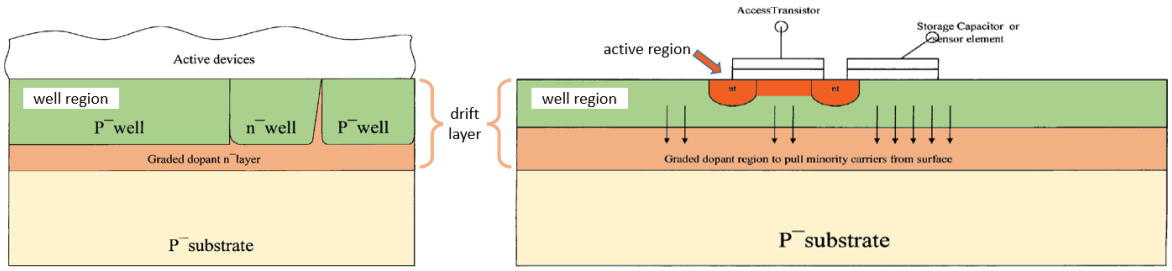
a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending ***between said surface layer and said substrate***; ...

at least one ***well region disposed in said single drift layer,*** said well region having a graded concentration of dopants ....



Ex. A, '195 Patent at Claim 1; *see also* Ex. V, ¶¶ 13-17. Accordingly, "surface layer" is the cornerstone of the claims, as the other elements are defined by their placement relative to the "surface layer."

No "surface layer" is disclosed in the specification. When faced with an ambiguous claim, a skilled artisan would turn to the specification for guidance, but the intrinsic evidence here injects nothing but uncertainty since the specification does not disclose any layer, of any kind, that satisfies the claimed spatial relationship of such layer to an "active region" and "single drift layer." The Asserted Patents' scant three-column specification is devoid of any suggestion of a "surface layer," nor anything that could plausibly constitute such a layer, either in the text or the figures. Ex. V, ¶¶ 24-34. In the relevant CMOS embodiments, illustrated in Figures 5(a) and 5(b) shown below, the active region directly abuts the single drift layer (which, as per the claim, includes the well region disposed within it) without any intervening layer.



Ex. V, ¶¶ 32-33 (citing '195 Patent at Figs. 5(a)-(b) (annotated and coloring added, including to show the channel in the active region between the source and drain)). The specification confirms that these figures "illustrate the cross sections of a MOS silicon substrate with two wells, and, ***an*** [*i.e.*, singular] underlying layer." Ex. A, '195 Patent at 2:27-29. And although the specification refers to a "surface" in several instances and discloses layers such an "underlying layer," a POSITA

would not understand any of these references to disclose a "surface layer" exhibiting the spatial relationships of the claims. Ex. V, ¶ 34.[3]

"Surface layer" has no plain meaning as used in the claims. Greenthread urges that "surface layer" be given its "plain meaning." But the term does not have any commonly accepted meaning to those of skill in the art. Ex. V, ¶¶ 37-38. Although "surface layer" may sometimes appear in the prior art, it is used as a nonce word that has varied meanings, which are defined by the context in which it is used. *Id.*, ¶ 37. Semiconductor devices are complex and consist of many "layers." *Id.*, ¶ 38. A POSITA could use "surface layer"—depending on context—to describe a gate oxide layer, a field oxide layer, the source and drains, mask layers, or any number of other layers that could be placed at a surface of the semiconductor device—none of which meet the spatial requirements of the claims because they are either above or within the active region. *Id.*, ¶¶ 38-44 (explaining exemplary prior art[4]). For example, *Silicon Processing for the VLSI Era* (2000) ("Wolf"), a widely used textbook, uses "surface layer" to refer to various distinct layers deposited on the top of the semiconductor wafer, such as a silicon oxide layer. *Id.*, ¶ 39 (*citing* Ex. N1 at 373 ("Ion implantation can inject dopant atoms into a semiconductor by implantation through a thin surface layer (*e.g.*, SiO_2)"), 385 ("ion implantation is frequently performed through a thin surface layer (e.g., SiO2, Si3N4, or even a composite layer)"), 419-20 (describing implanting dopants through a mask or gate oxide layer on the silicon wafer surface)). But Wolf also uses "surface

[3] Nothing in the prosecution history sheds any additional light on this term. "Surface layer" was introduced into the claims nearly six years after the initial patent application was filed. Ex. G at 164. Greenthread did not identify to the USPTO any "surface layer" in any embodiment described in the specification, nor did it describe any such layer at any point in prosecution. Ex. V, ¶¶ 35-36.

[4] *E.g.*, Ex. V, ¶43 (discussing Ex. Z at 1; Ex. Y at 10:61-61 ("an ordinary surface layer such as a CMOS source/drain"); Ex. X at 3:14-16 ("an oxide surface layer thereon"); Ex. FF at 3:55-61 ("channel surface layer").")).

layer" in an entirely different context to refer to source, drains, and doping in the channel, which is part of the active region and below the silicon oxide layer discussed above. Ex. V, ¶ 40-41 (citing Ex. N1 at 358, 427-28; Ex. N3 at 291-295, 307; Ex. N4 at 192, 195). Thus, Wolf confirms that while "surface layer" may occasionally be used as shorthand, it has no generally accepted meaning in the field. Importantly, the claims' usage of "surface layer" is inconsistent with Wolf's examples of what a "surface layer" could be because none of the "surface layers" described in Wolf would satisfy the required spatial limitations of the claims since each is either above the active region or within the active region itself. Ex. V, ¶ 42. Consequently, Greenthread cannot rely on Wolf to provide context for the phrase "surface layer" as that term is used in the Asserted Patents. Here, the specification provides no relevant context thus rendering the term indefinite as used in the claims. *Media Rts Techs., Inc. v. Cap. One Fin. Corp.*, 800 F.3d 1366, 1371 (Fed. Cir. 2015) ("[A] claim is indefinite if its language might mean several different things and no informed and confident choice is available among the contending definitions.") (internal quotations marks omitted).

"Surface layer" cannot mean "layer at the surface" in the context of the other limitations of the claims. To the extent that Greenthread's "plain meaning" of "surface layer" amounts to nothing more than a "layer at the surface of the semiconductor device," as suggested by the extrinsic evidence it has provided,[5] such a generic meaning is incompatible with the requirements of the claim language and, indeed, underscores why this term is indefinite. Such a meaning is inconsistent with the claim language that paradoxically requires the ***"surface*** layer" to be disposed ***under*** the active region—sandwiched between the active region and the substrate—rather than at the surface of the semiconductor device. Where the claims themselves reveal

[5] *See* Ex. BB at 154, 234-239, 242, 266; Ex. CC at 209, 654, 1281, 1912, 2300.

contradictory positions as to the meaning of a claim term, as is the case here, the term is indefinite. *TVnGO Ltd. (BVI) v. LG Elecs. Inc.*, 861 F. App'x 453, 457-460 (Fed. Cir. 2021) (holding related dependent and independent claims invalid for indefiniteness where they dictated contradictory meanings for a phrase, which necessarily "create[ed] confusion as to which reading is correct").

In short, "surface layer" has no discernable structure, location, dimensions, composition, or boundaries. Ex. V, ¶¶ 45-46. Yet it is the cornerstone of the claims used to define the location of all other elements. Without knowing what the "surface layer" is or what its location or boundaries are, a POSITA would not be reasonably certain where to deposit the claimed graded concentrations of dopants—the alleged novel feature—to practice the claims. The specification provides no guidance as to what differentiates a single drift layer from a surface layer—in terms of structure or composition. *Id*. Accordingly, a POSITA would be left to speculate whether a particular graded concentration of dopants is within a single drift layer or well region (as claimed) or whether it is within a surface layer (which is outside the scope of the claims). *Id*. The asserted claims of the '195 and '502 Patents and Claim 44 of the '222 Patent are therefore indefinite. *Nautilus*, 572 U.S. at 909 (A claim "must be precise enough to afford clear notice of what is claimed, thereby 'appris[ing] the public of what is still open to them.'").

B. "substrate"

Claim Term	Defendants	Greenthread
"substrate"	"the initial material within which or on which the semiconductor device is fabricated"	Plain Meaning

Each of the asserted claims is directed to a semiconductor device having a "substrate." While Greenthread proposes this term should be given its "plain and ordinary meaning," it has not

stated what that meaning is. Instead, Greenthread merely takes issue with the use of the term "initial" in Defendants' construction, without providing a competing construction.[6]

Whether the claimed "substrate" is directed to the "initial" material is a dispute concerning the scope of the claims that the Court must decide. *O2 Micro Int'l. Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008). Defendants' proposed construction is supported by the intrinsic evidence and consistent with the extrinsic evidence. In contrast, a construction that omits "initial" (as Greenthread implicitly proposes) could broaden this term to read on essentially any portion of a semiconductor device—including regions, wells, layers, or other structures formed while a device is being fabricated—which are not understood by a POSITA to be a "substrate." Such a construction would be improper for several reasons.

First, the claims themselves distinguish the "substrate" from other structures that are subsequently formed in a substrate, such as an "active region," "well region," "drift layer," or "surface layer."[7] Because the claims use "different terms" to describe these subsequent structures, it is "presume[d] that those . . . terms have different meanings" than "substrate." *See SIPCO, LLC v. Emerson Elec. Co.*, 794 F. App'x 946, 949 (Fed. Cir. 2019).

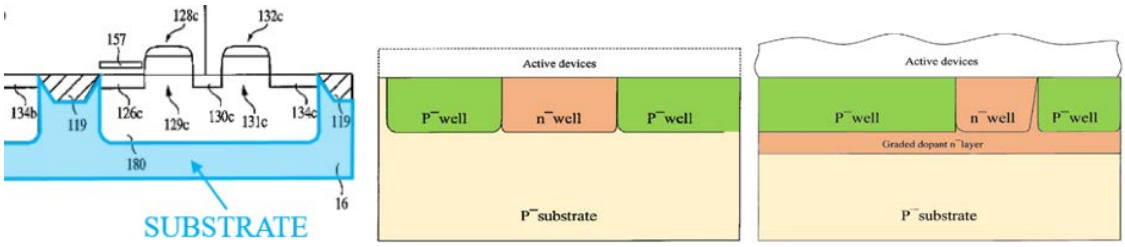
Second, the specification confirms that the claimed substrate is the initial material providing the mechanical support "on which . . . devices are ***subsequently fabricated***." Ex. A, '195 Patent at 1:61-63. This characteristic distinguishes a substrate from the other structures (such as

[6] *See, e.g.*, Ex. EE at 8-9.

[7] Ex. A, '195 Patent, Cl. 1, Ex. B, '502 Patent, Cl. 7, Ex. D, '842 Patent, Cls. 1, 9; Ex. E, '481 Patent, Cls. 1, 20; Ex. C, '222 Patent, Cls. 1, 21, 39, 41-42, 44; Ex. F, '014 Patent, Cls. 1, 21.

wells, layers, or transistors) of a device.[8] The initial substrate can be "a uniformly doped 'bulk' silicon substrate (as is commonly known in the semiconductor industry)."[9] Or it can be an "epitaxial substrate" combining "'bulk' silicon" with a layer of "epitaxial silicon."[10] But it cannot be some other region, well, layer, transistor, or other structure formed later in the fabrication process. That is, the substrate is the foundation—the initial structure—on which devices are subsequently built.

Lastly, Greenthread itself has previously confirmed that a "substrate" consists only of the initial material on which the semiconductor device is fabricated. In a prior IPR, both Greenthread and its expert witness identified ***just the initial material***, and not any regions, wells, layers, or other structures that are later fabricated on or in that material, as the claimed "substrate":



See Ex. P at 29, 46-47 ("semiconductor substrate 16" in blue; "P⁻substrate" in yellow; Ex. Q, ¶¶ 40.[11]

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[8] Ex. R at INTEL_GREENTHREAD00015553 (defining "substrate" as comprising the "physical material on which a microcircuit is fabricated").

[9] Ex. W, U.S. Patent No. 8,106,481 at 2:58-60. U.S. Patent No. 8,106,481 is relevant intrinsic evidence because it names the same inventor and claims priority to the same parent application.

[10] *See, e.g.*, *id*. at 2:58-63; Ex. E, '481 Patent, Cls. 3; Ex. C, '222 Patent, Cls. 3, 24; Ex. F, '014 Patent, Cls. 3, 24.

[11] *See also Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1362 (Fed. Cir. 2017) ("[s]tatements made by a patent owner during an IPR . . . can be considered for claim construction.").

Conversely, the intrinsic evidence does not describe a region, well, layer, or other structure formed later in the fabrication process as a "substrate."[12] A construction of "substrate" that permits this term to arbitrarily read on such structures would effectively read the term out of the claims. *See SIPCO*, 794 F. App'x at 949.

C. "active region"

Claim Term	Defendants	Greenthread
"active region"	"region that forms the current path of a device"	Plain Meaning

All asserted claims use the term "active region." The parties agree that this term should be afforded its ordinary meaning but dispute whether the term requires construction. A POSITA at the time of the alleged invention would have understood that the active region of a semiconductor device is the region in which current flows when that device is active, or "turned on"—*i.e.*, the region that forms the current path of a device. The claims distinguish this region from other claimed regions such as "well region." Greenthread's unspecified "plain meaning" construction fails to delineate for the jury the active region from these other claimed regions and fails to resolve the parties' dispute concerning the scope of the term. *See O2 Micro*, 521 F.3d at 1361.

The claims of the '195 and '502 Patents (and Claim 44 of the '222 Patent) require "***an active region including a source and a drain*** . . .," as well as a "single drift layer" and a "well region," both of which must contain "a graded concentration of dopants." Ex. A, '195 Patent at 4:14-29; Ex. B, '502 Patent at 4:55-67; Ex C, '222 Patent at 8:24-40. The remaining claims require first and second "***active region[s]*** . . . within which transistors can be formed" where at least one

[12] For example, the specification describes the "substrate" as being separate from the "active devices"/"transistors," "well region"/"well," and other "regions" or "layers" comprising the fabricated device. Ex. A, '195 Patent at 1:50-51, 1:61-63, 2:16-22, 3:30-43, Figs. 2-5.

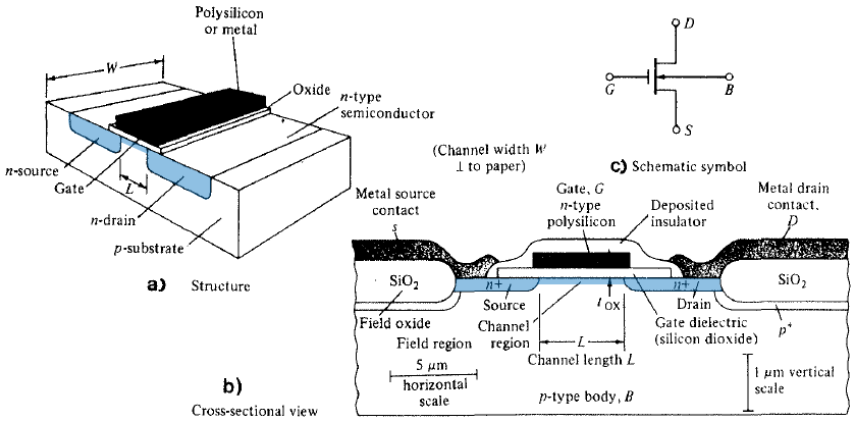
of the active regions contains a graded dopant concentration. Ex. A, ’842 Patent at 4:48-60; Ex. E, ’481 Patent at 4:53-5:3; Ex C, ’222 Patent at 4:42-62; Ex. F, ’014 Patent at 4:54-5:7. Many of these claims also require a “well region” that contains another graded dopant concentration. *Id*. The specification also uses the term “active region,” which it distinguishes from an “isolation” region. *See, e.g.*, Ex. A, ’195 Patent at Abstract; Ex. V, ¶ 55.

During prosecution, Greenthread repeatedly used the term “active region” to describe the region that forms the current path of a device, such as “from emitter to collector” (referencing the current path in a BJT) and “from source to drain” (referencing the current path in a CMOS transistor). Ex. G at 8; *Id.* at 123 (claiming an “active channel region”); Ex. H at 149 (“active region with a channel conduction surface”). Greenthread consistently distinguished this active region from isolation regions that do not form a current path, such as the “isolation well region.” Ex. G at 123 (claiming “an active channel region” separately from “an isolation well region”); Ex. H at 156; Ex. V, ¶ 56.

Greenthread’s use of the term “active region” in the intrinsic record is consistent with its well-known and accepted meaning to a POSITA at the time of the alleged invention: a region that forms the current path of a semiconductor device. *See* Ex. N2 at 299; Ex. S at INTEL_GREENTHREAD 00015584; Ex. V, ¶¶ 49-56. For example, in a CMOS transistor, the current path of that transistor is the source, drain, and channel of the device. *Id*. The device is ON (*i.e.*, active) when current flows from the source to the drain through the channel, and OFF (*i.e.*, non-active) when current does not flow in that region. *Id.*; *see also* Ex. N2 at 454-58 (defining the active state of a bipolar device in relation to current flowing in the device). These regions where current flows are thus known as “*active* or *transistor* regions.” Ex. N2 at 299 (emphasis in

original). The asserted claims use the term the same way: the ’195 and ’502 claims, limited to CMOS, recite that the active region includes “***a source and a drain.***”

A leading textbook defines the term similarly: “[t]he ***active regions are those in which transistor action occurs***; ***i.e., the channel and the heavily doped source and drain regions***.” Ex. N2 at 299; *see* Ex. N4 at 197 (“[T]he device-region in which transistor-action occurs is the ***channel under the gate***. ***The current*** coming from the metal-interconnect lines ***must flow*** . . . ***through the source or drain regions*** (Fig. 5-13).”); Ex. S at INTEL_GREENTHREAD00015595 (Fig. 4-7) (defining “active region” as the source and drain (“S/D”), and “V_T”, the minimum voltage required to make the device active, i.e., to create a conducting path in the channel), INTEL_GREENTHREAD00015601-02; Ex. U at INTEL_GREENTHREAD00015764 (defining “active region” as the “region in which amplifying, rectifying, light emitting, or other dynamic action occurs in a semiconductor device”); Ex. V, ¶¶ 50-52. A CMOS active region is shown highlighted in blue below:



Ex. N2 at 299 (Fig. 5-1); *see also id*. at 300 (Fig. 5-2(a)); Ex. N1 at 818-21 (contrasting isolation (i.e. field) regions and active regions); Ex. T at INTEL_GREENTHREAD00015737 (depicting “[a]ctive device area”), 37 (depicting channel with dashed lines between source and drain). The

specification depicts similar device structures. *See, e.g.*, Ex. A, '195 Patent at Fig. 5(b) (depicting CMOS device with source, drain, and channel).

Moreover, consistent with the intrinsic record, a POSITA would understand that the "active region" where the current path exists is distinct from non-active regions, such as wells. Ex. S at INTEL_GREENTHREAD00015595 (Fig. 4-7) (depicting and defining the "active region," including the source and drain ("S/D") and channel ("V_T"), as distinct from the surrounding wells); Ex. V, ¶¶ 55-56; *see also* Ex. H at 156 (applicant explaining that "the n-well shown in [Figure 5(a) of the specification] corresponds to the claimed 'isolation region' because the purpose of this well is to isolate [the active region of each transistor]").

Greenthread's own extrinsic evidence belies its attempt to conflate "active region" with "well region." For example, the textbook *CMOS Circuit Design, Layout, and Simulation* identifies "source and drain areas" of a CMOS transistor as the "active areas." Ex. AA at GREENTHREAD-WDTX-002709. As another example, the textbook *CMOS Devices and Technology for VLSI* confirms that a "conducting channel," *i.e.*, a channel in which current flows, "is allowed to form only in the active area" (Ex. BB at GREENTHREAD-WDTX-002734), and distinguishes the active areas in which current flows from the non-active areas such as wells. *Id.* at -2726.

D. "unidirectional electric drift field" terms

Claim Term	Defendants	Greenthread
"said [drift layer further/well region . . .] having a [first/second] static unidirectional electric drift field"	"said [drift layer further/well region . . .] having a [first/second] static electric drift field that is unidirectional over the [drift layer/well region]"	Plain Meaning
"said [drift layer/well region] having a graded concentration of dopants generating a [first/second] static	"said [drift layer/well region] having a graded concentration of dopants generating a [first/second] static electric	Plain Meaning

unidirectional electric drift field"	drift field that is unidirectional over the [drift layer/well region]"	

The parties dispute whether "static unidirectional electric drift field" appearing in Claim 1 of the '195 Patent, Claim 7 of the '502 Patent, and Claim 44 of the '222 Patent merely requires a unidirectional field occurring at any portion of the recited drift layer or well region or whether the field must be unidirectional over the entire layer or region. During prosecution, Greenthread disclaimed any interpretation that would permit multiple fields of opposite directions to be present in different portions. Indeed, Greenthread introduced the "unidirectional" limitation to overcome art disclosing a layer having two fields of opposite directions, emphasizing that this amendment required unidirectionality over the whole layer. Greenthread should be held to that here.

The intrinsic evidence fully supports Defendants' proposed construction. The claim language itself implies a single unidirectional field across the entire layer or region. For example, Claim 1 of the '195 Patent defines the "single drift layer" as being disposed between "***the other surface of said surface layer and said substrate***" and as having a "static unidirectional electric drift field to aid the movement of minority carriers" over the area defined as the drift layer, namely "***from said surface layer to the substrate***." Ex. A, '195 Patent, Cl. 1. The claim also requires a "well region disposed in said single drift layer" that similarly has another "static unidirectional electric drift field to aid the movement of minority carriers ***from said surface layer to said substrate***." *Id*. Claim 7 of the '502 Patent has similar limitations. Ex. B, '502 Patent, Cl. 7.

Consistent with this claim language, the specification discloses the use of a graded concentration of dopants to create a single unidirectional electric field that moves minority carriers over the region of grading. *See, e.g.*, Ex. A, '195 Patent at 1:34-36, 2:13-15, 2:35-47, 3:30-35, FIGS. 1, 5(a), 5(b), 5(c). The disclosure alleges that the relative slope of a dopant gradient creates

a "drift electric field" over the region of the gradient to move minority carriers over that region in the direction of the gradient. Ex. A, '195 Patent at 2:40-45; *see also, id.* at FIG. 1. The alleged invention employs such a "graded dopant concentration" in a layer or region to create a "drift field" to "sweep . . . minority carriers" from "active circuitry at the surface . . . deep into the substrate." Ex. A, '195 Patent at 3:30-35; *see also id*. at FIGS. 5(a), 5(b). This drift field is a single unidirectional field: the specification has no disclosure of a layer or region possessing multiple fields of different directions in different portions of a layer or region.

The prosecution history reveals that Greenthread disclaimed any field other than one that is unidirectional over the layer or region. Pending claim 10 (now Claim 1) recited a "drift layer having a graded concentration of dopants . . . to create a drift field drawing minority carriers from said surface layer to said substrate." Ex. G at 164. The Examiner rejected this claim over Kamins. Ex. G at 182; Ex. G at 221-22. Kamins discloses an "N+ Buried Layer" (annotated in green below in Kamins' Figure 2) that employs a bidirectional graded concentration (annotated in green below in Kamins' Figure 3) that creates two electric fields (annotated in yellow) with opposing directions. Ex. I at 2:32-35, 2:64-3:18, FIGS. 2-3.

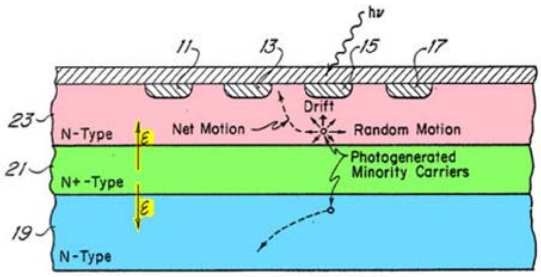


Figure 2

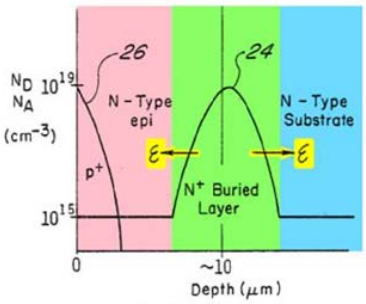


Figure 3

Kamins states that the two electric fields of the "N+ Buried Layer" move carriers both towards the surface and towards the substrate. *Id*. at 2:64-3:18.

To overcome Kamins, Greenthread amended pending claim 10 to require a "***unidirectional***

drift layer." Ex. G at 234. Greenthread noted that Kamins's "N+ Buried Layer" incorporates a bidirectional graded dopant concentration that creates ***two*** fields of "opposing directions": one that accelerated carriers to the surface and another that accelerated carriers to the substrate. *Id*. at 237. Greenthread distinguished Kamins on the basis that the field of the claimed drift layer was "***unidirectional***" permitting carriers to move in only one direction:

> The amendments to claim 10 further clarify that Applicant's claimed "drift layer" is a single ***unidirectional*** layer with a graded dopant concentration which ***draws all minority carriers away from the surface layer to the substrate - none of the carriers is drawn from the substrate to the surface layer***.

Id. And Greenthread emphasized that the drift field of the alleged invention was "unidirectional" over the entire drift layer, i.e., from the "surface layer" to the "substrate." G at 254-55. ("In other words, the drift field for the holes (minority carriers) ***is unidirectional, i.e., from the emitter (surface layer) to the collector (substrate)*** . . . ***moving all minority carriers in the same direction because of the unidirectional drift*** . . ."). Greenthread subsequently amended the claims to require that both the drift layer and a well region have a "static unidirectional electric drift field," while repeatedly arguing that Kamins "does not teach that the electric drift field is a 'unidirectional electric drift field.'" Ex. G at 286, 290; Ex. G, at 330, 333.

Greenthread benefited from amending its claims to distinguish the prior art to secure allowance, so Greenthread should now be held to its disclaimer. *See SpeedTrack, Inc. v. Amazon.com*, 998 F.3d 1373, 1379 (Fed. Cir. 2021) ("Prosecution disclaimer can arise from both claim amendments and arguments."). Greenthread, however, apparently contends that these claim terms could be satisfied by a unidirectional field that exists in only a portion of a drift layer or well region, even if a field of opposite direction existed in another portion. That interpretation, however, is precisely what Greenthread disclaimed during prosecution. *See id*. at 1379-80. Moreover, that interpretation would be tantamount to striking the word "unidirectional" from the allowed claims,

thereby permitting Greenthread to recapture the very subject matter it surrendered at the USPTO. *See Aylus Networks*, 856 F.3d at 1360 ("Ultimately, the doctrine of prosecution disclaimer ensures that claims are not 'construed one way in order to obtain their allowance and in a different way against accused infringers.'").

E. "to aid the movement of minority carriers from … to …" / "to aid carrier movement from … [to/towards] …"

Claim Term	Defendants	Greenthread
"to aid the movement of minority carriers from … to …"	Indefinite. Alternative construction: "to sweep the minority carriers from … to …"	Plain Meaning
"to aid carrier movement from … [to/towards] …"	Indefinite. Alternative construction: "to sweep the carriers from … [to/towards] …"	Plain Meaning

All asserted claims require regions in a semiconductor device to have a graded dopant concentration "to aid carrier movement" or "to aid the movement of minority carriers" from one location of the device to another. For example, Claim 1 of the '481 Patent claims "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration ***to aid carrier movement from*** the first surface ***to*** the second surface of the substrate" and "at least one well region…having at least one graded dopant region…***to aid carrier movement from*** the first surface ***to*** the second surface of the substrate." Ex. E, '481 Patent, Cl. 1. Claim 7 of the '502 Patent likewise claims "a single drift layer … having a graded concentration of dopants generating a first static unidirectional electric drift field ***to aid the movement of minority carriers from*** said surface layer ***to*** said substrate" and "at least one well region . . . having a graded concentration of dopants generating a second static unidirectional electric drift field **to** ***aid the movement of minority carriers from*** said surface layer ***to*** said substrate." Ex. B, '502 Patent, Cl. 7. The claims, however, do not articulate any particular graded dopant concentration and do not delineate what

constitutes sufficient "aiding." The intrinsic record does not "provide objective boundaries for those of skill in the art," thus leaving a POSITA wondering what graded concentrations and what "aiding" effects are within the scope of the claims and what are without. *See Interval Licensing LLC v. AOL, Inc.* 766 F.3d 1364, 1371 (Fed. Cir. 2014). Because the scope of the claims entirely depends "on the unpredictable vagaries of any one person's opinion," these phrases are indefinite and render all asserted claims invalid. *Id.*, 1374.

The "aid carrier movement" claim terms are subjective. Each "aid carrier movement" claim term is "highly subjective and, on its face, provides little guidance to one of skill in the art." *Interval Licensing,* 766 F.3d 1371 (finding "unobtrusive manner" indefinite); *Perfectvision Mftg., Inc v PPC Broadband, Inc*., No. 4:12CV00623 JLH, 2014 WL 4285786 (E.D. Ark. Aug. 29, 2014), at *22 (finding "***to help*** prevent a gap …" indefinite because "***introducing the clause with the term 'to help' makes the phraseology so subjective*** so that a person of ordinary skill in the art cannot discern with reasonable certainty the scope of the claim."). Carriers (or charge carriers) are holes or electrons, and an astronomically large number of carriers can exist in any semiconductor device.[13] Ex. V, ¶ 59. There is *always* movement of carriers in devices in operation; indeed, it is the movement of charge carriers that forms the electrical currents in active devices. Ex. A, '195 Patent at 1:23-27 ("both carriers (electrons and holes) play a role in the switching performance of BJTs."), *id.* at 1:43-4 ("MOS devices are majority carrier devices for conduction."). In particular, the CMOS transistors at issue in this litigation are called *field*-effect transistors (FETs) because the application of an input voltage to the gate electrode of a CMOS transistor sets up an *electric field* that controls the current flow (flow of charge carriers) through the channel region of the transistor. Ex. N2 at 299; *see also* Section IV.C (active region); Ex. V, ¶ 60. Such operational

[13] Minority carriers are charge carriers that are in the minority in a particular region. Ex. V, ¶ 12.

electric fields are unrelated to and dwarf any electric field allegedly due to graded dopant concentration. *Id.* In fact, carrier movement in CMOS devices is largely impacted by operational conditions and device characteristics unrelated to any graded dopant concentration, such as the voltage settings in the device, the operating temperature, the placement of ground paths, the location of p-n junctions, the distances separating device structures and the isolation regions. *Id.*, ¶¶ 59-62 Carriers can also be randomly generated due to external events (*e.g.*, in so-called single event upset or SEU). *Id.* Such an event generates millions of charge carriers that streak in all directions, including towards the substrate. *Id.*

Against this backdrop, the claims provide no objective indication of what constitutes sufficient "aiding" of carrier movement other than linking the claimed "aiding" to the presence of some unspecified graded dopant concentration. *Id.*, ¶ 63. Notably, the claims do not recite any numerical range of doping, any particular doping profile, or any specific, well-defined, result that could provide some measure of objective boundaries. A POSITA is thus left wondering whether the claims require that a graded dopant concentration (and any resulting electric field) be the sole source of the claimed carrier movement, be at least the dominant contributor to such movement, be only a contributing factor (however slight) to such movement, or simply not impede such movement (however defined). *Id.*, ¶ 64. A POSITA is further left wondering whether the claims require moving all carriers (or minority carriers) present in certain regions of the device to be swept down into the substrate, or moving only those "unwanted minority carriers" (however defined) to be swept into the substrate (*see, e.g.*, Ex. A, '195 Patent at 3:30-35).

In sum, the claims do not specify any particular "graded" dopant concentration that produces the alleged inventive effect, nor do they specify any particular result that such grading must achieve, instead using the vague term "to aid." Carriers are constantly in motion based on

factors unrelated to graded doping. A POSITA is therefore left to wonder what graded profiles and what carrier movement is within the scope of the claim, and what profiles and movement are outside the scope. The "aid carrier movement" claim terms thus fail to provide sufficient notice of their claim scope and are therefore indefinite. *Interval Licensing*, 766 F.3d 1371.

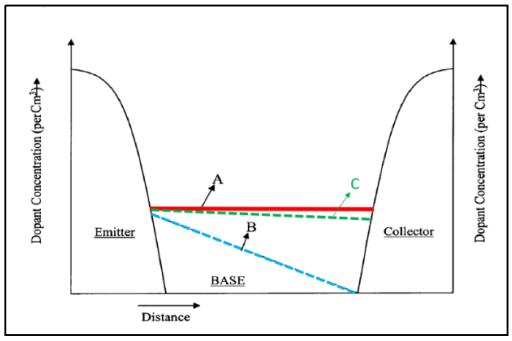
The intrinsic record does not provide any reasonable certainty as to claim scope. "Where, as here, we are faced with a 'purely subjective' claim phrase, we must look to the written description for guidance." *Interval Licensing*, 766 F.3d 1371. However, the specification is devoid of any such guidance, rendering the claims indefinite. *Id.* at 1372 (finding "unobtrusive manner" indefinite because "[t]he hazy relationship between the claims and the written description fails to provide the clarity that the subjective claim language needs")

The entire description of graded dopant concentration and purported carrier movement in CMOS devices (the only types of devices accused of infringement) is confined to two short paragraphs of the specification and associated figures 5(a)-(c). Ex. A, '195 Patent at 3:14-61, *id.* at Figures 5(a)-(c). Neither of these two paragraphs nor any of those three figures describe or provide any guidance as to the appropriate graded dopant concentrations that would adequately "aid" carrier movement, or the requisite degree or nature of such "aiding." Ex. V, ¶ 65. The specification, in fact, uses "graded" dopant broadly to describe a dopant concentration that is not uniform. *Id.* at 3:45-49 (discussing "graded channel instead of a uniformly doped channel (as practiced in prior art)."). Compounding the ambiguity, the specification states that the wells of CMOS devices "can be graded or retrograded in dopants, as desired" (*Id.* at 3:38-40), despite the fact that the "background of the invention" section criticizes the effectiveness of such prior-art retrograde wells. *Id.* at 1:59-62 ("'Retrograde' wells have been attempted, with little success…."). Most significantly, the specification is devoid of any numerical range of doping levels or doping

gradients, and bereft of any objective guidance on how to assess or measure carrier movement (is it displacement? speed? acceleration? or change of direction?) and how to objectively assess that a graded dopant concentration "aids" the movement of carriers. Ex. V, ¶ 66; *see U.S. Well Servs., Inc. v. Halliburton Co.*, No. 6:21-CV-00367-ADA, 2022 WL 819548 (W.D. Tex. Jan. 17, 2022) (Judge Albright), at *7 (finding "high pressure" indefinite because "[t]he specification . . . do[es] not provide guidance that would clarify the meaning of the term 'high pressure,' or provide a baseline of comparison to allow skilled artisans to differentiate a pump that is 'high pressure' from a pump that is 'not high pressure.'"); *Evicam Int'l, Inc. v. Enf't Video, LLC*, No. 4:16-CV-105, 2016 WL 6470967, at *20 (E.D. Tex. Nov. 2, 2016) ("The lack of objective criteria for evaluating the meaning of 'extended' renders the disputed term ['extended period of time'] indefinite."); *Nabors Drilling Techs. USA, Inc v. Helmerich & Payne Int'l Drilling Co.*, No. 3:20-CV-03126-M, 2022 WL 1689444, at *15 (N.D. Tex. May 26, 2022) (finding "optimized path" indefinite because "[t]he specification is bereft of any guidance on criteria that may be relevant to assessing whether a path … is optimized."); *JobDiva, Inc. v. Monster Worldwide, Inc*, No. 13-CV-8229 KBF, 2014 WL 5034674, at *17 (S.D.N.Y. Oct. 3, 2014) (finding "to improve a precision ratio …" indefinite, and noting that "[w]ithout some additional guidance, a person of ordinary skill in the art would not have known how to measure 'improvement' [] and thus could not have known whether he or she was infringing the Patents.").

Other sections of the specification further highlight the lack of objective guidance as to what constitutes an appropriate graded dopant concentration to "aid" carrier movement, or what constitutes the type and degree of "aid" that either falls within or outside the scope of the claims. Ex. V, ¶¶ 67-68. For example, with regard to bipolar junction transistors (BJT), the specification admits that there exists a baseline carrier movement through the base of a BJT even if the base is

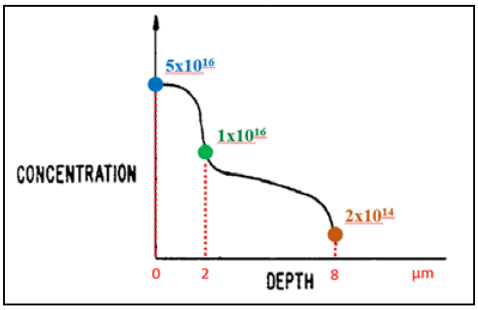
uniformly doped, as reflected in the uniform doping profile "A" (red) of Figure 1 below—the only figure of the specification that depicts any doping profile. Ex. A, '195 Patent at 1:31-33. The specification alleges that a graded base, as reflected in the illustrative graded doping profile "B" (blue) of Figure 1, could speed carrier movement. *Id.* at 1:34-36, 2:13-15, 2:42-45.



Ex. V, ¶ 67 (annotating Ex. A, '195 Patent at FIG. 1 ("Prior Art")). Here again, however, the specification is devoid of any objective guidance on how to assess carrier movement caused by graded dopants (in comparison to the baseline carrier movement that already exists in a uniformly doped base) that is sufficient to fall within the scope of the claimed "aiding" of carrier movement. *Id*. For example, profile "C" (green) illustrates a graded dopant concentration that is only marginally different from the uniform doping profile "A" (red)—does it "aid" movement of carriers?

The prosecution history and IPR record do not add clarity. To the contrary, they illustrate the difficulty in pinning down the objective claim scope of the "to aid" claim terms. Ex. V, ¶¶ 69-73. In a previous IPR, Greenthread was faced with prior art that disclosed graded, downward-sloping dopant concentration profiles, such as the graded profile illustrated in Figure 11 of the Payne prior art. Significantly, in contrast to the specification of the Asserted Patents which does not contain any dopant concentration data for CMOS devices (*see* Ex A, '195 Patent at 3:14-61), Payne provides detailed dopant concentration data, reflected in the annotated Figure 11 below. Ex.

V, ¶ 70-71.



Ex. V, ¶ 70 (annotating Ex. J at Fig. 11). Although Greenthread had previously argued to the USPTO that a downward-sloping dopant concentration moves carriers to the substrate (Ex G at 289-90), Greenthread distinguished Payne on the ground that its graded, downward-sloping doping profile is "inadequate" to satisfy the "aid carrier movement" claim terms.[14] Ex. P at 70 ("Fig. 11 is ***inadequate*** for determining Payne's doping gradient or electric fields, ***or the resulting impact on minority carrier movement***."). Greenthread's IPR position highlights the fact that the "aid carrier movement" claim phrases are indefinite because their claim scope is left to "the unpredictable vagaries of any one person's opinion" in the total absence of any objective boundaries. *Interval Licensing*, 766 F.3d at 1374.

Alternative Proposed Construction: "to sweep the [minority] carriers from … [to/towards] …" Greenthread's position that the "aid carrier movement" claim terms should be accorded plain meaning must be rejected because the terms are indefinite under their plain meaning, as detailed above. Should the Court decline to hold the claims invalid, however, it should limit their scope at least to what is clearly identified in the specification as the cornerstone of alleged invention. *Regents of Univ. of Minnesota v. AGA Med. Corp.*, 717 F.3d 929, 936 (Fed. Cir.

14 *See Aylus Networks*, 856 F.3d at 1362 ("[S]tatements made by a patent owner during an IPR proceeding, whether before or after an institution decision, can be considered for claim construction.").

2013) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention."). Here, the specification makes clear that the hallmark ("novel technique") of the alleged invention is the creation of an electric field through graded doping that is itself strong enough to "sweep" all unwanted carriers "into the substrate":

> Spurious minority carriers…can discharge dynamically-held 'actively held high' nodes. … Hence, ***a novel technique*** has been described here by creating a drift field ***to sweep these unwanted minority carriers into the substrate*** as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration ***to sweep the minority carriers deep into the substrate***.

Ex A, '195 Patent at 3:14-35; Ex. V, ¶ 75. Applicant attempted to claim precisely that during prosecution of the '195 Patent—a device having "a graded concentration of dopants … ***drawing all*** minority carriers ***from*** [the] surface layer ***to*** [the] substrate." Ex. G at 247, 250-52 (pending claims 10 and 18) and 253. Defendants' proposed alternative constructions are drawn from the applicant's express description of the "invention" in the specification, which does not provide any objective guidance as to what falls within the scope of "aiding" carrier movement (as detailed above), and are consistent with the file history.

F. "well region"

Claim Term	Defendants	Greenthread
"well region"	"A well, whether formed by single or multiple implants. Portions of a well are not well regions."	Plain Meaning

Defendants' proposed construction for "well region," which appears in all asserted claims of the '195, '502, '481, and '014 Patents and Claims 1, 21, 40, and 44 of the '222 Patent, is consistent with the intrinsic evidence, including Greenthread's disclaimer in a prior IPR proceeding that expressly refuted any interpretation of "well region" as a ***portion*** of a well. Each

of the asserted claims containing this term requires two separate elements having a graded dopant concentration: a "single drift layer" and a "well region,"[15] or an "active region" and a "well region."[16] Greenthread unequivocally told the USPTO that "***[n]either the claims . . . nor the specification suggests to a POSITA that the claimed 'well region' is broad enough to include only a portion of a well,***" Ex. P at 47, and that "well region" instead referred to an entire semiconductor well. Greenthread also disclaimed any interpretation that would permit "well region" to be read on a portion of a well and another claim element, such as a "single drift layer" to be read on another portion of that well.

Read in light of the specification, "at least one well region" refers to a semiconductor well. The specification describes using graded dopants in different locations, including an "n-layer" and a well. For example, the specification describes a "subterrain n-layer" that "has a graded donor concentration to sweep the minority carriers deep into the substrate," which can be a "deeply-implanted layer" or an "epitaxial layer." Ex. A, '195 Patent at 3:33-38. Separately from this layer, the specification notes that "***[t]he n-well and p-well also can be graded or retrograded in dopants***, as desired, to sweep those carriers away from the surface as well." *Id.* at 3:38-40. Figure 5(a) illustrates these wells as disposed in the "graded dopant n-layer." Indeed, the specification's one use of the term "well region" uses that term synonymously with a well, contrasting the well with the substrate. *Id.* at 1:50-51 ("Most MOS devices use a uniformly doped substrate (or a well

[15] For example, Claim 1 of the '195 Patent, Claim 7 of the '502 Patent, and Claim 44 of the '222 Patent each require a "single drift layer . . . having a graded concentration of dopants" and separately "at least one well region disposed in said single drift layer . . . having a graded concentration of dopants."

[16] The remaining asserted claims in which this term appears require an "active region[] having at least one graded dopant concentration" and separately "at least one well region adjacent to the first or second active region containing at least one graded dopant concentration." *See* Ex. E, '481 Patent, Cls. 1, 20; Ex. C, '222 Patent, Cls. 1, 21, and 40; and Ex. F, '014 Patent, Cls. 1, 21.

region).”).

Greenthread confirmed this understanding in a prior IPR proceeding where the petition argued that the asserted claims were anticipated and rendered obvious by U.S. Patent Application Publication No. 2003/0183856 to Wieczorek (“Wieczorek”). As shown below in Wieczorek’s Figure 1a, below, Wieczorek disclosed a CMOS semiconductor device having an N-well structure and a P-well structure, each of which were formed by multiple dopant implantation steps, followed by a heating (annealing step).

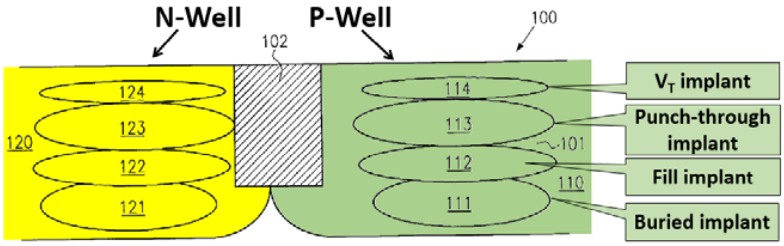


FIG.1a
(Prior Art)

Ex. K, at Fig. 1a (annotated), 3f, ¶¶[0004]-[0006]. As shown below in Wieczorek’s Figures 2(a) and 2(b), after annealing, the multiple implants in each well were smoothed into a graded dopant concentration, where the concentration was reduced with depth.

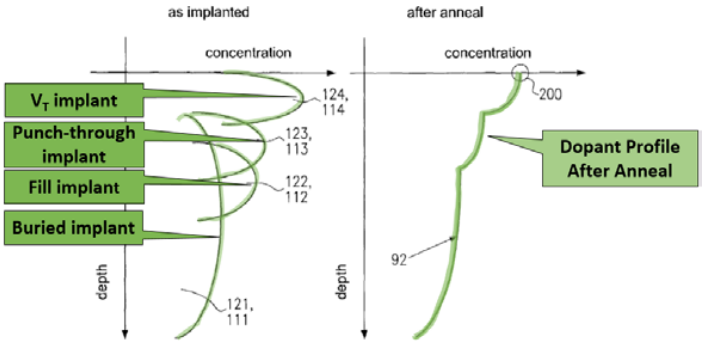


FIG.2a
(Prior Art)

FIG.2b
(Prior Art)

Ex. K, FIGS. at Figs. 2(a) and 2(b) (annotated), ¶¶[0009]-[0011]. The petition argued that a portion of each well structure constituted the claimed “single drift layer” having a graded concentration of

dopants and that another portion of the well structure was the claimed "at least one well region." Ex. O at 81, 73-82. The petition thus urged that the multiple implant steps used to form each well structure satisfied both the "single drift layer" and "well region" limitations of the asserted claims. *Id*. at 78-80.

Greenthread's response included a ten-page claim-construction section addressing the "plain and ordinary meaning" of the term "well region." Ex. P at 44-55. Greenthread unequivocally admitted that a POSITA would understand "well region" to encompass an entire well and that it would not encompass only a portion of a well: "***Nowhere in the claims or the specification does the '195 patent suggest that the claimed "well region" is a portion of a well. . . . [S]uch a construction [would] be inconsistent with . . . the manner in which a POSITA would understand the term "well region[.]***" *Id*. at 47; *see also id*. at 45 ("Petitioner's implied construction of 'well region,' i.e., ***'a portion of a well formed by an implantation step,' is inconsistent with the intrinsic record and the meaning of the term to a POSITA.***"). Greenthread's IPR expert similarly opined that a POSITA would not understand "well region" to be "broad enough to include only a portion of a well." Ex. Q, ¶ 41.

Having restricted "well region" to refer to an entire well, Greenthread argued that each of Wieczorek's well structures was a ***single well formed by multiple implant steps*** and could not satisfy both the "well region" and "single drift layer" limitations of the claims. Ex. P at 80. Greenthread emphasized that the fact that a well is formed by multiple implants does not transform that well into multiple "well regions": "A single well can be, and frequently is, formed by multiple implants. . . . [T]he fact that ***multiple implants*** are used to form a well ***does not mean that the well becomes a series of separate . . . well regions***." *Id.* at 50; *see also id.* at 55, 73. Greenthread's IPR expert likewise admitted that a "POSITA would understand that just because more than one

implant is used to form a well does not mean that that well constitutes multiple separate wells, or 'well regions.' ***This would be contrary to how a POSITA would understand wells generally and the term 'well region'*** in the '195 Patent specifically." Ex. Q, ¶ 50.

In view of these admissions, Greenthread cannot reasonably dispute that Defendants' proposed construction captures the plain and ordinary meaning of "well region." Moreover, Greenthread statements are a clear disclaimer of claim scope. Greenthread argued Wieczorek did not disclose both a "single drift layer" and a "well region," but rather disclosed only a conventional well structure with multiple-implant wells. Ex. P at 72. In doing so, Greenthread disclaimed any construction of "well region" under which "***a portion of a well***" could be a "well region" within the meaning of the claims. *Id.* at 74. Greenthread made these arguments in urging the USPTO to deny institution of IPR on the '195 and '502 Patents, and they constitute an express disclaimer that is "clear and unmistakable." *Aylus*, 856 F.3d at 1364 (Fed. Cir. 2017) (finding "statements [made] during an IPR proceeding were a clear and unmistakable disavowal of claim scope"). As such, Greenthread should be bound to its disclaimer here. *See id.* at 1360 ("Extending the prosecution disclaimer doctrine to IPR proceedings will ensure that claims are not argued one way in order to maintain their patentability and in a different way against accused infringers."). Defendants' proposed construction does just that: it reflects that the claimed "well region" is an entire well "whether formed by single or multiple implants" and makes clear that "portions of a well are not well regions."

G. "active region … within which transistors can be formed"

Claim Term	Defendants	Greenthread
"active region . . . within which transistors can be formed"	Indefinite	Plain Meaning

The claim term "active region . . . within which transistors can be formed," which appears in all asserted claims of the '842, '481, '014 Patents and Claims 1 and 21 of the '222 Patent, is indefinite. While the terms "active region" and "region . . . within which transistors can be formed" can be separately understood, they become indefinite when combined together to define the same region. A region is "active" when an existing device is formed there causing electrical current to flow. However, once a device exists, additional transistors cannot be formed in that same location without destroying the existing device. This unresolvable contradiction makes the claims indefinite.

The claims including this term each require (1) "a first active region . . . within which transistors can be formed," (2) "a second active region . . . within which transistors can be formed," and (3) "transistors formed in at least one of the first active region or second active region."[17] As such, the claimed semiconductor device has two "active regions" in which transistors "can be formed," at least one of which must include transistors that are already "formed."

The intrinsic and extrinsic evidence both describe what it means for a region to be an "active region." As the term "active" implies, an "active region" is the area in an existing device where current flows, such as the path created by the source, channel, and drain in a transistor.[18] This evidence also describes regions that are not electrically "active" where transistors can be

[17] Ex. D, '842 Patent, Cls. 1, 9; Ex. E, '481 Patent, Cls. 1, 20; Ex. C, '222 Patent, Cls. 1, 21, 39, 41-42; Ex. F, '014 Patent, Cls. 1, 21.

[18] *See supra* Section C; Ex. V, ¶ 79; *see also, e.g.*, Ex. D at Abstract, 2:16-18, 2:25-26, 3:62-63, Figs. 3A, 3C, 5A-5(C), Cls. 5, 7, 18 (claiming "active regions" including "p-channel and n-channel devices" such as "CMOS transistors requiring a source, a drain, a gate and a channel region"); Ex. GG at 21; Ex. DD at GREENTHREAD-WDTX-002863, 2871-2871 (describing "CMOS transistors" having the same "active regions").

formed, such as a non-active substrate or well.[19] But the patents provide no description of any region that is ***both*** (1) an "active region" and (2) a "region . . . within which transistors can be formed." Ex. V, ¶ [81]. Put differently, there is no discussion of how a region can be electrically "active" but not yet occupied by an existing device so that a transistor "can be formed" in it.

Rather than clarify the meaning of this term, the prosecution history further confuses it. Ex. V, ¶ 82. During prosecution of the earlier '195 and '502 Patents, Greenthread repeatedly referred to the claimed "active region" as the current path of an existing transistor,[20] such as the ***"electrically active surface region of [a] device"*** in Rhodes below,[21] and distinguished this region from the ***surrounding "wells" within which the transistors are formed***:[22]

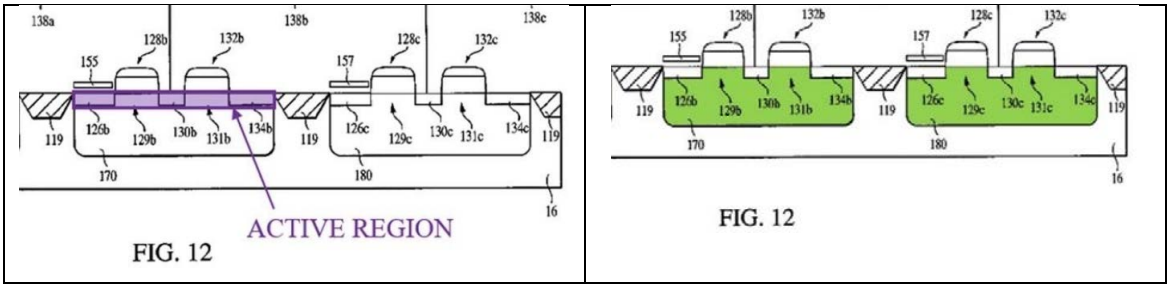
Active Region	Well Region
"Rhodes provides substantially the same disclosure . . . of an ***active region*** including a source and a drain, depicted in purple below":	"Rhodes discloses three separate ***wells***, p-wells 160 (deep retrograde p-well), 170 (shallow p-well), and 180 (shallow retrograde p-well), which are depicted in Figure 12, below":

[19] *See supra* Sections B-C, F; Ex. V, ¶ 80; *see also, e.g.*, Ex. D at Cl. 6, 2:16-18, 2:41-46, Figs. 3A, 3C (describing "a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated," such as "one n-well in which p-channel transistors are subsequently fabricated and one p-well in which n-channel transistors are subsequently fabricated"); Ex. W at Figs. 6-7, 10; Ex. DD at GREENTHREAD-WDTX-002860 ("nMOS transistors are built in a p-well and the pMOS transistor is placed in the n-type substrate" or "in an n-well").

[20] *See supra* Section C; see also Ex. G at 96-97, 164-65 (the "active elements" are a "transistor . . . that can be active when a voltage (or current) is applied"); Ex. GG at 21 (the "active region (devices)" are a "p-channel transistor" or "n-channel transistors").

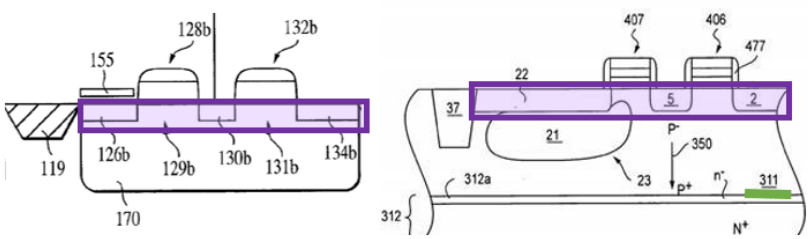
[21] Ex. L at ¶ 0045.

[22] Ex. P at 29-30, 34; *see also* Ex. G at 96-97, 164-65; Ex. GG at 21 (distinguishing "the active region (devices) on the surface" of Figures 3(a) and 5(a) from the "n^- well" and "p^- wells").



However, to obtain the later ’842, ’481, ’222, and ’014 Patents, Greenthread took the opposite position, and sought to conflate the claimed “active region” with the surrounding region or well within which transistors are formed. Ex. V, ¶¶ 82-83. The Hong reference cited by the examiner during prosecution of those patents[23] disclosed a CMOS image sensor with the same “active region” as Rhodes, including ***identical “transfer” and “reset” transistors***:[24]

Rhodes: **Hong:**



To distinguish Hong, Greenthread amended the claims to require a first/second active region “within which transistors can be formed,” and argued that the claimed “active region” was now the surrounding ***non-active region (311) within which the transistors are formed***:

[23] Ex. M; *see also* Ex. HH at 2-5; Ex. OO at 3-7.

[24] Ex. V, ¶ 83. In the CMOS image sensors of Rhodes and Hong, charge representing light accumulates in a region (126b in Rhodes, 21 in Hong) adjacent to the transfer transistor. Ex. L (Rhodes), ¶¶ 0007, 0059, Fig.12; Ex. M (Hong), ¶¶ 0003, 0005, 0038, Fig. 4D. The transfer transistor (128b/129b in Rhodes, 407 in Hong) transfers the accumulated charge to a diffusion region (130b in Rhodes, 5 in Hong), and a reset transistor (131b/132b in Rhodes, 406 in Hong) transfers out the charge to reset the charge level. Ex. L, ¶¶ 0006-0007, 0057, 0059, Fig. 12. Ex. M, ¶¶ 0002-0003, 0005, 0038-0040, Fig. 4D.

> [T]he term ***"wells"*** in semiconductor technology typically refers to a region formed in a substrate within which active components are formed. . . . Applicant had previously amended the claims to define the ***"active regions"*** as regions within which transistors can be formed . . . . Thus, there is provided ***only a "single" active region 311 within which two transistors are formed*** with the transistor gate stacks 407 and 406 and their associated source/drain regions.[25]

And, at the same time, it argued that the ***electrically active current paths in the existing transistors (21, 22, 5, and 2)*** of the pixel cells are no longer the claimed "active region":

> Applicant had previously amended the claims to define the "active regions" as regions within which transistors can be formed . . . . This is a clear distinction, as a well 2 or 5 ***cannot have a transistor formed therein***. . . . There are ***no transistors formed*** within the region 22 or the region 5 or the region 2 . . . . [T]here is no discussion in Hong that ***a transistor of any type can or could be formed*** in the active region 21.[26]

Thus, Greenthread first argued that an "active region" is the current path of an existing transistor, but later argued that an "active region" is the non-active region within which the transistor is formed. Not surprisingly, the examiner was confused by this contradiction and unable to determine what structures fall within the scope of the claims. Ex. V, ¶ 85. When he allowed the '842, '222, and '014 Patents to issue, the examiner concluded at different times that the ***region (311) of Hong within which the transistors are formed*** was the claimed "active region"[27] and that the ***region comprising the current path in the existing transistors of Hong (21, 22, 5, and 2)*** was

[25] Ex. II at 2-3, 5-9; Ex. JJ at 2-3, 5-7.

[26] Ex. V, ¶ 84; Ex. II at 5-9; Ex. JJ at 5-7.

[27] *Compare* Ex. II at 5-7 (Hong discloses "only a 'single' active region 311," because the current path in existing transistors "cannot have a transistor formed therein"), *with* Ex. KK at 2-3.

the claimed "active region."[28] And, when he allowed the '481 Patent, the examiner found that ***neither region of Hong*** was the claimed "active region."[29]

Moreover, this inconsistent record also means a POSITA would not understand the scope of other terms that require an "active region." For example, many asserted claims require not only an "active region . . . within which transistors can be formed," but also an "area . . . where there are ***no active regions***."[30] If the claimed "active region" encompasses non-active areas within which a transistor can be formed, a POSITA would not know where the claimed "active region" and "area . . . where there are no active regions" begin or end. Ex. V, ¶¶ 81, 85.

This confusing record concerning what is (and is not) an "active region . . . within which transistors can be formed" means that the scope of this term cannot be determined with reasonable certainty. Ex. V, ¶¶ 81, 85. Is the claimed "active region" the current path in an existing transistor (as Greenthread first argued to obtain its earlier patents), or is it the surrounding region such as a well or substrate within which a transistor can be formed (as it later argued to obtain its recent patents)?[31] If the "active region" is the current path in a transistor, how can additional transistors be formed in that existing device?[32] If the "active region" is the surrounding region where current

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[28] Ex. LL at 2-5 (Hong discloses only "a second active region . . . such as source/drain region 2 . . . or 5 or 22," but "the first region [311] is not an 'active' region"); Ex. MM at 2-3 (same).

[29] Ex. NN at 2-4 ("the 'first region' and 'second region' . . . are not 'active' regions and . . . transistor[s] cannot be formed in any of these regions.").

[30] Ex. V, ¶¶ 81, 85;'222 Patent, Cls. 1, 21, 39, 41-42; '014 Patent, Cls. 1, 21.

[31] *See, e.g., Infinity Computer Prod.*, 987 F.3d at 1059-61 ("The public-notice function requires that we hold patentees to what they declare during prosecution. But holding Infinity to both positions results in a flat contradiction, providing no notice to the public . . . ." (citation omitted)).

[32] *See, e.g.*, Ex. II at 5-9 (arguing that regions comprising the current path of an existing transistor "cannot have a transistor formed therein").

does not flow, what makes that region "active"?[33] And if it is the surrounding region, what is the difference between the claimed "active region" and other regions where transistors can be formed, such as a "well region" or "substrate"—where does one region end and the other begin?[34]

When, like here, "the claim language and specification do not provide reasonable certainty," and both Greenthread and the examiner took "conflicting positions during prosecution" regarding what the term means, the claims are indefinite. *Infinity Computer Prod.*, 987 F.3d at 1059-61 (the patentee took "inconsistent" and "contradictory positions" during prosecution of related patents, and "holding Infinity to both positions results in a flat contradiction, providing no notice to the public of 'what is still open to them.'" (quoting *Nautilus*, 572 U.S. at 909, emphasis removed)); *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1341-45 (Fed. Cir. 2015) (the patentee argued that "average molecular weight" had different meanings during prosecution of related patents); *TVnGO*, 861 F. App'x at 457-60 ("'the intrinsic evidence presents . . . irreconcilably inconsistent information" as to what a term means).

V. CONCLUSION

Based on the foregoing, Defendants respectfully request the Court to hold the Asserted Patents invalid for indefiniteness and otherwise adopt Defendants' proposed constructions of the remaining disputed terms.

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[33] *See, e.g.*, *Haemonetics Corp. v. Baxter Healthcare Corp.*, 607 F.3d 776, 781 (Fed. Cir. 2010) ("we construe claims with an eye toward giving effect to all of their terms, even if it renders the claims inoperable or invalid" (citation omitted)).

[34] *See, e.g.*, *SIPCO*, 794 F. App'x at 949 ("Because the patentee chose to use different terms… we presume that those two terms have different meanings.").

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are being served with a copy of the foregoing document via the Court's CM/ECF system on October 10, 2022.

/s/ J. Stephen Ravel
J. Stephen Ravel