UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELL TECHNOLOGIES INC. AND DELL INC.,

Petitioners,

v.

GREENTHREAD LLC,

Patent Owner.

Case: IPR2023-00506

U.S. Patent No. 10,510,842

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

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1004	Curriculum Vitae of Travis Blalock, PhD
1005	Publication Declaration of Sean O'Bryan for Maziasz ("O'Bryan Decl.")
1006	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe")
1008A	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2")
1008C	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3")
1008D	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4")
1009	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
1011	Publication Declaration of Martin L. Knott for Rabaey ("Knott Decl.")
1012	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
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1021	Defendants' Reply Claim Construction Brief
1022	Sze, Semiconductor Devices Physics and Technology, 2d Ed., John Wiley & Sons (2002)
1023	Maziasz and Hayes, Layout Minimization of CMOS Cells, Kluwer Academic Publishers (1992) ("Maziasz")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics, per Director Vidal, Memorandum, "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation" at n.4, dated June 21, 2022
1025	Rabaey et al., Digital Integrated Circuits, A Design Perspective, Prentice Hall Electronics and VLSI Series (2003) ("Rabaey")
1026	Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong et al. ("Hong")
1028	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 10/934,915 (the "'915 App.")
1029	Excerpts from the Prosecution History of U.S. Patent No. 9,190,502 (the "'502 Patent")
1030	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 13/854,319 (the "'319 App.")
1031	U.S. Patent No. 4,160,985 to Kamins et al. ("Kamins")
1032	McGraw-Hill Dictionary of Scientific and Technical Terms (2003)
1033	Excerpts from the Prosecution History of U.S. Patent No. 11,121,222 (the "'222 Patent")
1034	U.S. Patent No. 9,647,070 to Rao (the "'070 Patent")
1035	U.S. Patent Application Publication No. 2003/0030488 to Hueting et al. ("Hueting")
1036	Redacted District Court Case Transfer Order
1037	Order Cancelling Markman Hearing

Petitioners Dell Technologies Inc. and Dell Inc. ("Petitioners" or "Dell") request *inter partes* review ("IPR") of claims 1-18 (the "Challenged Claims") of U.S. Patent No. 10,510,842 (Ex. 1001, "the '842 Patent").

I. INTRODUCTION

The '842 Patent is directed to a semiconductor device having a graded dopant concentration in an active region to aid carrier movement. Ex. 1001, 4:45-60 (claim 1), 5:14-29 (claim 9). This Petition demonstrates that the Challenged Claims are unpatentable as obvious.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Dell Technologies Inc. and Dell Inc. ("Petitioners" or "Dell") are the real parties-in-interest.[1]

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[1] Certain suppliers of components of products at issue in the district court litigation are obligated to indemnify Dell against claims asserted in that litigation. However, none of these suppliers have directed, controlled, funded, reviewed, participated in, or otherwise influenced Dell's IPR petition. For at least these reasons, Dell does not believe that these suppliers constitute real parties in interest. Furthermore, none of

B. Related Matters

The following litigation or *inter partes* reviews related to the ’842 Patent are pending:

- *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.,* Civil Action No. 6:22-cv-105 in the Western District of Texas (“District Court Case”), filed January 27, 2022;
- *Intel Corporation v. Greenthread LLC*, IPR2023-00308, filed December 5, 2022;
- *Sony Group Corporation v. Greenthread, LLC,* IPR2023-00376, filed December 17, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 3-22-cv-02001 in the District of Oregon, filed December 29, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6-22-cv-01293 in the Western District of Texas, filed December 21, 2022.

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those suppliers are currently statutorily barred or estopped from filing an IPR petition directed to this patent.

C. Counsel Service Information

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D. 37 C.F.R. §42.8(b)(4): Service Information

Dell concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email addresses: Dell-Greenthread@alston.com; and christopher.douglas@alston.com.

III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R.§42.15(a)(1) for this Petition to Deposit Account No. 160605. Review of 18

claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '842 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Prior Art Printed Publications

The '842 Patent claims priority to September 3, 2004.[2] Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '842 Patent:

- **Kawagoe:** U.S. Patent No. 6,043,114 to Kawagoe *et al.* (Ex. 1007) issued on March 28, 2000 and is prior art under 35 U.S.C. §102(b).[3]
- **Wieczorek:** U.S. Patent Application Publication 2003/0183856 to Wieczorek *et al.* (Ex. 1006) was filed on October 29, 2002 and published on October 2, 2003. Wieczorek is prior art under 35 U.S.C. §102(a) and §102(e).

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[2] Petitioner reserves the right to challenge the priority date in other proceedings.

[3] Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

- **Wolf:** Stanley Wolf and Richard N. Tauber, *Silicon Processing for the VLSI Era*, Lattice Press (2000) (Exs. 1008A-D), was published and publicly available no later than 2002, and is prior art under 35 U.S.C. §102(b). Exs. 1012-1013.
- **Gupta:** U.S. Patent No. 6,163,877 to Gupta (Ex. 1014) issued on December 19, 2000 and is prior art under 35 U.S.C. §102(b).

B. Relief Requested

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Blalock (Ex. 1003).

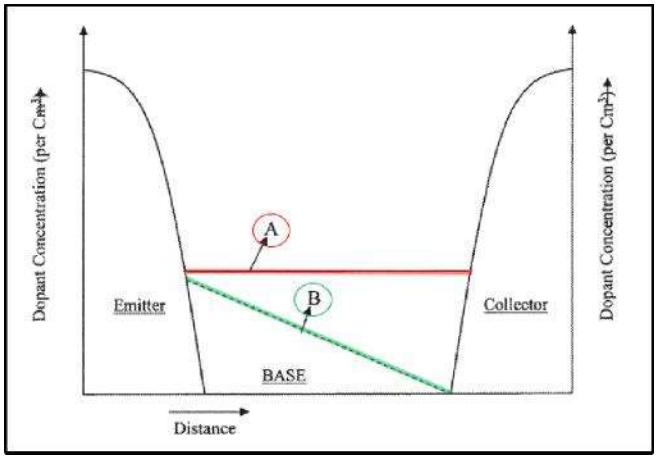
Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-2, 4-10, 12-18	Kawagoe
II	§103	1-3, 5-11, 13-18	Wieczorek, Wolf
III	§103	1-2, 4-10, 12-18	Kawagoe, Gupta
IV	§103	1-3, 5-11, 13-18	Wieczorek, Wolf, Gupta

VI. THE '842 PATENT

The '842 Patent is directed to "grading the dopant concentration" in certain regions of a semiconductor device. Ex. 1001, Abstract. The Challenged Claims

specifically claim that an active region of a semiconductor device has a graded dopant concentration to aid carrier movement. *Id.*, Cl. 1.

The ’842 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration “B” (green) in Figure 1 below is described as one of “the two most popular” doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile “A” (red). Ex. 1001, 2:35-38.



Ex. 1001, FIG. 1 (“Prior Art”).[4] The ’842 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the movement of carriers, but alleges, without support, that prior attempts were met with “little success.” *Id.*, 2:14-27.

[4] All colors and colored annotations to figures added.

The entire description of graded dopant concentration and purported carrier movement in CMOS devices (the only type of devices at issue in this Petition and in the District Court Case) is confined to two short paragraphs of the specification and associated Figures 5A-5C. Ex. 1001, 3:44-4:25, FIGS. 5A-5C. These paragraphs provide no guidance on how to grade a dopant concentration to "aid" carrier movement or the nature of such "aiding."[5] The specification, in fact, uses "graded" dopant broadly to describe a non-uniform dopant concentration. *Id.* at 4:10-13. The specification also does not describe grading in an active region of a CMOS device to move carriers to the substrate as claimed. Ex. 1001, Cl. 1. Instead, the specification only discusses grading the channel region of an active region "to accelerate majority carriers towards the drain." Ex. 1001, 4:5-7; 1003 ¶45.[6]

The Challenged Claims issued after two office actions rejecting the pending claims over Hong. Ex. 1002, 66-69, 109-113. According to the Examiner, the claims are allowed because Hong does not teach two separate "active" regions within which

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[5] Petitioner argues in the District Court Case that the "aid carrier movement" claim terms are indefinite. Ex. 1019, 18-24.

[6] Petitioner reserves the right to argue in the District Court Case that the claims are invalid for lack of written description support and for lack of enablement.

transistors can be formed "in conjunction with 'at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.'" Ex. 1002, 154-155.

Hong is in fact not prior art because it was filed on August 31, 2005, long after the claimed priority date of the '842 Patent. Ex. 1027. None of the prior art relied on in this Petition was cited or considered by the Examiner.

VII. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") of the subject matter of the '842 Patent would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Ex. 1003, ¶¶47-50. Additional education might compensate for a deficiency in experience, and vice-versa. *Id.*

VIII. CLAIM CONSTRUCTION

Claims in an IPR are construed under the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). The table below lists proposed constructions in the District Court Case. Exs. 1017-1021.

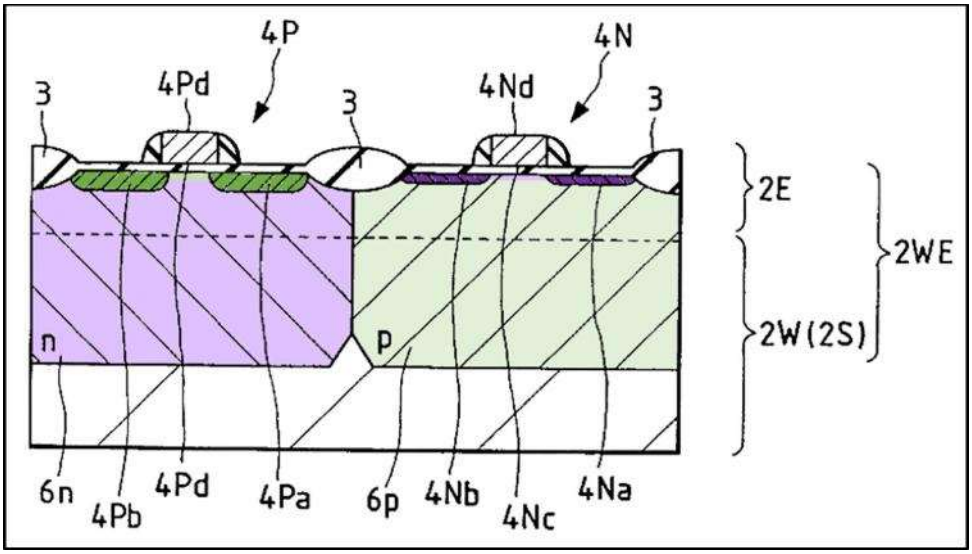
Claim Term	Patent Owner's Proposed Construction	Petitioner's Proposed Construction
"substrate"	Plain Meaning("an underlying layer")	"the initial material within which or on which the semiconductor device is fabricated"
"active region"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed")	"region that forms the current path of a device" or "the source,drain and channel region of a device"
"to aid carrier movement from ... [to/towards]	Plain Meaning	Indefinite Alternative Construction: "to sweep the carriers from ... [to/towards] ..."
"active region ... within which transistors	Plain Meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")	Indefinite

Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition, as the Challenged Claims are unpatentable under either party's proposed constructions (except for the term "active region ... within which transistors can be formed," which is addressed under Patent Owner's proposed construction). Ex. 1003 ¶54. Petitioner reserves the right to respond to any purported claim constructions that Patent Owner raises.

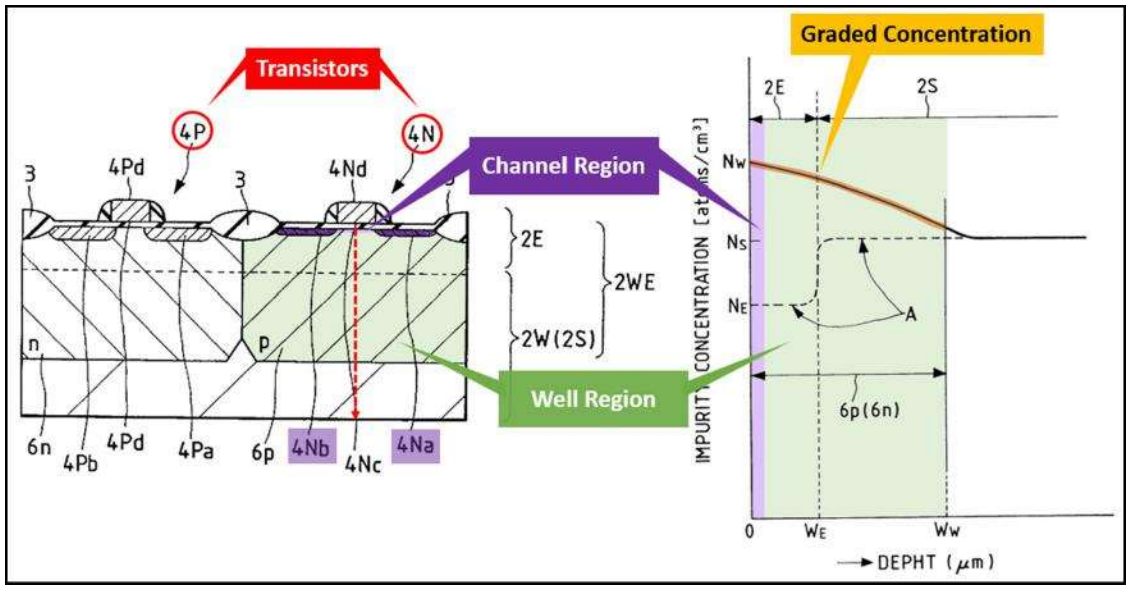
IX. OVERVIEW OF THE PRIOR ART

A. Kawagoe

Kawagoe describes CMOS devices fabricated using twin-well CMOS technology and an epitaxial substrate, whereby the epitaxial layer can be doped at the same level or at a lower level than the substrate body. Ex. 1007, 3:35-37, 6:657:3, 8:40-52, 15:13-17, 15:26-40. Kawagoe's figure below depicts a twin-well CMOS structure. Ex. 1007, 15:26-40, 18:18-23.



Id., FIG. 23. Kawagoe further teaches that the well regions have a graded dopant concentration that decreases with depth, as illustrated below in Figure 17. *Id.*, 14:46-55, 15:62-16:40 ("p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction ...").[7]

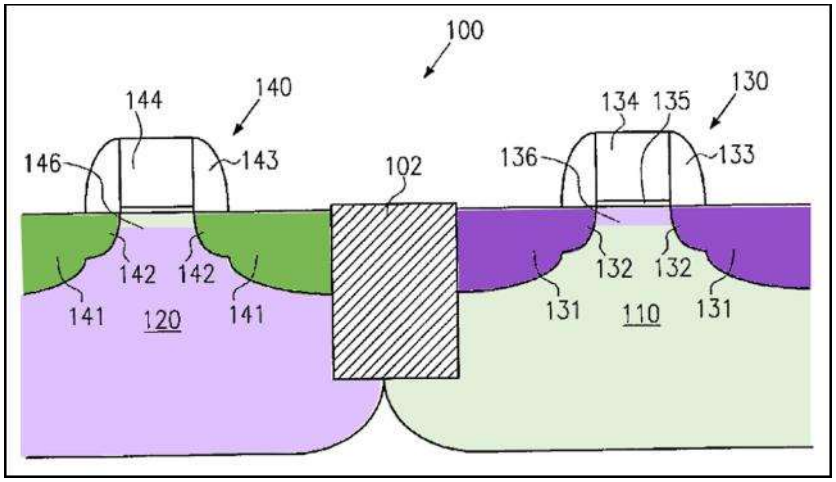


Id., FIGS. 17, 23. The graded dopant concentration reduces soft errors by sweeping unwanted carriers into the substrate body. *Id*., 16:2-11 ("electrons produced by the a-ray are ***attracted to the substrate body 2S*** by that concentration gradient ... so that the soft errors can be reduced.").

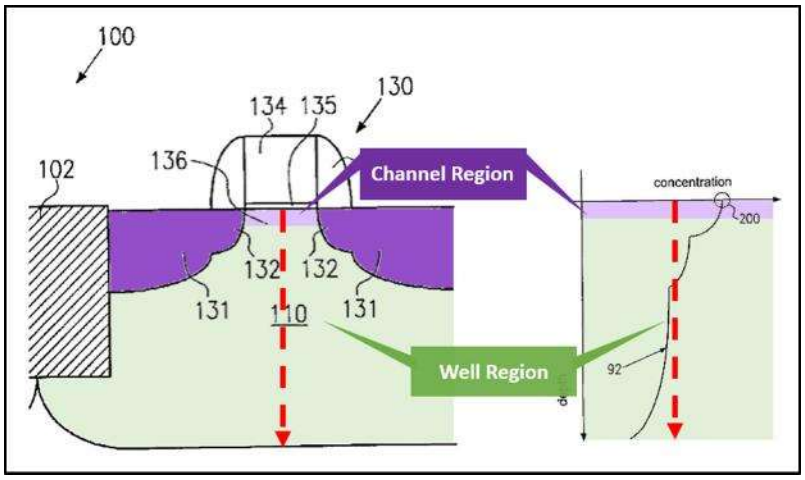
[7] All emphases added unless otherwise noted.

B. Wieczorek

This Petition relies on Wieczorek's description of conventional prior art CMOS devices, such as the twin-well CMOS device illustrated below in Figure 1b. Ex. 1006, [0007], [0012], [0020]-[0021].



Id., FIG. 1b. Wieczorek explains that graded dopant concentrations in prior art CMOS devices peak at the surface of the substrate and decrease with depth, as shown below. *Id*., [0004], [0007]-[0013].



Id., FIGS. 1b, 2b.

C. Wolf

Wolf is a four-volume textbook directed to semiconductor devices, with particular focus on CMOS devices. Exs. 1008A-D.

D. Gupta

Gupta is directed to circuit layout of CMOS devices. Ex. 1014. 1:7-10. As Gupta explains, "[c]onservation of semiconductor area is a primary goal in semiconductor chip development" and a common technique to conserve area is "by placing transistors so as to share diffusion area." *Id.*, 1:32-54, 2:17-21.

X. <u>SPECIFIC GROUNDS FOR PETITION</u>

A. Ground I:

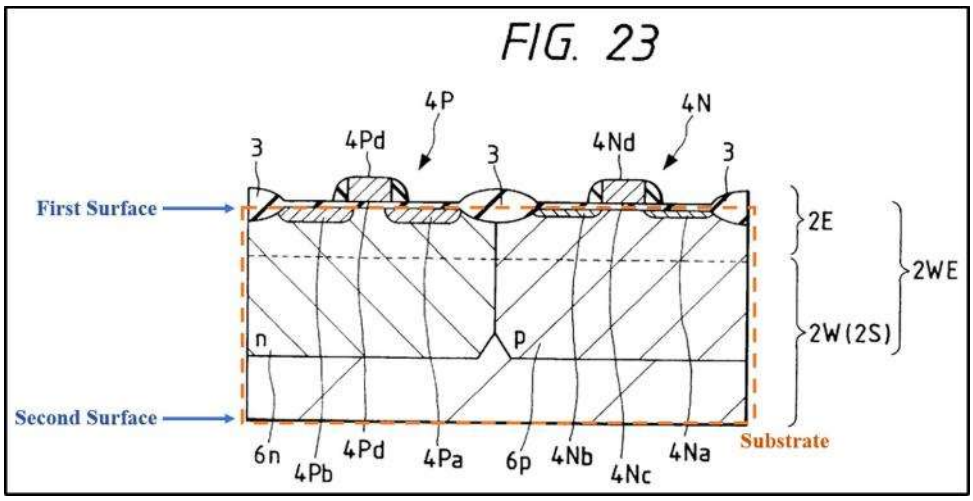
Kawagoe renders claims 1-2, 4-10, and 12-18 obvious. Ex. 1003, ¶¶65-119.

1. Independent Claim 1

Kawagoe is directed to a "semiconductor integrated circuit device" and process for making the same. Ex. 1007, Title, 1:13-23, 14:46-67, FIGS. 16-17, 23. The present Ground I primarily focuses on the twin-well CMOS device in Figure 23 (Embodiment 4), fabricated on a uniformly-doped epitaxial substrate, taught in Embodiment 1.[7] *See* X.A.1.b.

a. Preamble: "A semiconductor device, comprising:"

Kawagoe is directed to a "semiconductor integrated circuit device" and process for making the same. Ex. 1007, Title, 1:13-23, 14:46-67, FIGS. 16-17, 23. The present Ground I primarily focuses on the twin-well CMOS device in Figure 23 (Embodiment 4), fabricated on a uniformly-doped epitaxial substrate, taught in Embodiment 1.[8] *See* X.A.1.b.



Ex. 1007, FIG. 23.

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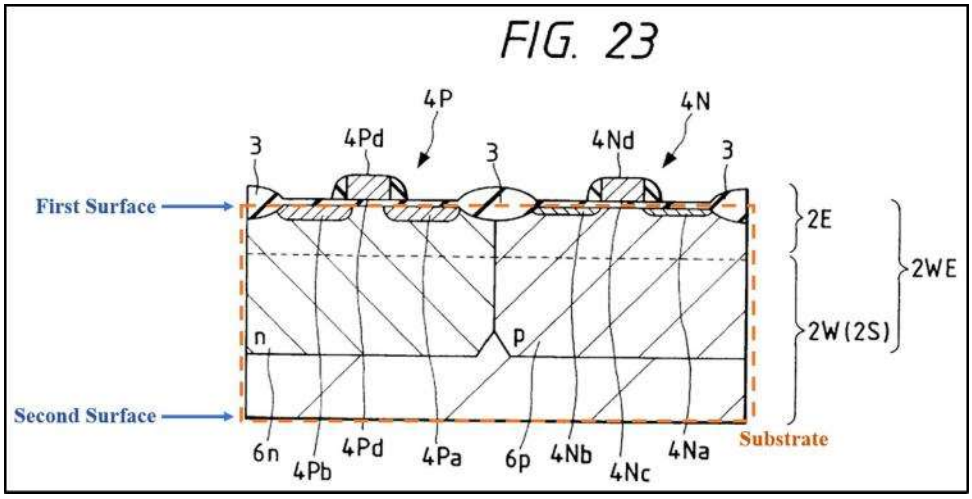
[8] Figures 16-17 and 23 are all directed to Kawagoe's Embodiment 4. Ex. 1007, 14:46-60. Figure 23 shows the same twin-well CMOS structures depicted in Figure 16 without the metal layers not relevant to the claims. Ex. 1007, 17:10-18:38; Ex. 1003, ¶66.

b. Element [1.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

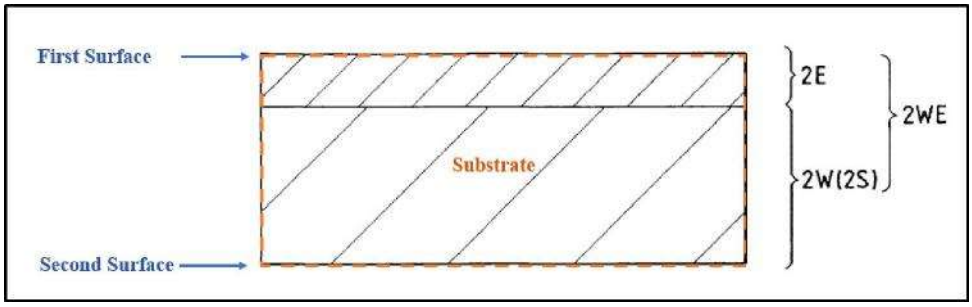
Kawagoe discloses a substrate ("semiconductor substrate 2") of a first doping type (p-type) having a silicon "epitaxial layer 2E [] doped with a ***p-type*** impurity such as boron" formed over non-epitaxial "semiconductor substrate body 2S [also] doped with a ***p-type*** impurity such as boron...." Ex. 1007, 14:61-15:12, 6:50-7:3. The substrate (orange) has top ("first surface") and bottom ("second surface") surfaces, as shown below. Ex. 1003, ¶67.



Id., FIG. 23.

Kawagoe satisfies element [1.1] under Patent Owner's plain meaning construction and under Petitioner's proposed construction because Kawagoe's epitaxial substrate is the initial material within or on which Kawagoe's

"semiconductor integrated circuit device 1" is later fabricated. Section VIII; Ex. 1007, 6:51-56, 14:61-67, 17:10-18:38; Ex. 1003, ¶68.



Ex. 1007, FIG. 20. As detailed below, Ground I relies on a uniformly-doped epitaxial substrate in which silicon epitaxial layer 2E of the substrate is doped at the same level as silicon substrate body 2S, so that the entire substrate in Figure 20 is "at a first doping level" as claimed. Ex. 1007, 6:60-7:3; Ex. 1003, ¶69.

<u>"at a first doping level"</u> - Kawagoe teaches an epitaxial substrate (2S+2E), illustrated in Figure 20, in which the non-epitaxial silicon substrate body (2S) is either doped at the same or higher level compared to the epitaxial silicon layer (2E). For example, Embodiment 1 describes a uniformly-doped epitaxial substrate in which the "epitaxial layer 2E is doped ... in a concentration ***equal*** to the [concentration] of the semiconductor substrate body 2S, e.g., 1.3×10^{15} atoms/cm^3." Ex. 1007, 6:60-7:3; *id.*, Abstract (describing "an epitaxial layer which contains an impurity of the ***same*** conduction type [and at] ... the ***same concentration***" as the bulk substrate), 2:57-3:9 (same). This uniformly-doped epitaxial substrate is

Kawagoe's "benchmark" substrate repeatedly discussed in other embodiments, including Embodiment 4. Ex. 1007, 12:64-65, 13:12-15, 13:66-67, 14:18-20, 15:7-25. Embodiment 4 introduces an optional latchup-resistant substrate in which "the impurity concentration of the semiconductor substrate body 2S is made ***higher*** than that of the epitaxial layer 2E ... ***to improve*** the resistance to latchup." Ex. 1007, 15:13-17; Ex. 1003, ¶71.

A POSITA would have understood that Kawagoe teaches forming Figure 23's twin-well CMOS device (Embodiment 4) on either a uniformly-doped epitaxial substrate described in Embodiment 1 or the optional latchup-resistant substrate described in Embodiment 4. Ex. 1003, ¶72. Indeed, Kawagoe emphasizes the benefits of Embodiment 1's uniformly-doped epitaxial substrate and explains that the substrate used in Embodiment 4 is formed "***as in the foregoing embodiment 1*** so that... the cost of the semiconductor substrate 2 is lowered to about one half." Ex. 1007, 15:7-25. A POSITA would have been motivated to use a uniformly-doped epitaxial substrate to form Figure 23's twin-well CMOS device because this substrate provides "excellent film quality" that "drastically reduce[s] the defect densities of the gate insulating films" and "improve[s] the [device's] performance, reliability and production yield." Ex. 1003, ¶73; Ex. 1007, 12:8-40; *id*., 15:7-25. This substrate is also easier to manufacture, helping "lower the cost" of the substrate and

chip. Ex. 1003, ¶73; Ex. 1007, 12:8-40. The use of uniformly-doped epitaxial substrate as the starting material in lieu of Embodiment 4's latchup-resistant substrate to form Figure 23's twin-well CMOS devices is a simple substitution of one known element with another known, closely-related element, both of which are described in Kawagoe, and would have been obvious to try because it involves nothing more than choosing one of two ways of doping an epitaxial substrate that are both described in Kawagoe.[9] Ex. 1003, ¶74. Twin-well CMOS devices (illustrated in Figure 23) fabricated on a uniformly-doped epitaxial substrate would have worked for their intended purpose. *Id.*, ¶75 As discussed in Wolf, twin-well CMOS devices were commonly formed over a "***uniform***, lightly doped *p*- or *n*-type substrate" that provides no improved latchup resistance. Ex. 1008C, 523; *id.,* 530 ("With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate ..."); Ex. 1008B, 387-389; Ex. 1007, 2:57-65 (discussing a uniform, "lightly doped" epitaxial substrate).

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[9] *Bos. Sci. Scimed, Inc. v. Cordis Corp.,* 554 F.3d 982, 991 (Fed. Cir. 2009) ("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.").

There would be reasonable expectation of success because Kawagoe describes in detail the use of both uniformly-doped epitaxial substrates and latchup-resistant substrates in forming CMOS devices, and repeatedly emphasizes their similarity. Ex. 1007, 8:40-52; 12:8-40, 14:58-60, 15:7-12 (substrate), 15:18-25 (epitaxial layer), 15:26-40 (transistors); Ex. 1003, ¶76. A uniformly-doped ***epitaxial*** substrate is also better than the bulk (non-epitaxial) substrate commonly used to fabricate twin-well CMOS devices. Ex. 1007, 1:33-40 ("The epitaxial wafer is advantageous [compared to bulk wafer/substrate] in that ... the gate insulating film to be formed over the epitaxial layer can have excellent breakdown characteristics to drastically reduce the defect density of the gate insulating film."); *id.*, 12:8-40; Ex. 1008B, 387-88 (discussing twin-well CMOS devices fabricated over bulk substrate); Ex. 1003, ¶76.

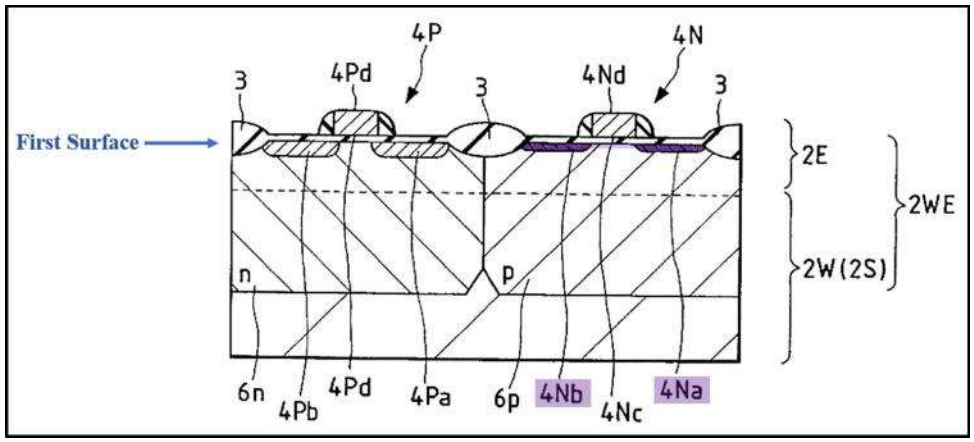
Kawagoe characterizes the improved latchup tolerance provided by Embodiment 4's optional latchup-tolerant substrate as just another "effect[] [that] can be achieved in addition to those of the foregoing embodiment 1." Ex. 1007, 19:49-63. Consistent with Kawagoe's teachings, a POSITA would have understood that a uniformly-doped epitaxial substrate is a suitable substrate because, among other benefits, it "drastically reduce[s] the defect densities of the gate insulating films" of CMOS transistors. Ex. 1007, 12:8-40 Ex. 1003, ¶77. Moreover, a POSITA

would have understood that improved latchup resistance is not needed for CMOS chips that are not susceptible to latchup or for which latchup (a "short-circuit" failure condition in poorly designed circuits) is not a concern. Ex. 1003 ¶77; Ex. 1008B, 406 ("four conditions must exist in a CMOS circuit in order for latchup to occur."); Ex. 1026, 1 ("several conditions must be met" to cause latchup). Indeed, twin-well CMOS devices were commonly fabricated on uniformly-doped bulk substrates that provide no improved latchup resistance. Ex. 1008B, 387-388 ("With the [twin-well] approach, ... [t]he substrate may be [] a lightly doped wafer ..."); Ex. 1003, ¶78. Even if latchup were to remain a concern, a POSITA would have understood that improved latchup resistance can be achieved by other means unrelated to the choice of substrate, such as careful circuit layout. Ex. 1003, ¶78; Ex. 1008B, 381 ("Latchup tolerance can [] be improved by spacing *n*- and *p*-channel transistors farther apart"), 419 ("Increasing the number of well contacts to VDD reduces latchup susceptibility" and thus "can serve as an alternative approach to improving latchup immunity.").

c. Element [1.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

Kawagoe discloses "semiconductor regions 4Na and 4Nb ... for forming the ***source-drain regions*** of the nMOS [n-channel transistor] 4N." Ex. 1007, 8:66-67;

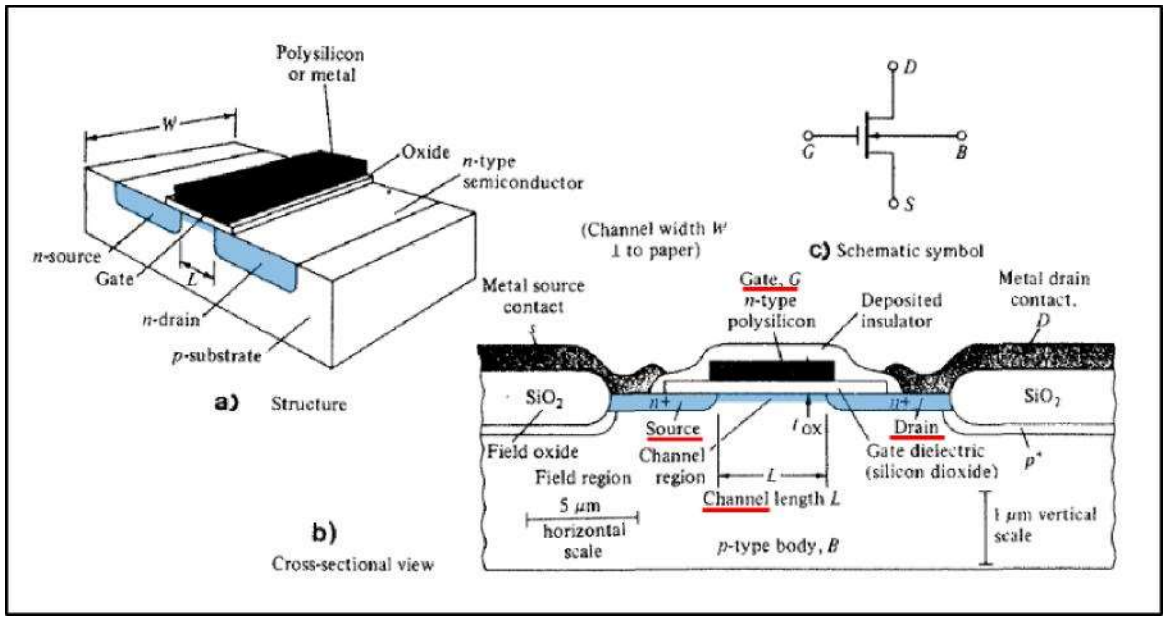
id., 3:35-37, 8:46-52, 14:46-55, 15:26-40. Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc. Ex. 1007, 8:46-65, 14:46-55, 15:26-40; Ex. 1003, ¶79; Ex. 1008B, 299-300 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), FIG. 52, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e). As shown in Figure 23, nMOS transistor 4N is formed in the first active region, which is adjacent the first surface of the substrate. Ex. 1003, ¶79.



Ex. 1007, FIG. 23. "[S]emiconductor regions 4Na and 4Nb are doped with an ***n-type impurity***" and thus have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate. Ex. 1007, 8:67-9:3, 14:46-55, 15:2640; Ex. 1003, ¶79.

While Figure 23 illustrates an exemplary nMOS transistor 4N in the first active region, a POSITA would have understood that Kawagoe teaches forming multiple nMOS transistors in this region to minimize chip area, as good layout practice dictates. Ex. 1003 ¶80; Ex. 1014, 1:52-54, 2:17-21. Regardless, according to Patent Owner, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex. 1020, 31.

Kawagoe satisfies element [1.2] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" because the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions," highlighted in blue in the figure below. Section VIII; Ex. 1008B, 299; Ex. 1003, ¶81.

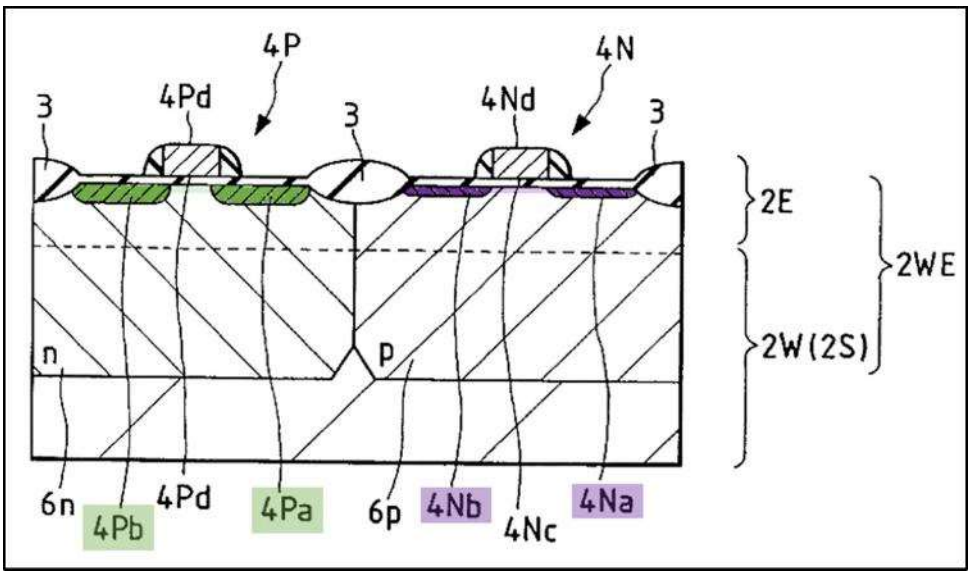


Ex. 1008B, FIG. 5-1; *id*., 298-301, FIGS. 5-2, 6-4. Kawagoe also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Section VIII; Ex. 1008B, 299-301, FIGS. 5-1, 5-2; Ex. 1008D, 197, FIG. 5-13; Ex. 1003 ¶82. Patent Owner does not dispute this. Ex. 1020, 3-4 ("when a positive voltage is applied to the gate ... a conductive ***channel*** [is formed] between the ***source*** and the ***drain***, and ***current*** can begin to flow through the transistor").

d. Element [1.3]: " a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

Kawagoe discloses "semiconductor regions 4Pa and 4Pb ... for forming the source-drain regions of the pMOS [p-channel transistor] 4P." Ex. 1007, 3:35-37, 8:46-52, 9:41-48, 15:26-40. Source-drain regions 4Pa/4Pb (green) are part of the claimed second active region, which also includes the channel region (light green) between them and below gate 4Pd. Ex. 1007, 8:46-57, 9:41-46, 14:46-55, 15:26-40; Ex. 1008B, 299-301, FIGS. 5-1, 5-2, 6-4; Section X.A.1.c; Ex. 1003, ¶83. As shown in Figure 23, pMOS transistor 4P is formed in the second active region (green/light

green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex. 1007, 14:46-55; Ex. 1003, ¶83. Adjacent active regions are separated by an isolation region (*e.g.*, insulating film 3). Ex. 1008A, 818-20, FIG. 16-11(f); Ex. 1003, ¶84. Indeed, claim 7 (depends from claim 1) recites, "the first active region and second active region are each separated by at least one isolation region." Ex. 1001, Cl. 7.



Ex. 1007, FIG. 23.

While Figure 23 illustrates an exemplary pMOS transistor 4P formed in the second active region, a POSITA would have understood that Kawagoe teaches forming multiple pMOS transistors in this region. Ex. 1003, ¶85; Section X.A.1.c. Regardless, according to Patent Owner, an "active region ... within which transistors

can be formed" means "an active region ... where ***a transistor*** can be formed." Ex. 1020, 31.

Kawagoe satisfies element [1.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex. 1003, ¶86; Section X.A.1.c. Kawagoe also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device." *Id*.

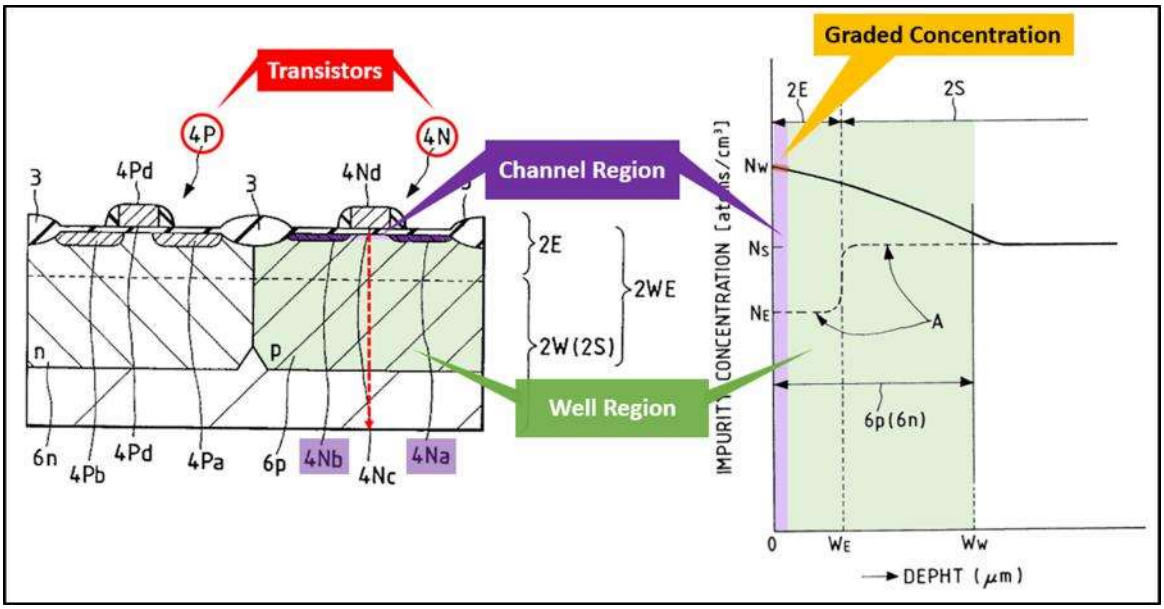
e. Element [1.4]: "transistors formed in at least one of the first active region or second active region; and"

Sections X.A.1.c-d

f. Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

As illustrated in Figure 23 (below left), a channel region (light purple) formed at the top surface of the substrate connects source-drain regions 4Na/4Nb (purple) of transistor 4N. Ex. 1008B, 298 ("A channel region in the semiconductor under the gate electrode separates the source and drain"), 300-301 ("When positive bias is applied to an NMOS transistor gate ... an *n*-type ***channel*** connects the ***source*** and

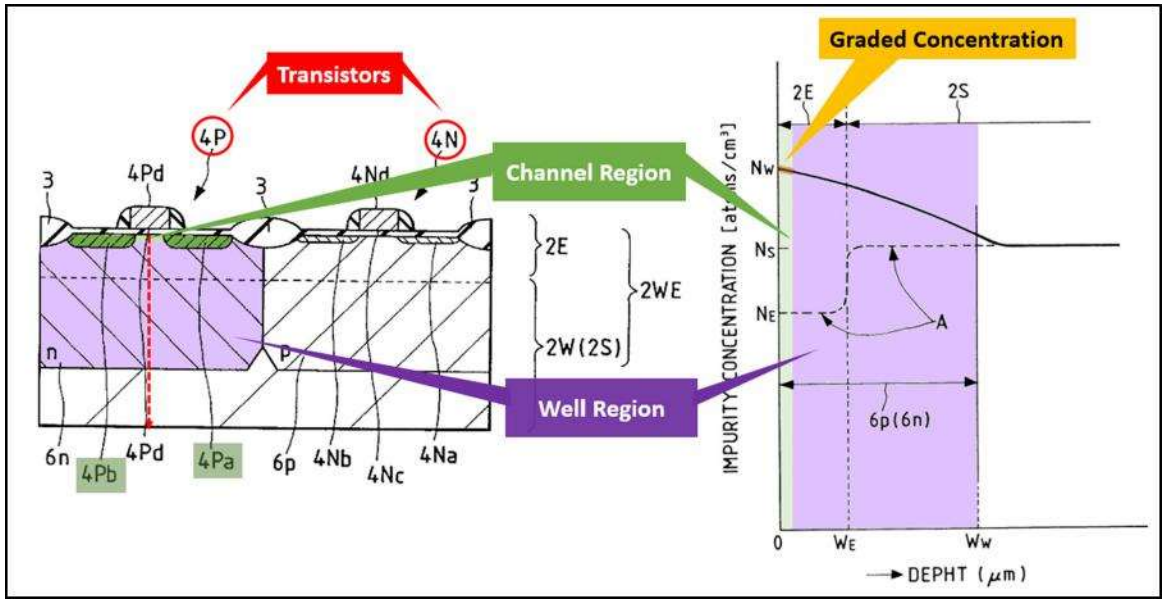
drain regions"), FIG. 5-2; Ex. 1007, 8:60-67, 14:46-55, 15:26-30, 15:37-40; Ex. 1003, ¶88. Patent Owner does not dispute this. Ex. 1020, 4 (the channel is "a thin layer below the surface" connecting the source and drain).



Ex. 1007, FIGS. 17, 23. Kawagoe's Figure 17 (above right) illustrates the doping concentration measured along the red dotted line in Figure 23 (above left), which starts from the top surface of the substrate (depth=0) and includes the doping profile in the channel region (light purple). *Id.*, 5:41-45. As Figure 17 shows, the dopant concentration is "gradually lowered in the depthwise direction ***from the principal surface*** (having an impurity concentration NW) of the epitaxial layer 2E." *Id.*, 15:6216:40. The dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at "the principal surface" (top surface) of epitaxial layer 2E. Ex. 1003, ¶89. As shown in Figure 17,

Kawagoe's graded dopant concentration is in fact downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region (light purple) and the underlying well region (green)—from depth=0 at the top surface of the epitaxial substrate to beyond depth=Ww where Ww is the depth at the bottom of the p-well 6p. Ex. 1007, 15:32-36; Ex. 1003, ¶89.

The same applies to the channel region of pMOS transistor 4P (a portion of the second active region), as illustrated below. Ex. 1007, 15:62-16:2 ("p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface [] of the epitaxial layer 2E."), 9:41-48, 14:4655, 15:32-40; Ex. 1008B, 298-301, FIGS. 5-2, 6-4; Ex. 1003, ¶90.



Ex. 1007, FIGS. 17, 23. Thus, Kawagoe discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex. 1003, ¶¶89-90.

Kawagoe further explains that such downward-sloping graded dopant concentration aids the movement of carriers from the top surface of the epitaxial layer (claimed "first surface") to the bottom surface of the substrate (claimed "second surface"):

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

Ex. 1007, 16:2-11.[10] Dr. Blalock explains that during a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or

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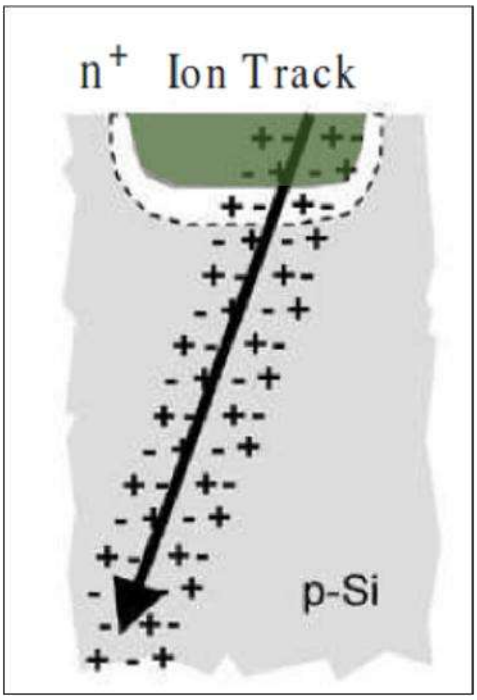
[10] Kawagoe also states that "electrons produced by the a-ray [are]... prevented from entering the p-well 6*p* ...." Ex. 1007, 16:7-9. This refers to electrons created by an a-

near the active region at the top surface of the substrate, as illustrated below. Ex. 1003, ¶92; Ex. 1009, 431 ("A[n] [a-]particle can induce SEU when it strikes at the ***channel region*** of an off nMOS transistor or the ***drain region*** [(green)] of an off pMOS transistor.").



Ex. 1009, FIG. 2. Kawagoe teaches that those carriers are "attracted to the substrate body by [the] concentration gradient" of the graded dopant concentration illustrated in Figure 17. Ex. 1007, 16:2-11.

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ray in the substrate body below the wells, by far the largest volumetric region of any chip. Ex. 1003, ¶91; Ex. 1009, FIG. 2.

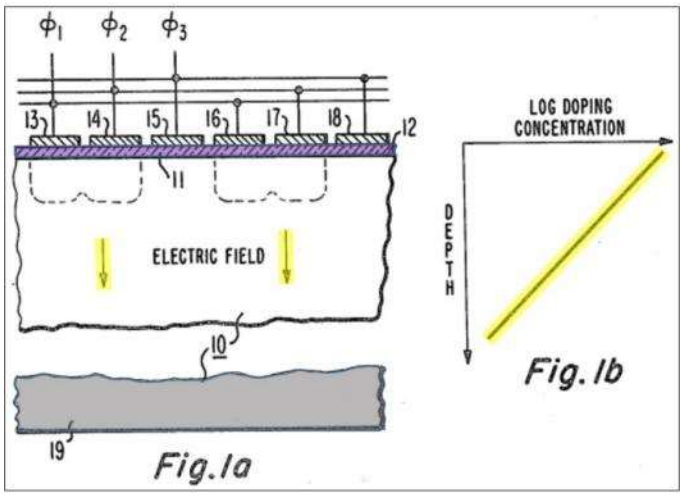
In light of the above, Kawagoe satisfies element [1.5] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Section VIII; Ex. 1003, ¶93. According to Patent Owner, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)" and "when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...." Ex. 1020, 2, 29. Here, Kawagoe's Figure 17 shows that the dopant concentration is downward-sloping with increasing depth towards the bottom of the substrate, and thus, according to Patent Owner (and also in light of Patent Owner's representation to the Patent Office, discussed below), this graded dopant concentration causes carriers to move deeper into the substrate as well. Ex. 1003 ¶93.

Kawagoe also satisfies this claim element under Petitioner's alternative proposed construction that the term means "to sweep the carriers from the first surface to the second surface of the substrate." Section VIII; Ex. 1003, ¶94. Notably, Kawagoe's Figure 17 illustrates a downward-sloping graded dopant concentration that aids carrier movement from the first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. Ex. 1003, ¶94. Applicant represented to Patent Office during prosecution

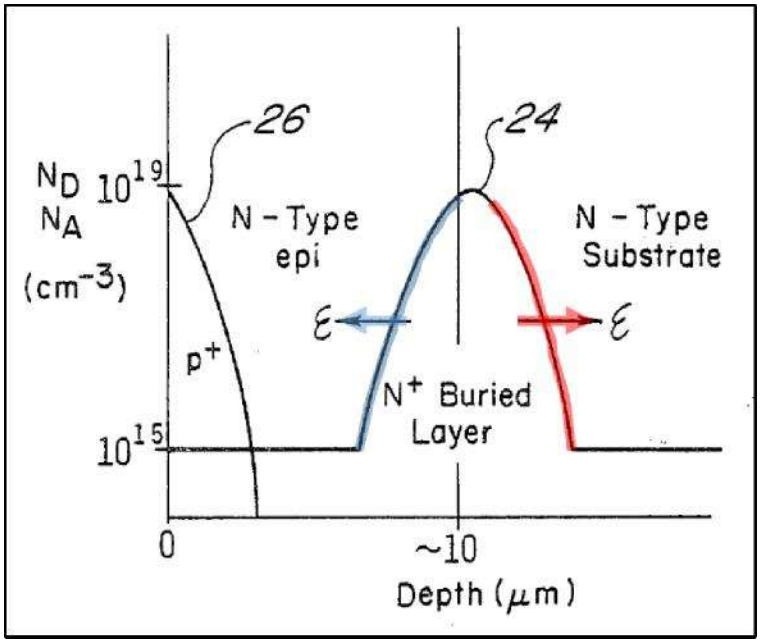
of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers down into the substrate (while an upward-sloping concentration, not at issue in Kawagoe, would move carriers in the opposite direction towards the surface):

> [T]he graded dopant concentration <u>itself</u> creates a ***'built-in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

Ex. 1016, 289-290 (underlining in original); Ex. 1003, ¶94. Applicant also represented that "a unidirectional drift (electric) field necessarily affects ***all*** the present minority carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, ***all*** minority carriers are either ***swept*** 'down' ... or 'up.'" *Id*., 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the doping concentration is "decreasing with depth" from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex. 1010, 5:14-22. Jastrzebski teaches that this downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers ... ***deep into the substrate***[.]" *Id.*, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b. Applicant made the same representation to the Patent Office regarding Kamins. Ex. 1016, 237-238. According to Applicant, Kamins' Figure 3 shows "two electric fields with opposing directions" (highlighted in blue and red) that correspond to increasing and decreasing graded dopant concentrations, respectively. *Id.*, 237 (citing Ex. 1031, 3:6-13). Applicant explained that the electric field associated with the downward-sloping graded concentration at depth beyond ~10mm (red) causes "carriers created [in that region to be] ... ***accelerated into the substrate*** ...." *Id.* (citing Ex. 1031, 3:6-13, FIGS. 2-3).



Ex. 1031, FIG. 3.

2. Claim 2: "The semiconductor device of claim 1, wherein the substrate is a p-type substrate

Section X.A.1.b.

3. Claim 4: "The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate

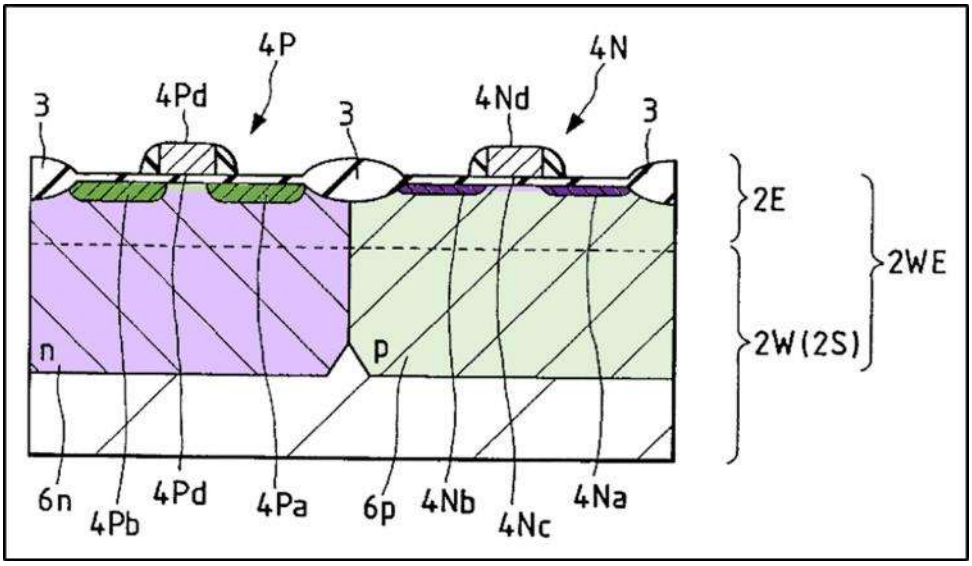
Section X.A.1.b.

4. Claim 5: "The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices."

Section X.A.1.c-e

5. Claim 6: "The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant."

Kawagoe's Figure 23 illustrates conventional twin-well architecture, whereby the first active region contains nMOS (n-channel) transistor 4N formed in p-well 6p, and the second active region contains pMOS (p-channel) transistor 4P formed in n-well 6n. Ex. 1007, 8:46-52, 14:46-55, 15:26-43; Sections X.A.1.c-d; Ex. 1008B, 387-88; Ex. 1003, ¶100. This mapping satisfies this claim under Patent Owner's interpretation that a claimed active region can contain "***a transistor***." Ex. 1020, 31; Ex. 1003, ¶101. A POSITA would have also understood that Kawagoe teaches forming multiple transistors in an active region to save chip area. Ex. 1003, ¶101.

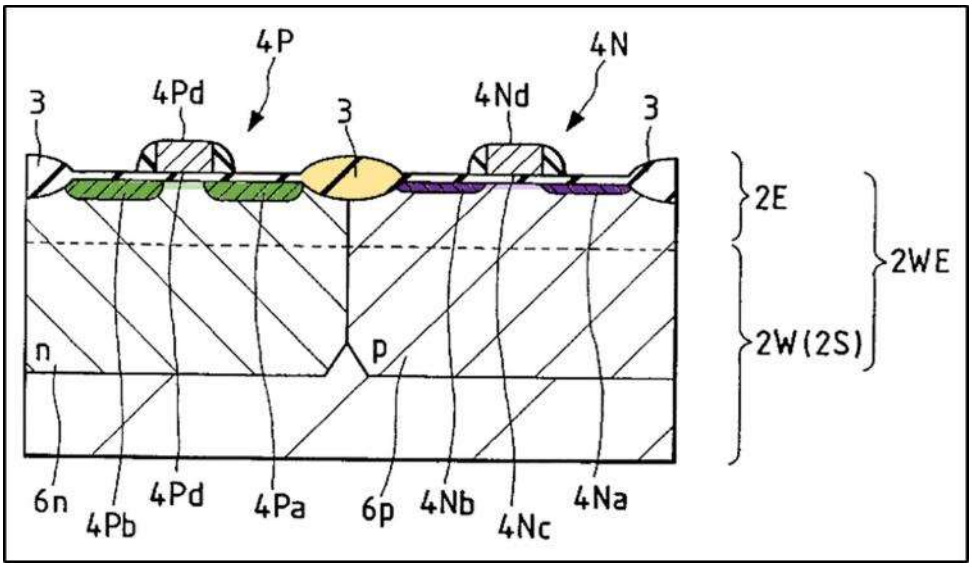


Ex. 1007, FIG. 23. Further, Kawagoe's n-wells and p-wells have graded dopants. *Id.*, 14:46-55, 15:62-16:2 ("as shown in FIGS. 16 and 17, ...the p-well 6p and n-well

6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration NW) of the epitaxial layer 2E."); Section X.A.1.f (discussing graded dopants in p-well 6p); Ex. 1003, ¶102.

6. Claim 7: "The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

As shown below, the first (purple/light purple) and second active regions (green/light green) are separated by "field insulating film 3" (claimed "isolation region") (yellow). Ex. 1007, 8:40-52, 15:37-40, 17:62-18:8; Ex. 1008A, 818-20, FIG. 16-11(f); Ex. 1003, ¶103.



Ex. 1007, FIG. 23.

7. Claim 8: "The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process."

Kawagoe discloses that the graded dopants in n-well 6n and p-well 6p, and therefore in the channel region of the first and second active regions, are "formed by the ion implantation method." Ex. 1007, 4:11-12, 15:26-36, 15:62-16:2, 17:10-12, 17:31-39 (n-well 6n formed by implanting "ions of an n-type impurity such as phosphor"), 17:43-49 (p-well 6p formed by implanting ions of "a p-type impurity such as boron"); Section X.A.1.f; Ex. 1003, ¶104.

8. Independent Claim 9

a. Preamble: "A semiconductor device, comprising:"

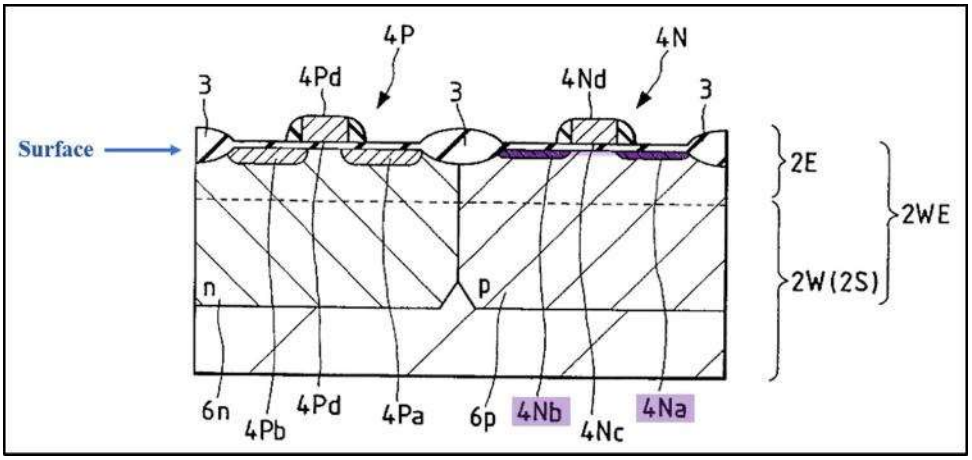
Section X.A.1.a

b. Element [9.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

Section X.A.1.b

c. Element [9.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

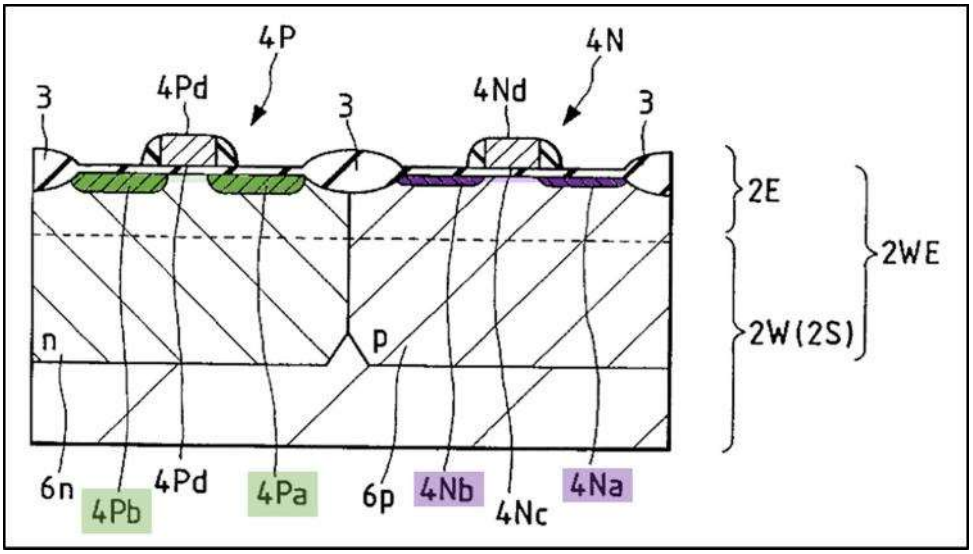
Section X.A.1.c. Kawagoe discloses nMOS transistor 4N formed in the surface of the first active region, as shown below. Ex. 1003, ¶107.



Ex. 1007, FIG. 23.

d. Element [9.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

Section X.A.1.d. Kawagoe discloses pMOS transistor 4P formed in the surface of the second active region, as shown below. Ex. 1003, ¶108.



Ex. 1007, FIG. 23.

e. Element [9.4]: "transistors formed in at least one of the first active region or second active region; and"

Section X.A.1.e.

f. Element [9.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate."

Section X.A.1.f.

9. Claim 10: "The semiconductor device of claim 9, wherein the substrate is a p-type substrate."

Section X.A.2.

10. Claim 12: "The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

Section X.A.3.

11. Claim 13: "The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices."

Section X.A.4.

12. Claim 14: "The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant."

Section X.A.5.

13. Claim 15: "The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region."

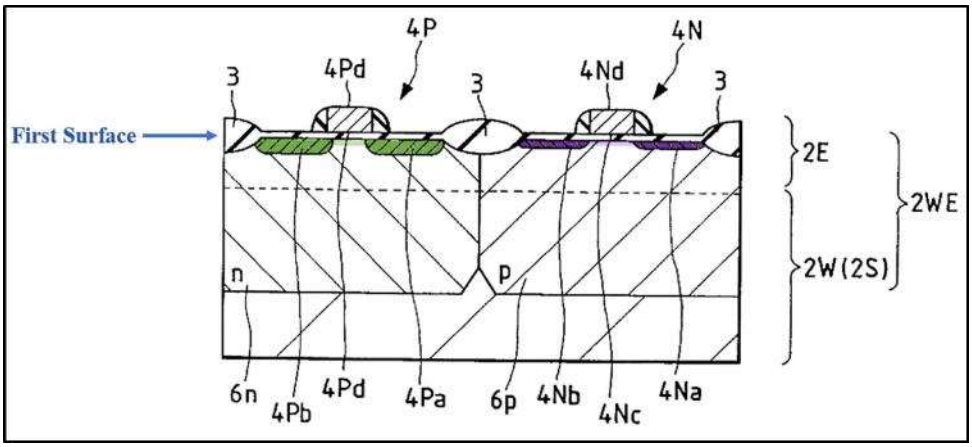
Section X.A.6.

14. Claim 16: "The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process."

Section X.A.7.

15. Claim 17: "The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

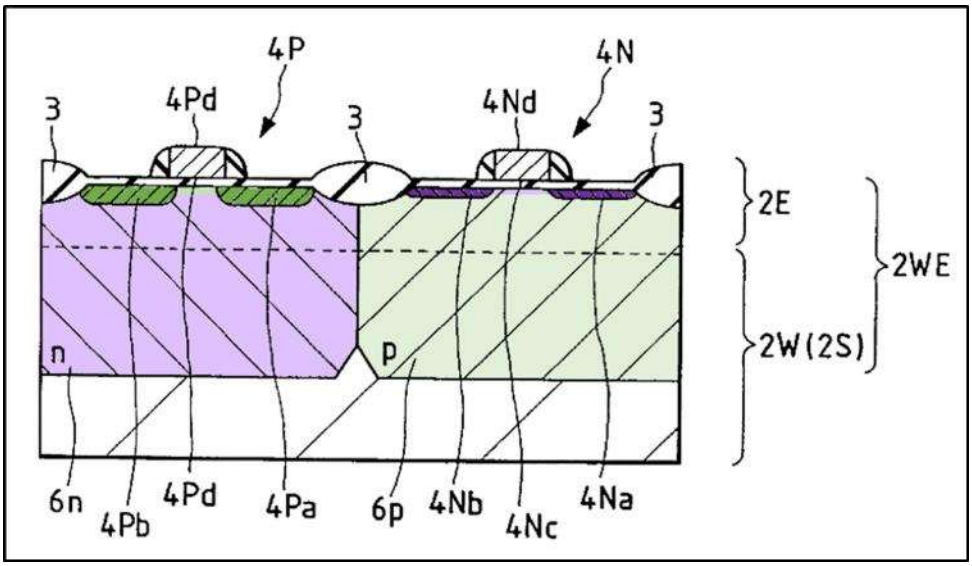
As shown below, Kawagoe discloses that the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex. 1007, 8:66-9:6, 9:47-54, 15:37-40, 17:10-12, 17:31-18:35; Ex. 1003, ¶117; Ex. 1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions...."), 298, 300-301, FIG. 5-2; Sections X.A.1.c-d.



Ex. 1007, FIG. 23.

16. Claim 18: "The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region."

Kawagoe teaches nMOS transistor 4N formed in the first active region and pMOS transistor 4P formed in the second active region, which are CMOS transistors. Ex. 1007, 8:45-52, 14:46-55, 15:37-40; Ex. 1003, ¶118.



Ex. 1007, FIG. 23. Each of the CMOS transistors includes a source, drain, gate, and channel region. Ex. 1003, ¶119. The nMOS transistor 4N includes "source-drain regions" 4Na/4Nb spaced apart by an "n-channel" region, and gate electrode 4Nd, and pMOS transistor 4P includes "source-drain regions" 4Pa/4Pb spaced apart by a "p-channel" region, and gate electrode 4Pd. Ex. 1007, 8:42-67, 9:41-48, 14:46-55, 15:37-40, FIG. 23; Ex. 1003, ¶119; Sections X.A.1.c-d, X.A.1.f.

B. Ground II:

Wieczorek in combination with Wolf renders claims 1-3, 5-11, and 13-18 obvious. Ex. 1003, ¶¶120-166. A POSITA would have been motivated to combine Wieczorek with Wolf. *Id.*, ¶¶121-122. This Petition relies on Wieczorek's description of a conventional prior-art CMOS device. Ex. 1006, [0020]-[0021], [0004] ("Field effect transistors, such as MOS transistors, represent one of the most frequently used circuit elements in modem [*sic*] integrated circuits."), [0007]-[0008] (describing "[a] typical process flow for forming the semiconductor device 100" which is "a complementary MOS transistor pair"), [0012], FIG. 1b. Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices. *See generally* Ex. 1008A; *id.*, Chapter 16 ("CMOS Process Integration"); Ex. 1003, ¶122. A POSITA would have therefore understood and expected that the teachings of Wolf would apply to Wieczorek's conventional CMOS device. *Id*. A POSITA would have looked to Wolf for additional details related to conventional CMOS devices, as further detailed below. *Id*.

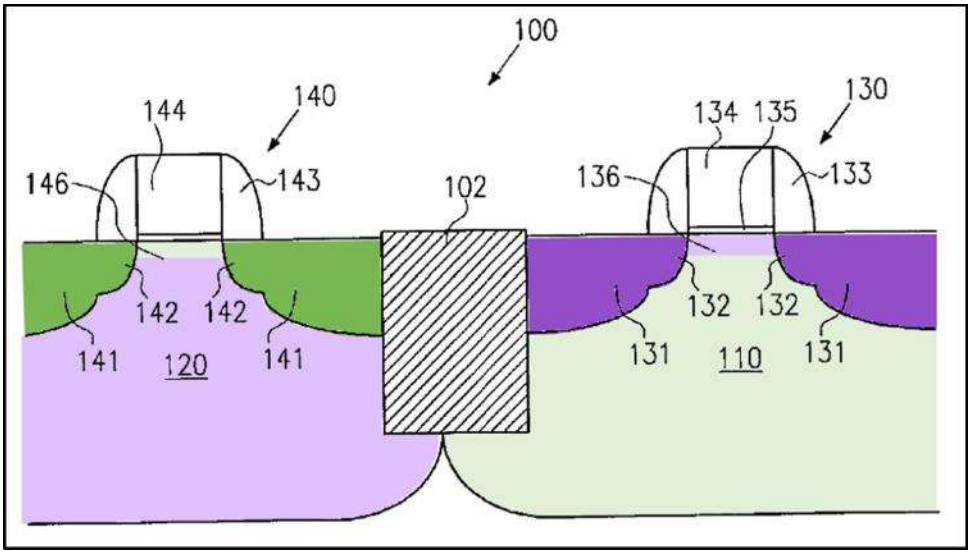
1. Independent Claim 1

a. Preamble: "A semiconductor device, comprising:"

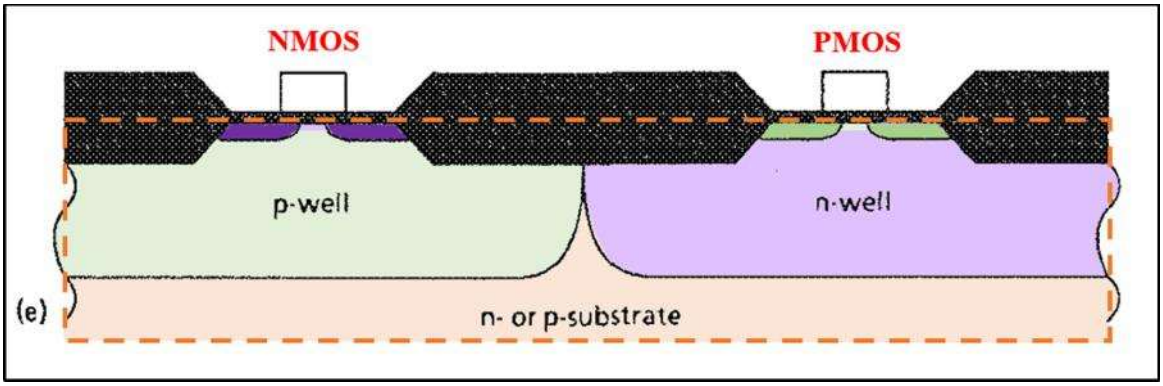
Wieczorek teaches a "semiconductor device 100." Ex. 1006, [0012]; Ex. 1003, ¶123.

b. Element [1.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

Wieczorek in combination with Wolf (hereinafter, "Wieczorek-Wolf") renders this element obvious. Ex. 1003, ¶¶123-129. Wieczorek's Figure 1b illustrates a conventional twin-well CMOS device, in which N-channel transistor 130 (nMOS) with source/drain regions 131-132 (purple) and channel region 136 (light purple) is formed in P-well 110 (light green) and P-channel transistor 140 (pMOS) with source/drain regions 141-142 (green) and channel region 146 (light green) is formed in N-well 120 (light purple). Ex. 1006, [0007], [0012], [0020]-[0021]; Ex. 1008C, 525, FIG. 8-1(e); Ex. 1003, ¶124.



Ex. 1006, FIG. 1b (labelled "Prior Art"). A POSITA would have understood that a twin well (or twin-tub) approach "is independent of starting material type" for the substrate. Ex. 1008C, 524; Ex. 1006, [0004] (discussing use of "an appropriate substrate" for forming MOS transistors without further specificity); Ex. 1003, ¶125. Because Wieczorek does not specify what constitutes an appropriate substrate, a POSITA would have been motivated to consult Wolf, which confirms that a "***uniform***, lightly doped *p*- or *n*-type substrate" is a suitable substrate commonly used in twin-well CMOS devices. Ex. 1008C, 523, 530 ("With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate ... of *n* or *p* material."); Ex. 1008B, 387-389; Ex. 1003, ¶126.

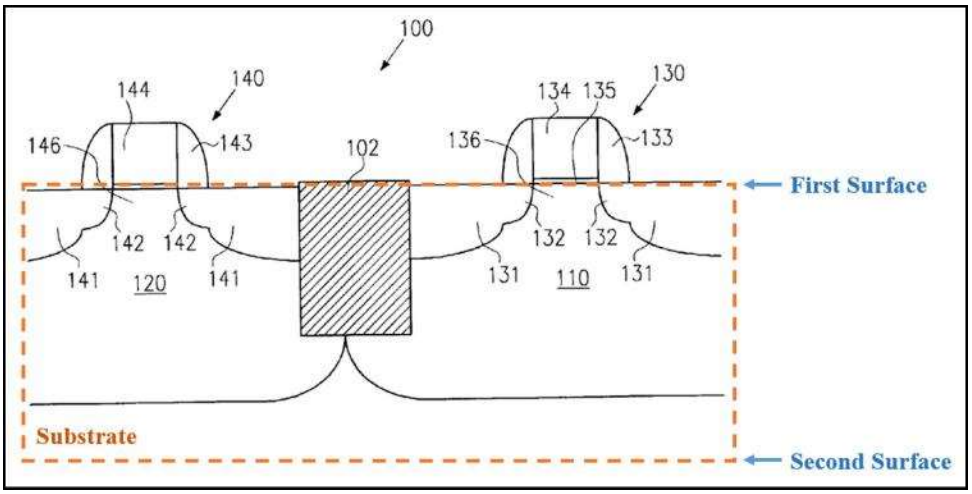


Ex. 1008C, 525, FIG. 8-1(e) ("twin-well CMOS on *n*- or *p*-substrate").

Thus, consistent with Wieczorek's teaching, a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ("a substrate of a first doping type at a first doping level") as a suitable substrate for Wieczorek's CMOS device in Figure 1b. Ex. 1003, ¶127. Doing so would amount to combining known prior art elements (*i.e.*, the use of a uniform, lightly doped n- or p-type substrate with Wieczorek's process for forming a conventional CMOS device) according to known methods (*i.e.*, the known use of an "appropriate substrate" for the conventional process of forming the CMOS device in Wieczorek [0007]-[0013]) to obtain predictable results (*i.e.*, the conventional CMOS device in Wieczorek's Figure 1b). Ex. 1003, ¶127. Doing so would have also been obvious to try because it involves nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device like Wieczorek's. *Id*. There would have been reasonable expectation of success

because Wolf shows that a POSITA would have known how to use a uniformly doped n- or p-type substrate to form a twin-well CMOS device similarly as described in Wieczorek. *Id*.

For purpose of claim mapping, Wieczorek-Wolf's substrate is taken as a p-type nonepitaxial substrate, which has the advantage of lower cost compared to an epitaxial substrate. Ex. 1003, ¶128; Ex. 1008A, 816 ("in twin-well CMOS the starting material is also ***either*** a lightly *p*-doped wafer (***p-bulk wafer***, Fig. 16-7a), or a heavily *p*-doped wafer on which a thin, lightly *p*-doped epi layer is grown" and noting the cost disadvantage of epitaxial wafers), FIG. 16-7. Consistent with the teachings of Wolf, Wieczorek's substrate (orange dotted line) in Figure 1b below, has a top surface ("first surface") and a bottom surface ("second surface"). Ex. 1008B, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e); Ex. 1003, ¶128.



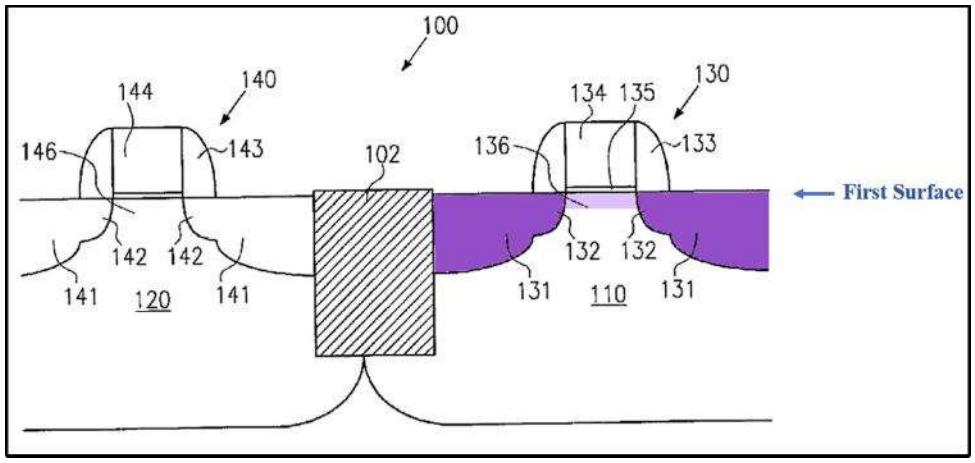
Ex. 1006, FIG. 1b.

Wieczorek-Wolf satisfies element [1.1] under Patent Owner's plain meaning construction and under Petitioner's proposed construction because Wieczorek-Wolf's substrate is the initial material within which or on which Wieczorek's "semiconductor device 100" is fabricated. Section VIII; Ex. 1006, [0004], [0012]; Ex. 1003, ¶129.

c. Element [1.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"

Wieczorek-Wolf renders obvious this element. Ex. 1003, ¶¶130-134. Wieczorek discloses "an N-channel transistor 130" that includes "heavily N-doped ***source and drain regions*** 131, including lightly doped extensions 132," and "***channel region*** 136." Ex. 1006, [0012]-[0013]; *id.,* [0004] ("[A] field effect transistor comprises two highly doped semiconductor regions...referred to as ***drain and source regions***, and which are embedded in a lightly and inversely doped semiconductor region, the so-called N-well or P-well ... The drain and source regions are spaced apart with a ***channel region*** interposed, wherein a conductive channel forms between the drain and source regions in the channel region" when the transistor is active). The source-drain regions 131-132 (purple) form part of the claimed first active region, which also includes channel region 136 (light purple)

between them. Ex. 1006, [0012]; Ex. 1003, ¶130; Ex. 1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e). As shown in Figure 1b, nMOS transistor 130 is formed in the first active region, which is adjacent the first surface of the substrate. Ex. 1003, ¶130.

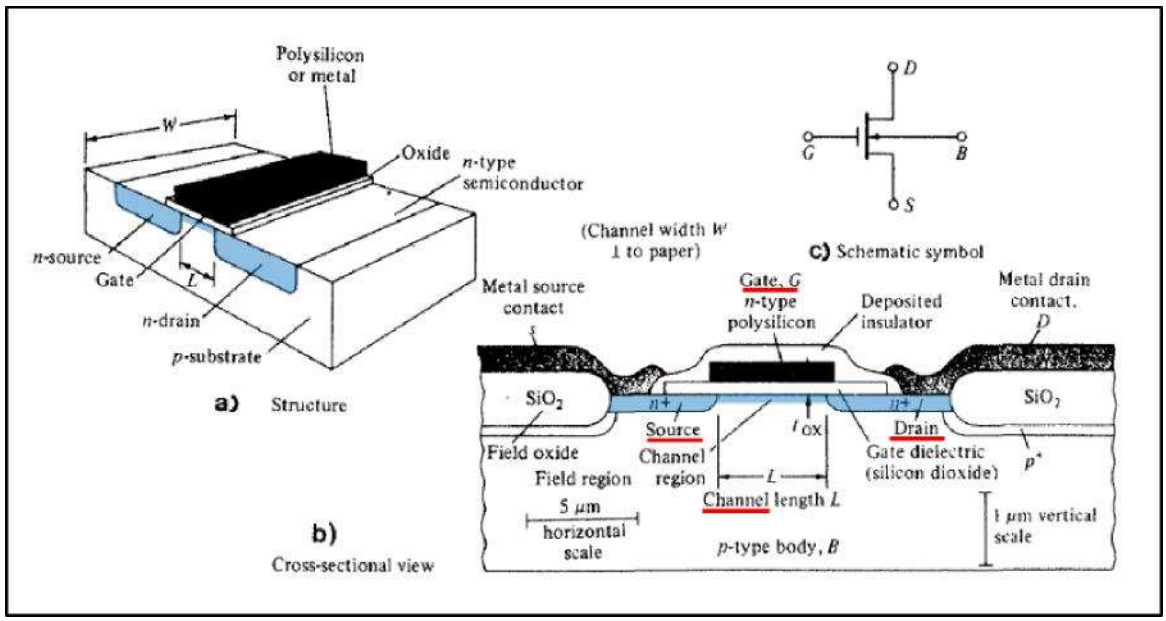


Ex. 1006, FIG. 1b, [0007]. Because the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-type) opposite in conductivity to the first doping type (P-type) of the substrate. Ex. 1006, [0012]; Ex. 1003, ¶131.

While Figure 1b illustrates a single exemplary nMOS transistor 130 formed in the first active region, a POSITA would have understood that Wieczorek teaches

forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates. Ex. 1006, [0004]; Ex. 1003 ¶132; Ex. 1014, 1:5254, 2:17-21. In any event, according to Patent Owner, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex. 1020, 31.

Wieczorek satisfies element [1.2] under Patent Owner's construction that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex. 1020, 20; Section VIII; Ex. 1003, ¶133. Indeed, the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions" (blue). Ex. 1008B, 299.

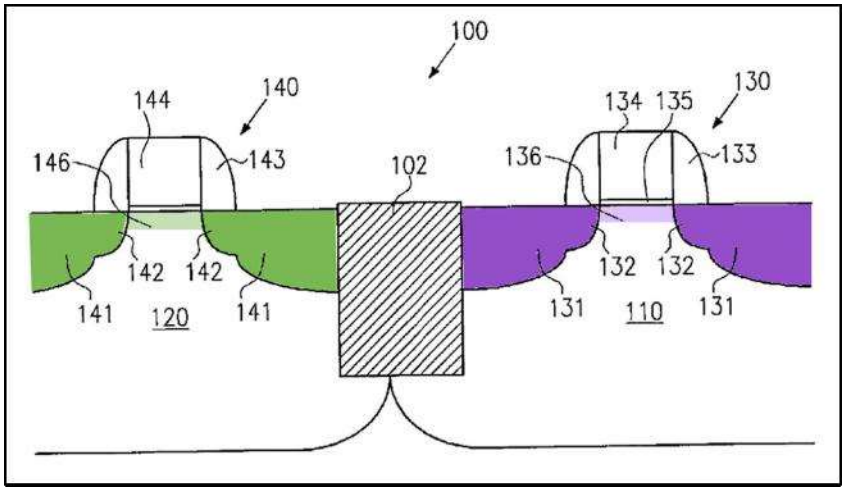


Ex. 1008B, FIG. 5-1; *id*., 298-301, FIGS. 5-2, FIG. 6-4. Wieczorek also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Section VIII; Ex. 1008B, 299-301; Ex. 1008D, 197, FIG. 5-13; Ex. 1003 ¶134. Patent Owner does not dispute this. Ex. 1020, 3-4 ("when a positive voltage is applied to the gate ... a ***conductive channel*** [is formed] between the ***source*** and the ***drain***, and ***current*** can begin to flow through the transistor").

d. Element [1.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"

Wieczorek discloses "a P-channel transistor 140," including "heavily P-doped source and drain regions 141, including lightly doped extensions 142," and "channel region 146." Ex. 1006, [0004], [0007], [0012]-[0013]; Ex. 1003, ¶¶135-138. The source and drain regions 141-142 (green) are part of the claimed second active region, which also includes channel region 146 (light green) between them. Ex. 1006, [0012]; Ex. 1008B, 298-301, FIGS. 5-1, 5-2, 6-4; Section X.B.1.c; Ex. 1003, ¶135. As shown in Figure 1b, pMOS transistor 140 is formed in the second active

region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex. 1006, [0012]; Ex. 1003, ¶136. Adjacent active regions are separated by an isolation region (*e.g.,* shallow trench isolation 102). Ex. 1006, [0007]; Ex. 1008A, 818-20, FIG. 16-11(f); Ex. 1001, Cl. 7; Ex. 1003, ¶136; Section X.A.1.d.



Ex. 1006, FIG. 1b, [0007].

While the figure shows an exemplary pMOS transistor 140 formed in the second active region, a POSITA would have understood that Wieczorek teaches forming multiple pMOS transistors in the second active region. Ex. 1006, [0004]; Ex. 1003, ¶137; Section X.B.1.c. Regardless, according to Patent Owner, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex. 1020, 31.

Wieczorek satisfies element [1.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Section X.B.1.c. Ex. 1003, ¶138. Wieczorek also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device." *Id*.

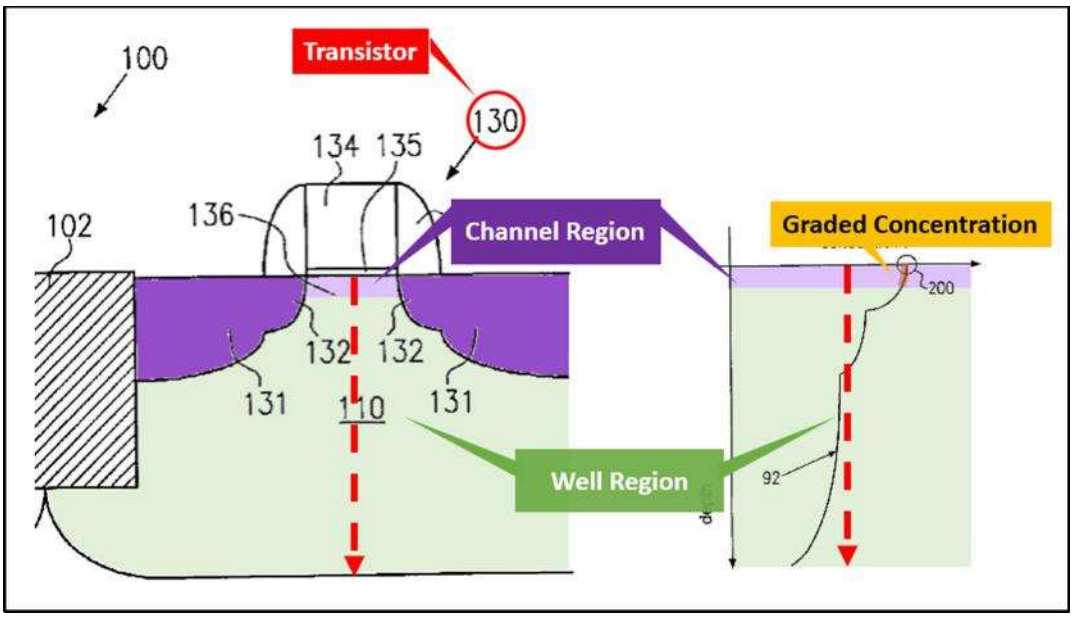
e. Element [1.4]: "transistors formed in at least one of the first active region or second active region; and"

Sections X.B.1.c-d.

f. Element [1.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate."

Wieczorek-Wolf renders obvious this element. Ex. 1003, ¶¶140-145. In Figure 1b (below left), the channel region 136 (light purple) of nMOS transistor 130, formed at the top surface of the substrate, is a portion of the first active region. Ex. 1006, [0012]-[0013], [0004] ("The drain and source regions are spaced apart with a ***channel region*** interposed"); Ex. 1008B, 298-301 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the

channel and the heavily doped ***source and drain*** regions."), FIG. 5-2; Ex. 1003, ¶140.

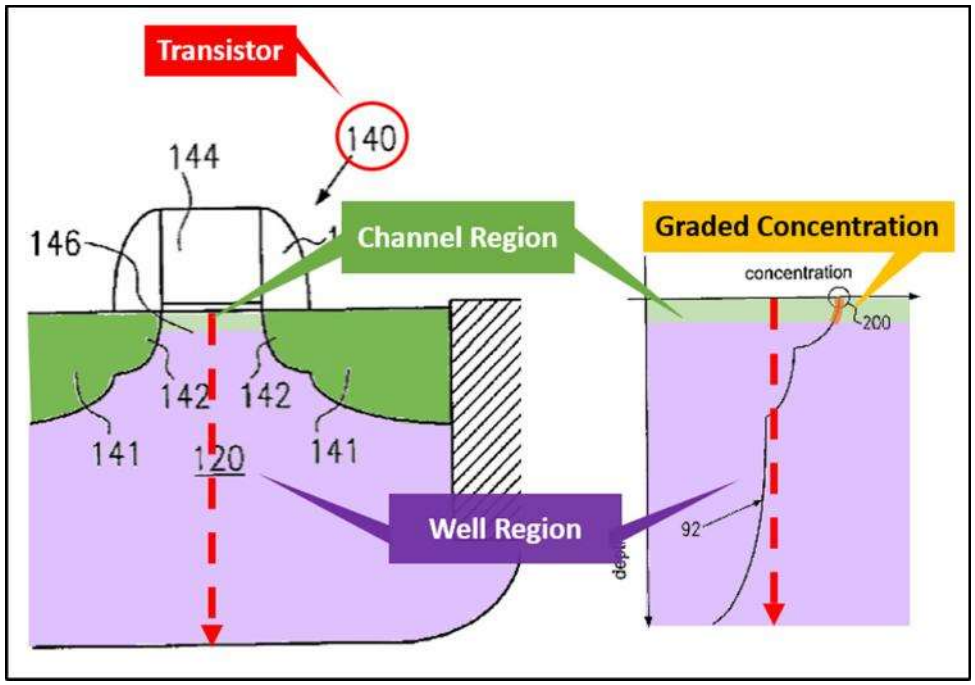


Ex. 1006, FIGS. 1b, 2b. The doping concentration in the channel region is highlighted in brown in the doping profile of Figure 2b (above right), which is measured for example along the red dotted line in Figure 1b that traverses the channel region. *Id*., [0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110/120]."), [0013] ("after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in FIG. 2b."), [0009], FIG. 2a.

As Figure 2b shows, the dopant concentration is highest at the surface of the substrate and decreases with depth. Ex. 1003, ¶141. Therefore, the channel region 136 has a graded dopant concentration. *Id*. As shown in Figure 2b above,

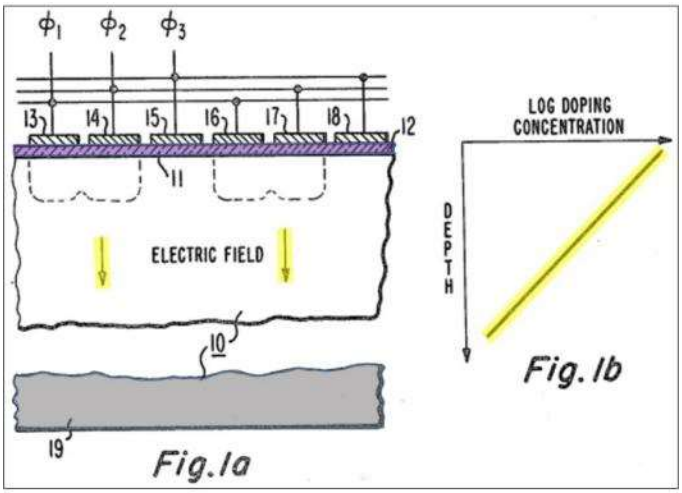
Wieczorek's graded dopant concentration is in fact downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region (light purple) and the underlying well-region (P-well 110) (green). Ex. 1006, [0011], Ex. 1003, ¶141.

And as shown in the figures below, Wieczorek teaches that the channel region 146 (light green) of pMOS transistor 140, which is a portion of the second active region, also has a graded dopant concentration for the same reasons. Ex. 1006, [0004], [0009], [0011]-[0013], FIGS. 2a-2b; Ex. 1008B, 298-301, FIG. 5-2; Ex. 1003, ¶141.



Ex. 1006, FIGS. 1b, 2b. Thus, Wieczorek discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex. 1006, [0009], [0011], [0013]; Ex. 1003, ¶141.

Further, Wieczorek's downward-sloping graded dopant concentration aids carrier movement from the first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. Ex. 1003, ¶¶142-143. As detailed in Section X.A.1.f, during prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to move carriers deep into the substrate. Applicant cited Jastrzebski and Kamins in support. Section X.A.1.f. Notably, according to Jastrzebski, a downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers ... ***deep into the substrate***[.]" Ex. 1010, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b.

In light of the above, Wieczorek satisfies element [1.5] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Section VIII; Ex. 1003, ¶144. According to Patent Owner, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)." Ex. 1020, 29. Also, according to Patent Owner, "when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...". *Id*., 2. Here, Wieczorek's Figure 2b shows that the dopant concentration is downward-sloping with increasing depth towards the bottom of the substrate, and thus, according to Patent Owner, this graded dopant concentration causes carriers to move deeper into the substrate as well. Ex. 1003 ¶144.

Wieczorek also satisfies Petitioner's alternative proposed construction that the term means "to sweep the carriers from the first surface to the second surface of the

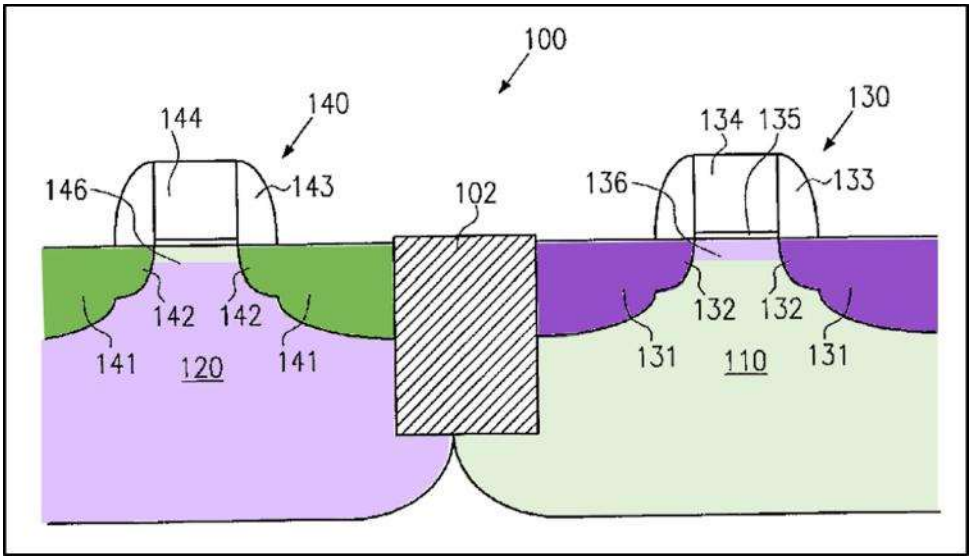
substrate." Section VIII; Ex. 1003, ¶145. Wieczorek's Figure 2b illustrates a downward-sloping graded dopant concentration in the channel regions and Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers into the substrate, as further detailed in Section X.A.1.f. Ex. 1016, 289-290.

2. Claim 2: "The semiconductor device of claim 1, wherein the substrate is a p-type substrate."

Section X.B.1b.

3. Claim 3: "The semiconductor device of claim 1, wherein the substrate is an n-type substrate.

As explained in Section X.B.1.b, n-type and p-type substrates are both suitable for Wieczorek's CMOS device. Section X.B.1.b; Ex. 1003, ¶147. With an n-type substrate, element [1.2] requiring "a first active region ... with a second doping type opposite in conductivity to the first doping type" of the substrate is met by mapping the first active region to the source/drain/channel regions 141/142/146 (green/light green) of pMOS transistor 140, and element [1.3] is met by mapping the second active region to the source/drain/channel regions 131/132/136 (purple/light purple) of nMOS transistor 130. *Id.*



Ex. 1006, FIG. 1b.

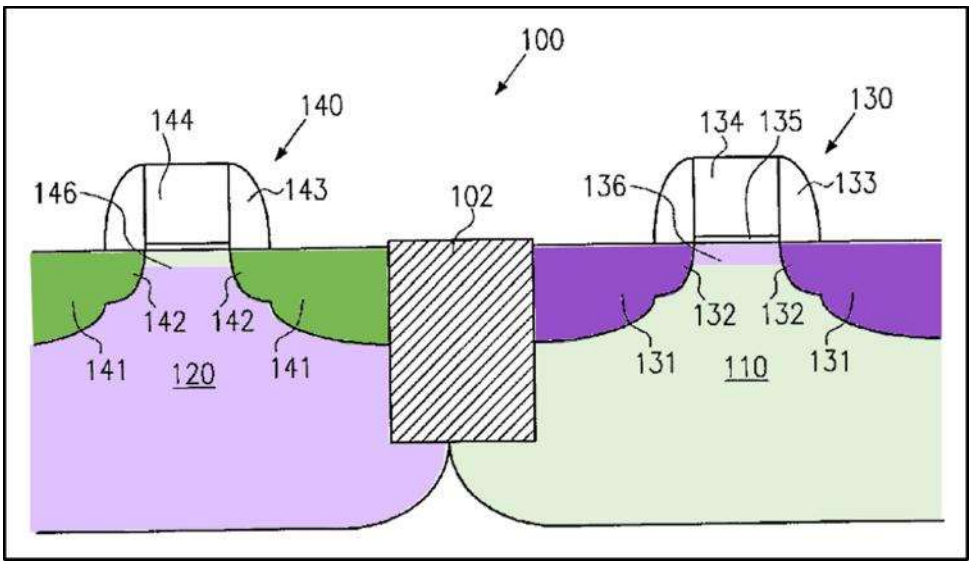
4. Claim 5: "The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices."

Sections X.B.1.c-e.

5. Claim 6: "The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant."

Wieczorek's Figure 1b illustrates a conventional twin-well architecture, whereby the first active region contains an "N-channel transistor 130" in "P-well" 110, and the second active region contains a "P-channel transistor 140" in "N-well" 120. Ex. 1006, [0012]-[0013], [0004]; Ex. 1003, ¶149; Sections X.B.1.c-d. This mapping satisfies this claim element under Patent Owner's interpretation that a claimed active region can contain "***a transistor***." Ex. 1020, 31; Ex. 1003, ¶149. A

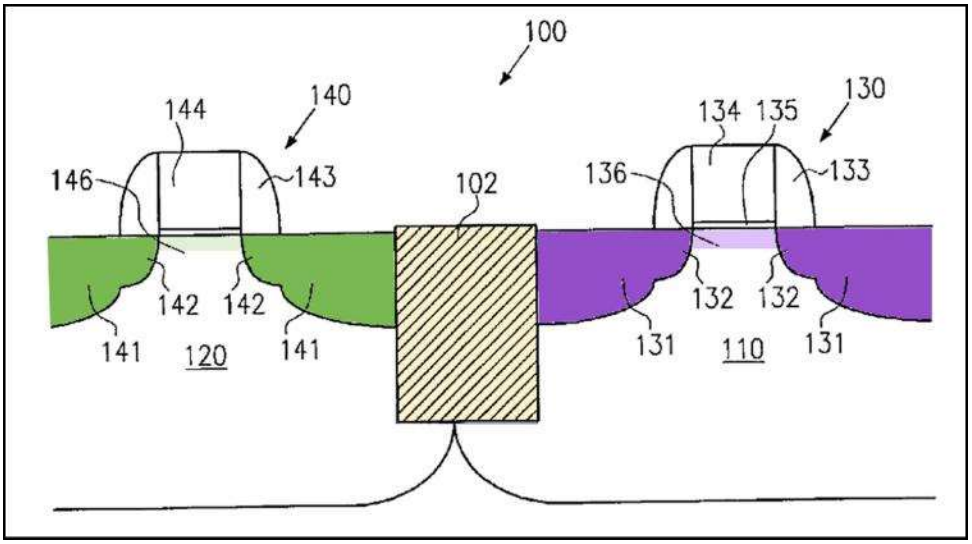
POSITA would have also understood that Wieczorek teaches forming multiple transistors in an active region to save chip area. Ex. 1003, ¶149.



Ex. 1006, FIG. 1b. Further, Wieczorek's wells have a graded concentration of dopants. Ex. 1006, [0009]-[0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110/120]."), [0013], FIGS. 2a-2b; Section X.B.1.f (discussing graded dopants in P-well 110); Ex. 1003, ¶149.

6. Claim 7: "The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

As shown below, the first (purple/light purple) and second (green/light green) active regions are separated by "shallow trench isolation 102" (yellow). Ex. 1006, [0007]; Ex. 1003, ¶150.



Ex. 1006, FIG. 1b.

7. Claim 8: "The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process."

Wieczorek teaches that the graded dopants in "P-well structure 110 and [] N-well structure 120," and therefore in channel regions 136 and 146 of the first and second active regions, "are defined by sequentially performed ion implantation processes." Ex. 1006, [0008], [0007]-[0012], FIGS. 1a-1b, 2a-2b; Ex. 1003, ¶151; Section X.B.1.f.

8. Independent Claim 9

a. Preamble: "A semiconductor device, comprising:"

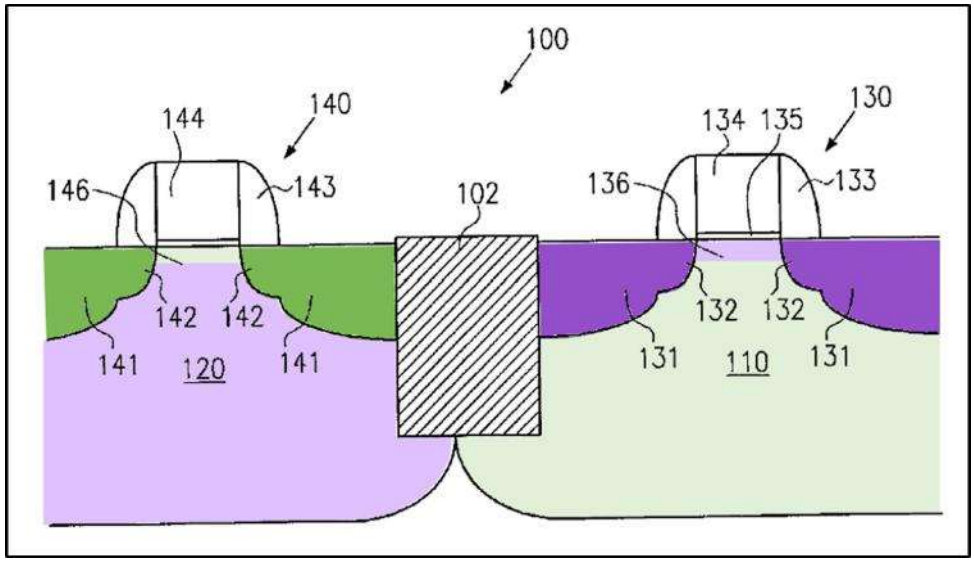
Section X.B.1.a.

b. Element [9.1]: "a substrate of a first doping type at a first doping level having first and second surfaces;"

Section X.B.1.b

c. Element 19.2]: "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;"

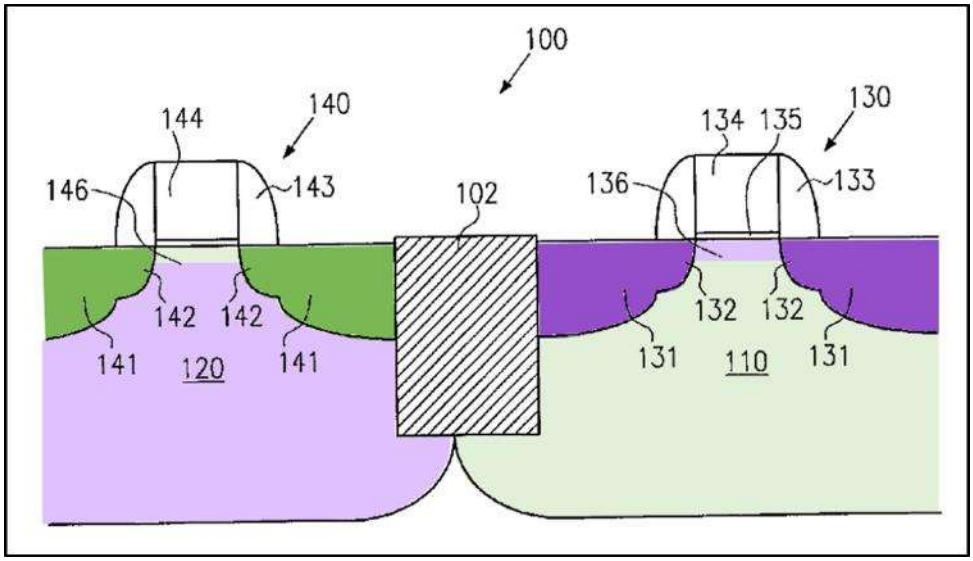
Section X.B.1.c. As shown below, Wieczorek discloses N-channel transistor 130 formed in the surface of the first active region. Ex. 1003, ¶154.



Ex. 1006, FIG. 1b.

d. Element [9.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;"

Section X.B.1.d. As shown below, Wieczorek discloses P-channel transistor 140 formed in the surface of the second active region. Ex. 1003, ¶155.



Ex. 1006, FIG. 1b.

e. Element [9.4]: "transistors formed in at least one of the first active region or second active region; and"

Section X.B.1.e.

f. Element [9.5]: "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate."

Section X.B.1.f.

9. **Claim 10: "The semiconductor device of claim 9, wherein the substrate is a p-type substrate."**

Section X.B.2.

10. **Claim 11: "The semiconductor device of claim 9, wherein the substrate is an n-type substrate."**

Section X.B.3.

11. **Claim 13: "The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices."**

Section X.B.4.

12. **Claim 14: "The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant."**

Section X.B.5.

13. **Claim 15: "The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region."**

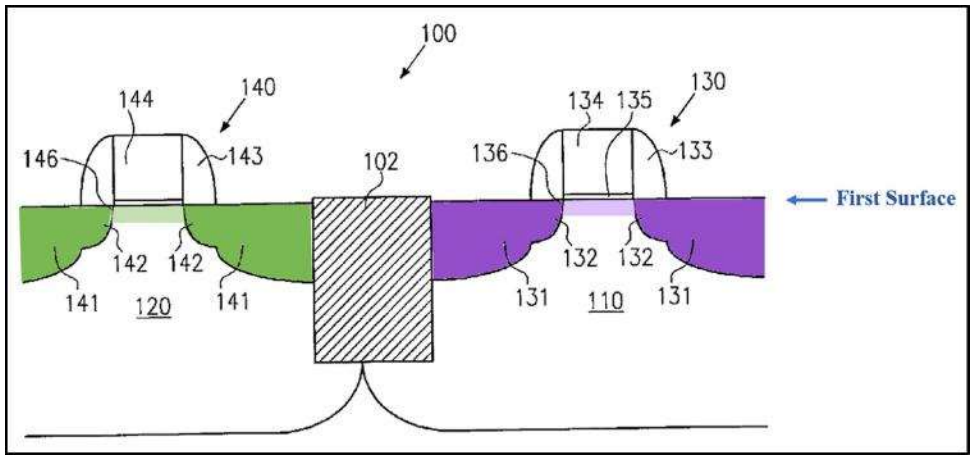
Section X.B.6.

14. **Claim 16: "The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process."**

Section X.B.7.

15. Claim 17: "The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

As shown below, the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex. 1006, [0007]-[0010], [0012]-[0013]; Ex. 1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions..."), 298-301, FIG. 5-2; Ex. 1003, ¶164; Sections X.B.1.c-d.

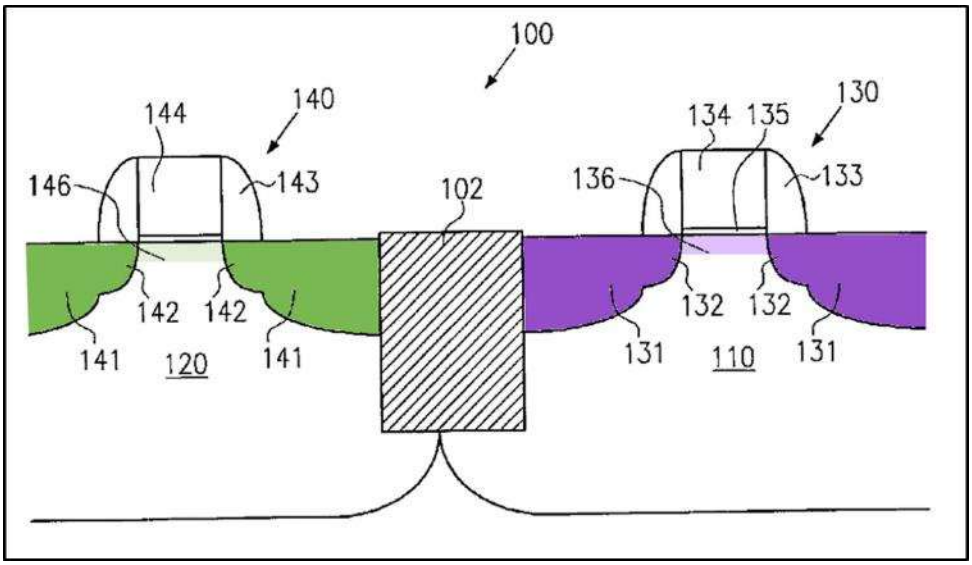


Ex. 1006, FIG. 1b.

16. Claim 18: "The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region."

Wieczorek discloses "a complementary MOS [(CMOS)] transistor pair" comprising "N-channel transistor 130" in the first active region (purple/light purple)

and "P-channel transistor 140" in the second active region (green/light green). Ex. 1006, [0007], [0012]-[0013]; Ex. 1003, ¶165.



Ex. 1006, FIG. 1b. Each of the CMOS transistors include a source, drain, gate, and channel region. Ex. 1003, ¶166. N-channel transistor 130 includes "heavily N-doped source and drain regions 131" (purple), "gate electrode 134," and "channel region 136" (light purple). Ex. 1006, [0012]-[0013]; Ex. 1003, ¶166. P-channel transistor 140 includes "heavily P-doped source and drain regions 141" (green), "gate electrode 144," and "channel region 146" (light green). *Id.*; Sections X.B.1.c-d, X.B.1.f.

C. GROUNDS III/IV

Several claim elements of the Challenged Claims recite "transistors" or "devices." *See* elements [1.2]-[1.4], [9.2]-[9.4] and claims 5, 6, 13, 14, and 18. As

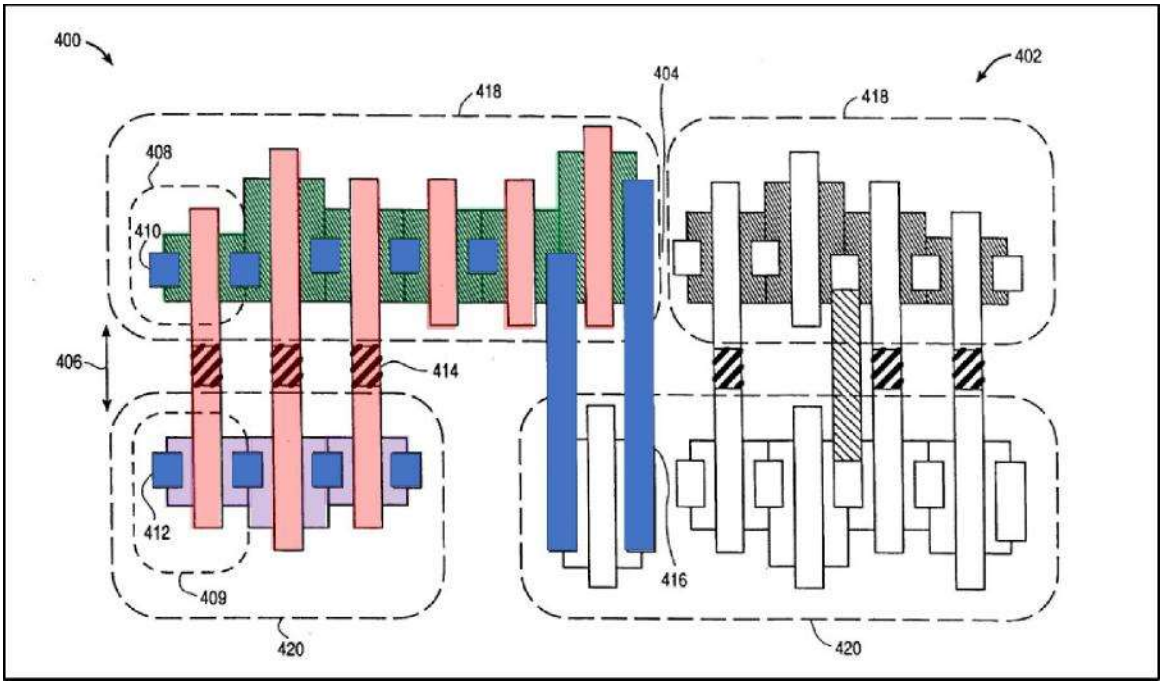
discussed under Grounds I and II, the Patent Owner interprets these claim elements as requiring one or more transistors, and not a plurality of transistors. Sections X.A.1.c-d, X.B.1.c-d. Notably, according to Patent Owner, an "active region ... within which ***transistors*** can be formed" means "an active region ... where ***a transistor*** can be formed." Ex. 1020, 31.

The present Grounds III and IV mirror grounds I and II, respectively, except that Gupta is explicitly combined with the ground references (Kawagoe of Ground I, Wieczorek-Wolf of Ground II) to render obvious those claim elements under an interpretation of "transistors" or "devices" to require a plurality of such devices. Ex. 1003, ¶168.

Gupta is directed to "automatically producing layouts for CMOS circuits," recognizing that "semiconductor chips [have] become ever larger, incorporating ever more devices." Ex. 1014, 1:7-10, 1:28-31. Wolf confirms that, at the time, various chips (e.g., DRAM, microprocessors, and flash memory) were fabricated with tens of millions to more than a billion devices. Ex. 1008A, xxxiii, FIG. 1; Ex. 1008B, 634. A "primary goal" of semiconductor chip development has therefore been to minimize the chip area required to form any circuit so that more transistors can be packed in the same chip, regardless of the technology and chip fabrication process. Ex. 1014, 1:28-35 ("[I]t becomes increasingly important to minimize semiconductor

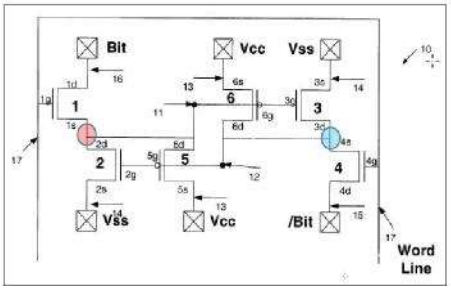
area used by a given number of devices. Conservation of semiconductor area is a primary goal in semiconductor chip development ....”); Ex. 1003, ¶169. Gupta further explains that good circuit layout practice dictates forming as many transistors in the same active region through diffusion abutment as possible, to minimize area-wasting diffusion gaps. Ex. 1014, 1:52-54 (“One technique conserves area by placing transistors so as to ***share diffusion area***.”), 2:17-21 (“Transistors which are abutted in a layout form transistor chains. It is desirable to produce a layout with a ***maximum number of transistors chained*** so as to minimize diffusion gaps.”); Ex. 1023, 5 (“An important layout task is to place and orient the transistors on the chip to ***minimize the layout area***” by avoiding “area-wasting diffusion gap[s]”). Gupta describes several techniques to perform this, such as transistor folding and chaining, to achieve an optimal layout. Ex. 1014, 1:49-2:24, 3:64-4:1, FIGS. 2-3.

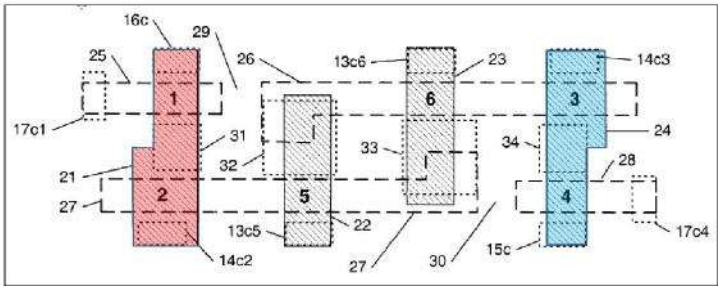
Gupta’s Figure 4 (below)—where transistor gates and metal contacts that overlay the active regions are colored red and blue, respectively—illustrates ***six*** chained PMOS transistors formed in a p-channel active region (green) and ***three*** chained NMOS transistors formed in an n-channel active region (purple). Ex. 1014, 4:12-43; Ex. 1003, ¶170.



Ex. 1014, FIG. 4.

Jin confirms that transistors arranged as in Gupta are formed in a common active region. Ex. 1003, ¶171. Below left is the circuit schematic of an SRAM cell, and the cell layout (below right) shows transistors 1 and 2 in active region 21 (red), and transistors 3 and 4 in active region 24 (blue). Ex. 1015, 6:17-29; Ex. 1025, 48 ("*Diffusion regions* (n^+ and p^+), which define the areas where transistors can be formed[,] are often called the *active areas*.") (italics in original).





Ex. 1015, FIGS. 1 and 2.

A POSITA would have been motivated to fabricate a CMOS chip according to the combined teachings of Kawagoe and Gupta (and likewise, of Wieczorek-Wolf and Gupta) to achieve high packing density (taught by Gupta) at submicron dimensions (for which a twin-well CMOS process of the type taught in Kawagoe and Wieczorek-Wolf was known to be the technology of choice (Ex. 1008B, 373, 388)). Ex. 1003, ¶172. The combinations gain the additional benefit of improved immunity to soft errors through appropriate well doping. Ex. 1007, 15:62-16:11; Ex. 1003, ¶173. Combining Gupta with Kawagoe or Wieczorek-Wolf merely amounts to (1) use of a known technique (*i.e.*, Kawagoe's or Wieczorek's CMOS fabrication process) to improve similar devices (*i.e.*, CMOS chips designed with Gupta's layout) in the same way (*i.e.*, to achieve submicron dimensions and improve immunity to soft errors); (2) use of a known technique (*i.e.*, Gupta's optimal layout generation) to improve similar devices (*i.e.*, submicron CMOS chips fabricated according to Kawagoe or Wieczorek-Wolf's CMOS fabrication process) in the same way (*i.e.*, to minimize chip area and increase packing density); and (3) combining prior art elements (*i.e.*, Kawagoe or Wieczorek's CMOS fabrication process and Gupta's CMOS layout generation) according to known methods (*i.e.*, as taught by Kawagoe or Wieczorek and Gupta). Ex. 1003, ¶173. There is reasonable expectation of success

with predictable results because Kawagoe's and Wieczorek's CMOS fabrication process would be used for their intended purpose of fabricating CMOS circuits according to known CMOS layouts generated by Gupta, which would also be used for its intended purpose. *Id*. Further, Gupta's optimal circuit layout is process-agnostic, and applies to the layout of ***any*** CMOS semiconductor chip, including the layout of CMOS chips fabricated according to the teachings of Kawagoe and/or Wieczorek-Wolf. *Id.*

A POSITA would have understood that, in such a combination, the active regions in Gupta's figures are formed in wells (n-channel active regions are formed in p-wells, and p-channel active regions are formed in n-wells), whereby the wells have downward-sloping graded dopant concentrations as shown in Kawagoe's Figure 17 and Wieczorek's Figure 2b. *Id.*, ¶174. The n-channel active region (purple) in Gupta's Figure 4 is an example of the claimed first active region, and the p-channel active region (green) is an example of the claimed second active region. Ex. 1003, ¶174. The two active regions are adjacent and separated by an isolation region (field oxide), as required under elements [1.3], [9.3] and claims 7 and 15. Ex. 1014, 1:16-19, 4:39; Ex. 1008A, 818-820; Sections X.A.1.d, X.A.6, X.B.1.d, X.B.6, Ex. 1003, ¶174.

Conversely, a POSITA would have understood that each of the active regions of Kawagoe's and Wieczorek's CMOS devices typically contain many transistors, as taught by Gupta and illustrated in Gupta's Figure 4. Ex. 1003, ¶175. This is the case whether the device is a DRAM, flash memory, logic device or CPU (as claimed in claims 14, 16-18, 33-35). *Id.* Each such device is a "very large scale integrated circuit" for which "it becomes increasingly important to minimize semiconductor area used[,]" and this requires forming as many transistors as possible in any active region. Ex. 1014, 1:13-14, 1:28-34, 2:17-21; Ex. 1003, ¶175.

In light of the above, Kawagoe in view of Gupta renders claims 1-2, 4-10, and 12-18 obvious (Ground III). Likewise, Wieczorek-Wolf in view of Gupta renders claims 1-3, 5-11, and 13-18 obvious (Ground IV). Ex. 1003, ¶¶167-176.

XI. THE BOARD SHOULD INSTITUTE IPR

The Board should decline to exercise its discretion to deny institution for several reasons.

First, the merits of this Petition are strong, which alone warrants institution. On June 21, 2022, the Director issued an interim procedure regarding application of the *Fintiv* factors (Interim Procedure) in which the Director clarified that "the PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling evidence of unpatentability." Director Vidal, Memorandum, "Interim Procedure for

Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation," 9 (June 21, 2022). Here, each ground in the Petition presents compelling evidence of unpatentability. As just one example, Ground I is a single-reference obviousness ground that explains how Kawagoe discloses or, at a minimum, renders obvious nearly all of the Challenged Claims. Further, none of the references presented in this Petition were before the Examiner during prosecution. This evidence, "if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable" (*Id.*, 4) and the Board must decline to exercise its discretion under §314(a) to deny institution. *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022-00938, Paper 8 (P.T.A.B. Nov. 1, 2022).

The *Fintiv* factors also weigh in favor of institution. ***First***, this Petition is substantially identical to the Petition filed in IPR2023-00308. The Petition in IPR2023-0308 was filed on December 5, 2022, an Institution Decision is expected on or before June 2023, and a final written decision (FWD) should issue in June 2024. Petitioner is filing a motion for joinder with respect to IPR2023-00308.

While trial in the District Court Case is set for December 2023, the Director noted in its Interim Procedure that "[a] court's scheduled trial date [] is not by itself a good indicator of whether the district court trial will occur before the statutory deadline for a [FWD]," and directed the PTAB to consider "statistics on median

time-to-trial for civil actions in the district court in which the parallel litigation resides." Interim Procedure, 8-9. The median time to trial in the Western District of Texas is 28.3 months (Ex. 1024, 37), giving a trial date of no earlier than June 2024.

Additionally, on December 27, 2022, the district court severed the claims against co-defendant Intel and transferred to the District of Oregon (*see* Section II), while staying Greenthread's claims against Dell based on the Accused Intel Products. Ex. 1036 at 22. The Markman hearing was rescheduled twice before the scheduled January 19th, 2023 hearing was canceled, without any indication if or when it would be rescheduled. Ex. 1037. Dell also has a pending motion to transfer venue, and Plaintiff filed an amended complaint on January 23, 2023 adding additional defendants, both of which may result in further delays to the existing schedule.

Second, fact discovery only recently opened in the District Court litigation, and the claims against Dell based on the Accused Intel Products have been stayed. No Markman date is scheduled. Because the district court has not yet invested significant resources this factor weighs against discretionary denial. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 13 (P.T.A.B. May 19, 2021).

Third, "there is a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial." *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-00339, Paper 21 at 18 (P.T.A.B Sept. 10, 2020).

Fourth, the Board should give little weight to the fact that Petitioner is a defendant in the District Court Case. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, IPR2020-01684, Paper 16 at 11-13 (P.T.A.B April 14, 2021).

Finally, "other circumstances" weigh against discretionary denial. Where, as here, "the information presented at the institution stage presents a compelling unpatentability challenge, that determination alone demonstrates that the PTAB should not discretionarily deny institution under *Fintiv*[.]" Interim Procedure, 4-5.

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *see also Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020).

The Board has consistently "held that a reference that 'was neither applied against the claims nor discussed by the Examiner' does not weigh in favor of exercising ... discretion under §325(d)." *Fasteners for Retail, Inc. v. RTC Indus.,*

Inc., IPR2019-00994, Paper 9 at 7-11 (P.T.A.B. Nov. 5, 2019). Here, the prior art references (Kawagoe, Wieczorek, Wolf and Gupta) are not cited in the '842 Patent, and the arguments presented herein are not the same or substantially the same as those considered during prosecution of the '842 Patent. Kawagoe is in fact not cited in any patent related to the '842 Patent. Wieczorek was first disclosed (but not discussed) during prosecution of a later-filed application, after the '842 Patent was allowed. Ex. 1033, 5. Additionally, none of the grounds in this Petition rely on prior art that was evaluated during prosecution of the '842 Patent. The Examiner improperly concluded that the Challenged Claims were not obvious because the Examiner did not have the opportunity to consider the prior art and grounds detailed in this Petition. *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5 (P.T.A.B. Aug. 6, 2019).

Wieczorek and Kawagoe are also not cumulative of references considered during prosecution of the '842 Patent. Hong, the only reference mentioned during prosecution of the '842 Patent, is not prior art because it was filed on August 31, 2005, long after the claimed priority date of the '842 Patent. Ex. 1027. Further, Wieczorek and Kawagoe are not cumulative to any art cited or discussed during prosecution of the '842 Patent's parents, such as Rhodes, Jastrzebski, Kamins or Hueting. Indeed, prosecution of the parent applications involved claims that are

wholly different from the Challenged Claims. *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 10 (P.T.A.B. Nov. 5, 2019) (refusing to deny institution because, despite allegation that the petition art was considered during prosecution of claims related to the challenged claims, "enough differences exist [between the two sets of claims] to convince us that the challenges presented in this petition are not cumulative to those already considered by the examiner."). Most significantly, none of the claims prosecuted in the parent applications claim graded dopants ***in an active region*** to aid carrier movement "***to the second surface of the substrate***" as claimed in Claim 1. For example, the claims of the parent '070 Patent are directed to bipolar transistors (not at issue in the District Court Case or in the present Petition) and claim aiding carrier movement "to a collector in the substrate," and not "to the second surface of the substrate." Ex. 1034, Cl. 1; Ex. 1003, ¶46. Other claims that claim graded dopant in an active region were withdrawn prior to substantive examination. Ex. 1016, 73 (withdrawing claims 1-2); Ex. 1028, 9 (same); Ex. 1029, 7 (canceling claims 1-2); Ex. 1030, 18 (same); Ex. 1003, ¶46. "Here, the Examiner did not consider [] the grounds asserted in the Petition, and certainly not with respect to the challenged claims" and therefore "there [is] no overlap between arguments made during examination and in the Petition." *Bowtech*, Paper 14 at 5-6.

A. The Sony Petition Does Not Warrant Denying Institution

The instant Petition is Dell's first petition challenging claims of the '842 Patent. On December 17, 2022, Sony filed a petition challenging claims 1-18 of the '842 Patent. *See Sony Group Corp. v. Greenthread LLC*, No. IPR2023-00376, Paper 1 (P.T.A.B. Dec. 17, 2022). Previously, Intel likewise filed a petition challenging claims 1-18 of the '842 Patent. *See Intel Corp. v. Greenthread LLC*, No. IPR2023-00308, Paper 1 (P.T.A.B. Dec. 5, 2022). The instant Petition is identical to the Intel Petition in substance, while being substantively different than the Sony petition. Dell is concurrently filing a motion for joinder to join the first Intel IPR filed on the '842 Patent – IPR2023-00308. *See* Dell's concurrently filed motion for joinder; IPR2023-00308.

The instant Petition should not be denied in view of the relationship between Sony and Dell. While Sony listed Dell as an RPI in IPR2023-00376, the two are unrelated companies, and have not funded, reviewed, or directed either's IPR filings. Dell further has other interests to protect due to other accused Dell products that are not provided by Sony. The prior art and grounds of this Petition do not overlap in any way with the prior art and grounds of the Sony petition. Finally, neither the Board nor the Patent Owner have substantively addressed the Sony Petition removing any potential that Dell is using the Sony case as a roadmap.

Furthermore, this Petition relies on the ***same*** prior art and grounds as in related Intel IPR2023-00308 which Dell seeks to join. Intel filed the IPR2023-00308 petition on December 5, 2022—***ahead of*** the Sony Petition directed to the same patent. In light of the foregoing, *General Plastic* factors weigh strongly against discretionary denial. *Xilinx, Inc. v. Arbor Global Strategies, LLC*, IPR2020-01568, Paper 12 at 10 (P.T.A.B. Mar. 5, 2021).

Dated: January 27, 2023

Respectfully submitted,

/ Christopher TL Douglas /
Christopher TL Douglas
Counsel for Petitioner Reg. No. 56,950

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,510,842 contains, as measured by the word-processing system used to prepare this paper, 12,042 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: January 27, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE ON PATENT OWNER UNDER 37 C.F.R. § 42.105

I hereby certify that on January 27, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,510,842 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center

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A courtesy copy was also served via electronic mail on Patent Owner's counsel of record in Western District of Texas litigation:

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