Travis N. Blalock

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Education:

Auburn University, Ph.D., July 1991. Major emphasis on CMOS analog and digital IC design. Dissertation - *Design of Very High Speed Sense Amplifiers for CMOS Random Access Memory*.

University of Tennessee, M.S.E.E., December 1988. Major emphasis on analog and digital circuit design. Thesis - *Development of a Radiation Hardened 600 Watt Switchmode Power Converter*.

University of Tennessee, B.S.E.E. with High Honors, January 1985. Senior year specialization in analog circuit design.

Work Experience:

8/17 – Founder, River Rock Engineering, primary activities are technical, startup, and IP consulting.

9/13 – 7/17 Fellow, Analogic Inc. Joined Analogic via acquisition of PocketSonics startup. Chief architect for handheld medical ultrasound imaging systems. This included leading a team and directing system architecture, fully custom CMOS integrated front-end circuit design, software architecture and interfaces, and overall product approach. This effort led to an FDA approved, hand-held, battery powered, 6000 channel, 3D imaging system targeted for vascular access applications.

8/98 – Associate, Professor, University of Virginia. Research in mixed-signal CMOS integrated circuit design. Principle focus areas are integrated imaging and signal processing, smart sensors, low-voltage low-power RF and baseband design, and analog design techniques in 'digital' processes. Developing and teaching courses in analog and mixed-signal integrated circuit design. Moved to non-resident appointment in the Fall of 2013 upon joining Analogic. Currently engaged in low power RF research.

1/04 – 9/13 Co-Founder, CEO, and CTO, PocketSonics, Inc. Built medical device startup based on unique ultrasound imaging architecture. Invented or co-invented several unique ultrasound imaging technologies. Negotiated University licensing, created business structure, hired long-term CEO, and led technical development of a handheld 3D volume capable ultrasound imaging system, including fully-custom CMOS integrated circuit front-end, and an industry unique signal processing stack, leading to partnership with and later acquisition by Analogic, Inc.

8/96 - 8/98 Principal Scientist, Hewlett-Packard Laboratories. Technical lead on multiple mixed-signal optoelectronic image capture, processing, and display IC designs. Extensive transistor level design of analog and digital CMOS circuits. Exploration of new technologies and mentoring of other engineers. Development of modeling software and

custom CAD tools for circuit analysis and design. Led IC designs in optical sensing and navigation, optical mouse, disk drive read channels, and microdisplays.

7/91 - 8/96 Member Technical Staff, Hewlett-Packard Laboratories. Designed CMOS mixed signal processing integrated circuits for mass storage products. Principal architect and designer of new integrated optoelectronic image acquisition and processing IC. This chip was the principal enabler of several new HP products.

3/88 - 7/91 Graduate Research Assistant, Auburn University. Developed high speed CMOS sense amplifier topologies for memory circuits. Also developed memory circuits optimized for quasi-static low temperature operation. Test circuits were fabricated and experimental results published.

3/88 - 7/91 Graduate Teaching Assistant, Auburn University. Served as instructor teaching junior and senior level electronics courses. Student teaching effectiveness average rating of 4.5/5.0 for last recent four quarters. Total teaching experience of 11 quarters.

9/86 - 3/88 Graduate Research Assistant, University of Tennessee. Designed and implemented radiation hardened switchmode power supply. Addressed key stability issues with extensive computer simulation techniques.

2/85 - 8/86 Development Engineer, NASA Langley Research Center, Hampton, VA. Developed measurement techniques and instrumentation for the characterization of composite materials.

9/84 - 1/85 Assistant Engineer, Control Technology Inc., Knoxville, TN, part-time while attending school, 25-30 hrs/week. Developed firmware and hardware for industrial controller peripherals.

9/82 - 12/83 Assistant Engineer, Technology for Energy Corporation, Knoxville, TN, part-time while attending school, 25 - 30 hrs/week. Developed graphics software for nuclear power system monitoring.

Consulting & Other Work:

5/22 - Expert Witness, TCL Electronics Holdings Limited, TTE Technology, Inc., TCT Mobile (US) Inc., and TCL Communication Limited, Patents and document analysis, Kirkland & Ellis LLP, Integrated circuits.

11/21 - 5/22 Expert Witness, Intel, Patents and document analysis, reports, Kirkland & Ellis LLP, Integrated circuits.

11/21 - 5/22 Expert Witness, Samsung, Patents and document analysis, Kirkland & Ellis LLP, Integrated circuits.

6/21 - 12/21 Expert Witness, Porsche AG and Porsche Cars North America, Inc., Patents and document analysis, Kirkland & Ellis LLP, Amplifier circuits.

4/21 – Technical Consulting, Dark Vision Technologies Inc., Ultrasound system and ASIC architecture design.

10/20 - 6/21 Expert Witness, RAI Strategic Holdings Inc., RAI Strategic Holdings Inc. et al. v. Altria Client Services LLC et al., 1:20-cv-00393-LO-TCB, Jones Day, electronic vapor systems, reports, depositions, IPR petition declarations.

10/19 – Expert Witness, NXP, NXP v. Impinj, IPR2020-00553, IPR2020-00556, Jones Day, RFID circuits, reports.

2/19 – 5/19 Expert Witness, Supersonic Imagine (SSI), SSI v. Verasonics, Morgan, Lewis & Bockius LLP, ultrasound data processing.

5/18 - 10/19 Expert Witness, Tektronix, Inc., Tektronix v. Rohde Schwarz, IPR2018-00643, IPR2018-00647, Jones Day (transferred from Perkins Coie), LLP, data acquisition systems and circuits, reports and deposition.

10/17 - 2/18 Technical Consulting, Caretaker Medical, Medical diagnostics design.

10/17 - 6/20 Expert Consultant, Intel Inc., Patents and documents analysis, Kirkland & Ellis, LLP, digital and mixed-signal CMOS circuits.

7/17 – 6/18 Expert Witness, Barco, Inc., Barco v. T-Rex Property, CV11-1375-PHX-SRB, Nuestel Law Offices, LTD, network system architectures, reports.

12/14 - 2/16 Expert Consultant, Samsung Inc., Patents and documents analysis, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

7/14 – 8/14 Expert Consultant, Intel Inc., Patents and documents analysis, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

11/12 - 5/13 Expert Witness, Sound Design Technologies, Sound Design v. Oticon, Inc., Perkins Coie, Brown & Bain, LLP, mixed-signal CMOS circuits.

2/09 – 6/11 Expert Witness, Samsung, Spansion v. Samsung, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

8/09 – 6/10 Expert Witness, IBM, MOSAID v. IBM, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

10/09 - 2/10 Expert Witness, Cisco, Cisco Systems v. MOSAID, Kirkland & Ellis, LLP, mixed-signal electronics.

4/09 – 6/09 Expert Witness, Apple Computer, Wong, Cabello, Rutherford & Brucculeri, LLP, mixed-signal electronics, USB protocol.

8/08 –12/10 Expert Witness, Samsung, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

3/08 – 3/09 Expert Witness, AMIS, AMIS v. PowerDsine, Perkins Coie Brown & Bain, pre-trial deposition, POE integrated circuits, protocols, POE product evals, reports.

10/07 – 2/08 Expert Witness, Analog Devices, Analog Devices v. Silicon Laboratories, Proskauer Rose LLP, pre-trial deposition, mixed-signal CMOS isolation circuits.

7/07 - 1/09 Expert Witness, Micron, MOSAID v. Micron, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

3/07 – 7/07 Expert Witness, Samsung, Samsung v. Matsushita, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

9/06 – 5/07 Expert Witness, Samsung, Samsung v. Ericson, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

3/05 – 11/05 Expert Witness, Sigmatel, Sigmatel v. Actions Semiconductor, Kirkland & Ellis, LLP, mixed-signal CMOS circuits, firmware evaluation.

12/03 – 9/04 Expert Witness, Agere, Agere v. Broadcom, Kirkland & Ellis, LLP. Testimony at Markman, pre-Markman and pre-trial depositions, mixed-signal CMOS circuits, VCOs, interface, biasing.

8/98 - 6/03 Technical Consultant, Agilent Technologies. Exploratory design and simulation of next-generation circuit technologies.

2/01 - 3/01 Technical Consultant, Displaytech. Analysis of circuit issues in silicon-backplane microdisplays.

Awards:

Best Paper of Conf. Award, Hewlett-Packard Design Technology Conference, May 1997.

Best Paper of Session Award, Hewlett-Packard Design Technology Conference, May 1994.

Auburn University Outstanding Graduate Student Award, March 1991.

Sigma Xi Carolyn Carr Outstanding Research Award, February 1991.

Tech Brief Award, NASA Langley Research Center, June 7, 1990.

Invention Disclosure Award, NASA Langley Research Center, December 1, 1989.

Outstanding Performance Award, NASA Langley Research Center, December 1985.

Invited Guest, National Security Forum, Air War College, May 23-27, 2002

Affiliations/Service:

Program Committee, VLSI Circuits Symposium, 2002 – 2007

Program Committee, Great Lakes Symposium on VLSI Circuits, 2003 - 2008

Associate Editor, IEEE/OSA Journal of Display Technology, 2004 - 2006

Associate Editor, IEEE Transactions on Very Large Scale Integration Systems, 2003 - 2005

Reviewer, IEEE Journal of Solid State Circuits, 1999 - 2005

Associate Director, Rodman Scholars Program, School of Engineering, UVa, 2000 – 2004

Mentor, NIH Biotech Training Grant, 2000-2005

Chairman, UVa ECE Graduate Committee, 2000-2002

Chairman, UVa SEAS Rules and Courses Committee, 2002- 2004

Board of Directors, University of Virginia Institute for Microelectronics, 1999 – 2008

Boy Scout Adult Leader, Troop 17, Charlottesville, VA, 2003 – 2006

Institute of Electrical and Electronics Engineers

Phi Eta Sigma and Sigma Xi, National Honor Societies

Tau Beta Pi, National Engineering Honor Society

Eta Kappa Nu, National Electrical Engineering Honor Society

Books and Book Chapters:

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Sixth Edition*, McGraw Hill, New York, in preparation.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Fifth Edition*, McGraw Hill, New York, February 2015.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Fourth Edition*, McGraw Hill, New York, April 2010.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Third Edition*, McGraw Hill, New York, January 2007.

J. Theil, M. Boehm, D. S. Gardner, and T. Blalock, editors, *Materials, Integration and Technology for Monolithic Instruments,* vol. 869, Materials Research Society, 2005.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Second Edition,* McGraw Hill, New York, July 2003.

R. W. Johnson, R. C. Jaeger, and T. N. Blalock, "Wafer-scale multichip packaging technology," *Wafer Scale Integration*, Chapter 10, Kluwer Publishing Company, 1989.

Refereed Journals:

X. Shen, D. Duvvuri, P. Bassirian, H. L. Bishop, X. Liu, A. Dissanayake, Y Zhang, T. N. Blalock, B. H. Calhoun, S. M. Bowers, "A 184-nW, -78.3-dBm Sensitivity Antenna-Coupled Supply, Temperature, and Interference-Robust Wake-Up Receiver at 4.9 GHz," in *IEEE Trans. on Microwave Theory and Techniques*, vol. 70, pp. 744 – 757, Jan. 2022.

J. F. Bolus, B. H. Calhoun, and T. N. Blalock, "39 fJ/bit On-Chip Identification of Wireless Sensors Based on Manufacturing Variation," *Journal of Low Power Electronics and Applications,* 2014, 4, 252-267.

S. N. Wooters, A. C. Cabe, Z. Qi. J. Wang, R. W. Mann, B. H. Calhoun, M. R. Stan, and T. N. Blalock. "Tracking on-chip age using distributed, embedded sensors," Tran. On VLSI Systems, vol. 20, pp.1974-1985, Nov. 2012.

S. N. Wooters, B. H. Calhoun, and T. N. Blalock, "An energy-efficient subthreshold level converter in 130-nm CMOS," Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 57, no. 4, pp. 290 –294, April 2010.

J. Hossack, Y. Li, W. F. Walker, T. N. Blalock, "Synthetic Axial Acquisition: Full Resolution Low-Cost C-Scan Ultrasonic Imaging," IEEE Trans. Ultrason. Ferroelec. Freq. Contr, vol. 55, no. 1, pp. 236-239, Jan. 2008.

Fuller, M. I., K. Ranganathan, S. Zhou, E. V. Brush, T.N. Blalock, J.A. Hossack, and W.F. Walker, "Experimental System Prototype of a Portable, Low-Cost, C-scan Ultrasound Imaging Device," IEEE Trans. Biomedical Engr., vol. 55, no. 2, pp. 519-530, Feb. 2008.

M. Fuller, T. N. Blalock, J. A. Hossack, and W. F. Walker, "Novel Transmit Protection Scheme for Ultrasound Systems," *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control,* vol. 54, no. 1, pp. 79-86, Jan. 2007.

K. Ranganathan, M. K. Santy, T. N. Blalock, J. A. Hossack, and W. F. Walker, "Direct Sampled I/Q Beamforming for Compact and Very Low Cost Ultrasound Imaging," *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control*, vol. 51, no. 9, pp. 1082-1094, Sep. 2004.

G. B. Ratanpal, R. D. Williams, and T. N. Blalock, "An on-chip signal suppression countermeasure to power analysis attacks," IEEE Transactions on Dependable and Secure Computing, vol. 1, no. 3, pp. 179-189, July-Sep. 2004.

T. N. Blalock, N. B. Gaddis, K. A. Nishimura, and T. A. Knotts, "True Color 1024x768 Microdisplay with Analog In-Pixel Pulse Width Modulation and Retinal Averaging Offset Correction," *IEEE Journal of Solid-State Circuits,* vol. 36, no. 5, pp. 838-845, May 2001.

T. N. Blalock and R. C. Jaeger, "A high speed sensing scheme for 1T dynamic RAMs utilizing the clamped-bit-line sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-27, no. 4, pp. 618-625, April 1992.

T. N. Blalock and R. C. Jaeger, "A high speed clamped-bit-line current-mode sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp. 542-548, April 1991.

R. C. Jaeger and T. N. Blalock, "Quasi-static RAM design for high performance operation at liquid nitrogen temperature," *Cryogenics*, vol. 30, no. 12, pp. 1030-1035, Dec. 1990.

T. N. Blalock and W. T. Yost, "Detection of fiber damage in a graphite epoxy composite using current injection and magnetic field mapping," *1985 Review of Progress in Quantitative NDE*, June 23-28, 1985, pp. 1207-1213.

Refereed Conference Proceedings:

D. Duvvuri, X. Shen, P. Bassirian, H. L. Bishop, X. Liu, C. Chen, A. Dissanayake, Y. Zhang, T. N. Blalock, B. H. Calhoun, S. M. Bowers, "A 366 nW, −74.5 dBm Sensitivity Antenna-Coupled Wakeup Receiver at 4.9 GHz with Integrated Voltage Regulation and References," *2021 IEEE MTT-S International Microwave Symposium*, 2021, pp. 641-645.

Z.Qi, J.Wang, A.Cabe, S.Wooters, T.Blalock, B.Calhoun,and M.Stan, "Sram-based NBTI/PBTI sensor system design," in Design Automation Conference, 2010. DAC '10. 47th ACM/IEEE, June 2010.

M. I. Fuller, K. Owen, T. N. Blalock, J. A. Hossack, W. F. Walker, "Real time imaging with the Sonic Window: A pocket-sized, C-scan, medical ultrasound device," *Ultrasonics Symposium (IUS), 2009 IEEE International Ultrasonics Symposium* , vol., no., pp.196-199, Sept. 2009.

S. C. Jocke, J. F. Bolus, S. N. Wooters, A. D. Jurik, A. C. Weaver, T. N. Blalock and B. H. Calhoun, "A 2.6-µW Sub-Threshold Mixed-Signal ECG SoC," Proc. of the 2009 VLSI Circuits Sym., June 2009, pp. 60-61.

A. Cabe, Z. Qi, S. Wooters, T. Blalock, and M. Stan, "Small embeddable NBTI sensors (sens) for tracking on-chip performance decay," in Quality of Electronic Design, 2009. ISQED 2009. Quality of Electronic Design, March 2009, pp. 1–6.

A. D. Jurik, J. F. Bolus, A. C. Weaver, B. H. Calhoun, and T. N. Blalock, "Mobile Health Monitoring Through Biotelemetry," International Conference on Body Area Networks (BodyNets), April 2009.

B. H. Calhoun, J. Bolus, S. Khanna, A. D. Jurik, A. F. Weaver, and T. N. Blalock, "Sub-threshold Operation and Cross-Hierarchy Design for Ultra Low Power Wearable Sensors," International Symposium on Circuits and Systems, pp. 1437-1440, May 2009.

B. L. Dell, J. F. Bolus, and T. N. Blalock, "An automated unique tagging system using CMOS process variation," Proceedings of the 17th Great Lakes Symposium on VLSI, March 11-13, 2007.

M. Fuller, E. Brush, M. Eames, T. N. Blalock, J. Hossack, W. Walker, "The Sonic Window: second generation prototype of low-cost, fully-integrated, pocket-sized medical ultrasound device." Proceedings from the 2005 IEEE Int. Ultrasonics Symp., Sept. 18-21, pp. 273-276, 2005.

M. K. Santy, T.N. Blalock, and W.F. Walker, "Design and Evaluation of a Low Cost PC Card Used for an Acoustic Radiation Force Based Mechanical Characterization System," Proceedings from the 2005 IEEE Int.. Ultrasonics Symp., Sept. 18-21, pp. 1428-1430, 2005.

Y. Li, T. N. Blalock, W. F. Walker, J. A. Hossack, "Synthetic axial acquisition full resolution C-Scan ultrasonic imaging," Proceedings from the 2005 IEEE Int. Ultrasonics Symp., Sept. 18-21, pp. 1392-1395, 2005.

Y. Li, T. N. Blalock, W. F. Walker, J. A. Hossack, "Phased subarrays for low cost C-Scan applications," Proceedings from the 2005 IEEE Int.. Ultrasonics Symp., Sept. 18-21, pp. 1408-1411, 2005.

Y. Zhang; T. Blalock, M. R. Stan, "A Three-level Toggle-avoid Bus Signaling Scheme," Proceedings from the 2005 IEEE Int. Sym. on Circuits and Systems Circuit, May 23-26, pp. 1843-1846, 2005.

K. Ranganathan, M.K. Santy, M.I. Fuller, S. Zhou, T.N. Blalock, J.A. Hossack, and W.F. Walker, "A Prototype Low Cost Handheld Ultrasound Imaging System," SPIE Medical Imaging 2004, Proc. SPIE 5373, pp. 24-32, 2004.

M. I. Fuller, K. Ranganathan, S. Zhou, T. N. Blalock, J. A. Hossack and W. F. Walker, "Portable, Low-Cost Medical Ultrasound Device Prototype," Proc. IEEE Int. Ultrasonics Symp., Aug. 24-27, 2004, pp. 106-107.

M. I. Fuller, T. N. Blalock, J. A. Hossack, and W. F. Walker, "A Portable, Low-Cost, Highly Integrated 3D Medical Ultrasound System," Proc. IEEE Int. Ultrasonics Symp., Oct. 5-8 2003, pp. 38-41.

E. E. Girard, S. Zhou, W. F. Walker, T. N. Blalock, and J. A. Hossack, "High Element Count Two Dimensional Transducer Array," Proc. IEEE Int. Ultrasonics Symp., Oct. 5-8 2003.

W. F. Walker, J. A. Hossack, and T. N. Blalock, "Direct Sampled I/Q Beamforming: A Strategy for Very Low Cost Ultrasound," Proc. IEEE Int. Ultrasonics Symp., Oct. 5-8 2003, pp. 1863-1866, pp. 964-967.

S. N. Chanderkar, M. L. Reed, and T. N. Blalock, "CMOS Non-Contacting Readout Circuits for Infrared Sensors," Proc. of the IASTED International Conference on Circuits, Signals, and Systems, May 19-21, 2003, pp. 368-372.

A. Gupta, R. Suryanarayan, and T. N. Blalock, "Tunable Active Capacitance Multiplication Circuit," Proc. of the IASTED International Conference on Circuits, Signals, and Systems, May 19-21, 2003, pp. 60-64.

A. Anumula, M. L. Reed, and T. N. Blalock, "CMOS Baseline Subtraction Readout Circuit for Infrared Sensors," Proc. of the IASTED International Conference on Circuits, Signals, and Systems, May 19-21, 2003, pp. 362-367.

M. I. Fuller, J. Mabry, J. A. Hossack, and T. N. Blalock, "40 MHz 0.25 um CMOS Embedded 1T Bit-Line Decoupled DRAM FIFO for Mixed-Signal Applications," Proc. of the 2003 GLSVLSI Conference, April 28-29, 2003, pp. 182-185.

R. Suryanarayan, A. Gupta, and T. N. Blalock, "A Slew Rate Enhancement Technique for Operational Amplifiers based on a Tunable Active G_m-based Capacitance Multiplication Circuit," Proc. of the 2003 GLSVLSI Conference, April 28-29, 2003, pp. 273-276.

R. Viswanathan, N. Jankowski, W. K. Lye, G. P. Dufrenoy, M. J. Harrison, J. A. Hossack, T. N. Blalock, and M. L. Reed, "Micromachined magnetic ultrasound transducer in post-processed CMOS," Proc. of the Materials Research Society Symposium - Biomicroelectromechanical Systems, April 21-25, 2003.

J. S. Wegman, A. Dwarka, M. Holzer, W. K. Lye, M. L. Reed, E. Herzog, and T. N. Blalock, "Transimpedance-mode CMOS Microelectrode Array for In-Vitro Neuronal Activity Recording," Proc. of the Materials Research Society Symposium - Biomicroelectromechanical Systems, April 21-25, 2003.

V.M. Igure, T.N. Blalock, and R.D. Williams. "A Defense Against 'Sleep-Deprivation' Attack". Proceedings of the IASTED International Conference on Communications and Computer Networks, CCN-2002, Cambridge,MA,USA. Nov 4-6, 2002. pp. 152-157.

Fabian, C. M., K. N. Ballu, J. A. Hossack, T. N. Blalock, and W. F. Walker, "Development of a Parallel Acquisition System for Ultrasound Research," Proc. SPIE vol. 4325, pp. 54-62, Medical Imaging 2001: Ultrasonic Imaging and Signal Processing, 2001.

M. Holzer, T. Blalock, E. Herzog, A. Kolla, W.-K. Lye, A.J. Nijdam, M. Stan, Y. Zu, M.L. Reed, "Integrated Microelectrode Arrays for In Vitro Neuronal Recording," Biomedical Engineering Society 2000 Annual Fall Meeting. Annals of Biomedical Engineering, Vol 28, Supplement 1.

H. E. Abraham, Homer Antoniadis, B. B. Roitman, K. Frischknecht, T. N. Blalock, K. A. Nishimura, T. A. Knotts, J. Theil, C. Gright, J. N. Miller, and R. Moon, "XGA Resolution Full Video Microdisplay Using Light Emitting Polymers on a Silicon Active-Matrix Circuit," *Proceedings of SPIE, vol. 4105: Organic Light-Emitting Materials and Devices IV*, pp. 37-52, July 2000.

T. N. Blalock, N. B. Gaddis, K. A. Nishimura, and T. A. Knotts, "8-bit/Color 1024x768 Microdisplay with Analog In-Pixel Pulse Width Modulation and Retinal Averaging Offset Correction," *Proc. of the 2000 Int. Sym. on VLSI Circuits*, pp. 20-23, June 2000.

T. N. Blalock, R. A. Baumgartner, and T. Hornak, "A 1.5 GOPS Analog CMOS Array Processor with Integrated Optical Image Acquisition for Position Encoding Applications," *Proc. of the 1998 Int. Sym. on VLSI Circuits,* pp. 204-205, June 1998.

K. Poulton, T. N. Blalock, K. Nishimura, "FET Mismatch Studies for CMOS26B and CMOS14B," *Proc. Hewlett-Packard Design Technology Conf.*, pp. 429-434, May 1996.

J. S. Ignowski, R. Badyal, C. E. Moore, K. R. Stafford, L. C. Tsai, T. Walley, R. A. Zimmer, R. A. Baumgartner, and T. N. Blalock, "Mesohippus: A 100 Mb/S CMOS Analog PRML Read/Write Channel for Hard Disk Drives," *Proc. Hewlett-Packard Design Technology Conf.*, pp. 53-60, May 1994.

T. N. Blalock, A. Brown, B. Zimmer, C. E. Moore, "Analog and Mixed Signal Design," Panel Discussion at the Hewlett-Packard Design Technology Conf., May 27, 1993.

T. N. Blalock and T. Hornak, "Bucket Brigade Analog Delay Line with Voltage Limiting Feedback," *Proc. Hewlett-Packard Design Technology Conf.*, pp. 183-196, May 1992.

T. N. Blalock and R. C. Jaeger, "A subnanosecond clamped-bit-line sense amplifier for 1T dynamic RAMs,"*Proc. of the 1991 Int. Sym. on VLSI Technology, Systems, and Applications*, pp. 82-86, Taipei, Taiwan, May 1991.

T. N. Blalock and R. C. Jaeger, "A high speed clamped-bit-line sensing scheme for 1T dynamic RAMs," *Proc. of the 1991 VLSI Circuits Sym.*, pp. 61-62, May 1991.

R. C. Jaeger and T. N. Blalock, "Optimization of CMOS low temperature quasi-static RAM based on non-destructive readout dynamic cell structures," *ECS Sym. on Low Temperature Electronic Device Operation*, May , 1991.

T. N. Blalock and R. C. Jaeger, "An experimental 2T cell RAM with 7 ns access time at low temperature," *1990 Sym. VLSI Circuits Dig. Tech. Papers*, June 1990, pp. 13-14, June 1990.

B.A Mineo, A. Cavalier, J. Companion, J. Heyman, T.N. Blalock, and F.A. Klein, "A portable, non-invasive ultrasonic bladder sensor for incontinence," *Proceedings of the Eighth Annual Conference of the IEEE/Engineering in Medicine and Biology* , pp.1864-7 vol. 3. New York, NY, 1986.

J. Companion, J. S. Heyman, T. N. Blalock, A. Cavalier, B. Mineo, F. Klein, and L. Fox, "Bladder distension sensor for the handicapped," *IEEE Ultrasonics Symposium Digest*, pp. 953-956, vol. 2, November 17-19, 1986.

Technical Reports:

J. Companion, J. S. Heyman, B. A. Mineo, A. R. Cavalier, and T. N. Blalock, "An ultrasonic monitor for bladder fullness," *NASA Tech Brief*, April 1991.

T. N. Blalock, "Laboratory technique for detection of composite fiber damage," *Research and Technology*, 1985 Annual Report of the Langley Research Center, pp. 23-24.

Other Presentations:

T. N. Blalock, A 1.5 GOPS Analog CMOS Array Processor with Integrated Optical Image Acquisition for Position Encoding Applications, ETH Zurich Physical Electronics Laboratory, January 26, 2001.

W. F. Walker and T. N. Blalock, "Development of a Next-Generation Ultrasound Research Platform," *Invited talk at Agilent Technologies*, Andover, MA, Dec. 8, 1999.

T. N. Blalock, "Real-Time CMOS Integrated Signal Processing*," DSP for Sampled Coherent Aperture Systems: Challenges, Synergies and Extensions*, Charlottesville, VA, July 7-9,1999.

T. N. Blalock, "Integrated Signal Processing and Imaging at the University of Virginia," *Southeastern Workshop on Mixed-Signal VLSI and Monolithic Sensors*, Oak Ridge, TN, April 8-9, 1999.

Patents (Issued US Patents Only):

W. F. Walker, M. I. Fuller, K. Ranganathan, J. A. Hossack, T. N. Blalock, “Front end circuitry with analog sampling and decoding for ultrasound imaging systems and methods of use,” U. S. Patent No. 9,989,497, June 5, 2018.

J. A. Hossack, M. I. Fuller, and T. N. Blalock, “Tracked ultrasound vessel imaging,” U. S. Patent No. 9,445,780 B2, September, 20, 2016.

T. N. Blalock, W. F. Walker, and J. A. Hossack, “Ultrasound imaging beam-former apparatus and method,” U. S. Patent No. 9,275,630, March 1, 2016.

T. N. Blalock, “Floating transducer drive, system employing the same and method of operating,” U. S. Patent No. 9,254,118 B2, March 3, 2015.

T. N. Blalock, W. F. Walker, and J. A. Hossack, “Ultrasonic transducer drive,” U. S. Patent No. 9,244,160, January 26, 2016.

J. A. Hossack, T. N. Blalock, and W. F. Walker, “Efficient architecture for 3D and planar Ultrasonic Imaging--Synthetic Axial Acquisition and Method Thereof,” U. S. Patent No. 8,057,392, November 15, 2011.

J. A. Hossack, T. N. Blalock, and W. F. Walker, “Hybrid Dual Layer Diagnostic Ultrasound Transducer Array,” U. S. Patent No. 7,750,537, July 6, 2010.

W. F. Walker, J. A. Hossack, and T. N. Blalock, "An Intuitive Ultrasonic Imaging System and Related Method Thereof," U. S. Patent No. 7,699,776, April 20, 2010.

J. A. Hossack, W. F. Walker, and T. N. Blalock, “Efficient ultrasound system for two-dimensional C-scan imaging and related method thereof,” U.S. Patent No. 7,402,136, July 22, 2008.

I. Bararav, T. N. Blalock, A. Machida, G. E. Smith, and J. K. Ang, “Imaging system and apparatus for combining finger recognition and finger navigation,” U. S. Patent No. 7,274,808, September 25, 2007.

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