

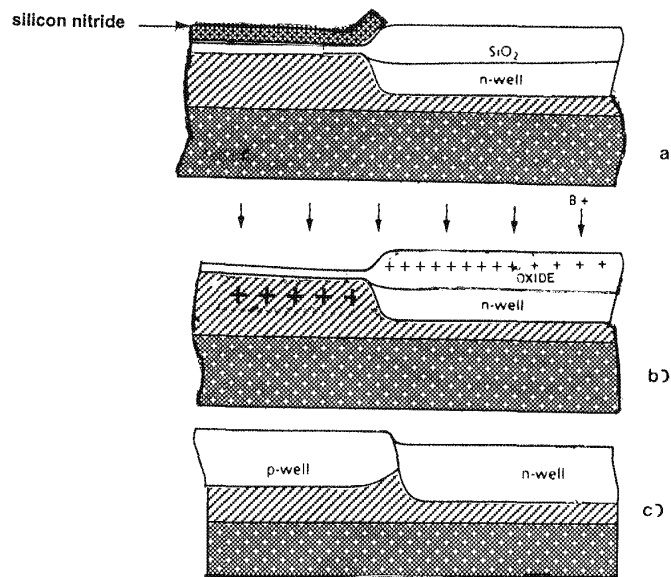


Fig. 16-9 (a) After the phosphorus that creates the n -well has been implanted, a thick oxide is grown, with the nitride preventing oxide from growing beneath it; (b) after stripping the nitride, a boron implant is performed that will form the p -well regions. The thick oxide above the n -wells prevents the boron from penetrating there; (c) wafer-surface topography after wells are driven-in and the oxide is stripped.

separate channel-stop implant step for the n -well. The oxide thickness is different over the n -well than the p -well, creating a step in the oxide film at the well boundaries. This oxide is nevertheless next etched away, but the step in the silicon remains behind (Fig. 16-9c). This step serves as an alignment mark to allow subsequent layers to be aligned to the well boundaries. (An alternative procedure that uses an additional mask can be used to create alignment marks. That is, deep pits can be etched into the wafer prior to the well formation step. Such marks provide improved registration accuracy for lithographic steps, and have become standard in deep-submicron CMOS technologies.)

It is important to observe that when wells are formed in this manner the well doping profile is at a maximum at the surface and then monotonically decreases with depth (see Fig. 16-10). The well doping concentrations are selected to be at least an order of magnitude higher than the epi-layer doping, so the expected variations in epi doping will not significantly affect the well concentration. The junction depth of the wells is typically $\sim 2 \mu\text{m}$ deep.

16.2.3 Definition of Active and Field Regions: In conventional CMOS processes a standard LOCOS process (described in more detail in Vols. 2 and 3) is next used to define the active and field regions, and to create isolation structures between the active devices (Fig. 16-11). This is done by selectively growing a thick thermal oxide over the field regions, while keeping the active regions devoid of oxide. The steps that accomplish this begin with the growth of a pad oxide by thermal oxidation over the entire wafer to a thickness of 40–50 nm. Next, a blanket layer of silicon nitride (140–200 nm thick) is deposited by LPCVD (Fig. 16-11a). Then photo-

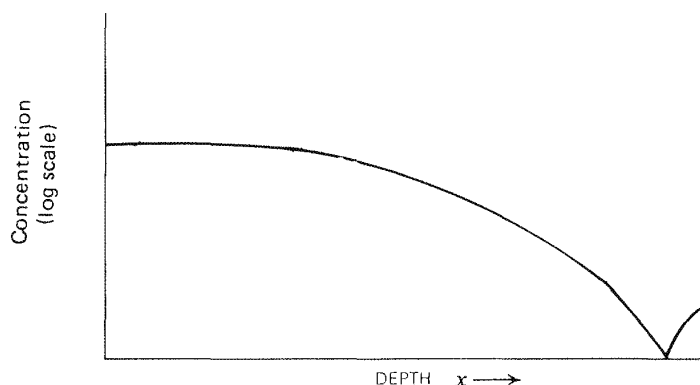


Fig. 16-10 Doping profile in a conventional well formed by a shallow implant and a drive-in step.

photoresist is spun onto the wafer and *Mask #2* is used to create the patterns that define the field and active regions of the circuit (Fig. 16-11b). After exposing and developing this pattern, the nitride is etched and the resist is stripped (Fig. 16-11c).

The next step creates the channel-stop dopant layer in the field regions of the *p*-wells. This is done by implanting a layer of boron atoms near the Si surface in the *p*-wells. This layer of implanted B atoms increases the threshold voltage of the parasitic PMOSFETs in the field regions of the *p*-wells. To prevent the boron from being implanted into the field regions of the *n*-wells, another mask is used. A layer of resist is applied prior to the boron channel-stop implant. *Mask #3* is used to form a pattern that covers the *n*-wells (Fig. 16-11d). Boron is then ion implanted into the surface (B with a dose of 10^{12} – 10^{13} atoms/cm² at 40–80 keV, using a medium-current implanter). Boron only enters the silicon substrate in regions not covered by *Mask #3* or nitride (Fig. 16-11e).

A thick oxide (called a *field oxide*) is next grown selectively to a thickness of 400–700 nm over the field regions using a wet oxidation process (Fig. 16-11f). The combination of a thick field-oxide and channel-stop dopants beneath this oxide forms *parasitic MOSFETs* in the field regions whose threshold voltages are too high to be turned on by normal voltages used to run the circuits. This keeps *active MOSFETs* in the IC electrically isolated from one another.

No oxide grows over regions covered with nitride (the active regions). Such a process of selectively growing field oxide has been named *local oxidation of silicon (LOCOS)*. Observe, however, that some oxide does grow under the edges of the nitride film as a result of the oxidizing species diffusing laterally as well vertically. This forms a tapered oxide region at the edge of the active region called a *birds beak* (Fig. 16-12 and Chap. 8). As the active regions get smaller with device scaling, bird's beak begins to limit the use of LOCOS.

16.2.4 Threshold-Adjust Implantation Step: After the field oxide is grown, the nitride is stripped and the circuit is almost ready for carrying out the threshold adjust (or V_T -adjust) implant process and for growing the gate oxide. Prior to this, however, a problem caused by the previous field oxidation step of the LOCOS process must be rectified. During the wet oxidation process

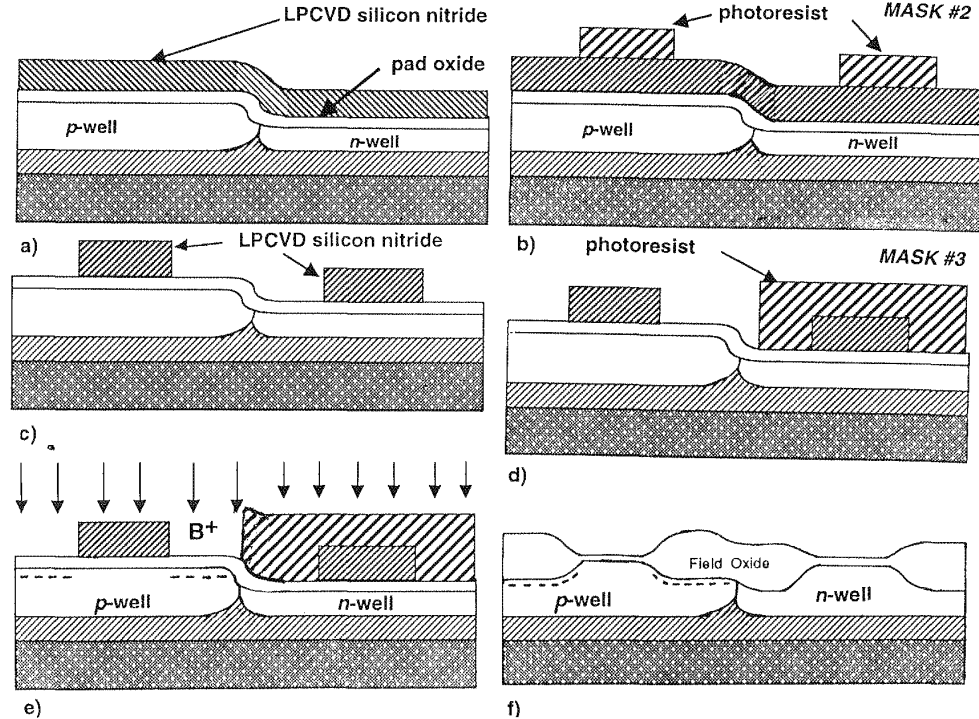
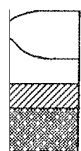


Fig. 16-11 Formation of the active and field regions using LOCOS isolation: (a) grow pad oxide and deposit silicon nitride film by LPCVD; (b) Use *Mask #2* to define active regions; (c) etch the nitride film; (d) Use resist and *Mask #3* to cover *n*-well regions; (e) implant B into the field-regions of the *p*-wells (channel-stop implant); (f) selectively grow field oxide with a wet-oxidation process, strip nitride.

a thin layer of nitride forms on the silicon surface of the active regions (near the edges of the nitride film). Such layers would interfere with the gate oxidation process, insofar as the gate oxide will not grow as rapidly over such regions (and hence it would be thinner there). This problem is called the *Kooi effect*. To overcome it a thin *sacrificial* (or *dummy*) oxide is next grown to a thickness of 50–100 nm. This also oxidizes the thin nitride layer so it can be removed with an HF etch. The V_T -adjust implant is usually performed with this dummy oxide layer in place, as the oxide serves another useful function. That is, it also acts as a screen oxide, preventing contaminants from the implantation process from entering the Si substrate.

The V_T -adjust implant step (Fig. 16-13a) sets the threshold voltage of both the NMOS and PMOS FETs, typically to values of 0.6 V and –0.6 V, respectively. The V_T -adjust implant process in CMOS technologies using only n^+ poly can be accomplished with either a single boron implant step (if the background doping is chosen correctly, see Fig. 16-13b), or with two separate boron implant steps (in which case an additional mask is required). A separate punchthrough-prevention implant for the NMOS devices is also usually needed, especially when the minimum device dimension decreases below about 1 μm (see Vol. 3). The punchthrough

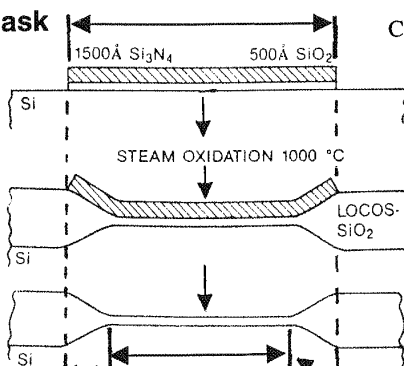


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Bird's Beak

Final Active Device

Fig. 16-12 "Bird's beak" in LOCOS isolation structure intrudes into the active regions of the wafer surface. This limits the use of LOCOS in deep-submicron IC process technologies.

implant can be performed sequentially using the same implanter, along with the V_T -adjust implant. Once the V_T -adjust implant step is completed, the dummy oxide is stripped with HF, leaving a residue-free Si surface upon which high-integrity gate oxides can be reliably grown.

16.2.5 Gate Oxide Growth: In the next step the gate oxide is formed. The growth of the gate oxide is a critical step. A defect-free, very thin (6-20-nm), high-quality oxide without contamination is essential for proper device operation. The gate oxide is grown only in the exposed active regions (actually, the field-oxide thickness is also very slightly increased as a result of the gate-oxide growth step). Since the drain current in an MOS transistor is inversely proportional to the gate-oxide thickness (for a given set of terminal voltages), the gate oxide is normally made as thin as possible – commensurate with oxide breakdown and reliability considerations. See Chap. 8 for details on thin gate-oxide growth.

16.2.6 Polysilicon Deposition and Patterning: Once the gate oxidation step is completed, a heavily n -doped polysilicon gate structure is fabricated. Polysilicon is the preferred gate material for several reasons. First, it can withstand the high-temperature steps required to form the source/drain junctions. Second, the polysilicon-SiO₂ interface is well understood and electrically stable. The gate formation procedure begins with the deposition of a 0.4–0.5 μm thick, undoped polysilicon film by LPCVD (Fig. 16-14a, and see Chap. 6 for details). This layer is then doped with phosphorus by ion implantation or chemical doping (Fig. 16-14b), producing a film with a sheet resistance of 20–30 Ω/sq . While this sheet-resistance value is small enough for MOS circuits with gate lengths $\geq 2 \mu\text{m}$, lower values are required for submicron ICs. In such applications, composite layers of refractory metal silicides and polysilicon (called *polycides*) are used to reduce the sheet resistance to $\sim 1\text{--}3 \Omega/\text{sq}$. This allows the benefits of the polysilicon-SiO₂ interface to be preserved and the gate sheet resistance to be lowered. For the CMOS processes being discussed here, CVD WSi_x became the most popular material used to form such polycide structures (see Chap. 6 for details on CVD WSi_x deposition).

The gate structure and polysilicon interconnect structures are then patterned using *Mask #4* (Fig. 16-14c). Following exposure and development of the resist, the polysilicon (or polycide) film is dry-etched (Fig. 16-14d). This is a critical etch step for several reasons. First, due to the

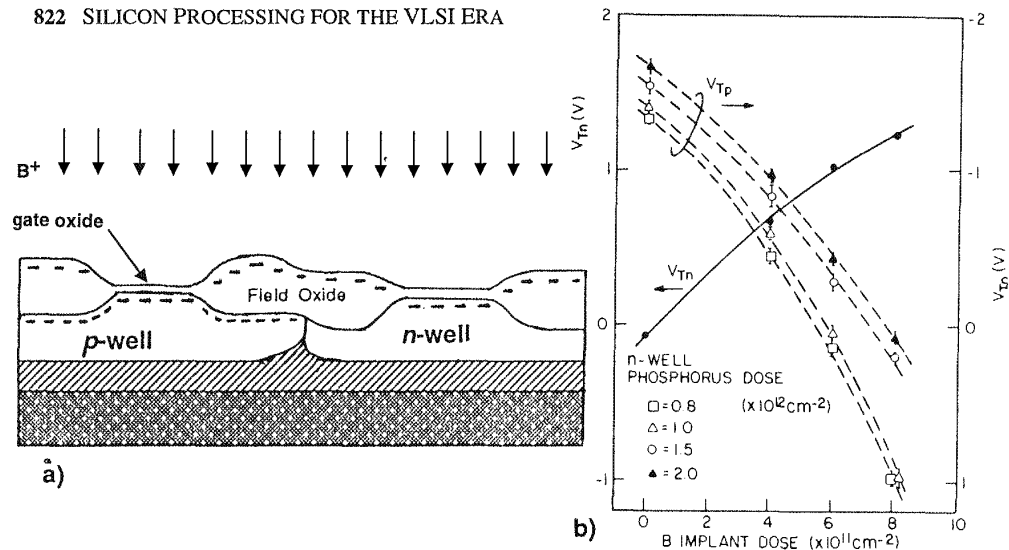


Fig. 16-13 (a) Threshold-voltage adjustment carried out using a single boron implant; (b) threshold voltages of NMOS (V_{Tn}) and PMOS (V_{Tp}) transistors as a function of boron dose. The CMOS structure uses an n -well implanted into a p -substrate (with doping level of $6 \times 10^{14} \text{ atoms/cm}^3$). V_{Tp} results are shown for various implant doses of the n -well.¹⁰ (© 1980 IEEE).

self-aligned nature of silicon-gate technology, the channel length of the device depends on the width of the polysilicon line. Hence, the gate-length dimension must be precisely maintained across the entire wafer, and from wafer to wafer. If the gate length is too long, the drain current of the MOSFETs will decrease, slowing down the performance of the IC. If the gate length is too short, the source and drain may punch through. Second, the profile of the etched poly gate structure should be vertical. This will prevent variation of channel lengths by the penetration of the ions of the thinner regions of the gate sidewalls during formation of the source/drain regions by ion implantation (Fig. 16-14e). Third, to achieve the above goals, an anisotropic polysilicon etch process must be employed. This process, however, requires overetching to remove the locally thicker regions of polysilicon that exist wherever it crosses steps on the wafer surface. During the overetch time, areas of the thin gate oxide are exposed to the etchants. Thus, it is necessary to use a polysilicon etch process that is highly selective with respect to SiO_2 .

After the polysilicon is etched, a step called *poly reox* is usually performed (16-14f). This grows a thin thermal SiO_2 layer on the polySi (on the order of 10 nm thick). The reasons for performing this step are discussed in Vol. 3, Chap. 9.

16.2.7 Formation of Source/Drain Regions: The next step in the process flow is the formation of source and drain (S/D) regions of the MOSFETs. Such regions are paths of current flow in the silicon between the metal interconnect lines and the channel of the transistor. As such, it is important that they have the lowest possible resistance. In addition, submicron MOSFETs require S/D junctions to be as shallow as possible to suppress such short-channel effects as *punch-through*, see Vol. 3. To obtain low resistivity, the S/D regions are doped as heavily as possible (typically using ion implantation, with a dose on the order of $\sim 10^{15} \text{ cm}^{-2}$). The NMOS S/D

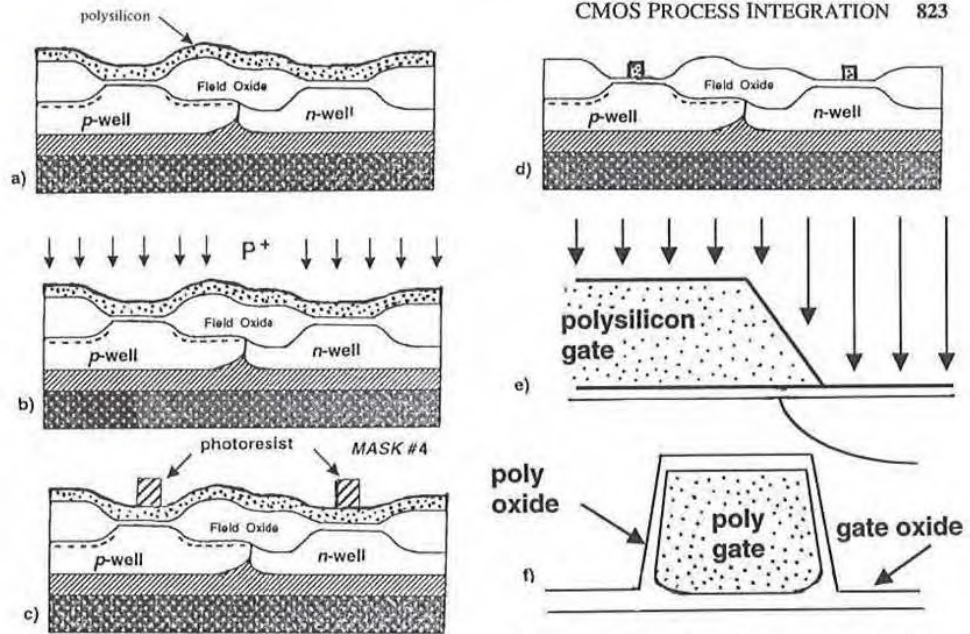


Fig. 16-14 n^+ -polysilicon gate formation: (a) deposition of undoped polysilicon film by LPCVD; (b) *ex-situ* doping of the polysilicon with phosphorus by chemical diffusion of ion implantation; (c) Use Mask #4 to define the polysilicon gates; (d) etch polysilicon and strip resist; (e) the etch process used to pattern the gate must yield poly features with vertical sidewalls (to maintain control of the effective gate length during the implant process that forms the source and drain regions); (f) polysilicon re-ox step grows a thin oxide on the poly by a short thermal oxidation process.

regions are doped with As, because it has a high solubility, low diffusivity, and a shallow projected range at the low ion implant energies that are used. Boron or BF_2^+ are used to dope the PMOSFET S/D regions. However, boron has a higher diffusivity than As. Hence, shallow S/D junctions in PMOSFETs are harder to achieve than in NMOSFETs. Since it is necessary to selectively implant source/drains to form n^+ regions for the n -channel FETs and p^+ regions for the p -channel FETs, this usually requires two masks (i.e., Mask #5 and Mask #6, Fig. 16-15).

In submicron-CMOS processes, gate lengths become so small that *lightly doped drain (LDD)* structures must be used to minimize hot-electron effects, especially in NMOS devices. Thus, procedures are integrated into the CMOS process flow to fabricate such LDD structures. If these structures are used only for NMOS transistors, Masks #5 and #6 will still allow the sources and drains of the two transistor types to be selectively implanted.* However, if LDD structures are needed for both PMOS and NMOS devices, two more masking layers may be needed.

* A procedure that requires only one masking step for creating both types of source and drain regions has also been reported. In this approach, the heavy boron implant is carried out non-selectively. The mask is then used to cover the PMOS device active regions. An n -type implant heavy enough to overcompensate for the boron implant in the active regions of the n -channel devices is used to form the sources and drains of the NMOS transistors.

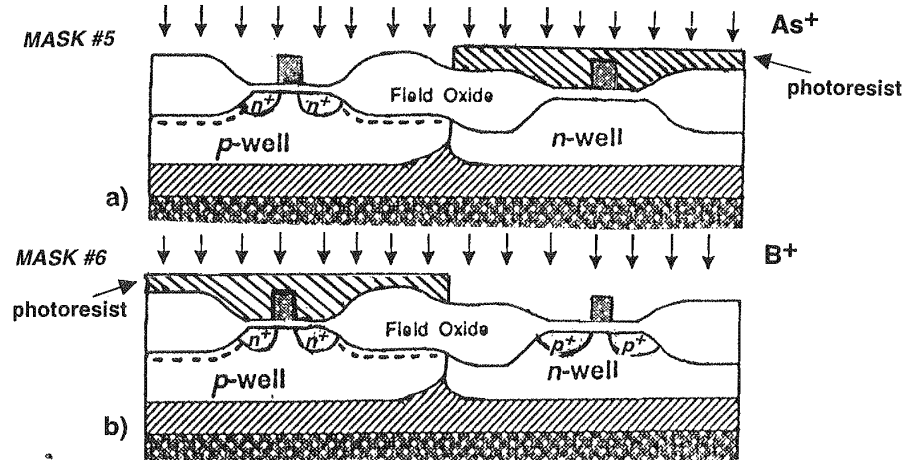


Fig. 16-15 Mask #5 and Mask #6 are used to allow selective implants of PMOS and NMOS source/drains.

The LDD structure is formed in the following way. The lightly doped regions of the source and drain are created with an ion implant step (Fig. 16-16b). A dose of approximately 3×10^{13} – 3×10^{14} cm^{-2} dopant ions is implanted at low energy (30–50 keV). The implantation process causes the edge of these implanted ions to be automatically aligned to the edge of the gate (i.e., it is a *self-aligned process*). A conformal layer of dielectric material (usually SiO_2 or silicon nitride) is then deposited over the entire wafer. An anisotropic etch process is used to clear the oxide in the flat areas while leaving sidewall spacers on the sidewalls of the poly gates (Fig. 16-16c). These spacers cover and protect the regions beneath them from the subsequent high-dose implant that forms the rest of the S/D regions. A dose of 1×10^{15} – 5×10^{15} atoms/ cm^2 at 40–80 keV is used for this step (as shown in Fig. 16-16d).

16.2.8 Premetal Oxide Deposition and Contact Formation: Following formation of the source and drain regions, a doped *premetal dielectric* (PMD) is deposited by CVD. (This layer is also known as an *interlevel dielectric* or *ILD*.) Contact windows are opened in this dielectric layer to allow electrical connections to be made between Metal 1 and the following structures: 1) source/drain contact regions; 2) gate contacts; 3) substrate-contact regions; and 4) well-contact regions. A CVD process is used to deposit doped SiO_2 , about $1 \mu m$ thick (Fig. 16-17a), onto the wafers (see Chap. 6 for details of this process). The dopant in the SiO_2 is either phosphorus (in which case the material is referred to as *phosphosilicate glass* or *PSG*), or both phosphorus and boron (making it *borophosphosilicate glass* or *BPSG*).

The doped CVD glass layer plays several roles in the fabrication and operating aspects of the circuit. First, it acts as an insulating layer between polysilicon and Metal 1. Second, it reduces the parasitic capacitance between Metal 1 and the substrate. Third, the addition of phosphorus to the glass makes the layer an excellent getter of Na ions (contamination by Na can destabilize the V_T of an MOS device). The PSG (or BPSG) binds otherwise mobile Na atoms within the doped-glass layer, preventing them from reaching the gate oxide and altering V_T . Finally, the dopants in the glass make it viscous at elevated temperatures (1000–1100°C for PSG, 850–950°C for BPSG, see Ch. 6). This allows the layer of glass to be flowed after it is deposited (Fig. 16-17b).

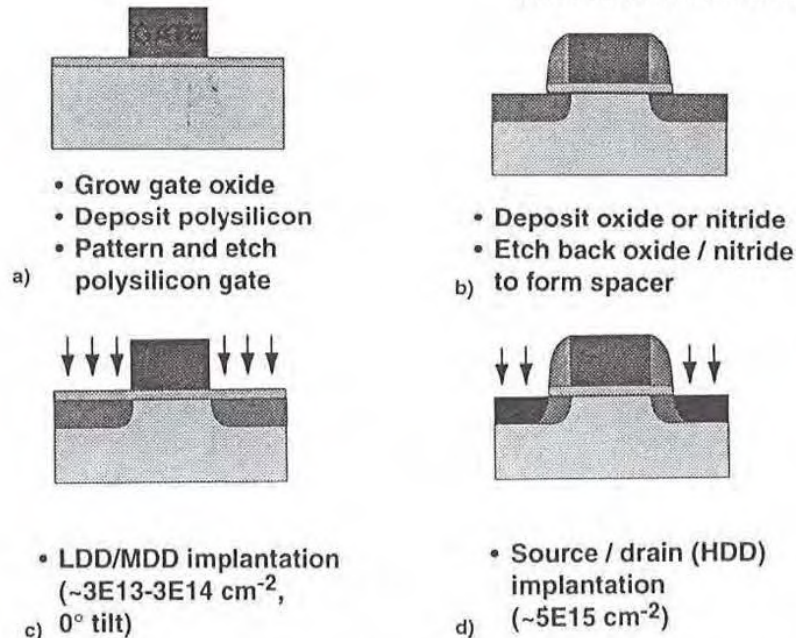


Fig. 16-16 Basic process to form an LDD NMOSFET: (a) after poly etch; (b) LDD implant; (c) after spacer material deposition and etch; (d) n^+ implant.

Through this procedure, a rounding of the glass contours and smoothing of any sharp steps is achieved. This produces better step coverage of the metal (which is deposited next) over the otherwise severe wafer topography. The high-temperature glass-flowing step also serves as an annealing process that activates the dopants implanted to create the source/drain junctions.

Contact openings are next created by a lithography-and-etch step (Fig. 16-17c). *Mask #7* is used to define contact patterns in a photoresist film. A dry-etch process is then used to open the contact windows through the interlevel dielectric to the underlying polysilicon and the source/drain regions in the silicon.

This contact-opening step can be critical, as the contact size and its alignment to underlying patterns limit the minimum size of the device. The source/drain regions must also be large enough for the contact to fit, with an allowance for alignment tolerance. If the contact opening exposes a part of the substrate, the drain or source will be shorted to it. Likewise, if the contact opening overlaps the both the source/drain and the gate, a short will be created between them.

After the contact etch is completed and the resist is stripped, the doped CVD glass is subjected to another flow step. This procedure rounds the corners of the top of the oxide windows so metal step coverage into the contact windows is improved (called *reflow* of the contact windows, see Chap. 6). It may still be too difficult to deposit metal into these contact holes with adequate step coverage. A number of techniques have been studied to improve the coverage of Metal-2 into the vias (Chap. 15). In Fig. 16-17d, the step coverage of Metal-1 into

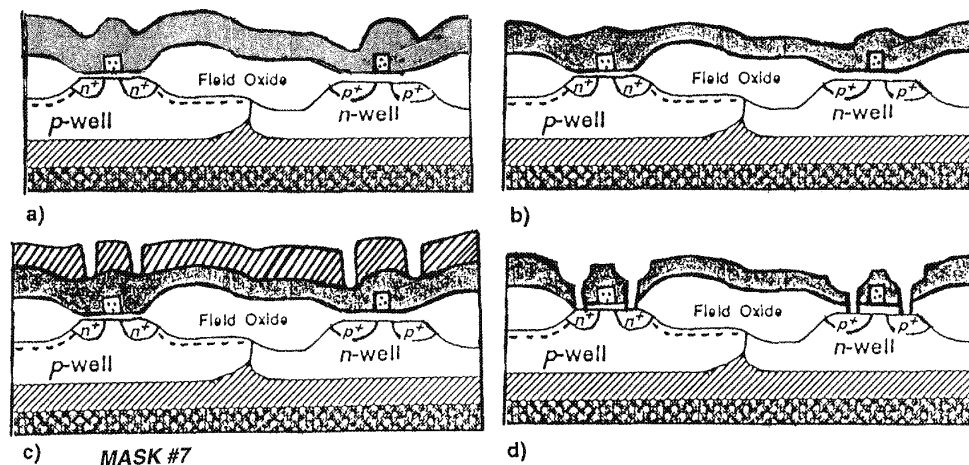


Fig. 16-17 (a) Deposit interlevel dielectric BPSG layer (ILD) by CVD; (b) flow BPSG. (c) use Mask #7 to define contact holes; (d) etch contact holes with "wine glass" etch and strip resist.

the contact hole is facilitated by the use of a *wine-glass* etch process. The contact hole is formed with a two-step via-etch process (i.e., using an isotropic etch process to etch half of the ILD thickness, and an anisotropic etch step to etch the remaining half). Reflow may still be carried out after such a two-step etch.

16.2.9 Metal Deposition and Patterning: After the contacts have been opened, the metallization layer is deposited. Because the metal layer is highly conductive, it is used whenever possible to interconnect circuit elements and to carry large amounts of supply current. The metal interconnect lines that are fabricated must have sufficient thickness, width, and step coverage to keep the current density in each line below the value that could produce electromigration failure (Vol. 2, Chap. 4). In addition, the space between adjacent metal lines must be kept large enough that the lines never touch, even under worst-case process variations.

Although evaporation was the method employed to deposit Al in the early days of MOS, it has generally been replaced by sputtering. The change was made because Al alloys with tightly controlled compositions became the materials of choice for the metal layer. Sputtering allows alloys to be deposited with much better compositional fidelity (see Chap. 11).

The metal alloy eventually chosen for NMOS was Al:1wt% Si. Silicon is added to the aluminum film to prevent spiking of the contacts during subsequent annealing steps (see Chap. 11). In CMOS, however, such Al:Si alloys were replaced with a metallization system that includes a diffusion barrier (typically Ti/TiN, see Chap. 15), and Al:Cu alloys for the main interconnect layer (Fig. 16-18a). Dry etching is used to pattern the interconnect films using Mask #8 (Fig. 16-18b).

If a single level of metal is used in the CMOS process, a sintering step occurs after the metal has been patterned. This step brings the metal and the n^+ and p^+ regions in the silicon into intimate contact. Such intimate contact between the metal and the heavily doped Si regions

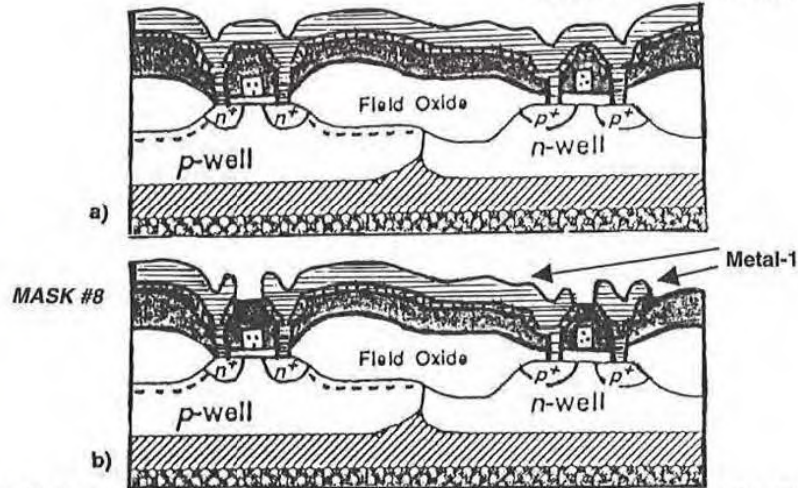


Fig. 16-18 (a) Deposit Ti/TiN/Al:Cu Metal-1 interconnect film. (b) Use Mask #8 to define Metal-1 pattern and then etch the metal with a dry-etch process.

establishes a low-resistance ohmic contact. The annealing process exposes the wafer to a 375–500°C temperature in an H_2 or $N_2 + H_2$ (5%) ambient for about 30 minutes. This step is also used as the annealing process for reducing the interface trap density in the gate oxide that was introduced by earlier processing steps (see Chap. 8).

16.2.10 Intermetal Dielectric Deposition and Via Patterning: If a two-level-metal interconnect structure is used, an *intermetal dielectric* (IMD) must be deposited to electrically isolate the Metal-1 layer from the Metal-2 layer (Fig. 16-19a). A variety of CVD processes for depositing such dielectric films have been developed (see Chap. 6).

Deposition of this layer may make the wafer topography once again too severe to allow Metal-2 films to be deposited with adequate step coverage. One of the planarization processes discussed in Chap. 15 may need to be used to overcome this difficulty.

If such techniques are successfully implemented, the wafer topography will be relatively planar, and any steps on its surface will be gently sloped rather than severely vertical. It is also necessary to open vias in the intermetal dielectric layer so an electrical connection can be established between Metal-2 and Metal-1 at desired locations (Mask #9). Metal-2 must be deposited with adequate step coverage into these vias, but reflow is not possible because Al is present on the wafer (Metal-1). Thus, in this example, a champagne glass etch process is again used to etch the vias (Fig. 16-19b).

16.2.11 Metal 2 Deposition and Patterning: The processing issues of depositing and patterning (Mask #10) the Metal-2 layer (Fig. 16-19c) are discussed in Chaps. 11, 14, and 15.

16.2.12 Passivation Layer and Pad Mask: Finally, a *passivation* (or *overcoat*) layer, such as CVD PSG or plasma-enhanced CVD silicon nitride (or both), is put down onto the wafer surface (Fig. 16-19d). This layer seals the device structures on the wafer, protecting them from contaminants and moisture. It also serves as a scratch protection layer.

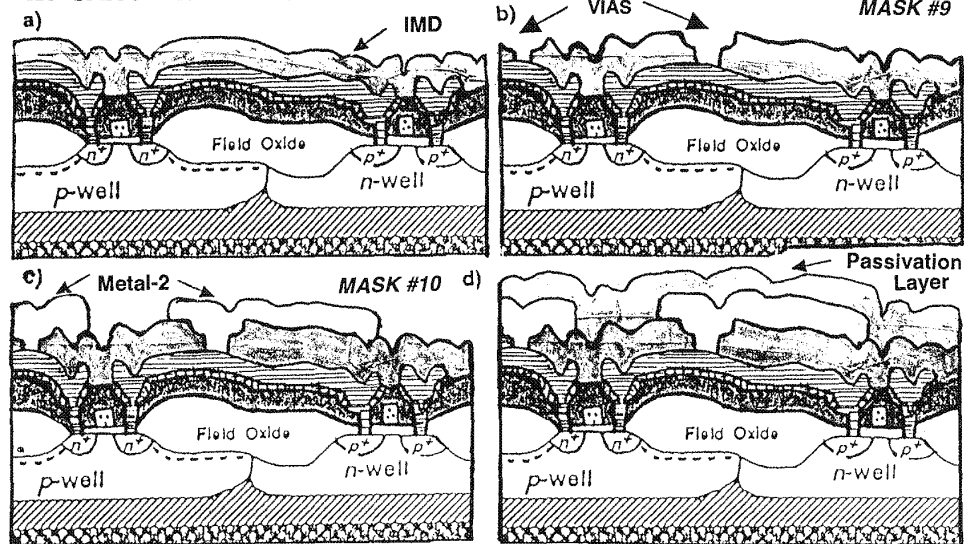


Fig. 16-19 (a) An intermetal dielectric (IMD) film is deposited by CVD. A planarization process such as resist etchback, or spin-on-glass, may be used to smooth this surface. (b) Vias are defined in the IMD film with *Mask #9* and an etch step. (c) Metal-2 is deposited and defined with *Mask #10* and a metal etch process. (d) A final passivation layer is deposited on the wafer by CVD.

Openings are etched into this layer so that a set of special metallization patterns under the passivation layer is exposed. These metal patterns are normally located in the periphery of the circuit and are called *bonding pads* (Fig. 16-20). Bonding pads are typically about $100 \times 100 \mu\text{m}$ in size and are separated by a space of 50 to $100 \mu\text{m}$. Wires are connected (bonded) to the metal of the bonding pads and are then bonded to the chip package. In this way connections are estab-

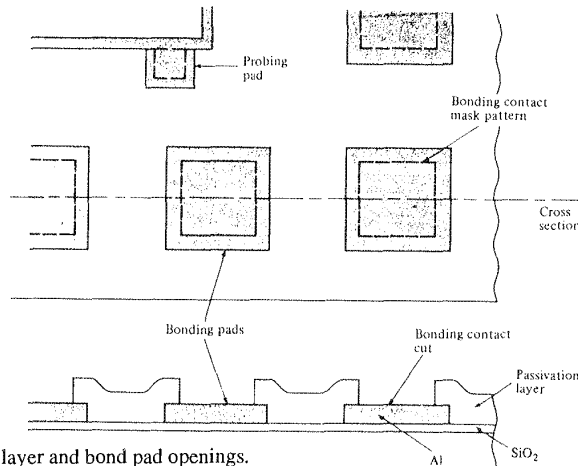


Fig. 16-20 Passivation layer and bond pad openings.



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lished from the chip to the package leads (see Chap. 17 for details on chip bonding).

The bond pad openings are created by patterning the passivation layer with *Mask #11*. If a PSG layer is used, the phosphorus (2-6 wt%) in the glass not only causes it to act as a getter for Na but also prevents the film from cracking. Care must be taken to ensure that not more than 6% phosphorus is incorporated into the PSG, as this can cause corrosion of the underlying metal if moisture enters the circuit package (see Chap. 11). When silicon nitride is used, care must be taken to ensure that the deposited nitride film exhibits low stress (either tensile or compressive), so it will not crack. Cracking would compromise the sealing capability of the film.

16.3 PROCESS FLOW FOR 0.25 μm CMOS

An example process flow for 0.25 μm CMOS (and perhaps for the 0.18 μm generation as well) will be presented in this section. (At this book's writing, the process flows for 0.25 μm CMOS, and below, were not yet "standardized," and many possible variations of the flow postulated here existed.) This flow is "compiled" from the literature, where a number of 0.25 μm CMOS technologies are reported, including those in Refs. 11, 12, 13, 14. Since the literature does not provide all the details of such flows, some of the information here is necessarily conjectural. Despite these issues, the 0.25 μm flow presented here should be a reasonable representation of those found in actual use.

A number of general characteristics of 0.25 μm CMOS process technology should be noted. First, the lithography technology used for the critical masking layers is DUV optical lithography, which is based on 248-nm KrF laser light sources (and *i*-line lithography perhaps being used for the non-critical layers). Second, the power supply voltages of the systems using 0.25 μm CMOS is 2.5 V, and for 0.18 μm CMOS is estimated to be 1.8 V. This is a deviation from the 5-V power supply used from the mid-1970s's and down to when CMOS reached 0.65 μm . However, when CMOS reached 0.5 μm , the gate oxide thickness had been scaled so much that the electric field across the gate oxide exceeded the value that would permit reliable operation for the designed life of the systems (e.g., 10 years). To ensure adequate device lifetime, the power supply voltage had to be changed for 0.5- μm CMOS to 3.3 V, and again at 0.25- μm CMOS to 2.5 V. (This is an example of how the limits of process technology impact the electronic systems specifications.) Third, the number of masking layers is likely to exceed 20, especially if 5 or more interconnect levels are needed. Finally, 0.25- μm CMOS was initially being manufactured on 200-mm wafers. It is likely that 0.18- μm CMOS will also use such wafer sizes. However, it appears that 0.15- μm CMOS, or 0.12- μm CMOS will enter large scale production on 300-mm wafers.

As mentioned in the introduction, there are a number of process modules that had to be fundamentally changed as CMOS technology was scaled below about 0.35 μm . Figure 16-21 demonstrates this quite clearly.¹³ The order of carrying out some of the steps has also changed. Why these changes in the process flow were necessary will be indicated.

16.3.1 Starting Material: The starting material for deep-submicron CMOS is predicted to shift more to *p*-epi-on-*p*⁺ wafers (Fig. 16-7b), because the gate-oxide-integrity is better on epi than on bulk wafers. However, the higher cost of epi compared to bulk wafers remains a concern, especially for such low-price commodity chips as DRAMs. Less expensive alternatives to epi are being studied. One process that shows great promise is the implantation of a high dose of

Generation	0.5um	0.35um	0.25um	0.18um	0.15um	0.13um
Isolation	LOCOS		STI			
Well	Diffused		Retrograde			
Gate	WiSix n+ Polycide		Dual Poly (n+/p+) Salicide			
Gate Oxide	Single Oxide		Dual/Triple Oxide => Oxynitride			
Gate Litho	I-line		248nm, Hi NA	PSM	193nm	
Silicide	None	TiSix		TiSix => CoSix		
Contact/Via	Etchback		CMP			
BEOL Dielectric	SOG	Oxide		Low-k		
Metal	Al		Al => Cu Damascene			

Fig. 16-21 The process modules used for successive submicron-CMOS generations.¹³ © IEEE (1998).

boron deep below the surface of a bulk wafer, using high-energy ion implantation. This step creates a heavily doped B buried layer that acts in the same way as the heavily doped substrate of the epi wafer.¹⁶ Good latchup protection and GOI are reportedly achieved by this approach. The cost for carrying out this step is 10–20% that of depositing an epi layer on a bulk wafer.

16.3.2 Formation of the Shallow-Trench-Isolation Structure: The isolation structures are formed next. Note that not only is a different type of isolation structure formed (*shallow trench isolation*, or *STI*) instead of LOCOS, but it is formed prior to the well structures. STI replaces LOCOS because STI has no bird's beak and provides a planar surface for further processing.¹⁵

The sequence of steps for forming STI structures begins with the growth of a pad oxide, followed by an LPCVD nitride layer. Then resist is applied and *Mask #1* is used to pattern the STI trench openings. The nitride and pad oxide are etched first. Then the trench is anisotropically etched (Fig. 16-22a) to a depth of 400–500 nm (e.g., using an etch gas mixture of $\text{HBr}/\text{Cl}_2/\text{O}_2$). The trench etching process should yield smooth trench sidewalls with angles of 70–85°, rounded bottom-corners (to minimize stress), and a residue-free silicon surface after etch (see Fig. 16-22f). After the trenches are etched the resist is stripped and a thin thermal oxide is grown on the trench walls (Fig. 16-22b). Next, a CVD dielectric film is used to fill the trench. This layer also covers the areas of the wafer where the nitride remains (Fig. 16-22c). A CMP step is used to polish back the dielectric layer until the nitride is reached (the nitride acts as a CMP-stop layer, Fig. 16-22d). The dielectric material is densified at about 900°C. Then the nitride is stripped, leaving the STI structure in place (Fig. 16-22e).

16.3.3 Formation of Retrograde Wells and Carrying Out of V_T -Adjust Implants: The well formation sequence occurs next. In addition, the V_T -adjust implants and the punchthrough implants are often carried out on the same ion implanter and during the same pumpdown as the well-formation implants. This process of performing multiple implants during the same pumpdown is termed a *chained implant*. The well formation step employs high-energy ion implantation to locate the well dopant peak ~1–2 μm below the Si surface. The implanted dopants will

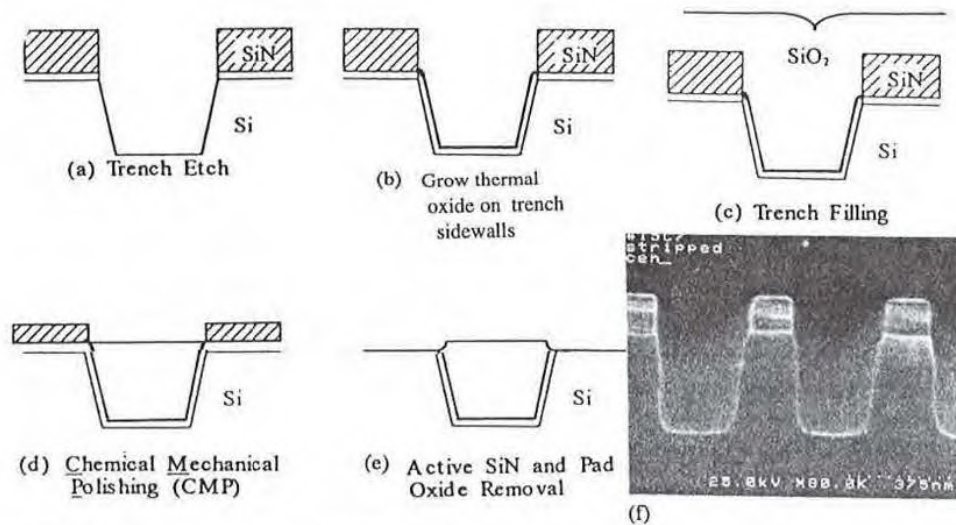


Fig. 16-22 Process sequence used to form shallow-trench isolation structures (STI): (a) etch trench in silicon substrate; (b) grow thermal oxide trench liner to improve trench Si/SiO₂ interface (and for trench corner rounding); (c) fill trench with CVD oxide; (d) use CMP to etch back the oxide to the nitride layer; (e) Strip nitride to leave the STI structure; (f) SEM of trench profile with 87° trench sidewall slope, and top and bottom trench corner rounding. Courtesy of Lam Research Corp.

have a *retrograde* concentration profile toward the surface from this peak (Fig. 16-23). Such a doping profile has several device performance advantages (discussed in Vol. 3). Since the dopants are placed deeply enough by the implant itself, there is no need for the long, high-temperature drive-in step required previously. Instead, only a lower-temperature anneal (carried out in a furnace at 900°C for 30 min), or a very-short, high-temperature RTP anneal (1100°C for 30 sec), is required to activate the implanted dopants. However, the high-energy ion beam used in the implantation process (500 keV–1 MeV) requires the use of a high-energy ion implanter and very thick resist films (~5 μm). Such thick resists are needed to prevent high-energy ions from reaching the Si surface in regions covered by the resist.

The well-formation process is begun by growing a layer of sacrificial oxide on the wafer. After applying the thick resist layer, *Mask #2* is applied to open the patterns for where the *n*-wells will exist. Then a high-energy P implant is carried out (700–850 keV, $1 \times 10^{13} \text{ cm}^{-2}$). The peak of the P implant is ~1 μm below the Si surface (Fig. 16-24b). Both the V_T -adjust implant for the PMOSFETs (using P, since the dual-doped poly will allow the use of surface-channel PMOS devices – see Vol. 3), and the punchthrough implant are carried out in this implanter in the same pumpdown. Then the resist is stripped, and a new coat of thick resist is applied. *Mask #3* is then used to pattern the *p*-well openings. A high-energy B implant is then carried out (450–500 keV, $1 \times 10^{13} \text{ cm}^{-2}$, Fig. 16-24c). A retrograde profile is again created, with the B peak concentration residing at 1–2 μm below the surface (Fig. 16-25). The V_T -adjust implant and the

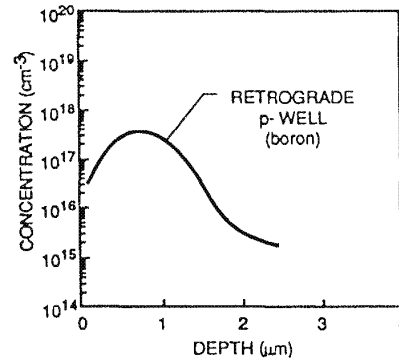


Fig. 16-23 Example of the doping profile of a retrograde *p*-well (boron) implant (400 keV).

punchthrough implant for the NMOSFETs (now using B) are also carried out during this “chained-implantation” procedure.

As discussed in Chap. 10, V_T -adjust implants with retrograde doping profiles have recently been introduced. A high-mass dopant of the same conductivity type is substituted for the ordinary dopant (e.g., indium for boron in NMOSFETs, antimony for phosphorus in PMOSFETs). The higher mass of the dopant reduces its diffusivity, which significantly decreases dopant redistribution during subsequent processes. Thus, the desired as-implanted profile is kept more intact. Such high-mass dopant V_T -adjust implants end up having a reduced

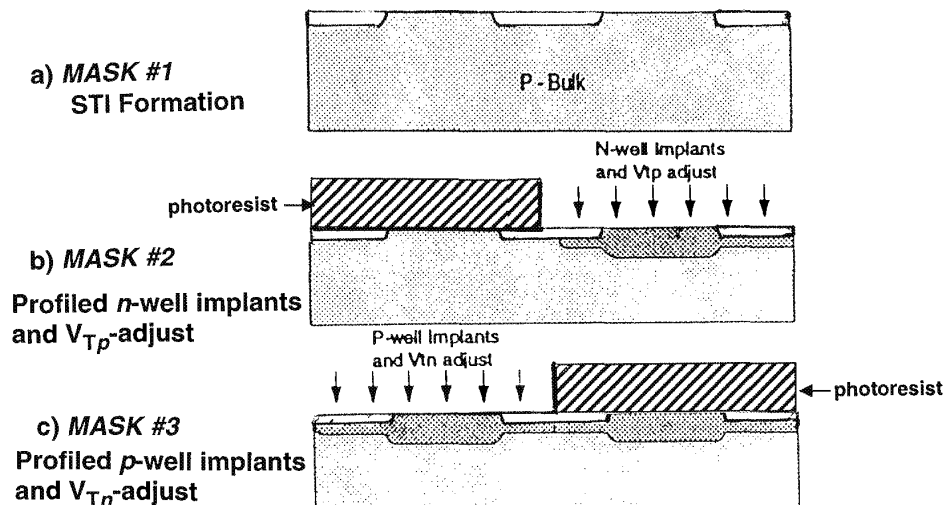


Fig. 16-24 (a) *Mask #1* patterns the shallow-trench isolation features; (b) *Mask #2* defines the *n*-well regions. A high-energy phosphorus (P) implant creates the retrograde *n*-wells, and a lower energy P (or Sb) implant is used to adjust V_{TP} ; (c) *Mask #3* defines the *p*-well regions. A high-energy boron (B) implant creates the retrograde *p*-wells, and a lower energy B (or In) implant is used to adjust V_{TN} .

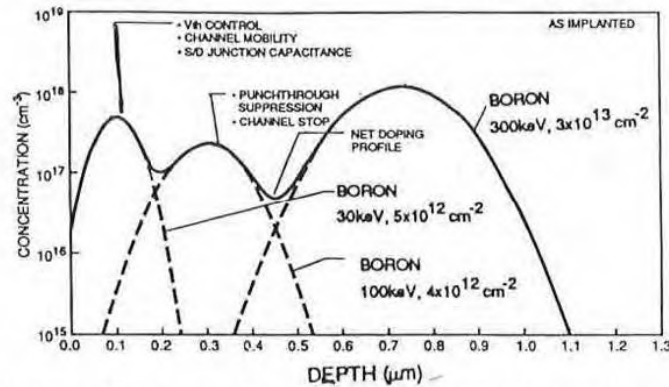


Fig. 16-25 Doping profile in the p -well showing the as-implemented: (a) retrograde p -well implant (B, 300keV); (b) the anti-punchthrough implant (B, 100 keV); and (c) the V_{Tn} implant (B, 30 keV). doping concentration ($\sim 5 \times 10^{16} \text{ cm}^{-2}$) at the interface while at the doping peak (about 80 nm below the oxide interface) the concentration is $\sim 1 \times 10^{18} \text{ cm}^{-2}$. These profiles have been named *super-steep retrograde* (SSR) channel profiles (Chap. 10, Fig. 10-39). Such SSR profiles allow deep-submicron MOSFETs to be fabricated in which short-channel V_T -rolloff and drain-induced barrier lowering (DIBL) effects are significantly suppressed (see Vol. 3).

16.3.4 Formation of the Gate Oxide: The gate oxides of deep-submicron CMOS will continue to scale, with gate oxides for logic CMOS predicted to get thinner than 30 nm (see Chap. 8). The gate oxide, however, will have to prevent boron (from the p^+ -poly) from penetrating into the Si substrate. The addition of nitrogen to the gate oxide has been reported to combat this problem, and so gate dielectric layers may be more like oxynitrides than SiO_2 .¹³ Different techniques have been investigated for incorporating the nitrogen into such films (see Chap. 8), including annealing the as-grown SiO_2 film in N_2O ¹⁸ or NO ,¹³ implanting N into Si and then growing SiO_2 ,¹⁹ or exposing the SiO_2 to a high-density nitrogen discharge and then performing a post-nitridation anneal.²⁰

16.3.5 Formation of the Gate-Stack Structures: Dual-doped polysilicon (i.e., n^+ -doping of NMOS poly gates and p^+ -doping of PMOS poly gates) is needed for 0.25- μm CMOS technologies (and smaller). This permits both the NMOS and PMOS devices to be fabricated as surface channel FETs (see Vol. 3), a necessity for being able to control short-channel effects.

The polysilicon layer is deposited undoped by LPCVD, to a thickness of 300-400 nm. But the selective doping of the appropriate poly structures is not carried out immediately. (Instead, it is performed later, simultaneously with the formation of the heavily doped regions of the source and drain junctions by ion implantation.) Mask #4 is used to pattern the poly layer, and the gate structure is etched with an anisotropic dry-etch step (Fig. 16-26a).

16.3.6 Formation of the Source/Drain Junctions: After the poly gate structure is etched, the formation of the source/drain regions is undertaken. These regions in the substrate have to provide a low-resistance path from the contact to the channel edge. They are formed in two steps. In the

first, so-called *source/drain extensions* (SDEs) are formed. In the previous flow these parts of the S/Ds were termed the *lightly doped areas* of the source and drain. Since they were formed by an ion implantation step, the doping in these regions is characterized in terms of the implant dose (typically 3×10^{13} – 3×10^{14} cm^{-2}). In deep-submicron FETs, the doping concentration is increased in the SDE areas above the values used in the first process flow presented earlier. If the SDEs are also formed by ion implantation, the doping in them can again be characterized by the implant dose, which in the present process flow is raised to about 1×10^{15} cm^{-2} .

However, the primary function of the SDE is no longer to act as a region that reduces the local electric field for the purpose of reducing hot-carrier effects (because this problem is reduced by the smaller power supply voltages used). Instead, the SDE has two other principle roles that must simultaneously be met: 1) to provide a low resistance path from the contact to the channel edge; and 2) to have extremely shallow junction depths (e.g., 50–100 nm for 0.25 μm CMOS, and 36–72 nm for 0.18 μm CMOS), so that short-channel effects can be effectively suppressed. It is imperative that a very high doping concentration be established within such a shallow structure so that the parasitic series resistance of the SDE becomes as small as possible. Unfortunately, forming a shallow junction at the wafer surface with a high doping concentration is a challenging task, especially for B-doped regions. Several techniques are being developed to try to achieve the above goals. Ion implantation at very low energies followed by an RTP anneal has been the most widely used process for forming these drain extension regions (see Sect. 10.6). Other techniques being investigated for this process include *gas immersion laser doping* ([GILD] - see Chap. 8), *plasma immersion doping* (see Chap. 10), and out-diffusion from a layer of deposited doped oxides (e.g., B from a layer of BSG), as described in Refs. 21 and 22.

Regardless of the technique being used, two masks are needed (i.e., *Mask #5* and *Mask #6*, shown in Fig. 16-26b and 16-26c). This allows the NMOS and PMOS source/drain extension (SDE) regions to be selectively doped. If ion implantation is being used, a “halo implant” (to control punch-through) can also be performed within the same pumpdown as the SDE implant step. This “halo implant” is also self-aligned with the channel edge; and it puts dopants at a depth beneath those dopants implanted into the SDE regions. “Halo” implants can be performed either with a 0° tilt angle or a high (30°) tilt angle (see Chap. 10).

The spacer formation is carried out next. Typically LPCVD silicon nitride is used as the spacer material. The deposited nitride layer is then anisotropically etched-back, to form the spacer. At that point the heavily doped, deeper part of the source/drain regions are formed. This is done with ion implantation, using two masks, so the NMOS S/D regions are formed with one implant, and the PMOS S/D regions with the other (*Mask #7* and *Mask #8*, as shown in Figs. 16-27a and 16-27b). Doses of 1 – 5×10^{15} cm^{-2} are used for this step. Note these regions have deeper junction depths than the SDEs (Fig. 16-28). The poly gates are also doped simultaneously by these implants. A single rapid-thermal annealing step is used to activate the implanted dopants in both the SDE and the heavily doped S/D regions.

16.3.7 Salicide Formation: A *salicide* (self-aligned silicide) structure is fabricated next. It consists of a metal silicide formed atop the lines of polysilicon that make up the gates and the local interconnects (akin to the polycide structure described in the first flow). However, in this case it is also formed on the source-drain regions. The silicide on the source/drain regions

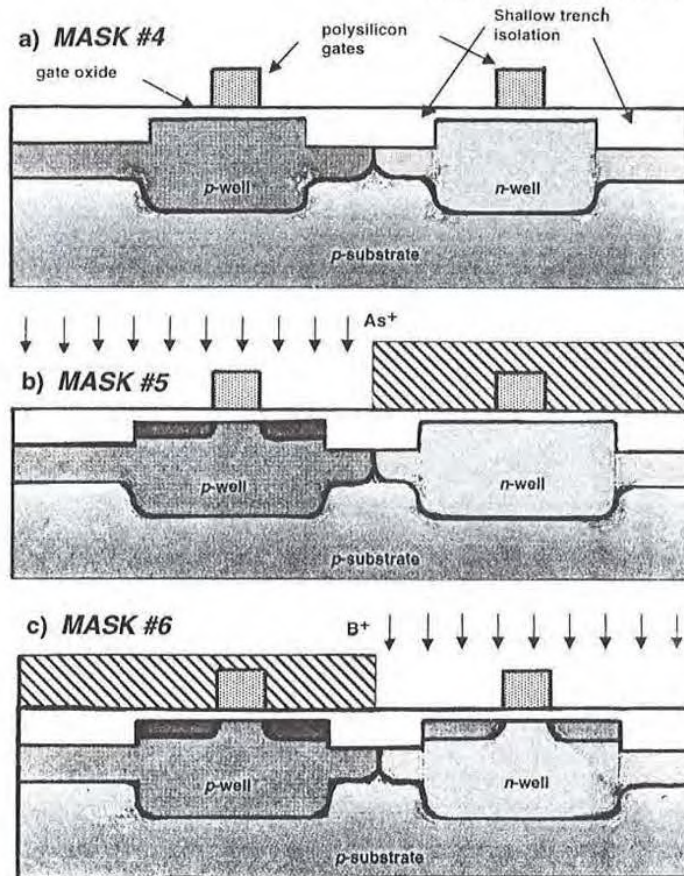


Fig. 16-26 (a) *Mask #4* is used to define the polysilicon gates; (b) *Mask #5* is used to cover the *n*-well regions, so that the NMOS SDEs can be selectively doped with an As implant; (c) *Mask #6* is used to cover the *p*-well regions, so that the PMOS SDEs can be selectively doped with a B implant.

reduces the sheet resistance of the path between the metal contact and the channel edge. The spacers formed on the sidewalls of the poly lines (in the course of fabricating the two parts of the source/drain regions) are now used once again in the salicide formation sequence. Two metals have been used to form such silicides, Ti and Co. They both form silicides with resistivities of 10–15 $\mu\Omega\text{-cm}$. Ti-silicide structures were the first ones implemented, but Co has become more popular as the dimensions have been scaled toward 0.18 μm .²³

The sequence to form the salicide begins with the removal of any oxide on the source/drain regions and the poly lines (Fig. 16-29). Then, Ti or Co is blanket deposited by PVD (sputtering) onto the wafer. A lower temperature thermal step (~650°C) is next used to react the metal and the Si exposed on the substrate and the poly lines. (Use of an RTP step, in which oxygen is

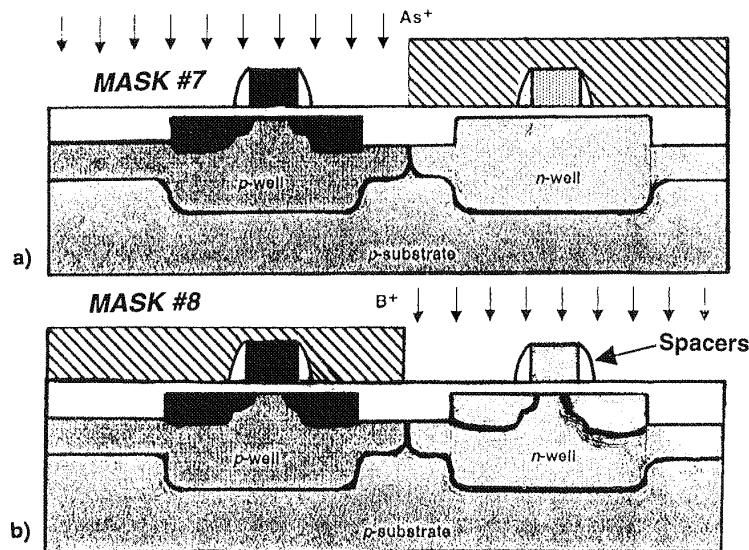


Fig. 16-27 (a) Mask #7 is used to cover the *p*-well regions, so that the heavily doped NMOS S/D regions can be selectively doped with an As implant; (b) Mask #8 is used to cover the *n*-well regions, so that the heavily doped PMOS S/D regions can be selectively doped with a B implant.

excluded from the ambient during the anneal, is a key aspect of this process.) This forms a metastable C49 phase of TiSi_2 . The Ti that lies on either the field oxide or the nitride spacers, in principle, not converted to TiSi_2 during this step. The C49, however, is a metastable, high resistivity material, not yet suitable for the interconnection task. The wafer is then etched in a bath of $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$ that selectively removes only the unreacted Ti, leaving behind the C49 TiSi_2 . A second thermal step using RTP is carried out, this time at a temperature greater than 750°C . This converts the C49-phase TiSi_2 to the more stable, lower resistivity ($\sim 10 \mu\Omega\text{-cm}$) C54-phase TiSi_2 . The thermal steps are carried out by RTP and in an N_2 atmosphere. Details of this sequence are found in Vol. 2, Sect. 3.9.1.1.

When the polysilicon lines become smaller than about $0.5 \mu\text{m}$, the formation of TiSi_2 becomes difficult. The transformation of the C49 phase to the C54 phase becomes the limiting factor. On such small lines, the density of C54 grains is low, and only a small fraction of the TiSi_2 consists of the C54 phase, because it can grow only from the few nuclei available. This problem could be solved by heating the TiSi_2 above 750°C to accelerate the nucleation of the C54 phase. Unfortunately, thin TiSi_2 agglomerates at high temperatures, rendering this solution unworkable. Since CoSi_2 does not exhibit this problem, it has started to replace TiSi_2 . CoSi_2 transformation occurs at a lower temperature (600 to 700°C). Thus, full formation of low-resistance CoSi_2 is achieved before the silicide agglomerates. The Co is also transformed to CoSi_2 by a two-step process. In the first, Co and Si are reacted to form CoSi at 450°C . After selectively etching the unreacted Co away, a second thermal step at 700°C reacts the CoSi with more Si to form CoSi_2 . An even lower resistance cobalt-silicide structure can be obtained by

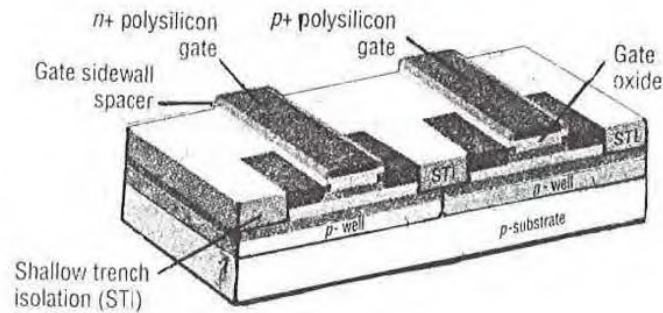


Fig. 16-28 Perspective drawing of a 0.25- μm CMOS structure just prior to the salicide formation process. It depicts the STI isolation structures, the wells, the gates, and the S/D regions. Courtesy of Eaton Corp.

depositing a 20-nm cap layer of TiN onto the Co film before the first thermal step. This TiN cap cuts the sheet resistance from $\sim 10 \Omega/\text{sq}$ to about $5 \Omega/\text{sq}$ by protecting the Co from oxidizing during the first silicidation anneal.²⁵

16.3.8 Premetal Dielectric Deposition and Contact Formation: The premetal dielectric layer is deposited next, much as was done in the first flow. To fill the narrow gaps between adjacent gate structures without voids, a number of dielectric processes may be used including such "sandwich" films as: (1) (PECVD-TEOS/Ozone-TEOS/PECVD-TEOS); or (2) (PECVD-TEOS/SOG/PECVD-TEOS), or an HDP-CVD dielectric film.²⁶ However, for planarization purposes, instead of performing a flow and reflow, this layer is polished by CMP to provide a flat topography. Mask #9 is used to pattern the contact hole openings in the premetal dielectric layer. The contact dry-etch process produces vertical-walled contacts, which must be filled (Fig. 16-30). These contact holes can be filled in various ways, including with CVD-W. In that case, a liner film is deposited first (e.g., TiN deposited by sputtering or CVD).

16.3.9 Interconnect Structure Formation: The technologies for fabricating the interconnect structures used in 0.25- μm CMOS were discussed in Chap. 15. A variety of possible materials and processing approaches can be used to implement a particular multilevel interconnect structure. Figures 16-31 and 15-61 show examples of the kinds of multilevel interconnect structures that are used in deep-submicron ICs.

A number of different materials and technologies can be incorporated when establishing the fabrication sequence for such structures. The exact combination chosen will depend on the IC manufacturer and the application that the chip will be serving. The following are some materials and processes that are used to manufacture such structures: (a) Ti/TiN diffusion barriers; (b) Al:Cu films deposited by sputtering; (c) TaN/Cu seed layers (deposited by sputtering) for Cu interconnects; (d) electroplated Cu films; (e) CMP of the dielectric and metal layers; (f) W-plugs (deposited by CVD); (g) low- k intermetal dielectrics; (h) second- or third-generation spin-on-glasses (SOG) for gap filling; (i) use of high-density plasmas (HDP) to deposit gap-filling

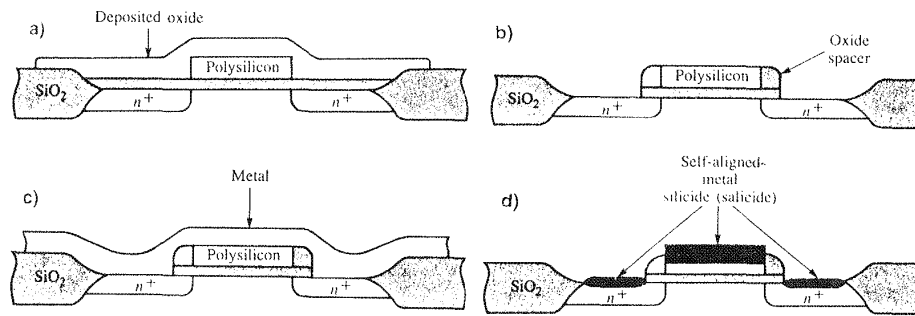


Fig. 16-29 Salicide (self-aligned silicide) processing steps.²⁴ (a) Oxide (or nitride) is deposited following polysilicon definition; (b) structure after etching back, leaving sidewall spacers on the polysilicon; (c) a metal film (Ti or Co) is deposited over the structure and heated. Where the metal is in contact with the silicon substrate, or the polysilicon gate, silicides form; (d) the unreacted metal is selectively etched away, leaving silicide automatically aligned to the gate and source/drain regions. (© 1984 IEEE).

dielectric layers; and (j) single damascene or dual-damascene interconnect structures. Some interconnect structures may use Al films for some interconnect levels, and Cu films for others.²⁷

An example of a 0.18- μm CMOS technology using six levels of metals was described in 1998.²⁸ Both contacts and vias were filled with CVD-W plugs (preceded in each case with a PVD-Ti/CVD-TiN liner film). To make the plugs, the CVD-W was blanket-deposited and then etched back by CMP. The metal interconnect lines consisted of multi-layer films of Ti/TiN/Al:Cu/TiN to achieve low resistance, good electromigration resistance, and low via resistance. The intermetal dielectric is HDP oxide doped with 5.5% fluorine (which reduces the dielectric constant to 3.5 from the 4.2 for undoped-CVD-SiO₂ films) and is planarized by CMP.

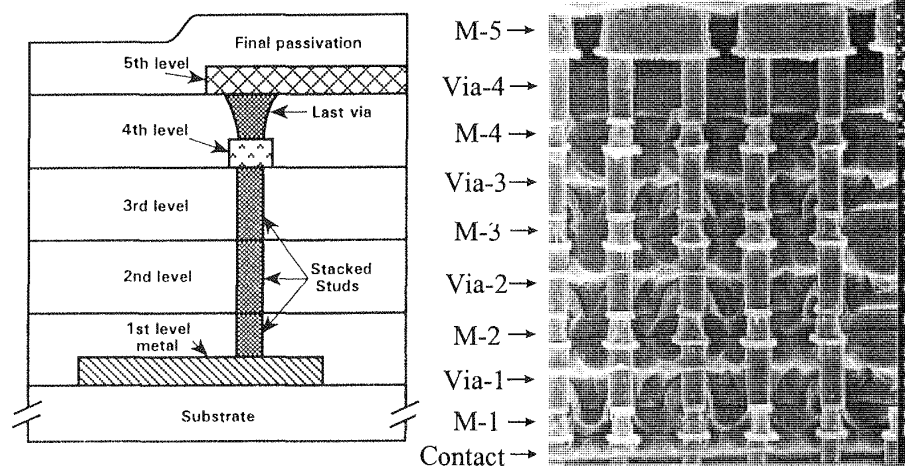


Fig. 16-30 Stacked vias in a 5-metal interconnect, showing filled vertical-walled vias.¹⁵ (© 1998 IEEE).

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PROBLEMS

1. Assume you were asked to design a MOS capacitor to act as a test structure for monitoring the threshold voltage of a silicon-gate NMOSFET. Formulate a detailed process flow of the fabrication steps needed to manufacture such an n -channel MOS capacitor.
2. Compare retrograde-well CMOS and conventional-well CMOS. What are the most important differences in the process technology and the finished device structure? List four advantages that retrograde well technology provides when compared to conventional-well CMOS technology.
3. (a) Why is the $\langle 100 \rangle$ orientation preferred for the Si wafers used to fabricate MOSFET ICs? (b) What are the disadvantages of using a field oxide that is too thin in CMOS ICs? (c) List three functions that the BPSG interlevel dielectric layer performs in CMOS ICs?
4. The following are some of the new technologies used in ULSI CMOS technologies (i.e., technologies in which the minimum feature size is 0.25 μm , or smaller). (a) shallow trench isolation; (b) dual-doped polysilicon; (c) TiSi_2 salicides; (d) shallow source/drain junctions; (e) copper interconnects; (f) low- k dielectrics. List at least two advantages and two problems associated with each of these technologies.
5. In an n -well 1 μm CMOS IC technology, the starting material is a p -type Si wafer with $\langle 100 \rangle$ orientation. The wafer may be either lightly doped bulk p -type Si, or heavily p -doped bulk Si with a lightly p -doped epi layer on its surface. In either case the resistivity of the Si near the surface is about 8 $\Omega\text{-cm}$. The well doping in the n -well near the Si surface is $3 \times 10^{16}/\text{cm}^3$. The gate material of the MOSFETs is a heavily n -doped polysilicon film. The source and drain regions of the NMOSFETs are formed with an As implant of 1×10^{16} As ions/ cm^2 at 50 keV. A channel implant with 8×10^{11} boron ions/ cm^2 is performed through a gate oxide that is 15 nm thick. (a) What would the threshold voltages of the NMOSFETs and PMOSFETs be if the devices were fabricated without implanting the channel with the boron ions? (b) Calculate the threshold voltage that the NMOSFETs and PMOSFETs would exhibit as a result of implanting the boron ions into the channel? (c) Draw a doping profile along the coordinate perpendicular to the surface and passing through (i) the channel region; and (ii) the drain region of both types of FET.
6. Discuss each of the following drawbacks of LOCOS technology: (a) bird's beak encroachment; (b) oxide thinning in narrow field-oxide openings; (c) boron encroachment; (d) non-planarity; (e) process complexity; (f) sensitivity of bird's beak encroachment on pattern geometry.