

CHAPTER II

FUNCTIONAL CELL LAYOUT METHODS

In this chapter, we discuss one-dimensional functional cell design in depth and present a detailed survey and evaluation of all important prior methods for generating layouts in this style.

2.1 FUNCTIONAL CELL DESIGN

First we discuss the general principles of functional cell design. We begin by introducing the original set of assumptions defining this layout style, followed by an extended illustration of these fundamental ideas. Uehara and vanCleemput originally proposed the style of interest, which is illustrated by Fig. 1.3(b) [Uv78]. To simplify the resulting design problem, they made various assumptions, which we list explicitly in Fig. 2.1.

-
1. Static CMOS technology is used.
 2. The pMOS and nMOS subcircuits are series-parallel connections of transistors.
 3. The pMOS and nMOS subcircuits are geometric duals of each other.
 4. The circuit height h is limited to four for performance reasons.
 5. Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.
 6. Complementary pMOS and nMOS transistor pairs are vertically aligned. This allows their gate terminals to be interconnected by vertical polysilicon columns without use of crossovers.
 7. Transistor drain and source terminals are connected by diffusion if the terminals are physically adjacent in the layout, or by metal if they are not adjacent. Only one metal layer is used.
-

Fig. 2.1. The assumptions defining the Uehara-vanCleemput layout style.

Figure 2.2 illustrates the first four assumptions of Fig. 2.1. A static CMOS gate is a transistor circuit composed of two 2-terminal subcircuits of MOS

transistors, a pullup subcircuit of pMOS transistors, the designated terminals of which are V_{DD} and the circuit's output z , and a pulldown subcircuit of nMOS transistors, whose terminals are z and GND. These subcircuits are functional duals, meaning that when there is a conducting path between the terminals of one subcircuit, there is not such a path between the terminals of the other subcircuit. The circuit of Fig. 2.2 is often referred to as a static CMOS "complex" gate. A pMOS transistor is shown in the pullup subcircuit. The circuit between the source and drain terminals of a pMOS transistor is closed, creating a path for current to flow, if the voltage on the gate terminal is low (at the logical 0 voltage, assuming the positive convention); otherwise the circuit is open, preventing the flow of current. Conversely, the circuit between the source and drain terminals of an nMOS transistor in the pulldown circuit is closed, if the voltage on the gate terminal is high (at the logical 1 voltage); otherwise the circuit is open. For example, if the signals c , d , a and g are low, then the path through the pMOS transistors with these signals on their gate terminals connects V_{DD} to the output terminal, and the output signal is logical 1. Note that under these conditions, no path from the output z to GND can be closed because the nMOS dual transistors labeled c , d , a and g open all possible paths to GND. If signals a and b are high, then the output is connected to GND through transistors a and b , and all paths from V_{DD} to the output are open resulting in a logical 0 output. The source terminal of an nMOS transistor in Fig. 2.2 is the

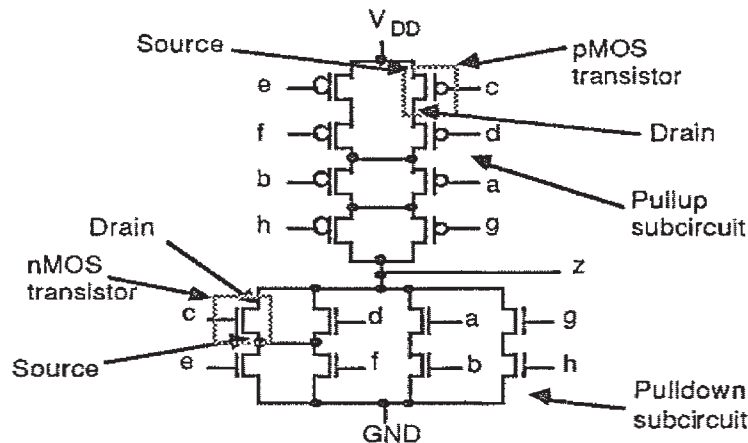


Fig. 2.2. A static CMOS complex gate.

one that is closer to GND, whereas the source terminal of a pMOS transistor is the one closer to the V_{DD} terminal; these two cases are illustrated in Fig. 2.2 for the transistors labeled c .