

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

40672

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

GREENTHREAD, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

3/20/2022

Name

Philip W. John, Jr.

Title

PRESIDENT

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AFFIRMATIVE RECESSION OF PREVIOUS DISCLAIMER

This Application is a continuation or continuation-in-part of previous applications and patents.

Except as explicitly set forth in the prosecution of this application, to the extent any amendments, characterizations, or other assertions made (in this or in any related patent applications or patents, including any parent, sibling, or child) with respect to any art, prior or otherwise, could be construed as a disclaimer of any subject matter supported by the present disclosure of this application, Applicant hereby rescinds and retracts such disclaimer. Applicant also respectfully submits that any prior art considered in any related patent applications or patents, including any parent, sibling, or child, may need to be re-visited.

New claims in this Application may be broader than the claims previously allowed in parent or related applications.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Bill R. Naifeh
Law Office of Bill Naifeh
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Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

RECESSION OF PREVIOUS DISCLAIMER - PAGE 1 of 1

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor	1					Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	G.R. Mohan		Rao				
Residence Information (Select One) • US Residency Non US Residency Active US Military Service							
City	Allen	State/Province	TX	Country of Residence	US		
Mailing Address of Inventor:							
Address 1	1611 Willingham Drive						
Address 2							
City	Allen	State/Province	TX				
Postal Code	72013	Country	US				
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.			
For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	40672		
Email Address	patents@naifeh.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
Attorney Docket Number	GRTD.01.01.DV7	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	40672		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16717950	2019-12-17

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		GRTD.01.01.DV7	
		Application Number			
Title of Invention		SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16717950	Continuation of	15590282	2017-05-09	10510842	2019-11-26
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15590282	Continuation of	14931636	2015-11-03	9647070	2017-05-09
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14931636	Continuation of	14515584	2014-10-16	9190502	2015-11-17
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
14515584	Continuation of	13854319	2013-04-01		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13854319	Continuation of	11622496	2007-01-12	8421195	2013-04-16
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
11622496	Division of	10934915	2004-09-03		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					
Add					

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
Additional Foreign Priority Data may be generated within this form by selecting the Add button. Add			

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant	1		Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
		Clear	
☒ Assignee	Legal Representative under 35 U.S.C. 117		Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	GREENTHREAD, LLC		
Mailing Address Information For Applicant:			
Address 1	4544 Harrys Lane		
Address 2			
City	Dallas	State/Province	TX
Country	US	Postal Code	75229
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				Remove
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				Add

Signature:[Remove](#)

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Bill R. Naifeh, Reg No. 44962/		Date (YYYY-MM-DD)	2020-07-27
First Name	Bill R.	Last Name	Naifeh	Registration Number
				44962
Additional Signature may be generated within this form by selecting the Add button.				Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	GRTD.01.01.DV7
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
16/947,294

RECEIPT DATE / TIME
07/27/2020 08:36:19 PM ET

ATTORNEY DOCKET #
GRTD.01.01.DV7

Title of Invention

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 6907

FILED BY April Reasoner

PATENT CENTER # 60059993

FILING DATE -

CUSTOMER # 40672

FIRST NAMED INVENTOR G.R. Mohan Rao

CORRESPONDENCE ADDRESS -

AUTHORIZED BY Bill Naifeh

Documents

TOTAL DOCUMENTS: 9

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
03_Drawings.pdf	10	Drawings-only black and white line drawings	480 KB
04_Declaration.pdf	1	Oath or Declaration filed	100 KB
05_POA-Greenthread.pdf	1	Power of Attorney	2920 KB
07_RecessionDisclaimer.pdf	1	Miscellaneous Incoming Letter	97 KB
01_ADS.pdf	9	Application Data Sheet	1227 KB
02_ContinuationAppDV7.pdf	16	-	1931 KB
02_ContinuationAppDV7- (1-7)	7	Specification	905 KB

SPEC.pdf				
02_ContinuationAppDV7-CLM.pdf	(8-15)	8	Claims	811 KB
02_ContinuationAppDV7-ABST.pdf	(16-16)	1	Abstract	58 KB
06_EmailAuthorization.pdf		1	Internet Communications Authorized	62 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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Respectfully submitted,

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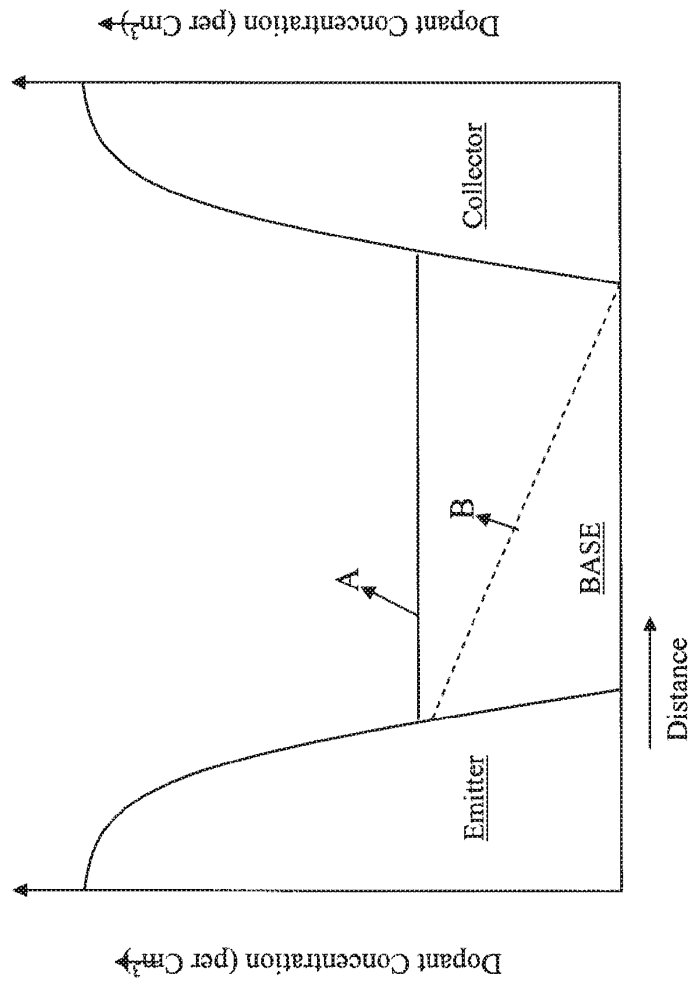


Figure 1 Prior Art

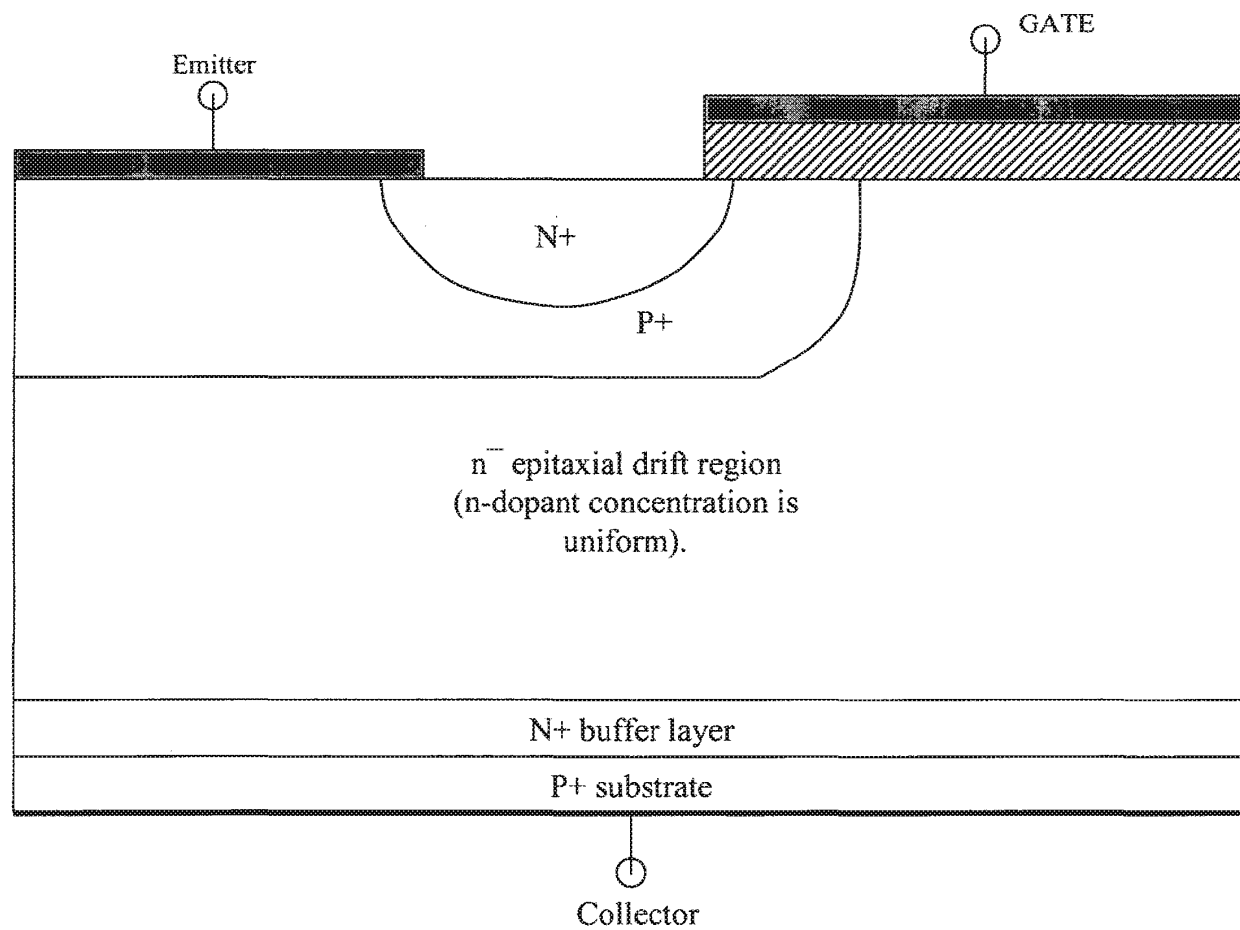
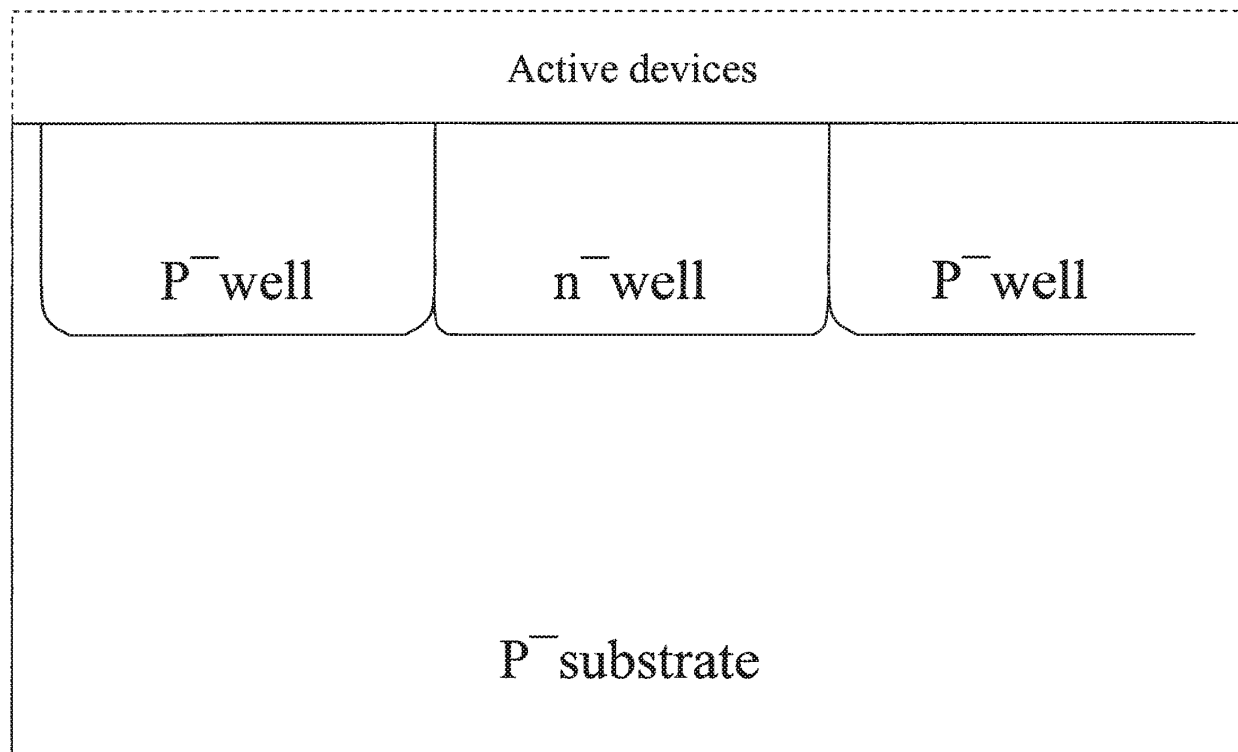


FIGURE 2 Prior art

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FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

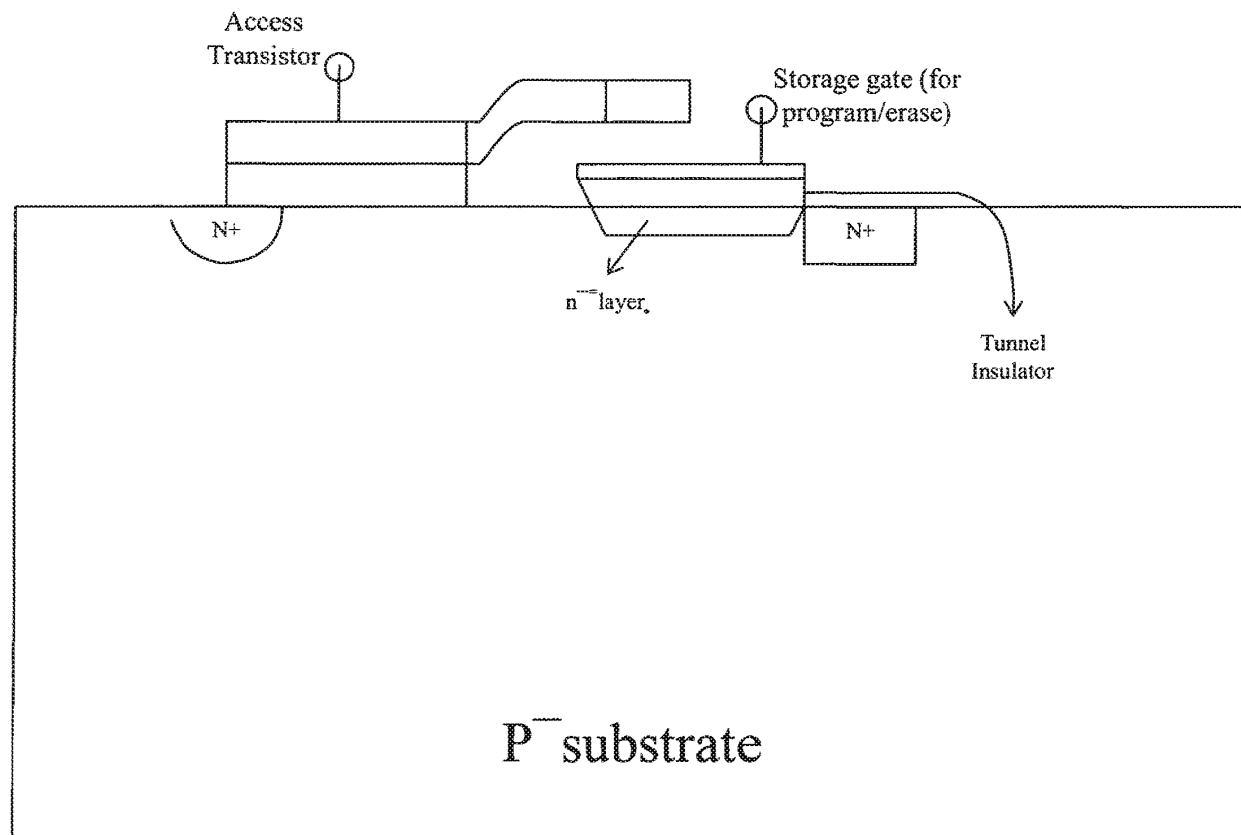


FIGURE 3B Prior art for a two-device EEPROM memory cell

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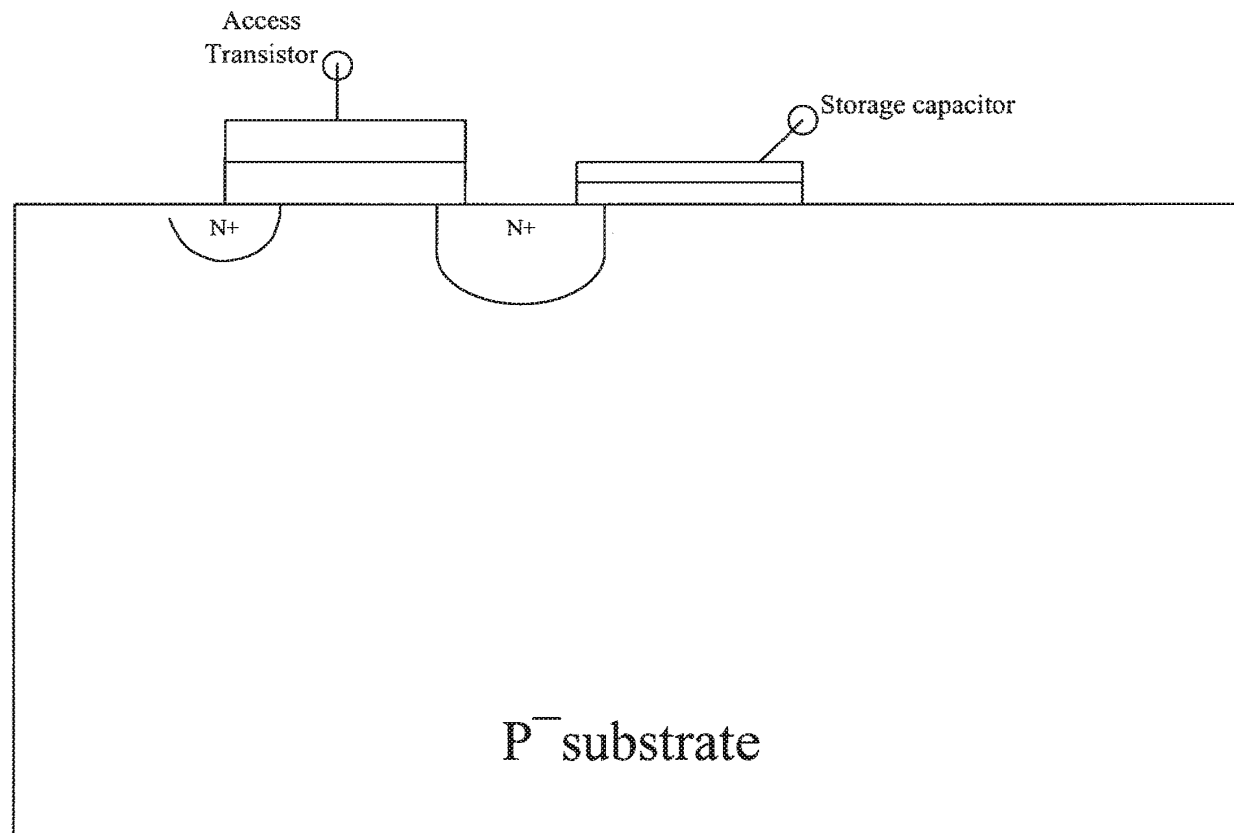


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

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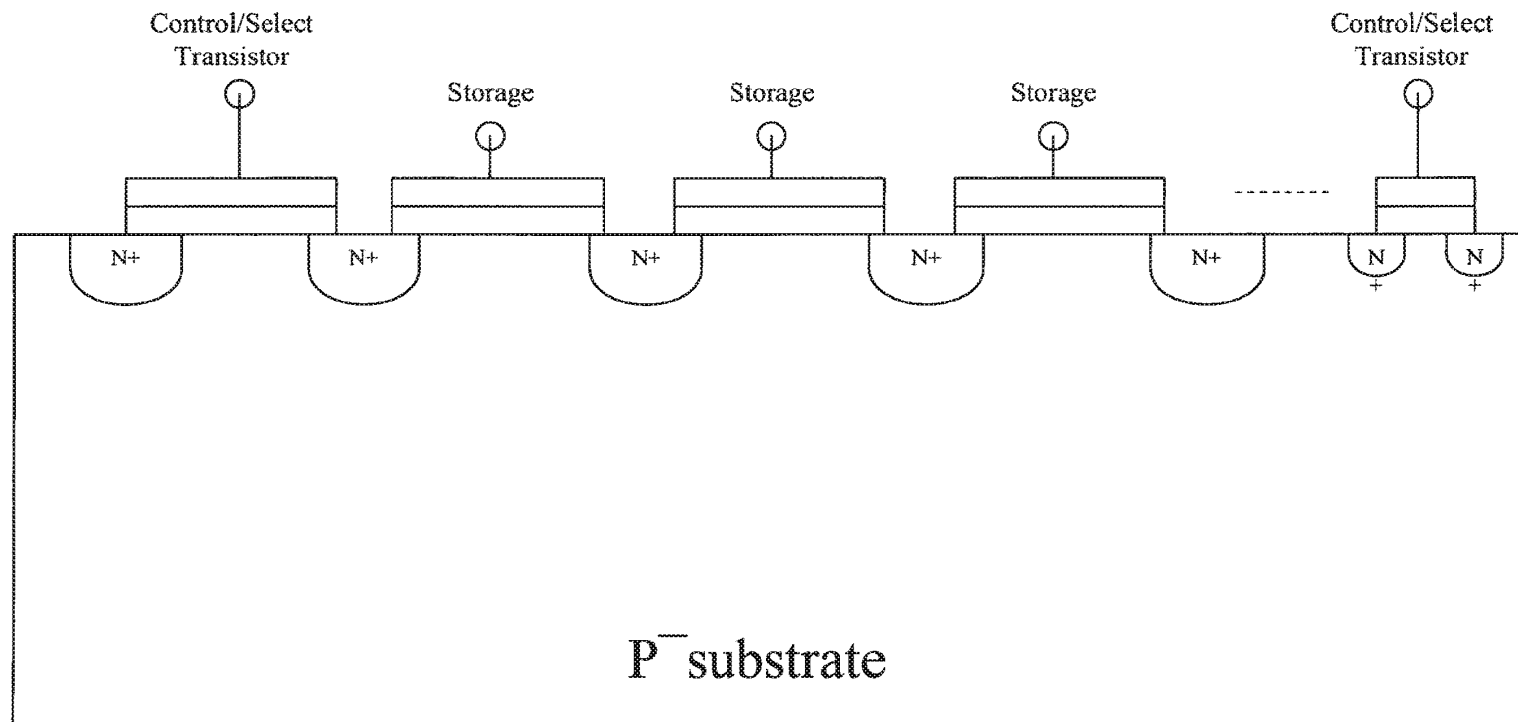


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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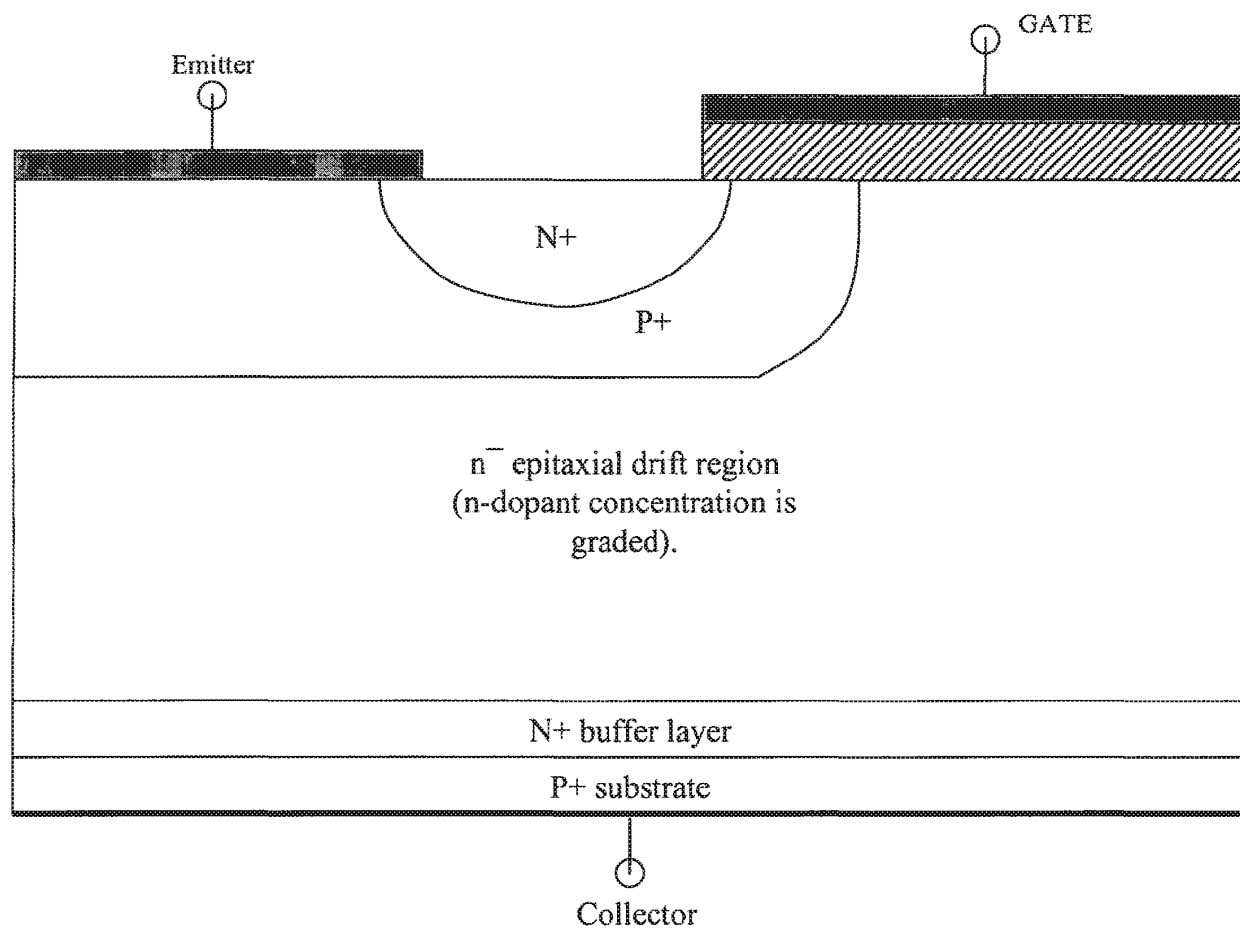


FIGURE 4 A dopant - concentration grinded drift region in a IGBT

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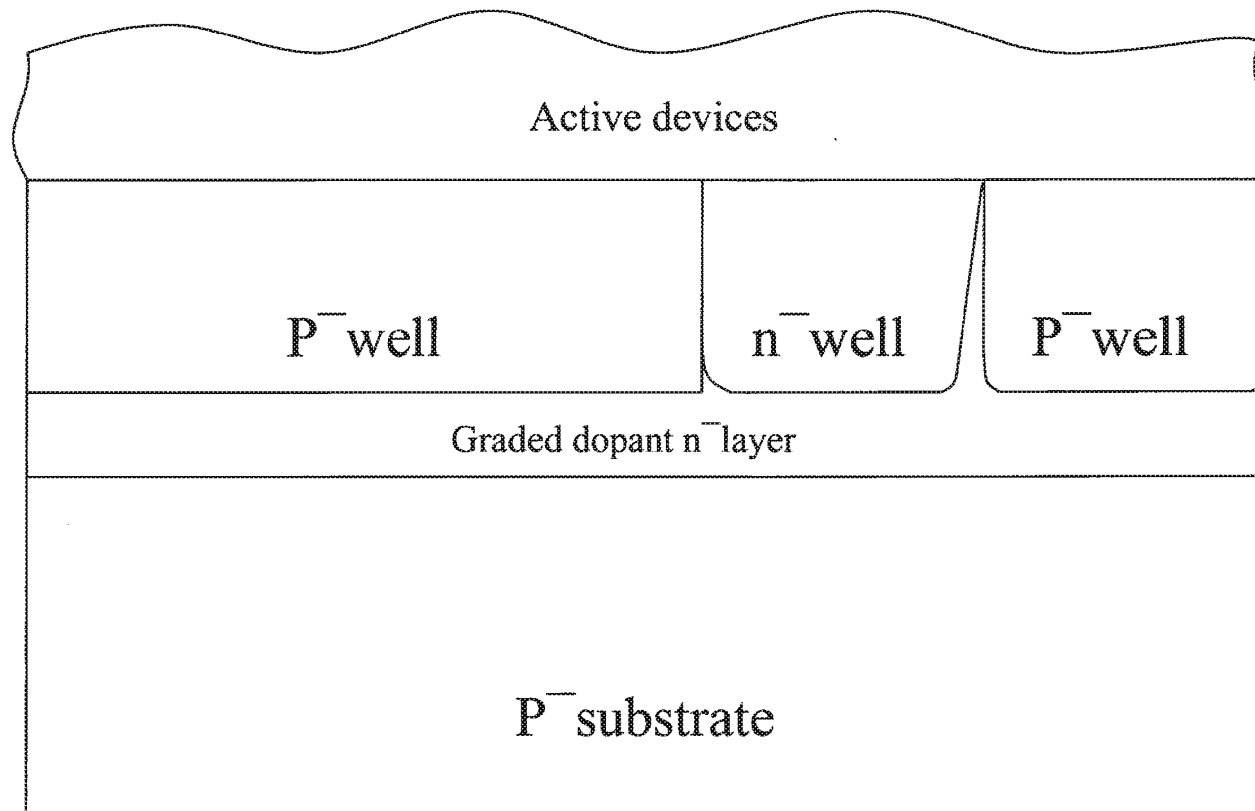
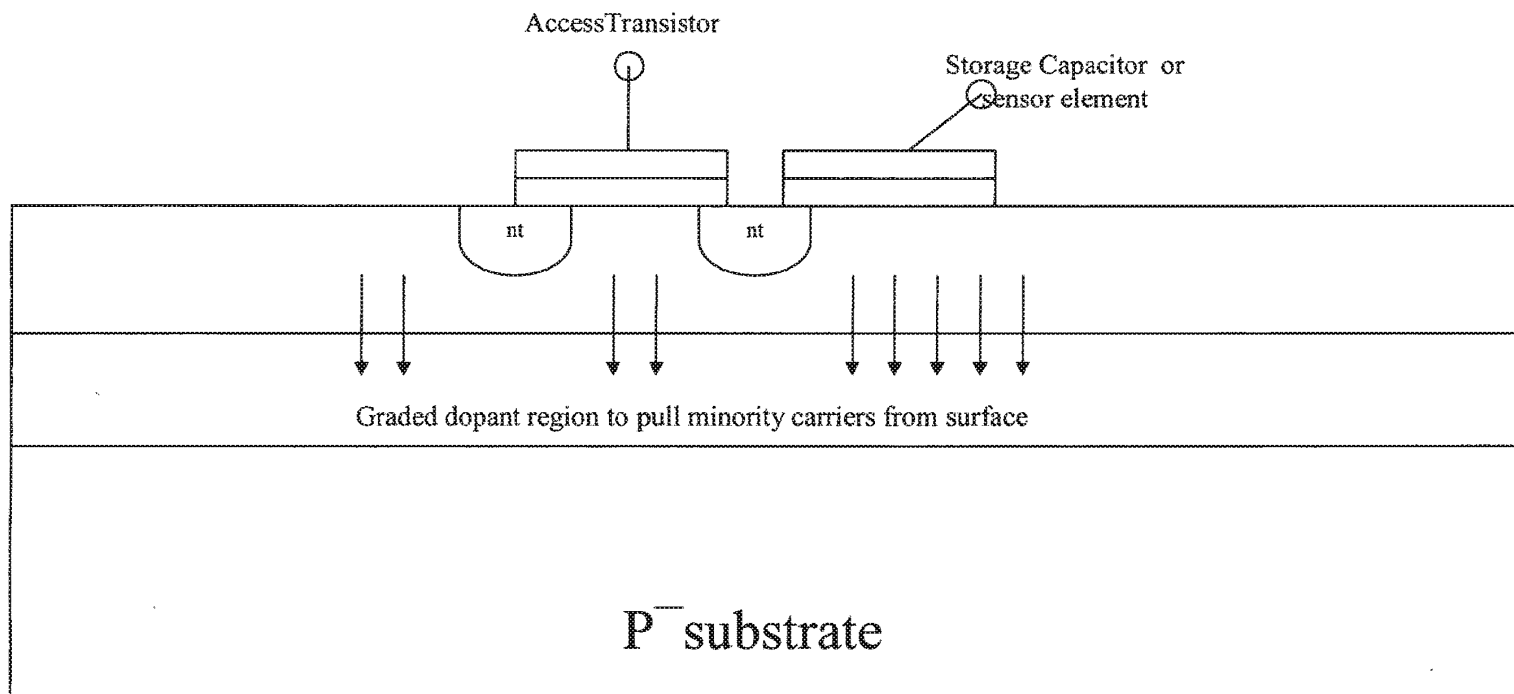


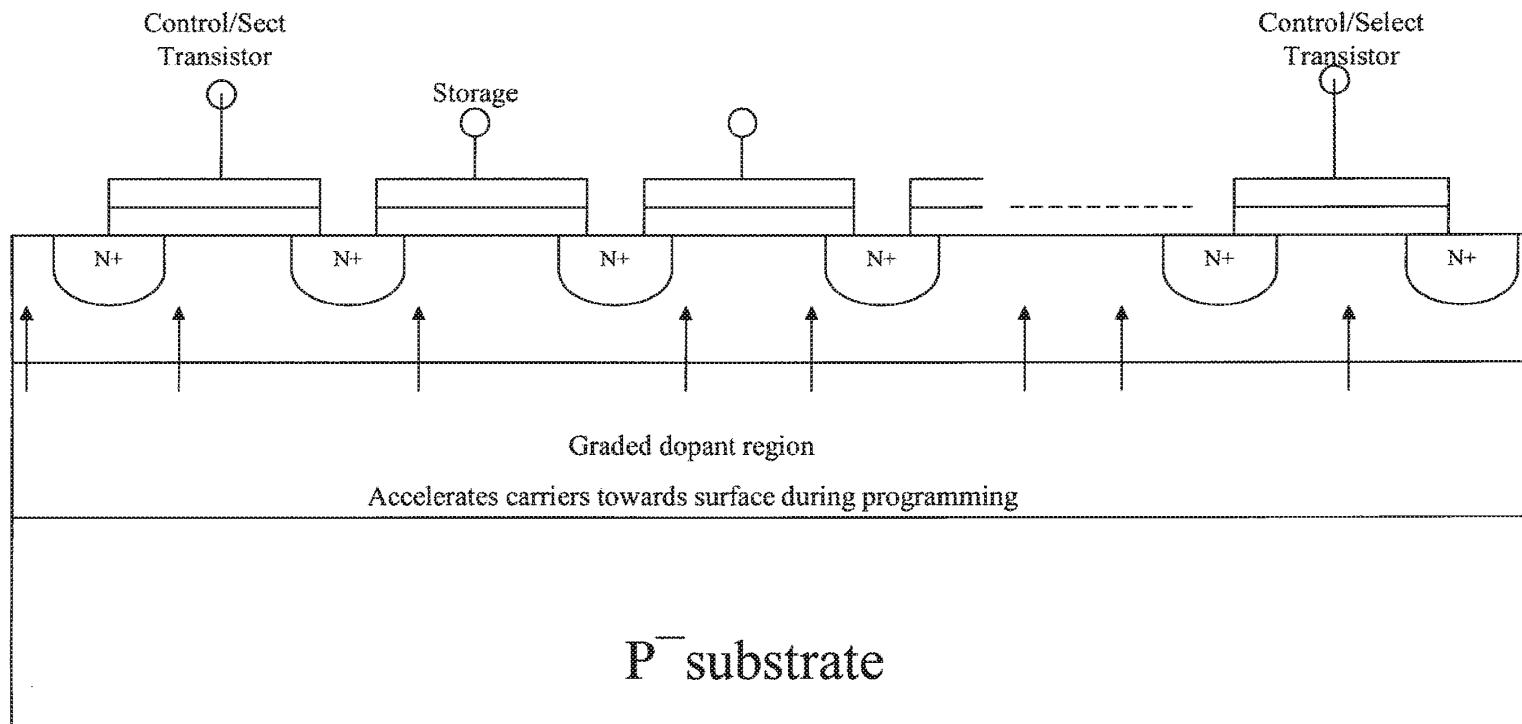
FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

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FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention



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FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent Application No. 16/717,950, filed December 17, 2019, which is a Continuation of U.S. Patent Application No. 15/590,282, filed May 9, 2017, which is a Continuation of U.S. Patent Application No. 14/931,636, filed November 3, 2015, which is a Continuation of U.S. Patent Application No. 14/515,584, filed October 16, 2014, which is a Continuation of U.S. Patent Application No. 13/854,319 filed April 1, 2013, which is a Continuation of 11/622,496, filed January 12, 2007, which is a Divisional of U.S. Patent Application No. 10/934,915, filed September 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

[0003] Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conductions are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

[0004] Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are

subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0006] FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

[0007] FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

[0008] FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁻ well in which p-channel transistors are subsequently fabricated and one p⁻well in which n-channel transistors are subsequently fabricated); FIG 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

[0009] FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

[0010] FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

[0011] The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

[0012] As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region— n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} , holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer

layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

[0013] As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

[0014] One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

[0015] Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

[0016] It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A VLSI semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level having a surface;
 - a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region;
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
 - at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.
2. The VLSI semiconductor device of Claim 1, wherein the substrate is a p-type substrate.
3. The VLSI semiconductor device of Claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
4. The VLSI semiconductor device of Claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.

5. The VLSI semiconductor device of Claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
6. The VLSI semiconductor device of Claim 1, wherein the first active region and second active region are each separated by at least one isolation region.
7. The VLSI semiconductor device of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.
8. The VLSI semiconductor device of Claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.
9. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
10. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.
11. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.
12. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.
14. The VLSI semiconductor device of Claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The VLSI semiconductor device of Claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
16. The VLSI semiconductor device of Claim 1, wherein the device is a flash memory.
17. The VLSI semiconductor device of Claim 1, wherein the device comprises digital logic and capacitors.
18. The VLSI semiconductor device of Claim 1, wherein the device is central processing unit.
19. The VLSI semiconductor device of Claim 1, wherein the device is an image sensor.
20. The VLSI semiconductor device of Claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.
21. A VLSI semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level having a surface;
 - a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;
 - transistors formed in at least one of the first active region or second active region;
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and
 - at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no

active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The VLSI semiconductor device of Claim 21, wherein the substrate is an n-type substrate.

23. The VLSI semiconductor device of Claim 21, wherein the substrate is a p-type substrate.

24. The VLSI semiconductor device of Claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

25. The VLSI semiconductor device of Claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

26. The VLSI semiconductor device of Claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The VLSI semiconductor device of Claim 21, wherein the first active region and second active region are each separated by at least one isolation region.

28. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

29. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

30. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

31. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant region in the well region are both p-type and n-type.
32. The VLSI semiconductor device of Claim 21, wherein the graded dopant is fabricated with an ion implantation process.
33. The VLSI semiconductor device of Claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.
34. The VLSI semiconductor device of Claim 21, wherein the device is a flash memory.
35. The VLSI semiconductor device of Claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.
36. The VLSI semiconductor device of Claim 21, wherein the device is central processing unit.
37. The VLSI semiconductor device of Claim 21, wherein the device is an image sensor.
38. The VLSI semiconductor device of Claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.
39. A semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level;
 - a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.

41. A semiconductor device, comprising:

- a substrate of a first doping type at a first doping level;
- a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
- a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
- transistors formed in at least one of the first active region or second active region; and
- at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

42. A semiconductor device, comprising:

- a substrate of a first doping type at a first doping level;
- a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
- a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

43. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;

a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

44. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of the surface layer;

a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from

the surface layer to an area of the substrate where there are no active regions;
and

at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
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Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
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LEGAL NAME OF INVENTOR Inventor: <u>G.R. Mohan Rao</u> Date (Optional): <u>Sept 30, 2015</u> Signature: <u>G.R. Mohan Rao</u>	
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16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7

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OC000000118944485

Date Mailed: 08/05/2020

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Additional claim fees of \$ **2120** as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
The surcharge is due for any one of:
 - late submission of the basic filing fee, search fee, or examination fee,
 - late submission of inventor's oath or declaration,
 - filing an application that does not contain at least one claim on filing, or
 - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ **75** basic filing fee.
- \$ **80** surcharge.
- \$ **330** search fee.
- \$ **380** examination fee.
- \$ **920** for **4** independent claims over 3.
- \$ **1200** for **24** total claims over 20.

- \$(0) previous unapplied payment amount.
- **\$ 2985** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at
(571) 272-4000 or **(571) 272-4200** or **1-888-786-0101**.

/Itan/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/947,294	07/27/2020	2812	0.00	GRTD.01.01.DV7	44	7

CONFIRMATION NO. 6907

FILING RECEIPT



0000000118944484

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

Date Mailed: 08/05/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

G.R. Mohan Rao, Allen, TX;

Applicant(s)

GREENTHREAD, LLC, Dallas, TX;

Power of Attorney: The patent practitioners associated with Customer Number 40672

Domestic Priority data as claimed by applicant

This application is a CON of 16/717,950 12/17/2019 PAT 10734481
which is a CON of 15/590,282 05/09/2017 PAT 10510842
which is a CON of 14/931,636 11/03/2015 PAT 9647070
which is a CON of 14/515,584 10/16/2014 PAT 9190502
which is a CON of 13/854,319 04/01/2013 ABN
which is a CON of 11/622,496 01/12/2007 PAT 8421195
which is a DIV of 10/934,915 09/03/2004 ABN

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/03/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/947,294**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative,

page 2 of 4

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/947,294				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A				
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	330		N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	44	minus 20 = * 24	x 50 =	1200	OR					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7	minus 3 = * 4	x 230 =	920						
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00						
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	2905		TOTAL				
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

UNITED STATES PATENT AND TRADEMARK OFFICE
COMMISSIONER FOR PATENTS
P.O.BOX 1450
ALEXANDRIA VA 22313-1451

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U.S. POSTAGE PAID
POSTEDIGITAL
NNNNN

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380



**Courtesy Reminder for
Application Serial No: 16/947,294**

Attorney Docket No: GRTD.01.01.DV7

Customer Number: 40672

Date of Electronic Notification: 08/05/2020

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

patents@naifeh.com

To view your correspondence online or update your email addresses, please visit us anytime at **<https://ppair-my.uspto.gov/pair/PrivatePair>**.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	G.R. Mohan Rao	§	Confirmation	6907
		§	No.	
		§		
Serial No:	16/947,294	§	Group Art Unit:	2812
		§		
Filed:	July 27, 2020	§	Examiner:	N/A
		§		

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

Via EFS

Mail Stop Missing Parts
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

RESPONSE TO NOTICE TO FILE MISSING PARTS

Dear Sir:

In Response to the Notice to File Missing Parts, mailed October 5, 2020, in the above application, Applicant hereby submits payment of the following fees:

Basic filing fee	\$ 75
Surcharge	\$ 80
Search fee	\$ 330
Examination fee	\$ 380
<u>Additional claim fees</u>	<u>\$2120</u>
Total Filing Fees	\$2985

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

Electronic Patent Application Fee Transmittal				
Application Number:		16947294		
Filing Date:		27-Jul-2020		
Title of Invention:		SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
First Named Inventor/Applicant Name:		G.R. Mohan Rao		
Filer:		Bill Naifeh/April Reasoner		
Attorney Docket Number:		GRTD.01.01.DV7		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	24	50	1200
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	4	230	920
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
LATE FILING FEE FOR OATH OR DECLARATION	2051	1	80	80
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2985

Electronic Acknowledgement Receipt	
EFS ID:	40672359
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Bill Naifeh/April Reasoner
Filer Authorized By:	Bill Naifeh
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	25-SEP-2020
Filing Date:	27-JUL-2020
Time Stamp:	14:43:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$2985
RAM confirmation Number	E20209OE43553297
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	GRTD-DV7_PayFees.pdf	239654	no	1
			6d5cb8beba15c7f385591146570e3692a0698df		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	40542	no	2
			d2a29a44d26086dd0df61801748cf9e5e4dc744		
Warnings:					
Information:					
Total Files Size (in bytes):			280196		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

RECEIVED
CENTRAL FAX CENTER

SEP 28 2020

Customer No. 000040672
Attorney Docket No. GRTD.01.01.DV7**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor:	G.R. Mohan Rao	§	Confirmation	6907
		§	No.	
Serial No:	16/947,294	§	Group Art Unit:	2812
		§		
Filed:	July 27, 2020	§	Examiner:	N/A
		§		
For:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS			

Via Facsimile
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Certificate of Facsimile Transmission

I hereby certify that this correspondence is being submitted to the U.S. Patent Office via facsimile transmission to (571) 273-8300 on September 28, 2020.

/April Reasoner/

April Reasoner, Paralegal

2020 OCT -1 PM 12:31

USPTO
RECEIPTS ACCOUNTING
DIVISION**NOTIFICATION OF LOSS OF ENTITLEMENT TO SMALL ENTITY STATUS**

Dear Sir:

Applicant hereby notifies the Office of its loss of entitlement to small entity status.

On September 25, 2020, Applicant submitted payment of fees in the amount of \$2985 in response to the Notice to File Missing Parts.

Applicant hereby submits payment of the additional fees due in the amount of \$3135 as follows:

Basic filing fee	\$ 300
Surcharge	\$ 160
Search Fee	\$ 660
Exam Fee	\$ 760
<u>Additional claim fees</u>	<u>\$4240</u>
Total Fees	\$6120
<u>Amount Paid</u>	<u>- \$2985</u>
Total Amount Due	\$3135

Customer No. 000040672
Attorney Docket No. GRTD.01.01.DV7

Attached is Form PTO-2038 Credit Card Payment Form for payment of the additional fees.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

RECEIVED
CENTRAL FAX CENTER 161

SEP 28 2020

FAX COVER SHEET

TO	USPTO
COMPANY	
FAX NUMBER	15712738300
FROM	Bill Naifeh
DATE	2020-09-29 01:12:06 GMT
RE	Entity Status and Payment of Fees

COVER MESSAGE

Dear Sir:
Attached is a Notification of Loss of Entitlement to Small Entity Status, along with
a cc authorization form for payment of the additional fees due.
Regards,
April Reasoner

WWW.EFAX.COM

PAGE 1/4 * RCVD AT 9/28/2020 9:12:23 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/27 * DNIS:2738300 * CSID:12145502542 * ANI:4803836933 * DURATION (mm-ss):02-35



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/947,294	07/27/2020	2812	2985	GRTD.01.01.DV7	44	7

CONFIRMATION NO. 6907
UPDATED FILING RECEIPT



0000000120229081

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

Date Mailed: 09/29/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

G.R. Mohan Rao, Allen, TX;

Applicant(s)

GREENTHREAD, LLC, Dallas, TX;

Power of Attorney: The patent practitioners associated with Customer Number 40672

Domestic Priority data as claimed by applicant

This application is a CON of 16/717,950 12/17/2019 PAT 10734481
which is a CON of 15/590,282 05/09/2017 PAT 10510842
which is a CON of 14/931,636 11/03/2015 PAT 9647070
which is a CON of 14/515,584 10/16/2014 PAT 9190502
which is a CON of 13/854,319 04/01/2013 ABN
which is a CON of 11/622,496 01/12/2007 PAT 8421195
which is a DIV of 10/934,915 09/03/2004 ABN

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/03/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/947,294**

Projected Publication Date: 01/07/2021

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative,

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this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/947,294				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A				
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	330		N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	44	minus 20 = *	24	x 50 =	1200	OR				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7	minus 3 = *	4	x 230 =	920					
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00						
				TOTAL	2905	TOTAL				
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4001864	A	1997-01-04	Gibbons	
	2	4160985	A	1979-07-10	Kamins et al.	
	3	4347654	A	1982-09-07	Allen et al.	
	4	4481522	A	1984-11-06	Jastrzebski et al.	
	5	4866000	A	1989-09-12	Okita	
	6	5029277	A	1991-07-02	Kane	
	7	5130262	A	1992-07-14	Masquelier et al.	
	8	5213988	A	1993-05-25	Yamauchi et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Examiner Name	NA	
Attorney Docket Number	GRTD.01.01.DV7	

9	5262345	A	1993-11-16	Nasser et al.	
10	5329144	A	1994-07-12	Luryi	
11	5448087	A	1995-09-05	Streit et al.	
12	5480816	A	1996-01-02	Uga et al.	
13	5496746	A	1996-03-05	Matthews	
14	5517052	A	1996-05-14	Ishaque	
15	5569612	A	1996-10-29	Frisina et al.	
16	5575862	A	1996-11-19	Nishida	
17	5637898	A	1997-06-10	Baliga	
18	5797999	A	1998-08-25	Sannomiya et al.	
19	5888857	A	1999-03-30	Zhang et al.	

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Attorney Docket Number	GRTD.01.01.DV7	

20	5973575	A	1999-10-26	Kamogawa et al.	
21	6211028	B1	2001-04-03	Tsai et al.	
22	6310366	B1	2001-10-30	Rhodes et al.	
23	RE37441	E	2001-11-13	Yamazaki	
24	6452086	B1	2002-09-17	Muller	
25	6465862	B1	2002-10-15	Harris	
26	6472715	B1	2002-10-29	Liu et al.	
27	6670544	B2	2003-12-30	Kibbel et al	
28	6683343	B2	2004-01-27	Matsudai et al.	
29	6696314	B2	2004-02-24	Rhodes	
30	6706550	B2	2004-03-16	Lee et al.	

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31	6713813	B2	2004-03-30	Marchant	
32	6720622	B1	2004-04-13	Yu	
33	6737722	B2	2004-05-18	Yamamoto et al.	
34	6744117	B2	2004-06-01	Dragon et al.	
35	6747883	B2	2004-06-08	Yasumura	
36	6753202	B2	2004-06-22	Chen et al.	
37	6754093	B2	2004-06-22	Lien	
38	6756616	B2	2004-06-29	Rhodes	
39	6780713	B2	2004-08-24	Bromberger et al.	
40	6831292	B2	2004-12-14	Currie et al.	
41	6878603	B2	2005-04-12	Bromberger et al.	

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42	6921946	B2	2005-07-26	Kenney et al.	
43	6933215	B2	2005-08-23	Bromberger et al.	
44	7064385	B2	2006-06-20	Dudek et al.	
45	7115925	B2	2006-10-03	Rhodes	
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47	7307327	B2	2007-12-11	Bahl et al.	
48	7504692	B2	2009-03-17	Dudek et al.	
49	8164124	B2	2012-04-24	Liu et al.	
50	8421195	B2	2013-04-16	Rao	
51	9190502	B2	2015-11-17	Rao	
52	9647070	B2	2017-05-09	Rao	

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Attorney Docket Number	GRTD.01.01.DV7

53	10510842	B2	2019-12-17	Rao	
54	10734481	B2	2020-08-04	Rao	
55	4684971	A	1987-08-04	Payne	

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	1	20010040622	A1	2001-11-15	Maruyama	
	2	20020056883	A1	2002-05-16	Baliga	
	3	20020074585	A1	2002-06-20	Tsang et al.	
	4	20020084430	A1	2002-07-04	Bamji et al.	
	5	20020093281	A1	2002-07-18	Cathey	
	6	20020102783	A1	2002-08-01	Fujimoto et al.	

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Art Unit	2892	
Examiner Name	NA	
Attorney Docket Number	GRTD.01.01.DV7	

7	20020134419	A1	2002-09-26	Macris	
8	20030026126	A1	2003-02-06	Jemura	
9	20030030488	A1	2003-02-13	Huetling et al.	
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11	20040027753	A1	2004-02-12	Friedrichs et al.	
12	20040063288	A1	2004-04-01	Kenney et al.	
13	20060113592	A1	2006-06-01	Pendharkar et al.	
14	20070045682	A1	2007-03-01	Hong	
15	20120048462	A1	2013-02-28	Lee	
16	20130001661	A1	2013-01-03	Mao et al.	
17	20150200314	A1	2015-07-16	Webster	

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	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

18	20030183856	A1	2003-10-02	Wieczorek
19	20080142899	A1	2008-06-19	Morris

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	1	P.D. Moor, Advanced CMOS-based pixel sensors, https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEEimecPdM.pdf , 2011, 41 pages	
	2	E. Parton, CMOS Sensors, Laser Focus World, http://www.laserfocusworld.com/articles/print/volume-49/issue-10/features/cmos-sensors-cmos-based-specialty-imagers-reach-new-performance-levels.html , Oct. 14, 2013, 5 pages	
	3	Z. Cao, Design of Pixel for High Speed CMOS Image Sensors, http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/07-11_072-Cao_papers.pdf , 4 pages	
	4	M. Tanenbaum, BSTJ: Diffused Emitter and Base Silicon Transistors, The Bell System Technical Journal, Jan. 1956, 22 pages, vol. XXXV, https://archive.org/details/bstj35-1-1	

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Filing Date	2020-07-27
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Art Unit	2892
Examiner Name	NA
Attorney Docket Number	GRTD.01.01.DV7

5	IMEC Image Sensors and Vision Systems, http://www2.imec.be/content/user/File/Brochures/cmos%20imagers%20brochure-april26.pdf , Apr. 2014, 2 pages
6	A.S. Grove, Physics and Technology of Semiconductor Devices, John Wiley Sons, Inc., New York, Nov. 1967.
7	W. Murray Bullis and W. R. Runyan, Influence of Mobility and Lifetime Variations on Drift-Field Effects in Silicon-Junction Devices, IEEE Transactions on Electron Devices, vol. Ed-14, No. 2, Feb. 1967
8	Berinder Brar et al., Herb's Bipolar Transistors, IEEE Transactions on Electron Devices, vol. 48, No. 11, Nov. 2001

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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Bill R. Naifeh, Reg. No. 44962/	Date (YYYY-MM-DD)	2020-09-29
Name/Print	Bill R. Naifeh	Registration Number	44962

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EFS ID:	40710276
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Bill Naifeh/April Reasoner
Filer Authorized By:	Bill Naifeh
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	29-SEP-2020
Filing Date:	27-JUL-2020
Time Stamp:	19:14:47
Application Type:	Utility under 35 USC 111(a)

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Information:					
Total Files Size (in bytes):			1064314		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	G.R. Mohan Rao	§	Conf. No.	6907
		§		
Serial No:	16/947,294	§	Group Art Unit:	2892
		§		
Filed:	July 27, 2020	§	Examiner:	NA
		§		

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

Via EFS

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313.1450

INFORMATION DISCLOSURE STATEMENT (IDS)

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, the attention of the United States Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of the above-identified application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in this Information Disclosure Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

Applicant has not submitted copies of each cited U.S. patent and U.S. patent application in accordance with 37 C.F.R. § 1.98(a)(2).

Applicant has not submitted copies of each cited non-patent literature document listed in the attached Information Disclosure Statement in accordance with 37 C.F.R. 1.98(d). Copies of the non-patent literature documents were submitted to the Office in earlier Application No. 16/717,950, which is relied on for an earlier effective filing date.

This Information Disclosure Statement is made pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office Action on the merits.

It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98, and the Examiner is respectfully requested to consider the listed references.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Bill R. Naifeh
Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :67142

Sale Accounting Date:10/05/2020

Sale Item Reference Number

16947294

Effective Date

09/28/2020

Document Number

I202005B53483009

Fee Code

1599

Fee Code Description

MAINTENANCE/PETITION
INTERNAL FEE CODE

Amount Paid

\$3,135.00

Payment Method

Credit Card



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7

CONFIRMATION NO. 6907

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

PUBLICATION NOTICE



OC000000122504813

Title:SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Publication No.US-2021-0005716-A1

Publication Date:01/07/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7	6907
40672	7590	01/15/2021	EXAMINER	
BILL R. NAIFEH PO BOX 803423 DALLAS, TX 75380				
			ART UNIT	PAPER NUMBER
			2892	
			NOTIFICATION DATE	DELIVERY MODE
			01/15/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@naifeh.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of :
Rao, G.R. Mohan :
Application No. 16/947,294 : **DECISION ON PETITION**
Filed: July 27, 2020 :
For: SEMICONDUCTOR DEVICES WITH :
GRADED DOPANT REGIONS :

This is a notice in response to the request filed on September 28, 2020, a request for acceptance of a fee deficiency submission under 37 CFR 1.28(c).

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. **1098 Off. Gaz. Pat. Office 502 (January 3, 1989)**. Therefore, nothing in this Notice is intended to imply that an investigation was done.

The fee deficiency submission under 37 CFR 1.28(c) is **NOT ACCEPTED**.

Applicant should note that 37 CFR 1.28(c) states in part: If status as a small entity is established in good faith, and fees as a small entity are paid in good faith, in any application or patent, and it is later discovered that such status as a small entity was established in error, or that through error the Office was not notified of a loss of entitlement to small entity status as required by § 1.27(g)(2), the error will be excused upon compliance with the separate submission and itemization. See 37 CFR 1.28(c)(2)(ii).

The itemization must include the following information:

- (A) Each particular type of fee that was erroneously paid as a small entity, (e.g., basic statutory filing fee, two-month extension of time fee) along with the current fee amount for a non-small entity;
- (B) The small entity fee actually paid, and when. This will permit the Office to differentiate, for example, between two one-month extension of time fees erroneously paid as a small entity but on different dates;
- (C) The deficiency owed amount (for each fee erroneously paid); and
- (D) The total deficiency payment owed, which is the sum or total of the individual deficiency owed amounts set forth in paragraph (c)(2)(ii)(C) of this section.

An itemization chart was not included with the request. Any renewed request must include the information in item(s) A-D above.

Applicant is given **ONE MONTH** to submit a complete listing of all the fees erroneously paid as a small entity and the total fee deficiency to avoid non acceptance of the present fee deficiency paper. This time period is not extendable under 37 CFR 1.136(a).

Further correspondence with respect to this matter should be addressed as follows:

By Mail: Mail Stop PETITION
 Commissioner for Patents
 P. O. Box 1450
 Alexandria, VA 22313-1450

By FAX: (571) 273-8300
 ATTN: Office of Petitions

By Hand: U. S. Patent and Trademark Office
 Customer Service Window, Mail Stop Petitions
 Randolph Building
 401 Dulany Street
 Alexandria, VA 22314

By Internet: EFS-Web¹

Telephone inquiries regarding this matter should be directed to undersigned at (571) 272-1058.

/Angela Walker/
Angela Walker
Paralegal Specialist
Office of Petitions

¹ www.uspto.gov/ebs/efs_help.html (for help using EFS-Web call the Patent Electronic Business Center at (866) 217-9197)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	G.R. Mohan Rao	§	Confirmation	6907
		§	No.	
		§		
Serial No:	16/947,294	§	Group Art Unit:	2812
		§		
Filed:	July 27, 2020	§	Examiner:	N/A
		§		

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

Via EFS-Web

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

RESPONSE TO DECISION ON PETITION AND
RENEWED NOTIFICATION OF LOSS OF ENTITLEMENT TO SMALL ENTITY STATUS

Dear Sir:

In response to the Decision on Petition mailed January 15, 2021, Applicant hereby submits the following itemization:

<u>Type of Fee Paid</u>	<u>Amount of Fee Paid</u>	<u>Date Paid</u>	<u>Deficiency Owed</u>
Basic filing fee	\$75.00	9/25/2020	\$225.00
Surcharge	\$80.00	9/25/2020	\$80.00
Search fee	\$330.00	9/25/2020	\$330.00
Exam Fee	\$380.00	9/25/2020	\$380.00
Additional claims fees	\$2,120.00	9/25/2020	\$2,120.00
Total Deficiency Payment Owed and Paid			\$3,135.00

Applicant hereby notifies the Office of its loss of entitlement to small entity status.

On September 25, 2020, Applicant submitted payment of fees in the amount of \$2,985.00 in response to the Notice to File Missing Parts.

On September 28, 2020, Applicant filed a Notification of Loss of Entitlement to Small Entity Statement and submitted payment of \$3,135.00 via Credit Card. On October 5, 2020, the Patent Office charged the Credit Card in the amount of \$3,135.00 for the deficiency fee payment owed. Therefore, no further fees are due.

Applicant hereby requests acceptance of this Response and Renewed Notification of Loss Entitlement to Small Entity Status.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

Electronic Acknowledgement Receipt	
EFS ID:	41719937
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Bill Naifeh/April Reasoner
Filer Authorized By:	Bill Naifeh
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	22-JAN-2021
Filing Date:	27-JUL-2020
Time Stamp:	14:57:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Notification of loss of entitlement to small entity status	ResponsetoDecision.pdf	19938	no	2
			78cd0f143b8a8a8f55848a65adc2cd020b2db564		

Warnings:

Information:	
Total Files Size (in bytes):	19938
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C41722

Sale Accounting Date:02/09/2021

Sale Item Reference Number	Effective Date
16947294	09/28/2020

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202129F04190768	1461	1.28(C) SUBMISSIONS - APPLIC FILE FEE	\$3,135.00	Salea



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7	6907
40672	7590	02/12/2021	EXAMINER	
BILL R. NAIFEH PO BOX 803423 DALLAS, TX 75380				
			ART UNIT	PAPER NUMBER
			2892	
			NOTIFICATION DATE	DELIVERY MODE
			02/12/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@naifeh.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of :
Rao, G.R. Mohan :
Application No. 16/947,294 : **DECISION ON PETITION**
Filed: 27 Jul 2020 :
For: SEMICONDUCTOR DEVICES WITH :
GRADED DOPANT REGIONS :

This is a notice regarding your renewed request filed January 22, 2021, for acceptance of a fee deficiency submission under 37 CFR 1.28(c).

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. **1098 Off. Gaz. Pat. Office 502 (January 3, 1989)**. Therefore, nothing in this Notice is intended to imply that an investigation was done.

Your fee deficiency submission under 37 CFR 1.28(c) is hereby **ACCEPTED**.

Accordingly, status as a small entity has been removed and any future fee(s) submitted must be paid at the undiscounted rate.

Inquiries related to this communication should be directed to the undersigned at (571) 272-1058.

/Angela Walker/
Angela Walker
Paralegal Specialist
Office of Petitions

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: G.R. Mohan RAO
Serial No.: 16/947,294
Confirmation No.: 6907
Filed: July 27, 2020
Group: 2892
Examiner: Ajay ARORA
For: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Mail Stop Amendments/DD
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

In accordance with the requirements of 37 C.F.R. §§ 1.56, 1.97, and 1.98, attached please find a Form PTO SB/08 listing information for consideration by the Office in connection with its examination of the above-captioned patent application. A copy of each listed document is enclosed herewith.

Information related to IPRs 2020-00288, 00289, 00290, 00291 has been submitted in the attached Form SB/08a. Additionally, the related patent family to these IPRS was the subject matter of District Court Action styled *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 1 (Apr. 30, 2019). All relevant information related to this District Court case is included in the IPR submitted document.

Applicant request that this information disclosure statement be considered and that a copy of the Form PTO SB/08 be returned to the undersigned indicating the consideration of each document listed.

Respectfully submitted,
MUNCK WILSON MANDALA, LLP
Attorneys for Applicant(s)

/Gregory M. Howison, Reg. #30,646/
Gregory M. Howison
Registration No. 30,646\

Filed pursuant to Rule 37 C.F.R. 1.34

GMH/jsr

P.O. Drawer 800889
Dallas, Texas 75380
Tel: 972-628-3600
Fax: 972-628-3616
June 30, 2021

Electronic Acknowledgement Receipt	
EFS ID:	43141257
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison/Joselyn Rodriguez
Filer Authorized By:	Gregory Michael Howison
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	30-JUN-2021
Filing Date:	27-JUL-2020
Time Stamp:	18:58:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL_IPR202000288SurReply.pdf	188110 016c23a9a82847065976072391f03ad987a03037	no	13

Warnings:

Information:					
2	Non Patent Literature	NPL_IPR202000292POPR.pdf	2474863	no	75
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Warnings:					
Information:					
3	Non Patent Literature	NPL292Exhibit2002Exhibit4toIn validityContentions.pdf	8383853	no	27
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Warnings:					
Information:					
4	Foreign Reference	WO2004049453A1.pdf	1000408	no	14
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Warnings:					
Information:					
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Warnings:					
Information:					
6	Non Patent Literature	NPL_00291Exhibit1020Sze.pdf	12801935	no	206
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Warnings:					
Information:					
7	Non Patent Literature	NPL_Ex_2013GlewDec.pdf	3369738	no	79
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Warnings:					
Information:					
8	Non Patent Literature	NPL_Ex_201300291_GlewDecla ration.pdf	1826545	no	47
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Warnings:					
Information:					

9	Non Patent Literature	NPL_Ex2012_WolfVol4.pdf	3779059	no	52
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Warnings:					
Information:					
10	Non Patent Literature	NPL_Ex2013_195GlewDec.pdf	2797823	no	69
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Warnings:					
Information:					
11	Non Patent Literature	NPL_IonImplantation.pdf	342865	no	4
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Warnings:					
Information:					
12	Non Patent Literature	NPL_Exhibit1011KhannaPart2.pdf	9657165	no	165
			492d544396816ed498881ebdcdcb77a3fc4f88ba6		
Warnings:					
Information:					
13	Transmittal Letter	GRTD60-35294IDSTransmittal.pdf	96496	no	2
			15ef1d14309a48eb913b3b06f0f00c74849e9a6a		
Warnings:					
Information:					
Total Files Size (in bytes):			49011239		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
10 June 2004 (10.06.2004)

PCT

(10) International Publication Number
WO 2004/049453 A1

(51) International Patent Classification⁷: **H01L 29/788**,
29/792, 21/8234, 21/336

(74) Agent: COLLOPY, Daniel, R.; Advanced Micro Devices,
Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-
3453 (US).

(21) International Application Number:
PCT/US2003/021682

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE,
SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC,
VN, YU, ZA, ZM, ZW.

(22) International Filing Date: 10 July 2003 (10.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/305,701 26 November 2002 (26.11.2002) US

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant: **ADVANCED MICRO DEVICES, INC.**
[US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA
94088-3453 (US).

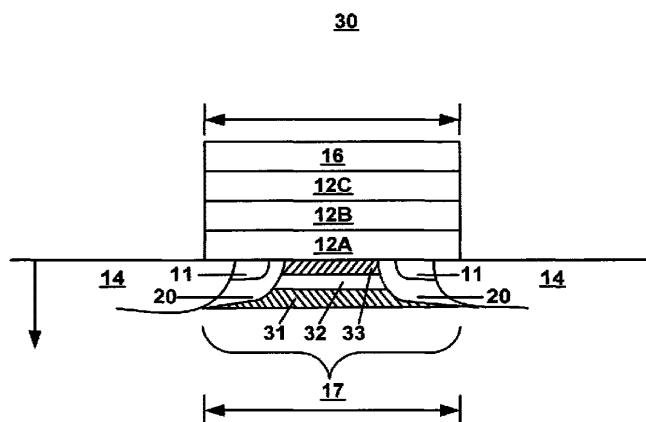
Published:

— with international search report

(72) Inventors: **ZHENG, Wei**; 2726 Estella Drive, Santa Clara,
CA 95051 (US). **LIU, Zhizheng**; 1319 Kingfisher Way
#1, Sunnyvale, CA 94087 (US). **RANDOLPH, Mark, W.**;
3673 Kendra Way, San Jose, CA 95130 (US). **HE, Yi**; 3919
Riverbend Terrace, Fremont, CA 94555 (US).

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT



(57) Abstract: A memory semiconductor cell (30) comprises a gate region (16), a source region (14) and a drain region (14). A channel region (17) is formed between the source region (14) and the drain region (14). The channel region (17) comprises a first channel portion (33) with a first concentration of doping material, the first channel portion (33) disposed adjacent to an edge of the channel region (17) closest to and substantially parallel to the gate region (16). The channel region (17) further comprises a second channel portion (31) with a second concentration of doping material, the second channel portion (31) disposed substantially parallel to the first channel portion (33) and a third channel portion (32), disposed between the first channel portion (33) and the second channel portion (31), with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration. The memory cell may be one of two general types of non-volatile memory, a floating gate cell or a nitride read only memory (NROM), whereby layer (12B) in a floating gate or a nitride layer respectively.

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RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT**TECHNICAL FIELD**

Embodiments of the present invention relate to design of sub-micron metal oxide semiconductors. More particularly, embodiments of the present invention provide retrograde channel doping to improve the short channel effect.

BACKGROUND ART

Figure 1 shows a memory cell 10 as has been well known in the conventional art. Regions 14 are the drain and/or source regions for memory cell 10. They may be used as source and/or drain interchangeably. Control gate 16 is used to control the operation of memory cell 10. A channel region 17 is formed between source/drain regions 14. Feature size 18 is the nominal size of the smallest feature that can be created by a particular semiconductor process. In memory cells of this type, the gate 16 width and channel 17 length typically correspond approximately to feature size 18. Memory cell 10 may also have a source/drain extension 11 structure. Source/drain extension 11 is a shallow diffusion that connects the channel 17 with the deeper source/drain 14, typically intended to prevent degradation of drive current.

Memory cell 10 may be one of two general types of non-volatile memory, a "floating gate" cell or a nitride read only memory (NROM) cell. In a floating gate cell, layer 12B of the gate stack is typically conductive polysilicon. Layers 12A and 12C are insulating materials which isolate or "float" gate layer 12B, which is usually referred to as a floating gate. Floating gate 12B is the storage element of memory cell 10.

Silicon nitride based flash memory has many advantages as compared to its floating gate and tunneling oxide based counterparts. Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) is potentially very dense in terms of number of cells per unit area that can be used and it requires fewer process steps as compared to floating gate memory. Moreover, it can be easily integrated with standard SRAM process technology. A further advantage of using SONOS devices is their suitability for applications requiring large temperature variations and radiation hardening. The SONOS stack is a gate dielectric stack and consists of a single layer of polysilicon, a triple stack ONO (Oxide-Nitride-Oxide) gate dielectric layer and a MOS channel 17. The ONO structure may consist of a tunnel oxide 12A, a nitride memory storage layer 12B and a blocking oxide layer 12C.

Memory device manufacturers are continually challenged to provide ever greater amounts of memory at ever lower costs. Recently, Advanced Micro Devices, Incorporated of California has introduced MIRROR BIT™ nitride-based flash ROM that stores multiple bits per memory cell 10 physically separated in nitride layer 12B. Such storage of multiple bits per cell increases the storage density of the memory device, thereby reducing the cost per bit of storage.

Another primary approach employed to achieve lower memory costs is the industry-wide on-going reduction in semiconductor feature size. By making features, such as signal lines and transistors smaller, more memory devices may be placed in a given die area, resulting in lower production costs.

However, as feature size decreases to, for example, about 0.3 microns and smaller, the channel length also decreases. As channel length grows shorter, threshold voltage begins to decrease and leakage current increases. These effects are commonly referred to in the semiconductor arts as the "short channel effect." An increase in leakage current is particularly onerous in flash memory devices as flash has found wide acceptance in very low power applications, for example mobile phones, due to the ability of flash to retain information without applied power. Increases in leakage current may have a significant deleterious effect on total power consumption

of the flash device and the product using the flash device. Consequently, much research and development effort has gone into mitigating the short channel effect.

Prior art approaches to improve leakage current and reduce the short channel effect include, for example, "halo" doping and retrograde wells. Halo doping 20 creates a steep dopant profile at the edges of the source/drain regions, as shown in Figure 1. A conventional retrograde well has a non-uniform doping concentration that increases, for example, linearly with depth 22 in the channel region 17. The doping of a conventional retrograde well generally follows a continuous, monotonically increasing profile with no abrupt changes. Conventional retrograde wells are typically created by using a slow diffusing dopant species such as arsenic or antimony for PMOS devices and indium for NMOS devices. Both halo doping and retrograde well profiles serve to inhibit the flow of charge carriers, raising the threshold voltage and reducing leakage current for the device.

However, both halo doping and conventional retrograde wells, alone and in combination, are found to be lacking. Such prior art approaches simply do not reduce leakage current to commercially acceptable levels for flash memory at modern process feature sizes, for example, 0.17 microns and smaller.

Semiconductor processing equipment is extremely expensive. Fundamental semiconductor processing steps, e.g., doping, typically require long periods of development and extensive qualification testing. Any solution to the short channel effect should be compatible with existing semiconductor processes and equipment without the need for revamping well established tools and techniques.

Thus a need exists to prevent short channel effects in memory cells. A further need exists for preventing short channel effects in a manner that is compatible and complimentary with conventional approaches to minimize short channel effects. A still further need exists for the above mentioned needs to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

DISCLOSURE OF THE INVENTION

Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

A memory semiconductor cell comprises a gate region, a source region and a drain region. A channel region is formed between the source region and the drain region. The channel region comprises a first channel portion with a first concentration of doping material, the first channel portion disposed adjacent to an edge of the channel region closest to and substantially parallel to the gate region. The channel region further comprises a second channel portion with a second concentration of doping material, the second portion disposed substantially parallel to the first channel portion and a third channel portion, disposed between the first channel portion and the second channel portion, with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a memory cell as has been well known in the conventional art.

Figure 2 illustrates a memory cell with a retrograde channel, according to an embodiment of the present invention.

Figure 3 illustrates an exemplary profile of doping concentration in a channel region versus channel depth, according to an embodiment of the present invention.

Figures 4A, 4B and 4C illustrate a charge carrier flow through a channel region of a memory cell, according to an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following detailed description of the present invention, retrograde channel doping to improve short channel effect, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT

Embodiments of the present invention are described in the context of design and operation of flash memory devices. However, it is appreciated that embodiments of the present invention may be utilized in other areas of electronic design and operation.

Figure 2 illustrates a memory cell 30 with a novel retrograde channel, according to an embodiment of the present invention. The channel region comprises three portions, 31, 32 and 33. Channel portion 33 is closest to gate 16 and substantially parallel to the long axis of gate 16. Channel portion 32 is substantially parallel to channel portion 33 and at a greater depth into the substrate material than channel portion 32. Channel portion 31 is substantially parallel to channel portion 32 and at a still greater depth into the substrate material. Channel portion 32 is disposed between channel portions 31 and 33. It is appreciated that memory cell 30 is shown with source/drain extensions 11 and halo implant regions 20. Embodiments of the present invention are well suited to memory cells with or without these features. If one or both were absent, channel portions 31, 32 and 33 would extend horizontally to the halo implant or the source drain extension or the source/drain.

By well known semiconductor processing techniques, for example implantation and diffusion, channel portion 33 may be constructed and given a particular concentration of doping material. Likewise, channel portion 31 may be constructed and given a particular concentration of doping material. In general, no specific operations are performed to construct channel portion 32, rather channel portion 32 is a result of constructing portions 31 and 33 with no overlap. The bottom of channel portion 31 may be, for example, 0.1 μm from the top edge of the substrate.

According to an embodiment of the present invention, the doping concentration in both channel portion 31 and channel portion 33 is higher than the doping concentration of channel portion 32. Graph 40 of Figure 3 illustrates an exemplary profile 41 of doping concentration in a channel region versus channel depth. Channel portion 33 may have a doping concentration as depicted by profile 41 in region 33A. Channel portion 32 may have a doping concentration as depicted by profile 41 in region 32A. Channel portion 31 may have a doping concentration as depicted by profile 41 in region 31A.

It is to be appreciated that, in contrast to conventional retrograde wells, the doping profile of this novel well is neither monotonic nor necessarily continuous, according to an embodiment of the present invention. There may be relatively abrupt (as allowed by semiconductor physics) changes in doping profile at the boundaries between channel portions, for example between channel portions 31 and 32, and between channel portions 32 and 33.

In channel portions 31 and 33 charge carrier migration is hindered due to the to relatively high concentration of doping material(s). Consequently, the effective channel region is reduced to approximately

channel portion 32. For example, channel portion 32 may form a "tunnel" (not to be confused with quantum effect tunneling) between channel portions 31 and 33. As a beneficial result of the reduced effective channel, threshold voltage is increased and leakage current is decreased, reducing or eliminating the short channel effect. It is to be appreciated that the depths, thickness and doping concentrations of the respective channel portions will vary according to a wide range of variables including, for example, source/drain thickness, channel length, operating voltage, doping materials and whether the device operates as a P channel or an N channel.

Channel portion 31 may be initially formed by using a slow diffusing dopant species, for example, arsenic or antimony for PMOS devices. Such a diffusion process may enable high concentrations of doping material to reach the channel depths required. Channel portion 33 may be formed by using faster diffusing dopants, e.g., boron. A shorter diffusion may produce a high concentration of doping material at relatively shallow depths in the channel region.

Figures 4A, 4B and 4C further illustrate a charge carrier flow through a channel region of memory cell 30, according to an embodiment of the present invention. In Figure 4A, charge carriers, for example, electrons 403 attempt to flow from source/drain region 401 to source/drain region 402. Electrons are impeded from flowing into channel portion 33 due to a high concentration of doping material. Likewise, electrons 405 are impeded from flowing into channel portion 31 due to a high concentration of doping material. In contrast, electrons 404 are able to overcome a relatively small energy barrier and flow into channel portion 32.

As shown in Figure 4B, electrons 403, otherwise disposed to travel horizontally (as depicted) into channel region 33, must change direction to travel around the "corner" of channel region 33 in order to enter channel region 32, wherein electrons are more able to flow. Such changes of direction require energy, resulting in a higher energy budget for electrons traversing a complex path, in contrast to electrons which may be able to travel in substantially a straight line. In addition, because region 401 is fully populated with charge carriers, e.g., electrons 404 and 405, additional energy is required to overcome the electrostatic repulsion of like charges in order to move the charge carriers closer together. As a beneficial result of the increased path length, the indirect nature of the path, as well as electrostatic repulsion, electrons 403 require more energy to travel from region 401 to 402 and consequently have a beneficially higher threshold voltage for embodiments of the present invention when compared to the prior art.

In a similar manner, electrons 405 must change direction and overcome electrostatic repulsion in order to travel into channel portion 32 from their original positions adjacent to channel portion 31. Consequently, electrons 405 have a higher threshold voltage than would otherwise be required.

Electrons 404, while disposed adjacent to channel portion 32, are also beneficially affected by embodiments of the present invention. Although electrons 404 are not obviously redirected to avoid channel portions of higher doping concentration, electrons 404 are affected by the localized increased concentration of charge carriers resulting in electrostatic forces acting upon electrons 404 in a similar manner to the electrostatic forces acting upon electrons 403 and 405.

Figure 4C shows a cumulative effect of the present retrograde channel on charge carrier flow, according to an embodiment of the present invention. Electrons in region 401 are inhibited from flowing in channel portions 33 and 31, favoring channel portion 32. However, due to the physically constrictive nature of channel portion 32 combined with electrostatic forces acting upon the like charge carriers, the electrons tend to "bunch up" at the interface between region 401 and channel portion 32. The net effect of "bunching up" is seen externally as a desirable increase in threshold voltage, and a corresponding decrease in leakage current.

It is to be appreciated that although a PMOS device has been illustrated herein, embodiments of the present invention are well suited to NMOS devices as well. The choices of materials, e.g., for dopants, for use with NMOS devices are well understood in the semiconductor arts.

5 This novel design and method to implement this design reduce and/or eliminate the short channel effect, allowing for decreased feature size and increased density of memory cells. These beneficial results allow for less expensive memory devices with lower power consumption, rendering a competitive advantage to the users practicing embodiments of the present invention.

10 Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

15 The preferred embodiment of the present invention retrograde channel doping to improve short channel effect is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.