

CLAIMS

What is claimed is:

1. A method of manufacturing a memory semiconductor cell (30) comprising:
forming a first channel portion (33) to produce a first concentration of doping material, said first
5 channel portion (33) disposed adjacent to an edge of a channel region closest to and substantially parallel
to a gate region (16) of said memory semiconductor cell;
forming a second channel portion (31) to produce a second concentration of doping material,
said second portion (31) disposed substantially parallel to said first channel portion (33); and
10 forming a third channel portion (32), disposed between said first channel portion (33) and said
second channel portion (31), comprising a third concentration of doping material, wherein said third
concentration is lower than said first concentration and lower than said second concentration.
2. The method as described in Claim 1 further comprising implanting a halo implant (20) disposed
adjacent to a source region or a drain region of said memory semiconductor cell (30).
3. The memory semiconductor cell (30) described in Claim 1 wherein a source region of said
15 memory semiconductor cell comprises a source extension region (11).
4. The method as described in Claim 1 further comprising forming said second channel portion
(31) prior to the formation of said first channel portion (33).
5. The method as described in Claim 1 wherein said memory semiconductor cell (30) is non-
volatile.
- 20 6. The method as described in Claim 5 wherein said memory semiconductor cell (30) comprises a
nitride layer as a storage element (12B).
7. The method as described in Claim 5 wherein said memory semiconductor cell comprises a
floating gate (12B) as a storage element.
8. A memory semiconductor cell (30) comprising:
25 a gate region (16), a source region (14) and a drain region (14);
a channel region (17) between said source region (14) and said drain region (14);
wherein said channel region (17) comprises:
a first channel portion (33) comprising a first concentration of doping material, said first
30 channel portion (33) disposed adjacent to an edge of said channel region (17) closest to and substantially
parallel to said gate region (16);
a second channel portion (31) comprising a second concentration of doping material, said
second portion (31) disposed substantially parallel to said first channel portion (33); and
a third channel portion (32), disposed between said first channel portion (33) and said second
35 channel portion (31), comprising a third concentration of doping material, wherein said third
concentration is lower than said first concentration and lower than said second concentration.
9. The memory semiconductor cell described in Claim 8 wherein said channel region (17) further
comprises a halo implant (20) disposed adjacent to said source region (14) or said drain region (14).
10. The memory semiconductor cell described in Claim 8 wherein said source region (17)
40 comprises a source extension region (11).

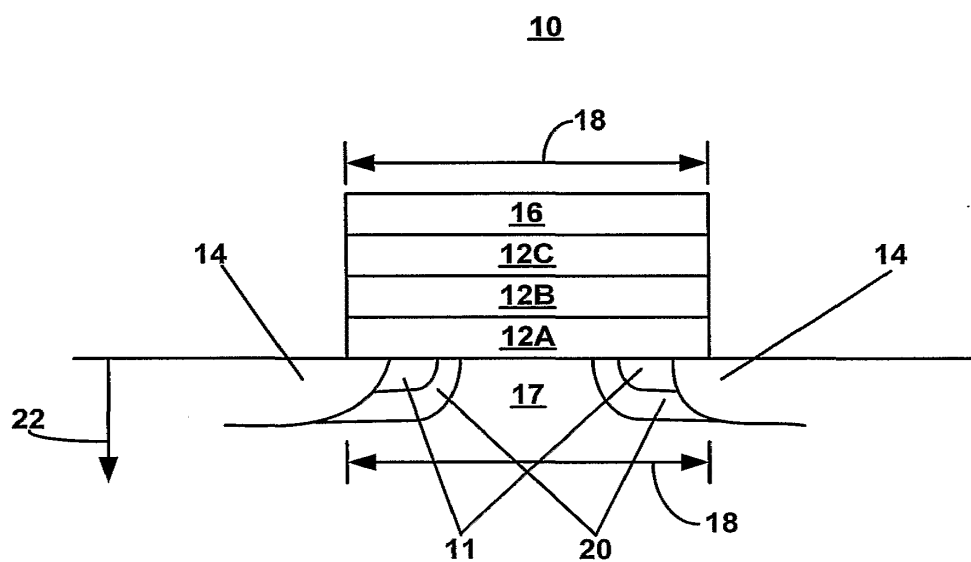
1/4

FIG. 1
(CONVENTIONAL ART)

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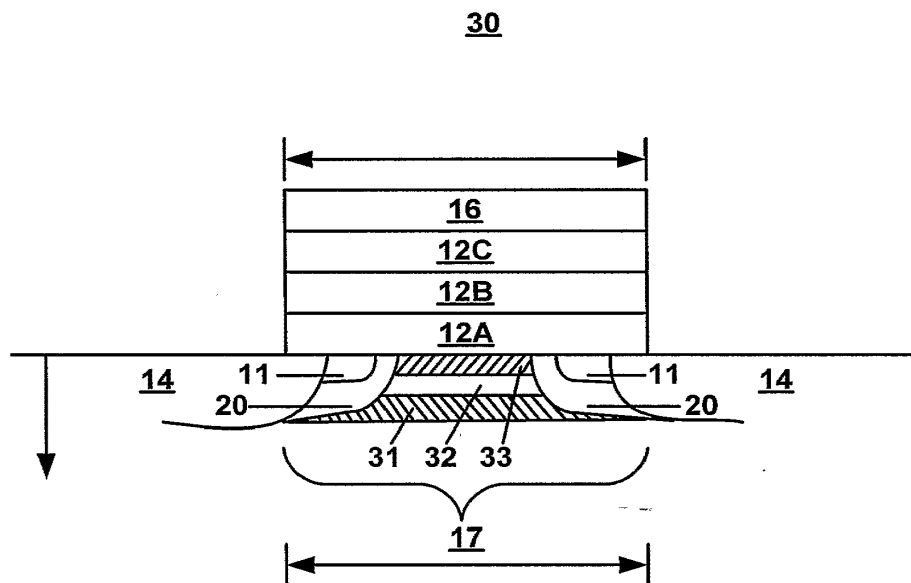


FIG. 2

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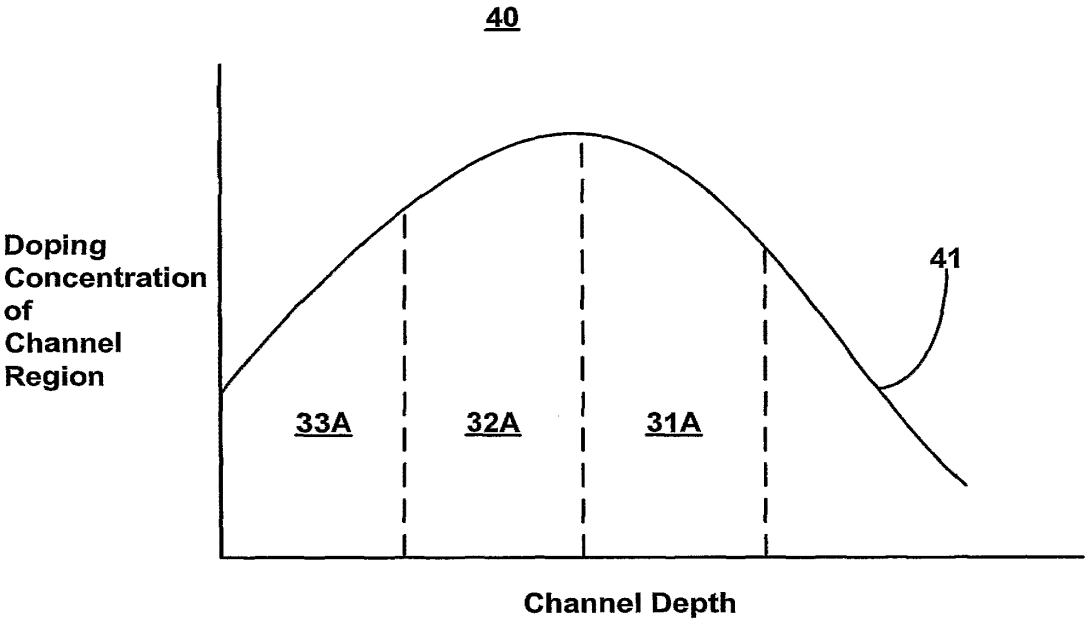
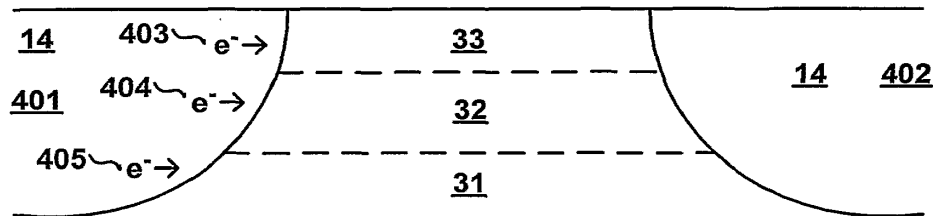
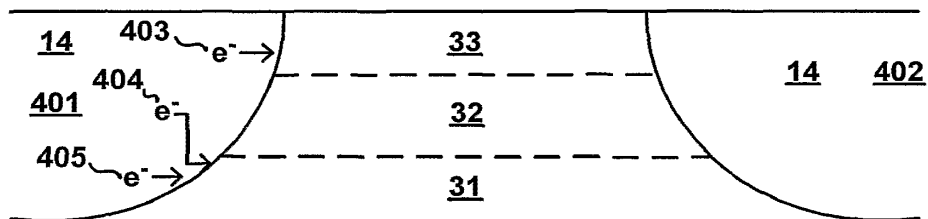
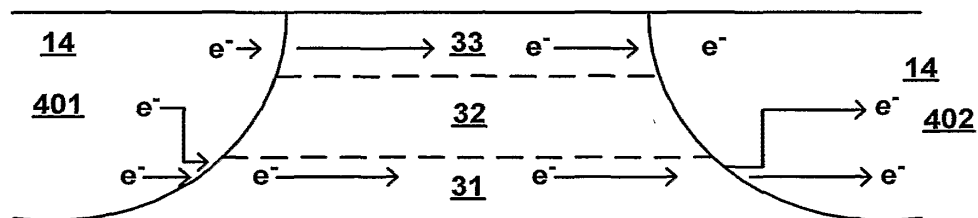


FIG. 3

4/4**FIG. 4A****FIG. 4B****FIG. 4C**

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 03/21682

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L29/788 H01L29/792 H01L21/8234 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/106852 A1 (CHANG CHI ET AL) 8 August 2002 (2002-08-08) paragraphs '0047!-'0055!; figures 5-8	1-10
Y	US 5 923 985 A (AOKI KENJI ET AL) 13 July 1999 (1999-07-13) column 3, line 60 -column 4, line 28; figures 8A-8D,9	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 03, 30 March 2000 (2000-03-30) -& JP 11 354778 A (MITSUBISHI ELECTRIC CORP), 24 December 1999 (1999-12-24) abstract; figures	1-10



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Patent family members are listed in annex.

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Date of the actual completion of the international search

11 February 2004

Date of mailing of the international search report

18/02/2004

Name and mailing address of the ISA

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INTERNATIONAL SEARCH REPORT

International Application No

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 929 486 A (KITAKADO HIDEHITO) 27 July 1999 (1999-07-27) column 5, line 55 -column 9, line 22; figures 3, 5A, 5B ----	1-10
Y	US 6 258 645 B1 (KANG WOO TAG) 10 July 2001 (2001-07-10) the whole document ----	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 161 (E-257), 26 July 1984 (1984-07-26) -& JP 59 061070 A (FUJITSU KK), 7 April 1984 (1984-04-07) abstract; figures -----	1-10

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 03/21682

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4160985	A	1979-07-10	Kamins et al.	
	2	4684971	A	1987-08-04	Payne	
	3	4688063	A	1987-08-18	Lu et al.	
	4	4907058	A	1990-03-06	Sakai	
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	6	5835402	A	1998-11-10	Rao et al.	
	7	6025237	A	2000-02-15	Choi	
	8	6384431	B1	2002-05-07	Takahashi et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

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Examiner Name	ARORA, AJAY
Attorney Docket Number	GRTD60-35294

9	6465862	B1	2002-10-15	Harris
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	3	20030183856	A1	2003-10-02	Wieczorek et al.	
	4	20080142899	A1	2008-06-19	Morris et al.	
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	1	2003051551	JP	A	2003-02-21	Miyamoto et al.		×

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	Attorney Docket Number	GRTD60-35294		

	2	2003218356	JP	A	2003-07-31	Matsumoto et al.	☒
	3	6482563	JP	A	1989-03-28	Kondo	☒
	4	2004049453	WO	A1	2004-06-10	Zheng et al.	☐

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	1	IPR2020-00288-Exhibit 1029-Claim Construction District Court 4 20-2020	
	2	IPR2020-00288-Exhibit 2007-Minutes for Markman Hearing Held Via Video Conference Before U.S. District Judge Rodney Gilstrap, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 61	
	3	IPR2020-00288-Petitioner Reply	
	4	IPR2020-00289-00289 Petitioner Reply	
	5	IPR2020-00292 - Petition for IPR	
	6	IPR2020-00292-Exhibit 2002-Excerpt from Exhibit 4 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on U.S. Patent No. 6,384,431 to Takahashi	

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7	IPR2020-00288 - Ex. 1020 - Michael Nastasi and James W. Mayer, Ion Implantation and Synthesis of Materials (2006). 4 pages
8	IPR2020-00288-Exhibit 2001 - IPR2020-00288 - Excerpt from Exhibit 1 to Appendix A of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Morris
9	IPR2020-00288-Exhibit 2002-xcerpt from Exhibit 2 to Appendix A of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Miyamoto
10	IPR2020-00288-Exhibit 2009-Complaint for Patent Infringement, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 1
11	IPR2020-00288-Exhibit 2011- Exhibit A to Revised Joint Claim Construction Chart Pursuant to Patent Rule 4-5, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 60-1
12	IPR2020-00288-Exhibit 2012-Samsungs Responsive Claim Construction Brief - District Court
13	IPR2020-00288-Exhibit 2013- Glew Dec
14	IPR2020-00288-Exhibit 2014- Excerpt from Exhibit 10 to Appendix A of Samsung Electronics Co., Ltd.'s Invalidity Contentions
15	IPR2020-00288-Patent Owner Preliminary Response
16	IPR2020-00288-Patent Owner Sur Reply
17	IPR2020-00288-Petition

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18	PR2020-00289-Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Payne
19	PR2020-00289-Exhibit 1003-Smith Dec
20	PR2020-00289-Exhibit 1010- S. M. Sze et al., Semiconductor Devices: Physics and Technology, John Wiley & Sons, 2nd Ed., 2002 ("Sze '02")
21	PR2020-00289-Exhibit 1012-Ben G. Streetman, Solid State Electronic Devices, 2nd Ed., Prentice-Hall, 1980 ("Streetman")
22	PR2020-00289-Exhibit 2001-Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Payne
23	PR2020-00289-Exhibit 2002- Exhibit 3 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Wieczorek
24	PR2020-00289-Exhibit 2011-Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2001 ("Razavi")
25	PR2020-00289-Exhibit 2012-Excerpts from Wolf, S., Silicon Processing for the VLSI Era, Vol.4 - Deep-Submicron Process Technology (2002) ("Wolf Vol. 4")
26	PR2020-00289-Exhibit 2013-Glew Dec
27	PR2020-00289-Patent Owner Pre Resp
28	PR2020-00289-Patent Owner Sur reply

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	Art Unit	2892
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	Attorney Docket Number	GRTD60-35294

29	PR2020-00289-Petition
30	PR2020-00290-Exhibit 1003-Declaration of Dr. Bruce Smith
31	PR2020-00290-Exhibit 1013-Tango, Mega bit Memory Technology
32	PR2020-00290-Patent Owner Preliminary Resp
33	PR2020-00290-Patent Owner Sur Reply
34	PR2020-00290-Petition
35	PR2020-00290-Petitioners Reply to Patent Owner Preliminary Response
36	PR2020-00291-Exhibit 1003-Declaration of Dr. Bruce Smith
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	Examiner Name	ARORA, AJAY	
	Attorney Docket Number	GRTD60-35294	

40	PR2020-00291-Exhibit 2001-Exhibit 2 to Appendix B of Samsung Electronics Co., LTD's Invalidity Contentions (Invalidity Contention based on U.S. Patent Application Publication No. 2002/0195656 ("Hattori"))	
41	PR2020-00291-Exhibit 2013- Declaration of Dr. Alexander D. Glew	
42	PR2020-00291-Patent Owner Preliminary Resp	
43	PR2020-00291-Patent Owner Sur Reply	
44	PR2020-00291-Petition	
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46	PR2020-00292-Exhibit 1003-Declaration of Dr. Bruce Smith	
47	PR2020-00292-Exhibit 2001-Excerpt from Exhibit 1 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on "Insulated Gate Bipolar Transistor IGBT Theory and Design" by Vinod Kumar Khanna	
48	PR2020-00292-Exhibit 2012-Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 53-1 (Mar. 18, 2020)	
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	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gregory M. Howison, Reg. #30646/	Date (YYYY-MM-DD)	2021-06-24
Name/Print	Gregory M. Howison	Registration Number	30646

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I, Michael Fletcher, declare:

1. I am well versed in both the Japanese and English languages and have over 15 years of experience translating Japanese technical documents into English.
2. The following translation of the patent document JPS64-482563 to English is accurate and complete to the best of my knowledge.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Executed this 18th day of September 2019, at Parowan, UT

A handwritten signature in cursive script that reads "Michael Fletcher". The ink is dark and the signature is fluid.

Michael Fletcher

1

(19) JAPANESE PATENT
OFFICE (JP)

(12) Laid Open Patent Application
Bulletin (A)

(11) Unexamined Patent
Application (*Kokai*) Patent S64-
82563

(43) Laid-Open Publication Date: March 28, 1989

(51) Int. Cl.⁴
H 01 L 29/78
29/68

Classification No.
321

JPO File No.
J-8422-5F
8526-5F

Request for Examination: No

Number of inventions: 1 (Total number of pages: 7)

(54) Title of The Invention Semiconductor Device

(21) Application No. S62-241827

(22) Filing Date September 24, 1987

(72) Inventors KONDO, Hisao c/o LSA Research Center Mitsubishi Electric 1, 4-chome, Itano-
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Specification

(57) [Abstract] This publication is application data prior to electronic applications and so there is no abstract data recorded.

1. Title of The Invention

Semiconductor Device

2. What is Claimed Is

(1) A semiconductor device comprising a first conduction type first area; a second conduction type second area formed on the primary surface of one side of the first area; a first conductive type third area formed at least partially on the upper layer of the second area; a second conductive type fourth area formed partially on the upper layer of the third area; an insulator formed so as to cover at least from the primary surface of the second area to the primary surface of the third area reaching the primary surface of the fourth area; a first electrode formed on the primary surface of the other side of the first area; a second electrode formed on the primary surface of the insulator; and a third electrode formed at least in contact with the primary surface of the fourth area, wherein the impurity distribution of the second area comprises a gradient in the vertical direction relative to the primary surface.

(2) The semiconductor device according to claim 1, wherein the second area is prepared as a two layer structure of a medium concentration impurity area in contact with the first area and a low concentration impurity area in contact with the third area and there is an impurity distribution established in the medium concentration impurity area such that the impurity concentration decreases moving from the low concentration impurity area towards the first area.

(3) The semiconductor device according to claim 1, wherein an impurity distribution of the impurity concentration is established in the medium concentration impurity area with an increase moving from the low concentration impurity area toward the first area.

(4) The semiconductor device according to claim 1, wherein an impurity distribution of the impurity concentration is established in the low concentration impurity area with an increase moving from the third area toward the medium concentration impurity area.

(5) The semiconductor device according to claim 1, wherein an impurity distribution of the impurity concentration is established in the low concentration impurity area with an increase moving from the medium concentration impurity area towards the third area.

DETAILED DESCRIPTION OF THE INVENTION

FIELD OF INDUSTRIAL USE

The present invention is related to a semiconductor device and in particular to the improving of turn-off time for an insulated gate bipolar transistor (hereafter "IGBT").

BACKGROUND TECHNOLOGY

FIG. 5 (a) is a cross-section view of a conventional IGBT and FIG. 5 (b) is a schematic drawing showing the impurity distribution of each of the areas along the E-E line. In FIG. 5, 1 is a first P-type area with a P type impurity uniformly distributed at high concentration. A first N-type area 2 is formed on the primary surface of one side of this first P-type area 1 with N type impurities uniformly distributed at a medium concentration. In addition, a second N-type area 3 is formed on this first N-type area 2 with N type impurities uniformly distributed at low concentration. Furthermore, a plurality of mutually isolated second P-type areas 4 are formed on the upper layer of this second N-type area 3 with P type impurities uniformly distributed at a medium concentration. Also, a third N-type area 5 is formed over a part of the upper layers of the respective second P-type areas 4 with N type impurities uniformly distributed at high concentration. Furthermore, a gate electrode 7 is formed with an insulating film 6 interposed on the main surface of the second N-type area 3 and on a part of the main surface of the second P-type area 4. In addition, an emitter electrode 8 is formed on the remaining part of the main surface of the second P-type area 4 and the main surface of the third N-type area 5. On the other hand, a collector electrode 9 is formed overlain on the other primary surface of the first P-type area 1.

Next, the operating mechanism of the IGBT above will be described. First, under normal operating conditions, relative to the emitter electrode 8, positive high DC voltage is applied to the collector electrode 9 and further, positive stepped constant voltage is applied to the gate electrode 7. With stepped positive voltage applied between the gate and emitter in this manner, an N channel is formed at the boundary layer of the second P-type area 4 and insulating film 6, and electrons are injected through this N channel from the third N-type area 5 to the second N-type area 3 and first N-type area 2. Therefore, the potential of the second N-type area 3 and first N-type area 2 is reduced and the P-N junction at the boundary layer of the first P-type area 1 and first N-type area 2 is biased in the forward direction causing electron holes to be injected from the first P-type area 1 to the first N-type area 2. The injected electrons and electron holes neutralize electrically so large numbers of electrons and electron holes are supplemented and injected respectively from the third N-type area 5 and first P-type area 1 causing accumulation of a lot of electron holes and electrons on the first N-type area 2 and second N-type area 3. As a result, the specific resistance of the first N-type area 2 and second N-type area 3 is lowered setting the IGBT in conduction state with high current from the collector electrode 9 to the emitter electrode 8.

Next, when positive voltage is no longer applied to the gate electrode 7, the N channel at the boundary layer of the second P-type area 4 and insulating film 6 vanishes and electrons are no longer injected from the third N-type area 5 to the second N-type area 3 and first N-type area 2. The current based on this type of electron injection is equivalent to a PNP transistor with the first P-type area 1 as the emitter, the second N-type area 3 and first N-type area 2 as base, and the second P-type area 4 as the collector. Therefore, IGBT current in the case that electron injection is terminated is anticipated to be approximately the equivalent of PNP transistor current for the case that base current has been terminated for the PNP transistor. In other words, when electron injection is terminated, current flowing through the IGBT is reduced and FIG. 6 shows a schematic of this waveform.

In FIG. 6, the vertical axis is current flowing through the IGBT and horizontal axis is time. As shown in FIG. 6, at time $t = t_0$, when gate electrode positive voltage is terminated, current instantaneously drops from I_0 to I_1 and then gradually reduces to zero.

THE PROBLEM(S) THAT THIS INVENTION INTENDS TO RESOLVE

One of the elements that exhibits the current characteristics of this IGBT is the turn-off time t_{off} . This turn-off time is defined as

$$t_{off} = t_1 - t_0 \quad (1)$$

Here, t_0 is the time that positive voltage is terminated on the gate electrode and t_1 is the time that current reaches $0.1I_0$.

As can be seen in FIG. 6, the turn-off time t_{off} is dependent on the current attenuation characteristics of the attenuation region from time t_0 to time t_1 . Here, as described above, this IGBT approximates a PNP transistor so the current waveform in the attenuation region can be approximated using

$$I(t) = I_1 \exp\left(-\frac{t - t_0}{\beta \tau_b}\right) \quad \dots (2)$$

Here, β is the grounded emitter current gain and τ_b is the base travel time for a PNP transistor. In formula (2), if the value of $\beta\tau_b$ is reduced, attenuation in the attenuation region becomes remarkable enabling shortening the turn-off time t_{off} of the IGBT. Furthermore, approximation of $\beta\tau_b$,

$$\beta \tau_b = \frac{\gamma \alpha_T}{1 - \gamma \alpha_T} \tau_b \quad \dots (3)$$

However,

$$\alpha_T = \operatorname{sech}\left(\sqrt{\frac{2 \tau_b}{\tau_{eff}}}\right) \quad \dots (4)$$

Here, γ is the emitter injection efficiency of the PNP transistor. α_T is the base transport efficiency of the PNP transistor and τ_{eff} is the effective carrier lifespan inside the PNP transistor base area.

In the past, the effective carrier lifespan τ_{eff} inside the PNP transistor base area was reduced using electron beam irradiation to shorten the IGBT turn off time t_{off} . In other words, reducing the effective carrier lifetime τ_{eff} in the PNP transistor base area reduces the $\beta\tau_b$ value and as a result, current attenuation in the attenuation region becomes remarkable and the IGBT turn-off time t_{off} is shortened.

However, when the effective carrier lifespan τ_{eff} in the PNP transistor base area is reduce in this manner, there was the problem that the number of electron holes and electrons accumulated on the first N-type area 2 and second N-type area 3 was reduced while in conduction status and thus increased effective resistance.

An objective of the present invention is to resolve the problems as described above and obtain a semiconductor device with a short turn-off time while also having a small effective resistance while in conduction state.

MEANS FOR SOLVING THE VARIOUS PROBLEMS

The semiconductor device according to the present invention comprises a first conduction type first area; a second conduction type second area formed on the primary surface of one side of the first area; a first conductive type third area formed at least partially on the upper layer of the second area; a second conductive type fourth area formed partially on the upper layer of the third area; an insulator formed so as to cover at least from the primary surface of the second area to the primary surface of the third area reaching the primary surface of the fourth area; a first electrode formed on the primary surface of the other side of the first area; a second electrode formed on the primary surface of the insulator; and a third electrode formed at least in contact with the primary surface of the fourth area, wherein the impurity distribution of the second area is established so as to comprise a gradient in the vertical direction relative to the primary surface.

FUNCTION

Regarding the semiconductor device according to the present invention, the impurity distribution comprises a gradient in the vertical direction relative to the primary surface generating an internal electric field in the second area and the effective diffusion constant of carriers in the second area are controlled by this internal electric field, shortening the turn-off time.

EMBODIMENTS

FIG. 1 (a) is a cross-section view of the IGBT that is an embodiment of this invention, and FIG. 1 (b) is a schematic drawing showing the impurity distribution of each of the areas along the A-A line. In FIG. (1), the only point of difference from conventional is the N-type impurity distribution of a first N-type area 2. As shown in FIG. 1 (b), the N-type impurity concentration of the first N-type area 2 is the lowest at the boundary surface of a first P-type area 1. The value thereof increases when approaching a second N-type area 3, and reaches a medium concentration on the boundary surface of the second N-type area 3 in a similar manner to conventional. In this manner, an internal electric field is generated within the first N-type area 2 by providing a slope to the N-type impurity concentration of the first N-type area 2. The type of internal electric field that is generated based on the slope of the N-type impurity concentration is described as follows. The relationship between this internal electric field and the N type impurities is given by

$$E(x) = - \frac{k T}{q} \cdot \frac{1}{N(x)} \cdot \frac{d N(x)}{d x} \quad \dots (5)$$

Here, $E(x)$ is the internal electric field, k is the Boltzmann's constant, T is absolute temperature, q is the amount of electron charge, and $N(x)$ is the N-type impurity concentration distribution. As understood from formula (5), the internal electric field direction and the N-type impurity concentration distribution gradient are in opposite directions. Therefore, when indicating an N-Type impurity concentration distribution such as the one shown in FIG. 1, the internal electric field directionality is from the second N-type area 3 towards the first P-type area 1. This type of internal electric field will act to obstruct the diffusion of electron holes that are injected through the first P-type area 1 and attempting to diffuse to the second N-type area 3, reducing the effective electron hole diffusion constant.

FIG. 2 (a) is a cross-section view of the IGBT that is another embodiment of this invention, and FIG. 2 (b) is a schematic drawing showing the impurity distribution of each of the areas along the B-B line. Regarding points of difference from conventional in this drawing, as shown in FIG. 2 (b), the N-type impurity concentration of the first N-type area 2 at the boundary surface with the second N-type area 3 has a low concentration in a similar manner to the N-type impurity concentration of the second N-type area 3. With approaching the first P-type

area 1, the value thereof increases, reaching a medium concentration at the boundary surface similar to conventional.

By providing a slope opposite to what is shown in FIG. 1 for the N-type impurity concentration of the first N-type area 2 in this manner, an internal electric field opposite of the one shown in the first drawing is generated in the first N-type area 2. Therefore, as this internal electric field acts in a direction accelerating electron hole diffusion, the effective electron hole diffusion constant is increased.

FIG. 3 (a) is a cross-section view of the IGBT that is another embodiment of this invention, and (b) of the same FIG. is a schematic drawing showing the impurity distribution of each of the areas along the C-C line. Regarding points of difference from conventional in this drawing, as shown in FIG. 3 (b), the N-type impurity concentration of the second N-type area 3 has a low concentration at the boundary surface with the second p-type area 4 in a similar manner to that of conventional. With approaching the first N-type area 2, the value thereof increases, reaching a medium concentration of N type impurity concentration in the first N-type area 2 at the boundary surface with the first N-type area 2.

By providing a slope opposite to that shown in FIG. 1 for the N-type impurity concentration of the second N-type area 3 in this manner, an internal electric field opposite of the one shown in FIG. 1 is generated in the second N-type area 3. Therefore, as this internal electric field acts in a direction accelerating electron hole diffusion, the effective electron hole diffusion constant is increased.

FIG. 4 (a) is a cross-section view of the IGBT that is another embodiment of this invention, and FIG. 4 (b) is a schematic drawing showing the impurity distribution of each of the areas along the D-D line. For points of difference from convention in this drawing as shown in FIG. 4 (b), the N-type impurity concentration of the second N-type area 3 has a low concentration at the boundary surface with the first N-type area 2 in a similar manner to that of conventional. With approaching the second P-type area 4, the value thereof increases, reaching a high concentration at the boundary surface with the second P-type area 4.

By providing a slope the same as that shown in FIG. 1 for the N-type impurity concentration of the second N-type area 3 in this manner, an internal electric field the same as the one shown in FIG. 1 is generated in the second N-type area 3. Therefore, as this internal electric field acts in the direction of obstructing electron hole diffusion, the effective electron hole diffusion constant is decreased.

As stated above, a suitable internal electric field is generated in either the first N-type area 2 or the second N-type area 3 by applying a gradient to the impurity distribution of either the first N-type area 2 or the second N-type area 3 in the direction vertical relative to the main surface, and the effective diffusion constant of the electron holes of the first N-type area 2 or the second N-type area 3 can be controlled.

Next is a description of the theory behind shortening of the IGBT turn-off time by controlling the electron hole effective diffusion constant.

Here, for the base area, or in other words when assuming that the thickness of the first N-type area 2 and the second N-type area 3 do not change, the base travel time is reduced as the electron hole diffusion constant becomes larger, and conversely, the base travel time increases as the electron hole diffusion constant becomes smaller. In other words, the base travel time can be controlled by controlling the electron hole diffusion constant. Furthermore, the IGBT turn-off time can be controlled by controlling the base travel time. Next is a description of the reasons why this is the case.

First, differentiating the approximation formula $\beta\tau_b$ (3) by the base travel time T_b is

$$\frac{d y}{d \tau_b} > 0 \quad \text{Gives} \quad \frac{2 \tau_b}{\tau_{eff}} < \sqrt{2} \quad \dots (6)$$

$$\frac{d y}{d \tau_b} < 0 \quad \text{Gives} \quad \frac{2 \tau_b}{\tau_{eff}} > \sqrt{2} \quad \dots (7)$$

If equation (6) is valid, the turn-off time t_{off} is shortened as the base travel time τ_b becomes smaller. On the other hand, if equation (7) is valid, the turn-off time t_{off} is shortened as the base travel time τ_b becomes larger.

By generating an internal electric field in the first N-type area 2 or the second N-type area 3 as a result of applying a slope to the impurity concentration distribution of either the first N-type area 2 or the second N-type area 3, the electron hole diffusion constant in addition to the base travel time can be controlled, which enables shortening the IGBT turn-off time. In addition, the actions described above enable shortening the turn-off time without reduction of the effective carrier lifespan of the first N-type area 2 or second N-type area 3 that was required previously and enables suppressing the effective resistance of the first N-type area 2 or second N-type area 3.

Next is a description based on the FIG. 1 regarding a manufacturing method of a semiconductor device according to the present invention. First, the first N-type area 2 is formed on the first P-type area 1 using the vapor-phase epitaxial growth method. When conducting vapor-phase epitaxial growth, the first N-type area 2 with an N-type impurity concentration distribution as shown in FIG. 1 (b) can be obtained by gradually increasing the N-type impurity concentration in proportion to the growth film thickness. Next, the second N-type area 3 is formed on the first N-type area 2 using the vapor-phase epitaxial growth principle. Furthermore, by applying the manufacturing process of a normal double-diffusion-type MOS transistor, the second P-type area 4, third N-type area 5, insulating film 6, gate electrode 7, and emitter electrode 8 are formed, and the IGBT as shown in the FIG. can be produced.

In addition, if a gradient is applied to the N-type impurity concentration to a first N-type area 3 [sic] as shown in FIG. 2, the N-type impurity concentration can be reduced gradually based on the growth film thickness when forming the first N-type area 2 on the first P-type area 1 in accordance with the vapor-phase epitaxial growth principle.

In addition, if a gradient is applied to the N-type impurity concentration of the second N-type area 3 as shown in FIG. 3 and FIG. 4, the N-type impurity concentration can be changed gradually based on the growth film thickness when forming the second N-type area 3 on the first N-type area 2 in accordance with the vapor-phase epitaxial growth principle.

EFFECT OF THE INVENTION

The turn-off time is shortened for the semiconductor device of the present invention by controlling the carrier effective diffusion constant in addition to the base travel time using the internal electric field generated by the

impurity concentration distribution. This results in enabling obtaining a high-performance semiconductor device without increasing the effective resistance while in a conductive state.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a drawing showing an embodiment of the present invention. FIG. 2 through FIG. 4 are drawings showing other embodiments of the present invention. FIG. 5 is a drawing showing a conventional example. FIG. 6 is a drawing showing the relationship between the electric current and the time where voltage applied to the IGBT gate electrode is stopped.

In the drawings, 1 is the first P-type area, 2 is the first N-type area, 3 is the second N-type area, 4 is the second P-type area, 5 is the third N-type area, 6 is the insulating film, 7 is the gate electrode, 8 is the emitter electrode, and 9 is the collector electrode

Furthermore, the same symbols in the drawings indicate the same or corresponding parts.

FIG. 6

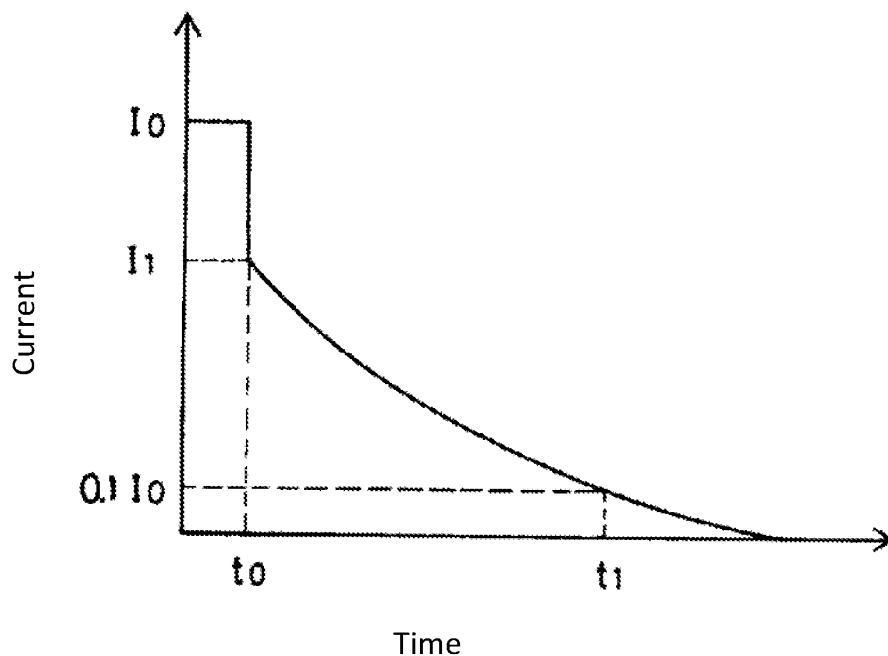
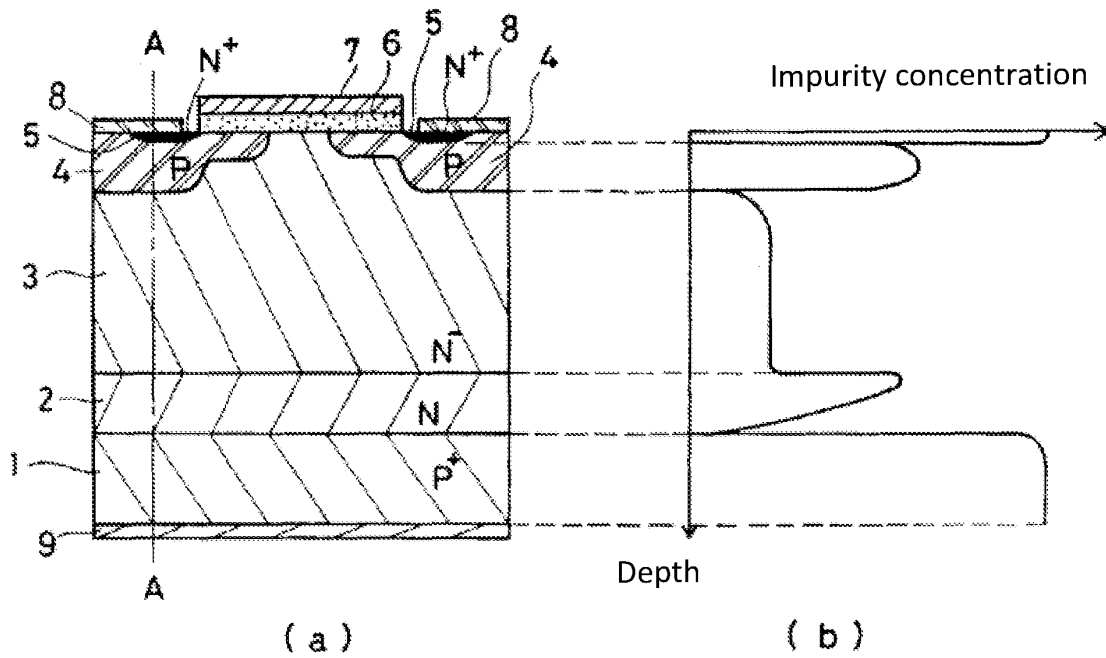


FIG. 1



1: First P type area
3: Second N type area
5: Third N type area
7: Gate electrode
9: Collector electrode

2: First N type area
4: Second P type area
6: Insulator film
8: Emitter electrode

FIG. 2

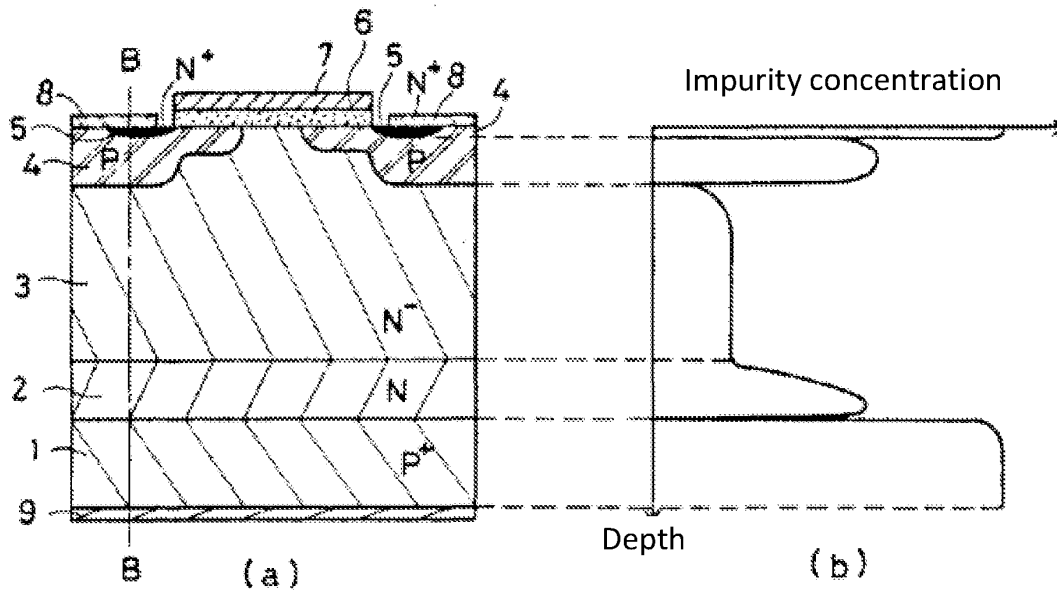


FIG. 3

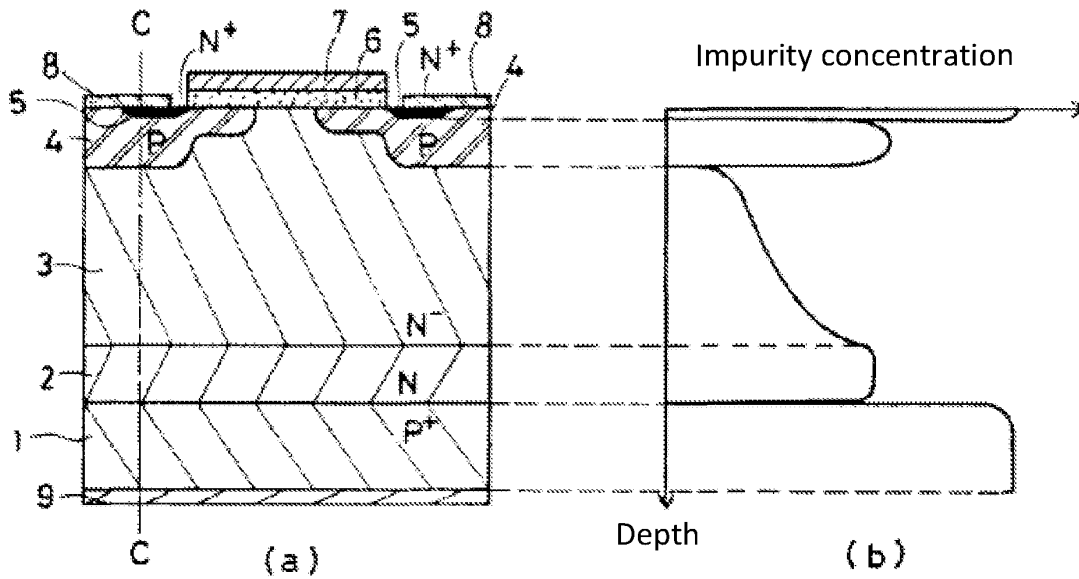


Figure 1 consists of two parts: (a) a schematic diagram of a semiconductor device structure and (b) a graph of Impurity concentration versus Depth.

Part (a) shows a cross-section of the device. The layers are numbered 1 through 9 from bottom to top. The structure includes a substrate (1) with a P^+ region, followed by an N region (2), an N^- region (3), and a P region (4). A central N^+ region (5) is shown, with N^+ regions (6) on either side. A P region (7) is located above the central N^+ region. A D region (8) is shown on the left and right sides. A P region (9) is at the bottom. The device is labeled with N^+ , P , N^- , N , and P^+ regions.

Part (b) is a graph of Impurity concentration versus Depth. The vertical axis is labeled "Depth" and the horizontal axis is labeled "Impurity concentration". The graph shows the impurity profile of the device, with the concentration of each layer corresponding to the regions in part (a). The profile shows a sharp increase in concentration at the surface, followed by a gradual decrease, and then a sharp increase again at the bottom.

Figure 1 consists of two parts. Part (a) is a cross-sectional schematic of a semiconductor device. It shows a substrate with layers labeled 1 through 9. Layer 1 is the bottom-most, followed by 2, 3, 4, 5, 6, 7, 8, and 9 at the top. The substrate has regions labeled N^+ , N^- , N , and P . A vertical line labeled E is on the left. Part (b) is a graph of Impurity concentration versus Depth. The depth axis is vertical, pointing downwards. The impurity concentration profile shows a step-like function corresponding to the layers in (a). The concentration is high in the N^+ region, drops in the N^- region, rises in the N region, and drops again in the P region. The profile is labeled with 1, 2, 3, 4, 5, 6, 7, 8, and 9 at the boundaries between layers.

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明 細 書

1. 発明の名称

半導体装置

2. 特許請求の範囲

(1) 第1導電型の第1領域と、

前記第1領域の一方の主表面上に形成された第2導電型の第2領域と、

前記第2領域の上層部に少なくとも1箇所部分的に形成された第1導電型の第3領域と、

前記第3領域の上層部に部分的に形成された第2導電型の第4領域と、

前記第2領域の主表面から前記第4領域の主表面に至る前記第3領域の主表面を少なくとも覆うように形成された絶縁体と、

前記第1領域の他方の主表面に形成された第1電極と、

前記絶縁体の主表面上に形成された第2電極と、
少なくとも前記第4領域の主表面に接するように形成された第3電極とを有する半導体装置において、

前記第2領域内における不純物分布が主表面に対して垂直な方向に勾配を有することを特徴とする半導体装置。

(2) 前記第2領域は、前記第1領域に接する中濃度不純物領域と前記第3領域に接する低濃度不純物領域の2層構造に仕上げられ、前記中濃度不純物領域内の不純物濃度が前記低濃度不純物領域から前記第1領域に向かうにつれて減少するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

(3) 前記中濃度不純物領域内の不純物濃度が前記低濃度不純物領域から前記第1領域に向かうにつれて増加するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

(4) 前記低濃度不純物領域内の不純物濃度が前記第3領域から前記中濃度不純物領域に向かうにつれて増加するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

(5) 前記低濃度不純物領域内の不純物濃度が前記中濃度不純物領域から前記第3領域に向かう

につれて増加するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

3. 発明の詳細な説明

(産業上の利用分野)

この発明は半導体装置、特に絶縁ゲート型バイポーラトランジスタ(以下「IGBT」という)のターンオフ時間の改善に関するものである。

(従来の技術)

第5図(a)は従来のIGBTの断面図であり、同図(b)はE-E線に沿った各領域における不純物分布を模式的に示した図である。同図において、1は高濃度で均一にP型不純物が分布されている第1P型領域であり、この第1P型領域1の一方の主表面上に中濃度で均一にN型不純物が分布されている第1N型領域2が形成されている。また、この第1N型領域2上に低濃度で均一にN型不純物が分布されている第2N型領域3が形成されている。そして、この第2N型領域3の上層部に中濃度で均一にP型不純物が分布されている第2P型領域4が複数相互に隔離されて形成されており、

さらに、この第2P型領域4のそれぞれの上層部に高濃度で均一にN型不純物が分布されている第3N型領域5が部分的に形成されている。そして、第2N型領域3の主表面および第2P型領域4の主表面の一部上に絶縁薄膜6を介してゲート電極7が形成されている。また、第2P型領域4の主表面の残りの部分および第3N型領域5の主表面上にエミッタ電極8が形成されている。一方、第1P型領域1の他方の主表面にはコレクタ電極9が積層して形成されている。

次に、上記IGBTの動作機構について説明する。まず、通常の動作状態では、エミッタ電極8に対して負荷抵抗を通して正の直流高電圧をコレクタ電極9に印加し、さらに、正のステップ状電圧をゲート電極7に印加する。このようにステップ状の正電圧がゲート・エミッタ間に印加されると、第2P型領域4と絶縁薄膜6との境界面にNチャネルが形成され、そのNチャネルを通して第3N型領域5から第2N型領域3および第1N型領域2に電子が注入される。そのため、第2N

型領域3および第1N型領域2の電位が低下し、第1P型領域1と第1N型領域2との界面にあるP-N接合が順方向バイアスされることとなり、第1P型領域1から第1N型領域2および第2N型領域3に正孔が注入される。注入された電子と正孔は電気的に中和されるので、第3N型領域5および第1P型領域1からそれぞれ電子および正孔がさらに補充されて多数注入され、第1N型領域2および第2N型領域3に多数の正孔および電子が蓄積される。その結果、第1N型領域2および第2N型領域3の比抵抗が低下し、コレクタ電極9からエミッタ電極8へ大電流が流れIGBTは導通状態になる。

次に、ゲート電極7への正電圧の印加がなくなると、第2P型領域4と絶縁薄膜6との界面のNチャネルが消滅し、第3N型領域5から第2N型領域3および第1N型領域2の電子への注入がなくなる。このような電子注入による電流は、第1P型領域1をエミッタ、第2N型領域3と第1N型領域2をベース、また第2P型領域4をコレク

タとするPNPトランジスタのベース電流に相当している。したがって、電子注入がなくなった場合のIGBTの電流は、近似的にPNPトランジスタにおいてベース電流がなくなった場合のPNPトランジスタの電流に等しいと考えられる。つまり、電子注入がなくなった場合、IGBTを流れる電流は減少し、その波形は模式的に第6図に示すようになる。

第6図において、縦軸はIGBT中を流れる電流であり、横軸は時間を示す。同図に示すように、時刻 $t = t_0$ においてゲート電極の正電圧がなくなると、電流は瞬間的に I_0 から I_1 に減少したのち、徐々に零まで減少する。

(発明が解決しようとする問題点)

このIGBTの電流特性を表す要素のひとつとして、ターンオフ時間 t_{off} がある。このターンオフ時間 t_{off} は、

$$t_{off} = t_1 - t_0 \quad \dots (1)$$

と定義される。ここで、 t_0 はゲート電極の正電圧がなくなる時刻であり、 t_1 は電流が0.1

I_0 になる時刻である。

同図からわかるように、このターンオフ時間 t_{off} は時刻 t_0 から時刻 t_1 にかけての減衰領域における電流の減衰特性に依存する。そこで、上記のごとく、この IGBT が PNP トランジスタに類似していることから減衰領域における電流波形を

$$I(t) = I_1 \exp\left(-\frac{t-t_0}{\beta\tau_b}\right) \quad \dots (2)$$

のように近似的に表すことができる。ここで、 β は PNP トランジスタにおけるエミッタ接地電流利得であり、 τ_b は PNP トランジスタにおけるベース走行時間である。(2) 式において、 $\beta\tau_b$ の値を小さくすれば減衰領域における減衰が顕著になり、IGBT のターンオフ時間 t_{off} を短くすることができる。さらに、 $\beta\tau_b$ の近似式は、

$$\beta\tau_b = \frac{\tau\alpha_T}{1-\alpha_T} \tau_b \quad \dots (3)$$

ただし、

減少するため、実効抵抗が大きくなるという問題点があった。

この発明は上記のような問題点を解消するためになされたものであり、ターンオフ時間が短く、かつ導通状態での実効抵抗が小さい半導体装置を得ることを目的とする。

(問題点を解決するための手段)

この発明に係る半導体装置は、第1導電型の第1領域と、前記第1領域の一方の主表面上に形成された第2導電型の第2領域と、前記第2領域の上層部に少なくとも1箇所部分的に形成された第1導電型の第3領域と、前記第3領域の上層部に部分的に形成された第2導電型の第4領域と、前記第2領域の主表面から前記第4領域の主表面に至る前記第3領域の主表面を少なくとも覆うように形成された絶縁体と、前記第1領域の他方の主表面上に形成された第1電極と、前記絶縁体の主表面上に形成された第2電極と、少なくとも前記第4領域の主表面に接するように形成された第3電極とを有する半導体装置において、前記第2領域

$$\alpha_T = \operatorname{sech}\left(\sqrt{\frac{2\tau_b}{\tau_{eff}}}\right) \quad \dots (4)$$

となる。ここで、 τ は PNP トランジスタのエミッタ注入効率であり、 α_T は PNP トランジスタのベース輸送効率であり、 τ_{eff} は PNP トランジスタのベース領域内での実効キャリア寿命である。

従来においては、IGBT のターンオフ時間 t_{off} を短くするために電子ビーム照射等により PNP トランジスタのベース領域内での実効キャリア寿命 τ_{eff} を小さくするようにしていた。すなわち、この PNP トランジスタのベース領域内での実効キャリア寿命 τ_{eff} を小さくすることにより $\beta\tau_b$ の値が小さくなり、その結果、減衰領域における電流の減衰が顕著になり IGBT のターンオフ時間 t_{off} が短くなる。

しかしながら、このように PNP トランジスタのベース領域内での実効キャリア寿命 τ_{eff} を小さくすると、導通状態で第1N型領域2および第2N型領域3に蓄積される正孔および電子の数が

内における不純物分布が主表面に対して垂直な方向に勾配を有するように定めている。

(作用)

この発明における半導体装置は、第2領域内における不純物分布が主表面に対して垂直な方向に勾配を有するようにしたことにより、前記第2領域内に内蔵電界が発生し、この内蔵電界により前記第2領域内でのキャリアの実効的な拡散定数が制御されてターンオフ時間を短くする。

(実施例)

第1図(a)はこの発明に係る一実施例である IGBT の断面図であり、同図(b)は A-A 線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は第1N型領域2におけるN型不純物の分布のみである。同図(b)に示すように、第1N型領域2におけるN型不純物の濃度は第1P型領域1との境界面で最低であり、第2N型領域3に近づくにしたがってその値は高くなっていき、第2N型領域3との境界面で従来と同じく中濃度となる。

このように第1N型領域2におけるN型不純物の濃度に傾斜を設けたことにより第1N型領域2ないで内蔵電界が発生する。ここで、N型不純物濃度の傾斜によりどのような内蔵電界が発生するかについて詳説する。この内蔵電界とN型不純物の分布との関係は、

$$E(x) = -\frac{kT}{q} \cdot \frac{1}{N(x)} \cdot \frac{dN(x)}{dx} \quad \dots (5)$$

である。ここで、 $E(x)$ は内蔵電界であり、 k はボルツマン定数であり、 T は絶対温度であり、 q は電子の電荷量であり、 $N(x)$ はN型不純物濃度分布である。(5)式からわかるように、内蔵電界の方向とN型不純物濃度分布の勾配とが逆方向である。そのため、第1図に示すようなN型不純物濃度分布を示す場合には内蔵電界は第2N型領域3から第1P型領域1に向っている。このような内蔵電界は第1P型領域1から注入され第2N型領域3に拡散しようとしている正孔の拡散を阻止する方向に働くので、実効的な正孔の拡散定数は小さくなる。

沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は、同図(b)に示すように、第2N型領域3におけるN型不純物の濃度は第2P型領域4との境界面で従来と同じく低濃度であり、第1N型領域2に近づくにしたがってその値は高くなっていき、第1N型領域2との境界面で第1N型領域2におけるN型不純物の濃度と同じく中濃度となるようにしたことである。

このように第2N型領域3におけるN型不純物の濃度に第1図に示したものと逆の傾斜を設けたことにより第2N型領域3内で第1図に示したものと逆の内蔵電界が発生する。したがって、この内蔵電界が正孔の拡散を加速する方向に働くので、実効的な正孔の拡散定数は大きくなる。

第4図(a)はこの発明に係る他の実施例であるIGBTの断面図であり、同図(b)はD-D線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は、同図(b)に示すように、第2N型領域3における

第2図(a)はこの発明に係る他の実施例であるIGBTの断面図であり、同図(b)はB-B線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は、同図(b)に示すように、第1N型領域2におけるN型不純物の濃度が第2N型領域3との境界面で第2N型領域3におけるN型不純物の濃度と同じく低濃度であり、第1P型領域1に近づくにしたがってその値は高くなっていき、第1P型領域1との境界面で従来と同じく中濃度となるようにしたことである。

このように第1N型領域2におけるN型不純物の濃度において第1図に示したものと逆の傾斜を設けたことにより、第1N型領域2内で第1図に示したものと逆の内蔵電界が発生する。したがって、この内蔵電界が正孔の拡散を加速する方向に働くので、実効的な正孔の拡散定数は大きくなる。

第3図(a)はこの発明に係る他の実施例であるIGBTの断面図であり、同図(b)はC-C線に

N型不純物の濃度は第1N型領域2との境界面で従来と同じく低濃度であり、第2P型領域4に近づくにしたがってその値は高くなっていき、第2P型領域4との境界面で従来よりもやや高い濃度となるようにしたことである。

このように第2N型領域3におけるN型不純物の濃度に第1図に示したものと同じ傾斜を設けたことにより第2N型領域3内で第1図に示したものと同じ内蔵電界が発生する。したがって、この内蔵電界が正孔の拡散を阻止する方向に働くので、実効的な正孔の拡散定数は小さくなる。

以上のように、第1N型領域2あるいは第2N型領域3における不純物分布を主表面に対して垂直な方向に勾配を有するようにすることにより第1N型領域2あるいは第2N型領域3に適当な内蔵電界が発生して、この第1N型領域2あるいは第2N型領域3での正孔の実効的な拡散定数を制御することができる。

次に、この正孔の実効的な拡散定数を制御することによりIGBTのターンオフ時間を短くする

ことができる原理について説明する。

ここでベース領域、言い換えれば第1N型領域2および第2N型領域3の厚みが変らないと仮定すると、正孔の拡散定数が大きくなるとベース走行時間が小さくなり、逆に正孔の拡散定数が小さくなると、ベース走行時間が大きくなる。すなわち、正孔の拡散定数を制御することによりベース走行時間を制御することができる。さらに、このベース走行時間を制御することにより、IGBTのターンオフ時間を制御することができる。ここで、その理由について詳説する。

まず、 $\beta \tau_b$ の近似式である(3)式をベース走行時間 τ_b で微分すると、

$$\frac{dy}{d\tau_b} > 0 \quad \text{但し} \quad \frac{2\tau_b}{\tau_{eff}} < \sqrt{2} \quad \dots (6)$$

$$\frac{dy}{d\tau_b} < 0 \quad \text{但し} \quad \frac{2\tau_b}{\tau_{eff}} > \sqrt{2} \quad \dots (7)$$

となる。(6)式が成立する場合には、ベース走行

時間 τ_b が小さくなるにしたがってターンオフ時間 t_{off} は短くなり、一方、(7)式が成立する場合には、ベース走行時間 τ_b が大きくなるにしたがってターンオフ時間 t_{off} は短くなる。

以上のように第1N型領域2あるいは第2N型領域3の不純物濃度分布に傾斜をもたせ、その結果として、第1N型領域2あるいは第2N型領域3に発生する内蔵電界により正孔の拡散定数、ひいてはベース走行時間を制御し、これによりIGBTのターンオフ時間を短くすることができる。また、上記のようにしてターンオフ時間を短くすることができ、従来のように第1N型領域2あるいは第2N型領域3の実効キャリア寿命を小さくする必要がないので、第1N型領域2あるいは第2N型領域3の実効抵抗は低く抑えることができる。

次に、この発明に係る半導体装置の製造方法について第1図を基に説明する。まず、気相エピタキシャル成長法により第1P型領域1上に第1N型領域2を形成する。この気相エピタキシャル成

長を行なう際、成長の膜厚に応じて徐々にN型不純物の濃度を高くすることにより第1図(b)に示すようなN型不純物濃度の分布を持った第1N型領域2が得られる。次に、気相エピタキシャル成長法により第1N型領域2上に第2N型領域3を形成する。さらに、通常の二重拡散型MOSトランジスタの製造工程を適用することにより、第2P型領域4、第3N型領域5、絶縁薄膜6、ゲート電極7およびエミッタ電極8を形成して同図に示すIGBTを製造することができる。

また、第1N型領域3に第2図に示すようなN型不純物濃度の分布の勾配を持たせる場合には、気相エピタキシャル成長法により第1P型領域1上に第1N型領域2を形成する際に、成長の膜厚に応じて徐々にN型不純物の濃度を低くしてやればよい。

また、第2N型領域3に第3図や第4図に示すようなN型不純物濃度の分布の勾配を持たせる場合には、気相エピタキシャル成長法により第1N型領域2上に第2N型領域3を形成する際に、成

長の膜厚に応じて徐々にN型不純物の濃度を変化させてやればよい。

(発明の効果)

以上のように、この発明の半導体装置によれば、不純物濃度の分布によって発生する内蔵電界を利用してキャリアの実効拡散定数を、ひいてはベース走行時間を制御することによりターンオフ時間を短くしているので、導通状態での実効抵抗が増加することなく、高性能の半導体装置が得られる効果がある。

4. 図面の簡単な説明

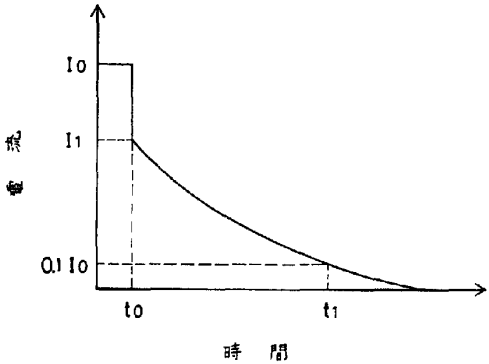
第1図はこの発明に係る一実施例を示す図、第2図ないし第4図はこの発明に係る他の実施例を示す図、第5図は従来例を示す図、第6図はIGBTのゲート電極への電圧印加を停止した際の時間と電流との関係を示す図である。

図において、1は第1P型領域、2は第1N型領域、3は第2N型領域、4は第2P型領域、5は第3N型領域、6は絶縁薄膜、7はゲート電極、8はエミッタ電極、9はコレクタ電極である。

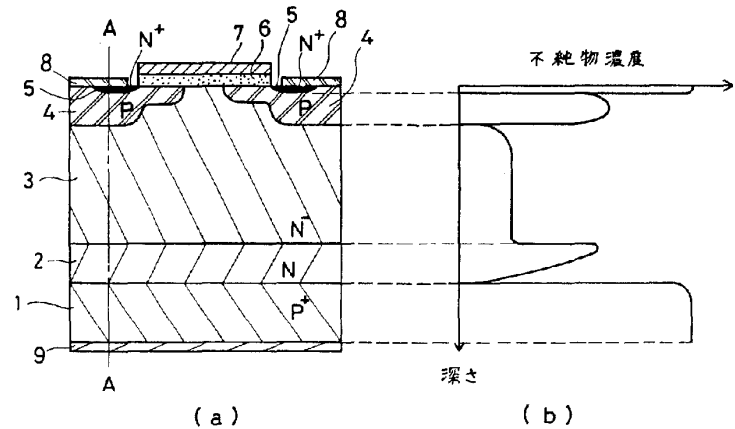
なお、各図中同一符号は同一または相当部分を示す。

代理人 大 岩 増 雄

第 6 図

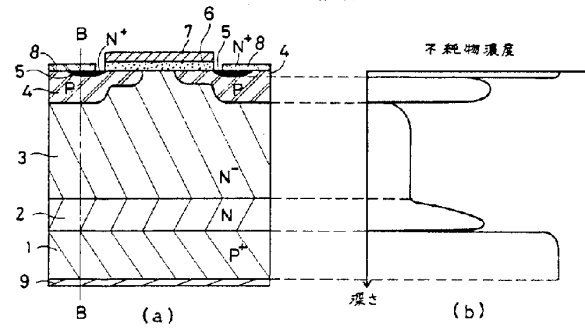


第 1 図

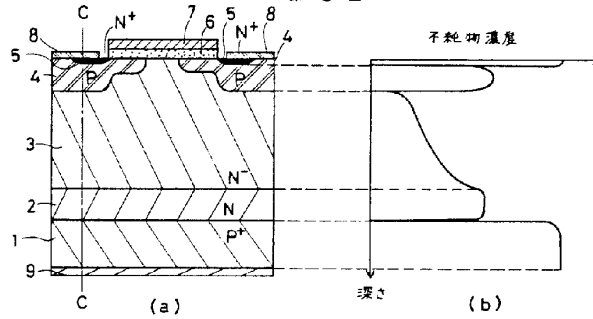


- | | |
|-----------|-----------|
| 1: 第1P型領域 | 2: 第1N型領域 |
| 3: 第2N型領域 | 4: 第2P型領域 |
| 5: 第3N型領域 | 6: 絶縁薄膜 |
| 7: ゲート電極 | 8: エミッタ電極 |
| 9: コレクタ電極 | |

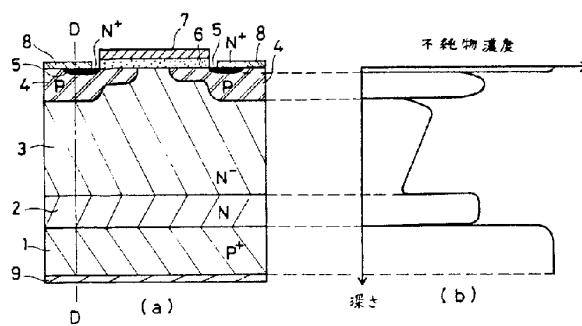
第 2 図



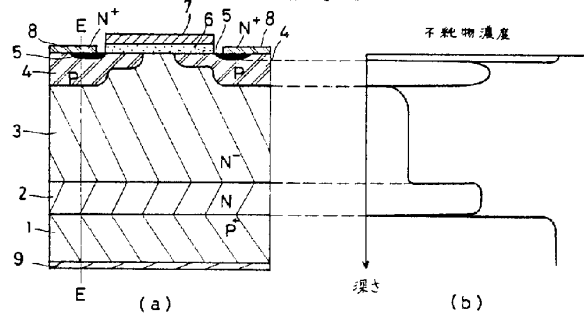
第 3 図



第 4 図



第 5 図



**JP2003218356A METHOD FOR MANUFACTURING AND DESIGNING SOI TYPE
SEMICONDUCTOR DEVICE, AND SOI TYPE SEMICONDUCTOR DEVICE**

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[0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to an SOI type semiconductor device manufacturing method, design method and SOI type semiconductor device having an SOI semiconductor layer formed on a semiconductor substrate with a buried insulating film interposed.

[0002] 2. Description of the Related Art SOI (Silicon On Insulator) structure facilitates complete isolation from the substrate or between elements, reducing various parasitic capacitances, and suppressing soft errors and latch-up characteristic of CMOS transistor circuits. become. For this reason, the role that SOI isolation technology plays in increasing the speed, lowering the voltage, and improving the reliability of so-called SOI-type CMOS LSIs has become increasingly important.

[0003] On the other hand, in many CMOS LSIs at present, P-type and N-type wells are formed in a semiconductor substrate (semiconductor bulk), N-type channel NMOS transistors are formed in the P-type well, and P-type wells are formed in the N-type well. This is a so-called bulk type semiconductor device in which a type-channel PMOS transistor is formed.

[0004] However, when designing an SOI type semiconductor device, since it has a substrate structure different from that of a bulk type semiconductor device having the same function, an already designed bulk type semiconductor device is provided. The layout pattern cannot be applied as it is. Therefore, in many cases, it has been necessary to re-design the pattern for SOI type semiconductor devices. This is because the bulk semiconductor device requires an electrode for fixing the well potential, while the SOI type semiconductor device uses the SOI semiconductor layer in a floating state, fixes the potential, or fixes the semiconductor substrate potential. One of the main reasons was the existence of various potential fixing methods.

[0005] The first object of the present invention is suitable, for example, when the SOI semiconductor layer is in a floating state and the substrate potential is fixed, and the layout pattern used in the bulk type semiconductor device is changed to the SOI type with a minimum change. An object of the present invention is to provide a design method for converting to a layout pattern of a semiconductor device and a method for manufacturing an SOI type semiconductor device including a step of forming a photomask using the method. A second object of the present invention is to provide an SOI type semiconductor device having a structure capable of making substrate contact even if the layout pattern of elements and wirings used in a bulk type semiconductor device is applied as it is.

[0006] According to a first aspect of the present invention, there is provided an SOI type semiconductor device manufacturing method for achieving the first object, wherein a buried insulating film is formed on a semiconductor substrate. A method for manufacturing an SOI type semiconductor device in which elements are integrated in an SOI semiconductor layer formed through the interposition, and corresponds to a well contact region of a bulk type semiconductor device in which elements are integrated in a well formed in a semiconductor substrate. A step of modifying the pattern of the element isolation insulating layer of the bulk type semiconductor device to form a photomask so that the element isolation insulating layer is also formed at the location, and the inside of the SOI semiconductor layer using the formed photomask Forming an element isolation insulating layer on the substrate, dividing the SOI semiconductor layer into a plurality of active layers in which elements are formed, and a portion corresponding to a well contact region of the bulk type semiconductor device Etching the element isolation insulating layer and the buried insulating film therebelow to form a substrate contact region, and utilizing a photomask for a well contact of the bulk type semiconductor device, the substrate in the substrate contact region Forming a contact plug.

[0007] Preferably, the method further includes a step of forming a source / drain impurity region to be a source or a drain of the insulated gate transistor in the active layer, and the same impurity is implanted from the substrate contact region simultaneously with the formation of the source / drain impurity region. Then, impurity regions for substrate contact connection are formed in the semiconductor substrate. Alternatively, preferably, a step of forming a source / drain impurity region to be a source or drain of an insulated gate transistor in the

active layer, and a step of forming a voltage supply plug connected on the source / drain impurity region; A step of forming a voltage supply wiring layer connected on the voltage supply plug, and in the step of forming the substrate contact plug, the well contact and source / drain impurity regions of the bulk type semiconductor device are formed. A contact opening using a photomask for simultaneously forming a voltage supply contact is formed, and the substrate contact plug is formed simultaneously with the voltage supply plug.

[0008] Preferably, the step of forming the element isolation insulating layer includes a step of forming a mask layer around a region where the element isolation insulating layer is to be formed, and an etching using the mask layer to form the buried insulating film on the SOI semiconductor layer. A step of forming a trench reaching, a step of depositing an element isolation insulating film filling the entire surface of the trench, and a step of partially removing the element insulating film around the trench, and forming the substrate contact region, Simultaneously with the step of removing the element isolation insulating film around the trench. In that case, the mask layer at the time of forming the trench includes a stopper film made of a material having a high etching selectivity with respect to the element isolation insulating film. In the step of forming the substrate contact region, the semiconductor surface of the active layer is formed by the stopper film. It is preferable to expose the surface portion of the semiconductor substrate to be contacted while protecting. Or after the said trench formation, you may further have the process of removing the said embedded insulating film part exposed in the trench by the etching using the said mask layer used for the said trench formation as it is.

[0009] An SOI type semiconductor device design method according to a second aspect of the present invention is for achieving the first object, and a bulk type semiconductor device in which elements are integrated in a well formed in a semiconductor substrate. The method for designing an SOI type semiconductor device includes a step of converting a pattern for use into an SOI type semiconductor device in which elements are integrated in an SOI semiconductor layer formed on a substrate with a buried insulating film interposed therebetween. When the bulk type semiconductor device has a well contact, the well contact pattern is used as it is as a substrate contact pattern reaching the semiconductor substrate of the SOI type semiconductor device in the conversion step.

[0010] Preferably, in the conversion step, the pattern of the element isolation insulating layer of the bulk type semiconductor device is partially modified so that the well contact region becomes the element isolation insulating layer, and the element isolation isolation of the SOI type semiconductor device is performed. Generating a pattern of layers. In that case, more preferably, the pattern for the bulk type semiconductor device is a pattern for partially removing the element isolation insulator deposited so as to be embedded in the trench when the element isolation insulating layer is formed by etching around the trench. And the conversion step adds a pattern of openings to the pattern for removing the element isolation insulator around the trench of the bulk semiconductor device so that the well contact region is also etched. And a step of generating a pattern for forming an impurity region for connecting a substrate contact of the SOI type semiconductor device on the semiconductor substrate.

[0011] In such an SOI type semiconductor device design method, a layout pattern for a bulk type semiconductor device can be easily converted into a layout pattern for an SOI type semiconductor device with only a slight modification of the pattern of the element isolation insulating layer. . If there is no step of removing the element isolation insulating film around the trench, a layout pattern dedicated to the substrate contact is required separately from this.

[0012] In addition, in the manufacturing method of the SOI type semiconductor device described above, it is necessary to correct the photomask in one step (element isolation step), and if necessary, a new photomask is added in one step (substrate contact region forming step). Is required. Thus, the change from the well contact to the substrate contact is very easy.

[0013] An SOI type semiconductor device according to a third aspect of the present invention is for achieving the second object described above, and an element is formed on an SOI semiconductor layer formed on a semiconductor substrate with a buried insulating film interposed therebetween. An SOI type semiconductor device in which a chip integrated with a semiconductor chip is fixed on a die pad of a lead frame in a state where the semiconductor substrate is electrically connected to the die pad, and an element formed in the SOI semiconductor layer and its wiring have the same function. By forming the pattern for the bulk type semiconductor device having the island-shaped SOI semiconductor layer portion surrounded by the element isolation insulating layer at a location corresponding to the well contact region of the bulk type semiconductor device. Then, the island-shaped SOI semiconductor layer portion is connected to a wiring for supplying a ground potential or a power supply voltage to the element, so that the wiring, bonding pad, It is electrically

connected to the die pad via the Ya.

[0014] In this SOI type semiconductor device, the layout pattern at the time of forming the elements and wirings is the same as that of the bulk type semiconductor device. Therefore, in the bulk type, an isolated SOI semiconductor layer portion is necessarily formed at a position corresponding to the well contact region. However, this part is not used for the substrate contact. The substrate contact is achieved by electrically connecting the semiconductor substrate to a wiring for supplying a ground potential or a power supply voltage to the transistor via a bonding pad, a wire, and a die pad of a lead frame.

[0015] DESCRIPTION OF THE PREFERRED EMBODIMENTS [First Embodiment] A first embodiment of the present invention will be described below with reference to the drawings, taking as an example a CMOS logic LSI having an SOI type substrate separation structure. FIG. 1 and FIG. 2 are an inverter and a NAND gate showing examples of gate circuits in a CMOS logic LSI. In each figure, (A) shows each gate circuit symbol, and (B) is a pattern plan view of each gate circuit in this embodiment adopting an SOI type substrate separation structure.

[0016] The pattern of the inverter 1 shown in FIG. 1B includes a region (PMOS region) 2 where a P-type MOS transistor and a region (NMOS region) 3 where an N-type MOS transistor is formed. It is divided roughly into. An N-type active layer 21 made of a semiconductor doped with an N-type impurity is formed in the PMOS region 2, and a P-type active layer 31 made of a semiconductor doped with a P-type impurity is formed in the NMOS region 3. Has been. The periphery of these active layers 21 and 31 is surrounded by the element isolation insulating layer 4 to achieve isolation between elements.

[0017] A gate electrode 5 to which an input signal of the inverter is applied is overlaid on these active layers 21 and 31. The gate electrode 5 is made of doped polycrystalline silicon to which an impurity is added, for example, and impurities of different conductivity types are arranged as necessary. In general, in order to make each MOS transistor a buried channel type and to be strong against a fine shape effect such as a short channel effect, a P-type impurity is present in the gate electrode portion on the PMOS side, and an N-type impurity is present in the gate electrode portion on the NMOS side. Is added. P-type impurities are implanted into the surface of the N-type active layer 21 using the gate electrode 5 as a mask, thereby forming a source impurity region S2 and a drain impurity region D2. Similarly, N-type impurities are implanted into the surface of the P-type active layer 31 using the gate electrode 5 as a mask, thereby forming a source impurity region S3 and a drain impurity region D3. A gate contact GC that constitutes an input terminal of the inverter is provided at the center of the gate electrode 5.

[0018] The source impurity region S2 of the PMOS transistor is electrically connected to the supply line (VDD line) 6 of the power supply voltage Vdd made of the upper metal layer via the source contact SCp on the PMOS transistor. The drain impurity region D2 of the PMOS transistor is electrically connected to the drain impurity region D3 of the NMOS transistor via the drain contact DCp, the internal connection line 7 made of an upper metal layer, and the drain contact DCn. Further, the source impurity region S3 of the NMOS transistor is connected to a power supply voltage GND supply line (GND line) 8 made of an upper metal layer through a source contact SCn thereon.

[0019] In the pattern of the NAND gate 10 according to this embodiment shown in FIG. 2B, two PMOS transistors are arranged in parallel in the N-type active layer 21. The source impurity regions S2a and S2b of the two PMOS transistors are electrically connected to the upper VDD line 6 via source contacts SCa and SCb, respectively. The common drain-in impurity region D2 between the two PMOS transistors is electrically connected to the output line 9 made of the upper metal layer via the drain contact DCp.

[0020] On the other hand, two NMOS transistors are arranged in parallel in the P-type active layer 31. The two NMOS transistors are electrically connected in series, and are inserted between the output line 9 and the GND line. That is, the drain impurity region D3 of one NMOS transistor is connected to the output line 9 via the drain contact DCn, and the source impurity region S3 of the other NMOS transistor is connected to the GND line 8 via the source contact SCn. Since the common source / drain region SD between the two NMOS transistors is not connected to the other, it is in a floating state when both transistors are off.

[0021] The gate electrode 4a to which the first input signal is applied from the gate contact GCa is disposed on the left side of the figure, and the gate electrode 4b to which the second input signal is applied from the gate contact GCb is disposed on the left side of the figure. The gate electrode intersects the N-type active layer 21 and the P-type active layer 31.

[0022] The gate circuit configured in this way has an SOI type configuration. FIG. 3 shows a cross-sectional structure of an inverter as a representative. This figure is a schematic cross-sectional view along the line BB in FIG. In this embodiment, a buried insulating film 11 made of silicon dioxide or the like is formed on a semiconductor substrate 10 made of an N-type silicon wafer or the like, and a silicon layer (hereinafter referred to as an SOI semiconductor layer) having an SOI type substrate isolation structure formed thereon. The N-type active layer 21, the P-type active layer 31, and the element isolation insulating layer 4 described above are formed in 12. Further, source impurity regions S2 and S3 (and drain impurity regions D2 and D3) are formed on the surface portion in the N-type active layer 21.

[0023] An interlayer insulating film 13 made of, for example, silicon dioxide is deposited on the entire surface of the SOI semiconductor layer 12. Plugs made of metal, doped polycrystalline silicon, or the like are embedded in the interlayer insulating film 13, thereby forming the source contacts SCp and SCn. The source contact SCp is connected to the source impurity region S2 on the PMOS side, and the source contact SCn is connected to the source impurity region S3 on the NMOS side. On the interlayer insulating film 13, the VCC line 6 connected to the source contact SCp and the GND line 8 connected to the source contact SCn are formed. These wirings 6 and 8 are made of a metal layer such as aluminum.

[0024] By the way, in an SOI type semiconductor device, there may be a case where a substrate contact for fixing a semiconductor substrate in potential with a constant voltage is required. An SOI-type MOS transistor may be used when an SOI semiconductor layer is used with a potential fixed, or may be used while a potential is floating. If the thickness of the so-called SOI semiconductor layer is reduced to about 50 nm, the SOI semiconductor layer is completely depleted in the thickness direction during operation, resulting in a fully depleted device. In this case, in order to suppress fluctuations in threshold value, substrate bias and it is often performed to fix the semiconductor substrate in potential with the same idea. Even when the SOI semiconductor layer is relatively thick and partially depleted, it is possible to fix the potential of the SOI semiconductor layer only in a circuit portion critical to threshold fluctuations and use the other SOI semiconductor layers in a floating state. Many. This is because the number of contacts to the SOI semiconductor layer is reduced as much as possible to suppress an increase in area. Even in this case, a substrate bias is often applied with the intention of suppressing threshold fluctuation as much as possible or reducing leakage at the interface between the SOI semiconductor layer and the buried insulating film.

[0025] This embodiment corresponds to the case where the substrate bias is applied without fixing the potential of the SOI semiconductor layer, and the ground potential VGND is applied to the semiconductor substrate 10. Therefore, it is necessary to short-circuit the semiconductor substrate 10 with the GND line 8. Specifically, as shown in FIG. 3, the element isolation insulating layer 4 and a portion of the buried insulating film 11 therebelow are opened, and the upper GND is placed in the interlayer insulating film 13 buried therein. A substrate contact VSC made of a plug reaching the line 8 is formed. An N-type contact impurity region 14 having a higher concentration than the substrate bulk is formed on the surface portion in the semiconductor substrate 10 provided with the substrate contact VSC. The reason why the element isolation insulating layer 4 and a part of the buried insulating film 11 therebelow are opened is to form the contact impurity region 14. This formation is desirably performed simultaneously with the source impurity region S3 (and the drain impurity region D3) of the NMOS transistor. In this sense, the semiconductor substrate 10 of this embodiment is an N type.

[0026] When this part is seen in the plan view of FIG. 1 (A), at the branch branch point extending from the backbone of the GND line 8 arranged in the lateral direction so as to be shared with the adjacent gate circuit (not shown) to the NMOS side. A substrate contact VSC is provided, and a large contact impurity region 14 is formed around the substrate contact VSC.

[0027] On the other hand, also in the VDD line 6, a contact VDC is formed at a branch branch point extending from the trunk to the PMOS side. However, as shown in FIG. 3, the contact VDC is connected via a contact impurity region 16 to an active layer 15 surrounded by the element isolation insulating layer 4 and in a potential floating state. These contact VDC, active layer 15 and contact impurity region 16 are unnecessary in terms of circuit function, and are inevitably formed by sharing a pattern with the bulk type semiconductor device of the comparative example, as will be described later. It is a part that ends up.

[0028] In the case where it is desired to shift the circuit configuration and the threshold as a whole, the substrate bias can be performed by applying the power supply voltage Vdd. In that case, the pattern is changed so that the element isolation insulating layer 4 is formed also in this portion so that the contact VDC reaches the

semiconductor substrate 10. The contact impurity region 16 is preferably formed simultaneously with the P-type impurity region (source impurity region S2 and drain impurity region D2) of the PMOS transistor.

[0029] Next, a comparative example of a bulk structure inverter will be described in comparison with such an SOI structure inverter.

[0030] FIG. 1C is a pattern plan view of a bulk type inverter in which the same function is formed in a semiconductor bulk or well as a comparative example. FIG. 4 is a schematic sectional view taken along the line CC of FIG. The plane pattern of the bulk type inverter 100 is almost the same as the plane pattern of the SOI type inverter described above. A slightly different point is that an active layer (well) is exposed at a position where the SOI type substrate contact VSC is provided, and a well contact impurity region 101 is formed on the surface portion thereof. In the illustrated example, the pattern of the well contact impurity region 101 is the same as the pattern of the substrate contact VSC in the SOI type. The other patterns are the same as those of the bulk type, and unless otherwise specified, in FIG. 1C, the same reference numerals as those in FIG.

[0031] In the cross section of FIG. 4, the substrate structure is different from the SOI type. An N-type well 103 serving as an active layer of a PMOS transistor and a P-type well 104 serving as an active layer of an NMOS transistor are formed on a semiconductor substrate 102 made of a silicon wafer of any conductivity type. The surface portions in and around the wells are separated by the element isolation insulating layer 4.

[0032] Source impurity regions S2, S3 (and drain impurity regions D2, D3) are formed in the same pattern as the SOI type on the surface portion in the N-type well 103 and the surface portion in the P-well 104. A well contact portion is provided in each of the N well 103 and the P well 104 in a state separated from the impurity regions of these transistors by the element isolation insulating layer 4. The well contact portion of the N well 103 is an N-type contact impurity region 16 provided on the inner surface of the well, and a plug connecting the upper surface of the contact impurity region 16 and the upper VDD line 6. It consists of a well contact NWC. The N well contact NWC corresponds to the SOI type contact VDC, and is embedded in the interlayer insulating film 13.

[0033] Similarly, the well contact portion of the P well 4 is a plug provided on the inner surface of the well for connecting the higher concentration N-type contact impurity region 101, the upper surface of the contact impurity region 101, and the upper GND line 8. And a P-well contact NWC. The P well contact PWC is provided in place of the SOI type substrate contact VSC, and is buried in the interlayer insulating film 13.

[0034] Other configurations, that is, the gate electrode 4, the gate contact GC, the source contacts SCp and SCn, the drain contacts DCp and DCn, the interlayer insulating film 13, the VDD line 6 and the GND line 8 are made of the same pattern and material as the SOI type described above. .

[0035] Such a difference in pattern and structure is the same in the NAND gate circuit. The description is abbreviate | omitted with the same code | symbol.

[0036] When a new SOI type semiconductor device having the same function is newly designed using the existing pattern and layout data of the bulk type semiconductor device having such a configuration, a part of the pattern of the element isolation insulating film 4 is first modified. Specifically, in the case of the illustrated inverter, for example, the opening of the pattern of the element isolation insulating film 4 is eliminated for the P-well contact on the NMOS side.

[0037] In addition, a pattern for partially opening the element isolation insulating layer 4 and the buried insulating film 11 thereunder is required for the substrate contact. As will be described later, if a process for selectively etching the insulating film deposited on the entire surface when the element isolation insulating layer 4 is formed on the active layer is necessary, the pattern at the time of the selective etching is changed. It can be dealt with by correcting. In that case, no photomask is added. On the other hand, when such a selective etching process is not originally performed, a new photomask is added for the substrate contact.

[0038] In this way, conversion from bulk type to SOI type can be performed by performing pattern correction twice or by adding one pattern layer for making a new additional photomask. In addition, these pattern corrections and creation of new patterns are simple and simple by adding at least one simple rectangular pattern. Therefore, there is an advantage that the cost associated with the change of the substrate separation structure can be suppressed as much as possible. In addition, since there is no change in the effective element pattern, it is possible to easily estimate the effect of improving characteristics due to the change from the bulk type to the

SOI type. This is because there is no change in the element characteristic parameter depending on the planar pattern shape, and the improvement of the characteristic due to the change of the substrate separation structure is reflected in the electric characteristic of the element as it is.

[0039] Finally, an embodiment of the method for manufacturing the SOI type semiconductor device will be described by taking an inverter as an example. 5 to 11 are cross-sectional views in the middle of manufacturing this inverter. First, a substrate having an SOI type substrate separation structure (SOI substrate) is formed by a known method. For example, in the method of laminating the substrates, a buried insulating film 11 is formed on the surface of a first silicon wafer (substrate to be polished) to be the SOI semiconductor layer 12, and further, for example, polycrystalline silicon or the like is formed on the surface as necessary. An adhesive layer is formed, and the surface of the adhesive layer is polished and planarized. The substrate to be polished is bonded to the second silicon wafer (support substrate) 10 from the flattened surface and annealed to improve the adhesive strength. When the surface of the substrate to be polished is ground and thinned to a certain extent, it is thinned to a predetermined thickness, for example, about 100 nm by chemical mechanical polishing (CMP). Thereby, the SOI semiconductor layer 12 is formed. A stopper 17 made of a material having a high etching selectivity with respect to the element isolation insulating material is formed on the surface of the SOI semiconductor layer 12. As the film material of the stopper, when the element isolation insulating material is silicon dioxide, for example, silicon nitride can be selected. FIG. 5 is a cross-sectional view after the stopper is formed. Note that the SOI substrate may be formed by a so-called SIMOX method.

[0040] A resist pattern is formed on the stopper film 17 using a photomask of an element isolation pattern whose design has been partially changed, and the stopper 17 and the SOI semiconductor layer 12 therebelow are etched by RIE or the like using this as a mask. As a result, as shown in FIG. 6, the SOI semiconductor layer 12 is divided by the trench, and an active layer having a predetermined pattern is formed.

[0041] As shown in FIG. 7, a film 4a of element isolation insulating material is deposited so as to cover the active layer and completely fill the trench.

[0042] Next, the insulating film 4a is polished and flattened. Before that, a resist R1 having a pattern opening above each active layer is formed on the insulating film 4a as shown in FIG. The resist R1 is partially opened at portions other than the active layer in order to form a substrate contact region. The photomask used for the pattern formation of the resist R1 is prepared in advance using pattern data obtained by partially correcting an existing bulk type pattern. Etching is performed using the resist R1 as a mask to pattern the insulating film 4a. In the etching at this time, the surface of the active layer is protected by the presence of the stopper 17. This etching is performed until the buried insulating film portion under the substrate contact region is further etched and the semiconductor substrate 10 is exposed.

[0043] After removing the resist R1, the surface of the insulating film 4a is planarized by CMP or the like. If the stopper 17 is formed of a material having high hardness, the surface of the active layer is protected by the stopper 17 even in this CMP, and the end point of the CMP can be easily detected. As a result, the insulating film 4a is separated at a necessary portion, and as a result, the element isolation insulating layer 4 is formed.

[0044] The stopper 17 is removed by chemical treatment. Before or after removing the stopper, N-type impurity ions and P-type impurity ions are divided into the active layer to form the N-type active layers 21 and 15 on the PMOS side, and the P-type active layer 31 is formed on the NMOS side. To do. Further, if necessary, the threshold value is adjusted by introducing a P-type or N-type impurity into the surface of the active layer. Thereafter, a gate insulating film (not shown) made of silicon dioxide or the like and a polycrystalline silicon film are sequentially formed and patterned to form the gate electrode 5. Since the polycrystalline silicon film at this time has not yet been doped with impurities, its conductivity is low. Further, since the gate oxide film is formed by thermally oxidizing the surface of the active layer, it is hardly formed between the gate electrode 5 on the element isolation insulating layer 4 as shown in FIG.

[0045] As shown in FIG. 11, resist R2 opening in the NMOS formation region 3 is formed, and using this as a mask, low concentration ion implantation for LDD or ions for Extension S/D having a higher concentration than LDD in order to reduce parasitic resistance. Implantation is performed, and N-type impurities are introduced into the exposed surface portion of the active layer. Thereby, pocket ion implantation is performed as necessary. In this ion implantation, for example, the total dose is $1 \times 10^{14} / \text{cm}^2$, the energy is 1 keV, and phosphorus ions P or BF₂ ions are implanted at an implantation angle of 15°. Further, ion implantation is performed by dividing the wafer into eight directions from eight directions. Although not particularly illustrated, a 10 nm TEOS film, a silicon nitride film, etc. are CVD-etched and etched back to form sidewall spacers. Using this

sidewall spacer as a mask, an N-type impurity (for example, arsenic As) is ion-implanted at a relatively high dose of about $3 \times 10^{15} / \text{cm}^2$. As a result, the source impurity region S3 (and the drain impurity region D3) is formed on the surface portion in the P-type active layer 31, and at the same time, the substrate contact impurity region 14 is formed in the opening of the semiconductor substrate 10. Further, this NMOS gate electrode portion is made N-type conductive.

[0046] Although not particularly shown, a resist opening on the PMOS side is formed in the same manner, and ion implantation of P-type impurities for LDD or Extension S / D, formation of sidewall spacers, and ion implantation for S / D are performed. In this S / D ion implantation, for example, boron BF₂ is ion-implanted at a high dose of about $3 \times 10^{15} / \text{cm}^2$. Thereby, a source impurity region S2 (and a drain impurity region D2) is formed on the surface portion in the N-type active layer 21. In addition, the PMOS gate electrode portion is made P-type conductive.

[0047] Thereafter, an interlayer insulating film 13 is deposited on the entire surface, and this is opened, and a metal material such as tungsten W or doped polycrystalline silicon or the like is buried in the opening to flatten the surface, thereby various contacts SCn, SCp, VSC, VDC, etc. Further, various wirings 6 and 8 made of a metal material or the like are formed.

[0048] As a modification of this embodiment, the portion of the buried insulating film 11 opened in the trench may be removed by etching following the formation of the element isolation trench (FIG. 6). In this case, it is not necessary to etch the buried insulating film 11 when forming a substrate contact region (to be described later) (FIG. 8), so that the etching amount above the active layer can be made substantially the same, which is desirable. In this case, the etching stopper 17 can be omitted on condition that low damage etching is performed.

[0049] [Second Embodiment] In this embodiment, the substrate contact is taken from the back surface of the chip. FIG. 12 is a view when the SOI type semiconductor chip described in the first embodiment is fixed to a lead frame. An SOI type semiconductor chip is fixed to a die pad of a lead frame 40 made of a metal material having a high conductivity via a conductive adhesive layer 41 such as an Ag paste, and the back surface of the semiconductor substrate 10 is connected to the lead frame 40 with a low resistance. Conducted at. A lead frame 40 and a bonding pad 43 formed on the surface of the semiconductor chip and electrically connected to the GND line 8 are bonded by a wire 41. Such a die-bonded lead frame is accommodated in a mold resin or other package. At this time, the lead is pulled out of the package, but the lead to which the ground potential VGND is applied is usually a part of the illustrated lead frame 40 having a die pad, so that the ground potential VGND is the lead frame 40, the wire 41, and the bonding. It is supplied to the element through the pad 43, the GND line 8, the source contact SCn, and the like. At the same time, the ground potential VGND is supplied to the semiconductor substrate 10 via the lead frame 40 and the conductive adhesive layer 41.

[0050] In the above embodiment, the substrate contact inside the chip is unnecessary, and as shown in the figure, the contact VCS is connected only to the active layer surrounded by the element isolation insulating layer 4 and reaches the semiconductor substrate 10. Absent. Therefore, in the manufacture of such a chip, there is no need to change the pattern, and there is an advantage that the photomask used for the bulk type manufacturing can be used as it is.

[0051] The manufacturing method and design method of an SOI type semiconductor device according to the present invention are used in a bulk type semiconductor device when the SOI semiconductor layer is floating and the substrate potential is fixed. It is possible to easily manufacture the SOI type semiconductor device by converting the layout pattern to the layout pattern of the SOI type semiconductor device with a minimum change and forming a photomask with the converted pattern. According to the SOI semiconductor device of the present invention, it is possible to make substrate contact by directly applying the element and wiring layout pattern used in the bulk type semiconductor device.

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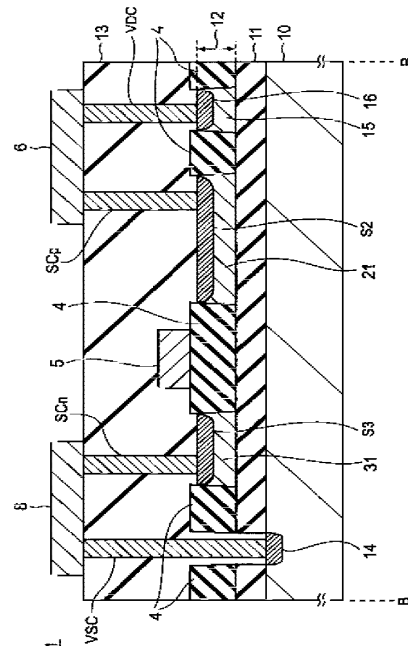
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(54) 【発明の名称】 S O I 型半導体装置の製造方法、設計方法および S O I 型半導体装置

(57) 【要約】

【課題】 バルク型半導体装置に用いられていたレイアウトパターンを必要最小限の変更で S O I 型半導体装置のレイアウトパターンに変換して用いる。

【解決手段】 S O I 型半導体装置の製造方法であって、バルク型半導体装置のウェルコンタクト領域に相当する箇所にも素子分離絶縁層4が形成されるように、バルク型半導体装置パターンを修正してフォトマスクを形成する工程と、このフォトマスクを用いて S O I 半導体層12内に素子分離絶縁層4、活性層15、31、32を形成する工程と、バルク型半導体装置のウェルコンタクト領域に相当する箇所の素子分離絶縁層4およびその下の埋込絶縁膜11をエッチングして基板コンタクト領域を形成する工程と、バルク型半導体装置のウェルコンタクトのフォトマスクを流用して、基板コンタクト領域内に基板コンタクト用のプラグVSCを形成する工程とを含む。



【特許請求の範囲】

【請求項1】半導体基板上に埋込絶縁膜を介在させて形成されたSOI半導体層に素子が集積されたSOI型半導体装置の製造方法であって、半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置のウェルコンタクト領域に相当する箇所にも素子分離絶縁層が形成されるように、バルク型半導体装置の素子分離絶縁層のパターンを修正してフォトマスクを形成する工程と、形成したフォトマスクを利用して上記SOI半導体層内に素子分離絶縁層を形成し、当該SOI半導体層を素子が形成される複数の活性層に分割する工程と、上記バルク型半導体装置のウェルコンタクト領域に相当する箇所の上記素子分離絶縁層およびその下の上記埋込絶縁膜をエッチングして基板コンタクト領域を形成する工程と、上記バルク型半導体装置のウェルコンタクトのフォトマスクを流用して、上記基板コンタクト領域内に基板コンタクト用のプラグを形成する工程とを含むSOI型半導体装置の製造方法。

【請求項2】上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程を更に有し、当該ソース・ドレイン不純物領域の形成と同時に、同じ不純物を上記基板コンタクト領域から注入し、基板コンタクト接続用の不純物領域を上記半導体基板に形成する請求項1に記載のSOI型半導体装置の製造方法。

【請求項3】上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程と、当該ソース・ドレイン不純物領域上に接続した電圧供給用のプラグを形成する工程と、当該電圧供給用のプラグ上に接続した電圧供給配線層を形成する工程とを更に有し、上記基板コンタクト用のプラグを形成する工程では、上記バルク型半導体装置のウェルコンタクトとソース・ドレイン不純物領域への電圧供給用のコンタクトとを同時に形成するためのフォトマスクを流用したコンタクト開口を行い、上記基板コンタクト用のプラグを上記電圧供給用のプラグと同時に形成する請求項1記載のSOI型半導体装置の製造方法。

【請求項4】上記素子分離絶縁層の形成工程が、素子分離絶縁層を形成する領域の周囲にマスク層を形成する工程と、マスク層を用いたエッチングにより上記SOI半導体層に上記埋込絶縁膜に達するトレンチを形成する工程と、トレンチ内を埋め込む素子分離絶縁膜を全面に堆積する工程と、トレンチ周囲の素子絶縁膜を一部除去する工程とを有し、

上記基板コンタクト領域の形成工程を、トレンチ周囲の素子分離絶縁膜の除去工程と同時に有する請求項1記載のSOI型半導体装置の製造方法。

【請求項5】上記トレンチ形成時のマスク層に、上記素子分離絶縁膜に対しエッチング選択比が高い材料からなるストッパ膜を含み、上記基板コンタクト領域の形成工程では、ストッパ膜により活性層の半導体表面を保護しながら、基板コンタクトを行う半導体基板の表面部分を露出させる請求項4記載のSOI型半導体装置の製造方法。

【請求項6】上記トレンチ形成後に、当該トレンチ形成に用いた上記マスク層をそのまま利用したエッチングにより、トレンチ内に表出した上記埋込絶縁膜部分を除去する工程を更に有する請求項4記載のSOI型半導体装置の製造方法。

【請求項7】半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置用のパターンを、基板上に埋込絶縁膜を介在させて形成されたSOI半導体層に素子が集積されたSOI型半導体装置用のパターンに変換する工程を含むSOI型半導体装置の設計方法であって、上記バルク型半導体装置がウェルコンタクトを有する場合に、上記変換工程では、当該ウェルコンタクトのパターンを、そのまま上記SOI型半導体装置の半導体基板に達する基板コンタクトのパターンに流用するSOI型半導体装置の設計方法。

【請求項8】上記バルク型およびSOI型の半導体装置は、導電型が異なる2種類のウェルまたはSOI半導体層からなる活性層のそれぞれに活性層導電型とは逆のチャネル導電型を有した絶縁ゲートトランジスタが形成された相補型絶縁ゲートトランジスタ回路を有し、上記バルク型半導体装置のP型ウェルがウェルコンタクトを有する場合に、上記変換工程では、当該P型ウェルのウェルコンタクトのパターンを、そのまま上記SOI型半導体装置の半導体基板に達し接地電圧を供給するための基板コンタクトのパターンに流用する請求項7記載のSOI型半導体装置の設計方法。

【請求項9】上記バルク型およびSOI型の半導体装置は、導電型が異なる2種類のウェルまたはSOI半導体層からなる活性層のそれぞれに活性層導電型とは逆のチャネル導電型を有した絶縁ゲートトランジスタが形成された相補型絶縁ゲートトランジスタ回路を有し、上記バルク型半導体装置のN型ウェルがウェルコンタクトを有する場合に、上記変換工程では、当該N型ウェルのウェルコンタクトのパターンを、そのまま上記SOI型半導体装置の半導体基板に達し電源電圧を供給するための基板コンタクトのパターンに流用する請求項7記載のSOI型半導体装置の設計方法。

【請求項10】上記変換工程が、上記バルク型半導体装置の素子分離絶縁層のパターン

を、そのウェルコンタクト領域が素子分離絶縁層となるように一部修正して、上記SOI型半導体装置の素子分離絶縁層のパターンを生成する工程を含む請求項7記載のSOI型半導体装置の設計方法。

【請求項11】上記バルク型半導体装置用のパターンが、素子分離絶縁層の形成時にトレンチ内に埋め込むように堆積された素子分離絶縁物をトレンチ周囲でエッチングにより一部除去するためのパターンを有し、上記変換工程が、上記バルク型半導体装置のトレンチ周囲の素子分離絶縁物を除去するためのパターンに、そのウェルコンタクト領域でもエッチングがされるように開口部のパターンを付加することにより、上記SOI型半導体装置の基板コンタクト接続用の不純物領域を上記半導体基板に形成するためのパターンを生成する工程を更に含む請求項10記載のSOI型半導体装置の設計方法。

【請求項12】半導体基板上に埋込絶縁膜を介在させて形成されたSOI半導体層に素子が集積されたチップがリードフレームのダイパッド上に、その半導体基板がダイパッドと導通した状態で固着されたSOI型半導体装置であって、SOI半導体層に形成する素子とその配線とを、同じ機能を有するバルク型半導体装置用のパターンを流用して形成することにより、バルク型半導体装置のウェルコンタクト領域に相当した箇所に、周囲を素子分離絶縁層に囲まれた島状のSOI半導体層部分を有し、当該島状のSOI半導体層部分が、上記素子に接地電圧 V_{GND} または電源電圧を供給する配線に対し接続されることにより、当該配線、ボンディングパッド、ワイヤを介して上記ダイパッドと電気的に接続されたSOI型半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体基板に対し埋込絶縁膜を介在させて形成されたSOI半導体層を有したSOI型半導体装置の製造方法、設計方法およびSOI型半導体装置に関する。

【0002】

【従来の技術】SOI (Silicon On Insulator) 構造によって基板との、あるいは素子間同士の完全分離が容易となり各種寄生容量が低下するほか、ソフトウェアやCMOSトランジスタ回路に特有なラッチアップの抑制が可能になる。このため、いわゆるSOI型のCMOS・LSIの高速化、低電圧化および信頼性の向上に、SOI分離技術が果たす役割がますます重要になってきている。

【0003】これに対し、現在でも多くのCMOS・LSIでは、半導体基板(半導体バルク)にP型およびN型のウェルを形成し、P型ウェルにN型チャネルのNM

OSトランジスタを形成し、N型ウェルにP型チャネルのPMOSトランジスタを形成した、いわゆるバルク型半導体装置となっている。

【0004】

【発明が解決しようとする課題】ところが、SOI型半導体装置を設計する場合、同じ機能を有したバルク型半導体装置とは異なった基板構造を有しているため、既に設計済みのバルク型半導体装置のレイアウトパターンをそのまま適用することができない。したがって、多くの場合、SOI型半導体装置用として新たにパターン設計をやり直す必要があった。これは、バルク半導体装置ではウェル電位を固定する電極が必要であり、その一方、SOI型半導体装置ではSOI半導体層をフローティングにして用いる場合、電位を固定する場合、あるいは半導体基板電位を固定する場合など、様々な電位固定方法が存在することが主な理由の一つであった。

【0005】本発明の第1の目的は、たとえばSOI半導体層をフローティングとし基板電位を固定して使用するような場合に好適で、バルク型半導体装置に用いられていたレイアウトパターンを最小限の変更でSOI型半導体装置のレイアウトパターンに変換する設計方法と、その方法を用いてフォトマスクを形成する工程を含むSOI型半導体装置の製造方法とを提供することにある。本発明の第2の目的は、バルク型半導体装置に用いられていた素子および配線のレイアウトパターンをそのまま適用しても基板コンタクトが可能な構造のSOI型半導体装置を提供することにある。

【0006】

【課題を解決するための手段】本発明の第1の観点にかかるSOI型半導体装置の製造方法は、上記第1の目的を達成するためのものであり、半導体基板上に埋込絶縁膜を介在させて形成されたSOI半導体層に素子が集積されたSOI型半導体装置の製造方法であって、半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置のウェルコンタクト領域に相当する箇所にも素子分離絶縁層が形成されるように、バルク型半導体装置の素子分離絶縁層のパターンを修正してフォトマスクを形成する工程と、形成したフォトマスクを利用して上記SOI半導体層内に素子分離絶縁層を形成し、当該SOI半導体層を素子が形成される複数の活性層に分割する工程と、上記バルク型半導体装置のウェルコンタクト領域に相当する箇所の上記素子分離絶縁層およびその下の上記埋込絶縁膜をエッチングして基板コンタクト領域を形成する工程と、上記バルク型半導体装置のウェルコンタクトのフォトマスクを流用して、上記基板コンタクト領域内に基板コンタクト用のプラグを形成する工程とを含む。

【0007】好適に、上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程を更に有し、当該ソース・ドレ

イン不純物領域の形成と同時に、同じ不純物を上記基板コンタクト領域から注入し、基板コンタクト接続用の不純物領域を上記半導体基板に形成する。あるいは、好適に、上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程と、当該ソース・ドレイン不純物領域上に接続した電圧供給用のプラグを形成する工程と、当該電圧供給用のプラグ上に接続した電圧供給配線層を形成する工程とを更に有し、上記基板コンタクト用のプラグを形成する工程では、上記バルク型半導体装置のウェルコンタクトとソース・ドレイン不純物領域への電圧供給用のコンタクトとを同時に形成するためのフォトマスクを流用したコンタクト開口を行い、上記基板コンタクト用のプラグを上記電圧供給用のプラグと同時に形成する。

【0008】好適に、上記素子分離絶縁層の形成工程が、素子分離絶縁層を形成する領域の周囲にマスク層を形成する工程と、マスク層を用いたエッチングにより上記SOI半導体層に上記埋込絶縁膜に達するトレンチを形成する工程と、トレンチ内を埋め込む素子分離絶縁膜を全面に堆積する工程と、トレンチ周囲の素子絶縁膜を一部除去する工程とを有し、上記基板コンタクト領域の形成工程を、トレンチ周囲の素子分離絶縁膜の除去工程と同時に進行。その場合、上記トレンチ形成時のマスク層に、上記素子分離絶縁膜に対しエッチング選択比が高い材料からなるストッパ膜を含み、上記基板コンタクト領域の形成工程では、ストッパ膜により活性層の半導体表面を保護しながら、基板コンタクトを行う半導体基板の表面部分を露出させるとよい。あるいは、上記トレンチ形成後に、当該トレンチ形成に用いた上記マスク層をそのまま利用したエッチングにより、トレンチ内に表出した上記埋込絶縁膜部分を除去する工程を更に有していてもよい。

【0009】本発明の第2の観点にかかるSOI型半導体装置の設計方法は、前記した第1の目的を達成するためのものであり、半導体基板上に形成されたウェルに素子が集積されたバルク型半導体装置用のパターンを、基板上に埋込絶縁膜を介在させて形成されたSOI半導体層に素子が集積されたSOI型半導体装置用のパターンに変換する工程を含むSOI型半導体装置の設計方法であって、上記バルク型半導体装置がウェルコンタクトを有する場合に、上記変換工程では、当該ウェルコンタクトのパターンを、そのまま上記SOI型半導体装置の半導体基板に達する基板コンタクトのパターンに流用する。

【0010】好適に、上記変換工程が、上記バルク型半導体装置の素子分離絶縁層のパターンを、そのウェルコンタクト領域が素子分離絶縁層となるように一部修正して、上記SOI型半導体装置の素子分離絶縁層のパターンを生成する工程を含む。その場合、更に好適に、上記バルク型半導体装置用のパターンが、素子分離絶縁層の形成時にトレンチ内に埋め込むように堆積された素子分

離絶縁物をトレンチ周囲でエッチングにより一部除去するためのパターンを有し、上記変換工程が、上記バルク型半導体装置のトレンチ周囲の素子分離絶縁物を除去するためのパターンに、そのウェルコンタクト領域でもエッチングがされるように開口部のパターンを付加することにより、上記SOI型半導体装置の基板コンタクト接続用の不純物領域を上記半導体基板に形成するためのパターンを生成する工程を更に含む。

【0011】このようなSOI型半導体装置の設計方法では、最低でも素子分離絶縁層のパターンを少しだけ修正するだけで、バルク型半導体装置用のレイアウトパターンをSOI型半導体装置用のレイアウトパターンに容易に変換できる。なお、素子分離絶縁膜をトレンチの周囲で除去する工程がない場合は、これとは別に、基板コンタクト専用のレイアウトパターンが必要となる。

【0012】また、前記したSOI型半導体装置の製造方法では、1工程（素子分離工程）でフォトマスクの修正が必要となり、必要に応じて、更に1工程（基板コンタクト領域の形成工程）で新たなフォトマスクが必要となる。このようにウェルコンタクトから基板コンタクトへの変更が極めて容易である。

【0013】本発明の第3の観点に係るSOI型半導体装置は、前記した第2の目的を達成するためのものであり、半導体基板上に埋込絶縁膜を介在させて形成されたSOI半導体層に素子が集積されたチップがリードフレームのダイパッド上に、その半導体基板がダイパッドと導通した状態で固着されたSOI型半導体装置であって、SOI半導体層に形成する素子とその配線とを、同じ機能を有するバルク型半導体装置用のパターンを流用して形成することにより、バルク型半導体装置のウェルコンタクト領域に相当した箇所に、周囲を素子分離絶縁層に囲まれた島状のSOI半導体層部分を有し、当該島状のSOI半導体層部分が、上記素子に接地電位または電源電圧を供給する配線に対し接続されることにより、当該配線、ボンディングパッド、ワイヤを介して上記ダイパッドと電気的に接続されている。

【0014】このSOI型半導体装置では、その素子および配線の形成時のレイアウトパターンをバルク型半導体装置と同じとしているため、バルク型ではウェルコンタクト領域に相当する箇所に孤立したSOI半導体層部分が必然的に形成されるが、この部分は基板コンタクトに使用されていない。基板コンタクトは、ボンディングパッド、ワイヤ、リードフレームのダイパッドを介して、半導体基板が、接地電位または電源電圧等をトランジスタに供給する配線に電気的に接続されていることにより達成されている。

【0015】

【発明の実施の形態】〔第1実施形態〕以下、本発明の第1の実施形態を、SOI形基板分離構造を有したCMOS・ロジックLSIを例に図面を参照しながら説明す

る。図1と図2は、CMOS・ロジックLSI内のゲート回路例を示すインバータとNANDゲートである。各図において、(A)は各ゲート回路記号を示し、(B)はSOI形基板分離構造を採用した本実施形態における各ゲート回路のパターン平面図である。

【0016】図1(B)に示すインバータ1のパターンは、それを構成するP型のMOSTランジスタが形成される領域(PMOS領域)2と、N型のMOSTランジスタが形成される領域(NMOS領域)3とに大別される。PMOS領域2には、N型の不純物が導入された半導体からなるN型活性層21が形成され、NMOS領域3には、P型の不純物が導入された半導体からなるP型活性層31が形成されている。これらの活性層21、31の周囲は素子分離絶縁層4に囲まれ、素子間の分離が達成されている。

【0017】これらの活性層21、31に対して、インバータの入力信号が印加されるゲート電極5が重ねられている。ゲート電極5は、たとえば不純物が添加されたドーパド多結晶珪素からなり、必要に応じて異なる導電型の不純物が打ち分けられている。一般的には、各MOSTランジスタを埋め込みチャンネル型として短チャンネル効果等の微細形状効果に対し強くするために、PMOS側のゲート電極部分にP型不純物が、NMOS側のゲート電極部分にN型不純物が添加されている。ゲート電極5をマスクにしてN型活性層21の表面にP型不純物が注入され、これによりソース不純物領域S2とドレイン不純物領域D2が形成されている。同様に、ゲート電極5をマスクにしてP型活性層31の表面にN型不純物が注入され、これによりソース不純物領域S3とドレイン不純物領域D3が形成されている。ゲート電極5の中央部にはインバータの入力端子を構成するゲートコンタクトGCが設けられている。

【0018】PMOSTランジスタのソース不純物領域S2は、その上のソースコンタクトSCpを介して、上層のメタル層からなる電源電圧Vddの供給線(VDD線)6に電気的に接続されている。PMOSTランジスタのドレイン不純物領域D2は、ドレインコンタクトDCp、上層のメタル層からなる内部接続線7、およびドレインコンタクトDCnを介して、NMOSTランジスタのドレイン不純物領域D3に電気的に接続されている。さらに、NMOSTランジスタのソース不純物領域S3は、その上のソースコンタクトSCnを介して、上層のメタル層からなる電源電圧GNDの供給線(GND線)8に接続されている。

【0019】図2(B)に示す本実施形態に係るNANDゲート10のパターンでは、N型活性層21に2つのPMOSTランジスタが並列に配置されている。2つのPMOSTランジスタの各ソース不純物領域S2a、S2bは、それぞれソースコンタクトSCa、SCbを介して上層のVDD線6に電気的に接続されている。2つ

のPMOSTランジスタの間の共通なドレイン不純物領域D2は、ドレインコンタクトDCpを介して上層のメタル層からなる出力線9に電気的に接続されている。

【0020】一方、P型活性層31に2つのNMOSTランジスタが並列に配置されている。この2つのNMOSTランジスタは電気的には直列接続され、前記した出力線9とGND線との間に挿入されている。つまり、一方のNMOSTランジスタのドレイン不純物領域D3がドレインコンタクトDCnを介して出力線9に接続され、他方のNMOSTランジスタのソース不純物領域S3がソースコンタクトSCnを介してGND線8に接続されている。2つのNMOSTランジスタ間の共通なソース・ドレイン領域SDは、他に接続されていないので、両ランジスタがオフのときはフローティング状態となる。

【0021】ゲートコンタクトGCaから第1の入力信号が印加されるゲート電極4aが図の左側に配置され、ゲートコンタクトGCbから第2の入力信号が印加されるゲート電極4bが図の左側に配置され、それぞれのゲート電極がN型活性層21とP型活性層31に交差している。

【0022】このように構成されたゲート回路は、SOI型の構成を有している。図3に、代表してインバータの断面構造を示す。この図は、図2(B)のB-B線に沿った概略断面図である。本実施形態ではN型シリコンウェーハなどからなる半導体基板10に、二酸化珪素などからなる埋込絶縁膜11が形成され、その上に形成されたSOI形基板分離構造のシリコン層(以下、SOI半導体層という)12に、前述したN型活性層21、P型活性層31および素子分離絶縁層4が形成されている。また、N型活性層21内の表面部分にソース不純物領域S2、S3(及びドレイン不純物領域D2、D3)が形成されている。

【0023】SOI半導体層12の表面全域には、たとえば二酸化珪素などからなる層間絶縁膜13が堆積されている。金属またはドーパド多結晶珪素などからなるプラグが層間絶縁膜13内に埋め込まれ、これにより前記したソースコンタクトSCp、SCnが形成されている。ソースコンタクトSCpはPMOS側のソース不純物領域S2上に接続し、ソースコンタクトSCnはNMOS側のソース不純物領域S3上に接続している。層間絶縁膜13上に、ソースコンタクトSCpに接続した前記VCC線6と、ソースコンタクトSCnに接続したGND線8が形成されている。これらの配線6、8は、アルミニウムなどのメタル層などからなる。

【0024】ところで、SOI型半導体装置では、半導体基板を一定の電圧で電位的に固定する基板コンタクトが必要となる場合がある。SOI型MOSTランジスタは、SOI半導体層を電位的に固定して使用する場合は、電位的にフローティング状態にして使用する場合は、

ある。いわゆるSOI半導体層の厚さを50nm程度まで薄くするとSOI半導体層が動作時に厚さ方向に完全に空乏化して完全空乏型の素子となるが、この場合、閾値の変動を抑えるには基板バイアスと同じ考えで半導体基板を電位的に固定しておくことが良く行われる。また、SOI半導体層が比較的厚く部分空乏型となる場合でも、閾値変動に対しクリティカルな回路部分のみSOI半導体層を電位固定して、その他のSOI半導体層を電位的にフローティングにして用いることが多い。SOI半導体層へのコンタクト数をできるだけ少なくして面積増大を抑制するためである。この場合でも閾値変動を極力抑制し、あるいはSOI半導体層と埋め込み絶縁膜との界面でのリークを低減する意図で、基板バイアスを印加することが良く行われる。

【0025】本実施形態はSOI半導体層の電位固定は行わないで基板バイアスを印加する場合に対応し、半導体基板10に接地電位 V_{GND} を付与することとしている。そこで、半導体基板10をGND線8と短絡する必要がある。具体的には、図3に示すように、素子分離絶縁層4とその下の埋込絶縁膜11の一部を開口して、その中に埋め込まれた層間絶縁膜13内に、上方のGND線8に達するプラグからなる基板コンタクトVSCを形成している。基板コンタクトVSCが設けられた半導体基板10内の表面部分に、基板バルクより高濃度なN型のコンタクト不純物領域14が形成されている。素子分離絶縁層4とその下の埋込絶縁膜11の一部を開口させているのは、コンタクト不純物領域14を形成するためである。この形成は、NMOSTランジスタのソース不純物領域S3（およびドレイン不純物領域D3）と同時に行うことが望ましく、その意味で、本実施形態の半導体基板10はN型となっている。

【0026】この部分を図1(A)の平面図で見ると、隣接する不図示のゲート回路と共有できるように横方向に配置されたGND線8の基幹からNMOS側に延びた枝の分岐の箇所に基板コンタクトVSCを設け、その周囲に一回り大きなコンタクト不純物領域14が形成されている。

【0027】一方、VDD線6においても、その基幹からPMOS側に延びた枝の分岐の箇所にコンタクトVDCが形成されている。ただし、このコンタクトVDCは、図3に示すように、周囲を素子分離絶縁層4に囲まれて電位的にフローティング状態となった活性層15にコンタクト不純物領域16を介して接続されている。これらのコンタクトVDC、活性層15およびコンタクト不純物領域16は、回路機能的には不要なものであり、後述するように、比較例のバルク型半導体装置とパターンを共用したことにより必然的にできてしまう部分である。

【0028】なお、回路の構成や閾値を全体的にシフトさせたい場合においては、基板バイアスを電源電圧Vd

dの印加により行うこともできる。その場合、この部分にも素子分離絶縁層4が形成されるようにパターンを変更して、コンタクトVDCが半導体基板10に達するようにする。そして、コンタクト不純物領域16は、PMOSTランジスタのP型不純物領域（ソース不純物領域S2およびドレイン不純物領域D2）と同時に形成することが望ましい。

【0029】つぎに、このようなSOI構造のインバータとの比較において、比較例のバルク構造のインバータを説明する。

【0030】図1(C)は、比較例として同じ機能を半導体バルクまたはウェルに形成したバルク型インバータのパターン平面図である。図4は、図1(C)のC-C線に沿った概略断面図である。このバルク型インバータ100の平面パターンは、上記したSOI型インバータの平面パターンと殆ど同じである。わずかに異なる点は、SOI型で基板コンタクトVSCが設けられた箇所に活性層（ウェル）が表出し、その表面部分にウェルコンタクト不純物領域101が形成されていることである。この図示例では、ウェルコンタクト不純物領域101のパターンは、SOI型における基板コンタクトVSCのパターンと同じとなっている。それ以外のパターンはバルク型と同じであり、以下、特に言及しない限り、図1(C)において図1(B)と同じ符号を付して、それらの説明を省略する。

【0031】図4の断面では、その基板構造がSOI型と異なる。任意の導電型のシリコンウェーハからなる半導体基板102に、PMOSTランジスタの活性層となるN型ウェル103と、NMOSTランジスタの活性層となるP型ウェル104とが形成されている。そして、これらのウェル内およびウェル周囲の表面部分が素子分離絶縁層4により分離されている。

【0032】N型ウェル103内の表面部分、Pウェル104内の表面部分に、SOI型と同じパターンにてソース不純物領域S2、S3（およびドレイン不純物領域D2、D3）が形成されている。これらランジスタの不純物領域とは素子分離絶縁層4により分離された状態で、Nウェル103とPウェル104のそれぞれにウェルコンタクト部が設けられている。Nウェル103のウェルコンタクト部は、ウェル内表面部に設けられた、より高濃度なN型のコンタクト不純物領域16と、コンタクト不純物領域16上面と上層のVDD線6とを接続するプラグからなるNウェルコンタクトNWCとからなる。NウェルコンタクトNWCは、SOI型におけるコンタクトVDCに該当し、層間絶縁膜13中に埋め込んで形成されている。

【0033】同様に、Pウェル4のウェルコンタクト部は、ウェル内表面部に設けられた、より高濃度なN型のコンタクト不純物領域101と、コンタクト不純物領域101上面と上層のGND線8とを接続するプラグから

なるPウェルコンタクトNWCとからなる。PウェルコンタクトPWCは、SOI型における基板コンタクトVSCの代わりに設けられ、層間絶縁膜13中に埋め込んで形成されている。

【0034】その他の構成、すなわちゲート電極4、ゲートコンタクトGC、ソースコンタクトSCP、SCn、ドレインコンタクトDCP、DCn、層間絶縁膜13、VDD線6およびGND線8は、前記したSOI型と同じパターン、材料からなる。

【0035】このようなパターンおよび構造の相違は、NANDゲート回路でも同じである。同一符号をもって、その説明を省略する。

【0036】このような構成のバルク型半導体装置の既存のパターンおよびレイアウトデータを用いて、同じ機能のSOI型半導体装置を新たに設計する場合、まず、素子分離絶縁膜4のパターンを一部修正する。具体的には、図示例のインバータの場合、たとえばNMOS側のPウェルコンタクトのために素子分離絶縁膜4のパターンの開口部をなくす。

【0037】また、基板コンタクト用に素子分離絶縁層4およびその下の埋込絶縁膜11を一部開口させるパターンが必要となる。このパターンは、後述するように素子分離絶縁層4の形成時に全面に堆積した絶縁膜を活性層上で選択的にエッチングするための工程が必要であるならば、その選択的エッチング時のパターンを修正することで対応できる。その場合、フォトマスクの追加はない。これに対し、そのような選択的エッチング工程がもともとない場合は、基板コンタクト用に新たなフォトマスクが1枚追加となる。

【0038】このように、パターン修正を2回行うか、1回のパターン修正と、新たな追加フォトマスク作製のための1枚のパターンレイヤの追加によって、バルク型からSOI型の変換が可能となる。しかも、これらのパターン修正や新規パターンの作成は、単純な矩形パターンを最低1個付加するだけよく簡単である。したがって、基板分離構造の変更にともなう経費を極力抑制できる利点が得られる。また、実効的な素子パターンに変更がないので、バルク型からSOI型に変更したことによる特性改善の効果を容易に見積もることができる。平面パターン形状に依存した素子特性パラメータに変化がないため、純粋に基板分離構造の変更による特性の向上がそのまま素子の電気的特性に反映されるためである。

【0039】最後に、このSOI型半導体装置の製造方法の実施形態を、インバータを例として説明する。図5～図11は、このインバータの製造途中の断面図である。まず、SOI型基板分離構造の基板（SOI基板）を既知の方法によって形成する。たとえば基板張り合わせ方では、SOI半導体層12となる第1のシリコンウェーハ（被研磨基板）の表面に埋込絶縁膜11を形成し、さらにその表面に必要な応じて、たとえば多結晶珪

素などからなる接着層を形成し、接着層の表面を研磨して平坦化する。被研磨基板を、その平坦化した面から第2のシリコンウェーハ（支持基板）10と張り合わせ、アニールして接着強度を向上させる。被研磨基板の裏面から研削して、ある程度まで薄くなった後化学的機械研磨（CMP）により所定の厚さ、たとえば100nm程度まで薄くする。これによりSOI半導体層12が形成される。SOI半導体層12の表面に、素子分離絶縁材料とのエッチング選択比が高い材料のストッパ17を形成する。ストッパの膜材料は、素子分離絶縁材料が二酸化珪素の場合、たとえば窒化珪素が選択できる。図5は、このストッパ形成後の断面図である。なお、SOI基板を、いわゆるSIMOX法により形成してもよい。

【0040】ストッパ膜17上に、一部設計変更した素子分離パターンのフォトマスクを用いてレジストパターンを形成し、これをマスクとしてストッパ17およびその下のSOI半導体層12をRIE等でエッチングする。これにより、図6に示すように、SOI半導体層12がトレンチにより分割され、所定パターンの活性層が形成される。

【0041】図7に示すように、活性層を覆って、かつトレンチ内を完全に埋め込むように素子分離絶縁材料の膜4aを堆積する。

【0042】つぎに、この絶縁膜4aを研磨して平坦化するのであるが、その前に、図8に示すように、各活性層の上方で開口するパターンのレジストR1を絶縁膜4a上に形成する。このレジストR1は、さらに基板コンタクト領域を形成するために一部、活性層以外の箇所でも開口している。このレジストR1のパターン形成に用いるフォトマスクは、既存のバルク型のパターンを一部修正したパターンデータを用いて予め作製される。レジストR1をマスクとしたエッチングを行って、絶縁膜4aをパターンニングする。このときのエッチングでは、ストッパ17の存在により活性層表面が保護される。また、このエッチングは、基板コンタクト領域ではさらにその下の埋込絶縁膜部分がエッチングされて半導体基板10が露出するまで行う。

【0043】レジストR1を除去後、絶縁膜4aの表面をCMPなどで平坦化する。ストッパ17を硬度が高い材料から形成しておくこと、このCMPにおいてもストッパ17により活性層表面が保護され、またCMPの終点検出も容易である。これにより絶縁膜4aが必要箇所分離され、その結果、素子分離絶縁層4が形成される。

【0044】ストッパ17を薬液処理で除去する。このストッパの除去前または後で、活性層にN型不純物イオンとP型不純物イオンを打ち分けて、PMOS側でN型活性層21、15を形成し、NMOS側でP型活性層31を形成する。また、必要に応じて、P型またはN型の不純物を活性層表面部に導入して閾値の調整を行う。その後、二酸化珪素などからなるゲート絶縁膜（不図示）

および多結晶珪素膜を順次形成して、これをパターンニングしてゲート電極5を形成する。このときの多結晶珪素膜にはまだ不純物は添加されていないので導電率は低い。また、ゲート酸化膜は活性層表面を熱酸化して形成するので、図10のように素子分離絶縁層4上のゲート電極5との間には殆ど形成されない。

【0045】図11に示すように、NMOS形成領域3で開口するレジストR2を形成し、これをマスクとして、LDD用の低濃度イオン注入、あるいは寄生抵抗下げるためLDDより高濃度なExtentio S/D用のイオン注入を行い、N型不純物を表出した活性層表面部分に導入する。これにより、また、必要に応じて、ポケットイオン注入を行う。このイオン注入は、たとえばトータルのドーズを $1 \times 10^{14} / \text{cm}^2$ 、エネルギーを1 keVで、燐イオンPまたは BF_2 イオンを注入角度 15° で注入する。また、ウェーハの8方向から8分割りにてイオン注入する。特に図示しないが、10 nmのTEOS膜、窒化珪素膜などをCVDし、これをエッチバックしてサイドウォールスペーサを形成する。このサイドウォールスペーサをマスクにして、 $3 \times 10^{15} / \text{cm}^2$ 程度の比較的高いドーズでN型不純物（たとえば、砒素As）をイオン注入する。これにより、P型活性層31内の表面部にソース不純物領域S3（およびドレイン不純物領域D3）が形成され、これと同時に半導体基板10の開口部分に基板コンタクト不純物領域14が形成される。また、このNMOSゲート電極部分がN型に導電化される。

【0046】特に図示しないが、同様にしてPMOS側で開口するレジストを形成してLDDまたはExtentio S/D用のP型不純物のイオン注入、サイドウォールスペーサの形成、S/D用のイオン注入を行う。このS/D用のイオン注入では、たとえば、ホウ素 BF_2 を $3 \times 10^{15} / \text{cm}^2$ 程度の高ドーズでイオン注入する。これにより、N型活性層21内の表面部にソース不純物領域S2（およびドレイン不純物領域D2）が形成される。また、このPMOSゲート電極部分がP型に導電化される。

【0047】その後は、層間絶縁膜13を全面に堆積し、これを開口して、開口部にタングステンW等の金属材料またはドーパド多結晶珪素などを埋め込んで表面を平坦化することにより、各種コンタクトScn, SCp, VSC, VDC等を形成する。また、金属材料などからなる各種配線6, 8等を形成する。

【0048】本実施形態の変形例として、素子分離用のトレンチ形成時（図6）に続けて、トレンチ内に開口した埋込絶縁膜11の部分をエッチングにより除去してもよい。こうすると、後述する基板コンタクト領域の形成時（図8）に埋込絶縁膜11をエッチングしないですむので、活性層上方とのエッチング量をほぼ同じとすることができ、望ましい。この場合、低ダメージエッチング

を行うことを条件にエッチングストップ17の省略も可能である。

【0049】〔第2実施形態〕この実施形態では、基板コンタクトをチップ裏面からとる。図12は、第1実施形態で説明したSOI型半導体チップをリードフレームに固着させたときの図である。導電率が高い金属材料からなるリードフレーム40のダイパッドに、SOI型半導体チップが、たとえばAgペーストなどの導電性接着層41を介して固着され、半導体基板10の裏面が、リードフレーム40と低抵抗で導通している。また、リードフレーム40と、半導体チップ表面に形成されGND線8と電気的に導通したボンディングパッド43とがワイヤ41によりボンディングされている。このようなダイボンド後のリードフレームはモールド樹脂、その他のパッケージ内に收容される。このときパッケージ外部にリードが引き出されるが、接地電位 V_{GND} が印加されるリードは、通常、ダイパッドを有する図示のリードフレーム40の一部であるので、接地電位 V_{GND} がリードフレーム40、ワイヤ41、ボンディングパッド43、GND線8、ソースコンタクトScn等を介して素子に供給される。それと同時に、接地電位 V_{GND} がリードフレーム40、導電性接着層41を介して半導体基板10に供給される。

【0050】上記形態では、チップ内部の基板コンタクトは不要であり、図示のように、コンタクトVCSは周囲を素子分離絶縁層4に囲まれた活性層に接続されるのみで、半導体基板10にまでは達していない。したがって、このようなチップの製造ではパターンの変更は一切不要となり、バルク型の製造に用いていたフォトマスクをそのまま流用できるという利点がある。

【0051】

【発明の効果】本発明に係るSOI型半導体装置の製造方法および設計方法によれば、SOI半導体層をフローティングとし基板電位を固定して使用するような場合に、バルク型半導体装置に用いられていたレイアウトパターンを最小限の変更でSOI型半導体装置のレイアウトパターンに変換し、この変換後のパターンによりフォトマスクを形成してSOI型半導体装置を容易に製造することができる。本発明に係るSOI型半導体装置によれば、バルク型半導体装置に用いられていた素子および配線のレイアウトパターンをそのまま適用して基板コンタクトが可能となる。

【図面の簡単な説明】

【図1】（A）は、本発明の第1実施形態に係るCMOS・ロジックLSI内のSOI型インバータの回路記号、（B）はそのパターン平面図である。（C）は、比較例としてのバルク型インバータのパターン平面図である。

【図2】（A）は、本発明の第1実施形態に係るCMOS・ロジックLSI内のSOI型NANDゲートの回路

記号、(B)はそのパターン平面図である。(C)は、比較例としてのバルク型NANDゲートのパターン平面図である。

【図3】本発明の第1の実施形態に係るSOI型インバータにおいて、図1(B)のB-B線に沿った概略断面図である。

【図4】比較例のSOI型インバータにおいて、図1(C)のC-C線に沿った概略断面図である。

【図5】本発明の第1の実施形態に係るSOI型インバータの製造において、エッチングストップとなる膜の形成後の断面図である。

【図6】本発明の第1の実施形態に係るSOI型インバータの製造において、トレンチ形成後の断面図である。

【図7】本発明の第1の実施形態に係るSOI型インバータの製造において、素子分離絶縁膜の堆積後の断面図である。

【図8】本発明の第1の実施形態に係るSOI型インバータの製造において、基板コンタクト領域の開口後の断面図である。

【図9】本発明の第1の実施形態に係るSOI型インバータの製造において、素子分離絶縁層の形成後の断面図である。

【図10】本発明の第1の実施形態に係るSOI型インバータの製造において、エッチングストップとなる膜の

形成後の断面図である。

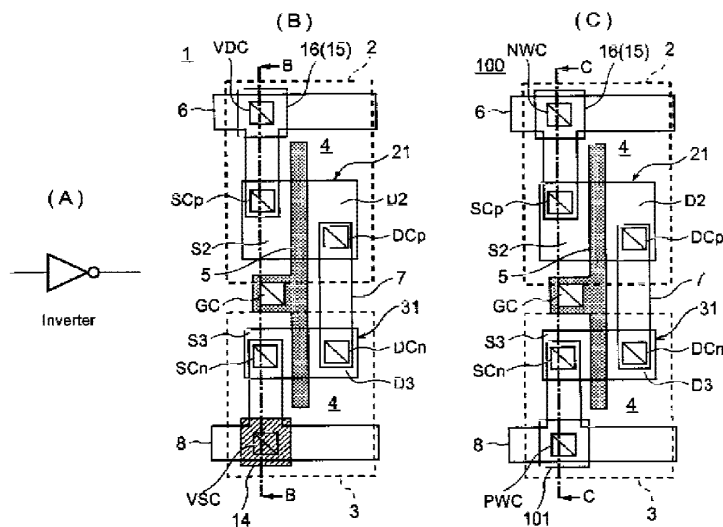
【図11】本発明の第1の実施形態に係るSOI型インバータの製造において、基板コンタクト不純物領域形成のためのイオン注入時の断面図である。

【図12】本発明の第2の実施形態に係るSOI型半導体装置の要部構成を示す図である。

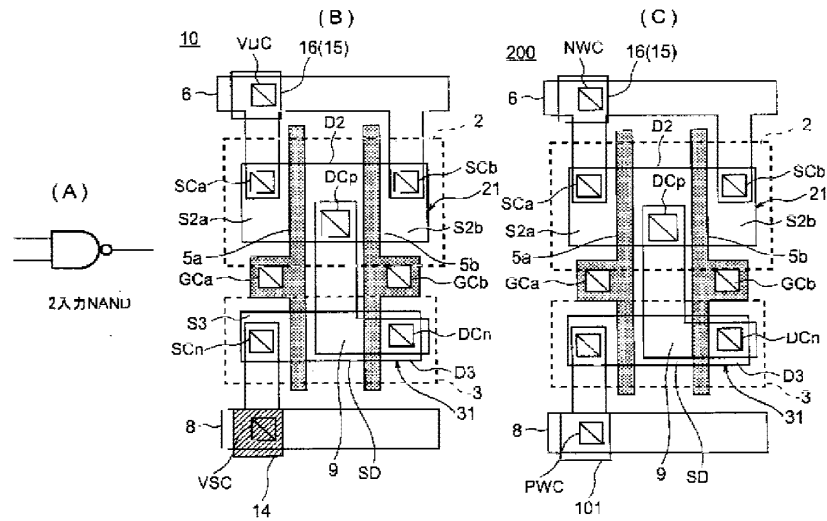
【符号の説明】

1…SOI型インバータ、2…PMOS形成領域、3…NMOS形成領域、4…素子分離絶縁層、4a…素子分離絶縁膜、5、5a、5b…ゲート電極、6…VDD線、7…内部接続線、8…GND線、9…出力線、10、102…半導体基板、11…埋込絶縁膜、12…SOI半導体層、13…層間絶縁膜、14…基板コンタクト不純物領域、15…活性層、16、101…コンタクト不純物領域、17…エッチングストップ、21…N型活性層、31…P型活性層、40…リードフレーム、41…導電性接着層、42…ワイヤ、43…ボンディングパッド、103…N型ウェル、104…P型ウェル、SCn、SCp…ソースコンタクト、DCn、DCp…ドレインコンタクト、GC、GCa、GCb…ゲートコンタクト、VSC、VDC…コンタクト、S2、S2a、S2b、S3…ソース不純物領域、D2、D3…ドレイン不純物領域、SD…ソース・ドレイン不純物領域、PWC、NWC…ウェルコンタクト

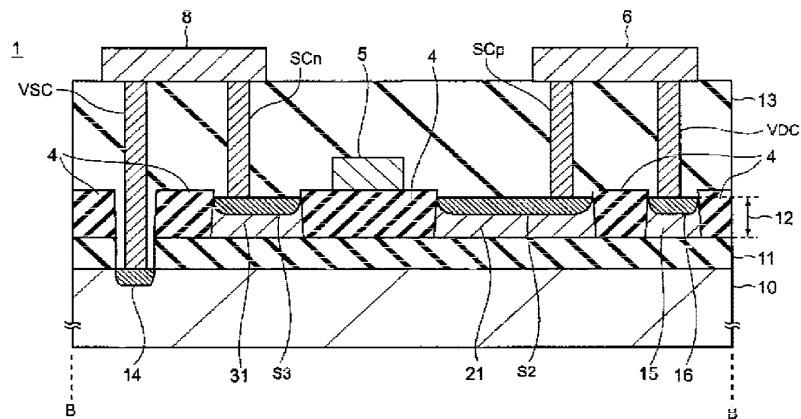
【図1】



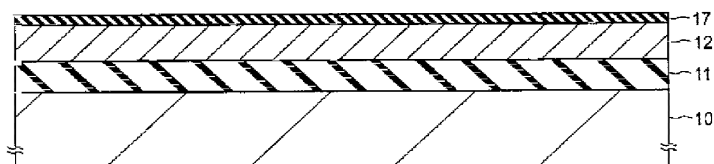
【図2】



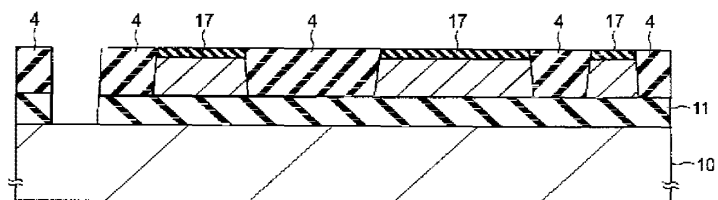
【図3】



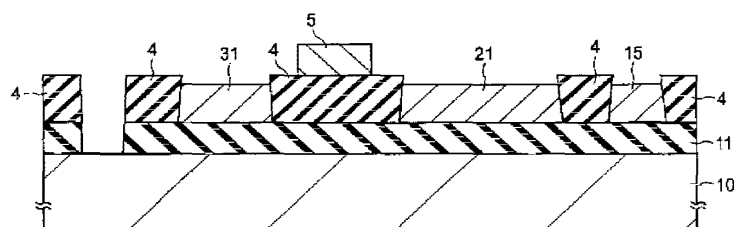
【図5】



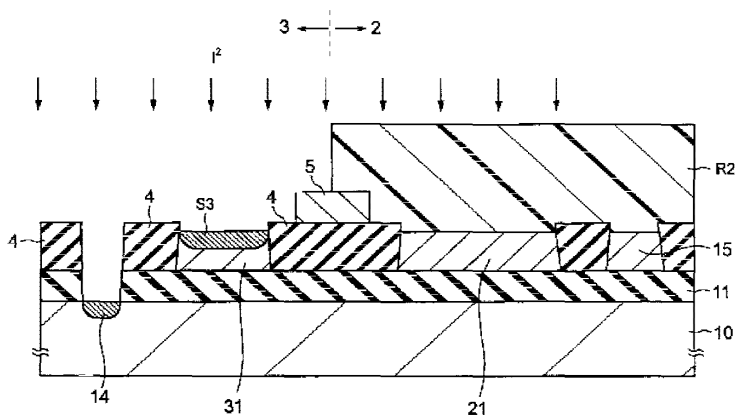
【例9】



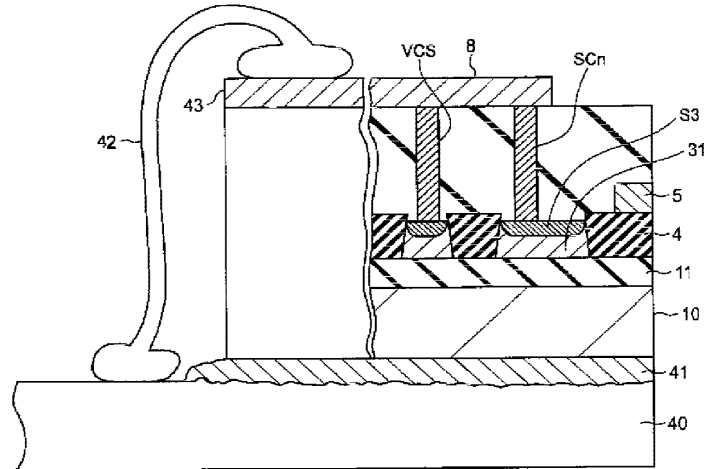
【図 10】



【例 1 1】



【図12】



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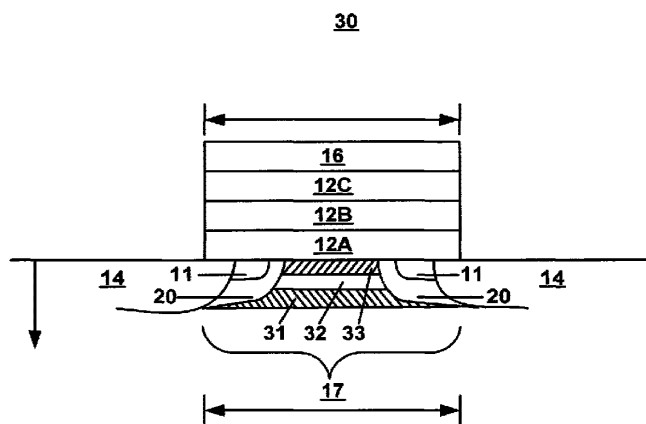
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(57) Abstract: A memory semiconductor cell (30) comprises a gate region (16), a source region (14) and a drain region (14). A channel region (17) is formed between the source region (14) and the drain region (14). The channel region (17) comprises a first channel portion (33) with a first concentration of doping material, the first channel portion (33) disposed adjacent to an edge of the channel region (17) closest to and substantially parallel to the gate region (16). The channel region (17) further comprises a second channel portion (31) with a second concentration of doping material, the second channel portion (31) disposed substantially parallel to the first channel portion (33) and a third channel portion (32), disposed between the first channel portion (33) and the second channel portion (31), with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration. The memory cell may be one of two general types of non-volatile memory, a floating gate cell or a nitride read only memory (NROM), whereby layer (12B) in a floating gate or a nitride layer respectively.

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RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT**TECHNICAL FIELD**

Embodiments of the present invention relate to design of sub-micron metal oxide semiconductors. More particularly, embodiments of the present invention provide retrograde channel doping to improve the short channel effect.

BACKGROUND ART

Figure 1 shows a memory cell 10 as has been well known in the conventional art. Regions 14 are the drain and/or source regions for memory cell 10. They may be used as source and/or drain interchangeably. Control gate 16 is used to control the operation of memory cell 10. A channel region 17 is formed between source/drain regions 14. Feature size 18 is the nominal size of the smallest feature that can be created by a particular semiconductor process. In memory cells of this type, the gate 16 width and channel 17 length typically correspond approximately to feature size 18. Memory cell 10 may also have a source/drain extension 11 structure. Source/drain extension 11 is a shallow diffusion that connects the channel 17 with the deeper source/drain 14, typically intended to prevent degradation of drive current.

Memory cell 10 may be one of two general types of non-volatile memory, a "floating gate" cell or a nitride read only memory (NROM) cell. In a floating gate cell, layer 12B of the gate stack is typically conductive polysilicon. Layers 12A and 12C are insulating materials which isolate or "float" gate layer 12B, which is usually referred to as a floating gate. Floating gate 12B is the storage element of memory cell 10.

Silicon nitride based flash memory has many advantages as compared to its floating gate and tunneling oxide based counterparts. Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) is potentially very dense in terms of number of cells per unit area that can be used and it requires fewer process steps as compared to floating gate memory. Moreover, it can be easily integrated with standard SRAM process technology. A further advantage of using SONOS devices is their suitability for applications requiring large temperature variations and radiation hardening. The SONOS stack is a gate dielectric stack and consists of a single layer of polysilicon, a triple stack ONO (Oxide-Nitride-Oxide) gate dielectric layer and a MOS channel 17. The ONO structure may consist of a tunnel oxide 12A, a nitride memory storage layer 12B and a blocking oxide layer 12C.

Memory device manufacturers are continually challenged to provide ever greater amounts of memory at ever lower costs. Recently, Advanced Micro Devices, Incorporated of California has introduced MIRROR BIT™ nitride-based flash ROM that stores multiple bits per memory cell 10 physically separated in nitride layer 12B. Such storage of multiple bits per cell increases the storage density of the memory device, thereby reducing the cost per bit of storage.

Another primary approach employed to achieve lower memory costs is the industry-wide on-going reduction in semiconductor feature size. By making features, such as signal lines and transistors smaller, more memory devices may be placed in a given die area, resulting in lower production costs.

However, as feature size decreases to, for example, about 0.3 microns and smaller, the channel length also decreases. As channel length grows shorter, threshold voltage begins to decrease and leakage current increases. These effects are commonly referred to in the semiconductor arts as the "short channel effect." An increase in leakage current is particularly onerous in flash memory devices as flash has found wide acceptance in very low power applications, for example mobile phones, due to the ability of flash to retain information without applied power. Increases in leakage current may have a significant deleterious effect on total power consumption

of the flash device and the product using the flash device. Consequently, much research and development effort has gone into mitigating the short channel effect.

Prior art approaches to improve leakage current and reduce the short channel effect include, for example, "halo" doping and retrograde wells. Halo doping 20 creates a steep dopant profile at the edges of the source/drain regions, as shown in Figure 1. A conventional retrograde well has a non-uniform doping concentration that increases, for example, linearly with depth 22 in the channel region 17. The doping of a conventional retrograde well generally follows a continuous, monotonically increasing profile with no abrupt changes. Conventional retrograde wells are typically created by using a slow diffusing dopant species such as arsenic or antimony for PMOS devices and indium for NMOS devices. Both halo doping and retrograde well profiles serve to inhibit the flow of charge carriers, raising the threshold voltage and reducing leakage current for the device.

However, both halo doping and conventional retrograde wells, alone and in combination, are found to be lacking. Such prior art approaches simply do not reduce leakage current to commercially acceptable levels for flash memory at modern process feature sizes, for example, 0.17 microns and smaller.

Semiconductor processing equipment is extremely expensive. Fundamental semiconductor processing steps, e.g., doping, typically require long periods of development and extensive qualification testing. Any solution to the short channel effect should be compatible with existing semiconductor processes and equipment without the need for revamping well established tools and techniques.

Thus a need exists to prevent short channel effects in memory cells. A further need exists for preventing short channel effects in a manner that is compatible and complimentary with conventional approaches to minimize short channel effects. A still further need exists for the above mentioned needs to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

DISCLOSURE OF THE INVENTION

Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

A memory semiconductor cell comprises a gate region, a source region and a drain region. A channel region is formed between the source region and the drain region. The channel region comprises a first channel portion with a first concentration of doping material, the first channel portion disposed adjacent to an edge of the channel region closest to and substantially parallel to the gate region. The channel region further comprises a second channel portion with a second concentration of doping material, the second portion disposed substantially parallel to the first channel portion and a third channel portion, disposed between the first channel portion and the second channel portion, with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a memory cell as has been well known in the conventional art.

Figure 2 illustrates a memory cell with a retrograde channel, according to an embodiment of the present invention.

Figure 3 illustrates an exemplary profile of doping concentration in a channel region versus channel depth, according to an embodiment of the present invention.

Figures 4A, 4B and 4C illustrate a charge carrier flow through a channel region of a memory cell, according to an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following detailed description of the present invention, retrograde channel doping to improve short channel effect, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT

Embodiments of the present invention are described in the context of design and operation of flash memory devices. However, it is appreciated that embodiments of the present invention may be utilized in other areas of electronic design and operation.

Figure 2 illustrates a memory cell 30 with a novel retrograde channel, according to an embodiment of the present invention. The channel region comprises three portions, 31, 32 and 33. Channel portion 33 is closest to gate 16 and substantially parallel to the long axis of gate 16. Channel portion 32 is substantially parallel to channel portion 33 and at a greater depth into the substrate material than channel portion 32. Channel portion 31 is substantially parallel to channel portion 32 and at a still greater depth into the substrate material. Channel portion 32 is disposed between channel portions 31 and 33. It is appreciated that memory cell 30 is shown with source/drain extensions 11 and halo implant regions 20. Embodiments of the present invention are well suited to memory cells with or without these features. If one or both were absent, channel portions 31, 32 and 33 would extend horizontally to the halo implant or the source drain extension or the source/drain.

By well known semiconductor processing techniques, for example implantation and diffusion, channel portion 33 may be constructed and given a particular concentration of doping material. Likewise, channel portion 31 may be constructed and given a particular concentration of doping material. In general, no specific operations are performed to construct channel portion 32, rather channel portion 32 is a result of constructing portions 31 and 33 with no overlap. The bottom of channel portion 31 may be, for example, 0.1 μm from the top edge of the substrate.

According to an embodiment of the present invention, the doping concentration in both channel portion 31 and channel portion 33 is higher than the doping concentration of channel portion 32. Graph 40 of Figure 3 illustrates an exemplary profile 41 of doping concentration in a channel region versus channel depth. Channel portion 33 may have a doping concentration as depicted by profile 41 in region 33A. Channel portion 32 may have a doping concentration as depicted by profile 41 in region 32A. Channel portion 31 may have a doping concentration as depicted by profile 41 in region 31A.

It is to be appreciated that, in contrast to conventional retrograde wells, the doping profile of this novel well is neither monotonic nor necessarily continuous, according to an embodiment of the present invention. There may be relatively abrupt (as allowed by semiconductor physics) changes in doping profile at the boundaries between channel portions, for example between channel portions 31 and 32, and between channel portions 32 and 33.

In channel portions 31 and 33 charge carrier migration is hindered due to the to relatively high concentration of doping material(s). Consequently, the effective channel region is reduced to approximately

channel portion 32. For example, channel portion 32 may form a "tunnel" (not to be confused with quantum effect tunneling) between channel portions 31 and 33. As a beneficial result of the reduced effective channel, threshold voltage is increased and leakage current is decreased, reducing or eliminating the short channel effect. It is to be appreciated that the depths, thickness and doping concentrations of the respective channel portions will vary according to a wide range of variables including, for example, source/drain thickness, channel length, operating voltage, doping materials and whether the device operates as a P channel or an N channel.

Channel portion 31 may be initially formed by using a slow diffusing dopant species, for example, arsenic or antimony for PMOS devices. Such a diffusion process may enable high concentrations of doping material to reach the channel depths required. Channel portion 33 may be formed by using faster diffusing dopants, e.g., boron. A shorter diffusion may produce a high concentration of doping material at relatively shallow depths in the channel region.

Figures 4A, 4B and 4C further illustrate a charge carrier flow through a channel region of memory cell 30, according to an embodiment of the present invention. In Figure 4A, charge carriers, for example, electrons 403 attempt to flow from source/drain region 401 to source/drain region 402. Electrons are impeded from flowing into channel portion 33 due to a high concentration of doping material. Likewise, electrons 405 are impeded from flowing into channel portion 31 due to a high concentration of doping material. In contrast, electrons 404 are able to overcome a relatively small energy barrier and flow into channel portion 32.

As shown in Figure 4B, electrons 403, otherwise disposed to travel horizontally (as depicted) into channel region 33, must change direction to travel around the "corner" of channel region 33 in order to enter channel region 32, wherein electrons are more able to flow. Such changes of direction require energy, resulting in a higher energy budget for electrons traversing a complex path, in contrast to electrons which may be able to travel in substantially a straight line. In addition, because region 401 is fully populated with charge carriers, e.g., electrons 404 and 405, additional energy is required to overcome the electrostatic repulsion of like charges in order to move the charge carriers closer together. As a beneficial result of the increased path length, the indirect nature of the path, as well as electrostatic repulsion, electrons 403 require more energy to travel from region 401 to 402 and consequently have a beneficially higher threshold voltage for embodiments of the present invention when compared to the prior art.

In a similar manner, electrons 405 must change direction and overcome electrostatic repulsion in order to travel into channel portion 32 from their original positions adjacent to channel portion 31. Consequently, electrons 405 have a higher threshold voltage than would otherwise be required.

Electrons 404, while disposed adjacent to channel portion 32, are also beneficially affected by embodiments of the present invention. Although electrons 404 are not obviously redirected to avoid channel portions of higher doping concentration, electrons 404 are affected by the localized increased concentration of charge carriers resulting in electrostatic forces acting upon electrons 404 in a similar manner to the electrostatic forces acting upon electrons 403 and 405.

Figure 4C shows a cumulative effect of the present retrograde channel on charge carrier flow, according to an embodiment of the present invention. Electrons in region 401 are inhibited from flowing in channel portions 33 and 31, favoring channel portion 32. However, due to the physically constrictive nature of channel portion 32 combined with electrostatic forces acting upon the like charge carriers, the electrons tend to "bunch up" at the interface between region 401 and channel portion 32. The net effect of "bunching up" is seen externally as a desirable increase in threshold voltage, and a corresponding decrease in leakage current.

It is to be appreciated that although a PMOS device has been illustrated herein, embodiments of the present invention are well suited to NMOS devices as well. The choices of materials, e.g., for dopants, for use with NMOS devices are well understood in the semiconductor arts.

5 This novel design and method to implement this design reduce and/or eliminate the short channel effect, allowing for decreased feature size and increased density of memory cells. These beneficial results allow for less expensive memory devices with lower power consumption, rendering a competitive advantage to the users practicing embodiments of the present invention.

10 Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

15 The preferred embodiment of the present invention retrograde channel doping to improve short channel effect is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.