

CLAIMS

What is claimed is:

1. A method of manufacturing a memory semiconductor cell (30) comprising:
forming a first channel portion (33) to produce a first concentration of doping material, said first
channel portion (33) disposed adjacent to an edge of a channel region closest to and substantially parallel
to a gate region (16) of said memory semiconductor cell;
forming a second channel portion (31) to produce a second concentration of doping material,
said second portion (31) disposed substantially parallel to said first channel portion (33); and
forming a third channel portion (32), disposed between said first channel portion (33) and said
second channel portion (31), comprising a third concentration of doping material, wherein said third
concentration is lower than said first concentration and lower than said second concentration.
2. The method as described in Claim 1 further comprising implanting a halo implant (20) disposed
adjacent to a source region or a drain region of said memory semiconductor cell (30).
3. The memory semiconductor cell (30) described in Claim 1 wherein a source region of said
memory semiconductor cell comprises a source extension region (11).
4. The method as described in Claim 1 further comprising forming said second channel portion
(31) prior to the formation of said first channel portion (33).
5. The method as described in Claim 1 wherein said memory semiconductor cell (30) is non-
volatile.
6. The method as described in Claim 5 wherein said memory semiconductor cell (30) comprises a
nitride layer as a storage element (12B).
7. The method as described in Claim 5 wherein said memory semiconductor cell comprises a
floating gate (12B) as a storage element.
8. A memory semiconductor cell (30) comprising:
a gate region (16), a source region (14) and a drain region (14);
a channel region (17) between said source region (14) and said drain region (14);
wherein said channel region (17) comprises:
a first channel portion (33) comprising a first concentration of doping material, said first
channel portion (33) disposed adjacent to an edge of said channel region (17) closest to and substantially
parallel to said gate region (16);
a second channel portion (31) comprising a second concentration of doping material, said
second portion (31) disposed substantially parallel to said first channel portion (33); and
a third channel portion (32), disposed between said first channel portion (33) and said second
channel portion (31), comprising a third concentration of doping material, wherein said third
concentration is lower than said first concentration and lower than said second concentration.
9. The memory semiconductor cell described in Claim 8 wherein said channel region (17) further
comprises a halo implant (20) disposed adjacent to said source region (14) or said drain region (14).
10. The memory semiconductor cell described in Claim 8 wherein said source region (17)
comprises a source extension region (11).

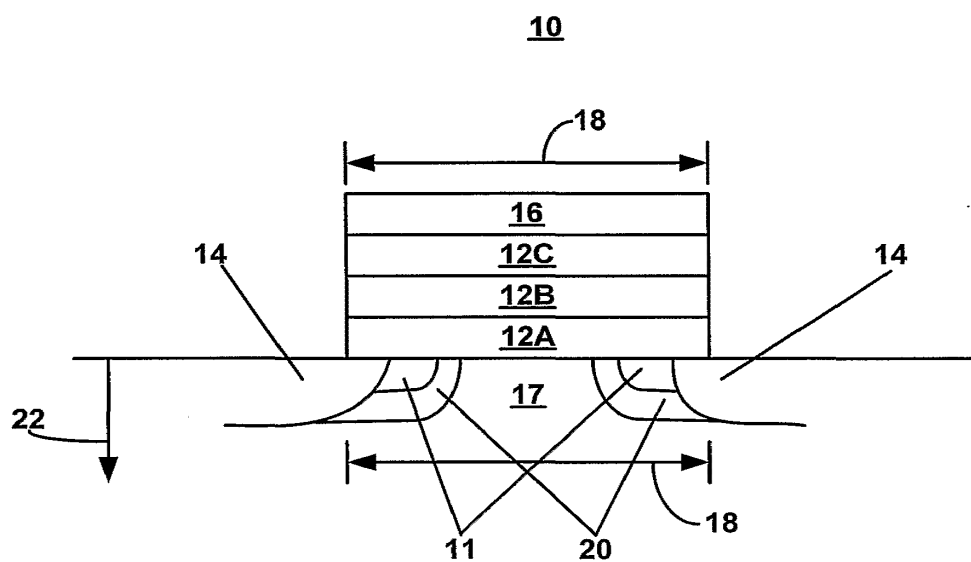
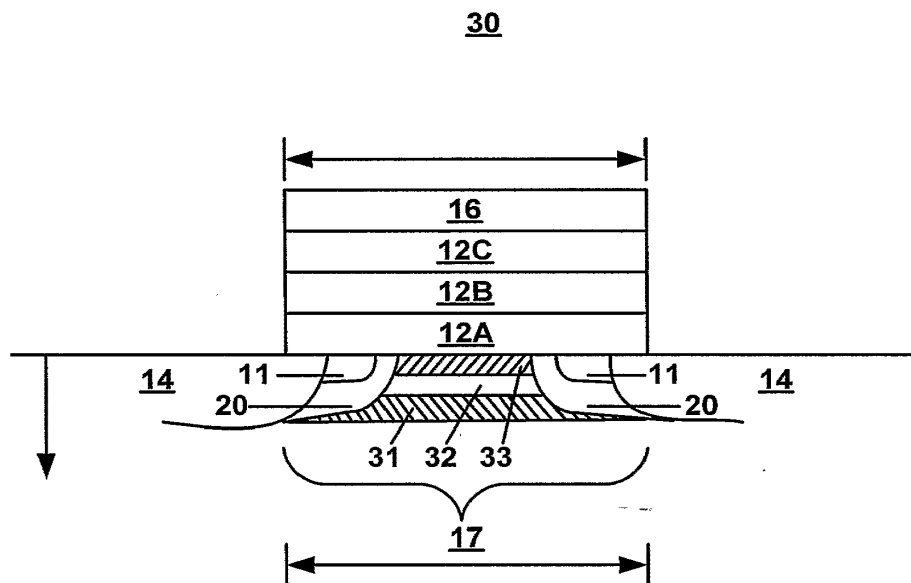
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FIG. 1
(CONVENTIONAL ART)

2/4**FIG. 2**

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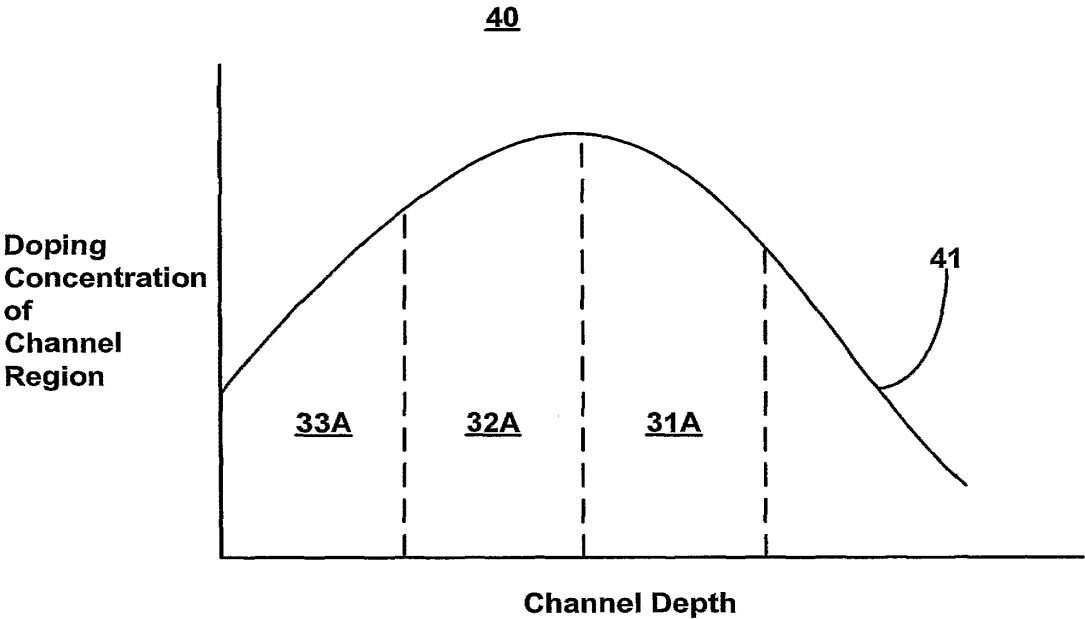
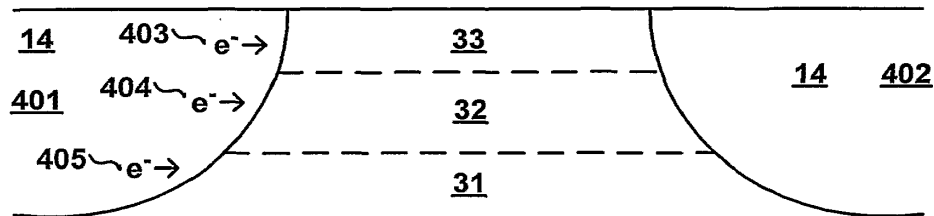
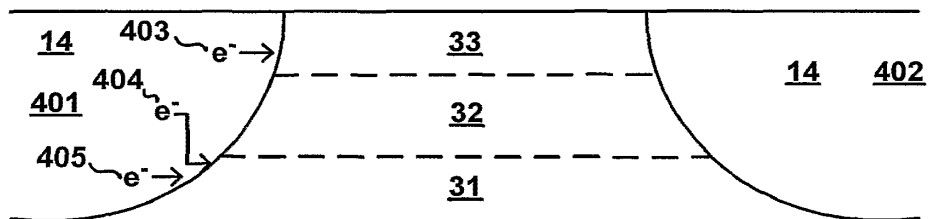
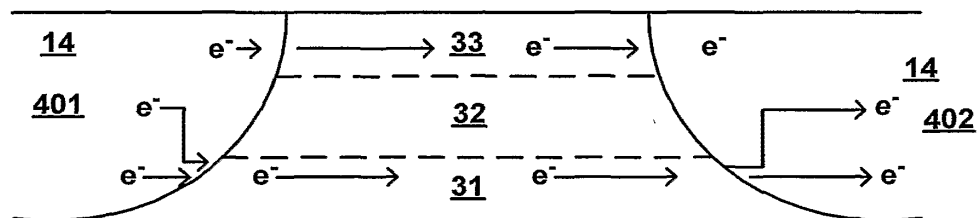


FIG. 3

4/4**FIG. 4A****FIG. 4B****FIG. 4C**

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 03/21682

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L29/788 H01L29/792 H01L21/8234 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/106852 A1 (CHANG CHI ET AL) 8 August 2002 (2002-08-08) paragraphs '0047!-'0055!; figures 5-8	1-10
Y	US 5 923 985 A (AOKI KENJI ET AL) 13 July 1999 (1999-07-13) column 3, line 60 -column 4, line 28; figures 8A-8D,9	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 03, 30 March 2000 (2000-03-30) -& JP 11 354778 A (MITSUBISHI ELECTRIC CORP), 24 December 1999 (1999-12-24) abstract; figures	1-10



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
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- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search

11 February 2004

Date of mailing of the international search report

18/02/2004

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 03/21682

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 6 258 645 B1 (KANG WOO TAG) 10 July 2001 (2001-07-10) the whole document ----	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 161 (E-257), 26 July 1984 (1984-07-26) -& JP 59 061070 A (FUJITSU KK), 7 April 1984 (1984-04-07) abstract; figures -----	1-10

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 03/21682

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I, Michael Fletcher, declare:

1. I am well versed in both the Japanese and English languages and have over 15 years of experience translating Japanese technical documents into English.
2. The following translation of the patent document JP07-306752 to English is accurate and complete to the best of my knowledge.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Executed this 4th day of September 2019, at Parowan, UT

A handwritten signature in cursive script that reads "Michael Fletcher".

Michael Fletcher

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Office (JP)

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(21) Application No.: 2001-235765	(71) Applicant	000005108 Hitachi Ltd. 6, 4-chome, Kandasurgadai, Chiyoda-ku, Tokyo
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(54) TITLE OF THE INVENTION:

Semiconductor Device Manufacturing Method and Semiconductor Device

(57) ABSTRACT (Revised)

[Issue] Achieve increase in drive current through substrate floating, achieve reduction in junction capacitance, and resolve thermal insulation and crystal defects that are shortcomings of SOI substrates.

MEANS FOR SOLVING THE PROBLEM

Providing of an n (p) well NWL (PML) between the p (n) type semiconductor area PA (PN) and semiconductor substrate 15 arranged using n (p) channel type MISFETQn (Qp) to electrically isolate the p (n) type semiconductor area PA (PN) and the semiconductor substrate 15.

second conductivity type semiconductor area, and (c) a step of forming a field effect transistor with a second conductivity type channel area within the first conductivity type semiconductor area.

[Claim 2]

A semiconductor device with a field effect transistor provided within a first conductivity type semiconductor area provided on a semiconductor substrate having a second conductivity type channel area with the opposite conductivity type than the first conductivity type, wherein a second conductivity type semiconductor area is provided between said semiconductor substrate and said first conductivity type semiconductor area to isolate said first conductivity type semiconductor area on which the second conductivity type channel area of said field effect transistor is formed from said semiconductor substrate.

[Claim 3]

A semiconductor device with a field effect transistor provided within a first conductivity type semiconductor area provided on a semiconductor substrate having a second conductivity type channel area with the opposite conductivity type than the first conductivity type, and a configuration where a second conductivity type semiconductor area is provided between said semiconductor substrate and said first conductivity type semiconductor area to isolate said first conductivity type semiconductor area on which the second conductivity type channel area of said field effect transistor is formed from said semiconductor substrate, wherein the thickness of said first conductivity type semiconductor area under the semiconductor area for said field effect transistor source and drain is greater than the sum of the width of the depletion layer of the junction between the semiconductor areas for source and drain for when supply voltage is applied and said first conductivity type semiconductor area and the width of the depletion layer of the junction between the first conductivity type semiconductor area and the second conductivity type semiconductor area.

[Claim 4]

A semiconductor device with a field effect transistor provided within a first conductivity type semiconductor area provided on a semiconductor substrate having a second conductivity type channel area with the opposite conductivity type than the first conductivity type and a configuration where a second conductivity type semiconductor area is provided between said semiconductor substrate and said first conductivity type semiconductor area to isolate said first conductivity type semiconductor area on which the second conductivity type channel area of said field effect transistor is formed from said semiconductor substrate, wherein the thickness of the second conductivity type semiconductor area is greater than the sum of the width of the depletion layer of the junction between the first conductivity type semiconductor area and the second conductivity type semiconductor area and the width of the depletion layer of the junction between the second conductivity type semiconductor area and the semiconductor substrate.

[Claim 5]

A semiconductor device with a first field effect transistor and a second field effect transistor on the main surface of a semiconductor substrate, wherein said first field effect transistor is provided with a first conductivity type semiconductor area provided on said semiconductor substrate, this first conductivity type semiconductor area is electrically isolated from said semiconductor substrate by a second conductivity type semiconductor area with opposite conductivity type than the first conductivity type provided between the first conductivity type semiconductor area and said semiconductor substrate and the second field effect transistor is provided within said second conductivity type semiconductor area.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNOLOGICAL FIELD INVENTION BELONGS TO

The present invention is related to a semiconductor device manufacturing method and a semiconductor device and in particular related to effective technology applied to a manufacturing method for a semiconductor device with a field effect transistor as well as to semiconductor device technology.

[0002]

BACKGROUND TECHNOLOGY

The technology investigated by the inventors is a semiconductor device structure providing a field effect transistor on a, for example, partially depleted SOI (Silicon On Insulator) substrate. An SOI substrate has a structure of a thin semiconductor layer provided on a substrate insulator layer with an element such as a field effect transistor or the like formed on the primary surface of the semiconductor layer. When voltage is applied to the gate electrode of the field effect transistor of this structure, the depletion layer expands from the gate insulation film but does not reach the substrate insulator layer even at maximum depletion layer width leaving substrate area that is not depleted. This is the structure most widely used and the substrate (in other words, semiconductor layer) is electrically insulated so when conducting, the substrate potential rises and threshold voltage lowers and this results in achieving high drive current. In addition, semiconductor area for source and drain and depletion layer for joining with a channel layer extends as far as the substrate insulator layer dramatically reducing junction capacitance.

[0003]

A partially depleted SOI substrate is described in Scalability of SOI Technology into 0.13 μm 1.2V CMOS Generation, E. Leobandung, et. al, Tech Digest of IEDM98, PP403-406, 1998 IBM.

[0004]

THE ISSUE(S) THAT THIS INVENTION INTENDS TO RESOLVE

However, with the semiconductor device technology that uses an SOI substrate described above, the substrate price is high price, 5 times that of a normal substrate. The structure is an element area covered with an insulator body so thermal resistance is high and this readily leads to increase in bonding temperature. Currently, crystal defects are high compared to normal substrate structures. In addition, the element area is completely isolated by the insulator leading to the problem that substrate floating control is difficult. Here, achieving the advantages of a SOI structure on a normal substrate structure in some manner is an important issue.

[0005]

An objective of the present invention is to provide technology that improves the performance of semiconductor devices.

[0006]

Furthermore, an objective of the present invention is to provide technology reducing the cost of semiconductor devices.

[0007]

This and other objects of the present invention will become clear through the description in this specification as well as the attached drawings.

[0008]

MEANS FOR SOLVING THE VARIOUS ISSUES

A simple description of a summary representing the invention disclosed in this application is provided below.

[0009]

In other words, the present invention is separation of a semiconductor substrate and a semiconductor area formed by a channel of a field effect transistor formed on the primary surface thereof using a pn junction.

[0010]

In addition, the present invention is, with a semiconductor substrate and semiconductor area having a field effect transistor formed on the main surface thereof, a semiconductor area with a conductivity type opposite that of the semiconductor area is provided therebetween to isolate the semiconductor substrate and semiconductor area.

[0011]

EMBODIMENTS OF THE INVENTION

In the following embodiments, the description is separated into a plurality of sections or embodiments as needed for convenience. However, except for when stated explicitly, these are not mutually unrelated where one is a partial or full modified example of another and are related in terms of detail and supplemental description and the like.

[0012]

In addition, in the embodiments below, when number of elements are referred to (including pieces, number amount, range and the like), it is not limited to the indicated number and can be more or less than the indicated number except where stated explicitly and when clearly limited to a specific number based on principle.

[0013]

Furthermore, in the following embodiments, it goes without saying that the structural elements (including element steps and the like) are not necessarily essential unless stated explicitly or can be considered to be clearly essential based on principle.

[0014]

In a similar manner, when structural element shape and positional relationships are referenced in the embodiments below, this includes items that are approximate or similar or the like essentially that shape or the like except when stated explicitly or can be considered that this is clearly not the case based on principle. The same goes for numerical values and range described above.

[0015]

In addition, items with the same function are given the same code in all drawings for describing the embodiments and repeated description is omitted.

[0016]

In addition, in the present embodiments, MISFET (Metal Insulator Semiconductor Field Effect Transistor) that is representative of field effect transistors is abbreviated as MIS, p channel type MISFET is abbreviated as pMIS, and n channel type MISFET is abbreviated as nMIS.

[0017]

An embodiment of the present invention will be described in detail below based on the drawings.

[0018]

(Embodiment 1) FIG. 1 shows a cross section of the main part of the logic circuit on the semiconductor chip 1C that makes up the semiconductor device that is embodiment 1 of the present invention. In addition, FIG. 2

shows the impurity concentration distribution of the semiconductor substrate (hereafter, simply substrate) 1S that makes up the semiconductor chip 1C.

[0019]

The substrate 1S is made up of a single crystal of, for example, p type silicon (Si). A groove type partitioning part (SGI; Shallow Groove Isolation) 2 is formed on the main surface (device forming surface). The groove type partitioning part 2 is formed, for example after forming a groove for partitioning on the main surface of the substrate 1S, by depositing an insulating membrane such as a silicon oxide membrane (SiO_2) and the like on the main surface of the substrate 1S embedded within the groove, and further by polishing using CMP (Chemical Mechanical Polishing) and the like such that the insulating membrane is left only within the groove. The depth of the groove type partitioning part 2 (distance from main surface of substrate 1S to bottom surface of partition part 2) is, for example, roughly 0.2 to 0.3 μm . The area surrounded by this groove type partitioning part 2 is an active area (device forming area). With regards to this substrate 1S, a p type semiconductor area PA (first conductivity type semiconductor area) is formed in this active area. Boron (B) or Boron difluoride (BF_2), for example, is included in this p type semiconductor area PA. Here, nMISQn for a logic circuit formed inside this p type semiconductor area PA is shown as an example.

[0020]

The nMISQn comprises semiconductor areas 3, 3 for source and drain, a channel area CHn, a gate insulating film 4, and a gate electrode 5. The semiconductor areas 3, 3 for source and drain are arranged in a pair on both sides with the channel areas CHn formed in the p type semiconductor area PA interposed, each comprising an n type semiconductor area 3a arranged in the vicinity of each of the channel areas CHn and an n^+ type semiconductor area 3b arranged in a position at a distance from the channel area CHn with the n type semiconductor 3a interposed. The n type semiconductor 3a and n^+ type semiconductor area 3b both contain, for example, phosphorus (P) or arsenic (As). However, the n type semiconductor 3a is also called an extension area, of which impurity concentration is set to be lower than that of the n^+ type semiconductor area 3b. In other words, it is a LDD (Lightly Doped Drain) structure.

[0021]

In addition, with the structure of the present embodiment 1 as described below, as the p type semiconductor area PA is in a state of floating electrically, reducing the threshold voltage, the threshold voltage is set such that it is 50 mV to 100 mV higher than normal by having a comparatively high impurity concentration of the channel area CHn to prevent the threshold voltage from falling too much. Here, ions are implanted on the main surface of the substrate 1S, for example, with boron at an ion implantation energy of around 10 keV into the channel area CHn, as a way to adjust the threshold voltage.

[0022]

The gate insulating film 4 is made up of, for example, silicon oxide (SiO_2). The thickness thereof is the silicon dioxide exchange film thickness, for example, 2.5 nm or less, or roughly 1.5 nm as an example. However, materials for the gate insulating film are not limited to this, and can be changed, for example, the gate insulating film 4 can be a silicon oxynitride film (SiON). In other words, there can be a structure segregating nitrogen at the interface layer between the gate insulating film 4 and the substrate 1S. A silicon oxynitride film can suppress interface level generation in the film and has high effectiveness in decreasing electron trap compared to a silicon oxide film, such that it can improve hot carrier tolerance in the gate insulating film 4 and improve dielectric strength. In addition, it is more difficult for impurities to penetrate a silicon oxynitride membrane compared to a silicon oxide membrane; therefore, use of a silicon oxynitride membrane enables control of fluctuations in threshold voltage that can cause scattering of impurities in the gate electrode material on the substrate 1S side. In order to form a silicon oxynitride membrane, for example, the substrate 1S is subjected to heat treatment in a

nitrogen-containing gas atmosphere such as NO, NO₂, or NH₃. In addition, the effects as stated above can also be obtained by heat treating the substrate 1S in the nitrogen-containing gas atmosphere after forming a gate insulating film 4 made up of silicon oxide on the surface of the substrate 1S, and segregating the nitrogen in the interface layer between the gate insulating film 4 and the substrate 1S. In addition, the gate insulating film 4 can have a structure where a silicon nitride film is laminated on the silicon oxide film. Furthermore, the gate insulating film 4 can be formed from an insulating film made up of high dielectric films, for example, HfO₂ (dielectric constant $\epsilon_r = 20.6$), ZrO₂ ($\epsilon_r = 24.7$), Al₂O₃ ($\epsilon_r = 8.4$), Y₂O₃ ($\epsilon_r = 14$), HfSiO₄, ZrSiO₄ ($\epsilon_r = 19.4$), and the like.

[0023]

The gate electrode 5, for example, is made up of a low-resistance polycrystalline silicon. However, it is not limited to this, and various modifications are feasible, for example, it can be a so-called polymetal gate electrode structure providing a metal membrane such as tungsten and the like on a so-called polycide gate electrode structure or low-resistance polycrystalline silicon membrane through a barrier metal layer such as a tungsten nitride (WN) and the like, which provides a silicide layer such as a cobalt silicide (CoSi₂) on the low-resistance polycrystalline silicon membrane. A sidewall 7 made up of a silicon oxide membrane is formed to form a LDD structure on the side surface of the gate electrode 5. In addition, the gate lengths are around 0.14 μm for a gate insulating film 4 thickness of 2.5 nm, and around 0.08 μm for a gate insulating film 4 thickness of 1.5 nm. In addition, the source voltage on the high-voltage side of the logic circuit area formed on the nMISQn is, for example, around 1.5 V to 0.7 V, and is comparatively lower than the source voltage on the high-voltage side of the surrounding circuit areas. Furthermore, regarding the semiconductor chip 1C, the source voltage on the high-voltage side of the surrounding circuit areas (for example, the input circuit, output circuit, and input/output bidirectional circuit) is around 3.0 V or 3.3 V.

[0024]

This type of nMISQn is covered by an interlayer insulating membrane 8 deposited on the main surface of the substrate 1S. The interlayer insulating membrane 8 is made up of, for example, a silicon oxide membrane, and a first layer wiring 9 is formed on the surface thereof. The first layer wiring 9, is made up of, for example, aluminum or aluminum alloy, and is electrically connected to a semiconductor area 3 for source and drain through contact holes 10 that are bored in the interlayer insulating membrane 8.

[0025]

Incidentally, the present inventors found while developing a semiconductor device using a partially depleted SOI substrate, that many of the merits of using a partially depleted SOI substrate compared to use of a normal substrate were an increase in drive current due to floating of the substrate and a decrease in junction capacitance. Here, a structure such as the one that follows was used in order to achieve a structure that has these kinds of merits with a normal substrate.

[0026]

In other words, regarding the present embodiment 1, an n-well NWL (second conductive type semiconductor area) is provided between the p type semiconductor area PA where the nMISQn is formed and the lower layer substrate 1S. Regarding the depth from the main surface of the substrate 1S so that the substrate 1S and p type semiconductor area PA as well as the channel area CHn and substrate 1S are not electrically connected, the impurity distribution of the n-well NWL is formed at a position slightly more shallow than the bottom of the groove type partitioning part 2, and distributed from a position deeper than the peak position of the p type semiconductor area PA to a position slightly more shallow than the bottom of the groove type partitioning part 2. In other words, regarding the present embodiment 1, the channel areas CHn of the nMISQn, and the p type semiconductor area PA and the substrate 1S, are electrically isolated by a pn junction between the n-well NWL

and the substrate 15. Here, with a power supply voltage applied to the semiconductor area 3 for the nMISQn source and drain, connecting of the n⁺ type semiconductor area 3b and n-well NWL needs to be prevented by a depleted layer with the junction of the channel area CHn (p type semiconductor area PA) and depleted layer spreading between the channel area CHn (p type semiconductor area PA) and n-well NWL. In other words, the distance x 1 in FIG.1 needs to be larger than the sum of the widths of the depletion layers described above. In addition, the width x2 of the n-well NWL itself can not be allowed to be reduced by the depletion layer with the channel area CHn (p type semiconductor area PA) or the depletion layer with the substrate 15. In other words, the width x2 needs to be larger than the sum of the depletion layer widths. This type of n-well NWL can be formed using ion implantation of phosphorus, for example, onto the main surface of the substrate 15 with an ion implantation energy of around 450 keV of phosphorus, for example, after the groove type partitioning part 2 is formed. Furthermore, the impurity concentration of the n-well NWL at its peak position is, for example, around 10¹⁸/cm³ or somewhat lower, as shown in FIG. 2.

[0027]

By providing this type of n-well NWL, similar effects to those of using an SOI substrate can be obtained depending on the performance of the semiconductor device. In other words, while conducting, the threshold voltage of the nMISQn decreases and current increases, due to an increase in potential of the channel area CHn (p type semiconductor area PA) from a capacitive coupling of the gate electrode 5 and the channel area CHn (p type semiconductor area PA), and an increase in potential of the channel area CHn (p type semiconductor area PA) due to the generation of impact ionization holes from drain current flow. FIG. 3 shows the gate voltage dependence of the drain current between the nMISQn of the present embodiment 1 and the nMIS formed on a normal substrate that does not contain an n-well isolation structure. In the present embodiment 1, as the channel area CHn (p type semiconductor area PA) is electrically insulated, threshold voltage is lowered and drain current can be increased when gate voltage is applied. In addition, the junction capacitance between the semiconductor area 3 for source and drain and the substrate 15 can be decreased to 1/3 of a case where the n-well NWL is not provided, as the junction capacitance of the n⁺ type semiconductor area 3b and the channel area CHn (p type semiconductor area PA), the junction capacitance of the channel area CHn (p type semiconductor area PA) and the n-well NWL, and the junction capacitance of the n-well NWL and the substrate 15 are put in a state of serial connection. Therefore, operation speeds of a circuit comprising this transistor can be increased.

[0028]

In addition, as the channel area CHn (p type semiconductor area PA) and the substrate 15 are not completely isolated by an insulator, and have a structure such that they are isolated by the n-well NWL that more readily releases heat in comparison to an SOI substrate, increase in heat resistance can be substantially reduced, suppressing an increase in junction temperature. Therefore, operation reliability of the semiconductor device can be improved. In addition, a cooling structure of the package itself, or a cooling device or cooling mechanism for cooling the semiconductor device can be simplified.

[0029]

In addition, crystal defects can be reduced in comparison to an SOI substrate. Therefore, the yield and reliability of the semiconductor device can be improved.

[0030]

In addition, an increase in substrate potential can be controlled with comparative ease by controlling the leakage current of the pn junction under the channel area CHn. In other words, the controllability of substrate floating can be improved. Therefore, this can simplify circuit design.

[0031]

In addition, providing of an n-well NWL is basically a normal substrate structure and so this enables reducing costs of the semiconductor device compared to the case of using a high cost SOI substrate.

[0032]

(Embodiment 2) Embodiment 2 is a description of applying the present invention to a semiconductor device that has a CMIS (Complementary MIS).

[0033]

FIG. 4 shows a cross section of the main part of a CMIS circuit that makes up a logic circuit on the semiconductor chip 1C that forms the semiconductor device of another embodiment of the present invention.

[0034]

As the vertical structure of the area the nMISQn is formed on is the same as that in embodiment 1, the explanation thereof is omitted. Here, a description of the vertical structure of the area pMISQp is formed on is provided. Regarding the area the pMISQp is formed on, an n type semiconductor area NA (second conductive type semiconductor area) is formed on the active area of the substrate 1S, and the pMISQp is formed within this n type semiconductor area NA. The n type semiconductor area NA, for example, contains phosphorus (P) or arsenic (As).

[0035]

The pMISQp comprises semiconductor areas 11, 11 for a source and drain, a channel area CHp, a gate insulating film 4, and a gate electrode 5. The semiconductor areas 11, 11 for source and drain are arranged as a pair with a channel area CHp interposed can comprise p type semiconductor areas 11a arranged respectively close to the channel area CHp and p⁺ type semiconductor area 11b arranged at a distance from the channel area CHp with the p type semiconductor areas 11a interposed. The p type semiconductor area 11a and p⁺ type semiconductor area 11b both contain, for example, boron (B) or boron difluoride (BF₂). However, the p type semiconductor area 11a can be called an extension area, of which impurity concentration is set to be lower than that of the p⁺ type semiconductor area 11b. In other words, it is a LDD structure.

[0036]

In addition, regarding the present embodiment 2, a p-well PWL (first conductivity type semiconductor area) is provided between the n type semiconductor area NA where the pMISQp is formed and the substrate 1S. In other words, regarding the present embodiment 2, the channel areas CHp (n type semiconductor area NA) of the pMISQp and the substrate 1S are electrically isolated by the pn junction between the p-well PWL and the n type semiconductor area NA. As the impurity distribution forming conditions for the p-well PWL are the same as the n-well NWL, the explanation thereof is omitted. This type of p-well PWL can be formed by ion implantation on the main surface of the substrate 1S with an ion implantation energy of around 160 keV of boron, for example, after the groove type partitioning part 2 is formed. Furthermore, the impurity concentration at the peak position of the p-well PWL is around the same as the n-well NWL. The channel area CHp of the pMISQp is formed by ion implantation of phosphorus onto the main surface of the substrate 1S surface with using roughly 20 keV, for example, to reach the prescribed desired threshold (enhancement of roughly 50 mV to 100 mV compared to a conventional structure). Other items are the same as embodiment 1, and the description is omitted.

[0037]

In this manner, with embodiment 2, the following effects, other than the effects obtained in embodiment 1, can be obtained. In other words, the pMISQp achieves the same effects as the nMISQn. Therefore, the operating

speed (performance) of a semiconductor device that has a logic circuit configured with a CMIS circuit can be improved.

[0038]

(Embodiment 3) Regarding the vertical structure of the MIS in embodiments 1 and 2, operation speed can be improved as stated above, however, MIS threshold voltage fluctuates within the active area and becomes unstable. Here, regarding the present embodiment 3, MIS that use a vertical structure and those that do not, even for MIS that are formed on the same substrate 1S, were produced separately. In other words, there are different purposes, a MIS vertical structure as explained in embodiments 1 and 2 according to the electrical characteristics required by the circuit, and a normal MIS vertical structure. More specifically, the MIS vertical structure above is used for a MIS configured with a circuit in which the operations thereof are not obstructed by threshold voltage to a certain extent, and a general MIS vertical structure is used and not the MIS vertical structure above for a MIS configured with a circuit in which operations thereof are obstructed by a fluctuating threshold voltage. For example, for a MIS that makes up a digital circuit, the MIS vertical structure as explained in embodiments 1 and 2 is used. In addition, for example, the MIS vertical structure described above were not used for MIS that make up analog circuits where, for example, high operation precision is required, input/output circuits, or memory cells or sense amp circuits of memory circuits (hereafter simply called analog circuits and the like). Here, normal MIS vertical structures were used. While a memory cell is a digital circuit, they read and write microscopic signals (charges), so threshold voltage fluctuations of the MISFET that makes up the memory cell can hinder data processing, such that use of a common MIS vertical structure is preferable. In addition, based on analysis by the present inventors, when considering from the perspective of the MIS operating voltage (source voltage on the high-voltage side), if the operating voltage is 1.5 V or less, for example, use of the MIS vertical structure as explained in embodiments 1 and 2 is preferable. On the other hand, if the operating voltage of the MIS is higher than 1.5 V, use of the common MIS vertical structure is preferable.

[0039]

FIG. 5 shows an example of a cross-section view of the main part of the semiconductor device of the present embodiment 3. An area A1 shows an arrangement area of the nMISQn that makes up a logic circuit (digital circuit) and the pMISQp (first field effect transistor). In the area A1, the MIS vertical structure as described in embodiments 1 and 2 is used.

[0040]

On the other hand, an area A2 shows an arrangement area of a nMISQn1, Qp1 (2nd field effect transistor) that makes up a circuit generating an obstruction when threshold voltage such as the analog circuit, input/output circuit, memory cells or sense circuit of a memory circuit, or the like fluctuates. In the area A2, a common MIS vertical structure is used. In other words, the nMISQn1 is formed inside of the p-well PWL, and a pMISQp1 is formed inside the n-well NWL. The structures of the p-well PWL and the n-well NWL of the area A2 are the same structures of the p-well PWL and the n-well NWL of the area A1. Channel ion implantation is performed for channel areas CHn1, CHp1 of the nMISQn1 and the pMISQp1 in area A2 as well; performing adjustments to threshold voltage.

[0041]

In this manner, regarding the present embodiment 3, effects as follows other than those that were obtained in the embodiments 1 and 2 can be obtained.

[0042]

In other words, by using a MIS vertical structure as described in embodiments 1 and 2 for a logic circuit MIS, and using a normal MIS vertical structure for an analog circuit and the like, an improvement in operating speed of

the logic circuit and an improvement in operating reliability of the analog circuit and the like can both be achieved.

[0043]

(Embodiment 4) In the CMIS circuit structure of embodiment 2, there are cases where the increase in substrate potential when voltage is applied to the gate is too large. In this case, as shown in FIG. 6, a crystal defect 12 is formed in the vicinity of the junction of the p type semiconductor area PA and the n-well NWL by ion implantation of impurity ions such as argon (Ar), germanium (Ge), and the like. As this causes a moderate re-combination in the depletion layer of the pn junction of the p type semiconductor area PA and the n-well NWL, allowing a leakage current to flow, ability to control this enables suppressing rise in potential of the p type semiconductor area PA. Therefore, as this improves controllability of nMISQn threshold voltage settings, operating reliability of the semiconductor device can be improved. Furthermore, electrons that were generated by the impact ionization of the pMISQp n type semiconductor area flow to the source p⁺ type semiconductor area 11b (power supply wiring on the high-potential side). On the pMISQp side, a floating suppression effect for substrate potential is not produced even if a re-combination nucleus is formed so a crystal defect is not provided on the pMISQp side.

[0044]

(Embodiment 5) The present embodiment 5 is an explanation of a modified example to achieve the same objective as explained in embodiment 4. In other words, with an objective of suppressing an increase in substrate potential, a p⁺ type semiconductor area 13P with a high impurity concentration is provided on the lower part of the p type semiconductor area PA (between the p type semiconductor area PA and the n-well NWL), as shown in FIG. 7. The p⁺ type semiconductor area 13P comes in contact with both the p type semiconductor area PA and the n-well NWL. By providing this type of p⁺ type semiconductor area 13P, the impurity concentrations in the area corresponding to the parasitic bipolar transistor base area formed by the source and drain semiconductor area 3 of the nMISQn and the p type semiconductor area PA can be increased, such that the current amplification factor of the parasitic bipolar transistor can be reduced. As a result, increase in substrate potential can be controlled. Therefore, as this improves controllability of nMISQn threshold voltage settings, operating reliability of the semiconductor device can be improved.

[0045]

In addition, regarding the present embodiment 5, with an objective of suppressing rise in substrate potential, an n⁺ type semiconductor area 13N with a high impurity concentration is provided on the lower part of the n type semiconductor area NA (between the n type semiconductor area NA and the p-well PWL). The n⁺ type semiconductor area 13N comes in contact with both the n type semiconductor area NA and the p-well PWL. Providing this type of n⁺ type semiconductor area 13N, improves setting controllability of the pMISQp threshold value for the same reasons as with the nMISQn, enabling improving operating reliability of the semiconductor device.

[0046]

(Embodiment 6) The present embodiment 6 is a description of a modified example to achieve the same objective as explained in embodiments 4 and 5. In other words, with an objective of suppressing rise in substrate potential, regarding the forming area of the nMISQn, a p⁺ type semiconductor area 13 is provided in a state of contact with the lower part of the p type semiconductor area PA, and an n⁺ type semiconductor area 14 is provided in a state of contact with the lower part thereof, and the n-well NWL is provided in a state of contact with the lower part thereof, as shown in FIG. 8. This enables forming p⁺ and n⁺ high impurity concentration junctions, increasing the diode tunnel current, and causing a re-combination, such that the increase in substrate potential of the p type semiconductor area PA can be further suppressed. Therefore, as this improves

controllability of nMISQn threshold voltage settings, operating reliability of the semiconductor device can be improved. Furthermore, on the pMISQp side, an n⁺ semiconductor area and a p⁺ semiconductor area are not provided on the lower part of the n type semiconductor area NA for the same reasons as explained in embodiments 4 and 5.

[0047]

The present invention discovered by inventors has been specifically described using an embodiment; however, the present invention is not restricted to the embodiment described above and it goes without saying that various changes that do not deviate from the essentials of the invention can be made.

[0048]

In these explanations the invention made by the present inventors were mainly explained by application to semiconductor devices that have CMIS circuits, a use field of their background. However, use is not limited as such, and for example, can also be applied to semiconductor devices that have memory circuits such as DRAM (Dynamic Random Access Memory), SRAM (Static Random Access Memory), or flash memory (EEPROM; Electric Erasable Programmable Read Only Memory), and the like, semiconductor devices that have logic circuits such as a microprocessor, or consolidated type semiconductor devices that provide a memory circuit and a logic circuit on the same semiconductor substrate.

[0049]

EFFECT OF THE INVENTION

A simple description of the effects that can be obtained representing the invention disclosed in this application is provided below.

- (1) The performance of a semiconductor device can be improved by using a pn junction to isolate a semiconductor substrate and a semiconductor area formed by a field effect transistor channel formed on the main surface thereof.
- (2) A semiconductor device can be configured using a normal substrate structure without using an SOI structure that has a relatively high number of defects and is highly priced, by isolating a semiconductor substrate and a semiconductor area formed by a field effect transistor channel formed on the main surface thereof using a pn junction, enabling cost reduction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of the first embodiment of the present invention.

FIG. 2 is a graph diagram showing the impurity concentration distribution of the semiconductor substrate of the semiconductor device in FIG. 1.

FIG. 3 is a graph diagram showing the drain current gate voltage dependence of the field effect transistor of the semiconductor device in FIG. 1 and the field effect transistor formed on a normal semiconductor substrate.

FIG. 4 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.

FIG. 5 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.

FIG. 6 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.

FIG. 7 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.

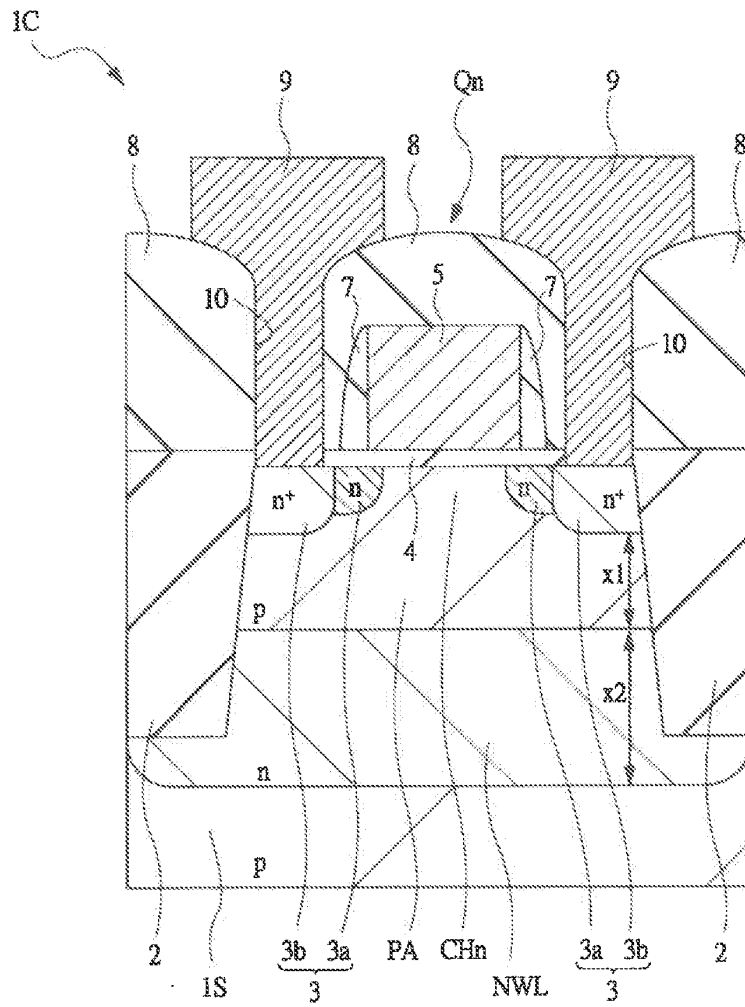
FIG. 8 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of a further additional embodiment of the present invention.

EXPLANATION OF CODES

1C. semiconductor chip
1S. semiconductor substrate
2. Partitioning part
3. Semiconductor area
3a. n type semiconductor area
3b. n⁺ semiconductor area
4. Gate insulating film
5. Gate electrode
7. Sidewall
8. Interlayer insulating membrane
9. First layer wiring
10. Contact hole
11. Semiconductor area
11a. p type semiconductor area
11b. p⁺ type semiconductor area
12. Crystal defect
13P. p⁺ type semiconductor area
13N. n⁺ semiconductor area
14. n⁺ semiconductor area
PA. p type semiconductor area (first conductivity type semiconductor area)
NWL. n-well (second conductivity type semiconductor area)
NA. n type semiconductor area (second conductivity type semiconductor)
PWL. p-well (first conductivity type semiconductor area)
Qp. p-channel type MISFET (first field effect transistor)
Qn. n-channel type MISFET (first field effect transistor)
Qp1. p-channel type MISFET (second field effect transistor)
Qn1. n-channel type MISFET (second field effect transistor)
CHn, CHn1 channel areas
CHp, CHp1 channel areas

[FIG. 1]

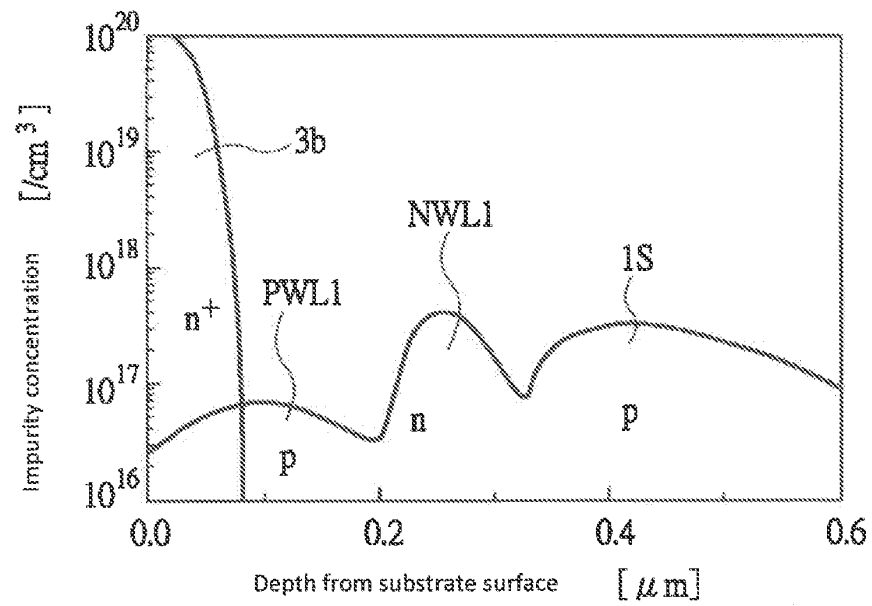
FIG. 1



15: Semiconductor substrate
 NWL: n-Well
 Qn: n-channel type MISFET
 PA: p type semiconductor area

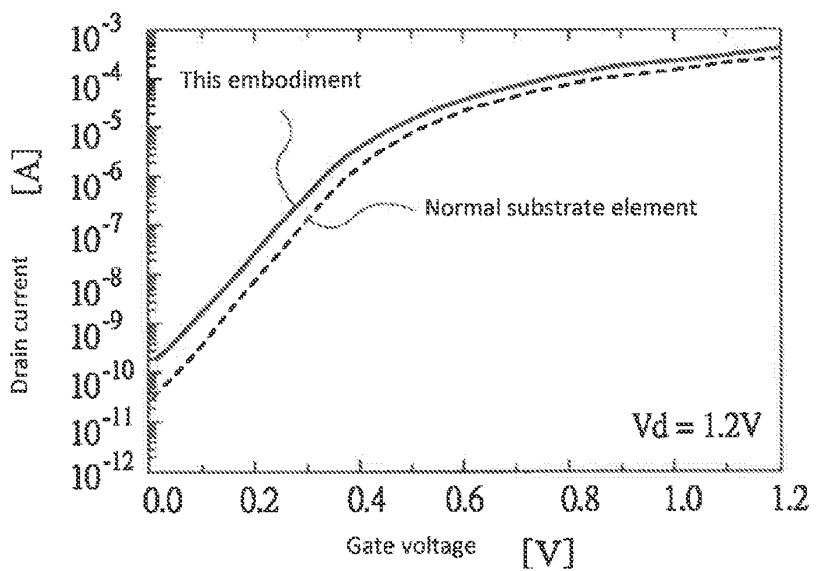
[FIG. 2]

FIG. 2



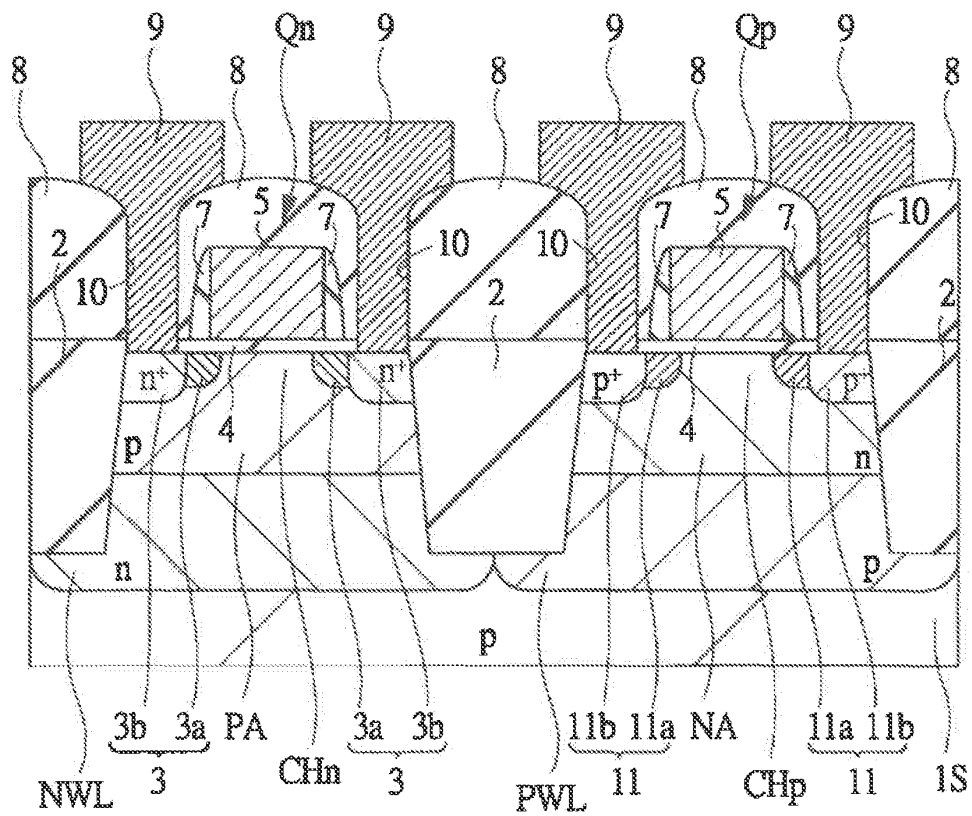
[FIG. 3]

FIG. 3



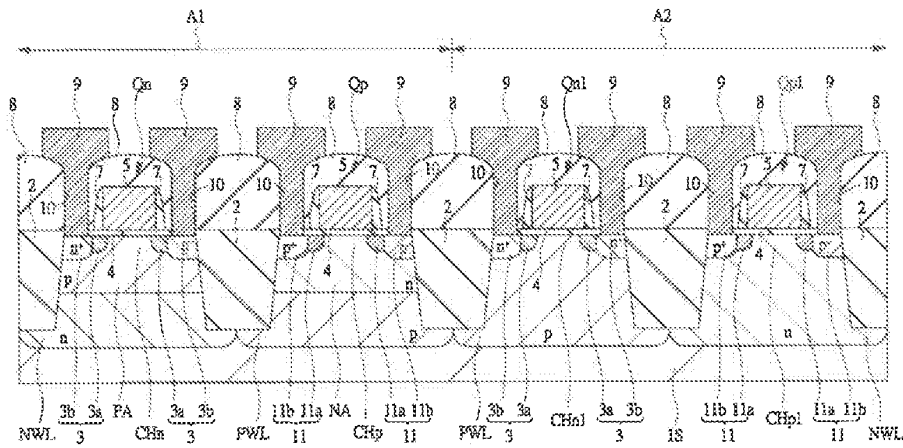
[FIG. 4]

FIG. 4



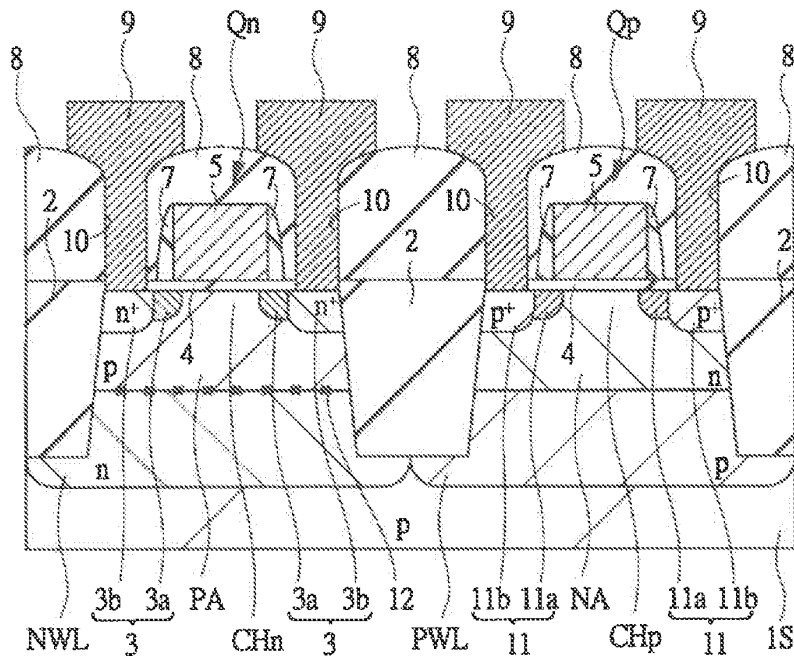
[FIG. 5]

FIG. 5



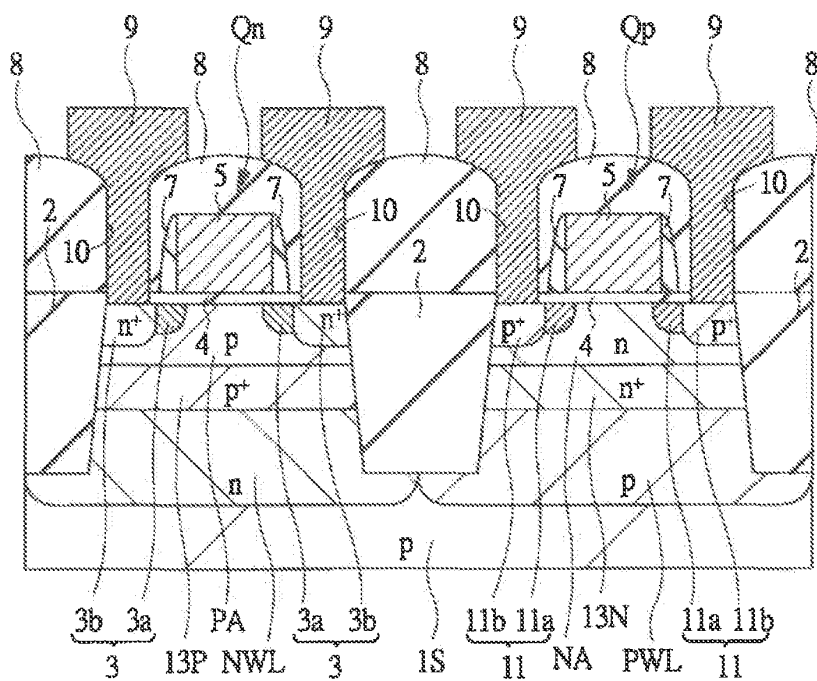
[FIG. 6]

FIG. 6



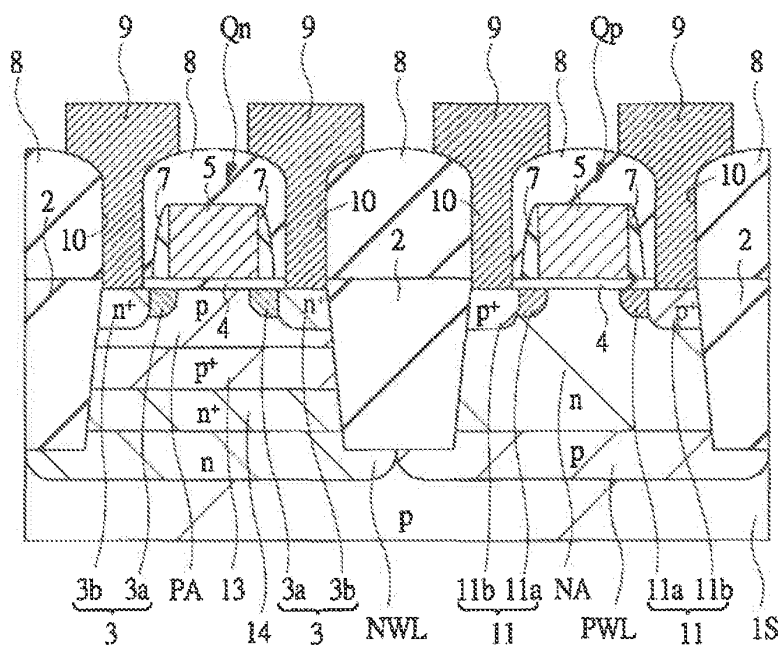
[FIG. 7]

FIG. 7



[FIG. 8]

FIG. 8



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F-Terms (reference)

SF032 AA35 AA44 AB01 AB03 CA01
CA03 CA17 CA20 DA60 DA63

SF048 AA01 AA03 AA04 AA07 AB01
AB03 BA01 BA13 BB05 BB08
BB09 BB11 BB12 BB13 BB14
BC06 BE02 BE03 BG14 BH01
BH03 DA25

SF140 AA00 AB03 BA01 BD09 BD11
BD13 BF01 BF04 BF11 BF18
BF20 BF21 BF25 BF27 BG08
BG12 BH15 BH50 BJ01 BJ05
BK13 CB04 CB08 CB10 CD02

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附記

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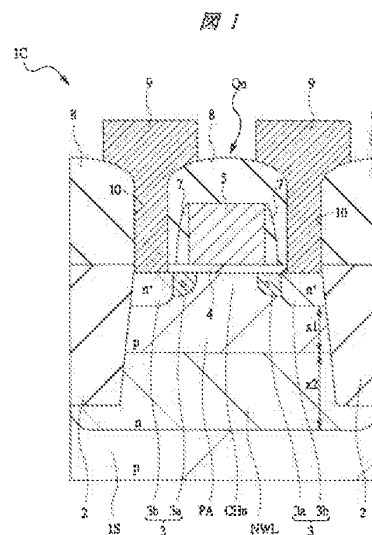
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(54) 【発明の名称】 半導体装置の製造方法および半導体装置

(57) 【要約】 (修正有)

【課題】 高価なSOI基板を用いることなく、基板フローティングによる駆動電流の増加と、接合容量の低減を実現するとともに、SOI基板の欠点である熱抵抗と結晶欠陥の課題を解決する。

【解決手段】 $n(p)$ チャネル型の MIS・FETQ $n(Qp)$ が配置された $p(n)$ 型の半導体領域 PA (PN) と、半導体基板 1S との間に $n(p)$ ウエル NWL (PML) を設けることにより、その $p(n)$ 型の半導体領域 PA (PN) と半導体基板 1S とを電気的に分離する。



IS: 半導体基板
 NWL: nウエル
 Co: nチャネル型のMOS・FET
 PA: p型の半導体領域

【特許請求の範囲】

【請求項1】 以下の工程を有することを特徴とする半導体装置の製造方法；

(a) 第1導電型の半導体基板に第1不純物を導入することにより、前記第1導電型とは反対の導電型の第2導電型の半導体領域を形成する工程、(b) 前記半導体基板に第2不純物を導入することにより、前記第2導電型の半導体領域の不純物ピーク位置よりも、前記半導体基板の主面から浅い位置に不純物ピーク位置が配置するように形成された第1導電型の半導体領域を形成する工程、(c) 前記第1導電型の半導体領域内に、第2導電型のチャンネル領域を有する電界効果トランジスタを形成する工程。

【請求項2】 半導体基板に設けられた第1導電型の半導体領域内に、その第1導電型とは反対導電型の第2導電型のチャンネル領域を有する電界効果トランジスタを設け、前記半導体基板と、前記第1導電型の半導体領域との間に、第2導電型の半導体領域を設けることで、前記電界効果トランジスタの第2導電型のチャンネル領域が形成される前記第1導電型の半導体領域と、前記半導体基板とを電気的に分離したことを特徴とする半導体装置。

【請求項3】 半導体基板に設けられた第1導電型の半導体領域内に、その第1導電型とは反対導電型の第2導電型のチャンネル領域を有する電界効果トランジスタを設け、前記半導体基板と、前記第1導電型の半導体領域との間に、第2導電型の半導体領域を設けることで、前記電界効果トランジスタの第2導電型のチャンネル領域が形成される前記第1導電型の半導体領域と、前記半導体基板とを電気的に分離した構造を有し、

前記電界効果トランジスタのソースおよびドレイン用の半導体領域下における前記第1導電型の半導体領域の厚さは、電源電圧の印加時に前記ソースおよびドレイン用の半導体領域および前記第1導電型の半導体領域の間における接合の空乏層幅と、前記第1導電型の半導体領域および前記第2導電型の半導体領域の間における接合の空乏層幅との和よりも大きいことを特徴とする半導体装置。

【請求項4】 半導体基板に設けられた第1導電型の半導体領域内に、その第1導電型とは反対導電型の第2導電型のチャンネル領域を有する電界効果トランジスタを設け、前記半導体基板と、前記第1導電型の半導体領域との間に、第2導電型の半導体領域を設けることで、前記電界効果トランジスタの第2導電型のチャンネル領域が形成される前記第1導電型の半導体領域と、前記半導体基板とを電気的に分離した構造を有し、前記第2導電型の半導体領域の厚さは、前記第1導電型の半導体領域および第2導電型の半導体領域の間における接合の空乏層幅と、前記第2導電型の半導体領域および前記半導体基板の間における接合の空乏層幅との和よりも大きいことを特徴とする半導体装置。

【請求項5】 半導体基板の主面に第1の電界効果トランジスタと、第2の電界効果トランジスタとを有し、前記第1の電界効果トランジスタは、前記半導体基板に設けられた第1導電型の半導体領域内に設けられ、その第1導電型の半導体領域は、その第1導電型の半導体領域と前記半導体基板との間に設けられた第1導電型とは反対導電型の第2導電型の半導体領域によって前記半導体基板と電気的に分離され、

前記第2の電界効果トランジスタは、前記半導体基板に設けられた前記第2導電型の半導体領域内に設けられていることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置の製造方法および半導体装置技術に関し、特に、電界効果トランジスタを有する半導体装置の製造方法および半導体装置技術に適用して有効な技術に関するものである。

【0002】

【従来の技術】本発明者らが検討した技術は、例えば部分空乏型のSOI(Silicon On Insulator)基板に電界効果トランジスタを設けた半導体装置構造である。SOI基板は、下地絶縁層上に薄い半導体層を設け、その半導体層の主面上に電界効果トランジスタ等のような素子を形成する構造を有している。この構造の電界効果トランジスタのゲート電極に電圧が印加されると、ゲート絶縁膜側から空乏層が広がるが、反転層が形成される最大の空乏層幅となっても下地絶縁層には到達せず、空乏化しない基板領域が残される。この構造は最も良く用いられているが、基板(すなわち、半導体層)が電気的に絶縁されていることにより、導通時に基板電位が上昇し、しきい値電圧が下がる結果、駆動電流を多くとれる効果がある。また、ソースおよびドレイン用の半導体領域とチャンネル層との接合の空乏層が下地絶縁層の上まで広がり、接合容量を大幅に低減できる。

【0003】なお、部分空乏化型のSOI基板については、例えばScalability of SOI Technology into 0.13 μm 1.2V CMOS Generation, E.Leobandung, et al, Tech. Digest of IEDM98, pp403-406, 1998, IBMに記載がある。

【0004】

【発明が解決しようとする課題】ところが、上記SOI基板を用いた半導体装置技術においては、基板価格が通常基板の5倍以上と高価である。素子領域が絶縁体で覆われる構造のため熱抵抗が大きく接合温度が上昇し易い、現状では結晶欠陥が通常の基板構造に比べて多い、また、素子領域が絶縁体で完全に分離されるため基板電位のフローティングの制御が難しい等のような問題がある。そこで、SOI構造が有している長所を如何にして通常の基板構造で実現するかが重要な課題となっている。

【0005】本発明の目的は、半導体装置の性能を向上させることのできる技術を提供することにある。

【0006】また、本発明の目的は、半導体装置のコストを低減することのできる技術を提供することにある。

【0007】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【0008】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。

【0009】すなわち、本発明は、半導体基板と、その主面に形成された電界効果トランジスタのチャネルが形成される半導体領域とをpn接合によって分離するものである。

【0010】また、本発明は、半導体基板と、その主面に形成された電界効果トランジスタが形成された半導体領域との間に、前記半導体基板と半導体領域とを分離するように、その半導体領域とは反対導電型の半導体領域を設けるものである。

【0011】

【発明の実施の形態】以下の実施の形態においては便宜上その必要があるときは、複数のセクションまたは実施の形態に分割して説明するが、特に明示した場合を除き、それらはお互いに無関係なものではなく、一方は他方の一部または全部の変形例、詳細、補足説明等の関係にある。

【0012】また、以下の実施の形態において、要素の数等（個数、数値、量、範囲等を含む）に言及する場合、特に明示した場合および原理的に明らかに特定の数に限定される場合等を除き、その特定の数に限定されるものではなく、特定の数以上でも以下でも良い。

【0013】さらに、以下の実施の形態において、その構成要素（要素ステップ等も含む）は、特に明示した場合および原理的に明らかに必須であると考えられる場合等を除き、必ずしも必須のものではないことは言うまでもない。

【0014】同様に、以下の実施の形態において、構成要素等の形状、位置関係等に言及するときは、特に明示した場合および原理的に明らかにそうでないと考えられる場合等を除き、実質的にその形状等に近似または類似するもの等を含むものとする。このことは、上記数値および範囲についても同様である。

【0015】また、本実施の形態を説明するための全図において同一機能を有するものは同一の符号を付し、その繰り返しの説明は省略する。

【0016】また、本実施の形態においては、電界効果トランジスタを代表するMIS・FET (Metal Insulator Semiconductor Field Effect Transistor) をMISと略し、pチャネル型のMIS・FETをpMISと

略し、nチャネル型のMIS・FETをnMISと略す。

【0017】以下、本発明の実施の形態を図面に基いて詳細に説明する。

【0018】（実施の形態1）図1は、本発明の一実施の形態である半導体装置を構成する半導体チップ1Cのロジック回路部における要部断面図を示している。また、図2は、半導体チップ1Cを構成する半導体基板（以下、単に基板という）1Sの不純物濃度分布を示している。

【0019】基板1Sは、例えばp型のシリコン（Si）単結晶からなり、その主面（デバイス形成面）には、溝型の分離部（SGI: Shallow Groove Isolation）2が形成されている。溝型の分離部2は、例えば基板1Sの主面に分離用の溝を形成した後、その溝内を埋め込むように基板1Sの主面上に酸化シリコン膜（SiO₂）等のような絶縁膜を堆積し、さらにその絶縁膜を溝内にのみに残されるようにCMP（Chemical Mechanical Polishing）等によって研磨することにより形成されている。溝型の分離部2の深さ（基板1Sの主面から分離部2の底面までの距離）は、例えば0.2〜0.3μm程度である。この溝型の分離部2に囲まれた領域は活性領域（デバイス形成領域）となっている。この基板1Sにおいて活性領域にはp型の半導体領域PA（第1導電型の半導体領域）が形成されている。p型の半導体領域PAには、例えばホウ素（B）または二フッ化ホウ素（BF₃）が含有されている。ここでは、そのp型の半導体領域PA内に形成されたロジック回路用のnMISQnが例示されている。

【0020】nMISQnは、ソースおよびドレイン用の半導体領域3、3と、チャネル領域CHnと、ゲート絶縁膜4と、ゲート電極5とを有している。ソースおよびドレイン用の半導体領域3、3は、p型の半導体領域PA内に形成されるチャネル領域CHnを挟んでその両側に一対となるように配置されており、それぞれチャネル領域CHnの近傍に配置されたn型の半導体領域3aと、そのn型の半導体領域3a分を挟んでチャネル領域CHnから離れた位置に配置されたn型の半導体領域3bとを有している。n型の半導体領域3aおよびn型の半導体領域3bには、共に、例えばリン（P）またはヒ素（As）が含有されているが、n型の半導体領域3aは、いわゆるエクステンション領域とも呼ばれ、その不純物濃度の方が、n型の半導体領域3bのそれよりも低くなるように設定されている。すなわち、LD D（Lightly Doped Drain）構造とされている。

【0021】また、後述する本実施の形態1の構造では、p型の半導体領域PAが電気的にフローティング状態となり、しきい値電圧が低下するので、そのしきい値電圧の低下し過ぎを防ぐべく、チャネル領域CHnの不純物濃度を高めにすることで、しきい値電圧が通常より

も50mV～100mVほど高めになるように設定されている。ここでは、しきい値電圧を調整するために、チャネル領域CHnに、例えばホウ素が10keV程度のイオン打ち込みエネルギーで基板1Sの主面からイオン注入されている。

【0022】ゲート絶縁膜4は、例えば酸化シリコン(SiO₂)からなり、その厚さは、二酸化シリコン換算膜厚で、例えば2.5nm以下、一例としては1.5nm程度である。ただし、ゲート絶縁膜の材料は、これに限定されるものではなく種々変更可能であり、例えばゲート絶縁膜4を酸化シリコン膜(SiON)としても良い。すなわち、ゲート絶縁膜4と基板1Sとの界面に窒素を偏析させる構造としても良い。酸化シリコン膜は、酸化シリコン膜に比べて膜中における界面単位での発生を抑制したり、電子トラップを低減したりする効果が高いので、ゲート絶縁膜4のホットキャリア耐性を向上でき、絶縁性を向上させることができる。また、酸化シリコン膜は、酸化シリコン膜に比べて不純物が貫通し難いので、酸化シリコン膜を用いることにより、ゲート電極材料中の不純物が基板1S側に拡散すること

に起因するしきい値電圧の変動を抑制することができる。酸化シリコン膜を形成するには、例えば基板1SをNO、NO₂またはNH₃といった含窒素ガス雰囲気中で熱処理すれば良い。また、基板1Sの表面に酸化シリコンからなるゲート絶縁膜4を形成した後、基板1Sを上記した含窒素ガス雰囲気中で熱処理し、ゲート絶縁膜4と基板1Sとの界面に窒素を偏析させることによって、上記と同様の効果を得ることができる。また、ゲート絶縁膜4を、酸化シリコン膜上に窒化シリコン膜を積層した構造としても良い。さらに、ゲート絶縁膜4を、例えばHfO₂(誘電率ε=20.6)、ZrO₂(ε=24.7)、Al₂O₃(ε=8.4)、Y₂O₃(ε=14)やHfSiO₄、ZrSiO₄(ε=19.4)等のような高誘電体膜からなる絶縁膜で形成しても良い。

【0023】上記ゲート電極5は、例えば低抵抗多結晶シリコンからなる。ただし、これに限定されるものではなく種々変更可能であり、例えば低抵抗多結晶シリコン膜上にコバルトシリサイド(CoSi₂)等のようなシリサイド層を設けた、いわゆるポリサイドゲート電極構造や低抵抗多結晶シリコン膜上に窒化タンゲステン(WN)等のようなバリア金属層を介してタンゲステン等のような金属膜を設けた、いわゆるポリ金属ゲート電極構造としても良い。ゲート電極5の側面には、LDD構造を形成すべく、例えば酸化シリコン膜からなるサイドウォール7が形成されている。また、ゲート長は、ゲート絶縁膜4の厚さが2.5nm程度であれば0.14μm程度、ゲート絶縁膜4の厚さが1.5nm程度であれば0.08μm程度である。また、nMISQnが形成されたロジック回路領域の高電位側の電源電圧は、例えば1.5V～0.7V程度であり、周辺回路領域の

高電位側の電源電圧よりも相対的に低い。なお、半導体チップ1Cにおいて、周辺回路領域(例えば入力回路、出力回路および入出力双方向回路)の高電位側の電源電圧は、例えば3.0Vまたは3.3V程度である。

【0024】このようなnMISQnは、基板1Sの主面に堆積された層間絶縁膜8によって覆われている。層間絶縁膜8は、例えば酸化シリコン膜からなり、その上面には、第1層配線9が形成されている。第1層配線9は、例えばアルミニウムまたはアルミニウム合金からなり、層間絶縁膜8に穿孔されたコンタクトホール10を通じてソースおよびドレイン用の半導体領域3と電気的に接続されている。

【0025】ところで、本発明者らは、部分空乏型のSOI基板を用いた半導体装置の開発中に、部分空乏型のSOI基板を用いた場合において、通常の基板を用いた場合に対するメリットの多くが、基板フローティングによる駆動電流の増加と、接合容量の低減とにあることを見出した。そこで、そのようなメリットを生じさせるような構造を通常の基板で実現するために、次のような構成を採用した。

【0026】すなわち、本実施の形態1においては、nMISQnが形成されたp型の半導体領域PAとその下層の基板1Sとの間にnウエルNWL(第2導電型の半導体領域)が設けられている。このnウエルNWLの不純物分布は、基板1Sとp型の半導体領域PAおよびチャネル領域CHnと基板1Sとが電気的に接続されないように、基板1Sの主面からの深さにおいて、溝型の分離部2の底部よりは若干浅い位置であって、p型の半導体領域PAのピーク位置よりは深い位置から溝型の分離部2の底部よりは若干深い位置に広がって分布されるように形成されている。すなわち、本実施の形態1においては、nMISQnのチャネル領域CHnおよびp型の半導体領域PAと基板1Sとが、nウエルNWLと基板1Sとのpn接合によって電気的に分離されている。ここでは、nMISQnのソースおよびドレイン用の半導体領域3に対して電源電圧を印加した状態で、チャネル領域CHn(p型の半導体領域PA)の接合間の空乏層幅と、チャネル領域CHn(p型の半導体領域PA)とnウエルNWLとの間に広がる空乏層によって、n型の半導体領域3bと、nウエルNWLとが接続されないようにする必要がある。すなわち、図1中の距離x1は、上記の空乏層幅の和よりも大きい必要がある。また、nウエルNWL自体の幅x2もチャネル領域CHn(p型の半導体領域PA)との間の空乏層、基板1Sとの間の空乏層によって消滅しないようにする必要がある。すなわち、幅x2は、上記空乏層の幅の和よりも大きい必要がある。このようなnウエルNWLは、上記溝型の分離部2を形成した後、例えばリンを450keV程度のイオン打ち込みエネルギーで基板1Sの主面からイオン注入することにより形成されている。なお、nウ

エルNWLのピーク位置での不純物濃度は、図2に示すように、例えば $10^8/\text{cm}^3$ が若干それより低い程度である。

【0027】このようなnウエルNWLを設けたことにより、半導体装置の性能上においてSOI基板を用いた場合と同様の効果を得ることができる。すなわち、導通時には、ゲート電極5と、チャネル領域CHn（p型の半導体領域PA）との容量結合によるチャネル領域CHn（p型の半導体領域PA）の電位の上昇と、ドレイン電流が流れインパクトイオン化によるホールが発生することによるチャネル領域CHn（p型の半導体領域PA）の電位の上昇とによって、nMISQnのしきい値電圧が下がり電流が増加する。図3は、本実施の形態1のnMISQnと、nウエル分離構造を有しない通常の基板に形成されたnMISとのドレイン電流のゲート電圧依存性を示している。本実施の形態1では、チャネル領域CHn（p型の半導体領域PA）が電気的に絶縁されているためにゲート電圧印加時には、しきい値電圧が低下し、ドレイン電流を増加させることができる。また、ソースおよびドレイン用の半導体領域3と基板1Sとの間の接合容量は、n型の半導体領域3bとチャネル領域CHn（p型の半導体領域PA）との接合容量と、チャネル領域CHn（p型の半導体領域PA）とnウエルNWLとの接合容量と、nウエルNWLと基板1Sとの接合容量とが直列接続された状態となるため、nウエルNWLを設けない場合の約1/3に低減することができる。これらにより、このトランジスタを含む回路の動作速度を向上させることが可能となる。

【0028】また、チャネル領域CHn（p型の半導体領域PA）と基板1Sとが絶縁体で完全に分離されるわけではなく、nウエルNWLで分離される構造とされており、SOI基板に比べて熱を逃がし易い構造となっており、熱抵抗の増大を大幅に低減することができる。このため、半導体装置の動作信頼性を向上させることができる。また、パッケージ自体の冷却構造または半導体装置を冷却するための冷却装置や冷却機構を簡略化できる。

【0029】また、SOI基板に比べて結晶欠陥を低減できる。このため、半導体装置の歩留まりおよび信頼性を向上させることができる。

【0030】また、基板電位の上昇の制御に際しても、チャネル領域CHnの下にpn接合のリーク電流を制御することにより、比較的容易に制御することができる。すなわち、基板フローティングの制御性を向上させることができる。このため、回路設計を容易にすることができる。

【0031】また、nウエルNWLを設けているだけで基本的に通常の基板構造なので、高価なSOI基板を用いた場合に比べて半導体装置のコストを低減することができる。

【0032】（実施の形態2）本実施の形態2においては、CMIS（Complementary MIS）回路を有する半導体装置に本発明を適用した場合について説明する。

【0033】図4は、本発明の他の実施の形態である半導体装置を構成する半導体チップ1Cのロジック回路部を構成するCMIS回路部の要部断面図を示している。

【0034】nMISQnの形成領域の縦構造は、前記実施の形態1と同じなので説明を省略し、ここでは、pMISQpの形成領域において基板1Sの活性領域には、n型の半導体領域NA（第2導電型の半導体領域）が形成されており、このn型の半導体領域NA内にpMISQpが形成されている。このn型の半導体領域NAには、例えばリン（P）またはヒ素（As）が含有されている。

【0035】pMISQpは、ソースおよびドレイン用の半導体領域11、11と、チャネル領域CHpと、ゲート絶縁膜4と、ゲート電極5とを有している。ソースおよびドレイン用の半導体領域11、11は、チャネル領域CHpを挟んで一対となるように配置されており、それぞれチャネル領域CHpの近傍に配置されたp型の半導体領域11aと、そのp型の半導体領域11a分を挟んでチャネル領域CHpから離隔した位置に配置されたp型の半導体領域11bとを有している。p型の半導体領域11aおよびp型の半導体領域11bには、共に、例えばボウ素（B）または二フッ化ボウ素（BF₂）が含有されているが、p型の半導体領域11aは、いわゆるエクステンション領域とも呼ばれ、その不純物濃度の方が、p型の半導体領域11bのそれよりも低くなるように設定されている。すなわち、LDD構造とされている。

【0036】そして、本実施の形態2においては、pMISQpが形成されたn型の半導体領域NAとその下層の基板1Sとの間にpウエルPWL（第1導電型の半導体領域）が設けられている。すなわち、本実施の形態2においては、pMISQpのチャネル領域CHp（n型の半導体領域NA）と基板1Sとが、pウエルPWLとn型の半導体領域NAとのpn接合によって電気的に分離されている。このpウエルPWLの不純物分布や形成状態は、前記nウエルNWLと同じなので説明を省略する。このようなpウエルPWLは、上記導電型の分離部2を形成した後、例えばボウ素を160keV程度のイオン打ち込みエネルギーで基板1Sの正面からイオン注入することにより形成されている。なお、pウエルPWLのピーク位置での不純物濃度は、nウエルNWLと同じ程度である。pMISQpのチャネル領域CHpは、所望のしきい値（従来の構造の場合よりも50mV～100mV程度エンハンス側）となるように、例えばリンを20keV程度基板1Sの正面側からイオン注入することによって形成されている。これ以外は、前記実施の形態1と同

じなので説明を省略する。

【0037】このように本実施の形態2によれば、前記実施の形態1で得られた効果の他に、以下の効果を得ることができる。すなわち、pMISQpでも、上記nMISQnと同様の効果を得ることができる。したがって、CMIS回路で構成されるロジック回路を有する半導体装置の動作速度（性能）を向上させることができる。

【0038】（実施の形態3）前記実施の形態1、2のMISの縦構造においては、上記のように動作速度を向上させることはできるが、MISのしきい値電圧が動作領域内で変動し不安定になる。そこで、本実施の形態3においては、同一の基板15に形成されるMISであっても、前記MISの縦構造を採用するものと、採用しないものとの作り分けを行った。すなわち、回路に必要とされる電気的特性に応じて前記実施の形態1、2で説明したMISの縦構造と、通常のMISの縦構造を使い分けた。具体的には、しきい値電圧がある程度変動しても動作に支障をきたさない回路を構成するMISには前記MISの縦構造を採用し、しきい値電圧が変動すると動作に支障をきたす回路を構成するMISには前記MISの縦構造を採用せず一般的なMISの縦構造とした。例えばデジタル回路を構成するMISには、前記実施の形態1、2で説明したMISの縦構造を採用した。また、例えば高い動作精度を必要とするアナログ回路、入出力回路またはメモリ回路のメモリセルやセンスアンプ回路等（以下、単にアナログ回路等という）を構成するMISは、前記MISの縦構造を採用せず、通常のMISの縦構造を採用した。メモリセルは、デジタル回路ではあるが、微小な信号（電荷）を読み出したり、書き込んだりするので、メモリセルを構成するMIS・FETのしきい値電圧が変動するとデータ処理に支障をきたすことから、通常のMISの縦構造を採用することが好ましい。また、本発明者らの検討によれば、MISの動作電圧（高電位側の電源電圧）の観点で考慮した場合、その動作電圧が、例えば1.5V以下ならば、前記実施の形態1、2で説明したMISの縦構造を採用することが好ましい。一方、MISの動作電圧が、例えば1.5Vよりも高いならば、上記通常のMISの縦構造を採用することが好ましい。

【0039】図6は、本実施の形態3の半導体装置の要部断面図の一例を示している。領域A1は、ロジック回路（デジタル回路）を構成するnMISQnおよびpMISQp（第1の電界効果トランジスタ）の配置領域を示している。この領域A1では、前記実施の形態1、2で説明したMISの縦構造が採用されている。

【0040】一方、領域A2は、上記アナログ回路、入出力回路、メモリ回路のメモリセルやセンスアンプ回路等のようなしきい値電圧が変動すると支障をきたす回路を構成するnMISQn1、Qp1（第2の電界効果トラ

ンジスタ）の配置領域を示している。この領域A2では、上記通常のMISの縦構造が採用されている。すなわち、nMISQn1は、pウェルPWL内に形成され、pMISQp1は、nウェルNWL内に形成されている。領域A2のpウェルPWLおよびnウェルNWLの構造は、領域A1のpウェルPWLおよびnウェルNWLの構造と同じである。この領域A2のnMISQn1およびpMISQp1においても、チャネル領域CHn1、CHp1へのチャネルイオン注入が行われ、しきい値電圧の調整が行われている。

【0041】このように、本実施の形態3においては、前記実施の形態1、2で得られた効果の他に以下の効果を得ることが可能となる。

【0042】すなわち、ロジック回路のMISには、前記実施の形態1、2で説明したMISの縦構造を採用し、アナログ回路等のMISには、通常のMISの縦構造を採用したことにより、ロジック回路における動作速度の向上と、アナログ回路等における動作信頼性の向上とを両立することが可能となる。

【0043】（実施の形態4）前記実施の形態2のCMIS回路の構造では、ゲート電圧印加時の基板電位の上昇が大きすぎる場合がある。この場合には、図6に示すように、p型の半導体領域PAとnウェルNWLとの接合周辺に、例えばアルゴン（Ar）またはゲルマニウム（Ge）等のような不純物イオンをイオン注入することにより、結晶欠陥12を形成する。これにより、p型の半導体領域PAとnウェルNWLとのpn接合の空乏層内に適度な再結合を生じさせ、リーク電流を流し、これを制御することができるので、p型の半導体領域PAの電位の上昇を抑えることができる。したがって、nMISQnのしきい値電圧の駆動制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。なお、pMISQpのn型の半導体領域のインパクトイオン化で発生した電子は、ソース用のp型の半導体領域11b（高電位側の電源配線）に流れ、pMISQp側では再結合中心を形成しても基板電位のフローティング抑制に効果が生じないので、pMISQp側には結晶欠陥を設けていない。

【0044】（実施の形態5）本実施の形態5は、前記実施の形態4で説明したのと同じ目的を達成するための変形例を説明するものである。すなわち、基板電位の上昇を抑制することを目的として、図7に示すように、p型の半導体領域PAの下部（p型の半導体領域PAとnウェルNWLとの間）に高不純物濃度のp型の半導体領域13Pを設ける。p型の半導体領域13Pは、p型の半導体領域PAおよびnウェルNWLの両方に接している。このようなp型の半導体領域13Pを設けることにより、nMISQnのソースおよびドレイン用の半導体領域3と、p型の半導体領域PAとで形成される寄生バイポーラトランジスタのベース領域に相当する領域

域の不純物濃度を高くすることができるので、その寄生バイポーラトランジスタの電流増幅率を低減することができる。その結果、基板電位の上昇を抑制することができる。したがって、nMISQnのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。

【0045】また、本実施の形態5においては、基板電位の上昇を抑制することを目的として、n型の半導体領域NAの下部（n型の半導体領域NAとpウェルPWLとの間）に高不純物濃度のn型の半導体領域13Nを設ける。n型の半導体領域13Nは、n型の半導体領域NAおよびpウェルPWLの両方に接している。このようなn型の半導体領域13Nを設けることにより、上記のnMISQnと同様の理由からpMISQpのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。

【0046】（実施の形態6）本実施の形態6は、前記実施の形態4、5で説明したのと同じ目的を達成するための変形例を説明するものである。すなわち、基板電位の上昇を抑制することを目的として、図8に示すように、nMISQnの形成領域において、p型の半導体領域PAの下部に、これに接した状態でp型の半導体領域13を設け、さらにその下部に、これに接した状態でn型の半導体領域14を設け、その下部に、これに接した状態で上記nウェルNWLが設けられている。これにより、p'n'の高不純物濃度の接合を形成することができるので、ダイオードのトンネル電流を増大させ、再結合を生じさせることができるので、p型の半導体領域PAの基板電位の上昇をさらに抑制することができる。したがって、nMISQnのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。なお、pMISQp側には、前記実施の形態4、5で説明したのと同じ理由から、n型の半導体領域NAの下部にn型の半導体領域およびp型の半導体領域を設けていない。

【0047】以上、本発明者によってなされた発明を実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変変可能であることはいふまでもない。

【0048】以上の説明では主として本発明者によってなされた発明をその背景となった利用分野であるCMIS回路を有する半導体装置に適用した場合について主に説明したが、それに限定されるものではなく、例えばDRAM（Dynamic Random Access Memory）、SRAM（Static Random Access Memory）またはフラッシュメモリ（EEPROM；Electric Erasable Programmable Read Only Memory）等のようなメモリ回路を有する半導体装置、マイクロプロセッサ等の論理回路を有する半導体装置あるいは上記メモリ回路と論理回路とを

同一半導体基板に設けている混成型の半導体装置にも適用できる。

【0049】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下の通りである。

(1)半導体基板と、その主面に形成された電界効果トランジスタのチャネルが形成される半導体領域とをpn接合によって分離することにより、半導体装置の性能を向上させることが可能となる。

(2)半導体基板と、その主面に形成された電界効果トランジスタのチャネルが形成される半導体領域とをpn接合によって分離することにより、比較的欠陥が多く高価なSOI構造を用いず、通常の基板構造を用いて半導体装置を構成することができるので、半導体装置のコストを低減することが可能となる。

【図面の簡単な説明】

【図1】本発明の一実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図2】図1の半導体装置の半導体基板における不純物濃度分布を示すグラフ図である。

【図3】図1の半導体装置の電界効果トランジスタと通常の半導体基板に形成された電界効果トランジスタとのドレイン電流のゲート電圧依存性を示すグラフ図である。

【図4】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図5】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図6】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図7】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図8】本発明のさらに他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【符号の説明】

- 1 C 半導体チップ
- 1 S 半導体基板
- 2 分離部
- 3 半導体領域
- 3 a n型の半導体領域
- 3 b n型の半導体領域
- 4 ゲート絶縁膜
- 5 ゲート電極
- 7 サイドウォール
- 8 側面絶縁膜
- 9 第1層配線
- 10 コンタクトホール
- 11 半導体領域
- 11 a p型の半導体領域

11b p型の半導体領域
 12 結晶欠陥
 13P p型の半導体領域
 13N n型の半導体領域
 14 n型の半導体領域
 PA p型の半導体領域 (第1導電型の半導体領域)
 NWL nウエル (第2導電型の半導体領域)
 NA n型の半導体領域 (第2導電型の半導体領域)
 PWL pウエル (第1導電型の半導体領域)
 Qp pチャネル型のMIS・FET (第1の電界効果 *10

*トランジスタ)

Qn nチャネル型のMIS・FET (第1の電界効果
 トランジスタ)

Qp1 pチャネル型のMIS・FET (第2の電界効果
 トランジスタ)

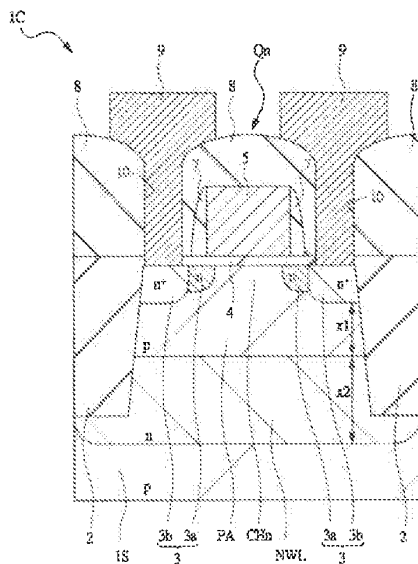
Qn1 nチャネル型のMIS・FET (第2の電界効果
 トランジスタ)

CHn, CHn1 チャネル領域

CHp, CHp1 チャネル領域

【図1】

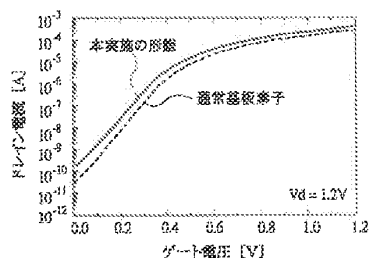
図 1



1S: 半導体基板
 NWL: nウエル
 Qn: nチャネル型のMIS・FET
 PA: p型の半導体領域

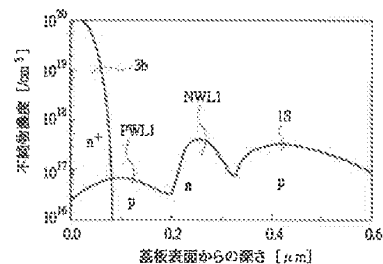
【図3】

図 3



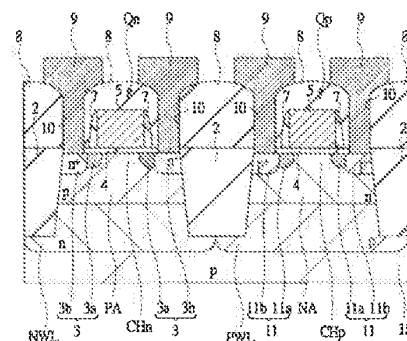
【図2】

図 2



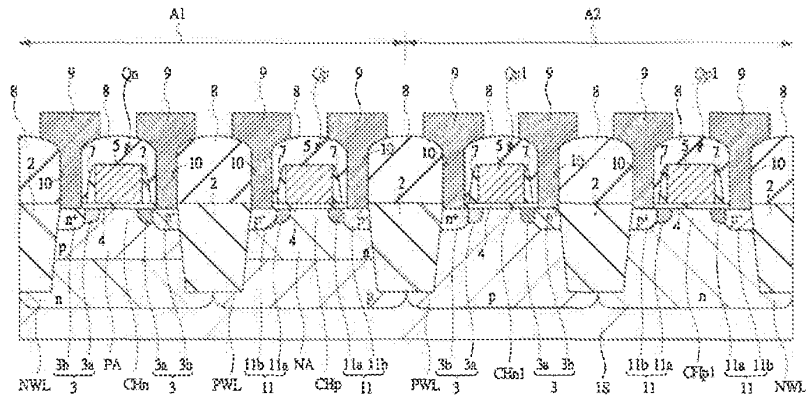
【図4】

図 4



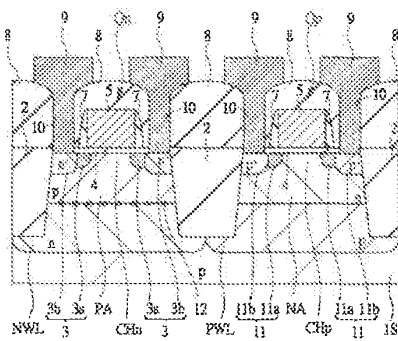
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図 5



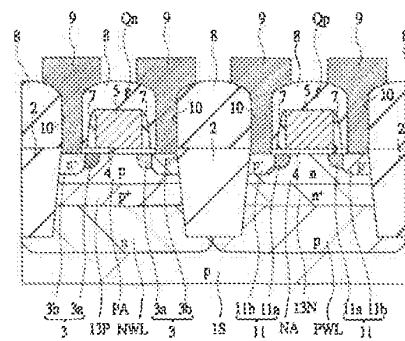
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図 6

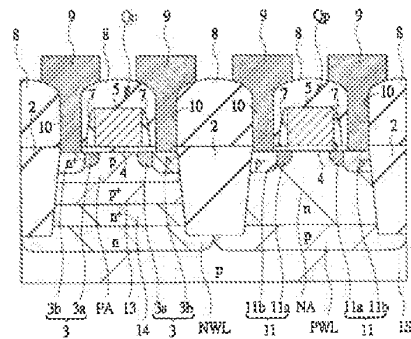


【図7】

図 7



特開2003-51551



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F ターム(参考) 5F032 AA35 AA44 AB01 AB03 CA01
                  CA03 CA17 CA20 DA60 DA63
5F048 AA01 AA03 AA04 AA07 AB01
                  AB03 BA01 BA13 BB05 BB08
                  BB09 BB11 BB12 BB13 BB14
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                  BH03 DA25
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                  BD13 BF01 BF04 BF11 BF18
                  BF20 BF21 BF25 BF27 BG06
                  BG12 BH15 BH50 BJ01 BJ05
                  BK13 CB04 CB08 CB10 CD02

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Electronic Acknowledgement Receipt	
EFS ID:	43081214
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison/Joselyn Rodriguez
Filer Authorized By:	Gregory Michael Howison
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	30-JUN-2021
Filing Date:	27-JUL-2020
Time Stamp:	18:55:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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1	Information Disclosure Statement (IDS) Form (SB08)	GRT35294IDS.pdf	1055732 cc674ed0f5a92e99f49716a1e1cb55e262dc a969	no	10

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

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Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison/Joselyn Rodriguez
Filer Authorized By:	Gregory Michael Howison
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	30-JUN-2021
Filing Date:	27-JUL-2020
Time Stamp:	18:56:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/947,294
Filing Date	2020-07-27
First Named Inventor	R Mohan Rao G
Title	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
Art Unit	
Examiner Name	
Attorney Docket Number	GRTD60-35294

SIGNATURE of Applicant or Patent Practitioner

Signature	/GregoryMHowison#30646/	Date (Optional)	2021-07-15
Name	Gregory M. Howison	Registration Number	30646
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐

*Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

16/947,294

2020-07-27

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

25883

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number: 25883

OR



Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Greenthread, LLC



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

2021-07-15

Name

Phil John

Title

President

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.



Total of

forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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POWER OF ATTORNEY BY APPLICANT

No more than ten (10) patent practitioners total may be appointed as set forth below by name and registration number. This page need not be submitted if appointing the Patent Practitioner(s) associated with a Customer Number (see form PTO/AIA/82B):

Name	Registration Number

Electronic Acknowledgement Receipt	
EFS ID:	43300849
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison
Filer Authorized By:	
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	20-JUL-2021
Filing Date:	27-JUL-2020
Time Stamp:	17:44:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	GRTDREVPOA.pdf	2993357	no	3
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Warnings:

Information:	
Total Files Size (in bytes):	2993357
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7

CONFIRMATION NO. 6907

POWER OF ATTORNEY NOTICE

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380



OC000000127152011

Date Mailed: 07/23/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/20/2021.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/ibrahim/



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294

CONFIRMATION NO. 6907

POA ACCEPTANCE LETTER

25883
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380



Date Mailed: 07/23/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/20/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sibrahim/



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

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MUNCK WILSON MANDALA L.L.P.
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER

ARORA, AJAY

ART UNIT

PAPER NUMBER

2892

DATE MAILED: 08/11/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907

TITLE OF INVENTION: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	11/12/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25883 7590 08/11/2021
MUNCK WILSON MANDALA L.L.P.
P.O. Drawer 800889
DALLAS, TX 75380

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907

TITLE OF INVENTION: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	11/12/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARORA, AJAY	2892	257-025000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907
25883	7590	08/11/2021	EXAMINER	
MUNCK WILSON MANDALA L.L.P.			ARORA, AJAY	
P.O. Drawer 800889			ART UNIT	
DALLAS, TX 75380			PAPER NUMBER	
			2892	
DATE MAILED: 08/11/2021				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/947,294	Applicant(s) Rao, G.R. Mohan	
	Examiner AJAY ARORA	Art Unit 2892	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 7/27/2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-44 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>9/29/2020 & 6/30/2021</u> .	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/AJAY ARORA/ Primary Examiner, Art Unit 2892	
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DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Reasons for Allowance

2. Claims 1-44 are allowed. The following is an examiner's statement of reasons for allowance:

Claims 1-20 are allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of the base claim 1 that requires "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions" (see last 5 lines).

The closest reference is Hong (US 2007/0045682), hereinafter Hong. More specifically, regarding claim 17, Hong (refer to Figures 4A-4D and 5A-5C) teaches a semiconductor device, comprising:

a substrate (312 – see para 29) of a first doping type (i.e. parts 312 and 21 of the substrate have n-type doping, see para 29) at a first doping level having a surface;

a first region (311, which includes wells such as 21, 22, 5, 2) disposed adjacent the first surface,

a second active region (such as source/drain region 2, see para 40; or 2 or 5 or 22 of pixel cell formed in an adjacent region separated by shallow trench isolation 37 – see para 30) separate from the first region disposed adjacent to the first active region and within which transistors (406, 407) may be formed;

at least a portion of at least one of the first and second regions having at least one graded dopant concentration (350 – see para 24, last 3 sentences; also see Figure 5C and para 29) to aid carrier movement (para 26).

However, the first region is not an “active” region and the structure does not show that the graded dopant region is to “aid carrier movement from the surface to the area of the substrate where there are no active regions”. Further, it is not obvious to modify Hong as changing first region and second region as above would change the intended function of the device.

Similarly, claims 21-38 are allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of base claim 21 that requires “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions” (see last 5 lines). Again, the closest reference is Hong.

Similarly, claims 39-40 are allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of base claim 30 that requires “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region” (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 41 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of “at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region” (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 42 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of “at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region” (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 43 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of “at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region” (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 44 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of “a second static

unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions” (see last 3 lines). Again, the closest reference is Hong.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on 9 AM - 5 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Thao X. Le can be reached on 5712721708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair->

my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AJAY ARORA/
Primary Examiner, Art Unit 2892

<i>Notice of References Cited</i>	Application/Control No. 16/947,294		Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan	
	Examiner AJAY ARORA		Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20070045682-A1	03-2007	Hong; Sungkwon C.	H01L27/14689	257/292
*	B	US-20140034997-A1	02-2014	RAHIMO; Munaf	H01L29/861	257/139
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan
	Examiner AJAY ARORA	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM			DATE							
Final	Original	07/31/2021								
	1	=								
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	3	=								
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	40	=								
	41	=								
	42	=								

<i>Index of Claims</i> 	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan
	Examiner AJAY ARORA	Art Unit 2892

CLAIM		DATE								
Final	Original	07/31/2021								
	43	=								
	44	=								

<i>Search Notes</i> 	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan
	Examiner AJAY ARORA	Art Unit 2892

CPC - Searched*		
Symbol	Date	Examiner
H01L 29/1095	07/31/2021	AKA

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

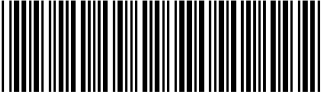
US Classification - Searched*			
Class	Subclass	Date	Examiner
257	25	07/31/2021	AKA

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor search	07/31/2021	AKA
Assignee search	07/31/2021	AKA
All references for parent applications considered	07/31/2021	AKA
.clm. interference search	07/31/2021	AKA
EAST search history report	07/31/2021	AKA

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	29/1095	07/31/2021	AKA
257	25	07/31/2021	AKA

/AJAY ARORA/ Primary Examiner, Art Unit 2892	
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Issue Classification 	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan
	Examiner AJAY ARORA	Art Unit 2892

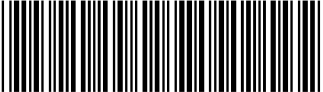
CPC						
Symbol					Type	Version
H01L	/	29	/	1095	F	2013-01-01
H01L	/	27	/	11524	I	2013-01-01
H01L	/	27	/	14643	I	2013-01-01
H01L	/	27	/	11521	I	2013-01-01
H01L	/	29	/	7395	I	2013-01-01
H01L	/	29	/	36	I	2013-01-01
H01L	/	27	/	0214	A	2013-01-01
H01L	/	27	/	10844	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

NONE (Assistant Examiner)		Total Claims Allowed: 44	
/AJAY ARORA/ Primary Examiner, Art Unit 2892 (Primary Examiner)		O.G. Print Claim(s) 1	O.G. Print Figure 5B

U.S. Patent and Trademark Office

Part of Paper No.: 20210731

Issue Classification 	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan
	Examiner AJAY ARORA	Art Unit 2892

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L29/10		29	10
NON-CLAIMED			

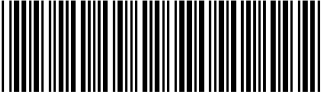
US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
257	25

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	44	
/AJAY ARORA/ Primary Examiner, Art Unit 2892	31 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office

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Issue Classification 	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan
	Examiner AJAY ARORA	Art Unit 2892

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	2		11		20		29		38						
	3		12		21		30		39						
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	7		16		25		34		43						
	8		17		26		35		44						
	9		18		27		36								

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 44	
/AJAY ARORA/ Primary Examiner, Art Unit 2892 (Primary Examiner) _____ (Date) 31 July 2021		O.G. Print Claim(s) 1	O.G. Print Figure 5B

U.S. Patent and Trademark Office

Part of Paper No.: 20210731

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	16/947,294	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:23
L2	3	16/717,950	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:23
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L18	25,665	H01L27/11521.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/31 19:30