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for the VLSI Era

Volume 1 - Process Technology

Second Edition

S. Wolf and R.N. Tauber

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PROCESS TECHNOLOGY

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STANLEY WOLF Ph.D.

RICHARD N. TAUBER Ph.D.

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PREFACE
SECOND EDITION

This second edition of *Silicon Processing for the VLSI Era: Volume 1 - Process Technology* follows the 1986 publication of the first edition. More than 20,000 volumes of that version were sold, attesting to its widespread acceptance throughout the microelectronics community. Professionals and students of this vibrant technology should find the new edition equally useful.

Many new processes and materials have been incorporated into IC fabrication in the fifteen years since the first edition was written. The new materials and processes covered in the second edition include: 300-mm wafers, DUV lithography, chemically-amplified resists, high-energy ion implantation, high-density plasma sources for CVD and etching, step-and-scan aligners, chemical-mechanical polishing, dual-damascene interconnects, copper metallization, and low-*k* dielectrics. Altogether the material of our book comprises more than 900 pages, 600 illustrations, and 1500 references (with over half of the citations from 1996 to 1999). It also includes those topics from the first edition that are still in use.

The effort of writing and producing this new edition was predominantly carried out by Stanley Wolf. He revised eight chapters (Chaps. 1, 2, 3, 4, 6, 11, 12, and 14), and entirely wrote the five new ones (Chaps. 5, 13, 15, 16, and 17). Three chapters were revised by Richard N. Tauber (Chaps. 7, 8, and 9), and Michael Current revised Chap. 10.

Valuable input to Stanley Wolf was also provided by many persons. Foremost of these were R. N. Tauber and C. A. Wolf. They each carefully read the entire manuscript and offered extensive editorial assistance (Tauber: primarily technical, and Wolf: grammatical). Others who provided important technical assistance and critical reviews were: Jerry Healey, Richard Cohen, Chris Mack, Bruce Smith, Robert Simonton, Dennis Hess, Moshe Preil, Wilbur Krussell, Bob Climo, Kathleen Perry, Peter Loewenhardt, and Donald Smith. Roy Montebin, of Vox Mundi, designed the book's cover.

Stanley Wolf, Ph.D.
Professor Emeritus, Department of Electrical Engineering, CSULB

I would also like to acknowledge the support of my former colleagues at Applied Materials for their helpful discussions and for kindly providing some of the figures used herein: Chris Fulmer, Gary Miner, Gary Xing, Kelly Truman, Majeed Foad, Norma Riley, Parvin Katebi, and Satheesh Kuppurao.

In addition, I would like to thank the following persons for providing additional background material and figures used in this textbook: Al Geise - SVG/Thermco; Clyve Hayzelden - KLA/Tencor; Gerhardt Kneissal - ADE; Jim Cable - Peregrine Semiconductor; Pat Shanks - Semitool; Sang-Shin Kim - GaSonics; and Terry Ma - Avant!/TMA.

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PREFACE TO THE FIRST EDITION

SILICON PROCESSING FOR THE VLSI ERA is a text designed to provide a comprehensive and up-to-date treatment of this important and rapidly changing field. The text consists of three volumes of which this book is the first, subtitled, *Process Technology*. Volume 2, subtitled, *Process Integration* was published in 1990. Volume 3, subtitled *The Submicron MOSFET* was published in 1995. In this first volume, the individual processes employed in the fabrication of silicon VLSI circuits are covered in depth (e.g., epitaxial growth, chemical vapor and physical vapor deposition of amorphous and polycrystalline films, thermal oxidation of silicon, diffusion, ion implantation, microlithography, and etching processes). In addition, chapters are also provided on technical subjects that are common to many of the individual processes, such as vacuum technology, the properties of thin films, and CMOS process integration. The topics covered in the book are listed in more detail in the Table of Contents.

The purpose of writing this text was to provide professionals involved in the microelectronics industry with a single source that offers a complete overview of the technology associated with the manufacture of silicon integrated circuits. Most other texts on the subject are available only in the form of specialized books (i.e., that treat just a small subset of all of the processes), or in the form of edited volumes (i.e., books in which a group of authors each contribute a small portion of the contents). Such edited volumes typically suffer from a lack of unity in the presented material from chapter-to-chapter, as well as an uneven writing style and level of presentation. In addition, in multi-disciplinary fields (such as microelectronic fabrication), it is difficult for most readers to follow technical arguments in such books, especially if the information is presented without defining each technical "buzzword" as it is first introduced. In our book, we hope to overcome such drawbacks by treating the subject of VLSI fabrication from a unified and more pedagogical viewpoint, and by being careful to define technical terms when they are first used. The result is intended to be a user friendly book for workers who have come to the semiconductor industry after having been trained in but one of the many traditional technical disciplines.

An important technical breakthrough has occurred in book publishing that the authors also felt could be exploited in creating a unique book on silicon processing. That is, revolutionary electronic publishing techniques became available in the mid-1980's, and these can cut the time required to produce a published book from a finished manuscript. The task traditionally took 15-18 months, but can be now reduced to less than 4 months. If traditional techniques are used to produce books in such fast-breaking fields as VLSI fabrication, these books automatically possess a built-in obsolescence, even upon being first published. The authors took advantage of these rapid production techniques, and were able to successfully meet the reduced production-time schedule. As a result, it was possible to include information contained in technical journals and conferences within four months of the book's publication date. Most other books on silicon processing undergo such 15-18 month production cycles. This is the first book on the subject where such time-delay effects have been eliminated from the production process!

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Written for the professional, the book belongs on the shelf of workers in several microelectronic disciplines. *Microelectronic fabrication engineers* who seek to develop a more complete perspective of the subject, or who are new to the field, will find it invaluable. *integrated circuit design enegineers, test engineers,* and *integrated circuit equipment engineers,* who must understand VLSI processing issues to effectively interface with the fabrication environment, will also find it a uniquely useful reference. The book should also be very suitable as a text for graduate-level courses on silicon processing techniques, offered to students of electrical engineering, applied physics, and materials science. Problems are included at the end of each chapter to assist readers in gauging how well they have assimilated the material in the text.

The book was an outgrowth of an intensive seminar of the same title as the book, conducted by the authors through the Engineering Extension of the University of California, Berkeley. In the fifteen years that this course has been conducted (1984-1999), several thousand engineers and managers from more than 100 companies have enrolled in it. Its fine reputation is attested to by the fact that many firms have sent participants to subsequent courses, presumably based on the recommendations of earlier participants.

In setting out to create a comprehensive text on VLSI fabrication, the authors each contributed a set of unique and complementary skills to the project. Professor Wolf"s proficiency as a teacher and writer were utilized to produce a clearly written and logically organized book. Some of this expertise was gained in authoring an earlier best-selling text *Electronic Measurements and Laboratory Practice,* Prentice-Hall, 1973. Dr. Tauber brought a technical expertise acquired from his long involvement in the semiconductor industry. He used this background to insure that the most important topics of VLSI fabrication were addressed, and that the information was up-to-date and presented in a technically correct fashion. Note that for over twenty-five years, Dr. Tauber has held positions at Bell Telephone Laboratories, Xerox, Hughes Aircraft Company Microelectronics Research Center, the Microelectronics Center of TRW, and Applied Materials. The labor of the writing effort was divided between the authors in the following manner: Professor Wolf was responsible for writing Chapters 1, 2, 3, 9, 10, 12, 13, 15, 16, 17, and 18, and Dr. Tauber undertook the writing of Chapters 4, 5, 7, 8, 11, and 14. Material for Chap. 6 was jointly contributed by Andrew R. Coulson and Dr. Tauber.

A book of this length and diversity would not have been possible without the indirect and direct assistance of many other workers. To begin with, virtually all of the information presented in this text is based on the research efforts of a countless number of scientists and engineers. Their contributions are recognized to a small degree by citing some of their articles in the references given at the end of each chapter. The direct help came in a variety of forms, and was generously provided by many people. The text is a much better work as a result of this aid, and the authors express heartfelt thanks to those who gave of their time, energy, and intellect.

Each of the chapters was reviewed after the writing was completed. The engineers and scientists who participated in this review were numerous. Special thanks are given to Warren Flack, Stephen Franz, Kenneth Tokunaga, and Simon Prussin for their critical reviews. Superlative computer support and access to computer resources was generously made available by Donald E. Carlile, Harry T. Hayes, and Dale Lambertson of the Personal Computer Support Section of the Electronic Systems Group of TRW. Henry Nicholas was a computer expert and friend who lit the fire of inspiration that led to the undertaking of the project. The management

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of the Electronics Systems Group and the Microelectronics Center of TRW are warmly thanked for providing a supportive environment, conducive to producing such an intensive technical project. They made available technical literature and other resources to the authors, especially S. Wolf, who was able to avail himself of this generosity while writing during a Sabbatical leave from his teaching duties at California State University, Long Beach. Roy Montibon and Donald Strout of New Archetype Publishing, Inc., Los Angeles, CA designed the cover. Finally, we wish to thank Shirley Rome, Carrol Ann Wolf, and Barbara Tauber for typing the manuscript.

Stanley Wolf and Richard N. Tauber

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PROLOGUE

Since the invention of the first integrated circuit in 1960, there has been an ever-increasing density of devices manufacturable on semiconductor substrates. Silicon technology has remained the dominant force in integrated circuit fabrication and is likely to retain this position in the foreseeable future. The number of devices manufactured on a single chip exceeded the generally accepted definition of *very large scale integration,* or *VLSI* (i.e., more than 100,000 devices per chip) in the mid-1970's (Fig. 1a). By 1986 this number had grown to over 1 million devices per chip, and by 2000 had exceeded *1 billion devices* per chip (e.g., the 1 GB DRAM). This increasing device count has been accompanied by a shrinking minimum feature size (Fig. 1b), which is expected to be smaller than 0.18 μm by 2000. Progress in ULSI manufacturing technology seems likely to continue to proceed in this manner. Further reductions in the unit cost per function, and in the power-delay product of ULSI devices, are projected. The entire saga of IC fabrication represents a remarkable application of scientific knowledge to the requirements of technology. This book represents an enthusiastic report on the state-of-the-art of ULSI silicon processing, as practiced at the time of its publication.

Figure 2 illustrates the sequence of steps that occurs in the course of manufacturing an integrated circuit. These steps can be grouped into two phases: 1) the *design phase*; and 2) the *fabrication phase* (Fig. 3). While this book is concerned only with the fabrication phase of this undertaking, it is also useful to briefly outline the steps of the design phase here. This provides the context which allows readers to perceive the role of silicon processing within the totality of integrated circuit manufacturing. Readers wishing to explore steps of the design phase in detail are referred to other technical literature, including the texts listed in References. 1, 2 and 3.

The desired functions and necessary operating specifications of the circuit are initially decided upon in the *design phase*. The chip is designed from the "top down." That is, the required large *functional blocks* are first identified. Next, their *sub-blocks* are defined, and finally

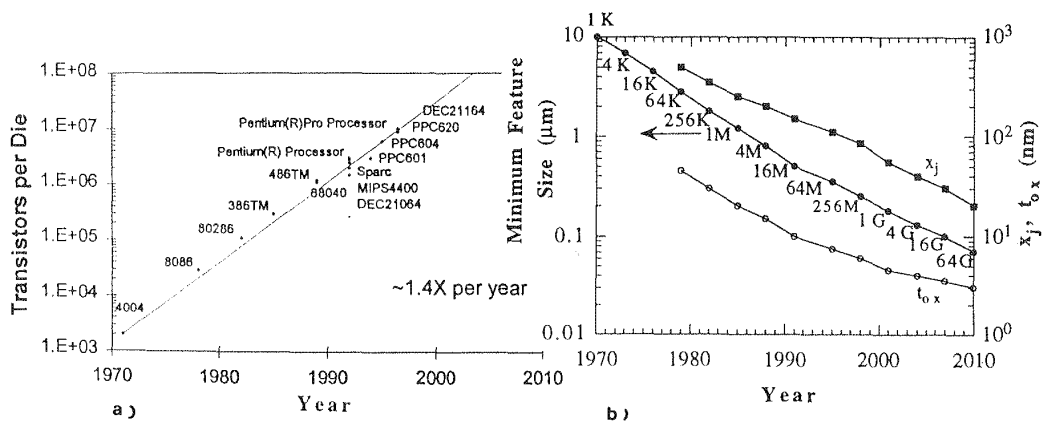

Fig. 1 (a) Increase in the number of transistors per microprocessor chip versus year of introduction, for a variety of microprocessor designs.[4] (© IEEE 1998) (b) Predictions of the decrease in minimum device feature size, junction depth, and gate oxide thickness versus time on integrated circuits, according to the SIA National Technology Roadmap for Semiconductors.

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the *logic gates* needed to implement the sub-blocks are chosen. Each logic gate is designed by appropriately connecting devices that are ultimately slated for fabrication on the Si wafers. Upon completion of these various levels of design, each level is rechecked to insure that correct functionality has been achieved. When all aspects of the circuit design are correct to the designer's satisfaction, *test vectors* (that will be used to test the manufactured circuits), are generated from the schematic of the logic gates.

The circuit is then layed out. The *layout* consists of sets of patterns that will be transferred to the silicon wafer. These patterns correspond to device regions or interconnect structures, and such patterns are sequentially transferred to the wafers as part of the wafer fabrication sequence (That is, through the use of photolithographic processes and a set of masks, see Fig. 4a). The

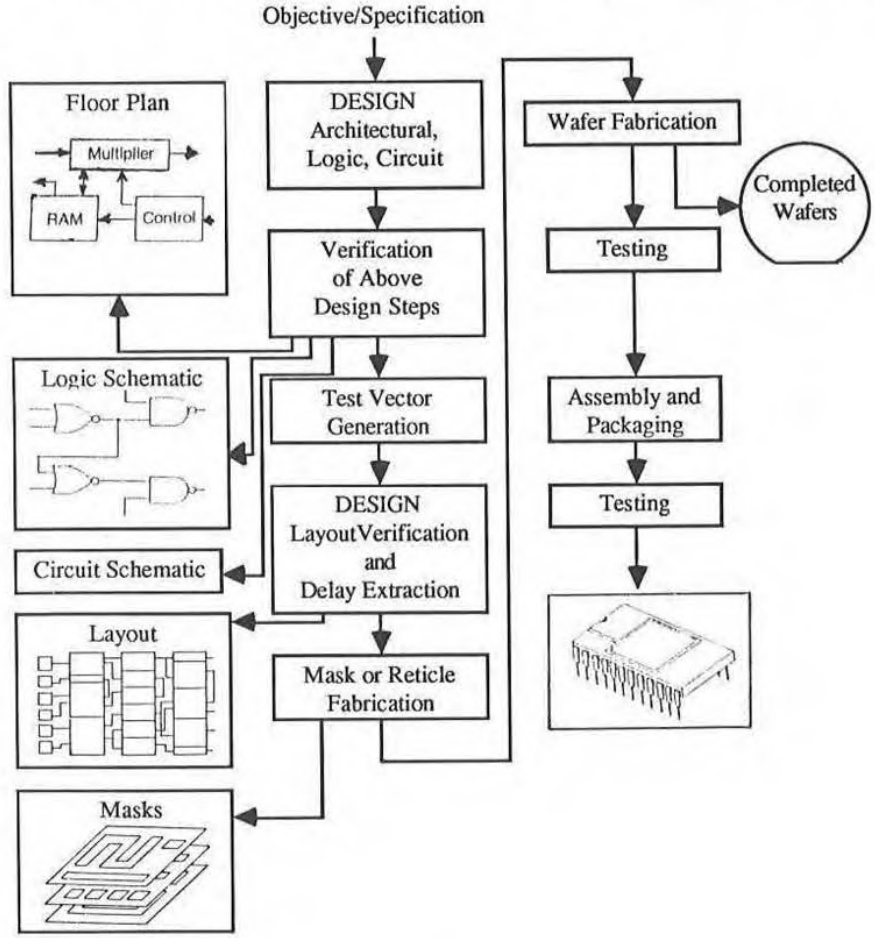

Fig. 2 Steps required for the manufacture of integrated circuits.

result of each pattern-transfer step is a set of features created on the wafer surface. These features are generally either in the form of: a) an etched opening in a film (or region of the substrate), or b) a patterned feature of a film present on the surface (e.g., an interconnect line or pad). After the openings (or *windows*) are created by the pattern transfer step, either controlled quantities of dopant are added to the silicon substrate through the openings, another layer is deposited that makes contact to the underlying layer through the opening. In either case, device regions and structures that interconnect device regions, are produced by the patterning processes and associated fabrication steps. A cross-section of a completed device is shown in Fig. 4b.

While the circuit is designed from the "top down," creation of the layout proceeds from the "bottom up." A variety of typical devices (e.g., transistors and resistors) are first layed out. Then, a set of cells representing the required primitive logic gates are created by interconnecting appropriate devices. Next, sub-blocks are generated by connecting these logic gates, and finally the functional blocks are layed out by connecting the sub-blocks. Additional items required by the circuit design are also incorporated during the layout process (e.g., power busses, clock-lines, and input-output pads). The completed layout is then subjected to a set of *design rule checks* and *propagation delay simulations* to verify that correct implementation of the circuit

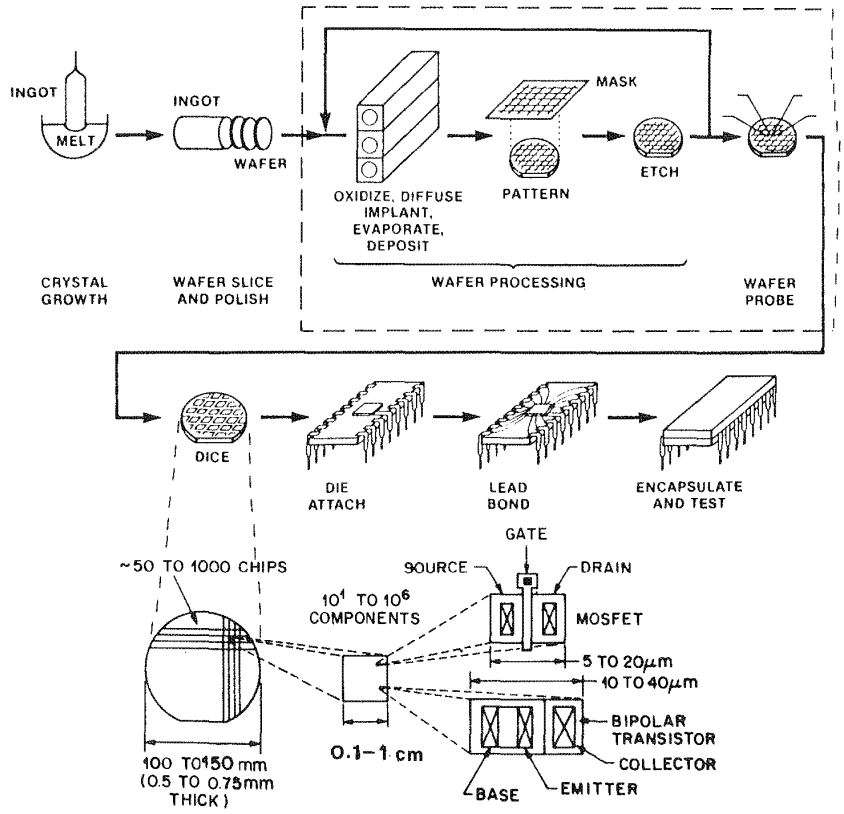

Fig. 3 The *wafer fabrication* process sequence of integrated circuits.

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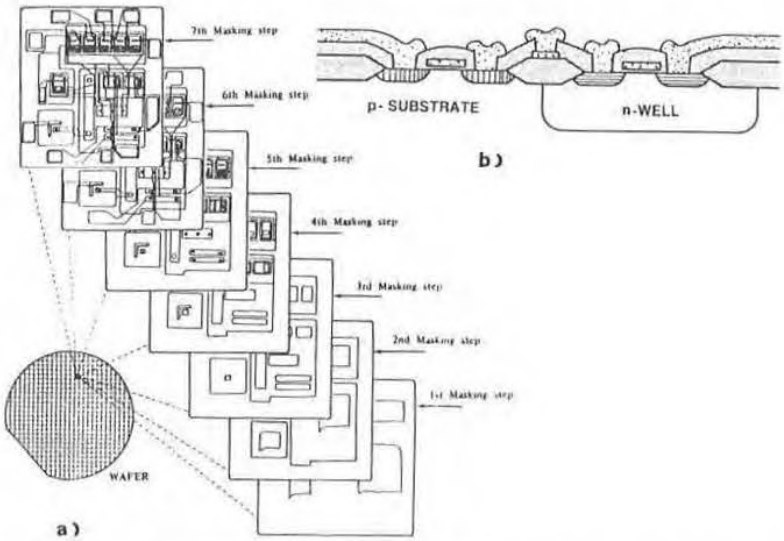

Fig. 4 (a) Example of the patterns transferred to a wafer during a seven-mask process sequence, and (b) Cross section of completed devices in a basic CMOS process.

has been achieved in layout form. Upon completion of this checking procedure, the layout information is ready to be used to generate a set of masks that will serve as tools for specifying the circuit patterns on silicon wafers. This layout information is stored on a computer.

In the three volumes of *Silicon Processing for the VLSI Era* integrated circuit manufacturing steps are described (Fig. 3). These steps start at the point where the layout information has been finalized. At that point procedures are utilized to convert the layout information stored on the computer, into a set of masks or reticles. This is described in Chap. 13. The individual fabrication process modules associated with creating patterns, introducing dopants, and depositing films on silicon substrates (to form integrated circuit features) are also subjects of this volume.

In Volume 2, information about how such individual process modules are combined to create complete ICs are covered in detail (namely the tasks of *process integration*). A brief discussion of process integration issues is also provided in Chaps. 15 and 16 of Volume 1. Volume 3 concentrates on the device physics of the submicron MOSFET and how device characteristics and the device processing steps are interrelated.

In Vol. 1, background information on science and technology common to many IC fabrication steps is also provided (e.g., vacuum technology [Chap. 3], material properties of thin films [Chap. 5], and optical science for microlithography [Chap. 13]). A short description of the so-called *back end* of IC processing (i.e., assembly and packaging) is given in Chap. 17. These three books can be read selectively to glean specific information. References are made to other chapters of the texts to clarify points for readers who wish to use the text in this manner.

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Chapter 7

SILICON EPITAXIAL GROWTH and SILICON ON INSULATOR

The *epitaxial* growth process provides an excellent means of growing a thin film of single crystal material upon the surface of a single crystal substrate. The term *epitaxy* is derived from two Greek words meaning "arranged upon." If the grown film is the same material as the substrate, the process is termed *homoepitaxy*. Homoepitaxy is generally referred to as *epitaxy* or simply *epi* and these terms will be used interchangeably throughout this text. Homoepitaxy of single crystalline silicon is the most important technological use of epitaxy, and is the primary subject of this chapter.

On the other hand, if the epitaxial film is grown on a substrate that is chemically different, the process is then termed *heteroepitaxy*. The principal applications of heteroepitaxy are in the deposition of silicon on sapphire (SOS) and in the fabrication of heterojunction semiconductor devices. When a heteroepitaxial deposition is made on a substrate that has a lattice constant very different than that of the film, a strained layer can form near the film/substrate interface. If the deposited film is thin enough, the strain can be accommodated elastically, but if the film is too thick the strain becomes relaxed through the generation of defects (e.g., misfit dislocations). These defects are known to propagate from the interface into the device region where they can adversely affect device properties. Conversely, if the lattice mismatch is small (as in the case of the growth of silicon-germanium alloys on silicon substrates), the strain is accommodated elastically. Under these conditions the epitaxial growth is termed *pseudomorphic* growth. Pseudomorphic growth is the method used in the formation of silicon-heterojunction-bipolar transistors (HBTs). Figures 7-1a, 7-1b, and 7-1c show a schematic representation of homoepitaxy, heteroepitaxy (strain relieved), and pseudomorphic epitaxial growth, respectively.

Epitaxial growth can be achieved by depositing the film directly from either the vapor phase,

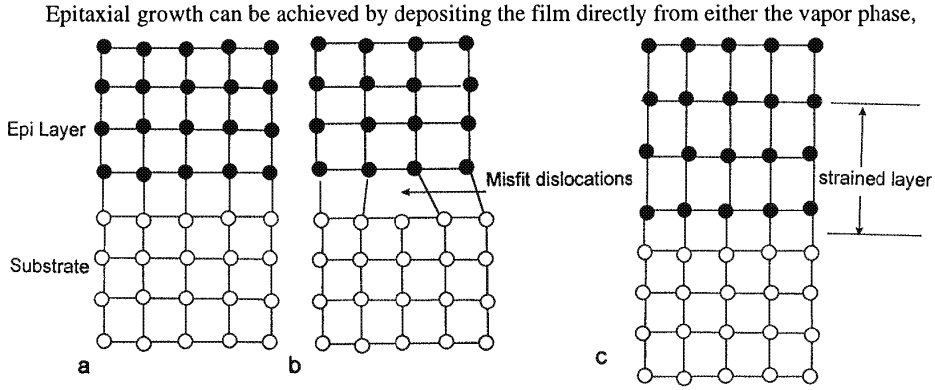

Fig. 7-1 Schematic of epitaxial structures: a) homoepitaxy; b) strain relieved heteroepitaxy (e.g., silicon-on-sapphire [SOS]); and c) psuedomorphic epitaxy.

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the liquid phase, or the solid phase. These techniques are termed *vapor-phase epitaxy* (VPE), *liquid-phase epitaxy* (LPE), and *solid-phase epitaxy* (SPE), respectively. VPE is the predominant method used in silicon processing, since it provides a means of achieving excellent control of the film thickness, impurity concentration, and crystalline perfection. A disadvantage of VPE is that it is requires relatively high temperatures (800–1150°C) in order to realize the necessary crystalline perfection. Such high-temperature processing can lead to the occurrence of *out-diffusion* and *autodoping*. These phenomena place a limitation on the ability to control the doping level in the epi layer and are discussed in detail in Section 7.4.4 of this chapter.

LPE has found its widest use producing epitaxial layers of III-V compounds (e.g., GaAs and InP). LPE, however, occurs during the re-freezing of molten layers of silicon on a silicon surface during the laser melting GILD process (see Chap. 9). SPE occurs during the crystalline re-growth that takes place during the low-temperature annealing of amorphous layers formed as a result of damage during high-dose ion implantation (see Chap. 10).

This chapter covers: 1) device applications of epitaxy; 2) fundamentals of epitaxial film growth; 3) epitaxial process considerations, including silicon precursors and doping effects; 4) defects in epitaxial layers; 5) pattern effects; 6) low-temperature epitaxy; 7) selective epitaxy; 8) epitaxial film characterization; and 9) silicon on insulators (SOI). The fundamentals of the kinetics and gas dynamics of CVD (epitaxial growth is a CVD process) are covered in detail in Chapter 6. In this chapter only the relevant results are repeated.

7.1 THE DEVICE APPLICATIONS OF EPITAXY

In the early days of semiconductor fabrication, epitaxial deposition was used to improve the performance of bipolar transistors that were then commonly used. By growing a lightly doped n-type epitaxial layer over a heavily doped n^+ substrate the bipolar device could be optimized for high breakdown voltage of the collector-substrate junction, while preserving a low collector resistance. The low collector resistance was required to improve the device operating speeds at moderate currents. Figure 7-2 depicts a cross-section of a high-speed oxide-isolated bipolar transistor showing the presence of the epitaxial layer. A key feature of bipolar epitaxy is that the film is deposited over patterned, n^+-doped diffused layers called *buried layers* or *sub-collectors*. BiCMOS devices are also be fabricated in epitaxial films deposited over buried layers.

More recently, epitaxial processes have been used to fabricate CMOS integrated circuits. In CMOS circuits the complete device is built in a thin (2–4 μm), lightly-doped p-type (or in some cases, intrinsic) epitaxial layer that is deposited over a uniformly heavily p^+-doped substrate. Figure 7-3 shows a cross section of a twin-well CMOS device depicting the epi layer.

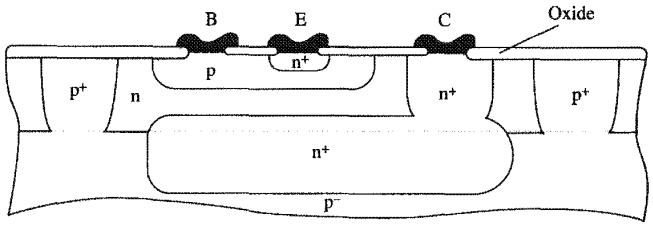

Fig. 7-2 Cross-section of a bipolar transistor built in an epitaxial layer. The light line indicates the boundary of the deposited n-type epi layer. Note that the n^+-buried layer extends into the epi layer as a result of autodoping and out-diffusion.

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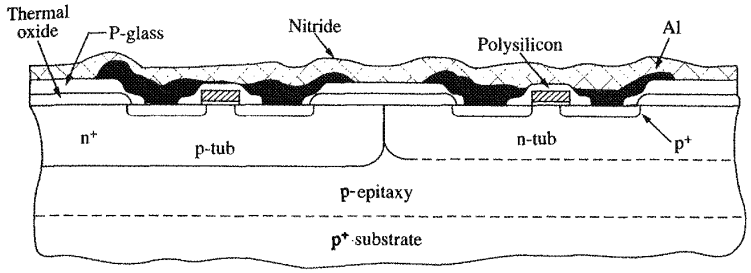

Fig. 7-3 Cross-section of a twin-well CMOS structure built in a p^- epitaxial layer and a p^+ substrate. Note that the p^+-region extends into the epi layer as a result of autodoping and out-diffusion.

In the next section we discuss the reasons for using epitaxial silicon rather than *polished bulk wafers* (*PBW*) for constructing advanced CMOS devices. It is interesting to note that IC manufacturers usually purchase CMOS epitaxial wafers directly from the wafer suppliers, while for bipolar ICs they process the epitaxy themselves. The reason is that a masking layer is required to produce the buried layer prior to the epi in the bipolar process.

7.1.1. Why Are CMOS Epitaxial Wafers Used?

CMOS epitaxial wafers, when compared to polished bulk wafers provide: a) improved latch-up immunity; b) layers of silicon free of SiO_x precipitates, COPs, or vacancy condensates (all of which are formed during crystal growth); and c) a silicon surface that is smoother than that found on PWBs, with minimal surface damage.

Latch-up in CMOS circuits is a phenomenon that causes the formation of a low resistance path between the supply voltage and ground. As a result, it is possible for the circuit to draw an unusually high amount of current. Such current draw can cause the circuit to cease functioning or even to "burn-up." The device physics underlying latch-up is beyond the scope of this text, but is covered in detail in Vol. 2 of this series. Although there are process and design techniques that can minimize latch-up, the use of epitaxial silicon has become the "standard" approach to fabricating ULSI CMOS microprocessor circuits because it provides latch-up protection.

Polished bulk wafers are known to include SiO_x precipitates, COPs, and vacancy condensate defects at or near the wafer surface. Moreover, despite the best polishing techniques, the wafer surface can retain polishing defects such as micro-damage and surface roughness. Surface defects are known to diminish the gate-oxide integrity and increase junction leakage. Epitaxial layers, on the other hand, do not contain oxygen (hence no SiO_x precipitates), COPs, or vacancy condensates, since these defects only form during crystal growth (during which oxygen is dissolved in the as-grown Si crystal, see Chaps 1 and 2). Since epi is deposited on a polished wafer, the new surface that forms is generally free of polishing micro-damage and surface roughness. As a result, CMOS devices produced in epitaxial material have superior dielectric integrity and junction leakage currents, compared to similar devices made on polished wafers.

The use of epitaxial wafers in the fabrication of microprocessors is now standard, while its use in DRAM devices is rather limited. There are two reasons for this. First, the gate oxide thickness required for DRAM devices is generally thicker than that required for microprocessor devices, even for the same "generation" of technology. These thicker gate oxides are less susceptible to the presence of surface defects and do not benefit as much from the advantages of the epi layer. Second, the cost to purchase a 200-mm epitaxial wafer is about 1.5–1.8 times that of a polished wafer. Since low manufacturing costs for DRAMs are vital for profitability, the

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Table 7-1 APPLICATIONS OF EPITAXY

Application	Thickness (μm)	Resistivity Range (ohm-cm)
Bipolar devices	0.8–1.6	0.5–4.0
CMOS devices	2–4	2–10
BiCMOS devices	3–5	2–20
High voltage devices	5–50	50–80

added cost per wafer is often too high to justify its use. However, the use of epi wafers for DRAM manufacturing is under serious consideration as thinner gate oxides become necessary. When the yields on devices fabricated in bulk wafers no longer meets the requirements for DRAM manufacturing, the industry may be compelled to change to epitaxial wafers. On the other hand, the DRAM manufacturers will try to find alternative processes to extend the life of bulk wafers, rather than pay the added cost associated with the use of epitaxial wafers.

Table 7-1 shows some of the applications of silicon epitaxy along with the epi thickness and resistivity ranges that are commonly used. Table 7-2 (which is extracted from the SIA roadmap) shows the epi layer requirements for the most advanced CMOS devices.[1] The two key points illustrated in that table are: 1) thinner epi layers are required (i.e., down to 1 μm); and 2) the structural defect density must be reduced by more than a factor of 2 from its current level. These two discordant requirements represent a significant challenge, since thinner films require lower growth temperatures, and lower temperatures can lead to increased defect density.

7.2 GROWTH OF EPITAXIAL LAYERS

In this section an atomic mechanism that has been proposed to explain epi film growth is first discussed. Then the various chemicals precursors used in conventional epitaxial growth are described. The kinetics of CVD were covered in detail in Chap. 6, and only the results pertinent to epitaxial growth will be repeated here.

7.2.1 Atomistic Model of Film Growth

Whatever *precursor* (source gas) is used and whatever chain of reactions occur (see next section) the final reactant species must be adsorbed on the growing surface where the reaction takes place. The reaction produces silicon and some by-product. In order for film growth to occur, the silicon atoms must remain adsorbed on the surface and the by-products desorbed. The adsorbed silicon atoms are referred to as *adatoms*. If an adatom is in a position such as A in Fig. 7-4, one of several events can take place. If the adatom A remains in its position other silicon atoms can become attached to it and a small silicon cluster or island can form. If numerous clusters form and begin to grow, it is likely that as they merge, a highly defected or even polycrystalline film will form. However, as it turns out, adatoms in position A are quite mobile at the deposition

Table 7-2 EPITAXIAL LAYER REQUIREMENTS vs. TECHNOLOGY NODE
Extracted from NTRS, SIA (1997)[1]

First year product shipment	1997	1999	2001	2003
Feature size (nm)	250	180	150	130
Layer thickness (μm)	2–5	2–5	2–4	2–4
Thickness tolerance (±%)	5	4	4	4
Layer structural defect density (m^2)	≤3.3	≤2.9	≤2.6	≤2.3

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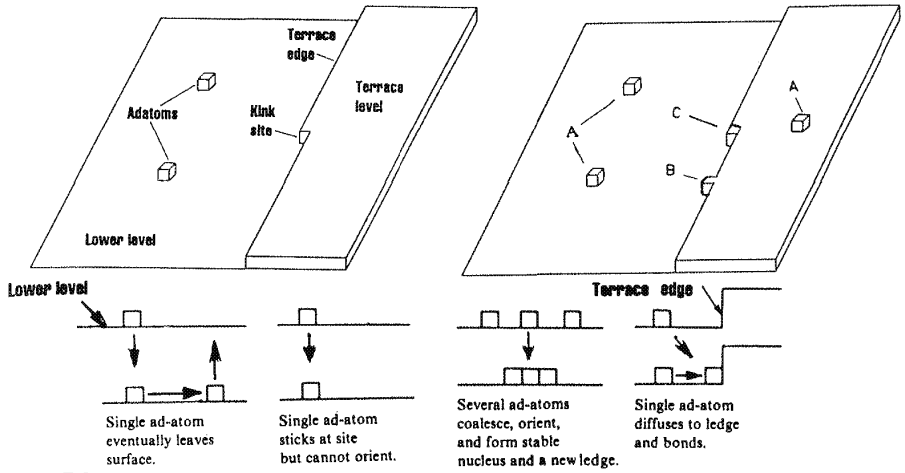

Fig. 7-4 Epitaxial growth model showing step-wise growth with adatoms in terrace positions A, adatoms at steps (or terrace edges) B, and adatoms at stable kink positions C.

temperatures and are likely to migrate along the surface. If a migrating adatom reaches a position along a growing *step* (or *terrace edge*), such as position B in Fig. 7-4, the adatom is more likely to remain in place (since atoms at position B are more energetically stable than at positions A). The stability arises from the fact that more Si-Si bonds have already formed when the adatom is at position B. The most energetically favored site for the adatom, however, is the so-called *kink position* (position-C in Fig. 7-4). When the adatom arrives at such a kink position, one-half of the Si-Si bonds can be established and further migration is thereafter unlikely to occur. For growth to continue, additional adatoms must migrate to kink positions and become incorporated in the growing film. In this respect, film growth proceeds by lateral movement (2-dimensional) of the steps on the lattice surface. After one layer is completed a second layer grows. Since epi proceeds by this lateral growth, an impurity sitting on the wafer surface can impede the motion and produce a stacking fault or dislocation defect in the film. For this reason, extremely clean silicon surfaces are required to achieve high-quality epi growth.

If adatom migration is suppressed during growth, a polycrystalline film is more likely to be deposited. Atom mobility is restricted by high deposition rates and low temperatures. At any particular deposition temperature there exists a maximum deposition rate above which polycrystalline films are deposited, but below which single crystal epitaxial films are formed.[2] Figure 7-5, shows a plot of the effect of growth rate and temperature on the formation of single (monocrystalline) or polycrystalline films. From that curve we observe that monocrystalline growth is favored at high temperatures and low growth rates, and polycrystalline deposition is favored under conditions of high growth rates and low temperatures. The maximum deposition rate at which single-crystal growth can be maintained is found to increase exponentially with temperature. When these results are plotted on an Arrhenius plot (Fig. 7-5) a straight-line dependence is obtained (indicative of a thermally activated process). The value of the activation energy extracted from this curve is ~5 eV. These results may be explained as follows. At high growth rates there is not sufficient time for the adatoms to migrate to the kink sites, thereby polycrystalline growth is favored. As the temperatures increase, however, the surface migration rate also increases, allowing time for silicon to reach the kink sites before additional adatoms form other clusters. Once at the kink site, the film continues to grow by lateral motion. The

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Chapter 9
DIFFUSION in SILICON

Diffusion is the phenomenon by which one chemical constituent moves within another as a result of the presence of a chemical gradient (more accurately, a chemical potential gradient). The diffusion of controlled impurities or dopants in silicon is the foundation of *pn* junction formation and device fabrication. In the early days of transistor and IC processing, dopants were supplied to the silicon by *chemical sources*. These dopants were then thermally diffused to the desired depth by subjecting the wafers to an elevated temperature treatment (900–1200°C) in a furnace. However, with the onset of submicron device fabrication, *ion implantation* became the standard method for introducing dopants into Si, and chemical-source diffusion was essentially abandoned. However, interest in this method was revived to some degree, primarily for forming ultra-shallow junctions (<100 nm). The chemical techniques being investigated for this application include rapid vapor doping (RVD) and P-GILD. They are described later in this chapter.

Nevertheless, after the dopants are introduced into silicon wafers by ion implantation they still need to be electrically activated. Such electrical activation requires a high-temperature operation called an *anneal*. Dopant diffusion also occurs during these activation anneals, as well as during any other high-temperature processes that may take place after the anneal (e.g., thermal oxidation, BPSG reflow). This implies that a high-temperature treatment will affect the distribution of all dopants already in the silicon. Therefore, it must be possible to trace the doping profile of all of the previous implants up to the last high-temperature thermal process. The control of the doping profile becomes ever more difficult as the devices shrink in size, and for that reason a fundamental understanding of diffusion remains important for ULSI fabrication.

Unfortunately, diffusion in silicon is not accounted for simply by solving the mathematical equations of diffusion. In this regard, the diffusion of dopants in silicon differs from that of diffusion in metals. Since silicon is a semiconductor, and the diffusing dopants are electrically charged, one must account for the interaction of the dopants with silicon point defects. These interactions are controlled by equilibrium reactions relating the balance of charge from all sources in the silicon crystal (i.e., intrinsic electron-hole pairs, *n*-type and *p*-type dopants, and the various charged defects). Silicon defects are discussed in Chap. 2.

In the early days of silicon technology, the junction depths in devices were typically as deep as 2000–4000 nm and their fabrication was relatively uncomplicated. With current generations of technology, the required junction depth has been scaled to 50–100 nm and future requirements will dictate junctions as shallow as 20 nm. This reduction in junction depth has made the fabrication of diffused junctions a major challenge. Notable advances in ion implantation (see Chap. 10) and thermal processing technology (RTP) have gone a long way to enabling the formation of such shallow junctions. Accompanying the fabrication of ultra-shallow junctions is the challenge of developing reliable analytical techniques for determining junction depths and concentration profiles. These techniques are also discussed in this chapter. Table 9-1 shows the National Technology Roadmap for Semiconductors[1] requirements for the range of minimum junction depth necessary for each successive technology generation from 1997 to 2012.

In this chapter the following topics are covered: a) mathematics governing the mass transport phenomena of diffusion (Fick's equations and their solutions); b) the temperature dependence

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Table 9-1 MINIMUM JUNCTION DEPTH VERSUS TECHNOLOGY NODE
(Extracted from NTRS, SIA [1997]).

First year product was shipped	1997	1999	2001	2003	2006	2009	2012
Linewidth in nm	250	180	150	130	100	70	50
Minimum junction depth, nm	50–100	36–72	30–60	26–52	20–40	15–30	10–20

of diffusion coefficients; c) the diffusion coefficients of the substitutional impurities; d) the simulation of one-dimensional doping profiles with SUPREM; e) atomistic models of diffusion in Si; f) diffusion in polycrystalline-Si; g) diffusion in SiO_2; h) anomalous diffusion effects; i) transient enhanced diffusion (TED); and j) measurement techniques used in diffusion studies.

9.1 THE MATHEMATICS OF DIFFUSION

In this section the basic differential equations of simple diffusion and their solutions for some special cases of diffusion in Si are described. The meaning of the *diffusion coefficient* D is defined and a method to experimentally determine its value is discussed. (The terms *diffusion coefficient, diffusivity,* and *diffusion constant* are used interchangably.) The atomic nature of the Si matrix and the interaction of the dopants with Si defects is reviewed in a subsequent section.

9.1.1 Fick's First Law

The basic mathematical tools for treating diffusion were elucidated in 1855 when Fick proposed that equations analogous to Fourier's heat-flow equations, should also apply to the diffusive flow of matter.[2] The first law posited by Fick states that if a concentration gradient, $\partial C/\partial x$, of an impurity exists in a finite volume of a matrix substance, then there exists a tendency for the impurity material to move in such a direction as to decrease the gradient. When diffusion occurs, the impurity concentration at any location becomes a function of both distance and time. One can represent the concentration profile by $C(x,t)$. If the flow persists for a sufficiently long time, the material will become homogeneous and the net flow of matter will cease. Fick went on to state that the flow of the impurity, represented by the *flux* J is proportional to the concentration gradient, $\partial C/\partial x$ and that the constant of proportionality is defined as the *diffusivity* D of the impurity in that particular matrix. Fick's statements can be represented mathematically as:

$$J = -D\frac{\partial C(x,t)}{\partial x} \tag{9.1}$$

Equation 9-1 implies that as the concentration gradient decreases, the flux or diffusion decreases. The flux, J, is defined as the mass of material moving per unit area, per unit time. The units used in Eq. 9-1 are shown in Eq. 9-1a:

$$J\ (\mathrm{gm/cm^2sec}) = -D(\mathrm{cm^2/sec})\frac{\partial C(\mathrm{gm/cm^3})}{\partial x(\mathrm{cm})} \tag{9.1a}$$

Equation 9-1a shows the units for D as cm^2/sec, but D can also be given in other units (e.g., μm^2/hr, or m^2/sec). The constant D depends on the diffusion temperature, the diffusing species (also called the *diffusant*), and the concentration of the diffusant. Other factors such as the ambient conditions during diffusion and the presence of other dopants also affect the measured value of D, and they will be discussed in ensuing sections of this chapter.

9.1.2 Fick's Second Law

Fick's Second Law in one-dimension is now derived from the first law. In order to obtain useful results one needs to determine what happens to the concentration gradient with the progression

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of time. To do this refer to Fig. 9-1, where the amount of dopant entering and leaving a finite volume of matrix is illustrated. Consider a finite volume of matrix material ΔV, having a thickness Δx and a unit cross-sectional area (i.e., $\Delta V = 1 \cdot 1 \cdot \Delta x$). Material enters or leaves this volume only in one dimension (i.e., only in the $\pm x$ direction). We define J_1 as the flux of material *entering* the volume Δx, and J_2 as the flux *leaving* the same volume element. If the volume element is very thin (i.e., $\Delta x \rightarrow 0$), then the difference in the fluxes is:

$$J_2 - J_1 = -\Delta x\left(\frac{\partial J}{\partial x}\right) \tag{9.2}$$

Since the mass of material that enters the element in unit time (J_1) is different than the amount which leaves (J_2), the concentration within the element must also be changing with time. The change of the concentration with respect to time is given by:

$$\frac{\partial C}{\partial t} = \frac{J_2 - J_1}{\Delta x} \tag{9.3}$$

By rearranging Eq. 9-2 to get $(J_2 - J_1)/\Delta x$ on one side, and substituting the other side into Eq. 9-3 one gets:

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial J}{\partial x} \tag{9.4}$$

Now substitute J from Eq. 9-1 into Eq. 9-4, to obtain *Fick's Second Law*, which can be written:

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \tag{9.5}$$

Equation 9-5 is the most general representation of Fick's second law. If the diffusion coefficient D is independent of position (concentration) then D can be brought outside the partial differential and Eq. 9-5 can be rewritten in a simpler form as:

$$\frac{\partial C(x,t)}{\partial t} = D\left[\frac{\partial^2 C(x,t)}{\partial x^2}\right] \tag{9.6}$$

The fact that D in Eq. 9-6 is assumed to be independent of position implies it is also independent of concentration (which varies with position as a result of the concentration gradient). As it turns out, for low concentrations of diffusant the assumption that D is independent of position is valid, and Eq. 9-6 can be used. But for high diffusant concentrations one must use Eq. 9-5.

9.1.3 Solutions to Fick's Second Law

Two solutions to Fick's Second Law when D is independent of concentration (i.e., Eq. 9-6 prevails), will be examined. The first solution relates to the case where dopants are introduced into the silicon from a vapor source. The source is considered to bring a constant supply of dopant atoms to the silicon surface where they diffuse into the silicon at the process temperature.

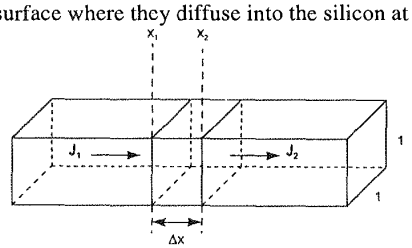

Fig. 9-1 Schematic showing an element of volume with the flux J_1 entering and J_2 leaving.

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it supply of do-
emperature.

It is assumed that the source maintains a constant value of surface concentration during this entire diffusion process. In diffusion technology, this type of dopant incorporation is termed *predeposition*, and is used to introduce a known quantity of impurities into the silicon. As noted earlier, this step in the past was carried out by diffusion from a chemical source, but now has been largely replaced by ion implantation. The pre-deposited dopant (whether chemically or ion implanted) is then redistributed in the silicon by a further thermal treatment called a *drive-in* or *redistribution diffusion*. Despite the reliance on ion implantation for the pre-deposition step, it is still illustrative to solve Fick's differential equation for the pre-deposition boundary conditions. Moreover, chemical source pre-deposition is still being used for some deep junction applications and is now under consideration again for some ultra-shallow junction applications.

9.1.3.1 Chemical Pre-Deposition: In order to solve the second-order differential equation (Eq. 9-6) it is necessary to establish initial and boundary conditions. For the chemical predeposition step the initial condition is that the concentration of dopant in the silicon at t = 0 for all values of x is equal to 0. This condition is written as:

$$C(x, 0) = 0 \tag{9.7}$$

The two boundary conditions for this process step are established next. The first boundary condition (Eq. 9-8) states that the concentration of dopant at x = 0 (i.e., the concentration at the surface of the Si), for any time during the diffusion, is fixed at a value C_s for the entire diffusion cycle. The units of C_S are atoms/cm^3 and the condition is described mathematically as:

$$C(0, t) = C_S \tag{9.8}$$

The second boundary condition states that the concentration of dopant at $x = \infty$ is equal to 0 for any time, or:

$$C(\infty, t) = 0 \tag{9.9}$$

The solution to the partial differential equation (Eq. 9-6) with the application of the initial and boundary conditions is given by Eq. 9-10:

$$C(x, t) = C_S \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \tag{9.10}$$

where D is the diffusion coefficient, x is the distance coordinate, t is the time of the diffusion, and *erfc* is the *complementary error function*. The complementary error function is tabulated[3] for values of the dummy variable $z = x/2(Dt)^{1/2}$. The denominator of Eq. 9.10, $2(Dt)^{1/2}$, is termed the *diffusion length*, which is representative of how far atoms move during a given thermal step. The term is also referred to as *"root Dt"*. The units of "root Dt" are length (cm) and its value is used when comparing the thermal exposure or thermal budget of a process (see Chap. 8).

Figure 9-2 shows a plot of the concentration profile for a predeposition for several different times at a constant temperature. D is assumed to be constant and the profile only depends on the time of the diffusion. As the diffusion time is increased the surface concentration remains constant at C_s, while the dopants move deeper into the silicon. The total amount of dopant introduced into the silicon also increases with time. The *junction depth*, x_j, can be defined as the point at which the concentration of the diffusant equals the background doping in the Si. The total amount of dopant that accumulates in the silicon (Q_o) during the predeposition can now be calculated by integrating Eq. 9-10 with respect to x over all of space (in one-dimension) and obtain Eq. 9-11.

$$Q_o = \int_{-\infty}^{+\infty} C(x, t) = \int_{-\infty}^{+\infty} C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) dx = \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt} \tag{9.11}$$

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