

electric field jump for
charged boundary

The charge density $\rho(x)$ [units: C/cm^3] that describes the sheet charge is a “delta function” at the boundary—it integrates to Q even when $\Delta \rightarrow 0$. The boundary condition for the case with a sheet charge is

$$E(0^+) = \left(\frac{\epsilon_1}{\epsilon_2} \right) E(0^-) + \frac{Q}{\epsilon_2} \quad (3.14)$$

Figure 3.4(d) shows the jump in E for the case of a positive sheet charge Q and $\epsilon_1 > \epsilon_2$. The discontinuity in E is increased by the presence of the positive charge sheet, in comparison to the uncharged boundary in Fig. 3.4(a)-(b).

EXAMPLE 3.1 Metal-Metal Capacitor Electrostatics

In many IC processes, there are two or more levels of metallization separated by deposited oxide films. A planar capacitor can be formed by overlapping metal layers as shown in the layout and cross section in Fig. Ex3.1A below. Assume that a one-dimensional, parallel-plate analysis is adequate.

(a) Find the capacitance C in $fF/(\mu m)^2$, where $1 fF = 10^{-15} F$.

SOLUTION

By definition, capacitance is the derivative of charge with respect to voltage $C = dQ/dV$; in this case, C is constant. We are interested in finding the capacitance per unit area, so the charge Q is also interpreted as per unit area. When a positive voltage V is applied to the capacitor, a positive surface charge density $+Q$ accumulates on the top plate of the capacitor, which is mirrored by an equal and opposite negative charge surface charge density $-Q$ on the bottom plate.

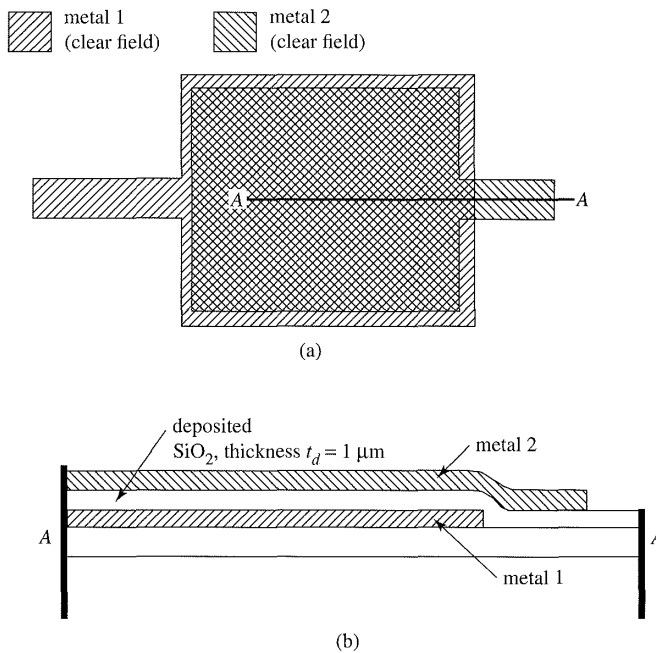
The close-up view of the gap between the plates in Fig. Ex3.1B shows an interior region of the capacitor with all the electric field lines pointing in the $+x$ direction. In this one-dimensional analysis, we will neglect the 2-D effects at the perimeter of the capacitor and assume that all the field lines are parallel to the x axis.

As shown in the close-up view of the capacitor, the electric field is constant in the oxide since there is no charge present (see Eq. (3.1), Gauss's Law). Since the electric field is constant and the voltage drop across the gap is V , it follows that $E = V/t_d$. The boundary condition in Eq. (3.14) connects the electric field to the charge density Q [C/cm^2] on the plates

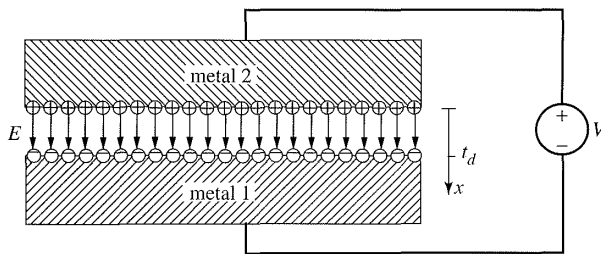
$$E = \left(\frac{\epsilon_o}{\epsilon_{ox}} \right) E_{metal} + \frac{Q}{\epsilon_{ox}} = \frac{Q}{\epsilon_{ox}}$$

where ϵ_{ox} is the permittivity of the deposited SiO_2 and $E_{metal} = 0$ (no electric field inside metals). We can substitute $E = V/t_d$ and find the capacitance per unit area

$$\frac{V}{t_d} = \frac{Q}{\epsilon_{ox}} \rightarrow C = \frac{dQ}{dV} = \frac{\epsilon_{ox}}{t_d}$$



► **Figure Ex3.1A** Metal-metal IC capacitor: a) layout and (b) cross section.



► **Figure Ex3.1B** Close-up of metal-metal capacitor with applied voltage, showing surface charges on top and bottom metal plates and electric field lines.

Substituting $\epsilon_{ox} = 3.9 \epsilon_o = 3.45 \times 10^{-13} \text{ F/cm}$ and $t_d = 1 \mu\text{m} = 1 \times 10^{-4} \text{ cm}$ for the deposited oxide film, we find that

$$C = 3.45 \times 10^{-9} \text{ F/cm}^2 = 34.5 \text{ aF}/\mu\text{m}^2$$

where $1 \text{ aF} = 1 \text{ attofarad} = 10^{-18} \text{ F}$. For example, a $100 \times 100 \mu\text{m}^2$ overlap area between metal 1 and metal 2 yields a capacitance of 345 fF, where $1 \text{ fF} = 1 \text{ femtofarad} = 10^{-15} \text{ F}$.

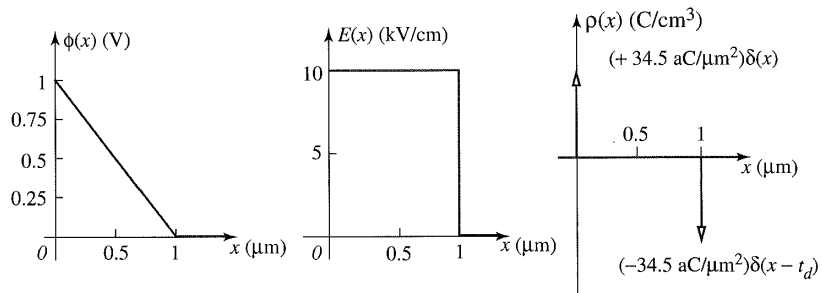
(b) Sketch the charge density, electric field, and potential when a voltage $V = 1 \text{ V}$ is applied between the top and bottom metal layers.

SOLUTION

For an applied voltage of $V = 1 \text{ V}$, the electric field in the gap is

$$E = (1 \text{ V}) / (1 \times 10^{-4} \text{ cm}) = 10 \text{ kV/cm}$$

From the definition of potential, the electrostatic potential $\phi(x)$ has a constant slope equal to -10 kV/cm . The bottom electrode is taken as the zero reference in the plot of $\phi(x)$ below. Finally, the charge density $\rho \text{ [C/cm}^3\text{]}$ is zero everywhere except on the inside surfaces of the metal plates. The mathematical function for the surface charge Q is a delta function, which is represented by “spikes” at the two surfaces. Note that the derivative of the electric field is consistent with these spikes at $x = 0$ and $x = t_d$.



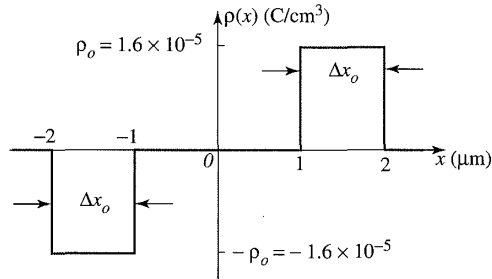
► **Figure Ex3.1C** Potential, electric field, and charge density for the capacitor with $t_d = 1 \mu\text{m}$.

EXAMPLE 3.2 Field and Potential from a Distributed Charge Density

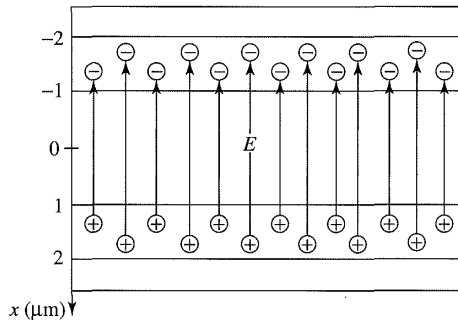
(a) Given the following charge distribution, sketch the electric field $E(x)$ and find the numerical value of $E(0)$.

SOLUTION

We should first be sure which way the electric field points. The electric field points from positive charges to negative charges—in the opposite direction as the x axis. Therefore, the electric field is negative. A sketch of the charge distribution with the electric field lines is shown in Fig. Ex3.2B, which indicates that the electric field is constant between the charged layers for $-1 \mu\text{m} < x < 1 \mu\text{m}$, and zero outside the charged layers for $x < -2 \mu\text{m}$ or $x > 2 \mu\text{m}$. Our basic intuition from the parallel-plate capacitor in Ex. 3.1 (derived from Gauss’s Law) also applies to this “smeared” charge distribution.



► **Figure Ex3.2A** Arbitrary charge distribution in silicon.

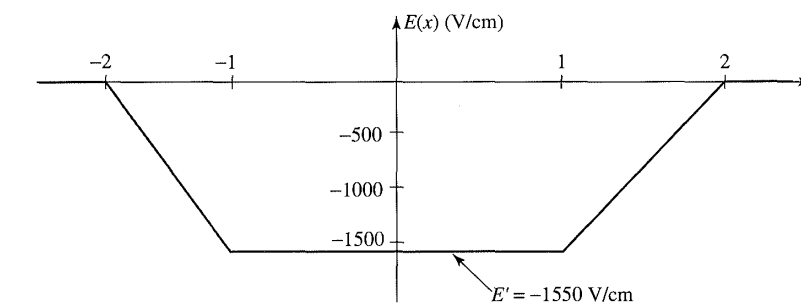


► **Figure Ex3.2B** Sketch of electric field lines pointing from positive to negative charges.

We now want to find the field in between the charged layers. Rather than integrate the charge density, we can use the integral form of Gauss's Law to relate the total charge $+Q$ or $-Q$ [C/cm^2] in one of the charged regions to the electric field

$$E(x) - E(-2\mu\text{m}) = \frac{-Q}{\epsilon_s} = \frac{-\rho_o \Delta x_o}{\epsilon_s} = \frac{-1.6 \times 10^{-9}}{1.036 \times 10^{-12}} = -1.55 \times 10^3 \text{ V/cm}$$

where the boundary at x is anywhere between the charged layers: $-1 \mu\text{m} < x < 1 \mu\text{m}$. Since the field at the other boundary at $x = -2 \mu\text{m}$ is zero, the electric field between the charged layers is $E' = -1550 \text{ V/cm}$. Within the charged layers, the charge density is constant and the electric field must vary linearly with x according to the differential form of Gauss's Law. This knowledge, combined with the electric field being zero at the boundaries of the charged region at $x = -2 \mu\text{m}$ and $x = 2 \mu\text{m}$, enables us to sketch the trapezoidal shape of $E(x)$ in Fig. Ex3.2C. By "turning the crank" and integrating $\rho(x)/\epsilon_s$, we could have directly calculated the functional form of $E(x)$ assuming we didn't make algebraic errors along the way. By reasoning through the implications of Gauss's Law and the shape of the charge distribution, we are certain we have the correct answer before doing the math.



► **Figure Ex3.2C** Plot of electric field $E(x)$ for the charge distribution in this example.

(b) Sketch $\phi(x)$ assuming $\phi(0) = 0$ V. What is $\phi(2 \mu\text{m})$?

SOLUTION

In order to plot the potential $\phi(x)$, we must graphically integrate $-E(x)$. Starting from $x = 0$, at which point we are given that $\phi(0) = 0$, we can integrate in the $+x$ direction. We know $\phi(2 \mu\text{m}) > 0$ since the positive charge is on the right side of the plot of $\rho(x)$ and also that the electric field points from right to left.

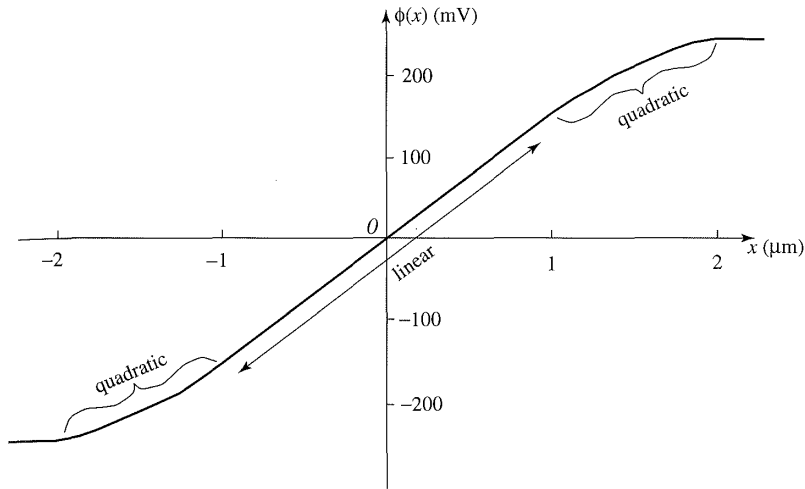
Over the interval $0 < x < 1 \mu\text{m}$, the potential varies linearly since the field is constant. The potential at $x = 1 \mu\text{m}$ is given by

$$\phi(1 \mu\text{m}) = \phi(0) + \int_0^{1 \mu\text{m}} -E(x') dx' = (1550 \text{ V/cm})(10^{-4} \text{ cm}) = 155 \text{ mV}$$

Over the interval $1 \mu\text{m} < x < 2 \mu\text{m}$, the potential varies quadratically since the field is a linear function. The potential change from $x = 1 \mu\text{m}$ to $x = 2 \mu\text{m}$ is given by the area under $-E(x)$

$$\phi(2 \mu\text{m}) - \phi(1 \mu\text{m}) = \left(\frac{1}{2}\right)(10^{-4} \text{ cm})(1550 \text{ V/cm}) = 77.5 \text{ mV}$$

Therefore, the potential at $x = 2 \mu\text{m}$ is $\phi(2 \mu\text{m}) = 155 + 77.5 \text{ mV} = 232.5 \text{ mV}$. Since the electric field is symmetric about $x = 0$, the potential for $x < 0$ is $\phi(-x) = -\phi(x)$. The potential $\phi(x)$ is plotted below. If the function for $\phi(x)$ is needed, then the negative of $E(x)$ can be integrated and the solutions in each interval patched together using the continuity boundary condition.



► **Figure Ex3.2D** Plot of the potential for the distributed charge density in Example 3.2

EXAMPLE 3.3 Metal-Oxide-Semiconductor (MOS) Capacitor

Another type of common IC capacitor is the Metal-Oxide-Semiconductor (MOS) capacitor. It is formed by a metal layer, an oxide layer, and a layer of silicon. A single mask is needed to create the basic sandwich as shown in the layout and cross section in Fig. Ex3.3A.

(a) Given the qualitative picture of the charge distribution and electric field lines shown in Fig. Ex3.3B, plot the charge density $\rho(x)$. Find an equation relating Q_G and X_d .

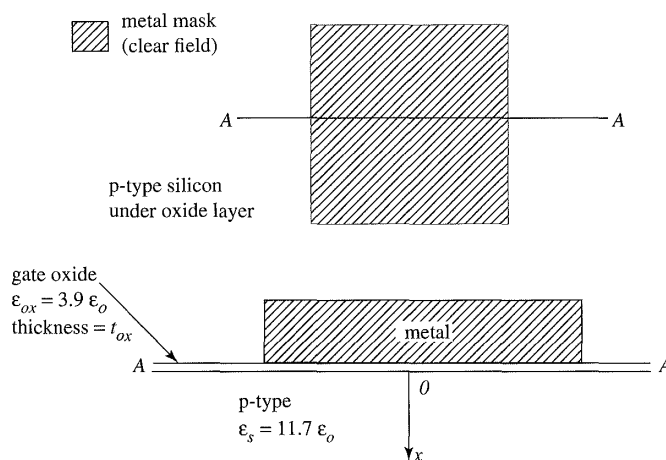
SOLUTION

First, we need to define the coordinate system. The origin is located at the interface between the oxide and p-type silicon. The oxide and metal extend into the $-x$ region and the silicon extends into the $+x$ region. The charge on the metal gate is located at the bottom surface as a sheet charge density, with units C/cm^2 . On the plot of charge density in C/cm^3 in Fig. Ex3.3C, the gate charge is plotted as a delta function $Q_G \delta(x + t_{ox})$ that is located at the metal/oxide interface at $x = -t_{ox}$.

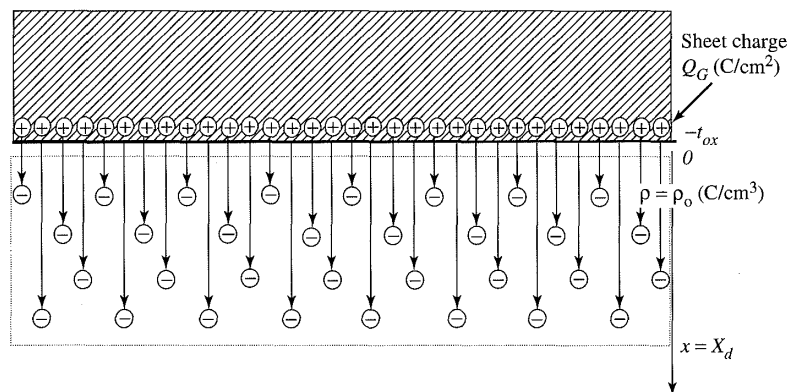
The total charge (gate charge + charge in the silicon substrate) is zero; therefore, the total charge in the silicon per unit area must be equal and opposite to the charge on the gate

$$Q_G = -(\rho_o X_d) = -\rho_o X_d \rightarrow X_d = Q_G / (-\rho_o)$$

(b) Find and sketch the electric field $E(x)$ and find an expression for the field in the oxide, E_{ox} , in terms of ρ_o , X_d , and ϵ_{ox} .



► **Figure Ex3.3A** Metal-oxide-silicon capacitor: (a) layout and (b) cross section.



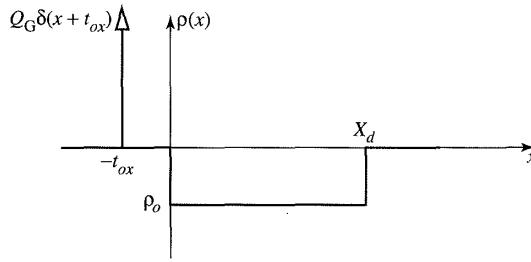
► **Figure Ex3.3B** Charge distribution and electric field lines for Example 3.3.

SOLUTION

The electric field points from positive charges to negative charges in the $+x$ direction, and is, therefore, positive. The electric field is confined to the region $-t_{ox} < x < X_d$ because the total charge in this interval is zero. In the oxide $\rho(x) = 0$ and the differential form of Gauss's Law

$$\frac{dE}{dx} = \frac{\rho(x)}{\epsilon_{ox}} = 0, \text{ for } -t_{ox} < x < 0$$

indicates that the field $E(x) = E_{ox}$ is constant for $-t_{ox} < x < 0$. In the charged region in the silicon, the charge density is constant at $\rho(x) = \rho_o$ and, therefore, the



► **Figure Ex3.3C** Charge density $\rho(x)$ corresponding to the qualitative charge distribution in Fig. Ex3.3B.

electric field is a linear function of x there. Since the field is known to be zero at $x = X_d$, we only need the value of the field at $x = 0$ to complete the sketch. The boundary condition at the oxide/silicon interface is

$$\epsilon_{ox} E_{ox} = \epsilon_s E(x = 0^+) \rightarrow E(x = 0^+) = (\epsilon_{ox}/\epsilon_s) E_{ox} = E_{ox}/3$$

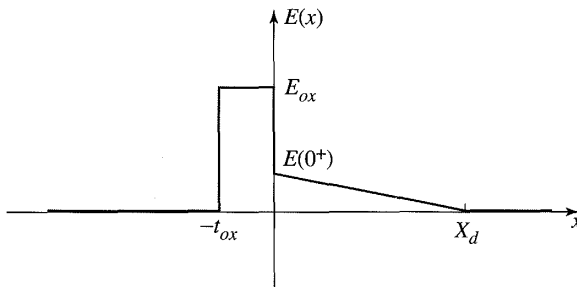
Gauss's Law in integral form is a convenient way to find the value of the electric field at the boundary of a charged region. Using Eq. (3.2) over the interval $0 \leq x \leq X_d$, we find

$$\epsilon_s E(X_d) - \epsilon_{ox} E_{ox} = \int_0^{X_d} \rho_o dx = \rho_o X_d$$

Since $E(X_d) = 0$, the oxide field is

$$E_{ox} = \frac{-\rho_o X_d}{\epsilon_{ox}}$$

Note that there is the possibility of sign errors in applying Eq. (3.2); however, we are not depending on the math to tell us the sign since we already *know* $E_{ox} > 0$. The electric field $E(x)$ is plotted in Fig. Ex3.3D.



► **Figure Ex3.3D** Sketch of electric field for metal-oxide-silicon capacitor with the charge distribution in Fig. Ex3.3B.

(c) Sketch the potential $\phi(x)$ through the structure given that the potential of the metal gate is $\phi(-t_{ox}) = \phi_m$. Find an expression for the surface potential $\phi_s = \phi(0)$ in terms of ϕ_m , ρ_o , X_d , ϵ_{ox} , and t_{ox} . In addition, find an expression for the potential drop across the charged region in the silicon in terms of ρ_o , X_d , and ϵ_s .

SOLUTION

As we learned in Example 3.2, there is no need to integrate $-E(x)$ in order to sketch the potential. From the definition of potential and the sketch of $E(x)$ above, the potential is a linear function in the oxide and a quadratic function of x in the charged region of the silicon substrate. Poisson's Equation is useful for finding the concavity of the potential in the charged region

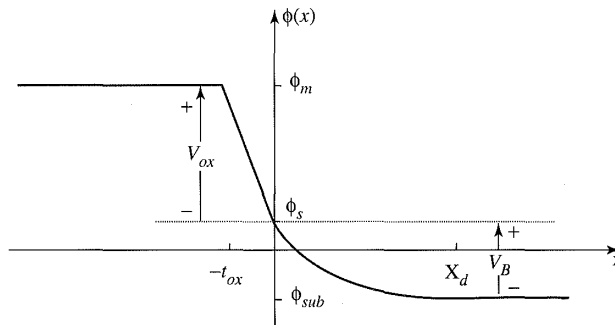
$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho_o}{\epsilon_s} > 0$$

Therefore, the potential is “concave up” in the charged region. Finally, we also know that the potential is continuous at the boundary $x = 0$ between the oxide and silicon. We can piece together the linear and quadratic solutions and sketch the potential between the metal and underlying substrate ($x > X_d$), the potential of which is defined as ϕ_{sub} . Figure Ex3.3E is a plot of the potential through the MOS capacitor.

On the sketch of $\phi(x)$ below, the total drop has been divided into two parts, the drop across the oxide V_{ox} and the drop across the charged region in the silicon V_B .

$$\phi_m - \phi_{sub} = V_{ox} + V_B$$

Note that the polarities of V_{ox} and V_B are defined on the potential plot in Fig. Ex3.3E to avoid confusion with signs. The drop across the oxide can be found by integrating the oxide field from $x = -t_{ox}$ to $x = 0$.



► **Figure Ex3.3E** Potential plot for metal-oxide-silicon capacitor with the charge distribution in Fig. Ex3.3B.

$$\phi_s - \phi_m = \int_{-t_{ox}}^0 (-E_{ox}) dx = -E_{ox} (0 - (-t_{ox})) = -V_{ox}$$

and therefore, $V_{ox} = E_{ox} t_{ox}$. The surface potential can be found in terms of the given parameters by substituting for the oxide field

$$\phi_s = \phi_m - E_{ox} t_{ox} = \phi_m - \frac{(-\rho_o) X_d t_{ox}}{\epsilon_{ox}}$$

This expression can be simplified by defining the charge Q_B [C/cm²] in the substrate as $Q_B = \rho_o X_d = -Q_G$, and by recognizing that the oxide capacitance per unit area is $C_{ox} = \epsilon_{ox}/t_{ox}$. The surface potential and drop across the oxide are related to these charges by

$$\phi_s = \phi_m + \frac{Q_B}{C_{ox}} \text{ and } V_{ox} = -\frac{Q_B}{C_{ox}} = \frac{Q_G}{C_{ox}}$$

The last result is not unexpected since the voltage drop V_{ox} must be proportional to the charge $\pm Q_G$ stored on each side of the insulating oxide. Finally, Poisson's Equation is used to find the drop V_B across the charged region

$$\frac{d^2 \phi(x)}{dx^2} = -\frac{\rho_o}{\epsilon_s} \text{ for } 0 < x < X_d$$

This ordinary differential equation can be solved for $\phi(x)$. The drop across the charged region is

$$\phi(0) - \phi(X_d) = V_B = \frac{1}{2} \left(-\frac{\rho_o}{\epsilon_s} \right) X_d^2 = \left(-\frac{\rho_o X_d}{2\epsilon_s} \right) X_d = \frac{-Q_B}{2\epsilon_s} X_d$$

Note that we have quantified the essential features of the electric field and the potential in the MOS structure without depending on formal mathematical analysis.

► 3.2

CARRIER CONCENTRATION AND POTENTIAL IN THERMAL EQUILIBRIUM

In order to find complete solutions for the electrostatic potential in silicon, we must define a potential reference. Although the choice is arbitrary, we will find it very convenient to select a reference that is related to the thermal equilibrium carrier concentration.

Recall from Chapter 2 that thermal equilibrium is equivalent to the absence of any stimulus to the device—zero applied voltage, no external light source, etc. In this state, the current density J_o must be zero. Perhaps less obvious is that the electron and

hole current densities J_{no} and J_{po} must *each* be equal to zero in thermal equilibrium. The physical reasoning is that the populations of electrons and the holes are each in equilibrium and, therefore, must have zero current densities. For example, $J_{no} \neq 0$ implies that electrons will pile up with time at one end of a structure in thermal equilibrium, which is hardly reasonable.

Setting the electron current density equal to zero in thermal equilibrium:

$$0 = qn_o\mu_n E_o + qD_n \frac{dn_o}{dx} \quad (3.15)$$

Solving for the gradient and using Einstein's Relation (Eq. 2.51) to eliminate the ratio of the mobility to the diffusion coefficient, we find that

$$\frac{dn_o}{dx} = \left(-\frac{\mu_n}{D_n}\right)n_o E_o = \left(-\frac{q}{kT}\right)n_o \left(-\frac{d\phi_o}{dx}\right) \quad (3.16)$$

where the negative gradient of the potential ϕ_o has been substituted for the electric field. Solving for the differential potential $d\phi_o$, we find

$$d\phi_o = \left(\frac{kT}{q}\right) \frac{dn_o}{n_o} = V_{th} \frac{dn_o}{n_o} \quad (3.17)$$

in which we have substituted the thermal voltage $V_{th} = kT/q$.

This differential equation can be solved by direct integration from a reference point x_o to an arbitrary point x

$$\phi_o(x) - \phi_o(x_o) = V_{th} \ln \left(\frac{n_o(x)}{n_o(x_o)} \right) \quad (3.18)$$

To find a numerical value for $\phi_o(x)$, we need to select a reference for the potential. By convention, the reference for potential is chosen to be the point where the electron concentration is the intrinsic concentration

$$\phi_o(x_o) = 0 \text{ when } n_o(x_o) = n_i \quad (3.19)$$

potential reference in
thermal equilibrium

Substituting this reference into Eq. (3.18) defines the potential in terms of the electron concentration in thermal equilibrium

$$\phi_o(x) = V_{th} \ln \left(\frac{n_o(x)}{n_i} \right) \quad (3.20)$$

Note that n-type silicon has a positive electrostatic potential since $n_o > n_i$ when electrons are the majority carriers. In other words, a region of n-type silicon is *relatively* positive, when compared with an intrinsic region.

By inverting this equation, we can express the electron concentration in terms of the electrostatic potential

$$n_o(x) = n_i e^{\phi_o(x)/V_{th}} \quad (3.21)$$

A parallel derivation for hole concentration leads to the following results

$$\phi_o(x) = -V_{th} \ln\left(\frac{p_o(x)}{n_i}\right) \quad p_o(x) = n_i e^{-\phi_o(x)/V_{th}} \quad (3.22)$$

so that p-type silicon ($p_o > n_i$) has a negative electrostatic potential, with respect to intrinsic silicon.

3.2.1 The 60mV Rule

In order to get an easy-to-remember rule, we replace the natural logarithm with the base 10 logarithm in Eq. (3.20) and evaluate the expression at a “warm” room temperature ($V_{th} = 26$ mV):

$$\phi_o(x) = (26\text{mV}) \ln(10) \log\left(\frac{n_o(x)}{10^{10}}\right) = (60\text{mV}) \log\left(\frac{n_o(x)}{10^{10}}\right). \quad (3.23)$$

60mV rule

This **60 mV rule** can be evaluated without a calculator for carrier concentrations that are equal to 10^{14}cm^{-3} , 10^{15}cm^{-3} , etc. For example, $n_o = 10^{16}\text{cm}^{-3}$ corresponds to the potential

$$\phi_o = (60\text{ mV}) \log(10^{16}/10^{10}) = (60\text{ mV})(6) = 360\text{ mV} \quad (3.24)$$

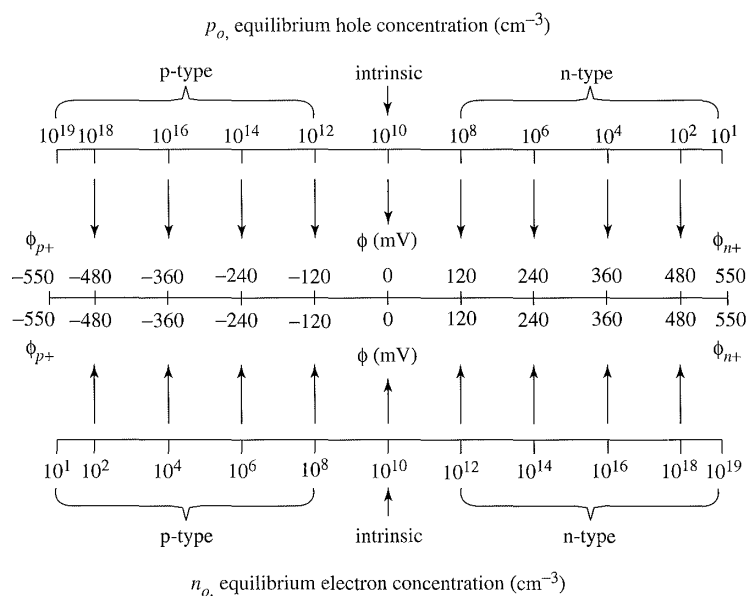
We can also express the potential as a function of the hole concentration in thermal equilibrium by substituting the mass-action law $n_o = n_i^2/p_o$ into Eq. (3.23):

$$\phi_o(x) = -(60\text{mV}) \log\left(\frac{p_o(x)}{10^{10}}\right) \quad (3.25)$$

For a hole concentration of $p_o = 10^{16}\text{cm}^{-3}$, the potential is $\phi_o = -360$ mV. The carrier concentrations can range from the intrinsic concentration to about 10^{19}cm^{-3} for electrons or for holes, which corresponds to a potential range in thermal equilibrium of $-540\text{ mV} \leq \phi_o \leq 540\text{ mV}$. The potential of silicon that is extremely heavily doped with donors (called **n⁺ silicon**) is $\phi_{n+} = 550$ mV. For **p⁺ silicon**, which is heavily doped with acceptors, the potential is $\phi_{p+} = -550$ mV. Figure 3.5 shows the 60 mV rule in graphical form.

n⁺ and p⁺ silicon

The derivation of Eq. (3.23) only required that the electron and hole currents are zero throughout the sample. In addition to thermal equilibrium, this requirement is also satisfied in capacitors since the insulator prevents carrier transport through the structure.



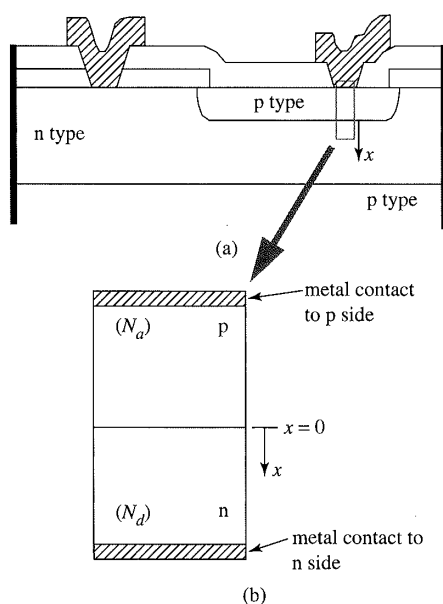
► **Figure 3.5** 60 mV rule relating electrostatic potential in thermal equilibrium to hole or electron concentration at room temperature.

► 3.3 THE pn JUNCTION: A FIRST PASS

A **pn junction** consists of a p-type silicon region immediately adjacent to an n-type silicon region. As we have seen in Chapter 2, pn junctions are built into nearly all IC device structures—either intentionally or as by-products of the fabrication process. Figure 3.6(a) shows the cross section of a pn junction. The p and n regions are contacted by metal interconnections on the top surface of the chip which are used to apply a voltage across the junction. For now, we will ignore the underlying p-type substrate that forms another junction with the n side of the pn junction. The substrate is electrically contacted and set at a voltage (often ground) to ensure that adjacent device structures have minimum electrical interaction.

The essential features of the pn junction can be understood from the one-dimensional simplification shown in Fig. 3.6(b). For mathematical simplicity, the doping concentrations N_a on the p-side and N_d on the n-side are assumed to be constant. Furthermore, it is assumed that N_a and N_d already incorporate any doping compensation effects and thus represent the net concentrations of acceptors and donors.

How do we develop a qualitative picture of the electrostatics of the pn junction? As a start, we consider the case of thermal equilibrium. We know that the hole and electron current densities $J_{po} = 0$ and $J_{no} = 0$ throughout the structure. Therefore, it follows that the hole drift current density must be equal in magnitude and opposite in direction to the hole diffusion current density throughout the pn junction in thermal equilibrium.



► **Figure 3.6** (a) Cross section of a typical pn junction fabricated in an IC process, (b) one-dimensional pn junction consisting of boxed region in (a) with metal contact to n-side added at the bottom. The metallurgical junction (boundary between p-type and n-type regions) is located at $x = 0$.

$$J_{p_o} = J_{p_o}^{dr} + J_{p_o}^{diff} = qp_o\mu_p E_o - qD_p \frac{dp_o}{dx} = 0 \rightarrow qp_o\mu_p E_o = qD_p \frac{dp_o}{dx} \quad (3.26)$$

Similarly, the electron drift and diffusion current densities must cancel

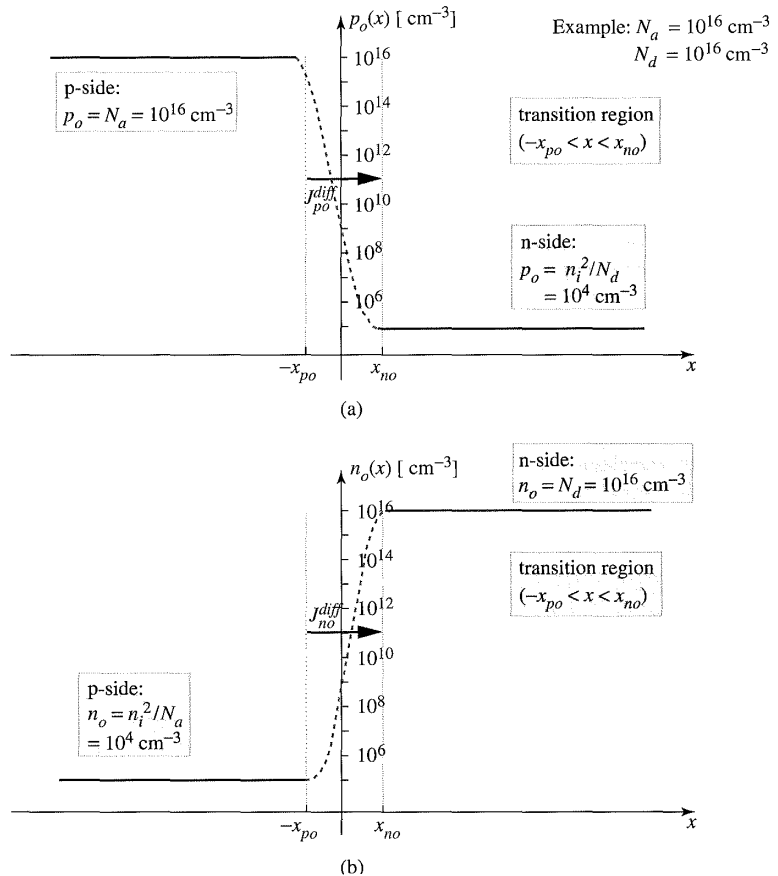
$$J_{n_o} = J_{n_o}^{dr} + J_{n_o}^{diff} = qn_o\mu_n E_o + qD_n \frac{dn_o}{dx} = 0 \rightarrow qn_o\mu_n E_o = -qD_n \frac{dn_o}{dx} \quad (3.27)$$

A rough sketch of the hole concentration $p_o(x)$ is helpful in developing insights into the implications of Eq. (3.26) for the pn junction. Far enough from the metallurgical junction at $x = 0$, the hole concentration on the p-side of the junction must be $p_o(x) = N_a$. In effect, we are asserting that the p-type region can be considered as bulk silicon when it is far enough from the junction since the effects of the pn junction are confined to a region near $x = 0$. We shall quantify the width of the “transition region” when the junction is quantitatively analyzed later in the chapter. However, as a preview of that analysis, the order of magnitude of a typical transition width is $1 \mu\text{m}$. On the n-side of the junction, the hole concentration far enough from the junction is $p_o(x) = n_i^2/n_o = n_i^2/N_d$ —the hole concentration in bulk n-type silicon. In Fig. 3.7(a), the hole concentration $p_o(x)$ is sketched through the pn junction in thermal equilibrium. The transition region is confined to a region of undetermined width $-x_{po} < x < x_{no}$, where $-x_{po}$ is its border on the p-side and x_{no} is its border on the n-side of the junction in thermal equilibrium. Using similar reasoning, we can sketch the electron concentration $n_o(x)$ in thermal equilibrium through the pn junction.

The concentrations in the transition region are shown as dotted lines connecting the bulk concentrations since we do not know the functional forms.

The most obvious feature of the equilibrium concentrations $p_o(x)$ and $n_o(x)$ is the large gradients across the transition region. The diffusion current densities are proportional to these gradients as described in Eqs. (3.26) and (3.27). Figure 3.7 shows that both $J_{p_o}^{diff}$ and $J_{n_o}^{diff}$ are large and positive in the transition region. In order for $J_{p_o} = 0$ and $J_{n_o} = 0$ in the transition region, as they must in thermal equilibrium, it is necessary that there be balancing drift current densities $J_{p_o}^{dr} = -J_{p_o}^{diff}$ and $J_{n_o}^{dr} = -J_{n_o}^{diff}$. Substituting into Eq. (3.26), the required electric field E_o in thermal equilibrium is

$$E_o = \frac{qD_p \frac{dp_o}{dx}}{qp_o\mu_p} = \frac{-qD_n \frac{dn_o}{dx}}{qn_o\mu_n} \quad (3.28)$$



► **Figure 3.7** (a) Qualitative hole concentration $p_o(x)$ and (b) electron concentration $n_o(x)$ in thermal equilibrium. The doping concentrations are 10^{16} cm^{-3} for this example. The equilibrium hole and electron diffusion current densities are both large and positive in the transition region because of the large concentration gradients.

Since we do not know the functional forms for $p_o(x)$ or for $n_o(x)$, we cannot quantify the electric field in the transition region. However, we do know from Eq. (3.28) and from Fig. 3.7 that the electric field in the transition region must be *large* in magnitude and must point in the $-x$ direction so its sign is *negative*. In contrast, outside the transition region p_o and n_o are constants and we conclude that the diffusion current densities and the electric field are zero.

How can a large electric field exist in the transition region? From our understanding of electrostatics, there must be a region of negative and positive charge near $x = 0$. There are four charged species in silicon, two mobile (holes and electrons) and two fixed (ionized donors and ionized acceptors). The charge density in thermal equilibrium $\rho_o(x)$ is given by

$$\rho_o(x) = q(p_o - n_o + N_d - N_a) \quad (3.29)$$

In the transition region on the p-side of the junction over the interval $-x_{po} \leq x \leq 0$, there are very few electrons (see Fig. 3.7(b)) and no donors, so Eq. (3.29) simplifies to

$$\rho_o(x) \equiv q(p_o - N_a), \text{ for } -x_{po} \leq x \leq 0 \quad (3.30)$$

As shown in Fig. 3.7(a), the thermal equilibrium hole concentration $p_o \ll N_a$ in the interval $-x_{po} \leq x \leq 0$, which leads to a *negative* charge density

$$\rho_o(x) < 0, \text{ for } -x_{po} \leq x \leq 0 \quad (3.31)$$

On the n-side of the transition region in the interval $0 \leq x \leq x_{no}$, there are few holes (see Fig. 3.7(a)) and no acceptors, therefore Eq. (3.29) simplifies to

$$\rho_o(x) \equiv q(-n_o + N_d), \text{ for } 0 \leq x \leq x_{no} \quad (3.32)$$

The electron concentration in thermal equilibrium $n_o(x) < N_d$ in this interval (see Fig. 3.7(b)), making the charge density there *positive*

$$\rho_o(x) > 0, \text{ for } 0 \leq x \leq x_{no} \quad (3.33)$$

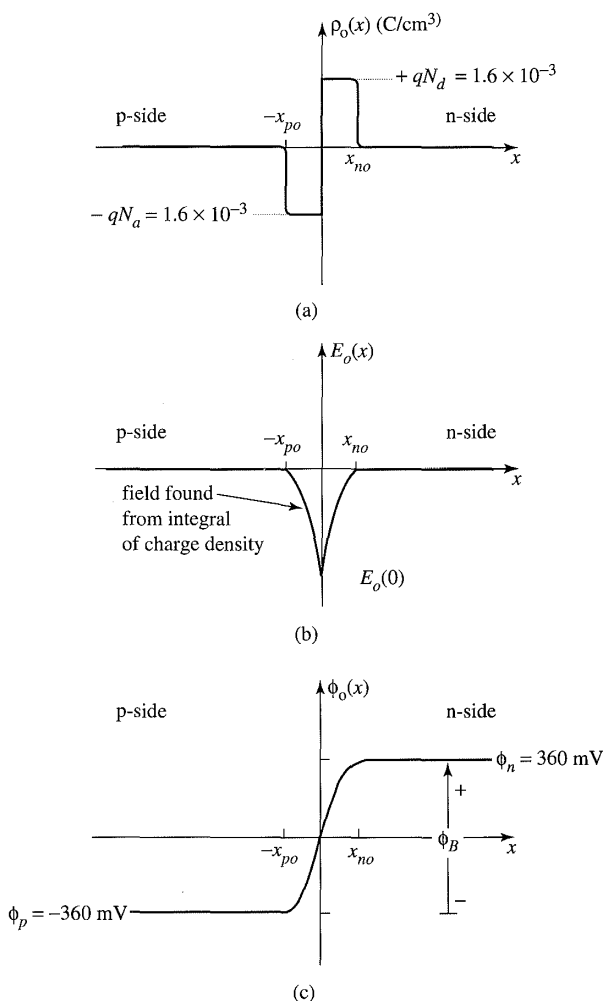
From the sketches of $p_o(x)$ and $n_o(x)$ in Fig. 3.7 and Eqs. (3.30) and (3.32), we can develop the rough sketch of the thermal equilibrium charge density $\rho_o(x)$ in Fig. 3.8(a). Since the doping is symmetrical in Fig. 3.7 ($N_a = N_d = 10^{16} \text{ cm}^{-3}$), the transition region is equally split around $x = 0$ in order to maintain charge neutrality. Given the rapid change in concentrations in Fig. 3.7 (note the logarithmic scale), the slopes in $\rho_o(x)$ at $x = -x_{po}$ and $x = x_{no}$ should be greater than depicted in Fig. 3.8(a). Inside the transition region, the mobile carrier concentrations are negligible for finding the charge density. In effect, the mobile carriers have been depleted from the transition region. We will refer to the high-field region at the junction as the **depletion region**.

The sketches for the electric field $E_o(x)$ and the potential $\phi_o(x)$ in thermal equilibrium are given in Figs. 3.8(b) and 3.8(c). The field is found by graphical integration and is approximately triangular in shape. In the regions away from the junction, the potential is given by the 60 mV rule, as shown in Fig. 3.8(c). The potential on the p-side is

defined as ϕ_p and is -360 mV for this diode, since $N_a = 10^{16} \text{ cm}^{-3}$. On the n-side, the potential is $\phi_n = 360$ mV since $N_d = 10^{16} \text{ cm}^{-3}$. The **built-in potential** ϕ_B is defined as

$$\phi_B = \phi_n - \phi_p = 360 \text{ mV} - (-360 \text{ mV}) = 720 \text{ mV}. \quad (3.34)$$

The sign of the built-in potential is consistent with the direction of the electric field in Fig. 3.7(b) and the fact that the charge density is positive on the n-side of the



► **Figure 3.8** Qualitative electrostatics of the pn junction in thermal equilibrium: (a) charge density, (b) electric field, and (c) electrostatic potential. The doping is $N_a = N_d = 10^{16} \text{ cm}^{-3}$, as given in Fig. 3.7, which leads to $x_{no} = x_{po}$.

transition region. One way of rationalizing the potential barrier at the junction is that it prevents holes from flooding from the p-side (where they are majority carriers) to the n-side (where they are minority carriers.) Of course, the potential barrier also confines the majority electrons to the n-side of the transition region.

As an electrical device structure, the pn junction has an interesting feature: it has a stored charge with no applied voltage, due to the built-in potential barrier. The charge stored per unit area on the p-side is called the **depletion charge**. In thermal equilibrium, the depletion charge Q_{Jo} [units: C/cm²] is

$$Q_{Jo} = -qN_a x_{po} \quad (3.35)$$

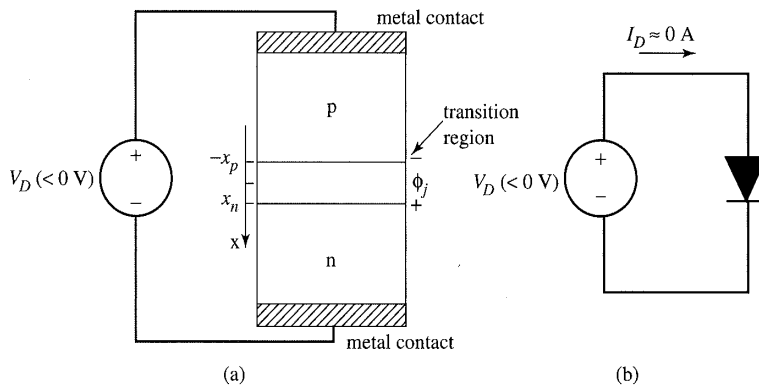
The sign of the depletion charge stored on the p-side of junction is negative, which is consistent with the sign of the potential drop from the p-side to the n-side of the junction in thermal equilibrium:

$$\phi_p - \phi_n = -\phi_B < 0. \quad (3.36)$$

Having developed a qualitative picture of the pn junction in thermal equilibrium, we now extend our understanding to the case of an applied voltage. In this chapter, we are considering only the electrostatics of the junction and will only discuss the reverse-biased situation. The reference polarity for the applied voltage V_D is chosen so that a forward bias is positive, as shown in Fig. 3.9(a) and (b), so for reverse bias $V_D < 0$.

In Fig. 3.9(a), we have defined the potential increase from the p to the n side as the **barrier potential** ϕ_j . As we know from basic electronics, the current through the reverse-biased diode is negligible. Since there can be no resistive potential drops across the p and n bulk regions, the applied voltage must be dropped across the depletion region. Accounting for the presence of the built-in potential ϕ_B , the barrier potential under an applied bias is

$$\phi_j = \phi_B - V_D. \quad (3.37)$$



► **Figure 3.9** (a) pn junction with negative applied voltage V_D (reverse bias) and (b) corresponding circuit schematic.

In thermal equilibrium, $V_D = 0$ and Eq. (3.37) correctly indicates that the barrier potential must equal the built-in potential ϕ_B . Under reverse bias with $V_D < 0$, the barrier at the junction increases, which is consistent with the polarities of V_D and ϕ_j in Fig. 3.9(a).

We have *not* derived Eq. (3.37) from first principles, but rather have established that it correctly accounts for the presence of a built-in barrier at the junction in thermal equilibrium. In Section 3.5, we will investigate in detail how the internal barrier ϕ_j is offset from the externally applied voltage V_D .

What is the effect of the increase in potential barrier on the charge distribution and electric field? More charge is needed on each side of the junction in order to generate enough electric field to yield the larger potential barrier. Since the mobile carriers have been depleted from the depletion region, the charge density is constant at $-qN_a$ on the p-side and $+qN_d$ on the n-side of the junction. In order to get more charge, the width of the depletion region must increase. In Fig. 3.10(a), the edges of the depletion region are shown to have doubled over their thermal-equilibrium values, for the particular reverse bias voltage.

In Fig. 3.10(b), the magnitude of the peak electric field is double that in thermal equilibrium, since the charge on each side of the junction has doubled. Finally, the potential plot in Fig. 3.10(c) shows that the barrier potential under reverse bias has increased over its value in thermal equilibrium: $\phi_j = \phi_B - V_D > \phi_B$. For convenience in plotting $\phi(x)$, we have kept the n-side of the junction fixed at its equilibrium potential and applied the negative diode voltage to the p-side. We can visualize the reverse bias voltage $V_D < 0$ as pulling down the potential on the p-side of the junction, as shown in Fig. 3.10(c).

The effect of reverse bias is to increase the magnitude of the depletion charge q_J , as can be seen by comparing Fig. 3.10(a) with Fig. 3.8(a). As we will derive in Section 3.5, the functional dependence of the depletion charge on the applied bias is:

$$Q_J(V_D) = Q_{Jo} \sqrt{1 - (V_D/\phi_B)} = -qN_a x_{po} \sqrt{1 - (V_D/\phi_B)}, \quad (3.38)$$

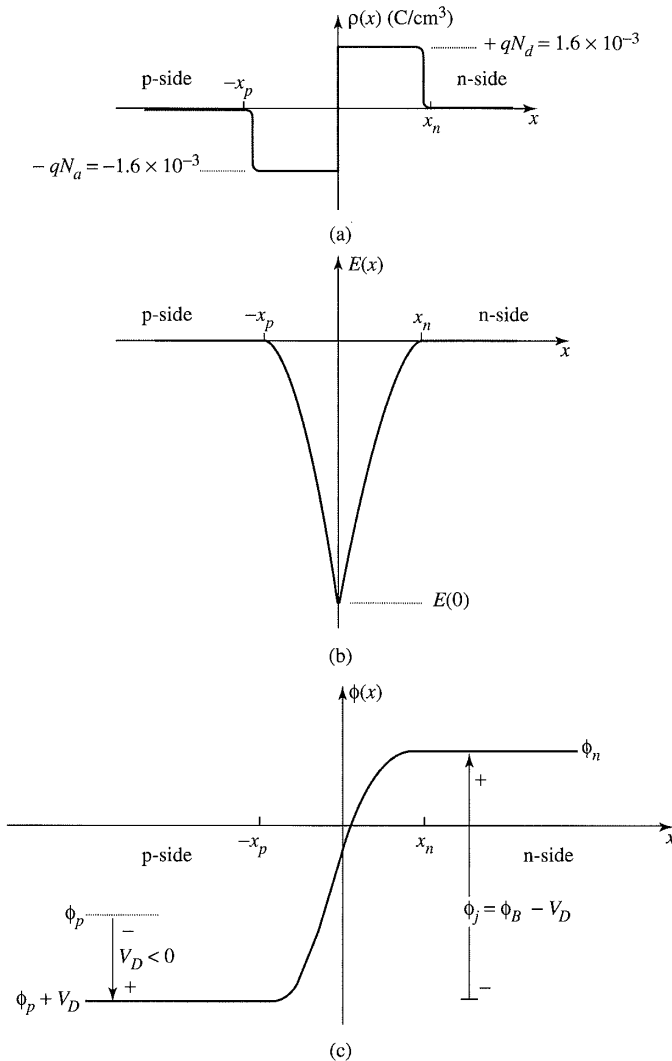
where Q_{Jo} (< 0) is the depletion charge in thermal equilibrium. In summary, the pn junction under reverse bias is a non-linear charge-storage element. Its charge-voltage characteristic in Eq. (3.38) is the starting point for deriving equivalent circuit elements in Section 3.6.

► 3.4 THE pn JUNCTION IN THERMAL EQUILIBRIUM

From the previous section, we have gained a “feel” for the pn junction in equilibrium and under reverse bias, which will be valuable in analyzing the electrostatics of the pn junction. Our approach will be to investigate the functional form of the charge density in the transition region and develop an expedient approximation that will simplify the mathematics. We will then solve for the electric field and potential in the transition region and connect these solutions to the known potential in the regions far away from the junction.

3.4.1 The Depletion Approximation

With confidence that we have a correct picture of the electrostatics in Fig. 3.8, we now make a very important approximation that will greatly simplify the mathematics.



► **Figure 3.10** Qualitative electrostatics of the pn junction under reverse bias $V_D < 0$ which is sufficient to double the width of the depletion region: (a) charge density, (b) electric field, and (c) electrostatic potential. The doping is $N_a = N_d = 10^{16} \text{ cm}^{-3}$, as in Fig. 3.9.

First, we assume that the charge density is zero outside of the transition region near the junction. These regions are “bulk” silicon as defined in Section 2.3. Recall that bulk silicon is electrically neutral and that the majority carrier concentration is equal to the net doping concentration, to an excellent approximation. Inside the transition region, the charge density is given by the general expression

$$\rho_o(x) = q(p_o - n_o + N_d - N_a) \cong \begin{cases} q(p_o - N_a) & (-x_{po} \leq x \leq 0) \\ q(N_d - n_o) & (0 \leq x \leq x_{no}) \end{cases} \quad (3.39)$$

where the approximations involve neglecting the minority electrons on the p-side and the minority holes on the n side—both many orders of magnitude less the majority carrier concentrations and doping concentrations. Since the pn junction is in thermal equilibrium, we can substitute for the carrier concentrations in terms of the potential from Eqs. (3.21) and (3.22)

$$\rho_o(x) \cong \begin{cases} q \left(n_i e^{-\phi_o(x)/V_{th}} - N_a \right) & (-x_{po} \leq x \leq 0) \\ q \left(N_d - n_i e^{\phi_o(x)/V_{th}} \right) & (0 \leq x \leq x_{no}) \end{cases} \quad (3.40)$$

The exponential functions of the potential present a daunting challenge in solving for $\phi_o(x)$, which leads us to explore whether there is a way to make a further simplification of Eq. (3.40). On the p-side, the hole concentration falls off exponentially with distance for $x > -x_{po}$ as shown qualitatively in Fig. 3.7(a). On the n-side, the electron concentration is similarly negligible for points well inside the transition region. For points very near the edges of the transition region, the majority carrier concentrations are close to the doping concentrations and cannot be neglected. We propose a simplifying approximation to Eq. (3.40) that will be referred to as the **depletion approximation**.

depletion approximation

$$\rho_o(x) \approx \begin{cases} -qN_a & (-x_{po} \leq x \leq 0) \\ qN_d & (0 \leq x \leq x_{no}) \end{cases} \quad \text{and} \quad \rho_o(x) = \begin{cases} 0 & (x \leq -x_{po}) \\ 0 & (x_{no} \leq x) \end{cases} \quad (3.41)$$

In effect, we consider the transition region to be *completely depleted* of mobile holes and electrons. The depletion approximation is slightly inaccurate near the edges of the depletion region since it overestimates the charge density there by neglecting the majority carriers. In Fig. 3.8(a), the charge density $\rho_o(x)$ is shown to taper off at the edges of the junction, which is what Eq. (3.40) predicts and what actually occurs. The depletion approximation in Eq. (3.41) gives a reasonably accurate solution for the depletion region width.

What is the motivation for making this approximation? The answer is simple—the mathematics of solving Poisson’s Equation using Eq. (3.40) in the depletion region is too messy. By making the depletion approximation and dividing the pn junction into a depletion region, sandwiched between bulk p and n regions, we can develop relatively simple solutions for the potential, field, and depletion region width. These solutions will be useful for gaining an appreciation of the essential physics of pn junctions.

Several device simulators are available for numerically solving the two- or three-dimensional versions of Poisson's Equation in semiconductors should we desire to study a particular device structure with more accuracy.

Quantitative Analysis Using the Depletion

3.4.2 Approximation

In Eq. (3.41), we have an approximate expression for the charge density $\rho_o(x)$ in thermal equilibrium. We now integrate the charge density twice to find first the electric field $E_o(x)$ and then the electrostatic potential $\phi_o(x)$. Gauss's Law relates the charge density to the derivative of the electric field

$$\frac{dE_o}{dx} = \frac{\rho_o(x)}{\epsilon_s} \quad (3.42)$$

where $\epsilon_s = 11.7 \epsilon_0$ is the electric permittivity of silicon. On the p-side of the depletion region $-x_{po} < x < 0$, we can integrate Eq. (3.42) and find that

$$E_o(x) = \int_{-x_{po}}^x \frac{\rho_o(x')}{\epsilon_s} dx' + E_o(x = -x_{po}) = \int_{-x_{po}}^x \frac{-qN_a}{\epsilon_s} dx' + 0 = -\frac{qN_a}{\epsilon_s} (x - (-x_{po})) \quad (3.43)$$

where we have used the fact that the electric field is zero at the edge of the depletion region in thermal equilibrium since there is no charge density in the bulk p region. We can integrate the field and find an expression for the electrostatic potential on the p-side, $-x_{po} < x < 0$

$$\phi_o(x) = \int_{-x_{po}}^x -E_o(x') dx' + \phi_o(x = -x_{po}) = \frac{qN_a}{2\epsilon_s} (x + x_{po})^2 + \phi_p \quad (3.44)$$

where ϕ_p is the potential of the p-type bulk p region in thermal equilibrium. According to Eq. (3.22), this potential is

$$\phi_p = -V_{th} \ln\left(\frac{N_a}{n_i}\right) \quad (3.45)$$

Using exactly the same approach, we can integrate the charge density in Eq. (3.41) starting from the n-side of the depletion region $0 < x < x_{no}$

$$E_o(x = x_{no}) = E_o(x) + \int_x^{x_{no}} \frac{\rho_o(x')}{\epsilon_s} dx' = E_o(x) + \int_x^{x_{no}} \frac{qN_d}{\epsilon_s} dx' = E_o(x) + \frac{qN_d}{\epsilon_s} (x_{no} - x) \quad (3.46)$$

in which we have been careful to keep the limits of integration consistent with the positive x direction. Since the electric field $E_o(x = x_{no}) = 0$ at the edge of the depletion region, we can solve Eq. (3.46) for $E_o(x)$ on the n-side of the depletion region $0 < x < x_{no}$

$$E_o(x) = -\frac{qN_d}{\epsilon_s}(x_{no} - x) \quad (3.47)$$

The potential for $0 \leq x \leq x_n$ can be found by direct integration of the electric field

$$\phi_o(x = x_{no}) = \phi_o(x) + \int_x^{x_{no}} -E(x') dx' = \phi_o(x) + \int_x^{x_{no}} \frac{qN_d}{\epsilon_s}(x_{no} - x') dx' \quad (3.48)$$

Solving for $\phi_o(x)$ and evaluating the integral, we find

$$\phi_o(x) = \phi_n - \frac{qN_d}{2\epsilon_s}(x_{no} - x)^2 \quad (0 \leq x \leq x_n) \quad (3.49)$$

where ϕ_n is the potential of the bulk n region from Eq. (3.20)

$$\phi_n = V_{th} \ln\left(\frac{N_d}{n_i}\right) \quad (3.50)$$

The two solutions for the electric field must connect at $x = 0$, the metallurgical junction, since there is no sheet of charge at this surface (see the discussion on boundary conditions for the electric field in Section 3.1). By substituting $x = 0$ into Eqs. (3.43) and (3.47), we find that

$$-\frac{qN_a}{\epsilon_s}(0 + x_{po}) = -\frac{qN_d}{\epsilon_s}(x_{no} - 0) \quad (3.51)$$

Simplifying, we find

$$N_a x_{po} = N_d x_{no} \quad (3.52)$$

This result states that the negative charge (per unit area) on the p-side of the depletion region $-qN_a x_{po}$, is equal in magnitude and opposite in sign to the positive charge on the n-side: $+qN_d x_{no}$. Equation (3.52) is hardly surprising since we are safe in assuming that the total charge in IC device structures is zero, as discussed in Section 3.1.

In order to find expressions for the edges of the depletion region $-x_{po}$ and x_{no} , we first use Eq. (3.52) to substitute for one of them into the two solutions for $\phi_o(x)$, Eqs. (3.44) and (3.49). We then require that they match at the metallurgical junction $x = 0$

$$\frac{qN_a}{2\epsilon_s}(0 + x_{po})^2 + \phi_p = \phi_n - \frac{qN_d}{2\epsilon_s}(x_{no} - 0)^2 = \phi_n - \frac{qN_d}{2\epsilon_s}\left(\frac{N_a}{N_d}x_{po}\right)^2 \quad (3.53)$$

Solving for x_{po} and substituting the built-in potential $\phi_B = \phi_n - \phi_p$, we find that

$$x_{po} = \sqrt{\left(\frac{2\epsilon_s\phi_B}{qN_a}\right)\left(\frac{N_d}{N_d + N_a}\right)} \quad (3.54)$$

The width on the n-side can now be found directly from Eq. (3.52)

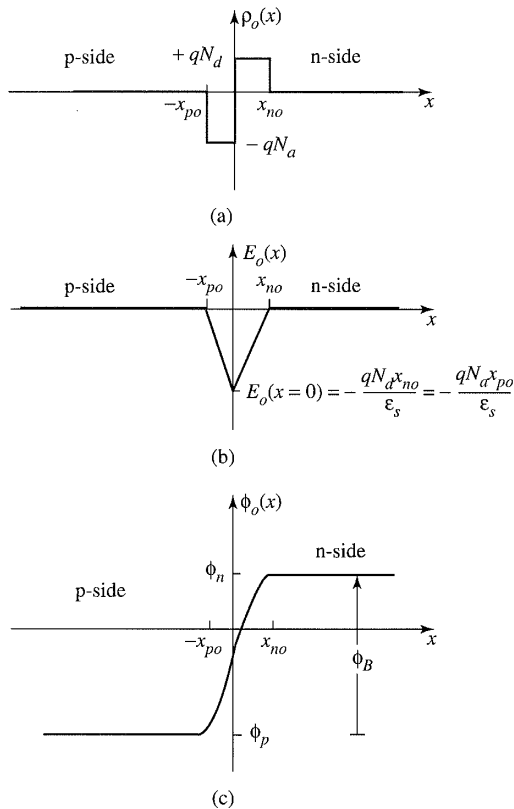
$$x_{no} = \sqrt{\left(\frac{2\epsilon_s\phi_B}{qN_d}\right)\left(\frac{N_a}{N_d+N_a}\right)} \quad (3.55)$$

The sum of Eqs. (3.54) and (3.55) yields X_{do} , which is the width of the depletion region in thermal equilibrium

$$X_{do} = x_{no} + x_{po} = \sqrt{\left(\frac{2\epsilon_s\phi_B}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \quad (3.56)$$

equilibrium depletion width

Figure 3.11 summarizes the electrostatics of the pn junction in thermal equilibrium using the depletion approximation.



► **Figure 3.11** (a) Charge density, (b) electric field, and (c) potential in thermal equilibrium based on the depletion approximation.

EXAMPLE 3.4 Depletion Regions in Thermal Equilibrium

In this example, we will investigate the electrostatics of three pn junctions with progressively more asymmetrical doping. Our goal is to plot $\rho_o(x)$, $E_o(x)$, and $\phi_o(x)$ for junctions 1–3 in thermal equilibrium. The p-side is located on the negative side of the x axis as in Fig. 3.5.

Junction	N_a [cm^{-3}]	N_d [cm^{-3}]
1	5×10^{16}	5×10^{16}
2	5×10^{16}	2×10^{17}
3	5×10^{16}	5×10^{17}

SOLUTION

We start by applying the Eqs. (3.23 and 3.25) to find the potentials on the p and n sides and the built-in voltage.

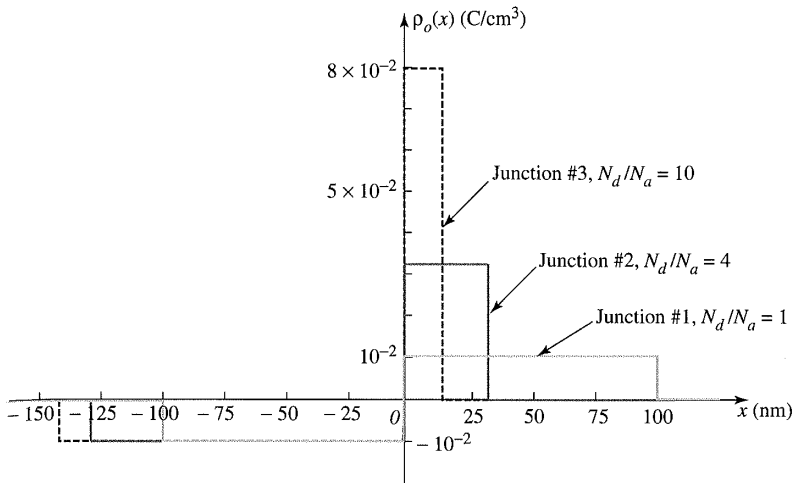
Junction	ϕ_p [mV]	ϕ_n [mV]	ϕ_B [mV]
1	–402	402	804
2	–402	438	840
3	–402	462	864

Note that the built-in voltage is a weak function of the n-side doping concentration, increasing less than 10% between junctions #1 and #3 that have an order-of-magnitude difference in N_d . We substitute into Eqs. (3.54) and (3.55) to find the edges of the depletion region on the p-side and n-side. The results for junction 2 are

$$x_{po} = \sqrt{\left(\frac{(2)(11.7)(8.85 \times 10^{-14} \text{ Fcm}^{-1})(0.840 \text{ V})}{(1.6 \times 10^{-19} \text{ C})(5 \times 10^{16} \text{ cm}^{-3})} \right) \left(\frac{2 \times 10^{17}}{2 \times 10^{17} + 5 \times 10^{16}} \right)} = 134 \text{ nm}$$

$$x_{no} = \sqrt{\left(\frac{(2)(11.7)(8.85 \times 10^{-14} \text{ Fcm}^{-1})(0.840 \text{ V})}{(1.6 \times 10^{-19} \text{ C})(2 \times 10^{17} \text{ cm}^{-3})} \right) \left(\frac{5 \times 10^{16}}{2 \times 10^{17} + 5 \times 10^{16}} \right)} = 33 \text{ nm}$$

In the plot of the charge density $\rho(x)$ for the three cases in Fig. Ex3.4A, note that the ratios of the depletion widths x_{po}/x_{no} are inversely related to the doping ratios N_d/N_a .



► **Figure Ex3.4A** Charge density in thermal equilibrium for the three junctions.

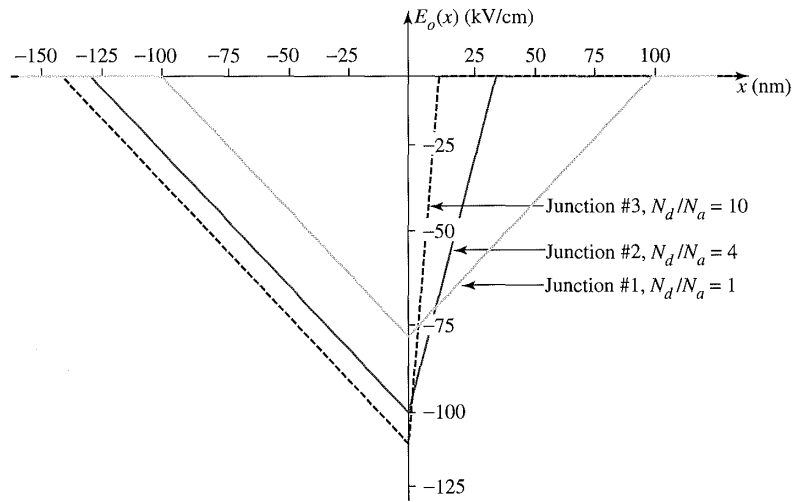
The numerical results for the depletion widths are summarized in this table.

Junction	x_{po} [nm]	x_{no} [nm]
1	102	102
2	134	33
3	143	14.3

To plot the electric field in equilibrium, we need only find its value at $x = 0$ from Eq. (3.47) since we know the shape of $E(x)$ from Fig. 3.11(b). For junction 2, the calculation is

$$E_o(0) = -\frac{qN_d x_{no}}{\epsilon_s} = \frac{(1.6 \times 10^{-19} \text{ C}) (2 \times 10^{17} \text{ cm}^{-3}) (3.3 \times 10^{-6} \text{ cm})}{(11.7) (8.85 \times 10^{-14} \text{ Fcm}^{-1})} = -102 \text{ kV/cm}$$

The peak electric field weakly depends on the doping ratio of the junction when the concentration on one side is fixed. The electric field is plotted in Fig. Ex3.4B, with the numerical results for the peak electric field summarized in the following table.



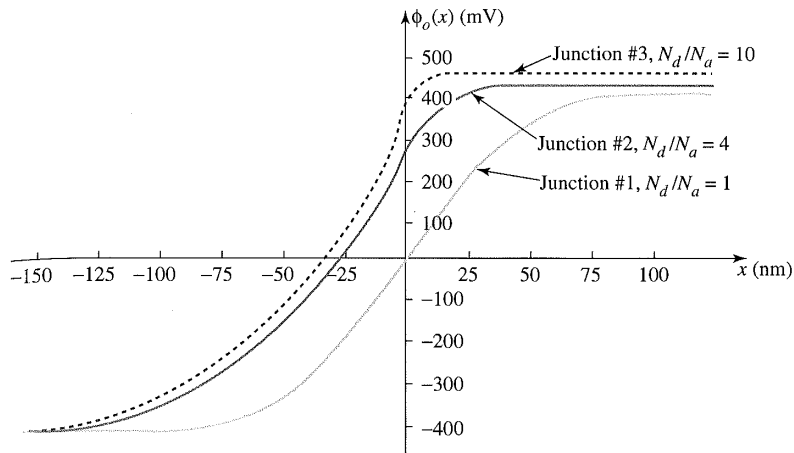
► **Figure Ex3.4B** Equilibrium electric field $E_o(x)$ for the three pn junctions in Example 3.4.

Junction	$E_o(0)$ [kV/cm]
1	-79
2	-102
3	-110.5

Poisson's Equation tells us that if the charge distribution is constant, then the potential will behave quadratically as shown in Eqs. (3.44) and (3.49). Evaluating Eq. (3.44) for junction 2, we find that the potential at $x = 0$ is

$$\phi_o(0) = \frac{(1.6 \times 10^{-19} \text{ C}) (5 \times 10^{16} \text{ cm}^{-3}) (1.34 \times 10^{-5} \text{ cm})^2}{2 (11.7) (8.85 \times 10^{-14} \text{ F/cm})} - 402 \text{ mV} = 289 \text{ mV}$$

In summary, only a factor of 10 difference in doping is needed for the depletion region to be mostly located on the lightly doped side. Many IC pn junctions have higher doping ratios and can be considered “one-sided” for practical purposes.

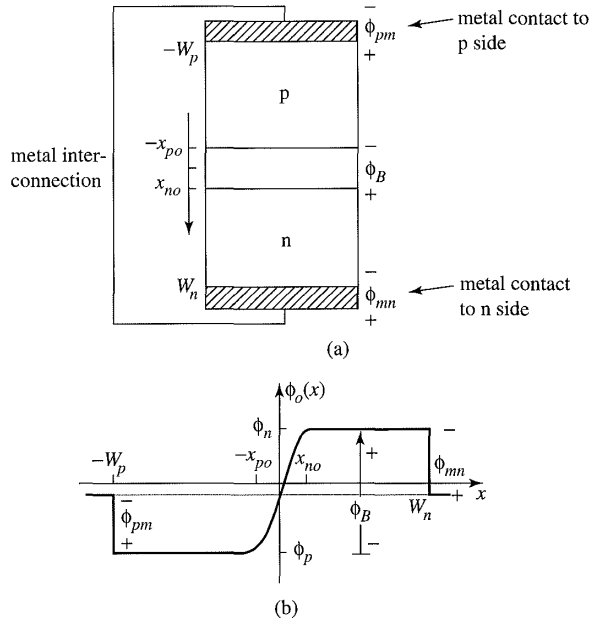


► **Figure Ex3.4C** Equilibrium potential $\phi_o(x)$ for the three pn junctions having different doping ratios.

3.4.3 Metal-Semiconductor Contact Potentials

The fact that a pn junction in thermal equilibrium has a built-in potential barrier of approximately 1 V is initially puzzling. For example, the sum of the potential drops around the short-circuited pn junction in Fig. 3.12(a) must be zero since there are no voltage or current sources in the loop and the diode is not illuminated. How then is the built-in potential barrier cancelled around the loop? The metal and bulk silicon regions have constant potentials in equilibrium. Inspection of Fig. 3.12(a) shows the only possibility is that built-in potential drops occur at the metal contacts to the p and n bulk regions. The extended thermal equilibrium potential plot in Fig. 3.12(b) represents these potential changes qualitatively as abrupt jumps at the metal-silicon contacts. We will leave the analysis of the potential variation at the contacts to more advanced courses. In this text, we will ignore that there is a non-zero width to these potential changes.

These contact potentials occur between any dissimilar pair of materials because of the difference in the potential energy of the conduction electrons across the junction. By properly engineering the metal-silicon contact, it is possible to approach an **ohmic contact**. The essential property of an ohmic contact is that it presents no barrier to hole or electron flow in either direction. These specially processed metal-silicon junctions behave like batteries, in that their potential drops are not functions of the forward or reverse current through them. The abrupt changes in potential ϕ_{pm} and ϕ_{nn} shown in Fig. 3.12(b) indicate qualitatively the narrow region of potential change that occurs in ohmic metal-silicon contacts. Note that the metal is *not* at zero potential in Fig. 3.12(b) since the potential reference for the plot is the *internal* silicon reference. The point where $\phi(x) = 0$ occurs when the electron and hole concentrations equal the intrinsic concentration, which is located inside the depletion region on the n-side of the metallurgical junction, from Fig. 3.12(b).



► **Figure 3.12** (a) pn diode including ohmic metal-silicon contacts, (b) extended plot of potential in thermal equilibrium including the metal interconnections.

By summing the potential drops around the loop in Fig. 3.12(a), Kirchhoff's voltage law (KVL) around the loop yields

$$0 = \phi_{pm} + \phi_B + \phi_{mn} \quad (3.57)$$

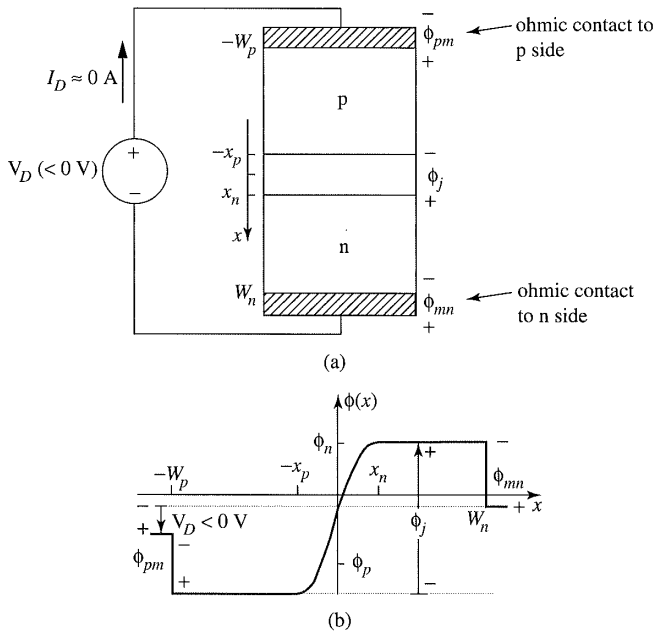
Solving for the sum of the contact potentials, we find that

$$\phi_B = -(\phi_{pm} + \phi_{mn}) \quad (3.58)$$

At first glance, it seems strange that the potential drops at the contacts would have to add up to cancel the built-in potential of the junction. Were this not the case, KVL would imply that current would flow in thermal equilibrium when a resistor is connected across the metal contacts to the p and n regions. This conclusion violates our basic understanding of the meaning of equilibrium; namely, that the net current must be zero for this state.

► 3.5 THE pn JUNCTION UNDER REVERSE BIAS

Given our quantitative model for the pn junction in thermal equilibrium, we are in position to analyze how the electrostatics are changed by application of a reverse bias voltage. In Fig. 3.13, we have connected a battery $V_D < 0$ V across the pn junction.



► **Figure 3.13** (a) pn junction with negative applied voltage V_D (reverse bias) and (b) plot of the potential across the structure under reverse bias including the ohmic contacts. The “o” subscript has been removed from all variables since the structure is no longer in thermal equilibrium.

Since V_D is negative, it lowers the potential of the p-side of the junction with respect to that of the n-side, which we will consider fixed at ϕ_n . (Alternatively, we could consider the p-side fixed and then $V_D < 0$ V would raise the n-side potential. Recall from Section 3.1 that only potential differences matter.) The effect of the reverse bias is to increase the potential barrier ϕ_j between the p and n bulk regions as shown in Fig. 3.13(b).

Since we are no longer in equilibrium, we must consider whether or not there is a significant current I_D through the pn junction. Raising the potential barrier between the p-side and n-side of the junction is *not* likely to result in a large net carrier transport. In fact, reverse-biased diodes are considered open circuits to a first approximation. We will use this fact and assume $I_D \approx 0$ A for the reverse-biased diode in this chapter. In Chapter 6 we will verify this assumption in a detailed study of the diode under forward and reverse bias.

The potential barrier ϕ_j across the depletion region under reverse bias can be found by applying Kirchhoff’s voltage law. Note that the metal-silicon contact potentials at the ohmic contacts are unaffected by the applied voltage. The sum of the potential drops is given by

$$-V_D - \phi_{pm} - \phi_j - \phi_{mn} = 0 \quad (3.59)$$

Solving for the barrier potential, we find that

$$\phi_j = (-\phi_{pm} - \phi_{mn}) - V_D = \phi_B - V_D \quad (3.60)$$

where we have substituted Eq. (3.58) for the built-in potential. We asserted this result for ϕ_j in our first-pass treatment in Section 3.3. Figure 3.13(b) shows the potential variation through the structure. The negative applied voltage increases the barrier height and separates the potential levels of the metal interconnections, which is consistent with our concept of a voltage source.

Now that the barrier height is known as a function of the applied voltage V_D , we can proceed with the analysis of the electrostatics under reverse bias. After applying the depletion approximation, we must solve for the electric field and the potential in the depletion region, assuming it is confined to the interval $-x_p(V_D) < x < x_n(V_D)$. The boundaries of the depletion region are functions of the applied bias since they will change with the barrier height ϕ_j .

Rather than integrate the charge density $\rho(x)$ over the depletion region, we can avoid needless mathematics by recognizing that the form of $\rho(x)$ is *identical* to the charge density $\rho_o(x)$ in thermal equilibrium. The only change is that the boundaries are now $-x_p$ and x_n and the barrier height is ϕ_j . Therefore, the previous solutions for $\phi_o(x)$ and $E_o(x)$ can be adapted to the reverse bias case by simply substituting $\phi_j = \phi_B - V_D$ for ϕ_B . The edges of the depletion region under reverse bias ($V_D < 0$) are given in Eqs. (3.61) and (3.62), and their sum yields the total width in Eq. (3.63)

$$x_p(V_D) = \sqrt{\left(\frac{2\epsilon_s(\phi_B - V_D)}{qN_a}\right)\left(\frac{N_d}{N_d + N_a}\right)} = x_{po}\sqrt{1 - (V_D/\phi_B)} \quad (3.61)$$

$$x_n(V_D) = \sqrt{\left(\frac{2\epsilon_s(\phi_B - V_D)}{qN_d}\right)\left(\frac{N_a}{N_d + N_a}\right)} = x_{no}\sqrt{1 - (V_D/\phi_B)} \quad (3.62)$$

$$X_d(V_D) = \sqrt{\left(\frac{2\epsilon_s(\phi_B - V_D)}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = X_{do}\sqrt{1 - (V_D/\phi_B)} \quad (3.63)$$

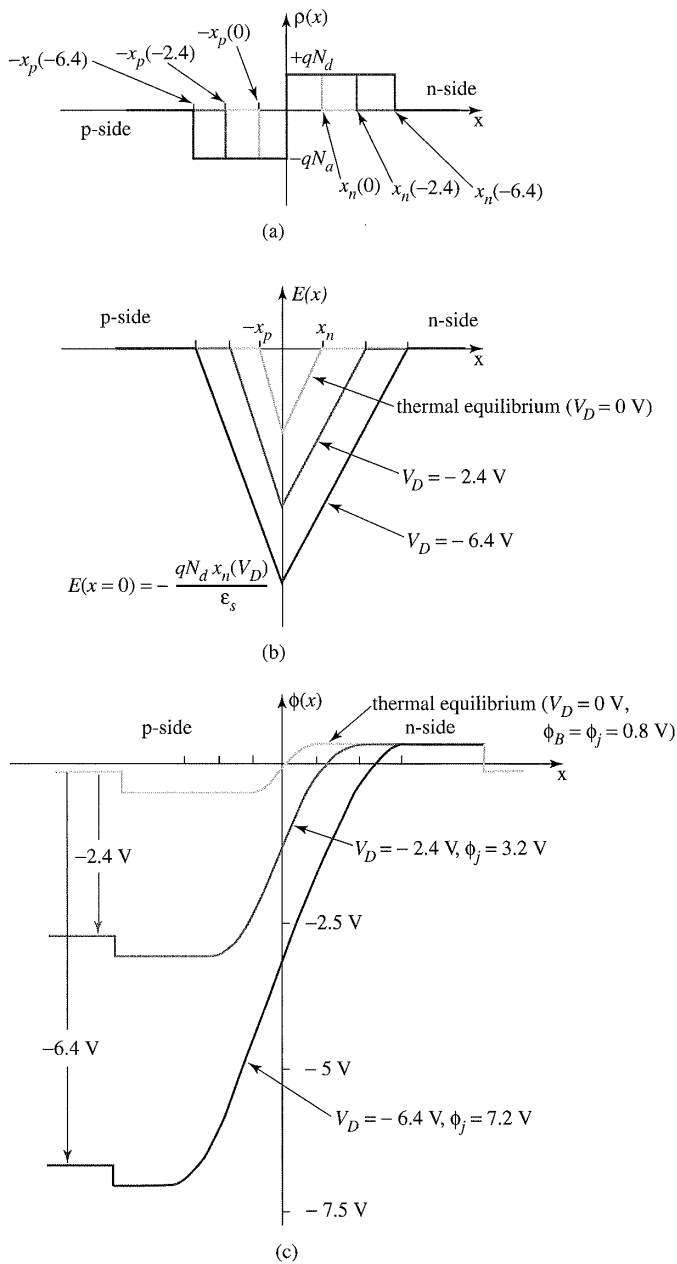
depletion widths under reverse bias

where the thermal equilibrium values x_{po} , x_{no} , and X_{do} are defined in Eqs. (3.54)–(3.56). Figure 3.14 shows the effects on the depletion width, electric field, and potential of applying voltages of $V_D = -2.4$ V and $V_D = -6.4$ V across a pn junction with a thermal equilibrium barrier height of $\phi_B = 0.8$ V. These values of reverse bias will double and triple the widths of the depletion region over the thermal equilibrium width since

$$\sqrt{1 - (V_D/\phi_B)} = \sqrt{1 - ((-2.4)/0.8)} = \sqrt{4} = 2 \quad \text{and} \quad (3.64)$$

$$\sqrt{1 - (V_D/\phi_B)} = \sqrt{1 - ((-6.4)/0.8)} = \sqrt{9} = 3 \quad (3.65)$$

We conclude this section with a numerical example.



► **Figure 3.14** pn junction under reverse biases $V_D = -2.4$ V and $V_D = -6.4$ V. (a) charge, (b) electric field, and (c) potential, according to the depletion approximation.

EXAMPLE 3.5 Depletion Regions in Reverse Bias

Consider a pn junction with doping $N_a = 10^{16} \text{ cm}^{-3}$ and $N_d = 10^{18} \text{ cm}^{-3}$. (a) What applied voltage is required for $X_d = 1.5 \mu\text{m}$? (b) What distance x_n does the depletion region penetrate into the n-side of the junction? (c) Plot the potential $\phi(x)$ for this applied reverse bias keeping the n-side of the junction fixed and neglecting contact potentials.

SOLUTIONS

(a) In thermal equilibrium, the potential in the bulk regions can be found using Eqs. (3.23) and (3.25): $\phi_n = 480 \text{ mV}$, $\phi_p = -360 \text{ mV}$, and $\phi_B = \phi_n - \phi_p = 840 \text{ mV}$. The thermal equilibrium depletion width is found using Eq. (3.56)

$$X_{do} = \sqrt{\frac{2(11.7)(8.85 \times 10^{-14} \text{ F cm}^{-1})(0.84 \text{ V})}{1.6 \times 10^{-19} \text{ C}} \left(\frac{1}{10^{18} \text{ cm}^{-3}} + \frac{1}{10^{16} \text{ cm}^{-3}} \right)} = 0.33 \mu\text{m}$$

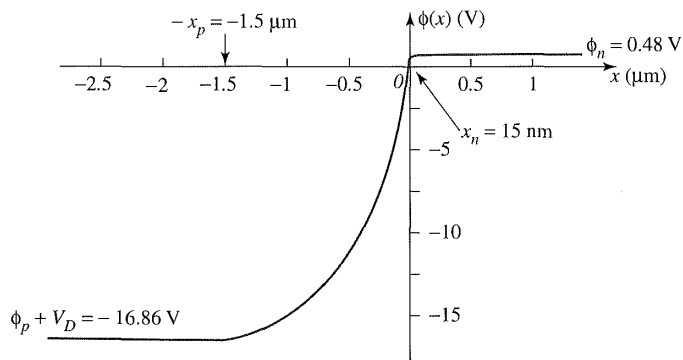
We can now use Eq. (3.63) to solve for the applied voltage V_D necessary for the depletion region to grow to $X_d = 1.5 \mu\text{m}$

$$X_d(V_D) = X_{do} \sqrt{1 - \frac{V_D}{\phi_B}} = (0.33 \mu\text{m}) \sqrt{1 - \frac{V_D}{0.84 \text{ V}}} = 1.5 \mu\text{m}$$

which yields $V_D = -16.5 \text{ V}$.

(b) In order to find the width on the n-side of the junction, we can substitute into Eq. (3.62) after calculating x_{no} or recall that the charge per unit area on the n-side is equal and opposite to that on the p-side, which implies that $x_n N_d = x_p N_a$. From (a), the total depletion width is $X_d = x_n + x_p = 1.5 \mu\text{m}$. Eliminating x_p and noting that $N_d = 100 N_a$, it follows that $x_n = x_p / 100 \cong X_d / 100 = 15 \text{ nm}$.

(c) In plotting the potential across the junction, the n-side remains at $\phi_n = 0.48 \text{ V}$ while the p-side potential drops to $\phi_p + V_D = -16.86 \text{ V}$.



► **Figure Ex3.5** Potential plot for Example 3.5 pn junction under applied bias of $V_D = -16.5 \text{ V}$.

► 3.6 DEPLETION CAPACITANCE

The pn junction under reverse bias is a two-terminal charge-storage element. It is essential to connect the electrostatics of the reverse-biased pn junction with its circuit models. We will explain modeling of this device structure from several perspectives since the pn junction is universal in ICs and also, since this is our first exposure to circuit modeling.

As we have seen from Sections 3.3–3.5, the charge on the p-side of the depletion region is a function of the applied voltage. Repeating Eq. (3.38), the depletion charge varies with the applied voltage as

$$Q_J(V_D) = -qN_a x_{po} \sqrt{1 - (V_D/\phi_B)} = -qN_a x_p(V_D), \quad V_D \leq 0, \quad (3.66)$$

with the right-hand side coming from Eq. (3.61). Unlike a conventional capacitor, the depletion charge does not change linearly with applied voltage.

To proceed further, we must become more precise in defining symbols for electrical quantities. The convention in this text is that an upper-case symbol with an upper-case subscript (e.g., Q_J or V_D) will refer to a DC or average quantity. A lower-case symbol with an upper-case subscript (e.g., q_J or v_D) will indicate the total quantity, including its time variation.

We have not considered the possibility that the applied voltage or the depletion charge may be functions of time in our analysis thus far. We will model the time-varying depletion charge by simply substituting q_J and v_D into Eq. (3.66). This “quasi-static” approach is an excellent approximation over the range of frequencies for microelectronics. Our starting point for developing circuit models for the reverse-biased pn junction is

$$q_J(v_D) = -qN_a x_{po} \sqrt{1 - (v_D/\phi_B)}, \quad v_D \leq 0 \quad (3.67)$$

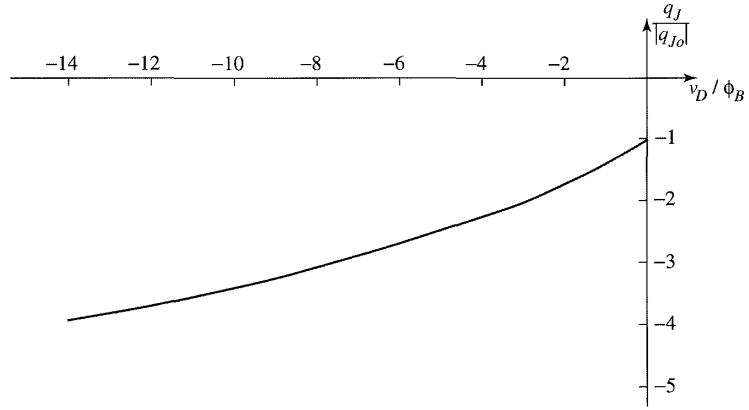
Figure 3.15 is a plot of Eq. (3.67) for negative applied voltages. We have normalized q_J by its magnitude in thermal equilibrium $qN_a x_{po}$ and v_D by the built-in potential ϕ_B .

A numerical circuit simulator such as SPICE incorporates Eq. (3.67) into its model for a reverse-biased pn junction with an abrupt change in doping concentration at the metallurgical junction. For hand analysis, however, it is quite burdensome to have nonlinear models in the node or loop equations. Therefore, we will develop an approach to linearizing the charge-storage characteristics of the pn junction that will be valid under conditions that often occur in practical cases. We will derive an equivalent capacitor that describes the incremental charge storage for small deviations from a specified DC voltage. This technique, termed **small-signal modeling**, is a powerful approach to nonlinear circuit elements and will be used later for transistors.

In order to further develop this technique, we introduce the special case where the total depletion charge q_J can be written as the sum of its DC (average) value Q_J and an incremental (i.e., very small) component that is considered time-varying $q_j = q_j(t)$

$$q_J = Q_J + q_j, \text{ where } |q_j| \ll |Q_J| \quad (3.68)$$

small-signal modeling



► **Figure 3.15** Depletion charge q_J , normalized to the magnitude of the equilibrium charge $|q_{Jo}| = qN_a x_{po}$, as a function of the applied voltage v_D , normalized to ϕ_B , the built-in potential barrier.

For this case, we can also express the applied voltage v_D as the sum of its DC value V_D , and a much smaller time-varying component $v_d = v_d(t)$

$$v_D = V_D + v_d \text{ where } |v_d| \ll |V_D| \quad (3.69)$$

The lower-case variables with lower-case subscripts in these equations are reserved for “small signals” which meet the test of being very small compared with the average value of the signal. It is helpful to interpret Eqs. (3.68) and (3.69) on a graph of the depletion charge before pursuing the mathematical analysis further.

3.6.1 Graphical Interpretation

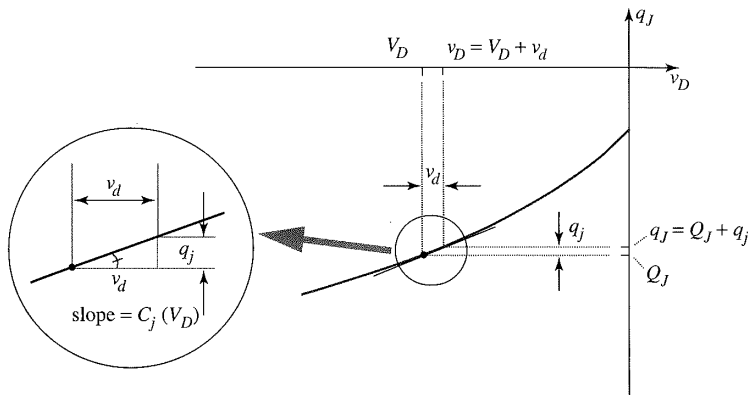
Figure 3.16 shows the depletion charge as a function of the applied voltage with the function $q_J(v_D)$ evaluated at V_D and at $v_D = V_D + v_d$. For illustrative purposes, we have assumed that $v_d \ll V_D$ is a constant, positive voltage. From Eq. (3.68), the small-signal depletion charge q_j is given by

$$q_j = q_J - Q_J = q_J(v_D) - q_J(V_D) \quad (3.70)$$

in which we have substituted for the DC depletion charge $Q_J = q_J(V_D)$. In Fig. 3.16, the small-signal depletion charge is the product of the small-signal voltage and the slope of the function $q_J(v_D)$, evaluated at $v_D = V_D$

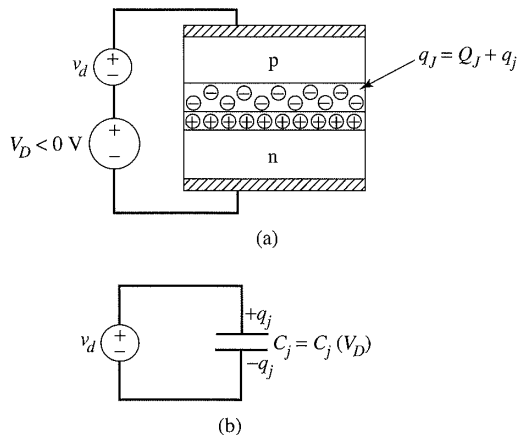
$$q_j = (\text{slope}) \times v_d \quad (3.71)$$

The slope has units of $(\text{C}/\text{cm}^2)/\text{V} = \text{F}/\text{cm}^2$ and is defined as the **depletion capacitance** $C_j(V_D)$. As shown in Fig. 3.16, the slope of $q_J(v_D)$ decreases with increasing reverse bias on the junction. We will consider the physical interpretation of this fact after developing an equation for the depletion capacitance.



► **Figure 3.16** Graphical interpretation of the depletion capacitance as the slope of the depletion-charge vs. applied voltage curve evaluated at the point $q_J(V_D) = Q_J$.

The concept of small-signal modeling can be viewed from a circuit perspective as well. In Fig. 3.17(a), the total circuit quantities are broken into their DC and small-signal components. In many cases, we are concerned only with the small-signal behavior of the device structure. Therefore, it is convenient to work with the small-signal equivalent circuit for the reverse-biased pn junction shown in Fig. 3.17(b). Needless to say, this circuit describes only the response of the reverse-biased junction to small changes in the applied voltage. In order to find the numerical value for the capacitance from the slope of $q_J(v_D)$, we must first know the DC bias voltage V_D .



► **Figure 3.17** (a) Circuit model with the total voltage $v_D = V_D + v_d$ and the total charge q_J broken into their DC and small-signal components and (b) small-signal equivalent circuit for the reverse-biased pn junction.

3.6.2 Mathematical Formulation

From Fig. 3.16, we can apply calculus to find an expression for the depletion capacitance. Since v_d is a small increment on the average diode voltage V_D , we need to retain only the linear term in the Taylor expansion for the depletion charge at v_D

$$q_J(v_D) = q_J(V_D) + \left[\frac{dq_J}{dv_D} \right]_{V_D} \times (v_D - V_D) \quad (3.72)$$

The total depletion charge $q_J(V_D)$ is the sum of its DC and small-signal components

$$q_J(v_D) = Q_J + q_j = q_J(V_D) + q_j \quad (3.73)$$

Substitution of Eq. (3.73) and the small-signal voltage $v_d = v_D - V_D$ into the Taylor expansion results in cancellation of the DC depletion charge

$$q_J(V_D) + q_j = q_J(V_D) + \left[\frac{dq_J}{dv_D} \right]_{V_D} \times v_d \quad \text{and} \quad (3.74)$$

$$q_j = \left[\frac{dq_J}{dv_D} \right]_{V_D} \times v_d \quad (3.75)$$

We identify the derivative in Eq. (3.75) with the slope in Eq. (3.71) and therefore, the depletion capacitance is defined as

depletion capacitance

$$C_j = C_j(V_D) = \left[\frac{dq_J}{dv_D} \right]_{V_D} \quad (3.76)$$

in which the second equality is a reminder that C_j is a function of the DC bias voltage.

In order to evaluate the functional form of the depletion capacitance, we substitute the expression for the depletion charge as a function of the diode voltage from Eq. (3.67) into the definition

$$C_j = \frac{d}{dv_D} \{ -qN_a x_{po} \sqrt{1 - v_D/\phi_B} \} \Big|_{V_D} = \frac{qN_a x_{po}}{2\phi_B \sqrt{1 - V_D/\phi_B}} = \frac{C_{jo}}{\sqrt{1 - V_D/\phi_B}} \quad (3.77)$$

in which the various constants are collected and defined as C_{jo} . Closer inspection of the final equality in Eq. (3.77) shows that C_{jo} is the depletion capacitance in thermal equilibrium, or the **zero-bias** capacitance, $C_j(V_D = 0 \text{ V}) = C_{jo}$.

There should be a simple physical interpretation for C_{jo} , so we substitute from the definition of x_{po} in Eq. (3.54) to find

$$C_{jo} = \frac{qN_a x_{po}}{2\phi_B} = \frac{qN_a}{2\phi_B} \sqrt{\left(\frac{2\epsilon_s \phi_B}{qN_a}\right) \left(\frac{N_d}{N_d + N_a}\right)} = \sqrt{\frac{q\epsilon_s}{2\phi_B} \left(\frac{N_a N_d}{N_d + N_a}\right)} \quad (3.78)$$

The right-hand equality has many common terms with X_{do} , the depletion width in thermal equilibrium (Eq. (3.56)). Factoring out the permittivity of silicon, Eq. (3.78) simplifies to

$$C_{jo} = \epsilon_s \sqrt{\frac{q}{2\epsilon_s \phi_B} \left(\frac{1}{N_a} + \frac{1}{N_d}\right)^{-1}} = \frac{\epsilon_s}{X_{do}} \quad (3.79)$$

zero-bias depletion capacitance

As a final expression for the depletion capacitance that will be useful in the next section, we substitute for C_{jo} in Eq. (3.77)

$$C_j(V_D) = \frac{C_{jo}}{\sqrt{1 - V_D/\phi_B}} = \frac{\epsilon_s}{X_{do}\sqrt{1 - V_D/\phi_B}} = \frac{\epsilon_s}{X_d(V_D)} \quad (3.80)$$

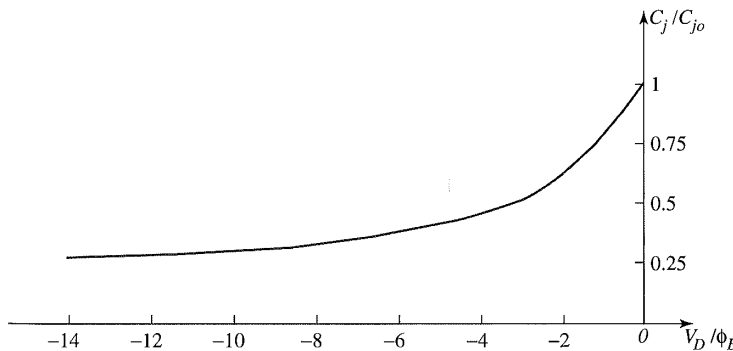
depletion capacitance for reverse bias

where we have substituted for the depletion width under reverse bias in Eq. (3.63).

The normalized depletion capacitance C_j/C_{jo} is plotted in Fig. 3.18. The capacitance decreases with increasing reverse bias, which is consistent with its interpretation as the slope of the depletion charge function plotted in Fig. 3.15. Since a typical equilibrium barrier height $\phi_B \approx 1$ V, the normalized voltage is roughly the same as the DC bias.

3.6.3 Physical Interpretation

Our final perspective on the depletion capacitance will be to develop some insight into the physical meaning of what appears to be a purely mathematical concept. An important clue is provided by Eq. (3.80), which is identical to the capacitance of a par-



► **Figure 3.18** Depletion capacitance, normalized to its zero-bias (thermal equilibrium) value, as a function of the applied DC voltage, normalized to the barrier height ϕ_B in thermal equilibrium.

allel-plate capacitor with its electrodes separated by the depletion width $X_d(V_D)$ at the particular DC voltage. What charges are separated by X_d ? From Eq. (3.76), the depletion capacitance is the ratio of the small-signal depletion charge q_j to the small-signal voltage v_d

$$C_j = \frac{q_j}{v_d} = \frac{\epsilon_s}{X_d} \quad (3.81)$$

which indicates that the small-signal charge layers $\pm q_j$ are separated by X_d .

In Fig. 3.19, the charge density in the depletion region is plotted, first for the case where the diode voltage is $V_D < 0$ V in (a), and then where a positive small-signal voltage is added to give $v_D = V_D + v_d$ in (a). The depletion region narrows slightly in the second case since the positive v_d means that $v_D > V_D$. The depletion charge q_j for (b) is less negative than is Q_j in (a) since the depletion region is narrower for v_D .

We graphically subtract (a) from (b) to find the incremental charge density that accounts for the small-signal depletion charge q_j since by definition $q_j = q_j - Q_j$. The result is plotted in Fig. 3.19(c), in which the change in the charge density due to the addition of v_d is confined to the edges of the depletion region. In the limit of $v_d \rightarrow 0$, the small-signal charges $\pm q_j$ become sheets that are separated by a gap width of X_d , which explains the physical origin of the parallel-plate formula in Eq. (3.81).

Although we have derived Eq. (3.81) for the case of an abrupt pn junction with constant doping, it is in fact a general result for any pn junction. The functional dependence of the depletion width on the reverse bias will depend on the details of the particular dopant distributions and consequently, the dependence of C_j on the reverse bias may differ slightly from that in Fig. 3.18.

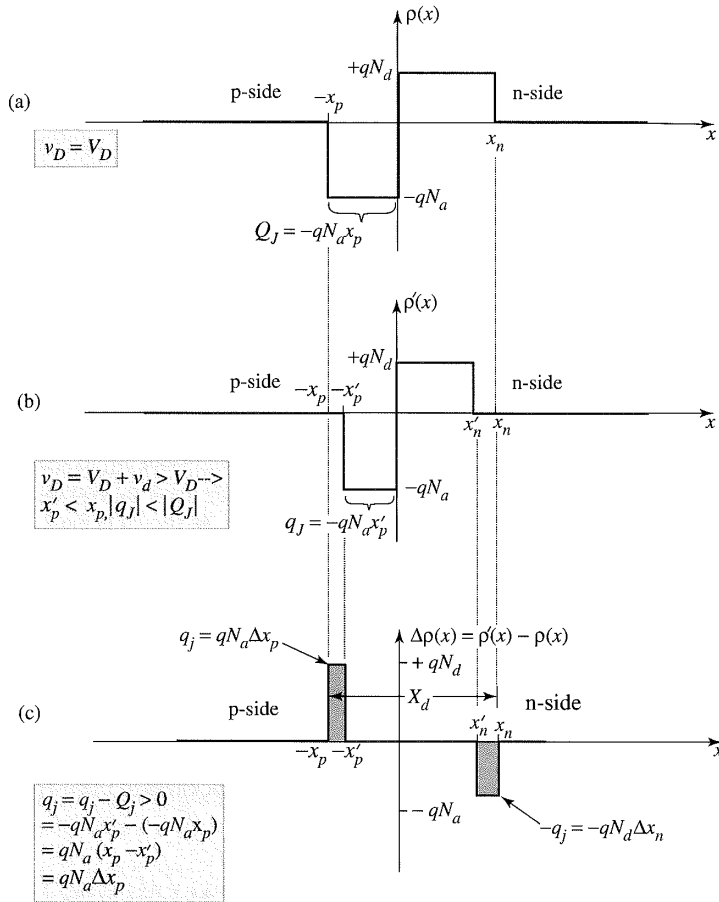
3.6.4 SPICE Models for IC pn Junctions

SPICE is a powerful circuit simulator that is commonly used to simulate integrated circuits. In SPICE, the depletion capacitance of a pn junction under reverse bias is modeled by the following equation

$$C_j = \frac{CJO}{(1 - V_D/VJ)^M} \quad (3.82)$$

in which the SPICE symbols are $CJO = C_{j0}$, the zero-bias (equilibrium) capacitance, $VJ = \phi_B$, the built-in barrier voltage, and M is the grading coefficient of the junction. From Eq. (3.80), $M = 0.5$ for the abrupt pn junction that we have modeled in this chapter. For IC pn junctions, M is usually curve-fit to measurements of $C_j(V_D)$ or is extracted from a numerical device simulator. Typical values for M range from 0.3 to 0.7.

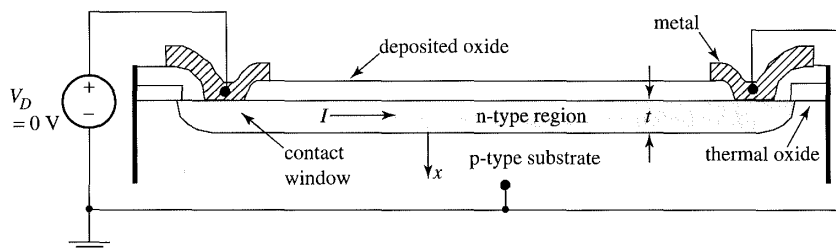
The effect of changing the width of the depletion region is that a displacement current must be supplied through the adjacent bulk silicon regions. The small-signal junction capacitance incorporates this effect into the circuit model, which is illustrated by the following example. This example revisits the ion-implanted resistor and adds charge-storage at the pn junction to the small-signal model.



► **Figure 3.19** (a) Charge density $\rho(x)$ in depletion region for a reverse bias of $V_D < 0$, (b) charge density $\rho'(x)$ in depletion region for a perturbed reverse bias $V_D = V_D + v_d$ with $v_d > 0$, and (c) difference $\Delta\rho(x)$ between (b) and (a) showing incremental depletion charge $\pm q_j$ separated by approximately the depletion width X_d . Note that the magnitude of v_d is exaggerated in order to clarify its effect on the depletion region width.

EXAMPLE 3.6 Depletion Capacitance of an IC Resistor

(a) For the ion-implanted resistor described in Ex. 2.5 and shown in cross section below, find the depletion width x_{no} for $V_D = 0$ V.



► **Figure Ex3.6A** Cross section of the IC resistor from Example 2.5. The doping concentrations are $N_d = 2.5 \times 10^{16} \text{ cm}^{-3}$ and $N_a = 2.5 \times 10^{15} \text{ cm}^{-3}$. The junction depth is $t = 0.4 \text{ } \mu\text{m} = 400 \text{ nm}$, the width of the n-type region is $W = 2.5 \text{ } \mu\text{m}$, and its length is $L = 20 \text{ } \mu\text{m}$. The contact regions are each $3W \times 3W$ in area, as shown in Fig. 2.22(a).

SOLUTION

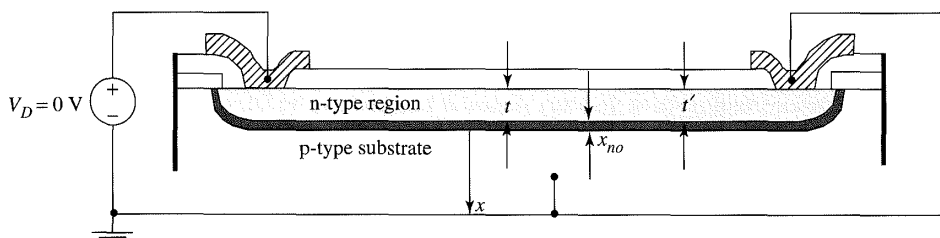
Since N_a is a factor of 10 less than N_d , most of the depletion region will reside on the p-side of the junction. In order to use Eq. (3.55) to find the depletion edge in thermal equilibrium, we first find the potentials of each side under zero bias using Eqs. (3.23) and (3.25): $\phi_n = 384 \text{ mV}$, $\phi_p = -324 \text{ mV}$. The depletion edge on the n-side is then $x_{no} = 58 \text{ nm}$ from Eq. (3.55).

(b) Recalculate the sheet resistance by correcting the thickness of the n-type region for the depletion at the junction.

SOLUTION

There are no carriers in the depletion region, so the thickness of the n-type bulk region t' is

$$t' = t - x_{no} = 400 \text{ nm} - 58 \text{ nm} = 342 \text{ nm}$$



► **Figure Ex3.6B** IC resistor showing the junction depth t and the narrowing of the n-type region due to depletion width x_{no} on the n-side of the junction.

The sheet resistance increases due to the encroachment of the depletion region into the n-type region as shown in Fig. Ex3.6B.

$$R_{\square} = \frac{1}{q N_d \mu_n t'} = \frac{1}{q N_d \mu_n (t - x_{no})}$$

$$R_{\square} = \frac{1}{(1.6 \times 10^{-19} \text{ C})(1050 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1})(2.5 \times 10^{16} \text{ cm}^{-3})(400 \text{ nm} - 58 \text{ nm})} = 6.9 \text{ k}\Omega/\square$$

represents a 15% increase over the value in Ex. 2.5 where the depletion region was neglected. The resistance is $R = (6.9 \text{ k}\Omega/\square)(9.3\square) = 64.2 \text{ k}\Omega$.

(c) Calculate the depletion capacitance C_R in fF between the n region and the p-type substrate assuming the DC voltage $V_D = 0 \text{ V}$.

SOLUTION

The area of the ion-implanted n-type region from the layout (including the two contact areas) in Example 2.5 is

$$A_R = L W + 2(3W)^2 = 162.5 \mu\text{m}^2 = 1.625 \times 10^{-6} \text{ cm}^2$$

where the area of each contact region $(3W)^2$ is included.

The depletion capacitance (per unit area) for $V_D = 0$ is

$$C_{jo} = \frac{\epsilon_s}{X_{do}} = \frac{(11.7)(8.85 \times 10^{-14} \text{ F cm}^{-1})}{0.635 \mu\text{m}} = 16.3 \times 10^{-9} \text{ F/cm}^2$$

in which we used $X_{do} = x_{no} + x_{po} = x_{no} + (N_d/N_a) x_{no} = 11 x_{no} = 635 \text{ nm}$. Multiplying by the area A_R , the capacitance is

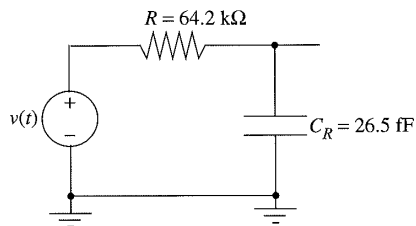
$$C_R = C_{jo} A_R = (16.3 \times 10^{-9} \text{ F/cm}^2)(1.625 \times 10^{-6} \text{ cm}^2) = 26.5 \text{ fF}$$

If a DC reverse bias is applied across the pn junction and the depletion region widens, then the resistance will increase, due to further reduction of the bulk n region thickness, and the capacitance will decrease, due to the wider depletion region.

(d) Draw a simple small-signal model of the ion-implanted resistor for the case where $V_D = 0 \text{ V}$.

SOLUTION

The ion-implanted resistor with depletion capacitance is best modeled as a series of N segments with resistance R/N and capacitance C_R/N . For simplicity, we lump the resistance and capacitance into single elements in the circuit below in Fig. Ex3.6C.



► **Figure Ex3.6C** Small-signal circuit for the ion-implanted resistor in Example 2.5 with zero DC bias between the n region and p-type substrate. The resistance includes the effect of encroachment by the depletion region. The capacitance is the depletion capacitance of the entire n region.

► 3.7 THE MOS CAPACITOR: A FIRST PASS

We now turn our attention to the more complex, but far more important metal-oxide-semiconductor (MOS) capacitor. Figure 3.20 shows a cross section of the three-layer sandwich in which a heavily doped, n-type polycrystalline silicon layer serves as the “metal” layer. In practice, polysilicon is the most common material used for the “metal” in integrated MOS structures, having supplanted aluminum and other metal films since the 1970s. The oxide film is a thermally grown layer of SiO_2 . The silicon substrate could be either p-type or n-type—we will first concentrate on the former. Metal interconnections to the polysilicon gate and to the p-type bulk silicon are shown schematically in Fig. 3.20.

3.7.1 MOS Capacitor in Thermal Equilibrium

As we did with the pn junction, we will start our investigation of MOS electrostatics with the structure in thermal equilibrium. Since the oxide is a near-perfect insulator, we short together the gate and bulk metal layers to enable the charge exchange needed to reach equilibrium as indicated in Fig. 3.20. For the pn junction, $V_D = 0$ V also was a necessary condition for equilibrium.

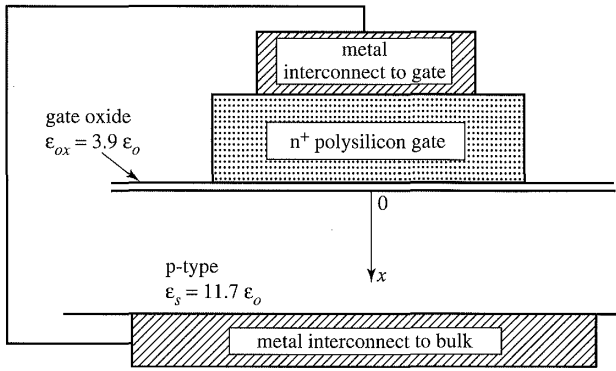
The boundary condition on the potential in the silicon, far from the oxide, is given by Eq. (3.25)

$$\phi_p = -V_{th} \ln\left(\frac{N_a}{n_i}\right) \quad (3.83)$$

For a typical doping concentration of 10^{17} cm^{-3} , the potential of the p-type bulk region far from the surface is $\phi_p = -420$ mV. The n^+ designation on the polysilicon gate indicates that it is very heavily doped with donors, to the point that its potential can be taken as the maximum possible for silicon in thermal equilibrium

$$\phi_{n^+} = 550 \text{ mV} \quad (3.84)$$

Based on our intuitive understanding of electrostatics, we can understand the qualitative electrostatics in the MOS structure in thermal equilibrium. The sign of the potential drop (gate positive, p-type silicon negative) means that the electric field E_o



► **Figure 3.20** MOS capacitor with p-type substrate. Gate and bulk metal contacts are shorted together for thermal equilibrium.

is positive (points from gate to bulk, in the $+x$ direction as defined in Fig. 3.20). Therefore, a positive charge must be present on the bottom of the polysilicon gate and there must be a balancing negative charge in the p-type silicon underlying the gate oxide. The gate oxide itself will be considered a charge-free perfect insulator in this text. In more advanced courses, the effect of oxide charge on the MOS structure will be investigated in detail.

As we saw with the pn junction in Section 3.2, negative charge density in p-type silicon can occur if a depletion region forms under the gate oxide. Figure 3.21 shows a sketch of the charges in the MOS capacitor with p-type substrate, in the state of thermal equilibrium. Since the gate is highly conductive n^+ polysilicon, the gate charge Q_{Go} (units: C/cm^2) is depicted as a sheet charge located on its bottom surface. An intuitive picture of why the depletion region forms is to view the positive charge on the gate as repelling mobile holes in the silicon under the gate oxide, leaving behind the immobile, negatively charged acceptor ions to a depth X_{do} . The gate charge Q_{Go} is equal and opposite to the bulk charge Q_{Bo} in the silicon substrate

$$Q_{Go} = -Q_{Bo} = -qN_aX_{do} \quad (3.85)$$

Just as we found for the pn junction, there is charge stored on the MOS capacitor in thermal equilibrium. It is helpful to sketch the potential variation through the MOS structure in equilibrium. Example 3.3 analyzed the electrostatics of the MOS capacitor with the charge distribution in Fig. 3.21. Figure 3.22 is a sketch of the potential $\phi(x)$, which is based on the analysis in Ex. 3.3.

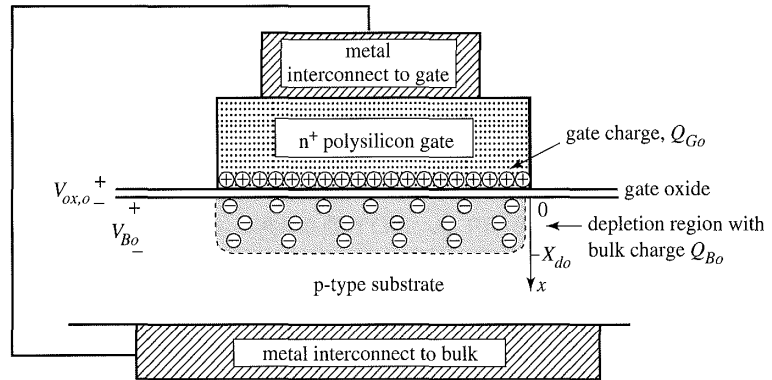
The potential drop across the MOS structure is the difference between the potentials of the n^+ polysilicon gate and the p-type substrate. For the plot in Fig. 3.22, we have used a substrate doping concentration of $N_a = 10^{17} \text{ cm}^{-3}$ and the total drop is:

$$\phi_{n+} - \phi_p = 550 \text{ mV} - (-420 \text{ mV}) = 970 \text{ mV} \quad (3.86)$$

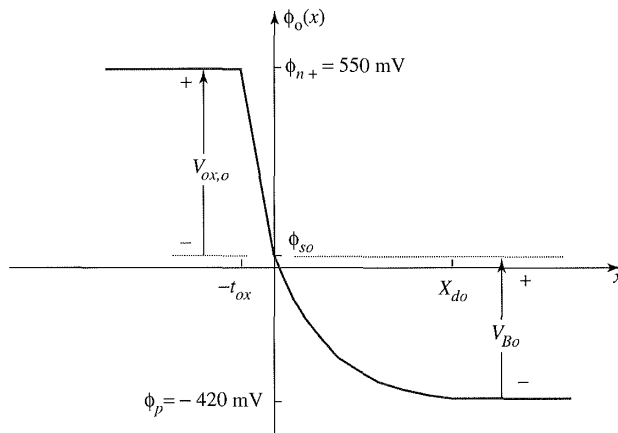
In Figs. 3.21 and 3.22, the potential drop across the capacitor is divided into the sum of the drop across the oxide $V_{ox,o}$ and the drop across the depletion region V_{Bo}

$$\phi_{n+} - \phi_p = V_{ox,o} + V_{Bo} \quad (3.87)$$

Finally, we have defined the potential at $x = 0$ (the SiO_2 -silicon interface) as the thermal equilibrium **surface potential**, ϕ_{so} .



► **Figure 3.21** Qualitative picture of charge distribution in an MOS capacitor with p-type substrate in thermal equilibrium.



► **Figure 3.22** Potential plot for MOS capacitor with p-type substrate in thermal equilibrium. The substrate doping concentration is $N_a = 10^{17} \text{ cm}^{-3}$.

3.7.2 MOS Capacitor under Applied Bias

The effect on the gate charge of an applied voltage V_{GB} is rather complicated. The easiest place to start is by applying a voltage that is equal and opposite to the “built-in” voltage across the MOS capacitor in thermal equilibrium. We define this special voltage as the **flatband voltage**, V_{FB} :

$$V_{FB} = -(\phi_{n+} - \phi_p) \quad (3.88)$$

flatband voltage for
p-type substrate

For a substrate acceptor concentration of 10^{17} cm^{-3} , the flatband voltage is $V_{FB} = -970 \text{ mV}$. In plotting the potential variation under applied bias, we will keep the substrate fixed and move the gate. With $V_{GB} = V_{FB} = -970 \text{ mV}$, the n^+ polysilicon gate’s potential is pulled down to $550 \text{ mV} - 970 \text{ mV} = -420 \text{ mV}$, as shown in Fig. 3.23 (a). Therefore, there is no internal potential drop across the MOS capacitor when $V_{GB} = V_{FB}$ and as a result, the gate charge is zero:

$$Q_G(V_{GB} = V_{FB}) = 0 \quad (3.89)$$

If we make the applied voltage more negative than the flatband voltage, $V_{GB} < V_{FB}$, then the gate potential drops below that of the substrate. The gate charge therefore becomes negative, as shown in Fig. 3.23(b), and the nature of the charge in the substrate changes. The identity of the positive substrate charge is not hard to determine, since there are plenty of positively charged holes in the p-type silicon that can accumulate under the gate oxide, as shown in Fig. 3.23(b), to cancel the negative gate charge. The MOS capacitor is said to be in **accumulation** for $V_{GB} < V_{FB}$. The potential and charge density in accumulation are shown in Fig. 3.23(b). These plots are identical to those for the parallel-plate capacitor analyzed in Ex. 3.1. Therefore, the gate charge in accumulation is linearly related to the difference between the applied voltage and the flatband voltage:

$$Q_G = C_{ox}(V_{GB} - V_{FB}) \text{ for } V_{GB} \leq V_{FB} \quad (3.90)$$

gate charge in
accumulation for p-type
substrate

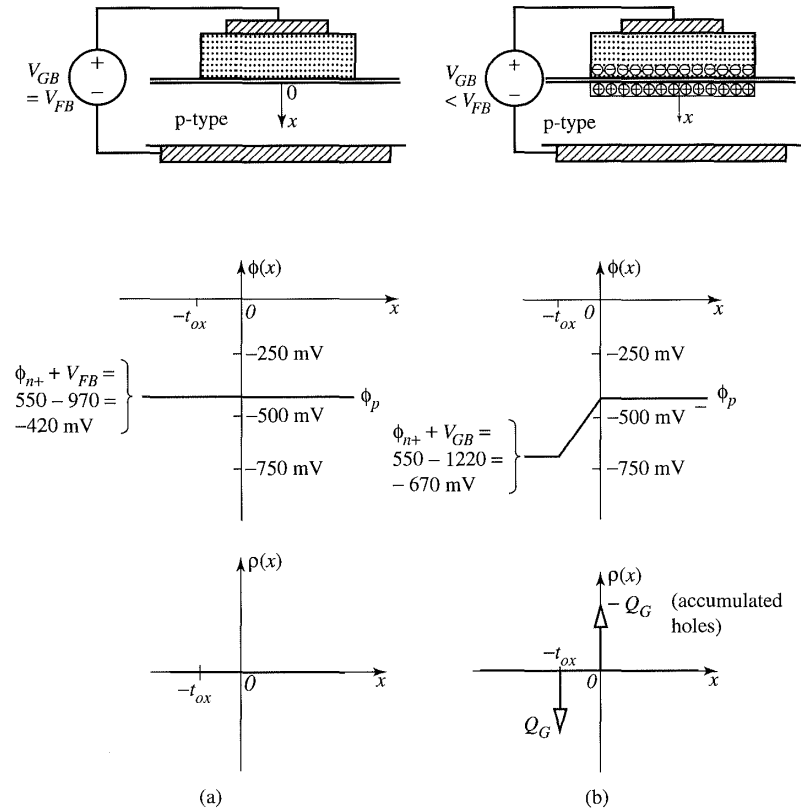
where $C_{ox} = \epsilon_{ox}/t_{ox}$ is the capacitance per unit area of the gate oxide.

We now apply voltages $V_{GB} > V_{FB}$. Since $V_{GB} = 0 \text{ V} > V_{FB}$, we already have examined this case when we considered the MOS capacitor in thermal equilibrium. The gate charge is positive and increases with increasing applied bias

$$Q_G(V_{GB}) = -Q_B = -(-qN_aX_d) = qN_aX_d(V_{GB}) \text{ (depletion)} \quad (3.91)$$

where $X_d(V_{GB})$ indicates the dependence of depletion width on V_{GB} . In order to quantify $X_d(V_{GB})$, we need to find the dependence of the surface potential on the gate-bulk voltage V_{GB} , which we will do in the next section.

Figure 3.24(a) shows the electrostatics of the MOS capacitor biased in **depletion**, with $V_{GB} = 250 \text{ mV}$. For this bias voltage, the electrostatic analysis in the next section shows that the surface potential is $\phi_s = 185 \text{ mV}$. The surface potential corresponds to silicon that is slightly n-type—opposite to the p-type substrate. Even though the MOS capacitor is under applied bias, $J_n = 0$ and $J_p = 0$ through the structure due to



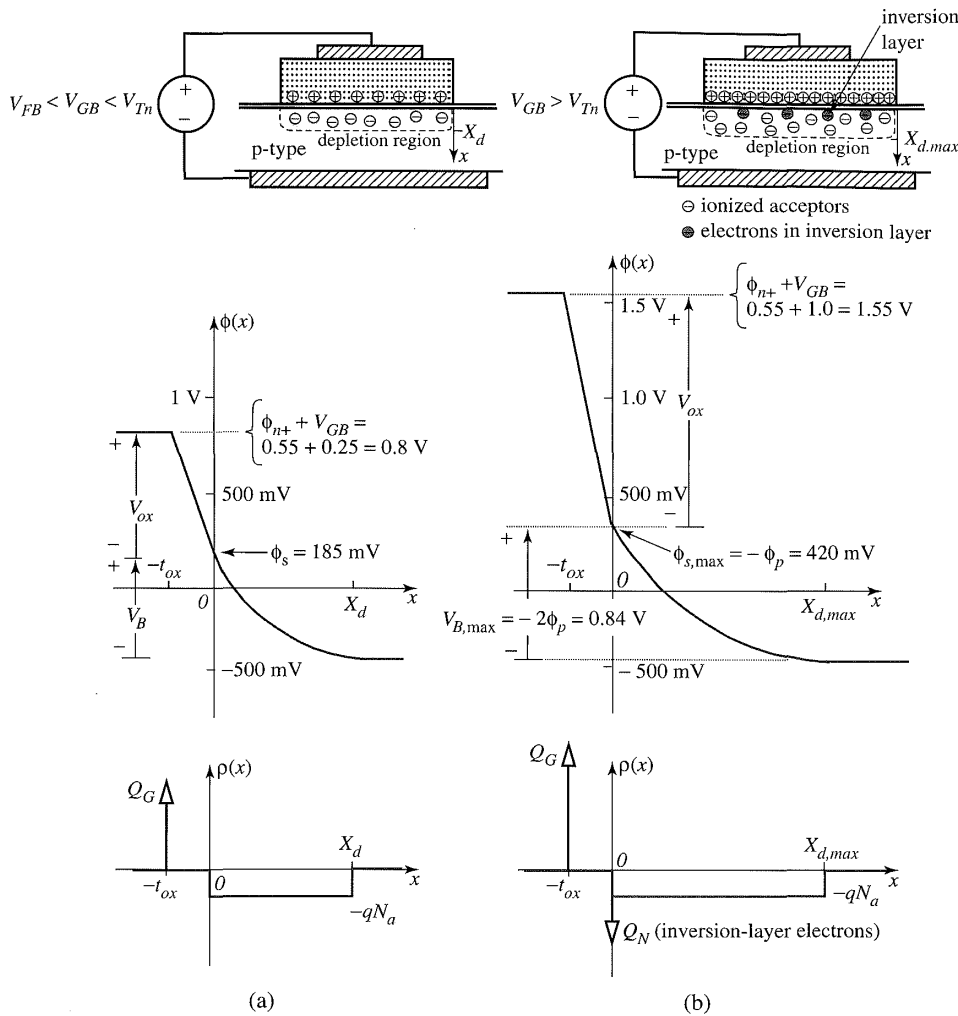
► **Figure 3.23** MOS capacitor with p-type substrate under an applied bias. (a) $V_{GB} = V_{FB}$ (flatband) and (b) $V_{GB} = -1.22$ V $< V_{FB}$ (accumulation.) The potential and charge densities are plotted, for the case where the substrate is doped at $N_a = 10^{17}$ cm $^{-3}$.

the SiO $_2$ insulating film. Therefore, the carrier concentration is linked to the electrostatic potential by the analysis in Section 3.3.1. Note that this argument is not valid for the reverse-biased pn junction since there is a current, albeit small, through the structure when $V_D < 0$ V.

According to Eq. (3.21), the surface electron concentration at $x = 0$ is

$$n_s = n_i \cdot 10^{\phi_s / (60 \text{ mV})} = 10^{10} \cdot 10^{185/60} \text{ cm}^{-3} = 1.2 \times 10^{13} \text{ cm}^{-3} \quad (3.92)$$

This concentration of electrons is negligible compared to the ionized acceptor concentration in the depletion region. As a result, the additional negative charge at the SiO $_2$ -silicon interface from the electrons at $x = 0$ does not appear in the charge density plot in Fig. 3.24(a).



► **Figure 3.24** MOS capacitor with p-type substrate under an applied bias. (a) $V_{FB} < V_{GB} = 250$ mV and $V_{GB} < V_{Tn}$ (depletion) and (b) $V_{GB} = 1.0$ V $> V_{Tn}$ (inversion). The potential and charge densities are plotted, for the case where the substrate is doped at $N_a = 10^{17}$ cm $^{-3}$.

If the gate-bulk voltage V_{GB} is increased further, the surface potential will continue to rise and eventually, there will be a significant electron concentration at the surface. For a first-order analysis of the MOS capacitor, we consider that the surface has **inverted** when the surface potential becomes equal and opposite to the potential of the substrate:

$$\phi_s = -\phi_p \quad (3.93)$$

Note that the surface electron concentration at the onset of inversion is

$$n_s = n_i e^{\phi_s / V_{th}} = n_i e^{-\phi_p / V_{th}} = N_a, \quad (3.94)$$

where the last equality follows from the definition of the potential of p-type silicon in Eq. (3.22). In other words, the surface electron concentration is equal to the hole concentration in the undepleted p-type substrate, when the surface has just inverted.

The applied voltage at which the surface inverts is called the **threshold voltage**, which is given the symbol V_{Tn} for a MOS capacitor on a p-type substrate. Note that the **n** refers to the n-type surface after inversion—not to the p-type substrate. The threshold voltage is the sum of three terms

threshold voltage for
p-type substrate

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\epsilon_s N_a (-2\phi_p)} \quad (3.95)$$

The derivation of Eq. (3.95) will be left to Section 3.8. A typical range for the threshold voltage of a MOS capacitor on an n-type substrate is $V_{Tn} = 0.5 - 1$ V.

The electron concentration at the surface increases exponentially with increasing ϕ_s as indicated by Eq. (3.94). After inversion occurs, further increases in V_{GB} only slightly increase the surface potential. Note that the maximum possible surface potential is $\phi_{s(max)} = 550$ mV, which is only 130 mV higher than the value of $-\phi_p = -(-420$ mV), for the case where $N_a = 10^{17} \text{ cm}^{-3}$. In order to simplify the electrostatics of the MOS capacitor, we will assume that the surface potential stops increasing after the onset of inversion for $V_{GB} > V_{Tn}$ and remains “pinned” at $-\phi_p$, which we will consider its maximum.

Figure 3.24(b) shows the electrostatics for a MOS capacitor biased with $V_{GB} > V_{Tn}$. The surface potential is $\phi_s = -\phi_p$, which means that the bulk voltage V_B (the drop across the depletion region) has reached its maximum value

$$V_B = V_{B,max} = \phi_{s,max} - \phi_p = -\phi_p - \phi_p = -2\phi_p \quad (3.96)$$

Much of the electrostatics in inversion is easily quantified, since the bulk voltage is a known quantity for $V_{GB} \geq V_{Tn}$. For example, the depletion width and bulk charge are constant at their maximum values $X_{d,max}$ and $Q_{B,max}$ in inversion. The oxide voltage is

$$V_{ox} = (V_{GB} + \phi_{n+}) - \phi_s = V_{GB} + \phi_{n+} + \phi_p \text{ for } V_{GB} \geq V_{Tn} \quad (3.97)$$

We now consider the important question of how the gate charge varies with applied bias in inversion. The gate charge balances the bulk charge $Q_{B,max}$ in the depletion region and the electron charge Q_N in the surface inversion layer

$$Q_G(V_{GB}) = -(Q_N + Q_{B,max}) \text{ for } V_{GB} \geq V_{Tn} \quad (3.98)$$

For $V_{GB} = V_{Tn}$, we consider that the electron charge $Q_N \approx 0$ since the MOS capacitor is at the onset of inversion, which implies that

$$Q_G(V_{Tn}) \approx -Q_{B,max} \quad (3.99)$$

Taking equalities in these approximations, we find that the additional gate charge from increasing the bias voltage above threshold is

$$Q_G(V_{GB}) - Q_G(V_{Tn}) = -Q_N \quad (3.100)$$

In other words, the additional gate charge is balanced by the inversion-layer electron charge. The added gate charge and the inversion-layer electrons are separated by the gate oxide, from which we conclude that the parallel-plate capacitance applies

$$Q_G(V_{GB}) - Q_G(V_{Tn}) = C_{ox}(V_{GB} - V_{Tn}) \quad \text{for } V_{GB} \geq V_{Tn} \quad (3.101)$$

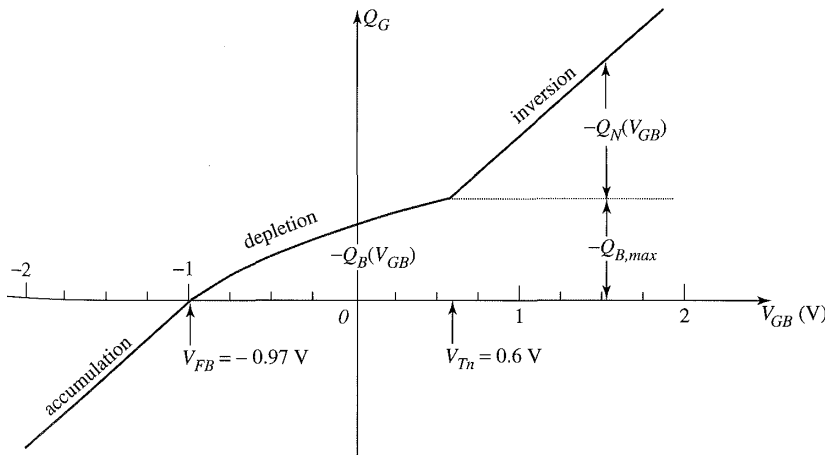
From Eqs. (3.99) and (3.101), the gate charge in inversion is

$$Q_G(V_{GB}) = C_{ox}(V_{GB} - V_{Tn}) - Q_{B,max} \quad (3.102)$$

gate charge in inversion
for p-type substrate

A qualitative picture of the functional dependence of the gate charge on the applied bias for a MOS capacitor with p-type substrate is given in Fig. 3.25, for the case of a substrate doping of $N_a = 10^{17} \text{ cm}^{-3}$ and a 150 Å-thick oxide. From Eq. (3.88), the flatband voltage is $V_{FB} = -0.97 \text{ V}$ and from Eq. (3.95), the threshold voltage is $V_{Tn} = 0.6 \text{ V}$. The gate charge varies linearly in accumulation and in inversion, since the additional charge in the substrate due to a change in the gate-bulk voltage is stored at the SiO_2 silicon surface. The slope in these regions is the oxide capacitance per unit area, C_{ox} . In depletion, the substrate charge is smeared over the depletion region. Therefore, Q_G has a non-linear dependence on V_{GB} which has been sketched qualitatively in Fig. 3.25.

In order to quantify the charge storage in the MOS capacitor, we must solve for the charge, field, and potential in the three regions of operation. Prior to tackling the



► **Figure 3.25** Gate charge as a function of gate-bulk voltage for an MOS capacitor with a 150 Å-thick gate oxide and a substrate doping $N_a = 10^{17} \text{ cm}^{-3}$.

rather involved algebra, it is helpful to summarize the qualitative behavior of the MOS capacitor on an n-type substrate.

3.7.3 MOS Capacitor on an n-type Substrate

Figure 3.26 shows a MOS capacitor with an n^+ polysilicon gate which is fabricated with an n-type substrate. We will use a typical substrate doping of $N_d = 10^{17} \text{ cm}^{-3}$, as we did in the previous section. Our qualitative understanding of the MOS capacitor on a p-type substrate is a good foundation for understanding this “complementary” structure.

In thermal equilibrium, the potential drop from the n^+ polysilicon gate to the n-type substrate for a typical doping concentration $N_d = 10^{17} \text{ cm}^{-3}$ is:

$$\phi_{n+} - \phi_n = 550 \text{ mV} - 420 \text{ mV} = 130 \text{ mV} \quad (3.103)$$

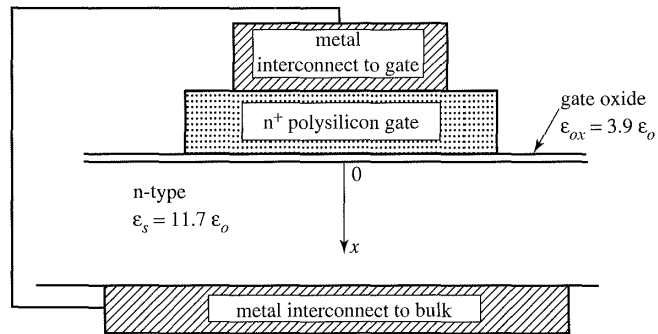
Therefore, the electric field in the oxide is positive (in the same direction as x) in Fig. 3.26 and we conclude that the charge on the gate is positive and that the charge in the n-type substrate is negative. The negative charge consists of accumulated electrons at the SiO_2 silicon interface under the gate. We can visualize the positive charge on the gate attracting the electrons and causing them to accumulate under the gate. In contrast to the situation with a p-type substrate, the MOS capacitor on an n-type substrate is in accumulation when in thermal equilibrium.

Following our procedure from the previous section, we can null the internal voltage drop by applying the flatband voltage $V_{GB} = V_{FB}$

flatband voltage for
n-type substrate

$$V_{FB} = -(\phi_{n+} - \phi_n) = -130 \text{ mV} \quad (3.104)$$

For applied voltages more positive than the flatband voltage, the electric field is positive and the MOS capacitor is in accumulation. As we have seen, thermal equilibrium with $V_{GB} = 0 \text{ V} > V_{FB}$ falls into this region. The gate charge in the accumulation region is



► **Figure 3.26** MOS capacitor with n-type substrate. $V_{GB} = 0$ for investigating the capacitor in thermal equilibrium.

$$Q_G = C_{ox}(V_{GB} - V_{FB}) \text{ for } V_{GB} \geq V_{FB} \quad (3.105)$$

gate charge in
accumulation for n-type
substrate

For applied voltages more negative than the flatband voltage, the electric field reverses and a positive charge is needed in the silicon substrate. Since the substrate is n-type, a depletion region forms under the gate that consists of positively ionized donors. The gate charge for depletion is negative for this case

$$Q_G(V_{GB}) = -Q_B = -qN_d X_d(V_{GB}) \quad (3.106)$$

As the gate-bulk voltage becomes more negative, the surface potential is pulled down and the surface hole concentration p_s increases. The gate-bulk voltage when the surface potential is equal and opposite to that of the n-type substrate ($\phi_s = -\phi_n$) is defined as the threshold voltage, which is given by

$$V_{Tp} = V_{FB} - 2\phi_n - \frac{1}{C_{ox}} \sqrt{2q\epsilon_s N_d (2\phi_n)} \quad (3.107)$$

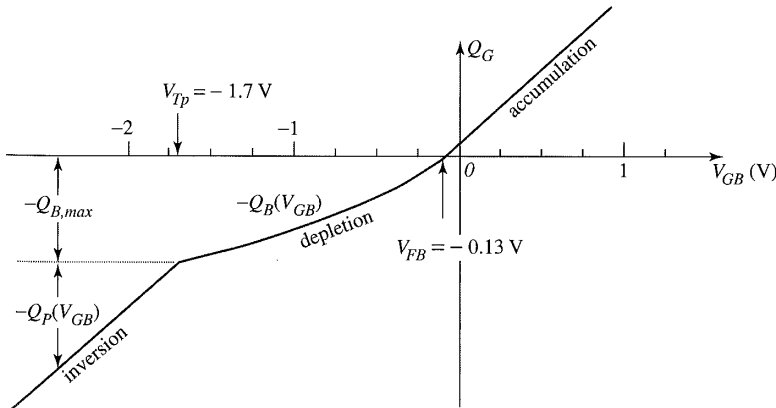
threshold voltage for
n-type substrate

The signs of the potential drops across the depletion region and across the oxide are negative for the case of an n-type substrate. For voltages more negative than the threshold voltage, the MOS capacitor is inverted and the gate charge balances holes in the surface inversion layer and the maximum depletion charge:

$$Q_G = -Q_p - Q_{B, \max} = C_{ox}(V_{GB} - V_{Tp}) - Q_{B, \max} \text{ for } V_{GB} \leq V_{Tp} \quad (3.108)$$

gate charge in inversion
for n-type substrate

The gate charge as a function of the applied bias voltage is sketched in Fig. 3.27.



► **Figure 3.27** Gate charge as a function of gate-bulk voltage for an MOS capacitor on an n-type substrate with doping $N_d = 10^{17} \text{ cm}^{-3}$ and a 150 Å-thick gate oxide.

EXAMPLE 3.7 MOS Electrostatics in Accumulation and in Inversion

In this example, we consider a MOS capacitor with $t_{ox} = 200 \text{ \AA}$ on a p-type substrate with acceptor concentration $N_a = 5 \times 10^{16} \text{ cm}^{-3}$.

(a) Find the electric field in the oxide and the charge per unit area in the silicon substrate (units C/cm^2) for $V_{GB} = -2.5 \text{ V}$.

SOLUTION

The first step is to determine whether the capacitor is in the accumulation, depletion, or inversion regions. The flatband voltage for an MOS capacitor on a p-type substrate with these parameters is given by Eq. (3.88)

$$V_{FB} = -(\phi_{n+} - \phi_p) = -(550 - (-402)) = -0.95 \text{ V}$$

and the threshold voltage is found from Eq. (3.95)

$$V_{Tn} = -0.95 \text{ V} - 2(-0.40) + \frac{\sqrt{2(1.6 \times 10^{-19})(1.04 \times 10^{-12})(5 \times 10^{16})(-2)(-0.40)}}{(3.45 \times 10^{-13}) / (2 \times 10^{-6})}$$

$$V_{Tn} = -0.95 \text{ V} - 2(-0.40) + 0.67 = 0.52 \text{ V}$$

In evaluating the final term, we have substituted the permittivities of silicon and SiO_2

$$\epsilon_s = 1.04 \times 10^{-12} \text{ F/cm} \text{ and } \epsilon_{ox} = 3.45 \times 10^{-13} \text{ F/cm}.$$

The applied bias is $V_{GB} = -2.5 \text{ V} < V_{FB} = -0.95 \text{ V}$ and we conclude that the p-type substrate is accumulated and the electrostatics of Fig. 3.23(b) apply. We can find the electric field from the information on the potential plot in accumulation:

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n+}) - \phi_p}{t_{ox}} = \frac{-2.5 + 0.55 - (-0.40)}{2 \times 10^{-6}} = -7.8 \times 10^5 \text{ V/cm}$$

The charge in the substrate consists of accumulated holes. It is opposite in sign to the gate charge, which is given by Eq. (3.90)

$$Q_p = -Q_G = -C_{ox}(V_{GB} - V_{FB}) = -1.72 \times 10^{-7}(-2.5 - (-0.95)) = 2.67 \times 10^{-7} \text{ C/cm}^2$$

(b) Find the numerical value of the depletion width and depletion charge when the capacitor is biased in the inversion region.

SOLUTION

In inversion, the potential drop across the depletion region is

$$V_{B,\max} = \phi_s - \phi_p = -\phi_p - \phi_p = -2\phi_p = -2(-0.40) = 0.8 \text{ V}.$$

Adapting the results of Ex. 3.3, the relationship between the depletion region width $X_{d,\max}$ and the potential drop $V_{B,\max}$ is

$$V_{B,\max} = \frac{1}{2} \left(\frac{qN_a}{\epsilon_s} \right) X_{d,\max}^2$$

Solving for the depletion region width, we find that

$$X_{d,\max} = \sqrt{\frac{2\epsilon_s V_{B,\max}}{qN_a}} = \sqrt{\frac{2(1.035 \times 10^{-12})(0.8)}{(1.6 \times 10^{-19})(5 \times 10^{16})}} = 1440 \text{ Å}.$$

The bulk charge in the depletion region is

$$Q_{B,\max} = -qN_a X_{d,\max} = -(1.6 \times 10^{-19})(5 \times 10^{16})(1.44 \times 10^{-5}) = -1.15 \times 10^{-7} \text{ C/cm}^2.$$

- (c) Find the electric field in the oxide and the inversion-layer electron charge, for $V_{GB} = 2.5 \text{ V}$.

SOLUTION

We know that the MOS capacitor is inverted, since $V_{GB} = 2.5 \text{ V} > V_{Tn} = 0.52 \text{ V}$. The electrostatics in Fig. 3.24(b) apply for this region. From the potential plot, we can evaluate the electric field in the oxide:

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n+}) - (-\phi_p)}{t_{ox}} = \frac{2.5 + 0.55 - 0.40}{2 \times 10^{-6}} = 1.32 \times 10^6 \text{ V/cm}.$$

Electrons in the inversion layer are one component of the total charge in the silicon substrate. Using Gauss's Law, we can relate the electric field in the oxide to the substrate charge:

$$E_{ox} = \frac{-(Q_{B,\max} + Q_N)}{\epsilon_{ox}}$$

Solving for the inversion-layer charge, we find that

$$Q_N = -\epsilon_{ox} E_{ox} - Q_{B,\max} = -4.55 \times 10^{-7} - (-1.15 \times 10^{-7}) = -3.4 \times 10^{-7} \text{ C/cm}^2$$

We could have found the electron charge directly from Eq. (3.101)

$$Q_N = -C_{ox}(V_{GB} - V_{Tn}) = -\left(\frac{3.45 \times 10^{-13}}{2 \times 10^{-6}}\right)(2.5 - 0.52) = -3.4 \times 10^{-7} \text{ C/cm}^2$$

- (d) Electric fields with magnitudes greater than $E_{ox,\max} = 5 \times 10^6 \text{ V/cm}$ will cause irreversible damage to the gate oxide. Find the permissible range of gate-bulk voltages.

SOLUTION

In accumulation, the electric field in the oxide is

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n+}) - \phi_p}{t_{ox}}$$

Solving for the most negative gate-bulk voltage using $E_{ox} = -5 \times 10^6$ V/cm, we find that

$$V_{GB,min} = E_{ox} t_{ox} - \phi_{n+} + \phi_p = (-5 \times 10^6) (2 \times 10^{-6}) - 0.55 + (-0.4) = -10.95 \text{ V}$$

In inversion, the electric field in the oxide is

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n+}) - (-\phi_p)}{t_{ox}}$$

Substituting the maximum positive field $E_{ox} = 5 \times 10^6$ V/cm, we find that

$$V_{GB,max} = E_{ox} t_{ox} - \phi_{n+} - \phi_p = (5 \times 10^6) (2 \times 10^{-6}) - 0.55 - 0.4 = 9.05 \text{ V}$$

In this example, we have found numerical values for several properties of the MOS capacitor when biased in accumulation and in inversion. A clear understanding of the MOS structure and its regions of operation, combined with one-dimensional electrostatics, can prove adequate for solving practical problems—without the need for complicated analysis.

► 3.8

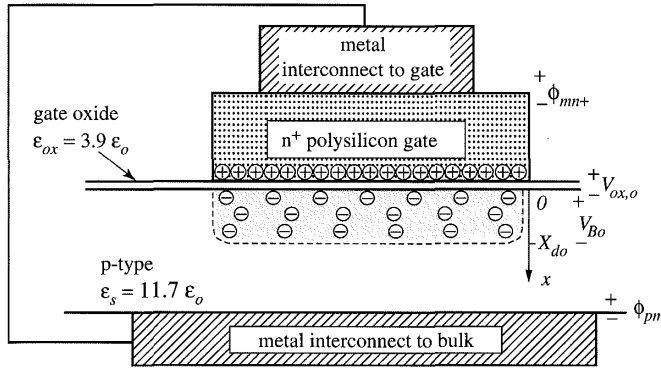
THE ELECTROSTATICS OF THE MOS CAPACITOR

In the previous section, the basic features of the MOS capacitor were outlined without deriving the results from a thorough analysis of the electrostatics. In this section, the MOS capacitor is considered more systematically, beginning with the MOS capacitor on a p-type substrate in thermal equilibrium. We will rely on the previous section to provide the context for the electrostatics.

3.8.1 MOS Electrostatics in Thermal Equilibrium

Figure 3.28 shows the MOS capacitor with $V_{GB} = 0$ V and indicates the locations and symbols for the internal potential drops. In particular, the contact potentials ϕ_{mn+} between the metal and n⁺ polysilicon gate, and ϕ_{pm} between the p-type bulk and its metal contact are included in this section. These battery-like potential drops were described in Section 3.4.3 in the analysis of the pn junction under reverse bias. We define the potential drop across the oxide is defined as $V_{ox,o}$ and the drop across the depletion region as $V_{Bo,o}$, where the subscript *o* indicates thermal equilibrium.

The charge density $\rho_o(x)$ through the MOS capacitor on a p-type substrate is sketched in Fig. 3.29(a), for the case of thermal equilibrium. We would like to quantify the width of the depletion region X_{do} as a function of the material properties and oxide thickness. The bulk charge Q_{Bo} in the depletion region must be equal in magnitude and opposite in sign to the gate charge



► **Figure 3.28** MOS capacitor with p-type substrate, with the charge distribution taken from Fig. 3.21. Gate and bulk metal contacts shorted together for the thermal equilibrium analysis.

$$Q_{Bo} = -qN_a X_{do} = -Q_{Go} \quad (3.109)$$

where N_a is the doping concentration in the bulk. As in Section 3.7, numerical values will be calculated for a substrate acceptor concentration of $N_a = 10^{17} \text{ cm}^{-3}$ and an oxide thickness $t_{ox} = 150 \text{ \AA}$. The charge density in Fig. 3.29(a) is the same as in Ex. 3.3. Following the same steps as in that analysis, we graphically integrate $\rho_o(x)$ and find that the electric field in the gate oxide is constant and that $E_o(x)$ varies linearly in the depletion region as shown in Fig. 3.29(b). The boundary condition on electric field

$$\epsilon_{ox} E_o(x = 0^-) = \epsilon_s E_o(x = 0^+) \quad (3.110)$$

is used to connect the electric field solutions across the oxide/silicon interface. The electric field drops a factor of three across $x = 0$ since the permittivity of silicon is a factor of three larger than that of oxide.

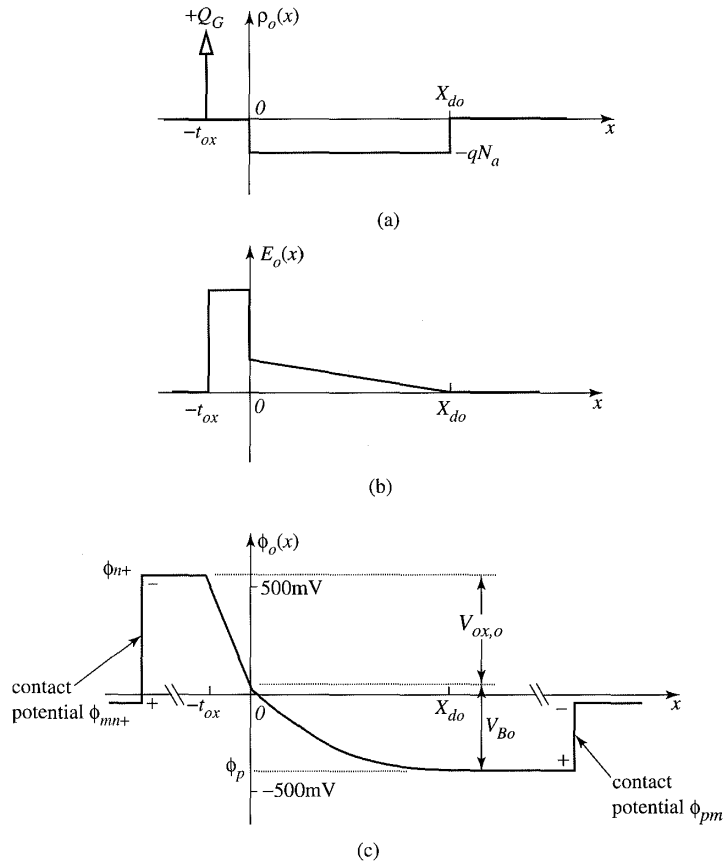
The first step in plotting the potential is to apply Kirchhoff's voltage law to the MOS capacitor in thermal equilibrium. From Fig. 3.28,

$$-\phi_{mn+} - V_{ox,o} - V_{Bo} - \phi_{pm} = 0 \quad (3.111)$$

Solving for the internal drop from the n^+ polysilicon gate to the p-type bulk, we find that

$$V_{ox,o} + V_{Bo} = -(\phi_{mn+} + \phi_{pm}) \quad (3.112)$$

For the MOS capacitor, the internal potential drop is known to be the difference in the thermal equilibrium potentials of the n^+ gate and the p-type bulk:



► **Figure 3.29** MOS capacitor in thermal equilibrium: (a) charge density $\rho_o(x)$, (b) electric field $E_o(x)$, and (c) electrostatic potential $\phi_o(x)$. The potential jumps at the metal contacts to the n^+ polysilicon gate and to the p-type bulk are both negative quantities in (c).

$$V_{ox,o} + V_{Bo} = \phi_{n+} - \phi_p \quad (3.113)$$

By equating Eqs. (3.113) and (3.112), the sum of the contact potentials is equal to the difference in the potentials of the gate and the bulk

$$\phi_{n+} - \phi_p = -(\phi_{mn+} + \phi_{pm}) \quad (3.114)$$

which is similar to Eq. (3.58) for the pn junction in thermal equilibrium.

In order to plot the potential $\phi_o(x)$ in thermal equilibrium, we graphically integrate the negative of the electric field across the depletion region and the oxide. The potential varies linearly in the oxide since E_o is constant there, and quadratically in

the depletion region. As a sign check, we verify that the potential of the gate comes out higher than that of the underlying bulk silicon. The contact potentials ϕ_{mn+} between the metal and n^+ polysilicon gate, and ϕ_{pm} between the p-type bulk and its metal contact are shown schematically in Fig. 3.29(c) as abrupt jumps. For the case of thermal equilibrium, note that the gate and bulk metal contacts are at the same potential in Fig. 3.29(c).

In order to quantify the potential variation $\phi_o(x)$ and the width of the depletion region X_{do} , it is necessary to wade through considerable algebra. This is an unfortunate feature of MOS device physics, as will be seen in this chapter and Chapter 4. Nevertheless, it is worthwhile to work out the detailed solutions for $E_o(x)$ and $\phi_o(x)$.

To start, Gauss's Law in integral form connects the electric field just inside the silicon to the depletion charge Q_{Bo} [C/cm^2]

$$E_o(0^+) = \frac{-Q_{Bo}}{\epsilon_s} = \frac{qN_a X_{do}}{\epsilon_s} \quad (3.115)$$

Since there is no charge layer at the oxide/silicon interface, the boundary condition in Eq. (3.11) connects the silicon field to the oxide field on the other side of the interface

$$E_o(0^-) = \frac{\epsilon_s}{\epsilon_{ox}} \left(\frac{qN_a X_{do}}{\epsilon_s} \right) = \frac{qN_a X_{do}}{\epsilon_{ox}} = E_{ox} \quad (3.116)$$

From the definition of potential, it follows that the potential in the oxide where $-t_{ox} \leq x \leq 0$ is given by

$$\phi_o(x) - \phi_{n+} = \int_{-t_{ox}}^x -E_{ox} dx = -E_{ox}(x + t_{ox}) = -\frac{qN_a X_{do}}{\epsilon_{ox}}(x + t_{ox}) \quad (3.117)$$

It is not difficult to make a sign error, but we can check our algebra since we know the potential decreases through the oxide. The potential at the oxide/silicon interface can be found by evaluating Eq. (3.117) at the origin

$$\phi_o(0) = \phi_{n+} - \frac{qN_a X_{do} t_{ox}}{\epsilon_{ox}} \quad (3.118)$$

This result can be expressed in terms of $V_{ox,o}$ which is the drop across the oxide

$$V_{ox,o} = \phi_{n+} - \phi_o(0) = \frac{qN_a X_{do}}{C_{ox}} = \frac{Q_{Go}}{C_{ox}} \quad (3.119)$$

where we have substituted the oxide capacitance $C_{ox} = \epsilon_{ox}/t_{ox}$ [F/cm^2]. In Eq. (3.119), we have also substituted the equality between the charge (per unit area) on the gate Q_{Go} and the negative of the charge (per unit area) in the silicon $-Q_{Bo} = qN_a X_{do}$.

We now turn our attention to the depletion region in the silicon substrate. From the integral form of Gauss's Law, the electric field $E_o(x)$ in the charged region ($0 \leq x \leq X_{do}$) is given by

$$\epsilon_s E_o(x) - \epsilon_s E_o(0^+) = \int_{0^+}^x -q N_a dx = -q N_a x \quad (3.120)$$

Solving for $E_o(x)$ and substituting Eq. (3.115) for $E_o(0^+)$, the electric field at the interface, we find the linear equation sketched in Fig. 3.29(b)

$$E_o(x) = \frac{q N_a (X_{do} - x)}{\epsilon_s} \quad (3.121)$$

We then integrate the electric field to find $\phi_o(x)$ in the charged region $0 \leq x \leq X_{do}$

$$\phi_o(x) - \phi_o(0) = \int_{0^+}^x -E_o(x) dx = \left(-\frac{q N_a}{\epsilon_s} \right) \left(X_{do} x - \frac{x^2}{2} \right) \quad (3.122)$$

Substituting $\phi_o(0)$ from Eq. (3.118), the potential in the charged region is given by

$$\phi_o(x) = \left(\phi_{n+} - \frac{q N_a X_{do}}{C_{ox}} \right) - \frac{q N_a}{\epsilon_s} \left(X_{do} x - \frac{x^2}{2} \right) \quad (3.123)$$

Since the potential at the bottom of the charged region is $\phi_o(X_{do}) = \phi_p$, we can solve for the thermal equilibrium built-in potential across the polysilicon-oxide-silicon sandwich

$$\phi_{n+} - \phi_p = \frac{q N_a X_{do}}{C_{ox}} + \frac{q N_a X_{do}^2}{2 \epsilon_s} \quad (3.124)$$

The first term in on the right-hand side of Eq. (3.124) is $V_{ox,o}$, the equilibrium drop across the oxide (see Eq. (3.119)), therefore the second term is the potential drop across the charged region V_{Bo} , as can also be shown from Eq. (3.122). This result is represented graphically in Fig. 3.29(c).

The width of the depletion region can be found by solving for X_{do}

$$X_{do} = t_{ox} \left(\frac{\epsilon_s}{\epsilon_{ox}} \right) \left(\sqrt{1 + \frac{2 C_{ox}^2 (\phi_{n+} - \phi_p)}{q \epsilon_s N_a}} - 1 \right) \quad (3.125)$$

Evaluating Eq. (3.123) at $x = 0$, we find that the thermal equilibrium surface potential is

$$\phi_{so} = \phi_o(x=0) = \phi_{n+} - \frac{q N_a X_{do}}{C_{ox}} \quad (3.126)$$

where X_{do} is given in Eq. (3.125).

EXAMPLE 3.8 MOS Capacitor in Thermal Equilibrium

It is always helpful to substitute typical dimensions and material properties into complicated expressions such as Eqs. (3.125) and (3.126) in order to develop a feel for the magnitudes of the quantities. For a typical gate oxide thickness of $t_{ox} = 15 \text{ nm}$ and a typical bulk doping of $N_a = 10^{17} \text{ cm}^{-3}$, we find that the depletion layer is

$$X_{do} = 76 \text{ nm}$$

and that the surface potential at the oxide/silicon interface is

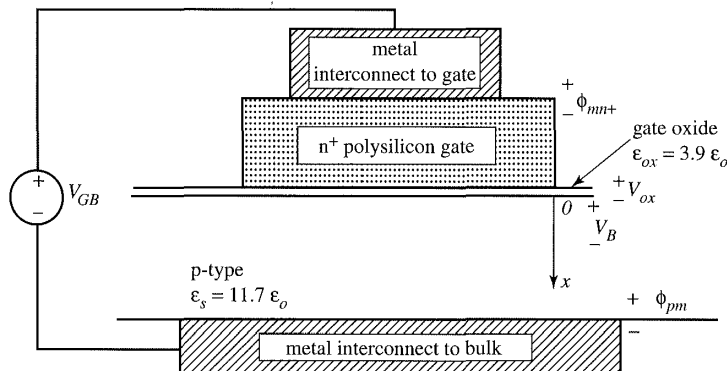
$$\phi_{so} = \phi(x=0) = 550 \text{ mV} - 529 \text{ mV} = 21 \text{ mV}$$

For this particular case, the potential drop across the oxide $V_{ox,o} = 529 \text{ mV}$ is slightly larger than the drop across the depletion region $V_{Bo} = 21 - (-420) = 441 \text{ mV}$, with the depletion region width equal to about five times the oxide thickness.

3.8.2 MOS Electrostatics under Applied Bias

From the numerical results in Ex. 3.8, we note that the surface potential for this example corresponds to silicon that is nearly intrinsic. In other words, the “built-in” voltage drop across the MOS capacitor, $\phi_{n+} - \phi_p$, has set up electric fields that have affected the electrical properties of the silicon underlying the gate oxide. This phenomenon, termed the **field effect**, is controllable through an applied voltage on the gate. We will see in the next chapter that it forms the basic principle of MOS transistors.

Having done a thorough analysis of the electrostatics of the MOS capacitor in thermal equilibrium, we now turn to the case where an external bias V_{GB} is applied between the metal interconnections to the polysilicon gate and p-type bulk silicon. Figure 3.30 shows the MOS capacitor with a voltage source V_{GB} connected from the



► **Figure 3.30** MOS capacitor on a p-type substrate for one-dimensional analysis of charge distribution $\rho(x)$, electric field $E(x)$, and potential $\phi(x)$ for the case of an applied bias V_{GB} .

gate to the bulk. We would like to investigate the effect of V_{GB} on the potential $\phi(x)$ through the structure. For convenience, the metal interconnection to the bulk will be kept fixed in plotting the change in potential under applied bias. As we have seen in Section 3.6, the electrostatics of the MOS capacitor are very different depending on the sign and magnitude of the applied voltage. We now quantify the charge, electric field, and potential for the MOS capacitor for the different regions of applied bias.

FLATBAND

A good starting point is to apply a gate voltage that is *opposite* to the built-in internal potential drop $\phi_{n+} - \phi_p$, which we define as the flatband voltage V_{FB} . For example, the built-in drop is 970 mV for the case where the substrate doping is $N_a = 10^{17} \text{ cm}^{-3}$. Applying $V_{GB} = V_{FB} = -970 \text{ mV}$ shifts the gate interconnect lower by 970 mV with respect to the bulk interconnect. The contact potential ϕ_{mn+} is unchanged by the applied bias, so the polysilicon gate potential is lowered to

$$\phi_{n+} - V_{FB} = 550 \text{ mV} - 970 \text{ mV} = -420 \text{ mV} \quad (3.127)$$

The bulk metal contact is considered fixed under applied bias and its contact potential ϕ_{pm} is also unchanged, so the p-type bulk remains at $\phi_p = -420 \text{ mV}$. Therefore, there is no potential drop between the n^+ polysilicon and p-type bulk in flatband. The potential is therefore constant at $\phi(x) = -420 \text{ mV}$ throughout the MOS structure when biased at flatband. There is no electric field or charge density in the MOS capacitor for this case either, as shown in Fig. 3.31.

ACCUMULATION

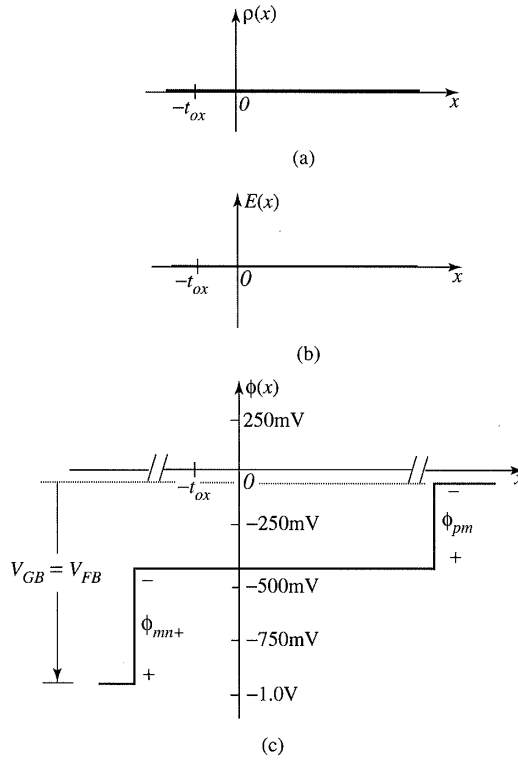
The electrostatics of the MOS capacitor are very different for voltages $V_{GB} < V_{FB}$ compared with $V_{GB} > V_{FB}$. In the former case, the potential of the n^+ polysilicon gate is pulled less than that of the p-type bulk, leading to a negative charge on the gate and a positive charge in the silicon underneath the gate oxide. As we have seen in Section 3.7, the p-type substrate has a high concentration of mobile holes that accumulate at the SiO_2 -silicon interface due to attraction by the negative gate charge. An excess of holes over the acceptor concentration results in a net positive charge at the silicon surface. The surface potential is pulled lower, due to the surface hole concentration p_s exceeding the bulk doping concentration:

$$\phi_s = -V_{th} \ln(p_s/n_i) < -V_{th} \ln(N_a/n_i) \quad (3.128)$$

However, the logarithmic function is weak and it is a reasonable approximation that $\phi_s \approx \phi_p$ in accumulation. In Section 3.7, we were able to quantify the electrostatics in accumulation since the parallel-plate analysis in Ex. 3.1 could be adapted to this case.

DEPLETION

We have already worked through an example of the MOS capacitor with $V_{GB} > V_{FB}$ in the case of thermal equilibrium since $V_{GB} = 0 \text{ V}$ and $V_{FB} = -0.97 \text{ V}$. As shown in Fig. 3.29(a), the positive sheet charge on the gate in thermal equilibrium is mirrored in a negatively charged depletion region in the silicon substrate. In this section, we will establish the range of voltages V_{GB} for which the MOS capacitor is in the depletion region. Since the form of the charge density for a depleted MOS capacitor is identical to that in thermal equilibrium, the results of the equilibrium electrostatic analysis can be adapted and applied here.



► **Figure 3.31** MOS capacitor on a p-type substrate biased in flatband with $V_{GB} = V_{FB} = -0.97$ V. (a) Charge density, (b) electric field, and (c) potential. The arrow on the potential plot graphically indicates that the flatband voltage pulls the gate metallization lower relative to the bulk metallization.

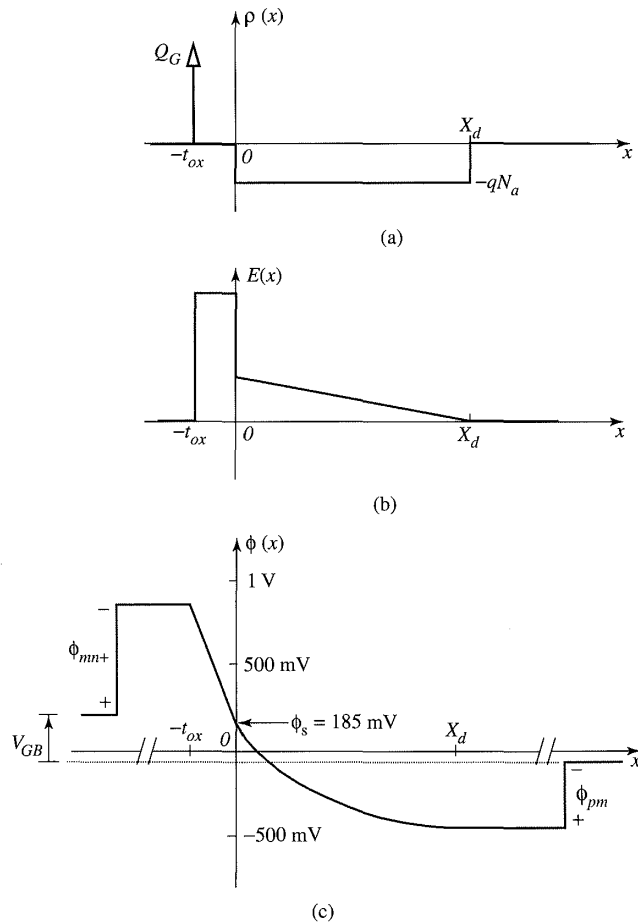
Figure 3.32 shows the electrostatics of a MOS capacitor with $V_{GB} = 250$ mV and $V_{FB} = -970$ mV. Later in this section, we will justify that the capacitor is depleted for this particular gate-bulk bias. The only difference from equilibrium is that the internal voltage drop across the oxide and depletion region is now

$$V_{GB} - V_{FB} = V_{ox} + V_b = 250 - (-970) = 1220 \text{ mV} = 1.22 \text{ V} \quad (3.129)$$

rather than $-V_{FB} = \phi_{n+} - \phi_p = 0.97$ V. Making the substitution $V_{GB} - V_{FB}$ for $-V_{FB}$ in the equilibrium depletion width in Eq. (3.125) and $V_{GB} + \phi_{n+}$ for ϕ_{n+} in the equilibrium surface potential in (3.126), we find that

$$X_d(V_{GB}) = t_{ox} \left(\frac{\epsilon_s}{\epsilon_{ox}} \right) \left(\sqrt{1 + \frac{2C_{ox}^2 (V_{GB} - V_{FB})}{q\epsilon_s N_a}} - 1 \right) \quad (3.130)$$

$$\phi_s(V_{GB}) = (V_{GB} + \phi_{n+}) - \frac{qN_a X_d(V_{GB})}{C_{ox}} \quad (3.131)$$



► **Figure 3.32** MOS capacitor on a p-type substrate biased in depletion with an applied bias $V_{GB} = 250 \text{ mV}$ for $V_{FB} = -970 \text{ mV}$: (a) charge density, (b) electric field, and (c) potential.

For $V_{GB} = 250 \text{ mV}$, the depletion region width increases to $X_d = 88.5 \text{ nm}$ and the surface potential is $\phi_s = (250 \text{ mV} + 550 \text{ mV}) - 615 \text{ mV} = 185 \text{ mV}$.

We discussed the implications of the surface becoming n-type in Section 3.7. Here, we will quantify the onset of inversion and derive the expression for the threshold voltage.

THE THRESHOLD VOLTAGE

As we increase the applied bias, the surface potential rises according to Eq. (3.131). At some point the assumptions underlying the depletion charge distribution in Fig.

3.32(a) become invalid. For example, if we substitute $V_{GB} = 1$ V into Eqs. (3.130) and (3.131), we find that the surface potential $\phi_s = 740$ mV, which is greater than the maximum potential possible in silicon ($\phi_{n+} = 550$ mV).

The electron concentration increases exponentially as the surface potential increases, according to Eq. (3.92), to the point where it eventually becomes the dominant component of the negative charge in the silicon substrate. After the surface becomes strongly n-type, the charge density in the silicon substrate must be modified to include the electron contribution

$$\rho(x) = -q(N_a + n(x)) = -q(N_a + n_i e^{\phi(x)/V_{th}}) \text{ for } 0 \leq x \leq X_d \quad (3.132)$$

Substitution of Eq. (3.132) into Poisson's Equation results in a nonlinear differential equation for the potential $\phi(x)$. The solution will be left for an advanced device physics course. As usual, our goal is to find an approximation that allows us to capture the essential results in relatively simple equations.

The exponential increase in the electron concentration with increasing surface potential turns out to be the key to making a reasonable approximation to the charge density. We are able to set a critical surface potential ϕ'_s below which $n(x)$ can be neglected in Eq. (3.132) and the MOS capacitor considered depleted. The **onset of inversion** is defined to be when the surface potential is equal and opposite to the potential of the bulk p-type substrate.

$$\boxed{\phi'_s = -\phi_p} \quad (3.133)$$

onset of inversion for p-type substrate

In simplifying the charge density in Eq. (3.132), we will neglect the surface electron concentration for surface potentials less than the critical surface potential at the onset of inversion

$$n_s \approx 0 \text{ for } \phi_s \leq \phi'_s = -\phi_p \quad (3.134)$$

Note that the surface electron concentration when $\phi'_s = -\phi_p$ is

$$n_s = n_i e^{\phi'_s/V_{th}} = n_i e^{-\phi_p/V_{th}} = N_a = p(x > X_d) \quad (3.135)$$

In other words, Eq. (3.135) states that at the critical surface potential, the electron concentration is equal to the acceptor concentration, or that the surface is “as much n-type as the bulk is p-type.” Although the electron concentration $n_s = N_a$ at this point, we will nevertheless neglect n_s in solving the electrostatics for $\phi'_s = -\phi_p$ according to the approximation in Eq. (3.134). This approach seems likely to lead to large errors, but the very rapid (exponential) change in n_s with surface potential makes the results reasonably accurate and very useful for understanding the essentials of MOS electrostatics.

The applied gate bias V_{GB} at which the onset of inversion occurs is obviously a very important quantity for the MOS capacitor. We define it as the **threshold voltage** V_{Tn} for capacitors on p-type substrates. In order to find an expression for V_{Tn} , we can

1. Not to be confused with the thermal voltage, $V_{th} = kT/q$.

directly apply our understanding of the electrostatics of the depleted MOS capacitor. According to Eq. (3.134), $n_s \approx 0$ for $\phi_s \leq -\phi_p$ and so the charge density from Fig. 3.32(a) remains valid. We can solve for V_{Tn} by substituting $\phi_s = -\phi_p$ into Eqs. (3.130) and (3.131). However, there is little insight gained. Instead, we will begin from the plot of potential at the onset of inversion in Fig. 3.33.

At the onset of inversion, the potential drop V_B' across the depletion region is a known quantity

$$V_B' = \phi_s' - \phi_p = -\phi_p - \phi_p = -2\phi_p \quad (3.136)$$

The charge density in the depletion region is $\rho(x) = -qN_a$ and can be integrated twice using Poisson's Equation, as we did in Ex. 3.3. At the onset of inversion, the depletion width has increased to its maximum value which we call $X_{d,max}$. Integration of the constant charge density in the depletion region leads to

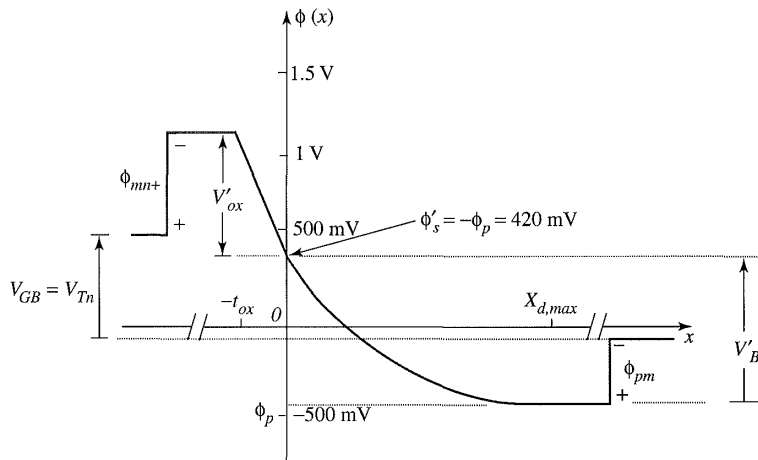
$$V_B' = \left(\frac{qN_a}{2\epsilon_s} \right) X_{d,max}^2 = -2\phi_p \quad (3.137)$$

Solving for $X_{d,max}$ we find it is related to the drop across the depletion region by

$$X_{d,max} = \sqrt{2 \frac{\epsilon_s}{qN_a} (-2\phi_p)} \quad (3.138)$$

The charge in the depletion region at the onset of inversion $Q_B' = Q_{B,max}$ is the product of its charge density and the depletion width

$$Q_{B,max} = -qN_a X_{d,max} = -\sqrt{2q\epsilon_s N_a (-2\phi_p)} \quad (3.139)$$



► **Figure 3.33** Potential for gate biased at the threshold voltage $V_{GB} = V_{Tn}$, the onset of inversion. The surface potential is equal and opposite to the bulk potential.

Gauss's integral law can be applied to find the electric field in the oxide, which when multiplied by the oxide thickness yields V_{ox}' , the potential drop across the oxide in Fig. 3.33

$$V_{ox}' = E_{ox}' t_{ox} = \frac{-Q_{B,max} t_{ox}}{\epsilon_{ox}} = \left(\frac{t_{ox}}{\epsilon_{ox}} \right) \sqrt{2q\epsilon_s N_a (-2\phi_p)} \quad (3.140)$$

The term in parentheses in Eq. (3.140) is the inverse of the oxide capacitance C_{ox} . Since the internal voltage drop in the MOS capacitor is the sum of the drops across the depletion region and across the oxide as shown in Fig. 3.33

$$V_{GB} - V_{FB} = V_{Tn} - V_{FB} = V_B' + V_{ox}' \quad (3.141)$$

Substituting from Eqs. (3.137) and (3.140), we can solve for the threshold voltage on a p-type substrate, which was given previously in Eq. (3.95) in Section 3.7

$$V_{Tn} = V_{FB} + V_B' + V_{ox}' = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\epsilon_s N_a (-2\phi_p)} \quad (3.142)$$

This expression hardly seems like a “neat” final result. However, V_{Tn} is the sum of three simple terms. First, the flatband voltage is the built-in offset across the MOS structure. The second term is the drop across the depletion region at the onset of inversion. The final term is the magnitude of the depletion charge at inversion divided by the oxide capacitance, which turns out to be the potential drop across the gate oxide. For the typical case where $t_{ox} = 15$ nm and $N_a = 10^{17}$ cm⁻³, the threshold voltage from Eq. (3.142) is $V_{Tn} = 600$ mV.

INVERSION

What happens when the applied gate-bulk voltage V_{GB} is increased further? From Eq. (3.135), small changes in the surface potential lead to large increases in the surface electron concentration. As we know from Eq. (3.23), a 60 mV increase in ϕ_s over ϕ_s' corresponds to an order-of-magnitude increase in n_s . Therefore, we conclude that the surface potential only slowly increases as V_{GB} is raised, since the electron charge will increase linearly with V_{GB} . This insight allows us to greatly simplify the electrostatics in inversion, by making the **delta-depletion approximation**

$$\phi_s \approx \phi_s' = -\phi_p \text{ for } V_{GB} \geq V_{Tn} \quad (3.143)$$

delta-depletion
approximation

In other words, we consider the surface potential **pinned** at $-\phi_p$ in inversion. The approximation that ϕ_s is pinned means that we cannot use Eq. (3.21) to find the electron concentration at the surface in the inversion region. However, we will be able to find the inversion-layer electron charge Q_N [C/cm²] by other means.

Now that the boundary between depletion and inversion has been established using the delta-depletion approximation, we can analyze the electrostatics of the inverted MOS capacitor. Our primary goal is to find the relationship between the electron charge in the inversion layer and the applied voltage V_{GB} .

Figure 3.34(a) shows the charge density for the case where $V_{GB} = 1.0$ V when $V_{Tn} = 600$ mV. Electrons at the SiO₂-silicon surface constitute a sheet charge Q_N

$[C/cm^2]$ that is represented by the delta function in Fig. 3.34(a). The depletion region width is $X_{d,max}$ after inversion because the drop across it remains fixed at $-2\phi_p$. The potential drop across the oxide increases since $V_{GB} > V_{Tn}$ and

$$V_{GB} - V_{FB} = V_{ox} - 2\phi_p \quad (3.144)$$

Once again, the integral form of Gauss's Law is useful for connecting V_{ox} to the charge in the silicon that consists of the sum of the electron charge Q_N , and the (maximum) depletion charge $Q'_B = Q_{B,max}$

$$V_{ox} = E_{ox} t_{ox} = \left(\frac{t_{ox}}{\epsilon_{ox}} \right) (-Q_{B,max} - Q_N) \quad (3.145)$$

In Fig. 3.34(b), the electric field drops a factor of three from the oxide to just inside the silicon at $x = 0$

$$E(0) = \frac{-Q_N - Q_{B,max}}{\epsilon_s} = E_{ox} \left(\frac{\epsilon_{ox}}{\epsilon_s} \right) = \frac{E_{ox}}{3} \quad (3.146)$$

In inversion, there is a second discontinuity in the electric field, as shown in Fig. 3.34(b). The electrons in the inversion layer form a charge sheet located at the SiO_2 -silicon interface. Therefore, the electric field just below the inversion layer at $x = 0^+$ does not include the contribution of the inversion charge

$$E(0^+) = -\frac{Q_{B,max}}{\epsilon_s} = E(0) - \frac{(-Q_N)}{\epsilon_s} \quad (3.147)$$

The width of the inversion layer is determined in an advanced course to be on the order of $50 \text{ \AA}$, so the drop in electric field is not quite as abrupt as shown in Fig. 3.34(b).

Our goal is to express the inversion-layer charge Q_N as a function of the applied voltage, so we substitute Eq. (3.145) into Eq. (3.144)

$$V_{GB} - V_{FB} = V_{ox} - 2\phi_p = \frac{(-Q_{B,max} - Q_N)}{C_{ox}} - 2\phi_p \quad (3.148)$$

in which we have also substituted $C_{ox} = \epsilon_{ox}/t_{ox}$. Solving Eq. (3.148) for the inversion-layer charge, we find that

$$Q_N = -C_{ox} \left(V_{GB} - V_{FB} + 2\phi_p - \frac{-Q_{B,max}}{C_{ox}} \right) = -C_{ox} (V_{GB} - V_{Tn}) \text{ for } V_{GB} \geq V_{Tn} \quad (3.149)$$

where we have identified the threshold voltage from Eq. (3.142). Note that there is *no* inversion layer charge unless the gate voltage is greater than the threshold voltage. This result is central to the model of the MOS field-effect transistor that will be developed in Chapter 4.

The results of this section for the MOS capacitor on a p-type substrate can be summarized by writing the gate charge as a function of the applied gate-bulk bias in accumulation, depletion, and inversion.

inversion-layer electron
charge for p-type
substrate

Gate charge for:
accumulation
depletion
inversion

$$Q_G = C_{ox}(V_{GB} - V_{FB}) \quad \text{for } V_{GB} \leq V_{FB} \quad (3.150)$$

$$Q_G = -Q_B(V_{GB}) = \frac{q\epsilon_s N_a}{C_{ox}} \left(\sqrt{1 + \frac{2C_{ox}^2 (V_{GB} - V_{FB})}{q\epsilon_s N_a}} - 1 \right) \quad (V_{FB} \leq V_{GB} \leq V_{Tn}) \quad (3.151)$$

$$Q_G = C_{ox}(V_{GB} - V_{Tn}) + \frac{q\epsilon_s N_a}{C_{ox}} \left(\sqrt{1 + \frac{2C_{ox}^2 (V_{Tn} - V_{FB})}{q\epsilon_s N_a}} - 1 \right) \quad \text{for } V_{GB} \geq V_{Tn} \quad (3.152)$$

The depletion charge in Eq. (3.151) is found from Eq. (3.130) which gives the depletion width as a function of bias $X_d(V_{GB})$. The results in Eqs. (3.150)–(3.152) quantify the sketch of Q_G versus V_{GB} in Fig. 3.25 and will be useful for finding the MOS capacitance in the next section.

We conclude this section with an example that adapts the quantitative analysis of the MOS capacitor to the case of an n-type substrate.

EXAMPLE 3.9 MOS Electrostatics with an N-type Substrate

Given a MOS capacitor on an n-type substrate with an n^+ poly gate ($\phi_{n^+} = 550\text{mV}$), a donor concentration $N_d = 10^{16}\text{cm}^{-3}$, and an oxide thickness $t_{ox} = 500\text{Å}$. The contact potentials have values $\phi_{mn^+} = -400\text{mV}$ and $\phi_{nm} = 210\text{mV}$.

(a) Find the flatband voltage V_{FB} .

SOLUTION

The flatband voltage is equal and opposite to the built-in voltage in the MOS structure

$$V_{FB} = -(\phi_{n^+} - \phi_n) = -(550\text{mV} - 360\text{mV}) = -190\text{mV}$$

(b) Plot the potential $\phi_o(x)$ in thermal equilibrium

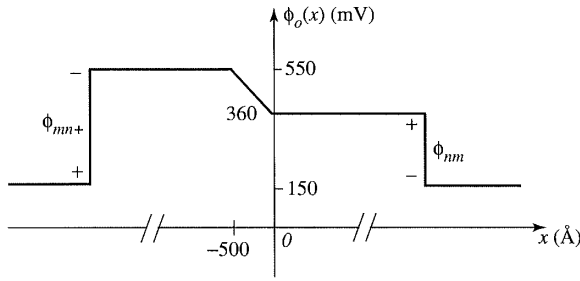
SOLUTION

The MOS capacitor is accumulated in thermal equilibrium, since accumulated electrons under the gate balance the positive gate charge. We can sketch the potential since the substrate charge is a delta function at the SiO_2 silicon interface with value $Q_{No} = -Q_{Go}$, as shown in Fig. Ex3.9A.

(c) Find the threshold voltage V_{Tp} .

SOLUTION

In order to invert the surface, we must first apply V_{FB} to reach flatband. To deplete the substrate, we must apply $V_{GB} < V_{FB}$ to repel the mobile electrons from the surface and leave the positively charged ionized donors. At the onset of inversion, the surface potential will be lowered to the point where it is equal and opposite to that of the n-type bulk: $\phi'_s = -\phi_n$. Adding the flatband voltage, the



► **Figure Ex3.9A** Potential of the MOS structure with n-type substrate in thermal equilibrium.

voltage drop across the depletion region $V_B' = V_{B,\max} = -2\phi_n$ and the voltage drop across the oxide V_{ox}' the threshold voltage V_{Tp} is

$$V_{Tp} = V_{FB} - 2\phi_n + V_{ox}' = V_{FB} - 2\phi_n - \frac{Q_{B,\max}}{C_{ox}}$$

Note that the drop across the oxide is negative since the substrate has a positive depletion charge $Q_{B,\max} > 0$ and the gate charge is negative. Substituting for the maximum depletion charge $Q_{B,\max}$, we find

$$V_{Tp} = V_{FB} - 2\phi_n - \frac{\sqrt{2q\epsilon_s N_d (2\phi_n)}}{C_{ox}} = -0.19 - 0.72 - \frac{4.88 \times 10^{-8} \text{ C/cm}^2}{6.9 \times 10^{-8} \text{ F/cm}} = -1.62 \text{ V}$$

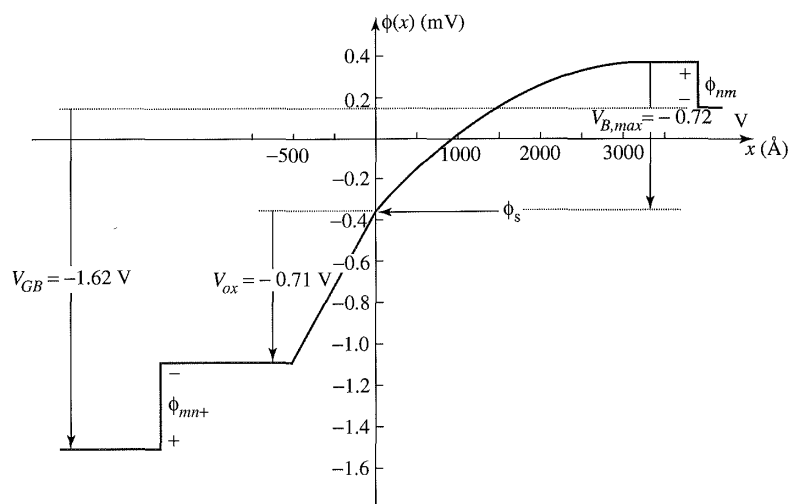
(d) Plot the potential $\phi(x)$ for $V_{GB} = V_{Tp}$.

SOLUTION

When $V_{GB} = V_{Tp} = -1.62 \text{ V}$, the n^+ polysilicon gate has a potential of $0.55 - 1.62 = -1.07 \text{ V}$. The potential in the n-type bulk remains fixed at $\phi_n = 0.36 \text{ V}$ with the surface potential at the onset of inversion $\phi_s = -\phi_n = -0.36 \text{ V}$. The potential varies quadratically in the depletion region, which has a width

$$X_{d,\max} = \sqrt{\frac{2\epsilon_s (2\phi_n)}{qN_d}} = \sqrt{\frac{2 \cdot 11.7 \cdot 8.85 \times 10^{-14} \cdot 0.72}{1.6 \times 10^{-19} \cdot 10^{16}}} = 0.31 \mu\text{m}$$

and linearly in the oxide as shown in Fig. Ex3.9B.



► **Figure Ex3.9B** Potential of MOS structure with n-type substrate for the case where $V_{GB} = V_{Tp}$.

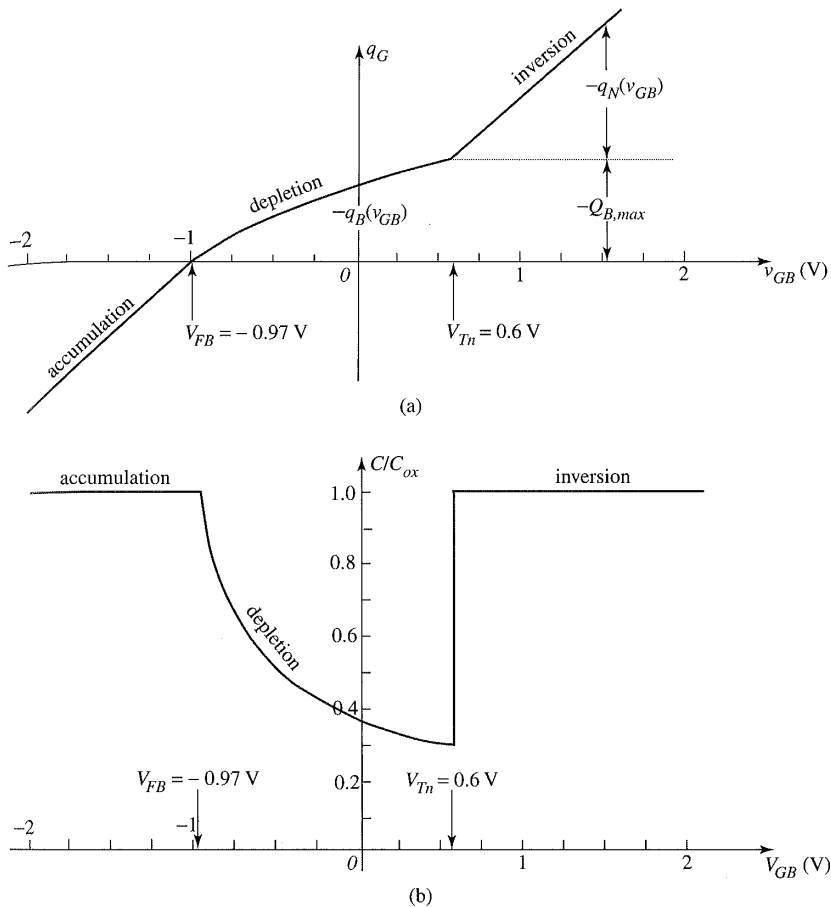
► 3.9 CAPACITANCE OF THE MOS STRUCTURE

In this section, we will investigate the small-signal modeling of the MOS structure. Our approach will parallel Section 3.6 for the pn junction under reverse bias. We begin by viewing the capacitance as a graphical derivative of the charge-voltage characteristics of the capacitor sketched in Fig. 3.25 (for p-type substrate) and Fig. 3.27 (for n-type substrate). By differentiating the expressions for gate charge as a function of gate-bulk bias, we can find mathematical results for the MOS capacitance. Finally, we can gain insight into the physics of the MOS capacitor by determining where the small-signal increment in gate charge is mirrored in the underlying silicon substrate, for the three regions of gate-bulk bias.

3.9.1 Graphical Interpretation

Compared to the pn junction, the MOS structure has a much more complicated charge-storage characteristic. For case of a p-type substrate, we can apply the definition of the capacitance as the slope of $q_G(V_{GB})$ to Fig. 3.25 (repeated for convenience in Fig. 3.35(a)) to derive the plot of $C(V_{GB})$ in Fig. 3.35(b). We have used symbols for the total variables (DC + small-signal) in Fig. 3.35(a), since we are assuming that our analysis in Section 3.7 and Section 3.8 can be extended to time-varying signals.

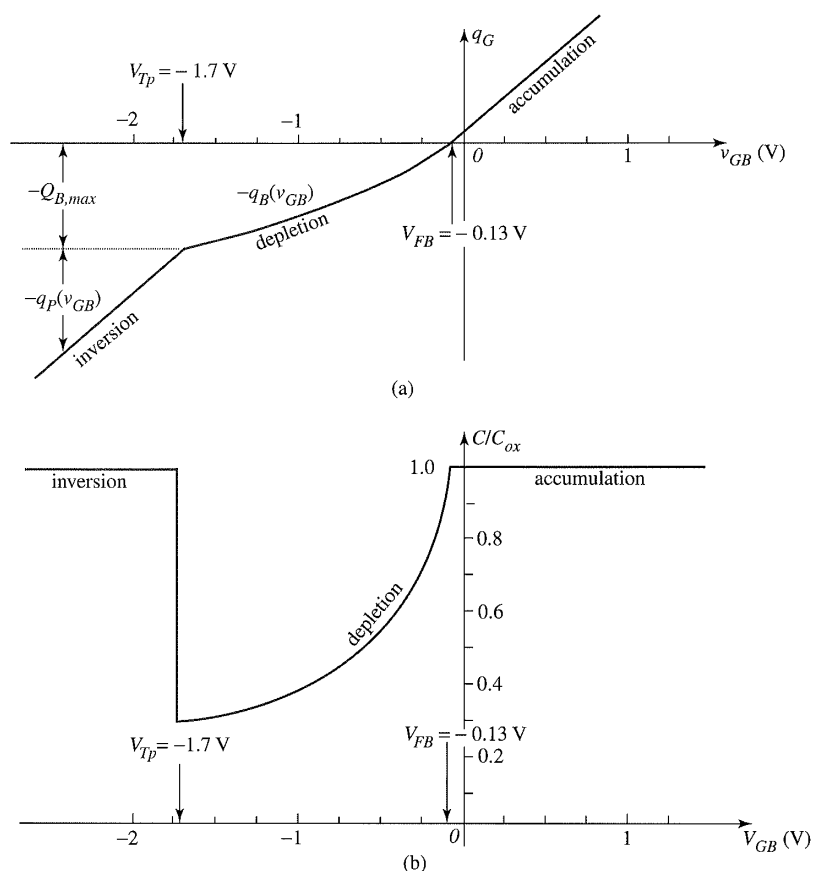
By definition, the capacitance of the MOS structure is the slope of the $q_G(V_{GB})$ curve in Fig. 3.35, (a) evaluated at a particular DC bias voltage V_{GB} . In accumulation and inversion, the gate charge has a term that is proportional to v_{GB} , with a slope equal to C_{ox} . Therefore, the capacitance is independent of the DC bias and is equal



► **Figure 3.35** (a) Gate charge as a function of gate-bulk voltage for an MOS capacitor on a p-type substrate with a 150 Å-thick gate oxide and a substrate doping $N_a = 10^{17} \text{ cm}^{-3}$ and (b) capacitance as a function of gate-bulk voltage, found by graphically differentiating (a).

to the oxide capacitance $C_{ox} = \epsilon_{ox}/t_{ox}$. In Fig. 3.35(b), the capacitance is plotted normalized to C_{ox} . Later in this section, we will explain the reason for the variation of the MOS capacitance with gate bias in the depletion region. The abrupt jump in capacitance at the threshold voltage is a convenient way to measure V_{Tn} .

For an MOS capacitor on an n-type substrate, the gate charge versus gate-bulk voltage is plotted in Fig. 3.27, which is repeated as Fig. 3.36(a). Graphical differentiation yields the capacitance as a function of the DC gate-bulk voltage V_{GB} in Fig. 3.36(b). Note that substrate type can be determined from the capacitance plots in Figs. 3.35(b) and 3.36(b).



► **Figure 3.36** (a) Gate charge as a function of gate-bulk voltage for an MOS capacitor on an n-type substrate, with a 150 Å-thick gate oxide and a substrate doping $N_d = 10^{17} \text{ cm}^{-3}$ and (b) capacitance as a function of gate-bulk voltage, found by graphically differentiating (a).

3.9.2 Mathematical Formulation

The expressions for gate charge as a function of gate-bulk bias in Eqs. (3.150)–(3.152) can be differentiated to find the capacitance in accumulation, depletion, and inversion. The capacitance of the metal-oxide-semiconductor structure is defined as

$$C = \left. \frac{dq_G}{dv_{GB}} \right|_{v_{GB}} \quad (3.153)$$

In accumulation, the MOS capacitance for a p-type substrate is

$$C = \frac{d}{dv_{GB}} [C_{ox} (v_{GB} - V_{FB})] \Big|_{v_{GB} \leq v_{FB}} = C_{ox} \text{ for } V_{GB} \leq V_{FB} \quad (3.154)$$

For the case of inversion, the MOS capacitance for a p-type substrate is the same

$$C = \frac{d}{dv_{GB}} [(C_{ox} (v_{GB} - V_{Tn}) - Q_{B,max})] \Big|_{v_{GB} \geq v_{Tn}} = C_{ox} \quad (3.155)$$

since the bulk charge is fixed at $Q_{B,max}$ in inversion. The situation in depletion requires differentiation of Eq. (3.151), which is valid for gate-bulk biases $V_{FB} \leq V_{GB} \leq V_{Tn}$

$$C = \frac{dq_G}{dv_{GB}} \Big|_{V_{FB} \leq v_{GB} \leq v_{Tn}} = \frac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2 (V_{GB} - V_{FB})}{q\epsilon_s N_a}}} \quad (3.156)$$

This result allows the capacitance versus gate-bulk bias to be quantified in the depletion region. The minimum capacitance occurs just prior to inversion, which we can evaluate by substituting $V_{GB} = V_{Tn}$ into Eq. (3.156)

$$C(V_{GB} = V_{Tn}) = \frac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2 (V_{Tn} - V_{FB})}{q\epsilon_s N_a}}} \quad (3.157)$$

In order to interpret the meaning Eq. (3.156), we will express it in terms of the depletion width $X_d(V_{GB})$ from Eq. (3.130), which we repeat here for convenience

$$X_d(V_{GB}) = \left(\frac{\epsilon_s}{C_{ox}} \right) \left(\sqrt{1 + \frac{2C_{ox}^2 (V_{GB} - V_{FB})}{q\epsilon_s N_a}} - 1 \right) \quad (3.158)$$

After some algebra, the capacitance in the depletion region can be written as

$$C = \frac{C_{ox}}{\left(\frac{C_{ox}}{\epsilon_s} \right) X_d(V_{GB}) + 1} = \frac{C_{ox} \left(\frac{\epsilon_s}{X_d(V_{GB})} \right)}{C_{ox} + \left(\frac{\epsilon_s}{X_d(V_{GB})} \right)} \text{ for } V_{FB} \leq V_{GB} \leq V_{Tn} \quad (3.159)$$

From Section 3.6, we can identify the capacitance C_b of the depletion region as

$$C_b = \frac{\epsilon_s}{X_d(V_{GB})} \quad (3.160)$$

which enables Eq. (3.159) to be rewritten as the capacitances C_{ox} and C_b in series

$$C = \frac{C_{ox} C_b}{C_{ox} + C_b} \text{ for } V_{FB} \leq V_{GB} \leq V_{Tn} \quad (3.161)$$

Later in this section, we will see why the oxide and depletion capacitances are in series combination when the MOS capacitor is biased in depletion.

EXAMPLE 3.10 MOS Capacitance-Voltage Curves

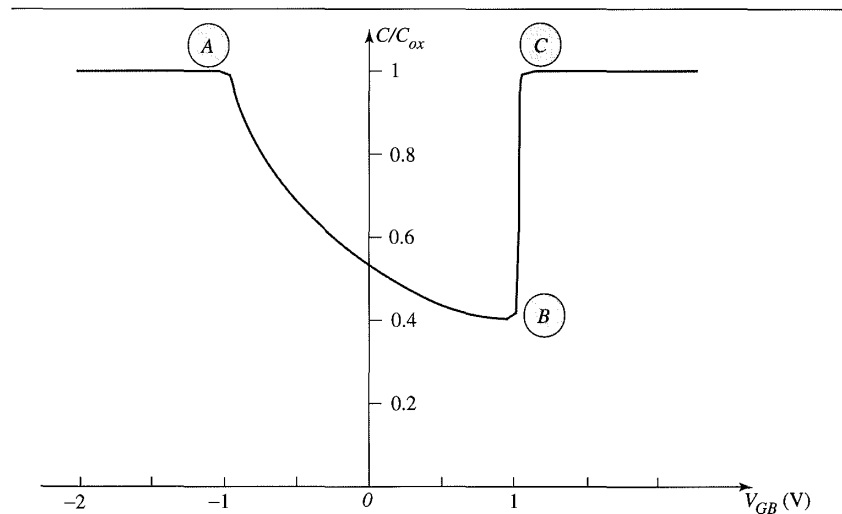
Shown below is a measured “C-V” curve for an MOS capacitor. The gate is n⁺ polysilicon with $\phi_{n+} = 550$ mV.

(a) From the normalized capacitance-voltage characteristic, determine the substrate type and doping level.

SOLUTION

To make sense of the C-V curve, we must determine whether point A or C corresponds to flatband. Going from point A to point B, the capacitance decreases with increasing voltage, which corresponds to a widening depletion region. Also, the transition from B to C is much more abrupt than the transition from A to B. These observations are consistent with A being the flatband condition and C being inversion. From the characteristic, we estimate that

$$V_{FB} = -1\text{V} \quad V_T = 1\text{V}$$



► **Figure Ex3.10** Measured capacitance-voltage curve for an MOS structure with the capacitance normalized to its maximum value—the oxide capacitance.

Using the definition of the flatband voltage

$$V_{FB} = -1\text{ V} = -(0.55\text{ V} - \phi_{sub}) \rightarrow \phi_{sub} = -450\text{ mV}$$

where ϕ_{sub} is the substrate potential. Since ϕ_{sub} is negative, the substrate is p-type. To find the acceptor doping level in the substrate, we apply the 60mV rule.

$$\phi_p = (-60\text{ mV}) \log\left(\frac{N_a}{1 \times 10^{10}\text{ cm}^{-3}}\right) = -450\text{ mV} \rightarrow N_a = 3.16 \times 10^{17}\text{ cm}^{-3}$$

(b) Determine the oxide thickness t_{ox} .

SOLUTION

To find the oxide thickness t_{ox} , we must first find the oxide capacitance. Since the capacitance has been normalized, it is not possible to use the measurements in accumulation or in inversion to find C_{ox} directly. Instead, we use the depletion region curve where the capacitance is the series combination of C_{ox} and the capacitance of the depletion region C_b . From Eq. (3.157), the minimum normalized capacitance is given by

$$C_{\min}/C_{ox} = C(V_{GB} = V_{Tn}^-)/C_{ox} = \frac{1}{\sqrt{1 + \frac{2C_{ox}^2 (V_{Tn} - V_{FB})}{q\epsilon_s N_a}}}$$

Solving for the oxide capacitance, we find that

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \sqrt{\frac{q\epsilon_s N_a}{2(V_{Tn} - V_{FB})} \left[\left(\frac{C_{ox}}{C_{\min}} \right)^2 - 1 \right]}$$

Substituting $C_{\min}/C_{ox} = 0.4$ and the other parameters from part (a) into the expression for the oxide thickness, we find that

$$t_{ox} = \frac{\epsilon_{ox}}{\sqrt{\frac{q\epsilon_s N_a}{2(V_{Tn} - V_{FB})} \left[\left(\frac{C_{ox}}{C_{\min}} \right)^2 - 1 \right]}}$$

$$t_{ox} = \frac{(3.9)(8.85 \times 10^{-14})}{\sqrt{\frac{1.6 \times 10^{19}(1.035 \times 10^{-12})(3.16 \times 10^{17})}{2(1 - (-1))} \left(\left(\frac{1}{0.4} \right)^2 - 1 \right)}} = 132\text{ \AA}$$

An alternative approach is to use the threshold voltage to calculate C_{ox} from Eq. (3.95). Using this approach, we find that $t_{ox} = 125\text{ \AA}$ which is about 5% lower. Uncertainties in reading the threshold voltage from the C - V curve and limitations of the delta-depletion approximation account for the discrepancy.

(c) From your results from part (a) and (b), find the gate charge Q_G for $V_{GB} = -3\text{ V}$ and for $V_{GB} = +3\text{ V}$

SOLUTION

For $V_{GB} = -3 \text{ V} < V_{FB}$, the MOS capacitor is in accumulation. The gate charge is

$$Q_G = C_{ox}(V_{GB} - V_{FB}) = 2.55 \times 10^{-7} \text{ F/cm}^2 (-3 \text{ V} - (-1 \text{ V})) = -5.1 \times 10^{-7} \text{ C/cm}^2$$

For $V_{GB} = 3 \text{ V} > V_{Tn}$, the MOS capacitor is in inversion. The gate charge is equal and opposite to the sum of the magnitudes of the inversion electron charge and the magnitude of the maximum depletion charge. The latter is found from Eq. (3.140) and Eq. (3.142)

$$Q_G = C_{ox}(V_{GB} - V_{Tn}) - Q_{B,\max} = 5.1 \times 10^{-7} + 2.8 \times 10^{-7} \text{ C/cm}^2 = 7.9 \times 10^{-7} \text{ C/cm}^2$$

3.9.3 Physical Interpretation

In order to make physical sense of this rather complicated capacitance-voltage curve, we will investigate where the increment in gate charge q_g is mirrored for each of the three different regions of operation: accumulation, depletion, and inversion. Starting with a MOS capacitor biased in accumulation, Fig. 3.37 illustrates the charge density before and after a positive increment q_g is added to the DC gate charge Q_G . The increment in gate charge is due to a positive increment in the gate voltage v_{gb} . In Fig. 3.37(a), we note that $Q_G < 0$ for accumulation. The charge increment on the gate is mirrored in the accumulated holes under the gate oxide as shown in the small-signal charge density plotted in Fig. 3.37(c). The incremental charge distribution is identical to that of the parallel-plate capacitor in Ex. 3.1. Therefore, the capacitance of the MOS structure in accumulation is C_{ox} , the oxide capacitance.

Figure 3.38 shows the more complicated situation for a MOS capacitor biased in depletion. In this case, the gate charge is positive and the gate-bulk bias voltage is in the range $V_{FB} \leq V_{GB} \leq V_{Tn}$. The gate charge increment is mirrored at the bottom of the depletion region as shown in Fig. 3.38(c). The incremental charges $+q_g$ and $-q_g$ are separated by an oxide layer of thickness t_{ox} with capacitance $C_{ox} = \epsilon_{ox}/t_{ox}$, and a depletion region of thickness $X_d(V_{GB})$ with capacitance $C_b = \epsilon_s/X_d(V_{GB})$. The equivalent circuit is the series combination of C_{ox} and C_b as shown in Fig. 3.38(c). Therefore, the MOS capacitance when biased in depletion is

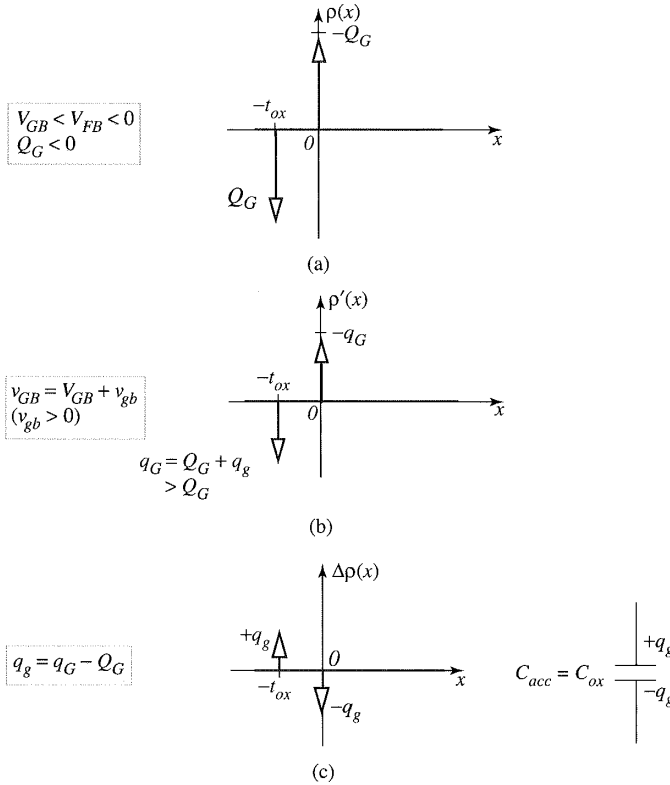
$$C = \frac{C_{ox} C_b}{C_{ox} + C_b} \text{ for } V_{FB} \leq V_{GB} \leq V_{Tn}. \quad (3.162)$$

which explains the physical basis for Eq. (3.161).

For an inverted MOS capacitor, an increment in gate voltage is mirrored in an increase electron charge in the inversion layer as shown in Fig. 3.39. The depletion charge is fixed and does not vary with gate voltage as is reflected in the constant depletion width $X_{d,\max}$ in inversion. As a result, the capacitance in inversion is again the oxide capacitance

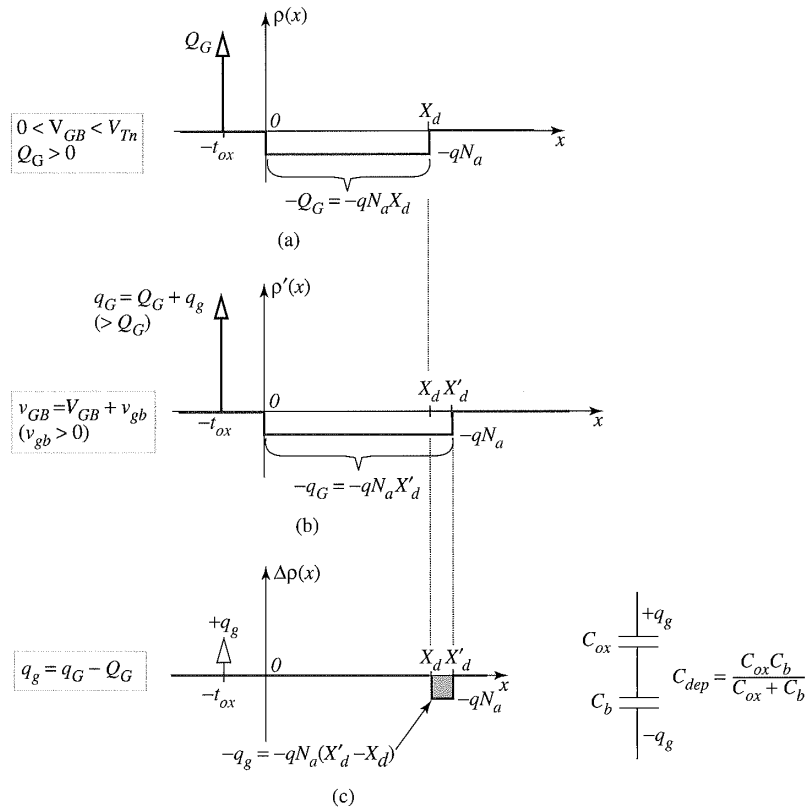
$$C = C_{ox} \text{ for } V_{GB} \geq V_{Tn} \quad (3.163)$$

Our analysis of the MOS structure has not considered the time variation of voltages or charges. In fact, our use of the logarithmic relationship between potential and carrier concentration for finding the carrier concentrations in the silicon substrate means we have implicitly assumed that sufficient time has elapsed for transient currents to die out. Measurement of the capacitance-voltage curves shown in this chapter requires use of a slow ramp of the bias voltage V_{GB} and a low-frequency AC

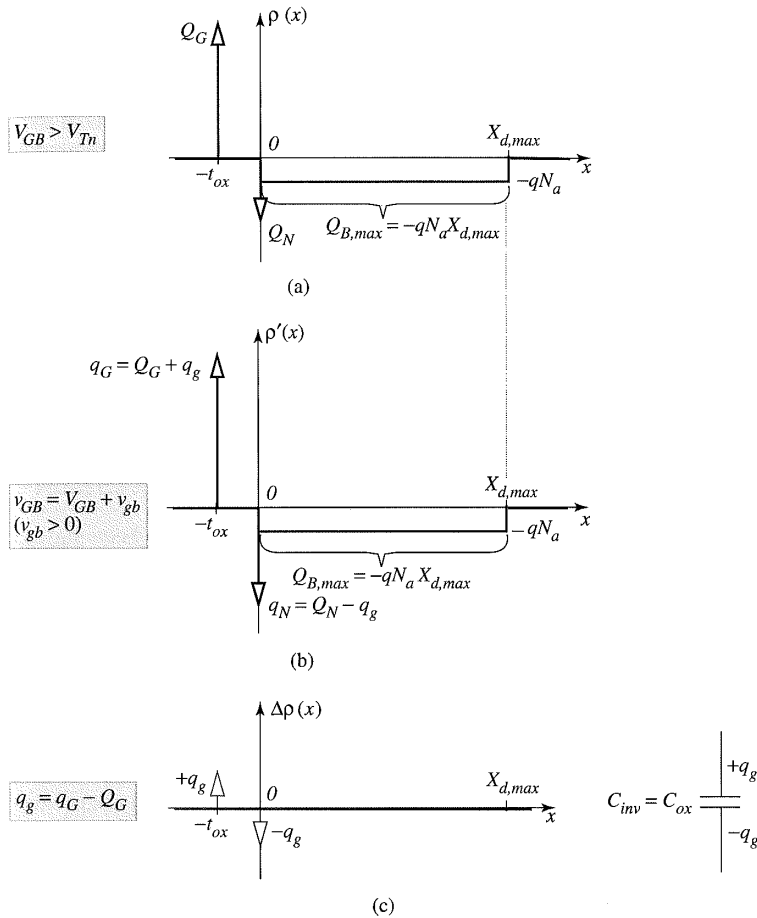


► **Figure 3.37** Charge density $\rho(x)$ for a MOS structure on a p-type substrate in accumulation: (a) bias voltage $V_{GB} < V_{FB}$, (b) perturbed charge density $\rho'(x)$ for $V_{GB} = V_{GB} + v_{gb}$, where the incremental voltage $v_{gb} > 0$, and (c) incremental charge density $\Delta\rho(x) = \rho'(x) - \rho(x)$ showing that the incremental charges $\pm q_g$ are separated by the gate oxide. The small-signal model in accumulation is the oxide capacitance.

incremental voltage $v_{gb}(t)$. We will leave further discussion of the various ways to measure MOS C-V curves to more advanced texts in device physics or IC fabrication technology.



► **Figure 3.38** Charge density $\rho(x)$ for a MOS structure on a p-type substrate in depletion: (a) bias voltage $V_{FB} < V_{GB} < V_{Tn}$, (b) perturbed charge density $\rho'(x)$ for $v_{GB} = V_{GB} + v_{gb}$, where the incremental voltage $v_{gb} > 0$, and (c) incremental charge density $\Delta\rho(x) = \rho'(x) - \rho(x)$ showing that the incremental charges $\pm q_g$ are separated by the gate oxide and the depletion region. The small-signal model in depletion is two capacitors in series.



► **Figure 3.39** Charge density $\rho(x)$ for a MOS capacitor on a p-type substrate in inversion: (a) bias voltage $V_{GB} > V_{Tn}$, (b) perturbed charge density $\rho'(x)$ for $V_{GB} = V_{GB} + v_{gb}$, where the incremental voltage $v_{gb} > 0$, and (c) incremental charge density $\Delta\rho(x) = \rho'(x) - \rho(x)$ showing that the incremental gate charge is mirrored by an increment in the electron inversion charge. Therefore, the small-signal model in the inversion region is again the oxide capacitance.

► SUMMARY

This chapter began with a review of basic electrostatic theory and its application to one-dimensional device structures. These concepts were applied to the pn junction, first in thermal equilibrium and then under a reverse bias $V_D < 0$. The charge density in this structure was modeled using the depletion approximation, in which the electron and hole concentrations in the transition region at the junction were assumed to be negligible. In order to pin down the potential in silicon in thermal equilibrium, we selected a potential reference such that intrinsic silicon is at zero volts. The relationship of potential to the logarithm of carrier concentration followed from this reference, with n-type silicon having a positive potential and p-type silicon a negative potential. The very important concept of small-signal modeling was introduced by finding the capacitance of the reverse-biased pn junction.

The MOS capacitor was the second important device structure analyzed in this chapter. Its nonlinear charge-storage characteristics were described by finding the charge stored on the gate as a function of the applied voltage using the delta-depletion approximation. An unusual and very useful feature of the MOS structure is the possibility of inverting the type of the substrate, which means creating a surface layer that is of opposite type to the substrate. Finally, the small-signal capacitance of the MOS capacitor was found as a function of the applied voltage.

The following important concepts and techniques should have been mastered in Chapter 3.

- ◆ Interrelationships between charge density, electric field, and electrostatic potential in one dimension from Gauss's Law and the definition of potential.
- ◆ One-dimensional boundary conditions on electric field and potential.
- ◆ Techniques for graphically sketching the charge density, electric field, and potential without doing the formal mathematics.
- ◆ Equilibrium in the pn junction as a balance of drift and diffusion current densities.
- ◆ The logarithmic relationship between potential and electron and hole concentration in thermal equilibrium.
- ◆ Charge density in pn junctions using the depletion approximation.
- ◆ Electrostatics of the pn junction under reverse bias.
- ◆ Contact potentials and the use of Kirchhoff's voltage law to show the current is zero in a short-circuited pn junction in equilibrium.
- ◆ Capacitance of the pn junction and its interpretation from the small-signal model of charge storage.
- ◆ The MOS structure and its electrostatics in thermal equilibrium.
- ◆ Accumulation, depletion, and inversion of the MOS capacitor and the corresponding charge densities
- ◆ The delta-depletion approximation and the quantitative analysis of MOS electrostatics
- ◆ Capacitance of the MOS structure in accumulation, depletion, and inversion.

► FURTHER READING

Reverse-Biased pn Junction

1. G. N. Neudeck, *The PN Junction Diode*, Modular Series on Solid State Devices, 2nd ed. Vol. II, G. W. Neudeck and R. F. Pierret, eds., Addison-Wesley, 1989, Chapter 2. About the same level.
2. R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed., Wiley, 1986, Chapter 4. More advanced discussion of the depletion approximation; includes Fermi level concept.

MOS Capacitor

1. C. G. Fonstad, *Microelectronic Devices and Circuits*, McGraw-Hill, 1994, Chapter 9. About the same level; includes a discussion of the effects of oxide charge.
2. R. F. Pierret, *Field Effect Devices*, Modular Series on Solid State Devices, Vol. IV, G. W. Neudeck and R. F. Pierret, eds., Addison-Wesley, 1983, Chapters 2–4. More advanced discussion, including the concept of the Fermi level.

► PROBLEMS

EXERCISES

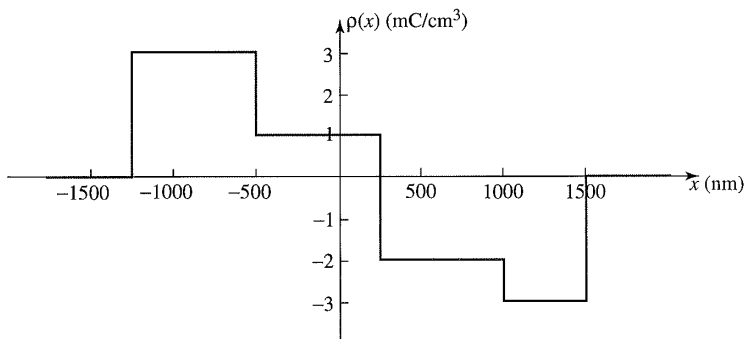
Permittivities: crystalline silicon: $\epsilon_s = 1.035 \times 10^{-12}$ F/cm
 silicon dioxide (SiO_2): $\epsilon_{ox} = 3.45 \times 10^{-13}$ F/cm
 silicon nitride (Si_3N_4): $\epsilon_n = 8.63 \times 10^{-13}$ F/cm

E3.1 The charge distribution in a sample of silicon is given in Fig. E3.1.

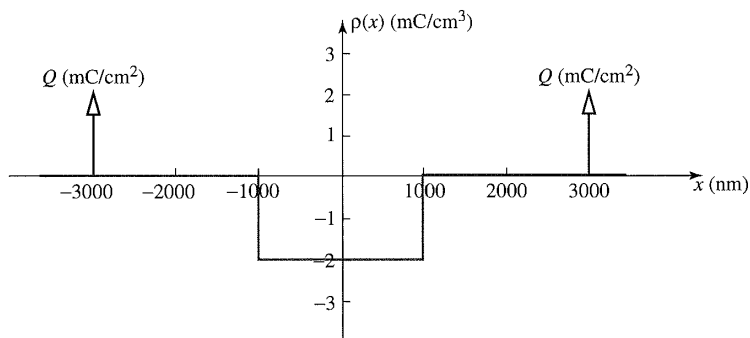
- (a) Determine the sign of the electric field at $x = -750$ nm and $x = 250$ nm.
- (b) Determine the numerical value of the electric field at $x = -250$ nm.
- (c) Plot the electric field as a function of x .

E3.2 The charge distribution in an IC structure is shown in Fig. E3.2.

- (a) Find the numerical value of the surface charges Q so that the total charge is zero in the structure. Note that the units of Q are C/cm^2 .



► Figure E3.1



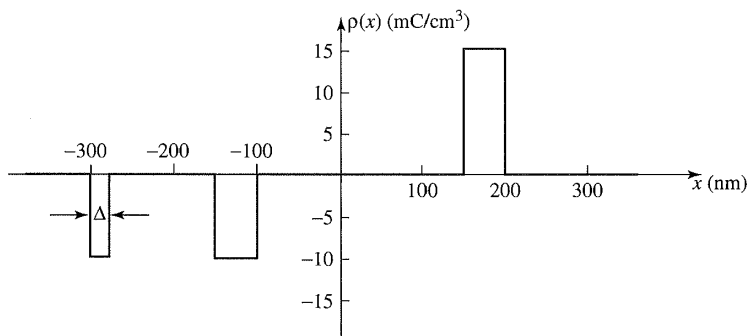
► Figure E3.2

- (b) Plot the electric field $E(x)$ through the structure.
 (c) Sketch the potential $\phi(x)$, given that the potential $\phi(\pm 3000) = 0$.

E3.3 The charge distribution in a silicon region is plotted in Fig. E3.3.

- (a) Find the width Δ so that the silicon region is electrically neutral. The boundary at $x = -300$ nm is fixed.
 (b) Find the numerical value of the electric field at $x = -250$ nm and at $x = 150$ nm.
 (c) Plot the electric field $E(x)$.
 (d) If the potential $\phi(-300 \text{ nm}) = -500$ mV, find the potential at $x = 350$ nm.

E3.4 The charge distribution in a silicon region is given in Fig. E3.4. There is no need to find $E(x)$ to solve (a)–(c).

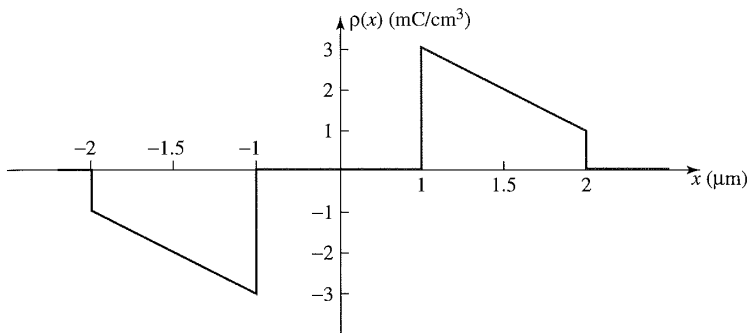


► Figure E3.3

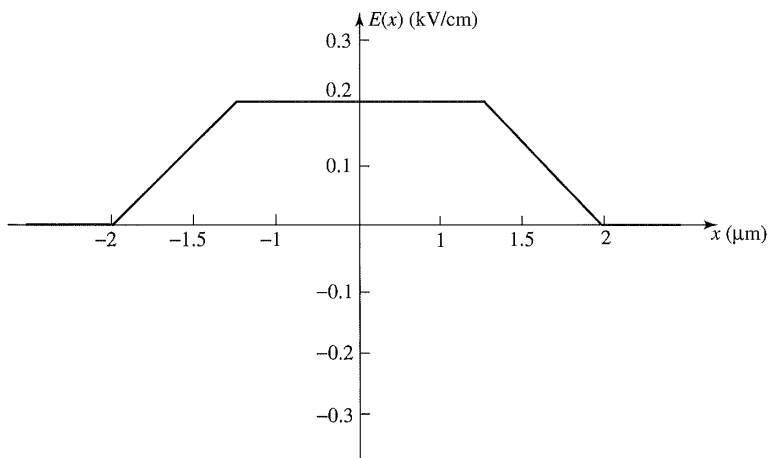
- (a) Find the numerical value of the electric field E at $x = -1.5 \mu\text{m}$.
 (b) Find the numerical value of the electric field E at $x = 0$.
 (c) Find the numerical value of the electric field E at $x = 1.5 \mu\text{m}$.

E3.5 The electric field in a silicon structure is given in Fig. E3.5.

- (a) Plot the charge density $\rho(x)$.



► **Figure E3.4**



► **Figure E3.5**

(b) If the potential $\phi(-2\text{ }\mu\text{m}) = -500\text{ mV}$, what is the potential at $x = 0$? What is the potential at $x = 2\text{ }\mu\text{m}$. Note that you don't need to solve for the potential function in order to answer this question.

(c) Sketch the potential $\phi(x)$, given that the potential $\phi(-2\text{ }\mu\text{m}) = -500\text{ mV}$.

E3.6 In the plot of the electric field $E(x)$ in Fig. E3.6, the materials consist of a metal film ($x < t_i$), an insulator with unknown permittivity ($t_i < x < 0$) and silicon ($x \geq 0$).

(a) Given that there is no sheet charge located at $x = 0$, what is the numerical value of the permittivity of the insulating film?

(b) Sketch the charge density $\rho(x)$ through the structure.

(c) How much charge [C/cm^2] is on the metal film at $x = t_i$?

(d) Given that the potential of the metal is $\phi_m = 350\text{ mV}$, sketch $\phi(x)$.

E3.7 The electric field in a metal-SiO₂-silicon sandwich is shown in Fig. E3.7. The metal is located at $x < -100\text{ }\text{\AA}$, the oxide film is located between $-100\text{ }\text{\AA} < x < 0$, and the silicon substrate ranges over $x > 0$. There is a sheet charge at $x = 0$ with units of C/cm^2 .

(a) From the plot of electric field in Fig. E3.7, determine the magnitude and sign of the sheet charge at $x = 0$.

(b) What is the charge on the metal film at $x = -100\text{ }\text{\AA}$?

(c) Sketch the potential $\phi(x)$, given that $\phi(-100\text{ }\text{\AA}) = -850\text{ mV}$.

E3.8 The electric field $E(x)$ in a silicon region is given in Fig. E3.8.

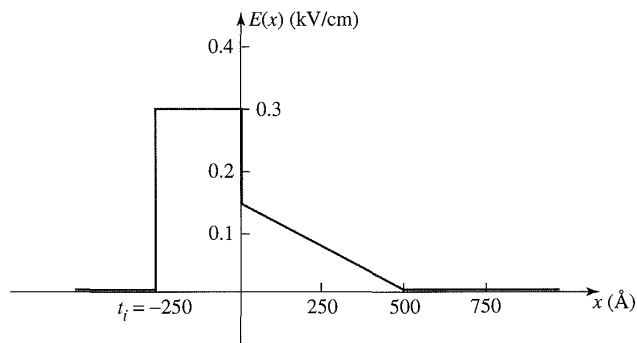
(a) Plot the charge density $\rho(x)$.

(b) Given that the potential $\phi(0) = 0$, sketch the potential $\phi(x)$.

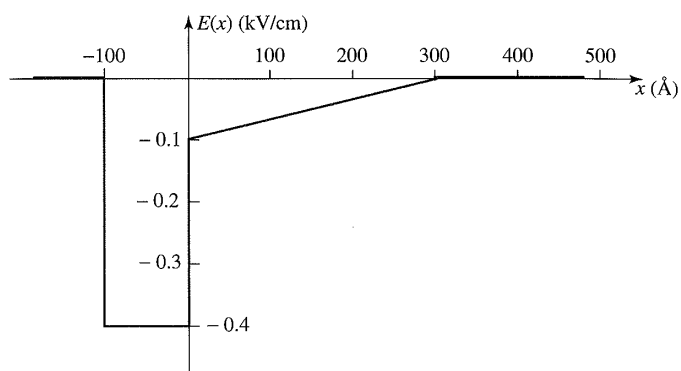
E3.9 The potential $E(x)$ through a silicon sample is graphed in Fig. E3.9.

(a) Sketch the potential $\phi(x)$, given that $\phi(0) = 0.5\text{ V}$.

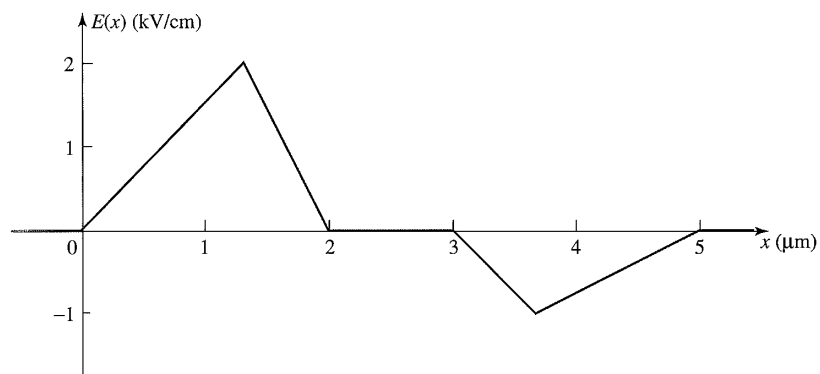
(b) Sketch the charge density $\rho(x)$.



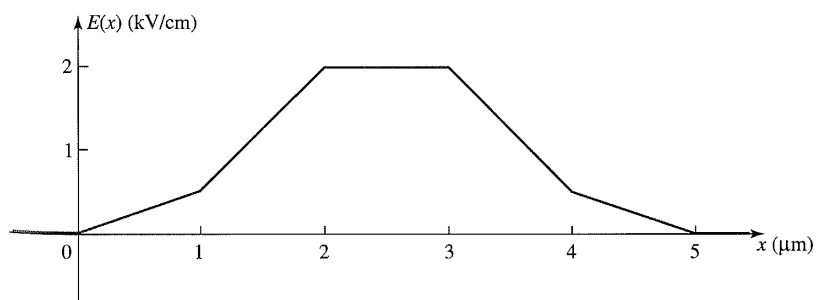
► Figure E3.6



► Figure E3.7



► Figure E3.8



► Figure E3.9