

E3.10 This exercise investigates the depletion approximation, for a pn junction diode with symmetrical doping $N_a = N_d = 10^{15} \text{ cm}^{-3}$.

- Find the thermal equilibrium potential $\phi_o(x)$ according to the depletion approximation.
- Plot on a linear scale the electron and hole concentrations through the depletion region, in thermal equilibrium.
- Plot on a linear scale the charge density $\rho(x)$ in the depletion region, including the contributions of the electrons and holes from your answer in part (b). Estimate the percentage error in the charge on one side of the junction, if we neglect the electron and hole charge.

E3.11 Consider a pn junction diode with symmetrical doping $N_a = N_d = 10^{17} \text{ cm}^{-3}$.

- What is the magnitude of the electric field $|E_o(x=0)|$ (where the metallurgical junction is located at $x=0$) in thermal equilibrium?
- For what value of bias voltage V_D is the electric field at $x=0$ increased by a factor of 3?
- Plot $|E(0)|$ as a function of V_D for $-7.5 \text{ V} < V_D < 0$.

E3.12 Consider a pn junction with p-side doping $N_a = 10^{19} \text{ cm}^{-3}$ and n-side doping $N_d = 10^{17} \text{ cm}^{-3}$.

- Sketch the potential in thermal equilibrium, using the approximation that the junction is “one-sided” as discussed in Ex. 3.5.
- What is the electric field $|E_o(x=0)|$ (where the metallurgical junction is located at $x=0$) in thermal equilibrium?
- If the maximum electric field allowable in the junction is $E_{\max} = 10^4 \text{ V/cm}$ what is the maximum reverse bias permitted?

E3.13 Low doped silicon is used in particle detectors, in order to obtain a wide depletion region. Consider a pn junction with p-side doping $N_a = 5 \times 10^{12} \text{ cm}^{-3}$ and n-side doping $N_d = 10^{17} \text{ cm}^{-3}$.

- What is the thermal equilibrium depletion region width?
- What is the reverse bias needed to increase the depletion width to $50 \mu\text{m}$?
- If the maximum electric field allowable in the junction is $E_{\max} = 5 \times 10^5 \text{ V/cm}$ what is the maximum depletion width? What is the bias voltage corresponding to the maximum depletion width?

E3.14 We would like to investigate the charge distribution in a pn junction with doping levels $N_a = 10^{16} \text{ cm}^{-3}$ and $N_d = 5 \times 10^{16} \text{ cm}^{-3}$.

- For $V_D = -2.5 \text{ V}$, plot the charge density $\rho(x)$.
- We add to V_D a time-varying voltage $v_d(t) = (250 \text{ mV})\cos(\omega t)$. Plot the charge density when $v_D(t) = V_D + v_d(t)$ is at its maximum ($\rho_{\max}(x)$) and its minimum ($\rho_{\min}(x)$).
- Plot the difference between $\rho_{\max}(x)$ and $\rho(x)$ and the difference between $\rho_{\min}(x)$ and $\rho(x)$ on the same graph. Find the small-signal charge per unit area q_j in units C/cm^2 for each case. Are they equal and opposite? Why or why not?

- (d) Find the depletion capacitance $C(V_D)$ for $V_D = -2.5$ V and the small-signal depletion charge q_j , assuming that $v_d(t)$ can be considered a small signal. Compare with your answer to (c).

E3.15 In order to evaluate the junction diode as a circuit element, we would like to know the capacitance per unit area and the tuning range.

- Plot the capacitance per unit area in thermal equilibrium versus the p-side doping concentration from $N_a = 10^{16} \text{ cm}^{-3}$ to 10^{17} cm^{-3} . Assume that the n-side doping concentration is $N_d = 10^{19} \text{ cm}^{-3}$.
- If the maximum electric field allowable in the junction is $E_{\max} = 10^4$ V/cm, plot the maximum reverse bias $V_{D,\max}$ on the capacitor as a function of the p-side doping concentration.
- From your results in part (b), plot the ratio of $C(0)/C(V_{D,\max})$ as a function of p-side doping concentration.

E3.16 We are interested in using a reverse-biased pn junction as a small-signal capacitor. The doping levels are $N_a = 10^{16} \text{ cm}^{-3}$ and $N_d = 10^{18} \text{ cm}^{-3}$. We would like to have a capacitor with $C = 500 \text{ fF} \pm 150 \text{ fF}$.

- What is the capacitance per unit area [units: $\text{fF}/\mu\text{m}^2$] for $V_D = 0$ V.
- What is the area needed for the capacitor and the voltage range needed for tuning? Note that $V_D = 0$ V must correspond to $C = 650 \text{ fF}$, the maximum capacitance.

E3.17 An MOS capacitor is fabricated on a p-type silicon substrate with doping concentration $N_a = 10^{16} \text{ cm}^{-3}$, using an n^+ polysilicon gate.

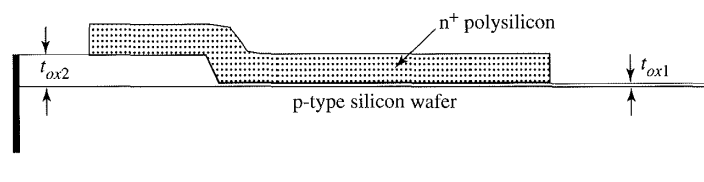
- What is the flatband voltage, V_{FB} ?
- What is the surface potential in inversion?
- What is the maximum width of the depletion region?
- For $t_{ox} = 200 \text{ \AA}$, what is the threshold voltage V_{Tn} ?

E3.18 An MOS capacitor is fabricated on an n-type silicon substrate with doping concentration $N_d = 5 \times 10^{15} \text{ cm}^{-3}$, using an n^+ polysilicon gate.

- What is the flatband voltage, V_{FB} ?
- What is the surface potential in inversion?
- What is the maximum width of the depletion region?
- For $t_{ox} = 150 \text{ \AA}$, what is the threshold voltage V_{Tp} ?

E3.19 In an IC containing MOS structures, the n^+ polysilicon gate is often used as an interconnect layer. In the cross section in Fig. E3.19, the polysilicon layer forms a parasitic MOS capacitor over the “field” region in between devices. The oxide thickness $t_{ox1} = 200 \text{ \AA}$ and the substrate doping is $N_a = 5 \times 10^{16} \text{ cm}^{-3}$.

- Find the threshold voltage V_{Tn1} of the MOS capacitor formed over the thin oxide of thickness t_{ox1} .
- What thickness t_{ox2} of field oxide is required if the threshold voltage V_{Tn2} of this MOS capacitor must be a factor of 5 higher than V_{Tn1} ?
- If the substrate doping under the field regions is increased by a factor of 10 and the doping in the thin-oxide region kept at $5 \times 10^{16} \text{ cm}^{-3}$, what is the thickness t_{ox2} such that $V_{Tn2} = 5 V_{Tn1}$?



► Figure E3.19

E3.20 It is occasionally useful to design a MOS capacitor with a threshold voltage $V_T = 0$ V. The oxide thickness is $t_{ox} = 250$ Å and we use an n^+ polysilicon gate.

- What p-type substrate doping concentration is required for $V_{Tn} = 0$ V? An iterative approach may be helpful, since the substrate potential ϕ_p is a weak function of the doping concentration.
- Sketch the potential $\phi_0(x)$ in thermal equilibrium.

E3.21 This exercise concerns an MOS capacitor with an n^+ polysilicon gate, a 500 Å-thick gate oxide, and a p-type substrate with acceptor concentration $N_a = 7.5 \times 10^{15} \text{ cm}^{-3}$.

- If the gate charge is $Q_G = -1 \times 10^{-7} \text{ C/cm}^2$, sketch the charge density through the MOS capacitor.
- For the gate charge in part (a), what is the gate-bulk bias V_{GB} ?
- If the gate charge is $Q_G = +2.5 \times 10^{-7} \text{ C/cm}^2$, sketch the charge density through the MOS capacitor.
- For the gate charge in part (c), what is the inversion charge Q_N in C/cm^2 ?
- For the gate charge in part (c), what is the gate-bulk bias V_{GB} ?

E3.22 For this exercise, the MOS capacitor has an n^+ polysilicon gate, a 450 Å-thick gate oxide, and an n-type substrate with donor concentration $N_d = 7.5 \times 10^{16} \text{ cm}^{-3}$.

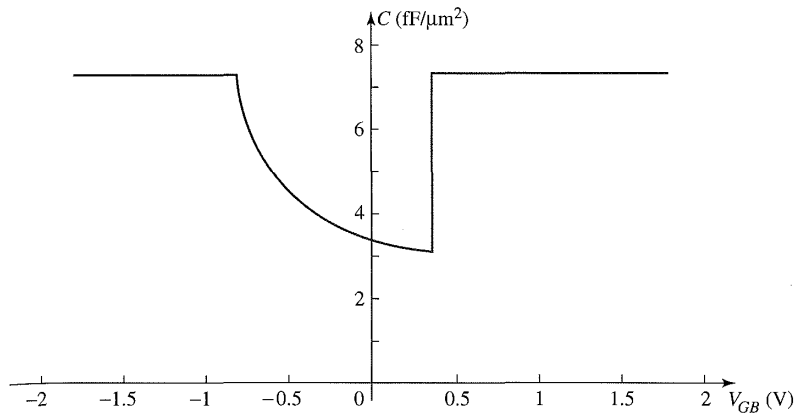
- If the gate charge is $Q_G = 2 \times 10^{-7} \text{ C/cm}^2$, sketch the charge density through the MOS capacitor.
- For the gate charge in part (a), what is the gate-bulk bias V_{GB} ?
- If the gate charge is $Q_G = -5 \times 10^{-7} \text{ C/cm}^2$, sketch the charge density through the MOS capacitor.
- For the gate charge in part (c), what is the inversion charge Q_P in C/cm^2 ?

E3.23 The MOS capacitor is sometimes used for storing charge. Consider an MOS capacitor with n^+ polysilicon gate, $t_{ox} = 100$ Å, and a p-type silicon substrate with an acceptor concentration $N_a = 10^{17} \text{ cm}^{-3}$.

- What is the threshold voltage, V_{Tn} ?
- For a capacitor with area $1 \mu\text{m} \times 5 \mu\text{m}$ and a bias voltage $V_{GB} = 2.9$ V, what is the inversion layer electron charge, Q_N in C? What is the number of electrons stored in the capacitor?

E3.24 The capacitance-voltage curve for an MOS capacitor with an n^+ polysilicon gate is given in Fig. E3.24.

- What is the flatband voltage, V_{FB} ? What is the threshold voltage, V_T ?
- What is the oxide thickness, t_{ox} ?

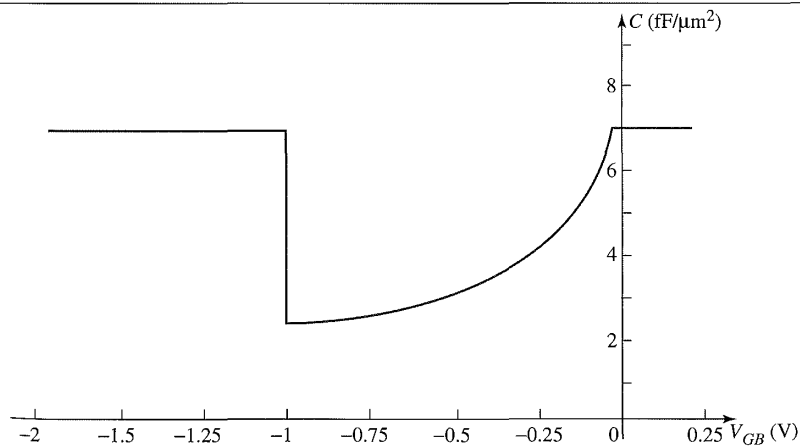


► Figure E3.24

- (c) What is the substrate type?
- (d) What is the substrate doping?

E3.25 The capacitance-voltage curve for an MOS capacitor with an n^+ polysilicon gate is given in Fig. E3.25.

- (a) What is the flatband voltage, V_{FB} ? What is the threshold voltage, V_T ?
- (b) What is the oxide thickness, t_{ox} ?
- (c) What is the substrate type?
- (d) What is the substrate doping?



► Figure E3.25

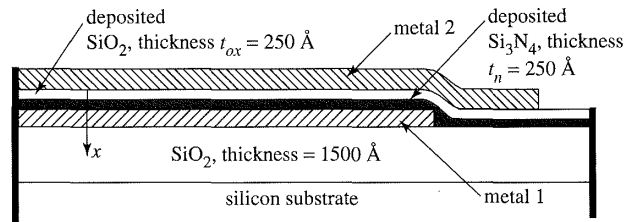
PROBLEMS

P3.1 An aluminum-aluminum capacitor has a composite dielectric of Si_3N_4 (silicon nitride) and SiO_2 with thicknesses indicated in Fig. P3.1.

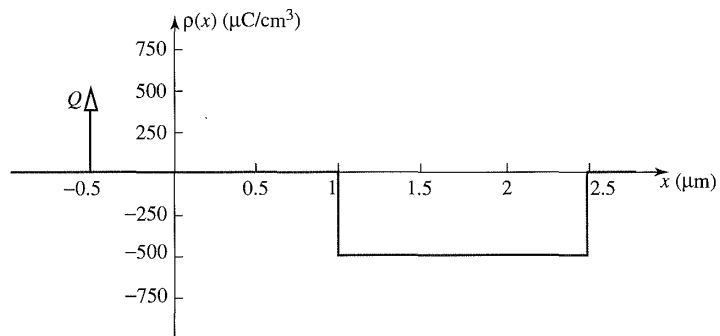
- For an applied voltage $V_{21} = 1$ V between the metal layers, plot the electric field $E(x)$ in the composite dielectric ($0 < x < 500$ Å).
- Plot the potential $\phi(x)$, with the bottom plate (metal 2) being considered the reference ($\phi(500 \text{ Å}) = 0$).
- What is the magnitude and sign of the sheet charge on the top plate (metal 2), for $V_{21} = 1$ V? A circuit approach to this part might be helpful.

P3.2 A region of silicon has the charge density shown in Fig. P3.2.

- What is the sheet charge Q [units: C/cm^2] needed to balance the negative charge density over the interval $1 \mu\text{m} < x < 2.5 \mu\text{m}$.
- Find the electric field at $x = 0.5 \mu\text{m}$.
- Find the potential at $x = 0$, given that $\phi(2.5 \mu\text{m}) = -0.4$ V.



► Figure P3.1



► Figure P3.2

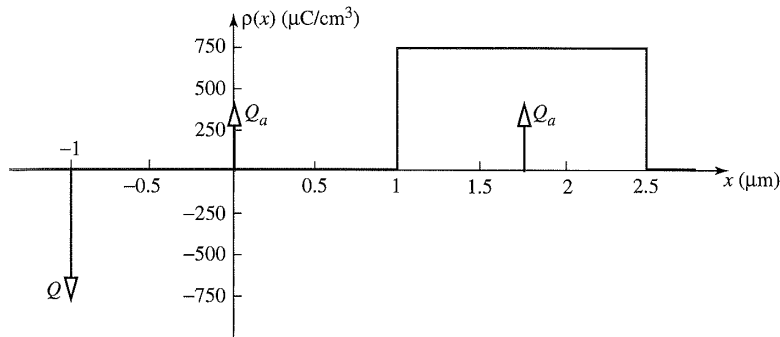
P3.3 A region of silicon has the charge density given in Fig. P3.3. The sheet charge $Q = -2.5 \times 10^{-7} \text{ C/cm}^2$.

- Find the sheet charges Q_a at $x = 0$ and $x = 1.75 \mu\text{m}$ needed to have the region of silicon be electrically neutral.
- Sketch the electric field $E(x)$ through the structure.
- Sketch the potential $\phi(x)$ given that $\phi(-1 \mu\text{m}) = 0$.

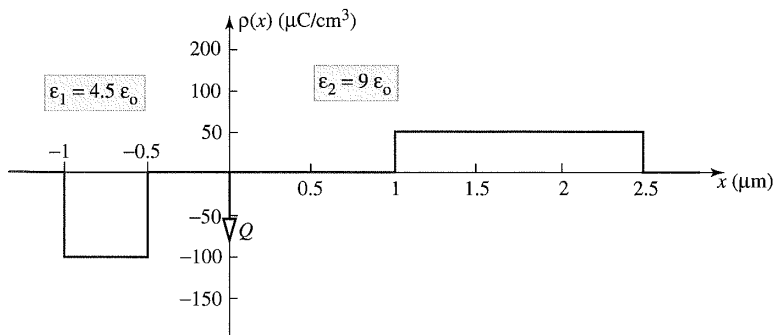
P3.4 In the aluminum-aluminum capacitor shown in cross section in Fig. P3.1, we now add a sheet charge $Q_I = 5 \times 10^{-10} \text{ C/cm}^2$ at the interface between the SiO_2 and Si_3N_4 at $x = 250 \text{ \AA}$.

- For $V_1 = V_2 = 0$, plot the electric field $E(x)$ through the dielectrics.
- Repeat part (a) for $V_1 = 1 \text{ V}$ and $V_2 = 0 \text{ V}$.
- Plot the potential $\phi(x)$ for part (b).

P3.5 In Fig. P3.5, there is a material interface at $x = 0$ at which a sheet charge is also located, with value $Q = -2.5 \text{ nC/cm}^2$.



► Figure P3.3



► Figure P3.5

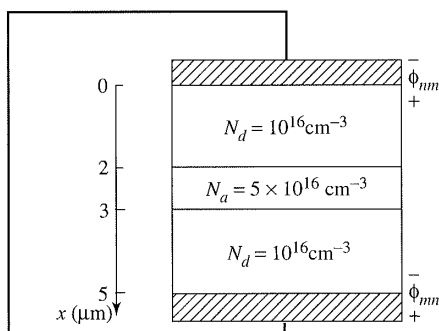
- (a) What is the relationship between $E(0^-)$ and $E(0^+)$?
 (b) Sketch the electric field through the structure.

P3.6 The silicon structure in Fig. P3.6 consists of two pn junctions that are separated by $1\ \mu\text{m}$. The n-type to metal contact potential $\phi_{nm} = 400\ \text{mV} = \phi_n - \phi_m = -\phi_{mn}$.

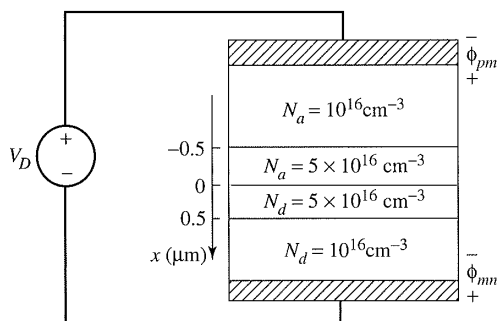
- (a) Find the depletion widths for each junction in thermal equilibrium.
 (b) Plot the electric field $E_o(x)$ through the structure in thermal equilibrium.
 (c) Plot the potential $\phi_o(x)$ in thermal equilibrium, including the contact potentials.

P3.7 The pn junction in Fig. P3.7 has a stepped doping concentration on each side of the metallurgical junction.

- (a) Find the depletion width X_{do} in thermal equilibrium.
 (b) If the n and p sides of the junction are each depleted by $1\ \mu\text{m}$, sketch the charge density, the electric field, and the potential.



► Figure P3.6



► Figure P3.7

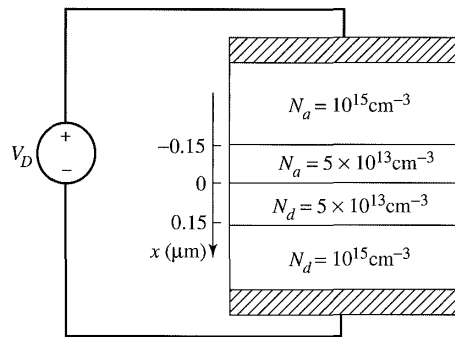
- (c) Find the applied voltage V_D (< 0 V) that corresponds to the depletion width in part (b).

P3.8 The pn junction diode in Fig. P3.8 has a stepped doping concentration.

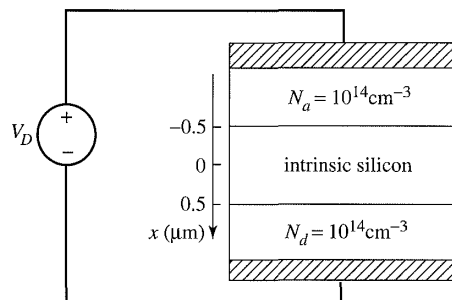
- (a) Find the depletion width X_{do} in thermal equilibrium.
 (b) If the n and p sides of the junction are depleted to ± 1.0 μm , sketch the charge density, the electric field, and the potential.
 (c) Find the applied voltage V_D (< 0 V) that corresponds to the depletion width in part (b).

P3.9 Figure P3.9 shows a p-i-n diode. The i stands for intrinsic silicon, which in practice means silicon that is compensated with $N_a = N_d$.

- (a) Sketch the charge density, electric field, and potential in thermal equilibrium.



► Figure P3.8



► Figure P3.9

- (b) For an applied bias $V_D = -3$ V, find the widths of the depletion regions in the p and the n silicon.

P3.10 The IC structure shown in cross section in Fig. P3.10 is part of a voltage-controlled resistor.

- (a) What is the thickness t of the undepleted n-type layer for $V_C = 0$. The distance between the metallurgical junctions between the n-type layer and the p^+ layers is $t_o = 1$ μm .
 (b) For what value of V_C does $t = 0$? This condition is called pinch-off.
 (c) Sketch the potential $\phi(x)$ at pinch-off.

P3.11 This problem continues the voltage-controlled resistor from Fig. P3.10.

- (a) Plot the sheet resistance of the n-type layer as a function of V_C .
 (b) Plot the junction capacitance per unit area ($\text{fF}/\mu\text{m}^2$) of the n-type layer as a function of V_C .

P3.12 Sketch the depletion capacitance of the pn junction in Fig. P3.8 as a function of the applied bias V_D . The capacitance at any breakpoints (where the slope of $C(V_D)$ changes) should be accurate.

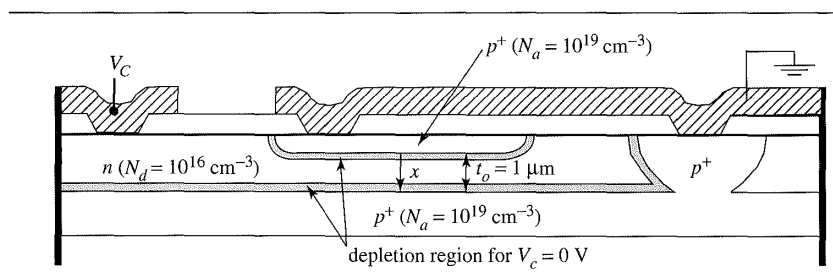
P3.13 Sketch the depletion capacitance of the pn junction in Fig. P3.9 as a function of the applied bias V_D . The capacitance at any breakpoints (where the slope of $C(V_D)$ changes) should be accurate.

P3.14 The analysis of the electrostatics of the pn junction remains valid for small forward biases $V_D < 250$ mV. What is the percentage increase in junction capacitance per unit area over that of thermal equilibrium is found for the voltage-controlled resistor in Fig. P3.10 if we use $V_C = -250$ mV?

P3.15 The fabrication process used to make the voltage-controlled resistor in Fig. P3.10 has the following normalized uncertainties for each junction depth x_j and each doping concentration N .

$$x_j = \bar{x}_j (1 \pm 0.02) \quad \text{and} \quad N = \bar{N} (1 \pm 0.04)$$

- (a) Find the uncertainty in the pinch-off voltage, assuming that all of the contributions are independent.
 (b) Find the uncertainty in the zero-bias junction capacitance per unit area.



► **Figure P3.10**

P3.16 Figure P3.16 is the cross section of an ion-implanted region. In this problem, we will develop a very simple model for the extra capacitance contributed by the edges (or sidewalls) of the region. The bottom of the region has area $W \times W$ and the edges are modeled as half-circles in cross section, with a radius equal to the junction depth x_j . The doping concentrations for the bottom and sidewalls are approximated by:

$$\text{bottom: } N_a = 10^{17} \text{ cm}^{-3}, N_d = 10^{16} \text{ cm}^{-3}$$

$$\text{sidewall: } N_a = 5 \times 10^{17} \text{ cm}^{-3}, N_d = 10^{17} \text{ cm}^{-3}$$

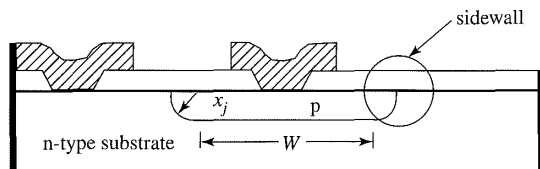
- Find the sidewall capacitance per unit edge length in thermal equilibrium by applying the one-dimensional depletion model to the semi-circular edge of the region. Use $x_j = 0.75 \mu\text{m}$.
- Plot the ratio of the sidewall capacitance to the total junction capacitance in thermal equilibrium, as a function of the lateral dimension W over the range $W = 2 \mu\text{m} - 100 \mu\text{m}$. Use $x_j = 0.75 \mu\text{m}$.

P3.17 Heavily boron-doped polysilicon (referred to as p^+ polysilicon) is sometimes used as a gate material. Its thermal equilibrium potential is $\phi_{p^+} = -550 \text{ mV}$. The gate oxide is $t_{ox} = 200 \text{ \AA}$ and the substrate doping is $N_a = 7.5 \times 10^{16} \text{ cm}^{-3}$ for this problem.

- Find the flatband voltage V_{FB} . What state is the capacitor in for the case of thermal equilibrium?
- Find the threshold voltage V_{Tn} .
- Sketch the charge density, electric field, and potential through the MOS capacitor in thermal equilibrium.
- Sketch the charge density, electric field, and potential through the MOS capacitor for $V_{GB} = V_{Tn}$.

P3.18 Using the p^+ polysilicon gate introduced in P3.17, we fabricate an MOS capacitor with a gate oxide is $t_{ox} = 250 \text{ \AA}$ and a substrate doping is $N_d = 5 \times 10^{16} \text{ cm}^{-3}$ of

- Find the flatband voltage V_{FB} . What state is the capacitor in for the case of thermal equilibrium?
- Find the threshold voltage V_{Tp} .
- Sketch the charge density, electric field, and potential through the MOS capacitor in thermal equilibrium.



► **Figure P3.16**

- (d) Sketch the charge density, electric field, and potential through the MOS capacitor for $V_{GB} = V_{Tp}$.

P3.19 A composite dielectric is sometimes useful in an MOS capacitor. For this problem, the gate insulator consists of 50 Å of oxide (on the substrate), over which is 450 Å of *vacuum*. The gate is n^+ polysilicon and the substrate is doped p-type with $N_a = 5 \times 10^{15} \text{ cm}^{-3}$.

- What is the threshold voltage?
- Sketch the electric field through the MOS capacitor for $V_{GB} = -2.5 \text{ V}$.
- Sketch the electric field through the MOS capacitor for $V_{GB} = +2.5 \text{ V}$.
- For $V_{GB} = 2.5 \text{ V}$, what is the change in the gate charge if the vacuum gap is reduced by 10%? A pressure transducer has been made using this principle.
- What is the electrostatic force f_E per unit area on the polysilicon gate for a gate-bulk bias $V_{GB} = 2.5 \text{ V}$? This effect must be accounted for in designing a pressure sensor.

P3.20 This problem considers the effect of fixed charge at the SiO_2 -silicon interface on the parameters of an MOS capacitor. For a MOS capacitor with n^+ polysilicon gate, $t_{ox} = 150 \text{ Å}$, and $N_a = 10^{17} \text{ cm}^{-3}$, we have $Q_F = +2.5 \times 10^{-8} \text{ C/cm}^2$ located at $x = 0$.

- Sketch the charge density in thermal equilibrium for this MOS capacitor. What is the shift in the flatband voltage V_{FB} due to the fixed charge?
- What is the shift in the threshold voltage V_{Tn} due to the fixed charge?
- Sketch normalized C - V curve with and without the fixed charge.

P3.21 This problem considers the effect of fixed charge at the SiO_2 -silicon interface on the parameters of an MOS capacitor. For a MOS capacitor with n^+ polysilicon gate, $t_{ox} = 150 \text{ Å}$, and $N_d = 10^{17} \text{ cm}^{-3}$, we have $Q_F = +2.5 \times 10^{-8} \text{ C/cm}^2$ located at $x = 0$.

- Sketch the charge density in thermal equilibrium for this MOS capacitor. What is the shift in the flatband voltage V_{FB} due to the fixed charge?
- What is the shift in the threshold voltage V_{Tp} due to the fixed charge?
- Sketch normalized C - V curve with and without the fixed charge.

P3.22 The control of the threshold voltage is critical for VLSI CMOS processes. In this problem, we explore the implications for the control of gate oxide thickness. We would like the threshold voltage to be $V_{Tn} = 500 \text{ mV} \pm 50 \text{ mV}$ in a particular process.

- Find the required average gate oxide thickness is $\bar{t}_{ox}$ in Å, given $N_a = 10^{17} \text{ cm}^{-3}$.
- Assuming that the substrate doping is $N_a = 10^{17} \text{ cm}^{-3}$ and is perfectly controlled, what is the allowable variation in the gate oxide thickness?
- Now consider that $N_a = 10^{17} \text{ cm}^{-3} \pm 2 \times 10^{15} \text{ cm}^{-3}$. How much does the substrate doping variation add to the variation in V_{Tn} ?

P3.23 Due to a processing error, the n^+ polysilicon gate of an MOS capacitor is merely n-type with a doping concentration $N_d = 10^{17} \text{ cm}^{-3}$. In this problem, assume you can treat the electrostatics of the n-type polycrystalline silicon gate exactly as you would treat n-type crystalline silicon. The gate oxide thickness is 200 Å and the substrate doping concentration is $N_a = 10^{17} \text{ cm}^{-3}$.

- What is the flatband voltage V_{FB} ?

(b) For $V_{GB} = 2\text{V}$, what is the width of the depletion region in the n-type gate polysilicon? Sketch the electric field and the potential.

(c) Sketch the normalized C - V curve for this capacitor.

P3.24 In this problem, the substrate is doped at $N_a = 5 \times 10^{16} \text{ cm}^{-3}$ for $0 < x < 500 \text{ \AA}$ and $N_a = 5 \times 10^{17} \text{ cm}^{-3}$ for $x > 500 \text{ \AA}$. The gate oxide is $250 \text{ \AA}$ thick and the gate is n^+ polysilicon.

(a) Sketch the charge density in thermal equilibrium.

(b) What is the flatband voltage V_{FB} ?

(c) What is the threshold voltage V_{Tn} ?

P3.25 Due to an error in implantation, the substrate doping for an MOS capacitor is $N_a = 10^{16} \text{ cm}^{-3}$ rather than $5 \times 10^{16} \text{ cm}^{-3}$. The gate oxide is $250 \text{ \AA}$ thick and the gate is n^+ polysilicon. We would like to remedy this error by doing another boron implant.

(a) What are the minimum dose and depth of the implant required to obtain the desired threshold voltage?

(b) Sketch the normalized C - V curve before and after the corrective implant.

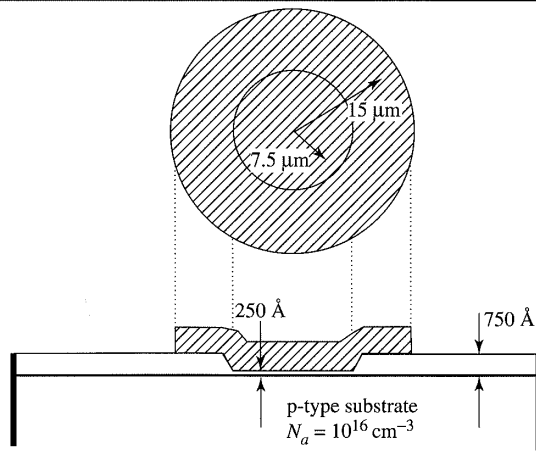
P3.26 Sketch the normalized C - V curve for the MOS capacitor with the stepped substrate doping in P3.24.

P3.27 The layout and cross section of a MOS structure is shown in Fig. P3.27.

(a) What are the threshold voltages of the thin oxide and thick oxide portions of this MOS capacitor?

(b) For $V_{GB} = 5 \text{ V}$, what is the ratio of the inversion layer charge stored on the thick-oxide to the thin-oxide portions?

(c) Sketch the capacitance (in fF) versus V_{GB} for this structure.



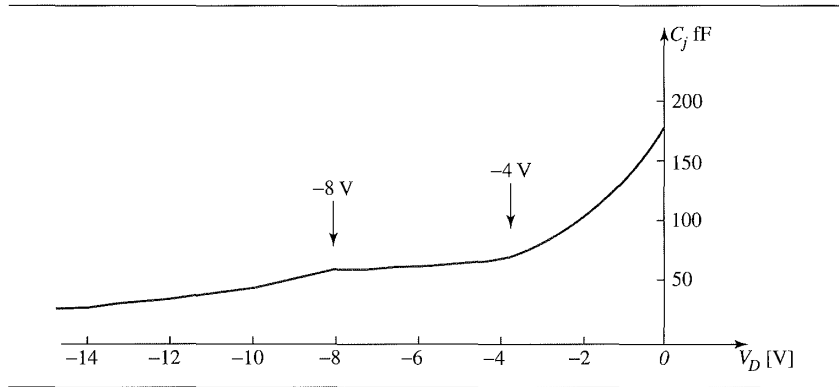
► Figure P3.27

DESIGN PROBLEMS

D3.1 The junction capacitance versus voltage curve is given below for a one-sided pn-junction. Determine the area and the (nonuniform) doping concentration that are required to have this capacitance curve. Note the breakpoints at $V_D = -4$ V and at $V_D = -8$ V.

D3.2 The requirement for a particular CMOS process is that the threshold voltage variation is $V_{Tn} = 0.7 \pm 0.1$ V. The oxide thickness is controlled to $t_{ox} = \bar{t}_{ox} (1 \pm 0.1)$ and the doping concentration is controlled to $N_a = \bar{N}_a (1 \pm 0.02)$. The possible range for the oxide thickness is limited to $100 \text{ \AA} \leq t_{ox} \leq 500 \text{ \AA}$ and the doping concentration is limited to $10^{15} \leq N_a \leq 10^{17} \text{ cm}^{-3}$.

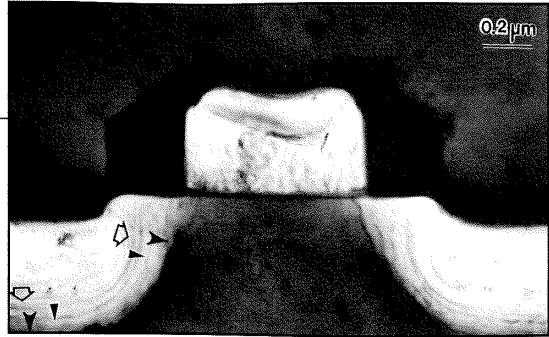
- Choose an average doping concentration and an average oxide thickness that yield $\bar{V}_{Tn} = 0.7$ V.
- Find the variation in the threshold voltage, given the uncertainties in the oxide thickness and the doping concentration. Iterate to find a solution for $\bar{t}_{ox}$ and $\bar{N}_a$ that satisfies the 100 mV variation in the threshold voltage.
- Rather than use the statistical model for the uncertainties, it is more conservative to use worst-case analysis in which the signs of the variations in t_{ox} and in N_a are chosen to largest magnitude shift in V_{Tn} . Repeat (b) using this approach and compare your answers with the statistical model.



► **Figure D3.1**

chapter 4

The MOS Field-Effect Transistor



Transmission electron micrograph (TEM) of a 0.6 μm channel length MOSFET. (Courtesy of Prof. R. Gronsky, Dept. of MSME, Univ. of California at Berkeley)

This chapter introduces our first multi-terminal microelectronic device—the MOS field-effect transistor (MOSFET). Your understanding of the MOS capacitor will be the foundation for seeing how MOSFETs work and developing more accurate models. MOSFETs are the dominant transistor type for digital ICs and also have important applications in analog signal processing circuits.

Chapter Objectives

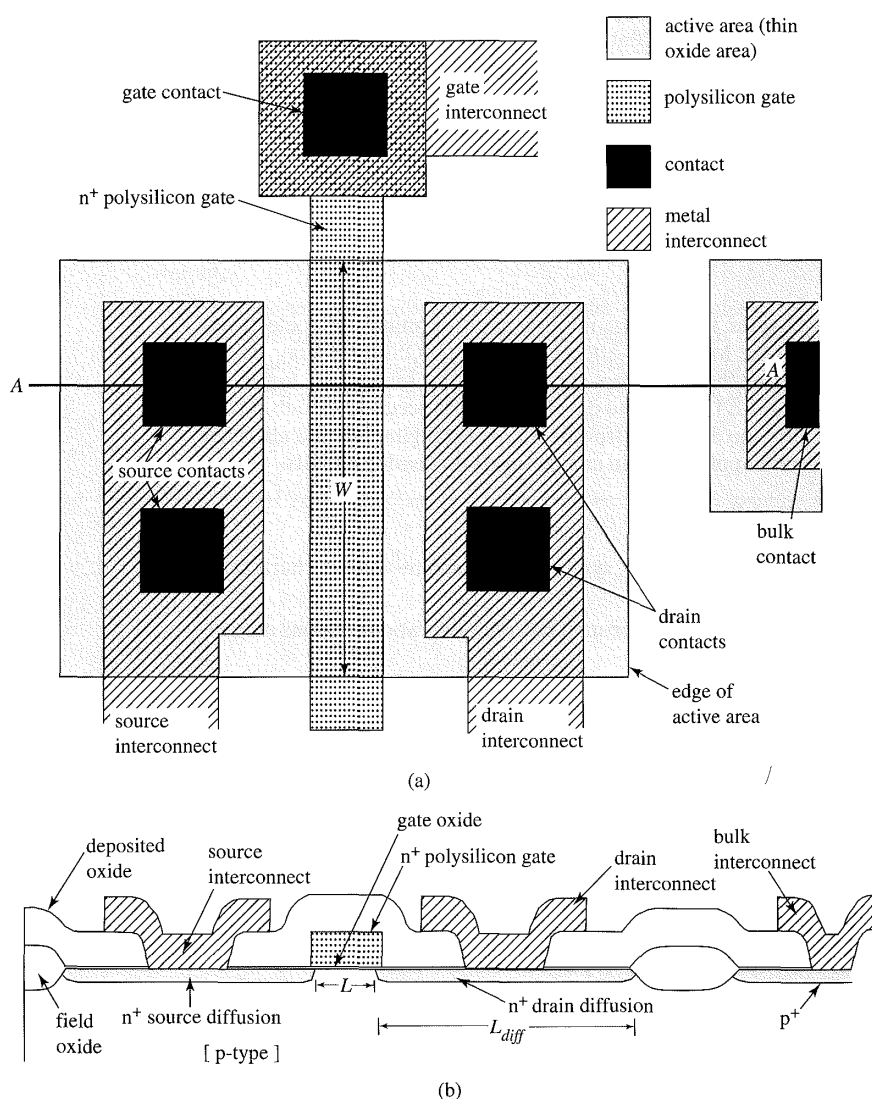
- ◆ MOSFET structures, symbols, and current-voltage characteristics.
- ◆ Cutoff, triode, and constant current (saturation) regions of operation.
- ◆ The gradual channel approximation and its use to model the current-voltage characteristics.
- ◆ Large- and small-signal models of n-channel and p-channel MOSFETs for circuit design.
- ◆ Level 1 SPICE model for the MOSFET.

► 4.1 INTRODUCTION

4.1.1 MOSFET Physical Structure

The **MOS field-effect transistor (MOSFET)** is the electronic device behind the explosive growth in digital electronics since 1970. The complexity and capability of MOS integrated circuits have increased many orders of magnitude over the past 25 years. To begin your study of this device, the layout and cross section of a

modern n-channel MOSFET is shown in Fig. 4.1. The basic structure is identical to that of the simple MOSFET whose fabrication process was described in detail in Chapter 2. The **gate** of the transistor is a film of n^+ polycrystalline silicon (polysilicon). Underlying the gate is the **gate oxide** which is a layer of thermally grown silicon dioxide (SiO_2).



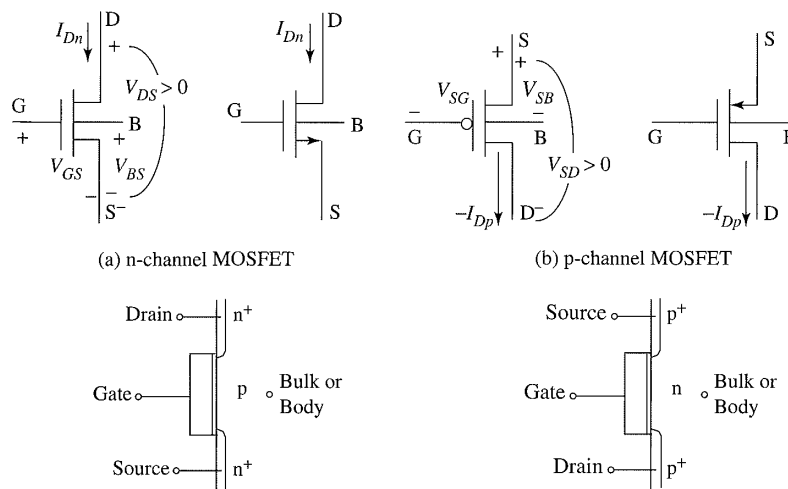
► **Figure 4.1** (a) Four-mask layout and (b) cross section of an integrated n-channel MOSFET.

The **channel** is formed under the polysilicon gate between the two n^+ regions as shown in Fig. 4.1 (b). The **channel length L** of the MOSFET as is defined in Fig. 4.1 (b) as the gap between the n^+ diffusions. On the layout in Fig. 4.1(a), the **channel width W** of the MOSFET is defined as the width of the active area. One n^+ diffusion is called the **source**, the other is called the **drain**. The potentials on the diffusions will be the basis for differentiating the source from the drain, as discussed in the next section. The source and drain diffusions have a length L_{diff} and the same width W as the channel. Metal interconnections make ohmic contacts to the gate, source, and drain. In addition, the underlying p-type bulk region (the substrate or a deep p-type diffusion) is contacted with a fourth metal interconnection called the **bulk** or **body**.

MOSFET Circuit Symbol and 4.1.2 Terminal Characteristics

Before introducing the current-voltage characteristics of the MOSFET, it is helpful to have a symbol for this device. Unfortunately, there are two common symbols for each MOSFET type. Figure 4.2 shows the circuit symbols and basic structure for an **n-channel MOSFET** (shown in Fig. 4.1) and for the complementary **p-channel MOSFET** that has p^+ source and drain diffusions in an n-type bulk region. In this text we will use the symbols without arrows for digital circuits and the symbols with arrows for analog circuits. The cross sections for the two MOSFETs have been rotated 90° in order to illustrate the close correspondence between the symbols and the physical structure.

The MOSFETs are oriented as they often appear in circuit schematics: the drain for the n-channel MOSFET and the source for the p-channel MOSFET are on top—toward the positive voltage supply. Voltages between terminals are labeled by an ordered pair of subscripts such as $V_{GS} = V_G - V_S$. By IEEE convention, the reference



► **Figure 4.2** (a) n-channel MOSFET symbols and structure and (b) p-channel symbols and structure.

directions for currents are defined as positive *into* the device terminals. Since the drain current for the p-channel device is negative, it is convenient to use $-I_{DP} > 0$, which is positive leaving the drain terminal. For the n-channel MOSFET in Fig. 4.2(a), the drain and source terminals are selected so that $V_{DS} > 0$, which is equivalent to defining the source as the one with the *lower* potential. As shown in Fig. 4.2(b), the labeling convention is opposite for the p-channel MOSFET. Its source and drain are identified so that $V_{SD} > 0$, which means its source is defined as the one with the *higher* potential.

The n-channel MOSFET's static (DC) terminal characteristics can be measured with voltage sources and ammeters. Since the MOSFET is a four terminal device, we need to experiment and discover which voltages are most important. For our initial investigation, we short the bulk to the source to set $V_{BS} = 0$ V. Since the voltage *differences* between the drain and source and gate and source are most important, we ground the source ($V_S = 0$ V) for convenience. Since the gate terminal is insulated, the only current of interest is that into the drain terminal I_{Dn} .

Figure 4.3(a) is a schematic of the circuit used to find the drain current's functional dependence on the two voltages under our control: the gate-source voltage V_{GS} and the drain-source voltage V_{DS} . The conventional way to graph the measured data is to plot a family of curves $I_{Dn}(V_{GS}, V_{DS})$, with V_{GS} as a parameter. The drain current versus drain-source voltage curves for a selected set of gate-source voltages are called the MOSFET **drain characteristics**.

Figure 4.3(b) shows measured drain characteristics for an n-channel MOSFET in a digital CMOS process. Although the voltage and current ranges can vary with the technology and device layout, the ranges in Fig. 4.3(b) are typical. In this graph, the drain current I_D is measured as a function of drain-source voltage V_{DS} for eight gate-source voltages

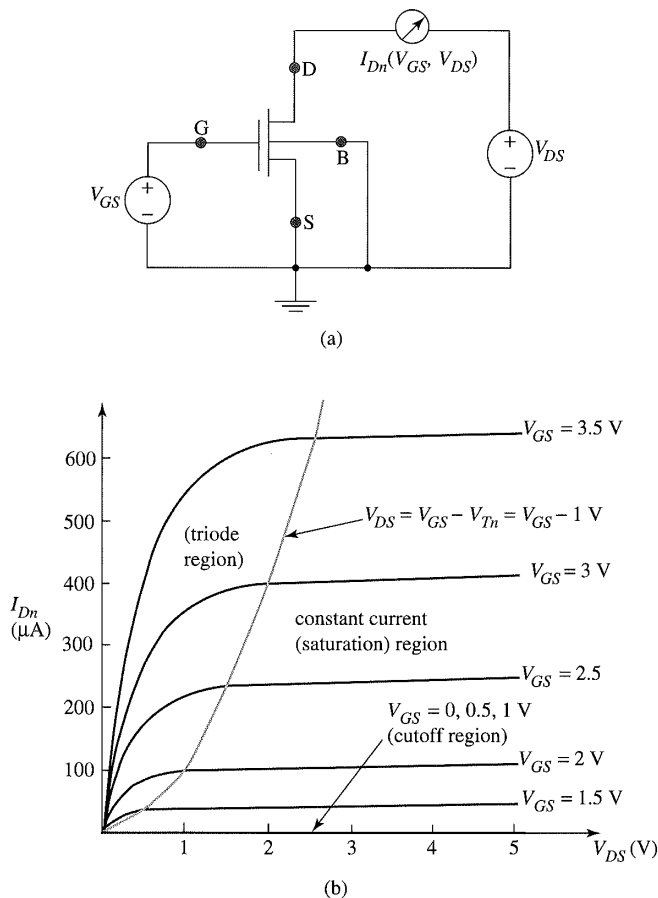
$$I_{Dn}(V_{GS} = 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 \text{ V}, V_{DS}), \text{ for } 0 \text{ V} < V_{DS} < 5 \text{ V} \quad (4.1)$$

Several observations can be made from studying the drain characteristics in Fig. 4.3(b).

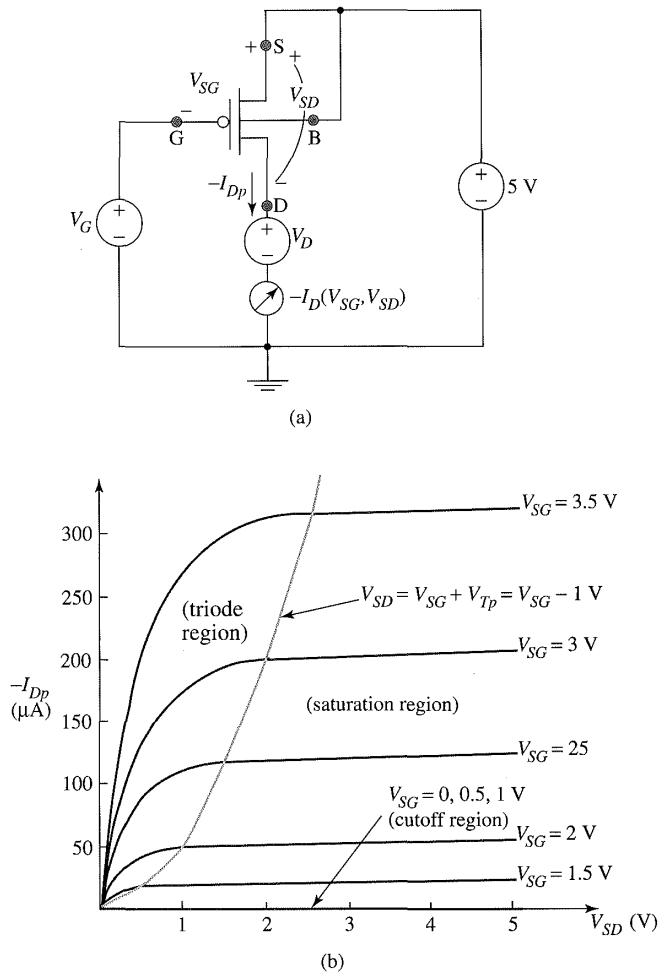
1. The MOSFET is **cutoff** ($I_{Dn} = 0$ A) for gate-source voltages that are less than some critical voltage, which is defined as the **threshold voltage** V_{Tn} of the n-channel device. A typical value for the n-channel threshold voltage is $V_{Tn} = 1$ V. The n^+ source and drain are electrically isolated until sufficient voltage is applied to the gate to create an n-type inversion layer or **channel** between them.
2. The drain current is nearly independent of the drain-source voltage once $V_{DS} > V_{GS} - V_{Tn}$. In this region of operation, called **saturation**, the MOSFET behaves like a current source. Further study reveals that the drain current in saturation is proportional to the square of the gate-source voltage above threshold $(V_{GS} - V_{Tn})^2$. This can be seen from the ratios of drain current for $V_{GS} = 3$ V and for $V_{GS} = 2$ V. This constant-current behavior will be exploited in both analog and digital circuit design.
3. The region where I_{Dn} depends on both V_{GS} and V_{DS} is termed the **triode** region.

The p-channel MOSFET's drain characteristics are shown in Fig. 4.4. In this case, the source and n-type bulk terminals are both connected to a 5 V supply. The effect of varying the drain voltage and gate voltage on the drain current can be investigated. The shape of the drain characteristics are identical to those of the n-channel MOSFET

if $-I_{Dp}$ (which is positive) is plotted against the source-drain drop $V_{SD} = 5\text{ V} - V_D$ as a function of the source-gate voltage $V_{SG} = 5\text{ V} - V_G$. The drain current is zero unless the source-gate voltage $V_{SG} > -V_{Tp}$, where V_{Tp} is the p-channel threshold voltage. A typical value for the p-channel threshold voltage is $V_{Tp} = -1\text{ V}$.



► **Figure 4.3** n-channel MOSFET drain characteristics: (a) test circuit and (b) measurements of drain current as function of drain-source voltage, with gate-source voltage as a parameter for a typical integrated device.

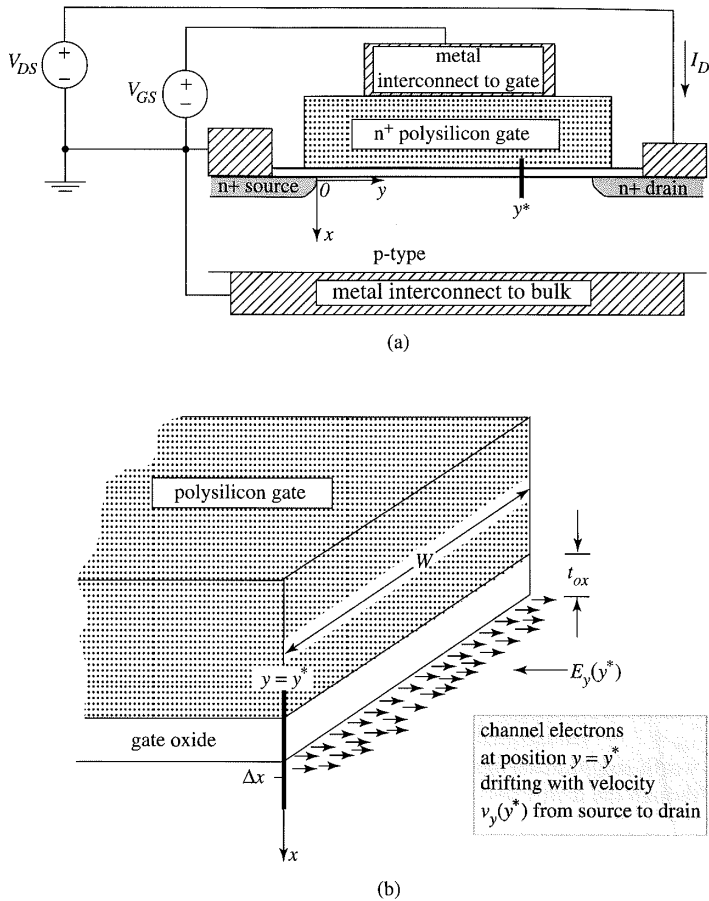


► **Figure 4.4** (a) Test circuit and (b) measured drain characteristics of a p-channel MOSFET with the same geometric dimensions as the n-channel device used for Fig. 4.3. The negative of the drain current $-I_{Dp}$ (> 0) is plotted against the source-drain drop V_{SD} , with the source-gate drop V_{SG} as a parameter. The drain current for the p-channel is about half that of the n-channel device for identical geometries and complementary threshold voltages $V_{Tp} = -V_{Tn} = -1$ V.

► 4.2

DEVICE PHYSICS OF THE MOSFET: DRAIN CURRENT AND CHANNEL CHARGE

We are now prepared to quantify how the drain current varies with the terminal voltages for the n-channel MOSFET. As a starting point, we will build upon the electrostatics of the MOS capacitor that were discussed in Chapter 3. Once the channel forms, an inversion layer of electrons exists between source and drain. An applied



► **Figure 4.5** (a) MOSFET biased with $V_{GS} > V_{Tn}$ and $V_{DS} > 0$. (b) Cutaway view of drifting electrons in the channel at position y^* (see (a)) between the source ($y = 0$) and drain ($y = L$).

voltage between the drain and source will impose an electric field across the channel that results in a drift current density. A good first step is to relate this drift current density, which is the origin of the drain current I_D , to the charge in the inversion layer.

Figure 4.5(a) illustrates an n-channel MOSFET with applied voltages $V_{GS} > V_{Tn}$ and $V_{DS} > 0$. For simplicity, we again short the bulk to the source so $V_{BS} = 0$. Furthermore, we assume that a channel extends from the source to the drain. The drain current I_D consists of electrons drifting from source to drain along the channel. At any point along the channel, the electron drift current must equal the drain current I_D since there is no current to the substrate or through the insulating oxide to the gate.

Figure 4.5(b) shows a perspective view of a portion of the channel at position y^* between the source and drain. From basic semiconductor physics, the drift current density J_y at any point (x, y) in the channel is given by

$$J_y = -qn(x, y)v_y(y) \quad (4.2)$$

where $n(x, y)$ is the electron concentration (cm^{-3}) in the channel and $v_y(y)$ is the drift velocity. The channel is a very thin region under the gate oxide—there are negligible electrons for $x > \Delta x \approx 50 \text{ \AA} = 0.005 \text{ \mu m}$. The drain current I_D is equal to the integral of the drift current density J_y over the cross section of the channel in Fig. 4.5(b), which has an area of $W\Delta x$. Adding a negative sign to account for the fact that the reference direction for I_D in Fig. 4.4(a) is opposite to the positive direction of the y coordinate, we find

$$I_D = -W \int_0^{\Delta x} J_y(x, y) dx = Wv_y(y) \left(\int_0^{\Delta x} qn(x, y) dx \right) \quad (4.3)$$

where we have used the fact that v_y is not a function of the position x in the thin channel. The integral in Eq. (4.3) is the negative of the electron charge $Q_N(y)$ (units: C/cm^2) in the channel at point y between source and drain, since

$$Q_N(y) = - \int_0^{\Delta x} qn(x, y) dx \quad (4.4)$$

As we will investigate shortly, the electron charge will vary along the channel between the source and drain. Substituting Eq. (4.4) into Eq. (4.3), we relate the drain current to the channel charge

drain current = product
of channel charge,
width, and drift velocity

$$I_D = -Wv_y(y)Q_N(y) \quad (4.5)$$

It is worth emphasizing again that the drain current does *not* vary from source to drain, although the drift velocity $v_y(y)$ and channel electron charge $Q_N(y)$ generally do.

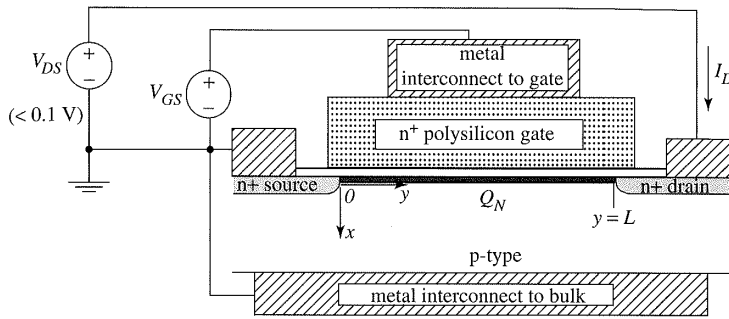
The drain current equation in Eq. (4.5) has been derived from basic physics. Next, we must determine how the channel electron charge and drift velocity vary with position in the channel in order to proceed toward finding the functional dependence of drain current on V_{GS} and V_{DS} . Since the full analysis is rather involved, we will make a “first pass” to gain an understanding of the important features of MOSFET operation.

► 4.3 MOSFET DEVICE PHYSICS: A FIRST PASS

From Chapter 3, we have a quantitative result for the inversion charge under a MOS capacitor

$$Q_N = -C_{ox}(V_{GB} - V_{Tn}) \quad (4.6)$$

In order to apply this one-dimensional result to the two-dimensional channel of a MOSFET, first consider the special case where the drain-source voltage V_{DS} is very small—on the order of $100 \text{ mV} = 0.1 \text{ V}$ or less. As shown in Fig. 4.6, the channel is uniform from source to drain for small drain-source biases. Note that for $V_{DS} = 0 \text{ V}$,



► **Figure 4.6** MOSFET biased with $V_{GS} > V_{Tn}$ and very small V_{DS} , so the channel can be assumed to be uniform from source to drain. The channel thickness is greatly exaggerated in order to be visible.

the structure degenerates to a capacitor and Eq. (4.6) is an *exact* expression for the channel charge.

Substituting Eq. (4.6) into the drain current expression from the previous section and noting from Fig. 4.6 that $V_{GB} = V_{GS}$, we find

$$I_D = -Wv_y Q_N = Wv_y C_{ox} (V_{GS} - V_{Tn}), \text{ where } V_{GS} > V_{Tn} \text{ and } V_{DS} < 0.1 \text{ V} \quad (4.7)$$

The remaining unknown in Eq. (4.7) is the drift velocity in the channel $v_y(y)$. Since the channel is nearly uniform, the voltage in the channel must vary linearly from source to drain with a constant electric field in the channel

$$E_y = -\left(\frac{V_{DS}}{L}\right) \quad (4.8)$$

Given the small V_{DS} , the channel electric field is also small in magnitude, making it a good approximation that the drift velocity is proportional to the electric field

$$v_y = -\mu_n E_y = -\mu_n (-V_{DS}/L) = \mu_n (V_{DS}/L) \quad (4.9)$$

Substitution of Eq. (4.9) into (4.7) results in an equation for the drain current in terms of V_{GS} and V_{DS} , for the special case of $V_{DS} < 0.1 \text{ V}$:

$$I_D = \left(\frac{W}{L}\right) \mu_n C_{ox} (V_{GS} - V_{Tn}) V_{DS} \text{ where } V_{GS} > V_{Tn} \text{ and } V_{DS} < 0.1 \text{ V} \quad (4.10)$$

For a fixed gate-source bias and small drain-source bias, Eq. (4.10) indicates that the MOSFET behaves like a voltage-controlled resistor, with resistance given by

$$R = \frac{V_{DS}}{I_D} = \left(\frac{1}{\mu_n C_{ox} (V_{GS} - V_T)} \right) \left(\frac{L}{W} \right) = [R_{\square} (V_{GS})] \left(\frac{L}{W} \right). \quad (4.11)$$

In order to model the MOSFET for $V_{DS} > 0.1 \text{ V}$ without solving differential equations, first approximate Eq. (4.5) by taking the averages of the channel charge and drift velocity over the channel

$$I_D \approx -W_y \overline{Q_N} \quad (4.12)$$

Since we do not know the functional dependence of Q_N , we estimate it as the mean of the channel charge at the source and drain ends of the channel. On the source side, the channel is adjacent to an n^+ diffusion that is connected to the p-type bulk region so $V_{GS} = V_{GB}$. The n^+ source diffusion supplies electrons to the inversion layer as soon as the surface inverts. Therefore, the channel charge stored on the source side of the circuit is

$$Q_N(y=0) = -C_{ox} (V_{GS} - V_{Tn}) \quad \text{where } V_{GS} > V_{Tn} \quad (4.13)$$

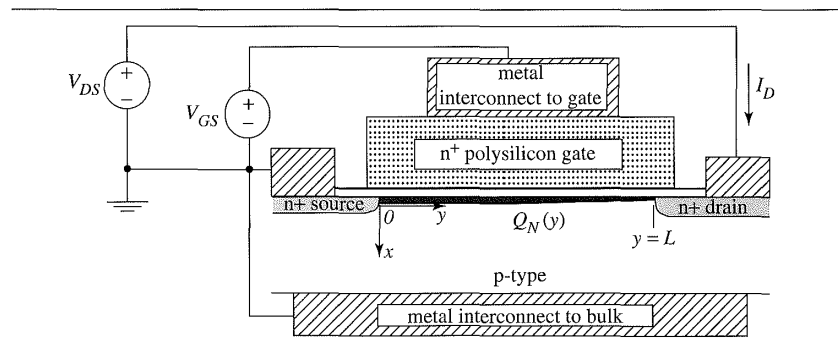
On the drain side of the circuit, the results from the MOS capacitor must be modified since the voltage of the n^+ diffusion adjacent to the drain end of the channel is V_{DS} and the electrostatics of the problem are changed. What is the effect of the higher potential at the drain end? The elevated drain potential lowers the voltage drop from the gate to the channel at the drain end and *reduces* the channel charge. This phenomenon can be approximated by using the gate-drain voltage drop $V_{GD} = V_{GS} - V_{DS}$ rather than the gate-source voltage drop in Eq. (4.13). The channel charge at the drain end is

$$Q_N(y=L) = -C_{ox} (V_{GD} - V_{Tn}), \quad \text{where } V_{GD} = V_{GS} - V_{DS} > V_{Tn} \quad (4.14)$$

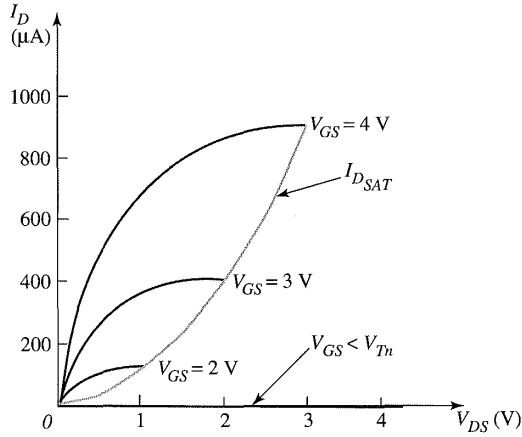
The conditions on V_{GS} and V_{DS} in Eq. (4.14) ensure that the channel charge is greater than zero at the drain end. The reduced charge at the drain end of the channel is shown qualitatively in Fig. 4.7. An estimate of the average channel charge from its values at the ends of the channel is

$$\overline{Q_N} \approx \frac{Q_N(y=0) + Q_N(y=L)}{2} = \frac{-C_{ox} (V_{GS} - V_{Tn}) - C_{ox} (V_{GS} - V_{DS} - V_{Tn})}{2} \quad (4.15)$$

Now that the channel charge varies from source to drain, it is no longer true that the channel voltage will increase linearly along the channel, or equivalently, that the



► **Figure 4.7** MOSFET biased in the triode region with $V_{GS} - V_{DS} > V_{Tn}$. The channel charge decreases from source to drain. The thickness of the channel is greatly exaggerated.



► **Figure 4.8** Drain characteristics for $V_{DS} \leq V_{GS} - V_{Tn}$, according to Eq. (4.17), assuming $V_{Tn} = 1$ V, $\mu_n C_{ox} = 50 \mu\text{A/V}^2$, and $(W/L) = 4$.

channel electric field is constant. However, in the spirit of this approximate analysis, we will estimate the average electric field by

$$\bar{E}_y = -\left(\frac{dV_C}{dy}\right) \approx \frac{-V_{DS}}{L} \quad (4.16)$$

where $V_C(y)$ is the channel voltage at position y between source and drain. The average drift velocity is then $\bar{v}_y = -\mu_n \bar{E}_y = \mu_n V_{DS}/L$. Substituting the estimates of average channel charge from Eq. (4.15) and average drift velocity into Eq. (4.12), we find

$$I_D = \left(\frac{W}{L}\right) \mu_n C_{ox} [V_{GS} - V_{Tn} - (V_{DS}/2)] V_{DS} \quad \text{where } V_{GS} - V_{DS} > V_{Tn} \quad (4.17)$$

As a check, Eq. (4.17) reduces to Eq. (4.10) for small V_{DS} . Figure 4.8 is a plot of Eq. (4.17) for three values of gate-source voltage. The curves have the general shape of the measured MOSFET drain characteristics in the triode region from Fig. 4.3. The inverted parabolas reach their maxima when the drain-source voltage is equal to $V_{DS_{SAT}}$, which is defined by

$$V_{DS_{SAT}} = V_{GS} - V_{Tn} \quad (4.18)$$

This voltage is also the largest drain-source voltage for which Eq. (4.17) is valid. The maximum drain current, called the **saturation current** $I_{D_{SAT}}$, is found by substituting $V_{DS_{SAT}}$ into Eq. (4.17)

$$I_{D_{SAT}} = \left(\frac{W}{2L}\right) \mu_n C_{ox} (V_{GS} - V_{Tn})^2 = \left(\frac{W}{2L}\right) \mu_n C_{ox} V_{DS_{SAT}}^2 \quad (4.19)$$

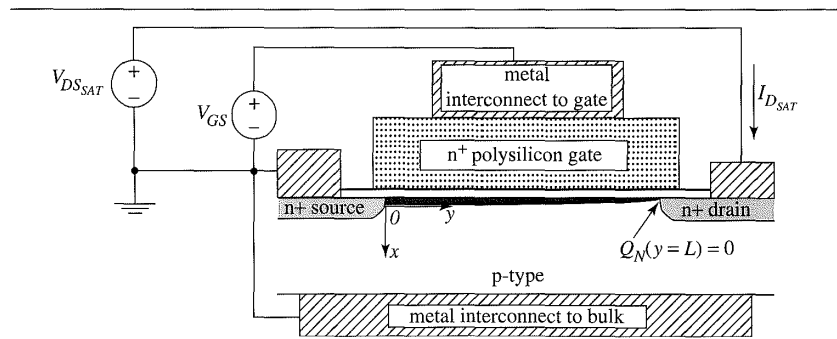
From the measured drain characteristics in Fig. 4.3, we know the drain current remains nearly constant at $I_{D_{SAT}}$ when the drain-source voltage increases above the saturation voltage $V_{DS} > V_{D_{SAT}}$. How can this fact be explained? The behavior of the channel charge at the drain end with increasing V_{DS} is an important clue. For the case where $V_{DS} = V_{D_{SAT}} = V_{GS} - V_{Tn}$, the channel charge vanishes at the drain end

$$Q_N(y=L)|_{V_{D_{SAT}}} = -C_{ox}(V_{GD} - V_{Tn}) = -C_{ox}(V_{GS} - V_{D_{SAT}} - V_{Tn}) = 0 \quad (4.20)$$

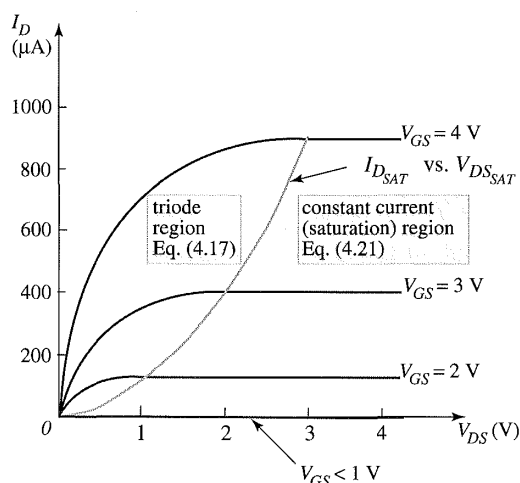
In Fig. 4.9, the channel charge in a MOSFET biased with $V_{DS} = V_{GS} - V_{Tn}$ is shown qualitatively. How can $Q_N(y=L) = 0$ and the drain current not also vanish? The answer is contained in Eq. (4.5)—the drain current is proportional to the product of the channel charge and drift velocity. For the drain current to remain constant in saturation, the drift velocity must become infinite at the drain end. In reality, the channel charge becomes very small and the drift velocity reaches its limiting value. Further increases in the drain-source voltage essentially have no effect on the channel charge at the drain end $Q_N(y=L)$ since it has already been reduced to nearly zero. As a result, the drain current remains constant, to first order, at its maximum value

$$I_D = I_{D_{SAT}} = \left(\frac{W}{2L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn})^2 \text{ for } V_{DS} \geq V_{D_{SAT}} \quad (4.21)$$

The very simple models constructed in this section for the triode region (Eq. (4.17)) and the saturation region (Eq. (4.21)) reproduce the essential features of the MOSFET drain characteristics as shown in Fig. 4.10. After some minor refinements in Section 4.6, we will find their simplicity makes them very useful for hand analysis and design of digital and analog circuits.



► **Figure 4.9** MOSFET biased with $V_{DS} = V_{D_{SAT}} = V_{GS} - V_{Tn}$ with the channel charge vanishing at the drain end. As in Figs. 4.6 and 4.7, the thickness of the channel is greatly exaggerated in order to be visible.

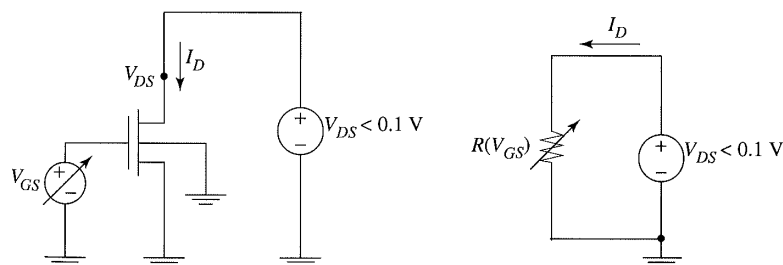


► **Figure 4.10** MOSFET drain characteristics generated from Eq. (4.17) for the triode region and Eq. (4.21) for the saturation region. Device parameters are the same as for Fig. 4.8.

► **EXAMPLE 4.1** MOSFET as a Voltage Controlled Resistor

The circuit below shows an n-channel MOSFET that is used as a voltage-controlled resistor. A MOSFET in this configuration is found in circuits such as variable gain amplifiers.

(a) Find the sheet resistance of the MOSFET over the range $V_{GS} = 1.5$ V to $V_{GS} = 4$ V using $\mu_n = 215 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $C_{ox} = 2.3 \text{ fF}/\mu\text{m}^2$ and $V_{Th} = 1$ V.



► **Figure Ex4.1A** An n-channel MOSFET used as a voltage controlled resistor.

SOLUTION

Note that for a gate-source voltage $V_{GS} > V_{Tn} + 0.1 \text{ V} = 1.1 \text{ V}$, the MOSFET will be operating in the **triode** region. Since the drain-source voltage is small, Eq. (4.17) reduces to Eq. (4.10)

$$I_D = \left(\frac{W}{L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn}) V_{DS} = \frac{1}{R} V_{DS}$$

For a particular value of V_{GS} , I_D is a *linear* function of V_{DS} and the circuit model for the MOSFET is a resistor as shown in the figure. Now we relate R to the sheet resistance.

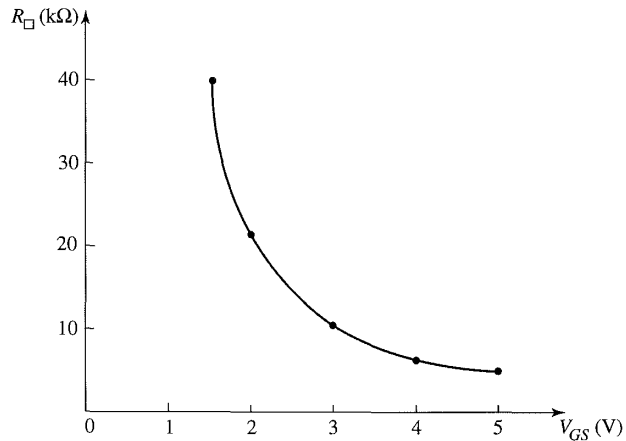
$$R = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{Tn})} = \frac{1}{\mu_n C_{ox} (V_{GS} - V_{Tn})} \left(\frac{L}{W} \right) = R_{\square} (L/W)$$

$R_{\square}$ as a function of V_{GS} is

$$R_{\square} = \frac{1}{(215 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}) (2.3 \times 10^{-7} \text{ F/cm}^2) (V_{GS} - 1 \text{ V})} = \frac{20 \text{ k}\Omega \cdot \text{V}}{(V_{GS} - 1 \text{ V})}$$

The plot of $R_{\square}$ as a function of V_{GS} is shown below

(b) For a particular application, we need to control the resistor between 200Ω and $1 \text{ k}\Omega$ for $V_{GS} = 1.5 \text{ V}$ to 4 V . How wide should the MOSFET be if the channel length $L = 1.5 \mu\text{m}$?



► **Figure Ex4.1B** Plot of sheet resistance vs. V_{GS} for a n-channel MOSFET operating with very small V_{DS} .

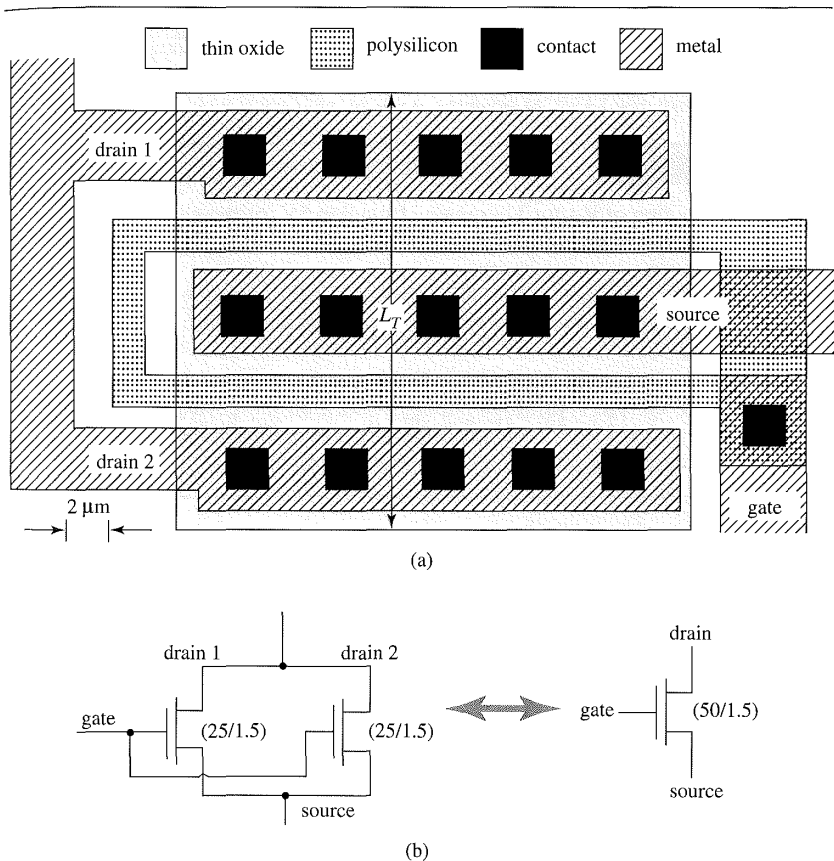
SOLUTION

We already solved for the sheet resistance in part (a), so we can find the range of sheet resistances for $V_{GS} = 1.5 \text{ V}$ to 4 V

$$R_{\square\min} = \frac{20 \text{ k}\Omega \cdot \text{V}}{(4 \text{ V} - 1 \text{ V})} = 6666.7 \Omega \text{ and } R_{\square\max} = \frac{20 \text{ k}\Omega \cdot \text{V}}{(1.5 \text{ V} - 1 \text{ V})} = 40 \text{ k}\Omega$$

Solving for (W/L) to obtain $R_{\min} = 200 \Omega$ and $R_{\max} = 1 \text{ k}\Omega$ yields

$$\left(\frac{W}{L}\right)_{\min} = \frac{6666.7 \Omega}{200 \Omega} = 33.3 \text{ and } \left(\frac{W}{L}\right)_{\max} = \frac{40000 \Omega}{1000 \Omega} = 40$$



► **Figure Ex4.1C** (a) Layout of folded n-channel MOSFET with $L=1.5\mu\text{m}$ and $W=50 \mu\text{m}$ and (b) schematic showing the equivalence of the two MOSFETs with $W=25 \mu\text{m}$ in parallel with a single MOSFET having $L=50 \mu\text{m}$

$(W/L) = 33.3$ will satisfy the requirements for both R_{min} and R_{max} so the width of the MOSFET should be

$$W = 1.5\mu\text{m} (33.3) = 50\mu\text{m}$$

(c) Design the layout for this MOS resistor so it occupies a minimum area. The length of the source/drain diffusions is $L_{diff} = 6\mu\text{m}$ with contacts that are $2\mu\text{m} \times 2\mu\text{m}$.

SOLUTION

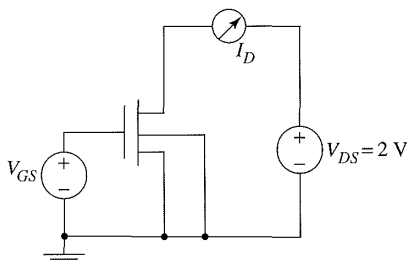
Given the high ratio of width to length, it is desirable to fold the MOSFET, which is equivalent to putting two MOSFETs of half the width in parallel. Since the diffusions are $6\mu\text{m}$ long, the total length is $L_T = 3 L_{diff} + 2 L = 3 \times 6\mu\text{m} + 2 \times 1.5\mu\text{m} = 21\mu\text{m}$, which is nearly equal to half the width $W/2 = 25\mu\text{m}$. The layout, drawn to scale, and the equivalent circuit are shown in Fig. Ex 4.1C.

► EXAMPLE 4.2 MOSFET operating regions

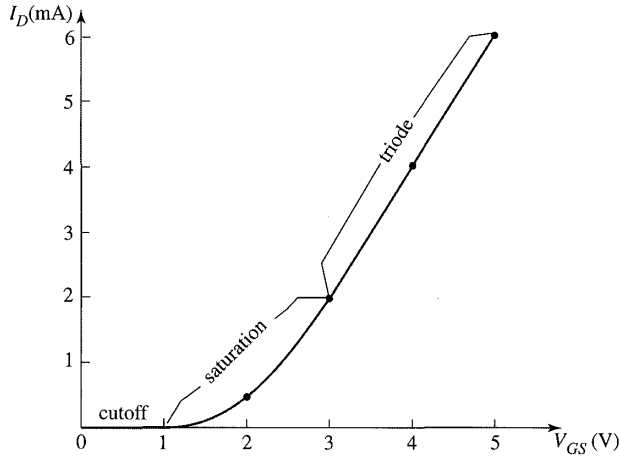
Plot I_D as a function of V_{GS} for V_{GS} ranging from 0 to 5V for the n-channel MOSFET shown in the circuit below with $\mu_n = 215\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $t_{ox} = 150\text{ \AA}$, $V_{Tn} = 1\text{ V}$, $L = 1.5\mu\text{m}$, and $W = 30\mu\text{m}$.

SOLUTION

For $V_{GS} < 1\text{ V} = V_{Tn}$, the MOSFET is in the *cutoff* region and I_D is zero. Once the gate-source voltage is just high enough to turn on the device, the drain-source voltage $V_{DS} = 2\text{ V} > V_{GS} - 1$ and the MOSFET is operating in the *saturation* region. The drain current in saturation is given by Eq. (4.21)



► Figure Ex4.2A n-channel MOSFET circuit.



► **Figure Ex4.2B** Plot of the I_D vs. V_{GS} for a n-channel MOSFET with fixed V_{DS} at 2 V.

$$I_D = \left(\frac{20}{2} \right) \left(50 \frac{\mu A}{V^2} \right) (V_{GS} - 1 V)^2 = 500 \frac{\mu A}{V^2} (V_{GS} - 1 V)^2$$

Once the gate-source voltage is high enough so $V_{GS} - V_{Th} = V_{GS} - 1 V = V_{DS} = 2 V$, the MOSFET operates in the *triode* region with Eq. (4.17) describing the drain current

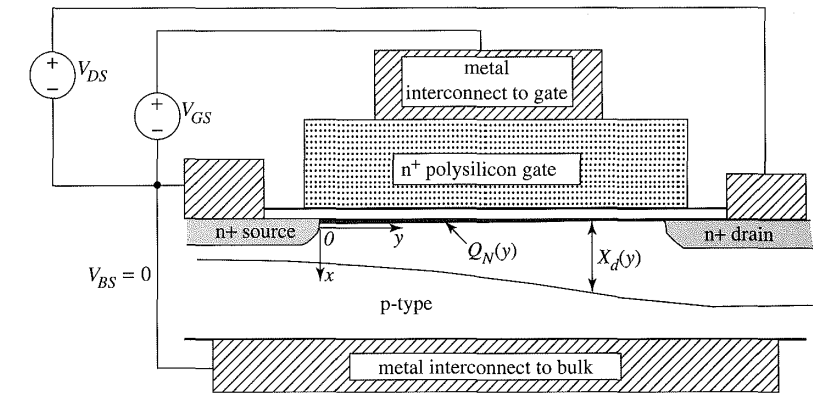
$$I_D = (20) \left(50 \frac{\mu A}{V^2} \right) \left(V_{GS} - 1 V - \frac{V_{DS}}{2} \right) V_{DS} = 2 \frac{mA}{V^2} (V_{GS} - 2 V) \text{ for } V_{GS} \geq 3 V$$

► 4.4 MOSFET DEVICE PHYSICS: THE GRADUAL CHANNEL APPROXIMATION

The starting point for developing a physical model for the current-voltage characteristics of the n-channel MOSFET is Eq. (4.5), which is repeated here.

$$I_D = -Wv_y(y)Q_N(y) \quad (4.22)$$

Our first step will be to find the functional dependence of the channel electron charge $Q_N(y)$ on the position y between the source and drain. Fig. 4.11 shows the cross section of a MOSFET that has bias voltages V_{GS} and V_{DS} . The bulk terminal is shorted to the source to make $V_{BS} = 0$ to simplify the initial analysis. Later in this section we will consider the case where the bulk is biased at a voltage different from the source.



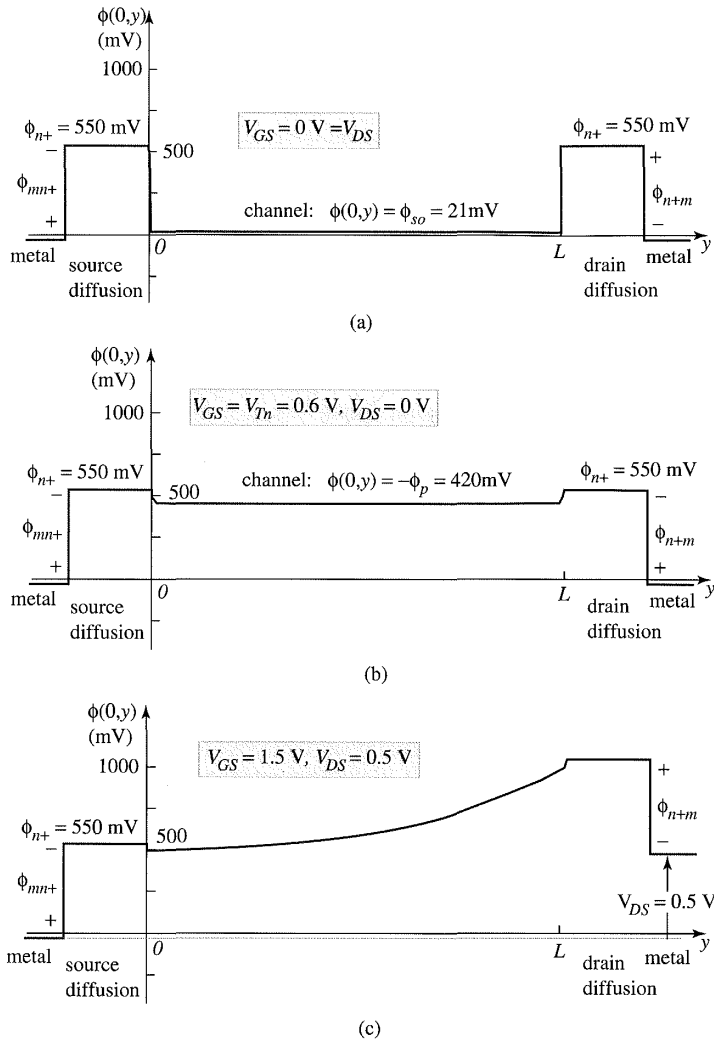
► **Figure 4.11** Cross section of n-channel MOSFET operating in the triode region with the applied voltages satisfying $V_{GS} > V_{Tn}$ and $V_{DS} < V_{GS} - V_{Tn}$. The depletion width increases and the channel charge decreases in magnitude from source to drain.

The coordinate system in Fig. 4.11 has its origin at the intersection of the boundary of the n⁺ source diffusion with the oxide/silicon interface. In Chapter 3 we saw that the surface potential $\phi_s = \phi(0, y)$ is important in calculating the charge in the bulk depletion region and the charge in the inversion layer (the channel electron charge). Starting with thermal equilibrium, Fig. 4.12(a) plots the surface potential from source to drain. The example structure has a substrate doping of $N_a = 10^{17} \text{ cm}^{-3}$ and an oxide thickness $t_{ox} = 150 \text{ \AA}$. The potential reference is the internal reference for silicon with intrinsic silicon being defined as zero. Note that the metal source and drain interconnections have the same potential since $V_{DS} = 0$ for equilibrium. The surface potential $\phi(0, y) = 21 \text{ mV}$ as calculated in Ex. 3.8, which corresponds to the surface being very slightly n-type. When a gate-source voltage is applied that is equal to the threshold voltage $V_{GS} = V_{Tn} = 0.6 \text{ V}$ and we maintain $V_{DS} = 0$, the surface potential increases to $\phi(0, y) = -\phi_p = 420 \text{ mV}$ as plotted in Fig. 4.12(b). The surface is inverted and an n-type channel has formed between the source and drain. Further increasing the gate-source voltage to $V_{GS} = V_{Tn} + 0.9 \text{ V} = 1.5 \text{ V}$ and then applying a drain-source voltage of $V_{DS} = 0.5 \text{ V}$, the sketch in Fig. 4.12(c) shows that the potential $\phi(0, y)$ increases by V_{DS} from the source to the drain. The metal contact to the n⁺ source has been kept fixed in Fig. 4.12(c).

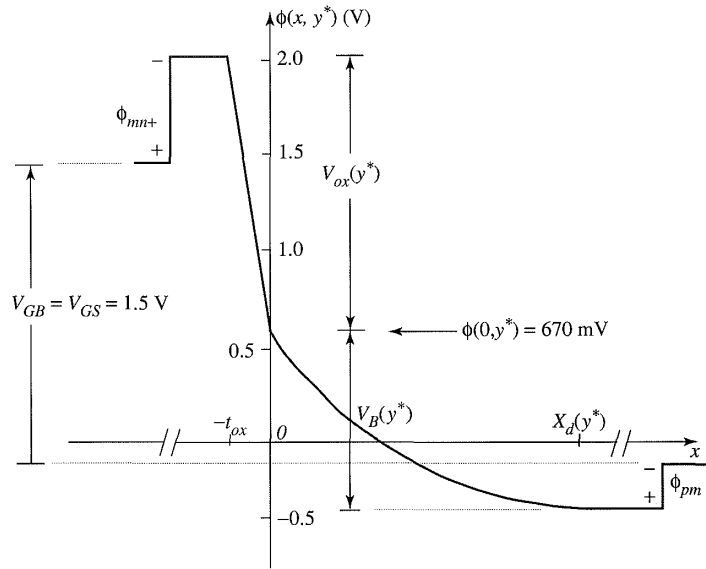
In Fig. 4.12(b), note that the potential in the channel is slightly lower than that of the n⁺ source and drain regions when the gate is biased at the onset of inversion. For higher gate biases, the surface potential increases somewhat and reaches a maximum value of $\phi_{n+} = 550 \text{ mV}$, an effect that is ignored in the delta-depletion approximation. In fact, the potential jump at the source becomes negligible for normal gate biases.

We now consider the potential variation perpendicular to the channel (in the x direction in Fig. 4.11). In order to use the one-dimensional analysis from Chapter 3, we assume the lateral electric field (in the y direction) caused by V_{DS} is much smaller in magnitude than the vertical electric field caused by V_{GS} . Overall, this assumption is plausible since the gate oxide thickness ($150 \text{ \AA}$) is much smaller than the channel length (on the order of $1 \text{ }\mu\text{m}$ or longer), while the drain and gate voltages are each on

gradual channel
approximation



► **Figure 4.12** Surface potential along the channel of a MOSFET with the substrate doping concentration $N_a = 10^{17} \text{ cm}^{-3}$ and oxide thickness $t_{ox} = 150 \text{ \AA}$. (a) Thermal equilibrium, (b) gate biased at the threshold voltage with no drain-source bias, and (c) gate bias increased to well above threshold $V_{GS} = 1.5 \text{ V}$ with a drain-source bias $V_{DS} = 0.5 \text{ V}$ that places the MOSFET in the triode region.



► **Figure 4.13** Potential $\phi(x, y^*)$, where the potential at point $y = y^*$ is 250 mV above its potential at the onset of inversion. The MOSFET is biased at the operating point used for Fig. 4.12(c).

the order of a few volts. This standard approach to MOSFET modeling is known as the **gradual channel approximation**.

Applying the one-dimensional results from Chapter 3, we equate the vertical potential drop through the MOSFET at any position in the channel to the sum of the drop across the oxide and the drop across the depletion region. In Fig. 4.13, we plot the potential as a function of x for a point y^* in the channel of a MOSFET biased with $V_{GS} = V_{GB} = 1.5$ V and $V_{DS} = 0.5$ V. In order to plot numerical values, we choose y^* so

$$\phi(0, y^*) = -\phi_p + 250 \text{ mV} = 670 \text{ mV} \quad (4.23)$$

At a general point y in the channel, we can equate

$$V_{GB} - V_{FB} = V_{GS} - V_{FB} = V_{ox}(y) + V_B(y) \quad (4.24)$$

since $V_{GB} = V_{GS}$ from Fig. 4.10. The drop across the depletion region is

$$V_B(y) = \phi(0, y) - \phi_p \quad (4.25)$$

At the source end of the channel ($y = 0$), the drop across the depletion region is

$$V_B(0) = \phi(0, 0) - \phi_p = -2\phi_p \quad (4.26)$$

which is the familiar result for an MOS capacitor from Chapter 3. As shown in Fig. 4.12(c), the applied drain-source bias does not affect the potential at the source end of the channel.

Since we need to find the variation of the channel electron charge $Q_N(y)$, we apply Gauss's Law to relate the oxide field to the charge in the silicon

$$V_{ox}(y) = E_{ox}(y)t_{ox} = \left(\frac{t_{ox}}{\epsilon_{ox}}\right)(-Q_N(y) - Q_B(y)) = \frac{-Q_N(y) - Q_B(y)}{C_{ox}} \quad (4.27)$$

Substituting for $V_{ox}(y)$ from Eq. (4.24), we can solve for $Q_N(y)$

$$Q_N(y) = -C_{ox}\left(V_{ox}(y) + \frac{Q_B(y)}{C_{ox}}\right) = -C_{ox}\left(V_{GS} - V_{FB} - V_B(y) + \frac{Q_B(y)}{C_{ox}}\right) \quad (4.28)$$

The drop across the depletion region is known in terms of the surface potential from Eq. (4.25), which leads to

$$Q_N(y) = -C_{ox}\left(V_{GS} - V_{FB} - \phi(0, y) + \phi_p + \frac{Q_B(y)}{C_{ox}}\right) \quad (4.29)$$

This result can be compacted by defining the threshold voltage $V_{Tn}(y)$ to account for the variation in the bulk charge $Q_B(y)$ along the channel

$$V_{Tn}(y) = V_{FB} - 2\phi_p - \frac{Q_B(y)}{C_{ox}} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_a (\phi(0, y) - \phi_p)} \quad (4.30)$$

in which we substitute from Eq. (4.25) for the drop across the depletion region. Note from Eq. (4.30) and Fig. 4.12(c) that the threshold at the drain end is higher than at the source end of the channel because of the larger depletion charge resulting from $V_B(L) > V_B(0) = -2\phi_p$. This varying of threshold voltage along the channel is referred to as the **body effect**. Substituting Eq. (4.30) into Eq. (4.29), we find

$$Q_N(y) = -C_{ox}(V_{GS} - V_{Tn}(y) - \phi(0, y) - \phi_p) \quad (4.31)$$

Another convenient variable is the **channel voltage** $V_C(y)$, which is defined as

$$V_C(y) = \phi(0, y) + \phi_p \quad (4.32)$$

and is the component of the surface potential in the channel due to the drain-source voltage. Note from Fig. 4.12(c) that $V_C(0) = 0$ at the source end and $V_C(L) = V_{DS}$ at the drain end. Substituting for $V_C(y)$ into Eq. (4.31), the electron charge in the channel at point y is given by

$$Q_N(y) = -C_{ox}(V_{GS} - V_{Tn}(y) - V_C(y)) \quad (4.33)$$

in which the threshold voltage in terms of $V_C(y)$ is found by substituting into Eq. (4.30)

$$V_{Tn}(y) = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_a (V_C(y) - 2\phi_p)} \quad (4.34)$$

Having expressed the electron charge in terms of the channel voltage in Eqs. (4.33) and (4.34), we now turn to the drift velocity term in Eq. (4.22). Assuming that the drift velocity is proportional to the electric field component along the channel E_y ,

$$v_y(y) = -\mu_n E_y(y) = \mu_n \frac{dV_C(y)}{dy} \quad (4.35)$$

Note that this assumption will be invalid for high electric fields, due to velocity saturation. The channel electron mobility in Eq. (4.35) is around one-third the bulk electron mobility from Fig. 2.8 due to excess scattering off the gate oxide in the thin channel. Substituting for the drift velocity and channel electron charge in Eq. (4.22), we find a differential equation in the channel voltage

$$I_D = -WQ_N(y)v_y(y) = WC_{ox} [V_{GS} - V_{Tn}(y) - V_C(y)] \mu_n \frac{dV_C(y)}{dy} \quad (4.36)$$

This equation can be integrated along the channel by separation of variables to eliminate V_C , resulting in an analytical expression for drain current as a function of V_{GS} and V_{DS} in the triode region. The final expression for $I_D(V_{GS}, V_{DS})$ is too complicated to be useful for hand design or analysis. Note that the square-root term in $V_{Tn}(y)$ leads to three-halves powers of the terminal voltages.

To find a simpler expression for the drain current, we neglect the complication of a varying threshold voltage along the channel. We can see the nature of this approximation by first evaluating Eq. (4.34) at the source end of the channel, which is defined as the MOSFET threshold voltage V_{Tn}

n-channel MOSFET
threshold voltage

$$V_{Tn} = V_{Tn}(0) = V_{FB} - 2\phi_p + \frac{\sqrt{2q\epsilon_s N_a (-2\phi_p)}}{C_{ox}} \quad (4.37)$$

Substituting V_{Tn} into Eq. (4.30), the threshold voltage variation $V_{Tn}(y)$ due to the body effect is

$$V_{Tn}(y) = V_{Tn} + \frac{-Q_B(y) + Q_B(0)}{C_{ox}} = V_{Tn} + \frac{qN_a}{C_{ox}} (X_d(y) - X_d(0)) \quad (4.38)$$

Neglecting the body effect, we approximate $V_{Tn}(y) \approx V_{Tn}$ along the channel. The error in Eq. (4.38) due to body effect is small near the source and only depends on the square root of the channel voltage. This implies that we can model the essential features of the channel charge $Q_N(y)$ by approximating Eq. (4.33) with

$$Q_N(y) \approx -C_{ox} (V_{GS} - V_{Tn} - V_C(y)) \quad (4.39)$$

The differential equation for drain current Eq. (4.36) simplifies to

$$I_D = WC_{ox} (V_{GS} - V_{Tn} - V_C(y)) \mu_n \frac{dV_C(y)}{dy} \quad (4.40)$$

We can eliminate the channel voltage by separating variables and integrating

$$\int_0^L I_D dy = \int_0^{V_{DS}} W \mu_n C_{ox} (V_{GS} - V_{Tn} - V_C(y)) dV_C \quad (4.41)$$

which leads to a closed-form expression for the drain current

$$I_D = \left(\frac{W}{L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn} - V_{DS}/2) V_{DS} \quad (4.42)$$

Surprisingly, this expression is identical to Eq. (4.17) that we derived using very crude approximations for the drift velocity and channel electron charge. As mentioned in the previous section, this equation for drain current is valid in the triode region when the inversion layer extends from source to drain. This implies from Eq. (4.39) that

$$V_{GS} \geq V_{Tn} + V_C(L) = V_{Tn} + V_{DS} \quad (4.43)$$

or equivalently, that $V_{DS} \leq V_{GS} - V_{Tn}$

4.4.1 Backgate Effect

In some circuit configurations, the bulk terminal of the MOSFET is biased at a voltage V_{BS} with respect to the source, thereby making it a four-terminal device. The voltage V_{BS} in Fig. 4.14 is called the **backgate bias** since the bulk potential affects the electron charge in the channel and functions as a second gate. Since the source and drain form pn diodes with the bulk terminal, the voltage V_{BS} is negative (V_{SB} positive) in order to ensure that these diodes are reverse biased.

The effect of the backgate bias is to shift the potential of the substrate lower, thereby increasing the potential drop across the depletion region as shown in Fig. 4.15. The MOSFET is under the same gate-source and drain-source bias ($V_{GS} = 1.5$ V and $V_{DS} = 0.5$ V) and the potential is plotted where $\phi(0, y^*) = 670$ mV as in Fig. 4.13.

From Fig. 4.15, the potential drop across the depletion region at a general point y between the source and drain is increased by the backgate bias to

$$V_B(y) = \phi(0, y) - (\phi_p + V_{BS}) = V_C(y) - 2\phi_p - V_{BS} \quad (4.44)$$

in which we substituted the definition of the channel voltage from Eq. (4.32). The larger $V_B(y)$ increases the bulk charge $Q_B(y)$, resulting in a larger threshold voltage. At the source end of the channel, the channel voltage is zero and $V_B(0) = -2\phi_p - V_{BS}$. Substitution of the increased drop at the source end of the channel into Eq. (4.37) yields the dependence of the MOSFET threshold on the backgate bias

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{(2qN_a\epsilon_s) (-2\phi_p - V_{BS})} \quad (4.45)$$

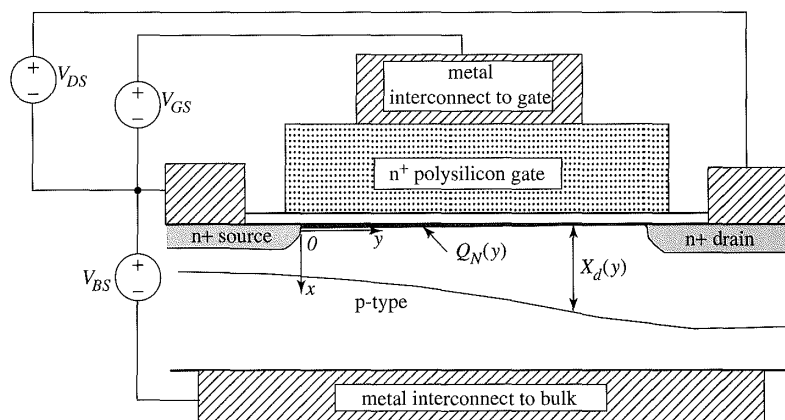
Note that both ϕ_p and V_{BS} are negative numbers. The conventional form for Eq. (4.45) is

$$V_{Tn} = V_{TOn} + \gamma_n (\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p}) \quad (4.46)$$

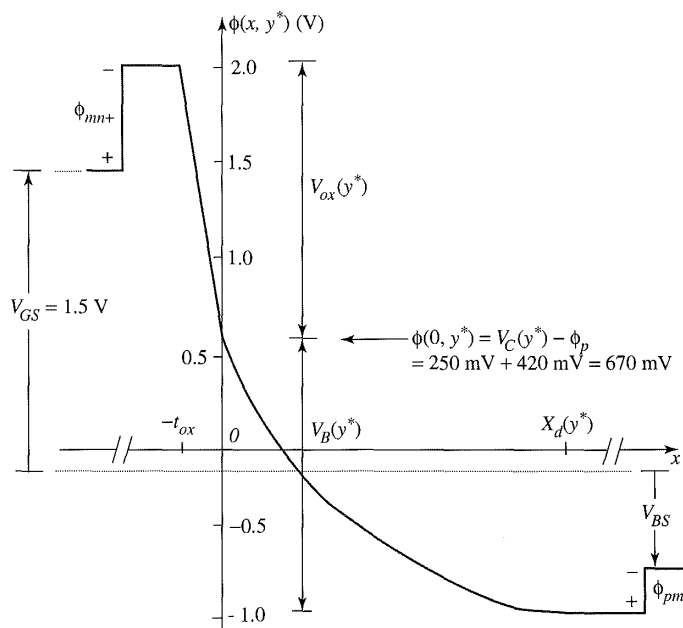
where the n-channel MOSFET **backgate effect parameter** is defined as

$$\gamma_n = (\sqrt{2qN_a\epsilon_s}) / C_{ox} \quad (4.47)$$

n-channel MOSFET
threshold voltage with
backgate bias



► **Figure 4.14** n-channel MOSFET with backgate bias $V_{BS} < 0$. The depletion region has widened in comparison with Fig. 4.11 due to the larger potential drop across it.



► **Figure 4.15** Potential variation in x direction through the MOSFET at y^* where the channel voltage is $V_C(y^*) = 250$ mV. The bias voltages are $V_{GS} = 1.5$ V, $V_{DS} = 0.5$ V, and $V_{BS} = -0.5$ V.

and V_{TO_n} is the threshold voltage without backgate effect (Eq. (4.37)). Therefore, the drain current is a function of the backgate bias through its effect on V_{Tn} . In Chapters 8 and 9 we will see that the backgate bias can have significant consequences for circuit design with MOSFETs.

n-channel backgate
effect parameter

► EXAMPLE 4.3 Measuring the Backgate Effect Parameter

The test circuit from Example 4.1 can be modified to find an experimental value for the backgate parameter, γ_n . Note that a negative voltage V_{BS} is applied from the bulk to the source of the MOSFET. The circuit varies V_{GS} continuously from 0 to 5V, for $V_{BS} = 0$ and $V_{BS} = -5$ V. The drain-source voltage is $V_{DS} = 100$ mV.

(a) From the drain current measurements plotted below, find the backgate effect parameter. Assume that the device parameters are the same as in Example 4.1 with the substrate doping $N_a = 10^{17} \text{ cm}^{-3}$.

SOLUTION

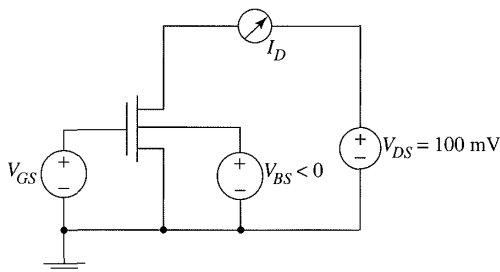
Since the drain voltage is only 100 mV, the MOSFET operates in its triode region once V_{GS} exceeds the threshold voltage. The drain current I_D is given by Eq. (4.42)

$$I_D = \left(\frac{W}{L} \right) \mu_n C_{ox} [V_{GS} - V_{Tn}(V_{BS}) - V_{DS}/2] V_{DS}$$

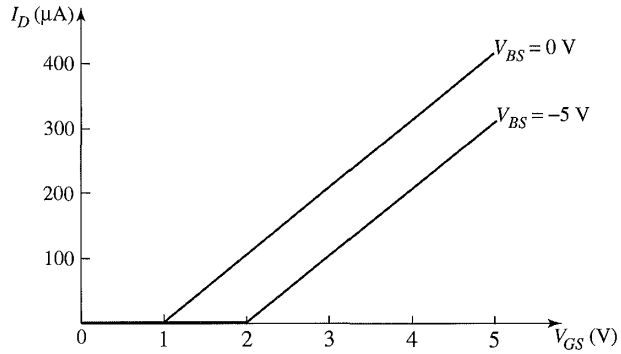
where the functional dependence of the threshold voltage on the backgate bias is indicated explicitly. The triode equation can be approximated with little error by neglecting $V_{DS}/2 = 50$ mV in the parentheses

$$I_D \cong \left(\frac{W}{L} \right) \mu_n C_{ox} [V_{GS} - V_{Tn}(V_{BS})] V_{DS}$$

This equation is linear in V_{GS} , with $V_{Tn}(V_{BS})$ as the intercept. From the graph, we can see $V_{TO_n} = 1.0$ V and for $V_{BS} = -5$ V, $V_{Tn} = 2$ V.



► Figure Ex.4.3A Circuit to find the backgate effect parameter.



► **Figure Ex4.3B** Experimental data for circuit in Example 4.3

Applying Eq. (4.46) with $\phi_p = -0.42$ V, we can extract the backgate effect parameter

$$2 \text{ V} = 1 \text{ V} + \gamma_n (\sqrt{(0.84 \text{ V} + 5 \text{ V})} - \sqrt{0.84 \text{ V}}) \rightarrow \gamma_n = 0.67 \text{ V}^{1/2}$$

4.4.2 The MOSFET in Saturation

We will now consider the device physics of the MOSFET in saturation where the drain-source voltage increases up to and beyond the point where the channel charge vanishes at the drain end of the channel, according to our simple one-dimensional analysis. The variation of channel voltage $V_C(y)$ from source to drain can be derived from Eqs. (4.40) and provides insight into this phenomenon. By integrating Eq. (4.40) to a point y along the channel, we find that the channel voltage is given by

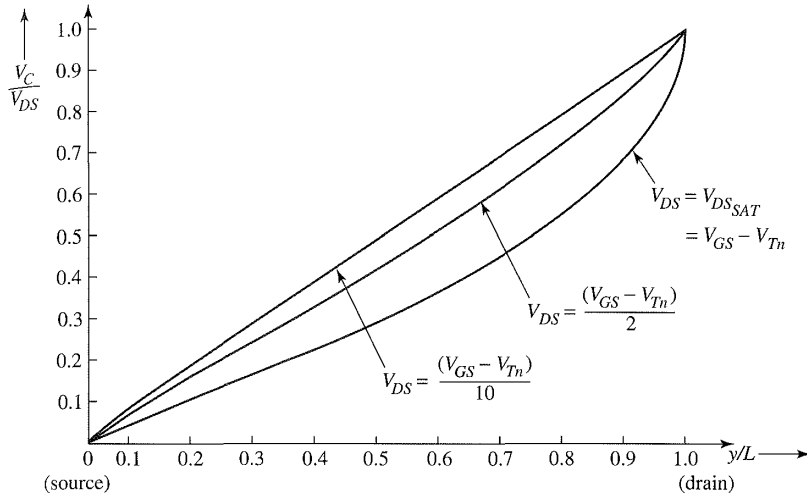
$$\int_0^y \frac{I_D}{\mu_n W C_{ox}} dy = \int_0^{V_C} (V_{GS} - V_{Tn} - V_C) dV_C = (V_{GS} - V_{Tn}) V_C - V_C^2/2 \quad (4.48)$$

After integrating the left hand side (remembering that I_D is constant along the channel), a quadratic equation yields the channel voltage

$$V_C(y) = V_{GS} - V_{Tn} - \sqrt{(V_{GS} - V_{Tn})^2 - 2(V_{GS} - V_{Tn} - V_{DS}/2)V_{DS}(y/L)} \quad (4.49)$$

where we have substituted Eq. (4.42) for the drain current.

Figure 4.16 is a plot of the channel voltage, normalized to V_{DS} , from source to drain for three values of V_{DS} . For the smallest drain-source voltage, one-tenth of $V_{GS} - V_{Tn}$, the channel voltage increases nearly linearly from source to drain. With V_{DS} equal to one-half of $V_{GS} - V_{Tn}$, more of the channel voltage is dropped near the drain end. Finally, for the saturation drain voltage, $V_{DS_{SAT}} = V_{GS} - V_{Tn}$, most of the



► **Figure 4.16** Normalized channel voltage $V_C(y)/V_{DS}$ along the channel for three values of drain-source voltage.

voltage drop occurs at the drain end with the channel voltage becoming vertical at the drain.

The channel electric field E_y is the negative derivative of $V_C(y)$:

$$E_y(y) = -\frac{dV_C}{dy} = \frac{-(V_{GS} - V_{Tn} - V_{DS}/2) V_{DS}}{L \sqrt{(V_{GS} - V_{Tn})^2 - 2(V_{GS} - V_{Tn} - V_{DS}/2) V_{DS}}} \quad (4.50)$$

which becomes infinite at the drain ($y = L$) when $V_{DS} = V_{DS_SAT} = V_{GS} - V_{Tn}$. However, an infinite electric field is not reasonable and we must reexamine the assumptions underlying the gradual channel approximation. The reason why E_y blows up at the drain is seen from the basic equation for drain current, evaluated at $y = L$

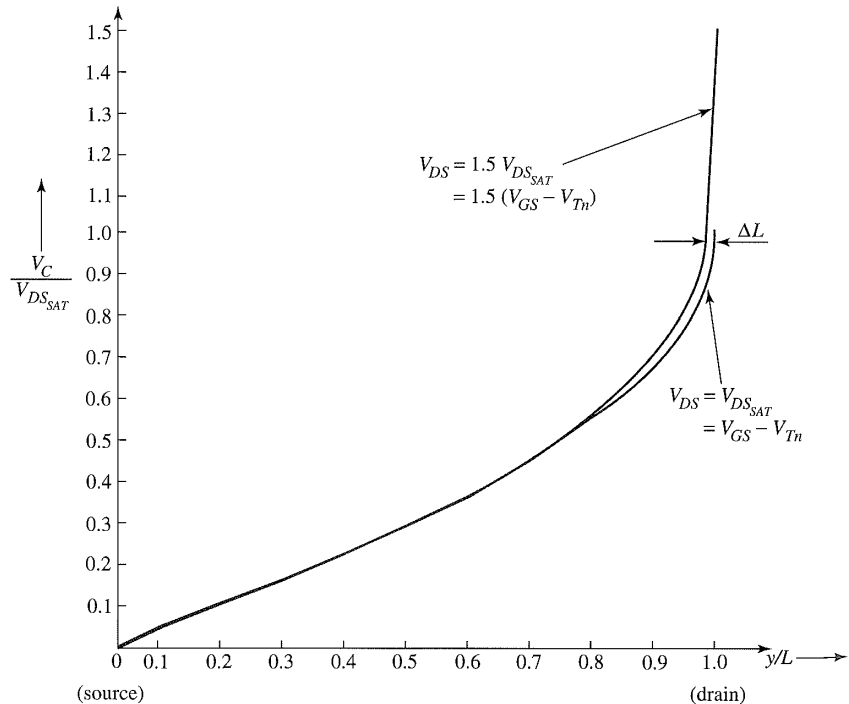
$$I_D = -WQ_N(L)v_y(L) = WC_{ox}(V_{GS} - V_{Tn} - V_C(L))\mu_n \left. \frac{dV_C}{dy} \right|_{y=L} \quad (4.51)$$

When the drain voltage is $V_{DS} = V_{GS} - V_{Tn}$, the channel charge vanishes at the drain end of the channel. Consequently, the channel is said to be “pinched off” at the drain. In order for the drain current to remain constant, the drift velocity must be infinite at $y = L$. Since we assumed that the drift velocity is proportional to the electric field, this condition can be satisfied mathematically by the channel voltage having an infinite slope at the drain as shown in Fig. 4.16. In reality, the drift velocity saturates and consequently, the channel electron charge is very small, but does not vanish, at the drain end of the channel.

We know from the measured drain characteristics in Fig. 4.3 that the drain current I_D **saturates** or remains nearly constant as the drain voltage increases beyond V_{DS_SAT} . The explanation for this phenomenon lies in the drain current equation (Eq. (4.41)) that is repeated here for convenience.

$$\int_0^L I_D dy = \int_0^{V_{DS}} W \mu_n C_{ox} (V_{GS} - V_{Th} - V_C(y)) dV_C \quad (4.52)$$

When $V_{DS} < V_{DS_{SAT}}$, increasing the drain voltage increases the upper limit on the integral on the right-hand side, but also modifies the integrand by changing $V_C(y)$ as shown in Fig. 4.16. Once the channel pinches off for $V_{DS} = V_{DS_{SAT}}$ the channel charge nearly vanishes at the drain end and the lateral electric field becomes very large. An increase in drain voltage beyond $V_{DS_{SAT}}$ causes the high-field region at the drain to widen by a small distance ΔL —enough to accommodate the additional drop $V_{DS} - V_{DS_{SAT}}$. Figure 4.17 shows a qualitative picture of this effect that is called **channel length modulation**. To first order, the drain current I_D is unchanged by increases in V_{DS} above saturation. The right-hand integral in Eq. (4.52) is over the channel (where $0 < V_C(y) < V_{DS_{SAT}}$) and is unaffected. Electrons drifting along the channel enter the high-field region near the drain and are simply swept into the n^+ drain—at their saturation velocity.



► **Figure 4.17** Channel voltage, normalized to the saturation drain-source voltage $V_{DS_{SAT}}$, for $V_{DS} = V_{DS_{SAT}}$ and for $V_{DS} = 1.5 V_{DS_{SAT}}$.

Upon closer inspection, the drain current is perturbed slightly by an increase in drain voltage above $V_{GS} - V_{Tn}$. The point y in the channel at which $V_C(y) = V_{DS_{SAT}}$ and therefore $Q_N(y) = 0$ moves a small distance ΔL toward the source as the drain voltage increases beyond saturation. The channel length is shortened to $L - \Delta L$, which changes the limit of integration on the left-hand integral in Eq. (4.52)

$$\int_0^{(L - \Delta L)} I_D dy = I_D (L - \Delta L) = \mu_n C_{ox} W \int_0^{V_{DS_{SAT}}} (V_{GS} - V_{Tn} - V_C) dV_C \quad (4.53)$$

where the channel extends over $0 \leq y \leq L - \Delta L$ and the channel voltage ranges from $0 \leq V_C \leq V_{DS_{SAT}}$. Carrying out the integration and substituting $V_{DS_{SAT}} = V_{GS} - V_{Tn}$, we find

$$I_{D_{SAT}} = \frac{1}{2} \left(\frac{W}{L - \Delta L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn})^2 \text{ for } V_{DS} \geq V_{DS_{SAT}} = V_{GS} - V_{Tn} \quad (4.54)$$

An exact calculation of the channel-length modulation ΔL as a function of the terminal voltages involves solving the two-dimensional Poisson's Equation in the drain region. However, a useful approximation can be made by noting that $\Delta L \ll L$

$$\frac{1}{L - \Delta L} \approx \frac{1}{L} \left(1 + \frac{\Delta L}{L} \right) \quad (4.55)$$

For simplicity, we assume that the fractional change in channel length is proportional to the drain voltage

$$\frac{\Delta L}{L} = \lambda_n V_{DS} \quad (4.56)$$

where λ_n is the **channel-length modulation parameter**. Device measurements and simulations indicate that λ_n varies roughly with the inverse of channel length. For the MOSFETs in this text we will use

$$\lambda_n = \frac{0.1 \mu\text{mV}^{-1}}{L} \quad (4.57)$$

where L is in μm . Finally, we substitute Eqs. (4.55) and (4.56) into Eq. (4.54) and find a very useful approximation to the drain current in saturation

$$I_D = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS}) \quad (4.58)$$

where $V_{DS} \geq V_{DS_{SAT}} = V_{GS} - V_{Tn}$.

Considering the several simplifying assumptions that have gone into the drain current equations, it is remarkable that they are quite adequate models for hand analysis and design. In practice, the channel electron mobility μ_n is adjusted to fit Eq. (4.42) to the measured drain current. A typical value for channel electron mobility in modern MOSFETs is $200 \text{ cm}^2/(\text{Vs})$, substantially less than the electron mobility in bulk silicon.

► EXAMPLE 4.4 Vertical and lateral electric fields in the channel

For an n-channel MOSFET with $L = 1.5 \mu\text{m}$, $t_{ox} = 150 \text{ \AA}$, $N_a = 10^{17} \text{ cm}^{-3}$, and $V_{Th} = 0.6 \text{ V}$, evaluate $E_x(0, y)$ and $E_y(0, y)$ to verify the gradual channel approximation, which assumes $|E_y| \ll E_x$.

(a) For $V_{GS} = 1.5 \text{ V}$, $V_{DS} = V_{DSAT} = 0.9 \text{ V}$, $V_{BS} = 0 \text{ V}$, find the vertical and lateral electric fields at $y = 0.75 \mu\text{m}$.

SOLUTION

The vertical electric field in the silicon at $x = 0^+$ can be found from the oxide field by applying the boundary condition at the oxide/silicon interface

$$E_x(0^+, y = 0.75 \mu\text{m}) = \left(\frac{\epsilon_{ox}}{\epsilon_s} \right) \frac{V_{ox}(y = 0.75 \mu\text{m})}{t_{ox}}$$

The potential drop across the oxide is given by (see Fig. 4.13)

$$V_{ox}(y) = (V_{GS} + \phi_{n+}) - \phi(0, y) = V_{GS} + \phi_{n+} - V_C(y) + \phi_p$$

where we substituted the channel voltage $V_C(y)$ using Eq. (4.32). We can calculate the channel voltage at $y = 0.75 \mu\text{m}$ from Eq. (4.49)

$$V_C = (1.5 - 0.6) - \sqrt{(1.5 - 0.6)^2 - 2(1.5 - 0.6 - 0.45)(0.9)(0.75/1.5)} = 0.26 \text{ V}$$

Note that the channel voltage is much less than $V_{DS}/2 = 0.45 \text{ V}$ at the halfway point in the channel, which is consistent with the normalized plots in Fig. 4.16. The vertical electric field at $y = 0.75 \mu\text{m}$ is

$$E_x(0^+, y = 0.75 \mu\text{m}) = \left(\frac{1}{3} \right) \frac{(1.5 + 0.55 - (0.26 - 0.42))}{1.5 \times 10^{-6} \text{ cm}} = 3.3 \times 10^5 \text{ V/cm}$$

The lateral electric field at the halfway point in the channel can be found directly from Eq. (4.50)

$$E_y = \frac{-(1.5 - 0.6 - 0.45)(0.9)}{(1.5) \sqrt{(1.5 - 0.6)^2 - 2(1.5 - 0.6 - 0.45)(0.9)(0.75/1.5)}} = -4250 \text{ V/cm}$$

The ratio of the lateral field magnitude to the vertical field is $0.013 \ll 1$. The results of the gradual channel approximation justify the use of one-dimensional results from the MOS capacitor in Chapter 3.

(b) Find the vertical and lateral fields at $y = 1.45 \mu\text{m}$.

SOLUTION

Applying the same analysis near the drain end of the channel, we find that the channel voltage is $V_C(y = 1.45 \mu\text{m}) = 0.74 \text{ V}$. The vertical electric field is

$$E_x(0^+, y = 1.4 \mu\text{m}) = \left(\frac{1}{3} \right) \frac{(1.5 + 0.55 - (0.74 - 0.42))}{1.5 \times 10^{-6} \text{ cm}} = 2.0 \times 10^5 \text{ V/cm}$$

which is lower than at mid-channel because the channel potential is higher near the drain. The lateral electric field magnitude increases dramatically near the drain, as can be seen from Eq. (4.50)

$$E_y = \frac{-(1.5 - 0.6 - 0.45)(0.9)}{(1.5)\sqrt{(1.5 - 0.6)^2 - 2(1.5 - 0.6 - 0.45)(0.9)}(1.45/1.5)} = -3.3 \times 10^4 \text{ V/cm}$$

The ratio $|E_y|/E_x$ at $y = 1.45 \mu\text{m}$ is about 0.16—the lateral field is much more significant at the drain end of the channel. In order to model the MOSFET accurately near the drain in saturation, it is necessary to solve numerically the two-dimensional Poisson's Equation

► 4.5 MOSFET CIRCUIT MODELS

In the previous section, we developed the groundwork for circuit models for the MOSFET by deriving the steady-state equations for drain current as a function of the terminal voltages. These equations are useful for finding the steady-state behavior of digital circuits and for biasing analog amplifiers. For analog applications, MOSFETs are usually biased in the constant-current (saturation) region and the circuit is designed to process incremental signals. Therefore, we will derive a small-signal model for the n-channel MOSFET in the saturation region. In order to determine the response to time-varying signals, we must include capacitances between the terminals of the saturated MOSFET. We will find that the small-signal analysis of the pn junction and MOS capacitor from Chapter 3 can be applied here to find the capacitances in the MOSFET.

After deriving the n-channel MOSFET circuit models, we can adapt the analysis to the p-channel MOSFET. In a CMOS technology, both n-channel and p-channel MOSFETs are fabricated on the same substrate. One of the transistors is placed in a well of opposite type to the substrate, which affects the device models and the options for the circuit designer.

4.5.1 Steady-State Models

The drain current equations for cutoff, triode, and saturation for an n-channel MOSFET were derived in sections 4.3 and 4.4. The addition of the factor $(1 + \lambda_n V_{DS})$ in Eq. (4.58) to account for channel-length modulation in the saturation region creates a discontinuity in the drain current when $V_{DS} = V_{DS_{SAT}} = V_{GS} - V_{Tn}$. To avoid mathematical difficulties, this factor is added into the current equation for the triode region. The steady-state model for the n-channel MOSFET is

$$\begin{aligned} I_D &= 0 \text{ A} & (V_{GS} \leq V_{Tn}) \\ I_D &= (W/L)\mu_n C_{ox} [V_{GS} - V_{Tn} - (V_{DS}/2)](1 + \lambda_n V_{DS}) V_{DS} & (V_{GS} \geq V_{Tn}, V_{DS} \leq V_{GS} - V_{Tn}) \\ I_{D_{SAT}} &= (W/2L)\mu_n C_{ox} (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS}) & (V_{GS} \geq V_{Tn}, V_{DS} \geq V_{GS} - V_{Tn}) \end{aligned} \quad (4.59)$$

n-channel MOSFET
steady-state drain current

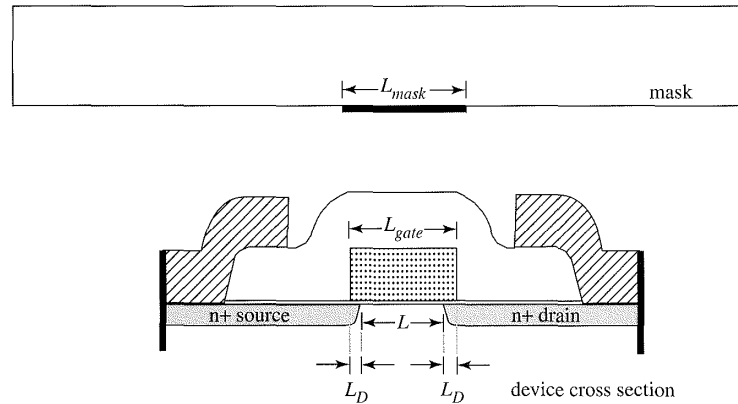
Channel-length modulation can be neglected in the triode region for hand calculations, since the drain voltage V_{DS} is relatively small and the effect has no practical significance. It is easy to forget that the drain current is also a function of the bulk voltage through the threshold voltage. Therefore, Eq. (4.46) is repeated here

$$V_{Tn} = V_{TO_n} + \gamma_n (\sqrt{-V_{BS} - 2\phi_p} - \sqrt{-2\phi_p}) \quad (4.60)$$

where $\gamma_n = (\sqrt{2q\epsilon_s N_a}) / C_{ox}$ is the backgate effect parameter.

Of the various terms in Eqs. (4.59) and (4.60), the gate oxide capacitance C_{ox} can be found directly from measurements of the gate oxide thickness t_{ox} . The MOSFET threshold voltage expression in Eq. (4.37) is very useful for indicating functional dependencies on device dimensions and parameters, although without additional terms it is not sufficiently accurate to predict V_{Tn} . These additional terms account for the contributions of oxide charges and the threshold-adjustment implant and are discussed in advanced device physics texts. In practice, experimental values for V_{TO_n} , μ_n , λ_n , and γ_n are found by “curve-fitting” Eqs. (4.59) and (4.60) to the measured drain characteristics.

At first glance, the ratio W/L in Eqs. (4.59) can be read directly from the device layout. However, the channel length is often designed as the minimum allowed dimension in the fabrication technology. Since the channel length is in the denominator, small errors in L can lead to substantial errors in W/L . Figure 4.18 illustrates the need to be precise in specifying the channel length for the MOSFET. The “as drawn” channel length L_{mask} on the layout becomes the “as etched” length L_{gate} of the polysilicon gate, due to systematic lithography and etching effects. Finally, the ion-implanted source and drain regions diffuse under the polysilicon gate by a dis-



► **Figure 4.18** Definitions of the as-drawn gate length L_{mask} on the mask, the “as-etched” polysilicon gate length L_{gate} , and the channel length $L = L_{gate} - 2L_D$.

tance L_D , as shown in Fig. 4.18. The actual channel length, as defined earlier in Fig. 4.1, is given by

$$L = L_{gate} - 2L_D. \quad (4.61)$$

For this reason and because of the limitations of the gradual channel approximation, the ratio W/L is determined by curve-fitting to the measured drain characteristics.

4.5.2 Small-Signal Model Elements

In analog applications, a DC operating point, specified by the bias voltages V_{GS} , V_{DS} , and V_{BS} , is established so $V_{DS} > V_{DS_{SAT}} = V_{GS} - V_{Tn}$. Incremental voltages v_{gs} , v_{ds} , and v_{bs} that are much smaller in magnitude than the bias voltages perturb the operating point. The small-signal model is a circuit representation of the response of the drain current of the MOSFET to these perturbations.

The total drain current $i_D = I_D + i_d$ is a function of the gate, drain, and bulk voltages in saturation. By summing the contributions from the perturbations v_{gs} , v_{bs} , and v_{ds} , we can write a first-order expansion for the drain current

$$I_D + i_d = I_D + \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q v_{gs} + \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q v_{bs} + \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q v_{ds} \quad (4.62)$$

where Q is the DC operating point of the MOSFET, which is defined by V_{GS} , V_{BS} , and V_{DS} . The partial derivatives in Eq. (4.62) represent small-signal circuit elements and are given the following symbols

$$i_d = g_m v_{gs} + g_{mb} v_{bs} + g_o v_{ds} \quad (4.63)$$

where

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q, \quad g_{mb} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q, \quad \text{and} \quad g_o = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q \quad (4.64)$$

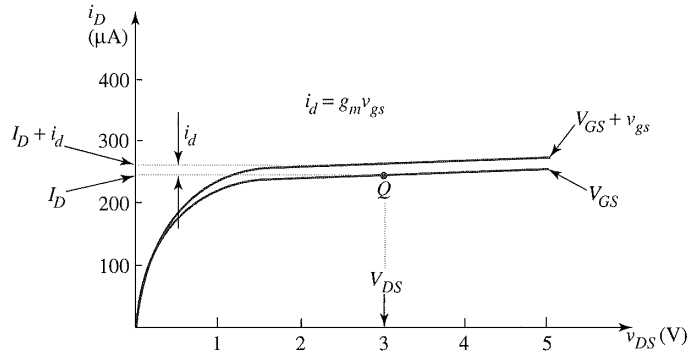
The MOSFET **transconductance** g_m connects the small-signal gate-source voltage v_{gs} to the resulting incremental drain current. The **backgate transconductance** g_{mb} represents the perturbation of the drain current by an incremental change in the bulk-source voltage. Finally, the **output conductance** g_o relates the incremental change in drain current due to a small-signal, drain-source voltage.

For an operating point Q in the saturation region, Fig. 4.19 is a graphical interpretation of the transconductance. Substituting the saturation drain current expression from Eq. (4.59), we find

$$g_m = \left. \frac{\partial}{\partial v_{GS}} \right|_Q \left\{ \left(\frac{W}{2L} \right) \mu_n C_{ox} (v_{GS} - V_{Tn})^2 (1 + \lambda_n v_{DS}) \right\} \quad (4.65)$$

Evaluating the partial derivative at the operating point, we find

$$g_m = \left(\frac{W}{L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn}) (1 + \lambda_n V_{DS}). \quad (4.66)$$



► **Figure 4.19** Graphical interpretation of the perturbation of the saturated drain current by the small-signal, gate-source voltage v_{gs} at bias point $Q = (V_{GS}, V_{DS}, V_{BS})$. Note that the drain-source and bulk-source voltages are kept constant so $v_{ds} = 0$ V, $v_{bs} = 0$ V,

A useful approximation to this equation can be made by neglecting the contribution from the channel length modulation, which will be a small error if $\lambda_n V_{DS} \ll 1$

n-channel MOSFET
transconductance g_m

$$g_m \equiv \left(\frac{W}{L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn}) = \sqrt{2 \left(\frac{W}{L} \right) \mu_n C_{ox} I_D} \quad (4.67)$$

These results indicate that g_m is equally sensitive to the bias drain current, the channel width-to-length ratio, and $\mu_n C_{ox}$. In Chapter 7 we will see that the bipolar junction transistor has a transconductance that is linearly related to the bias current, in contrast to the square-root dependence on bias current for the MOSFET. For a typical channel mobility $215 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, and oxide capacitance $2.3 \text{ fF} \mu\text{m}^{-2}$, bias drain current $I_D = 100 \text{ } \mu\text{A}$, and $(W/L) = 10$, we find that the transconductance $g_m = 316 \text{ } \mu\text{S}$ ($\text{S} = \text{A/V}$).

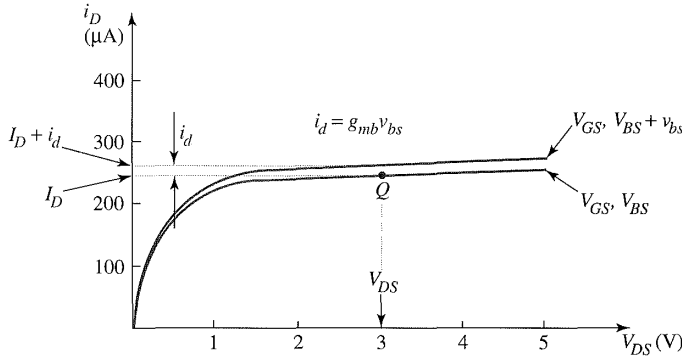
Continuing with the backgate transconductance g_{mb} , it is convenient to expand the partial derivative in Eq. (4.64) using the chain rule

$$g_{mb} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q = \left. \frac{\partial i_D}{\partial V_{Tn}} \right|_Q \left. \frac{\partial V_{Tn}}{\partial v_{BS}} \right|_Q \quad (4.68)$$

The first partial derivative can be evaluated by substitution of Eq. (4.59)

$$\left. \frac{\partial i_D}{\partial V_{Tn}} \right|_Q = \frac{\partial}{\partial V_{Tn}} \left(\frac{W}{2L} \right) \mu_n C_{ox} (v_{GS} - V_{Tn})^2 (1 + \lambda_n v_{DS}) = - \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q = -g_m \quad (4.69)$$

where we recognize that the result is the negative of the transconductance. Partial differentiation of the threshold voltage (Eq. (4.60)) yields an expression for the backgate transconductance



► **Figure 4.20** Perturbation of the saturated drain current by the small-signal, bulk-source voltage v_{bs} at bias point $Q = (V_{GS}, V_{DS}, V_{BS})$. Note that the gate-source and drain-source voltages are kept constant so $v_{gs} = 0$ V, $v_{ds} = 0$ V.

$$g_{mb} = (-g_m) \left. \frac{\partial V_{Tn}}{\partial v_{BS}} \right|_Q = (-g_m) \left(\frac{-\gamma_n}{2\sqrt{-2\phi_p - V_{BS}}} \right) = \frac{\gamma_n g_m}{2\sqrt{-2\phi_p - V_{BS}}} \quad (4.70)$$

n-channel MOSFET
backgate trans-
conductance g_{mb}

where γ_n is the n-channel backgate effect parameter defined in Eq. (4.47). Figure 4.20 shows how the backgate transconductance can be measured on the drain characteristics.

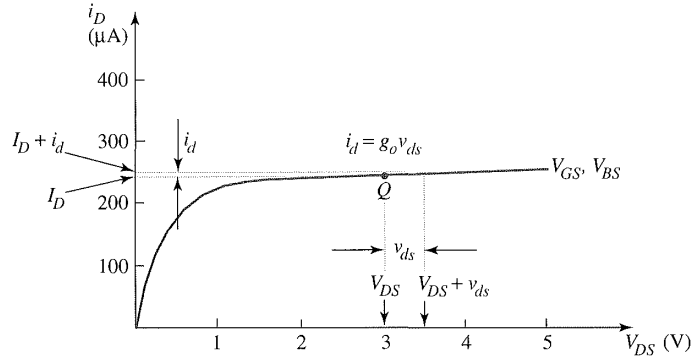
The physical meaning of the backgate transconductance is that incremental changes in the bulk-source voltage alter the electrostatics of the MOS structure and affect the channel charge exactly as do small-signal gate-source voltages. The bulk thus acts as a **backgate** (actually, “bottom gate” would be more descriptive) that is separated from the channel by a depletion layer. Using Eq. (4.70), we can solve for the ratio of the two transconductances

$$\frac{g_{mb}}{g_m} = \frac{\sqrt{2q\epsilon_s N_a}}{2C_{ox}\sqrt{-2\phi_p - V_{BS}}} = \frac{1}{C_{ox}} \sqrt{\frac{q\epsilon_s N_a}{2(-2\phi_p - V_{BS})}} = \frac{C_b(y=0)}{C_{ox}} \quad (4.71)$$

in which we identified the depletion capacitance at the source end of the channel, $C_b(y=0)$ from

$$C_b(y=0) = \frac{\epsilon_s}{X_d(y=0)} = \frac{\epsilon_s}{\sqrt{\frac{\epsilon_s V_B(y=0)}{2qN_a}}} \quad \text{and} \quad V_B(y=0) = -2\phi_p - V_{BS}. \quad (4.72)$$

Evaluating Eq. (4.71) with the bulk shorted to the source ($v_{BS} = 0$ V) and $N_a = 10^{17} \text{ cm}^{-3}$, the backgate transconductance is about 40% of the “front gate” transconductance g_m . However, the bulk-source signal $v_{bs} = 0$ V for this case, making $g_{mb}v_{bs} = 0$ A. For a MOSFET with $V_{BS} = -1.5$ V, $g_{mb}/g_m \approx 0.25$. In order to minimize



► **Figure 4.21** Perturbation of the saturated drain current by the small-signal, drain-source voltage v_{ds} at bias point $Q = (V_{GS}, V_{DS}, V_{BS})$. Note that the gate-source and bulk-source voltages are kept constant, so that $v_{gs} = 0$ V, $v_{bs} = 0$ V.

the relative magnitude of the backgate transconductance, Eq. (4.71) shows it is necessary to increase the gate capacitance (by reducing the gate oxide) or reduce the depletion capacitance between the channel and the bulk. The latter can be achieved by reducing the bulk doping or increasing the magnitude of the bulk-source bias voltage.

The final small-signal element is the drain conductance g_o that represents the dependence of the drain current on the drain-source voltage

n-channel MOSFET
output conductance g_o

$$g_o = \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q = \left(\frac{W}{2L} \right) \mu_n C_{ox} (V_{GS} - V_{Tn})^2 \lambda_n \equiv \lambda_n I_D \quad (4.73)$$

where we again make the approximation that $\lambda_n V_{DS} \ll 1$ at the operating point to obtain a simpler result. The graphical interpretation of the output conductance is shown in Fig. 4.21.

The channel-length modulation parameter λ_n has been found to vary inversely with the channel length

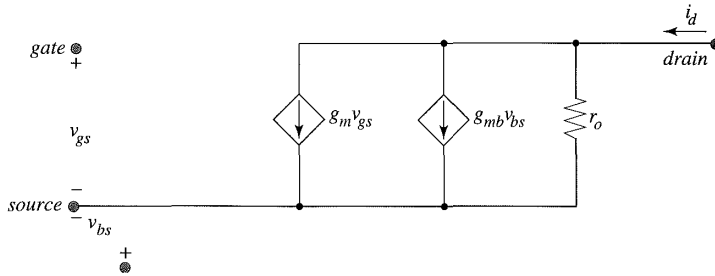
$$\lambda_n = \propto \frac{1}{L}, \quad (4.74)$$

For a MOSFET with $L = 1.5 \mu\text{m}$, $\lambda_n = 0.06 \text{ V}^{-1}$. At a DC bias current $I_D = 100 \mu\text{A}$, the inverse of the drain conductance, called the **output resistance**, is

$$(g_o)^{-1} = r_o = 150 \text{ k}\Omega \quad (4.75)$$

4.5.3 Small-Signal Circuit

We can assemble the small-signal model for steady-state perturbations on the operating point by properly connecting these three elements between the four terminals of the MOSFET. Kirchhoff's current law indicates that the three elements are con-



► **Figure 4.22** Steady-state small-signal model for the n-channel MOSFET in saturation.

ected in parallel at the drain node as shown in Fig. 4.22, since their contributions sum to give the small-signal drain current

$$i_d = g_m v_{gs} + g_{mb} v_{bs} + g_o v_{ds} \quad (4.76)$$

Note that the small-signal, steady-state gate current of the MOSFET is zero. In addition, the reverse-biased source-bulk junction is an open circuit in steady-state as shown in Fig. 4.22.

4.5.4 MOSFET Capacitances in Saturation

The MOS capacitor formed between the gate and substrate is the central structure of the MOSFET. The inversion-layer electron charge under the gate plays a fundamental role in the MOSFET by enabling current between the drain and source. In order to model the small-signal response to time-varying small signals, we must model the MOS capacitor and other capacitors in the transistor, when the MOSFET is operated in the saturation region.

In saturation, the channel charge is a function only of the gate-source voltage. As discussed in Sections 4.3 and 4.4, changes in the drain-source voltage have negligible effect on the channel for $V_{GS} > V_{DS_{SAT}}$. The total electron charge in the channel in saturation is given by

$$q_N(v_{GS}) = -W \int_0^L C_{ox} (v_{GS} - V_{Tn} - v_C(y)) dy \quad (4.77)$$

where we integrate the channel charge per unit area from Eq. (4.33) over the area of the channel. Symbols for total channel charge q_N , gate-source voltage v_{GS} , and channel voltage v_C are used since incremental (small) signals are present. We can change variables in the integral using Eq. (4.40)

$$dy = \left(\frac{W \mu_n C_{ox}}{i_D} \right) (v_{GS} - V_{Tn} - v_C) dv_C \quad (4.78)$$

and then integrate from the source ($y = 0$ and $v_C = 0$ V) to the drain ($y = L$ and $v_C = v_{DS} = v_{GS} - V_{Tn}$ for saturation)

$$q_N(v_{GS}) = - \left(\frac{W^2 \mu_n C_{ox}^2}{i_D} \right) \int_0^{v_{GS} - V_{Tn}} (v_{GS} - V_{Tn} - v_C^2) dv_C \quad (4.79)$$

After evaluation of the integral and substitution of the drain current equation in saturation, we can express the channel charge as a function of the gate-source voltage

$$q_N(v_{GS}) = -\frac{2}{3} W L C_{ox} (v_{GS} - V_{Tn}) \quad (4.80)$$

The gate charge is equal and opposite to the sum of the channel charge and the maximum bulk (depletion region) charge

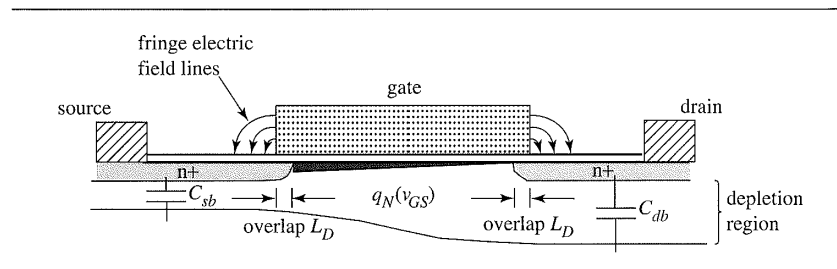
$$q_G(v_{GS}) = -q_N(v_{GS}) - Q_{B,max} = \frac{2}{3} W L C_{ox} (v_{GS} - V_{Tn}) - Q_{B,max} \quad (4.81)$$

The capacitance in saturation is the derivative of Eq. (4.81)

$$\left. \frac{dq_G}{dv_{GS}} \right|_{v_{GS} \geq v_{DS,SAT}} = \frac{2}{3} W L C_{ox} \quad (4.82)$$

where we have used the fact that the bulk charge is constant in saturation.

Figure 4.23 is a cross section of the MOSFET biased in saturation. Due to overlap of the source and drain diffusions and the polysilicon gate and the contribution of fringe electric fields from the gate, there is significant additional capacitance. The overlap capacitance C_{ov} is quantified as a linear capacitance proportional to the gate width, with units of fF/ μm . The total gate-source capacitance in saturation is the sum of Eq. (4.82) and the overlap capacitance:



► **Figure 4.23** MOSFET cross section in saturation showing the channel charge $q_N(v_{GS})$ and the overlap and fringe contributions to C_{ov} . The source-bulk and drain-bulk depletion capacitances are also shown qualitatively.

$$C_{gs} = \frac{2}{3} WLC_{ox} + WC_{ov} \quad (4.83)$$

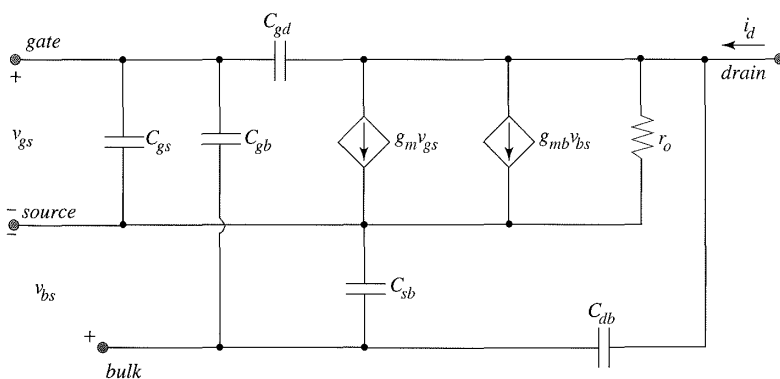
Since the drain has no influence on the channel charge, the only contribution to the gate-drain capacitance is C_{ov} :

$$C_{gd} = WC_{ov} \quad (4.84)$$

The drain-bulk and source-bulk capacitances C_{db} and C_{sb} originate from charge storage in the depletion regions between the drain and source n^+ regions and the p-type bulk. Given the area of these reverse-biased junctions $A_{diff} = L_{diff}W$ from the layout in Fig. 4.1, C_{db} and C_{sb} can be found as functions of the junction voltages V_{DB} and V_{SB} using the results from Section 3.6. Finally, the capacitance C_{gb} between gate and bulk is from the overlap of the polysilicon gate onto the field oxide region as shown in Fig. 4.1. This MOS capacitor is in depletion for normal gate voltages and its capacitance can be found from the MOS capacitor analysis in Section 3.9. It is often ignored as negligible, however, and is included only for completeness.

To predict the frequency response of the MOSFET, we add the capacitances between the terminals at the operating point. Figure 4.24 shows the schematic for the small-signal model of the intrinsic n-channel MOSFET with the capacitances added to the steady-state model in Fig. 4.22.

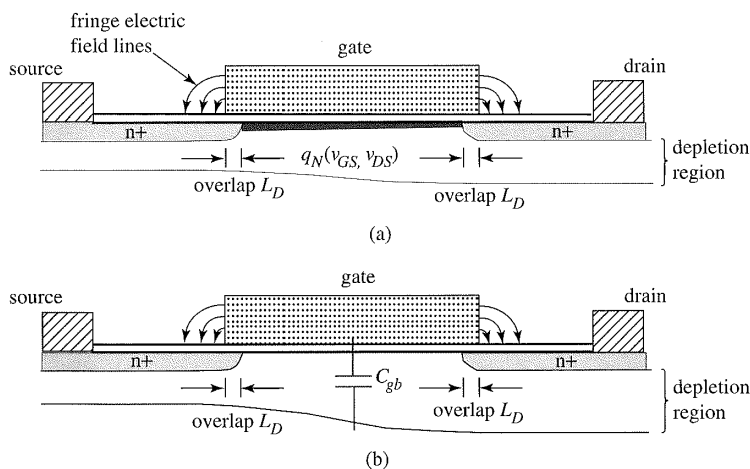
One final, but very important point. We have only modeled the *intrinsic* MOSFET, that is, the device without interconnections. The parasitic capacitances of the interconnections between MOSFETs are often the limiting factor in switching speed and *must* be estimated from the layout and cross section for accurate analysis of a design. Off-chip wiring and package capacitances are also critical for evaluating the performance of any integrated circuit.



► **Figure 4.24** Complete small-signal model for the n-channel MOSFET in saturation.

gate-source capacitance
in saturation

gate-drain capacitance
in saturation



► **Figure 4.25** MOSFET cross section showing components of C_{gs} , C_{gd} , and C_{gb} in (a) triode and (b) cutoff.

4.5.5 MOSFET Capacitances in Triode and Cutoff

A basic understanding of the terminal capacitances in triode and in cutoff is useful for digital IC design. Figure 4.25 (a) shows the channel charge in triode, which is a function of both v_{GS} and v_{DS} . Rather than derive models for C_{gs} or C_{gd} from $q_N(v_{GS}, v_{DS})$, we split the total channel charge equally between source and drain. After adding in the overlap capacitances, the triode-region capacitances are

C_{gs} and C_{gd} in triode

$$C_{gs} = C_{gd} = \frac{WLC_{ox}}{2} + WC_{ov} = C_{gd} \quad (4.85)$$

In triode, C_{gd} is much larger than its value in saturation, whereas the gate-source capacitance C_{gs} decreases from its value in saturation.

In cutoff, there is no channel present as shown in Fig. 4.25(b). The depletion region under the gate is under gate control and the MOS capacitor theory from Section 3.9 can be applied to find C_{gb} . The gate-bulk capacitance is a sensitive function of the gate-bulk bias voltage, as seen in Fig. 3.35. Since no channel is present in cutoff, the gate-source and gate-drain capacitances are each equal to the overlap capacitance.

C_{gs} and C_{gd} in cutoff

$$C_{gs} = C_{gd} = WC_{ov} \quad (4.86)$$

This result completes our overview of charge storage in the MOSFET. The terminal capacitances are very different in the three regions of operation, as can be seen from Eqs. (4.83)-(4.86). In the case of large transients such as in digital logic, the complexities of charge storage in the MOSFET are a challenge even for numerical simulators. For small-signal analysis in the saturation region, which is the usual case in analog design, the capacitances in Eqs. (4.83) and (4.84) are reasonably accurate for hand analysis.

► EXAMPLE 4.5 MOSFET small-signal model

For the n-channel MOSFET in Fig. 4.1, the channel length is $L = 2\text{ }\mu\text{m}$, the width is $W = 30\text{ }\mu\text{m}$, the length of the source-drain diffusions is $L_{\text{diff}} = 6\text{ }\mu\text{m}$, the channel mobility is $\mu_n = 215\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, the oxide thickness is $t_{\text{ox}} = 150\text{ }\text{\AA}$, and the substrate doping is $N_a = 10^{17}\text{ cm}^{-3}$, and the channel length modulation parameter is $\lambda_n = 0.05\text{ V}^{-1}$. The overlap capacitance is $C_{\text{ov}} = 0.5\text{ fF}/\mu\text{m}$. The threshold voltage without backgate bias is $V_{\text{TO}n} = 1\text{ V}$. Note that this measured threshold voltage is greater than predicted by the simple MOS theory in Chapter 3 (due to the presence of a shallow threshold-adjustment implant and charge in the oxide film.)

(a) For the DC operating point Q ($V_{\text{GS}} = 1.5\text{ V}$, $V_{\text{DS}} = 1.5\text{ V}$, $V_{\text{BS}} = 0\text{ V}$), find all the small-signal model parameters in Fig. 4.24, except the gate-bulk capacitance C_{gb} that we will consider negligible.

SOLUTION

Saturation drain current:

The first step is to find the DC bias current from Eq. (4.59)

$$I_D = \left(\frac{W}{2L} \right) \mu_n C_{\text{ox}} (V_{\text{GS}} - V_{\text{T}n})^2 (1 + \lambda_n V_{\text{DS}})$$

in which

$$\mu_n C_{\text{ox}} = (215\text{ cm}^2\text{V}^{-1}\text{s}^{-1})(3.9 \times 8.85 \times 10^{-14}\text{ F/cm})(1.5 \times 10^{-6}\text{ cm})^{-1} = 49.5\text{ }\mu\text{AV}^{-2}$$

The threshold voltage is

$$V_{\text{T}n} = V_{\text{TO}n} + \gamma_n (\sqrt{-2\phi_p - V_{\text{BS}}} - \sqrt{-2\phi_p}) = V_{\text{TO}n} = 1\text{ V} \text{ since } V_{\text{BS}} = 0\text{ V}$$

The error in neglecting the channel-length modulation term in finding I_D is $(0.05)(1.5) = 0.075$, less than 10%. Therefore, we neglect it for hand calculations. Substituting $\mu_n C_{\text{ox}}$, $V_{\text{T}n}$, (W/L) , and V_{GS} into the saturation drain current, we find

$$I_D = \frac{1}{2} \left(\frac{30}{2} \right) (49.5\text{ }\mu\text{AV}^{-2}) (1.5\text{ V} - 1\text{ V})^2 = 91\text{ }\mu\text{A}$$

Steady-State Parameters:

From Eq. (4.67), the transconductance is

$$g_m = \left(\frac{30}{2} \right) (49.5\text{ }\mu\text{AV}^{-2}) (1.5\text{ V} - 1\text{ V}) = 371\text{ }\mu\text{S}$$

The backgate effect parameter is found from Eq. (4.47)

$$\gamma_n = \frac{\sqrt{2 \cdot 1.6 \times 10^{-19} \cdot 11.7 \cdot 8.85 \times 10^{-14}\text{ F cm}^{-1} \cdot 10^{17}\text{ cm}^{-3}}}{(3.9 \cdot 8.85 \times 10^{-14}\text{ F cm}^{-1}) / (1.5 \times 10^{-6}\text{ cm})} = 0.79\text{ V}^{1/2}$$

Substitution of γ_n and $\phi_p = -0.42\text{ V}$ (from the known substrate doping) into Eq. (4.70) yields the backgate transconductance

$$g_{mb} = \frac{(0.79\text{ V}^{1/2}) \cdot (371\text{ }\mu\text{S})}{2\sqrt{-2(-0.42\text{ V})} - 0} = 160\text{ }\mu\text{S}$$

The output resistance is

$$r_o = \frac{1}{g_o} = \frac{1}{\frac{1}{2} \left(\frac{30}{2} \right) (49.5 \mu\text{A V}^{-2}) (1.5\text{ V} - 1\text{ V})^2 (0.05\text{ V}^{-1})} = 220\text{ k}\Omega$$

Capacitances:

The gate oxide capacitance (per unit area) is

$$C_{ox} = \frac{(3.9 \cdot 8.85 \times 10^{-14} \text{ F cm}^{-1})}{(1.5 \times 10^{-6} \text{ cm})} = 2.3\text{ fF}/\mu\text{m}^2$$

Substituting C_{ox} and $C_{ov} = 0.5\text{ fF}/\mu\text{m}$ into Eq. (4.83), together with the MOSFET dimensions, we find

$$C_{gs} = \left(\frac{2}{3} \right) (30 \cdot 2\text{ }\mu\text{m}^2) (2.3\text{ fF}/\mu\text{m}^2) + (30\text{ }\mu\text{m}) (0.5\text{ fF}/\mu\text{m}) = 107\text{ fF}$$

and the gate-drain capacitance: $C_{gd} = (0.5\text{ fF}/\mu\text{m})(30\text{ }\mu\text{m}) = 15\text{ fF}$.

The remaining capacitances are the pn junction depletion capacitances C_{db} between the n^+ drain and the substrate and C_{sb} between the n^+ source and the substrate. The zero-bias depletion capacitance per unit area for both junctions is

$$C_{jo} = \epsilon_s \sqrt{\frac{q}{2\epsilon_s \phi_B} \left(\frac{1}{N_a} + \frac{1}{N_d} \right)^{-1}} \equiv \sqrt{\frac{q\epsilon_s N_a}{2\phi_B}}$$

from Eq. (3.79). Since the source and drain are heavily doped, the junction can be considered one-sided and the contribution of the depletion region on the n-side of the junction can be neglected. The built-in voltage is

$$\phi_B = \phi_{n+} - \phi_p = 0.55\text{ V} - (-0.42\text{ V}) = 0.97\text{ V}$$

The zero-bias junction capacitance is

$$C_{jo} = \sqrt{\frac{(1.6 \times 10^{-19} \text{ C}) (11.7) (8.85 \times 10^{-14} \text{ F/cm}) (10^{17} \text{ cm}^{-3})}{2 (0.97\text{ V})}} = 0.92\text{ fF}/\mu\text{m}^2$$

The source junction has a bias voltage of $V_{BS} = 0\text{ V}$, which implies

$$C_{sb} = C_{jo} (WL_{diff}) = (0.92\text{ fF}/\mu\text{m}^2) (30\text{ }\mu\text{m} \cdot 6\text{ }\mu\text{m}) = 166\text{ fF}$$

The drain junction has a bias voltage of $V_{BD} = -V_{DS} = -1.5\text{ V}$, so its depletion capacitance is reduced (Eq. 3.80)

$$C_{db} = \frac{(WL_{diff}) C_{jo}}{\sqrt{1 - V_{BD}/\phi_B}} = \frac{(30\text{ }\mu\text{m} \cdot 6\text{ }\mu\text{m}) (0.92\text{ fF}/\mu\text{m}^2)}{\sqrt{1 - (-1.5\text{ V}) / (0.97\text{ V})}} = 104\text{ fF}$$

We have found the complete small-signal model for the n-channel MOSFET in Fig. 4.1 evaluated at the given operating point.

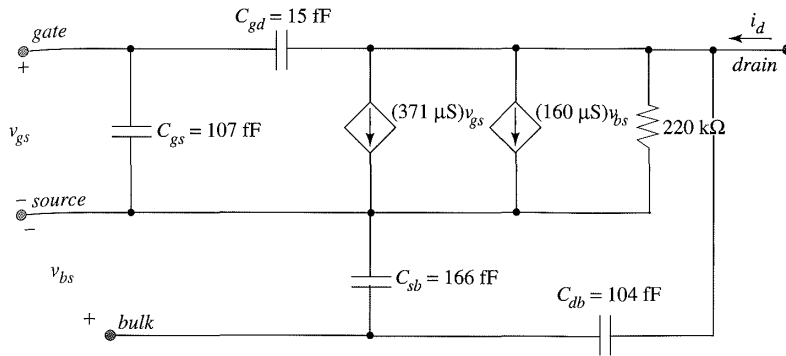


Figure Ex4.5 Small-signal model for the MOSFET in Fig. 4.1 as calculated in Example 4.5.

As we will see in Section 4.6 on the MOSFET SPICE model, the contribution of the perimeters of the source and drain diffusions can be important. The one-dimensional junction capacitance analysis in Chapter 3 is appropriate for the planar bottom of the junction. In order to estimate the perimeter capacitance, a two-dimensional or even three-dimensional analysis is needed.

(b) The product of the transconductance and the output resistance is an important quantity in small-signal amplifiers. For the MOSFET in part (a), this quantity is

$$g_m \cdot r_o = (371 \mu\text{S}) \cdot (220 \text{ k}\Omega) = 82$$

For many applications, $g_m r_o$ must be much larger. Given the same operating point as in part (a) and the same width-to-length ratio, redesign the MOSFET so that $g_m r_o = 150$. What penalty is paid for improving the product?

SOLUTION

It is worthwhile to examine the functional dependence of $g_m r_o$ by multiplying Eq. (4.67) and the inverse of Eq. (4.73)

$$g_m \cdot r_o = \frac{\left(\frac{W}{L}\right) \mu_n C_{ox} (V_{GS} - V_{Tn})}{\left(\frac{W}{2L}\right) \mu_n C_{ox} (V_{GS} - V_{Tn})^2 \lambda_n} = \frac{2}{(V_{GS} - V_{Tn}) \lambda_n}$$

Since the operating point is unchanged, the only term that can be adjusted is the channel length modulation parameter λ_n . From Eq. (4.74), λ_n varies inversely with channel length. Given that $\lambda_n = 0.05 \text{ V}^{-1}$ for $L = 2 \mu\text{m}$, we find the constant of proportionality to be $0.1 \mu\text{mV}^{-1}$. Solving for λ_n ,

$$\lambda_n = \frac{2}{(g_m \cdot r_o) (V_{GS} - V_{Tn})} = \frac{0.1 \mu\text{mV}^{-1}}{L}.$$

from which we can solve for L

$$L = \left(\frac{1}{2} \right) [150 \cdot (1.5\text{V} - 1\text{V})] (0.1 \mu\text{mV}^{-1}) = 3.75 \mu\text{m}$$

Since the width-to-length ratio has been held constant, the channel width is

$$W = (30/2)(3.75) \mu\text{m} = 56.25 \mu\text{m}$$

The penalty for improving the $g_m r_o$ product is an increase in the area of the MOSFET. In addition, C_{gs} and C_{gd} are increased due to larger W and L . The total area (not counting any backgate contact) is now

$$A = W(L + 2L_{diff}) = (56.25)(3.75 + 2(6)) \mu\text{m}^2 = 886 \mu\text{m}^2$$

By comparison, the original device area was $(30)(2 + 2(6)) = 420 \mu\text{m}^2$, so the area has more than doubled.

(c) An alternative approach to increasing the $g_m r_o$ product is to keep the device geometry the same and modify the operating point. We will also specify that $V_{DS} = 1.5\text{V}$ and that $V_{BS} = 0\text{V}$. Find V_{GS} and I_D for $g_m r_o = 150$.

SOLUTION

We can solve for the required gate-source bias from

$$g_m \cdot r_o = \frac{2}{(V_{GS} - V_{Tn}) \lambda_n}$$

The channel length remains $L = 2 \mu\text{m}$ and so the channel-length modulation parameter remains $\lambda_n = 0.05\text{V}^{-1}$. Solving for V_{GS} , we find

$$V_{GS} = V_{Tn} + \frac{2}{\lambda_n (g_m \cdot r_o)} = 1\text{V} + \frac{2}{(0.05\text{V}^{-1})(150)} = 1.27\text{V}$$

The drain current for this gate-source bias is

$$I_D = \left(\frac{30}{2} \right) \left(\frac{49.5 \mu\text{AV}^{-2}}{2} \right) (1.27\text{V} - 1\text{V})^2 = 27 \mu\text{A}$$

What is the trade-off for lowering the drain current? The transconductance g_m is reduced by more than a factor of two, which degrades the frequency response of the MOSFET, as we will see in Chapter 10. The increased capacitance in (b) also has the same affect, so increasing $g_m r_o$ comes at the cost of diminished bandwidth. This example is an introduction to the trade-offs in device and circuit design in ICs.

4.5.6 p-Channel MOSFET Circuit Models

The drain current equations for a p-channel MOSFET can be derived using exactly the same approach as for the n-channel device since the basic physics is the same. For a p-channel device, the gate must be made negative with respect to the n-type substrate in order to form an inversion layer of holes. Since holes drift across the channel from source to drain in the p-channel MOSFET, the drain voltage must be negative with respect to the source, and the drain current is negative.

A practical problem for the circuit designer is to keep track of the minus signs and negative quantities in the p-channel equations. The common orientation for the p-channel MOSFET on a schematic is with the source “up”—meaning near the positive supply as shown in Fig. 4.2. By taking the source potential as a positive reference, the source-drain potential difference V_{SD} , the source-gate potential V_{SG} , and the bulk-source potential V_{BS} are all positive. By using these quantities in the p-channel drain current equations, only the drain current and the threshold voltage are negative.

$$\begin{aligned} -I_D &= 0 \text{ A} & (V_{SG} \leq -V_{Tp}) \\ -I_D &= (W/L) \mu_p C_{ox} [V_{SG} + V_{Tp} - (V_{SD}/2)] (1 + \lambda_p V_{SD}) V_{SD} & (V_{SG} \geq -V_{Tp}, V_{SD} \leq V_{SG} + V_{Tp}) \\ -I_D &= (W/2L) \mu_p C_{ox} (V_{SG} + V_{Tp})^2 (1 + \lambda_p V_{SD}) & (V_{SG} \geq -V_{Tp}, V_{SD} \geq V_{SG} + V_{Tp}) \end{aligned} \quad (4.87)$$

p-channel MOSFET
steady-state drain
current

The p-channel MOSFET threshold voltage is

$$V_{Tp} = V_{T0p} - \gamma_p (\sqrt{2\phi_n - V_{SB}} - \sqrt{2\phi_n}) \quad (4.88)$$

p-channel MOSFET
threshold voltage

The small-signal parameters can be found from the drain current in the saturation region. Rather than carry out the derivations again, we adapt the n-channel results. The p-channel MOSFET transconductance is

$$g_m = \left(\frac{W}{L} \right) \mu_p C_{ox} (V_{SG} + V_{Tp}) \cong \sqrt{2 \left(\frac{W}{L} \right) \mu_p C_{ox} (-I_D)} \quad (4.89)$$

p-channel MOSFET
transconductance

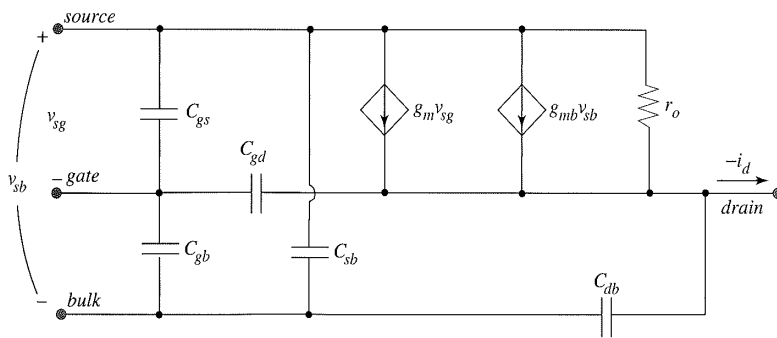
where the transconductance is defined as

$$g_m = \left. \frac{\partial}{\partial V_{SG}} (-i_D) \right|_Q \quad (4.90)$$

The backgate transconductance is

$$g_{mb} = \left. \frac{\partial V_{Tp}}{\partial V_{SB}} \right|_Q = \frac{\gamma_p g_m}{2\sqrt{2\phi_n - V_{SB}}} \quad (4.91)$$

p-channel MOSFET
backgate
transconductance



► **Figure 4.26** Small-signal model for the p-channel MOSFET in saturation.

and the output conductance is

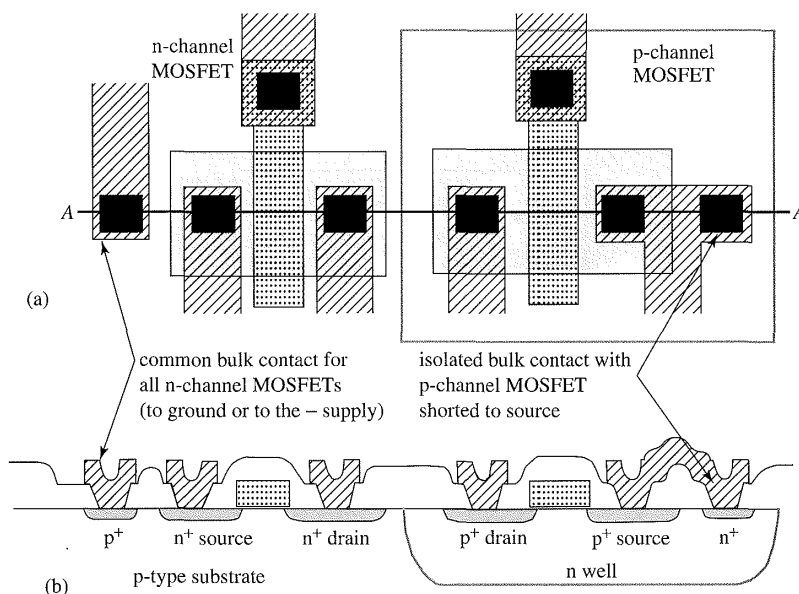
p-channel MOSFET
output conductance

$$g_o = \left. \frac{\partial(-i_D)}{\partial v_{SD}} \right|_Q = \left(\frac{W}{2L} \right) \mu_p C_{ox} (V_{SG} + V_{Tp})^2 \lambda_p \cong \lambda_p (-I_D) \quad (4.92)$$

Finally, the capacitances associated with the p-channel MOSFET are identical to those of its complementary device. Figure 4.26 is the small-signal model for the p-channel MOSFET with the source located at the top, which is its most common orientation.

4.5.7 MOSFET Structures in CMOS Processes

The n- and p-channel MOSFETs can be made together in a Complementary MOS (CMOS) process. Having both types of MOSFETs available has important advantages for both digital and analog circuit design. Since the two devices need a bulk region with the opposite doping type, a CMOS process includes a deep well diffusion. Figure 4.27 shows the layout and a schematic cross section of an n-well CMOS process, in which the p-channel MOSFETs are fabricated in an n-type well in a p-type substrate. The opposite scheme, the p-well CMOS process, is less common.



► **Figure 4.27** (a) layout and (b) cross section of an n-well CMOS technology with isolated bulk regions for p-channel MOSFETs.

All n-channel MOSFETs share a common bulk region (the p-type substrate) in an n-well technology. Multiple contacts are made to the substrate, one of which is shown in Fig. 4.27, to ensure a low-resistance connection to ground. The IC designer has the option of placing a p-channel MOSFET in its own well so that its bulk (the n-well) can be shorted to its source, as shown in Fig. 4.27. Alternatively, a large number of p-channel devices can share a single n-well.

As we will see in Chapter 8, there are circuit performance advantages if the bulk and source contacts can be shorted. For this configuration, the backgate transconductance generator does not add to the small-signal drain current since $v_{BS} = 0$ V. In an n-well process, $V_{BS} = 0$ V only for those n-channel MOSFETs that have their sources grounded, since their shared bulk terminal must be grounded. Other n-channel devices will have their thresholds shifted by the backgate effect through Eq. (4.60) and must have the backgate generator included in their small-signal models. For the p-channel MOSFETs, on the other hand, we can arrange for $v_{BS} = 0$ for a particular device by placing it in its own n-well. There is an area penalty for placing a device in an isolated well, rather than having it share a well with many other p-channel MOSFETs. As a result, an IC designer will only isolate a device when it is necessary for performance reasons.

► 4.6 SPICE MODELS FOR THE MOSFET

MOSFETs can be simulated using models with varying levels of complexity in SPICE. In this text, we will use the simplest model, which is referred to as the “Level 1” model. This model corresponds closely with the large-signal and small-signal models that have been developed in this chapter. In this section, we will introduce the Level 1 MOSFET model and define the notation used in SPICE.

4.6.1 Level 1 DC Model

SPICE models the drain-source current I_{DS} of an n-channel MOSFET in the cutoff, triode, and saturation regions by:

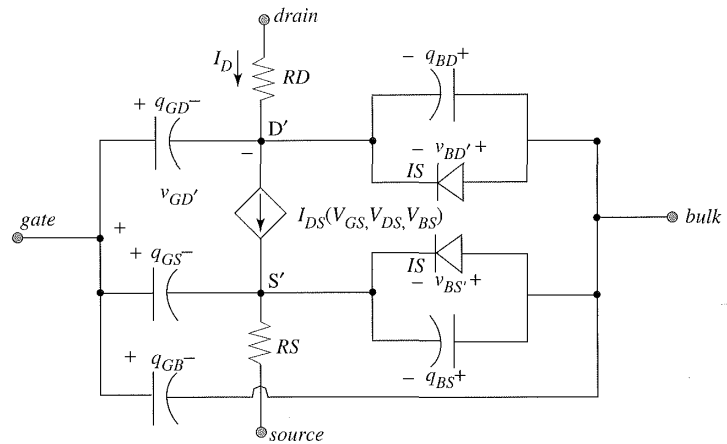
$$\begin{aligned} I_{DS} &= 0 & (V_{GS} \leq -V_{TH}) \\ I_{DS} &= \frac{KP}{2} (W/L_{eff}) V_{DS} [2(V_{GS} - V_{TH}) - V_{DS}] (1 + LAMBDA \cdot V_{DS}) & (0 \leq V_{DS} \leq V_{GS} - V_{TH}) \\ I_{DS} &= \frac{KP}{2} (W/L_{eff}) (V_{GS} - V_{TH})^2 (1 + LAMBDA \cdot V_{DS}) & (0 \leq V_{GS} - V_{TH} \leq V_{DS}) \end{aligned} \quad (4.93)$$

where the threshold voltage is given by

$$V_{TH} = V_{TO} + GAMMA (\sqrt{2 \cdot PHI} - \sqrt{V_{BS}} - \sqrt{2 \cdot PHI}) . \quad (4.94)$$

The SPICE parameter names correspond closely with the variables used in the analytical model developed in this chapter. In most cases, the SPICE parameter can be deduced from the symbol. However, the SPICE symbols for the channel length unfortunately conflict with the definitions in Fig. 4.18 and Eq. (4.61). The channel length in Eq. (4.93) is called L_{eff} in SPICE and is given by

$$L_{eff} = L - 2 \cdot LD , \quad (4.95)$$



► **Figure 4.28** SPICE large-signal model for an n-channel MOSFET, which includes nonlinear charge-storage between the gate and the other terminals and also in the drain and source depletion regions.

where L in SPICE is the length of the polysilicon gate and LD is the gate overlap of the source and drain.

Table 4.1 summarizes the DC SPICE parameter names and their equivalent analytical symbols and units, for the n-channel MOSFET. The elements in the large-signal MOSFET model are shown in Fig. 4.28.

4.6.2 Specifying MOSFET Geometry in SPICE

An n-channel MOSFET is defined by the following statement in SPICE:

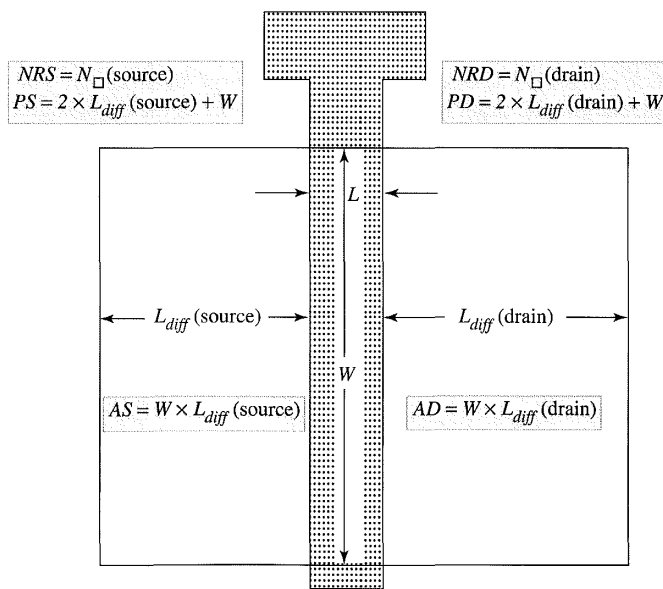
Mname D G S B MODname L= _W= _AD= _AS= _PD= _PS= _NRD= _NRS=

where *name* identifies the MOSFET with up to seven characters in SPICE2; D , G , S , and B are the drain, gate, source, and bulk node numbers, *MODname* is the model for the transistor, and the eight geometric parameters are defined in Fig. 4.29. The MOSFET in Fig. 4.29 has different diffusion widths for the source and the drain, which though unusual can be modeled in SPICE. The geometry parameters are:

- L = Polysilicon gate length,
- W = Polysilicon gate width,
- AD = Drain area,
- AS = Source area,
- PD = Perimeter of drain diffusion (not including the edge under the gate),
- PS = Perimeter of source diffusion (not including the edge under the gate),
- NRD = Equivalent number of squares in the drain diffusion, and
- NRS = Equivalent number of squares in the source diffusion.

■ **Table 4.1** n-Channel DC MOSFET SPICE parameters

Parameter Name (SPICE/this text)	SPICE Symbol Eqs. (4.93), (4.94)	Analytical Symbol Eqs. (4.59), (4.60)	Units
Channel length	L_{eff}	L	m
Polysilicon gate length	L	L_{gate}	m
Lateral diffusion/ gate-source overlap	LD	L_D	m
Transconductance parameter	KP	$\mu_n C_{ox}$	A/V ²
Threshold voltage / zero-bias threshold	VTO	V_{TO_n}	V
Channel-length modulation parameter	$LAMBDA$	λ_n	V ⁻¹
Bulk threshold/ backgate effect parameter	$GAMMA$	γ_n	V ^{1/2}
Surface potential/ depletion drop in inversion	PHI	$-\phi_p$	V



► **Figure 4.29** SPICE geometry parameters defined on the MOSFET layout.

Two-dimensional modeling (or curve-fitting to measurements) is needed to find the equivalent number of squares for the source and drain diffusions, which often have multiple contacts in order to minimize NRD and NRS (see the layout in Fig. 4.1, for example).

4.6.3 Level 1 Model Parameters

The MOSFET model statement in SPICE is

```
.MODEL MODname NMOS/PMOS VTO= KP= GAMMA= PHI=
LAMBDA= RD= RS= RSH= CBD= CBS= CJ= MJ= CJSW=
MJSW= PB= IS= CGDO= CGSO= CGBO= TOX= LD=
```

The MOSFET model must be specified as n-channel (**NMOS**) or p-channel (**PMOS**). The model parameters that have not been already defined in the DC drain current model Eqs. (4.93) and (4.94) are defined in this section.

The gate oxide thickness $t_{ox} = TOX$. When this parameter is specified, SPICE models the gate-source and gate-drain charge storage in cutoff, triode, and saturation. A cruder approximation for these capacitances is used if TOX is not specified. The capacitances $CGDO$, $CGSO$, and $CGBO$ describe the overlap capacitances of the gate with the drain, source, and bulk. The units for all three parameters are F/m, with $CGDO$ and $CGSO$ scaling with the channel width W , while $CGBO$ scales with the channel length L .

The resistance of the source and drain diffusions and their contacts can be described by directly specifying them or by giving their sheet resistance:

RD = Drain resistance (Ω)

RS = Source resistance (Ω)

RSH = Sheet resistance of the drain and source diffusions (NRD and NRS must be specified on the MOSFET statement) ($\Omega/\square$)

SPICE includes a model for the pn diode at both the drain and the source. IS is the saturation current of the diode. As shown in the large-signal circuit model in Fig. 4.28, the current into the drain terminal is the difference of the drain-source current I_{DS} and the diode current from the substrate. In normal operation, the diode is reverse biased and $I_D = I_{DS}$.

The final set of parameters concern the modeling of charge storage in the drain-bulk and source-bulk depletion regions. Again, SPICE allows alternative ways to specify the depletion capacitances. By specifying the parameters CBD , CBS , PB , and MJ , SPICE computes the voltage dependences of the drain-bulk and source-bulk capacitances:

$$C_{BD}(V_{BD}) = \frac{CBD}{(1 - V_{BD}/PB)^{MJ}} \quad (4.96)$$

$$C_{BS}(V_{BS}) = \frac{CBS}{(1 - V_{BS}/PB)^{MJ}} \quad (4.97)$$

CBD = Zero-bias drain-bulk junction capacitance (F)

CBS = Zero-bias source-bulk junction capacitance (F)

PB = Built-in potential for the bulk junction (V)
 MJ = Bulk junction grading coefficient (dimensionless)

A more accurate simulation of these important capacitances incorporates both the planar junction capacitance and the perimeter, or sidewall, capacitance. If the parameters CJ , $CJSW$, MJ , $MJSW$, and PB are included, SPICE computes the drain-bulk and source-bulk capacitances as follows:

$$C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}} \quad (4.98)$$

$$C_{BS}(V_{BS}) = \frac{CJ \cdot AS}{(1 - V_{BS}/PB)^{MJ}} + \frac{CJSW \cdot PS}{(1 - V_{BS}/PB)^{MJSW}} \quad (4.99)$$

CJ = Zero-bias planar bulk junction capacitance (F/m²)
 $CJSW$ = Zero-bias sidewall bulk junction capacitance (F/m)
 $MJSW$ = Sidewall junction grading coefficient (dimensionless)

The SPICE small-signal n-channel MOSFET model is identical to Fig. 4.24, except for the addition of the drain and source resistances RS and RD .

Example Level 1 SPICE Models for an n-well

4.6.4 CMOS Technology

It is convenient to define “standard” SPICE models for the n-channel and p-channel MOSFETs in an n-well CMOS technology. These models can then be used throughout the text for simulating both digital and analog circuits. With the exception of the additional capacitance due to the sidewalls of the source and drain diffusions, the device parameters are similar to those derived for the n-channel MOSFET in Ex. 4.5.

For these models, we assume that the lateral diffusion $LD = L_D = 0 \mu\text{m}$, to avoid confusion in specifying the channel length. The Level 1 models are not so accurate that the omission of L_D will make a significant difference, in any case. The length of the source and drain diffusions is $L_{diff} = 6 \mu\text{m}$. Therefore, the drain and source areas and perimeters are given by

$$AD = AS = L_{diff} \cdot W = (6 \cdot W) \times 10^{-12} \text{ m}^2 \text{ and} \quad (4.100)$$

$$PD = PS = 2L_{diff} + W = (12 + W) \times 10^{-6} \text{ m}, \quad (4.101)$$

where W is in μm .

The gate-bulk overlap capacitance will be neglected by letting $CGBO = 0 \text{ F/m}$ (the default value in SPICE). Finally, the source and drain resistances are small and will be omitted by letting $RD = RS = 0 \Omega$.

Table 4.2 describes the MOSFET parameters for the example n-well process.

■ **Table 4.2** n-well CMOS Level 1 SPICE Models.

Level 1 SPICE Parameter	n-channel MOSFET	p-channel MOSFET	Units
Gate oxide thickness <i>TOX</i>	150	150	Å
Transconductance parameter <i>KP</i>	50×10^{-6}	25×10^{-6}	A/V ²
Threshold voltage <i>VTO</i>	1.0	-1.0	V
Channel-length modulation parameter <i>LAMBDA</i>	0.1/ <i>L</i> <i>L</i> in μm	0.1/ <i>L</i> <i>L</i> in μm	V ⁻¹
Bulk threshold parameter <i>GAMMA</i>	0.6	0.6	V ^{1/2}
Surface potential <i>PHI</i>	0.8	0.8	V
Gate-drain overlap capacitance <i>CGDO</i>	5×10^{-10}	5×10^{-10}	F/m
Gate-source overlap capacitance <i>CGSO</i>	5×10^{-10}	5×10^{-10}	F/m
Zero-bias planar bulk depletion capacitance <i>CJ</i>	10^{-4}	3×10^{-4}	F/m ²
Zero-bias sidewall bulk depletion capacitance <i>CJSW</i>	5×10^{-10}	3.5×10^{-10}	F/m
Bulk junction potential <i>PB</i>	0.95	0.95	V
Planar bulk junction grading coefficient <i>MJ</i>	0.5	0.5	[]
Sidewall bulk junction grading coefficient <i>MJSW</i>	0.33	0.33	[]

For n-channel and p-channel MOSFETs with $L = 3 \mu\text{m}$, the parameters in Table 4.2 lead to the following model statements:

```
.MODEL MODN NMOS LEVEL = 1 VTO = 1 KP = 50U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 1E-4 CJSW = 5E-10
+ MJ = 0.5 PB = 0.95
```

```
.MODEL MODP PMOS LEVEL = 1 VTO = -1 KP = 25U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E-10 CGDO = 5E-10 CGSO = 5E-10 CJ = 3E-4 CJSW = 3.5E-10
+ MJ = 0.5 PB = 0.95
```

An n-channel MOSFET M_1 with $W = 150 \mu\text{m}$ and $L = 3 \mu\text{m}$ has source and drain areas and perimeters that are found from Eqs. (4.100) and (4.101)

$$AD = AS = 9 \times 10^{-10} \text{ m}^2 \text{ and } PD = PS = 1.62 \times 10^{-4} \text{ m}$$

Transistor M_1 is specified in SPICE by

M1 4 3 2 1 MODN W = 150U L = 3U AD = 9E-10 AS = 9E-10 PD = 1.62E-4 PS = 1.62E-4

where the drain is node 4, the gate is node 3, the source is node 2, and the bulk is node 1.

► SUMMARY

This chapter has covered the device physics and device modeling of the MOS field-effect transistor, which is by far the most important microelectronic device. It is essential that you grasped the basic device operation and the large- and small-signal models, since the MOSFET will be used in digital and analog circuits throughout this text. Also, a good understanding of the circuit models for the MOSFET will be helpful in learning how to model the other important multi-terminal device—the bipolar junction transistor.

The most important topics in Chapter 4 are:

- ◆ The piecewise modeling of the n-channel and p-channel MOSFETs in the three regions of operation: cutoff, triode, and saturation.
- ◆ The relationship between drain current, channel charge, and drift velocity.
- ◆ The key assumption behind the gradual channel approximation.
- ◆ The channel electron charge variation from source to drain in the triode region, neglecting the body effect.
- ◆ The concept of saturation.
- ◆ The backgate effect on the threshold voltage of the MOSFET.
- ◆ MOSFET capacitances in the three regions of operation.
- ◆ Small-signal models for the n-channel and the p-channel MOSFETs.
- ◆ The Level 1 SPICE model for the MOSFET.

► FURTHER READING

MOSFET Device Structures

1. W. Maly, *Atlas of VLSI Technologies*, Addison-Wesley, 1986. Has layouts for simple MOS circuits in several technologies.

MOSFET Device Physics

1. R. F. Pierret, *Field Effect Devices*, Modular Series on Solid State Devices, Vol. IV, R. F. Pierret and G. W. Neudeck, eds., Addison-Wesley, 1983, Chapter 5 has a good discussion of the MOSFET at slightly more advanced level.
2. R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed., Wiley, 1986. Chapter 9 has a good description of basic MOSFET operation; derivations use energy bands rather than potential.

MOSFET SPICE Models

1. A. Vladimirescu, *The SPICE Book*, Wiley, 1994. Chapter 3 has a complete description of the Level 1 model; selected examples of the more advanced MOSFET models are detailed in an appendix.

► PROBLEMS

EXERCISES

Unless stated otherwise, use the following parameters in the exercises and problems.

n-channel MOSFET

$$\begin{aligned}\mu_n C_{ox} &= 50 \mu\text{A/V}^2 \\ V_{TOn} &= 1.0 \text{ V} \\ \gamma_n &= 0.6 \text{ V}^{1/2} \\ \lambda_n &= (0.1/L) \text{ V}^{-1}, L \text{ in } \mu\text{m} \\ \phi_p &= -0.42 \text{ V}\end{aligned}$$

p-channel MOSFET

$$\begin{aligned}\mu_p C_{ox} &= 25 \mu\text{A/V}^2 \\ V_{TOp} &= -1.0 \text{ V} \\ \gamma_p &= 0.6 \text{ V}^{1/2} \\ \lambda_p &= (0.1/L) \text{ V}^{-1}, L \text{ in } \mu\text{m} \\ \phi_n &= 0.42 \text{ V}\end{aligned}$$

E4.1 For the n-channel MOSFET with terminal voltages in Fig. E4.1, determine (a) the operating region (cutoff, triode, or saturation) and (b) the drain current I_D .

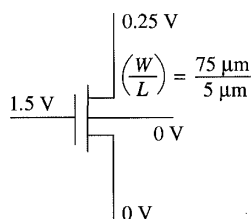
E4.2 Repeat E4.1 for the terminal voltages in Fig. E4.2.

E4.3 Repeat E4.1 for the terminal voltages in Fig. E4.3.

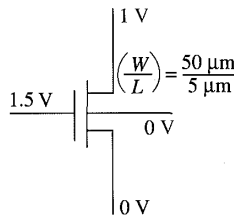
E4.4 For the n-channel MOSFET with terminal voltages in Fig. E4.4, determine (a) the operating region (cutoff, triode, or saturation) and (b) the drain current I_D . Note that the bulk-source voltage V_{BS} is *not* zero.

E4.5 Repeat E4.4 for the terminal voltages in Fig. E4.5.

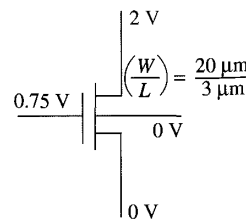
E4.6 Repeat E4.4 for the terminal voltages in Fig. E4.6.



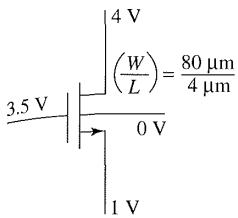
► Figure E4.1



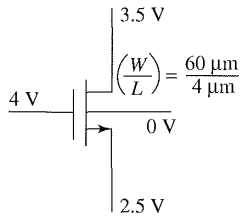
► Figure E4.2



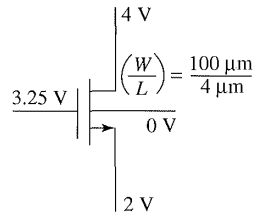
► Figure E4.3



► Figure E4.4



► Figure E4.5



► Figure E4.6

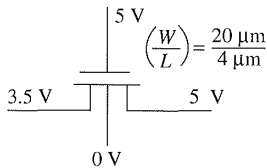
E4.7 For the n-channel MOSFET with terminal voltages in Fig. E4.7, (a) label the source and the drain terminals, (b) determine in which region the transistor is operating (cutoff, triode, or saturation), and (c) find the drain current I_D .

E4.8 Repeat E4.7 for the terminal voltages in Fig. E4.8.

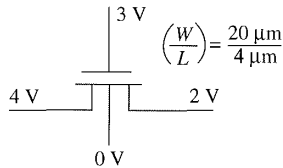
E4.9 For the p-channel MOSFET with terminal voltages in Fig. E4.9, determine (a) the operating region (cutoff, triode, or saturation) and (b) the drain current $-I_D$.

E4.10 Repeat E4.9 for the terminal voltages in Fig. E4.10.

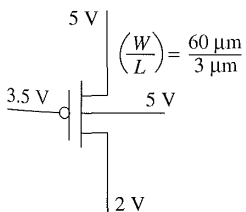
E4.11 Repeat E4.9 for the terminal voltages in Fig. E4.11.



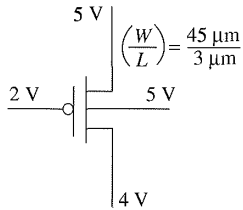
► Figure E4.7



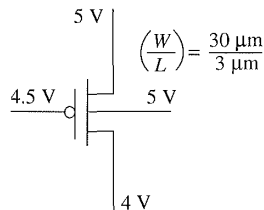
► Figure E4.8



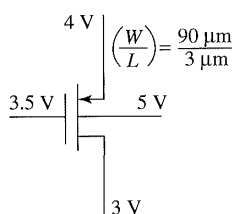
► Figure E4.9



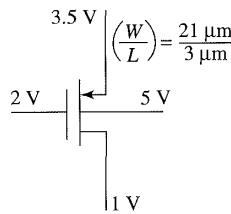
► Figure E4.10



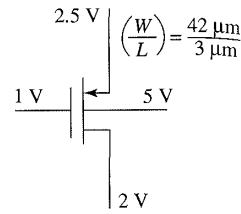
► Figure E4.11



► Figure E4.12



► Figure E4.13



► Figure E4.14

E4.12 For the p-channel MOSFET with terminal voltages in Fig. E4.12, determine (a) the operating region (cutoff, triode, or saturation) and (b) the drain current $-I_D$. Note that the source-bulk voltage V_{SB} is *not* zero.

E4.13 Repeat E4.12 for the terminal voltages in Fig. E4.13.

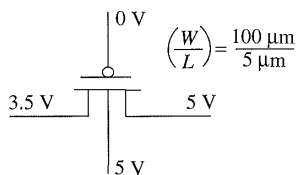
E4.14 Repeat E4.12 for the terminal voltages in Fig. E4.14.

E4.15 For the p-channel MOSFET with terminal voltages in Fig. E4.15, (a) label the source and the drain terminals, (b) determine in which region the transistor is operating (cutoff, triode, or saturation), and (c) find the drain current I_D .

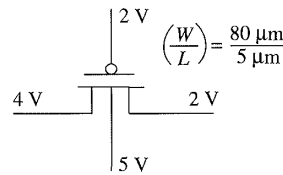
E4.16 Repeat E4.15 for the terminal voltages in Fig. E4.16.

E4.17 Consider an n-channel MOSFET with $(W/L) = 25 \mu\text{m}/2.5 \mu\text{m}$.

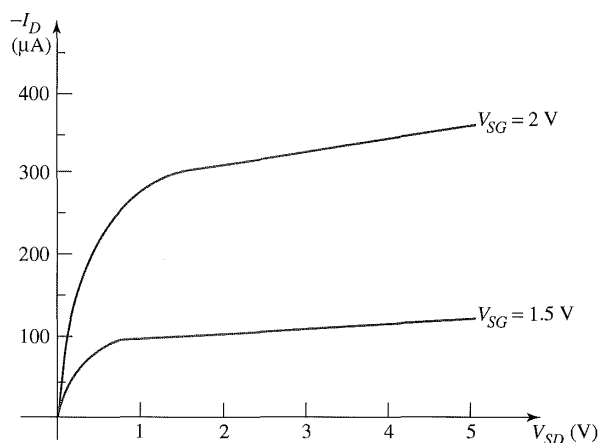
- Plot the drain current I_D versus V_{GS} for $V_{DS} = 250 \text{ mV}$ and $V_{BS} = 0$. Note that the threshold voltage can be found from this plot of the MOSFET in the triode region.
- Plot the square root of drain current $(I_D)^{1/2}$ versus V_{GS} for $V_{DS} = 5 \text{ V}$ and $V_{BS} = 0$. The threshold voltage can also be extracted from this plot of the MOSFET in the saturation region. Due to second-order effects, the measurement will differ somewhat from the threshold found in the triode region in part (a).



► Figure E4.15



► Figure E4.16



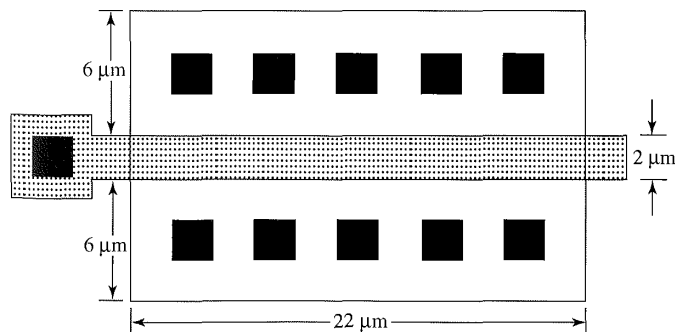
► Figure E4.18

E4.18 Figure E4.18 is a plot of two drain characteristics of a p-channel MOSFET, for $V_{BS} = 0$.

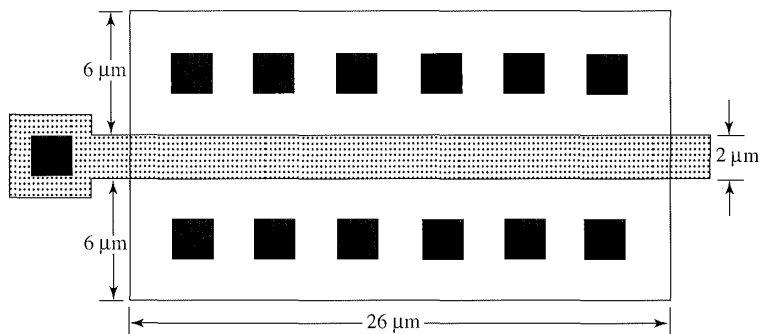
- From these measurements, what is the threshold voltage, V_{Tp} ?
- Estimate the channel-length modulation parameter, λ_p .

E4.19 The n-channel MOSFET shown in layout in Fig. E4.19 is biased at the operating point: $V_{GS} = 3.5$ V, $V_{DS} = 5$ V, $V_{BS} = -1$ V. For this problem, include $L_D = 0.1$ μm in finding the channel length L from the layout and let $C_{ox} = 1.42$ fF/ μm^2 .

- Find the small-signal parameters g_m , g_{mb} , and r_o at this operating point.
- Find the capacitances C_{gs} , C_{gd} , C_{db} , and C_{sb} . In calculating the overlap capacitances, only consider the under-diffusion of the drain and source



► Figure E4.19



► Figure E4.20

diffusions by L_D . Also, you can neglect the sidewall capacitance and use a substrate doping $N_a = 10^{17} \text{ cm}^{-3}$.

E4.20 The p-channel MOSFET shown in layout in Fig. E4.20 is biased at the operating point: $V_{SG} = 1.5 \text{ V}$, $V_{SD} = 4 \text{ V}$, $V_{SB} = -2 \text{ V}$. For this problem, include $L_D = 0.1 \mu\text{m}$ in finding the channel length L from the layout and let $C_{ox} = 1.42 \text{ fF}/\mu\text{m}^2$.

- Find the small-signal parameters g_m , g_{mb} , and r_o at this operating point.
- Find the capacitances C_{gs} , C_{gd} , C_{db} , and C_{sb} . In calculating the overlap capacitances, only consider the under-diffusion of the drain and source diffusions by L_D . Also, you can neglect the sidewall capacitance and use a substrate doping $N_a = 10^{17} \text{ cm}^{-3}$.

E4.21 A p-channel MOSFET has $W/L = 500 \mu\text{m}/2.5 \mu\text{m}$. The source and drain diffusions have a length $L_{diff} = 6 \mu\text{m}$. The operating point is: $V_{SG} = 2.5 \text{ V}$, $V_{SD} = 4 \text{ V}$, $V_{SB} = 0 \text{ V}$. For this problem, let $L_D = 0.1 \mu\text{m}$ and $C_{ox} = 1.42 \text{ fF}/\mu\text{m}^2$.

- Find the small-signal parameters g_m , g_{mb} , and r_o at this operating point.
- Find the capacitances C_{gs} , C_{gd} , C_{db} , and C_{sb} . In calculating the overlap capacitances, only consider the under-diffusion of the drain and source diffusions by L_D . Also, you can neglect the sidewall capacitance and use a substrate doping $N_a = 10^{17} \text{ cm}^{-3}$.

E4.22 An n-channel MOSFET with $(W/L) = 20 \mu\text{m}/3 \mu\text{m}$ is biased at $V_{GS} = 2 \text{ V}$, $V_{DS} = 3.5 \text{ V}$, and $V_{BS} = 0 \text{ V}$. A small signal $v_{gs}(t) = 20 \text{ mV} \cos(2\pi 1000 t)$ is added in series with V_{GS} .

- Find the DC drain current I_D .
- Find the small-signal drain current $i_d(t)$.
- Plot the total current $i_D(t)$ from your answers in (a) and (b).

E4.23 In a particular CMOS process, the gate oxide thickness is $t_{ox} = 150 \text{ \AA} \pm 20 \text{ \AA}$ and the substrate doping is $N_a = 8 \times 10^{16} \text{ cm}^{-3} \pm 10^{16} \text{ cm}^{-3}$. Using this process, we bias an n-channel MOSFET with dimensions $W = 100 \mu\text{m}$ and $L = 2.5 \mu\text{m}$ at the operating point: $V_{GS} = 3 \text{ V}$, $V_{DS} = 4 \text{ V}$, and $V_{BS} = -1.5 \text{ V}$.

- What is the average threshold voltage and its uncertainty?
- What is the DC drain current I_D and its uncertainty at this operating point?
- What is the transconductance and its uncertainty at this operating point?
- What is the backgate transconductance and its uncertainty at this operating point?

PROBLEMS

P4.1 Figure P4.1 plots the drain current I_D of an n-channel MOSFET as a function of the gate-source voltage V_{GS} , for a drain-source voltage $V_{DS} = 10$ mV and at three values of backgate bias V_{BS} . From the layout, you also know that $W/L = 10$.

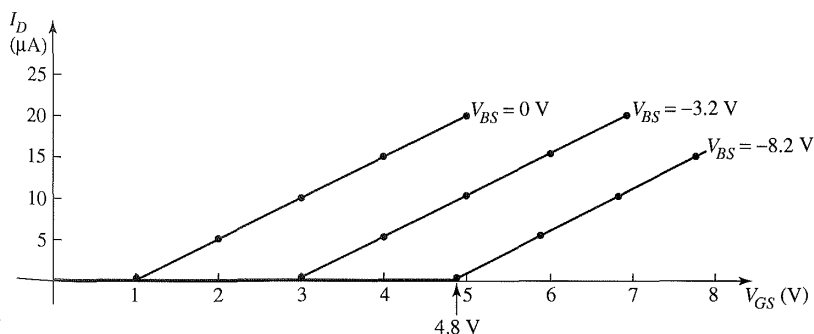
- Extract the following device parameters from these measurements: the substrate doping concentration N_a , the oxide thickness t_{ox} , and the channel mobility μ_n .
- Estimate the uncertainty in your parameters, given that the current measurements have an uncertainty of ± 1 μ A.

P4.2 In a particular CMOS technology, the substrate doping is $N_a = 4 \times 10^{17}$ cm⁻³, the gate oxide is $t_{ox} = 150$ Å, and n⁺ polysilicon is used for the gate.

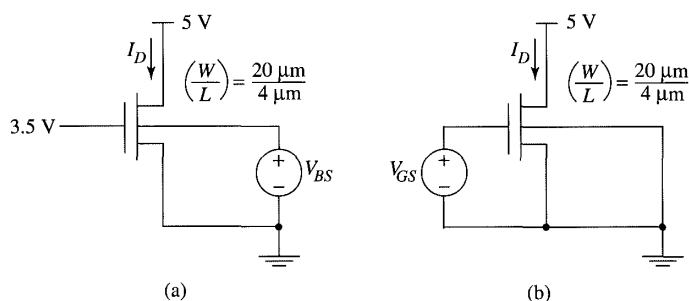
- Calculate the surface potential ϕ_{so} in thermal equilibrium.
- Calculate the threshold voltage V_{TOn} .
- If we require $V_{TOn} = 0.7$ V, what oxide thickness is required?
- If the oxide thickness couldn't be changed, what must the substrate doping concentration become in order to achieve $V_{TOn} = 0.7$ V.

P4.3 In a particular CMOS technology, the n-well doping is $N_d = 2.5 \times 10^{17}$ cm⁻³, the gate oxide is $t_{ox} = 200$ Å, and n⁺ polysilicon is used for the gate.

- Calculate the surface potential ϕ_{so} in thermal equilibrium.
- Calculate the threshold voltage V_{TOP} .
- If we require $V_{TOP} = -1.5$ V, what oxide thickness is required?



► **Figure P4.1**



► Figure P4.6

- (d) If the oxide thickness couldn't be changed, what must the substrate doping concentration become in order to achieve $V_{TOP} = -1.5$ V.

P4.4 In a particular CMOS technology, the n-well doping is $N_d = 2.5 \times 10^{17} \text{ cm}^{-3}$, the gate oxide is $t_{ox} = 200 \text{ \AA}$, and p^+ polysilicon is used for the gate. The thermal-equilibrium potential of p^+ polysilicon is $\phi_{p+} = -550 \text{ mV}$.

- Calculate the surface potential ϕ_{so} in thermal equilibrium.
- Calculate the threshold voltage V_{TOP} .
- If we require $V_{TOP} = -0.7$ V, what oxide thickness is required?
- If the oxide thickness couldn't be changed, what must the substrate doping concentration become in order to achieve $V_{TOP} = 0.7$ V.

P4.5 Silicon nitride (Si_3N_4 , $\epsilon_n = 6.64 \times 10^{13} \text{ F/cm}$) is a potential replacement for silicon dioxide as a gate insulator material. Assume the same operating point and transistor dimensions as used in Ex. 4.5.

- What thickness of Si_3N_4 is needed for $V_{TON} = 0.6$ V, if the substrate doping is $N_a = 10^{17} \text{ cm}^{-3}$?
- Find the backgate effect parameter, γ_n for the silicon nitride gate insulator thickness from (a).
- Find the transconductance, backgate transconductance, and output resistance at the operating point and compare with the values for an SiO_2 from Ex. 4.5.
- Find the MOSFET capacitances and compare to those for the SiO_2 gate.

P4.6 Figure P4.6(a) shows an n-channel MOSFET with $V_{GS} = 3.5$ V and $V_{DS} = 5$ V with a variable bulk-source voltage V_{BS} . Figure P4.6(b) shows an n-channel MOSFET with $V_{BS} = 0$ V and $V_{DS} = 5$ V with a variable gate-source voltage V_{GS} .

- Plot the drain current as a function of V_{BS} for the circuit in Fig. P4.6(a), over the range $-5 \text{ V} < V_{BS} < 0$.
- Plot the drain current as a function of V_{GS} for the circuit in Fig. P4.6(b), over the range $0 \text{ V} < V_{GS} < 5 \text{ V}$.

P4.7 This problem uses the results of P4.6 to extract small-signal parameters.

- From the $I_D(V_{BS})$ plot in P4.6(a), find graphically the backgate transconductance g_{mb} at the operating point $V_{GS} = 3.5$ V, $V_{DS} = 5$ V, $V_{BS} = -2$ V. Compare with the value you calculate from the analytical expression.
- From the plot of $I_D(V_{GS})$ in P4.6(b), find graphically the transconductance g_m at the operating point $V_{GS} = 3.5$ V, $V_{DS} = 5$ V, $V_{BS} = 0$ V. Again, compare your result with the analytical expression.

P4.8 A large-value, voltage-controlled resistor is useful in some analog ICs. Using the standard parameters, design a p-channel MOSFET with a resistance of $R = 1$ M Ω for $V_{GS} = 1.5$ V.

- What are the required channel width and length?
- Find the capacitance between the channel and the gate and between the channel and the substrate. Assume that the source and drain diffusion lengths are $L_{diff} = 6$ μ m. Note that the device is operating in the triode region for use as a voltage-controlled resistor.
- Model the transistor as a low-pass filter and find the break (-3 dB) frequency.

P4.9 For the case of a p-channel MOSFET, apply the gradual channel approximation. Assume $C_{ox} = 1.42$ fF/ μ m², $V_{FB} = 1$ V, and $V_{TP} = -1$ V.

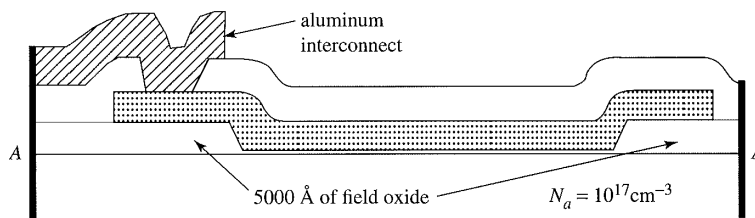
- Find the channel voltage $V_C(y)$ between the source and drain, assuming that $V_{SD} \leq V_{SG} + V_{Tp}$.
- Find the lateral electric field $E_y(y)$ between the source and drain for $V_{SD} \leq V_{SG} + V_{Tp}$.
- Find the vertical electric field $E_x(y)$ at the silicon surface ($x = 0$) between the source and drain for $V_{SD} \leq V_{SG} + V_{Tp}$.
- For $V_{SD} = (3/4)(V_{SG} + V_{Tp})$ plot the ratio E_y/E_x between the source and the drain.

P4.10 In the gradual-channel approximation, we found Eq. (4.36) prior to eliminating the variation of the bulk charge.

- Starting with Eq. (4.36), separate variables and find a new triode region equation for the drain current as a function of V_{GS} and V_{DS} . You can assume that $V_{BS} = 0$.
- What is the saturation drain current, from the triode equation in (a)?
- For $W/L = 25$ μ m/ 2.5 μ m, plot the drain characteristics for $V_{GS} = 1.5$ V, 2 V, 3 V, and 4 V over the range $0 < V_{DS} < 5$ V using your results from (a) and (b). In saturation, you can use the factor $(1 + \lambda_n V_{DS})$ in modeling channel-length modulation. On the same graph, plot Eqs. (4.59) and compare, using $N_a = 10^{17}$ cm⁻³, $C_{ox} = 1.42$ fF/ μ m², and standard Level 1 SPICE parameters.

P4.11 For this problem, use the approach used to derive Eq. (4.80) for the channel-charge in saturation.

- Find an expression for the channel charge in the triode region, $q_N(v_{GS}, v_{DS})$.
- From your result in (a), find expressions for the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} in the triode region. Omit the overlap capacitance.



► Figure P4.13

- (c) Plot the gate-source capacitance as a function of V_{DS} over the range 0 to $V_{GS} - V_{Tn}$. Show that the triode result converges with the saturation expression for C_{gs} at $V_{DS} = V_{GS} - V_{Tn}$.

P4.12 This problem concerns itself with the question of how small a “small signal” must be for the linearized model to be adequate. Consider an n-channel MOSFET with width-to-length ratio of $25\ \mu\text{m}/5\ \mu\text{m}$ biased at $V_{GS} = 2.5\ \text{V}$, $V_{DS} = 4\ \text{V}$, and $V_{BS} = 0\ \text{V}$.

- Find the DC drain current I_D and the transconductance g_m .
- Expand the expression for the total drain current in a power series, retaining only the DC, linear, and quadratic terms.
- The small-signal model neglects the quadratic term. For a particular application, we can only tolerate a quadratic term that is 5% of the linear term. How large is the “small-signal” v_{gs} that meets this requirement, for the given bias condition?

P4.13 For the layout in Fig. E4.19, the polysilicon gate overlaps thick (field) oxide on both sides of the channel, as shown in cross section AA in Fig. P4.13. The field oxide thickness is $t_{fox} = 5000\ \text{\AA}$. The substrate is doped at $N_a = 10^{17}\ \text{cm}^{-3}$ in the field region. The n-channel MOSFET is biased at $V_{GS} = 2.5\ \text{V}$, $V_{DS} = 4\ \text{V}$, and $V_{BS} = 0\ \text{V}$.

- What is the threshold voltage of the gate-bulk capacitor?
- Find the gate-bulk capacitor C_{gb} at the given operating point. Note that there is an overlap area at both ends of the gate. You will need to apply the MOS capacitor theory from Chapter 3.
- Sketch the gate-bulk capacitance as a function of the bulk-source bias V_{BS} over the range $-5 < V_{BS} < 0$.

P4.14 The field oxide thickness in a CMOS process (see Fig. 4.27) must be thick enough so that neither the p substrate nor the n-type well inverts under the extensions of the n^+ polysilicon gate. Assume that we have a case of symmetrical doping ($N_a = 10^{17}\ \text{cm}^{-3} = N_d$) in the field regions for the substrate and the well.

- What field oxide thickness is needed to have the field threshold voltage equal to $V_{Tnf} = 4\ \text{V}$ for the substrate?
- What field oxide thickness is needed to have the field threshold voltage equal to $V_{Tpf} = -4\ \text{V}$ for the n-well?

P4.15 In a CMOS process it is sometimes desirable to match, as much as possible, the circuit models of the n-channel and the p-channel MOSFETs. Assume that both devices have channel lengths of $L_n = L_p = 2\text{ }\mu\text{m}$ and that the n-channel MOSFET has a channel width $W_n = 20\text{ }\mu\text{m}$.

- In order to have identical saturation currents for the same gate-source drive ($V_{GS} = V_{SG}$), what is the width of the p-channel transistor?
- Given the dimensions from (a), lay out both devices assuming $L_{diff} = 6\text{ }\mu\text{m}$.
- Derive all the small-signal parameters (including capacitances) for the n-channel and the p-channel transistors.

P4.16 In some cases, it is helpful to have a small-signal model for the MOSFET in the triode region. Using Eq. (4.59) for the triode region.

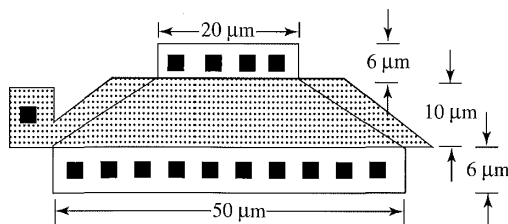
- Find the transconductance g_m as a function of operating point in the triode region.
- Find the output resistance r_o as a function of operating point in the triode region.
- Plot the output conductance g_o as a function of V_{DS} and show that it approaches its saturation value at $V_{DS} = V_{GS} - V_{Th}$.

P4.17 Figure P4.17 shows the layout of an n-channel MOSFET, in which the channel width tapers from $W_s = 50\text{ }\mu\text{m}$ at the source to $W_d = 20\text{ }\mu\text{m}$ at the drain. The channel length is $L = 10\text{ }\mu\text{m}$.

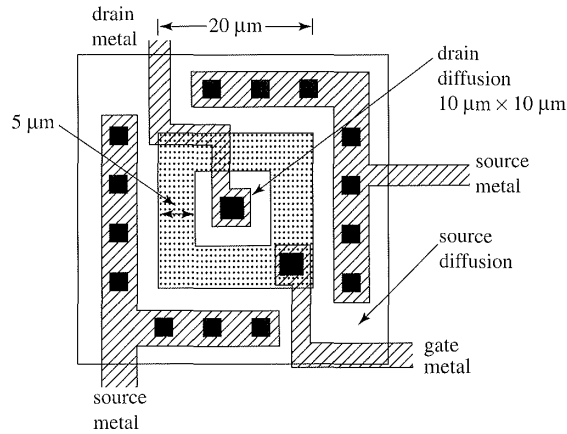
- Adapt the gradual channel approximation in Eq. (4.36) to this new geometry and find an expression for the drain current in the triode region.
- What is the effective channel width W_{eff} for this MOSFET?
- Find the gate-drain and drain-bulk capacitances for this layout and compare to those for a standard MOSFET with $W = W_{eff}$. The overlap capacitance between gate and drain is $C_{gdo} = 0.5\text{ fF}/\mu\text{m}$ and the operating point is $V_{GS} = 2\text{ V}$, $V_{DS} = 4\text{ V}$, and $V_{BS} = 0\text{ V}$.

P4.18 Figure P4.18 is a square MOSFET layout, which is an approach that is sometimes used to minimize the drain capacitance.

- Derive an approximate equation for the saturation drain current for this n-channel MOSFET. What is an estimate of the effective gate width W_{eff} ? *Hint:* consider the role of the corners.



► Figure P4.17



► Figure P4.18

- (b) Find the gate-drain and drain-bulk capacitances for this layout and compare to those for a standard MOSFET with $W = W_{eff}$. The overlap capacitance between gate and drain is $C_{gdo} = 0.5 \text{ fF}/\mu\text{m}$ and the operating point is $V_{GS} = 2 \text{ V}$, $V_{DS} = 3 \text{ V}$, and $V_{BS} = 0 \text{ V}$. The CVD SiO_2 thickness is $5000 \text{ \AA}$, which is needed to find C_{gd} .

DESIGN PROBLEMS

D4.1 MOSFETs are useful as switches in power supplies. For this application, the *on resistance* of the transistor is a critical parameter. In this problem, the goal is to design an n-channel MOSFET to satisfy:

$$R_{on} = 0.01 \Omega \text{ for } V_{GS} = 5 \text{ V}$$

Given that the maximum oxide field is $E_{ox,max} = 3 \times 10^6 \text{ V/cm}$ and that we limit the average lateral field in the channel to at most $(1/200)$ of the vertical field in the channel. The electron mobility in the channel is a function of the vertical field in the silicon $E_x(x=0)$:

$$\mu_n = \frac{\mu_{no}}{1 + \Theta E_x(0)} = \frac{215 \text{ cm}^2/\text{Vs}}{1 + (2 \times 10^{-6} \text{ cm/V}) E_x(0)}$$

The substrate doping is fixed at $N_a = 10^{16} \text{ cm}^{-3}$. The drain current should be linear with the drain-source voltage up to $V_{DS} = 500 \text{ mV}$, which is why there is a restriction on the lateral electric field in the channel. Note that the peak drain current for linear operation is $V_{DS}/R_{on} = 500 \text{ mV}/100 \text{ m}\Omega = 5 \text{ A}$!

- Find a combination of oxide thickness t_{ox} , channel length L , and (W/L) ratio that meet the specifications. You should try to minimize L by using the maximum possible channel electric fields.
- This huge transistor is best laid out as 10 MOSFETs in parallel, each one of which is folded to make a more compact IC structure. Assuming that the source and drain diffusions have a length $L_{diff} = 6 \mu\text{m}$, what is the area required by each of the 10 MOSFETs? Draw the layout of one of