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CMOS DIGITAL INTEGRATED CIRCUITS: ANALYSIS AND DESIGN
THIRD EDITION

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The amount of the critical charge drop in the soft node, which will eventually cause a change of logic state, is

$$\begin{aligned}\Delta Q_{critical} &= C_{x,min} \cdot \left(V_{x,max} - \frac{V_{DD}}{2}\right) \\ &= 8.55\ \text{fF} \cdot (3.68\ \text{V} - 2.5\ \text{V}) \\ &= 10.09\ \text{fC}\end{aligned}$$

assuming that the logic threshold voltage of the next gate is $(V_{DD}/2)$. In this example, the maximum leakage current responsible for charge depletion is given from the MOS characteristics (cf. equation (3.92) in Chapter 3) and the junction diode characteristics as

$$I_{leakage} = I_{subthreshold} + I_{reverse} = 0.85\ \text{pA}$$

Finally, we calculate the worst-case (minimum) hold time for the soft node using the expression (9.22).

$$\begin{aligned}t_{hold,min} &= \frac{\Delta Q_{critical}}{I_{leakage,max}} \\ &= \frac{10.09\ \text{fC}}{0.85\ \text{pA}} = \underline{\underline{11.87\ \text{ms}}}\end{aligned}$$

It is interesting to note that even with a very small soft-node capacitance of 8.55 fF, the worst-case hold time for this structure is relatively long, especially compared with the signal propagation delays encountered in nMOS or CMOS logic gates. This example proves the feasibility of the dynamic charge storage concept and shows that a logic state can be preserved in a soft node for a long time period when the leakage current is small.

9.3 Voltage Bootstrapping

In this section, we will briefly examine a very useful dynamic circuit technique for overcoming threshold voltage drops in digital circuits, which is called *voltage bootstrapping*. We have already seen that output voltage levels may suffer from threshold voltage drops in several circuit structures, such as pass transistor gates or enhancement-load inverters and logic gates.

Dynamic voltage bootstrapping techniques offer a simple yet effective way to overcome threshold voltage drops which occur in most situations. Consider the circuit shown in Fig. 9.11, where the voltage V_x is equal to or smaller than the power supply voltage, $V_x \leq V_{DD}$. Consequently, the enhancement-type nMOS transistor M2 will operate in saturation.

When the input voltage V_{in} is low, the maximum value that the output voltage can attain is limited by

$$V_{out}(max) = V_x - V_{T2}(V_{out}) \tag{9.24}$$

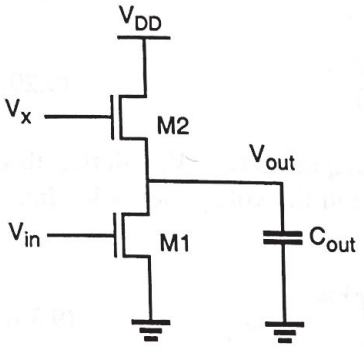


Figure 9.11 Enhancement-type circuit in which the output node is weakly driven.

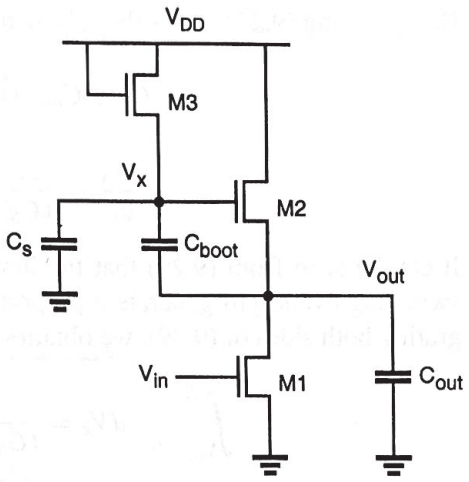


Figure 9.12 Dynamic bootstrapping arrangement to boost V_x during switching.

To overcome the threshold voltage drop and to obtain a full logic-high level (V_{DD}) at the output node, the voltage V_x must be increased. Now consider the circuit shown in Fig. 9.12, where a third transistor M3 has been added to the circuit. The two capacitors C_S and C_{boot} seen in the circuit diagram represent the capacitances which dynamically couple the voltage V_x to the ground and to the output, respectively. We will see that this circuit can produce a high V_x during switching, so that the threshold voltage drop can be overcome at the output node.

$$V_x \geq V_{DD} + V_{T2}(V_{out}) \tag{9.25}$$

Initially assume that the input voltage V_{in} is logic-high, so that M1 and M2 have a nonzero drain current and that the output voltage is low. At this point, M1 is in the linear region and M2 is in saturation. Since $I_{D3} = 0$, the initial condition for the voltage V_x can be found as

$$V_x = V_{DD} - V_{T3}(V_x) \tag{9.26}$$

Now, assume that the input switches from its logic-high level to 0 V at $t = 0$. As a result, the driver transistor M1 will turn off and the output voltage V_{out} will start to rise. This change in the output voltage level will now be coupled to V_x through the bootstrap capacitor, C_{boot}. Let i_{Cboot} represent the transient current flowing through the capacitor C_{boot} during this charge-up event, and let i_{Cs} be the current through C_S. Assuming that the two current components are approximately equal, we obtain

$$i_{Cs} \approx i_{Cboot} \Leftrightarrow C_S \frac{dV_x}{dt} \approx C_{boot} \frac{d(V_{out} - V_x)}{dt} \tag{9.27}$$

Reorganizing (9.27) yields the following equation.

$$(C_S + C_{boot})\frac{dV_x}{dt} \approx C_{boot}\frac{dV_{out}}{dt} \tag{9.28}$$

$$\frac{dV_x}{dt} \approx \frac{C_{boot}}{(C_S + C_{boot})} \cdot \frac{dV_{out}}{dt} \tag{9.29}$$

It can be seen from (9.29) that the increase in the output voltage V_{out} during this switching event will generate a proportional increase in the voltage level V_x. Integrating both sides of (9.29), we obtain

$$\int_{V_{DD}-V_{T3}}^{V_x} dV_x = \frac{C_{boot}}{(C_S + C_{boot})} \cdot \int_{V_{OL}}^{V_{DD}} dV_{out} \tag{9.30}$$

$$V_x = (V_{DD} - V_{T3}) + \frac{C_{boot}}{(C_S + C_{boot})}(V_{DD} - V_{OL}) \tag{9.31}$$

If the capacitor C_{boot} is much larger than C_S ($C_{boot} \gg C_S$), the maximum value of V_x can be approximated as

$$V_x(max) = 2V_{DD} - V_{T3} - V_{OL} \tag{9.32}$$

which proves that voltage bootstrapping can significantly boost the voltage level V_x. Now remember that in order to overcome the threshold voltage drop at the output, the minimum required voltage level V_x is

$$\begin{aligned} V_x(min) &= V_{DD} + V_{T2}|_{V_{out}=V_{DD}} \\ &= (V_{DD} - V_{T3}(V_x)) + \frac{C_{boot}}{(C_S + C_{boot})}(V_{DD} - V_{OL}) \end{aligned} \tag{9.33}$$

This equation can be rearranged to give the required capacitance ratio, as follows.

$$\frac{C_{boot}}{(C_S + C_{boot})} = \frac{V_{T2}|_{V_{out}=V_{DD}} + V_{T3}|_{V_x}}{(V_{DD} - V_{OL})} \tag{9.34}$$

$$\frac{C_{boot}}{C_S} = \frac{V_{T2}|_{V_{out}=V_{DD}} + V_{T3}|_{V_x}}{V_{DD} - V_{OL} - V_{T2}|_{V_{out}=V_{DD}} - V_{T3}|_{V_x}} \tag{9.35}$$

Note that C_S is essentially the sum of the parasitic source-to-substrate capacitance of M3 and the gate-to-substrate capacitance of M2. To obtain a sufficiently large bootstrap capacitance C_{boot} in comparison to C_S, an extra "dummy" transistor is typically added to the circuit, as shown in Fig. 9.13.

Since its drain and source terminals are connected together, the dummy transistor simply acts as an MOS capacitor between V_x and V_{out}. Although this circuit arrangement contains two additional transistors to achieve voltage bootstrapping, the resulting circuit-performance improvement is usually well worth the extra silicon area used for the bootstrapping devices.

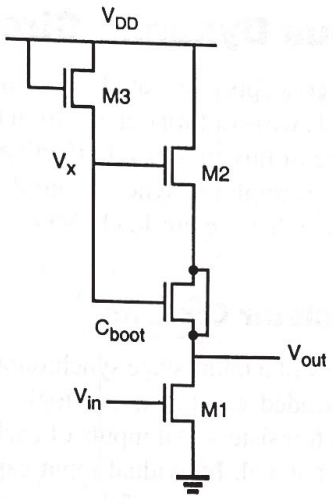
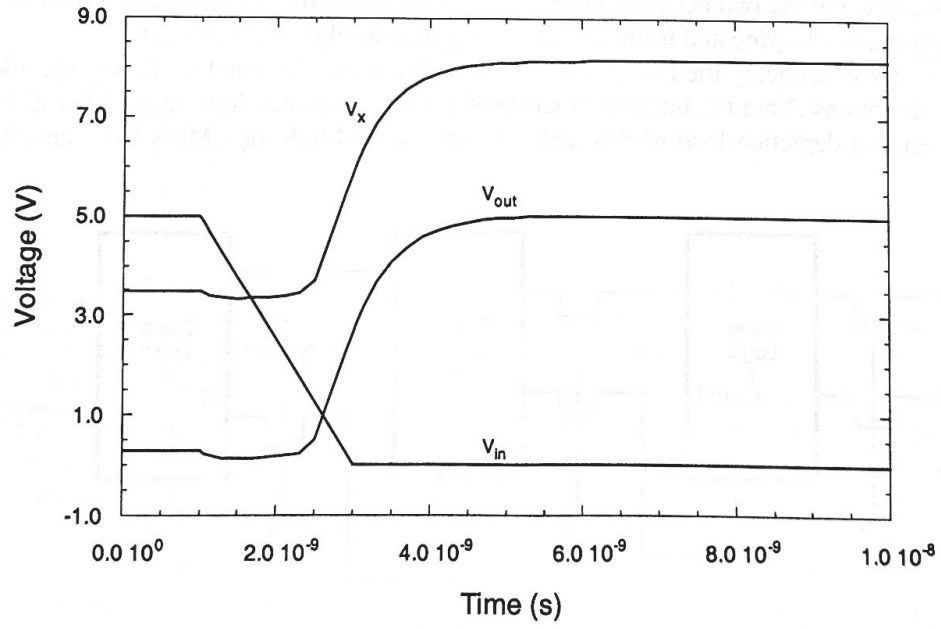


Figure 9.13 Realization of the bootstrapping capacitor with a dummy MOS device.

EXAMPLE 9.3

The transient operation of the simple bootstrap circuit shown in Fig. 9.13 is simulated using SPICE in the following. To provide the needed bootstrap capacitance C_{boot}, a dummy nMOS device with channel length $L = 5\ \mu$m and channel width $W = 50\ \mu$m is used. Transistor M1 has a (W/L) ratio of 2, while M2 and M3 each have a (W/L) ratio of 1.



Multilevel Cell Concept

To increase memory density, reducing the cell size has been the primary technique. By storing multilevel (e.g., 4) data in the cell, the effective memory density can be also improved. All memory cells have only two discrete states in the cell, "0" or "1". However, the inherent feature of the flash memory to control the threshold voltage of the cell transistor makes it more feasible than other memory devices to store multiple states in the cell. If the programming operation can be done accurately enough, the cell can have four discrete charge states, resulting in a structure that achieves 2 bits per cell. Figure 10.64 shows the threshold voltage distribution of 2 bits/cell storage. The number of possible states is limited by several constraints such as available charge range, the accuracy of programming and read operations, and disturbance of a state over time.

Flash Memory Circuit

Since the high voltage (V_{PP}) is required to program the cell, the on-chip charge pump circuit is used to generate the programming voltage. Charge pump circuits are implemented with nMOS or pMOS transistors for the generation of a high positive or a negative voltage, respectively. Figure 10.65 shows a typical circuit implementation of the charge pump circuit with nMOS transistors to generate a high positive voltage. The charge pump circuit consists of a chain of the diode and capacitors to be charged or discharged successively each half-clock cycle.

When *Clock* goes to low, the capacitors connected to *Clock* (i.e., $C_1, C_3, \ldots, C_{(n-1)}$) are discharged and the corresponding nodes (i.e., $V_1, V_3, \ldots, V_{(n-1)}$) are pulled down. These nodes are charged to a voltage equal to the voltage of a preceeding node minus a diode voltage (nMOS threshold voltage). For example, V_1 is charged to $V_{in} - V_T$(MN1) and V_3 to $V_2 - V_T$(MN3), and so forth.

As *Clock* goes high ($\overline{Clock}$ goes low) the nodes coupled to *Clock* are boosted while the nodes connected to $\overline{Clock}$ (i.e., $V_2, V_4, \ldots, V_n$) are pulled down. Therefore, charges at the nodes connected to *Clock* are transferred to the nodes connected to $\overline{Clock}$.

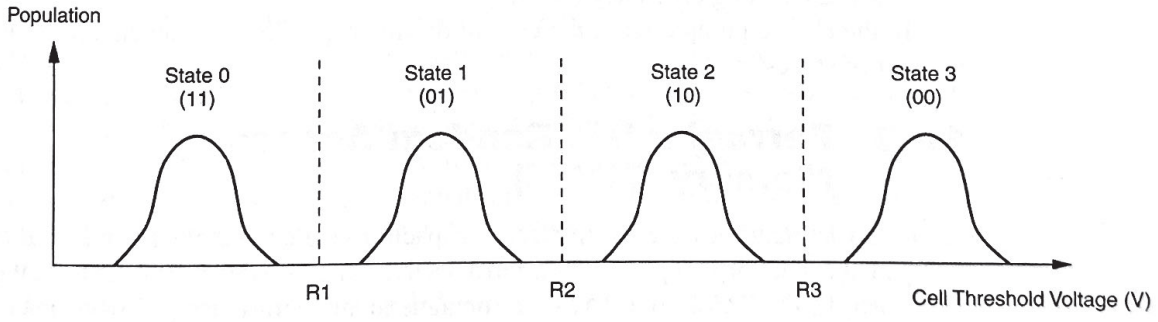


Figure 10.64 Multilevel-cell threshold voltage distribution.

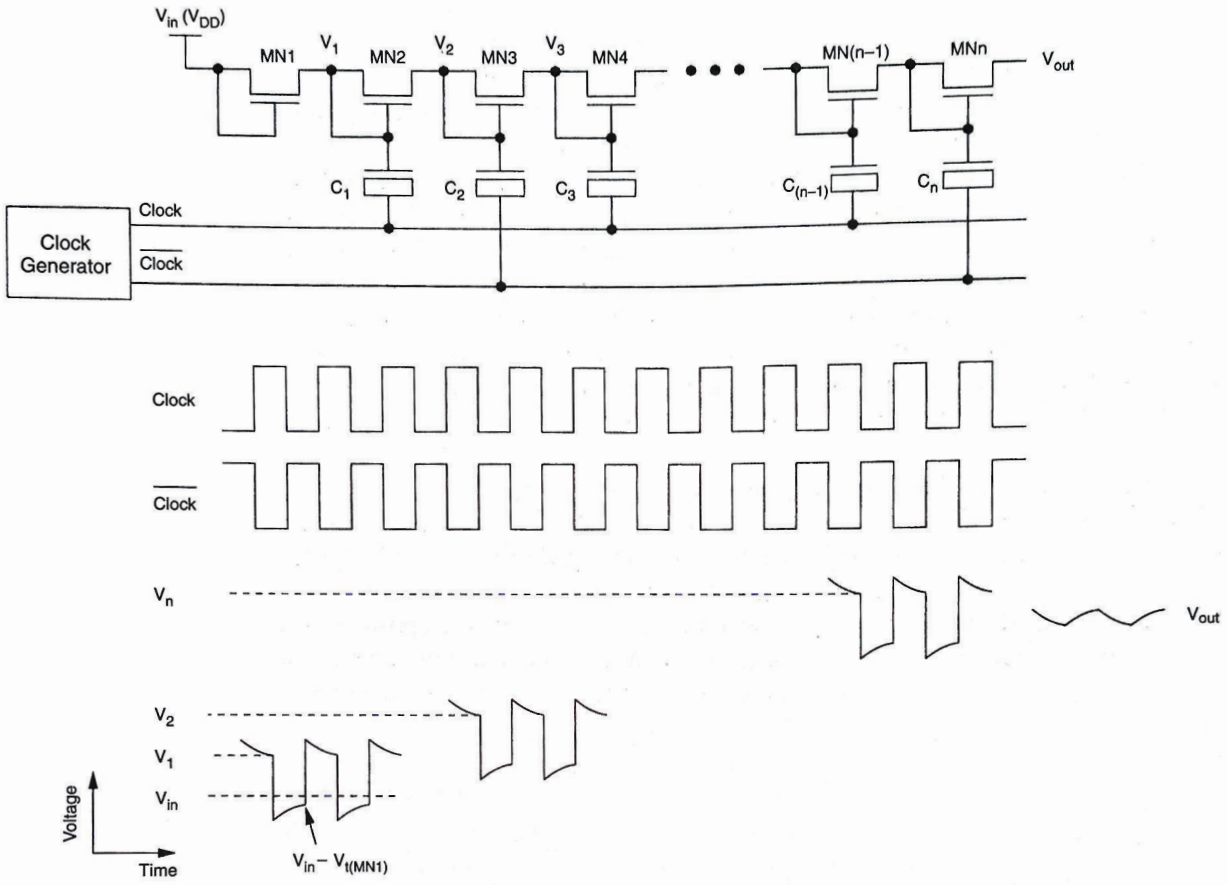


Figure 10.65 Positive charge pump circuit with nMOS transistors and voltage waveforms.

In the following half clock, charges at the nodes connected to $\overline{Clock}$ are transferred to the nodes connected to *Clock* in the same manner. Thus, the voltage of V_{out} is expressed as

$$V_{out} = V_{in} + (\gamma V_{DD} - V_T(\text{MN1})) + \cdots + (\gamma V_{DD} - V_T(\text{MNn})) \qquad (10.15)$$

where γ is a boosting efficiency factor.

In the charge pump circuit, the current driving capability is independent of the number of stages.

10.6 Ferroelectric Random Access Memory (FRAM)

Ferroelectric memories use a ferroelectric capacitor where the dielectric material of the typical capacitor is replaced by a ferroelectric material such as $Pb(Zr_xTi_{1-x})O_3$ and $SbBi_2Ta_2O_9$. Prior to FRAM, ferromagnetic memories using ferromagnetic cores with hysteresis characteristics were developed in 1950s. But those vanished due to large cell area and power consumption.