UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELL TECHNOLOGIES INC. AND DELL INC.,

Petitioners,

v.

GREENTHREAD LLC,

Patent Owner.

Case: IPR2023-00509

U.S. Patent No. 11,121,222

DECLARATION OF TRAVIS BLALOCK, PH.D.

I, Dr. Travis Blalock, declare as follows:

1. My name is Travis Blalock.

2. I have been retained as an expert witness on behalf of Dell Technologies Inc. and Dell (collectively "Dell" or "Petitioner") for the above-captioned Petition for *Inter Partes* Review ("Petition") of U.S. Patent No. 11,121,222 (the "'222 Patent") (Ex. 1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of $450 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1-9, 13-18, 20-28, 32-36, and 38-42 of the '222 Patent (the "Challenged Claims") are invalid as obvious to a person having ordinary skill in the art at the time of the alleged invention.

4. I am not currently, and have not at any time in the past been, an employee of Dell. I have no financial interest in Dell.

5. Previously, I submitted a declaration on December 28, 2022 in IPR2023-00420 on behalf of Intel Corporation. My declaration in IPR2023-00420 was directed to the same patent, the same Challenged Claims, the same combinations of prior art references, and the same invalidity theories that form the bases for my opinions here.

6. My opinions regarding the invalidity of the Challenged Claims of the ’222 Patent have not changed and are identical to my opinions in the declaration submitted in IPR2023-00420. My background and qualifications are also unchanged since that date. Therefore, I incorporate my previous declaration in its entirety and attach it as Exhibit A to this declaration, which is reproduced below.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: January 27, 2023

Respectfully Submitted,

Travis Blalock, Ph.D.

APPENDIX A

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner

v.

GREENTHREAD LLC,
Patent Owner

U.S. PATENT NO. 11,121,222

Case IPR2023-TBD

DECLARATION OF TRAVIS BLALOCK, PH.D.

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3. Claims 3/24: "The VLSI semiconductor device of claim [1/21], wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate." 55
4. Claims 4/25: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain [digital logic formed by/at least] one of either p-channel and n-channel devices." 55
5. Claims 5/26: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant." 55
6. Claims 6/27: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region are each separated by at least one isolation region." 57
7. Claims 7/32: "The VLSI semiconductor device of claim [1/21], wherein the graded dopant is fabricated with an ion implantation process." 57
8. Claim 8: "The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate." 58
9. Claims 9/28: "The VLSI semiconductor device of claim [1/21], wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type." 59
10. Claim 13: "The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel." 60
11. Claim 14: "The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)." 61
12. Claims 16/34: "The VLSI semiconductor device of claim [1/21], wherein the device is a flash memory." 62
13. Claim 17: "The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors." 63

14. Claims 18/36: "The VLSI semiconductor device of claim [1/21], wherein the device is central processing unit."....63
15. Claims 20/38: "The VLSI semiconductor device of claim [1/21], wherein each of the first and second active regions are in the lateral or vertical direction." 64
16. Claim 33: "The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device."....64
17. Claim 35: "The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions." 65
18. Claim 40: "The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region i the well to the substrate area where there is no well." 70

B. Ground II: 70

1. Claim 1/21/39/41/42 71
2. Claims 2/23: "The VLSI semiconductor device of claim [1/21], wherein the substrate is a p-type substrate."....90
3. Claims 4/25: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain [digital logic formed by/at least] one of either p-channel and n-channel devices." 91
4. Claims 5/26: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant." 91
5. Claims 6/27: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region are each separated by at least one isolation region."....92
6. Claims 7/32: "The VLSI semiconductor device of claim [1/21], wherein the graded dopant is fabricated with an ion implantation process." 93

7. Claim 8: "The VLSI semiconductor device of claim [1/21], wherein the first and second active regions are formed adjacent the first surface of the substrate." 93
8. Claims 9/28: "The VLSI semiconductor device of claim [1/21], wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type." 94
9. Claim 13: "The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel." 95
10. Claim 14: "The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)." 96
11. Claim 15: "The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate." 98
12. Claims 16/34: "The VLSI semiconductor device of claim [1/21], wherein the device is a flash memory." 98
13. Claim 17: "The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors." 99
14. Claims 18/36: "The VLSI semiconductor device of claim [1/21], wherein the device is central processing unit." 99
15. Claims 20/38: "The VLSI semiconductor device of claim [1/21], wherein each of the first and second active regions are in the lateral or vertical direction." 101
16. Claim 22: "The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate." 101
17. Claim 33: "The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device." 102
18. Claim 35: "The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions." 103
19. Claim 40: "The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier

movement from any region i the well to the substrate area where there is no well." 105

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I, Dr. Travis Blalock, declare as follows:

1. My name is Travis Blalock.

2. I have been retained as an expert witness on behalf of Intel Corporation ("Intel" or "Petitioner") for the above-captioned Petition for Inter Partes Review ("Petition") of U.S. Patent No. 11,121,222 (the "'222 Patent") (Ex. 1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of $450 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1-9, 13-18, 20-28, 32-36, and 38-42 of the '222 Patent (the "Challenged Claims") are invalid as obvious to a person having ordinary skill in the art at the time of the alleged invention.

4. The '222 Patent issued on September 14, 2021 from Application No. 16/947,294, filed on July 27, 2020. The '222 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004.

5. I am not currently, and have not at any time in the past been, an employee of Intel. I have no financial interest in Intel.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently an Associate Professor at the University of Virginia. I served as an Associate Professor from 1998 until 2013 when I moved to a non-resident Associate Professor position so I could lead a Handheld Ultrasound R&D

team for Analogic, Inc. I earned my Bachelor of Science and Master of Science in Electrical Engineering from the University of Tennessee at Knoxville in 1985 and 1988 respectively. I earned my Ph.D. from Auburn University in 1991. The primary emphasis of my doctoral research was CMOS analog and digital integrated circuit design.

7. From 1991 through August 1998, I worked at Hewlett Packard Laboratories, first as a Member of the Technical Staff, and then as a Principal Scientist. My work at Hewlett Packard Laboratories involved design and implementation of digital and analog integrated circuits. I was the principal architect and designer of integrated circuits having a diverse range of applications, including CMOS analog signal processing integrated circuits for mass storage devices and optoelectronic image acquisition and processing integrated circuits. I also have experience with software and custom design tools that allow for improved analysis, modeling, and simulation of integrated circuit analysis and design.

8. While I was employed at Hewlett-Packard Laboratories (now Agilent Laboratories) I was the lead designer on several mixed-signal CMOS chips. One of these was a massively parallel analog signal processing prototype integrated circuit [1]. The chip measures position with an accuracy of better than 100 μm over 10 inches by cross-correlating past and present images acquired by the integrated photo-array. The photodetector design was based on an understanding of dopant profiles

and the resulting effects on detector sensitivity. This was incorporated into the detection circuit design to optimize response. The chip has a 2048 element 25,000 frame/second photoreceiver array coupled with an analog signal processing cross-correlation array. The array performs a set of 9 nearest-neighbor cross-correlations between the two images at a total computation throughput of 1.5 billion operations per second. Over 100 million second generation versions of this chip have been sold and the architecture forms the core of most optical mice.

9. I was also the technical lead in the design of a 1024 x 768 silicon backplane ferro-electric liquid-crystal microdisplay. The chip also includes 1024 compact, offset-corrected column amplifiers and high-speed analog signal distribution. Both of the above chip designs were the highest density mixed-signal integrated circuits ever produced within Hewlett-Packard (at that time) and were fully functional at first silicon. I was also directly involved in the testing and verification of these chips in the laboratory.

10. At the University of Virginia, I led research in design of low-power mixed-signal integrated circuits. This work covered a broad range of application areas including medical ultrasound, subthreshold RFID for mobile health applications, wearable sensors, custom RFID for bio-tracking of plaque propagation, infrared imaging, cryptographic hardening, and sensors for CMOS process reliability.

11. More recently, I have led the development of a CMOS 600 channel low power medical imaging front-end integrated circuit. The chip simultaneously amplifies, filters, and digitizes signals from 600 independent ultrasound transducer elements. The chip development was part of an independent medical ultrasound startup (PocketSonics, Inc.) I founded which was acquired by Analogic, Inc in 2013. This work led to the development and release of a handheld medical ultrasound product by Analogic, Inc. This device was powered by a lithium-ion battery and included circuits to manage high peak currents, pulse-width modulation for controlled power delivery, charge management, and battery protection circuits.

12. I am currently a collaborator with the Integrated Electromagnetics, Circuits, and Systems Lab at the University of Virginia. In this group we design a variety of high frequency RF integrated circuits and merged RF/Optical circuits. Of particular interest are low power wake-up receivers, clock recovery, and high efficiency power amps for battery powered RF circuits.

13. I have written widely in the field of electrical engineering, including several editions of a textbook that is used across the world to teach principles of microelectronic circuit design to undergraduate and graduate students. I have authored or co-authored over 50 journal and conference papers. My textbook includes discussions of the solid-state physics needed to understand the operation of semiconductor diodes, BJT transistors, and CMOS transistors. In the course of

integrated circuit design teaching and practice, particularly the low noise, high sensitivity circuits I have focused on, it has been essential to understand the device physics and how neighboring devices may interact to understand subtle effects that impact the success of both industrial and academic designs.

14. I have contributed to or consulted on the design, fabrication, and/or operation of integrated circuits, including microelectronic integrated circuits, for organizations such as Hewlett-Packard, NASA Langley Research Center, Agilent Technologies, Displaytech, PocketSonics, and Analogic.

15. I am a named inventor on at least 27 U.S. patents. Several of these concern analog circuitry or semiconductor design, including guard rings, charge storage devices, and photosensors.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

18. I have considered the materials referenced herein, including the ’222 Patent (Ex. 1001), the file history of the ’222 Patent (Ex. 1002), the parent and

related applications, the file histories of the parent and related applications, including for the parent '195 Patent (Ex. 1016), the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Public Availability
U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek") (Ex. 1006)	Filed on October 29, 2002 (with priority to March 28, 2002).
U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe") (Ex. 1007)	Filed on September 22, 1997 (with priority to July 28, 1995) and issued on March 28, 2000.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1") (Ex. 1008A)	Published and publicly available no later than 2002.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2") (Ex. 1008B)	Published and publicly available no later than 2002.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3") (Ex. 1008C)	Published and publicly available no later than 2002.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4") (Ex. 1008D)	Published and publicly available no later than 2002.
Wang and Agrawal, Single Event Upset: An Embedded Tutorial, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang") (Ex. 1009)	Published and publicly available in 2008.
U.S. Patent No. 4,014,522 ("Jastrzebski") (Ex. 1010)	Filed March 24, 1982 and issued on November 6, 1984.
U.S. Patent No. 6,163,877 ("Gupta") (Ex. 1014)	Filed November 5, 1996 and issued on December 19, 2000.
U.S. Patent No. 6,534,805 ("Jin") (Ex. 1015)	Filed April 9, 2001 and issued on March 18, 2003.

Description	Date of Public Availability
Sze, *Semiconductor Devices Physics and Technology*, 2d Ed., John Wiley & Sons (2002) (Ex. 1022)	Published and publicly available in 2002.
Maziasz and Hayes, *Layout Minimization of CMOS Cells*, Kluwer Academic Publishers (1992) ("Maziasz") (Ex. 1023)	Published and publicly available in 1992.
Rabaey *et al.*, *Digital Integrated Circuits, A Design Perspective,* Prentice Hall Electronics and VLSI Series (2003) ("Rabaey") (Ex. 1025)	Published and publicly available in 2003.
Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973) (Ex. 1026)	Published and publicly available in 1973.
U.S. Patent No. 4,160,985 to Kamins *et al.* ("Kamins") (Ex. 1031)	Filed November 25, 1977 and issued July 10, 1979.
McGraw-Hill Dictionary of Scientific and Technical Terms (2003) (Ex. 1032)	Published and publicly available in 2003.
U.S. Patent Application Publication No. 2003/0030488 to Hueting *et al.* ("Hueting") (Ex. 1034)	Filed July 25, 2002 (with priority to August 7, 2001).
Howe and Sodini, *Microelectronics, An Integrated Approach*, Prentice Hall Electronics and VLSI Series (1997) ("Howe") (Ex. 1037)	Published and publicly available in 1997.
Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology,* 3rd Ed., McGraw-Hill (2004) ("Hodges") (Ex. 1038)	Published and publicly available in 2004.

Description	Date of Public Availability
Jaeger *et al.*, *Microelectronic Circuit Design*, McGraw-Hill (1997) ("Jaeger") (Ex. 1040)	Published and publicly available in 1997.
Kang and Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill (2003) ("Kang") (Ex. 1041)	Published and publicly available in 2003.

19. The references listed above include prior art to the '222 Patent which is entitled to a priority date not earlier than September 3, 2004. Kawagoe, Gupta, and Wolf.1-3 (Exs. 1008A-C) were not cited. Though Wieczorek and Wolf.4 were cited, they were not discussed.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Obviousness

22. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

23. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

24. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;

- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

25. I understand that a POSITA has ordinary creativity, and is not an automaton.

26. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

27. I understand that prior art to the ’222 Patent includes patents and printed publications in the relevant art that predate the Priority Date of the ’222 Patent.

28. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged

invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. SUMMARY OF OPINIONS

29. It is my opinion that claims 1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42 are disclosed or, at a minimum, rendered obvious by Kawagoe (Ground I).

30. It is my opinion that claims 1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42 are rendered obvious by Wieczorek in combination with Wolf (Ground II).

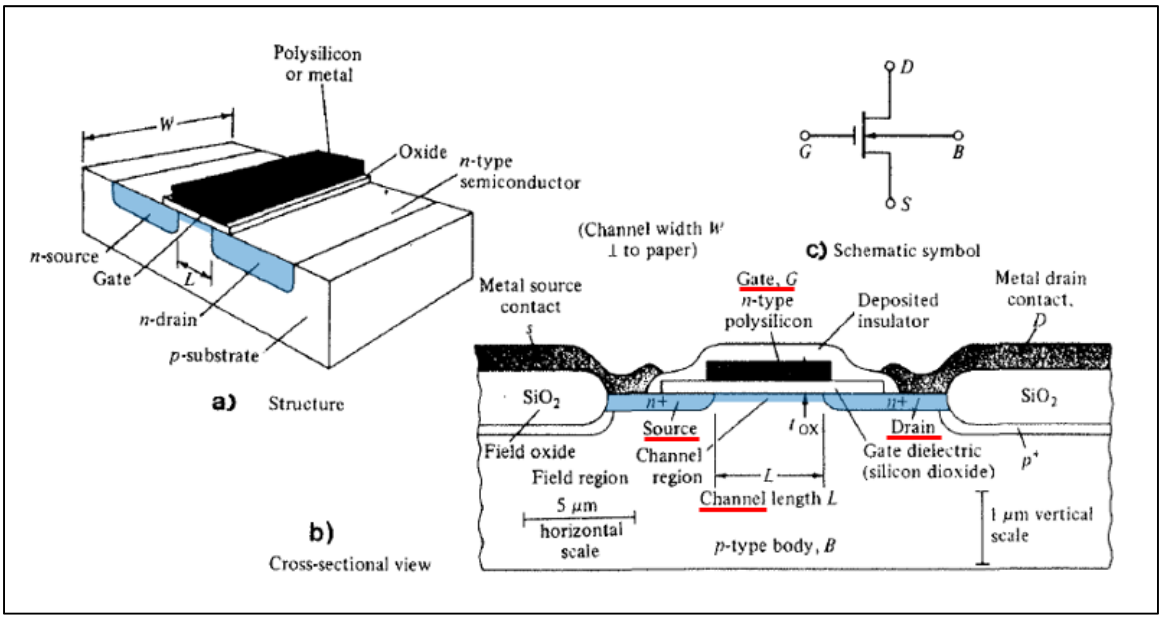
31. It is my opinion that claims 1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42 are rendered obvious by Kawagoe in view of Gupta (Ground III).

32. It is my opinion that claims 1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42 are rendered obvious by Wieczorek in combination with Wolf and Gupta (Ground IV).

33. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

V. OVERVIEW OF THE TECHNOLOGY

34. A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a transistor that switches from an OFF state to an ON state when a voltage is applied to a gate terminal. Ex. 1008B, 402. In the ON, or active state, current flows from a source to a drain through a channel region (the length of such channel region is labelled "L" below). The channel region is under the gate and gate oxide, and between the source and drain.

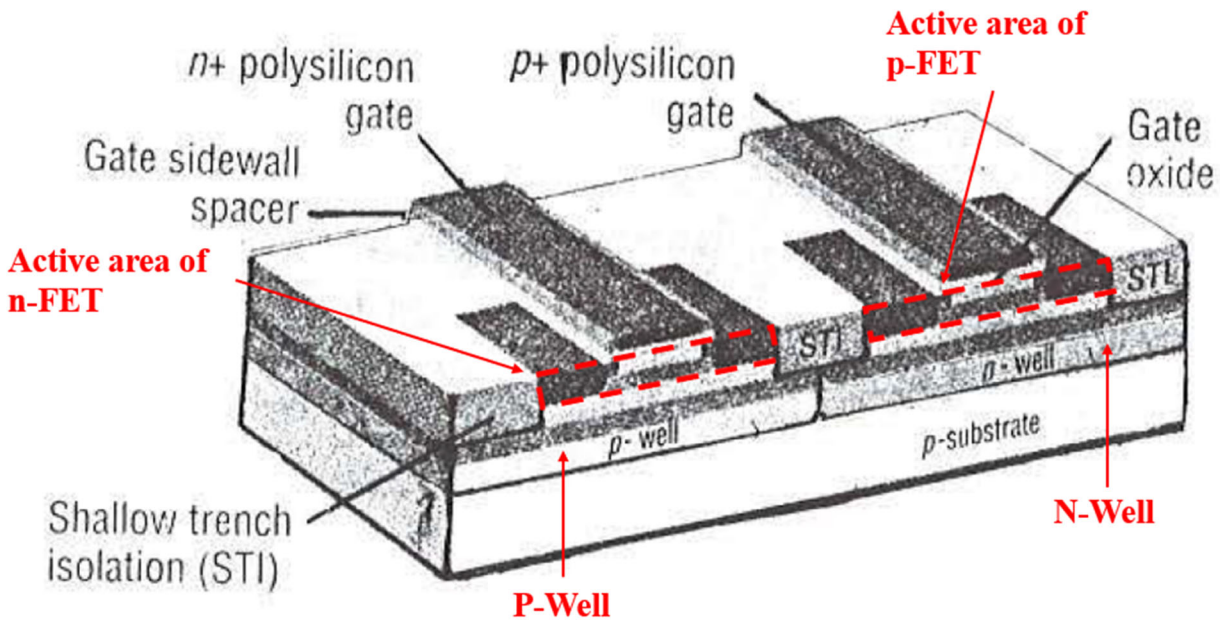


Ex. 1008B, FIG. 5-1 (annotations in red);[1] *id.*, 298-301, FIGS. 5-2, 6-4. The combination of the source, drain, and channel regions form the active region of a transistor. Ex. 1008B, 299-300 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The active regions

[1] All emphases and annotations added unless otherwise noted.

are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

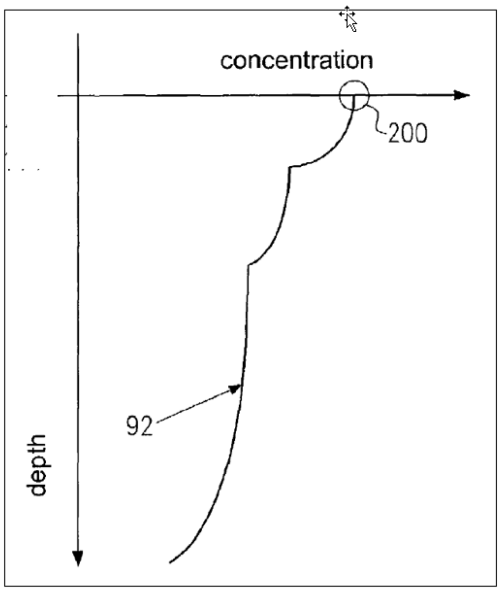
35. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from "p-type" material in such areas (as shown in the figure above, labelled "p^+") is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from "n-type" material ("n+") in such areas is known as a NMOS or n-FET. In the mid-1980s, Complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same device. In such devices, the active areas (and associated transistors) are generally formed in regions called "wells," which have opposite dopant type to the dopants of the source/drain, as illustrated below.

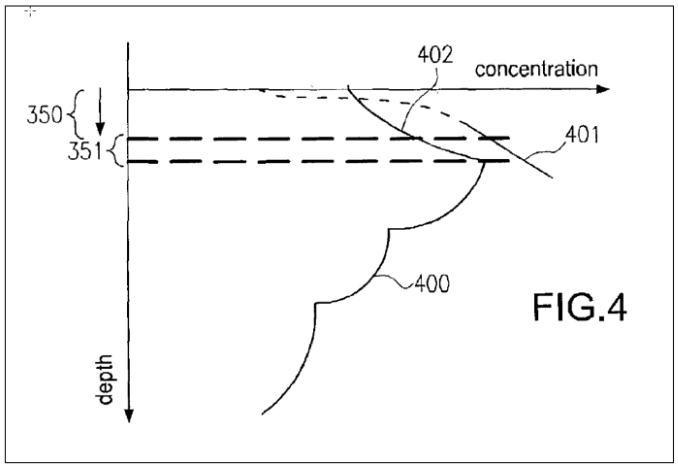


Ex. 1008A, FIG. 16-28 (annotations in red).

36. Impurities known as "dopants" are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions such as their conductivity. Charge carriers can be electrons or holes. Ex. 1008C, 86. When a region is doped with p-type dopants, the holes are majority carriers and the electrons are minority carriers. Ex. 1008C, 86. When a region is doped with n-type dopants, the electrons are majority carriers and the holes are minority carriers. Ex. 1008C, 86.

37. A "dopant profile" refers to the "map" of concentration of dopants over a doped region and, in certain simplified scenarios, can be expressed as as a function of depth. For example, a dopant concentration that does not change with depth is a uniform concentration. A non-uniform dopant concentration that varies for example with depth, e.g., increases or decreases with depth, is a non-uniform dopant concentration called "graded." A graded dopant concentration that peaks at some depth of the doped region(s) instead of at the top or bottom of the doped region(s) is called "retrograde." All such doping profiles were known in the art, as shown in the Wieczorek figures below.





See Ex. 1006, FIG. 2B (left) and FIG. 4 (right).

VI. THE '222 PATENT

38. The '222 Patent issued on September 14, 2021 from Application No. 16/947,294, filed on July 27, 2020. The '222 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004. Ex. 1001, cover.

A. Claims

39. The '222 Patent has 44 claims, including seven independent claims numbered 1, 21, 39, and 41-44. Ex. 1001, 4:38-8:40. Claims 1-9, 13-18, 20-28, 32-36, and 38-42 are the Challenged Claims.

40. Exemplary Claim 1 is reproduced below:

> **1.** A VLSI semiconductor device, comprising:
>
> a substrate of a first doping type at a first doping level having a surface;

> a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
>
> a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
>
> transistors formed in at least one of the first active region or second active region;
>
> at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
>
> at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

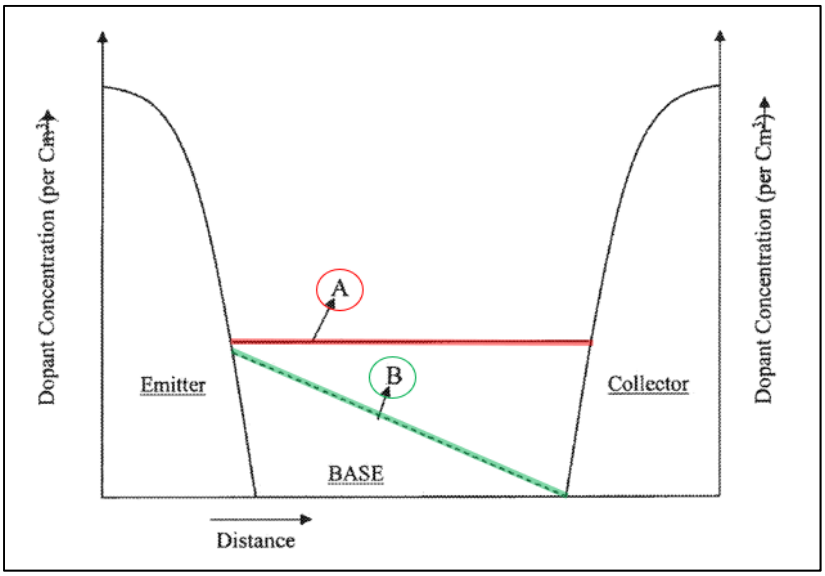
Ex. 1001, 4:39-62.

B. Summary of the Specification

41. The ’222 Patent is directed to “grading the dopant concentration” in active/well region(s) of a semiconductor device to aid carrier movement. Ex. 1001, Abstract. In particular, the Challenged Claims claim that an active region and a well region of a semiconductor device have graded dopant concentrations to aid carrier movement. *Id*., Cl. 1 (“at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement …” and “at least one well region … containing at least one graded dopant region, the

graded dopant region to aid carrier movement …"). I understand that those claims are asserted against CMOS products in the District Court Case. In my opinion, the references relied on in the Petition (*i.e.*, Kawagoe, Wieczorek, Wolf, and Gupta) are also directed to CMOS devices and technology.

42. According to the '222 Patent, the figure below "illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ('A') [(red)] and graded base ('B') [(green)]." Ex. 1001, 2:27-30.



Id., FIG. 1 ("Prior Art").[2] The '222 Patent states that such "uniform base" and "graded base" bipolar junction transistors existed in the prior art. *Id.*

[2] All colors and colored annotations to figures added.

43. The ’222 Patent explains that “[r]etrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits.” Ex. 1001, 2:5-7. The ’222 Patent further states that “[r]etrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs.” *Id*., 2:11-16. The ’222 Patent also explains that “these techniques” in the prior art “either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.” *Id*., 2:16-19.

44. In my opinion, the only description of graded dopant concentrations and purported carrier movement in CMOS devices (the only types of devices accused of infringement in the District Court Case) in the ’222 Patent is in two paragraphs of the specification and associated Figures 5A-5C. Ex. 1001, 3:36-4:18, FIGS. 5A-5C. In my opinion, the specification does not provide any guidance, such as dopant concentration ranges or doping gradients, on the grading of dopant concentration that would accomplish “sweep[ing] [] carriers from the active circuitry at the surface into the substrate” or “aid[ing]” carrier movement in CMOS devices as recited in the Challenged Claims. It is my further opinion that the specification does not provide any guidance as to the degree or nature of the “aiding” referenced

in the Challenged Claims. Instead, the specification contrasts "graded channel[s]" with "uniformly doped channel (as practiced in the prior art)." *Id*. at 4:2-5. Thus, in my opinion, the specification uses "graded" dopant to describe a dopant concentration that is not uniform.

45. In my opinion, the specification also does not describe grading in an active region of a CMOS device to move carriers to the "area of the substrate where there are no active regions" as claimed in the Challenged Claims. Ex. 1001, Cl. 1. Instead, the specification discusses only grading the channel region of an active region "to accelerate majority carriers towards the drain." *Id*., 3:64-66.

C. Summary of the Prosecution History

46. I understand that the Challenged Claims issued without any prior art rejection. None of the references relied on in this Petition were discussed during prosecution and Kawagoe, Gupta and Volumes 1-3 of Wolf were not cited. According to the Examiner, the claims issued over the "closest reference" (U.S. Patent Application Publication No. 2007/0045682 ("Hong")) because Hong does not disclose "active" regions. Ex. 1002, 226-229. I note that Hong is not prior art and was also the only reference discussed in prosecution of the immediate parent application that issued as U.S. Patent No. 10,734,481 ("the '481 Patent"). I also note that none of the claims at issue during prosecution of the earlier parent applications to both the '481 and '222 Patents are of the same or similar scope as the Challenged

Claims. For example, the claims of the parent U.S. Patent No. 9,647,070 ("the '070 Patent") are directed to bipolar devices and claim aiding carrier movement "from an ***emitter*** in the active region to a ***collector*** in the substrate," and not "from the first and second active regions towards an area of the substrate where there are no active regions" as claimed in the Challenged Claims. Ex. 1034, Cl. 1. Other claims that claim graded dopant in an active region were withdrawn prior to substantive examination. Ex. 1016, 73 (withdrawing claims 1-2); Ex. 1028, 9 (same); Ex. 1029, 7 (canceling claims 1-2); Ex. 1030, 18 (same).

VII. LEVEL OF ORDINARY SKILL IN THE ART

47. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

48. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '222 Patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to

understand the ’222 Patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

49. It is my opinion that a POSITA at the time of the ’222 Patent would have had a Bachelors degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for a deficiency in experience, and vice-versa.

50. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

51. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

52. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under § 112.

53. I understand that the parties have proposed claim constructions in the District Court Case as set forth in the table below. Exs. 1017-1021.

Claim Term	Patent Owner’s	Petitioner’s Proposed

	Proposed Construction	**Construction**
"substrate"	Plain Meaning ("an underlying layer")	"the initial material within which or on which the semiconductor device is fabricated"
"active region"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed")	"region that forms the current path of a device" or "the source, drain and channel region of a device"
"to aid carrier movement from … [to/towards] …"	Plain Meaning	Indefinite Alternative Construction: "to sweep the carriers from … [to/towards] …"
"well region"	Plain Meaning ("a doped region that surrounds the active region of a semiconductor device")	"A well, whether formed by single or multiple implants. Portions of a well are not well regions."
"active region … within which transistors can be formed"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")	Indefinite

54. I support Petitioner's proposed constructions. However, I do not believe any terms need be construed to resolve the issues presented in this Petition because, in my opinion, as the Challenged Claims are unpatentable under either party's proposed constructions (except for the term "active region … within which

transistors can be formed," which I address under Patent Owner's proposed construction). I reserve the right to respond to any purported claim constructions that Patent Owner raises.

IX. OVERVIEW OF THE PRIOR ART

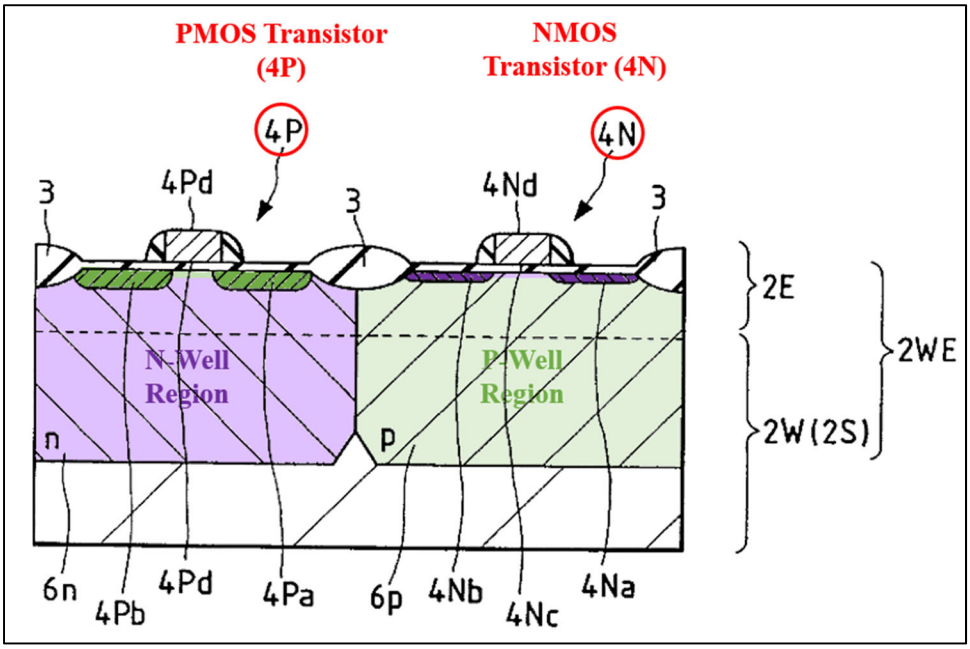
A. Kawagoe

55. Kawagoe discloses "a semiconductor integrated circuit device manufacturing method characterized in that said first semiconductor region is a well to be used for forming a complementary MOS.FET (Metal-Oxide-Semiconductor. Field Effect-Transistor) [(CMOS)] circuit (i.e., for forming a complementary MIS (Metal-Insulator-Semiconductor). FET circuit)." Ex. 1007, 3:32-38.

56. Kawagoe explains that, in its Embodiment 1, the "epitaxial layer 2E is doped … in a concentration equal to the [concentration] of the substrate body 2S." Ex. 1007, 6:65-7:3; *see also id*., 8:40-52. In its Embodiment 4, "the impurity concentration of the semiconductor substrate body 2S is made higher than that of the epitaxial layer 2E … to improve the resistance to the latchup." *Id*., 15:13-17; *see also id*., 15:26-40.

57. I am of the opinion that the figure below from Kawagoe illustrates a conventional twin-well CMOS structure. A conventional twin-well CMOS structure includes "two separate wells [] formed for *n*- and *p*-channel transistors." Ex. 1008B, 387; *see also, e.g.*, Ex. 1008A, 227, FIG. 7-3 (showing a "[c]ross-section of a twin-

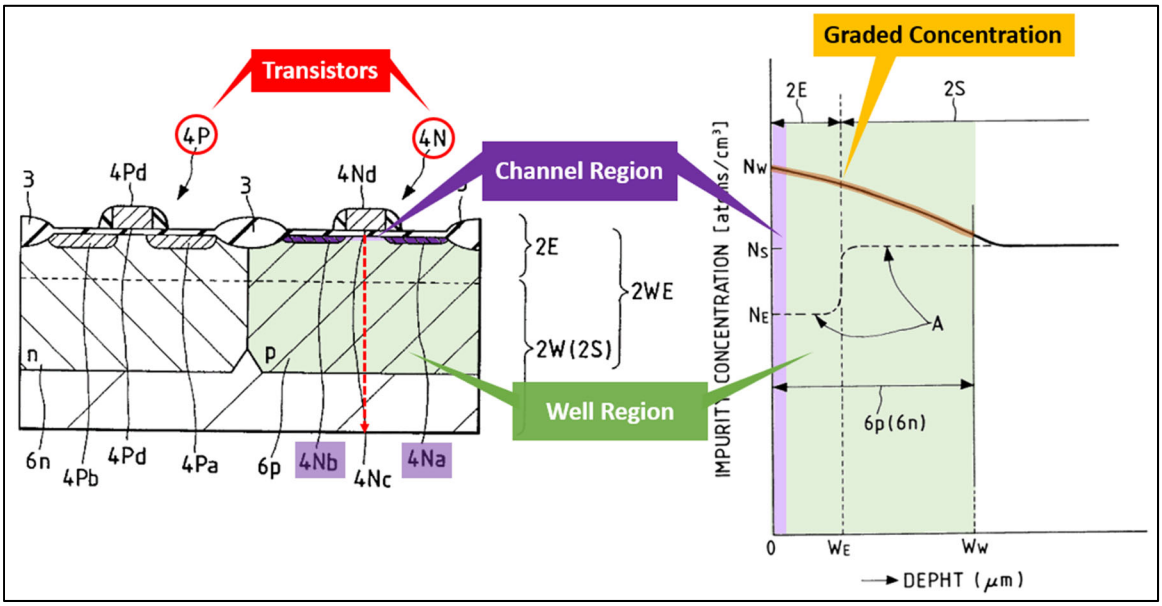
well CMOS structure built in a p^- epitaxial layer and a p^+ substrate"); Ex. 1008B, 382, FIG. 6-8(c) (illustrating a "CMOS circuit[] [] designed using … twin-well technology"). The figure below from Kawagoe shows source-drain regions (purple) of an NMOS transistor formed in a p-well (light green) and the source-drain regions (green) of a PMOS transistor formed in an n-well (light purple). Ex. 1007, 8:46-9:6, 9:32-54, 14:46-55, 15:26-40, 18:18-23.



Ex. 1007, FIG. 23.

58. Kawagoe further teaches that "the p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E." Ex. 1007, 15:62-16:2; *see also id.*, 14:46-55, 16:2-40. In other words, Kawagoe teaches that the well regions have a graded dopant concentration that decreases with

depth, as illustrated in the doping profile in Figure 17 below in the context of a p-well (light green).



Id., FIGS. 17 and 23.

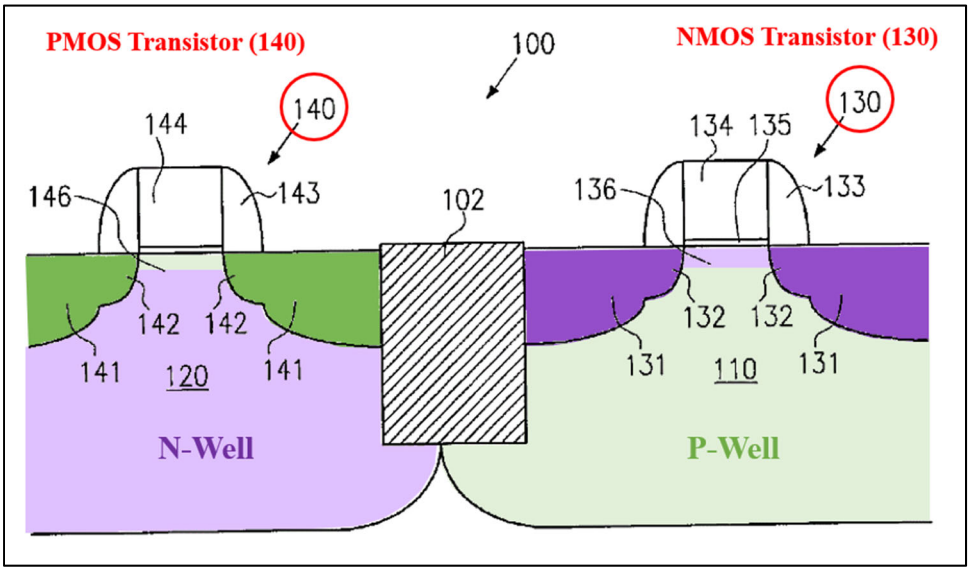
59. Kawagoe explains that "the impurity concentration of the p-well 6p is given such a gradient that it is ***gradually lowered*** in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered." Ex. 1007, 16:2-7.[3] Kawagoe further explains that "the electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p." *Id*., 16:7-11.

[3] All emphases added unless otherwise noted.

B. Wieczorek

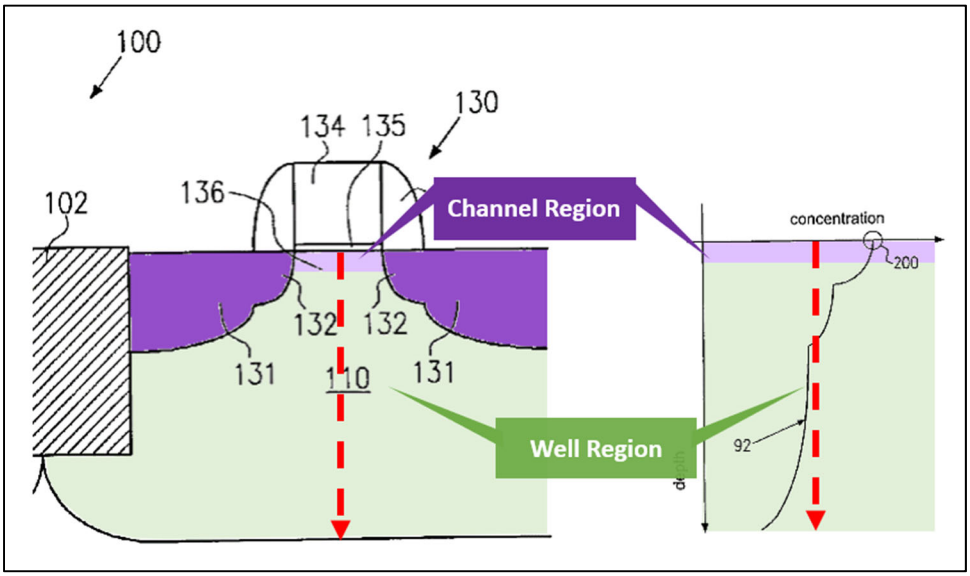
60. For purposes of this Petition, I rely on Wieczorek's description of conventional prior art CMOS devices, such as the twin-well CMOS device illustrated in Figure 1b below. Ex. 1006, [0007], [0012], [0020]-[0021]; *see also* Section IX.A (discussing conventional twin-well CMOS devices).

61. The semiconductor device 100 illustrated in the figure below from Wieczorek is "a complementary MOS transistor pair." Ex. 1006, [0007]. The figure below illustrates the source-drain and channel regions (purple/light purple) of an NMOS transistor formed in a p-well (light green) and the source-drain and channel regions (green/light green) of a PMOS transistor formed in an n-well (light purple). *Id*., [0007], [0012].



Ex. 1006, FIG. 1b.

62. Wieczorek explains that graded dopant concentrations in prior art CMOS devices peak at the surface of the substrate and decrease with depth, as shown below. Ex. 1006, [0004], [0007]-[0013]



Id., FIGS. 1b and 2b.

C. Wolf

63. *Silicon Processing For The VLSI Era* by Stanley Wolf is a four volume textbook related to semiconductor devices, with particular focus on CMOS devices. Exs. 1008A-D. I am familiar with the Wolf textbook. An internet search for this textbook title limited to the ".edu" domain yields over 800 results. Thus, it is clearly used as a teaching resource in engineering courses in many, many universities and is widely cited in scientific works.

D. Gupta

64. Gupta "relates to the field of complimentary metal oxide semiconductor (CMOS) circuits, and more particularly to [] layouts for CMOS circuits." Ex. 1014. 1:7-10. Gupta reflects the common knowledge of a POSITA when it explains that "[c]onservation of semiconductor area is a primary goal in semiconductor chip development" and a common technique to conserve area is "by placing transistors so as to share diffusion area [(active region)]." *Id*., 1:32-54, 2:17-21.

X. SPECIFIC GROUNDS FOR PETITION

A. Ground I:

65. In my opinion, Kawagoe renders claims 1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42 obvious.

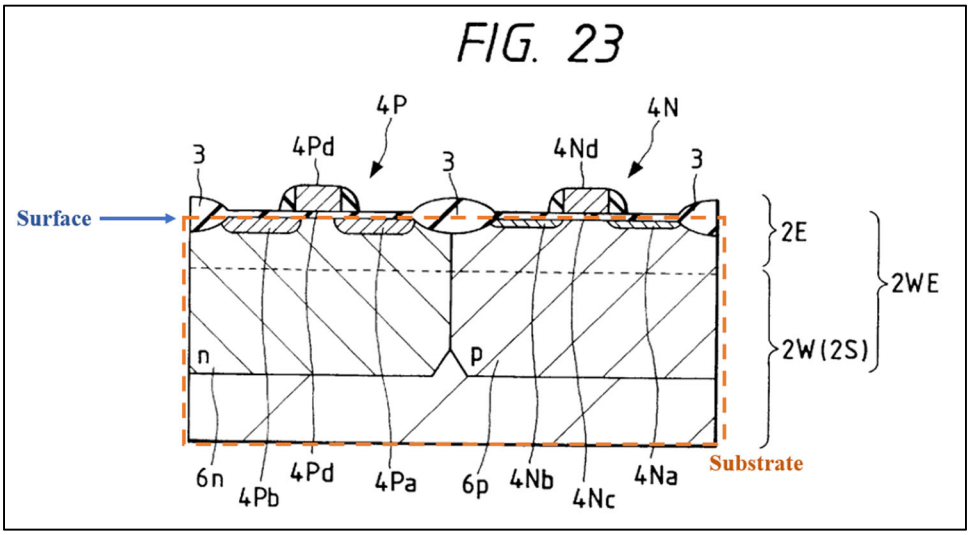
1. Claims 1/21/39/41/42

a. Preambles: "A [VLSI] semiconductor device, comprising:"[4]

66. To the extent the preamble is limiting, in my opinion, Kawagoe discloses it or, at a minimum, renders it obvious. Kawagoe is directed to a "semiconductor integrated circuit device." Ex. 1007, Title, 1:13-23, 14:46-67, FIGS. 16-17, 23.

[4] Bracketed language shows the difference between the claims. Appendix A lists the elements and corresponding language for all Challenged Claims.

67. For Ground I, I primarily focus on the twin-well CMOS device in Figure 23 (Embodiment 4) of Kawagoe, fabricated on a uniformly-doped epitaxial substrate, as taught in Embodiment 1 of Kawagoe.[5] *See* Section X.A.1.b.



Ex. 1007, FIG. 23.

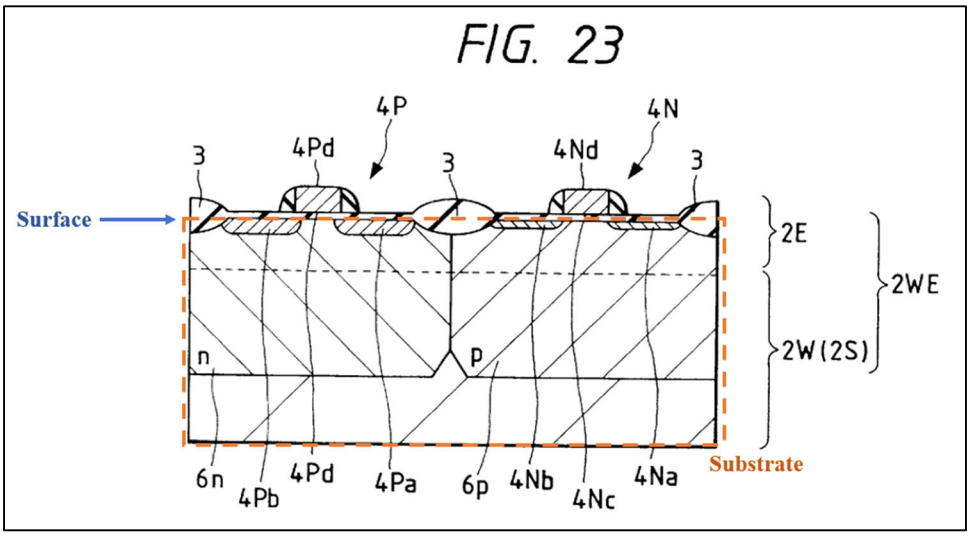
68. Kawagoe's teachings apply to "VLSI" DRAM, flash memory, and microcomputer devices. *Id.*, 1:24-30; Sections X.A.1.h, X.A.11/12/14. Notably, Kawagoe's teachings apply to multi-Megabit DRAM devices with at least one transistor per memory cell, totaling millions of transistors. Ex. 1007, 19:15-18, 20:1-15; Ex. 1016, 73 (VLSI refers to "at least one million active elements"). Wolf, which applies to "the VLSI Era," also confirms that such devices at the time were

[5] Figures 16-17 and 23 are all directed to Kawagoe's Embodiment 4. Ex. 1007, 14:46-60. Figure 23 shows the same twin-well CMOS structures depicted in Figure 16 without the metal layers not relevant to the claims. Ex. 1007, 17:10-18:38.

understood to have at least one million active elements. Ex. 1008A, cover, xxxiii, FIG. 1 (microprocessor with at least one million transistors); Ex. 1008B, 596-597 (1-Megabit CMOS DRAM with one transistor per memory cell), 633-635 (1-Megabit CMOS flash EEPROM with one floating gate per memory cell and other transistors, totaling at least one million active elements).

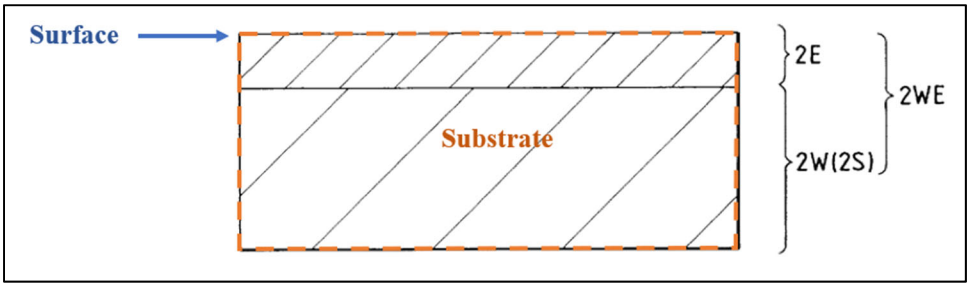
b. Elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1]: "a substrate of a first doping type at a first doping level [having a surface];"

69. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. Kawagoe discloses "semiconductor substrate 2" of a first doping type (p-type) having a silicon "epitaxial layer 2E [] doped with a ***p-type*** impurity such as boron" formed over non-epitaxial "semiconductor substrate body 2S [also] doped with a ***p-type*** impurity such as boron...." Ex. 1007, 14:61-15:12, 6:50-7:3. The substrate (orange) has a surface, as shown below.



Id., FIG. 23.

70. In my opinion, Kawagoe satisfies elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1] under Patent Owner's plain meaning construction and under Petitioner's proposed construction because Kawagoe's epitaxial substrate is the initial material within or on which Kawagoe's "semiconductor integrated circuit device 1" is later fabricated. Section VIII; Ex. 1007, 6:51-56, 14:61-67, 17:10-18:38.



Ex. 1007, FIG. 20. Specifically, 2WE epitaxial wafers are produced by manufacturers and supplied as the starting point material for subsequent processing by integrated circuit (IC) foundries. Alternatively, foundries may deposit their own epitaxial layer, but in either case, the result is the starting point for the circuit fabrication process.

71. As I explain in more detail below, Ground I relies on a uniformly-doped epitaxial substrate in which the silicon epitaxial layer 2E of the substrate is doped at the same level as the silicon substrate body 2S, so that the entire substrate in Figure 20 is "at a first doping level" as recited in the claims. Ex. 1007, 6:60-7:3.

72. **<u>"at a first doping level"</u> -** Kawagoe teaches an epitaxial substrate (2S+2E), illustrated in Figure 20, in which the non-epitaxial silicon substrate body (2S) is either doped at the same or higher level compared to the epitaxial silicon layer (2E). For example, Embodiment 1 describes a uniformly-doped epitaxial substrate in which the "epitaxial layer 2E is doped … in a concentration ***equal*** to the [concentration] of the semiconductor substrate body 2S, e.g., 1.3x1015 atoms/cm3." Ex. 1007, 6:60-7:3; *id.*, Abstract (describing "an epitaxial layer which contains an impurity of the ***same*** conduction type [and at] … the ***same concentration***" as the bulk substrate), 2:57-3:9 (same). This uniformly-doped epitaxial substrate is Kawagoe's "benchmark" substrate repeatedly discussed in other embodiments, including Embodiment 4. Ex. 1007, 12:64-65, 13:12-15, 13:66-67, 14:18-20, 15:7-25.

73. Embodiment 4 introduces an optional latchup-resistant substrate in which "the impurity concentration of the semiconductor substrate body 2S is made ***higher*** than that of the epitaxial layer 2E … ***to improve*** the resistance to latchup." Ex. 1007, 15:13-17.

74. In my opinion, a POSITA would have understood that Kawagoe teaches forming Figure 23's twin-well CMOS device (Embodiment 4) on either Embodiment 1's uniformly-doped epitaxial substrate or Embodiment 4's optional latchup-resistant substrate. My opinion is supported by the fact that Kawagoe

emphasizes the benefits of Embodiment 1's uniformly-doped epitaxial substrate and explains that the substrate used in Embodiment 4 is formed "***as in the foregoing embodiment 1*** so that … the cost of the semiconductor substrate 2 is lowered to about one half." Ex. 1007, 15:7-25.

75. In any event, in my opinion, a POSITA would have been motivated to use a uniformly-doped epitaxial substrate to form Figure 23's twin-well CMOS device because this substrate provides "excellent film quality" that "drastically reduce[s] the defect densities of the gate insulating films" and "improve[s] the [device's] performance, reliability and production yield." Ex. 1007, 12:8-40; *see also id*., 15:7-25. This substrate is also easier to manufacture, which helps "lower the cost" of the substrate and the chip. *Id*., 12:8-40.

76. In my opinion, a POSITA would understand that use of uniformly-doped epitaxial substrate as the starting material in lieu of Embodiment 4's latchup-resistant substrate to form Figure 23's twin-well CMOS devices is a simple substitution of one known element with another known, closely-related element, both of which are described in Kawagoe, and would have been obvious to try because it involves nothing more than choosing one of two ways of doping an epitaxial substrate that are both described in Kawagoe.

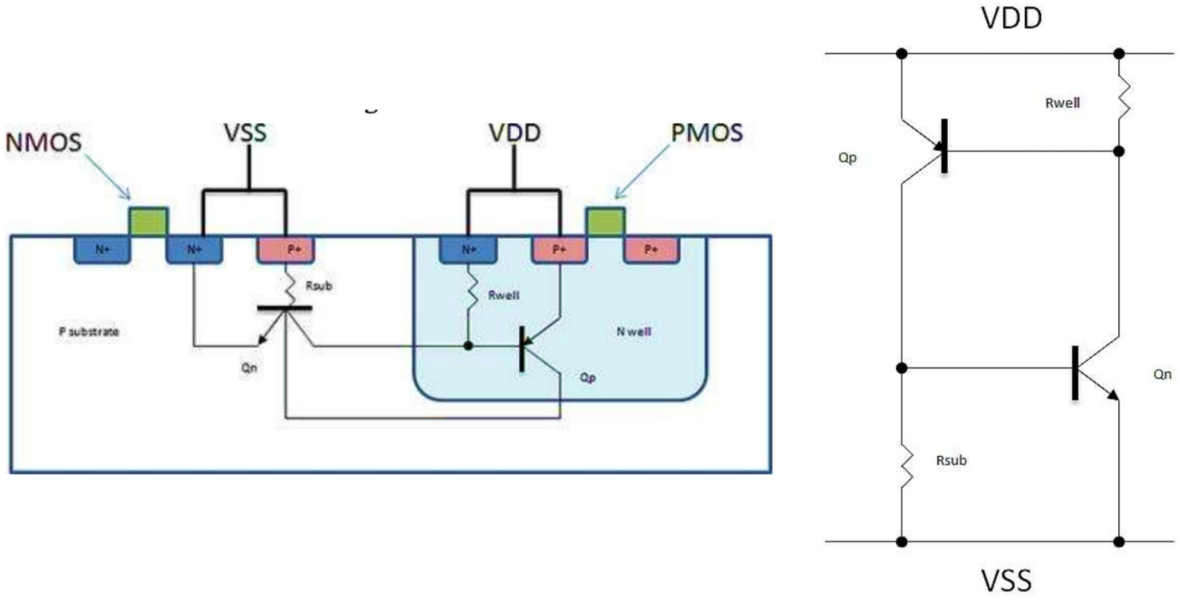
77. In my opinion, twin-well CMOS devices (illustrated in Figure 23) fabricated on a uniformly-doped epitaxial substrate would have worked for their

intended purpose. As discussed in Wolf, twin-well CMOS devices were commonly formed over a "***uniformly***, lightly doped *p*- or *n*- type substrate" that provides no improved latchup resistance. Ex. 1008C, 523, *id*., 530 ("With the twin-tub [(twin-well)] approach, … two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate …"); Ex. 1008B, 387-389; Ex. 1007, 2:57-65 (discussing a uniform "lightly doped" epitaxial substrate).

78. In my opinion, there would be reasonable expectation of success because Kawagoe describes in detail the use of both uniformly-doped epitaxial substrates and latchup-resistant substrates in forming CMOS devices, and repeatedly emphasizes their similarity. Ex. 1007, 8:40-52; 12:8-40, 14:58-60, 15:7-12 (substrate), 15:18-25 (epitaxial layer), 15:26-40 (transistors). A uniformly-doped ***epitaxial*** substrate is also better, in my opinion, than the bulk (non-epitaxial) substrate commonly used to fabricate twin-well CMOS devices. *Id.*, 1:33-40 ("The epitaxial wafer is advantageous [compared to bulk wafer/substrate] in that … the gate insulating film to be formed over the epitaxial layer can have excellent breakdown characteristics to drastically reduce the defect density of the gate insulating film."); *id.*, 12:8-40; Ex. 1008B, 387-88 (discussing twin-well CMOS devices fabricated over bulk substrate).

79. Kawagoe characterizes the improved latchup tolerance provided by Embodiment 4's optional latchup-tolerant substrate as just another "effect[] [that]

can be achieved in addition to those of the foregoing embodiment 1." Ex. 1007, 19:49-63. In my opinion, and consistent with Kawagoe's teachings, a POSITA would have understood that a uniformly-doped epitaxial substrate is a suitable substrate because, among other benefits, it "drastically reduce[s] the defect densities of the gate insulating films" of CMOS transistors. Ex. 1007, 12:8-40. Moreover, in my opinion, a POSITA would have understood that improved latchup resistance is not needed for CMOS chips that are not susceptible to latchup or for which latchup (a "short-circuit" failure condition in poorly designed circuits) is not a concern. Ex. 1008B, 406 ("four conditions must exist in a CMOS circuit in order for latchup to occur."); Ex. 1026, 1 ("several conditions must be met" to cause latchup). For example, in my opinion, a POSITA would have understood that latchup is dependent upon parasitic bipolar devices associated with the NMOS and PMOS structures of typical CMOS. The latchup phenomenon was first described in 1973 in a paper by Gregory and Shafer (Ex. 1026) and has been analyzed in more detail in numerous publications and books since that time. The simplified figure below is commonly used to illustrate the basic issue. The circuit on the right is a redrawing of the circuit super imposed on the device structure shown on the the left.



If there is enough current (and associated voltage drop) through Rsub and/or Rwell, and the current gain through the parasitic bipolar transistors is greater than 1, the cross coupled parasitic bipolar devices create a self-sustaining current that will flow through the circuit between VDD and VSS. That condition is known as latchup. This condition is avoided if the current gain of the parasitic bipolar devices is reduced, typically by increasing spacing as was well-known in the art and described in Wolf. Ex. 1008B, 381 ("Latchup tolerance can [] be improved by spacing *n*- and *p*-channel transistors farther apart"). The Rsub and Rwell resistors can be reduced by increasing dopant densities or using retrograde wells. Currents which lead to latchup can also be removed from the structure via additional well and substrate contacts and/or the addition of guard rings. Ex. 1008B, 419 ("Increasing the number of well contacts to V_{DD} reduces latchup susceptibility" and thus "can serve as an alternative approach to improving latchup immunity.") If these steps are taken, as was well-

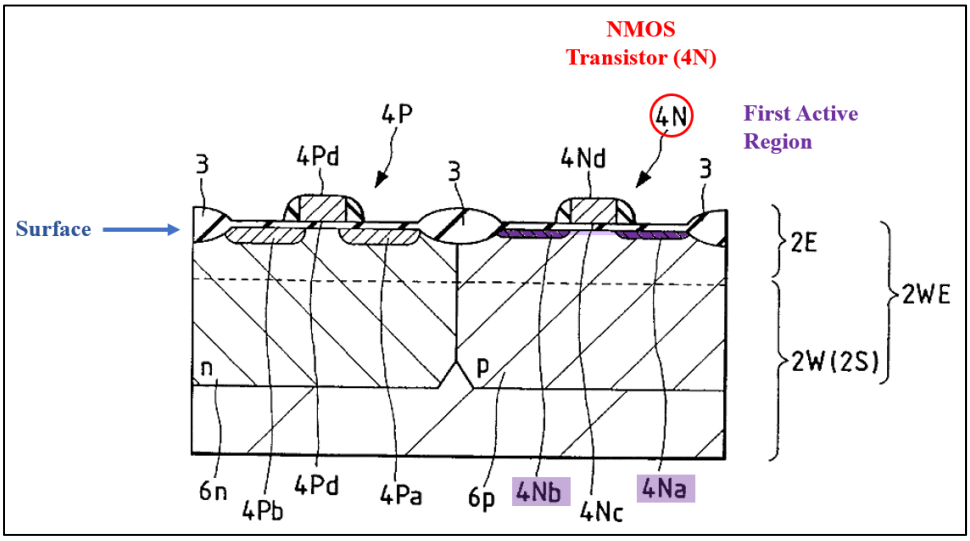
known in the art and described in Wolf, a chip can be fabricated on an epitaxial substrate that is uniformly doped, whereby the bulk substrate 2S and epitaxial layer 2E are doped at the same level, as described in Kawagoe's Embodiment 1, without being susceptible to latchup.

80. My opinion is also grounded in the well-known fact that twin-well CMOS devices were commonly fabricated on uniformly-doped bulk substrates that provide no improved latchup resistance. Ex. 1008B, 387-388 ("With the [twin-well] approach, … [t]he substrate may be [] a lightly doped wafer …"). And as I described above, even if latchup were to remain a concern, a POSITA would have understood, in my opinion, that improved latchup resistance can be achieved by other means unrelated to the choice of substrate, such as through careful circuit layout. Ex. 1008B, 381 ("Latchup tolerance can [] be improved by spacing *n*- and *p*-channel transistors farther apart"), 419 ("Increasing the number of well contacts to V_{DD} reduces latchup susceptibility" and thus "can serve as an alternative approach to improving latchup immunity.").

c. Elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2]: "a first active region disposed adjacent [the/to a] surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof];"

81. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. Kawagoe discloses "semiconductor regions 4Na and 4Nb … for

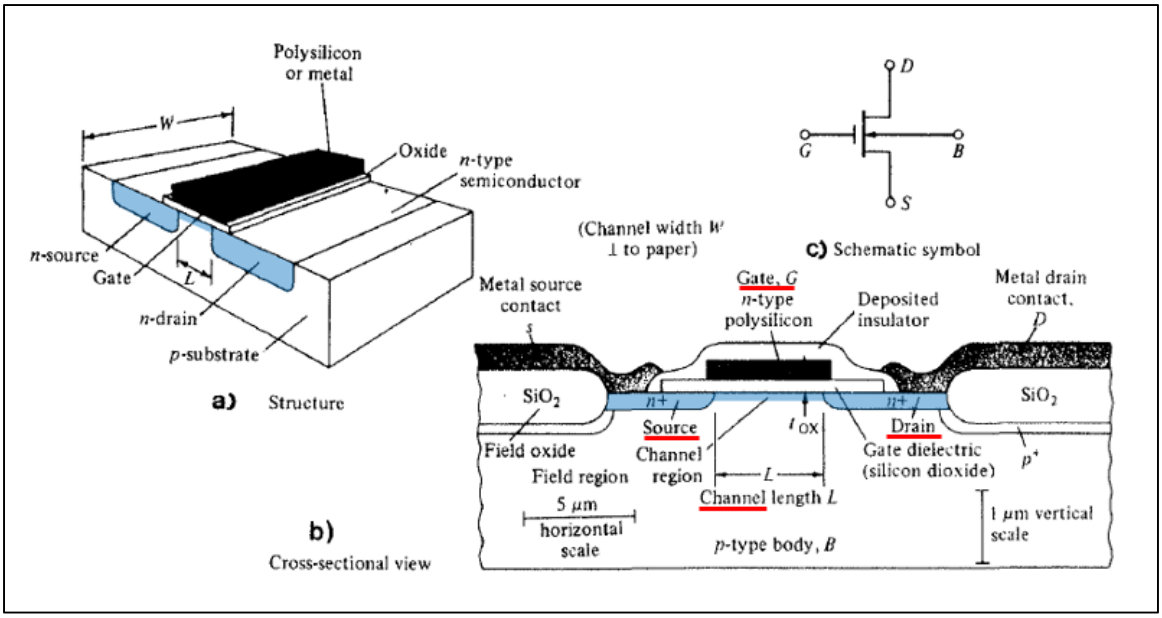
forming the ***source-drain regions*** of the nMOS [n-channel transistor] 4N." Ex. 1007, 8:66-67; *id.*, 3:35-37, 8:46-52, 14:46-55, 15:26-40. Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc. *Id.*, 8:46-65, 14:46-55, 15:26-40; Ex. 1008B, 299-300 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e). As shown in Figure 23, nMOS transistor 4N is formed in the surface of the first active region, which is adjacent the surface of the substrate.



Ex. 1007, FIG. 23. "[S]emiconductor regions 4Na and 4Nb are doped with an n-type impurity" and thus have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate. *Id.*, 8:67-9:3, 14:46-55, 15:26-40.

82. While Figure 23 above illustrates an exemplary nMOS (n-channel) transistor 4N formed in the first active region, in my opinion, a POSITA would have understood that Kawagoe teaches forming multiple nMOS transistors in this region to minimize chip area, as good layout practice dictates. Ex. 1014, 1:52-54, 2:17-21. Regardless, according to Patent Owner, an "active region … within which transistors can be formed" means "an active region … where ***a transistor*** can be formed." Ex. 1020, 31.

83. In my opinion, Kawagoe satisfies elements [1.3]/[21.3]/[39.2]/[41.2]/[42.2] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex. 1020, 20; *see also* Section VIII. This is consistent with a POSITA's understanding, and Wolf's teaching, that an active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions," highlighted in blue in the figure below. Ex. 1008B, 299.



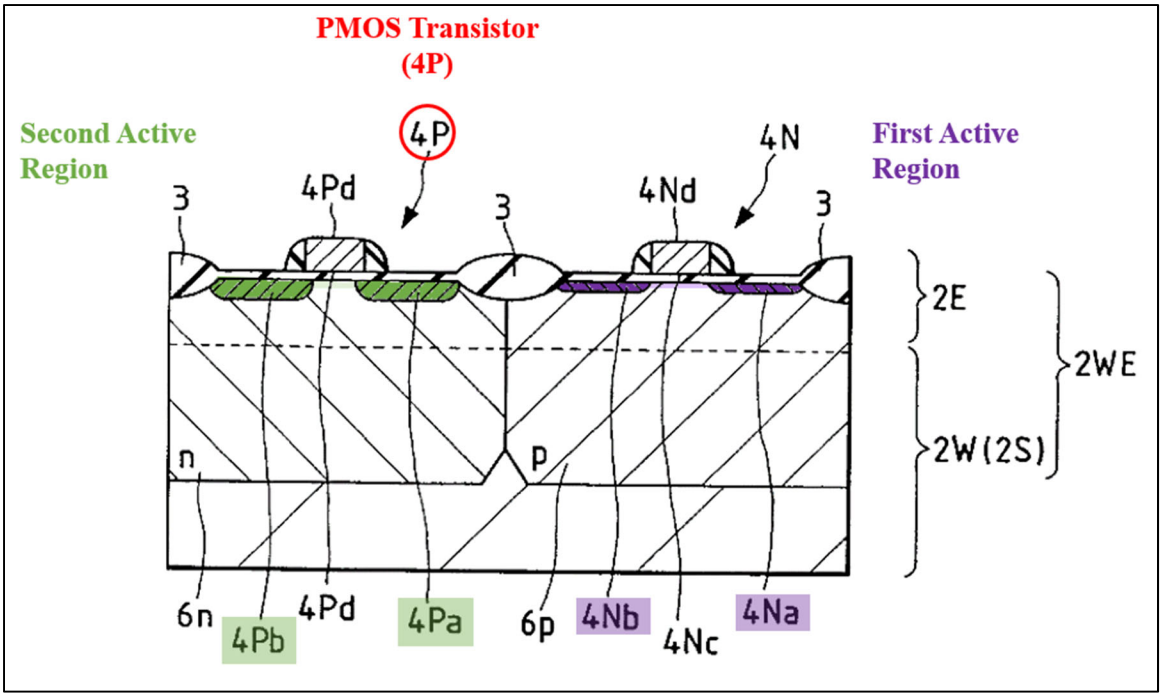
Ex. 1008B, FIG. 5-1; *see also id*., 298-301, FIGS. 5-2, 6-4.

84. It is also my opinion that Kawagoe also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). *See* Section VIII; Ex. 1008B, 299-301, FIGS. 5-1, 5-2. It is also common usage in the art to refer to the active region as the region defined by the thin oxide mask, which also includes the channel and the source-drain regions. In my opinion, Patent Owner agrees with this, as, in the District Court Case, Patent Owner represented that "when a positive voltage is applied to the gate … a conductive channel [is formed] between the source and the drain, and current can begin to flow through the transistor." Ex. 1020, 3-4.

d. Elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof];"

85. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. Kawagoe discloses "semiconductor regions 4Pa and 4Pb … for forming the source-drain regions of the pMOS [p-channel transistor] 4P." Ex. 1007, 3:35-37, 8:46-52, 9:41-48, 15:26-40. Source-drain regions 4Pa/4Pb (green) are part of the claimed second active region, which also includes the channel region (light green) between them and below gate 4Pd. Ex. 1007, 8:46-57, 9:41-46, 14:46-55, 15:26-40; Ex. 1008B, 299-301, FIGS. 5-1, 5-2, 6-4; Section X.A.1.c. As shown in Figure 23, pMOS transistor 4P is formed in the surface of the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex. 1007, 14:46-55.

86. In my opinion, a POSITA would understand that adjacent active regions are separated by an isolation region (e.g., insulating film 3). Ex. 1008A, 818-20, FIG. 16-11(f). In fact, claim 6 (depends from claim 1) recites, "the first active region and second active region are each separated by at least one isolation region." Ex. 1001, Cl. 6.



Ex. 1007, FIG. 23.

87. While Figure 23 illustrates an exemplary pMOS transistor 4P formed in the second active region, in my opinion, a POSITA would have understood that Kawagoe teaches forming multiple pMOS transistors in this region. Section X.A.1.c. Regardless, I understand that according to Patent Owner, an "active region … within which transistors can be formed" means "an active region … where ***a transistor*** can be formed." Ex. 1020, 31.

88. In my opinion, Kawagoe satisfies elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (e.g., the source and drain and silicon between them) where a transistor can be formed." Section X.A.1.c. In my opinion, Kawagoe also satisfies this claim element in my

opinion under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device." *Id.*

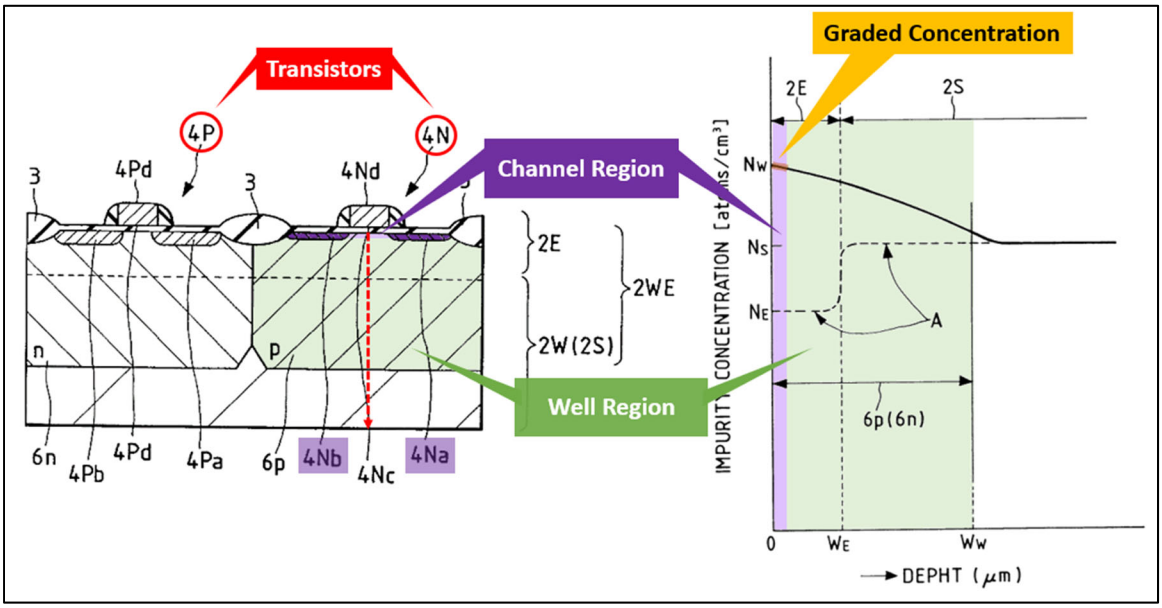
e. Elements [1.4]/[21.4]/[39.4]/[41.4]/[42.4]: "transistors formed in at least one of the first active region or second active region;"

89. In my opinion, Kawagoe discloses or, at a minimum, renders obvious these elements. *See* Sections X.A.1.c-d.

f. Elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5]: "at least a portion of at least one of the first and second active regions having at least one graded [dopant/dopant acceptor/donor dopant] concentration to aid carrier movement from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]; and"

90. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. As illustrated in Figure 23 (below left), a channel region (light purple) formed at the top surface of the substrate connects the source-drain regions 4Na and 4Nb (purple) of transistor 4N. *See* Ex. 1008B, 298 ("A channel region in the semiconductor under the gate electrode separates the source and drain"), 300-301 ("When positive bias is applied to an NMOS transistor gate … an *n*-type ***channel*** connects the ***source*** and ***drain*** regions"), FIG. 5-2; Ex. 1007, 8:60-67, 14:46-55,

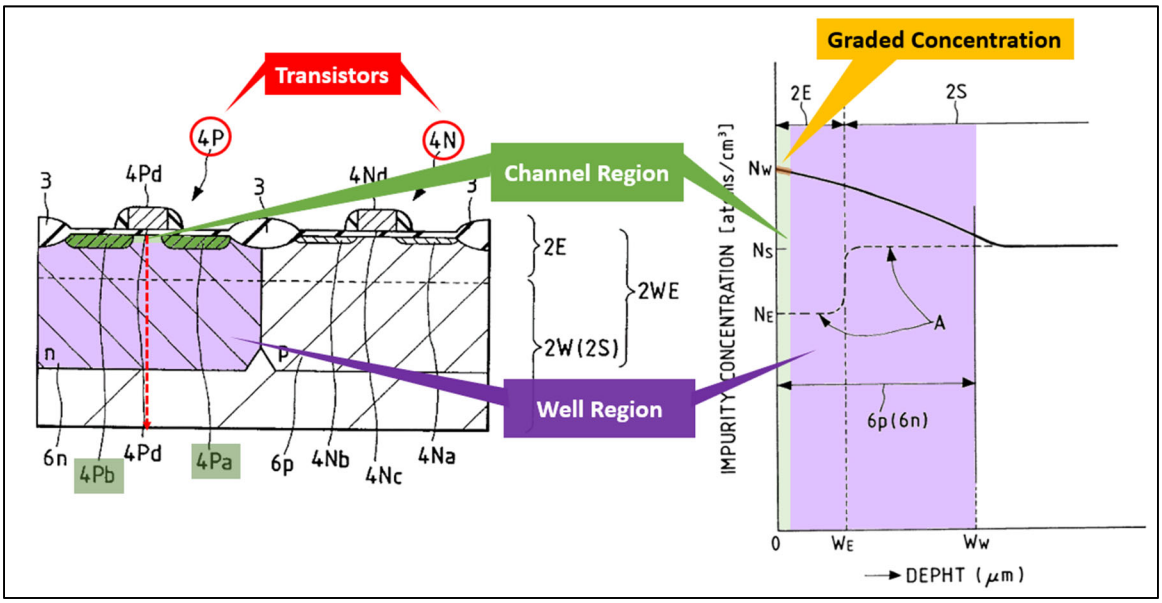
15:26-30, 15:37-40. In my opinion, Patent Owner does not dispute this. Ex. 1020, 4 (the channel is "a thin layer below the surface" connecting the source and drain).



Ex. 1007, FIGS. 17, 23.

91. Kawagoe's Figure 17 (above right) illustrates the doping concentration measured along the red dotted line in Figure 23 (above left), which starts from the top surface of the substrate (depth=0) and includes the doping profile in the channel region (light purple). *Id.*, 5:41-45. As Figure 17 shows, the dopant concentration is "gradually lowered in the depthwise direction ***from the principal surface*** (having an impurity concentration N_W) of the epitaxial layer 2E." *Id.*, 15:62-16:40. The dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at "the principal surface" of epitaxial layer 2E.

92. In my opinion, the same applies to the channel region of pMOS transistor 4P (a portion of the second active region), as illustrated below. Ex. 1007, 15:62-16:2 ("p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface [] of the epitaxial layer 2E."), 9:41-48, 14:46-55, 15:32, 15:37-40; Ex. 1008B, 298-301, FIGS. 5-2, 6-4.



Ex. 1007, FIGS. 17, 23. Thus, in my opinion, Kawagoe discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration.

93. In my opinion, Kawagoe satisfies elements [41.5] and [42.5]. Element [41.5] claims a "graded dopant ***acceptor*** concentration." The graded channel region of Kawagoe's first active region "is doped with a p-type impurity such as boron." Ex. 1007, 15:28-29; Section X.A.9. Boron is an acceptor dopant. Ex. 1037, 30. Element [42.5] claims a "graded ***donor*** dopant concentration." The graded channel

region of Kawagoe's second active region "is doped with an n-type impurity such as phosphor." Ex. 1007, 15:30-32; Section X.A.9. Phosphor is a donor dopant. Ex. 1037, 27.

94. Kawagoe further explains that such downward-sloping graded dopant concentration aids the movement of carriers from the first and second active regions towards/to the bottom of the substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6*p* is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

Ex. 1007, 16:2-11.[6]

95. During a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active region at the

[6] Kawagoe states that "electrons produced by the α-ray [are]… prevented from entering the p-well 6*p* …." Ex. 1007, 16:7-9. This refers to electrons produced in the large substrate body below the wells, by far the largest volumetric region of any chip. *See* Ex. 1009, FIG. 2.

surface of the substrate. Ex. 1009, 431 ("A[n] [α-]particle can induce SEU when it strikes at the ***channel region*** of an off transistor …"), FIG. 2. Kawagoe teaches that those carriers are "attracted to the substrate body by [the] concentration gradient" of the graded dopant concentration illustrated in Figure 17. Ex. 1007, 16:2-11.

96. In my opinion, Kawagoe satisfies elements [21.5]/[39.5]/[41.5]/[42.5] for the reasons discussed above.

97. In light of the above, it is my opinion that Kawagoe satisfies elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. *See* Section VIII. I understand that, according to Patent Owner's representations in the District Court Case, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)" and "when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction …." Ex. 1020, 2, 29. Here, Kawagoe's Figure 17 shows that the dopant concentration is downward-sloping with increasing depth towards/to the bottom of the substrate where there are no active regions, and thus, according to Patent Owner (and also in light of Patent Owner's representation to the Patent Office, discussed in X.A.1.g), causes carriers to move deeper into the substrate as well.

98. It is also my opinion that Kawagoe satisfies these claim elements under Petitioner's alternative proposed construction that the term means "to sweep the

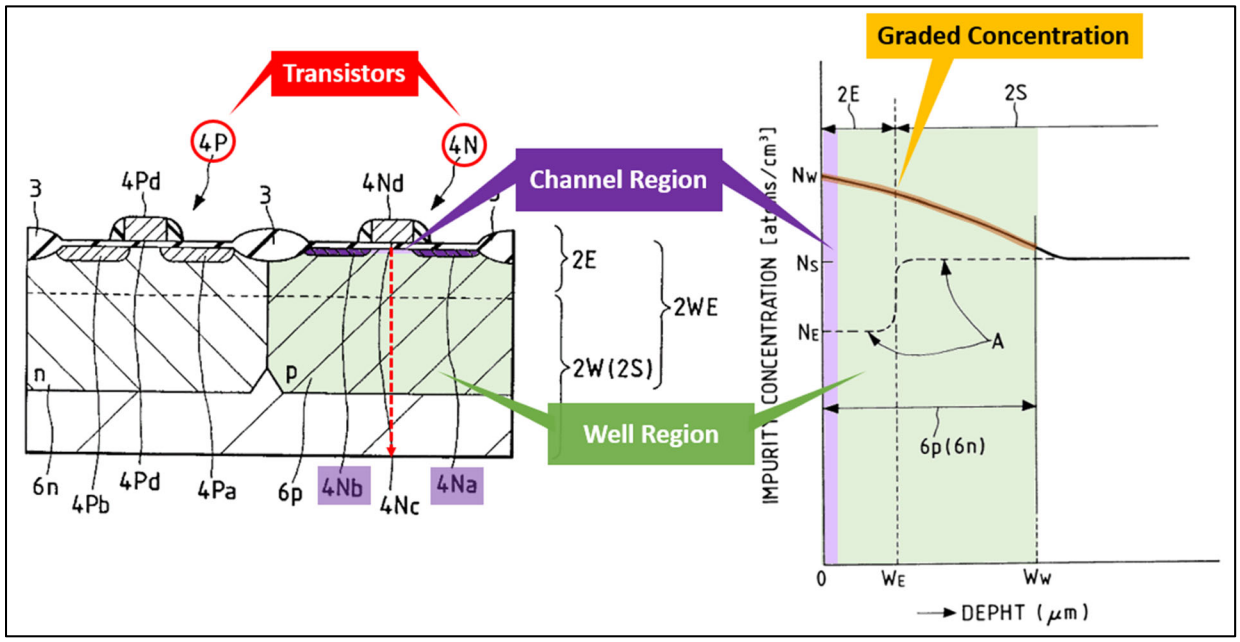
carriers from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]." *See* Section VIII. Kawagoe's Figure 17 illustrates a downward-sloping graded dopant concentration and Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers down into the substrate (where there are no active regions), as detailed below in Section X.A.1.g. Ex. 1016, 289-290.

g. Elements [1.6]/[21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions,"

99. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. As shown in Figure 23 (below left), Kawagoe discloses "a p-well 6p" (light green) adjacent to the first active region (purple/light purple). Ex. 1007, 8:66-67, 14:46-55, 15:26-40.

100. In addition, as discussed above and as shown in the dopant concentration profile (brown) of Figure 17 (below right), the dopant concentration in p-well 6p—measured along the exemplary red dotted line in Figure 23—gradually decreases with depth. Section X.A.1.f; Ex. 1007, 14:46-55, 15:62-16:40 ("p-well 6p

and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E"), 16:11-15. Thus, Kawagoe discloses a well region containing at least one graded dopant region (*e.g.,* the region highlighted in light green in both Figures 23 and 17) having a downward-sloping graded dopant concentration.



Ex. 1007, FIGS. 17 and 23.

101. Kawagoe further explains that this downward-sloping graded dopant concentrations aid carrier movement from the surface of the epitaxial layer towards or to an area of the substrate where there are no active regions:

> [T]he impurity concentration of the p-well 6p is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is

> lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.

Ex. 1007, 16:2-11.

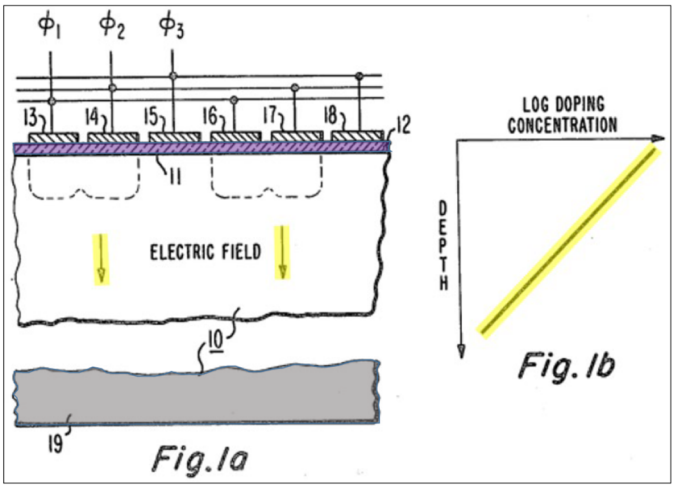
102. In my opinion, Kawagoe's teaching is consistent with Applicant's representation to the Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Kawagoe, would move carriers in the opposite direction towards the surface):

> [T]he graded dopant concentration <u>itself</u> creates a ***'built-in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

Ex. 1016, 289-290 (underlining in original). Applicant also represented that "a unidirectional drift (electric) field necessarily affects ***all*** the present minority carriers in the same way…. Depending on the particular slope of the graded concentration of dopant, ***all*** minority carriers are either ***swept*** 'down' … or 'up.'" Ex. 1016, 289.

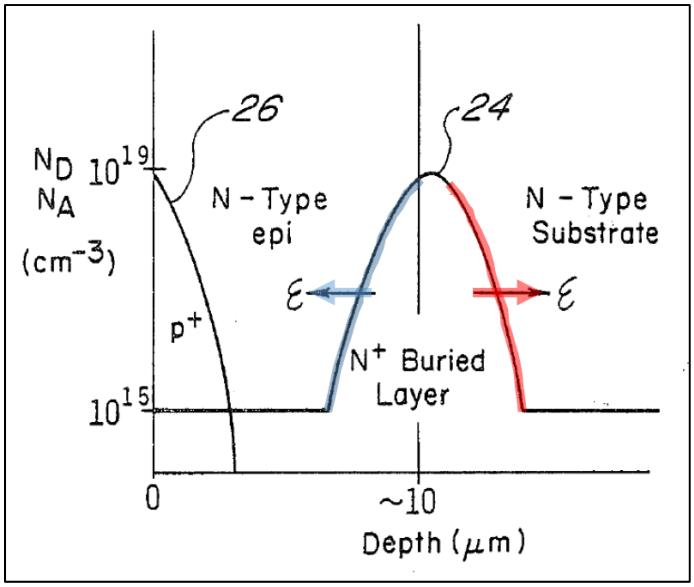
103. Applicant cited Jastrzebski in support. *See* Ex. 1016, 290. In Jastrzebski, the doping concentration is "decreasing with depth" from the top surface

11 (purple) of the substrate 10, as shown in Figure 1b below. Ex. 1010, 5:14-22. Jastrzebski teaches that this downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers … ***deep into the substrate***[.]" *Id.*, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b.

104. Applicant made the same representation to the Patent Office regarding Kamins. Ex. 1016, 237-238. According to Applicant, Kamins' Figure 3 shows "two electric fields with opposing directions" (highlighted in blue and red) that correspond to increasing and decreasing graded dopant concentrations, respectively. *Id.*, 237 (citing Ex. 1031, 3:6-13). Applicant explained that the electric field associated with the downward-sloping graded concentration at depth beyond ~10μm (red) causes "carriers created [in that region to be] … ***accelerated into the substrate*** …." *Id.* (citing Ex. 1031, 3:6-13, FIGS. 2-3).



Ex. 1031, FIG. 3.

105. In my opinion, and in light of the above, Kawagoe satisfies elements [1.6]/[21.6] under Patent Owner's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex. 1020, 30; Section VIII. As shown in Figure 23 above, p-well 6p (light green) is a doped region that surrounds the first active region (purple/light purple). Kawagoe also satisfies elements [1.6]/[21.6], in my opinion, under Patent Owner's plain meaning construction of the "to aid carrier movement" term. Section VIII.

106. It is also my opinion that Kawagoe also satisfies this claim element under Petitioner's proposed constructions of these terms. *See* Section VIII. The mapping of "well region" to Kawagoe's p-well 6p satisfies Petitioner's construction of the term because p-well 6p is formed by implanting ions of "a p-type impurity such as boron." Ex. 1007, 17:43-49; Section VIII. With regard to the "aid carrier

movement" term, Kawagoe satisfies Petitioner's alternative proposed construction that the term means "to sweep the carriers from the surface [towards/to] the area of the substrate where there are no active regions." *See* Section VIII. Indeed, as discussed in Wang and as was well understood in the art, an α-ray generates a stream of millions of carriers (*e.g.,* electrons) that can cause single-event upset (SEU) soft errors. Ex. 1009, 431, FIG. 2; Section X.A.1.f.

107. Kawagoe explains that the graded dopant concentration illustrated in Figure 17 reduces soft errors by sweeping those carriers towards or to the bottom of the substrate where there are no active regions. Ex. 1007, 16:2-11.

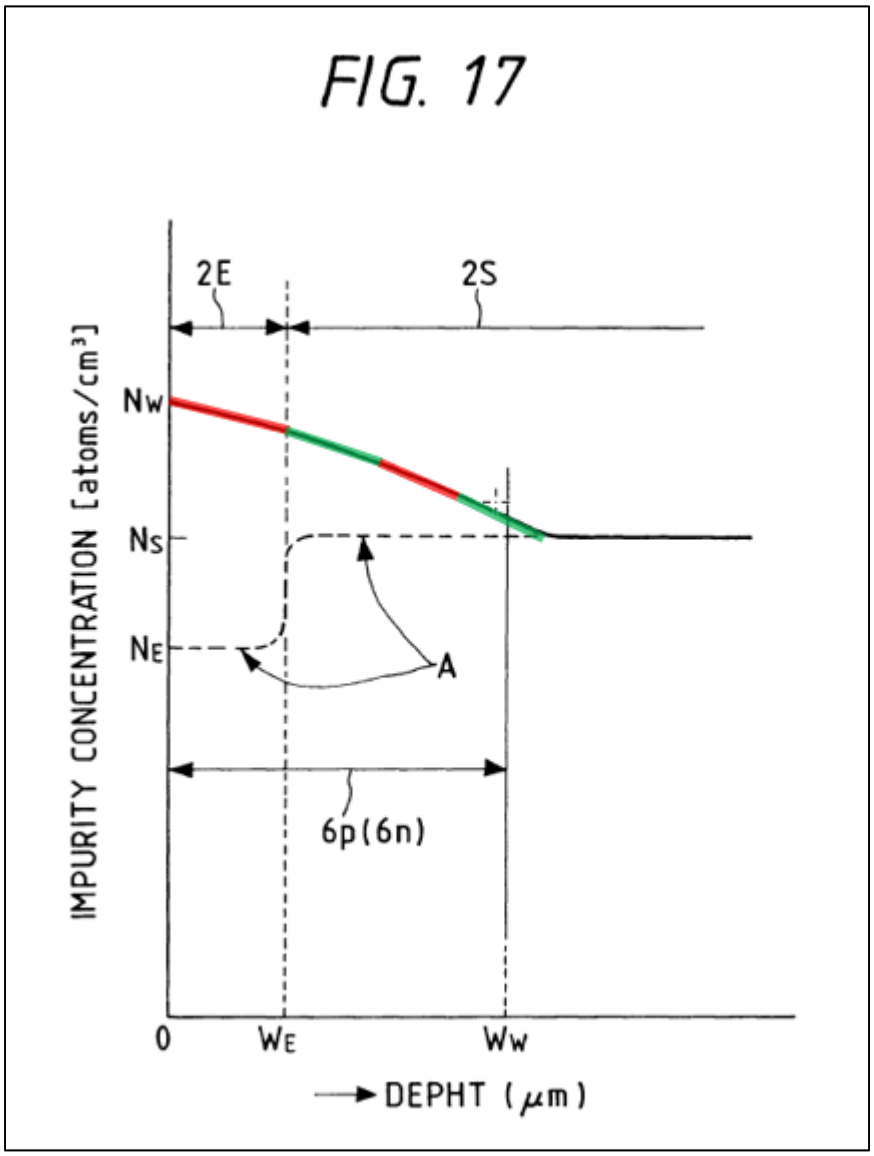
h. Element [1.7]: "wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

108. In my opinion, Kawagoe teaches that the transistors in its active regions form digital logic in teaching that they form "a CMOS … circuit" and that its "techniques … can … be applied to … a ***logic circuit*** such as [a] 'microcomputer'" and to a "peripheral circuit region of DRAM and flash memory." Ex. 1007, 8:46-52, 14:46-55, 15:26-40, 20:1-33, 22:10-29, 22:51-23:2, 24:28-31; Ex. 1008A, 810-811 (CMOS used "***to form low-power IC logic gates***").

i. Element [21.7]: "wherein the graded dopant concentration is linear, quasilinear, error function,

complementary error function, or any combination thereof."

109. In my opinion, as shown below, the graded dopant concentration is linear or nearly linear (quasilinear). It is also a combination of linear/quasilinear segments, illustrated in red and green; as the segments get smaller, they become even more linear/quasilinear. *Id.*



Ex. 1007, FIG. 17.

2. Claims 2/23: "The VLSI semiconductor device of claim [1/21], wherein the substrate is a p-type substrate."

110. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 2 and 23. *See* Section X.A.1.b.

3. Claims 3/24: "The VLSI semiconductor device of claim [1/21], wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate."

111. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 3 and 24. *See* Section X.A.1.b.

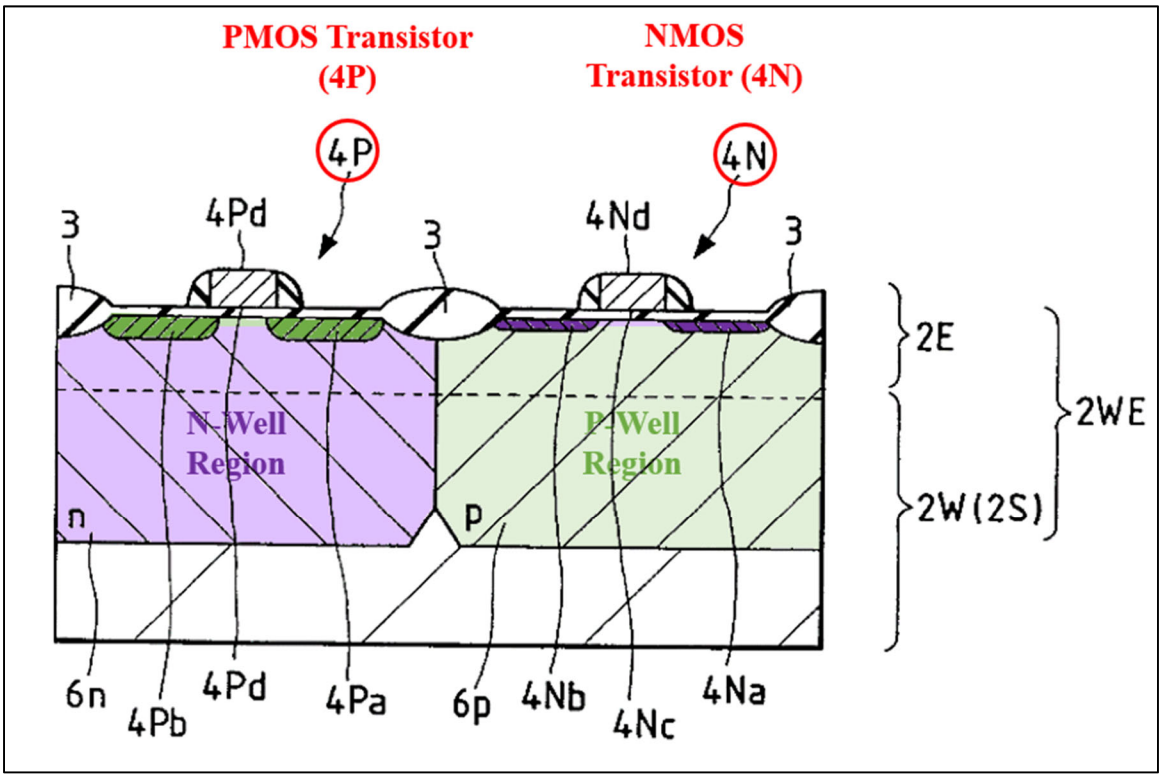
4. Claims 4/25: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain [digital logic formed by/at least] one of either p-channel and n-channel devices."

112. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 4 and 25. *See* Sections X.A.1.c-e, X.A.1.h.

5. Claims 5/26: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

113. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 5 and 26. Kawagoe's Figure 23 illustrates a conventional twin-well architecture, whereby the first active region contains nMOS (n-channel) transistor 4N) formed in "p-well 6p" and the second active region contains pMOS (p-channel) transistor 4P formed in "n-well 6n." Ex. 1007, 8:46-52, 14:46-55, 15:26-43; Sections X.A.1.c-d; Ex. 1008B, 387-88.

114. In my opinion, this mapping satisfies this claim under Patent Owner's interpretation that an active region in the claims can contain only "***a transistor***." Ex. 1020, 31. A POSITA would have also understood that Kawagoe teaches forming multiple transistors in an active region to save chip area, as good layout practice dictates. Ex. 1014, 1:52-54, 2:17-21.

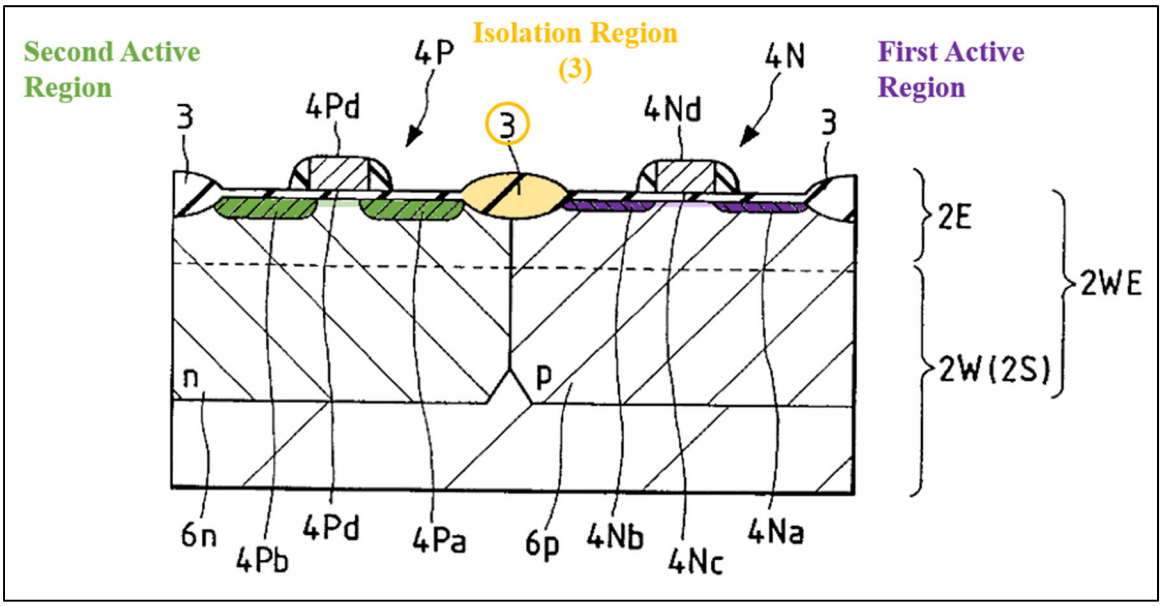


Ex. 1007, FIG. 23.

115. Further, in my opinion, Kawagoe's n-wells and p-wells have graded dopants. *Id.*, 14:46-55, 15:62-16:2 ("as shown in FIGS. 16 and 17, …the p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E."); Section X.A.1.g (discussing the graded dopants in p-well 6p).

6. Claims 6/27: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region are each separated by at least one isolation region."

116. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 6 and 27. As shown below, the first (purple/light purple) and second active regions (green/light green) are separated by "field insulating film 3" (claimed "isolation region") (yellow). Ex. 1007, 8:40-52, 15:37-40, 17:62-18:8; Ex. 1008A, 818-20, FIG. 16-11(f).



Ex. 1007, FIG. 23.

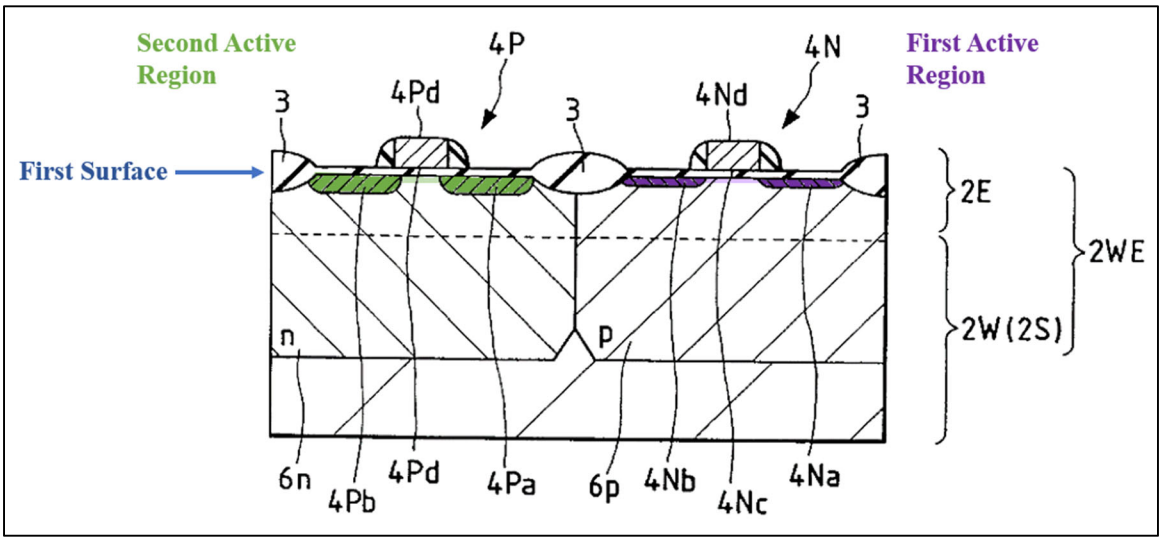
7. Claims 7/32: "The VLSI semiconductor device of claim [1/21], wherein the graded dopant is fabricated with an ion implantation process."

117. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 7 and 32. In my opinion, Kawagoe discloses that the graded dopants in n-well 6n and p-well 6p are "formed by the ion implantation

method." Ex. 1007, 4:11-12, 15:26-36, 17:10-12, 17:31-39 (n-well 6n formed by implanting "ions of an n-type impurity such as phosphor"), 17:43-49 (p-well 6p formed by implanting ions of "a p-type impurity such as boron"); Sections X.A.1.f-g.

8. Claim 8: "The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate."

118. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 8. In my opinion, and as shown below, Kawagoe discloses that the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex. 1007, 8:66-9:6, 9:47-54, 15:37-40, 17:10-12, 17:31-18:35; Ex. 1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions…."), 298, 300-301, FIG. 5-2; Sections X.A.1.c-d.

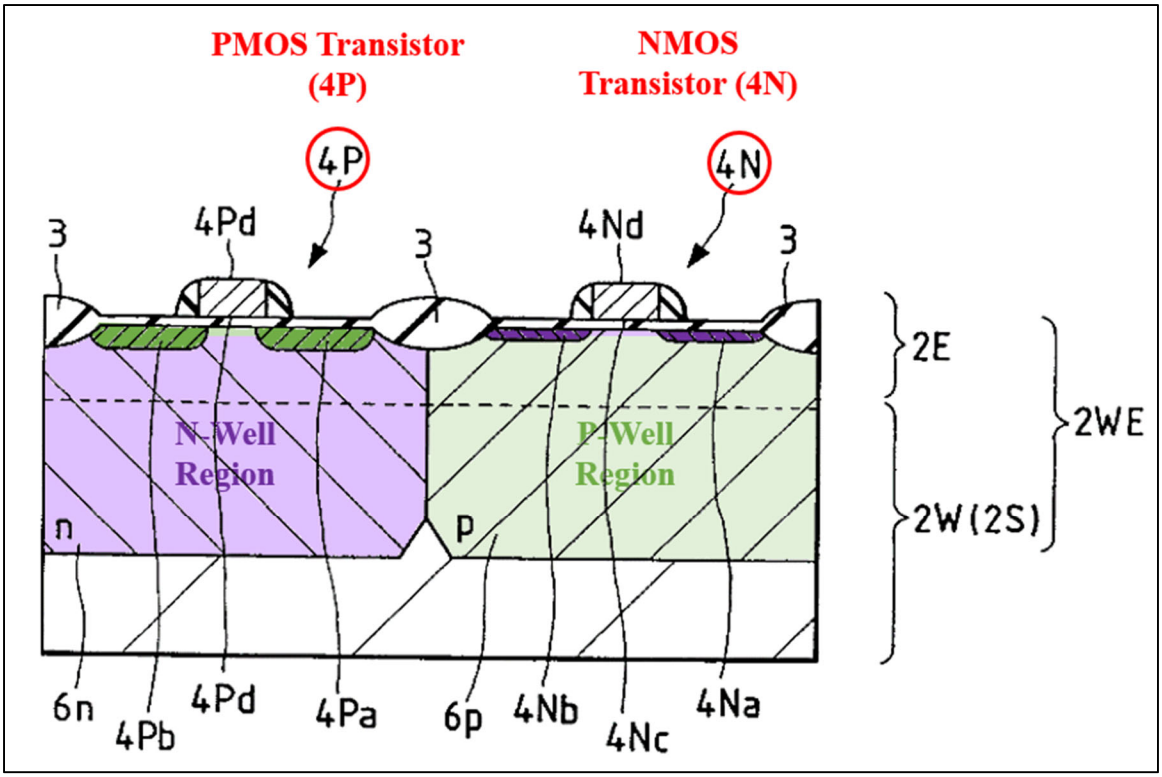


Ex. 1007, FIG. 23.

9. Claims 9/28: "The VLSI semiconductor device of claim [1/21], wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type."

119. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 9 and 28. In my opinion, as discussed above and shown in Figure 23 below, the channel region (light purple) of the first active region—between source-drain regions 4Na/4Nb and below insulating film 4Nc—formed at the top of p-well 6p is of the same doping type (p-type) as p-well 6p. Ex. 1007, 15:26-36 ("The p-well 6p is doped with a p-type impurity such as boron."); *id.*, 17:10-12, 17:43-49.

120. Likewise, in my opinion, the channel region (light green) of the second active region—between source-drain regions 4Pa/4Pb and below insulating film 4Pc—formed at the top of n-well 6n is of the same doping type (n-type) as n-well 6n. Ex. 1007, 15:26-36 ("n-well 6n is doped with an n-type impurity such as phosphor"), 17:10-12, 17:33-39.

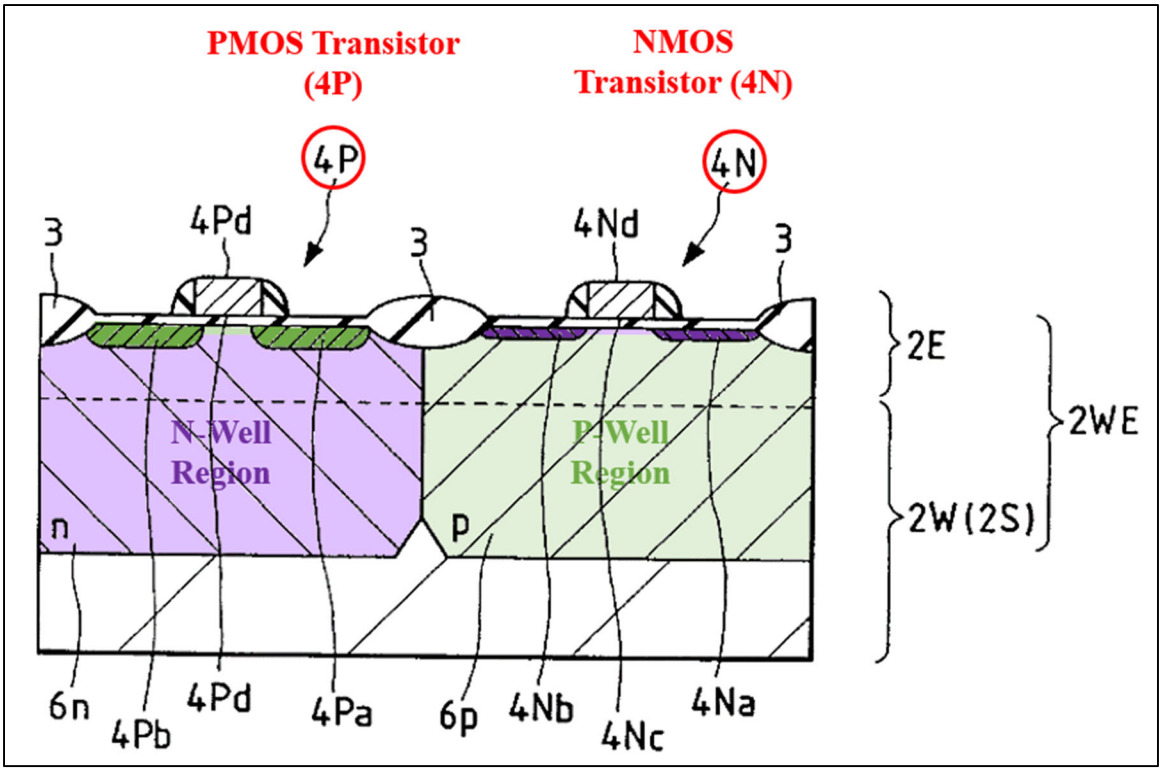


Ex. 1007, FIG. 23.

121. In my opinion, those channel regions have graded dopant concentrations. Section X.A.1.f.

10. Claim 13: "The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel."

122. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 13. In my opinion, Kawagoe teaches an nMOS transistor 4N formed in the first active region and a pMOS transistor 4P formed in the second active region, which are CMOS digital logic transistors. Ex. 1007, 8:45-52, 14:46-55, 15:37-40; Section X.A.1.h.



Ex. 1007, FIG. 23.

123. Each of the CMOS digital logic transistors includes a source, drain, gate, and channel. The nMOS transistor 4N includes "source-drain regions" 4Na/4Nb spaced apart by an "n-channel" region, and gate electrode 4Nd, and pMOS transistor 4P includes "source-drain regions" 4Pa/4Pb spaced apart by a "p-channel" region, and gate electrode 4Pd. Ex. 1007, 8:42-67, 9:41-48, 14:46-55, 15:37-40, FIG. 23; Sections X.A.1.c-d, X.A.1.f.

11. Claim 14: "The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)."

124. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 14. In my opinion, Kawagoe explains that

"embodiment 4" (Figures 16-17, 20-24), relied upon for claim 1, can be advantageously used to fabricate DRAM devices (having "MOS capacitors") with reduced soft errors, reduced defect density, and "excellent gate breakdown performance." Ex. 1007, 16:2-11 (explaining that the graded dopant concentration in p-well 6p (illustrated in Figure 17) moves "electrons produced by the α-ray" to the substrate body 2S so that "soft errors can be reduced in case … DRAM or the like is formed in the p-well 6p"), 19:15-23 ("the structure of the present embodiment 4 is applied to a 4M.DRAM"), 19:31-32, 19:43-48, 20:1-33 (DRAM with "transfer MOS.FET[s] [] and [] capacitor[s]" formed in accordance with embodiment 5, which uses Embodiment 4's downward sloping graded dopant concentration).

12. Claims 16/34: "The VLSI semiconductor device of claim [1/21], wherein the device is a flash memory."

125. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 16 and 34. In my opinion, Kawagoe teaches a semiconductor flash memory device. Ex. 1007, 22:14-18 ("The semiconductor integrated circuit device 1 of the present embodiment 7, as shown in FIG. 28, is exemplified by a flash memory."). The flash memory device includes a CMOS "peripheral circuit region [] formed with the nMOS 4N and the pMOS 4P…." Ex. 1007, 22:51-23:2. This peripheral circuit is fabricated according to twin-well CMOS technology, whereby NMOS transistors (*e.g.*, 4N) are formed in "p-well 6p3," and PMOS transistors (*e.g.*, 4P) are formed in "n-well 6n2." *Id.*, 22:51-65, FIG. 28.

126. Kawagoe explains that the teachings of Embodiment 4 (relied upon in the claim mapping for claim 1) are applicable to Embodiment 7 and therefore, in my opinion, to flash memory. In particular, Embodiment 7 applies the teachings of Embodiment 4 relating to the use of an epitaxial substrate to form a twin-well architecture with pMOS transistor 4P formed in an n-well and nMOS transistor 4N formed in a p-well, where both wells have a downward-sloping graded dopant concentration. Ex. 1007, 22:22-29 ("In the present embodiment 7, too, the semiconductor substrate 2 is formed thereover with a p-well 6*p*3 and an n-well 6*n*2. The p-well 6*p*3 and n-well 6*n*2 are formed, ***as in the foregoing embodiments 4 and 6***, to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S. Moreover, their impurity concentrations are made gradually lower depthwise of the semiconductor region 2, ***as in the foregoing embodiment 4***."), FIG. 28.

13. Claim 17: "The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors."

127. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 17. *See* Sections X.A.1.h, X.A.11.

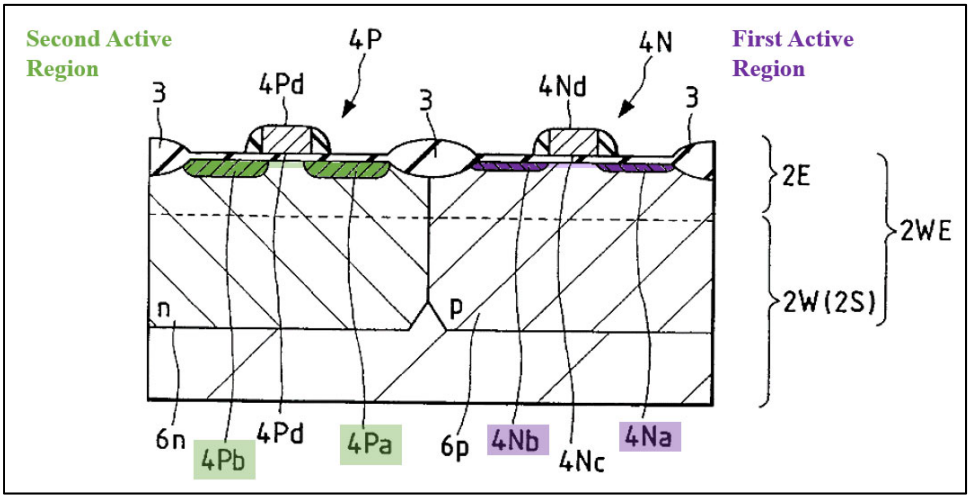
14. Claims 18/36: "The VLSI semiconductor device of claim [1/21], wherein the device is central processing unit."

128. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 18 and 36. In my opinion, Kawagoe teaches that

its disclosures can be applied to a "microcomputer." Section X.A.1.h. In my opinion, a POSITA would have understood that a microcomputer includes a central processing unit (CPU). Ex. 1032, 1334.

15. Claims 20/38: "The VLSI semiconductor device of claim [1/21], wherein each of the first and second active regions are in the lateral or vertical direction."

129. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 20 and 38. In my opinion, and as shown in Figure 23 below, the first (purple/light purple) and second (green/light green) active regions are in the lateral direction.



Ex. 1007, FIG. 23.

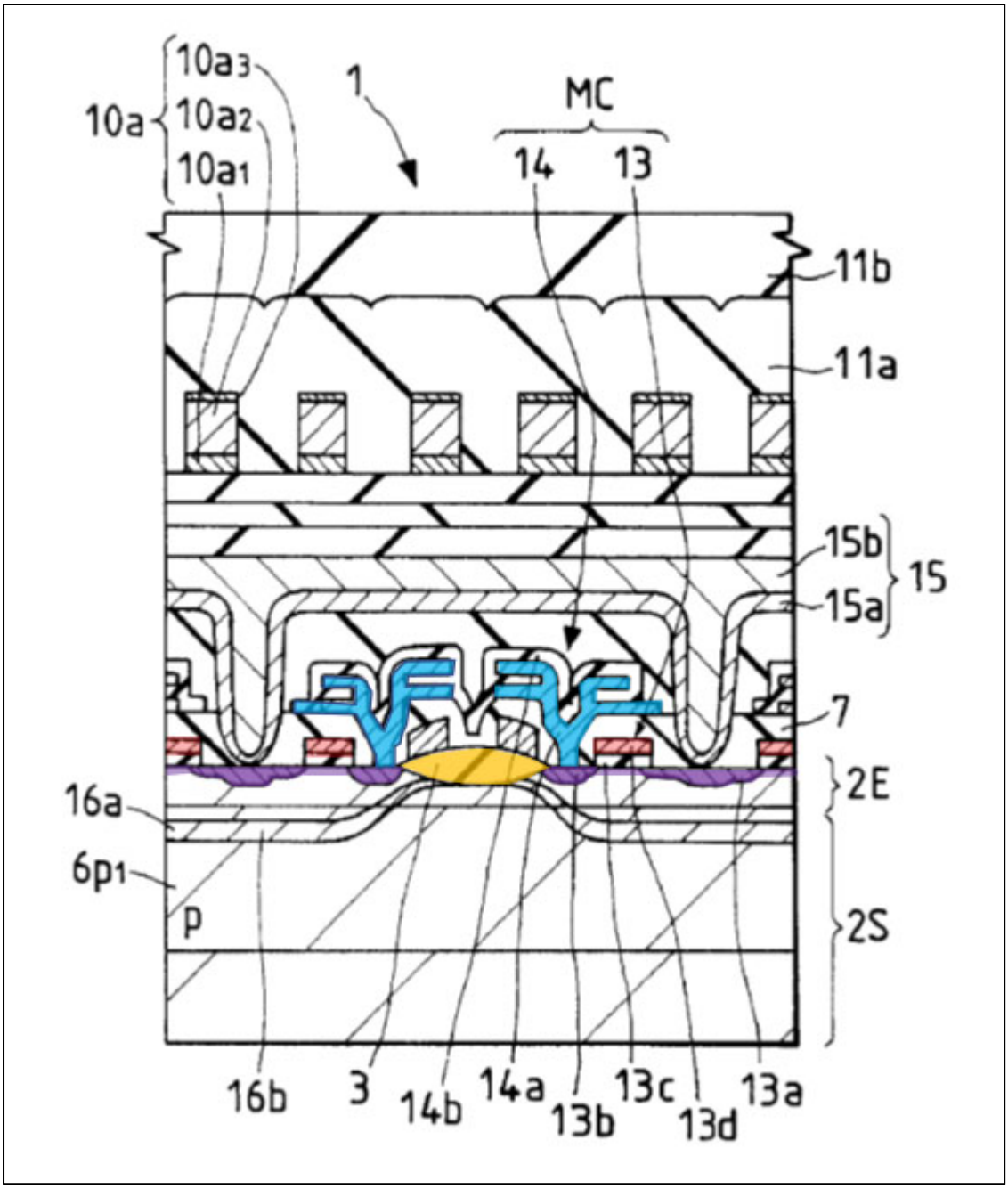
16. Claim 33: "The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device."

130. In my opinion, Kawagoe discloses this element or, at a minimum, renders it obvious. Kawagoe teaches that "nMOS 4N and pMOS 4P constitute a

CMOS" device formed in and including a substrate. Ex. 1007, 8:46-52, 15:26-40, 8:60-9:6, 9:41-54, 14:46-55; *see also* Section X.A.1.b.

17. Claim 35: "The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions."

131. In my opinion, Kawagoe discloses this element or, at a minimum, renders it obvious. Kawagoe's teachings apply to 16-Megabit DRAM logic devices. Sections X.A.1.a/h, X.A.11; Ex. 1007, 19:64-20:67. As shown below, capacitors 14 (blue electrodes) are in first and second n-type active regions (purple/light purple), which are adjacent the substrate surface and separate from and adjacent to one another, as described above. Ex. 1007, 20:12-28, 20:39-52; Sections X.A.1.c-d. Transistors 13 (red gates) are formed in the surface of each active region, the channel regions of which (light purple) have a graded dopant concentration to aid carrier movement, as described above. Ex. 1007, 20:12-28, FIG. 17; Sections X.A.1.c-f. P-well 6p1, adjacent the active regions, also has a graded dopant region to aid carrier movement, as described above. Ex. 1007, 20:12-28, FIG. 17; Section X.A.1.g.



Ex. 1007, Fig. 26(A).

132. In my opinion, to the extent the claim requires multiple first/second active regions, a POSITA would have understood Kawagoe to disclose this because Kawagoe's 16M DRAM has over 16 million memory cells (Figure 26A only shows

a small portion of them (*i.e.*, a few memory cells, each with transistor 13 and capacitor 14)). Ex. 1007, 20:1-14. Figure 26(A)'s DRAM also includes a peripheral circuit region with the same structure as Embodiment 4 and, therefore, additional first/second active regions. Ex. 1007, 20:1-8.

133. Further, MOS transistors are commonly used as capacitors to form dynamic circuits such as voltage bootstrapping circuits, charge pump circuits, delay/timing circuits, and to form decoupling capacitors ("decaps"). Hodges' figure below shows an NMOS transistor configured as a capacitor by connecting its gate to V_{DD} and its source/drain to V_{SS}. Ex. 1038, 493-494.

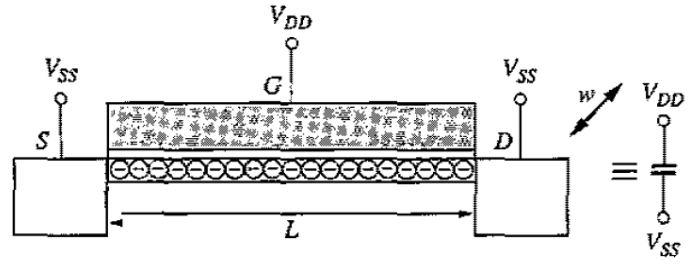


Figure 11.11
On-chip decap using MOS capacitance.

Id., FIG. 11.11. In my opinion, a POSITA would have understood (and found it obvious) that some of Kawagoe's transistors formed in some of the first/second active regions are configured as capacitors. For example, the voltage bootstrapping circuit below—a "very useful" and commonly used circuit—includes a transistor configured as a capacitor (C_{boot}) connected to other transistors (M1-M3). Ex. 1041, 370-373.

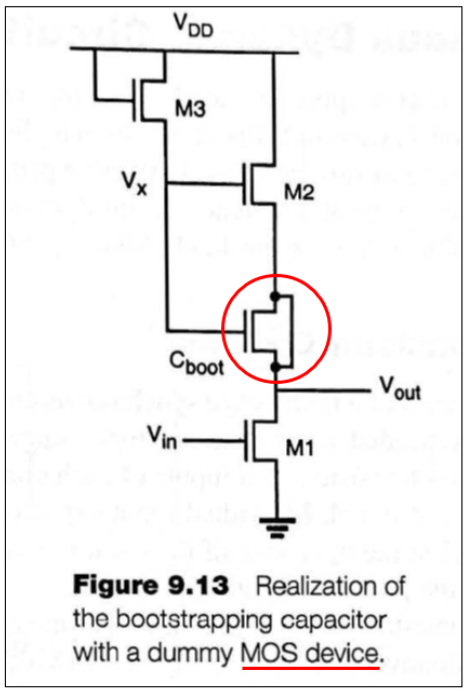


Figure 9.13 Realization of the bootstrapping capacitor with a dummy MOS device.

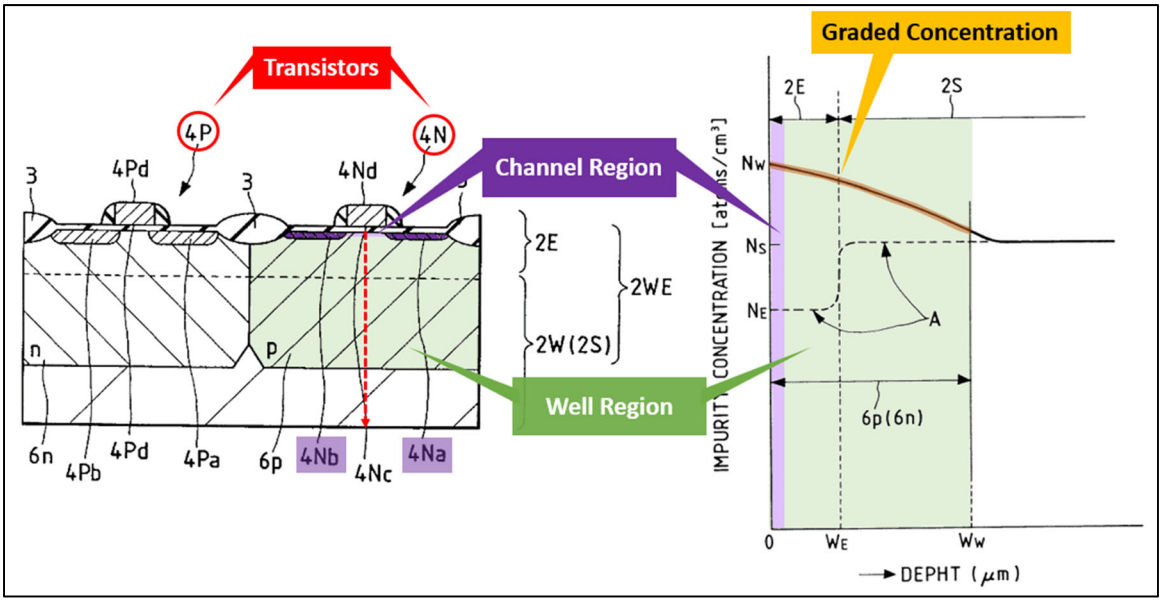
Id., Fig. 9.13. In my opinion, a POSITA would also find it obvious to configure transistors as decaps "scattered throughout the design" to filter out power supply noise and reduce "*IR* drop." Ex. 1038, 493 ("On-chip decoupling capacitors (decaps) are ***commonly used*** to keep the power supply within the noise budget, especially during peak demand periods in high-frequency switching operations."); *id.*, 498 ("The ***most effective approach*** [to reduce *IR* drop] is to use *decoupling capacitors* between power and ground … These decoupling caps are usually ***scattered*** throughout the design in any available space, using ***transistors*** with their gates tied to V_{DD} and their source-drain regions tied to Gnd.") (italics in original); *id.,* 499 ("you can never have enough" decaps). Doing so would have amounted to combining prior art elements (Kawagoe's devices and decaps) according to known

methods (scattering transistor decaps wherever available) and amounted to use of a known technique (scattering transistor decaps) to improve similar devices (Kawagoe's devices) in the same way (filter noise and reduce IR drop). *Id.* In my opinion, there is reasonable expectation of success with predictable results because the use of transistors as capacitors was a well-known, intended use of MOS transistors.

134. Moreover, there is a MOS capacitor inherent to every MOS gate or gate oxide structure built over an active region. *See* Ex. 1040, 116 ("At the heart of the MOSFET is the MOS capacitor structure depicted in Fig. 4.1."). This capacitor is formed by the gate, gate oxide, and active-region channel structure. *Id.* at 116-118 The gate is one plate and the active-region channel is the second plate of the capacitor. *Id.* As seen in Jaeger, the capacitor structure is taught as part of basic electronics pedagogy and is foundational to understanding MOS transistors. *See id.* In my opinion, many common uses of the MOS capacitor would have been obvious to a POSITA, including charge and information storage, bypass capacitance, filter elements, and delay elements. It is impossible to build MOS transistors without MOS capacitors and, in my opinion, it is hard to find a VLSI scale circuit that does not also include MOS capacitors as explicit circuit elements. In my opinion, this was well known to a POSITA at the time of the '222 patent and is fundamental to CMOS design.

18. Claim 40: "The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well."

135. In my opinion, Kawagoe discloses this element or, at a minimum, renders it obvious. Section X.A.1.g. As illustrated below, Kawagoe's graded dopant concentration is downward-sloping throughout each well (green) and moves carriers from any region of the well to deeper areas of the substrate where there is no well.



Ex. 1007, FIGS. 17/23.

B. Ground II:

136. In my opinion, Wieczorek in combination with Wolf (hereinafter, "Wieczorek-Wolf") renders claims 1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42 obvious.

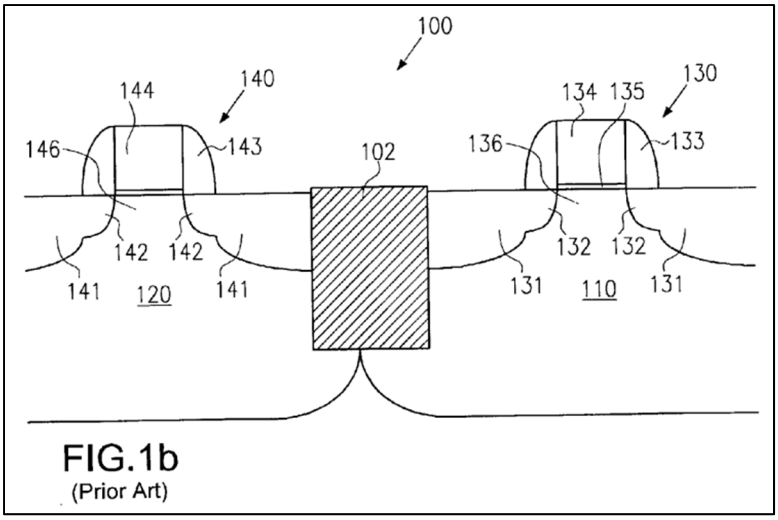
137. In my opinion, a POSITA would have been motivated to combine Wieczorek with Wolf. I rely herein on Wieczorek's description of a conventional prior-art CMOS device. *See, e.g.*, Ex. 1006, [0020]-[0021], [0004] ("Field effect transistors, such as MOS transistors, represent one of the most frequently used circuit elements in modem [*sic*] integrated circuits."), [0007]-[0008] (describing "[a] typical process flow for forming the semiconductor device 100" which is "a complementary MOS transistor pair"), [0012], FIG. 1b.

138. As discussed earlier, Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices. *See generally* Ex. 1008A; *id.*, Chapter 16 ("CMOS Process Integration"). In my opinion, a POSITA would have therefore understood and expected that the teachings of Wolf would apply to Wieczorek's conventional CMOS device. *Id.* A POSITA would have looked to Wolf for additional details related to conventional CMOS devices, as detailed below.

1. Claim 1/21/39/41/42

a. Preambles: "A [VLSI] semiconductor device, comprising:"

139. To the extent the preamble is limiting, in my opinion, Wieczorek discloses it or, at a minimum, renders it obvious. Wieczorek teaches a "semiconductor device 100." Ex. 1006, [0012]. Wieczorek's Figure 1b illustrates a conventional twin-well CMOS device. Section X.B.1.b.

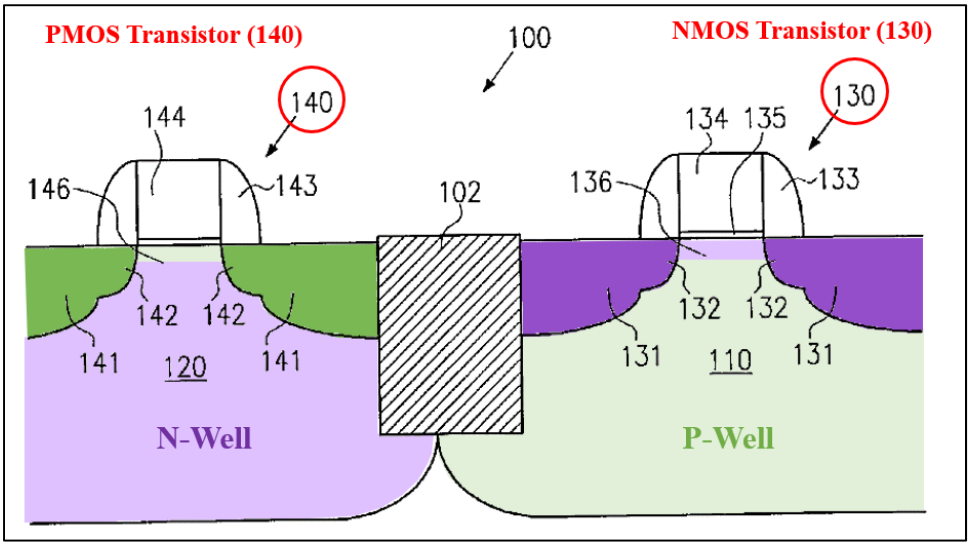


Ex. 1006, FIG. 1b. Wieczorek-Wolf renders obvious using Wieczorek's teachings to fabricate DRAM, microprocessor, and flash memory devices. Sections X.B.10/12/14. Wolf, which applies to "the VLSI Era," confirms that such devices at the time were understood to be VLSI devices having at least one million active elements. Ex. 1008A, cover, xxxiii, FIG. 1 (microprocessor with at least one million transistors); Ex. 1008B, 596-597 (1-Megabit CMOS DRAM with one transistor per memory cell, totaling at least one million transistors), 633-635 (1-Megabit CMOS flash EEPROM with one floating gate per memory cell and other transistors, totaling at least one million active elements); Ex. 1016, 73 (VLSI refers to "at least one million active elements").

b. Elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1]: "a substrate of a first doping type at a first doping level [having a surface];"

140. In my opinion, Wieczorek, alone or in combination with Wolf (hereinafter "Wieczorek-Wolf"), renders these elements obvious. Wieczorek's

Figure 1b illustrates a twin-well CMOS device, where N-channel transistor 130 (nMOS) with source/drain regions 131-132 (purple) and channel region 136 (light purple) is formed in P-well 110 (light green) and P-channel transistor 140 (pMOS) with source/drain regions 141-142 (green) and channel region 146 (light green) is formed in N-well 120 (light purple). Ex. 1006, [0007], [0012], [0020]-[0021]; Ex. 1008C, 525, FIG. 8-1(e).

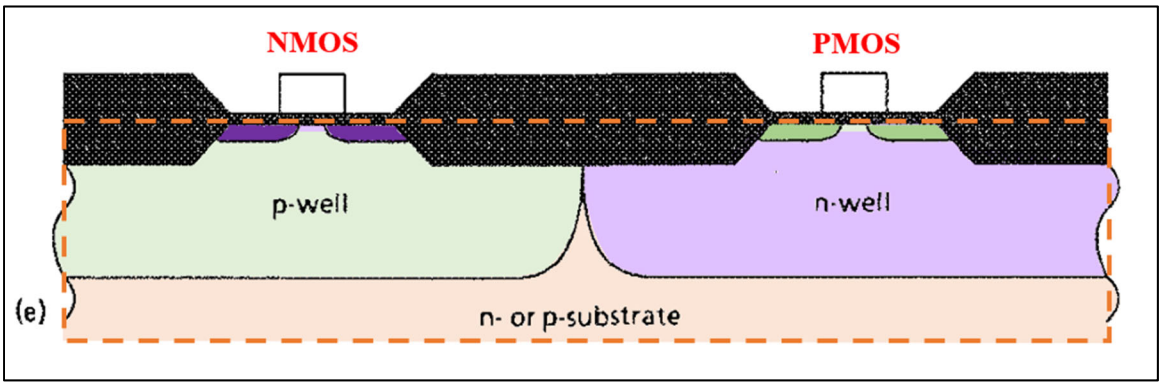


Ex. 1006, FIG. 1b (labelled as "Prior Art").

141. In my opinion, a POSITA would have understood that a twin well approach "is independent of starting material type" for the substrate. Ex. 1008C, 524; Ex. 1006, [0004] (discussing use of "an appropriate substrate" for forming MOS transistors without further specificity).

142. In my opinion, because Wieczorek does not specify what constitutes an appropriate substrate, a POSITA would have been motivated to consult Wolf, which

confirms that a "***uniform***, lightly doped *p*- or *n*-type substrate" is commonly used in twin-well CMOS devices. Ex. 1008C, 523, 530 ("With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate … of *n* or *p* material."); Ex. 1008B, 387-389.

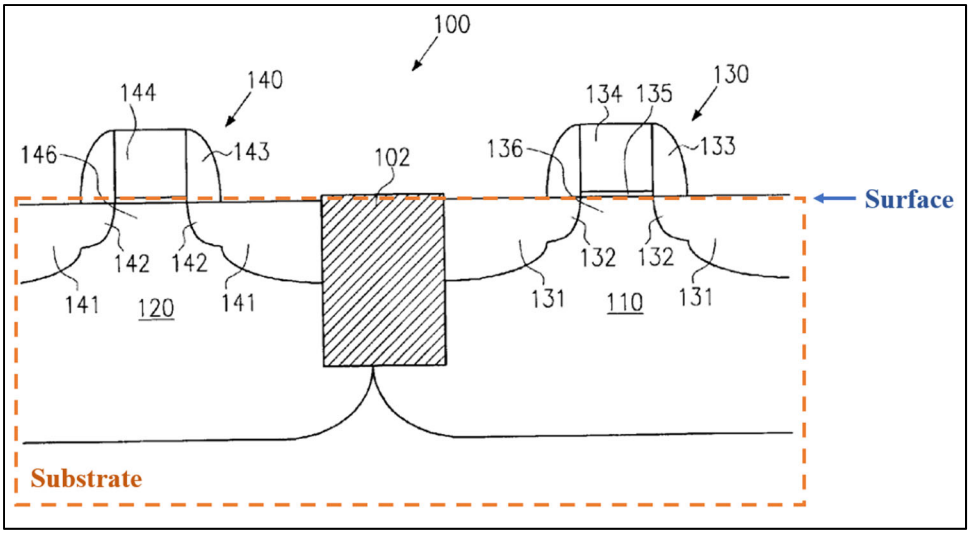


Ex. 1008C, 525, FIG. 8-1(e) ("twin-well CMOS on *n* or *p*-substrate").

143. In my opinion, and consistent with Wieczorek's teaching, a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ("a substrate of a first doping type at a first doping level") as a suitable substrate for Wieczorek's CMOS device in Figure 1b. Doing so would amount to combining known prior art elements (*i.e.*, use of a uniform, lightly doped n- or p-type substrate with Wieczorek's process for forming a conventional CMOS device) according to known methods (*i.e.*, known use of an "appropriate substrate" for the conventional process of forming the CMOS device in Wieczorek [0007]-[0013]) to obtain predictable results (*i.e.*, conventional CMOS device in Wieczorek's Figure 1b). Doing so would have also been obvious to try because it involves nothing more than

choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device like Wieczorek's. There would have been reasonable expectation of success because Wolf shows that a POSITA would have known how to use a uniformly doped n- or p-type substrate to form a twin-well CMOS device similarly as described in Wieczorek.

144. For purposes of claim mapping, and without loss of generality, I have considered Wieczorek-Wolf's substrate is taken as a p-type non-epitaxial substrate, a widely used choice in my experience and which has the advantage of lower cost compared to an epitaxial substrate. Ex. 1008A, 816 ("Typically, in twin-well CMOS the starting material is also ***either*** a lightly *p*-doped wafer (***p-bulk wafer***, Fig. 16-7a), or a heavily *p*-doped wafer on which a thin, lightly *p*-doped epi layer is grown" and noting the cost disadvantage of epitaxial wafers), FIG. 16-7. Consistent with the teachings of Wolf, Wieczorek's substrate in Figure 1b below, has a surface. Ex. 1008B, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).



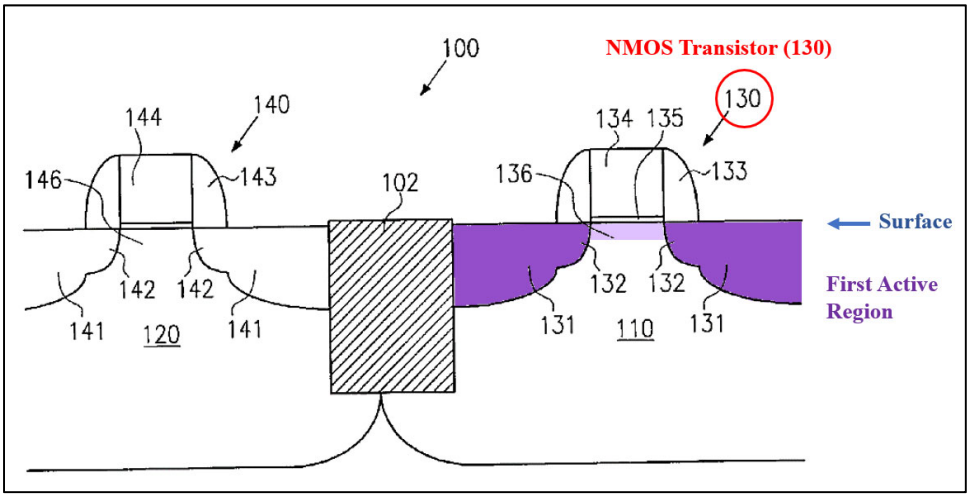
Ex. 1006, FIG. 1b.

145. In my opinion, Wieczorek-Wolf satisfies elements [1.1]/[21.1]/[39.1]/[41.1]/[42.1] under Patent Owner's plain meaning construction and under Petitioner's proposed construction because Wieczorek-Wolf's substrate is the initial material within or on which Wieczorek's "semiconductor device 100" is fabricated. *See* Section VIII; Ex. 1006, [0004], [0012].

c. Elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2]: "a first active region disposed adjacent [the/to a] surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof];"

146. In my opinion, Wieczorek-Wolf renders obvious these elements. Wieczorek discloses "an N-channel transistor 130" that includes "heavily N-doped ***source and drain regions*** 131, including lightly doped extensions 132," and "***channel region*** 136." Ex. 1006, [0012]-[0013]; *id.,* [0004] ("[A] field effect transistor comprises two highly doped semiconductor regions…referred to as ***drain***

and source regions, [] embedded in a lightly and inversely doped semiconductor region, the so-called N-well or P-well [and] spaced apart with a ***channel region*** interposed, wherein a conductive channel forms between the drain and source regions in the channel region" when the transistor is active). The source-drain regions 131-132 (purple) form part of the claimed first active region, which also includes channel region 136 (light purple) between them. Ex. 1006, [0012]; Ex. 1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e). As shown in Figure 1b, nMOS transistor 130 is formed in the surface of the first active region, which is adjacent the first surface of the substrate.

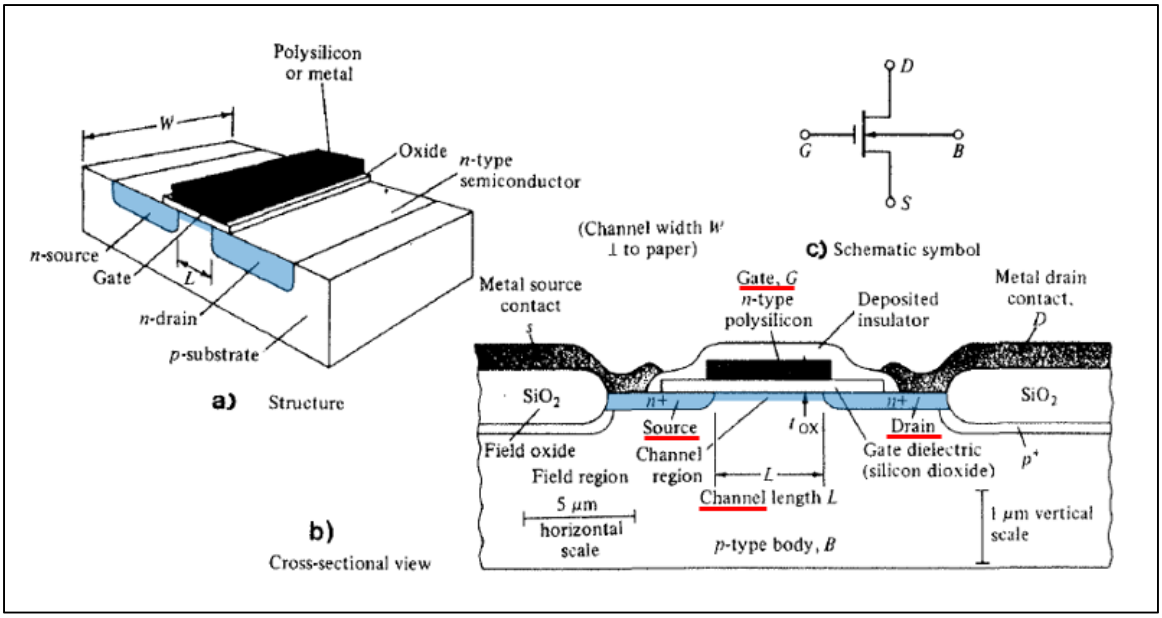


Ex. 1006, FIG. 1b, [0007].

147. In my opinion, because the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-type) opposite in conductivity to the first doping type (P-type) of the substrate. Ex. 1006, [0012].

148. While Figure 1b illustrates a single exemplary nMOS transistor 130 formed in the first active region, in my opinion, a POSITA would have understood that Wieczorek contemplates forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates. Ex. 1006, [0004]; Ex. 1014, 1:52-54, 2:17-21. I was taught this technique in school in the 1980s and had used it myself in numerous designs by 2000. In any event, I understand that according to Patent Owner's representations in the District Court Case, an "active region … within which transistors can be formed" means "an active region … where ***a transistor*** can be formed." Ex. 1020, 31.

149. In my opinion, Wieczorek satisfies elements [1.2]/[21.2]/[39.2]/[41.2]/[42.2] under Patent Owner's construction that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex. 1020, 20; *see also* Section VIII. In my opinion, the active region of a CMOS transistor is "[its] channel and [its] heavily doped source and drain regions" as illustrated in blue in the figure below. Ex. 1008B, 299.



Ex. 1008B, FIG. 5-1; *id*., 298-301, FIGS. 5-2, 6-4.

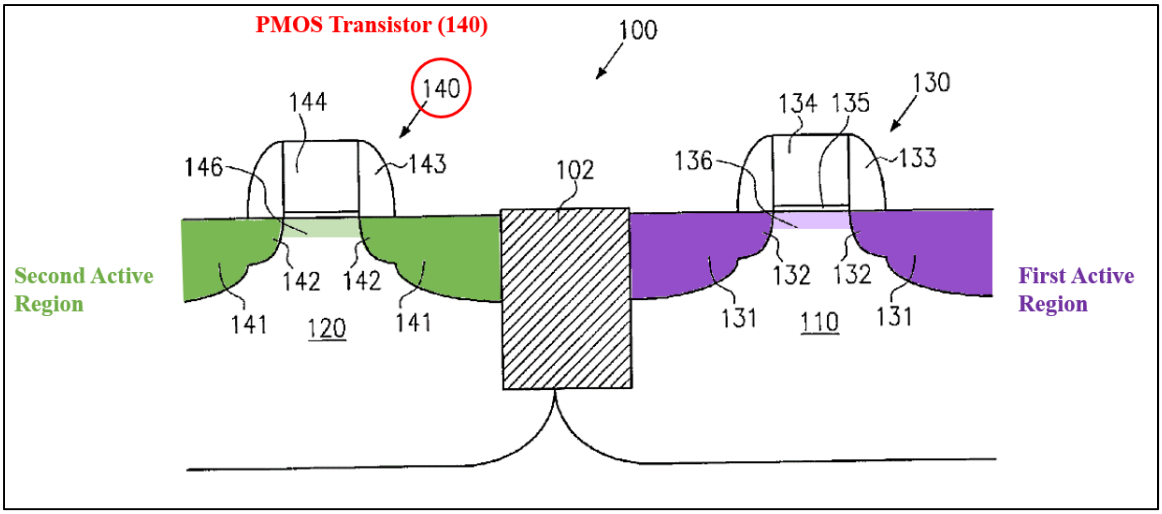
150. It is also my opinion that Wieczorek also satisfies this claim element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Section VIII; Ex. 1008B, 299-301; Ex. 1008D, 197, FIG. 5-13. In my opinion, and based on Patent Owner's representations in the District Court Case, Patent Owner does not dispute this. Ex. 1020, 3-4 ("when a positive voltage is applied to the gate … a ***conductive channel*** [is formed] between the ***source*** and the ***drain***, and ***current*** can begin to flow through the transistor").

d. Elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3]: "a second active region separate from the first active region disposed adjacent to the first active region and within

which transistors can be formed [in the surface thereof];"

151. Wieczorek discloses or, at a minimum, renders obvious these elements. Wieczorek discloses "P-channel transistor 140," including "heavily P-doped source and drain regions 141, including lightly doped extensions 142," and "channel region 146." Ex. 1006, [0004], [0007], [0012]-[0013]. Source and drain regions 141-142 (green) are part of the claimed second active region, which also includes channel region 146 (light green) between them. Ex. 1006, [0012]; Ex. 1008B, 298-301, FIGS. 5-1, 5-2, 6-4; Section X.B.1.c.

152. As shown in Figure 1b, pMOS transistor 140 is formed in the surface of the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex. 1006, [0012]. Adjacent active regions are separated by an isolation region (*e.g.,* shallow trench isolation 102). Ex. 1006, [0007]; Ex. 1008A, 818-20, FIG. 16-11(f); Ex. 1001, Cl. 6; Section X.A.1.d.



Ex. 1006, FIG. 1b, [0007].

153. While the figure shows an exemplary pMOS transistor 140 formed in the second active region, a POSITA would have understood that Wieczorek teaches forming multiple pMOS transistors in the second active region. Ex. 1006, [0004]; Section X.A.1.c. In any event, I understand that according to Patent Owner's representations in the District Court Case, an "active region … within which transistors can be formed" means "an active region … where ***a transistor*** can be formed." Ex. 1020, 31.

154. In my opinion, Wieczorek satisfies elements [1.3]/[21.3]/[39.3]/[41.3]/[42.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Section X.A.1.c. Wieczorek also satisfies this claim element under Petitioner's

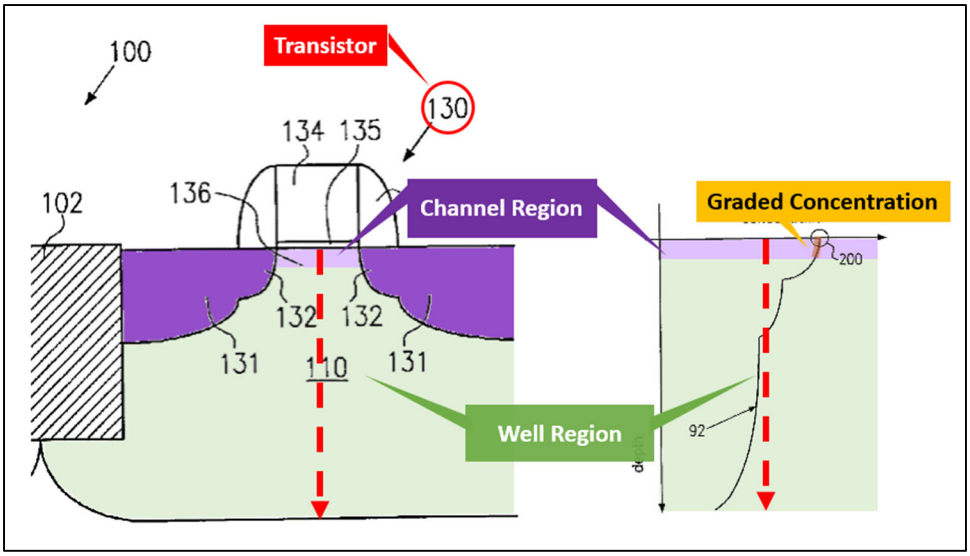
proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device." *Id*.

e. Elements [1.4]/[21.4]/[39.4]/[41.4]/[42.4]: "transistors formed in at least one of the first active region or second active region;"

155. It is my opinion that Wieczorek discloses or, at a minimum, renders obvious these elements. *See* Sections X.A.1.c-d.

f. Elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5]: "at least a portion of at least one of the first and second active regions having at least one graded [dopant/dopant acceptor/donor dopant] concentration to aid carrier movement from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]; and"

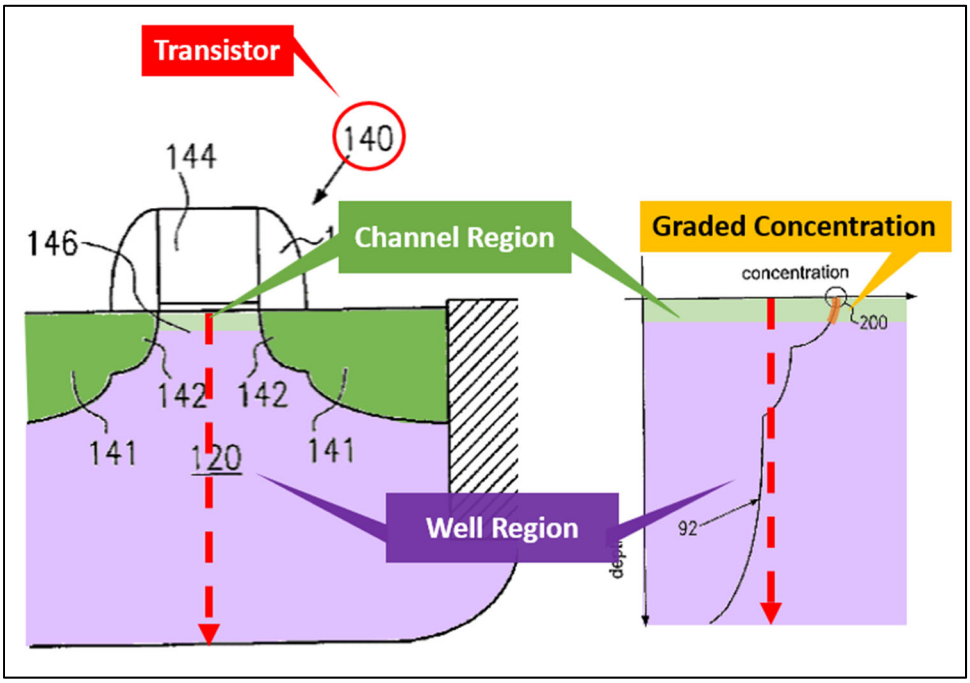
156. It is my opinion that Wieczorek-Wolf renders obvious these elements. As illustrated in Figure 1b (below left), channel region 136 (light purple) of nMOS transistor 130, formed at the top surface of the substrate, is a portion of the first active region. Ex. 1006, [0012]-[0013], [0004] ("The drain and source regions are spaced apart with a ***channel region*** interposed"); Ex. 1008B, 298-301 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), FIG. 5-2.



Ex. 1006, FIGS. 1b, 2b. The doping concentration in the channel region is highlighted in brown in the doping profile of Figure 2b (above right), which is measured for example along the red dotted line in Figure 1b that traverses the channel region. *Id*., [0011] ("FIG. 2b shows … a typical dopant profile with respect to the depth of the respective well structure."), [0013] ("after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in FIG. 2b."), [0009], FIG. 2a.

157. In my opinion, and as Figure 2b shows, the dopant concentration is highest at the surface of the substrate and decreases with depth. Therefore, channel region 136 has a graded dopant concentration. And as shown in the figures below, Wieczorek teaches that channel region 146 (light green) of pMOS transistor 140, which is a portion of the second active region, also has a graded dopant concentration

for the same reasons. Ex. 1006, [0004], [0009], [0011]-[0013], FIGS. 2a-2b; Ex. 1008B, 298-301, FIG. 5-2.

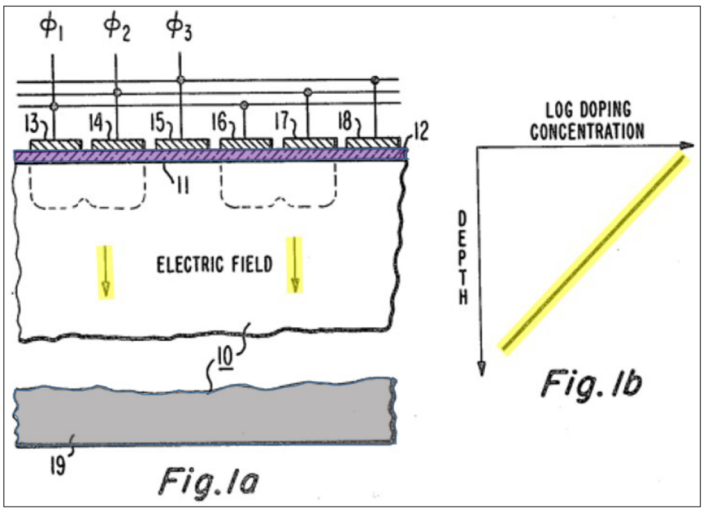


Ex. 1006, FIGS. 1b, 2b. Thus, in my opinion, Wieczorek discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex. 1006, [0009]. [0011], [0013].

158. In my opinion, Wieczorek satisfies elements 41.5 and 42.5. Element [41.5] claims a "graded dopant ***acceptor*** concentration." The graded channel region of Wieczorek's first active region is doped with a p-type impurity such as boron, an acceptor dopant. Ex. 1006, [0008]; Section X.B.8; Ex. 1037, 30. Element [42.5] claims a "graded ***donor*** dopant concentration." The graded channel region of Wieczorek's second active region is doped with an n-type impurity such as phosphorous, a donor dopant. Ex. 1006, [0008]; Section X.B.8; Ex. 1037, 27.

159. Further, Wieczorek's downward-sloping graded dopant concentrations aid carrier movement from the surface and from the first and second active regions towards/to an area of the substrate where there are no active regions to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. As detailed in Section X.A.1.g, during prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to move carriers deep into the substrate.

160. Applicant cited Jastrzebski and Kamins in support. Section X.A.1.g. According to Jastrzebski, a downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers … ***deep into the substrate***[.]". Ex. 1010, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b.

161. In my opinion, Wieczorek satisfies elements [21.5]/[39.5]/[41.5]/[42.5] for the reasons discussed above.

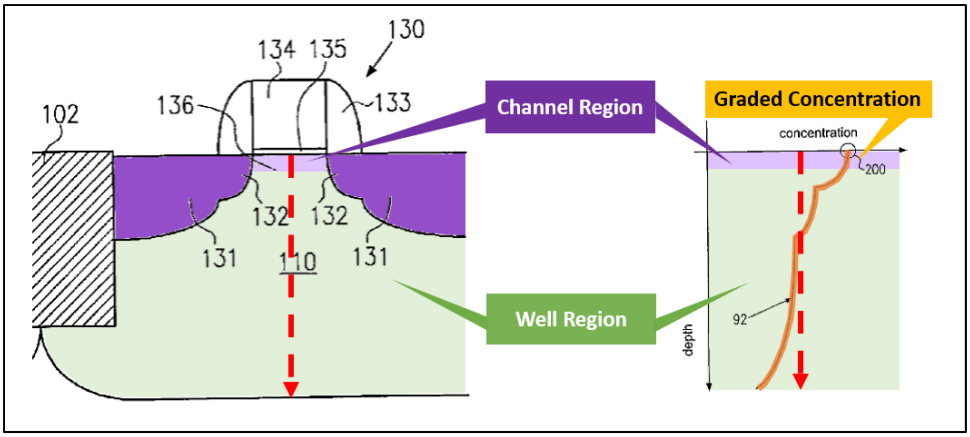
162. In light of the above, it is my opinion that Wieczorek satisfies elements [1.5]/[21.5]/[39.5]/[41.5]/[42.5] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. *See* Section VIII. According to Patent Owner, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)." Ex. 1020, 29. Also, according to Patent Owner, "when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction…." *Id*., 2. Here, Wieczorek's Figure 2b shows that the dopant concentration is downward-sloping with increasing depth towards/to the bottom of the substrate where there are no active regions, and thus, according to Patent Owner, causes carriers to move deeper into the substrate as well.

163. It is also my opinion that Wieczorek also satisfies this claim element under Petitioner's alternative proposed construction that the term means "to sweep the carriers from the [first and second active regions/surface/first or second active region] [towards/to] [an area of the substrate/at least one substrate area] where there [are/is] no active region[s]." *See* Section VIII. Wieczorek's Figure 2b illustrates a downward-sloping graded dopant concentration in the channel regions and Applicant represented to Patent Office during prosecution of the parent '195 Patent

that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers into the substrate (where there are no active regions), as further detailed in Section X.A.1.g. Ex. 1016, 289-290.

g. Elements [1.6]/[21.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions,"

164. In my opinion, Wieczorek-Wolf renders obvious these elements. As shown in Figure 1b (below left), Wieczorek discloses a "P-well structure 110" (light green) adjacent to the first active region (purple/light purple). Ex. 1006, [0012]-[0013]. As discussed above and shown in the dopant concentration profile (brown) of Figure 2b (below right), the dopant concentration in P-well 110—measured along the exemplary red dotted line in Figure 1b—is gradually decreasing with depth. Section X.B.1.f; Ex. 1006, [0009], [0011] ("FIG. 2b shows … a typical dopant profile with respect to the depth of the respective well structure [110 and 120]"), [0013]. Thus, Wieczorek discloses a well region containing at least one graded dopant region (e.g., the region highlighted in light green in both Figures 1b and 2b) having a downward-sloping graded dopant concentration.



Ex. 1006, FIGS. 1b, 2b.

165. Under Applicant's representation to the Patent Office, discussed above in Section X.A.1.g, such a downward-sloping graded dopant concentration was known in the prior art to create a "built-in" electric field that moves carriers deep into the substrate and thus aids carrier movement from the surface towards/to the area of the substrate where there are no active regions. *See* Section X.A.1.g.

166. In my opinion, Wieczorek satisfies elements [1.6]/[21.6] under Patent Owner's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex. 1020, 30; *see also* Section VIII. As shown in Figure 1b above, P-well 110 (light green) is a doped region that surrounds the first active region (purple/light purple). Ex. 1006, FIG. 1b. In my opinion, Wieczorek also satisfies elements [1.6]/[21.6] under Patent Owner's plain meaning construction of the "to aid carrier movement" term. *See* Section VIII.

167. It is also my opinion that Wieczorek also satisfies this claim element under Petitioner's proposed constructions of these terms. *See* Section VIII. The

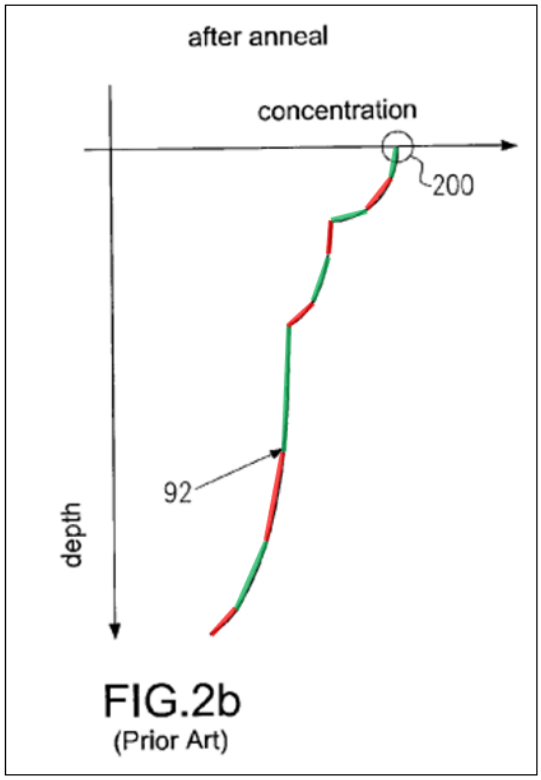
mapping of "well region" to Wieczorek's P-well 110 satisfies Petitioner's construction because P-well 110 and N-well 120 are formed using "ion implantation processes." Ex. 1006, [0008], [0007]-[0012], FIGS. 1a, 2a-2b. With regard to the "aid carrier movement" term, Wieczorek satisfies Petitioner's alternative proposed construction that the term means "to sweep the carriers from the surface towards/to the area of the substrate where there are no active regions." Notably, Wieczorek's Figure 2b illustrates a graded dopant region with a downward-sloping graded dopant concentration and Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers into the substrate (where there are no active regions), as further detailed in Section X.A.1.g. Ex. 1016, 289-290.

h. Element [1.7]: "wherein at least some of the transistors form digital logic of the VLSI semiconductor device."

168. In my opinion, Wieczorek's "complementary MOS transistor pair" is "a frequently used semiconductor device in modern integrated circuits" and was understood by a POSITA to form digital logic gates. Ex. 1006, [0007], [0026]; Ex. 1008A, 810-811 (CMOS, or "[t]he pairing of complementary n- and p-channel transistors ***to form low-power IC logic gates*** … is now the dominant integrated-circuit technology").

i. Element [21.7]: "wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof."

169. In my opinion, as shown in Figure 2b below, the graded dopant concentration is a combination of linear or nearly linear (quasilinear) segments, illustrated in green/red below. As the segments get smaller, they become even more linear/quasilinear. *Id.*



Ex. 1006, FIG. 2b.

2. Claims 2/23: "The VLSI semiconductor device of claim [1/21], wherein the substrate is a p-type substrate."

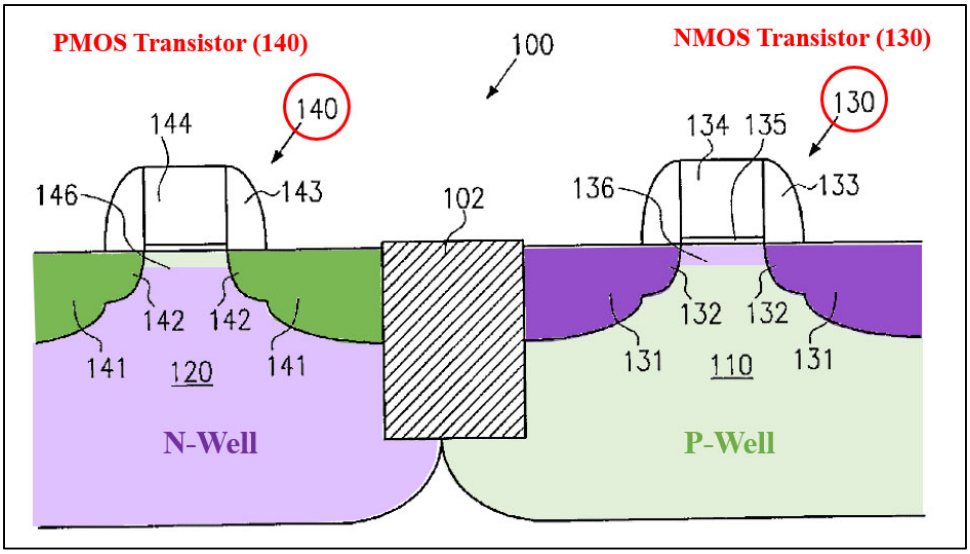
170. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claims 2 and 23. *See* Section X.B.1.b.

3. Claims 4/25: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain [digital logic formed by/at least] one of either p-channel and n-channel devices."

171. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claims 4 and 25. *See* Section X.B.1.c-e, X.B.1.h.

4. Claims 5/26: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant."

172. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claims 5 and 26. Wieczorek's Figure 1b illustrates a conventional twin-well architecture, whereby the first active region contains "N-channel transistor 130" in "P-well" 110, and the second active region contains "P-channel transistor 140" in "N-well" 120. Ex. 1006, [0012]-[0013], [0004]; Sections X.B.1.c-d. In my opinion, this mapping satisfies this claim element under Patent Owner's interpretation that an active region in the claims can contain only "***a transistor***." Ex. 1020, 31. A POSITA would have also understood that Wieczorek teaches forming multiple transistors in an active region to save chip area, as good layout practice dictates. Ex. 1014, 1:52-54, 2:17-21.

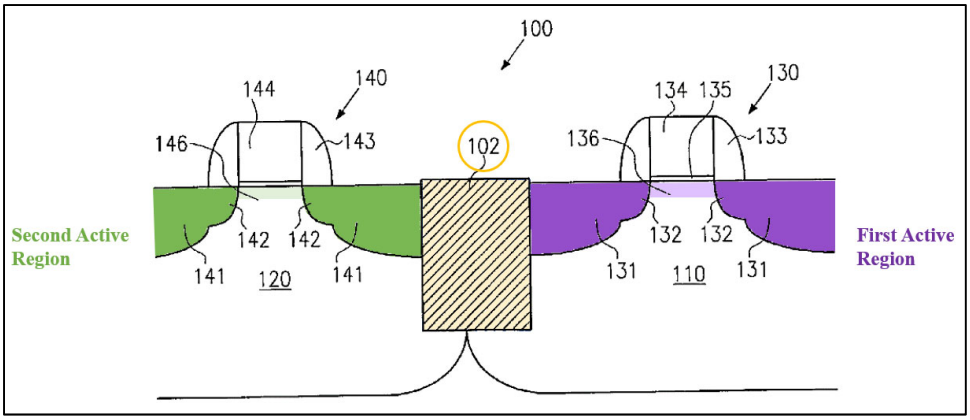


Ex. 1006, FIG. 1b.

173. Further, in my opinion, Wieczorek's wells have a graded concentration of dopants. Ex. 1006, [0009]-[0011] ("FIG. 2b shows … a typical dopant profile with respect to the depth of the respective well structure [110/120]."), [0013], FIGS. 2a-2b; Section X.B.1.g (discussing graded dopants in P-well 110).

5. Claims 6/27: "The VLSI semiconductor device of claim [1/21], wherein the first active region and second active region are each separated by at least one isolation region."

174. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claims 6 and 27. As shown below, the first active region (purple/light purple) and second active region (green/light green) are separated by the "shallow trench isolation 102" (yellow). Ex. 1006, [0007]; Ex. 1008A, 818-820, FIG. 16-11(f).



Ex. 1006, FIG. 1b.

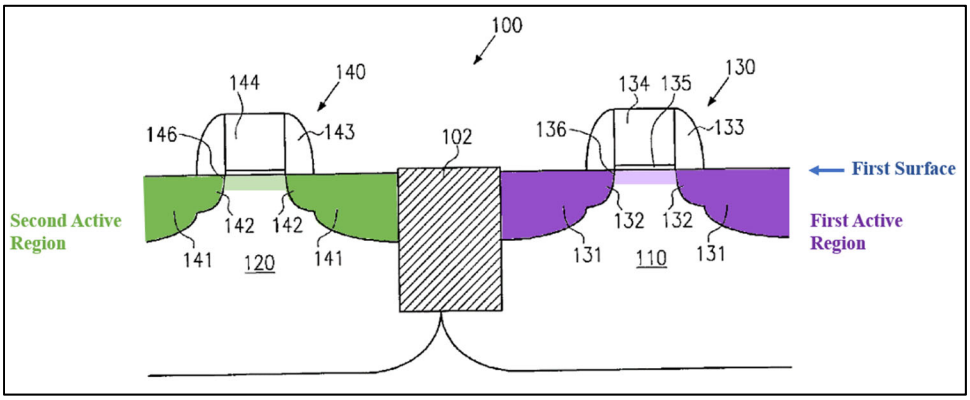
6. Claims 7/32: "The VLSI semiconductor device of claim [1/21], wherein the graded dopant is fabricated with an ion implantation process."

175. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claims 7 and 32. Wieczorek teaches that the graded dopants in "P-well structure 110 and [] N-well structure 120 are defined by sequentially performed ion implantation processes." Ex. 1006, [0008], [0007]-[0011], FIGS. 1a, 2a-2b; Sections X.A.1.f-g.

7. Claim 8: "The VLSI semiconductor device of claim [1/21], wherein the first and second active regions are formed adjacent the first surface of the substrate."

176. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 8. As shown below, the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex. 1006, [0007]-[0010], [0012]-[0013]; Ex. 1008B, 299 ("The top

surface of the [substrate] body consists of active or transistor regions…"), 298-301, FIG. 5-2; Sections X.B.1.c-d.

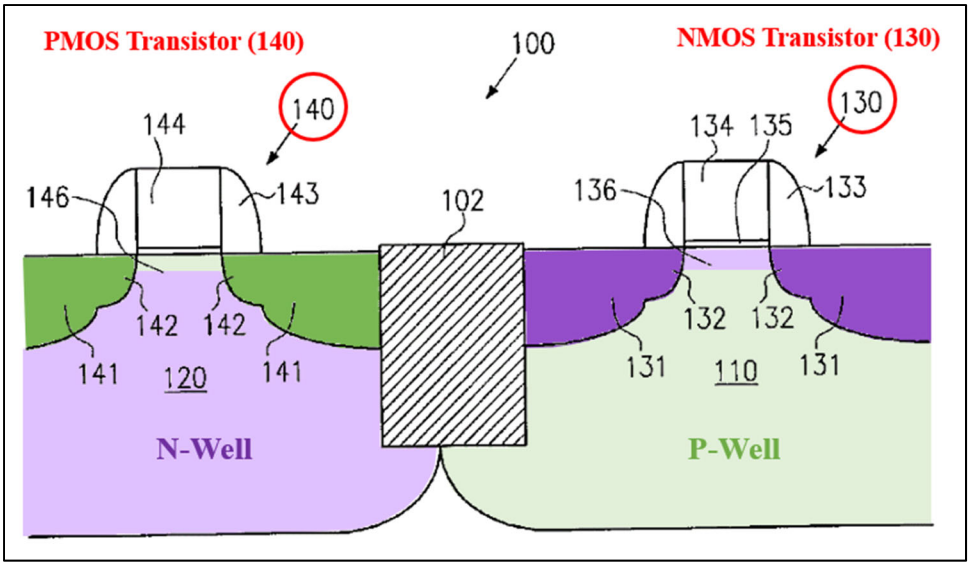


Ex. 1006, FIG. 1b.

8. Claims 9/28: "The VLSI semiconductor device of claim [1/21], wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type."

177. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claims 9 and 28. As discussed above and illustrated in Figure 1b below, channel region 136 (light purple) of the first active region is formed at the top of P-well 110 and is of the same doping type (p-type) as P-well 110. Ex. 1006, [0008] ("for defining the P-well structure 110, typically boron ions are employed"); Ex. 1007, 15:28-29.

178. Likewise, channel region 146 (light green) of the second active region is formed at the top of N-well 120 and is of the same doping type (n-type) as N-well 120. Ex. 1006, [0008] ("[f]or defining the N-well structure 120, typically phosphorous or arsenic ions are used"); Ex. 1007, 9:33-35.

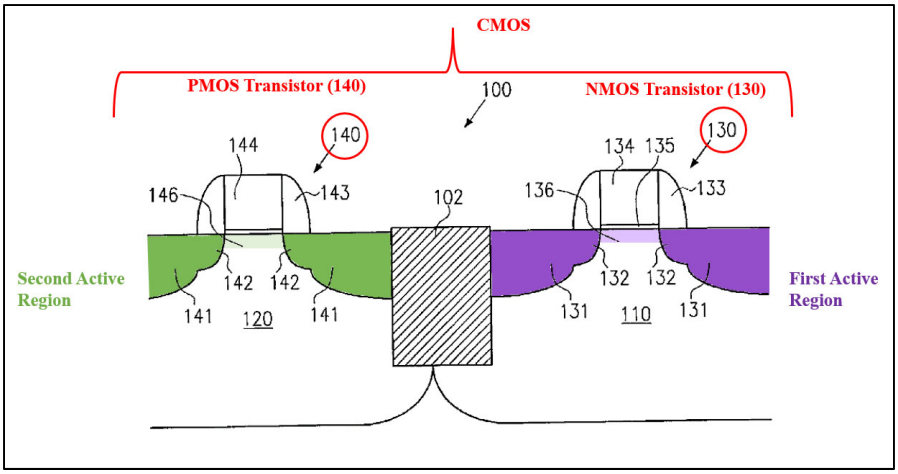


Ex. 1006, FIG. 1b.

179. In my opinion, those channel regions have a graded dopant concentration, as discussed above. Section X.B.1.f.

9. Claim 13: "The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel."

180. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claim 13. Wieczorek-Wolf discloses "a complementary [digital logic] MOS [(CMOS)] transistor pair" comprising "N-channel transistor 130" in the first active region (purple/light purple) and "P-channel transistor 140" in the second active region (green/light green). Ex. 1006, [0007], [0012]-[0013]; Section X.B.1.h.



Ex. 1006, FIG. 1b.

181. Each of the CMOS digital logic transistors include a source, drain, gate, and channel. N-channel transistor 130 includes "heavily N-doped source and drain regions 131" (purple), "gate electrode 134," and "channel region 136" (light purple). Ex. 1006, [0012]-[0013]; P-channel transistor 140 includes "heavily P-doped source and drain regions 141" (green), "gate electrode 144," and "channel region 146" (light green). *Id.*; Sections X.B.1.c-d, X.B.1.f.

10. Claim 14: "The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM)."

182. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 14. In my opinion, Wieczorek's teaching relied on in this declaration is directed to conventional CMOS technology. Section X.B.1.b; Ex. 1006, [0007], [0020]-[0021]. It would have been obvious to fabricate DRAMs, which include transistors and capacitors (Ex. 1008B, 589), using Wieczorek's

conventional CMOS technology to take advantage of "lower power dissipation [] and smaller soft error rates" of CMOS technology and "the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date." Ex. 1008B, 587, 597. Wieczorek also suggests doing so in teaching the frequent application of its technology to "modern integrated circuits." Ex. 1006, [0004], [0026]. Indeed, DRAMs were known to be designed using CMOS technology, "and such DRAMs included capacitors." Ex. 1008B, 596-597.

183. Additionally, in my opinion, using Wieczorek's technology to form a DRAM would have merely amounted to combining known, conventional prior art elements (*i.e.*, Wieczorek's CMOS process and known CMOS DRAM designs) according to known methods (*i.e.*, Wieczorek's CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology contemplated by Wolf for DRAM) with another (*i.e.*, Wieczorek's conventional CMOS technology). In my opinion, there would have been a reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was known and would have been used for its intended purpose in manufacturing a known DRAM designed for implementation using CMOS technology.

11. Claim 15: "The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate."

184. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 15. *See* Section X.B.1.b.

12. Claims 16/34: "The VLSI semiconductor device of claim [1/21], wherein the device is a flash memory."

185. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claims 16 and 34. In my opinion, Wieczorek's teaching relied on in this declaration is directed to conventional CMOS technology. Section X.B.1.b; Ex. 1006, [0007], [0020]-[0021]. Further, in my opinion, it would have been obvious to fabricate flash memory using Wieczorek's conventional CMOS technology to achieve the benefits of "lower power-dissipation" of CMOS technology and "high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs." Ex. 1008B, 634; Ex. 1008A, 808-810. Wieczorek also suggests doing so in teaching the frequent application of its technology to "modern integrated circuits." Ex. 1006, [0004], [0026]. Indeed, flash memory devices commonly used CMOS technology. Ex. 1008B, 633-635 (describing known "CMOS flash-EEPROM" devices); Ex. 1007, 22:16-17 (flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors); Section X.A.12.

186. Additionally, in my opinion, using Wieczorek's technology to form flash memory would have merely amounted to combining known, conventional prior art elements (*i.e.*, Wieczorek's CMOS process and known CMOS flash memory designs) according to known methods (*i.e.*, Wieczorek's CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology for prior art flash memory) with another (*i.e.*, Wieczorek's conventional CMOS technology). There would have been, in my opinion, a reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was known and would have been used for its intended purpose in manufacturing a known flash memory designed for implementation using CMOS technology.

13. Claim 17: "The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors."

187. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 17. Section X.B.1.h, X.B.10.

14. Claims 18/36: "The VLSI semiconductor device of claim [1/21], wherein the device is central processing unit."

188. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claims 18 and 36. Wieczorek's teaching relied on in this petition is directed to conventional twin-well CMOS technology. Section X.B.1.b. In my opinion, a POSITA would have found it obvious to fabricate known microprocessors (CPUs), using Wieczorek's conventional CMOS technology to achieve the benefits

of "lower power-dissipation" of CMOS technology in such devices. Ex. 1008B, 368-370; Ex. 1032, 1334. Wieczorek suggests doing so in teaching the frequent application of its technology to "modern integrated circuits." Ex. 1006, [0004], [0026]. Indeed, twin-well CMOS technology was, by the early 2000s, "the dominant CMOS technology in IC production." Ex. 1008D, 181.

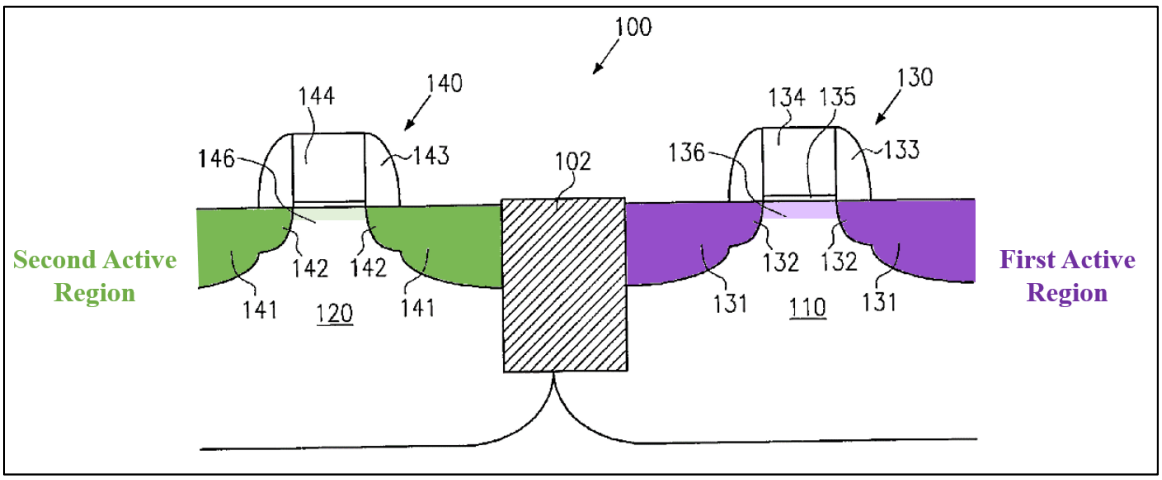
189. Rabaey confirms this. Ex. 1025, 180 ("The [CMOS] inverter is truly the nucleus of all digital [logic] designs" and, together with other "[logic] gates such as NAND, NOR, or XOR … form the building blocks for modules such as multipliers and processors."), 37 ("Modern [CMOS] processes are increasingly using a dual-well [(twin-well)] approach that uses both n- and p-wells …"), 383-84, FIG. 8-6 (showing Intel Pentium processor "designed in a 0.18μm CMOS technology."). Sze also confirms this, describing a system-on-a-chip that includes CMOS "***logic IC (e.g., CPU)***" fabricated using twin-well CMOS technology. Ex. 1022, 525-26, FIGS. 37-38.

190. Additionally, in my opinion, using Wieczorek's technology to form CPUs would have merely amounted to combining known, conventional prior art elements (*i.e.*, conventional twin-well CMOS process described in Wieczorek and known CPU designs) according to known methods (*i.e.*, Wieczorek's conventional twin-well CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology for prior art CPUs) with another (*i.e.*, Wieczorek's

conventional CMOS technology). There would have been a reasonable expectation of success with predictable results because Wieczorek's conventional twin-well CMOS process was known and would have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology.

15. Claims 20/38: "The VLSI semiconductor device of claim [1/21], wherein each of the first and second active regions are in the lateral or vertical direction."

191. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claims 20 and 38. In my opinion, and as shown in Figure 1b below, the first (purple/light purple) and second (green/light green) active regions are in the lateral direction.

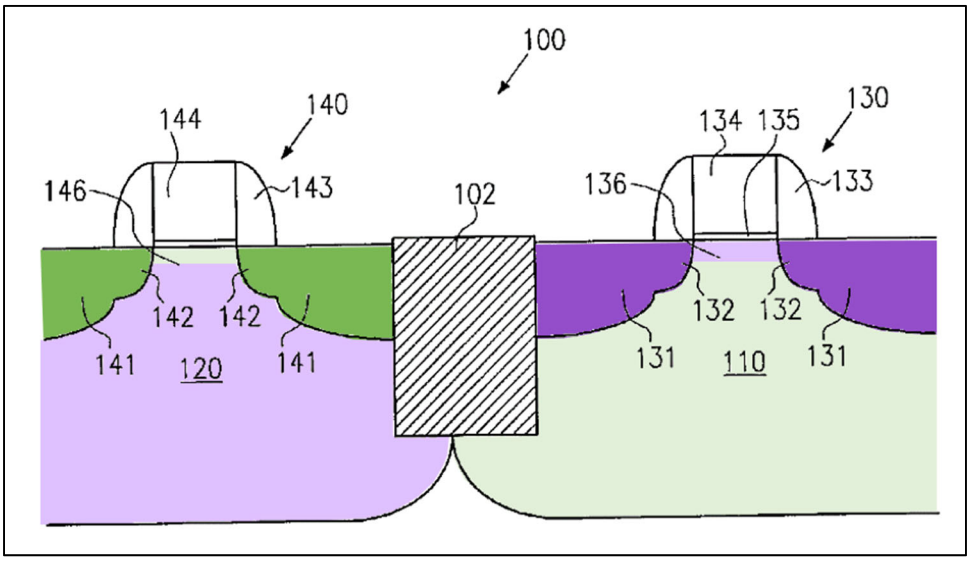


Ex. 1006, FIG. 1b.

16. Claim 22: "The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate."

192. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 22. As I explained in Section X.B.1.b, n-type and p-type

substrates are both suitable for Wieczorek's CMOS device, and a p-type substrate is chosen for claim mapping of claims 1 and 21. Section X.B.1.b. With an n-type substrate, claim element [21.2] requiring "a first active region … with a second doping type opposite in conductivity to the first doping type" of the substrate is met by mapping the first active region to the source/drain/channel regions 141/142/146 (green/light green) of pMOS transistor 140, and claim element [21.3] is met by mapping the second active region to the source/drain/channel regions 131/132/136 (purple/light purple) of nMOS transistor 130. *Id.*



Ex. 1006, FIG. 1b.

17. Claim 33: "The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device."

193. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 33. Wieczorek teaches "a complimentary MOS [(CMOS)]

transistor pair" formed in and including a substrate. Ex. 1006, [0007], [0012]-[0013]; Section X.B.1.b.

18. Claim 35: "The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions."

194. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 35. Sections X.B.1.e, X.B.1.h, X.B.10/12/14. MOS transistors are commonly used as capacitors to form dynamic circuits such as voltage bootstrapping circuits, charge pump circuits, delay/timing circuits, and to form decoupling capacitors ("decaps"). Hodges' figure below shows an NMOS transistor configured as a capacitor by connecting its gate to V_{DD} and its source/drain to V_{SS}. Ex. 1038, 493-494.

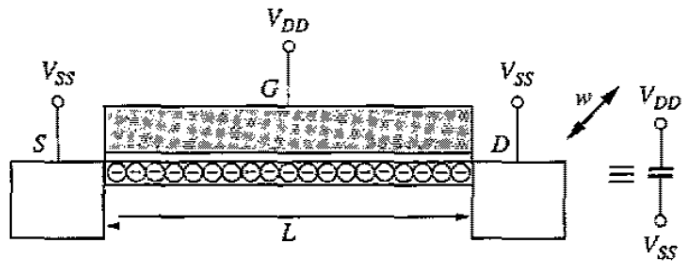


Figure 11.11
On-chip decap using MOS capacitance.

Id., FIG. 11.11.

195. In my opinion, a POSITA would have understood (and found it obvious) that some of Wieczorek's transistors formed in some of the first or second active regions are configured as capacitors. For example, the voltage bootstrapping

circuit below—a "very useful" and commonly used circuit—includes a transistor configured as a capacitor (C_{boot}) connected to other transistors (M1-M3). Ex. 1041, 370-373.

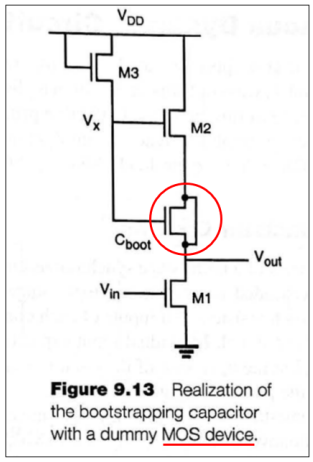


Figure 9.13 Realization of the bootstrapping capacitor with a dummy MOS device.

Id., FIG. 9.13.

196. In my opinion, a POSITA would also find it obvious to configure transistors as decaps "scattered throughout the design" to filter out power supply noise and reduce "*IR* drop." Ex. 1038, 493 ("On-chip decoupling capacitors (decaps) are ***commonly used*** to keep the power supply within the noise budget, especially during peak demand periods in high-frequency switching operations."); *id.*, 498 ("The ***most effective approach*** [to reduce *IR* drop] is to use *decoupling capacitors* between power and ground … These decoupling caps are usually ***scattered*** throughout the design in any available space, using ***transistors*** with their gates tied to V_{DD} and their source-drain regions tied to Gnd.") (italics in original); *id.,* 499 ("you can never have enough" decaps). In my opinion there is reasonable

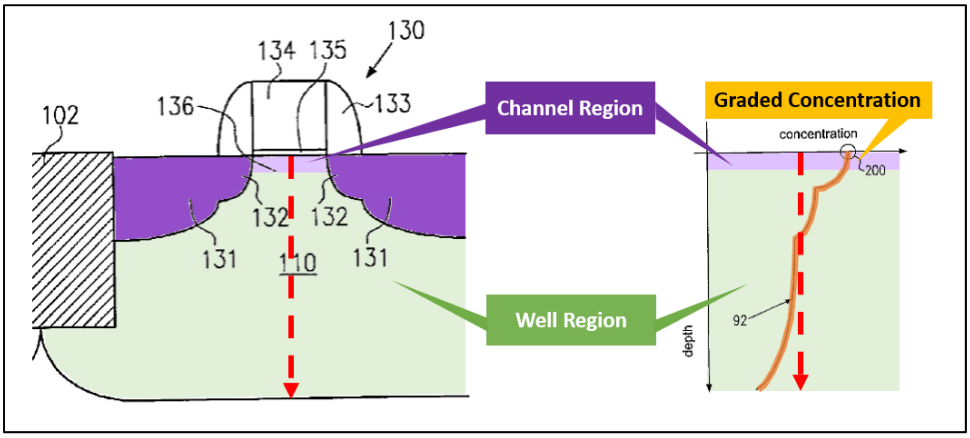
expectation of success with predictable results because the use of transistors as capacitors was a well-known, intended use of MOS transistors. *Id*.

197. Moreover, there is a MOS capacitor inherent to every MOS gate or gate oxide structure built over an active region. *See* Ex. 1040, 116 ("At the heart of the MOSFET is the MOS capacitor structure depicted in Fig. 4.1."). This capacitor is formed by the gate, gate oxide, and active-region channel structure. *Id.* at 116-118 The gate is one plate and the active-region channel is the second plate of the capacitor. *Id.* As seen in Jaeger, the capacitor structure is taught as part of basic electronics pedagogy and is foundational to understanding MOS transistors. *See id.* In my opinion, many common uses of the MOS capacitor would have been obvious to a POSITA, including charge and information storage, bypass capacitance, filter elements, and delay elements. It is impossible to build MOS transistors without MOS capacitors and, in my opinion, it is hard to find a VLSI scale circuit that does not also include MOS capacitors as explicit circuit elements. In my opinion, this was well known to a POSITA at the time of the '222 patent and is fundamental to CMOS design.

19. Claim 40: "The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier

> **movement from any region in the well to the substrate area where there is no well."**

198. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 40. Section X.B.1.g. As illustrated below, Wieczorek's graded dopant concentration is downward-sloping throughout each well (green) and moves carriers from any region of the well to deeper areas of Wieczorek-Wolf's substrate where there is no well. Ex. 1008C, 525, FIG. 8-1(e); Section X.B.1.b.



Ex. 1006, FIGS. 1b/2b.

C. GROUNDS III/IV

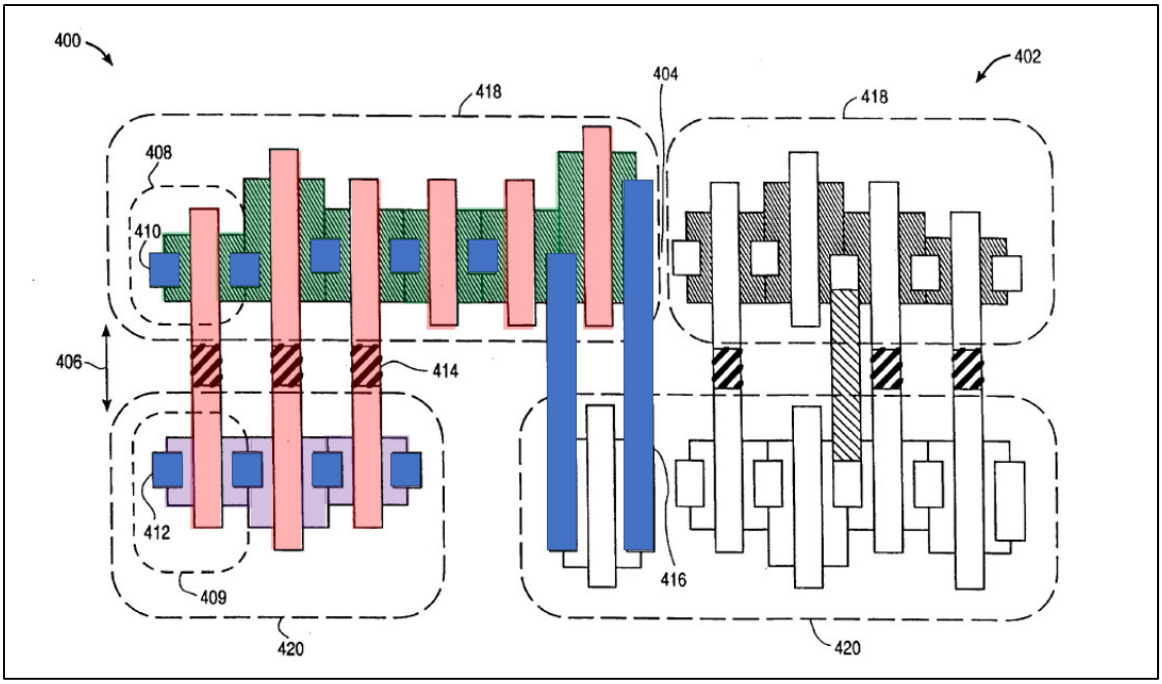
199. Several claim elements of the Challenged Claims recite "transistors" or "devices." *See* Elements [1.2]-[1.4]/[1.7]/[21.2]-[21.4]/[39.2]-[39.4]/[41.2]-[41.4], [42.2]-[42.4]; Cls. 4-5, 13, 25-26. As I discussed above under Grounds I and II, I understand that the Patent Owner interprets these claim elements as requiring one or more transistors, and not a plurality of transistors. *See* Sections X.A.1.c-d, X.B.1.c-d.

200. The present Grounds III-IV mirror Grounds I-II, respectively, except that Gupta is explicitly combined with Kawagoe of Ground I and Wieczorek-Wolf of Ground II to render obvious those claim elements under an interpretation of "transistors" or "devices" to require a plurality of such devices.

201. Gupta is directed to "automatically producing layouts for CMOS circuits," recognizing that "semiconductor chips [have] become ever larger, incorporating ever more devices." Ex. 1014, 1:7-10, 1:28-31. Wolf confirms that, at the time, various chips (e.g., DRAM, microprocessors, and flash memory) were fabricated with tens of millions to more than a billion devices. Ex. 1008A, xxxiii, FIG. 1; Ex. 1008B, 634. In my opinion, Gupta reflects the knowledge of a POSITA by explaining that a "primary goal" of semiconductor chip development has therefore been to minimize the chip area required to form any circuit so that more transistors can be packed in the same chip, regardless of the technology and chip fabrication process. Ex. 1014, 1:28-35 ("As semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices. Conservation of semiconductor area is a ***primary goal*** in semiconductor chip development…."). Gupta further reflects the knowledge of a POSITA by explaining that good circuit layout practice dictates forming as many transistors in the same active region through diffusion abutment as possible, to minimize area-wasting diffusion gaps. *Id.*,

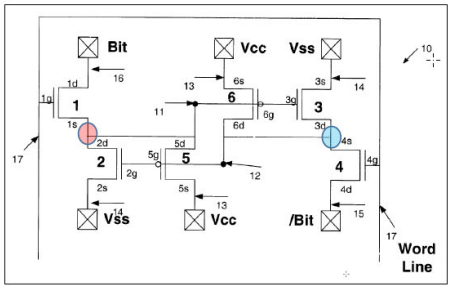
1:52-54 ("One technique conserves area by placing transistors so as to ***share diffusion area***."), 2:17-21 ("Transistors which are abutted in a layout form transistor chains. It is desirable to produce a layout with a ***maximum number of transistors chained*** so as to minimize diffusion gaps."); Ex. 1023, 5 ("An important layout task is to place and orient the transistors on the chip to ***minimize the layout area*** of the circuit" by avoiding "area-wasting diffusion gap[s]"). Gupta describes several techniques to achieve optimal layout, such as transistor folding and chaining. Ex. 1014, 1:49-2:24, 3:64-4:1, FIGS. 2-3.

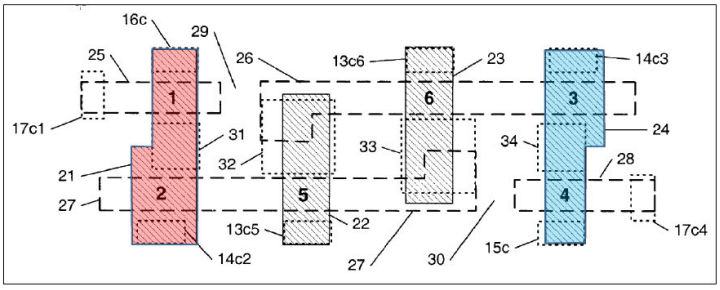
202. Gupta's Figure 4 (below)—where transistor gates and metal contacts that overlay the active regions are colored in red and blue respectively—illustrates ***six*** chained PMOS transistors formed in a p-channel active region (green) and ***three*** chained NMOS transistors formed in an n-channel active region (purple). Ex. 1014, 4:12-43.



Ex. 1014, FIG. 4.

203. In my opinion, Jin further confirms that transistors arranged as in Gupta are formed in a common active region. Below left is the circuit schematic of a conventional 6T SRAM cell, and the cell layout (below right) shows two transistors (1 and 2) formed in active region 21 (red), and two other transistors (3 and 4) formed in active region 24 (blue). Ex. 1015, 6:17-29; Ex. 1025, 48 ("*Diffusion regions* (n^+ and p^+), which define the areas where transistors can be formed[,] are often called the *active areas*.") (italics in original).





Ex. 1015, FIGS. 1 and 2.

204. In my opinion, a POSITA would have been motivated to fabricate a CMOS chip according to the combined teachings of Kawagoe and Gupta (and likewise, of Wieczorek-Wolf and Gupta) to achieve high packing density (as taught by Gupta) at submicron dimensions (for which a twin-well CMOS process of the type taught in Kawagoe and Wieczorek-Wolf was known to be the technology of choice (Ex. 1008B, 373, 388)).

205. In my opinion, the combinations gain the additional benefit of improved immunity to soft errors through appropriate well doping. Ex. 1007, 15:62-16:11. Combining the teachings of Gupta with those of Kawagoe or Wieczorek-Wolf merely amounts to (1) use of a known technique (*i.e.*, Kawagoe's or Wieczorek's CMOS fabrication process) to improve similar devices (*i.e.*, CMOS chips designed with Gupta's layout) in the same way (*i.e.*, to achieve submicron dimensions and improve immunity to soft errors); (2) use of a known technique (*i.e.*, Gupta's optimal layout generation) to improve similar devices (*i.e.*, submicron CMOS chips fabricated according to Kawagoe or Wieczorek-Wolf's CMOS fabrication process)

in the same way (*i.e.*, to minimize chip area and increase packing density); and (3) combining prior art elements (*i.e.*, Kawagoe or Wieczorek's CMOS fabrication process and Gupta's CMOS layout generation) according to known methods (*i.e.*, as taught by Kawagoe or Wieczorek and Gupta). There is reasonable expectation of success with predictable results because Kawagoe's and Wieczorek's CMOS fabrication process would be used for their intended purpose of fabricating CMOS circuits according to known CMOS layouts generated by Gupta, which would also be used for its intended purpose. Further, it is my opinion that Gupta's optimal circuit layout is process-agnostic, and applies to the layout of ***any*** CMOS semiconductor chip, including the layout of CMOS chips fabricated according to the teachings of Kawagoe and/or Wieczorek-Wolf.

206. In my opinion, a POSITA would have understood that, in such a combination, the active regions in Gupta's figures are formed in wells (*i.e.,* n-channel active regions are formed in p-wells, and p-channel active regions are formed in n-wells), whereby the wells have downward-sloping graded dopant concentrations as shown in Kawagoe's Figure 17 and Wieczorek's Figure 2b. I am also of the opinion that the n-channel active region (purple) in Gupta's Figure 4 is an example of the claimed first active region, and that the p-channel active region (green) is an example of the claimed second active region. The two active regions are adjacent and separated by an isolation region (field oxide), as required under

elements [1.3], [21.3], [39.3], [41.3], and [42.3] and claims 6 and 27. Ex. 1014, 1:16-19, 4:39; Ex. 1008A, 818-820; Sections X.A.1.d, X.A.6, X.B.1.d, X.B.5.

207. Conversely, in my opinion, a POSITA would have understood that each of the active regions of Kawagoe's and Wieczorek's CMOS devices typically contains many transistors, as taught by Gupta and illustrated in Gupta's Figure 4. This is the case whether the device is a DRAM, flash memory, logic device or CPU (as claimed in claims 14, 16-18, 34-36). Each such device is a "very large scale integrated circuit" for which "it becomes increasingly important to minimize semiconductor area used[,]" and this requires forming as many transistors as possible in any active region. Ex. 1014, 1:13-14, 1:28-34, 2:17-21.

208. In light of the above, in my opinion, Kawagoe in view of Gupta renders claims 1-9, 13-14, 16-18, 20-21, 23-28, 32-36, and 38-42 obvious (Ground III). Likewise, in my opinion, Wieczorek-Wolf in view of Gupta renders claims 1-2, 4-9, 13-18, 20-23, 25-28, 32-36, and 38-42 obvious (Ground IV).

XI. CONCLUSION

209. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '222 Patent are rendered obvious by the prior art.

210. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

211. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: December 28, 2022

Respectfully submitted,

Travis Blalock, Ph.D.

APPENDIX A

Element	Claim Language
[1.pre]	A VLSI semiconductor device, comprising:
[1.1]	a substrate of a first doping type at a first doping level having a surface;
[1.2]	a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[1.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[1.4]	transistors formed in at least one of the first active region or second active region;
[1.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
[1.6]	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,
[1.7]	wherein at least some of the transistors form digital logic of the VLSI semiconductor device.
2	The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.
3	The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
4	The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.
5	The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.
6	The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

Element	Claim Language
7	The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.
8	The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.
9	The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
13	The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.
14	The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).
15	The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
16	The VLSI semiconductor device of claim 1, wherein the device is a flash memory.
17	The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.
18	The VLSI semiconductor device of claim 1, wherein the device is central processing unit.
20	The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.
[21.pre]	A VLSI semiconductor device, comprising:
[21.1]	a substrate of a first doping type at a first doping level having a surface;
[21.2]	a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[21.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[21.4]	transistors formed in at least one of the first active region or second active region;

Element	Claim Language
[21.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and
[21.6]	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and
[21.7]	wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.
22	The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate.
23	The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.
24	The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
25	The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.
26	The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.
27	The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.
28	The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
32	The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.
33	The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.
34	The VLSI semiconductor device of claim 21, wherein the device is a flash memory.

Element	Claim Language
35	The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.
36	The VLSI semiconductor device of claim 21, wherein the device is central processing unit.
38	The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.
[39.pre]	A semiconductor device, comprising:
[39.1]	a substrate of a first doping type at a first doping level;
[39.2]	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[39.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[39.4]	transistors formed in at least one of the first active region or second active region;
[39.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active region to at least one substrate area where there is no active region.
40	The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.
[41.pre]	A semiconductor device, comprising:
[41.1]	a substrate of a first doping type at a first doping level;
[41.2]	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[41.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[41.4]	transistors formed in at least one of the first active region or second active region; and

Element	Claim Language
[41.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.
[42.pre]	A semiconductor device, comprising:
[42.1]	a substrate of a first doping type at a first doping level;
[42.2]	a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
[42.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
[42.4]	transistors formed in at least one of the first active region or second active region; and
[42.5]	at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.