

CHAPTER II

FUNCTIONAL CELL LAYOUT METHODS

In this chapter, we discuss one-dimensional functional cell design in depth and present a detailed survey and evaluation of all important prior methods for generating layouts in this style.

2.1 FUNCTIONAL CELL DESIGN

First we discuss the general principles of functional cell design. We begin by introducing the original set of assumptions defining this layout style, followed by an extended illustration of these fundamental ideas. Uehara and vanCleemput originally proposed the style of interest, which is illustrated by Fig. 1.3(b) [Uv78]. To simplify the resulting design problem, they made various assumptions, which we list explicitly in Fig. 2.1.

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1. Static CMOS technology is used.
 2. The pMOS and nMOS subcircuits are series-parallel connections of transistors.
 3. The pMOS and nMOS subcircuits are geometric duals of each other.
 4. The circuit height h is limited to four for performance reasons.
 5. Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.
 6. Complementary pMOS and nMOS transistor pairs are vertically aligned. This allows their gate terminals to be interconnected by vertical polysilicon columns without use of crossovers.
 7. Transistor drain and source terminals are connected by diffusion if the terminals are physically adjacent in the layout, or by metal if they are not adjacent. Only one metal layer is used.
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Fig. 2.1. The assumptions defining the Uehara-vanCleemput layout style.

Figure 2.2 illustrates the first four assumptions of Fig. 2.1. A static CMOS gate is a transistor circuit composed of two 2-terminal subcircuits of MOS

transistors, a pullup subcircuit of pMOS transistors, the designated terminals of which are V_{DD} and the circuit's output z , and a pulldown subcircuit of nMOS transistors, whose terminals are z and GND. These subcircuits are functional duals, meaning that when there is a conducting path between the terminals of one subcircuit, there is not such a path between the terminals of the other subcircuit. The circuit of Fig. 2.2 is often referred to as a static CMOS "complex" gate. A pMOS transistor is shown in the pullup subcircuit. The circuit between the source and drain terminals of a pMOS transistor is closed, creating a path for current to flow, if the voltage on the gate terminal is low (at the logical 0 voltage, assuming the positive convention); otherwise the circuit is open, preventing the flow of current. Conversely, the circuit between the source and drain terminals of an nMOS transistor in the pulldown circuit is closed, if the voltage on the gate terminal is high (at the logical 1 voltage); otherwise the circuit is open. For example, if the signals c , d , a and g are low, then the path through the pMOS transistors with these signals on their gate terminals connects V_{DD} to the output terminal, and the output signal is logical 1. Note that under these conditions, no path from the output z to GND can be closed because the nMOS dual transistors labeled c , d , a and g open all possible paths to GND. If signals a and b are high, then the output is connected to GND through transistors a and b , and all paths from V_{DD} to the output are open resulting in a logical 0 output. The source terminal of an nMOS transistor in Fig. 2.2 is the

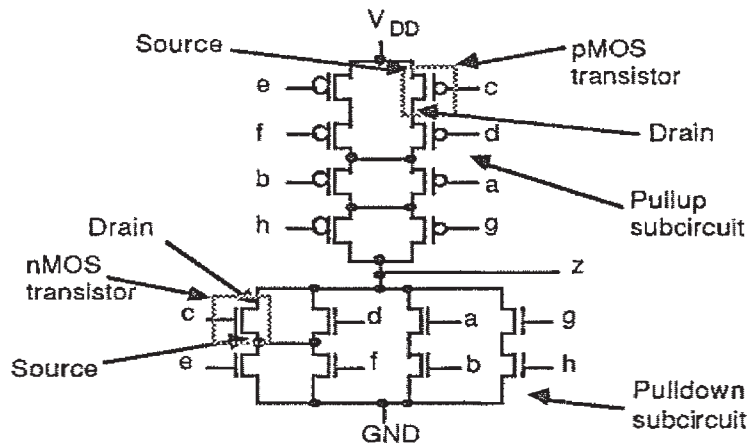


Fig. 2.2. A static CMOS complex gate.

one that is closer to GND, whereas the source terminal of a pMOS transistor is the one closer to the V_{DD} terminal; these two cases are illustrated in Fig. 2.2 for the transistors labeled c .

The second assumption of Fig. 2.1 is that the pullup and pulldown subcircuits are series-parallel. The circuit of Fig. 2.2 is of this type, where every transistor in either the pullup or pulldown subcircuit is either in series or in parallel with some other transistor. Transistors *a* and *b*, for example, are in series in the pulldown subcircuit and in parallel in the pullup subcircuit. The third assumption is that the pullup and pulldown subcircuits of the circuit are geometric duals [Ha69]. Dual subcircuits reverse the roles of the series and parallel operations; every transistor in series (parallel) with another transistor in one subcircuit is in parallel (series) with its dual transistor in the other subcircuit. Furthermore, dual transistor pairs in the subcircuits have the same signal label on their gate terminals. The pullup subcircuit of Fig. 2.2 the geometric dual of the pulldown subcircuit. The height restriction of the fourth assumption is illustrated by the longest path of transistors *c*, *d*, *a* and *g* in the pullup subcircuit. Since no path in either subcircuit is longer than this, the circuit height is four.

The remaining three assumptions relate to the layout of transistors in the functional cell. First, we briefly discuss the role of the three layers: metal, polysilicon and diffusion. Diffusion and polysilicon are primarily used for creating transistors, which occur where these layers cross, as shown in Fig. 1.9. They can also form interconnections, but they have higher resistance and capacitance than the metal layer, whose primary role is interconnection. The metal layer is on a different plane than either the diffusion or polysilicon layer, and requires a contact to make an electrical connection with these other layers. Two such contacts are shown in Fig. 2.3(b) along the bottom row of metal, interconnecting the diffusion regions of the pulldown regions to GND. Although we only use one metal layer, some IC manufacturing processes offer two or more layers.

The fifth assumption of two rows of transistors is illustrated in Fig. 2.3(b), where the pMOS transistors are placed in the upper row and the nMOS transistors in the lower row. The sixth assumption about interconnecting the gate terminals of a dual transistor pair with a vertical polysilicon column is illustrated in Fig. 2.3(a), where the pMOS and nMOS dual transistors labeled *c* in Fig. 2.2 are vertically aligned in the leftmost column also labeled *c*, and their gate terminals are connected.

Assumption 7 of Fig. 2.1 defines the methods of interconnecting those source and drain terminals in the layout that are connected in the transistor circuit. First, we outline how drain-source terminals of transistors are interconnected or electrically isolated in the functional cell, and how this affects cell size. Terminals connected in the transistor circuit are connected in the cell either by metal wires or diffusion abutment; those not connected in the circuit are isolated either by not placing such terminals adjacent to each other or, if placed adjacent, by inserting a diffusion gap between them. The position and orientation of transistors in the cell determines