

implemented in surface channel MOS devices to accelerate majority carriers towards the drain. ~~To decrease programming time~~ [[In]] in nonvolatile memory devices, ~~to decrease programming time,~~ carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction ~~field-effect~~ Field-Effect transistors where the “channel ~~pinchoff~~ pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

Please replace paragraph [0022] with the following amended paragraph:

[0022] One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface [[,]] to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, ~~single-well~~ single-well, ~~as well and~~ triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments [[,]] individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 1-16 (all Figures). The sheets replace all of the original drawing sheets, including Figs. 1-16. The amendments made to the drawings are limited to improving readability and to correcting editorial problems, such as typos. No substantive changes have been made and no new matter has been added.

Attachment: Replacement Sheets for Figures 1-16 (one figure per sheet)

Amendments to the Claims:

The listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-8 (Cancelled)

9. (Newly Added) A semiconductor device comprising:

a surface layer;

a substrate;

an active region including at least one emitter, at least one base and at least one collector disposed in the above said device;

at least one drift layer positioned between said emitter and said collector, said drift layer having at least one graded concentration of dopants, said drift layer further having a first static unidirectional electric field to aid movement of carriers from said emitter to said collector; and

at least one isolation region disposed in the semiconductor device, said isolation region having a graded concentration of dopants and a second static unidirectional electric field to aid isolation between active regions.

10. (Newly Added) The semiconductor device of claim 9 wherein said static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.

11. (Newly Added) A semiconductor device comprising:

- at least one active region with a channel conduction surface;
- at least one active device with a vertical conduction;
- a first static unidirectional electric field in said channel conducting region; said first unidirectional electric field having a graded dopant concentration;
- a second static unidirectional electric field in said vertical conduction; said second static unidirectional electric field having a graded dopant concentration; and
- a third static unidirectional electric field; said third static unidirectional electric field having a graded dopant concentration.

12. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is a silicon substrate.

13. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is an III-V compound substrate.

14. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is an II-VI compound substrate.

15. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is an organic material substrate.

16. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is a silicon carbide substrate.

17. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one bipolar transistor.

18. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one vertical bipolar transistor.

19. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one planar bipolar transistor with a conducting surface layer.

20. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one MOS transistor.

21. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one IGBT.

22. (Newly Added) A semiconductor device comprising:

a substrate;

a surface layer;

an active region including at least one emitter and one collector disposed in the device;

a single drift layer disposed between said emitter and said collector, said drift layer having at least one graded concentration of dopants, said drift layer further having a first static unidirectional electric field to aid movement of carriers from said emitter to said collector; and

at least one isolation region disposed in the semiconductor device, said isolation region having a graded concentration of dopants and a second static unidirectional electric field to aid movement of carriers.

23. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a varactor.

24. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a varistor.

25. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is an avalanche transistor.

26. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a Zener diode.

27. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a Schottky diode.

28. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a tunneling diode.

29. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is an Esaki diode.

REMARKS

In the specification, the paragraphs [0001], [0003], [0004], [0006], [0008] - [0014], and [0016] - [0022] have been amended to correct editorial problems. The amendments do not contain any new matter.

In amended Figs. 1-16 (all figures) amendments have been made to improve the readability and to correct editorial problems, such as typos. No substantive changes have been made and no new matter has been added.

Applicant has cancelled claims 1-8 and added new claims 9-29.

The Commissioner is authorized to charge any additional fees or deficiencies or credit any overpayments to Eugene M. Cummings, P.C., Deposit Account No. **50-4199**, with reference to attorney docket number (0299-0001.04).

Respectfully submitted,

Law Offices of Eugene M. Cummings P.C.

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