



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/461,380	07/31/2006	Georg Braun	1525.026262 (INFN/WB0310)

CONFIRMATION NO. 3530

POWER OF ATTORNEY NOTICE



OC000000132820169

46798
Patterson & Sheridan, LLP - Qimonda
24 Greenway Plaza, Suite 1600
Houston, TX 77046

Date Mailed: 03/31/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/29/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nrhayden/



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/461,380	07/31/2006	Georg Braun	US PATENT 7532523

CONFIRMATION NO. 3530

POA ACCEPTANCE LETTER

3624
VOLPE KOENIG
30 SOUTH 17TH STREET, 18TH FLOOR
PHILADELPHIA, PA 19103



Date Mailed: 03/31/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/29/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nrhayden/

PETITION TO ACCEPT UNINTENTIONALLY DELAYED PAYMENT OF MAINTENANCE FEE IN AN EXPIRED PATENT (37 CFR 1.378(b))				
Patent Number	Issue Date	Application Number	Filing Date	Docket Number (if applicable)
7532523	12-May-2009	11461380	31-Jul-2006	
CAUTION: Maintenance fee (and surcharge, if any) payment must correctly identify: (1) the patent number and (2) the application number of the actual U.S. application leading to issuance of that patent to ensure the fee(s) is/are associated with the correct patent. 37 CFR 1.366(c) and (d).				
Applicants claims the following fee status:				
☐ Small Entity				
☐ Micro Entity				
☒ Regular Undiscounted				
Applicants selects the following :				
☐ 3 1/2		☐ 7 1/2		☒ 11 1/2
PETITION FEE The petition fee required by 37 CFR 1.17(m) (Fee Code 1558/2558) must be paid as a condition of accepting unintentionally delayed payment of the maintenance fee.				
MAINTENANCE FEE (37 CFR 1.20(e)-(g)) The appropriate maintenance fee must be submitted with this petition.				
STATEMENT The delay in payment of the maintenance fee for this patent was unintentional. Petitioner is reminded that a delay resulting from a deliberately chosen course of action or a change in circumstance is not an unintentional delay. Petitioner is further reminded that a person seeking reinstatement of an expired patent should not make a statement that the delay in payment of the maintenance fee was unintentional unless the entire delay was unintentional, including the period from discovery that the maintenance fee was not timely paid until payment of the maintenance fee. For example, a statement that the delay in payment of the maintenance fee was unintentional would not be proper when the patentee becomes aware of an unintentional failure to timely pay the maintenance fee and then intentionally delays filing a petition for reinstatement of the patent under 37 CFR 1.378. See MPEP 2590. NOTE: Where the petition under 37 CFR 1.378 is filed more than two years after the date the patent expired for nonpayment of the maintenance fee, the United States Patent and Trademark Office requires an additional explanation of the circumstances surrounding the delay that establishes the entire delay was unintentional. This requirement is in addition to the requirement to provide a statement that the entire delay was unintentional. See <i>Clarification of the Practice for Requiring Additional Information in Petitions Filed in Patent Applications and Patents Based on Unintentional Delay</i> , 85 FR 12222 (March 2, 2020). See MPEP 711.03(c)(II)(C)-(F) for additional guidance on the information required to establish that the entire delay was unintentional.				
PETITIONER(S) REQUEST THAT THE DELAYED PAYMENT OF THE MAINTENANCE FEE BE ACCEPTED AND THE PATENT REINSTATED				
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES 37 CFR 1.378(c) states: "Any petition under this section must be signed in compliance with 37 CFR 1.33(b) ."				
I certify, in accordance with 37 CFR 1.4(d)(4) that I am				

- ☒ An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application.
- ☐ An attorney or agent registered to practice before the Patent and Trademark Office
- ☐ A sole patentee
- ☐ A joint patentee; I certify that I am authorized to sign this submission on behalf of all the other patentees as evidenced by the power of attorney in the application
- ☐ A joint patentee; all of whom are signing this e-petition
- ☐ The assignee of record of the entire interest that qualifies as an authorized party under 37 CFR 1.33(b)

Attorney

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature

Signature	/ROBERT D. LEONARD/		
Name	ROBERT D. LEONARD	Registration Number	57204

Electronic Patent Application Fee Transmittal

Application Number:	11461380			
Filing Date:	31-Jul-2006			
Title of Invention:	MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT			
First Named Inventor/Applicant Name:	Georg Braun			
Filer:	Robert D. Leonard/Angel Wolf			
Attorney Docket Number:	US PATENT 7532523			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
MAINTENANCE FEE DUE AT 11.5 YEARS	1553	1	7700	7700
PET. DELAY PYMT MAINTAIN PATENT IN FORCE	1558	1	2100	2100
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				9800



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Patent No. 7532523 :
Issue Date: May 12,2009 :
Application No. 11461380 :DECISION GRANTING PETITION
Filed: July 31,2006 :UNDER 37 CFR 1.378(b)
Attorney Docket No. US PATENT 7532523 :

This is a decision on the electronic petition, filed March 30,2022 ,under 37 CFR 1.378(b)
to accept the unintentionally delayed payment of the 11.5 year maintenance fee for the above-identified patent.

The petition is **GRANTED**.

The maintenance fee is accepted, and the above-identified patent reinstated as of March 30,2022 .
This decision also constitutes notice that the fee has been accepted. An electronic copy of the petition and
this decision has been created as an entry in the Image File Wrapper. Nevertheless, petitioner should print
and retain an independent copy.

Telephone inquiries related to this electronic decision should be directed to the Electronic Business Center at 1-866-217-9197.

Electronic Acknowledgement Receipt

EFS ID:	45352668
Application Number:	11461380
Patent Number:	7532523
Confirmation Number:	3530
Petition Issued Date:	March 30,2022
Title of Invention:	MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT
First Named Inventor/Applicant Name:	Georg Braun
Customer Number:	3624
Filer:	Robert D. Leonard/Angel Wolf
Filer Authorized By:	Robert D. Leonard
Attorney Docket Number:	US PATENT 7532523
Receipt Date:	30-MAR-2022
Filing Date:	31-JUL-2006
Time Stamp:	12:34:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$9800
RAM confirmation Number	E20223TC34172967
Deposit Account	220493
Authorized User	Angel Wolf
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

37 CFR 1.16 (National application filing, search, and examination fees)
 37 CFR 1.17 (Patent application and reexamination processing fees)
 37 CFR 1.19 (Document supply fees)
 37 CFR 1.20 (Post Issuance fees)
 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	ePetition Request Form	petition-request.pdf	47988	no	2
			ecc4cff11e7f1ebc03ab059b3ffd901fab32360		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	40345	no	2
			be851f98b41d21389509e1386568f881904d952a		

Warnings:

Information:

Total Files Size (in bytes):			88333
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	7532523
	Issue Date	May 12, 2009
	First Named Inventor	Georg Braun
	Title	MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT
	Attorney Docket No.	US Patent 7532523

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

3624

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or

Individual Name:

Address:

City:

State:

Zip:

Country:

Telephone:

Email:

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on: herewith

SIGNATURE of Applicant or Patent Owner

Signature		Date	Mar 24, 2009
Name	Michael McCartney	Telephone	
Title and Company	VP Program Development		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.31A. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-6188 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: POLARIS INNOVATIONS LIMITEDApplication No./Patent No.: 7532523 Filed/Issue Date: May 12, 2009Titled: MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUITPOLARIS INNOVATIONS LIMITED, a Company

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: BRAUN et al To: QIMONDA AG

The document was recorded in the United States Patent and Trademark Office at

Reel 018396, Frame 0075, or for which a copy thereof is attached.2. From: QIMONDA AG To: INFINEON TECHNOLOGIES AG

The document was recorded in the United States Patent and Trademark Office at

Reel 035623, Frame 0001, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)3. From: INFINEON TECHNOLOGIES AG To: POLARIS INNOVATIONS LIMITED

The document was recorded in the United States Patent and Trademark Office at
 Reel 036701, Frame 0926, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Robert D. Leonard/

March 29, 2022

Signature

Date

Robert D. Leonard

57204

Printed or Typed Name

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45346974
Application Number:	11461380
International Application Number:	
Confirmation Number:	3530
Title of Invention:	MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT
First Named Inventor/Applicant Name:	Georg Braun
Customer Number:	46798
Filer:	Robert D. Leonard/Angel Wolf
Filer Authorized By:	Robert D. Leonard
Attorney Docket Number:	1525.026262 (INFN/WB0310)
Receipt Date:	29-MAR-2022
Filing Date:	31-JUL-2006
Time Stamp:	17:27:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_7532523_20220329_EFS.pdf	1161843 390e209a1cdf2160436a9e94b7c8f1cfd1c1b5e	no	1

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	US_PATENT_7532523_373_STAT EMENT.pdf	201149	no	3
			94529a7626ba82ce1d2bcfda05bf3090f066 c897		
Warnings:					
Information:					
Total Files Size (in bytes):				1362992	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court _____ the District of Delaware _____ on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED 2/8/2022	U.S. DISTRICT COURT the District of Delaware
PLAINTIFF Polaris Innovations Limited		DEFENDANT Xilinx, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,157,589	12/5/2000	Polaris Innovations Limited
2 7,145,369	12/5/2006	Polaris Innovations Limited
3 7,532,523	5/12/2009	Polaris Innovations Limited
4 6,702,473	3/2/2004	Polaris Innovations Limited
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

TO: Mail Stop 8
 Director of the U.S. Patent & Trademark Office
 P.O. Box 1450
 Alexandria, VA 22313-1450

**REPORT ON THE
 FILING OR DETERMINATION OF AN
 ACTION REGARDING A PATENT OR
 TRADEMARK**

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of California on the following:

(X) Patents or () Trademarks

DOCKET NO:
17-cv-07157-JCS

DATE FILED:
 December 15, 2017

UNITED STATES DISTRICT COURT
 Phillip Burton Federal Building
 450 Golden Gate Avenue, 16th Floor
 San Francisco, CA 94102

PLAINTIFF:
Polaris Innovations Ltd.

DEFENDANT:
Elite Semiconductor Memory Technologies, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1. <u>6653882</u>		***see attach Complaint***
2. <u>6728143</u>		
3. <u>7532523</u>		
4.		
5.		

In the above-entitled case, the following patent(s) have been included.

DATE INCLUDED INCLUDED BY:
 () Amendment () Answer () Cross Bill () Other Pleading

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1.		
2.		
3.		
4.		
5.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT:

Susan Y. Soong
 Susan Y. Soong, Clerk

Gina Augustine
 (by) Deputy Clerk, Gina Augustine

Copy 1 – Upon initiation of action, mail this copy to Commissioner
 Copy 2 – Upon filing document adding patent(s) mail this copy to Commissioner
 Copy 3 – Upon termination of action, mail this copy to the Commissioner
 Copy 4 – Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/461,380	05/12/2009	7532523	1525.026262 (INFN/WB0310)	3530

46798 7590 04/22/2009
PATTERSON & SHERIDAN, LLP
Gero McClellan / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 263 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Georg Braun, Holzkirchen, GERMANY;
Christian Weis, Munich, GERMANY;
Eckehard Plaettner, Oberhaching, GERMANY;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

46798 7590 01/13/2009

PATTERSON & SHERIDAN, LLP
Gero McClellan / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/461,380	07/31/2006	Georg Braun	1525.026262 (INFN/WB0310)	3530

TITLE OF INVENTION: MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	04/13/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-194000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Patterson & Sheridan, L.L.P.

2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Qimonda AG

Munich, Germany

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. ~~Form PTO 2028 is attached.~~
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **20-0782** (enclose an extra copy of this form)

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature **/Joseph M. JONG, Reg. #42698/**

Date **April 3, 2009**

Typed or printed name **Joseph M. Jong**

Registration No. **42,698**

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		11461380		
Filing Date:		31-Jul-2006		
Title of Invention:		MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT		
First Named Inventor/Applicant Name:		Georg Braun		
Filer:		Joseph M. Jong		
Attorney Docket Number:		1525.026262 (INFN/WB0310)		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt

EFS ID:	5090735
Application Number:	11461380
International Application Number:	
Confirmation Number:	3530
Title of Invention:	MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT
First Named Inventor/Applicant Name:	Georg Braun
Customer Number:	46798
Filer:	Joseph M. Jong
Filer Authorized By:	
Attorney Docket Number:	1525.026262 (INFN/WB0310)
Receipt Date:	03-APR-2009
Filing Date:	31-JUL-2006
Time Stamp:	12:32:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1810
RAM confirmation Number	6662
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	0310_IssueFeeXmtl.pdf	86148 f6b99f7ab1d7c346074cf71d0a72cceabaa5843a	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	32048 fcc00ce5d9e8cca450acb32045420de713d27a74	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			118196		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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NOTICE OF ALLOWANCE AND FEE(S) DUE

46798 7590 01/13/2009

PATTERSON & SHERIDAN, LLP
Gero McClellan / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

EXAMINER

SOFOCLEOUS, ALEXANDER

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 01/13/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/461,380	07/31/2006	Georg Braun	1525.026262 (INFN/WB0310)	3530

TITLE OF INVENTION: MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	04/13/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46798 7590 01/13/2009

PATTERSON & SHERIDAN, LLP
 Gero McClellan / Qimonda
 3040 POST OAK BLVD.,
 SUITE 1500
 HOUSTON, TX 77056

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/461,380	07/31/2006	Georg Braun	1525.026262 (INFN/WB0310)	3530

TITLE OF INVENTION: MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	04/13/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-194000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/461,380	07/31/2006	Georg Braun	1525.026262 (INEN/WB0310)	3530
46798	7590	01/13/2009	EXAMINER	
PATTERSON & SHERIDAN, LLP Gero McClellan / Qimonda 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056			SOFOCLEOUS, ALEXANDER	
			ART UNIT	PAPER NUMBER
			2824	
DATE MAILED: 01/13/2009				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 263 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 263 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

11/461,380

Examiner

ALEXANDER SOFOCLEOUS

Applicant(s)

BRAUN ET AL.

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendmend filed September 19, 2008.
2. ☒ The allowed claim(s) is/are 6-9,16-19,25 and 26.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ | 7. ☐ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☐ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other ____. |

DETAILED ACTION

1. This action is responsive to the following communication: the Amendment filed September 19, 2008.
2. Claims 6-9, 16-19, 25, and 26 are pending in the case. Claims 1-5, 10-15, and 20-24 are cancelled. Claims 6, 16, 17, and 25 are currently amended. Claims 6, 16, and 25 are independent claims.

Specification

3. The proposed specification corrections (Title, Abstract) received on September 19, 2008 are acceptable.

Drawings

4. The drawings were received on September 19, 2008. These drawings are acceptable.

Allowable Subject Matter

5. **Claims 6-9, 16-19, 25, and 26 are allowed.**
6. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 6, 16, and 25, the record of the prosecution as a whole makes clear the reasons for allowance.

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

/VanThu Nguyen/
Primary Examiner, Art Unit 2824

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	11/461380	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 16:02
S4	16	S2 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 18:55
S3	61142	(terminat\$3 same memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 18:55
S2	158	(365/189.17).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 18:55
S20	78	S12 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S19	77	S11 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S18	131	S10 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S17	156	S9 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02

S16	0	S8 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S15	5	S7 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S14	5	S6 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S13	367	S5 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S12	771	(365/206).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S11	266	(365/198).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S10	1019	(365/191).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S9	1752	(365/51).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S8	173	(327/382).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02

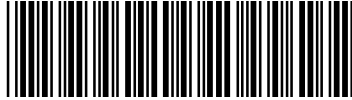
S7	586	(327/379).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S6	761	(327/310).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S5	2025	(326/30).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S21	206	(S13 S14 S15 S16 S17 S18 S19 S20) AND (terminat\$3 with resist \$4) AND ((adjust\$4 or configur\$4 or sett\$4) with resist\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/12 19:03
S22	208	(S13 S14 S15 S16 S17 S18 S19 S20) AND (terminat\$3 with (resist \$4 or resistances)) AND ((adjust\$4 or configur\$4 or sett\$4) with (resist \$4 or resistances))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/12 19:04
S23	6466	(configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:33
S25	346	(configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:34
S24	1558	(configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:34
S26	88	(configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory with (array or chip or module))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:35

S27	97	(calibrat\$3 or configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory with (array or chip or module))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:38
S28	97	(calibrat\$3 or configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory with (array or chip or module)) and ((calibrat\$3 or configur\$4 or set\$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with (resist\$4 or resistance\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 13:28
L1	14962	terminat\$3 with delay	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 16:26
L3	252	1 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 16:34
L2	6641	((326/30) or (365/191,194,198,206)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/01/07 16:34
L6	5855	(memory) (terminat\$3 with delay)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 16:35
L5	51	2 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 16:35
L4	1286	terminat\$3 with delay with resist\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 16:35

L7	198	2 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 16:36
L8	450	memory (terminat\$3 with delay) (resist\$4 near2 (vary\$3 or vari\$4 or set or setting or settable))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 17:24
L9	29	2 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/01/07 17:25

1/7/2009 5:40:30 PM

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<i>Index of Claims</i> 	Application/Control No. 11461380	Applicant(s)/Patent Under Reexamination BRAUN ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	06/13/2008	01/07/2009						
	1	✓	-						
	2	✓	-						
	3	✓	-						
	4	✓	-						
	5	✓	-						
	6	O	=						
	7	O	=						
	8	O	=						
	9	O	=						
	10	✓	-						
	11	✓	-						
	12	✓	-						
	13	✓	-						
	14	✓	-						
	15	✓	-						
	16	O	=						
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	18	O	=						
	19	O	=						
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	22	✓	-						
	23	✓	-						
	24	✓	-						
	25	O	=						
	26	O	=						

Search Notes 	Application/Control No. 11461380	Applicant(s)/Patent Under Reexamination BRAUN ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

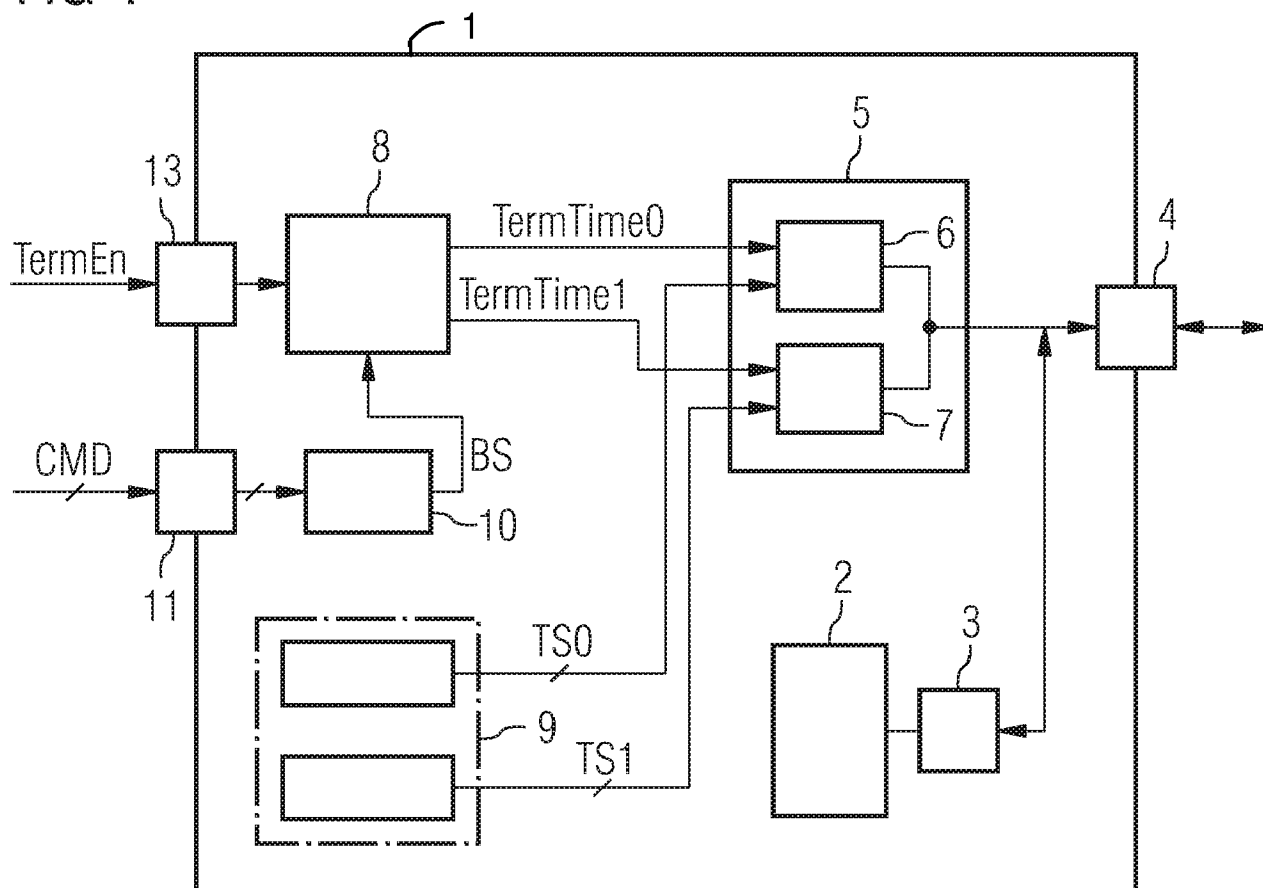
SEARCHED			
Class	Subclass	Date	Examiner
326	30	06/12/2008	AGS
365	51, 189.17, 191, 198, 206	06/12/2008	AGS
326	30	01/07/2009	AGS
365	191, 194, 198, 206	01/07/2009	AGS

SEARCH NOTES		
Search Notes	Date	Examiner
see EAST search history	06/13/2008	AGS
consulted VanThu Nguyen regarding class 365	01/06/2009	AGS
see updated EAST search history	01/07/2009	AGS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
326	30	01/07/2009	AGS
365	194, 198, 206	01/07/2009	AGS

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FIG 1



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT



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BIB DATA SHEET

CONFIRMATION NO. 3530

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
11/461,380	07/31/2006	326	2824	1525.026262 (INFN/WB0310)		
RULE						
APPLICANTS Georg Braun, Holzkirchen, GERMANY; Christian Weis, Munich, GERMANY; Eckehard Plaettner, Oberhaching, GERMANY; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** GERMANY DE 102005035780.6 07/29/2005 GERMANY DE 102005036528.0 08/03/2005 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/16/2006						
Foreign Priority claimed ☒ Yes ☐ No	35 USC 119(a-d) conditions met ☒ Yes ☐ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Verified and /ALEXANDER SOFOCLEOUS/	Acknowledged	Examiner's Signature	GERMANY	5	26	3
Initials						
ADDRESS PATTERSON & SHERIDAN, LLP Gero McClellan / Qimonda 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056 UNITED STATES						
TITLE MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT						
FILING FEE RECEIVED 1430	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees			
			☐ 1.16 Fees (Filing)			
			☐ 1.17 Fees (Processing Ext. of time)			
			☐ 1.18 Fees (Issue)			
			☐ Other _____			
☐ Credit						

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/461,380		Filing Date 07/31/2006		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	10/22/2008	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 10	Minus	** 26	= 0	X \$ =	OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$ =	OR	X \$220=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/JAMES w. TUNSTALL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	Filed: July 31, 2006
Braun et al.	§	
	§	Group Art Unit: 2824
Serial No.: 11/461,380	§	
	§	Examiner: Alexander Sofocleous
Confirmation No.: 3530	§	

For: MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office to fax number 571-273-8300 to the attention of Examiner Alexander Sofocleous, or electronically transmitted via EFS-Web, on the date shown below:

September 19, 2008
Date

/Joseph Jong/
Joseph Jong

RESPONSE TO OFFICE ACTION DATED JUNE 19, 2008

In response to the Office Action dated June 19, 2008, having a shortened statutory period for response set to expire on September 19, 2008, please enter this response and reconsider the claims pending in the application for reasons discussed below. While no fees are believed due, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 20-0782 / 1525.026262 (INFN/WB0310) / GGM for any fees, including extension of time fees or excess claim fees, required to make this response timely and acceptable to the Office.

Amendments to the Specification begin on page 2 of this paper. Amendments to the Specification begin on page 3 of this paper. Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper. Amendments to the Drawings begin on page 8 of this paper and include two attached replacement sheets. Remarks/Arguments begin on page 9 of this paper.

IN THE SPECIFICATION:

Please replace the title with the following amended title:

**MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP WITH
SETTABLE TERMINATION RESISTANCE CIRCUIT**

IN THE ABSTARCT:

Please replace the Abstract with the following amended Abstract:

Methods and apparatus for setting various terminations of a memory chip. ~~In one embodiment, the~~ The memory chip includes a terminal, a termination circuit that can be connected to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination circuit in order to set a resistance value as a function of a received control command signal.

IN THE CLAIMS:

Please cancel claims 1-5, 10-15 and 20-24, and amend the claims as follows:

1-5. (Canceled)

6. (Currently Amended) A memory chip for variably setting terminations, comprising:

a terminal;

a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

a control command port for receiving a control command signal for affecting accessibility of the memory chip;

a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,

~~The memory chip of claim 5, wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.~~

7. (Original) The memory chip of claim 6, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

8. (Original) The memory chip of claim 7, wherein the control circuit sets the first

switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

9. (Original) The memory chip of claim 8, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal.

10-15. (Canceled)

16. (Currently Amended) A system, comprising:
(a) a memory controller having a terminal;
(b) a plurality of memory chips, at least one of the memory chips comprising:
a terminal;
a termination circuit connectable with the terminal and configured to
terminate the terminal according to a settable resistance value;
a control command port for receiving a control command signal for
affecting accessibility of the memory chip; and
a control circuit connected to the termination circuit and configured to set
the resistance value as a function of the received control command signal;
(c) a memory bus comprising a signal line interconnecting the terminals of the
memory chips and the terminal of the memory controller; and
(d) a termination port to receive a termination signal, wherein the control
circuit is configured to selectively terminate the terminal of the respective memory chip
with the set resistance value in response to the termination signal.

~~The system of claim 15,~~ wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

17. (Currently Amended) The system of ~~claim 11~~ claim 16, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

18. (Previously Presented) The system of claim 17, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

19. (Previously Presented) The system of claim 18, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal of the respective memory chip, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal of the respective memory chip.

20-24. (Canceled)

25. (Currently Amended) A method for operating a memory chip, comprising:
receiving a control command signal for affecting accessibility of the memory chip;
setting a resistance value for a terminal as a function of the control command
signal;
terminating the terminal with the resistance value. ~~The method of claim 24,~~
wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and
receiving a termination enable signal, the presence of which is required for the
terminating to occur.

26. (Original) The method of claim 25, further comprising:
changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal;
and
terminating the terminal with the changed resistance value.

IN THE DRAWINGS:

The attached sheet of drawings includes changes to Figures 1 and 2.

Attachment: Two Replacement Sheets

REMARKS

This is intended as a full and complete response to the Office Action dated June 19, 2008, having a shortened statutory period for response set to expire on September 19, 2008. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-26 are pending in the application. Claims 6-9, 16-19 25 and 26 remain pending following entry of this response. Claims 6, 16, 17 and 25 have been amended. Claims 1-5, 10-15 and 20-24 have been canceled. Applicants submit that the amendments do not introduce new matter.

Drawing Objections

Figures 1 and 2 have been amended to include a legend of the reference numerals within each figure. The legends are believed to be sufficient alternatives to directly labeling the rectangular boxes.

Specification Objections

The title and the abstract have been amended as suggested by the Examiner.

Claim Rejections - 35 U.S.C. § 102

Claims 1-5, 10-15 and 20-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Jang et al.* (U.S. Patent 6,762,620).

Claims 1-5, 10-15 and 20-24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by *Park* (U.S. Patent 7,148,721).

Claims 1-5, 10-15 and 20-24 have been canceled. Therefore, the rejections are believed to be moot. Withdrawal of the rejections is respectfully requested.

Allowable Subject Matter

Claims 6-9, 16-19, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the

amendments presented above, claims 6-9, 16-19, 25 and 26 are believed to be in condition for allowance.

Applicants have amended claims 6, 16, 17 and 25 and cancelled claims 1-5, 10-15 and 20-24 from further consideration in this application. Applicants are not conceding in this application that those claims (i.e., pre-amended and/or canceled claims) are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the Examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

Conclusion

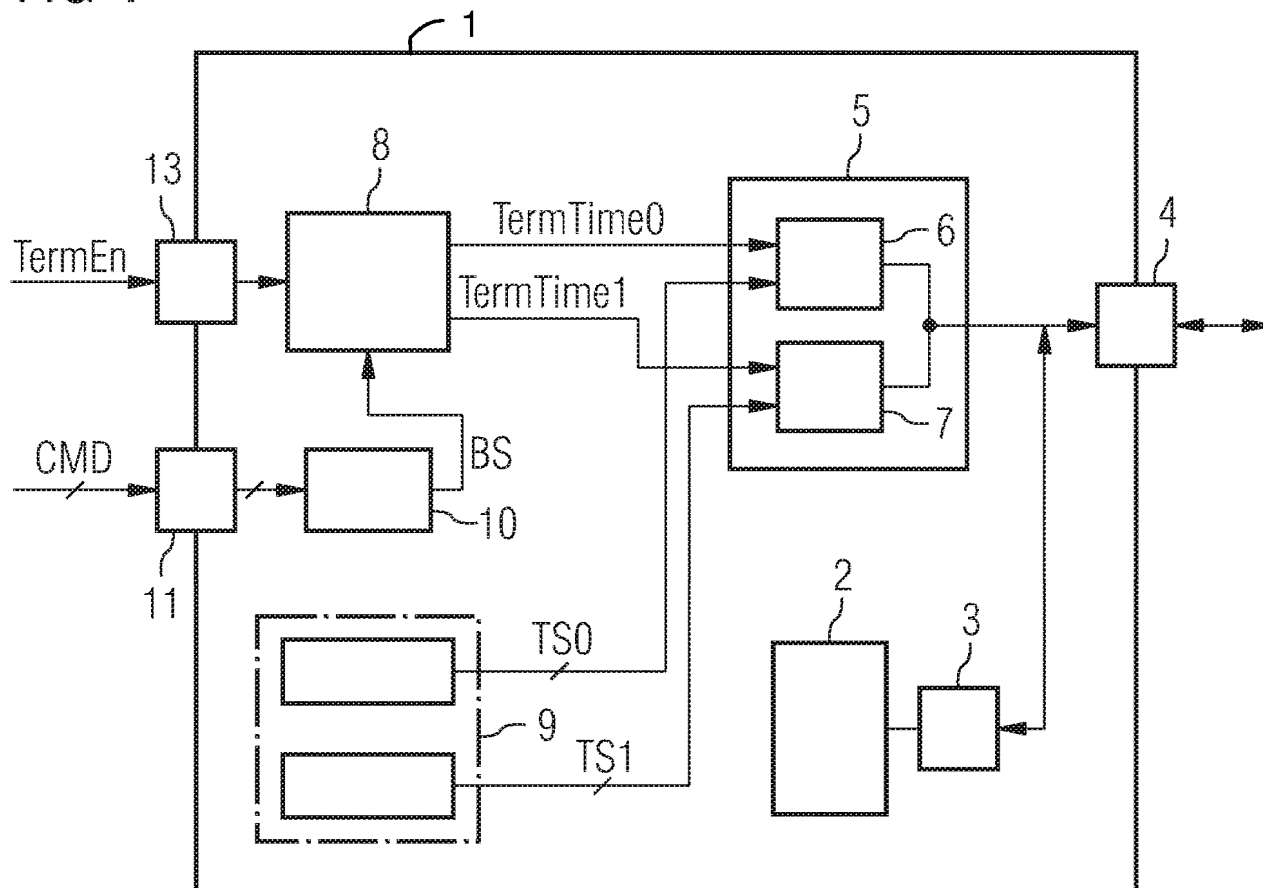
Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

/Gero G. McClellan, Reg. No. 44,227/

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3040 Post Oak Blvd. Suite 1500
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Facsimile: (713) 623-4846
Attorney for Applicants

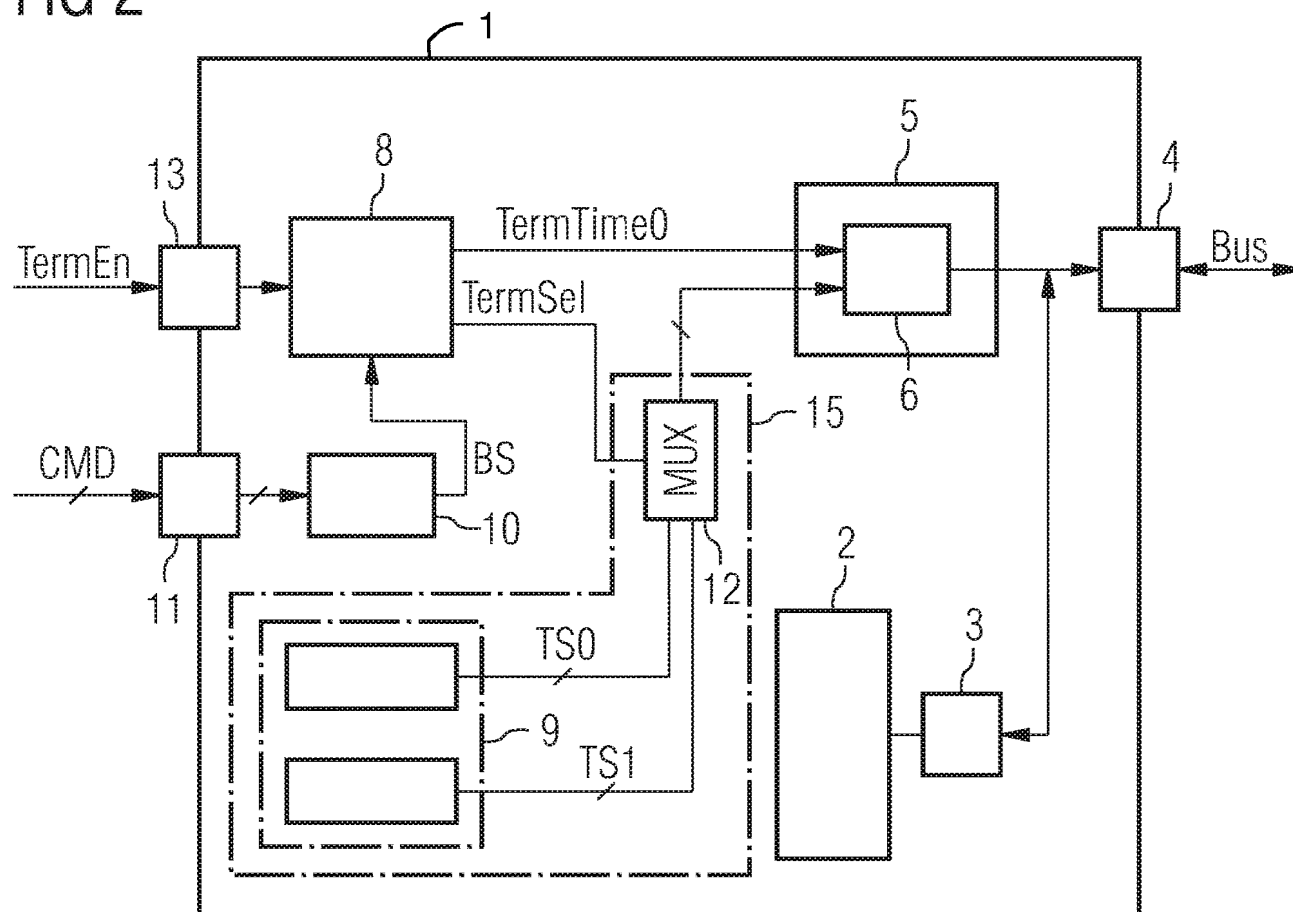
FIG 1



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT

FIG 2



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 12 - MULTIPLEXER
- 13 - EXTERNAL TERMINATION PORT
- 15 - SETTING UNIT

Electronic Acknowledgement Receipt

EFS ID:	3976038
Application Number:	11461380
International Application Number:	
Confirmation Number:	3530
Title of Invention:	MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP
First Named Inventor/Applicant Name:	Georg Braun
Customer Number:	46798
Filer:	Gero G. McClellan/Joseph Jong
Filer Authorized By:	Gero G. McClellan
Attorney Docket Number:	1525.026262 (INFN/WB0310)
Receipt Date:	19-SEP-2008
Filing Date:	31-JUL-2006
Time Stamp:	18:20:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		0310_ROA.pdf	92276 bf799ac01f6dd8027f955d5b88b892fc349849ec	yes	10

Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Amendment/Req. Reconsideration-After Non-Final Reject			1	1	
Specification			2	2	
Abstract			3	3	
Claims			4	7	
Drawings-only black and white line drawings			8	8	
Applicant Arguments/Remarks Made in an Amendment			9	10	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	0310_ReplacementSheets.pdf	32759	no	2
			4f92592d1a8f6b37ee627d8d8f49396b2efd0941		
Warnings:					
Information:					
Total Files Size (in bytes):			125035		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/461,380	07/31/2006	Georg Braun	1525.026262 (INFN/WB0310)	3530
46798 7590 06/19/2008 PATTERSON & SHERIDAN, LLP Gero McClellan / Qimonda 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056			EXAMINER SOFOCLEOUS, ALEXANDER	
			ART UNIT 2824	PAPER NUMBER
			MAIL DATE 06/19/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/461,380	Applicant(s) BRAUN ET AL.	
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 10-15 and 20-24 is/are rejected.
- 7) ☒ Claim(s) 6-9, 16-19, 25 and 26 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>11/7/07</u> . | 6) ☐ Other: ____. |

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed July 31, 2006, the Information Disclosure Statement filed November 7, 2007, the Foreign Priority filed November 13, 2007, and the Foreign Priority filed November 13, 2007.
2. Claims 1-26 are pending in the case. Claims 1, 11, and 21 are independent claims.

Information Disclosure Statement

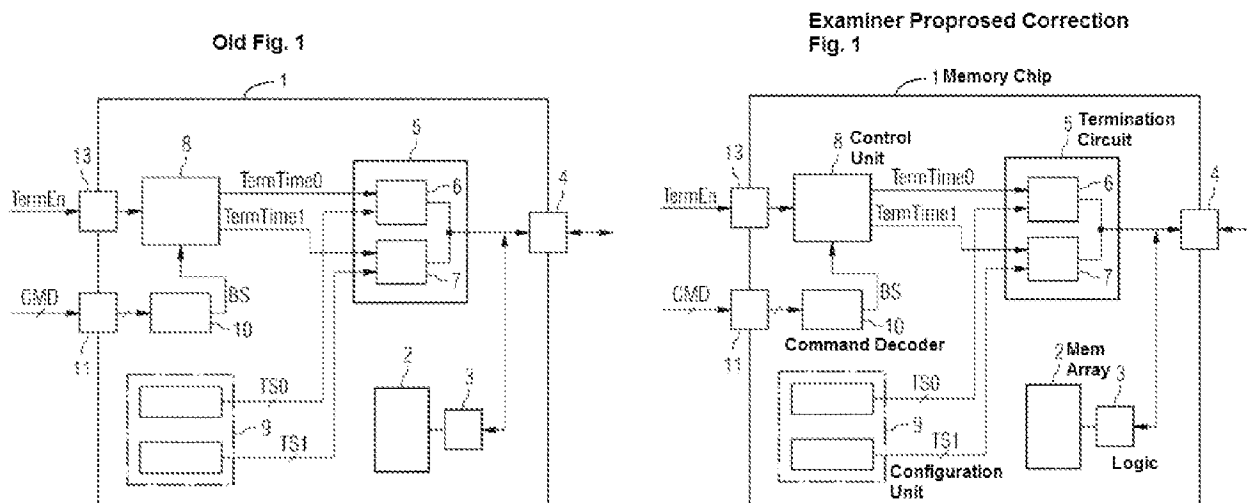
3. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on November 7, 2007. This IDS has been considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

5. Figure 1 and Figure 2 are objected to because the unlabeled rectangular box(es) shown in the Figures should be provided with descriptive text labels. For clarity purposes, Examiner suggests the following proposed correction for Figure 1; although Applicant is welcomed to suggest alternate corrections. Similar corrections should be made to Figure 2.



6. The abstract of the disclosure is objected to because of the following minor informalities: phraseology that may be implied.

In the Abstract, line 2, it is suggested to change "In one embodiment, the memory chip" to --The memory chip--.

Correction is required. See MPEP § 608.01(b).

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested, although Applicant is welcomed to provide alternate suggestions: Memory Chip with Adjustable Termination Resistance Circuit.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-5, 10-15, and 20-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Jang et al. (U.S. Patent 6,762,620).

Regarding independent claims 1 and 11, Jang et al. show a memory system (see column 1, lines 12-14), comprising:

(a) a memory controller (not shown but implicit; see e.g., column 1, lines 12-14, 51-53) having terminal;

(b) a plurality of memory chips (not shown but implicit; see e.g., column 1, lines 12-14, 51-53);

at least one of the memory chips comprising:

a terminal (Fig. 7: PD1);

a termination circuit (Fig. 4: 400; Fig. 7: 400-11...400-1N) connectable with the terminal (Fig. 7: PD1) and configured to terminate the terminal according to a settable resistance value (see Fig. 7: DRP1...DRPn, DRN1...DRNn);

a control command port (Fig. 4: IN) for receiving a control command signal (Fig.

4: IN; see column 12, lines 48-54) for affecting accessibility of the memory chip; and
a control circuit (Fig. 4: 300; Fig. 6-1: 300) connected to the termination circuit (Fig. 4: 400) and configured to set the resistance value as a function of the received control command signal (see Fig. 4: IN to 200 to MRS_DQi; see Fig. 6-1: MRS_DQi input to 300, ICONPi and CONNi output from 300; see Fig. 7: ICONPi and CONNi select the resistors DRP1...DRPn and DRN1...DRNn); and

(c) a memory bus (not shown but implicit; see e.g., column 1, lines 12-14, 51-53) comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller.

Regarding dependent claims 2 and 12, Jang et al. show the termination circuit comprises a plurality of terminating resistors (see Fig. 7: DRP1...DRPn, DRN1...DRNn) each having respective resistance values, wherein the control circuit (Fig. 4: 300; Fig. 6-1: 300) sets the resistance value by selecting at least one of the terminating resistors and applying it to the terminal of the respective memory chip (see Fig. 7: DRP1...DRPn, DRN1...DRNn).

Regarding dependent claims 3 and 13, Jang et al. show a configuration unit (Fig. 4: 100, CONPi, CONNi; Fig. 5: CONPi, CONNi become ICONPi, CONNi) configured to set the resistance values of the plurality of terminating resistors (see Fig. 7: ICONP1...ICONPn and CONN1...CONNn control the selection of resistors DRP1...DRPn and DRN1...DRNn).

Regarding dependent claims 4 and 14, Jang et al. show the termination circuit (Fig. 4: 400; 7: 400) comprises a settable terminating resistor (Fig. 7: DRP1...DRPn and

DRN1...DRNn), and further comprising:

a setting circuit (see Fig. 7: 400-11...400-1n) configured to selectively output a setting value (see Fig. 7: DRP1...DRPn and DRN1...DRNn outputting to PD1) on the basis of which the terminating resistor is set to the resistance value.

Regarding dependent claims 5 and 15, Jang et al. show a termination port (see Fig. 4: MRS_DQi) to receive a termination signal (Fig. 4: MRS_DQi) the control circuit (Fig. 4: 300) being configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal (see Fig. 4: MRS_DQi from 200 to 300 with respect to Fig. 6-1: MRS_DQi to 300 to control the output of ICONPi and ICONNi with respect to Fig. 7: ICONP1...ICONPn and ICONN1...ICONNn control the selection of resistors DRP1...DRPn and DRN1...DRNn).

Regarding dependent claims 10 and 20, Jang et al. show a command decoder (Fig. 4: 200) operable, as a function of the received control command signal (Fig. 4: IN; see column 12, lines 48-54), to communicate to the control circuit whether the resistance value is to be set to a first value or a second value (see Fig. 4: MRS_DQi from 200 to 300 with respect to Fig. 6-1: MRS_DQi to 300 to control the output of ICONPi and ICONNi with respect to Fig. 7: ICONP1...ICONPn and ICONN1...ICONNn control the selection of resistors DRP1...DRPn and DRN1...DRNn).

Regarding independent claim 21, Jang et al. show a method for operating a memory chip (see column 1, lines 12-14), comprising:

receiving a control command signal (Fig. 4: IN) for affecting accessibility of the

memory chip;

setting a resistance value for a terminal as a function of the control command signal (see Fig. 4: IN to 200 to MRS_DQi; see Fig. 6-1: MRS_DQi input to 300, ICONPi and ICONNi output from 300; see Fig. 7: ICONPi and ICONNi select the resistors DRP1...DRPn and DRN1...DRNn); and

terminating the terminal (Fig. 7: PD1) with the resistance value.

Regarding dependent claim 22, Jang et al. show setting the resistance value comprises selecting a setting value (see Fig. 7: DRP1...DRPn and DRN1...DRNn outputting to PD1) for a settable terminating resistor.

Regarding dependent claim 23, Jang et al. show setting the resistance value comprises selecting from a plurality of terminating resistors (Fig. 7: DRP1...DRPn and DRN1...DRNn) connected to the terminal (Fig. 7: PD1).

Regarding dependent claim 24, Jang et al. show receiving a termination enable signal (Fig. 4: MRS_DQi), the presence of which is required for the terminating to occur.

10. Claims 1-5, 10-15, and 20-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Park (U.S. Patent 7,148,721).

Regarding independent claims 1 and 11, Park shows a memory system (Fig. 2), comprising:

(a) a memory controller (not shown but implicit; see e.g., column 1, line 22: DDR; it is well-known in the art that DDR memory uses a memory controller) having terminal;

(b) a plurality of memory chips (not shown but implicit; see e.g., column 1, line

22: DDR; it is well-known in the art that DDR memory is a module with many memory chips);

at least one of the memory chips comprising:

a terminal (Fig. 2: PAD4...PAD6);

a termination circuit (Fig. 2: 290) connectable with the terminal (Fig. 2: PAD4...PAD6) and configured to terminate the terminal according to a settable resistance value (see Fig. 2: 290; Fig. 8: 290; Fig. 11: 1R...64R connectable by UPC<6>...UPC<0> and DNC<6>...DNC<0>);

a control command port (Fig. 2: PAD1...PAD3) for receiving a control command signal (see e.g., Fig. 2: PAD1...PAD3 are connected to command buffer 230) for affecting accessibility of the memory chip; and

a control circuit (Fig. 2: 340) connected to the termination circuit (Fig. 2: 290 by signal UPC) and configured to set the resistance value as a function of the received control command signal (see Fig. 2: PAD1...PAD3 connecting to 230 connecting to 330 connecting to SEL of 340 connecting to UPC to control 290); and

(c) a memory bus (not shown but implicit; see e.g., column 1, line 22; it is well-known that DDR uses a memory bus) comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller.

Regarding dependent claims 2 and 12, Park shows the termination circuit comprises a plurality of terminating resistors (see Fig. 11: 1R...64R) each having respective resistance values, wherein the control circuit (Fig. 340) sets the resistance value by selecting at least one of the terminating resistors and applying it to the terminal

of the respective memory chip (see Fig. 11: UPC and DPC controls the selection of 1R...64R).

Regarding dependent claims 3 and 13, Park shows a configuration unit (Fig. 2: 310 and 320) configured to set the resistance values of the plurality of terminating resistors (see Fig. 2: 310 and 320 output UPCF DNCF, UPCV, DNCV to control 340 outputting UPC and DNC to control the selection of certain Termination resistors of 290; see Fig. 11: 64WP...1WP and 64WN...1WN with respect to 1R...64R).

Regarding dependent claims 4 and 14, Park shows the termination circuit (Fig. 2: 290) comprises a settable terminating resistor (Fig. 11: 1R...64R), and further comprising:

a setting circuit (Fig. 2: 310, 320) configured to selectively output a setting value (Fig. 2: 310 or 320 output UPC and DNC to be selected by 340 to control the selection of resistors in 290) on the basis of which the terminating resistor is set to the resistance value.

Regarding dependent claims 5 and 15, Park shows a termination port (see Fig. 2: PAD1...PAD3) to receive a termination signal (see Fig. 2: PAD1...PAD3 connecting to 230 outputting a signal to 330 outputting SEL) the control circuit (Fig. 2: 340) being configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal (see Fig. 2: 340 outputting UPC and DNC to control the selection of certain Termination resistors of 290; see Fig. 11: 64WP...1WP and 64WN...1WN with respect to 1R...64R).

Regarding dependent claims 10 and 20, Park shows a command decoder (Fig.

2: 230) operable, as a function of the received control command signal (Fig. 2: PAD1...PAD3), to communicate to the control circuit whether the resistance value is to be set to a first value or a second value (see Fig. 2: PAD1...PAD3 connecting to 230 outputting a signal to 330 outputting SEL to 340 which selects UPC and DNC from either 320 or 310 to control the selection of certain Termination resistors of 290; see Fig. 11: 64WP...1WP and 64WN...1WN with respect to 1R...64R).

Regarding independent claim 21, Park shows a method for operating a memory chip (Fig. 2; see column 1, line 22), comprising:

receiving a control command signal (Fig. 2: PAD1...PAD3) for affecting accessibility of the memory chip;

setting a resistance value for a terminal as a function of the control command signal (see Fig. 2: PAD1...PAD3 connecting to 230 outputting a signal to 330 outputting SEL to 340 which selects UPC and DNC from either 320 or 310 to control the selection of certain Termination resistors of 290; see Fig. 11: 64WP...1WP and 64WN...1WN with respect to 1R...64R); and

terminating the terminal (Fig. 2: PAD4...PAD6) with the resistance value (see e.g., Fig. 11: 1R...64R to PAD4).

Regarding dependent claim 22, Park shows setting the resistance value comprises selecting a setting value for a settable terminating resistor (see Fig. 2: 340 which selects UPC and DNC from either 320 or 310 to control the selection of certain Termination resistors of 290; see Fig. 11: 64WP...1WP and 64WN...1WN with respect to 1R...64R).

Regarding dependent claim 23, Park shows setting the resistance value comprises selecting from a plurality of terminating resistors (Fig. 11: R1...R64) connected to the terminal (Fig. 2: PD4...PD6).

Regarding dependent claim 24, Park shows receiving a termination enable signal (see Fig. 2: PAD1...PAD3 connecting to 230 outputting a signal to 330 outputting SEL), the presence of which is required for the terminating to occur.

Allowable Subject Matter

11. **Claims 6-9, 16-19, 25, and 26 are objected to as being dependent upon a rejected base claim**, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

With respect to dependent claims 6 (and 7-9 which further depend), 16, and 25(and 26 which further depends), there is no teaching, suggestion, or motivation for combination in the prior art to terminating the terminal of the respective memory chip with the set resistance value after a first time delay or not terminating (stop terminating) the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient (selected) to set the resistance value.

With respect to dependent claim 17 (and 18-19 which further depend), there is no teaching, suggestion, or motivation for combination in the prior art to the

resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Greeff et al. (U.S. Patent 6,356,106) and Funaba et al. (U.S. Patent 6,970,369).

Greeff et al. show a memory system with active termination.

Funaba et al. show a prior art termination circuit for a memory device.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS
/ANH PHUNG/
Primary Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 11/461,380		Applicant(s)/Patent Under Reexamination BRAUN ET AL.	
	Examiner ALEXANDER SOFOCLEOUS		Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,762,620	07-2004	Jang et al.	326/30
*	B	US-7,148,721	12-2006	Park, Youn-Sik	326/30
*	C	US-6,356,106	03-2002	Greeff et al.	326/30
*	D	US-6,970,369	11-2005	Funaba et al.	365/63
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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CONFIRMATION NO. 3530

SERIAL NUMBER 11/461,380	FILING or 371(c) DATE 07/31/2006 RULE	CLASS 326	GROUP ART UNIT 2824	ATTORNEY DOCKET NO. 1525.026262 (INFN/WB0310)	
APPLICANTS Georg Braun, Holzkirchen, GERMANY; Christian Weis, Munich, GERMANY; Eckehard Plaettner, Oberhaching, GERMANY; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** GERMANY DE 102005035780.6 07/29/2005 GERMANY DE 102005036528.0 08/03/2005 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/16/2006					
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /ALEXANDER SOFOCLEOUS/ Acknowledged Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY GERMANY	SHEETS DRAWINGS 5	TOTAL CLAIMS 26	INDEPENDENT CLAIMS 3
ADDRESS PATTERSON & SHERIDAN, LLP Gero McClellan / Qimonda 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056 UNITED STATES					
TITLE MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP					
FILING FEE RECEIVED 1430	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 11461380	Applicant(s)/Patent Under Reexamination BRAUN ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

SEARCHED			
Class	Subclass	Date	Examiner
326	30	06/12/2008	AGS
365	51, 189.17, 191, 198, 206	06/12/2008	AGS

SEARCH NOTES		
Search Notes	Date	Examiner
see EAST search history	06/13/2008	AGS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

<i>Index of Claims</i> 	Application/Control No. 11461380	Applicant(s)/Patent Under Reexamination BRAUN ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	06/13/2008							
	1	✓							
	2	✓							
	3	✓							
	4	✓							
	5	✓							
	6	O							
	7	O							
	8	O							
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	11/461380	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 16:02
S4	16	S2 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 18:55
S3	61142	(terminat\$3 same memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 18:55
S2	158	(365/189.17).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 18:55
S20	78	S12 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S19	77	S11 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S18	131	S10 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02

S17	156	S9 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S16	0	S8 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S15	5	S7 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S14	5	S6 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S13	367	S5 S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/12 19:02
S12	771	(365/206).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S11	266	(365/198).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S10	1019	(365/191).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02

S9	1752	(365/51).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S8	173	(327/382).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S7	586	(327/379).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S6	761	(327/310).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S5	2025	(326/30).OCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/06/12 19:02
S21	206	(S13 S14 S15 S16 S17 S18 S19 S20) AND (terminat\$3 with resist\$4) AND ((adjust\$4 or configur\$4 or sett \$4) with resist\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/12 19:03
S22	208	(S13 S14 S15 S16 S17 S18 S19 S20) AND (terminat\$3 with (resist\$4 or resistances)) AND ((adjust\$4 or configur\$4 or sett \$4) with (resist\$4 or resistances))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/12 19:04

S23	6466	(configur\$4 or set \$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:33
S25	346	(configur\$4 or set \$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:34
S24	1558	(configur\$4 or set \$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:34
S26	88	(configur\$4 or set \$1 or sett\$4 or adjust\$4 or vary\$3 or vari\$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory with (array or chip or module))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:35
S27	97	(calibrat\$3 or configur\$4 or set \$1 or sett\$4 or adjust \$4 or vary\$3 or vari \$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory with (array or chip or module))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 08:38

S28	97	(calibrat\$3 or configur\$4 or set\$1 or sett\$4 or adjust \$4 or vary\$3 or vari \$4) with terminat\$3 with (resist\$4 or resistance\$1) same (memory with (array or chip or module)) and ((calibrat\$3 or configur\$4 or set\$1 or sett\$4 or adjust \$4 or vary\$3 or vari \$4) with (resist\$4 or resistance\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2008/06/13 13:28
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First Named Inventor	Georg Braun
Art Unit	2824
Examiner Name	
Attorney Docket Number	1525.026262 (INFN/WB0310)

U.S. PATENTS

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/AGS/	1	20040228196		2004-11-18	Kwak et al.	

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**INFORMATION DISCLOSURE
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Attorney Docket Number	1525.026262 (INFN/WB0310)

/AGS/	1	DDR2 SDRAM SPECIFICATION, JEDEC Standard No. 79-2A, pages 6 and 14-22, January 2004.	☐
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BUNDESREPUBLIK DEUTSCHLAND



Prioritätsbescheinigung DE 10 2005 036 528.0 über die Einreichung einer Patentanmeldung

Aktenzeichen: 10 2005 036 528.0

Anmeldetag: 03. August 2005

Anmelder/Inhaber: Infineon Technologies AG, 81669 München/DE

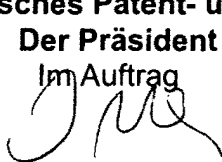
Bezeichnung: Speicherbaustein und Verfahren zum Betreiben eines Speicherbausteins

Priorität: 29. Juli 2005 DE 10 2005 035 780.6

IPC: G 11 C 7/10

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 26. Juli 2006
Deutsches Patent- und Markenamt
Der Präsident
Im Auftrag


Wallner

Beschreibung

Speicherbaustein und Verfahren zum Betreiben eines Speicherbausteins

5

Die Erfindung betrifft einen Speicherbaustein mit einem Anschluss zum Senden und/oder Empfangen von hochfrequenten Signalen. Die Erfindung betrifft weiterhin ein Verfahren zum Betreiben eines Speicherbausteins.

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In Speichersystemen werden üblicherweise eine Vielzahl von Speicherbausteinen eingesetzt, die über einen Speicherbus betrieben werden. Über den Speicherbus werden im allgemeinen Steuerbefehlssignale, Taktsignale, Datensignale und Adresssignale an die Speicherbausteine angelegt. Der Speicherbus umfasst Signalleitungen, die üblicherweise die Speicherbausteine miteinander und mit einem Speichercontroller verbinden. Bei einer Übertragung von hochfrequenten Signalen können jedoch an den Anschlüssen der Speicherbausteine Signalreflexionen auftreten, die die Datenübertragung auf dem Speicherbus stören und dadurch die Datenübertragungsraten begrenzen. Aus diesem Grund ist es notwendig, bei der Übertragung von Daten über den Speicherbus geeignete Terminierungen an den Anschlüssen der Speicherbausteinen vorzusehen, um die Signalreflexionen auf den Signalleitungen zu vermindern.

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Bei Speicherbausteinen ist bisher vorgesehen, abhängig von einem Terminierungssignal die Terminierung an einem Anschluss des Speicherbausteines ein- bzw. auszuschalten. D. h., der Speichercontroller stellt jedem der Speicherbausteine ein geeignetes Terminierungssignal zur Verfügung, um die nachfolgende Lese-, Schreib- oder sonstige Operation auf die Speicherbausteine mit einer optimalen Terminierung an allen an den Speicherbus angeschlossenen Speicherbausteinen zu unterstützen. Der Nachteil einer solchen Steuerung der Speicherbausteine besteht darin, dass ein Ein- und Ausschalten der Terminierungswiderstände in der Regel nicht ausreicht, um ei-

ne optimale Terminierung in jedem Betriebszustand zu erreichen und so die Datenübertragung über den Speicherbus zu verbessern.

- 5 Weiterhin kann vorgesehen sein, dass die Stärke der Terminierungswiderstände in den Speicherbausteinen gemäß einem Konfigurationswert festgelegt wird, der zu Beginn des Betriebes des Speichersystems in einer Initialisierungsphase den Speicherbausteinen durch den Speichercontroller mitgeteilt wird.
- 10 Eine Einstellung der Konfigurationswerte in den Speicherbausteinen vor jedem Schreib- und Lesevorgang ist zeitaufwändig. Daher ist auch die anfängliche Voreinstellung des Terminierungswiderstandes durch den Konfigurationswert nicht geeignet, für jeden Fall der Adressierung der Speicherbausteine
- 15 des Speichersystems geeignete Terminierungswiderstände zum Anlegen an den Speicherbus vorzusehen, da dadurch die Zugriffszeit in dem Speichersystem erheblich verlangsamt würde.
- 20 Es ist daher Aufgabe der vorliegenden Erfindung, einen Speicherbaustein zur Verfügung zu stellen, mit dem in einem Speichersystem eine verbesserte Terminierung des Speicherbusses zur Verfügung gestellt werden kann. Es ist weiterhin Aufgabe der vorliegenden Erfindung, ein Verfahren zum Betreiben des
- 25 Speicherbausteins zur Verfügung zu stellen, mit dem eine verbesserte Signalübertragung, insbesondere eine erhöhte Datenübertragungsrate in einem Speichersystem erreicht werden kann.
- 30 Diese Aufgabe wird durch den Speicherbaustein nach Anspruch 1, durch das Speichersystem nach Anspruch 11 sowie durch das Verfahren nach Anspruch 12 gelöst.

Weitere vorteilhafte Ausgestaltungen der Erfindung sind in

35 den abhängigen Ansprüchen angegeben.

Gemäß einem ersten Aspekt der vorliegenden Erfindung ist ein Speicherbaustein zur Einstellung verschiedener Terminierungen an einer Signalleitung des Datenbusses vorgesehen. Der Speicherbaustein umfasst einen Anschluss, eine mit dem Anschluss verbindbare Terminierungsschaltung, um den Anschluss mit einem einstellbaren Widerstandswert zu terminieren, einen Steueranschluss zum Empfangen eines Steuerbefehlssignals, und eine Steuerschaltung, die mit der Terminierungsschaltung verbunden ist, um abhängig von einem empfangenen Steuerbefehlssignal den Widerstandswert einzustellen und an dem Anschluss bereitzustellen.

Der erfindungsgemäße Speicherbaustein ermöglicht es, abhängig von einem an den Speicherbaustein angelegten Steuerbefehl einen Widerstandswert der Terminierungsschaltung einzustellen und den Anschluss in verbesserter Weise zu terminieren, so dass die Datenübertragung über den Speicherbus, der mit dem Speicherbaustein in einem Speichersystem verbindbar ist, in optimaler Weise unterstützt wird. Auf diese Weise kann der Terminierungswiderstand direkt abhängig von der Operation des Speichersystems eingestellt werden, ohne dass ein Konfigurationswert in dem Speicherbaustein unmittelbar vor dem Durchführen der Operation durch einen entsprechenden, von dem Speicherkontroller gesteuerten Einstellungsvorgang gespeichert werden muss. Zudem ist vorteilhaft, dass die Einstellung der jeweiligen Terminierung nicht von einem Speicherkontroller des Speichersystems gesteuert werden muss, sondern abhängig von der durch die Steuerbefehlssignale vorgegebenen Operation in dem Speichersystem vorgegeben wird.

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Vorzugsweise kann die Terminierungsschaltung eine Anzahl von Terminierungswiderständen aufweisen, um eine Anzahl von verschiedenen Widerstandswerten bereitzustellen, wobei die Steuerschaltung gestaltet ist, um mindestens einen der Terminierungswiderstände auszuwählen und an den Anschluss anzulegen. Durch das Vorsehen der Anzahl der Terminierungswiderstände in dem Speicherbaustein kann die Wahl des entsprechenden Termini-

nierungswiderstandes relativ schnell erfolgen, so dass kein oder kein wesentlicher Zeitverlust bei der Durchführung der Operation in dem Speichersystem auftritt.

- 5 Gemäß einer bevorzugten Ausführungsform der Erfindung ist eine Konfigurationseinheit vorgesehen, um die Widerstandswerte der Anzahl der Terminierungswiderstände einzustellen. Dadurch ist eine Vorauswahl der Widerstandswerte möglich, mit denen der Anschluss terminiert werden kann.

10

Gemäß einer bevorzugten Ausführungsform kann die Terminierungsschaltung einen einstellbaren Terminierungswiderstand umfassen, wobei eine Einstellungsschaltung vorgesehen ist, um abhängig von einem Auswahlsignal einen Einstellungswert bereitzustellen, mit dem der Widerstandswert des Terminierungswiderstandes bestimmt wird.

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Vorzugsweise weist der Speicherbaustein einen Terminierungsanschluss auf, um ein Terminierungssignal zu empfangen, wobei die Steuerschaltung mit der Terminierungsschaltung verbunden ist, um abhängig von dem Terminierungssignal entweder den Anschluss mit dem eingestellten Widerstandswert zu terminieren oder den Anschluss nicht zu terminieren. Auf diese Weise ist es möglich, an dem Anschluss wahlweise auch keine Terminierung vorzusehen, wenn dies durch den Speicherkontroller und/oder einem Steuerbefehl vorgegeben wird.

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Vorzugsweise kann die Steuerschaltung mit der Terminierungsschaltung verbunden sein, um abhängig von dem Terminierungssignal den Anschluss mit dem eingestellten Widerstand jeweils mit einer ersten Zeitverzögerung zu terminieren oder gemäß einer zweiten Zeitverzögerung nicht zu terminieren, wobei die erste Zeitverzögerung ausreicht, um den Widerstandswert einzustellen. Die erste und die zweite Zeitverzögerung kann gleich oder unterschiedlich sein.

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Vorzugsweise kann die Steuereinheit so gestaltet sein, dass der Widerstandswert abhängig von dem Anliegen eines Steuerbefehlssignals nach einer vorbestimmten ersten Umschaltzeit auf einen bestimmten zweiten Widerstandswert eingestellt wird
5 und/oder nach einer vorbestimmten zweiten Umschaltzeit auf einen bestimmten ersten Widerstandswert eingestellt wird.

10 Gemäß einer bevorzugten Ausführungsform der Erfindung stellt die Steuerschaltung die erste Umschaltzeit abhängig von der ersten Zeitverzögerung und/oder die zweite Umschaltzeit abhängig von der zweiten Zeitverzögerung ein.

15 Insbesondere kann die Steuereinheit so gestaltet sein, dass der Widerstandswert im Wesentlichen gleichzeitig mit dem Anliegen der Terminierung an den Anschluss auf den zweiten Widerstandswert eingestellt wird und/oder im Wesentlichen gleichzeitig mit dem Beenden des Terminierens des Anschlusses auf den ersten Widerstandswert eingestellt wird.

20 Gemäß einer bevorzugten Ausführungsform kann ein Befehlsdecoder vorgesehen sein, um abhängig von einem anliegenden Steuerbefehlssignal der Steuereinheit mitzuteilen, ob ein erster oder zweiter Widerstandswert zum Terminieren einzustellen ist.

25 Gemäß einem weiteren Aspekt der vorliegenden Erfindung ist ein Speichersystem mit einem Speicherkontroller, mit einer Anzahl von erfindungsgemäßen Speicherbausteinen und mit einem Speicherbus vorgesehen, mit dem der Speicherkontroller und
30 die Speicherbausteine verbunden sind, wobei der Speicherbus eine Signalleitung umfasst, die die Anschlüsse der Speicherbausteine und einen Anschluss des Speicherkontrollers miteinander verbindet.

35 Gemäß einem weiteren Aspekt der vorliegenden Erfindung ist ein Verfahren zum Betreiben eines Speicherbausteins vorgesehen, bei dem ein Steuerbefehlssignal empfangen wird, wobei

ein Anschluss mit einem einstellbaren Widerstandswert terminiert wird, wobei abhängig von dem empfangenen Steuerbefehlssignal der Widerstandswert eingestellt wird und der Anschluss mit dem eingestellten Widerstandswert terminiert wird. Auf diese Weise ist es möglich, den Terminierungswiderstand, der an einen Anschluss eines Speicherbausteins angelegt wird, abhängig von einem Steuerbefehl einzustellen, so dass es beim Betrieb des Speicherbausteins in einem Speichersystem möglich ist, für durchzuführende Operationen die geeignete Terminierung an jedem der Speicherbausteine einzustellen, um Signalreflexionen auf den Leitungen des Speicherbusses zu reduzieren und somit die mögliche Datenübertragungsrate zu erhöhen. Weiterhin ist vorteilhaft, dass die Einstellung des Widerstandswertes ohne das Bereitstellen weiterer von außen anzulegender Signale durchgeführt werden kann.

Vorzugsweise kann der Widerstandswert durch die Auswahl eines Einstellungswertes für einen einstellbaren Terminierungswiderstand eingestellt werden.

Vorzugsweise umfasst das Verfahren, dass der Widerstandswert über die Auswahl aus einer Anzahl von Terminierungswiderständen die an den Anschluss angelegt werden, eingestellt wird.

Gemäß einer bevorzugten Ausführungsform der Erfindung kann ein Terminierungssignal empfangen werden, wobei abhängig von dem Terminierungssignal entweder der Anschluss mit dem eingestellten Widerstandswert terminiert oder der Anschluss nicht terminiert wird.

Gemäß einer bevorzugten Ausführungsform der Erfindung kann abhängig von einem Pegelwechsel des Terminierungssignals entweder die Terminierung mit dem eingestellten Widerstandswert mit einer Zeitverzögerung eingeschaltet werden oder die Terminierung mit der Zeitverzögerung abgeschaltet werden, wobei die Zeitverzögerung so gewählt wird, dass der gewählte Terminierungswiderstand einstellbar ist.

Bevorzugte Ausführungsformen der Erfindung werden nachfolgend anhand der beigefügten Zeichnungen näher erläutert. Es zeigen:

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Figur 1 ein Blockschaltbild eines Speicherbausteins gemäß einer ersten Ausführungsform der Erfindung;

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Figur 2 ein Blockschaltbild eines Speicherbausteins gemäß einer weiteren Ausführungsform der Erfindung;

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Figur 3 ist ein Signal-Zeit-Diagramm, das die Funktionalität der Ausführungsformen der Figur 1 und Figur 2 bei Anliegen keiner den Speicherbaustein betreffenden Operation darstellt;

Figur 4 ein Signal-Zeit-Diagramm zur Darstellung der Funktionalität der Ausführungsformen der Figur 1 und 2, die das Durchführen einer Schreiboperation darstellt; und

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Figur 5 ein Signal-Zeit-Diagramm zur Darstellung der Funktionalität der Ausführungsformen der Figuren 1 und 2, die das Durchführen einer Schreiboperation bei aktiviertem Terminierungssignal darstellt.

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In Figur 1 ist ein Speicherbaustein 1 als Blockschaltbild dargestellt. Der Speicherbaustein 1 umfasst ein Speicherzellenfeld 2, wie z.B. ein DRAM-Speicherzellenfeld, das über einen Logikschaltkreis 3 beschrieben und ausgelesen werden kann. Der Logikschaltkreis 3 umfasst Ansteuerschaltkreise, wie auch Eingangsverstärker und Ausgangstreiber (nicht gezeigt). Die Logikschaltung 3 ist mit einem externen Anschluss 4 des Speicherbausteins 1 verbunden, über den z.B. Adress-, Takt- und Benutzerdaten eingelesen bzw. hinaus getrieben werden können.

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Der externe Anschluss 4 ist mit einer Terminierungsschaltung 5 verbunden, die einen ersten einstellbaren Terminierungswi-

derstand 6 mit einem ersten Widerstandswert und einen zweiten einstellbaren Terminierungswiderstand 7 mit einem zweiten Widerstandswert aufweist. Die Terminierungsschaltung 5 ist mit einer Steuereinheit 8 verbunden, die der Terminierungsschaltung 5 ein erstes Steuersignal TermTime0 und ein zweites Steuersignal TermTime1 zur Verfügung stellt. Bei einer Aktivierung des ersten Steuersignal TermTime0 wird der erste Terminierungswiderstand 6 an den externen Anschluss 4 angelegt, so dass der externe Anschluss 4 mit dem entsprechend in dem ersten Terminierungswiderstand 6 eingestellten ersten Widerstandswert terminiert wird. Bei Aktivierung des zweiten Steuersignals TermTime1 wird entsprechend der zweite Terminierungswiderstand 7 an dem ersten Anschluss angelegt, so dass der externe Anschluss 4 mit dem zweiten Widerstandswert terminiert wird. Weiterhin kann bei gleichzeitiger Aktivierung beider Steuersignale TermTime0, TermTime1 auch ein sich aus der Parallelschaltung des ersten und zweiten Widerstandswertes ergebender weiterer Widerstandswert zur Terminierung erzeugt werden.

Es ist weiterhin eine Konfigurationseinheit 9 vorgesehen, die einen ersten Konfigurationswert TS0 und einen zweiten Konfigurationswert TS1 bereitstellt. Der erste Konfigurationswert TS0 wird an den ersten Terminierungswiderstand 6 und der zweite Konfigurationswert an den zweiten Terminierungswiderstand 7 angelegt, um dort den jeweiligen Widerstandswert des entsprechenden Terminierungswiderstandes 6, 7 einzustellen. Die Konfigurationswerte TS0, TS1 können parallel über Konfigurationssignale bereitgestellt werden. Abhängig von dem jeweiligen Steuersignal TermTime0, TermTime1 wird dann der entsprechende Terminierungswiderstand 6, 7, dessen Widerstandswert durch den jeweiligen Konfigurationswert TS0, TS1 vorgesehen ist, an den externen Anschluss 4 angelegt.

Ein einstellbarer Terminierungswiderstand kann beispielsweise durch schaltbare, parallel geschaltete Widerstände erreicht werden, wobei die Widerstände auch durch ganz oder teilweise

- durchgeschaltete Transistoren mit gleicher oder verschiedener Kanalbreite realisierbar sind. Die Terminierungswiderstände können so gestaltet sein, dass das jeweilige Steuersignal TermTime0, TermTime1 mit jedem der Bits des bereitgestellten Konfigurationswertes TS0, TS1 mit einer UND-Verknüpfung logisch verknüpft werden und die jeweiligen Verknüpfungsergebnisse an die Eingänge von in dem Terminierungswiderstand vorgesehenen Transistoren angelegt werden.
- 10 Die Steuereinheit 8 erhält über einen externen Terminierungsanschluss 13 ein Terminierungssignal TermEn, das angibt, ob eine Terminierung an dem externen Anschluss 4 vorgesehen sein soll oder nicht. D.h., durch das erste und das zweite Steuersignal TermTime0, TermTime1 wird der jeweilige Terminierungswiderstand 6, 7 nur dann an den externen Anschluss 4 angelegt, wenn das Terminierungssignal TermEn angibt, dass eine Terminierung erfolgen soll. Andernfalls wird keine Terminierung des externen Anschlusses 4 vorgenommen.
- 20 Welcher der zwei Terminierungswiderstände 6, 7 an den externen Anschluss 4 angelegt wird, wird abhängig von einem Befehlssignal BS angegeben, das von einem Befehlsdecodierer 10, abhängig von einem empfangenen Steuerbefehl CMD, bereitgestellt wird. Der Befehlsdecodierer 10 empfängt über einen oder mehreren externe Anschlüsse 11 Steuerbefehlssignale CMD zur Aktivierung, Adressierung und/oder Ansteuerung des Speicherbausteins 1.
- 30 Die Steuerbefehlssignale CMD können einen aktiven oder inaktiven Zustand einnehmen. Handelt es sich bei dem Speicherbaustein 1 um einen DRAM-Speicherbaustein, so können die Steuerbefehlssignale beispielsweise das Chip-Select-Signal CS zum Auswählen des betreffenden Speicherbausteins für eine bestimmte Operation, das Schreib-Enable-Signal WE zum Anzeigen eines Write-Zugriffs auf den Speicherbaustein, das RAS-Signal (Zeilenaktivierungssignal) zum Übermitteln der Wortleitungsadresse und zum Aktivieren der Wortleitung sowie das CAS-
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Signal (Spaltenaktivierungssignal) zum Übertragen der Bitleitungsadresse und zum Aktivieren der Bitleitung zum Auslesen bzw. Hineinschreiben von Daten in das Speicherzellenfeld sein. Je nach dem, ob der betreffende Speicherbaustein in einem Speichersystem für eine Operation ausgewählt ist oder nicht (Chip-Select-Signal) bzw. ob ein Schreiben oder Lesen auf den betreffenden Speicherbaustein durchgeführt werden soll (Write-Enable-Signal) kann nun einer der beiden Terminierungswiderstände 6, 7 bzw. keiner der beiden Terminierungswiderstände (gesteuert durch das Terminierungssignal) ausgewählt werden, um den externen Anschluss 4 in geeigneter Weise zu terminieren.

In Figur 2 ist eine weitere Ausführungsform der Erfindung dargestellt. Darin sind Elemente gleicher oder vergleichbarer Funktion mit den gleichen Bezugszeichen versehen. Die Ausführungsform der Figur 2 unterscheidet sich von der Ausführungsform der Figur 1 dadurch, dass eine Einstellungseinheit 15 vorgesehen ist, die die Konfigurationseinheit 9 und einen Multiplexer 12 aufweist. An einem Steuereingang des Multiplexers 12 ist ein von der Steuereinheit 8 bereitgestelltes Terminierungsauswahlsignal TermSel angelegt. Mit Hilfe des Terminierungsauswahlsignals TermSel wird ausgewählt, welcher der durch die Konfigurationseinheit 9 bereitgestellte Konfigurationswert TS0, TS1 an die Terminierungsschaltung 5 angelegt wird. Die Terminierungsschaltung 5 umfasst in dieser Ausführungsform nur einen einstellbaren Terminierungswiderstand 6, dessen Widerstandswert abhängig von dem ausgewählten Konfigurationswert TS0, TS1 eingestellt wird. Abhängig von dem einzigen Steuersignal TermTime0, das durch die Steuereinheit 8 bereitgestellt wird, wird nun der einzige Terminierungswiderstand 6 aktiviert oder deaktiviert und somit an den externen Anschluss 4 angelegt oder nicht.

Die Größe des Widerstandswertes des Terminierungswiderstandes 6 bestimmt sich durch das Terminierungsauswahlsignal TermSel, mit dem einer der Konfigurationswerte TS0, TS1 ausgewählt

wird. Bei dieser Ausführungsform ist es möglich, im Gegensatz zur Ausführungsform der Figur 1, auf einen zweiten einstellbaren Terminierungswiderstand zu verzichten und statt dessen den einzigen einstellbaren Terminierungswiderstand gemäß einem über den Multiplexer 12 auswählbaren Konfigurationswert abhängig den von aktuellen Steuerbefehlssignalen auszuwählen. Eine Kombination von verschiedenen Terminierungswiderständen, die gleichzeitig an den externen Anschluss 4 angelegt werden, wie in Figur 1 gezeigt, ist damit nicht möglich, jedoch kann Chipfläche eingespart werden, da nur ein einstellbarer Terminierungswiderstand 6 benötigt wird.

In Figur 3 ist ein Signal-Zeit-Diagramm zur Verdeutlichung des Signalverlaufs für die Einstellung der Terminierung in einem erfindungsgemäßen Speicherbaustein gezeigt. In dem Signal-Zeit-Diagramm der Figur 3 ist ein Fall angegeben, bei dem eine Terminierung eingeschaltet werden soll, wenn das Befehlssteuersignal angibt, dass der betreffende Speicherbaustein nicht aktiviert ist, d.h. kein Zugriff auf den Speicherbaustein durchgeführt werden soll (Chip-Select-Signal deaktiviert). Ausgelöst durch das Aktivieren des Terminierungssignals TermEn durch den Speicherkontroller und durch eine steigende Flanke eines Taktsignals CK zu einem Zeitpunkt T0 wird nach einer vorbestimmten Terminierungseinschaltzeit ODTLon von in diesem Beispiel drei Taktperioden ein gewünschter erster Widerstandswert RTT_Nom (DRAM_RTT) an den externen Anschluss 4 angelegt. Nach Deaktivieren des Terminierungssignals TermEn während der fünften Taktperiode T5 beginnt mit der nächsten steigenden Flanke des Taktsignals T6 eine vorbestimmte Terminierungsausschaltzeit ODTLoff, die in diesem Ausführungsbeispiel dreieinhalb Taktperioden beträgt und nach deren Ablauf der Terminierungswiderstand von dem externen Anschluss 4 getrennt wird. Die Zeitdauern der Terminierungseinschaltzeit ODTLon und der Terminierungsausschaltzeit ODTLoff sind im Wesentlichen beliebig wählbar und sollten so gewählt sein, dass sie ausreichen, den Terminierungswiderstand zuverlässig mit dem externen Anschluss 4 zu verbinden oder von

diesem zu trennen. D.h., sie sollten mindestens die Zeitdauer betragen, die zum Ein- bzw. Ausschalten eines Terminierungswiderstandes bzw. dem Anlegen und dem Trennen des Terminierungswiderstandes von dem externen Anschluss 4 benötigt wird.

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Z. B. bei deaktiviertem Chip-Select-Signal, d.h., wenn keine Operation in dem Speicherbaustein durchgeführt werden soll, kann daher die Terminierung des externen Anschlusses 4 vorgenommen werden oder nicht, was in einem Speichersystem durch den Speichercontroller mit Hilfe des Terminierungssignals TermEn gesteuert wird. Gleichzeitig wird Speicherbaustein intern festgestellt, dass das Chip-Select-Signal CS deaktiviert ist und abhängig von dem Chip-Select-Signal CS ein entsprechender Konfigurationswert bzw. Steuersignal (je nach Ausführungsform) an die Terminierungsschaltung 5 angelegt wird, um den dort aktiven Terminierungswiderstand 6, 7 bzw. 6 abhängig von dem Terminierungssignal TermEn an den externen Anschluss 4 anzulegen.

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In Figur 4 ist ein weiteres Signal-Zeit-Diagramm für die Ausführungsform der Figur 1 und 2 dargestellt. Das Signal-Zeit-Diagramm der Figur 4 zeigt einen Fall an, bei dem der entsprechende Speicherbaustein durch das Chip-Select-Signal CS aktiviert ist und ein Schreibbefehl (WE-Signal) WRS8 an den Speicherbaustein durch den Speichercontroller gesendet werden. Der Speichercontroller legt vorzugsweise das Terminierungssignal TermEn und das Schreibsignal WRS8 so an, dass es zu einem Zeitpunkt T12 durch eine steigende Taktflanke in den Speicherbaustein übernommen werden kann. Der Befehlsdecoder decodiert das Schreibsignal WRS8 und generiert das Befehlssignal BS, das an die Steuereinheit 8 angelegt wird. In der Steuereinheit 8 wird abhängig von dem Befehlssignal BS festgestellt, dass nun ein Terminierungswiderstand an den externen Anschluss 4 angelegt werden soll, der durch den zweiten Konfigurationswert bestimmt ist. Die Steuereinheit 8 aktiviert daher bei der Ausführungsform der Figur 1 das zweite Steuersignal TermTimel, um den zweiten Terminierungswider-

stand 7 zu aktivieren. Bei der Ausführungsform der Figur 2 schaltet die Steuereinheit 8 das Terminierungsauswahlsignal TermSel so, dass der Multiplexer 12 den zweiten Konfigurationswert an die Terminierungsschaltung 5 anlegt, um dort den Widerstandswert des Terminierungswiderstandes 6 auf den entsprechenden Wert, in diesem Fall auf einen zweiten Widerstandswert RTT_WR einzustellen, der dem Terminierungswiderstand entspricht, der an die aktivierten Speicherbausteine bei einem Schreibzugriff an den externen Anschluss 4 angelegt werden soll.

Abhängig von dem Terminierungssignal TermEn wird nun nach der Terminierungseinschaltzeit ODTLon der Terminierungswiderstand an den externen Anschluss 4 angelegt, wobei nun der Terminierungswiderstand abhängig von dem Steuerbefehlssignal ein anderer ist, wie zuvor beim deaktivierten Speicherbaustein (Fig. 3). Gleichzeitig beginnt mit dem Empfang des Schreibbefehls WRS8 die Schreiblatenzzeitdauer WL zu laufen, die in den gezeigten Ausführungsbeispielen 5 Taktperioden beträgt. In einer Taktperiode vor dem Übertragen eines Datenburst, d.h. Übertragen von 8 Datenbits, kann das Daten-Strobe-Signal DQS synchron zu den Daten in den Speicherbaustein eingelesen werden. Die Terminierungseinschaltzeit ODTLon ist vorzugsweise gleich oder kleiner der Schreiblatenzzeitdauer WL gewählt, so dass sichergestellt wird, dass beim Übertragen der Daten zu dem Speicherbaustein (beim Schreibzugriff) der gewünschte Terminierungswiderstand an dem externen Anschluss 4 angelegt ist.

Im Allgemeinen wird das Befehlssignal BS in dem Befehlsdecodierer 10 so erzeugt, dass es der Steuereinheit 8 angibt, welcher Widerstandswert als Terminierungswiderstand RTT_Nom oder RTT_WR für den Anschluss eingestellt werden soll. Bei einer ersten Gruppe von anliegenden Steuerbefehlen CMD gibt der Befehlsdecodierer 10 ein Befehlssignal BS an die Steuereinheit 8 aus, das angibt, dass eine Terminierung mit dem ersten Widerstandswert RTT_Nom vorgenommen werden soll (bei

aktiviertem Terminierungssignal TermEn) und bei einer zweiten Gruppe von Steuerbefehlen gibt der Befehlsdecodierer 10 ein Befehlssignal BS an die Steuereinheit 8 aus, das angibt, dass der Anschluss 4 mit einem zweiten Widerstandswert terminiert werden soll (bei aktiviertem Terminierungssignal TermEn). Die erste Gruppe von Steuerbefehlen kann Steuerbefehle umfassen, die beispielsweise eine Deaktivierung der integrierten Schaltung bzw. einen Lesezugriff auf die integrierte Speicherschaltung anzeigen, während die zweite Gruppe von Steuerbefehlen Schreibbefehle auf die integrierte Speicherschaltung anzeigen kann.

Die Zeitdauer zwischen dem Anlegen eines Steuerbefehlssignals bzw. zwischen dem Bereitstellen des Befehlssignals BS an die Steuereinheit 8 und davon abhängigen Änderungen des Widerstandswertes in der Terminierungsschaltung 5 ist vorzugsweise als erste Umschaltzeit ODTLCNW festgelegt, die vorzugsweise gleich oder kleiner der Terminierungseinschaltzeit ODTLon ist.

Allgemein erfolgt vorzugsweise das Einschalten der Terminierung und das entsprechende Einstellen des Terminierungswiderstands auf den entsprechenden Widerstandswert durch die Steuereinheit 8 im Wesentlichen gleichzeitig. Weiterhin kann das Ausschalten der Terminierung und das Ändern des Widerstandswerts ebenfalls gleichzeitig erfolgen.

Weiterhin kann für einen Fall eines anliegenden Steuerbefehles der zweiten Gruppe von Steuerbefehlen beispielsweise vorgesehen sein, dass die Steuereinheit 8 nach Ablauf einer zweiten Umschaltzeit ODTLCWN die Terminierung von den zweiten Widerstandswert auf den ersten Widerstandswert ändert, unabhängig davon, ob das Terminierungssignal TermEn eine Terminierung vorsieht oder nicht. Die zweite Umschaltzeit ODTLCWN entspricht mindestens einer Zeitdauer, die durch das Beenden des Schreibzugriffs bzw. durch das Beenden eines Zugriffs auf den Speicherbaustein, der durch einen Steuerbefehl der zwei-

ten Gruppe von Steuerbefehlen ausgelöst ist, bestimmt ist. Im Falle eines Burst-Schreibzugriffes, wie in Verbindung mit Figur 4 beschrieben wurde, sollte die zweite Umschaltzeit abhängig von der Schreiblatenzzeit WL und abhängig von der Zeitdauer für den Burstzugriff sein. Alternativ kann die zweite Umschaltzeit auch abhängig von dem Ende eines Datentransfers von und zu dem Speicherbaustein 1 eingestellt werden. Die zweite Umschaltzeit ODTLCBM ist vorzugsweise die Summe der Schreiblatenz WL und der Dauer des Burstzugriffs (Burstlänge / 2 * Taktzykluslänge TCK) zuzüglich einer Sicherheitszeitdauer ($1/2 * TCK$ oder das Vielfache davon). Auf diese Weise ist es möglich, dass der zweite Widerstandswert RTT_WR zum Terminieren des Anschlusses abhängig von einem anliegenden Steuerbefehl CMD nur für eine bestimmte Zeitdauer zur Terminierung des Anschlusses bereitgestellt wird, wobei der Anschluss nach Ablauf dieser Zeitdauer wieder mit dem ersten Widerstandswert terminiert wird, sofern dieses durch das Terminierungssignal TermEn angegeben ist.

Zu Figur 5 ist ein Fall gezeigt, bei dem das Terminierungssignal TermEn die Terminierung des Anschlusses 4 vor während und nach einem Schreibzugriff WRS4 eingeschaltet lässt, wobei die Terminierung vor dem Schreibzugriff auf den ersten Widerstandswert RTT_Nom eingestellt ist. Nach Ablauf der ersten Umschaltzeit ODTLCNW wird der Anschluss 4 mit dem Widerstandswert RTT_WR terminiert und nach Ablauf der zweiten Umschaltzeit ODTLCWN die Terminierung wieder auf den ersten Widerstandswert RTT_Nom zurückgeschaltet.

Auch wenn in dem gezeigten Ausführungsbeispiel nur zwei verschiedene Terminierungswiderstände an den externen Anschluss 4 angelegt werden können, kann die Anzahl von verschiedenen einstellbaren Terminierungswiderständen jedoch beliebig hoch sein, so dass für verschieden Zugriffe in einem Speichersystem, in dem der Speicherbaustein betrieben wird, verschiedenen Terminierungswiderstände an die externen Anschlüsse angelegt werden können.

Eine Idee der Erfindung besteht darin, während des Betriebs die Speicherbausteine in einem Speichersystem die Terminierungswiderstände abhängig von der aktuell durchgeführten Operation für jeden der Speicherbausteine gezielt einstellen zu können. So können in erster Linie verschiedene Terminierungswiderstände vorgesehen sein, die wahlweise oder auch in Kombination an den externen Anschluss angelegt werden können. Zusätzlich kann es möglich sei, dass Anlegen eines Terminierungswiderstandes an den externen Anschluss abhängig von einem Terminierungssignal TermEn durchzuführen.

Ansprüche

1. Speicherbaustein (1) zur Einstellung verschiedener Terminierungen

5 mit einem Anschluss (4)

mit einer mit dem Anschluss (4) verbindbaren Terminierungsschaltung (5), um den Anschluss (4) mit einen einstellbaren Widerstandswert zu terminieren,

10 mit einem Ansteueranschluss zum Empfangen eines Steuerbefehlssignals;

mit einer Steuerschaltung, die mit der Terminierungsschaltung verbunden ist, um abhängig von einem empfangenen Steuerbefehlssignal den Widerstandswert einzustellen und den Anschluss mit diesem zu terminieren.

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2. Speicherbaustein (1) nach Anspruch 1, wobei die Terminierungsschaltung eine Anzahl von Terminierungswiderständen (6, 7) aufweist, um eine Anzahl von Widerstandswerten bereitzustellen, wobei die Steuerschaltung (8)

20 gestaltet ist, um mindestens einen der Terminierungswiderstände (6, 7) auszuwählen und an den Anschluss(4) anzulegen.

3. Speicherbaustein (1) nach Anspruch 2,

25 mit einer Konfigurationseinheit (9), um die Widerstandswerte der Anzahl der Terminierungswiderstände einzustellen.

4. Speicherbaustein (1) nach Anspruch 1, wobei die Terminierungsschaltung einen einstellbaren Terminierungswiderstand (6) umfasst, wobei eine Einstellungsschaltung

30 (15) vorgesehen ist, um abhängig von einem Auswahlsignal (TermSel) einen Einstellungswert bereitzustellen, mit

dem der Widerstandswert des Terminierungswiderstandes (6) bestimmt wird.

5. Speicherbaustein (1) nach einem der Ansprüche 1 bis 4, mit einem Terminierungsanschluss (13), um ein Terminierungssignal zu empfangen, wobei die Steuerschaltung (8) mit der Terminierungsschaltung verbunden ist, um abhängig von dem Terminierungssignal (TermEn) entweder den Anschluss (4) mit dem eingestellten Widerstandswert zu terminieren oder den Anschluss (4) nicht zu terminieren.
6. Speicherbaustein (1) nach einem der Ansprüche 1 bis 5, wobei die Steuerschaltung (8) mit der Terminierungsschaltung (5) verbunden ist, um den Anschluss (4) abhängig von dem Terminierungssignal entweder mit dem eingestellten Widerstandswert mit einer ersten Zeitverzögerung zu terminieren oder gemäß einer zweiten Zeitverzögerung nicht zu terminieren, wobei die Zeitverzögerung zum Terminieren ausreicht, um den Widerstandswert einzustellen.
7. Speicherbaustein nach einem der Ansprüche 1 bis 6, wobei die Steuerschaltung (8) so gewählt ist, dass der Widerstandswert abhängig von dem Anliegen eines Steuerbefehlssignals nach einer vorbestimmten ersten Umschaltzeit auf einen bestimmten zweiten Widerstandswert eingestellt wird und/oder nach einer vorbestimmten zweiten Umschaltzeit auf einen bestimmten ersten Widerstandswert eingestellt wird.
8. Speicherbaustein nach Anspruch 7, wobei die Steuerschaltung (8) die erste Umschaltzeit abhängig von der ersten

Zeitverzögerung und/oder die zweite Umschaltzeit abhängig von der zweiten Zeitverzögerung einstellt.

- 5 9. Speicherbaustein nach Anspruch 8, wobei die Steuerschaltung (8) so gestaltet ist, dass der Widerstandswert abhängig von dem Steuerbefehlssignal im Wesentlichen gleichzeitig mit dem Einschalten der Terminierung des Anschlusses (4) auf den zweiten Widerstandswert eingestellt wird und/oder im Wesentlichen gleichzeitig mit dem Beenden des Terminierens des Anschlusses (4) auf den ersten Widerstandswert eingestellt wird.
- 10 10. Speicherbaustein nach einem der Ansprüche 1 bis 9, wobei ein Befehlsdecodierer vorgesehen ist, um abhängig von einem anliegenden Steuerbefehlssignal der Steuerschaltung (8) mitzuteilen, ob ein erster oder ein zweiter Widerstandswert zum Terminieren einzustellen ist.
- 15 11. Speichersystem mit einem Speicherkontroller mit einer Anzahl von Speicherbausteinen (1) nach einem der Ansprüche 1 bis 10, mit einem Speicherbus, um den Speicherkontroller und die Speicherbausteine (1) zu verbinden, wobei der Speicherbus eine Signalleitung umfasst, die die Anschlüsse (4) der Speicherbausteine (1) und einen Anschluss des Speicherkontrollers miteinander verbindet.
- 20 25 12. Verfahren zum Betreiben eines Speicherbausteins (1), wobei ein Steuerbefehlssignal empfangen wird; wobei ein Anschluss (4) mit einem einstellbaren Widerstandswert terminiert wird, wobei abhängig von dem empfangenen Steuerbefehlssignal der Widerstandswert eingestellt und der Anschluss mit dem Widerstandswert terminiert wird.
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13. Verfahren nach Anspruch 12, wobei der Widerstandswert durch die Auswahl eines Einstellungswertes für einen einstellbaren Terminierungswiderstand eingestellt wird.

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14. Verfahren nach Anspruch 12, wobei der Widerstandswert über die Auswahl aus einer Anzahl von Terminierungswiderständen (6, 7), die an den Anschluss (4) angelegt werden, eingestellt wird.

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15. Verfahren nach einem der Ansprüche 12 bis 14, wobei ein Terminierungssignal (TermEn) empfangen wird, wobei abhängig von dem Terminierungssignal entweder der Anschluss (4) mit dem eingestellten Widerstandswert terminiert wird oder der Anschluss (4) nicht terminiert wird.

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16. Verfahren nach Anspruch 15, wobei abhängig von dem Terminierungssignal (TermEn) entweder die Terminierung mit dem eingestellten Widerstandswert mit einer ersten Zeitverzögerung eingeschaltet wird oder die Terminierung mit einer zweiten Zeitverzögerung abgeschaltet wird, wobei die erste Zeitverzögerung so gewählt wird, dass der ausgewählte Terminierungswiderstand einstellbar ist.

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17. Verfahren nach Anspruch 16, wobei der Widerstandswert abhängig von dem Anliegen eines Steuerbefehlssignals nach einer vorbestimmten ersten Umschaltzeit auf einen bestimmten zweiten Widerstandswert eingestellt wird und/oder nach einer vorbestimmten zweiten Umschaltzeit auf einen bestimmten ersten Widerstandswert eingestellt wird.

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18. Verfahren nach Anspruch 16 und 17, wobei die erste Umschaltzeit abhängig von der ersten Zeitverzögerung und/oder die zweite Umschaltzeit abhängig von der zweiten Zeitverzögerung eingestellt werden.

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19. Verfahren nach Anspruch 17 oder 18, wobei die Einstellung des Widerstandswerts auf den zweiten Widerstandswert abhängig von dem Steuerbefehlssignal im Wesentlichen gleichzeitig mit der Terminierung des Anschlusses (4) durchgeführt wird und/oder die Einstellung des Widerstandswerts auf den ersten Widerstandswert im Wesentlichen gleichzeitig mit dem Beenden des Terminierens des Anschlusses (4) durchgeführt wird.

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- 15 20. Verfahren nach einem der Ansprüche 17 bis 19, wobei das Terminierungssignal (TermEn) und das Steuerbefehlssignal zu Zeitpunkten an dem Speicherbaustein angelegt werden, so dass die Terminierung des Anschlusses gleichzeitig mit dem Ändern des Widerstandswerts erfolgt.

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Zusammenfassung

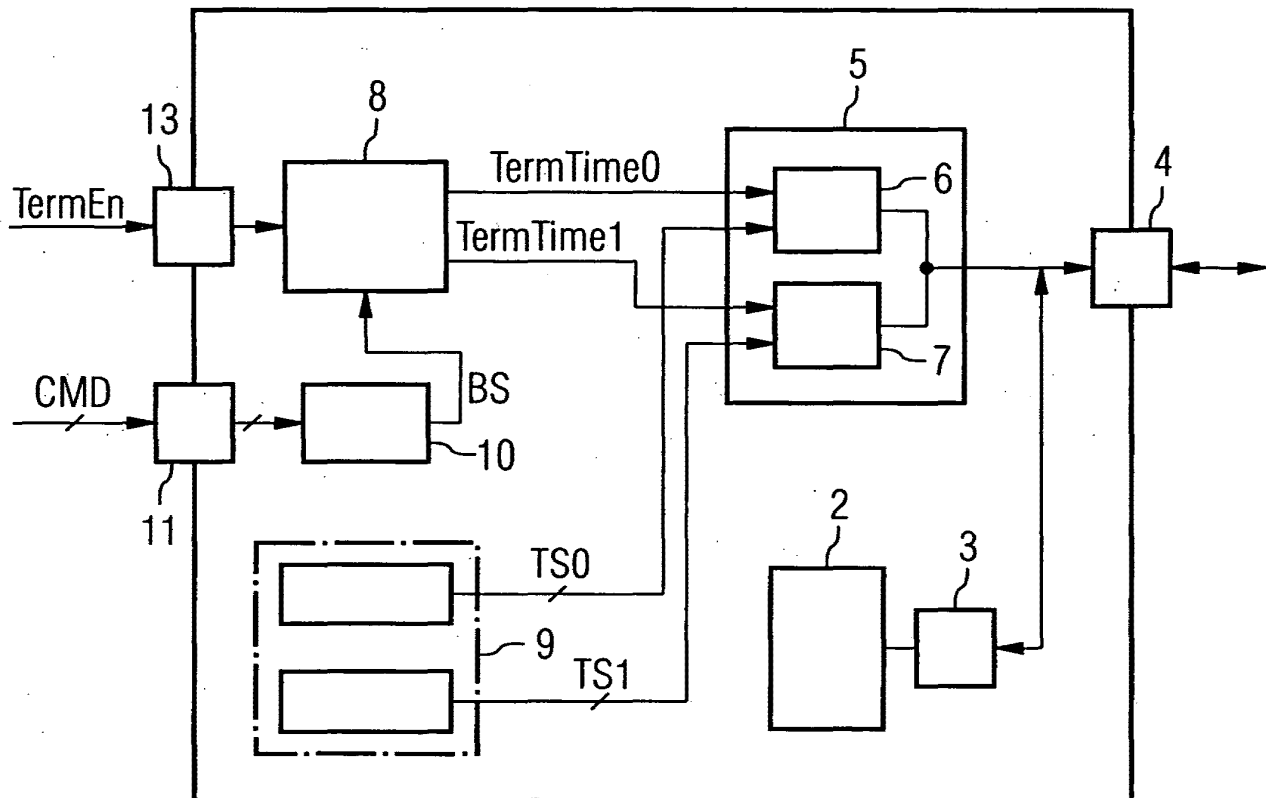
Speicherbaustein und Verfahren zum Betreiben eines Speicherbausteins

- 5 Die Erfindung betrifft einen Speicherbaustein (1) zur Einstellung verschiedener Terminierungen mit einem Anschluss (4), mit einer mit dem Anschluss (4) verbindbaren Terminierungsschaltung (6), um den Anschluss mit einen einstellbaren
- 10 Widerstandswert zu terminieren, mit einem Ansteueranschluss (11) zum Empfangen eines Steuerbefehlssignals, und mit einer Steuerschaltung (8), die mit der Terminierungsschaltung (5) verbunden ist, um abhängig von einem empfangenen Steuerbefehlssignal einen Widerstandswert einzustellen und den An-
- 15 schluss (4) mit diesem zu terminieren.

Figur 1

Figur für die Zusammenfassung

FIG 1



Bezugszeichenliste

	1	Speicherbaustein
	2	Speicherzellenfeld
5	3	Logikschaltkreise
	4	externer Anschluss
	5	Terminierungsschaltung
	6	erster Terminierungswiderstand
	7	zweiter Terminierungswiderstand
10	8	Steuereinheit
	9	Konfigurationseinheit
	10	Befehlsdecodierer
	11	Steuerbefehlsanschluss
	12	Multiplexer
15	13	Terminierungsanschluss
	15	Einstellungsschaltung

FIG 1

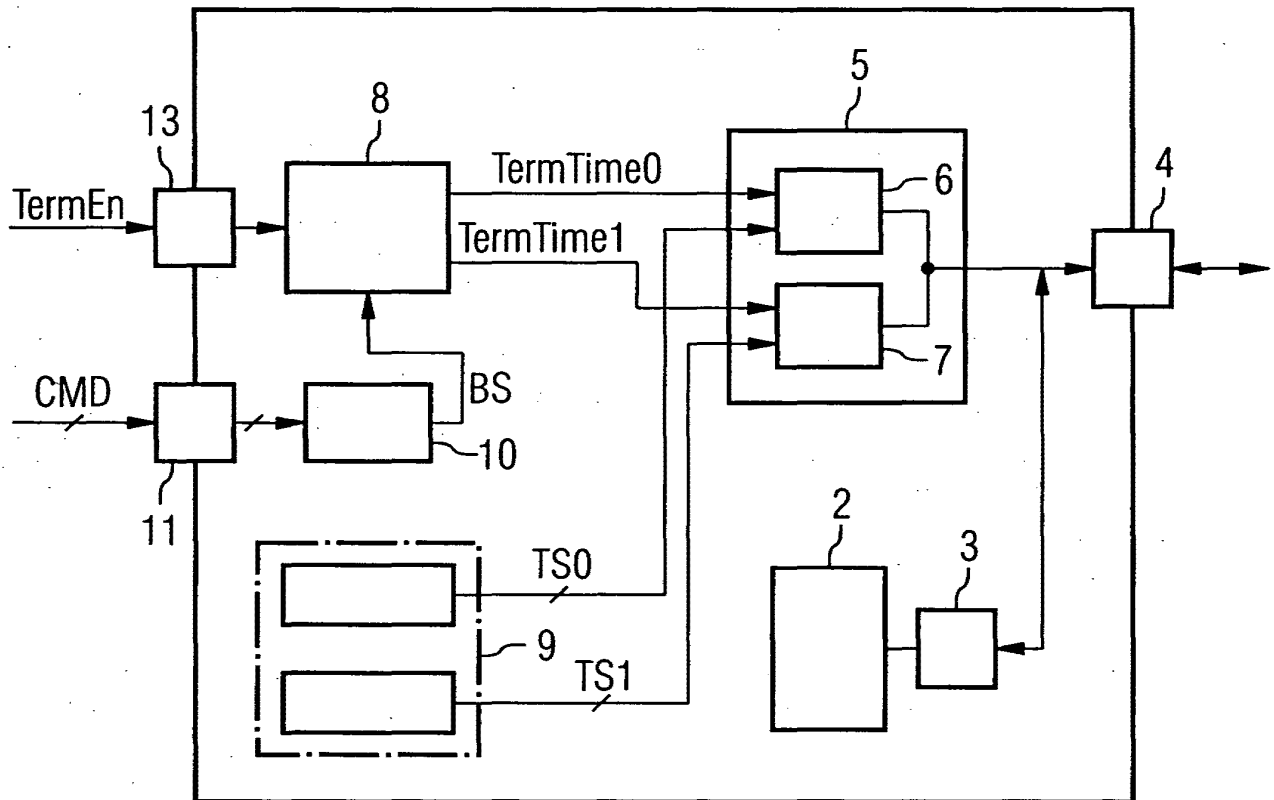


FIG 2

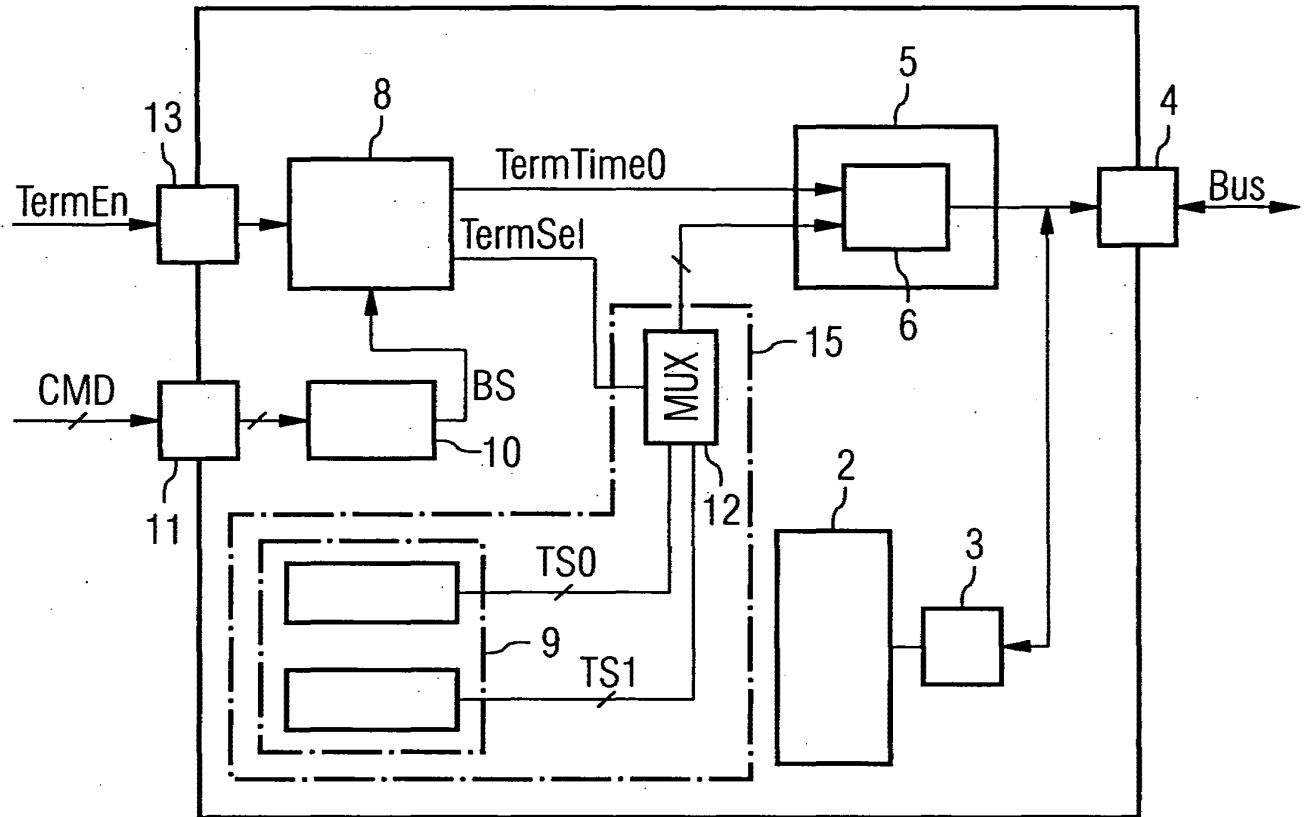


FIG 3

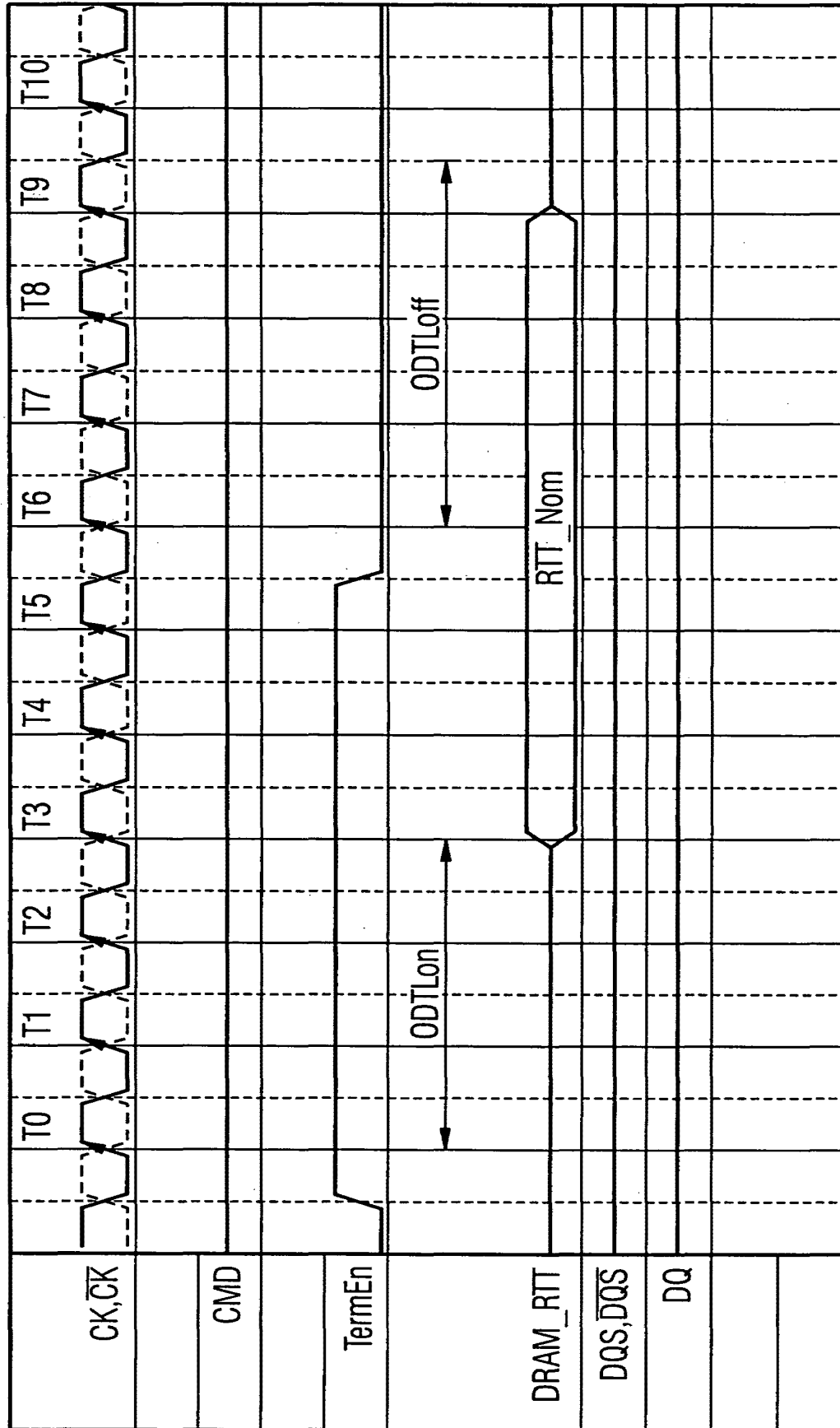


FIG 4

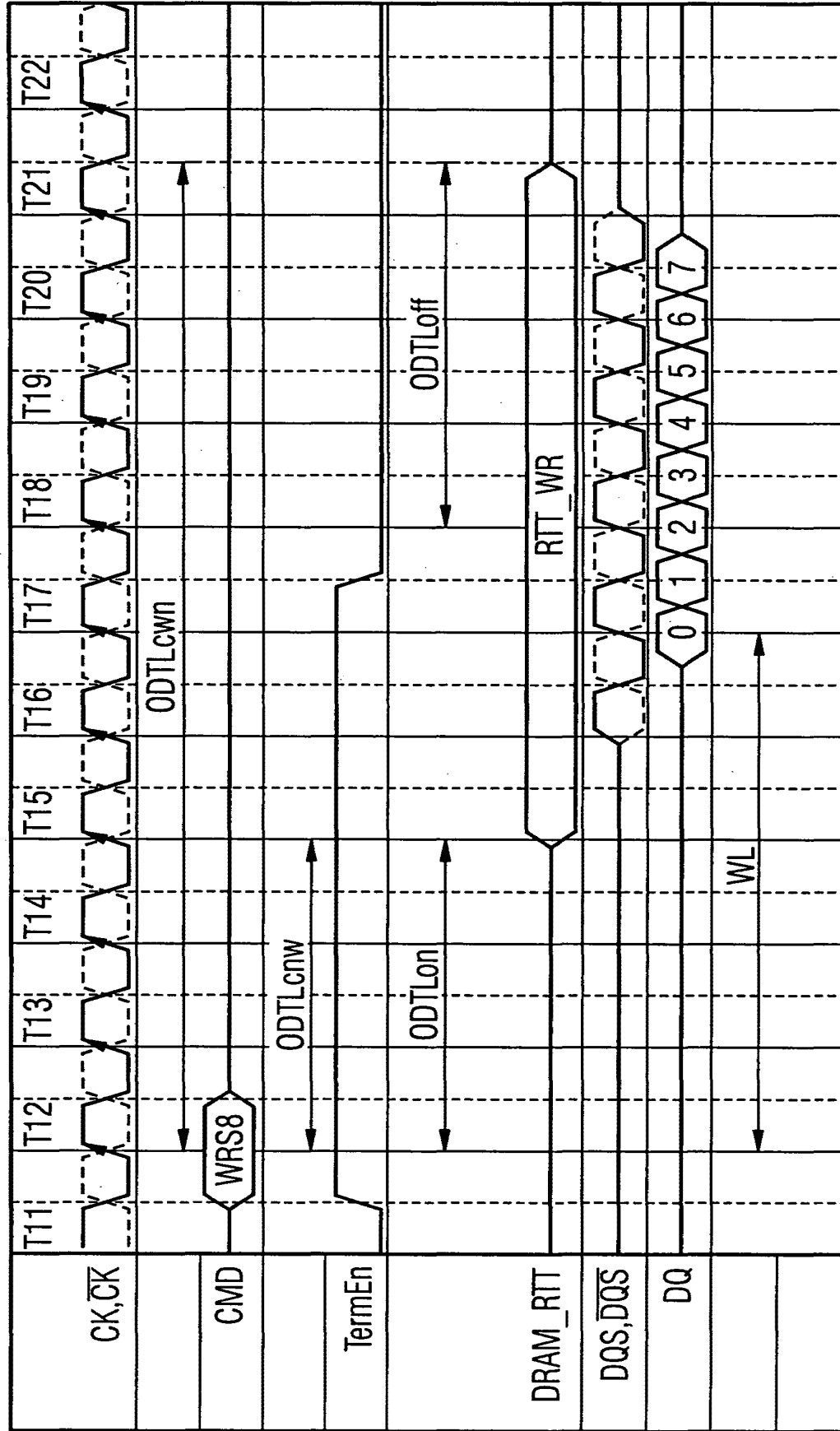
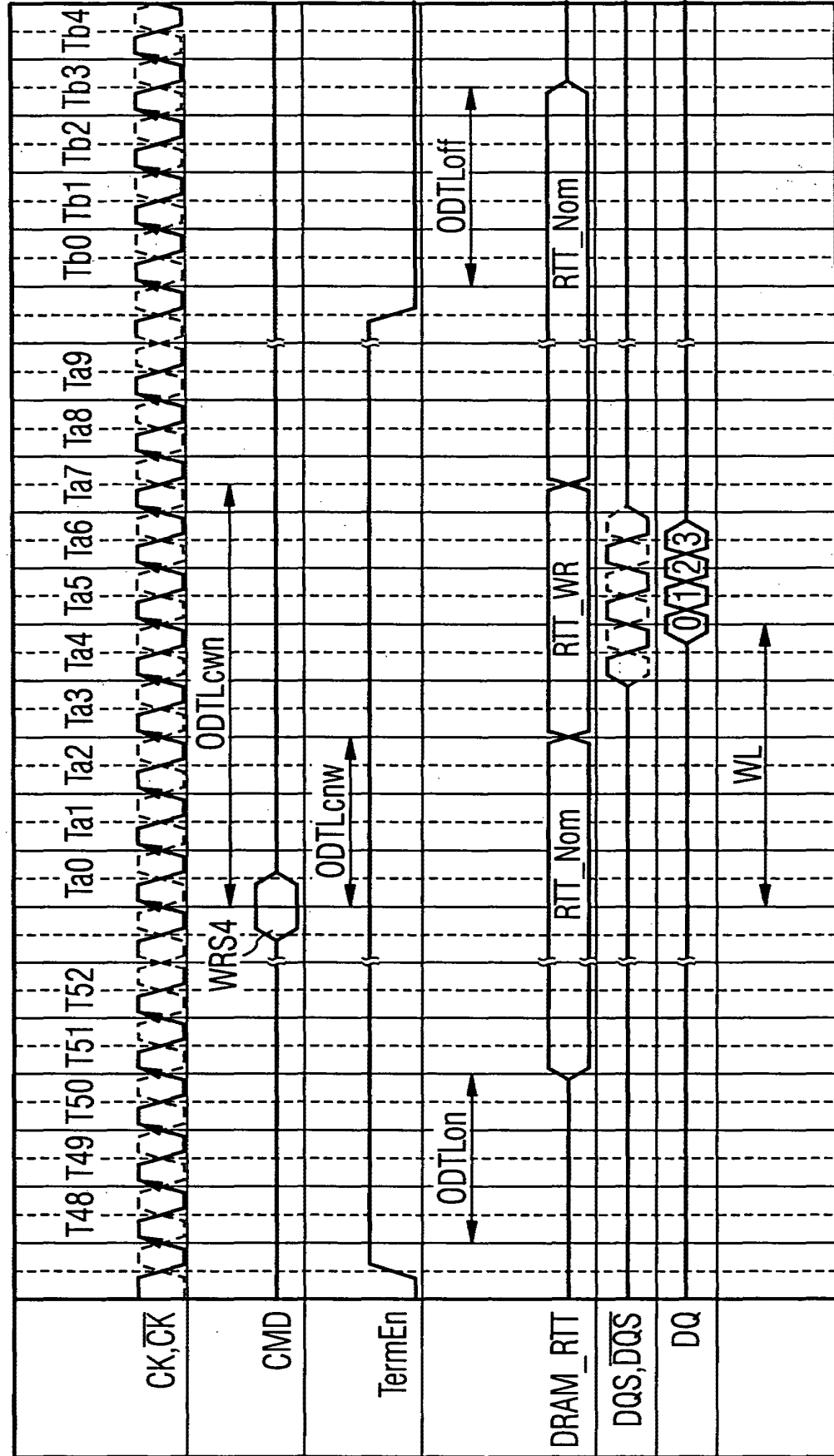


FIG 5





**Prioritätsbescheinigung
DE 10 2005 035 780.6
über die Einreichung einer Patentanmeldung**

Aktenzeichen: 10 2005 035 780.6

Anmeldetag: 29. Juli 2005

Anmelder/Inhaber: Infineon Technologies AG, 81669 München/DE

Bezeichnung: Speicherbaustein und Verfahren zum Betreiben eines Speicherbausteins

IPC: G 11 C 7/02

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 1. August 2006
Deutsches Patent- und Markenamt
Der Präsident
Im Auftrag

Ebert

Beschreibung

Speicherbaustein und Verfahren zum Betreiben eines Speicherbausteins

5

Die Erfindung betrifft einen Speicherbaustein mit einem Anschluss zum Senden und/oder Empfangen von hochfrequenten Signalen. Die Erfindung betrifft weiterhin ein Verfahren zum Betreiben eines Speicherbausteins.

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In Speichersystemen werden üblicherweise eine Vielzahl von Speicherbausteinen eingesetzt, die über einen Speicherbus betrieben werden. Über den Speicherbus werden im allgemeinen Steuerbefehlssignale, Taktsignale, Datensignale und Adresssignale an die Speicherbausteine angelegt. Der Speicherbus umfasst Signalleitungen, die üblicherweise die Speicherbausteine miteinander und mit einem Speicherkontroller verbinden. Bei einer Übertragung von hochfrequenten Signalen können jedoch an den Anschlüssen der Speicherbausteine Signalreflexionen auftreten, die die Datenübertragung auf dem Speicherbus stören und dadurch die Datenübertragungsraten begrenzen. Aus diesem Grund ist es notwendig, bei der Übertragung von Daten über den Speicherbus geeignete Terminierungen an den Anschlüssen der Speicherbausteinen vorzusehen, um die Signalreflexionen auf den Signalleitungen zu vermindern.

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Bei Speicherbausteinen ist bisher vorgesehen, abhängig von einem Terminierungssignal die Terminierung an einem Anschluss des Speicherbausteines ein- bzw. auszuschalten. D. h., der Speicherkontroller stellt jedem der Speicherbausteine ein geeignetes Terminierungssignal zur Verfügung, um die nachfolgende Lese-, Schreib- oder sonstige Operation auf die Speicherbausteine mit einer optimalen Terminierung an allen an den Speicherbus angeschlossenen Speicherbausteinen zu unterstützen. Der Nachteil einer solchen Steuerung der Speicherbausteine besteht darin, dass ein Ein- und Ausschalten der Terminierungswiderstände in der Regel nicht ausreicht, um ei-

ne optimale Terminierung in jedem Betriebszustand zu erreichen und so die Datenübertragung über den Speicherbus zu verbessern.

- 5 Weiterhin kann vorgesehen sein, dass die Stärke der Terminierungswiderstände in den Speicherbausteinen gemäß einem Konfigurationswert festgelegt wird, der zu Beginn des Betriebes des Speichersystems in einer Initialisierungsphase den Speicherbausteinen durch den Speicherkontroller mitgeteilt wird.
- 10 Eine Einstellung der Konfigurationswerte in den Speicherbausteinen vor jedem Schreib- und Lesevorgang ist zeitaufwändig. Daher ist auch die anfängliche Voreinstellung des Terminierungswiderstandes durch den Konfigurationswert nicht geeignet, für jeden Fall der Adressierung der Speicherbausteine
- 15 des Speichersystems geeignete Terminierungswiderstände zum Anlegen an den Speicherbus vorzusehen, da dadurch die Zugriffszeit in dem Speichersystem erheblich verlangsamt würde.
- 20 Es ist daher Aufgabe der vorliegenden Erfindung, einen Speicherbaustein zur Verfügung zu stellen, mit dem in einem Speichersystem eine verbesserte Terminierung des Speicherbusses zur Verfügung gestellt werden kann. Es ist weiterhin Aufgabe der vorliegenden Erfindung, ein Verfahren zum Betreiben des
- 25 Speicherbausteins zur Verfügung zu stellen, mit dem eine verbesserte Signalübertragung, insbesondere eine erhöhte Datenübertragungsrate in einem Speichersystem erreicht werden kann.
- 30 Diese Aufgabe wird durch den Speicherbaustein nach Anspruch 1, durch das Speichersystem nach Anspruch 10 sowie durch das Verfahren nach Anspruch 11 gelöst.

Weitere vorteilhafte Ausgestaltungen der Erfindung sind in

35 den abhängigen Ansprüchen angegeben.

Gemäß einem ersten Aspekt der vorliegenden Erfindung ist ein Speicherbaustein zur Einstellung verschiedener Terminierungen an einer Signalleitung des Datenbusses vorgesehen. Der Speicherbaustein umfasst einen Anschluss, eine mit dem Anschluss
5 verbindbare Terminierungsschaltung, um den Anschluss mit einem einstellbaren Widerstandswert zu terminieren, einen Steueranschluss zum Empfangen eines Steuerbefehlssignals, und eine Steuerschaltung, die mit der Terminierungsschaltung verbunden ist, um abhängig von einem empfangenen Steuerbefehlssignal den
10 Widerstandswert einzustellen und an dem Anschluss bereitzustellen.

Der erfindungsgemäße Speicherbaustein ermöglicht es, abhängig von einem an den Speicherbaustein angelegten Steuerbefehl
15 einen Widerstandswert der Terminierungsschaltung einzustellen und den Anschluss in verbesserter Weise zu terminieren, so dass die Datenübertragung über den Speicherbus, der mit dem Speicherbaustein in einem Speichersystem verbindbar ist, in optimaler Weise unterstützt wird. Auf diese Weise kann der
20 Terminierungswiderstand direkt abhängig von der Operation des Speichersystems eingestellt werden, ohne dass ein Konfigurationswert in dem Speicherbaustein unmittelbar vor dem Durchführen der Operation durch einen entsprechenden, von dem Speicherkontroller gesteuerten Einstellungsvorgang gespeichert werden muss. Zudem ist vorteilhaft, dass die Einstellung der jeweiligen Terminierung nicht von einem Speicherkontroller des Speichersystems gesteuert werden muss, sondern
25 abhängig von der durch die Steuerbefehlssignale vorgegebenen Operation in dem Speichersystem vorgegeben wird.

30 Vorzugsweise kann die Terminierungsschaltung eine Anzahl von Terminierungswiderständen aufweisen, um eine Anzahl von verschiedenen Widerstandswerten bereitzustellen, wobei die Steuerschaltung gestaltet ist, um mindestens einen der Terminierungswiderstände auszuwählen und an den Anschluss anzulegen.
35 Durch das Vorsehen der Anzahl der Terminierungswiderstände in dem Speicherbaustein kann die Wahl des entsprechenden Termini-

nierungswiderstandes relativ schnell erfolgen, so dass kein oder kein wesentlicher Zeitverlust bei der Durchführung der Operation in dem Speichersystem auftritt.

- 5 Gemäß einer bevorzugten Ausführungsform der Erfindung ist eine Konfigurationseinheit vorgesehen, um die Widerstandswerte der Anzahl der Terminierungswiderstände einzustellen. Dadurch ist eine Vorauswahl der Widerstandswerte möglich, mit denen der Anschluss terminiert werden kann.

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Gemäß einer bevorzugten Ausführungsform kann die Terminierungsschaltung einen einstellbaren Terminierungswiderstand umfassen, wobei eine Einstellungsschaltung vorgesehen ist, um abhängig von einem Auswahlsignal einen Einstellungswert bereitzustellen, mit dem der Widerstandswert des Terminierungswiderstandes bestimmt wird.

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Vorzugsweise weist der Speicherbaustein einen Terminierungsanschluss auf, um ein Terminierungssignal zu empfangen, wobei die Steuerschaltung mit der Terminierungsschaltung verbunden ist, um abhängig von dem Terminierungssignal entweder den Anschluss mit dem eingestellten Widerstandswert zu terminieren oder den Anschluss nicht zu terminieren. Auf diese Weise ist es möglich, an dem Anschluss wahlweise auch keine Terminierung vorzusehen, wenn dies durch den Speichercontroller und/oder einem Steuerbefehl vorgegeben wird.

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Vorzugsweise kann die Steuerschaltung mit der Terminierungsschaltung verbunden sein, um abhängig von dem Terminierungssignal den Anschluss mit dem eingestellten Widerstand jeweils mit einer Zeitverzögerung zu terminieren oder nicht zu terminieren, wobei die Zeitverzögerung ausreicht, um den Widerstandswert einzustellen.

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Vorzugsweise kann die Steuereinheit so gestaltet sein, dass der Widerstandswert abhängig von dem Anliegen eines Steuerbefehlssignals nach einer vorbestimmten ersten Umschaltzeit auf

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einen bestimmten zweiten Widerstandswert eingestellt wird und/oder nach einer vorbestimmten zweiten Umschaltzeit auf einen bestimmten ersten Widerstandswert eingestellt wird.

5 Insbesondere kann die Steuereinheit so gestaltet sein, dass der Widerstandswert im Wesentlichen gleichzeitig mit dem Anlegen der Terminierung an den Anschluss auf den zweiten Widerstandswert eingestellt wird und/oder im Wesentlichen gleichzeitig mit dem Beenden des Terminierens des Anschlusses
10 auf den ersten Widerstandswert eingestellt wird.

Gemäß einer bevorzugten Ausführungsform kann ein Befehlsdecoder vorgesehen sein, um abhängig von einem anliegenden Steuerbefehlssignal der Steuereinheit mitzuteilen, ob ein
15 erster oder zweiter Widerstandswert zum Terminieren einzustellen ist.

Gemäß einem weiteren Aspekt der vorliegenden Erfindung ist ein Speichersystem mit einem Speichercontroller, mit einer
20 Anzahl von erfindungsgemäßen Speicherbausteinen und mit einem Speicherbus vorgesehen, mit dem der Speichercontroller und die Speicherbausteine verbunden sind, wobei der Speicherbus eine Signalleitung umfasst, die die Anschlüsse der Speicherbausteine und einen Anschluss des Speichercontrollers miteinander verbindet.
25

Gemäß einem weiteren Aspekt der vorliegenden Erfindung ist ein Verfahren zum Betreiben eines Speicherbausteins vorgesehen, bei dem ein Steuerbefehlssignal empfangen wird, wobei
30 ein Anschluss mit einem einstellbaren Widerstandswert terminiert wird, wobei abhängig von dem empfangenen Steuerbefehlssignal der Widerstandswert eingestellt wird und der Anschluss mit dem eingestellten Widerstandswert terminiert wird. Auf diese Weise ist es möglich, den Terminierungswiderstand, der
35 an einen Anschluss eines Speicherbausteins angelegt wird, abhängig von einem Steuerbefehl einzustellen, so dass es beim Betrieb des Speicherbausteins in einem Speichersystem möglich

ist, für durchzuführende Operationen die geeignete Terminierung an jedem der Speicherbausteine einzustellen, um Signalreflexionen auf den Leitungen des Speicherbusses zu reduzieren und somit die mögliche Datenübertragungsrate zu erhöhen.

5 Weiterhin ist vorteilhaft, dass die Einstellung des Widerstandswertes ohne das Bereitstellen weiterer von außen anzulegender Signale durchgeführt werden kann.

10 Vorzugsweise kann der Widerstandswert durch die Auswahl eines Einstellungswertes für einen einstellbaren Terminierungswiderstand eingestellt werden.

15 Vorzugsweise umfasst das Verfahren, dass der Widerstandswert über die Auswahl aus einer Anzahl von Terminierungswiderständen die an den Anschluss angelegt werden, eingestellt wird.

20 Gemäß einer bevorzugten Ausführungsform der Erfindung kann ein Terminierungssignal empfangen werden, wobei abhängig von dem Terminierungssignal entweder der Anschluss mit dem eingestellten Widerstandswert terminiert oder der Anschluss nicht terminiert wird.

25 Gemäß einer bevorzugten Ausführungsform der Erfindung kann abhängig von einem Pegelwechsel des Terminierungssignals entweder die Terminierung mit dem eingestellten Widerstandswert mit einer Zeitverzögerung eingeschaltet werden oder die Terminierung mit der Zeitverzögerung abgeschaltet werden, wobei die Zeitverzögerung so gewählt wird, dass der gewählte Terminierungswiderstand einstellbar ist.

30 Bevorzugte Ausführungsformen der Erfindung werden nachfolgend anhand der beigefügten Zeichnungen näher erläutert. Es zeigen:

35 Figur 1 ein Blockschaltbild eines Speicherbausteins gemäß einer ersten Ausführungsform der Erfindung;

Figur 2 ein Blockschaltbild eines Speicherbausteins gemäß einer weiteren Ausführungsform der Erfindung;

Figur 3 ist ein Signal-Zeit-Diagramm, das die Funktionalität der Ausführungsformen der Figur 1 und Figur 2 bei Anliegen
5 keiner den Speicherbaustein betreffenden Operation darstellt;

Figur 4 ein Signal-Zeit-Diagramm zur Darstellung der Funktionalität der Ausführungsformen der Figur 1 und 2, die das
10 Durchführen einer Schreiboperation darstellt; und

Figur 5 ein Signal-Zeit-Diagramm zur Darstellung der Funktionalität der Ausführungsformen der Figuren 1 und 2, die das
15 Durchführen einer Schreiboperation bei aktiviertem Terminierungssignal darstellt.

In Figur 1 ist ein Speicherbaustein 1 als Blockschaltbild dargestellt. Der Speicherbaustein 1 umfasst ein Speicherzellenfeld 2, wie z.B. ein DRAM-Speicherzellenfeld, das über einen Logikschaltkreis 3 beschrieben und ausgelesen werden
20 kann. Der Logikschaltkreis 3 umfasst Ansteuerschaltkreise, wie auch Eingangsverstärker und Ausgangstreiber (nicht gezeigt). Die Logikschaltung 3 ist mit einem externen Anschluss 4 des Speicherbausteins 1 verbunden, über den z.B. Adress-, Takt- und Benutzerdaten eingelesen bzw. hinaus getrieben werden können.
25

Der externe Anschluss 4 ist mit einer Terminierungsschaltung 5 verbunden, die einen ersten einstellbaren Terminierungswiderstand 6 mit einem ersten Widerstandswert und einen zweiten einstellbaren Terminierungswiderstand 7 mit einem zweiten Widerstandswert aufweist. Die Terminierungsschaltung 5 ist mit einer Steuereinheit 8 verbunden, die der Terminierungsschaltung 5 ein erstes Steuersignal TermTime0 und ein zweites Steuersignal TermTime1 zur Verfügung stellt. Bei einer Aktivierung des ersten Steuersignal TermTime0 wird der erste Terminierungswiderstand 6 an den externen Anschluss 4 angelegt,
30
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so dass der externe Anschluss 4 mit dem entsprechend in dem ersten Terminierungswiderstand 6 eingestellten ersten Widerstandswert terminiert wird. Bei Aktivierung des zweiten Steuersignals TermTime1 wird entsprechend der zweite Terminierungswiderstand 7 an dem ersten Anschluss angelegt, so dass der externe Anschluss 4 mit dem zweiten Widerstandswert terminiert wird. Weiterhin kann bei gleichzeitiger Aktivierung beider Steuersignale TermTime0, TermTime1 auch ein sich aus der Parallelschaltung des ersten und zweiten Widerstandwertes ergebender weiterer Widerstandswert zur Terminierung erzeugt werden.

Es ist weiterhin eine Konfigurationseinheit 9 vorgesehen, die einen ersten Konfigurationswert TS0 und einen zweiten Konfigurationswert TS1 bereitstellt. Der erste Konfigurationswert TS0 wird an den ersten Terminierungswiderstand 6 und der zweite Konfigurationswert an den zweiten Terminierungswiderstand 7 angelegt, um dort den jeweiligen Widerstandswert des entsprechenden Terminierungswiderstandes 6, 7 einzustellen. Die Konfigurationswerte TS0, TS1 können parallel über Konfigurationssignale bereitgestellt werden. Abhängig von dem jeweiligen Steuersignal TermTime0, TermTime1 wird dann der entsprechende Terminierungswiderstand 6, 7, dessen Widerstandswert durch den jeweiligen Konfigurationswert TS0, TS1 vorgegeben ist, an den externen Anschluss 4 angelegt.

Ein einstellbarer Terminierungswiderstand kann beispielsweise durch schaltbare, parallel geschaltete Widerstände erreicht werden, wobei die Widerstände auch durch ganz oder teilweise durchgeschaltete Transistoren mit gleicher oder verschiedener Kanalbreite realisierbar sind. Die Terminierungswiderstände können so gestaltet sein, dass das jeweilige Steuersignal TermTime0, TermTime1 mit jedem der Bits des bereitgestellten Konfigurationswertes TS0, TS1 mit einer UND-Verknüpfung logisch verknüpft werden und die jeweiligen Verknüpfungsergebnisse an die Eingänge von in dem Terminierungswiderstand vorgesehenen Transistoren angelegt werden.

Die Steuereinheit 8 erhält über einen externen Terminierungs-
anschluss 13 ein Terminierungssignal TermEn, das angibt, ob
eine Terminierung an dem externen Anschluss 4 vorgesehen sein
5 soll oder nicht. D.h., durch das erste und das zweite Steuer-
signal TermTime0, TermTime1 wird der jeweilige Terminierungs-
widerstand 6, 7 nur dann an den externen Anschluss 4 ange-
legt, wenn das Terminierungssignal TermEn angibt, dass eine
Terminierung erfolgen soll. Andernfalls wird keine Terminie-
10 rung des externen Anschlusses 4 vorgenommen.

Welcher der zwei Terminierungswiderstände 6, 7 an den exter-
nen Anschluss 4 angelegt wird, wird abhängig von einem Be-
fehlssignal BS angegeben, das von einem Befehlsdecodierer 10,
15 abhängig von einem empfangenen Steuerbefehl CMD, bereitge-
stellt wird. Der Befehlsdecodierer 10 empfängt über einen o-
der mehreren externe Anschlüsse 11 Steuerbefehlssignale CMD
zur Aktivierung, Adressierung und/oder Ansteuerung des Spei-
cherbausteins 1.

20 Die Steuerbefehlssignale CMD können einen aktiven oder inak-
tiven Zustand einnehmen. Handelt es sich bei dem Speicherbau-
stein 1 um einen DRAM-Speicherbaustein, so können die Steuer-
befehlssignale beispielsweise das Chip-Select-Signal CS zum
Auswählen des betreffenden Speicherbausteins für eine be-
25 stimmte Operation, das Schreib-Enable-Signal WE zum Anzeigen
eines Write-Zugriffs auf den Speicherbaustein, das RAS-Signal
(Zeilenaktivierungssignal) zum Übermitteln der Wortleitungs-
adresse und zum Aktivieren der Wortleitung sowie das CAS-
30 Signal (Spaltenaktivierungssignal) zum Übertragen der Bitlei-
tungsadresse und zum Aktivieren der Bitleitung zum Auslesen
bzw. Hineinschreiben von Daten in das Speicherzellenfeld
sein. Je nach dem, ob der betreffende Speicherbaustein in ei-
nem Speichersystem für eine Operation ausgewählt ist oder
35 nicht (Chip-Select-Signal) bzw. ob ein Schreiben oder Lesen
auf den betreffenden Speicherbaustein durchgeführt werden
soll (Write-Enable-Signal) kann nun einer der beiden Termi-

nierungswiderstände 6, 7 bzw. keiner der beiden Terminierungswiderstände (gesteuert durch das Terminierungssignal) ausgewählt werden, um den externen Anschluss 4 in geeigneter Weise zu terminieren.

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In Figur 2 ist eine weitere Ausführungsform der Erfindung dargestellt. Darin sind Elemente gleicher oder vergleichbarer Funktion mit den gleichen Bezugszeichen versehen. Die Ausführungsform der Figur 2 unterscheidet sich von der Ausführungsform der Figur 1 dadurch, dass eine Einstellungseinheit 15 vorgesehen ist, die die Konfigurationseinheit 9 und einen Multiplexer 12 aufweist. An einem Steuereingang des Multiplexers 12 ist ein von der Steuereinheit 8 bereitgestelltes Terminierungsauswahlsignal TermSel angelegt. Mit Hilfe des Terminierungsauswahlsignals TermSel wird ausgewählt, welcher der durch die Konfigurationseinheit 9 bereitgestellte Konfigurationswert TS0, TS1 an die Terminierungsschaltung 5 angelegt wird. Die Terminierungsschaltung 5 umfasst in dieser Ausführungsform nur einen einstellbaren Terminierungswiderstand 6, dessen Widerstandswert abhängig von dem ausgewählten Konfigurationswert TS0, TS1 eingestellt wird. Abhängig von dem einzigen Steuersignal TermTime0, das durch die Steuereinheit 8 bereitgestellt wird, wird nun der einzige Terminierungswiderstand 6 aktiviert oder deaktiviert und somit an den externen Anschluss 4 angelegt oder nicht.

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Die Größe des Widerstandswertes des Terminierungswiderstandes 6 bestimmt sich durch das Terminierungsauswahlsignal TermSel, mit dem einer der Konfigurationswerte TS0, TS1 ausgewählt wird. Bei dieser Ausführungsform ist es möglich, im Gegensatz zur Ausführungsform der Figur 1, auf einen zweiten einstellbaren Terminierungswiderstand zu verzichten und statt dessen den einzigen einstellbaren Terminierungswiderstand gemäß einem über den Multiplexer 12 auswählbaren Konfigurationswert abhängig den von aktuellen Steuerbefehlssignalen auszuwählen. Eine Kombination von verschiedenen Terminierungswiderständen, die gleichzeitig an den externen Anschluss 4 angelegt werden,

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wie in Figur 1 gezeigt, ist damit nicht möglich, jedoch kann Chipfläche eingespart werden, da nur ein einstellbarer Terminierungswiderstand 6 benötigt wird.

- 5 In Figur 3 ist ein Signal-Zeit-Diagramm zur Verdeutlichung des Signalverlaufs für die Einstellung der Terminierung in einem erfindungsgemäßen Speicherbaustein gezeigt. In dem Signal-Zeit-Diagramm der Figur 3 ist ein Fall angegeben, bei dem eine Terminierung eingeschaltet werden soll, wenn das Befehlssteuersignal angibt, dass der betreffende Speicherbaustein nicht aktiviert ist, d.h. kein Zugriff auf den Speicherbaustein durchgeführt werden soll (Chip-Select-Signal deaktiviert). Ausgelöst durch das Aktivieren des Terminierungssignals TermEn durch den Speichercontroller und durch eine
- 10 steigende Flanke eines Taktsignals CK zu einem Zeitpunkt T0 wird nach einer vorbestimmten Terminierungseinschaltzeit ODTLon von in diesem Beispiel drei Taktperioden ein gewünschter erster Widerstandswert RTT_Nom (DRAM_RTT) an den externen Anschluss 4 angelegt. Nach Deaktivieren des Terminierungssignals TermEn während der fünften Taktperiode T5 beginnt mit der nächsten steigenden Flanke des Taktsignals T6 eine vorbestimmte Terminierungsausschaltzeit ODTLoff, die in diesem Ausführungsbeispiel dreieinhalb Taktperioden beträgt und nach deren Ablauf der Terminierungswiderstand von dem externen Anschluss 4 getrennt wird. Die Zeitdauern der Terminierungseinschaltzeit ODTLon und der Terminierungsausschaltzeit ODTLoff sind im Wesentlichen beliebig wählbar und sollten so gewählt sein, dass sie ausreichen, den Terminierungswiderstand zuverlässig mit dem externen Anschluss 4 zu verbinden oder von diesem zu trennen. D.h., sie sollten mindestens die Zeitdauer betragen, die zum Ein- bzw. Ausschalten eines Terminierungswiderstandes bzw. dem Anlegen und dem Trennen des Terminierungswiderstandes von dem externen Anschluss 4 benötigt wird.
- 25
- 30
- 35 Z. B. bei deaktiviertem Chip-Select-Signal, d.h., wenn keine Operation in dem Speicherbaustein durchgeführt werden soll, kann daher die Terminierung des externen Anschlusses 4 vorge-

nommen werden oder nicht, was in einem Speichersystem durch den Speichercontroller mit Hilfe des Terminierungssignals TermEn gesteuert wird. Gleichzeitig wird Speicherbaustein intern festgestellt, dass das Chip-Select-Signal CS deaktiviert ist und abhängig von dem Chip-Select-Signal CS ein entsprechender Konfigurationswert bzw. Steuersignal (je nach Ausführungsform) an die Terminierungsschaltung 5 angelegt wird, um den dort aktiven Terminierungswiderstand 6, 7 bzw. 6 abhängig von dem Terminierungssignal TermEn an den externen Anschluss 4 anzulegen.

In Figur 4 ist ein weiteres Signal-Zeit-Diagramm für die Ausführungsform der Figur 1 und 2 dargestellt. Das Signal-Zeit-Diagramm der Figur 4 zeigt einen Fall an, bei dem der entsprechende Speicherbaustein durch das Chip-Select-Signal CS aktiviert ist und ein Schreibbefehl (WE-Signal) WRS8 an den Speicherbaustein durch den Speichercontroller gesendet werden. Der Speichercontroller legt vorzugsweise das Terminierungssignal TermEn und das Schreibsignal WRS8 so an, dass es zu einem Zeitpunkt T12 durch eine steigende Taktflanke in den Speicherbaustein übernommen werden kann. Der Befehlsdecodierer decodiert das Schreibsignal WRS8 und generiert das Befehlssignal BS, das an die Steuereinheit 8 angelegt wird. In der Steuereinheit 8 wird abhängig von dem Befehlssignal BS festgestellt, dass nun ein Terminierungswiderstand an den externen Anschluss 4 angelegt werden soll, der durch den zweiten Konfigurationswert bestimmt ist. Die Steuereinheit 8 aktiviert daher bei der Ausführungsform der Figur 1 das zweite Steuersignal TermTimel, um den zweiten Terminierungswiderstand 7 zu aktivieren. Bei der Ausführungsform der Figur 2 schaltet die Steuereinheit 8 das Terminierungsauswahlsignal TermSel so, dass der Multiplexer 12 den zweiten Konfigurationswert an die Terminierungsschaltung 5 anlegt, um dort den Widerstandswert des Terminierungswiderstandes 6 auf den entsprechenden Wert, in diesem Fall auf einen zweiten Widerstandswert RTT_WR einzustellen, der dem Terminierungswiderstand entspricht, der an die aktivierten Speicherbausteine

bei einem Schreibzugriff an den externen Anschluss 4 angelegt werden soll.

Abhängig von dem Terminierungssignal TermEn wird nun nach der
5 Terminierungseinschaltzeit ODTLon der Terminierungswiderstand
an den externen Anschluss 4 angelegt, wobei nun der Terminie-
rungswiderstand abhängig von dem Steuerbefehlssignal ein an-
derer ist, wie zuvor beim deaktivierten Speicherbaustein
(Fig. 3). Gleichzeitig beginnt mit dem Empfang des Schreibbe-
10 fehls WRS8 die Schreiblatenzzeitdauer WL zu laufen, die in
den gezeigten Ausführungsbeispielen 5 Taktperioden beträgt.
In einer Taktperiode vor dem Übertragen eines Datenburst,
d.h. Übertragen von 8 Datenbits, kann das Daten-Strobe-Signal
DQS synchron zu den Daten in den Speicherbaustein eingelesen
15 werden. Die Terminierungseinschaltzeit ODTLon ist vorzugswei-
se gleich oder kleiner der Schreiblatenzzeitdauer WL gewählt,
so dass sichergestellt wird, dass beim Übertragen der Daten
zu dem Speicherbaustein (beim Schreibzugriff) der gewünschte
Terminierungswiderstand an dem externen Anschluss 4 angelegt
20 ist.

Im Allgemeinen wird das Befehlssignal BS in dem Befehlsdeco-
dierer 10 so erzeugt, dass es der Steuereinheit 8 angibt,
welcher Widerstandswert als Terminierungswiderstand RTT_Nom
25 oder RTT_WR für den Anschluss eingestellt werden soll. Bei
einer ersten Gruppe von anliegenden Steuerbefehlen CMD gibt
der Befehlsdecodierer 10 ein Befehlssignal BS an die Steuer-
einheit 8 aus, das angibt, dass eine Terminierung mit dem
ersten Widerstandswert RTT_Nom vorgenommen werden soll (bei
30 aktiviertem Terminierungssignal TermEn) und bei einer zweiten
Gruppe von Steuerbefehlen gibt der Befehlsdecodierer 10 ein
Befehlssignal BS an die Steuereinheit 8 aus, das angibt, dass
der Anschluss 4 mit einem zweiten Widerstandswert terminiert
werden soll (bei aktiviertem Terminierungssignal TermEn). Die
35 erste Gruppe von Steuerbefehlen kann Steuerbefehle umfassen,
die beispielsweise eine Deaktivierung der integrierten Schal-
tung bzw. einen Lesezugriff auf die integrierte Speicher-

schaltung anzeigen, während die zweite Gruppe von Steuerbefehlen Schreibbefehle auf die integrierte Speicherschaltung anzeigen kann.

- 5 Die Zeitdauer zwischen dem Anlegen eines Steuerbefehlssignals bzw. zwischen dem Bereitstellen des Befehlssignals BS an die Steuereinheit 8 und davon abhängigen Änderungen des Widerstandswertes in der Terminierungsschaltung 5 ist vorzugsweise als erste Umschaltzeit ODTLCNW festgelegt, die vorzugsweise
10 gleich oder kleiner der Terminierungseinschaltzeit ODTLon ist.

- Weiterhin kann für einen Fall eines anliegenden Steuerbefehles der zweiten Gruppe von Steuerbefehlen beispielsweise vor-
15 gesehen sein, dass die Steuereinheit 8 nach Ablauf einer zweiten Umschaltzeit ODTLCWN die Terminierung von den zweiten Widerstandswert auf den ersten Widerstandswert ändert, unabhängig davon, ob das Terminierungssignal TermEn eine Terminierung vorsieht oder nicht. Die zweite Umschaltzeit ODTLCWN
20 entspricht mindestens einer Zeitdauer, die durch das Beenden des Schreibzugriffs bzw. durch das Beenden eines Zugriffs auf den Speicherbaustein, der durch einen Steuerbefehl der zweiten Gruppe von Steuerbefehlen ausgelöst ist, bestimmt ist. Im Falle eines Burst-Schreibzugriffs, wie in Verbindung mit Fi-
25 gur 4 beschrieben wurde, sollte die zweite Umschaltzeit abhängig von der Schreiblatenzzeit WL und abhängig von der Zeitdauer für den Burstzugriff sein. Die zweite Umschaltzeit ODTLCBM ist vorzugsweise die Summe der Schreiblatenz WL und der Dauer des Burstzugriffs ($\text{Burstlänge} / 2 * \text{Taktzykluslänge}$
30 TCK) zuzüglich einer Sicherheitszeitdauer ($1/2 * \text{TCK}$ oder das Vielfache davon). Auf diese Weise ist es möglich, dass der zweite Widerstandswert RTT_WR zum Terminieren des Anschlusses abhängig von einem anliegenden Steuerbefehl CMD nur für eine bestimmte Zeitdauer zur Terminierung des Anschlusses bereit-
35 gestellt wird, wobei der Anschluss nach Ablauf dieser Zeitdauer wieder mit dem ersten Widerstandswert terminiert wird,

sofern dieses durch das Terminierungssignal TermEn angegeben ist.

5 Zu Figur 5 ist ein Fall gezeigt, bei dem das Terminierungs-
signal TermEn die Terminierung des Anschlusses 4 vor während
und nach einem Schreibzugriff WRS4 eingeschaltet lässt, wobei
die Terminierung vor dem Schreibzugriff auf den ersten Wider-
standswert RTT_Nom eingestellt ist. Nach Ablauf der ersten
10 Umschaltzeit ODTLCNW wird der Anschluss 4 mit dem Wider-
standswert RTT_WR terminiert und nach Ablauf der zweiten Um-
schaltzeit ODTLCWN die Terminierung wieder auf den ersten Wi-
derstandswert RTT_Nom zurückgeschaltet.

15 Auch wenn in dem gezeigten Ausführungsbeispiel nur zwei ver-
schiedene Terminierungswiderstände an den externen Anschluss
4 angelegt werden können, kann die Anzahl von verschiedenen
einstellbaren Terminierungswiderständen jedoch beliebig hoch
sein, so dass für verschieden Zugriffe in einem Speichersys-
tem, in dem der Speicherbaustein betrieben wird, verschiede-
20 nen Terminierungswiderstände an die externen Anschlüsse ange-
legt werden können.

25 Eine Idee der Erfindung besteht darin, während des Betriebs
die Speicherbausteine in einem Speichersystem die Terminie-
rungswiderstände abhängig von der aktuell durchgeführten Ope-
ration für jeden der Speicherbausteine gezielt einstellen zu
können. So können in erster Linie verschiedene Terminierungswi-
derstände vorgesehen sein, die wahlweise oder auch in Kombi-
nation an den externen Anschluss angelegt werden können. Zu-
30 sätzlich kann es möglich sei, dass Anlegen eines Terminie-
rungswiderstandes an den externen Anschluss abhängig von ei-
nem Terminierungssignal TermEn durchzuführen.

Ansprüche

1. Speicherbaustein (1) zur Einstellung verschiedener Terminierungen

5 mit einem Anschluss (4)

mit einer mit dem Anschluss (4) verbindbaren Terminierungsschaltung (5), um den Anschluss (4) mit einen einstellbaren Widerstandswert zu terminieren,

10 mit einem Ansteueranschluss zum Empfangen eines Steuerbefehlssignals;

mit einer Steuerschaltung, die mit der Terminierungsschaltung verbunden ist, um abhängig von einem empfangenen Steuerbefehlssignal den Widerstandswert einzustellen und den Anschluss mit diesem zu terminieren.

15

2. Speicherbaustein (1) nach Anspruch 1, wobei die Terminierungsschaltung eine Anzahl von Terminierungswiderständen (6, 7) aufweist, um eine Anzahl von Widerstandswerten bereitzustellen, wobei die Steuerschaltung (8) gestaltet ist, um mindestens einen der Terminierungswiderstände (6, 7) auszuwählen und an den Anschluss (4) anzulegen.

20

3. Speicherbaustein (1) nach Anspruch 2,

25 mit einer Konfigurationseinheit (9), um die Widerstandswerte der Anzahl der Terminierungswiderstände einzustellen.

4. Speicherbaustein (1) nach Anspruch 1, wobei die Terminierungsschaltung einen einstellbaren Terminierungswiderstand (6) umfasst, wobei eine Einstellungsschaltung

30

(15) vorgesehen ist, um abhängig von einem Auswahlsignal (TermSel) einen Einstellungswert bereitzustellen, mit

dem der Widerstandswert des Terminierungswiderstandes (6) bestimmt wird.

- 5 5. Speicherbaustein (1) nach einem der Ansprüche 1 bis 4,
mit einem Terminierungsanschluss (13), um ein Terminie-
rungssignal zu empfangen, wobei die Steuerschaltung (8)
mit der Terminierungsschaltung verbunden ist, um abhän-
gig von dem Terminierungssignal (TermEn) entweder den
Anschluss (4) mit dem eingestellten Widerstandswert zu
10 terminieren oder den Anschluss (4) nicht zu terminieren.
- 15 6. Speicherbaustein (1) nach einem der Ansprüche 1 bis 5,
wobei die Steuerschaltung mit der Terminierungsschaltung
(5) verbunden ist, um den Anschluss (4) abhängig von dem
Terminierungssignal entweder mit dem eingestellten Wi-
derstandswert mit einer Zeitverzögerung zu terminieren
oder nicht zu terminieren, wobei die Zeitverzögerung
ausreicht, um den Widerstandswert einzustellen.
- 20 7. Speicherbaustein nach einem der Ansprüche 1 bis 6, wobei
die Steuereinheit so gewählt ist, dass der Widerstands-
wert abhängig von dem Anliegen eines Steuerbefehlssig-
nals nach einer vorbestimmten ersten Umschaltzeit auf
einen bestimmten zweiten Widerstandswert eingestellt
25 wird und/oder nach einer vorbestimmten zweiten Umschalt-
zeit auf einen bestimmten ersten Widerstandswert einge-
stellt wird.
- 30 8. Speicherbaustein nach Anspruch 7, wobei die Steuerein-
heit so gestaltet ist, dass der Widerstandswert abhängig
von dem Steuerbefehlssignal im Wesentlichen gleichzeitig
mit der Terminierung des Anschlusses (4) auf den zweiten
Widerstandswert eingestellt wird und/oder im Wesentli-

chen gleichzeitig mit dem Beenden des Terminierens des Anschlusses (4) auf den ersten Widerstandswert eingestellt wird.

- 5 9. Speicherbaustein nach einem der Ansprüche 1 bis 8, wobei ein Befehlsdecodierer vorgesehen ist, um abhängig von einem anliegenden Steuerbefehlssignal der Steuereinheit mitzuteilen, ob ein erster oder ein zweiter Widerstandswert zum Terminieren einzustellen ist.

10

10. Speichersystem mit einem Speicherkontroller mit einer Anzahl von Speicherbausteinen (1) nach einem der Ansprüche 1 bis 6, mit einem Speicherbus, um den Speicherkontroller und die Speicherbausteine (1) zu verbinden, wobei der Speicherbus eine Signalleitung umfasst, die die Anschlüsse (4) der Speicherbausteine (1) und einen Anschluss des Speicherkontrollers miteinander verbindet.

15

11. Verfahren zum Betreiben eines Speicherbausteins (1),

20

wobei ein Steuerbefehlssignal empfangen wird;
wobei ein Anschluss (4) mit einem einstellbaren Widerstandswert terminiert wird,
wobei abhängig von dem empfangenen Steuerbefehlssignal der Widerstandswert eingestellt und der Anschluss mit dem Widerstandswert terminiert wird.

25

12. Verfahren nach Anspruch 11, wobei der Widerstandswert durch die Auswahl eines Einstellungswertes für einen einstellbaren Terminierungswiderstand eingestellt wird.

30

13. Verfahren nach Anspruch 11, wobei der Widerstandswert über die Auswahl aus einer Anzahl von Terminierungswiderständen (6, 7), die an den Anschluss (4) angelegt werden, eingestellt wird.

5

14. Verfahren nach einem der Ansprüche 11 bis 13, wobei ein Terminierungssignal (TermEn) empfangen wird, wobei abhängig von dem Terminierungssignal entweder der Anschluss (4) mit dem eingestellten Widerstandswert terminiert wird oder der Anschluss (4) nicht terminiert wird.

10

15. Verfahren nach Anspruch 14, wobei abhängig von dem Terminierungssignal (TermEn) entweder die Terminierung mit dem eingestellten Widerstandswert mit einer Zeitverzögerung eingeschaltet wird oder die Terminierung mit der Zeitverzögerung abgeschaltet wird, wobei die Zeitverzögerung so gewählt wird, dass der ausgewählte Terminierungswiderstand einstellbar ist.

15

16. Verfahren nach Anspruch 15, wobei der Widerstandswert abhängig von dem Anliegen eines Steuerbefehlssignals nach einer vorbestimmten ersten Umschaltzeit auf einen bestimmten zweiten Widerstandswert eingestellt wird und/oder nach einer vorbestimmten zweiten Umschaltzeit auf einen bestimmten ersten Widerstandswert eingestellt wird.

20

25

17. Verfahren nach Anspruch 16, wobei der Widerstandswert abhängig von dem Steuerbefehlssignal im Wesentlichen gleichzeitig mit der Terminierung des Anschlusses (4) auf den zweiten Widerstandswert eingestellt wird und/oder im Wesentlichen gleichzeitig mit dem Beenden des Terminierens des Anschlusses (4) auf den ersten Widerstandswert eingestellt wird.

30

Zusammenfassung

Speicherbaustein und Verfahren zum Betreiben eines Speicherbausteins

5 Die Erfindung betrifft einen Speicherbaustein (1) zur Einstellung verschiedener Terminierungen mit einem Anschluss (4), mit einer mit dem Anschluss (4) verbindbaren Terminierungsschaltung (6), um den Anschluss mit einen einstellbaren
10 Widerstandswert zu terminieren, mit einem Ansteueranschluss (11) zum Empfangen eines Steuerbefehlssignals, und mit einer Steuerschaltung (8), die mit der Terminierungsschaltung (5) verbunden ist, um abhängig von einem empfangenen Steuerbefehlssignal einen Widerstandswert einzustellen und den An-
15 schluss (4) mit diesem zu terminieren.

Figur 1

FIGUR FÜR DIE ZUSAMMENFASSUNG

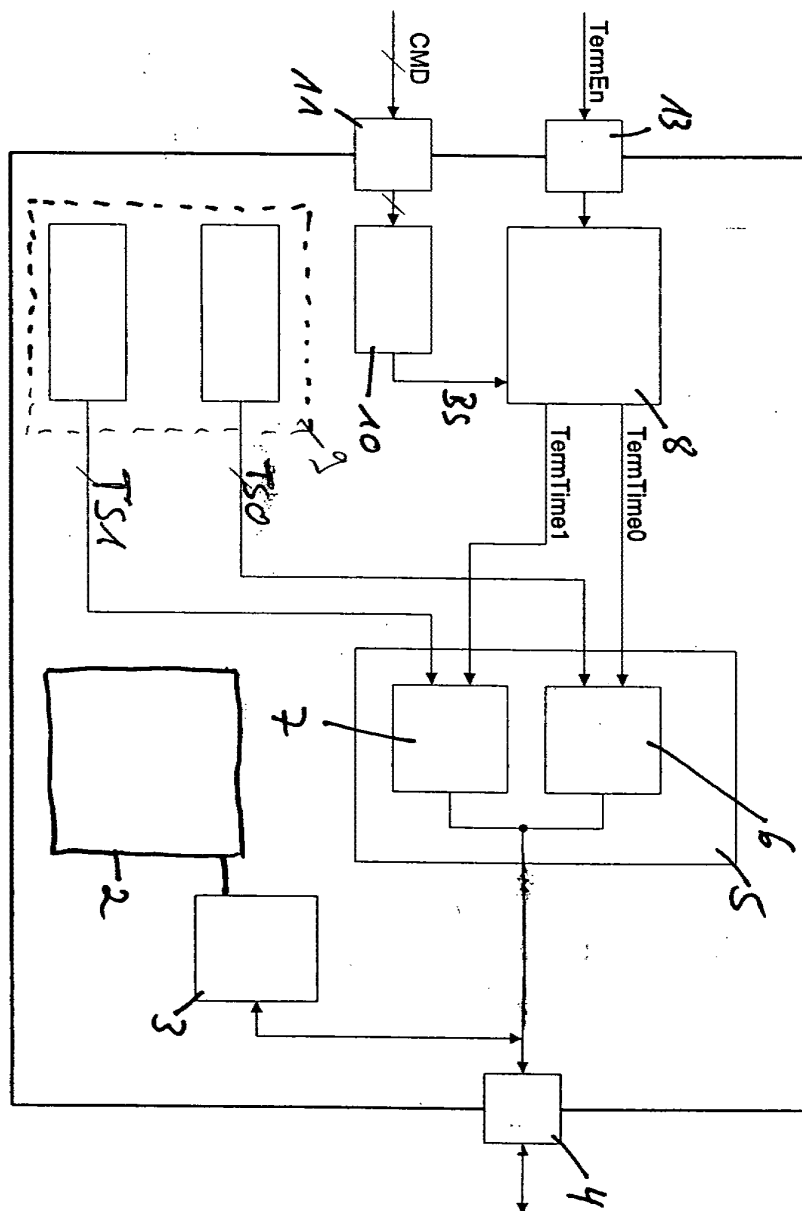


Fig. 1

Bezugszeichenliste

	1	Speicherbaustein
	2	Speicherzellenfeld
5	3	Logikschaltkreise
	4	externer Anschluss
	5	Terminierungsschaltung
	6	erster Terminierungswiderstand
	7	zweiter Terminierungswiderstand
10	8	Steuereinheit
	9	Konfigurationseinheit
	10	Befehlsdecodierer
	11	Steuerbefehlsanschluss
	12	Multiplexer
15	13	Terminierungsanschluss
	15	Einstellungsschaltung

215

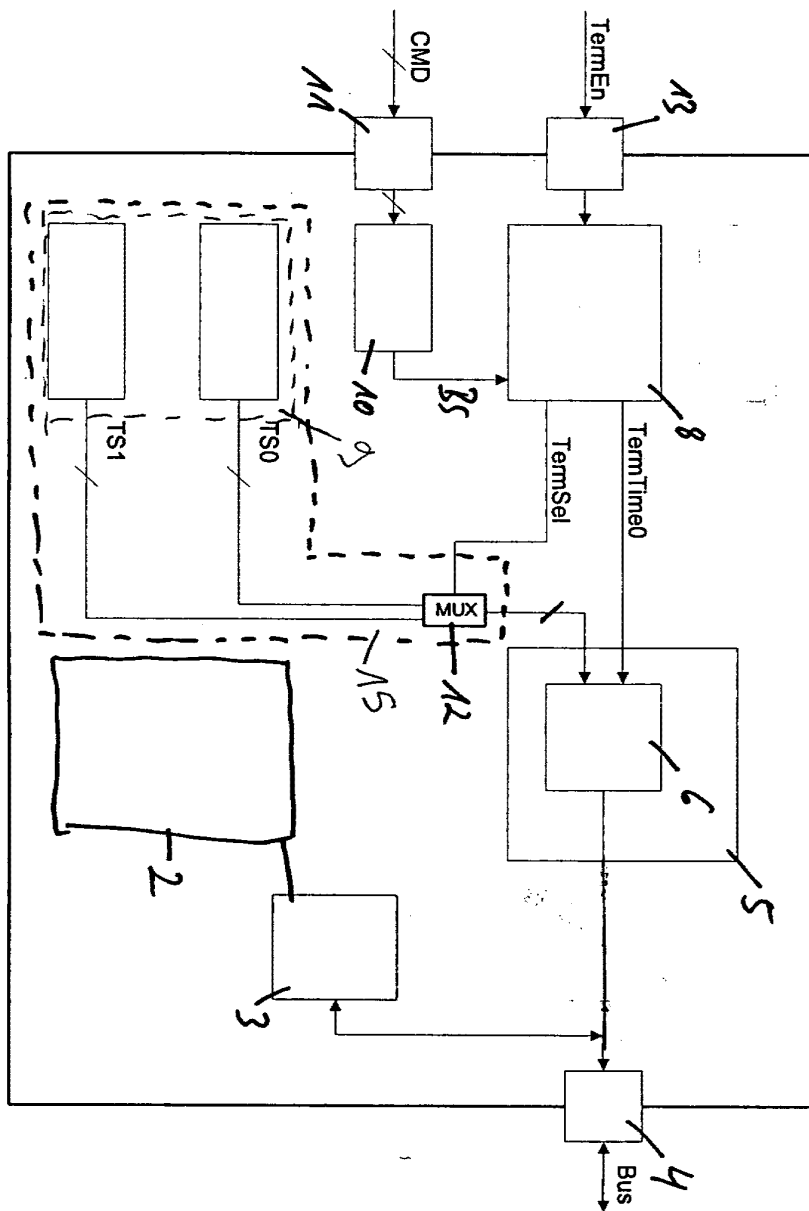


Fig. 2

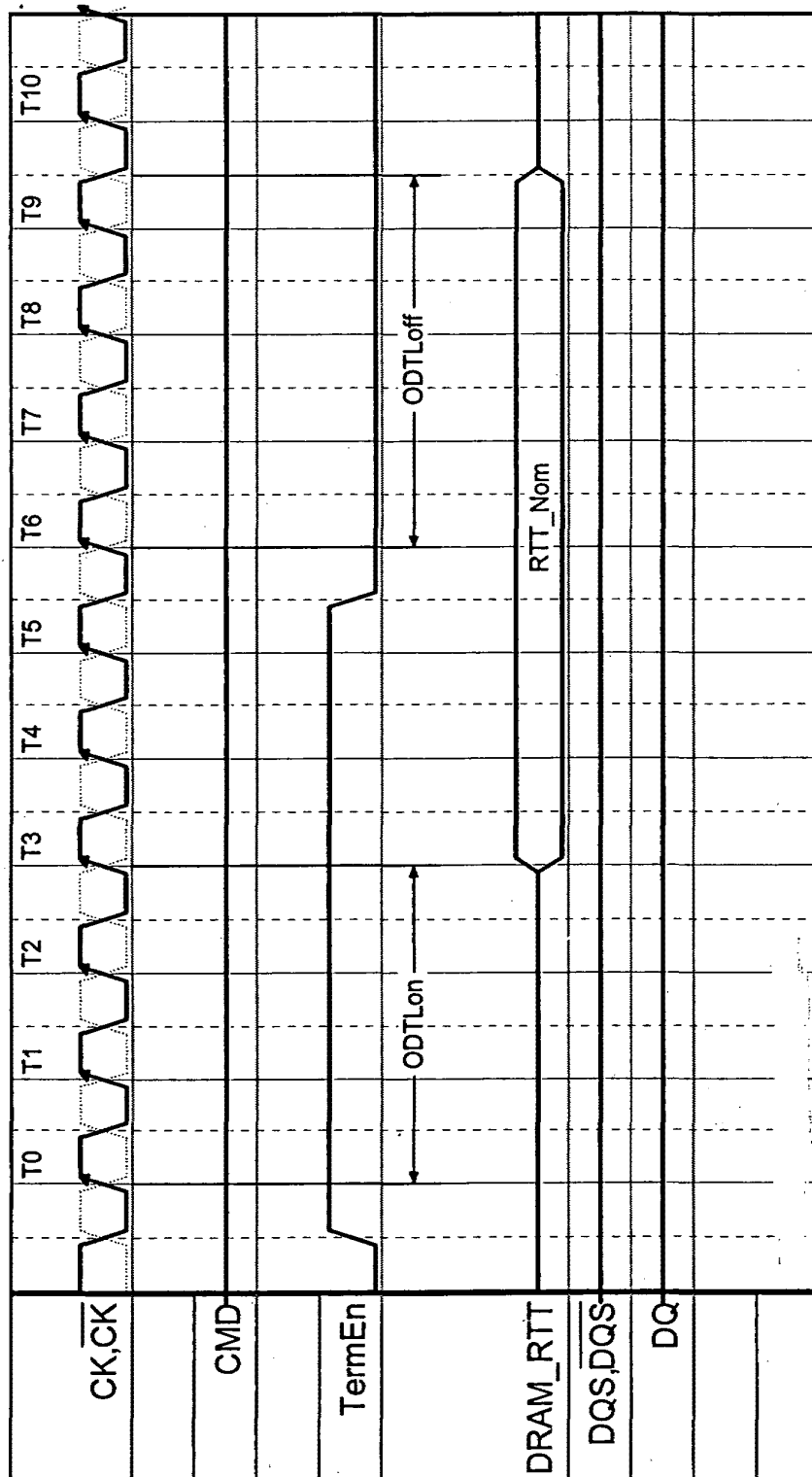


Fig. 3

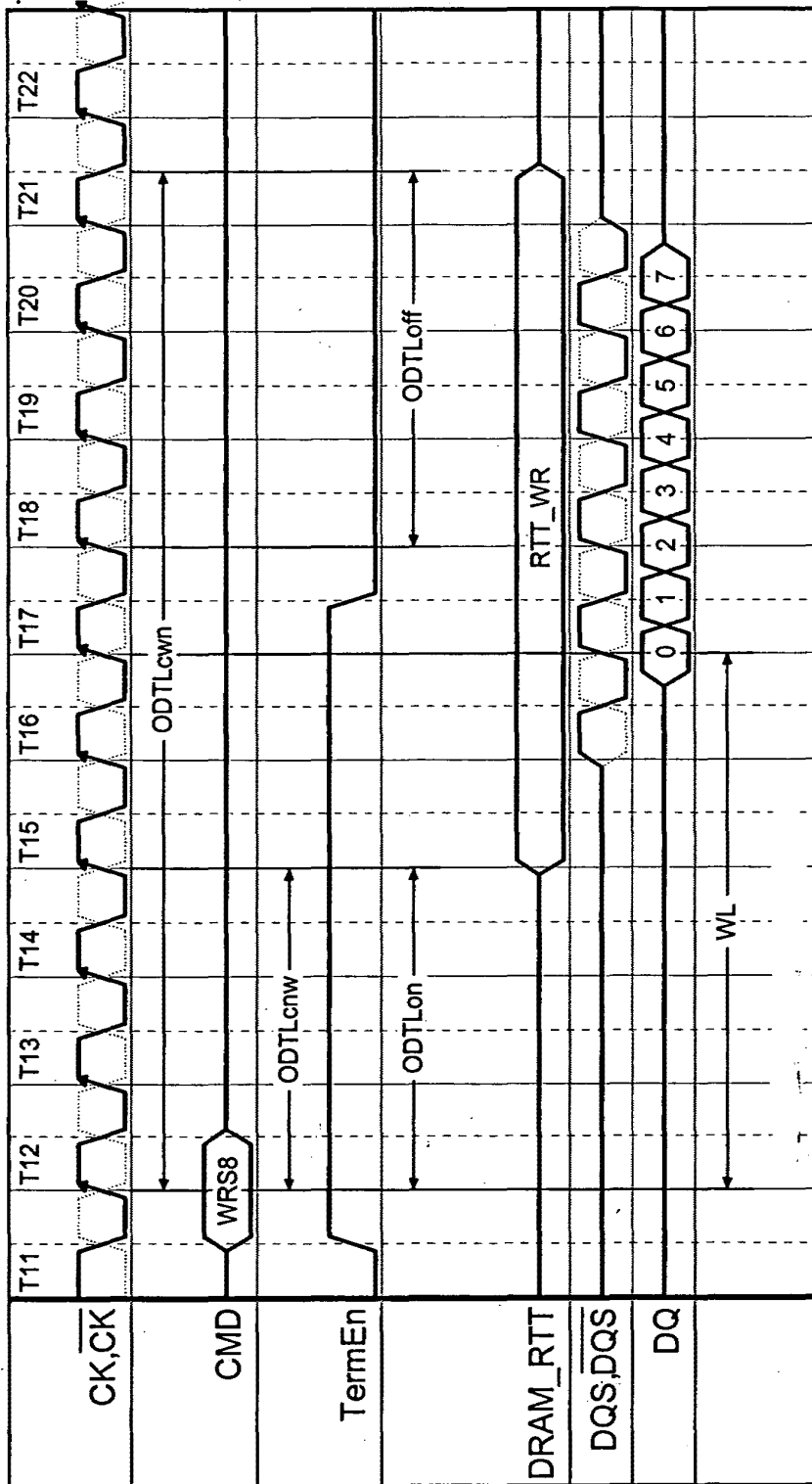


Fig. 4

4/5

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	Filing Date		2006-07-31	
	First Named Inventor	Georg Braun		
	Art Unit	2824		
	Examiner Name			
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	First Named Inventor	Georg Braun	
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	1	DDR2 SDRAM SPECIFICATION, JEDEC Standard No. 79-2A, pages 6 and 14-22, January 2004.	☐
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STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	11461380
Filing Date	2006-07-31
First Named Inventor	Georg Braun
Art Unit	2824
Examiner Name	
Attorney Docket Number	1525.026262 (INFN/WB0310)

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Joseph M. Jong, Reg. No. 42,698/	Date (YYYY-MM-DD)	2007-11-07
Name/Print	Joseph M. Jong	Registration Number	42698

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EFS ID:	2435400
Application Number:	11461380
International Application Number:	
Confirmation Number:	3530
Title of Invention:	MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP
First Named Inventor/Applicant Name:	Georg Braun
Customer Number:	46798
Filer:	Joseph M. Jong
Filer Authorized By:	
Attorney Docket Number:	1525.026262 (INFN/WB0310)
Receipt Date:	07-NOV-2007
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Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	0310_IDS.pdf	656944 226d600a6e9637a63a0e5362705a16d ab0d48f11	no	4

Warnings:

Information:					
2	NPL Documents	JEDEC_79-2A.PDF	357561	no	10
			8e290da8a2013b46ed0f3f26aa0711129ae54872		
Warnings:					
Information:					
Total Files Size (in bytes):			1014505		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	Confirmation No.:	3530
Braun et al.	§		
	§	Group Art Unit:	2819
Serial No.: 11/461,380	§		
	§	Examiner:	unknown
Filed: July 31, 2006	§		
	§		
For: MEMORY CHIP AND METHOD	§		
FOR OPERATING A MEMORY	§		
CHIP	§		

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office to fax number 571-273-8300 to the attention of Examiner unknown, or electronically transmitted via EFS-Web, on the date shown below:

November 2, 2007
Date

/Karla Marquez/
Karla Marquez

PRELIMINARY AMENDMENT

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A memory chip for variably setting terminations, comprising:

a terminal;

a termination circuit ~~[[in]]~~ coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

a control command port for receiving a control command signal for affecting accessibility of the memory chip; and

a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal.

2. (Original) The memory chip of claim 1, wherein the termination circuit comprises a plurality of terminating resistors each having respective resistance values, wherein the control circuit sets the resistance value by selecting at least one of the terminating resistors and applying it to the terminal.

3. (Original) The memory chip of claim 2, further comprising:
a configuration unit configured to set the resistance values of the plurality of terminating resistors.

4. (Original) The memory chip of claim 1, wherein the termination circuit comprises a settable terminating resistor, and further comprising a setting circuit configured to output a setting value on the basis of which the terminating resistor is set to the resistance value.

5. (Currently Amended) The memory chip of claim 1, further comprising:
a termination port to receive a termination signal, wherein the control circuit ~~being~~ is configured to selectively terminate the terminal with the set resistance value in

response to the termination signal.

6. (Original) The memory chip of claim 5, wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

7. (Original) The memory chip of claim 6, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

8. (Original) The memory chip of claim 7, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

9. (Original) The memory chip of claim 8, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal.

10. (Original) The memory chip of claim 1, further comprising:
a command decoder operable, as a function of the received control command signal, to communicate to the control circuit whether the resistance value is to be set to a first value or a second value.

11. (Currently Amended) A memory system, comprising:
(a) a memory controller having a terminal;

(b) a plurality of memory chips₁ at least one of the memory chips comprising:

a terminal;

a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;

a control command port for receiving a control command signal for affecting accessibility of the memory chip; and

a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller.

12. (Currently Amended) The ~~memory~~ system of claim 11, wherein the termination circuit comprises a plurality of terminating resistors each having respective resistance values, wherein the control circuit sets the resistance value by selecting at least one of the terminating resistors and applying it to the terminal of the respective memory chip.

13. (Currently Amended) The ~~memory~~ system of claim 12, further comprising:
a configuration unit configured to set the resistance values of the plurality of terminating resistors.

14. (Currently Amended) The ~~memory~~ system of claim 11, wherein the termination circuit comprises a settable terminating resistor, and further comprising:
a setting circuit configured to selectively output a setting value on the basis of which the terminating resistor is set to the resistance value.

15. (Currently Amended) The ~~memory~~ system of claim 11, further comprising:
a termination port to receive a termination signal, wherein the control circuit ~~being~~ is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal.

16. (Currently Amended) The ~~memory~~ system of claim 15, wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

17. (Currently Amended) The ~~memory~~ system of claim 11, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

18. (Currently Amended) The ~~memory~~ system of claim 17, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

19. (Currently Amended) The ~~memory~~ system of claim 18, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal of the respective memory chip, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal of the respective memory chip.

20. (Currently Amended) The ~~memory~~ system of claim 11, further comprising:
a command decoder operable, as a function of the received control command signal, to communicate to the control circuit whether the resistance value is to be set to a first value or a second value.

21. (Original) A method for operating a memory chip, comprising:

receiving a control command signal for affecting accessibility of the memory chip;
setting a resistance value for a terminal as a function of the control command
signal; and
terminating the terminal with the resistance value.

22. (Original) The method of claim 21, wherein setting the resistance value
comprises selecting a setting value for a settable terminating resistor.

23. (Original) The method of claim 21, wherein setting the resistance value
comprises selecting from a plurality of terminating resistors connected to the terminal.

24. (Original) The method of claim 21, further comprising:
receiving a termination enable signal, the presence of which is required for the
terminating to occur.

25. (Original) The method of claim 24, wherein terminating comprises at least
one of: beginning the terminating after a first time delay relative to the termination
enable signal and stopping the terminating after a second time delay relative to the
termination enable signal, the first time delay being selected such that the selected
terminating resistor can be set.

26. (Original) The method of claim 25, further comprising:
changing the resistance value after a predetermined first switchover time relative
to receiving a predetermined command represented by the control command signal;
and
terminating the terminal with the changed resistance value.

REMARKS

The Applicants request that the Examiner enter the amendment prior to examining the application. Claims 1, 5 and 11-20 have been amended to more clearly claim aspects of the invention and do not constitute new matter.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

/Gero G. McClellan, Reg. No. 44,227/

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Facsimile: (713) 623-4846
Attorney for Applicants

Electronic Acknowledgement Receipt

EFS ID:	2416726
Application Number:	11461380
International Application Number:	
Confirmation Number:	3530
Title of Invention:	MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP
First Named Inventor/Applicant Name:	Georg Braun
Customer Number:	46798
Filer:	Gero G. McClellan/Karla Marquez
Filer Authorized By:	Gero G. McClellan
Attorney Docket Number:	INFN/WB0310
Receipt Date:	02-NOV-2007
Filing Date:	31-JUL-2006
Time Stamp:	10:37:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		INFNWB0310_PreliminaryAmendment.pdf	66369 2e20a24cf8e81307835d4713d928a56c14534f8e	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Preliminary Amendment	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	7

Warnings:

Information:

Total Files Size (in bytes):	66369
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET Substitute for Form PTO-1360 (For use with Form PTO/SB/06)				Application Number 11/461,380		Filing Date 31 July, 2006		☐ To be Mailed					
				Applicant(s) BRAUN ET AL.				Page 1 of 1					
* May be used for additional claims or amendments													
CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SEC. AMENDMENT		*			*		*	
	Indep	Depend	Indep	Depend	Indep	Depend		Indep	Depend	Indep	Depend	Indep	Depend
1	1						51						
2		1					52						
3		1					53						
4		1					54						
5		1					55						
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47							97						
48							98						
49							99						
50							100						
Total Indep	3						Total Indep						
Total Depend		23					Total Depend						
Total Claims	26						Total Claims						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Part of Paper No20071108-1.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/461,380		Filing Date 07/31/2006		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL					
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	11/01/2007	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 26	Minus	** 26	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	=	X \$ =	OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))							OR			
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))							OR			
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
David Sasfai

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/461,380	07/31/2006	Georg Braun	INFN/WB0310

CONFIRMATION NO. 3530

46798
PATTERSON & SHERIDAN, LLP
Gero McClellan / Infineon / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

Title: MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP

Publication No. US-2007-0035326-A1

Publication Date: 02/15/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 703-305-3028.

Pre-Grant Publication Division, 703-605-4283

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OCT 16 2006

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Alexandria, Virginia 22313-1430
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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/461,380	07/31/2006	Georg Braun	INFN/WB0310

CONFIRMATION NO. 3530

FORMALITIES
LETTER

48798
PATTERSON & SHERIDAN, LLP
Gero McClellan / Infineon Technologies
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

Date Mailed: 08/17/2006

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$ 300 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is unsigned.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of \$300 as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$1430 for a non-small entity

10/18/2006 CNGUYEN2 00000008 200782 11461380

01 FC:1011	300.00 DA
02 FC:1111	500.00 DA
03 FC:1311	200.00 DA
04 FC:1051	130.00 DA
05 FC:1202	300.00 DA

- \$300 Statutory basic filing fee.
- \$130 Surcharge.

OCT 16 2006

- The application search fee has not been paid. Applicant must submit \$500 to complete the search fee.
- The application examination fee has not been paid. Applicant must submit \$200 to complete the examination fee for a non-small entity.
- Total additional claim fee(s) for this application is \$300
 - \$300 for 6 total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

K. Lee
Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
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002/011

OCT 16 2006

PATENT
W&B Ref. No.: QIM 3530-US
Attorney Docket No.: INFN/WB0310

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Georg Braun et al.

Serial No.: 11/461.380

Confirmation No.: 3530

Filed: July 31, 2006

For: **MEMORY CHIP AND METHOD
FOR OPERATING A MEMORY
CHIP**

١٠٠

Group Art Unit: 2819

Examiner: Unknown

MAIL STOP MISSING PARTS
Commissioner for Patents
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Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop MISSING PARTS, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office to fax number 571-273-8300, or electronically transmitted via EFS-Web, on the date shown below:

October 16, 2006
Date

Joseph Jorjo

RESPONSE TO NOTICE TO FILE MISSING PARTS

Applicants file this Response to a Notice to File Missing Parts (Form PTO-1533), within the two-month period set to expire on October 17, 2006. The notice (copy enclosed) indicates that the application was filed without the required fees and without a signed oath or declaration.

Enclosed for filing in the above-referenced application are an authorization for payment of the required fees and a signed Declaration for Patent Application, Power of Attorney & Designation of Correspondence Address in response to the missing parts request.

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PATENT
W&B Ref. No.: QIM 3530-US
Attorney Docket No.: INFN/WB0310

The Commissioner is hereby authorized to charge a total of \$1430 as payment of fees due and the surcharge associated with this Communication and Response, or credit any overpayment, to:

Deposit Account No. 20-0782 / INFN/WB0310 / GGM.

Respectfully submitted,



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Facsimile: (713) 623-4846
Attorney for Applicant(s)

**PATTERSON &
SHERIDAN, LLP**

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DATE: October 16, 2006
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COMPANY: USPTO
FROM: Gero G. McClellan / Joseph M. Jong
PAGE(S) with cover: 11
RE:
TITLE: **MEMORY CHIP AND METHOD FOR OPERATING A
MEMORY CHIP**
U.S. SERIAL NO.: 11/461,380
FILING DATE: July 31, 2006
INVENTOR(S): Georg Braun et al.
EXAMINER: unknown
GROUP ART UNIT: 2819
CONFIRMATION NO.: 3530

Attached are the following document(s) for the above-referenced application:

1. Response to Notice to File Missing Parts with authorization to charge
Deposit Account No.: 20-0782 / INFN/WB0310 / GGM
2. Copy of Notice to File Missing Parts
3. Signed Declaration

CONFIDENTIALITY NOTE

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W&B Ref. No.: QJM 3530-US
 Attorney Docket No.: INFN/WB0310

**DECLARATION FOR PATENT APPLICATION,
 POWER OF ATTORNEY &
 DESIGNATION OF CORRESPONDENCE ADDRESS**

As below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP

the specification of which (check one)

☐ is attached hereto.

☒ was filed on July 31, 2006 as Attorney Docket No. INFN/WB0310,
 Application Serial No. 11/461,380.

I hereby state that I have reviewed and understand the contents of the above-identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to the patentability of this application in accordance with 37 CFR §1.56(a).

**PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS
 FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS
 UNDER 35 U.S.C. § 119(a)-(d)**

I hereby claim foreign priority benefits under 35 USC § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
DE 10 2005 035 780.6	GERMANY	29 July 2005	X	
DE 10 2005 036 528.0	GERMANY	3 August 2005	X	

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W&B Ref. No.: QIM 3530-US
Attorney Docket No.: INFNWB0310**CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(35 U.S.C. § 119(e))**

I hereby claim the benefit under Title 35, United States Code, § 119 (e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date

**CLAIM FOR BENEFIT OF EARLIER US/PCT APPLICATION(S)
UNDER 35 U.S.C. § 120**

I hereby claim the benefits under 35 USC § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 USC § 112, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Appl. No.	Filing Date	Patented, Pending, Abandoned

Power of Attorney: As a named inventor, I hereby appoint the practitioners under Customer Number

46798

jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent(s), to transact all business in the United States Patent and Trademark Office connected therewith and to act on my behalf before the competent International Authorities in connection with any and all international applications filed.

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W&B Ref. No.: QIM3530-US
Attorney Docket No.: INFNAW60310

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under 18 USC §1001 and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of First Inventor:	Georg Braun	
Inventor's Signature:	<i>Georg Braun</i>	Date: <i>Sept 18, 2006</i>
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Citizenship:	Germany	
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Full Name of Second Inventor:	Christian Weis	
Inventor's Signature:		Date:
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Citizenship:	Germany	
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Full Name of Third Inventor:	Eckehard Plaettner	
Inventor's Signature:		Date:
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Citizenship:	Germany	
Mailing Address:	Same	

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W&B Ref. No.: QIM 3530-US
Attorney Docket No.: INFNWB0310**DECLARATION FOR PATENT APPLICATION,
POWER OF ATTORNEY &
DESIGNATION OF CORRESPONDENCE ADDRESS**

As below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

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MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP

the specification of which (check one)

_____ is attached hereto.

X was filed on July 31, 2006 as Attorney Docket No. INFNWB0310,
Application Serial No. 11/481,380.

I hereby state that I have reviewed and understand the contents of the above-identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to the patentability of this application in accordance with 37 CFR §1.56(a).

**PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS
FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS
UNDER 35 U.S.C. § 119(a)-(d)**

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W&B Ref. No.: QM 3530-US
 Attorney Docket No.: INFNWB0310

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(35 U.S.C. § 119(e))

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Provisional Application Number	Filing Date

CLAIM FOR BENEFIT OF EARLIER US/PCT APPLICATION(S)
UNDER 35 U.S.C. § 120

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Appl. No.	Filing Date	Patented, Pending, Abandoned

Power of Attorney: As a named inventor, I hereby appoint the practitioners under Customer Number

46798

jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent(s), to transact all business in the United States Patent and Trademark Office connected therewith and to act on my behalf before the competent International Authorities in connection with any and all international applications filed.

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W&B Ref. No.: QIM 3530-US
Attorney Docket No.: INFN/WB0310

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under 18 USC §1001 and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of First Inventor:	Georg Braun	
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Full Name of Second Inventor:	Christian Weis	
Inventor's Signature:	<i>Christian Weis</i>	Date: 22.08.2006
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Mailing Address:	Same	

Full Name of Third Inventor:	Eckehard Flaettner	
Inventor's Signature:	<i>Eckehard Flaettner</i>	Date: 22.8.2006
Residence:	Bachweg 3 82041 Oberhaching, Germany	
Citizenship:	Germany	
Mailing Address:	Same	



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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/461,380	07/31/2006	Georg Braun	INFN/WB0310

CONFIRMATION NO. 3530

FORMALITIES
 LETTER

46798
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 SUITE 1500
 HOUSTON, TX 77056

Date Mailed: 08/17/2006

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

*Filing Date Granted***Items Required To Avoid Abandonment:**

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$ 300 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is unsigned.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **\$300** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$1430** for a non-small entity

- **\$300** Statutory basic filing fee.
- **\$130** Surcharge.

- The application search fee has not been paid. Applicant must submit \$500 to complete the search fee.
- The application examination fee has not been paid. Applicant must submit \$200 to complete the examination fee for a non-small entity.
- Total additional claim fee(s) for this application is \$300
 - \$300 for 6 total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

JL. Lee

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199, or 1-800-972-6382
PART 3 - OFFICE COPY

MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number DE 10 2005 035 780.6, filed 29 July 2005. This application also claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number DE 10 2005 036 528.0, filed 3 August 2005. Each of these related patent applications is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The following description relates to a memory chip having a terminal for sending and/or receiving high-frequency signals. The description further relates to a method for operating a memory chip.

Description of the Related Art

[0003] In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller. However, during transmission of high-frequency signals, signal reflections that disturb the data transmission on the memory bus and thereby limit the data transmission rates can occur at the terminals of the memory chips. It is necessary for this reason when transmitting data via the memory bus to provide suitable terminations at the terminals of the memory chips in order to reduce the signal reflections on the signal lines.

[0004] It has previously been provided in the case of memory chips to switch the termination on or off at a terminal of the memory chip as a function of a termination signal. That is to say, the memory controller makes a suitable

termination signal available to each of the memory chips in order to support the following read, write or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus. The disadvantage of such a control of the memory chips consists in that switching the terminating resistors on and off is not sufficient as a rule to achieve an optimal termination in every operating state, and thus, also not sufficient to improve the data transmission via the memory bus.

[0005] Furthermore, it can be provided that the strength of the terminating resistors in the memory chips is fixed in accordance with a configuration value that is communicated to the memory chips by the memory controller in an initialization phase at the beginning of the operation of the memory system. Setting the configuration values in the memory chips before each write and read operation is time consuming. Consequently, the initial presetting of the terminating resistor by the configuration value is also not suitable for providing terminating resistors for applying to the memory bus that are suitable for every case of addressing the memory chips of the memory system, since the access time in the memory system would thereby be slowed down substantially.

SUMMARY OF THE INVENTION

[0006] According to a one aspect, a memory chip is provided for setting various terminations on a signal line of the data bus. The memory chip comprises a terminal, a termination circuit which is connectable to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination circuit in order to set the resistance value as a function of a received control command signal and to make the resistance value available at the terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the

invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0008] Figure 1 shows a block diagram of a memory chip in accordance with a first embodiment;

[0009] Figure 2 shows a block diagram of a memory chip in accordance with a further embodiment;

[0010] Figure 3 shows a signal-time diagram that illustrates the functionality of the embodiments of Figure 1 and Figure 2 given the presence of no operation affecting the memory chip;

[0011] Figure 4 shows a signal-time diagram for illustrating the functionality of the embodiments of Figures 1 and 2 that illustrates the carrying out of a write operation; and

[0012] Figure 5 shows a signal-time diagram for illustrating the functionality of the embodiments of Figures 1 and 2 that illustrates the carrying out of a write operation in conjunction with an activated termination signal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0013] A memory chip 1 is illustrated in Figure 1 as a block diagram. The memory chip 1 comprises a memory cell array 2, such as, for example, a DRAM memory cell array, that can be written to and read from via a logic circuit 3. The logic circuit 3 comprises driver circuits as well as input amplifiers and output drivers (not shown). The logic circuit 3 is connected to an external terminal 4 of the memory chip 1 via which, for example, address, clock and user data can be read in or driven out.

[0014] The external terminal 4 is connected to a termination circuit 5 that has a first settable terminating resistor 6 with a first resistance value, and a second

settable terminating resistor 7 with a second resistance value. The termination circuit 5 is connected to a control unit 8 that makes available to the termination circuit 5 a first control signal TermTime0, and a second control signal TermTime1. Upon activation of the first control signal TermTime0, the first terminating resistor 6 is connected to the external terminal 4 such that the external terminal 4 is terminated with the first resistance value set accordingly in the first terminating resistor 6. Upon activation of the second control signal TermTime1, the second terminating resistor 7 is correspondingly connected to the first terminal such that the external terminal 4 is terminated with the second resistance value. Furthermore, given simultaneous activation of the two control signals TermTime0, TermTime1, it is also possible to generate a further resistance value for termination that results from the parallel connection of the first and second resistance values.

[0015] Further provided is a configuration unit 9 that makes available a first configuration value TS0 and a second configuration value TS1. The first configuration value TS0 is connected to the first terminating resistor 6, and the second configuration value is connected to the second terminating resistor 7 in order to set the respective resistance value of the corresponding terminating resistor 6, 7. The configuration values TS0, TS1 can be made available in parallel via configuration signals. As a function of the respective control signal TermTime0, TermTime1, the corresponding terminating resistor 6, 7, whose resistance value is provided by the respective configuration value TS0, TS1, is then connected to the external terminal 4.

[0016] A settable terminating resistor can be achieved, for example, by switchable, parallel-connected resistors. It is also possible to implement the resistors by means of transistors with the same or different channel width that are completely or partially switched through. The terminating resistors can be fashioned such that the respective control signal TermTime0, TermTime1 is logically combined with each of the bits of the configuration value TS0, TS1 made available by means of AND operation, and the respective logic results are connected to the inputs of transistors provided in the terminating resistor.

[0017] Via an external termination port 13, the control unit 8 receives a termination enable signal TermEn that indicates whether or not a termination is to be provided at the external terminal 4. That is to say, via the first and the second control signal TermTime0, TermTime1, the respective terminating resistor 6, 7 is connected to the external terminal 4 only when the termination signal TermEn specifies that there is to be a termination. Otherwise, no termination of the external terminal 4 is undertaken.

[0018] Which of the two terminating resistors 6, 7 is connected to the external terminal 4 is specified as a function of a command signal BS that is made available by a command decoder 10, as a function of a received control command CMD. Via one or more external control command ports 11, the command decoder 10 receives control command signals CMD for activating, addressing and/or driving the memory chip 1.

[0019] The control command signals CMD can assume an active or inactive state. If the memory chip 1 is a DRAM memory chip, the control command signals can be, for example, the chip select signal CS for selecting the relevant memory chip for a specific operation, the write enable signal WE for enabling a write access to the memory chip, the RAS signal (row activation signal) for transmitting the word line address and for activating the word line, as well as the CAS signal (column activation signal) for transmitting the bit line address and for activating the bit line for reading data out and/or writing them into the memory cell field. Depending on whether the relevant memory chip in a memory system is or is not selected for an operation, or whether the aim is to carry out writing or reading on the relevant memory chip (write enable signal), only one of the two terminating resistors 6, 7 or none of the two terminating resistors can be selected (under the control of the termination signal) in order to terminate the external terminal 4 in a suitable way.

[0020] Figure 2 shows another embodiment of a memory chip 1. Like functions or components relative to Figure 1 are identified by like reference numbers or labels. The embodiment of Figure 2 differs from the embodiment of Figure 1 in that a setting unit 15 is provided that has the configuration unit 9 and a

multiplexer 12. A termination selection signal TermSel made available by the control unit 8 is connected to a control input of the multiplexer 12. The termination selection signal TermSel is used to select which of the configuration values TS0, TS1 made available by the configuration unit 9 is connected to the termination circuit 5. In this embodiment, the termination circuit 5 comprises only one settable terminating resistor 6 whose resistance value is set as a function of the selected configuration value TS0, TS1. The sole terminating resistor 6 is now activated or deactivated, and thereby connected to the external terminal 4 or not as a function of the single control signal TermTime0, which is made available by the control unit 8.

[0021] The magnitude of the resistance value of the terminating resistor 6 is determined by the termination selection signal TermSel with the aid of which one of the configuration values TS0, TS1 is selected. By contrast with the embodiment of figure 1, it is possible in the case of this embodiment to dispense with a second settable terminating resistor and instead of this to select the single settable terminating resistor in accordance with a configuration value that can be selected via the multiplexer 12, doing so as a function of the current control command signals. A combination of various terminating resistors that are simultaneously connected to the external terminal 4, as shown in figure 1, is therefore not possible, but chip area can be saved since only one settable terminating resistor 6 is required.

[0022] Figure 3 shows a signal-time diagram for explaining the signal profile for setting the termination in an inventive memory chip. Specified in the signal-time diagram of Figure 3 is a case where the goal is to switch on a termination when the command control signal specifies that the relevant memory chip is not activated, that is to say no access to the memory chip is to be carried out (chip select signal deactivated). After a predetermined termination switch-on time ODTLon of, in this example, three clock periods, a desired first resistance value RTT_Nom (DRAM_RTT) is connected to the external terminal 4 in a fashion triggered by the activation of the termination signal TermEn by the memory controller and by a rising edge of a clock signal CK at an instant T0. After

deactivation of the termination signal TermEn during the fifth clock period T5, the next rising edge of the clock signal T6 starts a predetermined termination switch-off time ODTLoff that amounts in this exemplary embodiment to three and a half clock periods, and after the elapse thereof the terminating resistor is disconnected from the external terminal 4. The time durations of the termination switch-on time ODTLon and of the termination switch-off time ODTLoff can be selected as desired, and should be selected such that they suffice to connect the terminating resistor reliably to the external terminal 4, or to disconnect it therefrom. That is to say, they should at least have the time duration required for switching a terminating resistor on or off, or for connecting and disconnecting the terminating resistor from the external terminal 4.

[0023] For example, given a deactivated chip select signal, that is to say when no operation is to be carried out in the memory chip, it is possible for the termination of the external terminal 4 to be undertaken or not, and this is controlled in a memory system by the memory controller issuing the termination signal TermEn. At the same time, it is established by the decoder 10 of the memory chip that the chip select signal CS is deactivated and as a function of the chip select signal CS an appropriate configuration value or control signal (according to the particular embodiment) is connected to the termination circuit 5 in order to connect the selected terminating resistor 6, 7 (Figure 1) or 6 (Figure 2) to the external terminal 4, doing so as a function of the termination signal TermEn.

[0024] Figure 4 illustrates a further signal-time diagram for the embodiment of figures 1 and 2. The signal-time diagram of figure 4 exhibits a case in which the corresponding memory chip is activated by the chip select signal CS, and a write command (WE-Signal) WRS8 is sent to the memory chip by the memory controller. The memory controller may assert the termination signal TermEn and the write signal WRS8 such that they can be accepted into the memory chip by a rising clock edge at an instant T12. The command decoder decodes the write signal WRS8 and generates the command signal BS, which is applied to the control unit 8. Depending on the command signal BS, it is established in the control unit 8 that it is now necessary to connect to the external terminal 4 a

terminating resistor that is determined by the second configuration value. In the case of the embodiment of Figure 1, the control unit 8 therefore activates the second control signal TermTime1 in order to activate the second terminating resistor 7. In the embodiment of Figure 2, the control unit 8 switches the termination selection signal TermSel such that the multiplexer 12 connects the second configuration value to the termination circuit 5 in order to set there the resistance value of the terminating resistor 6 to the corresponding value, in this case to a second resistance value RTT_WR that corresponds to the terminating resistor that is to be connected to the activated memory chips in the event of a write access to the external terminal 4.

[0025] Depending on the termination signal TermEn the terminating resistor is now connected to the external terminal 4 after the termination switch-on time ODTLon, the terminating resistor now being a different one, depending on the control command signal, as previously in the case of the deactivated memory chip (figure 3). The write latency time duration WL, which amounts to 5 clock periods in the exemplary embodiments shown, begins to run at the same time as the reception of the write command WRS8. The data strobe signal DQS can be read into the memory chip at the same time as the data in terms of one clock period before the transmission of a data burst, that is to say transmission of 8 data bits. The termination switch-on time ODTLon may be selected to be equal to or less than the write latency time duration WL in order to ensure that the desired terminating resistor is connected to the external terminal 4 during transmission of data to the memory chip (during write access).

[0026] In general, the command signal BS is generated in the command decoder 10 such that it specifies to the control unit 8 which resistance value, RTT_Nom or RTT_WR, is to be set as terminating resistor for the terminal. In the case of a first group of control commands CMD that are present, the command decoder 10 outputs a command signal BS to the control unit 8 which specifies that a termination needs to be undertaken with the first resistance value RTT_Nom (with the termination signal TermEn activated), and in the case of a second group of control commands the command decoder 10 outputs a command signal BS to

the control unit 8 which specifies that the terminal 4 is to be terminated with a second resistance value (with the termination signal TermEn activated). The first group of control commands can comprise control commands that, for example, indicate a deactivation of the integrated circuit, or a read access to the integrated memory circuit, while the second group of control commands can indicate write commands to the integrated memory circuit.

[0027] The time duration between the applying of a control command signal or between the making available of the command signal BS to the control unit 8 and changes, dependent thereon, to the resistance value in the termination circuit 5 may be established as first switchover time ODTLCNW that may be equal to or less than the termination switch-on time ODTLon.

[0028] In general, the control unit 8 may essentially switch on simultaneously the termination and the corresponding setting of the terminating resistor to the corresponding resistance value. Furthermore, it is likewise possible for the termination to be switched off and the resistance value to be changed simultaneously.

[0029] Furthermore, it can be provided, for example, when a control command of the second group of control commands is present that after the lapse of a second switchover time ODTLCWN the control unit 8 changes the termination of the second resistance value to the first resistance value irrespective of whether the termination signal TermEn provides a termination or not. The second switchover time ODTLCWN corresponds at least to a time duration that is determined by the ending of the write access or by the ending of an access to the memory chip that is triggered by a control command of the second group of control commands. In the case of a burst write access as described in conjunction with figure 4, the second switchover time should be a function of the write latency time WL and of the time duration for the burst access. Alternatively, the second switchover time can also be set as a function of the end of a data transfer from and to the memory chip 1. The second switchover time ODTLCBM may be the sum of the write latency WL, and the duration of the burst access (burst length/2* clock cycle length TCK) plus a safety period ($1/2 * TCK$ or a multiplier thereof). It is

possible in this way for the second resistance value RTT_WR for terminating the terminal to be made available for terminating the terminal only for a specific time duration as a function of a control command CMD that is present, the terminal being terminated again after the elapse of this time duration with the first resistance value if the latter is specified by the termination signal $TermEn$.

[0030] Referring to Figure 5, an embodiment, is shown in which the termination signal $TermEn$ permits the termination of the terminal 4 to be switched on before, during and after a write access $WRS4$, the termination being set before the write access to the first resistance value RTT_Nom . After the elapse of the first switchover time $ODTLCNW$ the terminal 4 is terminated with the resistance value RTT_WR , and after the elapse of the second switchover time $ODTLCWN$, the termination is switched back again to the first resistance value RTT_Nom .

[0031] While in the exemplary embodiment shown in Figure 1 only two different terminating resistors can be connected to the external terminal 4, the number of different settable terminating resistors can, however, be as high as desired. Accordingly, different terminating resistors can be connected to the external terminals for different accesses in a memory system in which the memory chip is operated.

[0032] According to one aspect of the invention, during the operation of the memory chips in a memory system the terminating resistors can be specifically set for each of the memory chips as a function of the operation currently being carried out. Thus, it is possible to provide different terminating resistors that can individually, or else in combination, be connected to the external terminal. It can be possible, in addition, to apply a terminating resistor to the external terminal as a function of a termination signal $TermEn$.

[0033] In summary, a memory chip for setting various terminations is provided on a signal line of the data bus. The memory chip comprises a terminal, a termination circuit that can be connected to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination

circuit in order to set the resistance value as a function of a received control command signal and to make it available at the terminal.

[0034] The memory chip renders it possible to set a resistance value of the termination circuit as a function of a control command connected to the memory chip, and to terminate the terminal in an improved way such that the data transmission via the memory bus, which can be connected to the memory chip in a memory system, is supported in an optimal way. It is possible in this way to set the terminating resistor directly as a function of the operation of the memory system without the need to store a configuration value in the memory chip immediately before carrying out the operation by a corresponding setting operation controlled by the memory controller. It is advantageous that the setting of the respective termination need not be controlled by a memory controller of the memory system, but is prescribed by the control command signals in the memory system.

[0035] The termination circuit can further have a number of terminating resistors in order to provide a number of various resistance values, the control circuit being fashioned in order to select at least one of the terminating resistors and apply it to the terminal. By providing the number of the terminating resistors in the memory chip, the corresponding terminating resistors can be selected relatively quickly such that there is no, or no substantial time loss in carrying out the operation in the memory system.

[0036] In accordance with a further embodiment, a configuration unit is provided in order to set the resistance values of the number of terminating resistors. It is thereby possible to preselect the resistance values with which the terminal can be terminated.

[0037] In accordance with a further embodiment, the termination circuit can comprise a settable terminating resistor, a setting circuit being provided in order to make available as a function of a selection signal a setting value with the aid of which the resistance value of the terminating resistor is determined.

[0038] The memory chip further has a termination port in order to receive a termination signal, the control circuit being connected to the termination circuit in order, as a function of the termination signal either to terminate the terminal with the set resistance value, or not to terminate the terminal. It is possible in this way optionally also not to provide any termination at the terminal when this is prescribed by the memory controller and/or a control command.

[0039] The control circuit can further be connected to the termination circuit in order as a function of the termination signal to terminate the terminal with the set resistance with a first time delay in each case, or not to terminate it in accordance with a second time delay, the first time delay sufficing in order to set the resistance value. The first and the second time delays can be the same or different.

[0040] The control unit can further be fashioned such that the resistance value is set to a specific second resistance value as a function of the presence of a control command signal after a predetermined first switchover time and/or is set to a specific first resistance value after a predetermined second switchover time.

[0041] In accordance with a further embodiment, the control circuit sets the first switchover time as a function of the first time delay, and/or sets the second switchover time as a function of the second time delay.

[0042] In particular, the control unit can be fashioned such that the resistance value is set to the second resistance value in a fashion substantially simultaneous with the appliance of the termination at the terminal, and/or is set to the first resistance value in a fashion substantially simultaneous with the ending of the termination of the terminal.

[0043] In accordance with a further embodiment, a command decoder can be provided in order as a function of a control command signal that is present to communicate to the control unit whether a first or a second resistance value is to be set for termination.

[0044] In accordance with a further aspect, a memory system is provided having a memory controller, with a number of inventive memory chips and having a memory bus to which the memory controller and the memory chips are connected, the memory bus comprising a signal line that interconnects the terminals of the memory chips and a terminal of the memory controller.

[0045] In accordance with a further aspect, a method is provided for operating a memory chip in the case of which a control command signal is received, in which a terminal is terminated with a settable resistance value, and the resistance value is set as a function of the received control command signal, and the terminal is terminated with the set resistance value. It is possible in this way to set the terminating resistor, which is connected to a terminal of a memory chip, as a function of a control command such that it is possible during operation of the memory chip in a memory system to set the termination suitable for operations to be carried out at each of the memory chips in order to reduce signal reflections on the lines of the memory bus, and thus to increase the possible data transmission rate. It is also advantageous that the setting of the resistance value can be carried out without providing further signals to be connected from outside.

[0046] The resistance value can further be set by the selection of a setting value for a settable terminating resistor.

[0047] The method further includes setting the resistance value by selection from a number of terminating resistors that are connected to the terminal.

[0048] In accordance with a further embodiment, it is possible to receive a termination signal and, as a function of the termination signal, either the terminal with the set resistance value is terminated, or the terminal is not terminated.

[0049] In accordance with a further embodiment, it is possible as a function of a change in level of the termination signal either to switch on the termination with the set resistance value with a time delay, or to switch off the termination with the time delay, the time delay being selected such that the selected terminating resistor can be set.

[0050] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

WHAT IS CLAIMED IS:

1. A memory chip for variably setting terminations, comprising:
 - a terminal;
 - a termination circuit in coupled to the terminal and configured to terminate the terminal according to a settable resistance value;
 - a control command port for receiving a control command signal for affecting accessibility of the memory chip; and
 - a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal.
2. The memory chip of claim 1, wherein the termination circuit comprises a plurality of terminating resistors each having respective resistance values, wherein the control circuit sets the resistance value by selecting at least one of the terminating resistors and applying it to the terminal.
3. The memory chip of claim 2, further comprising:
 - a configuration unit configured to set the resistance values of the plurality of terminating resistors.
4. The memory chip of claim 1, wherein the termination circuit comprises a settable terminating resistor, and further comprising a setting circuit configured to output a setting value on the basis of which the terminating resistor is set to the resistance value.
5. The memory chip of claim 1, further comprising:
 - a termination port to receive a termination signal, the control circuit being configured to selectively terminate the terminal with the set resistance value in response to the termination signal.
6. The memory chip of claim 5, wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the

set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

7. The memory chip of claim 6, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

8. The memory chip of claim 7, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

9. The memory chip of claim 8, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal.

10. The memory chip of claim 1, further comprising:
a command decoder operable, as a function of the received control command signal, to communicate to the control circuit whether the resistance value is to be set to a first value or a second value.

11. A memory system, comprising:
(a) a memory controller having terminal;
(b) a plurality of memory chips; at least one of the memory chips comprising:
a terminal;
a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;
a control command port for receiving a control command signal for affecting accessibility of the memory chip; and

a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller.

12. The memory system of claim 11, wherein the termination circuit comprises a plurality of terminating resistors each having respective resistance values, wherein the control circuit sets the resistance value by selecting at least one of the terminating resistors and applying it to the terminal of the respective memory chip.

13. The memory system of claim 12, further comprising:
a configuration unit configured to set the resistance values of the plurality of terminating resistors.

14. The memory system of claim 11, wherein the termination circuit comprises a settable terminating resistor, and further comprising:
a setting circuit configured to selectively output a setting value on the basis of which the terminating resistor is set to the resistance value.

15. The memory system of claim 11, further comprising:
a termination port to receive a termination signal, the control circuit being configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal.

16. The memory system of claim 15, wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

17. The memory system of claim 11, wherein the control circuit is configured

such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

18. The memory system of claim 17, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

19. The memory system of claim 18, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal of the respective memory chip, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal of the respective memory chip.

20. The memory system of claim 11, further comprising:
a command decoder operable, as a function of the received control command signal, to communicate to the control circuit whether the resistance value is to be set to a first value or a second value.

21. A method for operating a memory chip, comprising:
receiving a control command signal for affecting accessibility of the memory chip;
setting a resistance value for a terminal as a function of the control command signal; and
terminating the terminal with the resistance value.

22. The method of claim 21, wherein setting the resistance value comprises selecting a setting value for a settable terminating resistor.

23. The method of claim 21, wherein setting the resistance value comprises selecting from a plurality of terminating resistors connected to the terminal.

24. The method of claim 21, further comprising:
receiving a termination enable signal, the presence of which is required for the terminating to occur.
25. The method of claim 24, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set.
26. The method of claim 25, further comprising:
changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and
terminating the terminal with the changed resistance value.

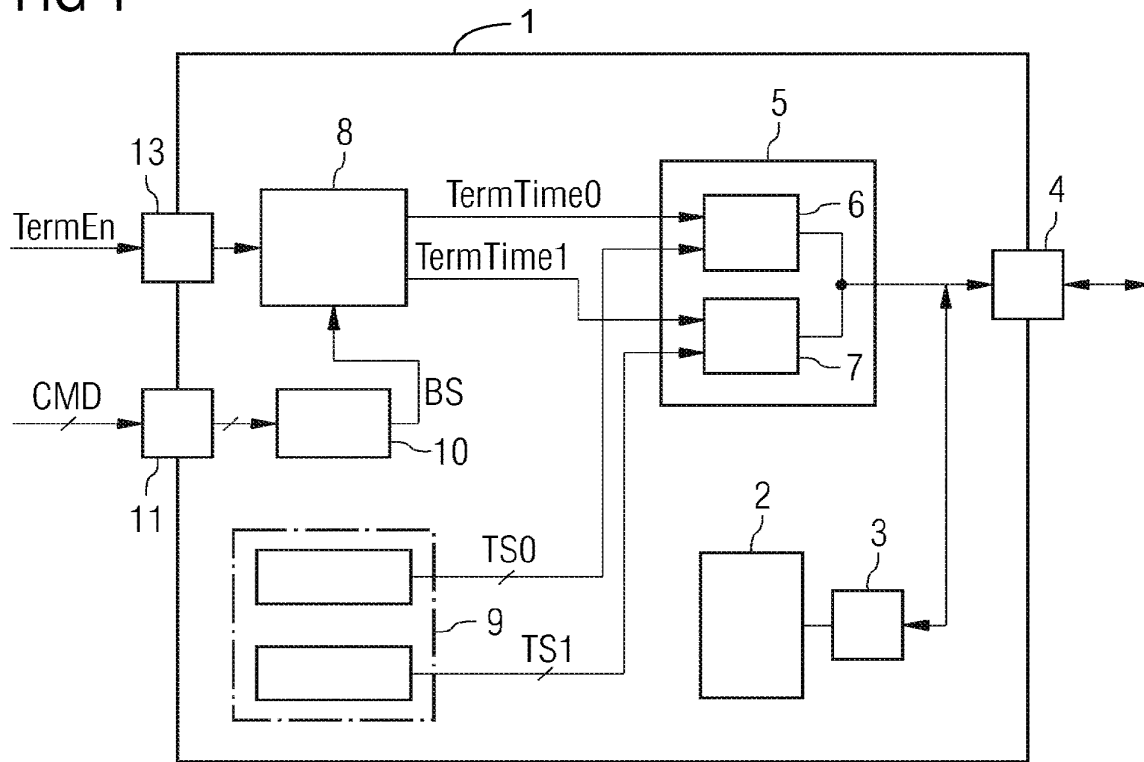
ABSTRACT OF THE DISCLOSURE

Methods and apparatus for setting various terminations of a memory chip. In one embodiment, the memory chip includes a terminal, a termination circuit that can be connected to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination circuit in order to set a resistance value as a function of a received control command signal.

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FIG 1



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FIG 2

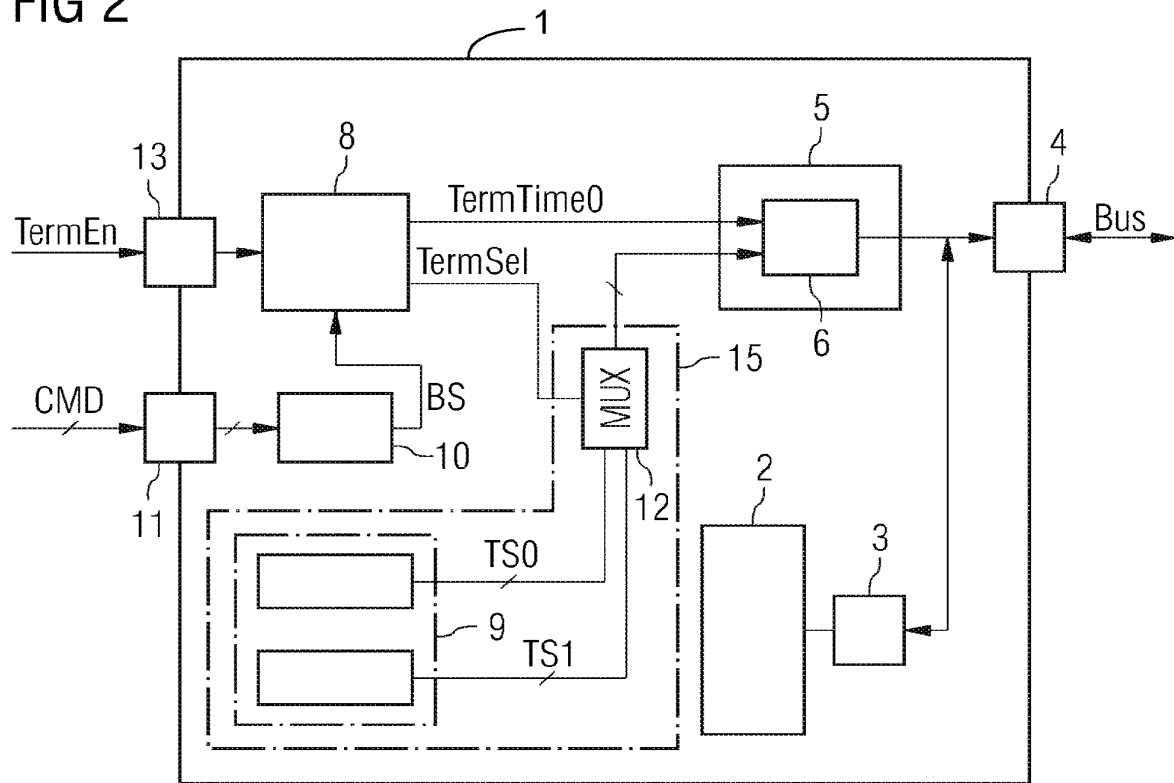
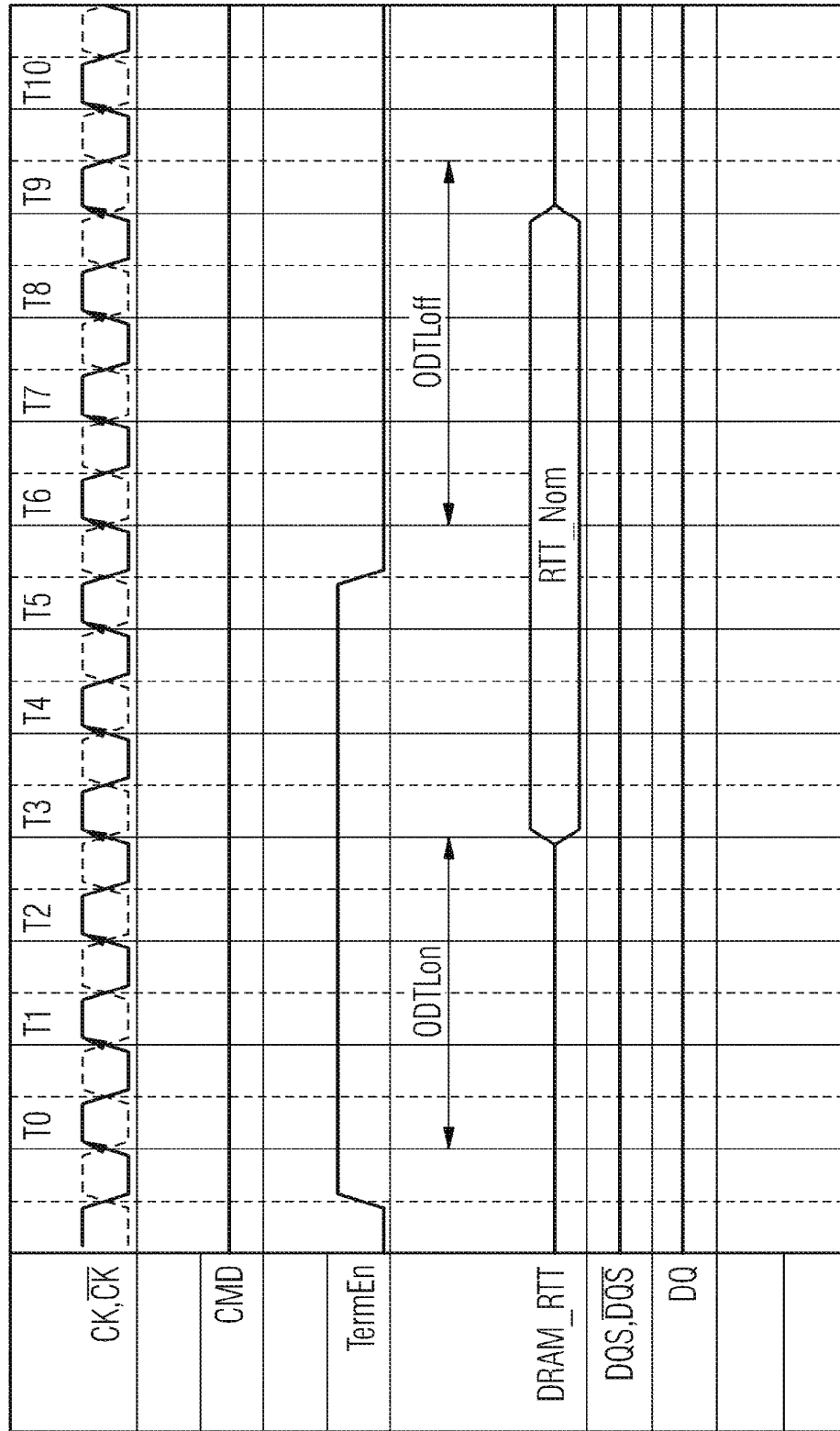
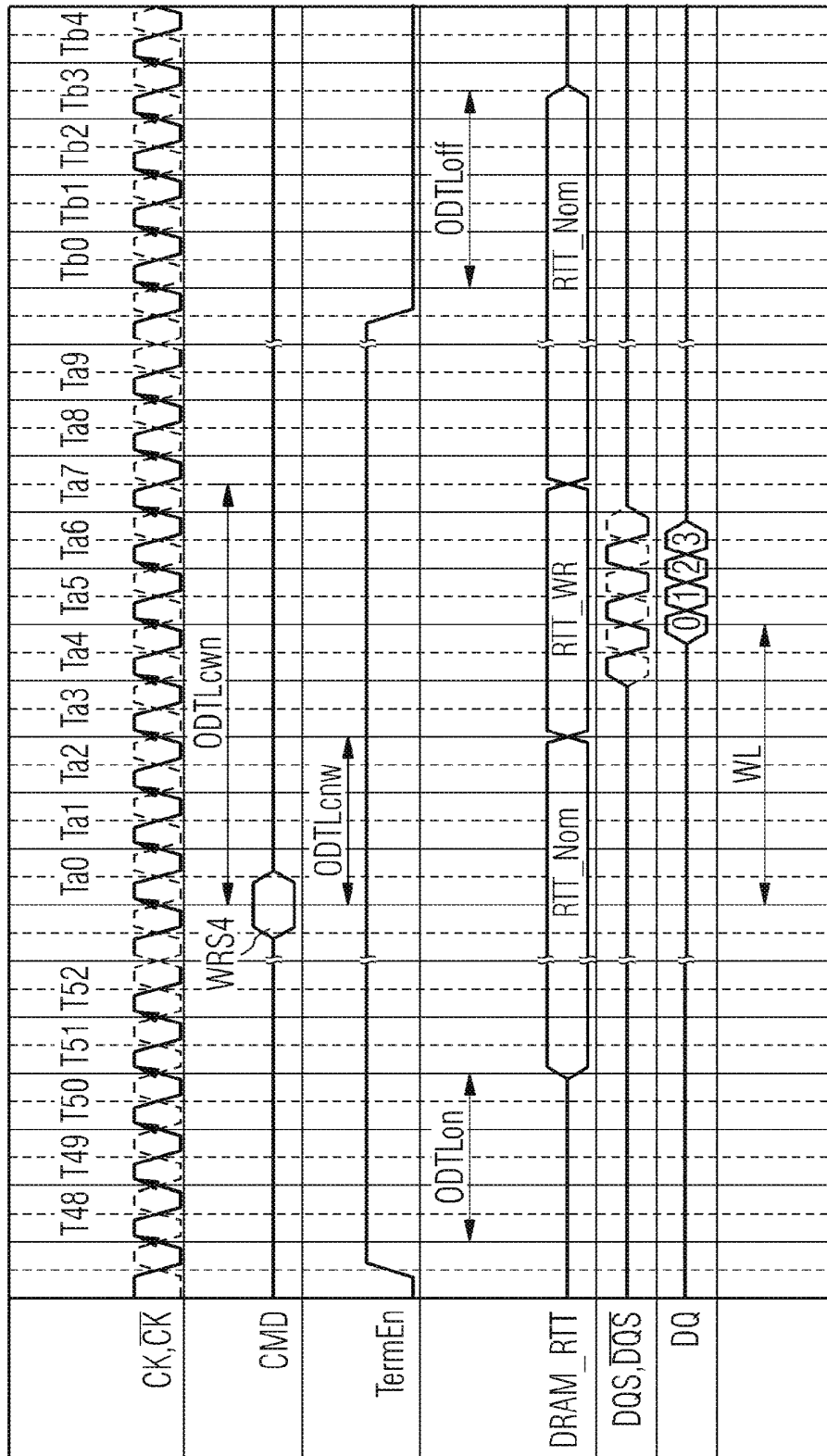


FIG 3



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**DECLARATION FOR PATENT APPLICATION,
POWER OF ATTORNEY &
DESIGNATION OF CORRESPONDENCE ADDRESS**

As below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP

the specification of which (check one)

_____ is attached hereto.

 X was filed on July 31, 2006 as Attorney Docket No. INFN/WB0310,
Application Serial No. unknown.

I hereby state that I have reviewed and understand the contents of the above-identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to the patentability of this application in accordance with 37 CFR §1.56(a).

**PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS
FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS
UNDER 35 U.S.C. § 119(a)-(d)**

I hereby claim foreign priority benefits under 35 USC § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
DE 10 2005 035 780.6	GERMANY	29 July 2005	X	
DE 10 2005 036 528.0	GERMANY	3 August 2005	X	

**CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(35 U.S.C. § 119(e))**

I hereby claim the benefit under Title 35, United States Code, § 119 (e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date

**CLAIM FOR BENEFIT OF EARLIER US/PCT APPLICATION(S)
UNDER 35 U.S.C. § 120**

I hereby claim the benefits under 35 USC § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 USC § 112, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Appl. No.	Filing Date	Patented, Pending, Abandoned

Power of Attorney: As a named inventor, I hereby appoint the practitioners under Customer Number

46798

jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent(s), to transact all business in the United States Patent and Trademark Office connected therewith and to act on my behalf before the competent International Authorities in connection with any and all international applications filed.

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I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under 18 USC §1001 and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	MEMORY CHIP AND METHOD FOR OPERATING A MEMORY CHIP			
First Named Inventor:	Georg Braun			
Filer:	Gero G. McClellan/Joseph Jong			
Attorney Docket Number:	INFN/WB0310			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Claims in excess of 20	1202	6	50	300
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1300

Electronic Acknowledgement Receipt

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Application Number:	11461380
Confirmation Number:	3530
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First Named Inventor:	Georg Braun
Customer Number:	46798
Filer:	Gero G. McClellan/Joseph Jong
Filer Authorized By:	Gero G. McClellan
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Receipt Date:	31-JUL-2006
Filing Date:	
Time Stamp:	19:41:32
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		0310_application.pdf	97580	yes	20

	Multipart Description				
	Doc Desc		Start	End	
	Specification		1	14	
	Claims		15	19	
	Abstract		20	20	
Warnings:					
Information:					
2	Drawings	0310_drawings.pdf	171692	no	5
Warnings:					
Information:					
3	Oath or Declaration filed	0310_declaration.pdf	72306	no	3
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	8453	no	2
Warnings:					
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Total Files Size (in bytes):			350031		
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