

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

DECLARATION OF DR. R. JACOB BAKER

Case No. IPR2022-00513

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

Contents

I.	Introduction.....	1
II.	Background and Qualifications	1
III.	Documents and Materials Considered.....	5
IV.	Relevant Legal Principles	5
V.	Person of Ordinary Skill in the Art.....	10
VI.	'523 Patent	12
	A. Overview	12
	B. Background / Applicant Admitted Prior Art.....	18
	C. Prosecution History	22
	D. Priority Date	23
VII.	Technology Background.....	23
VIII.	Claim Construction.....	27
IX.	Summary of Opinions.....	27
	A. Overview of Bains (EX1005).....	28
	B. Overview of JESD79-2A (EX1006)	31
X.	Claims 1, 2, 5, 6, 9, and 10 are Invalid.....	35
	A. Claims 1, 2, 5, 6, 9, and 10 are Obvious Over Bains	35
	1. Claim 1	36
	2. Claim 2: “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined	

switchover time and is set to a second resistance value after a second predetermined switchover time.”	54
3. Claim 5:.....	62
4. Claim 6: “The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”	68
5. Claim 9	69
6. Claim 10: “The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.”	70
B. Claims 1, 2, 5, 6, 9, and 10 are Obvious Over Bains in Combination with JESD79-2A	73
1. Combination of Bains and JESD79-2A	73
2. Claim 1	81
3. Claim 2: “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”	89
4. Claim 5	89
5. Claim 6: “The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined	

switchover time and is set to a second resistance value
after a second predetermined switchover time.” 92

6. Claim 9 93

7. Claim 10: “The method of claim 9, further
comprising: changing the resistance value after a
predetermined first switchover time relative to receiving
a predetermined command represented by the control
command signal; and terminating the terminal with the
changed resistance value.” 94

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 7,532,523 (“’523 Patent”)
1002	Prosecution History of the ’523 Patent
1003	Declaration of Dr. R. Jacob Baker
1004	Curriculum Vitae of Dr. R. Jacob Baker
1005	U.S. Patent No. 7,433,992 to Bains (“Bains”)
1006	JEDEC STANDARD, Double Data Rate (DDR) 2 SDRAM Specification, JESD79-2A (“JESD79-2A”)
1007	U.S. Patent No. 7,092,299 to Kwak (“Kwak”)
1008	Samuel D., <i>DDR-II: How it Works</i> , X86-SECRET (Sept. 8, 2004), http://www.x86-secret.com/articles/ram/ddr2_667/ddr2667-6en.htm .
1009	U.S. Patent No. 6,754,132 (“Kyung”)
1010	Declaration of Julie Carlson regarding JESD79-2A
1011	First Amended Complaint, <i>Polaris Innovations Ltd. v. Xilinx, Inc.</i> , 1:22-cv-00174-RGA (D. Del. April 28, 2022), ECF No. 14.
1012	Scheduling Order, <i>Polaris Innovations Ltd. v. Xilinx, Inc.</i> , 1:22-cv-00174-RGA (D. Del. May 31, 2022), ECF No. 20
1013	United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf
1014	Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)
1015	JEDEC STANDARD, Configurations for Solid State Memories, JEDEC Standard No. 21-C, Release 14

I. Introduction

1. My name is R. Jacob Baker, Ph.D., P.E. I have prepared this Declaration in connection with Xilinx, Inc.'s Petition for *Inter Partes* Review of U.S. Patent No. 7,532,523 (the "'523 Patent") (EX1001), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the '523 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have been retained by Xilinx, Inc. ("Xilinx" or "Petitioner") as an expert in the fields of computer engineering, computer memory systems, and related technologies. I have been asked to provide my opinion regarding the state of the art of the technology described in the '523 Patent and on the patentability of the claims of this patent. I am being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in Xilinx, the '523 Patent, or the owner of the '523 Patent.

II. Background and Qualifications

4. My professional qualifications, experience, publications, and presentations, as well as a list of previous cases in which I have provided expert testimony, are outlined in my *Curriculum Vitae* (EX1004).

5. I received a Ph.D. in electrical engineering from the University of Nevada, Reno in 1993 and B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas in 1986 and 1988, respectively. I have over 35 years of industry and academic experience, and I am the named inventor on over 150 US patents, many of which are directed to memory systems and components. *See, e.g.,* U.S. Patent No. 8,516,292; U.S. Patent No. 8,395,947; U.S. Patent No. 7,877,623; U.S. Patent No. 7,421,607; U.S. Patent No. 7,237,136; U.S. Patent No. 6,704,88; U.S. Patent No. 9,697,883; U.S. Patent No. 6,026,050.

6. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). I joined UNLV in 2012 after teaching at Boise State University (BSU), where I also served as the electrical and computer engineering (ECE) department chair for three years. Prior to BSU, I worked in the department of electrical engineering at UNLV (1991-1992), and as a professor in the electrical engineering department at the University of Idaho (UI) (1993-2000).

7. While at UNLV, BSU, and UI, I taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit, etc.), linear circuits, microelectronics, communication systems, and fiber optics. I have also advised over 100 graduate students on thesis and non-thesis research projects relating to the above topics.

8. Much of my research has focused on analog and digital integrated circuit design and fabrication. I have authored or co-authored several textbooks on the fundamentals of complementary metal oxide semiconductor (CMOS) and Dynamic Random Access Memory (DRAM) circuit design, including CMOS Circuit Design, Layout and Simulation; CMOS Mixed-Signal Circuit Design; DRAM Circuit Design: Fundamental and High-Speed Topics; and DRAM Circuit Design: A Tutorial. I have also authored or co-authored over 100 papers and presentations in the area of solid-state circuit design.

9. I am a licensed Professional Engineer with extensive industry experience in integrated circuit design and fabrication, including the design and fabrication of DRAM semiconductor integrated circuit chips. As a senior designer at Micron Technology, I designed CMOS circuits for DRAM applications and gained an understanding of the entire memory design process from fabrication to packaging. One of my projects at Micron involved the development of buffers for high-speed double-data rate (DDR) DRAM, which resulted in around 10 US patents in buffer design. I also led the development of the delay locked loop (DDL) in the 1990's to enable Micron's DRAM products to transition to the DDR memory protocol used in desktop, phone, and tablet computing systems. From 2009-2010, I served as a consultant for Sun Microsystems, where I helped design proximity connection (PxC) interfaces to DRAMs and SRAMs for transmitting data between

memory modules and memory controllers at higher speeds, and high-density 3D packaging for memory modules and controllers. I also served as a consultant for OmniVision from 2013-2015, where I designed specialty DRAM and high-speed DRAM interfaces.

10. For my contributions to memory design, I was named an IEEE Fellow in 2013. I am also a member of the honor societies Eta Kappa Nu and Tau Beta Pi. I have received a number of other honors and awards for my research contributions and teaching, including the Las Vegas (CSUN) Faculty Award (2017), Tau Beta Pi UNLV Outstanding Professor of the Year (2013-2016), UNLV ECE Department Distinguished Professor of the Year (2015), Distinguished Lecturer for the IEEE Solid-State Circuits Society (2012-2015), IEEE Circuits and Systems (CAS) Education Award (2011), Frederick Emmons Terman Award from the American Society of Engineering Education (2007), BSU President's Research and Scholarship Award (2005), IEEE Power Electronics Society's Best Paper Award (2000), and UI Department of Electrical Engineering Outstanding Researcher Award (1998-1999), among others.

11. I have significant experience providing expert witness services in the areas of electrical and computer engineering, and in the course of this work and my own research and patenting activities, I have gained experience studying and

analyzing patents and patent claims from the perspective of a person skilled in the art.

III. Documents and Materials Considered

12. In forming my opinions, in addition to my knowledge, education, training, and experience, I have considered the materials cited in this Declaration and the documents and things that I have obtained, or that have been provided to me, as listed in the Table of Exhibits.

13. I reserve the right to supplement or amend this Declaration if additional information that affects my opinions becomes available.

IV. Relevant Legal Principles

14. I am not an attorney, and I offer no opinions on the law. Counsel has informed me of legal standards that apply to the issue of patent validity. I have applied these standards in arriving at my conclusions.

15. I understand that in an *inter partes* review the petitioner has the burden of proving a proposition of unpatentability by a preponderance of the evidence. I understand this standard is different from the standard that applies in a district court, where I understand a challenger bears the burden of proving invalidity by clear and convincing evidence.

16. I understand that a patent claim is invalid based on anticipation if a single prior art reference discloses all of the features of that claim in a way that

enables one of ordinary skill in the art to make and use the invention. Each of the claim features may be expressly or inherently present in the prior art reference. I understand that if the prior art necessarily functions in accordance with, or includes a claim's feature, then that prior art inherently discloses that feature. I have relied on this understanding in expressing the opinions set forth below.

17. I understand that a prior art reference describes the claimed invention if it either expressly or inherently describes each and every feature set forth in the claim; *i.e.*, in determining whether a single item of prior art anticipates a patent claim, one should take into consideration not only what is expressly disclosed in that item, but also what is inherently present as a natural result of the practice of the system or method disclosed in that item.

18. I understand that to establish inherency, the evidence must make clear that the missing descriptive matter is necessarily present in the item of prior art and that it would be so recognized by persons of ordinary skill in the art. I also understand that prior art use of the claimed patented invention that was accidental, unrecognized, or unappreciated at the time of filing can still be an invalidating anticipation.

19. I understand that although multiple prior art references may not be combined to show anticipation, additional references may be used to interpret the allegedly anticipating reference and shed light on what it would have meant to those

skilled in the art at the time of the invention. These additional references must make it clear that the missing descriptive matter in the patent claim is necessarily present in the allegedly anticipating reference, and that it would be so recognized by persons of ordinary skill in the art.

20. I understand that a patent may not be valid even though the invention is not identically disclosed or described in the prior art if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art in the relevant subject matter at the time the invention was made.

21. I understand that obviousness must be tested as of the time the invention was made. I understand that the test for obviousness is what the combined teachings of the prior art references would have suggested, disclosed, or taught to one of ordinary skill in the art.

22. To determine if a claim is obvious, the following factors should be considered: (1) the level of ordinary skill in the art at the time the invention was made; (2) the scope and content of the prior art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations, including evidence of commercial success, long-felt but unsolved need, unsuccessful attempts by others, copying of the claimed invention, unexpected and superior results, acceptance and praise by others, independent invention by others, and the like.

23. For example, I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim because a court can take account of the inferences and/or creative steps that a person of ordinary skill in the art would employ.

24. I understand that the following rationales may be used to determine whether a piece of prior art can be combined with other prior art or with other information within the knowledge of one of ordinary skill in the art:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Predictable use or combination of prior art elements according to their established functions;
- Use of known techniques to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- “Obvious to try” - choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; or

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. I understand that when a work is available in one field of endeavor, design incentives and/or other market forces, for example, can prompt variations of it, either in the same field or a different one. Moreover, if a person of ordinary skill can implement a predictable variation, I understand this likely bars its patentability.

26. I understand that another factor to be considered is common sense. For example, I understand that common sense teaches that familiar items may have obvious uses beyond their primary purposes, and, in many cases, a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.

27. I understand that the Supreme Court articulated additional guidance for obviousness in its *KSR* decision. My understanding is that the Supreme Court said that technical people of ordinary skill look for guidance in other solutions to problems of a similar nature, and that the obviousness inquiry must track reality, and not legal fictions. I have relied on these understandings in expressing the opinions set forth below.

28. I understand that a new use of an old product or material cannot be claimed as a new product; the apparatus or system itself is old and cannot be

patented. I further understand that, in general, merely discovering and claiming a new benefit to an old process cannot render the process newly patentable.

29. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a person of ordinary skill in the art (“POSITA”). I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

30. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have been asked to use the priority date of July 29, 2005.

V. Person of Ordinary Skill in the Art

31. In order to determine the characteristics of a POSITA of the ’523 Patent, I have used July 29, 2005 as the relevant time frame. My understanding is

that this is the alleged earliest foreign priority date of the application that resulted in the '523 Patent. For purposes of this Declaration, any reference to the priority date of the '523 Patent is intended to refer to this July 29, 2005 date.

32. In determining the characteristics of a person of ordinary skill in the art for the '523 Patent, I have considered the state of the art of semiconductor memory devices at that time, the types of problems encountered with terminating the data pins of such devices and limiting signal reflections on memory buses, and the solutions that then existed. I have also considered the then-existing technology for semiconductor memory devices and computer memory systems, including the sophistication of the technology involved, and the education and experience of those working in the field at that time. I have also considered my personal knowledge and experience in the field at that time, including those I worked and interacted with regarding semiconductor memory devices and computer memory systems. I have also considered the knowledge, education, and experience of those in academia and industry at that time that were working, innovating, or performing research in the field of semiconductor memory devices and computer memory systems.

33. It is my opinion that a POSITA for the '523 Patent at the time of this filing date would have had a Bachelor's degree in Electrical Engineering, Computer Engineering, or an equivalent field, and at least two or three years of academic or

industry experience in the field of semiconductor memory design, or a person with equivalent education, work, or experience in this field.

34. Given this background, a POSITA would have been familiar with JEDEC industry standards and DRAM memory systems (memory devices, modules, controllers, and interfaces), as well as on die termination designs.

35. Based on my background and qualifications, I am currently and was as of the priority date of the '523 Patent at least a POSITA in the subject matter of the '523 Patent.

VI. '523 Patent

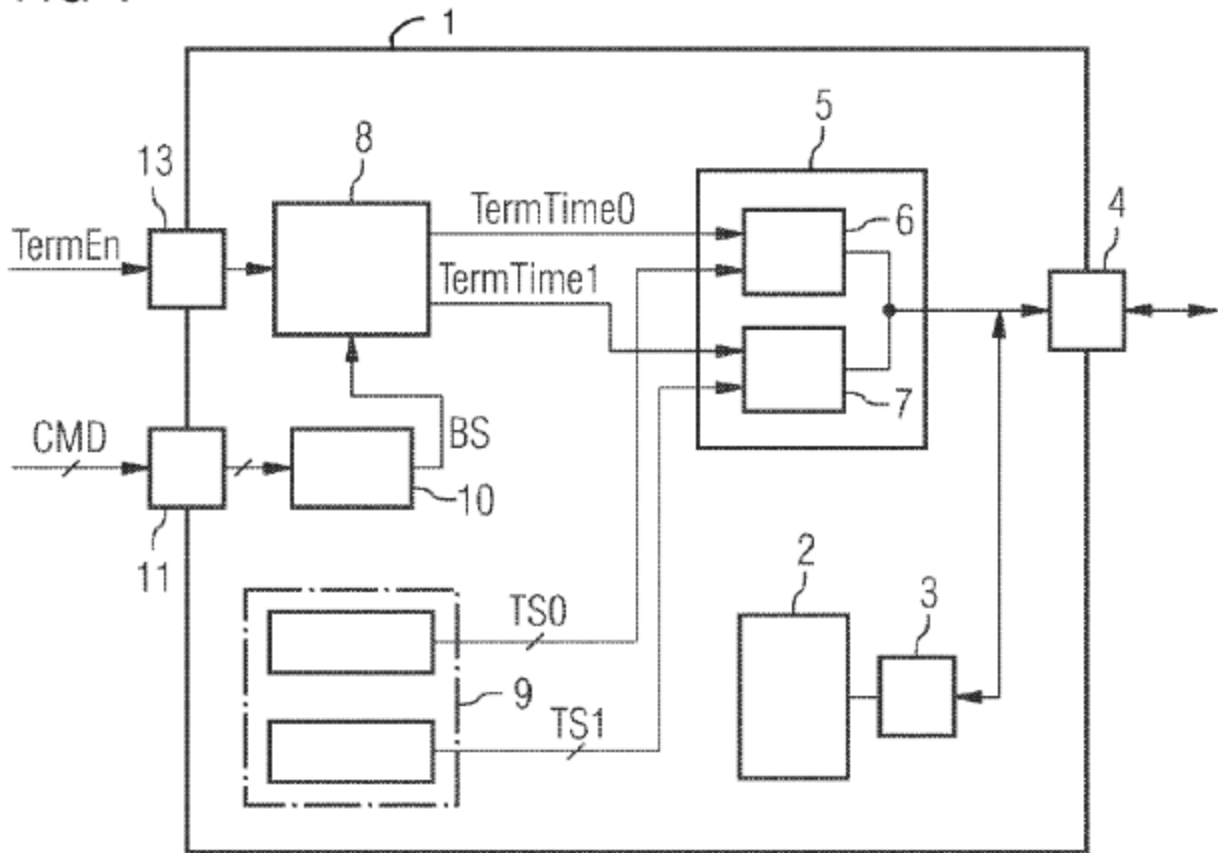
A. Overview

36. U.S. Patent No. 7,532,523 to Braun *et al.* is entitled “Memory Chip with Settable Termination Resistance Circuit” and was issued on May 12, 2009.

37. The '523 Patent is directed to a system and method for terminating a memory chip with various termination resistances using on die termination (ODT). EX1001 at 1:66-2:8. The claimed invention is designed to be used in a memory system comprising a plurality of memory chips operated via signal lines of a memory bus by a memory controller. *Id.* at 1:23-29. The system and method for terminating a memory chip purport to improve upon the prior art by providing suitable terminations at the terminals of the memory chips to reduce signal reflections on the signal lines, thereby allowing for higher data transmission rates. *Id.* at 1:29-36.

38. As shown in Fig. 1 below, the memory chip 1 includes a terminal 4 connected to a termination circuit 5 with resistors 6 and 7 for terminating the terminal 4. *Id.* at 2:40-52, Fig. 1. The termination circuit 5 is further connected to a control unit 8 that sends two control signals, TermTime0 and TermTime1, to the termination circuit 5 for controlling which resistor is connected to the terminal 4. *Id.* at 1:52-67. More particularly, when TermTime0 is activated, the first resistor 6 is connected to the terminal 4; when TermTime1 is activated, the second resistor 7 is connected to the terminal 4; and when both signals are activated, the first and second resistors 6 and 7 may be connected to terminal 4 in parallel. *Id.* In that way, the magnitude of the termination resistance may be changed based on the received control signal.

FIG 1



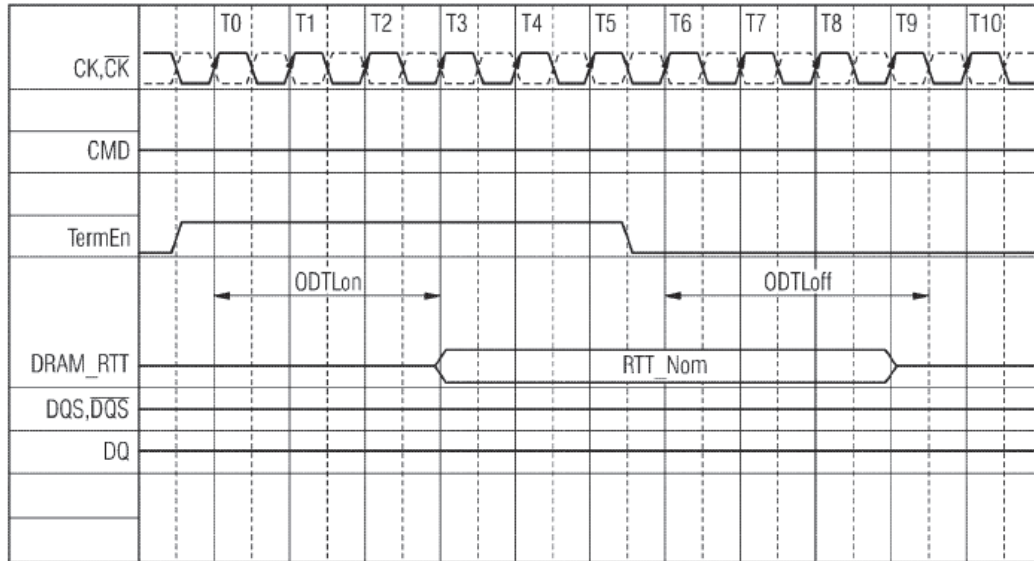
39. The memory chip 1 further includes a termination port 13 through which the control unit 8 receives a termination enable signal TermEn. *Id.* at 3:25-28. The termination enable signal controls whether termination is provided at terminal 4, such that, “via the first and the second control signal TermTime0, TermTime1, the respective terminating resistor 6, 7 is connected to the external terminal 4 only when the termination signal TermEn specifies that there is to be a termination.” *Id.* at 3:28-32.

40. The chip 1 also includes a control command port 11 for receiving a control command signal, which may be, for example, a chip select signal CS, a write enable signal WE, a row activation signal RAS, or a column activation signal CAS. *Id.* at 3:41-51. A command decoder 10 converts the control command signal into command signal BS, which determines which of the resistors 6 and 7 is connected to the terminal 4. *Id.* at 3:34-40. For a first group of control command signals, the command decoder outputs a command signal BS indicating to the control unit 8 that termination needs to be undertaken with a first resistance value when TermEn is activated. *Id.* at 5:40-58. Similarly, a second group of control command signals results in a command signal BS indicating to the control unit 8 that termination needs to be undertaken with a second resistance value. *Id.* As the specification explains, the first group of control command signals may comprise commands that indicate a deactivation of the integrated circuit or a read access, and the second group may comprise write commands. *Id.*

41. The timing of the termination enable signal and the termination of the memory chip when the chip is not accessed is illustrated in Fig. 3, below. The delay ODTLon represents a predetermined termination switch-on time, or the delay in terminating the terminal 4 after the termination signal TermEn is asserted, and the delay ODTLoff is the predetermined termination switch-off time, or the delay in

disconnecting the termination resistor after the termination signal TermEn is deactivated. *Id.* at 4:30-42, Fig. 3.

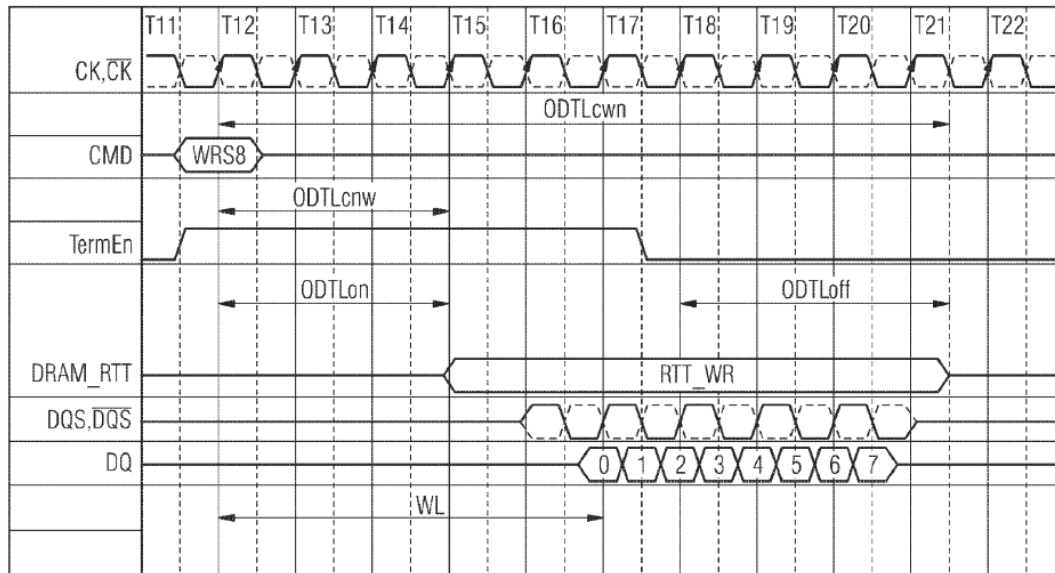
FIG 3



42. The timing of the control command signal, the termination enable signal, and the termination of the memory chip during a write command is illustrated in Fig. 4, below. *Id.* at 4:64-5:2, Fig. 4. As before, the delay ODTLon represents a predetermined termination switch-on time, or the delay in terminating the terminal 4 after the termination signal TermEn is asserted. *Id.* at 4:30-36. Similarly, ODTLoff is the predetermined termination switch-off time, or the delay in disconnecting the termination resistor after the termination signal TermEn is deactivated. *Id.* at 4:36-42. The termination switch-on and switch-off times ODTLon and ODTLoff may be selected to provide the terminating resistor enough time to connect or disconnect to the terminal without disrupting the data signal. *Id.* at 4:42-50. In particular, the

switch-on time ODTLon may be selected to be equal to or less than the write latency time duration WL of the data in order to ensure that the terminating resistor is connected before data transmission. *Id.* at 5:34-39.

FIG 4



43. The time delay between applying the control command signal (such as WRS8, above) and changing the resistance value is ODTLcwn, which may be less than or equal to the termination switch-on time ODTLon. *Id.* at 5:59-65. When the control command signal is one of the second group of control command signals, such as a write command, the control unit 8 changes the termination resistance value after a second switchover time ODTLcwn has lapsed, where ODTLcwn represents a time duration defined by the end of an access to the chip that is triggered by the control command signal, such as the end of a write access. *Id.* at 6:5-31. As shown in Fig.

4, the control unit 8 may switch the termination on or off and change the resistance value simultaneously. *Id.* at 5:66-6:4, Fig. 4.

B. Background / Applicant Admitted Prior Art

44. I have reviewed the '523 Patent, including the section of the Specification titled "BACKGROUND OF THE INVENTION." I understand this section of the '523 Patent to disclose technologies that were already known in the art as of the priority date of the '523 Patent. In particular, I note that many of the elements that are recited in the '523 Patent claims are described in this section. For example:

Claim	Claim Language	Background
[1.3]	a control command port for receiving a control command signal for affecting accessibility of the memory chip; <i>See also, claim [5.5]</i>	"Furthermore, it can be provided that the strength of the terminating resistors in the memory chips is fixed in accordance with a configuration value that is communicated to the memory chips by the memory controller in an initialization phase at the beginning of the operation of the memory system." EX1001 at 1:50-54. "In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller."

Claim	Claim Language	Background
		EX1001 at 1:23-29.
[1.4]	a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and <i>See also</i> , claim [5.6]	“Furthermore, it can be provided that the strength of the terminating resistors in the memory chips is fixed in accordance with a configuration value that is communicated to the memory chips by the memory controller in an initialization phase at the beginning of the operation of the memory system.” EX1001 at 1:50-54.
[1.5]	a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal, <i>See also</i> , claim [5.8]	“It has previously been provided in the case of memory chips to switch the termination on or off at a terminal of the memory chip as a function of a termination signal. That is to say, the memory controller makes a suitable termination signal available to each of the memory chips in order to support the following read, write or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus.” EX1001 at 1:37-44.
[5.1]	(a) a memory controller having a terminal;	“In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller.” EX1001 at 1:23-29.
[5.2]	(b) a plurality of memory chips, at least one of the memory chips comprising:	“In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus.

Claim	Claim Language	Background
		Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller.” EX1001 at 1:23-29.
[5.7]	(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and	“In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller.” EX1001 at 1:23-29.
[9.1]	receiving a control command signal for affecting accessibility of the memory chip;	“In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller.” EX1001 at 1:23-29. “Furthermore, it can be provided that the strength of the terminating resistors in the memory chips is fixed in accordance with a configuration value that is communicated to the memory

Claim	Claim Language	Background
		chips by the memory controller in an initialization phase at the beginning of the operation of the memory system.” EX1001 at 1:50-54.
[9.2]	setting a resistance value for a terminal as a function of the control command signal;	“Furthermore, it can be provided that the strength of the terminating resistors in the memory chips is fixed in accordance with a configuration value that is communicated to the memory chips by the memory controller in an initialization phase at the beginning of the operation of the memory system.” EX1001 at 1:50-54.
[9.4]	receiving a termination enable signal, the presence of which is required for the terminating to occur.	“It has previously been provided in the case of memory chips to switch the termination on or off at a terminal of the memory chip as a function of a termination signal. That is to say, the memory controller makes a suitable termination signal available to each of the memory chips in order to support the following read, write or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus.” EX1001 at 1:37-44.

45. These same applicant admitted prior art (AAPA) concepts are also found in the prior art references that I discuss in the grounds of unpatentability below.

C. Prosecution History

46. On July 31, 2006, the '523 Patent was filed as Application No. 11/461,380 (the "'380 Application") entitled "Memory Chip and Method for Operating a Memory Chip." EX1002 at 200. The '380 Application claims priority to German Patent Applications DE 10 2005 035 780 and DE 10 2005 036 528, filed July 29, 2005 and August 3, 2005, respectively. EX1002 at 195. The application originally listed twenty-six claims, and the Applicant filed a preliminary amendment on November 2, 2007 to primarily correct typographical and grammatical errors in claims 1, 5, and 11-20. EX1002 at 184-188, 145-151.

47. During prosecution of the '380 Application, the PTO issued one non-final office action on June 19, 2008, in which the Examiner rejected claims 1-5, 10-15, and 20-24 as anticipated by U.S. Patent No. 6,762,620 to Jang and as anticipated by U.S. Patent No. 7,148,721 to Park. EX1002 at 59-66. The Examiner objected to claims 6-9, 16-19, 25, and 26 as dependent upon a rejected base claim, noting that they would be allowable if rewritten in independent form. EX1002 at 66. In response, the Applicant canceled claims 1-5, 10-15, and 20-24 and amended claims 6, 16, and 25 by rewriting them in independent form. EX1002 at 44-50. The amended claims incorporated the limitations of the rejected base claims with an additional limitation from the allowable dependent claims relating to termination delays:

wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set

resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

EX1001 at 8:64-9:2; *see also* EX1001 at 9:42-10:4, 10:28-34; *compare* EX1002 at 44-47 *with* EX1002 at 146-150.

48. The Examiner allowed claims 6-9, 16-19, 25, and 26 on January 13, 2009 based on the above termination delay limitation. EX1002 at 28. However, as explained below, this limitation was already taught in the prior art.

D. Priority Date

49. As discussed above, the '380 Application claims priority to two German patent applications filed on July 29, 2005 and August 3, 2005. EX1001. For the purposes of this Declaration, I have been told to assume that the earliest priority date of the '523 Patent is July 29, 2005.

VII. Technology Background

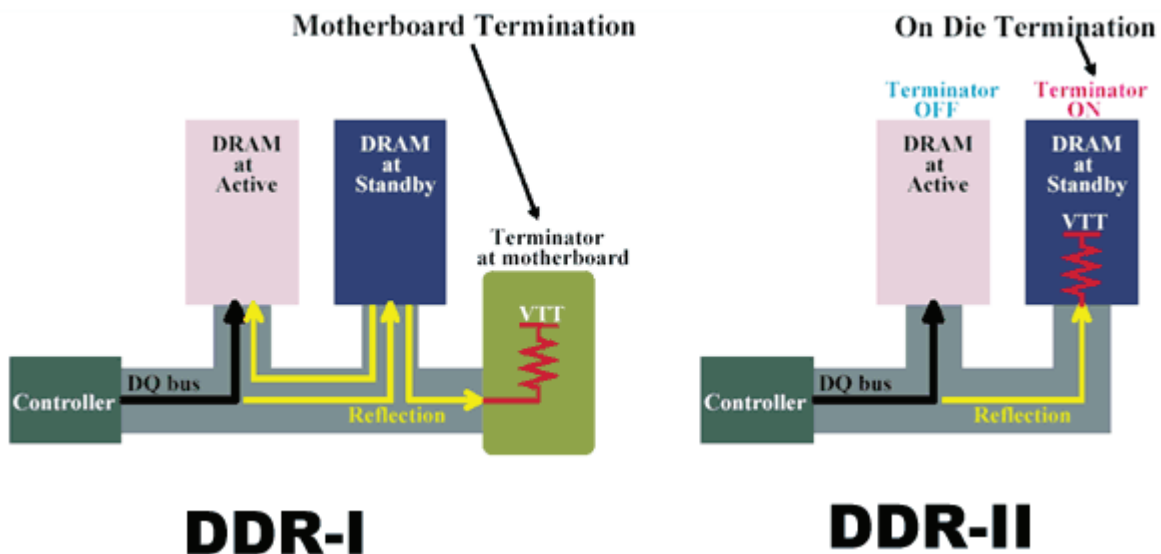
50. The technology of the '523 Patent relates to on die termination (ODT) of semiconductor memory chips. As of the filing date of the '523 Patent, ODT was well known and available in Double Data Rate 2 (DDR2) SDRAM memory chips and Graphics DDR3 (GDDR3) memory chips. EX1006 at 26-30; EX1015 at 85-88.

51. A memory system generally includes a memory controller connected to a number of memory chips through buses, which are bundles of wires that carry electrical signals and allow the memory controller and the memory chips to

communicate. The memory chips are typically organized in memory modules, which may be, for example, dual in-line memory modules (DIMMS). Each module may include only one “rank” of memory chips, or more than one “rank” of memory chips, where a “rank” is a group of memory chips that are selected together through a shared chip select signal. Each module is installed in a “slot” of the memory system. A memory system may include, as non-limiting examples, two single rank modules, or two dual rank modules.

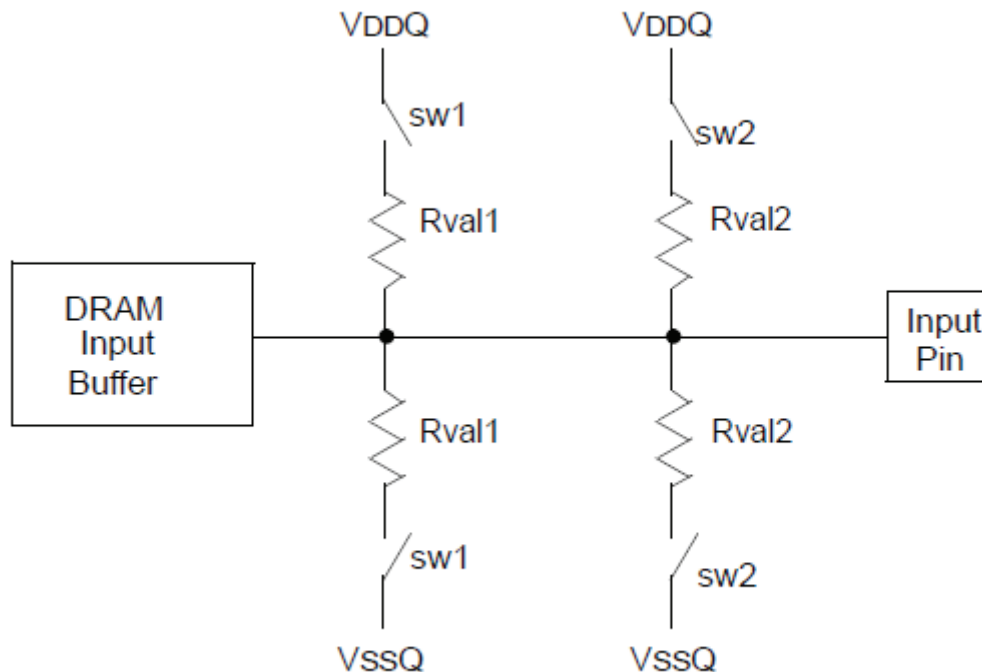
52. The buses are typically separated into data, address, control, chip select, and ODT buses. The address bus carries row and column addresses to the memory chips; the control bus carries write enable and other related command signals; and the chip select bus carries a chip select signal, which enables a memory chip’s command decoder and allows the memory controller to select particular chips for a command (such as a read or write command). During a read or write operation, data is transferred between the memory controller and one or more memory chips through the data bus. The ODT bus allows the memory controller to selectively enable or disable ODT in one or more memory chips by transmitting a termination enable signal to the chips. Each chip includes a number of pins for connecting to the buses and a command decoder, which accepts and interprets the above signals as a particular command.

53. During transmission of signals on the various buses, signal reflections can occur at the pins, or terminals, of the memory chips. These reflections diminish signal integrity and limit data transmission rates. To prevent interference from unwanted signal reflections, memory systems include a means of terminating the pins, or terminals, of the memory chips with a suitable resistance. In DDR SDRAM systems, this termination means is external to the memory chips on the motherboard. However, DDR2 SDRAM systems use ODT, where the termination circuits are provided within the memory chips. The diagram below illustrates the difference between the two termination schemes. EX1008 at 3.



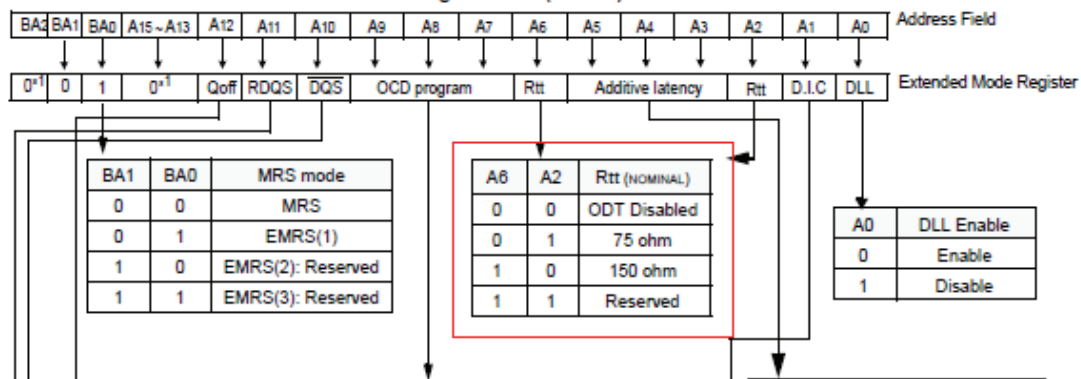
54. The ODT circuit in a DDR2 SDRAM chip, illustrated below, usually includes two or more sets of resistors and switches which enable the chip to be terminated with two or more effective resistance values. For example, when switches sw1 are closed, the chip is terminated with an effective resistance R_{tt} of $(R_{val1})/2$.

When switches sw2 are closed, the chip is terminated with an effective resistance R_{tt} of $(R_{val2})/2$. EX1006 at 27, Fig. 15.



55. The value of the termination resistance is controllable using extended mode register set (EMRS) commands. As shown below, each DDR2 SDRAM memory chip has an extended mode register (EMR) which is programmed with parameters that control the memory chip's operation. Bits A2 and A6 in the EMRS control whether ODT is enabled, as well as the value of the effective resistance. The EMRS is written by asserting low on CS, RAS, CAS, WE, high on BA0, and low on BA1. EX1006 at 21, 22, Fig. 9.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)



56. In a multi-rank memory module, ODT is generally enabled in the memory chips that are not receiving data during write operations. Thus, while one rank receives a write command, another rank receives an ODT signal for enabling termination.

57. Termination does not occur immediately after the termination enable signal is received by the memory chip. Instead, termination is defined by ODT turn-on and turn-off delays, which allow the pin to be terminated before data is transmitted.

VIII. Claim Construction

58. I have interpreted the terms of the '523 Patent according to their plain meaning. In interpreting the terms, I have carefully considered and applied the claim construction standards referred to in Section IV above.

IX. Summary of Opinions

59. In my opinion, U.S. Patent No. 7,433,992 to Bains, entitled "Command Controlling Different Operations in Different Chips" ("Bains"), either alone or in

combination with JEDEC Standard No. JESD79-2A, entitled “DDR2 SDRAM Specification,” and dated January 2004 (“JESD79-2A”), renders obvious claims 1, 2, 5, 6, 9 and 10 of the ’523 Patent (*see infra* Section X).

60. A table of the grounds is provided below for ease of reference:

	Grounds	Claims
1	§103: Bains	1, 2, 5, 6, 9, 10
2	§103: Bains in combination with JESD79-2A	1, 2, 5, 6, 9, 10

A. Overview of Bains (EX1005)

61. U.S. Patent No. 7,433,992 (“Bains”) was filed as U.S. Application No. 10/992,953 on November 18, 2004, published on May 18, 2006 as U.S. Patent Publication No. 2006/0106951, and issued on October 7, 2008. *See* EX1001 at 1.

62. Bains discloses a memory system comprising a memory controller 12 and memory chips MC0 and MC1 having on die termination (ODT) circuitry 38 and 48. EX1005 at 2:33-58, 3:41-58, Fig. 2 (below). The system also includes a control bus 20, a data bus 22, an address bus 24, and chip select buses 26 and 28 through which the memory controller and the memory chips communicate. EX1005 at 3:9-16.

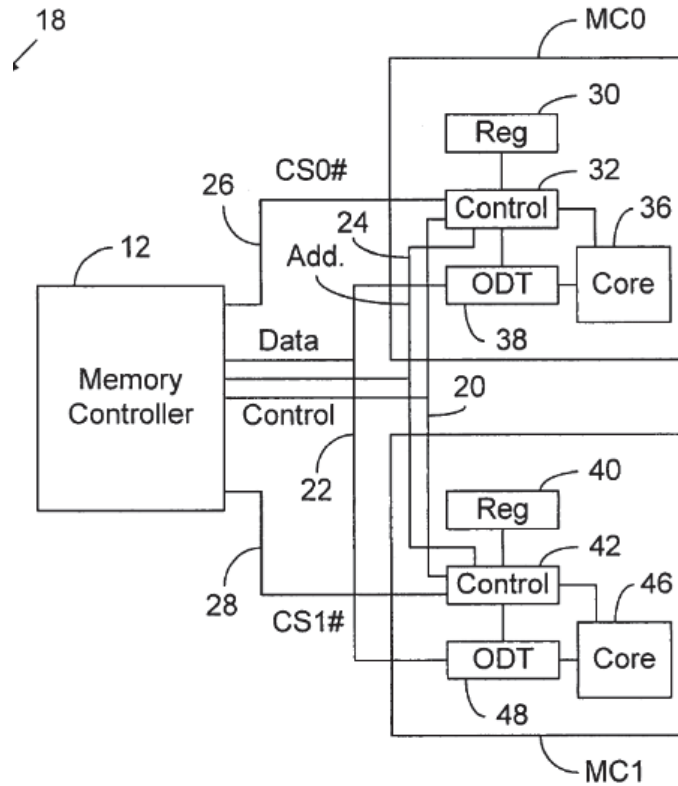


FIG. 2

63. EX1005 at Fig. 2. Commands such as commands A and B may be provided from memory controller 12 to chips MC0 and MC1 through control bus 20. EX1005 at 3:17-20, 41-42. Control circuitry 32 in chip MC0 and control circuitry 42 in chip MC1 receive the commands and control the operation of ODT circuitry 38 and 48, respectively, based on the commands. EX1005 at 3:41-58. For example, chip MC0 responds to command A as a write command, while control circuitry 42 in chip MC1 responds to command A by turning on ODT 48. *Id.* Conversely, chip MC1 responds to command B as a write command, while control circuitry 32 of chip MC0 turns on ODT 38. *Id.*

64. An exemplary ODT circuit 38 is shown in Fig. 4, below. Control circuitry 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off.” EX1005 at 4:39-40. Additionally, the number of switches that are closed may determine the amount of resistance that is applied to the data pin. EX1005 at 4:40-42. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. While Bains discloses that the commands control whether ODT is “on” as well as the level of ODT resistance, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands. EX1005 at 6:30-37.

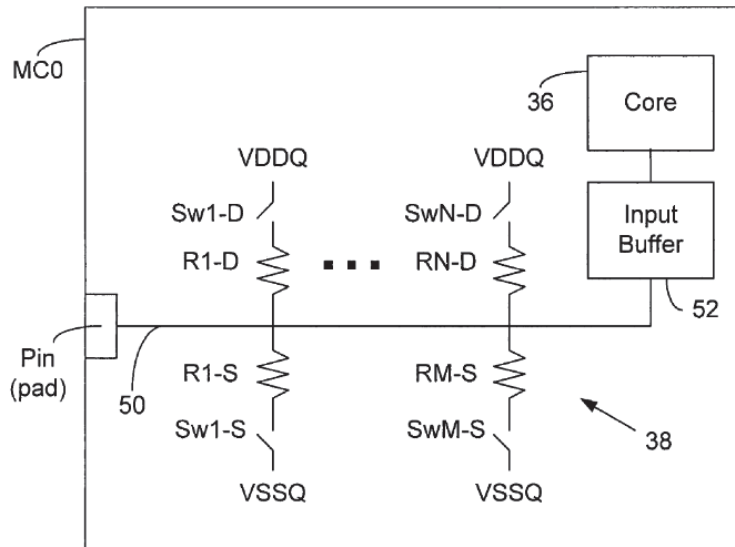


FIG. 4

EX1005 at Fig. 4.

65. Bains further teaches that the ODT is enabled and disabled according to predetermined delays. As illustrated in Fig. 7 below, ODT in chip MC1 is turned on after a delay of t_{AOND} after command A is asserted. EX1005 at 5:23-30. ODT in chip MC1 is turned off automatically after a fixed delay based on a burst length of 8. EX1005 at 5:40-42, Fig. 7.

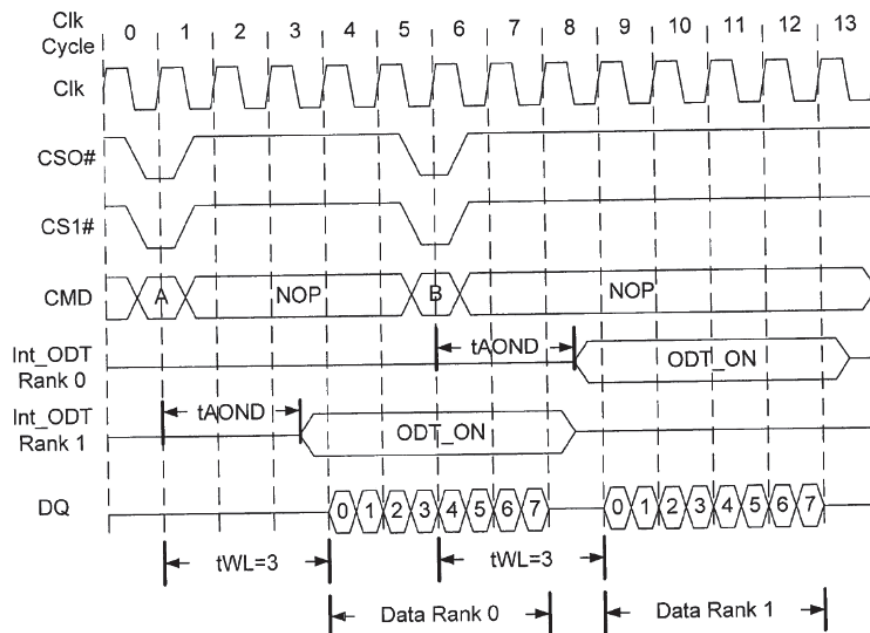


FIG. 7

B. Overview of JESD79-2A (EX1006)

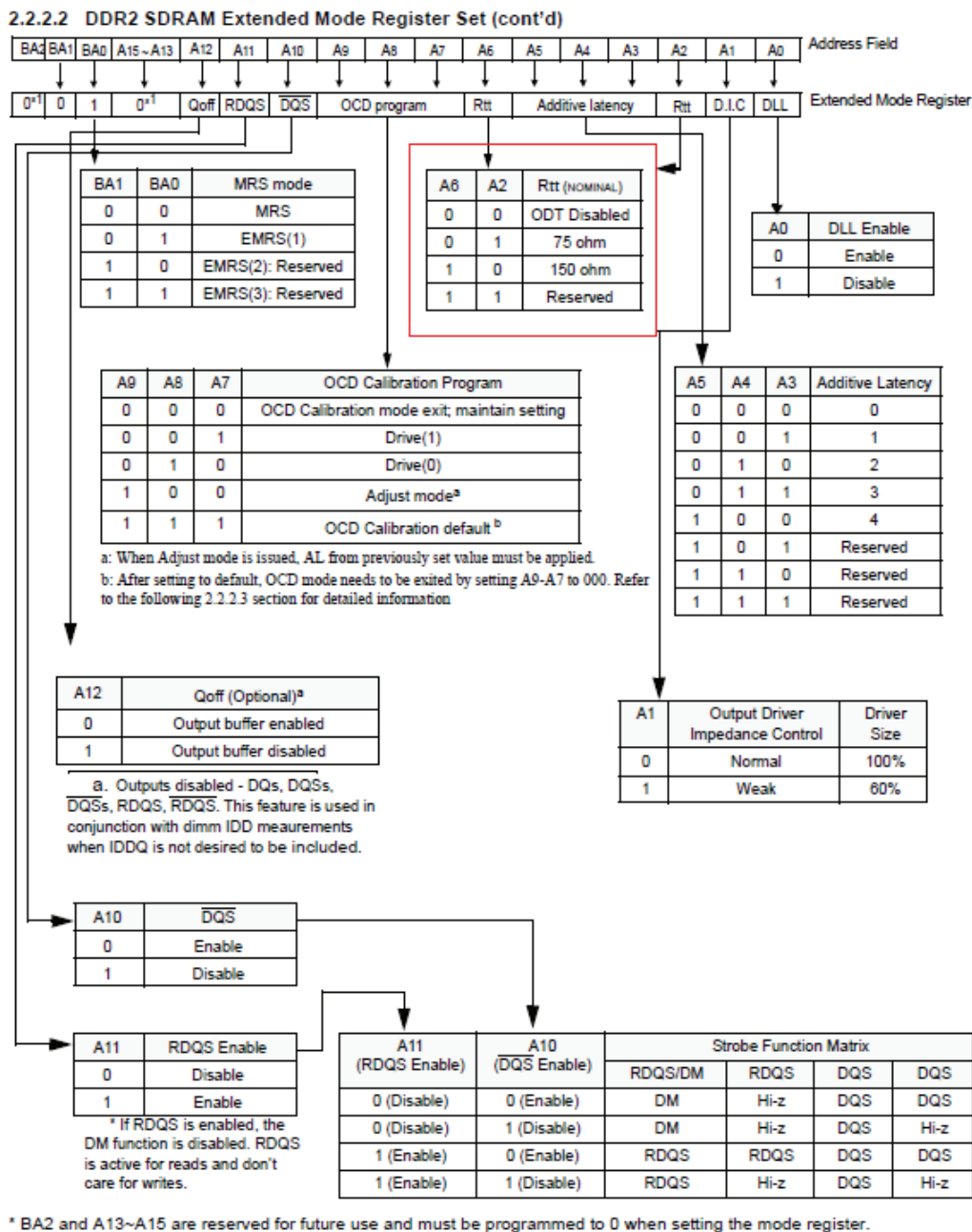
66. JEDEC Double Data Rate 2 (DDR2) SDRAM Specification, JESD79-2A (“JESD79-2A”), was and remains a well-known DDR2 memory standard published by a prominent memory standards setting organization, JEDEC. The JESD79-2A standard explains that the purpose of the standard is to “serve the public interest through eliminating misunderstandings between manufacturers and

purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product.” EX1006 at 2. A POSITA would have been familiar with JEDEC memory standards like JESD79-2A, as these standards are widely relied upon by manufacturers to create memory products with a high level of interoperability and interchangeability. In fact, many manufacturers’ product datasheets closely mirror JEDEC’s standards and specifications. JEDEC’s specifications are easily accessible on its website, and a POSITA would understand how to access the standards and use them to design a conforming memory device.

67. JESD79-2A discloses a specification for DDR2 SDRAM, which has ODT functionality. When the ODT signal on the ODT control pin is high, termination resistance internal to the DDR2 SDRAM is enabled and applied to the DQ terminal. EX1006 at 14, 26.¹ The ODT feature is designed to improve signal integrity by allowing the memory controller to independently enable termination resistance for connected memory chips. EX1006 at 26. As shown in Fig. 9, below, the extended mode register set (EMRS) stores data for enabling ODT functionality and setting the ODT resistance value in bits A2 and A6. EX1006 at 21, 22. The

¹ All page cites refer to the stamped page number of the exhibit.

EMRS is written by asserting low on CS, RAS, CAS, WE, high on BA0, and low on BA1. EX1006 at 21, 22, Fig. 9 (annotation added)².



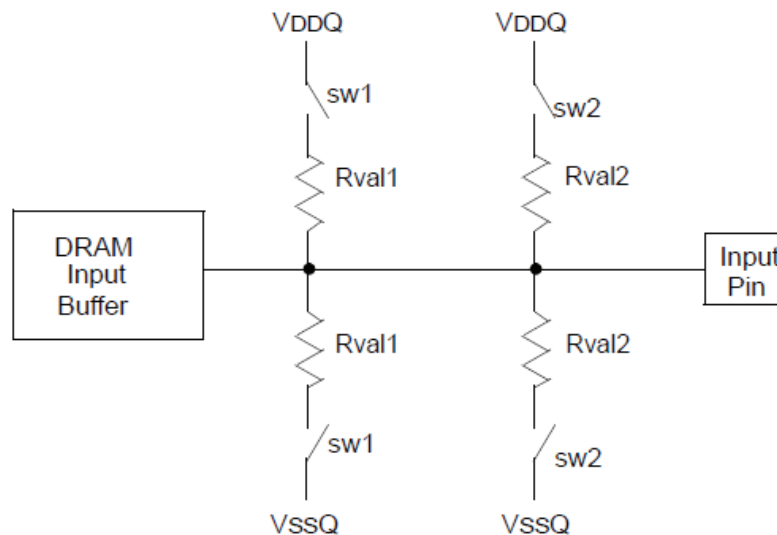
* BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

Figure 9 — EMRS(1) Programming

² All color annotations in figures have been added unless otherwise stated.

68. JESD79-2A illustrates an ODT circuit in Fig. 15, below. Switches sw1 and sw2 are enabled by the ODT pin, and the selection between sw1 and sw2 is determined by bits A2 and A6 in the EMRS, as explained above. EX1006 at 27, Fig. 15. For example, if Rval1 is associated with an effective resistance of 75 ohms, and Rval2 is associated with an effective resistance of 150 ohms, then switches sw1 are selected when bit A6 is set to 0 and bit A2 is set to 1, and switches sw2 are selected when bit A6 is set to 1 and bit A2 is set to 0. When a high level is applied to the ODT pin, switches sw1 or sw2 are closed depending on the values of bits A2 and A6.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
 Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
 Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
 Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

69. JESD79-2A also discloses the ODT timing for a DDR2 SDRAM in active/standby mode. As illustrated in Fig. 16 below, termination is applied after a period t_{AOND} after the ODT signal is enabled, and termination ends after a period t_{AOFD} after the ODT signal is disabled. EX1006 at 27, Fig. 16.

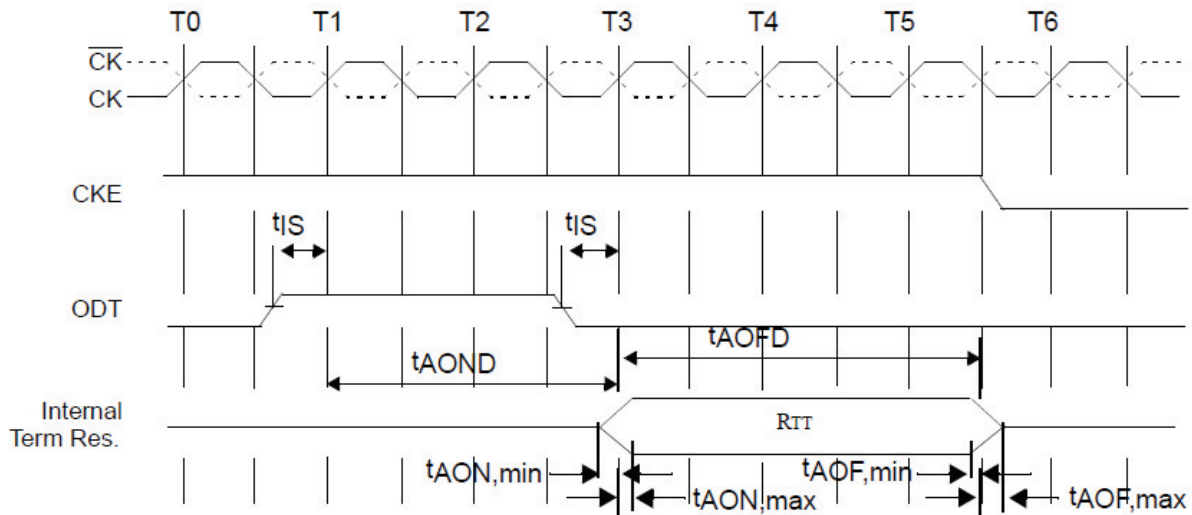


Figure 16 — ODT Timing for Active/Standby Mode

70.

X. Claims 1, 2, 5, 6, 9, and 10 are Invalid

A. Claims 1, 2, 5, 6, 9, and 10 are Obvious Over Bains

71. In my opinion, Bains renders obvious claims 1, 2, 5, 6, 9, and 10 of the '523 Patent.

1. Claim 1

a. “A memory chip for variably setting terminations, comprising:” [1.P]

72. I understand that the preamble of claim 1 is not limiting. Nevertheless, to the extent the preamble is limiting, Bains teaches the limitation. Specifically, Bains teaches a memory chip MC0 (or alternatively, MC1) with an ODT circuit 38 that may terminate a data pad with an infinite resistance³ or different finite resistances depending on the command A1 or A2 provided to the chip from the memory controller 12. EX1005 at 2:33-52, 3:41-58, 4:39-46, Figs. 2 and 4 (each figure reproduced below) (“The number of switches closed may determine the amount of resistance in the termination. For example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.”); *see also infra* limitation [1.2] at Section X.A.1.c. Bains further teaches that chips MC0 and MC1 in Fig. 2 may belong to different ranks of memory chips (ranks 0 and 1) that receive different chip select signals CS0# and CS1#:

In current typical implementations, more than one memory chip is included in a module. The chips are typically grouped in ranks. For example, FIG. 5 illustrates memory controller 12 being coupled to memory chips in a memory module 64, which has two ranks of chips supported by support 62. A first rank (rank 0) includes memory chips MC0-0 ... MC0-N (where N is not necessarily the same as in FIG. 4). A second rank (rank 1) includes memory chips MC1-0 ... MC1-N. The two ranks may have the same number of chips or a different number.

³ The term “infinite resistance” refers to the high impedance state that occurs when the termination circuit is open, or deactivated.

FIG. 5 illustrates each chip in a rank being selected by the same chip select signal (CS0 for the chips of rank 0 and CS1 for the chips of rank 1). The chip select signal could be provided on its own multi-drop bus as illustrated in FIG. 5 or through other ways such as a multiplexed or packetized signal.

EX1005 at 4:47-61, Fig. 5.

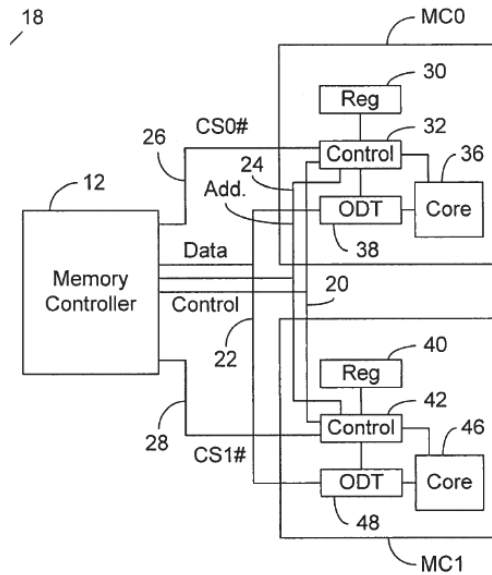


FIG. 2

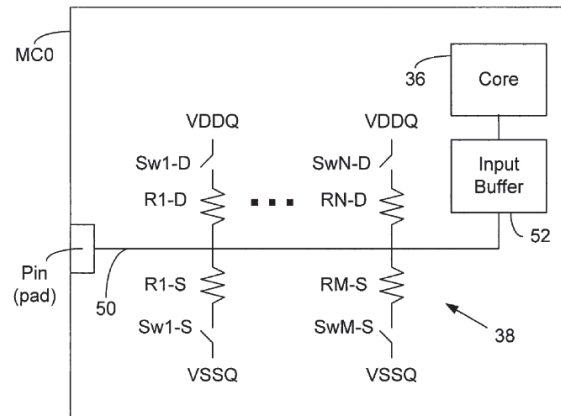


FIG. 4

b. “a terminal” [1.1]

73. Bains teaches this limitation. As shown below in Fig. 4, Bains teaches that the memory chip MC0 includes a data pin (pad), which is a terminal. EX1005 at Fig. 4 (annotated and reproduced below). Referring to Fig. 1 of the '523 Patent, which illustrates memory chip 1 with terminal 4, a POSITA would understand that terminal 4 is a pin or pad for receiving address, clock, or data signals. EX1001 at 2:45-48, Fig. 1 (“The logic circuit 3 is connected to an external terminal 4 of the memory chip 1 via which, for example, address, clock and user data can be read in

or driven out.”). Thus, the data pin (pad) in Fig. 4 of Bains is equivalent to the terminal 4 disclosed in the '523 Patent.

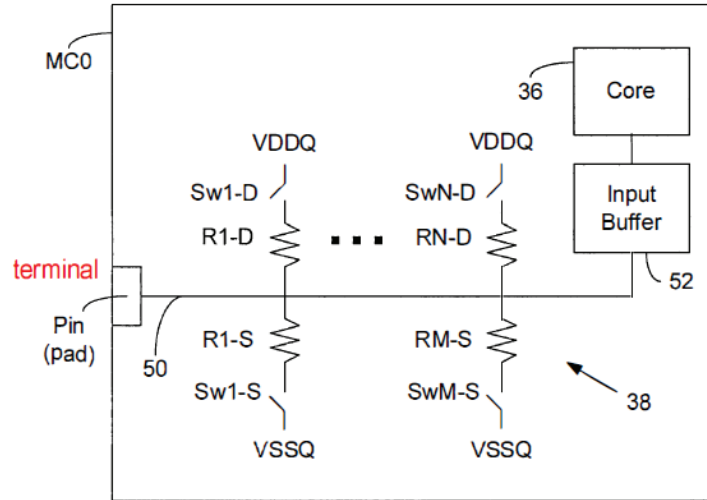
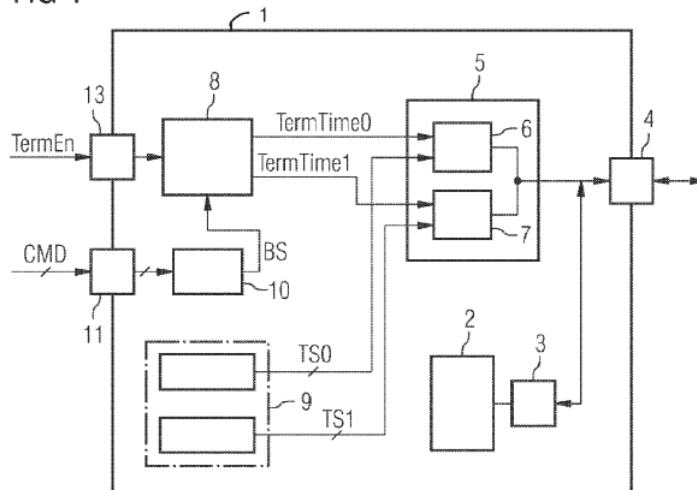


FIG. 4

FIG 1



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT

c. “a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;” [1.2]

74. Bains also teaches this limitation. As illustrated in Figs. 2 and 4 below, Bains discloses an ODT circuit 38 coupled to the terminal. EX1005 at Figs. 2, 4 (annotated and reproduced below). Control circuitry 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S of the termination circuit 38 and thus whether ODT is “on” or “off.”

Referring to FIG. 4, resistive structures R1-D . . . RN-D are between a data node 50 and switches Sw1-D . . . SwN-D, respectively, which in turn are coupled to a supply voltage node VDDQ. Resistive structures R1-S . . . RM-S are between data node 50 and switches Sw1-S . . . SwM-S, respectively, which in turn are coupled to a ground voltage node VSSQ. The numbers "N" and "M" may be the same or different and may have different values in different implementations. Control circuitry 32 controls the switches and hence whether ODT 38 is “on.”

EX1005 at 4:31-40.

75. Additionally, the number of switches that are closed determines the amount of resistance that is applied to the data pin. EX1005 at 4:40-42 (“The number of switches closed may determine the amount of resistance in the termination.”) As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. Thus, the termination circuit 38 may apply an infinite resistance to the terminal (open circuit, ODT “off”) or any one of a variety of finite resistances depending on which switches

Sw1-D...SwN-D and Sw1-S...SwM-S are activated by control circuitry 32 as a function of commands A1, A2...AN.

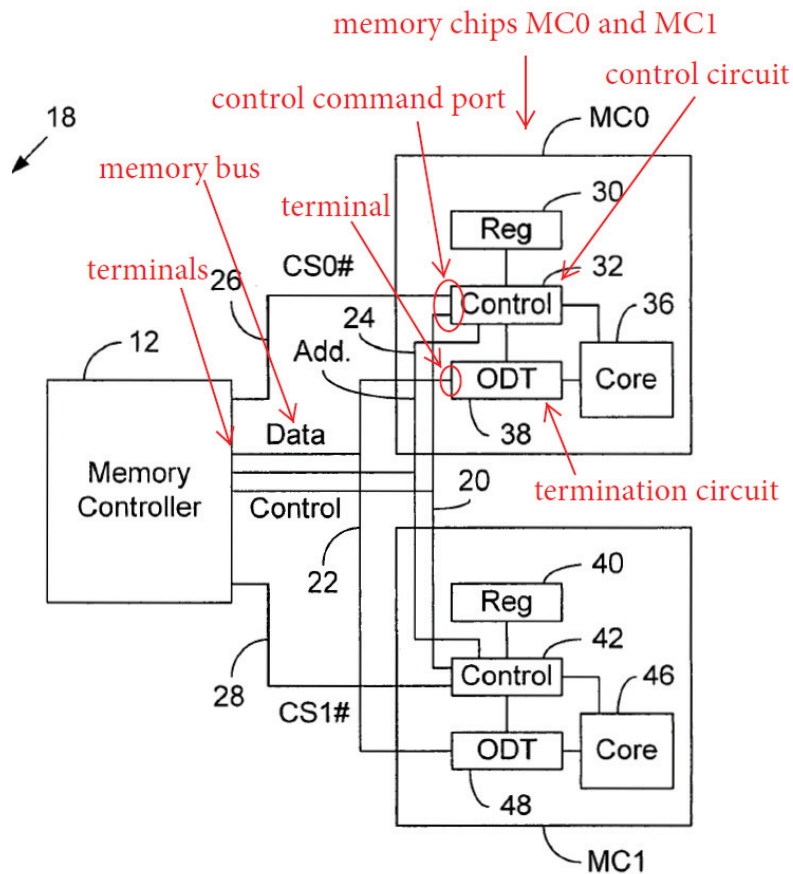


FIG. 2

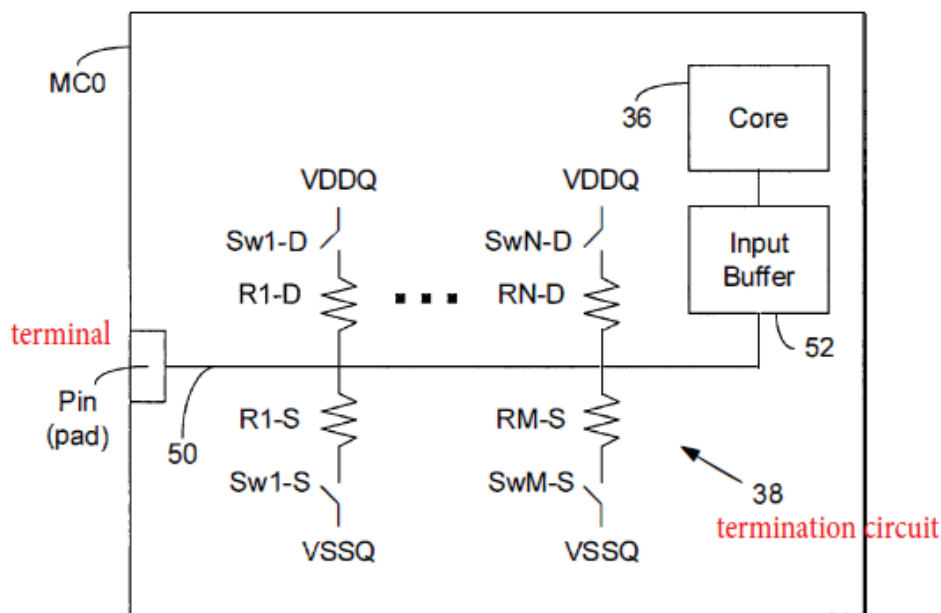


FIG. 4

d. “a control command port for receiving a control command signal for affecting accessibility of the memory chip;” [1.3]

76. Bains also teaches this limitation. As shown in annotated Fig. 2, below, Bains teaches that memory controller 12 is coupled to chips MC0 and MC1 through a control bus 20 and chip select buses 26 and 28 through which commands may be transmitted:

Referring to FIG. 2, memory controller 12 is coupled to chips MC0 and MC1 through a control bus 20, a data bus 22, and an address bus 24. Chip select (CS) signals are provided to chips MC0 and MC1 through buses 26 and 28....The commands referred to in this disclosure may be provided from memory controller 12 to chips MC0 and MC1 through various ways. In some embodiments, the commands described herein are provided only through control bus 20. In other embodiments, the commands are provided through a combination of control bus 20 and address bus 24. In still other embodiments, the data

bus is also used to communicate commands. Control circuitry 32 in chip MC0 and control circuitry 42 receive the commands from controller 12, although the signal including the commands may be modified or otherwise changed between the controller 12 and controller circuitry 32 and 42.

EX1005 at 3:9-28.

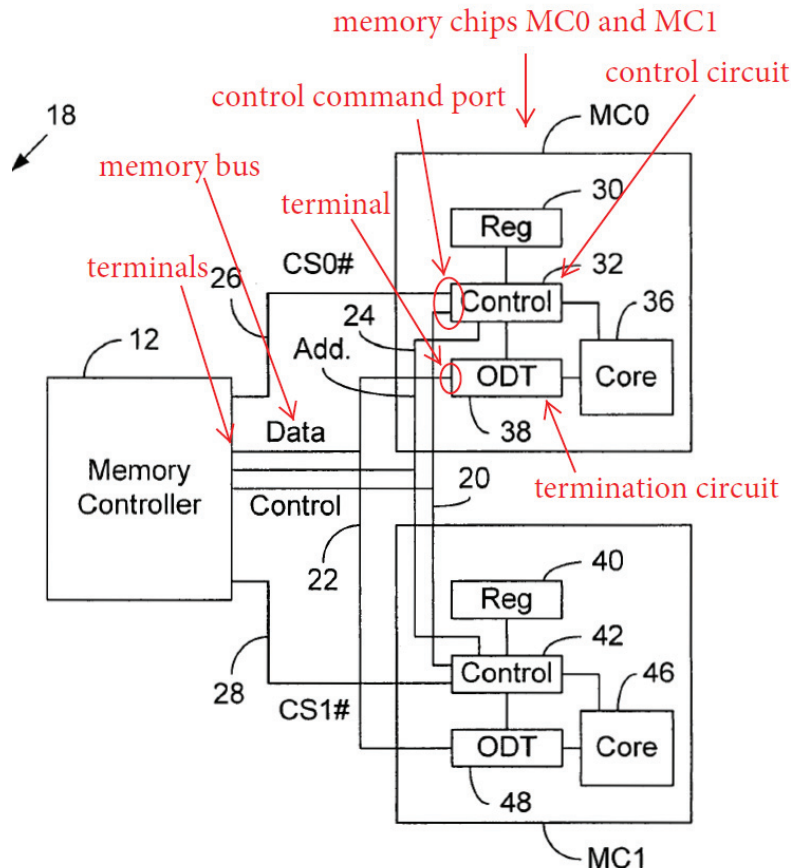


FIG. 2

EX1005 at Fig. 2 (annotated).

77. In order to receive commands from the memory controller 12 sent over the buses, a POSITA would understand that the control circuit 32 includes a port connected to the control bus 20 and chip select bus 26, as represented by the topmost circled portion in the above annotated Fig. 2. In particular, a POSITA would

understand that chip MC0 must have a pin or pad connected to the control bus 20 and chip select bus 26 in order to receive commands through control bus 20 and chip select bus 26 from the memory controller 12. EX1005 at 3:9-28. Because control bus 20 and chip select bus 26 are illustrated in the functional diagram in Fig. 2 as connecting to control circuit 32, a POSITA would further understand that the control circuit itself receives signals from control bus 20 and chip select bus 26. EX1005 at 3:24-28 (“Control circuitry 32 in chip MC0 and control circuitry 42 receive the commands from controller 12, although the signal including the commands may be modified or otherwise changed between the controller 12 and controller circuitry 32 and 42.”). To the extent Patent Owner were to argue such a control command port is not expressly disclosed, it certainly would have been obvious to a POSITA that the control circuit 32 includes such a port, given the above disclosures in Bains.

78. Furthermore, Bains discloses that the memory controller 12 transmits commands A, B, C, or D to the memory chips via the buses. EX1005 at 3:17, 28, 3:37-4:6. Bains describes that these commands may be, for example, write commands, read commands, or refresh commands, which affect accessibility of the chips MC0 and MC1.

In example 1, there are commands called commands A and B. Chip MC0 responds to command A as a write command, meaning that control circuitry 32 causes certain data bits on data bus 22 to be stored in core 36 of chip MC0. Chip MC1 responds to command A by turning on ODT 48. More particularly control circuitry 42 turns on ODT 48. Conversely, chip MC0 responds to command B by turning on ODT 38

and chip MC1 responds to command B as a write command. More particularly, in response to command B, control circuitry 32 turns on ODT 38 and control circuitry 42 causes data on bus 22 to be stored in core 46. In some embodiments, if the values of the operation type signals in registers 30 and 40 were reversed, then chip MC0 would respond to command A by turning on ODT 38 and to command B by performing a write operation; and chip MC1 would respond to command A by performing a write operation and to command B by performing an ODT operation.

As another example (called example 2), there are commands called commands C and D. An operation type signal in registers 30 and 40 could be set with particular values such that chip MC0 responds to command C as a read command and to a command D as a refresh command, whilst chip MC1 responds to command C as a refresh command and to command D as a read command.

EX1005 at 3:41-65.

79. Based on the '523 Patent's disclosure, a POSITA would understand commands that "affect accessibility of the chip" to include conventional command signals communicated via the control, address, or chip select buses.

The control command signals CMD can assume an active or inactive state. If the memory chip 1 is a DRAM memory chip, the control command signals can be, for example, the chip select signal CS for selecting the relevant memory chip for a specific operation, the write enable signal WE for enabling a write access to the memory chip, the RAS signal (row activation signal) for transmitting the word line address and for activating the word line, as well as the CAS signal (column activation signal) for transmitting the bit line address and for activating the bit line for reading data out and/or writing them into the memory cell field.

EX1001 at 3:41-51.

80. Commands A, B, C, and D are the same type of commands as the exemplary control command signals disclosed in the '523 Patent.

e. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and” [1.4]

81. This limitation is also taught by Bains. Control command signals such as commands A and B may be provided from memory controller 12 to chips MC0 and MC1 through the buses. EX1005 at 3:17-24, 41-42 (“The commands referred to in this disclosure may be provided from memory controller 12 to chips MC0 and MC1 through various ways. In some embodiments, the commands described herein are provided only through control bus 20. In other embodiments, the commands are provided through a combination of control bus 20 and address bus 24. In still other embodiments, the data bus is also used to communicate commands....In example 1, there are commands called commands A and B.”). Control circuit 32 in chip MC0 and control circuit 42 in chip MC1 receive the commands and control the operation of ODT circuitry 38 and 48, respectively, based on the commands.

In example 1, there are commands called commands A and B. Chip MC0 responds to command A as a write command, meaning that control circuitry 32 causes certain data bits on data bus 22 to be stored in core 36 of chip MC0. Chip MC1 responds to command A by turning on ODT 48. More particularly control circuitry 42 turns on ODT 48. Conversely, chip MC0 responds to command B by turning on ODT 38 and chip MC1 responds to command B as a write command. More particularly, in response to command B, control circuitry 32 turns on ODT 38 and control circuitry 42 causes data on bus 22 to be stored in core 46. In some embodiments, if the values of the operation type signals in registers 30 and 40 were reversed, then chip MC0 would respond to command A by turning on ODT 38 and to command B by performing a write operation; and chip MC1 would respond to

command A by performing a write operation and to command B by performing an ODT operation.

EX1005 at 3:41-58.

82. For example, chip MC0 responds to command A as a write command, while control circuit 42 in chip MC1 responds to command A by turning on ODT 48. EX1005 at 3:41-58. Conversely, chip MC1 responds to command B as a write command, while control circuit 32 of chip MC0 turns on ODT 38. *Id.*

83. As stated in Bains and shown in annotated Figs. 2 and 4, below, the control circuit 32 controls switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off.” EX1005 at 4:39-40, Figs. 2 and 4 (“Control circuitry 32 controls the switches and hence whether ODT 38 is ‘on.’”). Bains further teaches that the number of switches that are closed by control circuit 32 determines the amount of resistance that is applied to the data pin. EX1005 at 4:40-42 (“The number of switches closed may determine the amount of resistance in the termination. For example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.”). Furthermore, Bains discloses that the particular command received determines what resistance value is set. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44.

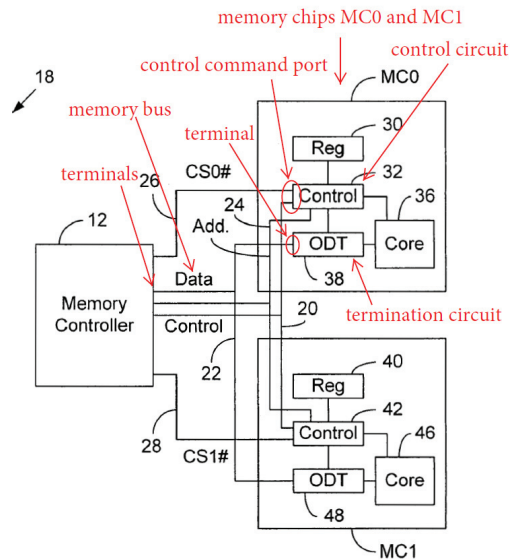


FIG. 2

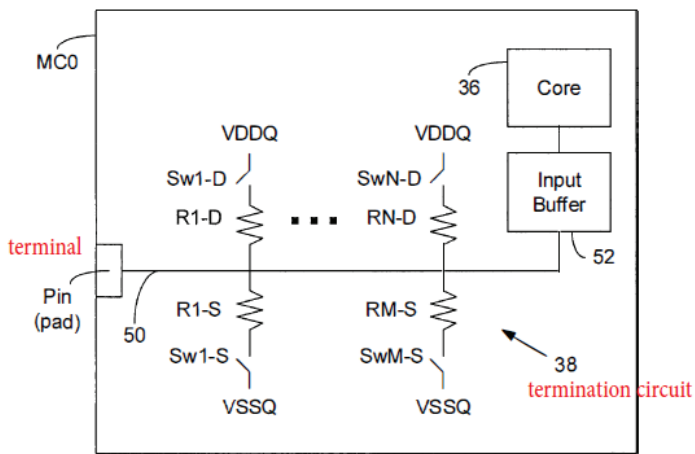


FIG. 4

f. “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,” [1.5]

84. Bains also teaches this limitation. As explained in the previous section with regards to limitation [1.4], Bains teaches that, in the embodiment illustrated in Fig. 2, the control command signals control whether ODT is “on” as well as the level of ODT resistance. *Supra* Section X.A.1.e. However, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands. EX1005 at 6:30-37 (“In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times.”). As admitted by the applicant in the Background section of the ’523 Patent, such ODT pins were well known in the art.

It has previously been provided in the case of memory chips to switch the termination on or off at a terminal of the memory chip as a

function of a termination signal. That is to say, the memory controller makes a suitable termination signal available to each of the memory chips in order to support the following read, write, or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus.

EX1001 at 1:37-44.

85. Indeed, Bains' Background section also refers to the use of such ODT pins, as prescribed by the JEDEC standards for DDR2 DRAM chips.

The JEDEC Solid State Technology Association has provided standards for DDR2 (dual data rate 2 or double data rate 2) DRAM chips. In DDR2 DRAM chips, the ODTs are controlled by using discrete signals per rank. In some two rank-1 DIMM systems, two ODT pins are used on the controller and the DIMM. Two pins may also be used per DRAM chip to support stacking solutions. As used in this disclosure, the word "pin" means traditional pins or other connections to die pads.

EX1005 at 1:37-45.

86. A POSITA (who is presumed to be familiar with JEDEC's widely used memory standards) would understand that memory chips such as DDR2 DRAMS use an ODT signal received at an ODT pin to turn termination on and off. A POSITA would further understand that the ODT signal does not vary or control the termination resistance. Because Bains explains that an ODT pin can be used in a memory system where the memory commands dictate the termination resistance value, a POSITA would have understood Bains' disclosure at 6:30-37 to include the use of an ODT pin for controlling whether ODT is "on" in addition to the use of

commands, such as the disclosed A1 and A2 commands discussed above, to indicate the amount of resistance to be applied.

87. Furthermore, to the extent that Patent Owner were to argue that this is not explicitly disclosed, it would have been obvious to a POSITA to provide such a configuration. As discussed above, the '523 Patent admits, and Bains discloses, that the use of an ODT pin to switch the termination on or off was well-known. Bains also discloses the use of command signals to set the resistance value. Based on Bains' disclosure, a POSITA would have been motivated to use an ODT pin to control whether ODT is "on" and to use commands to indicate the amount of resistance to be applied because this configuration would permit for more complex termination schemes and more customizable termination timing than a command-only control system. For example, by asserting the ODT enable signal before a command, ODT could be turned "on" before a command is asserted. In addition, by providing an ODT pin, a POSITA would also ensure compliance with JEDEC standards, which is essential for interoperability and interchangeability.

88. Lastly, a POSITA would understand that an ODT pin or pad is equivalent to a "termination port." The termination port 13 in Fig. 1 of the '523 Patent is merely a structure on the memory chip that receives a signal TermEn. EX1001, Fig. 1. An ODT pin or pad similarly connects a memory chip to the ODT bus for receiving an ODT enable signal from the memory controller.

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT

89. As discussed above, Bains teaches that the control circuit 32 controls termination circuit 38, and that termination may be turned on and off via a separate termination signal on an ODT pin. *Supra* Section X.A.1.e-f. Bains further teaches that the control circuit “performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in

accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.” As illustrated in Fig. 7 below, ODT in chip MC1 is turned on after a delay of tAOND (annotated below in pink) after command A (annotated below in blue) is asserted and turned off automatically after a fixed delay based on a burst length of 8 associated with the write command (annotated below in green).⁴ EX1005 at 5:23-42, Fig. 7 (“During clock cycle 3, the ODT in each of chips MC1-0 . . . MC1-N (rank 1) is turned on after a delay of tAOND....During clock cycle 8, the ODT in chips MC1-0 . . . MC1-N (rank 1) are turned off automatically (without a separate command) after a fixed delay based on a burst length of 8. (In some other embodiments, the ODTs are not turned off automatically.)”).

⁴ Fig. 7 is a timing diagram illustrating the operation of the system of Fig. 5, which includes a rank 0 of chips MC0-0 to MC0-N and a rank 1 of chips MC1-0 to MC1-N. EX1005 at 5:23-42. The operation of the systems in Figs. 2 and 5 are otherwise the same, and chips MC0 and MC1 in Fig. 2 operate the same as chips MC0-0 through MC0-N and MC1-0 through MC1-N in Fig. 5, respectively. EX1005 at 4:47-61.

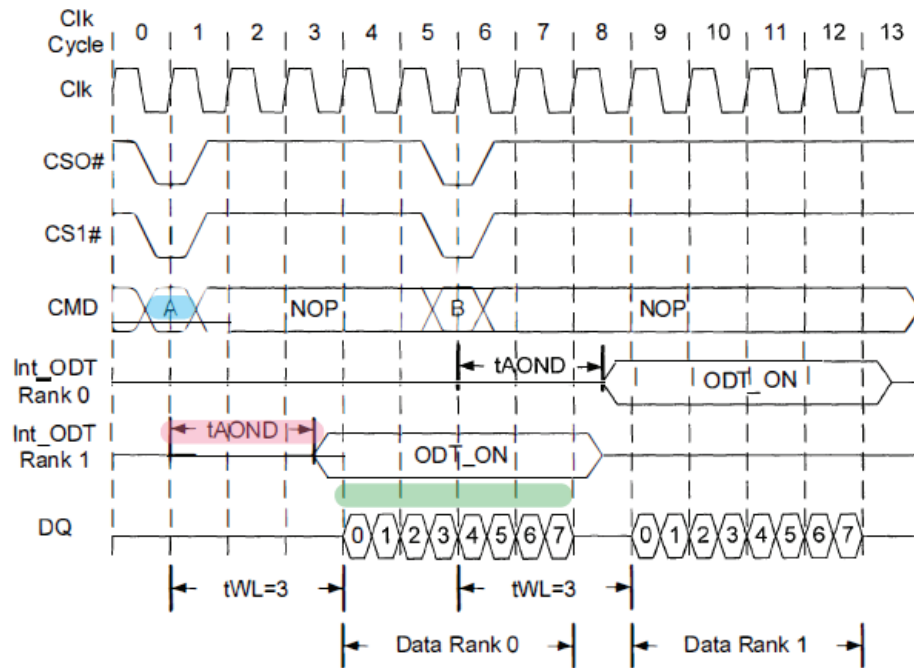


FIG. 7

90. While the first and second delays in Fig. 7 are relative to command A, when the system of Bains has an ODT pin for controlling the enabling and disabling of termination as discussed above with respect to limitation [1.5], a POSITA would have understood or have found obvious that the first and second delays are relative to the ODT signal, rather than the command signal. A POSITA would clearly recognize that any termination on and off delays must be keyed to the signal that turns termination on and off—here, the ODT signal. Thus, a POSITA would have understood that ODT is turned on after a delay of t_{AOND} after the ODT signal is asserted, and is turned off after a delay that is based on a write burst length (such that the termination is maintained throughout the write operation).

91. A POSITA would have further understood or found obvious that the timing of the second delay may alternatively be defined relative to the end of the ODT signal (i.e., relative to the ODT signal turning off), rather than the burst length. In particular, the second delay may be a fixed length of time after the ODT signal turns off. The fixed length of time may be programmed in the controller to end after the data has been written or read. A POSITA would appreciate that this is the timing scheme employed in JEDEC compliant DDR2 DRAM chips. This timing scheme is prevalent in the prior art—such as the JEDEC standard for DDR2 DRAM chips cited in Bains—and is well within the knowledge of a POSITA. EX1005 at 1:37-45; EX1006 at Fig. 16.

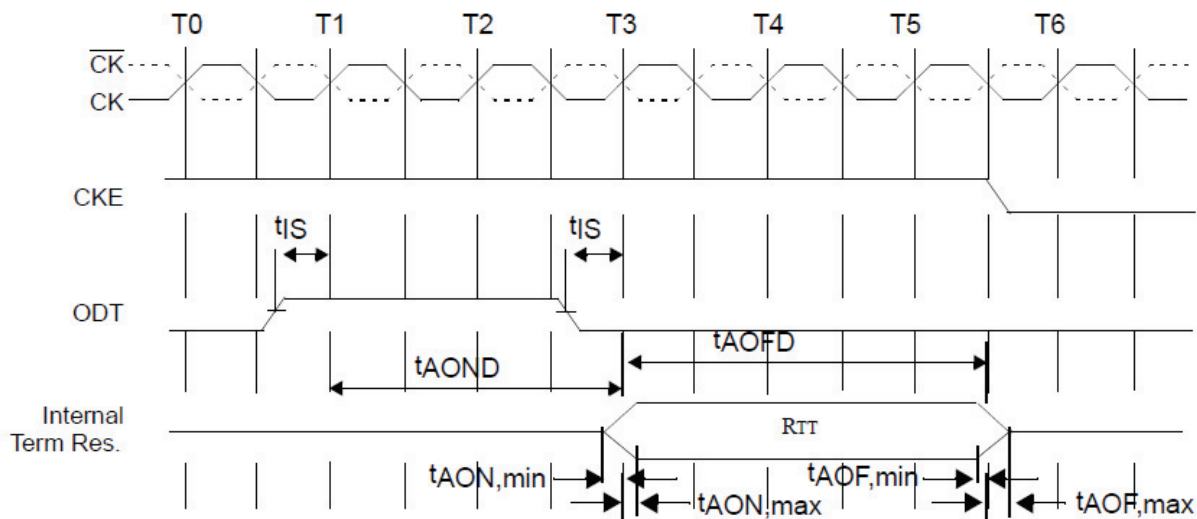


Figure 16 — ODT Timing for Active/Standby Mode

92. Furthermore, because the termination actually does occur after t_{AOND} in the timing diagram of Fig. 7, a POSITA would understand that the first time delay

tAOND is sufficiently long enough for the switches Sw1-D...SwN-D and Sw1-S...SwM-S to close and set the resistance value. It also would have been obvious to a POSITA that tAOND would be long enough to set and apply the resistance value because otherwise, at least the some of the data would be transmitted on the signal line without the proper termination in place, reducing the signal quality and defeating the purpose of ODT. *See supra* ¶¶ 53-57.

2. Claim 2: “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

93. As explained above, Bains teaches that the control circuit 32 controls switches Sw1-D...SwN-D and Sw1-S...SwM-S in the termination circuit, where the number of switches that are closed by control circuit 32 determines the amount of resistance that is applied to the data pin. EX1005 at 4:39-42; *supra* Section X.A.1.e. Bains further teaches that the number of switches closed by control circuit 32 is a function of the control command signal received by the control circuit 32. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. Thus, the termination circuit 38 may apply an infinite resistance to the terminal (open circuit, ODT “off”) or any one of a variety of finite resistances depending on which switches

Sw1-D...SwN-D and Sw1-S...SwM-S are activated by control circuitry 32 as a function of commands A1, A2...AN.

94. The first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2.

a. Mapping to a Finite Resistance and an Infinite Resistance

95. The above interpretation of “second resistance value” as including an infinite resistance value is consistent with the claims and specification of the ’523 Patent. Claims 4 and 8 recite that

the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal of the respective memory chip, and sets the resistance value to the *second resistance value substantially simultaneously with the ending of the termination* of the terminal of the respective memory chip.

EX1001 at 9:13-19 and 10:15-22 (emphasis added).

96. In particular, claims 4 and 8 state that the second resistance value is applied simultaneously with the ending of the termination. A POSITA would understand that when the termination is disabled, there is an open circuit, resulting in an infinite termination resistance. Accordingly, the second resistance value in

claims 4 and 8 must be an infinite resistance.⁵ Further, a POSITA would recognize that claims 4 and 8 merely describe the ODT system utilized in DDR2 SDRAM memory chips, where an ODT signal toggles termination on and off—or between infinite and finite resistance values. I understand that a dependent claim is narrower in scope than the claims from which it depends. Thus, because claims 4 and 8 depend from claims 2 and 6, respectively (via another dependent claim), the scope of claims 2 and 6 must also include an infinite resistance as one potential value for the second resistance.

97. Furthermore, because claims 4 and 8 require that the control circuit sets the resistance value to a first resistance value simultaneously with the switching on of the termination and to a second resistance value simultaneously with the switching off of the termination, the first and second time delays recited in claim 1, which govern the switching on and off of the termination, may be the same as the first and second predetermined switchover times recited in claim 2, which govern the switching of the termination from the first to the second resistance values. This is explicitly supported by the specification of the '523 Patent, which states that the

⁵ Other prior art references discussing ODT similarly recognize that a disabled termination circuit, which theoretically applies an infinite resistance, is understood as applying a high termination impedance value, rather than no termination impedance value. *See* EX1007 at 6:11-52 (During a read operation, the ODT circuit is deactivated and provides a “higher termination impedance.”).

“first switchover time $ODTL_{cnw}$...**may be equal to** or less than the termination switch-on time $ODTL_{on}$.” EX1001 at 5:63-65 (emphasis added).⁶

98. In Fig. 7, below, Bains demonstrates that the resistance value is set to a first resistance value based on the received command A (blue) after a first predetermined switchover time $tAOND$ (pink) and is then set to a second resistance value (infinite, closed circuit) after a second predetermined switchover time (green) based on a burst length of 8.

FIG. 7 provides an illustrative timing diagram for operation of the system of FIG. 5, although the invention is not limited to these details. During clock cycle 0, command A is issued with $CS0\#$ and $CS1\#$ asserted. During clock cycle 3, the ODT in each of chips $MC1-0 \dots MC1-N$ (rank 1) is turned on after a delay of $tAOND$. During clock cycles 4-7, data is written to chips $MC0-0 \dots MC0-N$ (rank 0) on the bus after a delay of tWL . As an example, a DDR3 memory chip may be used with a burst length (BL) of 8 and data double pumped (also called dual data rate or double data rate), meaning data is transmitted or received once each half clock cycle. Note that there is some time between the time the ODT is turned on in the chips of rank 1 and the time data is on the bus for the chips of rank 0. During clock cycle 5, command B is issued with $CS0\#$ and $CS1\#$ asserted. During clock cycle 8, the ODT in chips $MC1-0 \dots MC1-N$ (rank 1) are turned off

⁶ Indeed, Polaris also interprets claims 1 and 2 such that the time delays and the predetermined switchover times may be the same. See EX1011 at ¶¶ 52-53 (“On information and belief, the control circuit, as a function of the termination signal ODT, (1) selectively terminates the terminal with the set resistance value RTT_NOM after a first time delay, for example, $ODTL_{on} = CWL + AL - 2$, or (2) does not terminate the terminal in accordance with a second time delay, for example, $ODTL_{off} = CWL + AL - 2 \dots$. For example, as seen in the timing diagram below, the resistance value is set to a first resistance value (RTT_WR) after a first predetermined switchover time ($ODTL_{on}$), and is set to a second resistance value (RTT_NOM) after a second predetermined switchover time (e.g., $ODTL_{cwn4}$, $ODTL_{cwn8}$).”).

automatically (without a separate command) after a fixed delay based on a burst length of 8.

EX1005 at 5:23-42.

99. Where an ODT pin is employed, the resulting timing diagram would be equivalent to the ODT timing used in DDR2 DRAM chips and illustrated in JEDEC's DDR2 SDRAM specification. EX1005 at Fig. 7; EX1006 at Fig. 16.

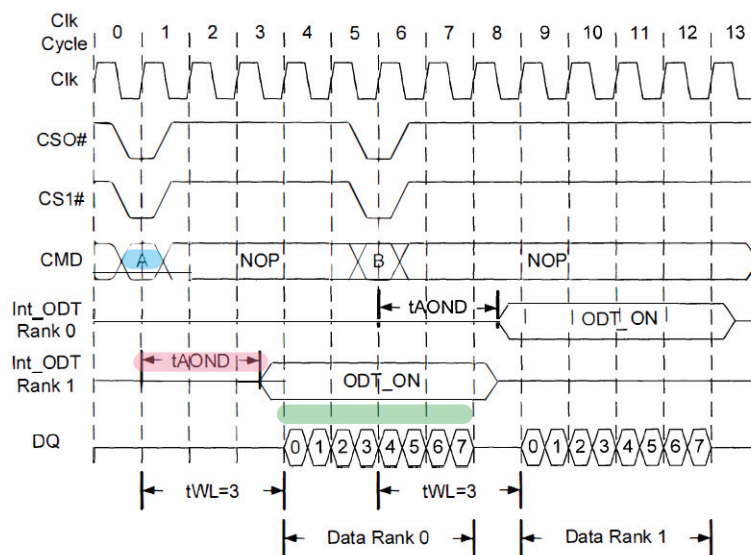


FIG. 7

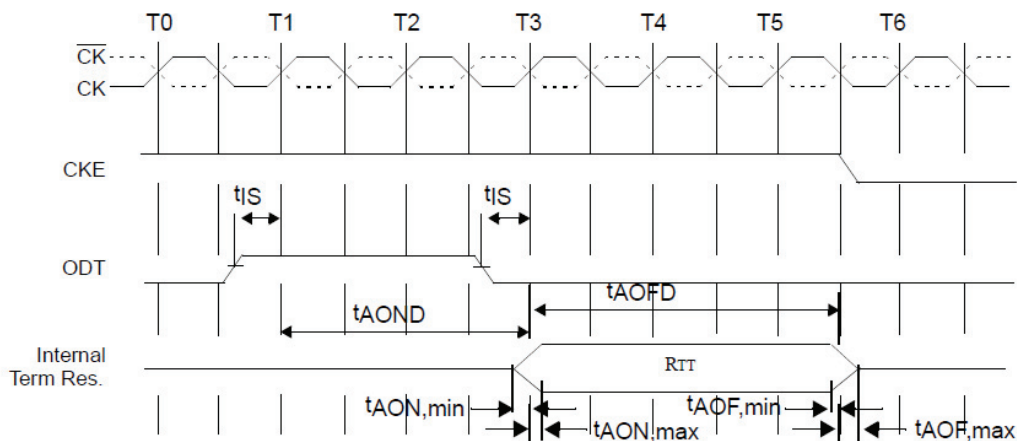


Figure 16 — ODT Timing for Active/Standby Mode

b. Mapping to Finite Resistances Associated with A1 and A2 Commands

100. The first and second resistance values recited in claim 2 are also disclosed by the two different finite resistance values applied when a command A1 is followed by a command A2. As explained above, the number of switches closed by control circuit 32 is a function of the control command signal received by the control circuit 32. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. Thus, in the situation where commands A1 and A2 are asserted back-to-back, switches Sw1-D...SwN-D and Sw1-S...SwM-S would cause “one level of resistance in the ODT” followed by “another level of resistance.”

101. The above scenario is illustrated in the following modified version of timing diagram Fig. 7, where commands A1 (orange) and A2 (yellow) are different commands to rank 0, each causing termination to be applied to rank 1. While Bains does not specify what type of commands A1 and A2 might be, a POSITA would have understood and also found obvious from Bains’ disclosure that these two commands could be any commands with which termination might be needed or desired. For example, commands A1 and A2 might be a write command and a read command respectively. Alternatively, A2 could be a chip select signal or a no operation command. *See* EX1006 at 57, Table 10. When command A1 is asserted, rank 1 is terminated with a first resistance value (light purple) after a first

predetermined switchover time (grey). When command A2 is asserted, rank 1 is terminated with a second resistance value (dark purple) after a second predetermined switchover time (dark green). EX1005 at Fig. 7 (modified and annotated). And, as noted above with respect to limitation [1.6], the first delay runs the same length of time as the first switchover time (t_{AOND}), but is triggered by an ODT “on” signal received on an ODT pin at the same time as command A1. Similarly, the second delay would be triggered by an ODT “off” signal received on an ODT pin after the A2 command (timed by the controller sending the ODT off signal to end termination once the operation associated with the A2 command has been accomplished).

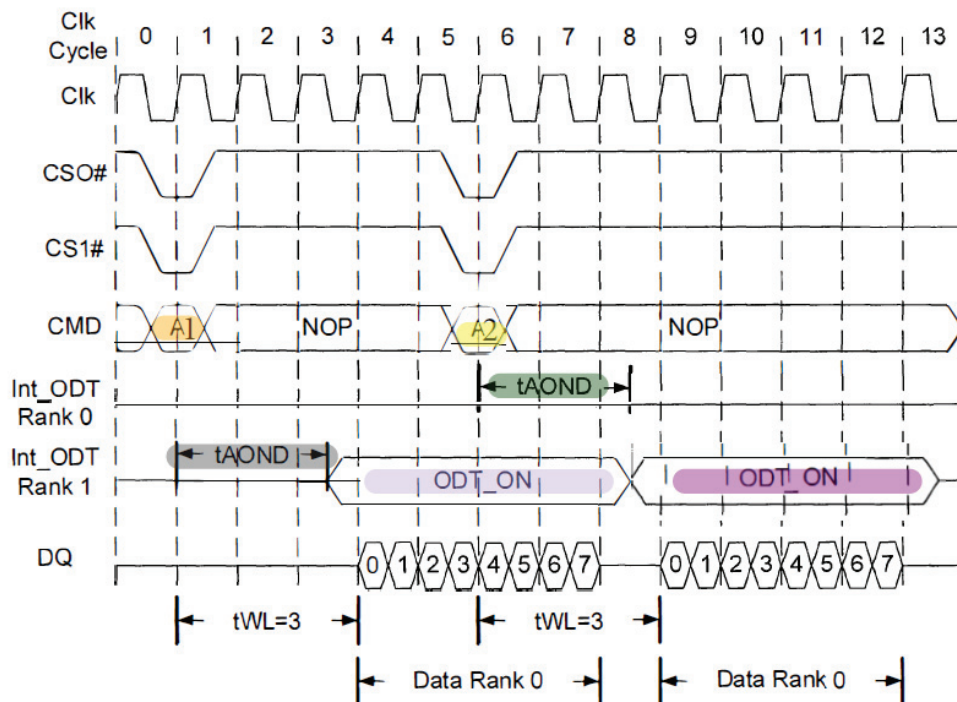


FIG. 7

102. A POSITA would have understood that the memory controller would maintain the ODT signal “on” long enough to accommodate both of the back-to-back commands A1 and A2, as this is well known in the art. See, for example, U.S. Patent No. 6,754,132 (“Kyung”), which teaches back-to-back Write (WR) and Read (RD) commands to DIMM0 (Fig. 10B) resulting in back-to-back termination on DIMM1 (Fig. 10C) by continuous ODT signal ATC1.

FIGS. 10A through 10C are timing charts of an operation of the memory system when the DiMM0 is in an active mode, and the DiMM1 is in a power down or standby mode. In this case, as described above in TABLE 1, the ATC control of the DiMM0 is off, and ATC control of the DiMM1 is carried out in an asynchronous mode. FIG. 10A illustrates the operation of the chip-set, FIG. 10B illustrates the operation of the DiMM0 module, and FIG. 10C illustrates the operation of the DiMM1 module. As shown, the chip-set issues a sequence of commands to the active DiMM0 module, including a read command RD to the DiMM0, a write command WR to the DiMM0, and another read command RD to the DiMM0.

To read the DiMM0, the active terminator of the DiMM1 must be enabled. Accordingly, the first read command RD of the chip-set is followed by an ATC1 signal which is received by the DiMM1. As shown, the DiMM1 is asynchronously responsive to the ATC1 signal to temporarily enable the active terminator thereof as shown by AT_DiMM1 of FIG. 10C. Also, during the period in which the active terminator of DiMM1 is enabled, data Ri1 is read from the DiMM0.

Likewise, to next write the DiMM0, the active terminator of the DiMM1 must be enabled. Accordingly, the write command WR of the chip-set is followed by another ATC1 signal which is received by the DiMM1. The DiMM0 is again asynchronously responsive to the ATC1 signal to enable the active terminator thereof as shown by AT_DiMM1 of FIG. 10C. At this time, data Di is written to the DiMM0.

In the example of FIGS. 10A through 10C, the second read command RD follows closely after the write command WR. As such, ACT1 signal remains high, and the active terminator of DiMM1 remains enabled throughout the second read operation. Note also, as is apparent from FIG. 10C, the disabling of the active terminator of the DiMM1 is asynchronous as well.

EX1009 at 8:42-9:32, Figs. 10A-10C (emphasis added).

FIG. 10B

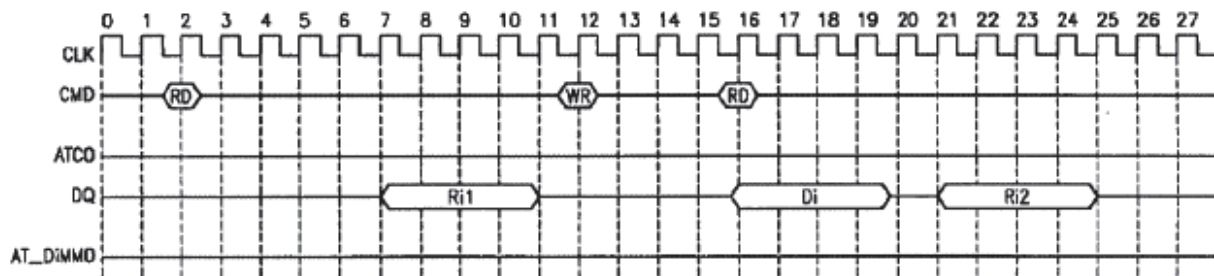
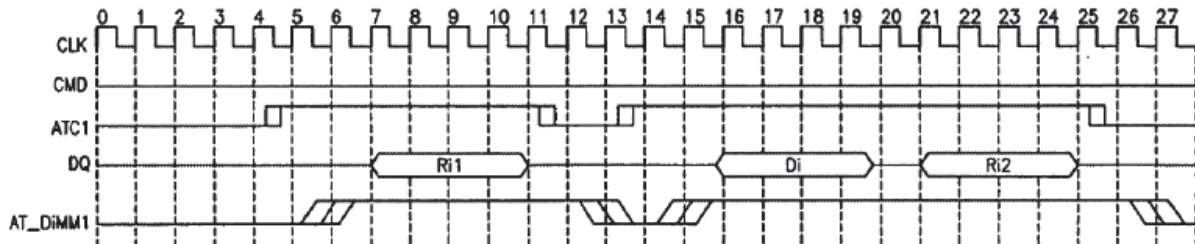


FIG. 10C



3. Claim 5:

a. “A system, comprising:” [5.P]

103. Claim 5 is similar to claim 1, but it recites additional system components, including a memory controller, a memory bus, and a plurality of memory chips, at least one chip having the features of claim 1. *Supra* Section X.A.1.

104. I understand that the preamble of claim 5 is not limiting. To the extent the preamble is limiting, Bains teaches a memory system comprising a memory controller 12 and memory chips MC0 and MC1 coupled by various buses. EX1005 at 2:33-46, Fig. 2. Exemplary memory chip MC0 has an ODT circuit 38 that may terminate a data pad with an infinite resistance or different finite resistances depending on the command A1 or A2 provided to the chip from the memory controller 12. EX1005 at 2:33-52, 3:41-58, 4:39-61, Figs. 2 and 4 (each figure reproduced below).

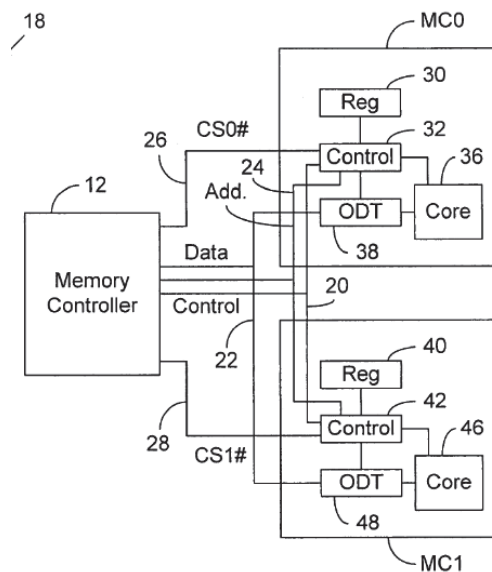


FIG. 2

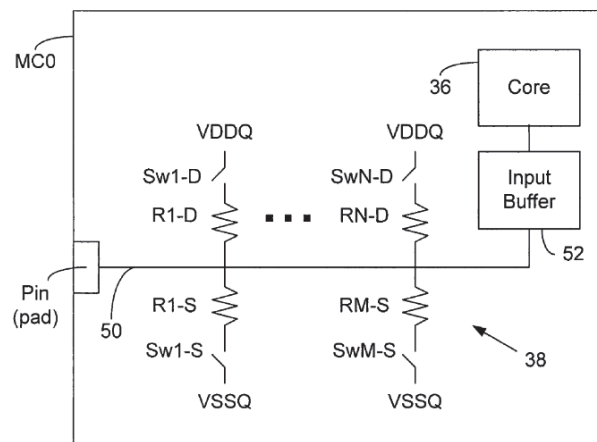


FIG. 4

b. “(a) a memory controller having a terminal;” [5.1]

105. Bains teaches this limitation. As shown below in annotated Fig. 2, Bains teaches a memory system comprising a memory controller 12 with terminals connected to a control bus 20, data bus 22, address bus 24, and chip select buses 26

and 28, through which the memory controller communicates with memory chips MC0 and MC1.

Referring to FIG. 2, memory controller 12 is coupled to chips MC0 and MC1 through a control bus 20, a data bus 22, and an address bus 24. Chip select (CS) signals are provided to chips MC0 and MC1 through buses 26 and 28. Chip select signals are sometimes active low and designated CS#. In the case of FIG. 2, the chip select signals are CS0# for chip MC0 and CS1# for chip MC1. Chip select signals are sometimes referred to as device select signals.

EX1005 at 3:9-16, Fig. 2 (annotated and reproduced below).

106. As with the memory chip “terminal” discussed with regards to limitation [1.1], a POSITA would similarly understand that the memory controller must also have pins or pads to connect to the various buses and send signals to the memory chips, and that these pins or pads would constitute “terminals.”

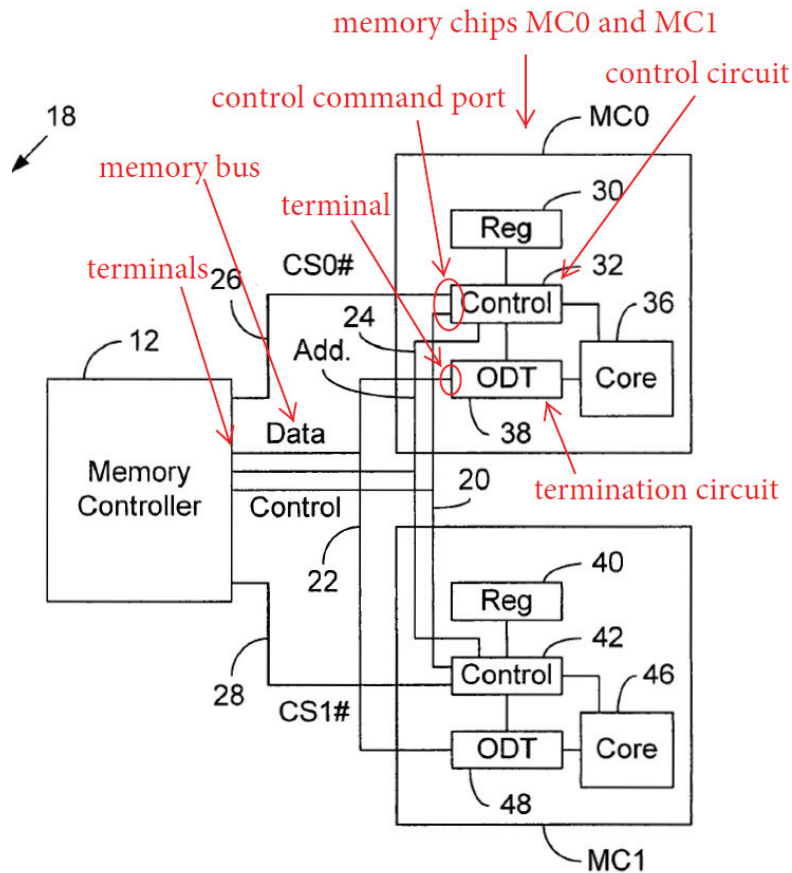


FIG. 2

c. “(b) a plurality of memory chips, at least one of the memory chips comprising:” [5.2]

107. Bains also teaches this limitation. As shown in annotated Fig. 2 above, the memory system comprises at least two memory chips MC0 and MC1. EX1005 at 2:33-36, Fig. 2; *see also* Figs. 5 and 6 (showing other embodiments with multi-chip/multi-bank memory modules).

d. “a terminal” [5.3]

108. As explained above with respect to limitation [1.1], Bains teaches limitation [5.3]. *Supra* Section X.A.1.b; *see* EX1005 at Fig. 4; EX1001 at 2:45-48, Fig. 1.

e. “a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;” [5.4]

109. As explained above with respect to limitation [1.2], Bains teaches limitation [5.4]. *Supra* Section X.A.1.c; *see* EX1005 at 4:31-44, Figs. 2, 4.

f. “a control command port for receiving a control command signal for affecting the accessibility of the memory chip; and” [5.5]

110. As explained above with respect to limitation [1.3], Bains teaches limitation [5.5]. *Supra* Section X.A.1.d; *see* EX1005 at 3:9-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51.

g. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;” [5.6]

111. As explained above with respect to limitation [1.4], Bains teaches limitation [5.6]. *Supra* Section X.A.1.e; *see* EX1005 at 3:17-24, 3:41-58, 4:39-44, Figs. 2, 4.

h. “(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and” [5.7]

112. Bains further teaches limitation [5.7]. As shown in annotated Fig. 2, below, the system includes a memory bus 22 interconnecting the terminals of the memory chips MC0 and MC1 and the terminal of the memory controller 12. EX1005 at 3:9-16, Fig. 2 (“Referring to FIG. 2, memory controller 12 is coupled to chips MC0 and MC1 through a control bus 20, a data bus 22, and an address bus 24.”).

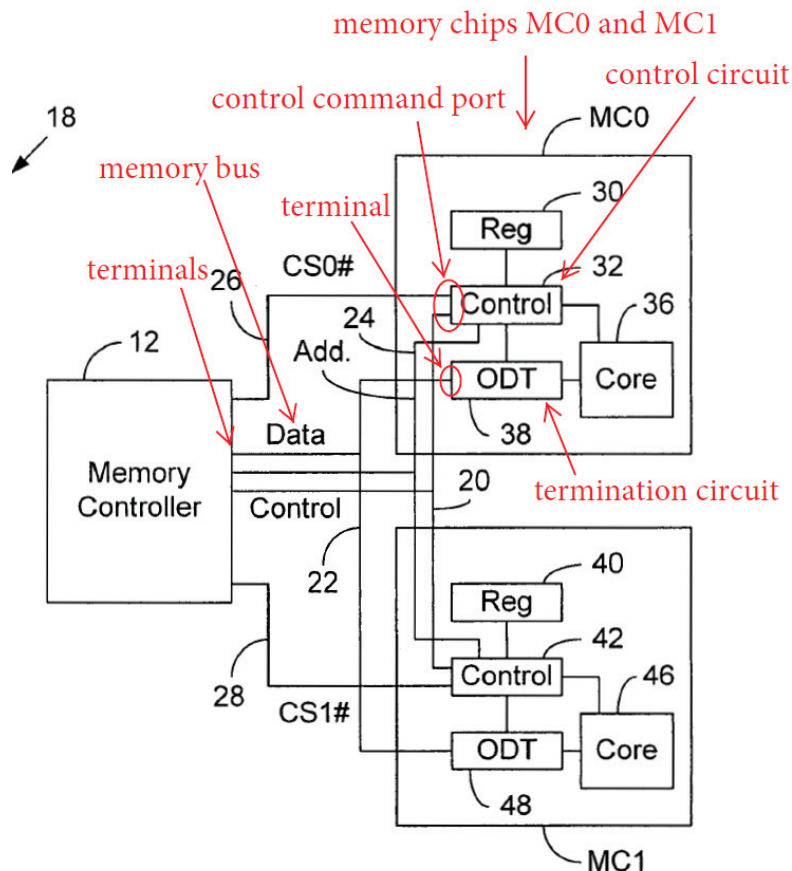


FIG. 2

i. “(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with

**the set resistance value in response to the termination signal,”
[5.8]**

113. Bain As explained above with respect to limitation [1.5], Bains teaches limitation [5.8]. *Supra* Section X.A.1.f; *see* EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig. 1.

j. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.” [5.9]

114. As explained above with respect to limitation [1.6], Bains teaches limitation [5.9]. *Supra* Section X.A.1.g; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16.

4. Claim 6: “The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

115. As explained above with respect to claim 2, Bains teaches the limitations of claim 6. *Supra* Section X.A.2; *see* EX1005 at 4:39-44, 5:23-42, Fig. 7; EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1006 at 57, Table 10, Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53.

5. Claim 9

a. “A method for operating a memory chip, comprising:” [9.P]”

116. Claim 9 is similar to claims 1 and 5, above. In particular, claim 9 recites various method steps corresponding to functionalities recited in claims 1 and 5. I understand that the preamble to claim 9 is not limiting. However, to the extent that the preamble is limiting, Bains teaches the limitation. In particular, Bains teaches a system and method for operating a memory chip (e.g., MC0) having an ODT circuit 38. EX1005 at 2:33-67, Fig. 2.

b. “receiving a control command signal for affecting accessibility of the memory chip” [9.1]

117. As explained above with respect to limitation [1.3], Bains teaches limitation [9.1]. *Supra* Section X.A.1.d; *see* EX1005 at 3:9-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51.

c. “setting a resistance value for a terminal as a function of the control command signal;” [9.2]

118. As explained above with respect to limitation [1.4], Bains teaches limitation [9.2]. *Supra* Section X.A.1.e; *see* EX1005 at 3:17-24, 3:41-58, 4:39-44, Figs. 2, 4.

d. “terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first

time delay being selected such that the selected terminating resistor can be set; and” [9.3]

119. Bains teaches this limitation. As explained above with respect to limitation [1.6], Bains teaches limitation [9.3]. *Supra* Section X.A.1.g; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16.

e. “receiving a termination enable signal, the presence of which is required for the terminating to occur.” [9.4]

120. As explained in the previous section and with respect to limitation [1.5], Bains teaches a termination enable signal received via an ODT pin which turns termination on and off. *Supra* Section X.A.5.d; *supra* Section X.A.1.f; EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig. 1.

6. Claim 10: “The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.”

121. Claim 10 is substantively the same as claim 2. In particular, claim 2 describes how the “resistance value” is set to a “first resistance value” after a “first predetermined switchover time” and is set to a “second resistance value” after a “second predetermined switchover time.” As explained above with respect to claim 2, Bains teaches the limitations of claim 10. *Supra* Section X.A.2; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at 57, Table 10, Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53. The “changed resistance value” in claim 10 may be met by either (a) the

finite resistance (dark blue) applied as a result of a first command A (light blue), where the resistance value changes from an infinite value to a finite value after a switchover time t_{AOND} (pink) relative to command A; (b) the infinite resistance applied after a switchover time based on the burst length (green) associated with the first command A (light blue), where the resistance value changes from a finite value (dark blue) to an infinite value; or (c) the finite resistance (dark purple) applied as a result of a second command A2 (yellow) that follows a first command A1 (orange), where the resistance value changes from a first finite value (light purple) to a second finite value (dark purple) after a switchover time t_{AOND} (dark green) relative to command A2 (yellow). EX1005 at Fig. 7 (annotated and modified versions below).

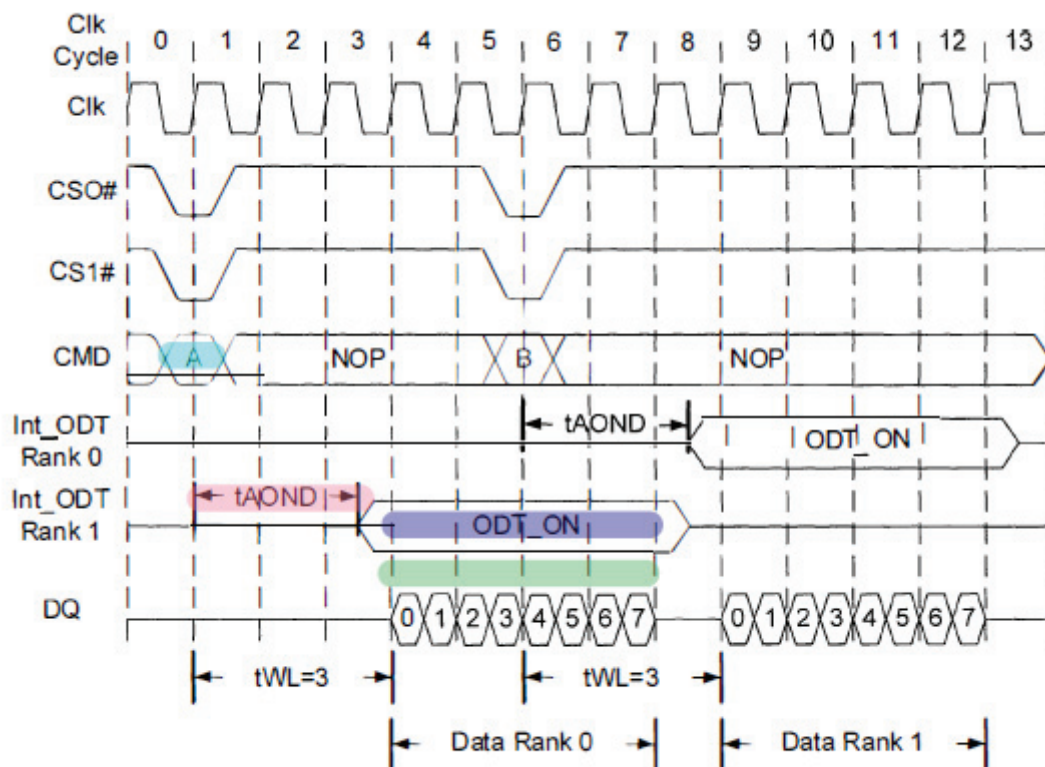


FIG. 7

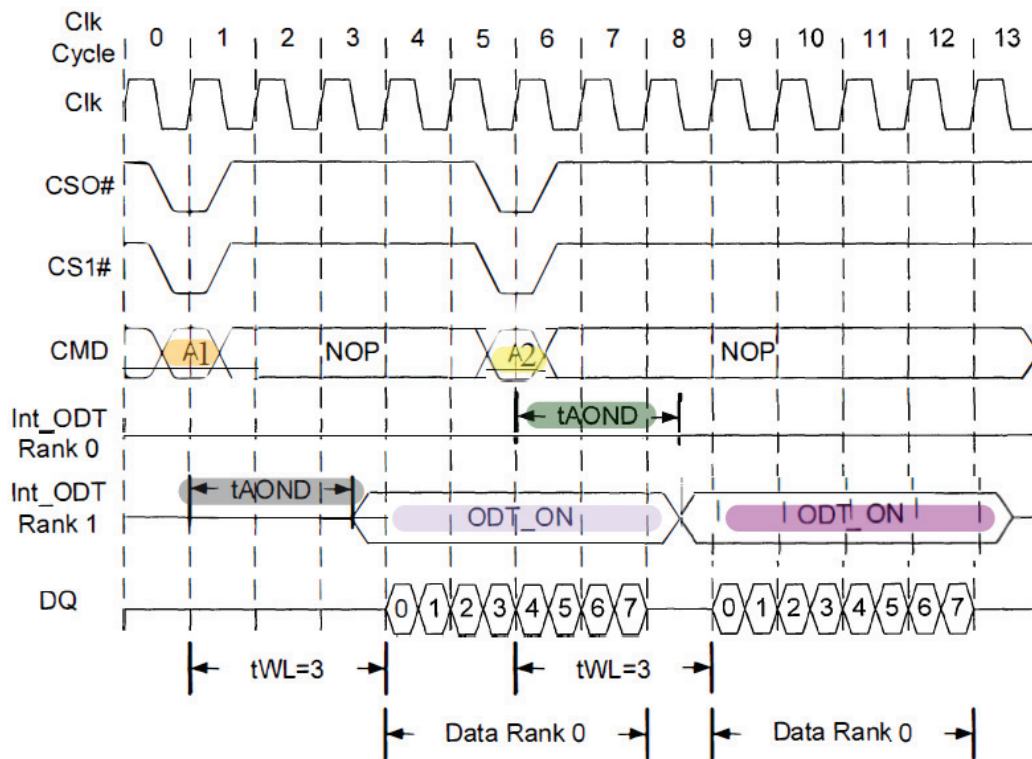


FIG. 7

B. Claims 1, 2, 5, 6, 9, and 10 are Obvious Over Bains in Combination with JESD79-2A

122. In my opinion, Bains in combination with JESD79-2A renders obvious claims 1, 2, 5, 6, 9, and 10 of the '523 Patent.

1. Combination of Bains and JESD79-2A

123. Claims 1, 2, 5, 6, 9, and 10 are also obvious over Bains in view of JESD79-2A. As explained below, JESD79-2A teaches a DDR2 SDRAM with on die termination having an ODT pin for turning termination on and off. EX1006 at 14, 26. JESD79-2A provides additional details not expressly disclosed in Bains regarding the operation of the ODT pin and associated signaling, further supporting

how a POSITA would understand Bains' teaching of using both control commands and an ODT pin to accomplish ODT.

124. A POSITA would have been motivated to combine Bains with JESD79-2A and would have had a reasonable expectation of success in doing so, because (a) JESD79-2A was and remains a well-known memory standard published by the preeminent memory standards setting organization, (b) Bains specifically teaches that the system may use ODT pins to control the termination, and (c) Bains refers to JEDEC's DDR2 standards with respect to the use of ODT pins.

The JEDEC Solid State Technology Association has provided standards for DDR2 (dual data rate 2 or double data rate 2) DRAM chips. In DDR2 DRAM chips, the ODTs are controlled by using discrete signals per rank. In some two rank-1 DIMM systems, two ODT pins are used on the controller and the DIMM. Two pins may also be used per DRAM chip to support stacking solutions. As used in this disclosure, the word "pin" means traditional pins or other connections to die pads....In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times.

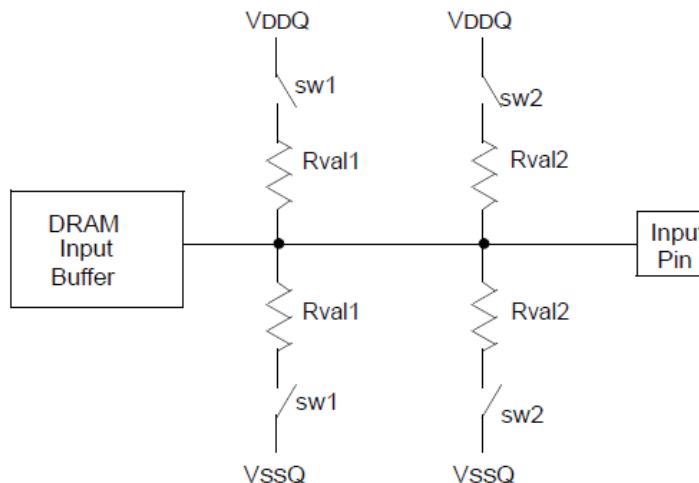
EX1005 at 1:37-45, 6:34-37.

125. Thus, to the extent that Bains does not sufficiently describe the use of ODT pins in its system, a POSITA would have been motivated by Bains' own disclosure to implement the ODT pin design taught by JESD79-2A in the memory system taught by Bains. This configuration may permit for more complex termination schemes and more customizable termination timing than a command-only control system. For example, by asserting the ODT enable signal before a

command, ODT could be turned “on” before a command is asserted. By providing an ODT pin, a POSITA would also ensure compliance with JEDEC standards, which is essential for interoperability. Furthermore, this straightforward modification simply applies a known technique (e.g., termination control with an ODT pin) to improve a similar device (e.g., Bains’ on die termination circuit with command-based resistance control) in the same way to yield predictable results (e.g. ODT control using an ODT specific signal, and resistance level control using commands).

126. In particular, and just like Bains, JESD79-2A teaches that the ODT pin in a DDR2 SDRAM turns termination on and off by controlling whether switches sw1 and sw2 in the termination circuit are enabled. EX1006 at 22, 27, Fig. 15. As shown below in Fig. 15, each set of switches sw1 and sw2 is connected to associated resistors Rval1 and Rval2 which cause a different level of resistance to be applied to the pin. However, only one set of switches, sw1 or sw2, are enabled at a time.

2.2.2.4 ODT (On Die Termination) (cont'd)

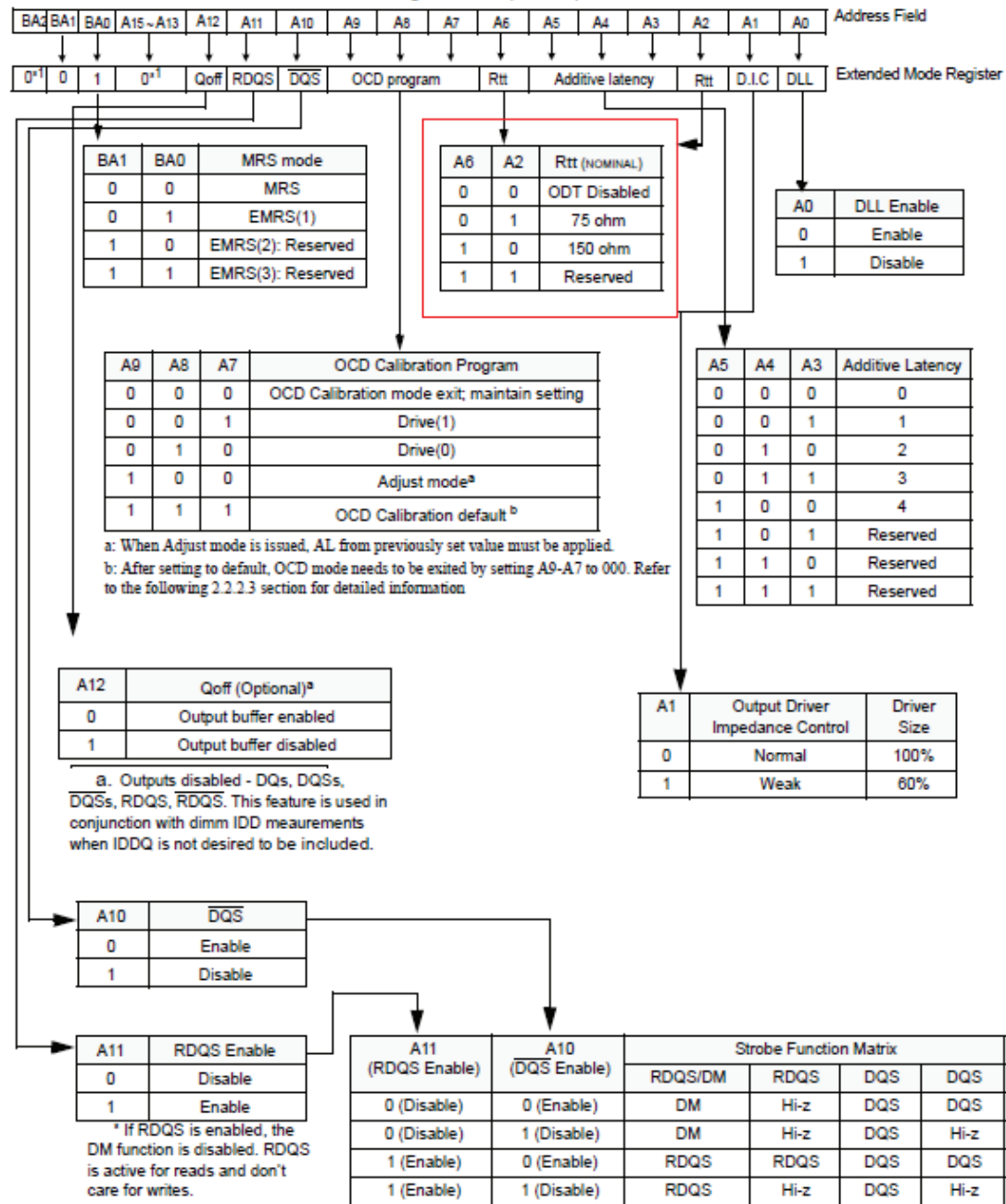


Switch sw1 or sw2 is enabled by ODT pin.
 Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
 Termination included on all DQs, DM, DQS, $\overline{DQS}$, RDQS, and $\overline{RDQS}$ pins.
 Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

127. The selection between sw1 or sw2—and thus, between the different resistances—is determined by bits A2 and A6 that are written in the EMRS. EX1006 at 27, Fig. 9 (“Selection between sw1 or sw2 is determined by ‘Rtt (nominal)’ in the EMRS”). For example, if Rval1 is associated with an effective resistance of 75 ohms, and Rval2 is associated with an effective resistance of 150 ohms, then switches sw1 are selected when bit A6 is set to 0 and bit A2 is set to 1, and switches sw2 are selected when bit A6 is set to 1 and bit A2 is set to 0. EX1006 at 27, Fig. 9. When a high level is applied to the ODT pin, switches sw1 or sw2 are closed depending on the values of bits A2 and A6.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)



^{*} BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

Figure 9 — EMRS(1) Programming

128. Bains teaches a nearly identical termination circuit with switches Sw1 to SwN and associated resistors R1 to RN, where the “number of switches closed may determine the amount of resistance in the termination.” EX1005 at 4:26-46, Fig.

4. In its illustrated embodiments, instead of using the EMRS to determine which switches should be closed, Bains uses the control command signals. “For example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:26-46.

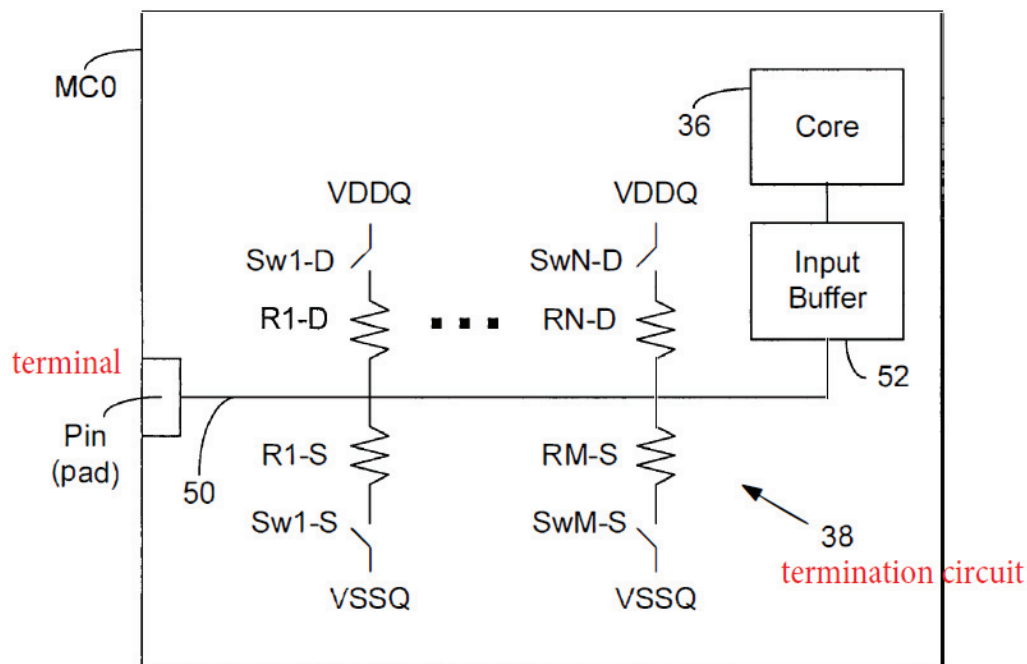


FIG. 4

129. However, as discussed above, Bains also discloses unillustrated embodiments that use an ODT pin. EX1005 at 6:30-37 (“In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times.”). Thus, Bains itself provides a teaching, suggestion, and motivation to modify the illustrated embodiments of Bains by adding an ODT pin, and it specifically refers to the DDR2

standard (a version of which is JESD79-2A) for an explanation of such ODT pins. In the combined system taught by Bains and JESD79-2A, the resistance value to be applied is a function of the control command signals as disclosed in Bains, and the ODT pin detailed in JESD79-2A is used to control when the switches are enabled to apply the selected resistance. As illustrated in Fig. 16 of JESD79-2A, below, the signal on the ODT pin determines when to apply the termination resistance.⁷ Specifically, termination is applied after a period t_{AOND} after the ODT signal is enabled (goes high), and termination ends after a period t_{AOFD} after the ODT signal is disabled (goes low). EX1006 at 27, Fig. 16. In the combination, the signal on the ODT pin controls when the switches are enabled according to first and second time delays t_{AOND} and t_{AOFD} , respectively, and control command signals A1, A2 through AN control which particular resistance level is applied.

⁷ The value of the termination to be applied is determined in JESD79-2A by the setting of EMRS bits, but the proposed combination uses Bains' improved technique of using the type of command to indicate the resistance to be applied.

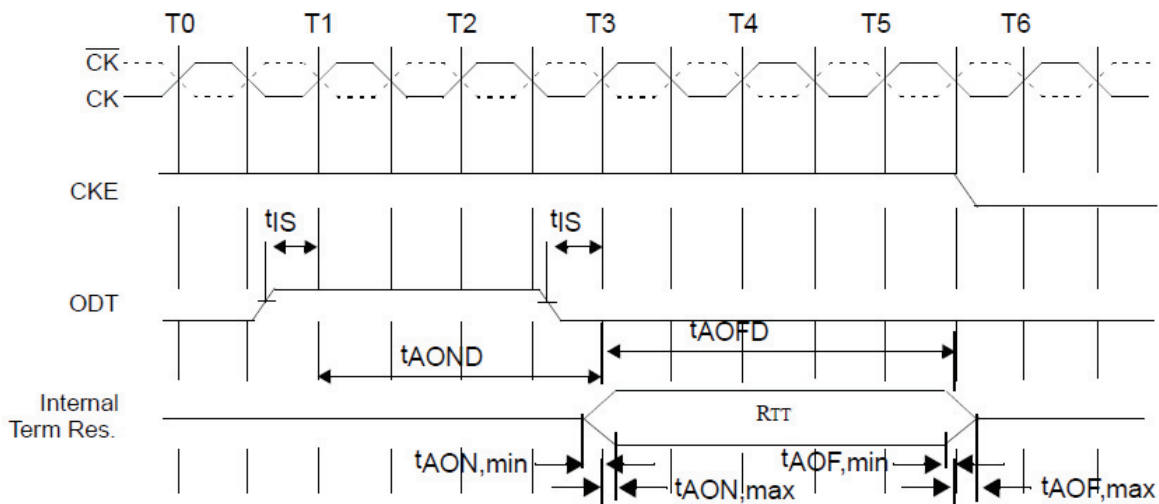


Figure 16 — ODT Timing for Active/Standby Mode

130. A POSITA would have had a reasonable expectation of success in combining Bains and JESD79-2A because the termination circuits taught by Bains and JESD79-2A are structurally similar, and Bains' control commands and JESD79-2A's EMRS bits serve analogous resistance setting functions. A POSITA would have understood that an ODT on/off pin could be used in a system with EMRS resistance control or control command resistance control to achieve the same end: separate control mechanisms for the timing of ODT and the value of ODT resistance. Thus, the combination involves the simple substitution of one known element (ODT on/off pin) for another (ODT on/off control using commands) to yield predictable results. This configuration also simplifies the system taught by Bains. Using this setup, a POSITA would not need to program chips in one rank to recognize

command A as a write and chips in another rank to recognize command A as a termination command, as is required in the illustrated embodiments of Bains:

In example 1, there are commands called commands A and B. Chip MC0 responds to command A as a write command, meaning that control circuitry 32 causes certain data bits on data bus 22 to be stored in core 36 of chip MC0. Chip MC1 responds to command A by turning on ODT 48. More particularly control circuitry 42 turns on ODT 48. Conversely, chip MC0 responds to command B by turning on ODT 38 and chip MC1 responds to command B as a write command. More particularly, in response to command B, control circuitry 32 turns on ODT 38 and control circuitry 42 causes data on bus 22 to be stored in core 46. In some embodiments, if the values of the operation type signals in registers 30 and 40 were reversed, then chip MC0 would respond to command A by turning on ODT 38 and to command B by performing a write operation; and chip MC1 would respond to command A by performing a write operation and to command B by performing an ODT operation.

EX1005 at 3:37-4:19.

131. Instead, in accordance with JEDEC standards, an ODT signal would be used to control which chips are terminated and when.

2. Claim 1

a. “A memory chip for variably setting terminations, comprising:” [1.P]

132. As explained above for Ground 1, Bains teaches the preamble of claim 1, to the extent it is limiting. *Supra* Section X.A.1.a; *see* EX1005 at 2:33-52, 3:41-58, 4:39-46, Figs. 2, 4 and 5.

b. “a terminal;” [1.1]

133. As explained above for Ground 1, Bains teaches claim limitation [1.1].

Supra Section X.A.1.b; *see* EX1005 at Fig. 4; EX1001 at 2:45-48, Fig. 1.

c. “a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;” [1.2]

134. As explained above for Ground 1, Bains teaches claim limitation [1.2].

Supra Section X.A.1.c; *see* EX1005 at 4:31-44, Figs. 2, 4.

d. “a control command port for receiving a control command signal for affecting accessibility of the memory chip;” [1.3]

135. As explained above for Ground 1, Bains teaches claim limitation [1.3].

Supra Section X.A.1.d; *see* EX1005 at 3:9-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51.

e. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and” [1.4]

136. As explained above for Ground 1, Bains teaches claim limitation [1.4].

Supra Section X.A.1.e; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs. 2, 4.

f. “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,” [1.5]

137. As explained above for Ground 1, Bains teaches claim limitation [1.5].

Supra Section X.A.1.f; *see* EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig. 1.

This limitation is also taught by Bains in view of JESD79-2A. Bains teaches that the

control command signals control whether ODT is “on” as well as the level of ODT resistance. *Supra* Section X.A.1.e. As shown in Fig. 4 below, control circuit 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off,” where the number of switches that are closed may determine the amount of resistance that is applied to the data pin. EX1005 at 4:40-42, Fig. 4 (“Control circuitry 32 controls the switches and hence whether ODT 38 is ‘on.’”). The number of switches closed is a function of the received control command signal. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. However, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands. EX1005 at 6:30-37 (“In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times.”).

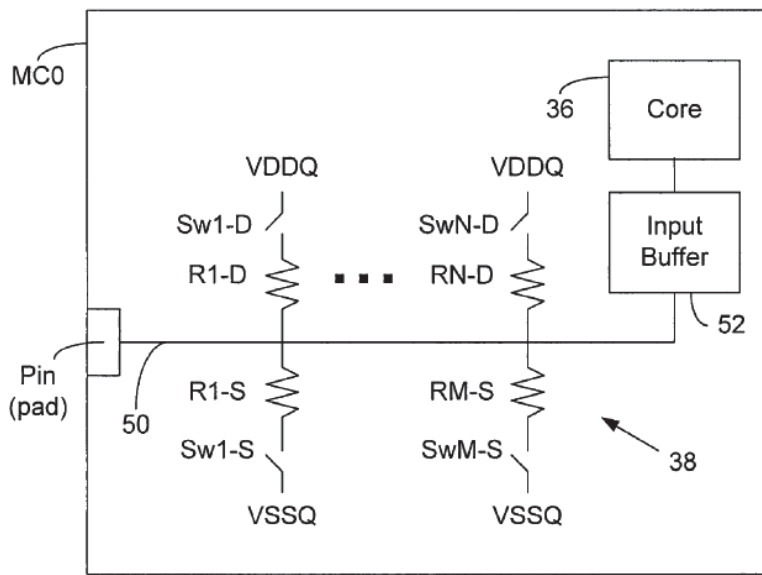
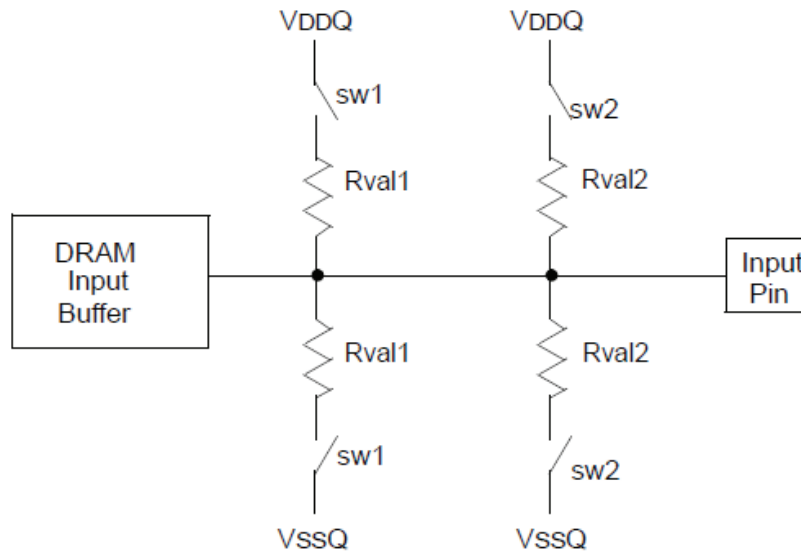


FIG. 4

138. JESD79-2A teaches a DDR2 SDRAM with an ODT pin for turning termination on and off. EX1006 at 22, 27. In particular, as shown in Fig. 15 below, the ODT pin determines whether switches sw1 or sw2 in the termination circuit are enabled, where selection between sw1 or sw2 is determined by the EMRS. EX1006 at 27, Fig. 15.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{DQS}$, RDQS, and $\overline{RDQS}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

139. In the combined system taught by Bains and JESD79-2A, the resistance value to be applied is a function of the control command signals as disclosed in Bains, and the ODT pin detailed in JESD79-2A is used to control when the switches are enabled to apply the selected resistance. In other words, the ODT pin controls when the switches are enabled according to first and second time delays tAOND and tAOFD, respectively (see Fig. 16, below), and control command signals A1, A2 through AN control which resistance level is applied, as discussed in Ground 1 with respect to limitation [1.4]. EX1006 at 27, Fig. 16.

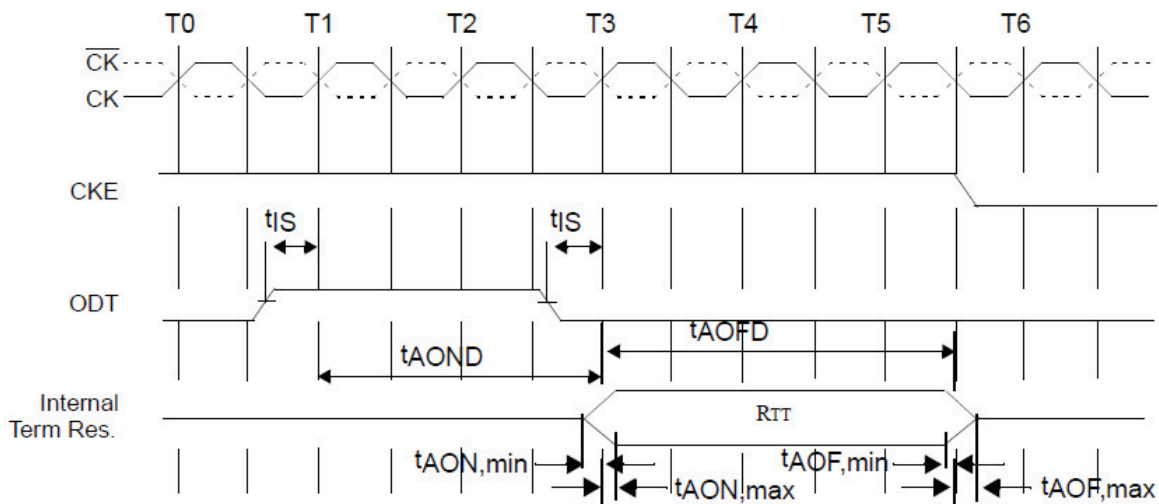


Figure 16 — ODT Timing for Active/Standby Mode

g. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.” [1.6]

140. As explained above with respect to limitation [1.5] in Ground 2, Bains as modified by JESD79-2A teaches claim limitation [1.6]. *Supra* Section X.B.1.f; *see* EX1006 at Fig. 16. Specifically, Bains as modified by JESD79-2A teaches that the chip’s control circuit terminates the terminal as a function of the termination signal ODT (pink) after a first time delay tAOND (green) that runs from when the ODT signal goes high (on), and does not terminate the terminal after a second time delay tAOFD (purple) that runs from when the ODT signal goes low (off). EX1006 at Fig. 16 (annotated below). The values of the first and second delays tAOND and tAOFD are further described in Table 36. EX1006 at 73, Fig. 16.

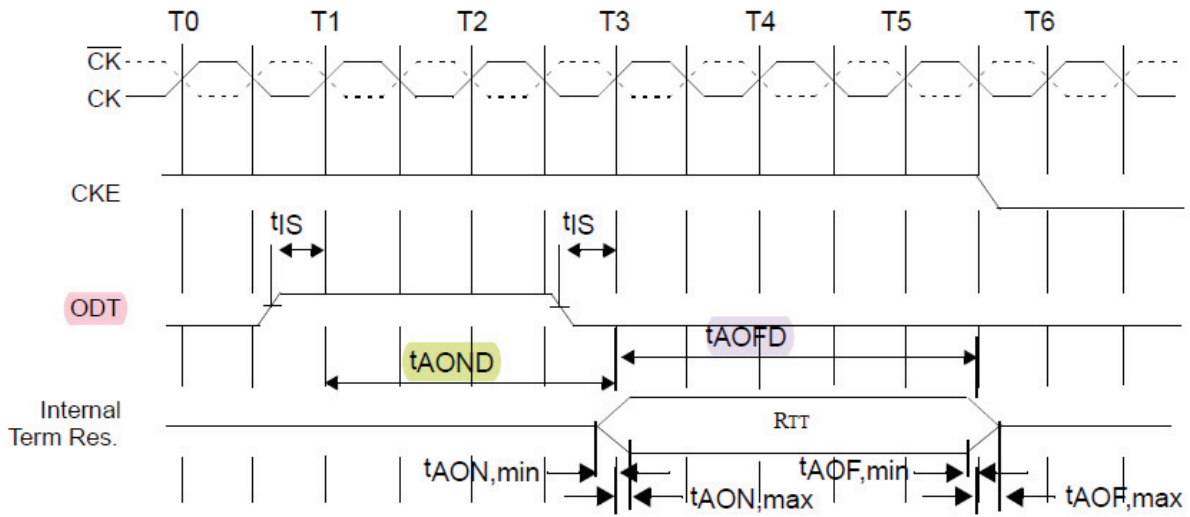


Figure 16 — ODT Timing for Active/Standby Mode

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ output access time from CK/ CK	t_{AC}	-600	+600	-500	+500	ps	
DQS output access time from CK/ CK	t_{DQSCK}	-500	+500	-450	+450	ps	
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	tCK	
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	tCK	
CK half period	t_{HP}	$\min(t_{CL}, t_{CH})$	x	$\min(t_{CL}, t_{CH})$	x	ps	11,12
Clock cycle time, CL=x	t_{CK}	5000	8000	3750	8000	ps	15
DQ and DM input hold time	t_{DH}	400	x	350	x	ps	6,7,8,18
DQ and DM input setup time	t_{DS}	400	x	350	x	ps	6,7,8,18
Control & Address input pulse width for each input	t_{IPW}	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	t_{DIPW}	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/ $\overline{CK}$	t_{HZ}	x	$t_{AC} \text{ max}$	x	$t_{AC} \text{ max}$	ps	
Data-out low-impedance time from CK/ $\overline{CK}$	t_{LZ}	$t_{AC} \text{ min}$	$t_{AC} \text{ max}$	$t_{AC} \text{ min}$	$t_{AC} \text{ max}$	ps	
DQS-DQ skew for DQS and associated DQ signals	t_{DQSQ}	x	350	x	300	ps	13
DQ hold skew factor	t_{QHS}	x	450	x	400	ps	12

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	t _{CKE}	3		3		tCK	
ODT turn-on delay	t _{AOND}	2	2	2	2	tCK	
ODT turn-on	t _{AON}	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	t _{AONPD}	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
ODT turn-off delay	t _{AOFD}	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	t _{AOF}	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17
ODT turn-off (Power-Down mode)	t _{AOFPD}	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

141. Furthermore, because the termination actually does occur after tAOND in the timing diagram of Fig. 16, a POSITA would understand that the first time delay tAOND is sufficiently long enough for the switches Sw1 and Sw2 to close and set the resistance value. It also would have been obvious to a POSITA that tAOND would be long enough to set and apply the resistance value because otherwise, at least the some of the data would be transmitted on the signal line without the proper

termination in place, reducing the signal quality and defeating the purpose of ODT.

See supra ¶¶ 53-57.

3. Claim 2: “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

142. As explained above for Ground 1, Bains teaches the additional limitations of claim 2. *Supra* Section X.A.2; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at 57, Table 10, Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53. In particular, Bains teaches that the first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2.

4. Claim 5

a. “A system, comprising:” [5.P]

143. As explained above for Ground 1, to the extent that the preamble is limiting, Bains teaches limitation [5.P]. *Supra* Section X.A.3.a; *see* EX1005 at 2:33-52, 3:41-58, 4:39-61, Figs. 2 and 4.

b. “(a) a memory controller having a terminal;” [5.1]

144. As explained above for Ground 1, Bains teaches limitation [5.1]. *Supra* Section X.A.3.b; *see* EX1005 at 3:9-16, Fig. 2.

c. “(b) a plurality of memory chips, at least one of the memory chips comprising;” [5.2]

145. As explained above for Ground 1, Bains teaches limitation [5.2]. *Supra* Section X.A.3.c; *see* EX1005 at 2:33-36, Figs. 2, 5, and 6.

d. “a terminal” [5.3]

146. As explained above for Ground 1, Bains teaches limitation [5.3]. *Supra* Section X.A.3.d; *see* EX1005 at Fig. 4; EX1001 at 2:45-48, Fig. 1.

e. “a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;” [5.4]

147. As explained above for Ground 1, Bains teaches limitation [5.4]. *Supra* Section X.A.3.e; *see* EX1005 at 4:31-44, Figs. 2, 4.

f. “a control command port for receiving a control command signal for affecting the accessibility of the memory chip; and” [5.5]

148. As explained above for Ground 1, Bains teaches limitation [5.5]. *Supra* Section X.A.3.f; *see* EX1005 at 3:9-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51.

g. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;” [5.6]

149. As explained above for Ground 1, Bains teaches limitation [5.6]. *Supra* Section X.A.3.g; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs. 2, 4.

h. “(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and” [5.7]

150. As explained above for Ground 1, Bains teaches limitation [5.7]. *Supra* Section X.A.3.h; *see* EX1005 at 3:9-16, Fig. 2.

i. “(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,” [5.8]

151. As explained above for Ground 1, Bains teaches limitation [5.8]. *Supra* Section X.A.3.i; *see* EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-44, Fig. 1. In addition, the limitation is also taught by Bains in view of JESD79-2A, as explained with respect to limitation [1.5], above. *Supra* Section X.B.2.f; *see* EX1005 at 4:40-44, 6:30-37, Fig. 4; EX1006 at 22, 27, Figs. 15 and 16.

j. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in

accordance with a second time delay, the first time delay being sufficient to set the resistance value.” [5.9]

152. As explained above for Ground 1, Bains teaches limitation [5.9]. *Supra* Section X.A.3.j; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16.

5. Claim 6: “The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

153. As explained above for Ground 1, Bains teaches the limitations of claim 6. *Supra* Section X.A.4; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at 57, Table 10, Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53. In particular, Bains teaches that the first and second resistance values recited in claim 6 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2.

6. Claim 9

a. “A method for operating a memory chip, comprising:” [9.P]

154. As explained above for Ground 1, to the extent the preamble is limiting, Bains teaches limitation [9.P]. *Supra* Section X.A.5.a; *see* EX1005 at 2:33-67, Fig. 2.

b. “receiving a control command signal for affecting accessibility of the memory chip” [9.1]

155. As explained above for Ground 1, Bains teaches limitation [9.1]. *Supra* Section X.A.5.b; *see* EX1005 at 3:9-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51.

c. “setting a resistance value for a terminal as a function of the control command signal;” [9.2]

156. As explained above for Ground 1, Bains teaches limitation [9.2]. *Supra* Section X.A.5.c; *see* EX1005 at 3:17-24, 3:41-58, 4:39-44, Figs 2 and 4.

d. “terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and” [9.3]

157. As explained above for Ground 1, Bains teaches limitation [9.3]. *Supra* Section X.A.5.d; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16; *see supra* ¶¶ 53-57. In addition, Bains in view of JESD79-2A teaches the limitation. This is explained with respect to limitations [1.5] and [1.6] in Ground 2.

Supra Section X.B.2.f-g; *see* EX1005 at 4:40-44, 6:30-37, Fig. 4; EX1006 at 22, 27, 73, Table 36, Figs. 15, 16.

e. “receiving a termination enable signal, the presence of which is required for the terminating to occur.” [9.4]

158. As explained above for Ground 1, Bains teaches limitation [9.4]. *Supra* Section X.A.5.e; EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig. 1. The combination of Bains and JESD79-2A also teaches that the termination enable signal ODT is required to enable the switches in the termination circuit and cause terminating to occur. *Supra* Section X.B.2.f; EX1005 at 4:40-44, 6:30-37, Fig. 4; EX1006 at 22, 27, Figs. 15 and 16.

7. Claim 10: “The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.”

159. As explained above for Ground 1, Bains teaches claim 10. *Supra* Section X.A.6; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at 57, Table 10, Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53.

I, R. Jacob Baker, Ph.D., P.E., declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Dated:

2/2/2023


R. Jacob Baker, Ph.D., P.E.