I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. During this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. After relocating to Maine in 2005, I transitioned to working as a full-time Consultant for JEDEC. Since June 2005, I have continued to work as a Consultant for JEDEC, where my responsibilities include the maintenance and publication of JEDEC documents and standards. I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members. During my tenure at JEDEC, JEDEC has not changed the system it uses to maintain JEDEC documents.

XILINX EXHIBIT 1010
Page 1

4. As a Consultant, I maintain all documents approved for publishing and have access to all documents at JEDEC. I receive JEDEC documents in draft form and prepare them for publishing. I also edit and help draft JEDEC's manuals of operation and procedure.

5. For over 60 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing over 350 member companies, and includes key technical individuals from most device, assembly, system, and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

6. Prior to 2000, JEDEC standards were typically available for purchase from JEDEC or approved reseller IHS. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (https://www.jedec.org), where they are cataloged and indexed by keyword and technological subject matter. Most of the standards are free to download, but larger volumes are available for purchase through JEDEC's website and approved reseller IHS.

7. By 2000, the JEDEC website was publicly available and commonly used by manufacturers, companies in the microelectronics industry, and other

interested parties to access and obtain standards information pertaining to that industry. Anyone can register online at JEDEC.org to access free standards and other JEDEC publications. Registration and most published standards are free and selected standards are only available to non-members for a fee. Between approximately 2000 and 2010, a registered user was required to log in before viewing JEDEC's free download area, which featured a list of standards and documents available for download. Around 2010, the website was re-designed so that a log-in was no longer required to visit the free download area and view a list of available standards and documents—instead, login information was only required to view and download a standard or other JEDEC document.

8. To confirm my statements above regarding access to JEDEC documents via JEDEC's website, I have visited the Internet Archive to look at captures of the "FREE Download Area" login and registration pages of JEDEC's website, which occurred on June 15, 2000 and September 1, 2000, respectively: <http://web.archive.org/web/20000615041617/http:/www.jedec.org/DOWNLOAD/default.cfm> and <http://web.archive.org/web/20000901000313/http://www.jedec.org/DOWNLOAD/copyright_agreement.htm>. Printouts of these captures are attached as Exhibits A and B and are consistent with my personal recollection of the JEDEC website. I have also visited the Internet Archive to look at the first capture after the re-design

of JEDEC's website, which occurred on February 24, 2010: <http://web.archive.org/web/20100224045304/http://www.jedec.org/standards-documents/results/field_doc_type%3A%22JESD%22?order=field_doc_full_number_value&sort=asc>. A printout of this capture is attached as Exhibit C and is consistent with my personal recollection of the JEDEC website.

9. This declaration concerns the following standards published by JEDEC:

(1) JEDEC STANDARD, Configurations for Solid State Memories, JEDEC Standard No. 21-C, Release 7 (January 1997) (hereinafter, "JESD21-C Release 7");

(2) JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, Release 1 (June 2000) (hereinafter, "JESD79 Release 1");

(3) JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, Release 2 (May 2002) (hereinafter, "JESD79 Release 2");

(4) JEDEC STANDARD, DDR2 SDRAM Specification, JESD79-2A (January 2004) (hereinafter, "JESD79-2A"); and

(5) JEDEC STANDARD, Configurations for Solid State Memories, JEDEC Standard No. 21-C, Release 14 (January 2005) (hereinafter, "JESD21-C Release 14") (collectively, "the JEDEC Standards"). I have reviewed the above JEDEC standards. The copies of the JEDEC Standards attached to this declaration as Exhibits D-H are identical to the copies of the JEDEC Standards in JEDEC's files.

10. The following statements on the public availability of the JEDEC Standards as of their respective publish dates are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and published. For the JESD21-C Release 7, JESD79 Release 1, JESD79 Release 2, JESD79-2A, and JESD21-C Release 14 standards, the dates on the covers (and thus the dates the standards were published and/or posted to JEDEC's website) are January 1997, June 2000, May 2002, January 2004, and January 2005, respectively.

11. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication and seeks final review and approval to publish from the JEDEC legal department.

12. Before 2000, once legal approval was received, the JEDEC publications department made the approved document available to the JEDEC membership and members of the public through JEDEC and, for most documents except larger volumes and subscription services, through an approved reseller IHS. For larger volumes, such as JESD21-C, the date on the cover of the Standard indicates the date that it was sent to those with a subscription to the annual updating

service for the volume, in which subscribers would receive the new and/or updated replacement pages of the various modules of the Standard as they were released and insertion instructions for the new and/or updated replacement pages. In addition, copies of the entire volume, as well as any other finalized standard, would have been available for purchase from JEDEC by anyone in the public. The release indicated at the bottom of a given page of larger volumes indicates the release in which that page would have received by subscribers and would have been available for purchase by anyone in the public.

13. Since 2000, once legal approval is received, the JEDEC publications department uploads the approved documents to the JEDEC website with a brief description. When a standard is published on JEDEC's website, it becomes available in the "Standards & Documents" section, where standards are listed by title, document number, and publish date. An email announcement is then sent to the sponsoring committee and any approved resellers.

14. Based on my personal knowledge of JEDEC's policies, the JESD21-C Release 7 Standard was made publicly available in January 1997, consistent with the date notation on the first page of the Standard, through a subscription and availability for purchase by any member of the public, and the JESD79 Release 1, JESD79 Release 2, JESD79-2A, and JESD21-C Release 14 standards were made publicly available via JEDEC's website in June 2000, May 2002, January 2004, and

January 2005, respectively, consistent with the date on the cover page of each respective Standard.

15. Based on my personal knowledge of JEDEC's policies, the JESD21-C Releases 1 through 6 were also publicly available at least by January 1997, when JESD21-C Release 7 was made publicly available, through a subscription and availability for purchase by any member of the public of JESD21-C as an entire volume. Similarly, the JESD21-C Releases 1 through 13 were also publicly available at least by January 2005, when JESD21-C Release 14 was made publicly available, through a subscription and availability for purchase by any member of the public of JESD21-C as an entire volume.

16. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's typical practice was not followed. I have no reason to believe that the JESD21-C Release 7 Standard was not published and made accessible to JEDEC membership and any member of the public in January 1997. I also have no reason to believe that the JESD21-C Release 14 Standard was not published and made accessible to JEDEC membership and any member of the public in January 2005. I also have no reason to believe that the JESD79 Release 1, JESD79 Release 2, and JESD79-2A standards were not

made publicly available via JEDEC's website in June 2000, May 2002, and January 2004, respectively. I also have no reason to believe that the JESD21-C Releases 1 through 6 were not published and made accessible to any member of the public by a subscription or purchase of JESD21-C at least by January 1997, when the JESD-21C Release 7 Standard was made publicly available. I also have no reason to believe that the JESD21-C Releases 1 through 13 were not published and made accessible to any member of the public by a subscription or purchase of JESD21-C at least by January 2005, when the JESD-21C Release 14 Standard was made publicly available.

17. To further confirm my statements above regarding the JESD79 DDR Standard, I visited the Internet Archive to look at the first capture of the JEDEC website after June 2000, which occurred on August 17, 2000: <http://web.archive.org/web/20000817100341/http://www.jedec.org/Default.htm>. A printout of this capture is attached as Exhibit I and is consistent with my personal recollection of the JEDEC website. As shown in Exhibit I, the JESD79 Release 1 "DDR" Standard was featured on the JEDEC homepage, which included a link to the following page captured on August 17, 2000, which allowed anyone to download the JESD79 DDR Standard for "DDR" memory: <http://web.archive.org/web/20000817100514/http:/www.jedec.org/DOWNLOAD/pub21/HotDDR/Default.cfm>. A printout of this capture is attached as Exhibit J

and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on August 17, 2000, the JESD79 Release 1 DDR Standard was described on the JEDEC website as the "JEDEC Standard 79, Double Data Rate (DDR) SDRAM Specification (datasheet for 64Mb SDRAM)" and was available for download by the public by that date, consistent with my statements above.

18. Exhibit K is a printout of <https://web.archive.org/web/20000711020535/http://www.jedec.org/service_members/New_Members/memberco.htm>, which is a capture on July 11, 2000 of JEDEC's list of member companies as of that date. Exhibit L is a printout of <https://web.archive.org/web/20020605015448/http://www.jedec.org/service_members/New_Members/memberco.htm>, which is a capture on June 5, 2002 of JEDEC's list of member companies as of that date. Exhibit M is a printout of <https://web.archive.org/web/20040202081543/http://jedec.org:80/service_members/New_Members/memberco.cfm>, which is a capture on February 2, 2004 of JEDEC's list of member companies as of that date. Exhibit N is a printout of <https://web.archive.org/web/20051024132448/http://www.jedec.org:80/service_members/New_Members/memberco.cfm>, which is a capture on October 24, 2005 of JEDEC's list of member companies as of that date. Exhibits K, L, M, and N are consistent with my personal recollection of JEDEC's membership. The member

companies listed in Exhibit K would have had access to JESD79 Release 1 by no later than July 11, 2000. The member companies listed in Exhibit L would have had access to JESD79 Release 2 by no later than June 5, 2002. The member companies listed in Exhibit M would have had access to JESD79-2A by no later than February 2, 2004. Lastly, the members listed in Exhibit N would have had access to JESD21-C Release 14 no later than October 24, 2005.

I, Julie Carlson, do hereby declare and state that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 1/27/2023



Julie D. Carlson

Exhibit A

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JEDEC Home: **http://www.jedec.org**

Exhibit B

The Wayback Machine - http://web.archive.org/web/20000901000313/http://www.jedec.org:80/DOWNLOAD/copyright_agreement.htm



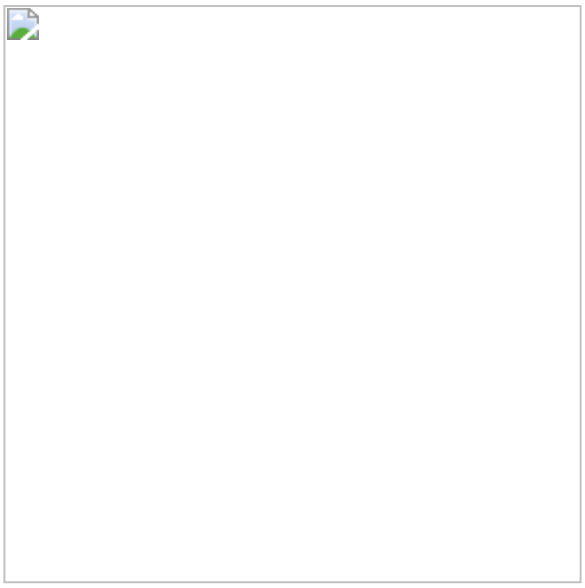
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Exhibit C

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Title	Document #	Date
LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS:	JESD1	Apr 1982

This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages.

Committee(s): JC-41

Download JESD1

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Title	Document #	Date
LOW FREQUENCY POWER TRANSISTORS:Status: Reaffirmed September 1981, October 2002	JESD10	Jan 1976

This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

Committee(s): JC-25

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Free download. Registration or login required.

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:	JESD100B.01	Dec 2002

A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, mircocontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

Committee(s): JC-10

Download JESD100B.01

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CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS:	JESD11	Dec 1984

This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

Committee(s): JC-40.2

Download JESD11

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SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET):	JESD12	Jun 1985

The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

Committee(s): JC-44

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Title	Document #	Date

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ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS:	JESD12-1B	Aug 1993

The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.

Committee(s): JC-44

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ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET:	JESD12-2	Feb 1986

The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs.

Committee(s): JC-44

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ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD:	JESD12-3	Jun 1986

This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits.

Committee(s): JC-44

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ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS:	JESD12-4	Apr 1987

This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation.

Committee(s): JC-44

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Title	Document #	Date
ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:	JESD12-5	Aug 1988

This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility.

Committee(s): JC-44

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ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:	JESD12-6	Mar 1991

This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation.

Committee(s): JC-44

Download JESD12-6

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STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES:	JESD13-B	May 1980

This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices.

Committee(s): JC-40.2

Download JESD13-B

Free download. Registration or login required.

SEMICONDUCTOR POWER CONTROL MODULES:Status: Reaffirmed June 1992, April 1999, April 2002	JESD14	Nov 1986

Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both.

Committee(s): JC-22.2

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Title	Document #	Date
THERMAL MODELING OVERVIEW	JESD15	Oct 2008

This document and the associated series of documents are intended to promote the continued development of modeling methods, while providing a coherent framework for their use by defining a common vocabulary to discuss modeling, creating requirements for what information should be included in a thermal modeling report, and specifying modeling procedures, where appropriate, and validation methods. This document provides an overview of the methodology necessary for performing meaningful thermal simulations for packages containing semiconductor devices. The actual methodology components are contained in separate detailed documents.

Committee(s): JC-15.1, JC-15

Download JESD15

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COMPACT THERMAL MODEL OVERVIEW	JESD15-1	Oct 2008

This document should be used in conjunction with the master document, JESD15, and JESD15-2, and subsidiary documents as they become available. This document is intended to function as an overview to support the effective use of Compact Thermal Model (CTM) methodologies as specified in the companion methods documents. At present, there are two such documents; JESD15-3, and JESD15-4.

Committee(s): JC-15.1, JC-15

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TWO-RESISTOR COMPACT THERMAL MODEL GUIDELINE	JESD15-3	Jul 2008

This document specifies the definition and construction of a two-resistor compact thermal model (CTM) from the JEDEC junction-to-case and junction-to-board thermal metrics. The guidance provided in this document only applies to thermal metrics defined in JEDEC standards JESD51-8 and JESD51-12. The scope of this document is limited to single-die packages that can be effectively represented by a single junction temperature.

Committee(s): JC-15

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DELPHI COMPACT THERMAL MODEL GUIDELINE	JESD15-4	Oct 2008

This guideline specifies the definition and lists acceptable approaches for constructing a compact thermal model (CTM) based on the DELPHI methodology. The purpose of this document is twofold. First, it aims to provide clear guidance to those seeking to create DELPHI compact models of packages. Second, it aims to provide users with an understanding of the methodology by which they are created and validated, and the issues associated with their use.

Title	Document #	Date

Committee(s): JC-15

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ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):Status: Reaffirmed September 2008	JESD16-A	Apr 1995

This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combing groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met. Not all sections of EIA-554 are appropriate for use by device manufacturers therefore JEDEC wishes to continue using JESD16A. In December 2008 the formulating committee approved to remove EIA-554 (July 1996, Reaffirmed September 2002) from the JEDEC website. To obtain a copy of EIA-554 please contact GEIA at http://www.geia.org/

Committee(s): JC-13

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LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999Status: Rescinded February 1999	JESD17	Aug 1988

Committee(s): JC-40.2

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STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC:	JESD18-A	Jan 1993

The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices.

Committee(s): JC-40.2

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- JC-25: Transistors (29)
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- JC-42: RAM Memory (15)
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- JC-64: Flash Memory Module (9)

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Exhibit D

JEDEC STANDARD

CONFIGURATIONS FOR SOLID STATE MEMORIES

JEDEC Standard No. 21–C Release 7

January 1997

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT





XILINX EXHIBIT 1010
Page 29

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JESD 21–C, Release 7 Insertion Instructions
Instructions for adding Release 7 to JEDEC Standard 21–C.
Inclosed with this instruction sheet are new and replacement pages for JEDEC Standard 21–C. Those pages which contain new material are labeled "Release 7" at the bottom of the page. In some cases, there will be old material on the back of the sheet containing a Release 7 page. This old material will be labeled Release 1, Release 2, Release 3, Release 4, Release 5. or Release 6 as there are no changes from the original release. All new text is marked by a "Revision Bar" in the outside margin in addition to the "Release 7" label in the inside footer of the page.

In this release, I have introduced a new feature in the Release #. In the past when an older sheet was replaced with a new one, either to make a correction, or to revise the original sheet, the new release number simply replaced the old number, thus loosing the information of the original release number. In this release, the old number will be retained followed by the letter "c" for correction, or "r" for revised, this followed by the new release number (e.f 4c7 or 6r7)

The following is a series of sheet by sheet instructions to be used to print the pages for this release. The instruction numbers correspond directly the instructions intended for the holders of the Standard. These are also included with the new originals for R–6. These instructions should be included as the first pages in Release 6. In the printing instructions, the Release # s are refered to as R#.
In the following 75 instructions, the material is arranged in 3 columns. The first column tells which sheet to remove from the 21–C binder. The second column tells which sheet to add to the binder. The third column gives an explanation of the reason for the change or addition.

REMOVE	ADD	REASON
1. Remove Cover Page	Add replacement Cover Page	Contains new Release level and date.
2. Remove Title Page;	Add replacement Title Page:	Contains revision Log for Standard.
3. Remove TOC, 8 sheets;	Add replacement TOC, 9 sheets;	Revised Table of Contents
4. Remove PP 2–3/4	Add replacement PP 2–3/4	New definitions added
5. Remove PP 2–5/6	Add replacement PP 2–5/6	
6. Remove PP 2–7/8	Add replacement PP 2–7/8	New material added.
7. Remove PP 2–9/10	Add replacement PP 2–9/10	New material added.
8. Remove P 3.5.1–3	Add replacement PP 3.5.1–3/4	New standards added
9.	Add new PP 3.5.1–33/34	New standard added
10. Remove P 3.5.2–3	Add replacement P 3.5.2–3	New standards added
11. Remove P 3.5.2–9	Add replacement PP 3.5.2–9/10	New devices added to existing standard.
12.	Add new P 3.5.2–11	New standard
13. Remove P 3.5.3–1	Add replacement P 3.5.3–1/2	Section re–orgainzed
14. Remove P 3.5.3–3/4	Add replacement PP 3.5.3–3/4	New standards added.
15. Remove P 3.5.3–5/6	Add replacement PP 3.5.3–5/6	New standard added
16. Remove P 3.5.3–7/8	Add replacement P 3.5.3–7/8	New standards added
17.	Add new P 3.5.3–9/10	New standards added
18.	Add new P 3.5.3–11/12	New standards added
19.	Add new P 3.5.3–13/14	New standards added
20.	Add new P 3.5.3–15	New standards added
21. Remove P 3.7.5–1/2	Add replacement PP 3.7.5–1/2	New standards added.
22. Remove P 3.7.5–3/4	Add replacement PP 3.7.5–3/4	New standards added.
23. Remove P 3.7.5–25/26	Add replacement PP 3.7.5–25/26	Errors corrected
24. Remove P 3.7.7–15/16	Add replacement PP 3.7.7–15/16	Errors corrected
25. Remove P 3.7.8–3	Add replacement P 3.7.8–3	Existing standard modified.

26.	Remove PP 3.7.8–9/10	Add replacement PP 3.7.8–9/10	New device added.
27.		Add new P 3.7.8–11	New standards added
28.	Remove P 3.9.1–15/16	Add replacement PP 3.9.1–15/16	New standards added.
29.	Remove P 3.9.2–3/4	Add replacement PP 3.9.2–3/4	New standards added.
30.	Remove PP 3.9.2–15/16	Add replacement PP 3.9.2–15/16	Modified drawing of existing standard.
31.	Remove PP 3.9.2–17/18	Add replacement PP 3.9.2–17/18	Modified drawing of existing standard
32.		Add new PP 3.9.2–19	New standard.
33.	Remove P 3.9.3–11/12	Add replacement P 3.9.3–11/12	Standard modified.
34.	Remove P 3.9.4–3/4	Add replacement PP 3.9.4–3/4	New standards added.
35.	Remove P 3.9.4–13/14	Add replacement PP 3.9.4–13/14	New standards added.
36.			
37.	Remove P 3.9.5–3	Add replacement P 3.9.5–3	New standards added.
38.	Remove P 3.9.5–15/16	Add replacement PP 3.9.5–15/16	New standard added.
39.	Remove P 3.10.3–1/2	Add replacement PP 3.10.3–1/2	New standards added.
40.	Remove P 3.10.3–5/6	Add replacement PP 3.10.3–5/6	Correct error.
41.		Add new PP 3.10.3–9	New standards added.
42.	Remove PP 3.10.4–3/4	Add replacement PP 3.10.4–3/4	New standards added
43.	Remove PP 3.10.4–17/18	Add replacement PP 3.10.4–17/18	New standards added
44.	Remove PP 3.10.4–19/20	Add replacement PP 3.10.4–19/20	New standards added
45.		Add new PP 3.10.4–21	New standards added
46.	Remove P 3.11.2–1	Add replacement P 3.11.2–1	New standard added.
47.	Remove P 3.11.2–3/4	Add replacement PP 3.11.2–3/4	Existing standard modified.
48.		Add new PP 3.11.2–5	New standards added
49.	Remove P 3.11.3–1	Add replacement P 3.11.3–1	New standard added.
50.	Remove P 3.11.3–3/4	Add replacement PP 3.11.3–3/4	Existing standard modified, new standard added.
51.		Add new PP 3.11.3–5	New standards added
52.	Remove P 3.11.4–1	Add replacement P 3.11.4–1/2	Standards revised.
53.	Remove P 3.11.4–3/4	Add replacement PP 3.11.4–3/4	Standards revised.
54.	Remove P 3.11.4–5/6	Add replacement PP 3.11.4–5/6	Standards revised.
55.	Remove P 3.11.4–7/8	Add replacement PP 3.11.4–7/8	Standards revised, correct error.
56.		Add new PP 3.11.4–9	New standards added.
57.	Remove PP 3.11.5–7/8	Add replacement PP 3.11.5–7/8	Correct error.
58.	Remove PP 3.11.5–9/10	Add replacement PP 3.11.5–9/10	Terminology corrections.

Section 4 on Modules has been completely re–organized. Remove and discard all of the old pages from Section 4 and replace them with the new ones supplied. No sub–dividers are supplied, but it will enhance the usability of the section by adding your own dividers. The individual sheets are not listed here as they are supplied in correct order for insertion.

JEDEC STANDARD

CONFIGURATIONS FOR SOLID STATE MEMORIES

JEDEC Standard No. 21–C Release 7

January 1997

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT

XILINX EXHIBIT 1010
Page 35

CONFIGURATIONS FOR SOLID STATE MEMORIES

Formulated under the cognizance of Committees JC–42.1, PLD devices, JC–42.3, volatile memories, JC–42.4, non–volatile memories, and JC–42.5, memory modules and cards, and approved by the JEDEC Council.

Standard 21–C Revision Log.

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Release 2, September 1991

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Contents

Section	Release #	Page #
1 BACKGROUND	Release 1	Page 1 – 1
2 TERMS AND DEFINITIONS	Release 1	Page 2 – 1
2.1 Conventional Device Pin Names	Release 6	Page 2 – 2
2.2 Multiport DRAM Pin Names	Release 3	Page 2 – 5
2.3 Power Pin Names	Release 5	Page 2 – 6
2.4 Device Type Names	Release 6	Page 2 – 7
2.5 Miscellaneous Device Related Terms	Release 1	Page 2 – 9
2.6 Special Operational Cycles for MPDRAM	Release 1	Page 2 – 10
2.7 Package–Related Terms	Release 5	Page 2 – 12
2.8 Memory Card Pin Names	Release 3	Page 2 – 13
2.9 SRAM and SSRAM special Pin Names	Release 6	Page 2–14
3 MEMORY DEVICE STANDARDS	Release 1	Page 3 – 1
3.1 General Standards	Release 1	Page 3 .1 –1
3.1.1 Bytewide	Release 1	Page 3 .1 –1
3.1.1.1 – 32K TO 256K BY 8 A/A MX FAMILY IN DIP	Release 1	Page 3 .1 –1
FIGURE 3.1–1, 32K TO 256K A/A MULTIPLEXED MEMORY IN DIP	Release 1	Page 3 .1 –2
3.2 Read Only Memory (ROM)	Release 1	Page 3.2–1
3.2.0 ROM General Standards	Release 5	Page 3.2–2
3.2.0.1 – Mask ROM Fast Address Mode Definition	Release 5	Page 3.2–2
3.2.1 ROM, Byte Wide	Release 1	Page 3.2.1–1
3.2.1.1 – 2K TO 8K BY 8 ROM FAMILY IN DIP, TYPE A	Release 1	Page 3.2.1–1
3.2.1.2 – 4K BY 8 ROM IN DIP, Type B	Release 1	Page 3.2.1–1
3.2.1.3 – 8K TO 128K BY 8 ROM FAMILY IN DIP,	Release 1	Page 3.2.1–1
3.2.1.4 – 2K TO 32K BY 8 ROM FAMILY IN RCC	Release 1	Page 3.2.1–1
3.2.1.5 – 32K TO 512K BY 8 ROM FAMILY IN SOJ,	Release 1	Page 3.2.1–1
3.2.1.6 – 128K TO 1M BY 8 ROM IN DIP,	Release 1	Page 3.2.1–1
3.2.1.7 – 64K TO 512K BY 9 ROM IN DIP,	Release 1	Page 3.2.1–1
3.2.1.8 – 2 TO 64 X 16K BY 8 PAGE SELECT ROM IN DIP,	Release 1	Page 3.2.1–1
3.2.1.9 – 512K and 1M BY 8 ROM IN QFP,	Release 2	Page 3.2.1–1
FIGURE 3.2.1–1, 2K TO 8K BY 8 ROM IN DIP, TYPES A & B	Release 1	Page 3.2.1–2
FIGURE 3.2.1–2, 8K TO 128K BY 8 ROM IN DIP	Release 1	Page 3.2.1–3
FIGURE 3.2.1–3, 2K TO 32K BY 8 ROM IN CC	Release 1	Page 3.2.1–4
FIGURE 3.2.1–4, 32K TO 512K BY 8 ROM IN SOJ	Release 1	Page 3.2.1–5
FIGURE 3.2.1–5, 128K TO 1M BY 8 ROM IN DIP	Release 1	Page 3.2.1–6
FIGURE 3.2.1–6, 64K TO 512K BY 9 ROM IN DIP	Release 1	Page 3.2.1–7
FIGURE 3.2.1–7, 2 TO 64 X 16K BY 8 PAGE SELECT	Release 1	Page 3.2.1–8
FIGURE 3.2.1–8, 512K AND 1M BY 8 ROM IN QFP	Release 2	Page 3.2.1–9
3.2.2 ROM, Word Wide	Release 1	Page 3.2.2–1
3.2.2.1 – 32K TO 256K BY 16 ROM IN DIP	Release 1	Page 3.2.2–3
3.2.2.2 – 32K TO 256K BY 16 ROM IN SCC	Release 1	Page 3.2.2–3
3.2.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN DIP	Release 1	Page 3.2.2–3
3.2.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN RCC	Release 1	Page 3.2.2–3
3.2.2.5 – 256K and 512K BY 16 ROM IN QFP	Release 2	Page 3.2.2–3
3.2.2.6 – 512K TO 128M BY 16 ROM IN DIP AND SOP	Release 6	Page 3.2.2–3
3.2.2.7 – 512K and 1M BY 16 ROM IN SCC	Release 3	Page 3.2.2–3
FIGURE 3.2.2–1, 32K TO 256K BY 16 ROM IN DIP	Release 1	Page 3.2.2–5
FIGURE 3.2.2–2, 32K TO 256K BY 16 ROM IN CC	Release 1	Page 3.2.2–6

Section	Release #	Page #
FIGURE 3.2.2–3, 16K TO 256K BY 16 AQ MX ROM IN DIP	Release 1	Page 3.2.2–7
FIGURE 3.2.2–4, 16K TO 256K BY 16 AQ MX ROM IN CC	Release 1	Page 3.2.2–8
FIGURE 3.2.2–5, 256K AND 512K BY 16 ROM IN QFP	Release 2	Page 3.2.2–9
FIGURE 3.2.2–6, 4M TO 128M BY 16 ROM IN DIP AND SOP	Release 2	Page 3.2.2–10
FIGURE 3.2.2–7, 512K & 1M BY 16 ROM IN SCC	Release 3	Page 3.2.2–11
FIGURE 3.2.2–8, 512K TO 2M BY 16 ROM IN DIP AND SOG	Release 6	Page 3.2.2–12
3.3 Programmable Read Only Memory (PROM)	**Release 1**	**Page 3.3–1**
3.3.1 PROM, Nibble Wide	**Release 1**	**Page 3.3.1–1**
3.3.1.1 – .25K & .5K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1–3
3.3.1.2 – .25K BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1–3
3.3.1.3 – 1K & 2K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1–3
3.3.1.4 – 1K & 2K BY 4 TTL PROM IN SOP	Release 1	Page 3.3.1–3
3.3.1.5 – 4K TO 8K BY 4 TTL PROM IN DIP	Release 2	Page 3.3.1–3
3.3.1.6 – .25K TO 2K BY 4 TTL PROM FAMILY IN RCC	Release 1	Page 3.3.1–3
3.3.1.7 – 4K BY 4 TTL PROM, 4K BY 4 TTL RPROM IN SCC	Release 1	Page 3.3.1–3
3.3.1.8 – 1K TO 8K TTL BY 4 PROM FAMILY IN RCC	Release 1	Page 3.3.1–3
3.3.1.9 – 1K TO 8K TTL BY 4 PROM FAMILY IN SCC	Release 1	Page 3.3.1–3
3.3.1.10 – 1K TO 4K BY 4 DPROM FAMILIES IN DIP & SCC	Release 1	Page 3.3.1–4
3.3.1.11 – 1K TO 16K BY 4 ECL PROM FAMILY IN DIP	Release 1	Page 3.3.1–4
FIGURE 3.3.1–1, .25K TO 2K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1–5
FIGURE 3.3.1–2, 256 BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1–6
FIGURE 3.3.1–3, 1K & 2K BY 4 TTL PROM IN SOG	Release 1	Page 3.3.1–7
FIGURE 3.3.1–4, 4K AND 8K BY 4 TTL PROM IN DIP	Release 2	Page 3.3.1–8
FIGURE 3.3.1–5, .25K TO 4K BY 4 TTL PROM FAMILY IN CC	Release 1	Page 3.3.1–9
FIGURE 3.3.1–6, 1K TO 8K BY 4 TTL PROM IN RCC	Release 1	Page 3.3.1–10
FIGURE 3.3.1–7, 1K TO 8K BY 4 TTL PROM IN SCC	Release 1	Page 3.3.1–11
FIGURE 3.3.1–8, 1K TO 4K BY 4 TTL DPROM IN DIP	Release 1	Page 3.3.1–12
FIGURE 3.3.1–9, 1K TO 4K BY 4 DPROM IN CC	Release 1	Page 3.3.1–13
FIGURE 3.3.1–10, 1K TO 16K BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1–14
3.3.2 PROM, Bytewide	**Release 1**	**Page 3.3.2–1**
3.3.2.1 – 32 BY 8 TTL PROM IN DIP & SCC	Release 1	Page 3.3.2–3
3.3.2.2 – 32 BY 8 ECL PROM IN DIP & SCC	Release 1	Page 3.3.2–3
3.3.2.3 – .25K & .5K BY 8 TTL PROM IN DIP & SCC	Release 1	Page 3.3.2–3
3.3.2.4 – .25K TO 8K BY 8 TTL PROM FAMILY IN DIP	Release 1	Page 3.3.2–3
3.3.2.5 – .5K TO 4K BY 8 TTL LPROM FAMILY IN DIP	Release 1	Page 3.3.2–3
3.3.2.6 – .5K TO 4K BY 8 TTL RPROM FAMILY IN DIP	Release 1	Page 3.3.2–3
3.3.2.7 – .5K TO 8K BY 8 TTL PROM FAMILIES IN RCC & SCC	Release 1	Page 3.3.2–3
3.3.2.8 – .5K TO 2K BY 8 TTL RPROM FAMILY IN SCC	Release 1	Page 3.3.2–4
3.3.2.9 – 16K TO 64K BY 8 TTL PROM FAMILY IN DIP	Release 1	Page 3.3.2–4
3.3.2.10 – 512 BY 8 ECL RPROM IN DIP & SCC	Release 2	Page 3.3.2–4
FIGURE 3.3.2–1, 32 BY 8 TTL & ECL PROM IN DIP	Release 1	Page 3.3.2–5
FIGURE 3.3.2–2, 32, 256, & 512 BY 8 TTL PROM IN CC, 32 BY 8 ECL PROM IN CC	Release 1	Page 3.3.2–6
FIGURE 3.3.2–3, 256 & 512 BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2–7
FIGURE 3.3.2–4, .25K TO 8K BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2–8
FIGURE 3.3.2–5, .5K TO 4K BY 8 TTL LPROM IN DIP	Release 1	Page 3.3.2–9
FIGURE 3.3.2–6, .5K TO 4K BY 8 TTL RPROM IN DIP	Release 1	Page 3.3.2–10
FIGURE 3.3.2–7, .5K TO 8K BY 8 TTL PROM IN SCC	Release 1	Page 3.3.2–11
FIGURE 3.3.2–8, .5K TO 8K BY 8 TTL PROM IN RCC	Release 1	Page 3.3.2–12
FIGURE 3.3.2–9, .5K TO 2K BY 8 RPROM IN CC	Release 1	Page 3.3.2–13
FIGURE 3.3.2–10, 16K TO 64K BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2–14
FIGURE 3.3.2–11, 512 BY 8 10K & 100K ECL RPROM IN DIP AND SCC	Release 2	Page 3.3.2–15

Release 7

XILINX EXHIBIT 1010
Page 40

Section	Release #	Page #
3.3.3 PROM, Word Wide	Release 1	Page 3.3.3–1
3.3.3.1 – 32 AND 64 BY 16 PROM IN DIP AND SCC	Release 1	Page 3.3.3–3
FIGURE 3.3.3–1, 32 AND 64 BY 16 TTL PROM IN DIP	Release 1	Page 3.3.3–5
FIGURE 3.3.3–2, 32 AND 64 BY 16 TTL PROM IN CC	Release 1	Page 3.3.3–6
3.3.4 PROM Package Conversion	Release 1	Page 3.3.4–1
3.3.4.1 – PROM DIP TO SO CONVERSION, 16, 18, 20, 24 DIP	Release 1	Page 3.3.4–1
FIGURE 3.3.4–1, 1K AND 2K TTL PROM 18 DIP TO 20 SO CONVERSION	Release 1	Page 3.3.4–3
3.4 Erasable Programmable Read Only Memory (EPROM)	Release 1	Page 3.4–1
3.4.1 EPROM, Byte Wide	Release 1	Page 3.4.1–1
3.4.1.1 – 4K BY 8 EPROM IN DIP, TYPE A	Release 1	Page 3.4.1–3
3.4.1.2 – 4K AND 8K BY 8 EPROM IN DIP,	Release 1	Page 3.4.1–3
3.4.1.3 – 8K TO 64K BY 8 EPROM FAMILY IN DIP,	Release 1	Page 3.4.1–3
3.4.1.4 – 2K TO 512K BY 8 EPROM FAMILY IN RCC	Release 1	Page 3.4.1–3
3.4.1.5 – 32K TO 512K BY 8 EPROM FAMILY IN SOJ,	Release 1	Page 3.4.1–3
3.4.1.6 – 128K TO 1M BY 8 EPROM FAMILY IN DIP,	Release 1	Page 3.4.1–3
3.4.1.7 – 64K TO 512K BY 9 EPROM FAMILY IN DIP,	Release 1	Page 3.4.1–3
3.4.1.8 – 2 TO 64 X 16K BY 8 PAGE SELECT EPROM FAMILY IN DIP,	Release 1	Page 3.4.1–3
3.4.1.9 – 128K TO 512K BY 8 EPROM FAMILY IN TSOP–1,	Release 4	Page 3.4.1–3
FIGURE 3.4.1–1, 4K AND 8K BY 8 EPROM IN DIP, TYPES A & B	Release 1	Page 3.4.1–5
FIGURE 3.4.1–2, 8K TO 64K BY 8 EPROM IN DIP	Release 1	Page 3.4.1–6
FIGURE 3.4.1–3, 2K TO 512K BY 8 EPROM IN CC	Release 1	Page 3.4.1–7
FIGURE 3.4.1–4, 32K TO 512K BY 8 EPROM IN SOJ	Release 1	Page 3.4.1–8
FIGURE 3.4.1–5, 128K TO 1M BY 8 EPROM IN DIP	Release 1	Page 3.4.1–9
FIGURE 3.4.1–6, 64K TO 512K BY 9 EPROM IN DIP	Release 1	Page 3.4.1–10
FIGURE 3.4.1–7, 2 TO 64 X 16K BY 8 PAGE SELECT EPROM IN DIP	Release 1	Page 3.4.1–11
FIGURE 3.4.1–8, 128K TO 512K BY 8 EPROM IN TSOP–1	Release 4	Page 3.4.1–12
3.4.2 EPROM, Word Wide	Release 1	Page 3.4.2–1
3.4.2.1 – 32K TO 256K BY 16 EPROM IN DIP	Release 1	Page 3.4.2–3
3.4.2.2 – 32K TO 256K BY 16 EPROM IN SCC	Release 1	Page 3.4.2–3
3.4.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP	Release 1	Page 3.4.2–3
3.4.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC	Release 1	Page 3.4.2–3
3.4.2.5 – 512K TO 128M BY 16 EPROM or OTP IN DIP AND SOP	Release 6	Page 3.4.2–3
3.4.2.6 – 512K and 1M BY 16 EPROM IN SCC	Release 3	Page 3.4.2–3
3.4.2.7 – 64K TO 256K BY 16 EPROM IN TSOP–1	Release 4	Page 3.4.2–3
FIGURE 3.4.2–1, 32K TO 256K BY 16 EPROM IN DIP	Release 1	Page 3.4.2–5
FIGURE 3.4.2–2, 32K TO 256K BY 16 EPROM IN SCC	Release 1	Page 3.4.2–6
FIGURE 3.4.2–3, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP	Release 1	Page 3.4.2–7
FIGURE 3.4.2–4, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC	Release 1	Page 3.4.2–8
FIGURE 3.4.2–5, 4M TO 128M BY 16 EPROM OR OTP IN DIP AND SOP	Release 1	Page 3.4.2–9
FIGURE 3.4.2–6, 512K & 1M BY 16 EPROM IN CC	Release 3	Page 3.4.2–10
FIGURE 3.4.2–7, 64K BY 256K BY 16 EPROM IN TSOP–1	Release 4	Page 3.4.2–11
FIGURE 3.4.2–8, 512K TO 2M BY 16 EPROM IN DIP AND SOG	Release 6	Page 3.4.2–12
3.5 Electrically Erasable Programmable Read Only Memory (EEPROM)	Release 1	Page 3.5–1
3.5.1 EEPROM, Byte Wide	Release 1	Page 3.5.1–1
3.5.1.1 – .5K TO 2K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1–2
3.5.1.2 – 2K & 4K BY 8 EEPROM IN RCC	Release 1	Page 3.5.1–2
3.5.1.3 – 1K TO 32K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1–2
3.5.1.4 – .5K TO 32K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1–2
3.5.1.5 – 32K TO 256K BY 8 EEPROM FAMILY IN SOJ,	Release 1	Page 3.5.1–2
3.5.1.6 – 32K TO 512K BY 8 EEPROM FAMILY IN DIP,	Release 1	Page 3.5.1–2

Release 7

XILINX EXHIBIT 1010
Page 41

Section	Release #	Page #
3.5.1.7 – 32K TO 256K BY 8 EEPROM FAMILY IN RCC,	Release 1	Page 3.5.1–2
3.5.1.8 – 32K TO 256K BY 9 EEPROM FAMILY IN DIP,	Release 1	Page 3.5.1–2
3.5.1.9 – 128K TO 1M BY 8 EEPROM FAMILY IN SCC,	Release 1	Page 3.5.1–2
3.5.1.10 – 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1	Release 2	Page 3.5.1–3
3.5.1.11 – EXTENDED FEATURE SET FOR 256K BIT EEPROM	Release 2	Page 3.5.1–3
3.5.1.12 – OPTIONAL COMMAND SET FOR DUAL–SUPPLY EEPROM	Release 3	Page 3.5.1–3
3.5.1.13 – 512K BY 8 DUAL–SUPPLY EEPROM IN RCC	Release 5	Page 3.5.1–3
3.5.1.14 – 128K to 512K BY 8 SINGLE–SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP1	Release 5	Page 3.5.1–3
3.5.1.15 – 256K, 512K, &1M BY 8 DUAL–SUPPLY EEPROM IN TSOP1	Release 6	Page 3.5.1–4
3.5.1.16 – 1M TO 8M BY 8 SINGLE–SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1–4
3.5.1.17 – 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2	Release 6	Page 3.5.1–4
3.5.1.18 – 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP2	Release 7	Page 3.5.1–4
FIGURE 3.5.1–1, .5K TO 2K BY 8 EEPROM IN DIP	Release 1	Page 3.5.1–5
FIGURE 3.5.1–2, 2K & 4K BY 8 EEPROM IN RCC	Release 1	Page 3.5.1–6
FIGURE 3.5.1–3, 1K TO 32K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1–7
FIGURE 3.5.1–4, .5K TO 32K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1–8
FIGURE 3.5.1–5, 32K TO 256K BY 8 EEPROM FAMILY IN SOJ	Release 1	Page 3.5.1–9
FIGURE 3.5.1–6, 32K TO 512K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1–10
FIGURE 3.5.1–7, 32K TO 256K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1–11
FIGURE 3.5.1–8, 32K TO 256K BY 9 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1–12
FIGURE 3.5.1–9, 128K TO 1M BY 8 EEPROM FAMILY IN SCC	Release 1	Page 3.5.1–13
FIGURE 3.5.1–10, 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1	Release 2	Page 3.5.1–14
ADDENDUM 1, 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARD	Release 2	Page 3.5.1–15
FIGURE 3.5.1–11, DUAL SUPPLY EEPROM COMMAND SET	Release 3	Page 3.5.1–23
FIGURE 3.5.1–12, 512K BY 8 DUAL–SUPPLY EEPROM IN RCC	Release 5	Page 3.5.1–24
FIGURE 3.5.1–13, 128K to 512K SINGLE–SUPPLY EEPROM FAMILY IN DIP	Release 5	Page 3.5.1–25
FIGURE 3.5.1–14, 128K to 512K SINGLE–SUPPLY EEPROM FAMILY IN RCC	Release 5	Page 3.5.1–26
FIGURE 3.5.1–15, 128K to 512K SINGLE–SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1–27
FIGURE 3.5.1–16, 1M BY 8 DUAL–SUPPLY EEPROM IN TSOP1	Release 5	Page 3.5.1–28
FIGURE 3.5.1–17. 1M TO 8M SINGLE–SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1–29
FIGURE 3.5.1–18, 256K & 512K BY 8 DUAL–SUPPLY EEPROM IN TSOP1	Release 6	Page 3.5.1–30
FIGURE 3.5.1–19 A⇒C 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2	Release 6	Page 3.5.1–31⇒33
FIGURE 3.5.1–20. 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP1	Release 7	Page 3.5.1–34
3.5.2 EEPROM, Word Wide	**Release 1**	**Page 3.5.2–1**
3.5.2.1 – 4K TO 32K BY 16 EEPROM IN DIP	Release 1	Page 3.5.2–3
3.5.2.2 – 4K TO 256K BY 16 EEPROM IN SCC	Release 1	Page 3.5.2–3
3.5.2.3 – 256K TO 128M BY 16 EEPROM IN DIP AND SOG	Release 6	Page 3.5.2–3
3.5.2.4 – 1M TO 4M BY 16 DS EEPROM IN SSOP	Release 6	Page 3.5.2–3
3.5.2.5 – 1M TO 4M DENSITY, BY 8 OR 16 FEEPROM IN PSOP	Release 7	Page 3.5.2–3
3.5.2.6 – 1M TO 32M DENSITY, BY 8 OR 16 FEEPROM IN TSOP1	Release 7	Page 3.5.2–3
FIGURE 3.5.2–1, 4K TO 32K BY 16 EEPROM FAMILY IN DIP	Release 1	Page 3.5.2–5
FIGURE 3.5.2–2, 4K TO 256K BY 16 EEPROM FAMILY IN SCC	Release 1	Page 3.5.2–6
FIGURE 3.5.2–3, 4M TO 128M BY 16 EEPROM FAMILY IN DIP AND SOG	Release 2	Page 3.5.2–7
FIGURE 3.5.2–4, 256K TO 2M BY 16 EEPROM FAMILY IN DIP AND SOG	Release 6	Page 3.5.2–8
FIGURE 3.5.2–5, 1M TO 4M BY 16 DS EEPROM IN SSOP	Release 6	Page 3.5.2–9
FIGURE 3.5.2–6, 1M TO 4M DENSITY BY 8 OR16 FEEPROM IN PSOP	Release 7	Page 3.5.2–10
FIGURE 3.5.2–7, 1M TO 32M DEBSITY BY 8 OR16 FEEPROM IN PSOP	Release 7	Page 3.5.2–11
3.5.3 EEPROM EXTENDED FEATURES	**Release 1**	**Page 3.5.3–1**
3.5.3.1 – EXTENDED FEATURE SET FOR 256Kb EEPROM	Release 1	Page 3.5.3–3
3.5.3.2 – DUAL SUPPLY EEPROM COMMAND SET	Release 7	Page 3.5.3–13

Release 7

XILINX EXHIBIT 1010
Page 42

Section	Release #	Page #
3.5.3.3 – SINGLE SUPPLY EEPROM COMMAND CODES	Release 7	Page 3.5.3–14
3.5.3.4 – EEPROM TOGGLE BIT FEATURE	Release 7	Page 3.5.3–15
3.6 Non volatile Random Access Memory (NVRAM)	**Release 1**	**Page 3.6–1**
3.6.1 NVRAM, Nibble Wide	**Release 1**	**Page 3.6–3**
3.6.1.1 – .25K & 1K BY 4 NVRAM IN DIP	Release 1	Page 3.6–3
3.6.2 NVRAM, BYTE WIDE	**Release 1**	**Page 3.6–3**
3.6.2.1 – .5K, 1K BY 8 NVRAM IN DIP	Release 1	Page 3.6–3
3.6.2.2 – .5K & 1K BY 8 NVRAM IN RCC	Release 1	Page 3.6–3
3.6.2.3 – .5K TO 16K BY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6–3
3.6.2.4 – .5K TO 16K BY 8 NVRAM FAMILY IN RCC	Release 1	Page 3.6–3
3.6.2.5 – 32K TO 256K BY 8 NVRAM FAMILY IN SOJ,	Release 1	Page 3.6–3
3.6.2.6 – 32K TO 256K BY 8 NVRAM FAMILY IN DIP,	Release 1	Page 3.6–3
3.6.2.7 – 16K TO 128K BY 9 NVRAM FAMILY IN DIP,	Release 1	Page 3.6–3
FIGURE 3.6–1, .25K & 1K BY 4 NVRAM IN DIP	Release 1	Page 3.6–5
FIGURE 3.6–2, .5K & 1K BY 8 NVRAM IN DIP	Release 1	Page 3.6–6
FIGURE 3.6–3, .5K & 1K BY 8 NVRAM IN RCC	Release 1	Page 3.6–7
FIGURE 3.6–4, .5K TO 16K BY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6–8
FIGURE 3.6–5, .5K TO 16K BY 8 NVRAM FAMILY IN RCC	Release 1	Page 3.6–9
FIGURE 3.6–6, 32K TO 256K BY 8 NVRAM FAMILY IN SOJ	Release 1	Page 3.6–10
FIGURE 3.6–7, 32K TO 256K NY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6–11
FIGURE 3.6–8, 16K TO 128K BY 9 NVRAM FAMILY IN DIP	Release 1	Page 3.6–12
3.7 Static Random Access Memory (SRAM)	**Release 1**	**Page 3.7–1**
3.7.1 – JTAG Extension to Revolutionary Pinout SRAM Devices	**Release 4**	**Page 3.7–1**
FIGURE 3.7–1, JTAG ADDITION TO REVOLUTIONARY PINOUT SRAM	Release 4	Page 3.7–3
3.7.1 Bit Wide TTL SRAM	**Release 1**	**Page 3.7.1–1**
3.7.1.1 – .25K & 1K BY 1 TTL SRAM IN DIP	Release 1	Page 3.7.1–3
3.7.1.2 – .25K & 1K BY 1 TTL SRAM IN SCC	Release 1	Page 3.7.1–3
3.7.1.3 – 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.1–3
3.7.1.4 – 16K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1–3
3.7.1.5 – 64K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1–3
3.7.1.6 – 16K TO 2M BY 1 TTL SRAM IN SOJ	Release 5	Page 3.7.1–3
3.7.1.7 – 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.1–3
3.7.1.8 – 256K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1–3
3.7.1.9 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.1–3
FIGURE 3.7.1–1, 0.25K & 1K BY 1 TTL SRAM IN DIP	Release 1	Page 3.7.1–5
FIGURE 3.7.1–2, 0.25K & 1K BY 1 TTL SRAM IN SCC	Release 1	Page 3.7.1–6
FIGURE 3.7.1–3, 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.1–7
FIGURE 3.7.1–4, 16K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1–8
FIGURE 3.7.1–5, 64K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1–9
FIGURE 3.7.1–6, 16K TO 2M BY 1 TTL SRAM IN SOJ AND TSOP–2	Release 5	Page 3.7.1–10
FIGURE 3.7.1–7, 256K TO 16M BY 1 TTL SRAM AND SSRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.1–11
FIGURE 3.7.1–8, 256K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1–12
FIGURE 3.7.1–9, 4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.1–13
3.7.2 Bit Wide ECL SRAM	**Release 1**	**Page 3.7.2–1**
3.7.2.1 – 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.2–3
3.7.2.2 – 256K TO 16M BY 1 ECL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.2–3
3.7.2.3 – 64K AND 256K BY 1 ECL SRAM IN FLATPACK	Release 2	Page 3.7.2–3

Release 7

XILINX EXHIBIT 1010
Page 43

Section	Release #	Page #
3.7.2.4 – 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.2–3
FIGURE 3.7.2–1, 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.2–5
FIGURE 3.7.2–2, 256K TO 16M BY 1 ECL SRAM AND SSRAM FAMILY IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.2–6
FIGURE 3.7.2–3, 64K AND 256K BY 1 ECL SRAM IN FP	Release 2	Page 3.7.2–7
FIGURE 3.7.2–4, 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.2–8
3.7.3 Nibble Wide TTL SRAM	**Release 1**	**Page 3.7.3–1**
3.7.3.1 – 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC	Release 1	Page 3.7.3–3
3.7.3.2 – .25K BY 4 TTL SRAM IN DIP & RCC	Release 1	Page 3.7.3–3
3.7.3.3 – 256 BY 4 TTL SRAM WITH G IN SCC	Release 1	Page 3.7.3–3
3.7.3.4 – 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP	Release 1	Page 3.7.3–3
3.7.3.5 – 4K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3–3
3.7.3.6 – 4K TO 1M BY 4 TTL SRAM WITH G FAMILY IN DIP	Release 1	Page 3.7.3–3
3.7.3.7 – 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN RCC	Release 1	Page 3.7.3–3
3.7.3.8 – 16K & 64K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3–3
3.7.3.9 – 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ AND TSOP–2	Release 5	Page 3.7.3–4
3.7.3.10 – 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.3–4
3.7.3.11 – 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.3–4
3.7.3.12 – 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.3–4
3.7.3.13 – 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ	Release 1	Page 3.7.3–4
3.7.3.14 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ	Release 1	Page 3.7.3–4
FIGURE 3.7.3–1, 16 BY 4 INVERTING AND NON–INVERTING TTL SRAM IN DIP	Release 1	Page 3.7.3–5
FIGURE 3.7.3–2, 16 BY 4 INVERTING AND NON–INVERTING TTL SRAM IN SCC	Release 1	Page 3.7.3–6
FIGURE 3.7.3–3, 256 BY 4 TTL SRAM IN DIP	Release 1	Page 3.7.3–7
FIGURE 3.7.3–4, 256 BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3–8
FIGURE 3.7.3–5, 256 BY 4 TTL SRAM IN SCC	Release 1	Page 3.7.3–9
FIGURE 3.7.3–6, 4K TO 64K BY 4 TTL SRAM FAMILY WITHOUT G IN DIP	Release 1	Page 3.7.3–10
FIGURE 3.7.3–7, 4K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3–11
FIGURE 3.7.3–8, 4K TO 256K BY 4 TTL SRAM FAMILY WITH G IN DIP	Release 1	Page 3.7.3–12
FIGURE 3.7.3–9, 16K TO 256K BY 4 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.3–13
FIGURE 3.7.3–10, 16K & 64K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3–14
FIGURE 3.7.3–11, 4K TO 1M BY 4 TTL SRAM WITH AND W/O G IN SOJ AND TSOP–2	Release 1	Page 3.7.3–15
FIGURE 3.7.3–12, 64K TO 4M BY 4 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.3–16
FIGURE 3.7.3–13, 64K TO 4M BY 4 TTL SRAM FAMILY WITH SEPARATE DATA I/O IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.3–17
FIGURE 3.7.3–14, 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) FAMILY IN DIP,SOJ,AND TSOP–2	Release 4	Page 3.7.3–18
FIGURE 3.7.3–15, 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ	Release 1	Page 3.7.3–19
3.7.4 Nibble Wide ECL SRAM	**Release 1**	**Page 3.7.4–1**
3.7.4.1 – .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP	Release 1	Page 3.7.4–3
3.7.4.2 – 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP	Release 1	Page 3.7.4–3
3.7.4.3 – .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.4–3
3.7.4.4 – 16K BY 4,10K & 100K ECL SSRAM IN DIP	Release 1	Page 3.7.4–3
3.7.4.5 – 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–3
3.7.4.6 – 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–3

XILINX EXHIBIT 1010
Page 44

Section	Release #	Page #
, 3.7.4.7 – 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–4
3.7.4.8 – 64K BY 4 ECL SRAM IN FP	Release 2	Page 3.7.4–4
3.7.4.9 – 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ	Release 2	Page 3.7.4–4
3.7.4.10 – 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–4
3.7.4.11 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–4
3.7.4.12 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–4
FIGURE 3.7.4–1, 256 BY 4, 100K ECL SRAM IN DIP, 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP	Release 1	Page 3.7.4–5
FIGURE 3.7.4–2, 256 & 1K BY 4, 100K ECL SRAM IN SFP	Release 1	Page 3.7.4–6
FIGURE 3.7.4–4, 0.25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.4–7
FIGURE 3.7.4–5, 16K BY 4, 10K & 100K ECL SSRAM IN DIP	Release 1	Page 3.7.4–8
FIGURE 3.7.4–6, 64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–9
FIGURE 3.7.4–7, 64K TO 4M BY 4 ECL SRAM WITH SEPARATE I/O FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–10
FIGURE 3.7.4–8, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–11
FIGURE 3.7.4–9, 64K BY 4 ECL SRAM IN FP	Release 2	Page 3.7.4–12
FIGURE 3.7.4–10, 256K BY 4 or 512K BY 2 CONFIGURABLE ECL SRAM IN DIP AND SOJ	Release 2	Page 3.7.4–13
FIGURE 3.7.4–11, 64K TO 4M BY 4 BIT SELECTABLE ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–14
FIGURE 3.7.4–12, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–15
FIGURE 3.7.4–13, 64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.4–16
3.7.5 Byte Wide TTL SRAM	**Release 1**	**Page 3.7.5–1**
3.7.5.1 – 64 BY 9 TTL SRAM IN SCC	Release 1	Page 3.7.5–3
3.7.5.2 – 1K & 2K BY 8 TTL SRAM IN DIP	Release 1	Page 3.7.5–3
3.7.5.3 – 2K & 4K BY 8 TTL SRAM IN RCC	Release 1	Page 3.7.5–3
3.7.5.4 – 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,	Release 1	Page 3.7.5–3
3.7.5.5 – .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.5–3
3.7.5.6 – 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP–2,	Release 4	Page 3.7.5–3
3.7.5.7 – 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,	Release 1	Page 3.7.5–3
3.7.5.8 – 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,	Release 1	Page 3.7.5–3
3.7.5.9 – 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP–2	Release 4	Page 3.7.5–3
, 3.7.5.10 – 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ	Release 1	Page 3.7.5–3
, 3.7.5.11 – 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC	Release 1	Page 3.7.5–4
3.7.5.12 – 32K BY 9 CACHE SRAM IN 44 SCC	Release 2	Page 3.7.5–4
3.7.5.13 – 128K BY 8 SRAM IN TSOP1	Release 2	Page 3.7.5–4
3.7.5.14 – 128K BY 8 & 9 SSRAM IN SOJ	Release 2	Page 3.7.5–4
3.7.5.15 – 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP	Release 2	Page 3.7.5–4
3.7.5.16 – 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO–N	Release 3	Page 3.7.5–4
3.7.5.17 – 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP AND SOJ	Release 3	Page 3.7.5–4
3.7.5.18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA	Release 5	Page 3.7.5–4
3.7.5.19 – 128K TO 2M BY 8/9 SSRAM IN BGA	Release 5	Page 3.7.5–4
3.7.5.20 – 32K BY 8 SRAM IN TSOP1	Release 7	Page 3.7.5–4
FIGURE 3.7.5–1, 64 BY 9 SRAM IN SCC	Release 1	Page 3.7.5–5
FIGURE 3.7.5–2, 1K & 2K BY 8 TTL SRAM IN DIP	Release 1	Page 3.7.5–6
FIGURE 3.7.5–3, 2K & 4K BY 8 TTL SRAM IN RCC	Release 1	Page 3.7.5–7

Release 7

XILINX EXHIBIT 1010
Page 45

Section	Release #	Page #
FIGURE 3.7.5–4, 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ	Release 1	Page 3.7.5–8
FIGURE 3.7.5–5, 0.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.5–9
FIGURE 3.7.5–6, 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ	Release 4	Page 3.7.5–10
FIGURE 3.7.5–7, 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5–11
FIGURE 3.7.5–8, 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5–12
FIGURE 3.7.5–9, 32K TO 2M BY 8 AND 9 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.5–13
FIGURE 3.7.5–10, 32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.5–14
FIGURE 3.7.5–11, 2K TO 32K BY 9 DPSRAM FAMILY IN SCC	Release 1	Page 3.7.5–15
FIGURE 3.7.5–12, 32K BY 9 TTL CACHE SRAM IN SCC	Release 2	Page 3.7.5–16
FIGURE 3.7.5–13, 128K BY 8 TTL SRAM IN TSOP1	Release 2	Page 3.7.5–17
FIGURE 3.7.5–14, 128K BY 8 & 9 TTL SSRAM IN SOJ	Release 2	Page 3.7.5–18
FIGURE 3.7.5–15A, 1K AND 2K BY 9 DPSRAM IN DIP	Release 2	Page 3.7.5–19
FIGURE 3.7.5–15B, 1K AND 2K BY 9 DPSRAM TRUTH TABLE	Release 2	Page 3.7.5–20
FIGURE 3.7.5–16, 128K TO 512K BY 8 SRAM IN CDSO–N	Release 3	Page 3.7.5–21
FIGURE 3.7.5–17, 128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.5–22
FIGURE 3.7.5–18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA	Release 5	Page 3.7.5–23
FIGURE 3.7.5–19 – 128K TO 2M BY 8/9 SSRAM BGA IN BGA	Release 5	Page 3.7.5–24
FIGURE 3.7.5–20 – 128K TO 2M BY 8/9 SSRAM BGA BOUNDRY SCAN ORDER	Release 5	Page 3.7.5–25
FIGURE 3.7.5–21, 32K BY 8 SRAM IN TSOP2	Release 7	Page 3.7.5–26
3.7.6 Byte Wide ECL SRAM	**Release 1**	**Page 3.7.6–1**
3.7.6.1 – 32K and 128K BY 8 ECL SSRAM IN SOJ, SSOP, AND FP	Release 2	Page 3.7.6–1
FIGURE 3.7.6–1, 32K AND 256K BY 9 ECL SSRAM IN SOJ, SOP, AND FP	Release 2	Page 3.7.6–3
3.7.7 Word Wide TTL SRAM	**Release 1**	**Page 3.7.7–1**
3.7.7.1 – 4K TO 64K BY 16 TTL SRAM IN DIP	Release 1	Page 3.7.7–3
3.7.7.2 – 4K TO 256K BY 16 TTL SRAM IN SCC	Release 1	Page 3.7.7–3
3.7.7.3 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP	Release 1	Page 3.7.7–3
3.7.7.4 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC	Release 1	Page 3.7.7–3
3.7.7.5 – 16K AND 64K BY 18 SRAM IN SCC	Release 1	Page 3.7.7–3
3.7.7.6 – 64K BY 16 & 18 SRAM IN 44 SOJ	Release 3	Page 3.7.7–3
3.7.7.7 – 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES	Release 4	Page 3.7.7–3
3.7.7.8 – 64K TO 256K BY 18 SRAM & SSRAM IN TQFP	Release 5	Page 3.7.7–4
3.7.7–9 – 64K TO 1M BY 16/18 BURST SRAM IN BGA	Release 5	Page 3.7.7–4
3.7.7–10 – 64K TO 1M BY 16/18 SSRAM IN BGA	Release 5	Page 3.7.7–4
3.7.7–11 – 64K TO 256K BY 16/18 BURST SRAM IN QFP/TQFP	Release 6	Page 3.7.7–4
3.7.7–12 – 256K AND 1M BY 16/18 SRAM IN TSOP2	Release 6	Page 3.7.7–4
FIGURE 3.7.7–1, 4K TO 64K BY 16 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.7–5
FIGURE 3.7.7–2, 4K TO 256K BY 16 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.7–6
FIGURE 3.7.7–3, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN DIP	Release 1	Page 3.7.7–7
FIGURE 3.7.7–4, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN RCC	Release 1	Page 3.7.7–8
FIGURE 3.7.7–5, 16K AND 64K BY 18 SRAM IN SCC	Release 1	Page 3.7.7–9
FIGURE 3.7.7–6, 64K BY 16 & 18 SRAM IN SOJ	Release 3	Page 3.7.7–10
FIGURE 3.7.7–7 A, 32K & 64K BY 16 & 18 SRAM AND SSRAM WITH LOGIC FEATURES IN SCC	Release 4	Page 3.7.7–11
FIGURE 3.7.7–7 B, WRITE CLOCK TIMING FOR SSRAM WITH BURST MODE	Release 4	Page 3.7.7–12
FIGURE 3.7.7–8, 64K TO 256K BY 18 SRAM AND SSRAM IN TQFP	Release 5	Page 3.7.7–13
FIGURE 3.7.7–9 – 64K TO 1M BY 16/18 BURST SRAM BGA PADOUT	Release 5	Page 3.7.7–14
FIGURE 3.7.7–10 – 64K TO 1M BY 16/18 SSRAM BGA PADOUT	Release 5	Page 3.7.7–15
FIGURE 3.7.7–11 – 64K TO 1M BY 16/18 SSRAM BGA BOUNDRY SCAN ORDER	Release 5c7	Page 3.7.7–16

Release 7

XILINX EXHIBIT 1010
Page 46

Section	Release #	Page #
FIGURE 3.7.7–12 – 64K TO 256K BY 16/18 BURST SRAM IN TQFP	Release 6	Page 3.7.7–17
FIGURE 3.7.7–10 – 256K AND 1M BY 16/18 SRAM IN TSOP2	Release 6	Page 3.7.7–18
3.7.8 Double Word Wide SRAM	**Release 5**	**Page 3.7.8–1**
3.7.8.1 – 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP	Release 6	Page 3.7.8–3
3.7.8.2 – 32K TO 128K BY 36 SRAM & SSRAM IN TQFP	Release 5	Page 3.7.8–3
3.7.8.3 – 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT	Release 5	Page 3.7.8–3
3.7.8.4 – 32K TO 512K BY 32/36 SSRAM BGA PADOUT	Release 5	Page 3.7.8–3
3.7.8.5 – 16K TO 64K BY 64 & 72 SSRAM IN QFP	Release 7	Page 3.7.8–3
FIGURE 3.7.8–1, 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP	Release 6	Page 3.7.8–5
FIGURE 3.7.8–2, 32K TO 128K BY 36 SRAM AND SSRAM IN TQFP	Release 5	Page 3.7.8–6
FIGURE 3.7.7–3 – 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT	Release 5	Page 3.7.8–7
FIGURE 3.7.7–4 – 32K TO 512K BY 32/36 SSRAM BGA PADOUT	Release 5	Page 3.7.8–8
FIGURE 3.7.7–5 – 32K TO 512K BY 32/36 SSRAM BGA BOUNDRY SCAN ORDER	Release 5	Page 3.7.8–9
FIGURE 3.7.8–6, 16K TO 64K BY 64 & 72 BURST SSRAM IN TQFP	Release 7	Page 3.7.8–10
3.8 Pseudostatic Random Access Memory (PSRAM)	**Release 1**	**Page 3.8–1**
3.8.1 PSRAM, Byte Wide	**Release 1**	**Page 3.8–3**
3.8.1.1 – 2K TO 8K BY 8 PSRAM FAMILY IN DIP	Release 1	Page 3.8–3
3.8.1.2 – 2K TO 16K BY 8 PSRAM FAMILY IN RCC	Release 1	Page 3.8–3
3.8.1.3 – 32K TO 512K BY 8 PSRAM FAMILY IN SOJ	Release 1	Page 3.8–3
3.8.2 PSRAM, Word Wide	**Release 1**	**Page 3.8–3**
3.8.2.1 – 4K TO 32K BY 16 PSRAM IN DIP	Release 1	Page 3.8–3
3.8.2.2 – 4K TO 256K BY 16 PSRAM IN SCC	Release 1	Page 3.8–3
FIGURE 3.8–1, 2K TO 8K BY 8 PSRAM FAMILY IN DIP	Release 1	Page 3.8–4
FIGURE 3.8–2, 2K TO 16K BY 8 PSRAM FAMILY IN RCC	Release 1	Page 3.8–5
FIGURE 3.8–3, 32K TO 512K BY 8 PSRAM FAMILY IN SOJ	Release 1	Page 3.8–6
FIGURE 3.8–4, 4K TO 32K BY 16 PSRAM FAMILY IN DIP	Release 1	Page 3.8–7
FIGURE 3.8–5, 4K TO 256K BY 16 PSRAM FAMILY IN SCC	Release 1	Page 3.8–8
3.9 Dynamic Random Access Memory (DRAM)	**Release 1**	**Page 3.9–1**
3.9.1 Bit Wide DRAM	**Release 1**	**Page 3.9.1–1**
3.9.1.1 – 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES	Release 1	Page 3.9.1–3
3.9.1.2 – 16K TO 256K BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1–3
3.9.1.3 – 16K TO 256K BY 1 DRAM IN RCC	Release 1	Page 3.9.1–3
3.9.1.4 – 64K & 256K BY 1 DRAM IN ZIP	Release 1	Page 3.9.1–3
3.9.1.5 – 1M AND 4M BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1–3
3.9.1.6 – 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2	Release 4	Page 3.9.1–3
3.9.1.7 – 1M TO 16M BY 1 DRAM FAMILY IN ZIP	Release 4	Page 3.9.1–3
3.9.1.8 – 1M TO 16M BY 1 NON–MUX DRAM FAMILY IN SOJ	Release 1	Page 3.9.1–3
, 3.9.1.9 – 1M BY 1 DRAM IN TSOP1	Release 1	Page 3.9.1–4
3.9.1.10 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ	Release 1	Page 3.9.1–4
3.9.1.11 – 64M BY 1 DRAM IN SOJ OR TSOP2	Release 5	Page 3.9.1–4
3.9.1.12 – 2 X 16M BY 1 DRAM IN TSOP2	Release 4	Page 3.9.1–4
FIGURE 3.9.1–1, 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES 16K TO 256K BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1–5
FIGURE 3.9.1–2, 16K TO 256K BY 1 DRAM IN RCC	Release 1	Page 3.9.1–6
FIGURE 3.9.1–3, 64K & 256K BY 1 DRAM IN ZIP	Release 1	Page 3.9.1–7
FIGURE 3.9.1–4, 1M TO 64M BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1–8
FIGURE 3.9.1–5, 1M TO 16M BY 1 DRAM FAMILY IN SOJ and TSOP–2	Release 4	Page 3.9.1–9
FIGURE 3.9.1–6, 1M TO 16M BY 1 DRAM FAMILY IN ZIP	Release 4	Page 3.9.1–10
FIGURE 3.9.1–7, 1M TO 16M BY 1 NON–MUX DRAM FAMILY IN SOJ	Release 2	Page 3.9.1–11
FIGURE 3.9.1–8, 1M BY 1 DRAM IN TSOP1	Release 2	Page 3.9.1–12

Release 7

XILINX EXHIBIT 1010
Page 47

Section	Release #	Page #
FIGURE 3.9.1–9, 16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.1–13
FIGURE 3.9.1–10, 64M BY 1 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.1–14
FIGURE 3.9.1–11, 2 X 16M BY 1 DRAM IN TSOP2	Release 4	Page 3.9.1–15
FIGURE 3.9.1–12, 64M BY 1 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.1–16
3.9.2 Nibble Wide DRAM	**Release 1**	**Page 3.9.2–1**
3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP	Release 1	Page 3.9.2–3
3.9.2.2 – 16K BY 4 DRAM IN DIP	Release 1	Page 3.9.2–3
3.9.2.3 – 64K BY 4 DRAM IN RCC	Release 1	Page 3.9.2–3
3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP	Release 2	Page 3.9.2–3
3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2	Release 4	Page 3.9.2–3
3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP	Release 2	Page 3.9.2–3
3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2	Release 3	Page 3.9.2–3
3.9.2.8 – 256K BY 4 DRAM IN TSOP1	Release 2	Page 3.9.2–3
3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.2–4
3.9.2.10 – 256K TO 4M BY 4 NON–MUX DRAM FAMILY IN SOJ	Release 2	Page 3.9.2–4
3.9.2.11 – 4M BY 4 DRAM WITH 1 CE AND 4 CE IN TSOP2	Release 2	Page 3.9.2–4
3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.2–4
3.9.2.13 – 1M, 2M, 4M BY 2 DRAM IN SOJ & TSOP2	Release 3r7	Page 3.9.2–4
3.9.2.14 – 16M BY 4 DRAM WITH 4 $\overline{CAS}$ IN SOJ & TSOP2	Release 6	Page 3.9.2–4
3.9.2.13 – 64M BY 4 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.2–4
FIGURE 3.9.2–1, 16K & 64K BY 4 DRAM IN DIP	Release 1	Page 3.9.2–5
FIGURE 3.9.2–2, 16K & 64K BY 4 DRAM IN RCC	Release 1	Page 3.9.2–6
FIGURE 3.9.2–3, 256K & 1M BY 4 DRAM FAMILY IN DIP	Release 1	Page 3.9.2–7
FIGURE 3.9.2–4, 256K TO 4M BY 4 DRAM IN SOJ AND TSOP–2	Release 4	Page 3.9.2–8
FIGURE 3.9.2–5, 64K TO 4M BY 4 DRAM IN ZIP	Release 1	Page 3.9.2–9
FIGURE 3.9.2–6, 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2	Release 6	Page 3.9.2–10
FIGURE 3.9.2–7, 256K BY 4 DRAM IN TSOP1	Release 2	Page 3.9.2–11
FIGURE 3.9.2–8, 4M BY 4/16M BY 1 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.2–12
FIGURE 3.9.2–9, 256K TO 4M BY 4 NON–MUX DRAM IN SOJ	Release 2	Page 3.9.2–13
FIGURE 3.9.2–10, 4M BY 4 DRAM WITH 4 CE IN SOJ AND TSOP2	Release 6	Page 3.9.2–14
FIGURE 3.9.2–11, 16M BY 4 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.2–15
FIGURE 3.9.2–12, 1M, 2M, 4M BY 2 DRAM WITH 2 CE IN SOJ AND TSOP2	Release 4r7	Page 3.9.2–16
FIGURE 3.9.2–13, 16M BY 4 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.2–17
FIGURE 3.9.2–14, 16M BY 4 DRAM WITH 4 $\overline{CAS}$ IN SOJ & TSOP2	Release 6r7	Page 3.9.2–18
FIGURE 3.9.2–15, 64M BY 4 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.2–19
3.9.3 Byte Wide DRAM	**Release 1**	**Page 3.9.3–1**
3.9.3.1 – 32K BY 8 DRAM IN DIP	Release 1	Page 3.9.3–3
3.9.3.2 – 32K BY 8 DRAM IN RCC	Release 1	Page 3.9.3–3
3.9.3.3 – 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP	Release 2	Page 3.9.3–3
3.9.3.4 – 512K BY 8 & BY 9 NON–MUX DRAM IN SOJ	Release 2	Page 3.9.3–3
3.9.3.5 – 2M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3–3
3.9.3.6 – 8M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3–3
3.9.3.7 – 32M BY 8 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.3–3
FIGURE 3.9.3–1, 32K BY 8 DRAM IN DIP	Release 1	Page 3.9.3–5
FIGURE 3.9.3–2, 32K BY 8 DRAM IN RCC	Release 1	Page 3.9.3–6
FIGURE 3.9.3–3, 512K BY 8 & 9 DRAM IN SOJ	Release 2	Page 3.9.3–7
FIGURE 3.9.3–4, 512K BY 8 & 9 DRAM IN ZIP	Release 2	Page 3.9.3–8
FIGURE 3.9.3–5, 512K BY 8 & 9 NON–MUX DRAM IN SOJ	Release 2	Page 3.9.3–9
FIGURE 3.9.3–6, 2M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3–10
FIGURE 3.9.3–7, 8M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.3–11
FIGURE 3.9.3–8, 8M BY 8 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.3–12

Section	Release #	Page #
FIGURE 3.9.3–9, 32M BY 8 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.3–13
3.9.4 Word Wide DRAM	**Release 1**	**Page 3.9.4–1**
3.9.4.1 – 64K BY 16 DRAM WITH 2 W IN SOJ & TSOP2	Release 1	Page 3.9.4–3
3.9.4.2 – 256K & 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ & TSOP2	Release 5	Page 3.9.4–3
3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ	Release 4	Page 3.9.4–3
3.9.4.4 – 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP2	Release 6r7	Page 3.9.4–3
3.9.4.5 – 128K AND 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, AND ZIP	Release 6	Page 3.9.4–3
3.9.4.6 – 16M BY 16 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4–4
3.9.4.7 – 128K ANS 256K BY 32 DRAM WITH 4 $\overline{CAS}$ IN TSOP2	Release 6	Page 3.9.4–4
3.9.4.8 – 512K AND 2M BY 32 & 36 DRAM WITH 4 $\overline{CAS}$ IN TSOP2	Release 6	Page 3.9.4–4
3.9.4.9 – 8M BY 32 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4–4
3.9.4.10 – 2M BY 32 DRAM IN TSOP2	Release 7	Page 3.9.4–4
FIGURE 3.9.4–1, 64K BY 16 DRAM IN SOJ	Release 1	Page 3.9.4–5
FIGURE 3.9.4–2, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN SOJ	Release 2	Page 3.9.4–6
FIGURE 3.9.4–3, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN TSOP2	Release 4	Page 3.9.4–7
FIGURE 3.9.4–4, 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ	Release 5	Page 3.9.4–8
FIGURE 3.9.4–5, 1M BY 16 & 18 DRAM WITH 2 CE IN TSOP2	Release 5	Page 3.9.4–9
FIGURE 3.9.4–6, 64K BY 16 DRAM WITH 2 W IN TSOP–2	Release 3	Page 3.9.4–10
FIGURE 3.9.4–7A, 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ	Release 4	Page 3.9.4–11
FIGURE 3.9.4–7B, 256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE	Release 4	Page 3.9.4–12
FIGURE 3.9.4–8, 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP–2	Release 6r7	Page 3.9.4–13
FIGURE 3.9.4–9, 128K AND 256K BY 16 BURST DRAM IN SOJ	Release 6	Page 3.9.4–14
FIGURE 3.9.4–10, 128K AND 256K BY 16 BURST DRAM IN TSOP2	Release 6	Page 3.9.4–15
FIGURE 3.9.4–11, 128K AND 256K BY 16 BURST DRAM IN ZIP	Release 6	Page 3.9.4–16
FIGURE 3.9.4–12, 16M BY 16 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4–17
FIGURE 3.9.4–13, 128K AND 256K BY 32 DRAM WITH 4 $\overline{CAS}$ IN SSOP	Release 6	Page 3.9.4–18
FIGURE 3.9.4–14, 512K AND 2M BY 32 & 36 DRAM IN SOJ AND TSOP2	Release 6	Page 3.9.4–19
FIGURE 3.9.4–15, 8M BY 32 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4–20
FIGURE 3.9.4–16, 2M BY 32 DRAM IN TSOP2	Release 7	Page 3.9.4–21
3.9.5 DRAM Optional Features	**Release 1**	**Page 3.9.5–1**
3.9.5.1 – OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM	Release 1	Page 3.9.5–3
3.9.5.2 – 1M DRAM BUILT IN TEST FUNCTION	Release 1	Page 3.9.5–3
3.9.5.3 – ON–CHIP REFRESH CONTROL FOR X8 DRAM	Release 1	Page 3.9.5–3
3.9.5.4 – G BEFORE E REFRESH	Release 1	Page 3.9.5–3
3.9.5.5 – DRAM SPECIAL TEST AND OPERATIONAL MODES	Release 1	Page 3.9.5–3
3.9.5.6 – NON–MULTIPLEXED DRAM OPERATION	Release 1	Page 3.9.5–3
3.9.5.7 – DRAM EXTENDED DATA OUT DEFINITION	Release 6	Page 3.9.5–3
3.9.5.8 – 256m DRAM TEST MODE DATA AND ADDRESS COMPRESSION	Release 7	Page 3.9.5–3
3.9.5.9 – PIPELINED NIBBLE MODE DEFINITION	Release 7	Page 3.9.5–3
FIGURE 3.9.5–1A, DRAM ON CHIP REFRESH TIMING	Release 1	Page 3.9.5–5
FIGURE 3.9.5–1B, DRAM SELF REFRESH MODE TIMING	Release 4	Page 3.9.5–5
FIGURE 3.9.5–2, DRAM BIT WRITE TIMING	Release 1	Page 3.9.5–6
DRAM SPECIAL TEST AND OPERATIONAL MODES	Release 4	Page 3.9.5–7
OPTIONAL DRAM OPERATIONAL MODES AND CYCLES	Release 3	Page 3.9.5–11
NON–ADDRESS MULTIPLEXED DRAM OPERATIONAL REQUIREMENTS	Release 3	Page 3.9.5–13
DRAM EXTENDED DATA OUT DEFINITION	Release 6	Page 3.9.5–14
256M DRAM ADDRESS AND DATA COMPRESSION DEFINITION	Release 7	Page 3.9.5–15
PIPELINED NIBBLE MODE DEFINITION	Release 7	Page 3.9.5–16
3.10 Multiport Dynamic RAM (MPDRAM)	**Release 1**	**Page 3.10–1**

Release 7

XILINX EXHIBIT 1010
Page 49

Section	Release #	Page #
3.10.1 Nibble Wide MPDRAM	**Release 1**	**Page 3.10.1–1**
3.10.1.1 – 64K BY 4 MPDRAM IN DIP, SOJ, & ZIP	Release 1	Page 3.10.1–1
3.10.1.2 – 256K BY 4 MPDRAM IN DIP, SOJ, TSOP2, & ZIP	Release 3	Page 3.10.1–1
3.10.1.3 – 256K BY 4 TPDRAM IN SOJ	Release 2	Page 3.10.1–1
FIGURE 3.10.1–1, 64K BY 4 MPDRAM IN DIP & SOJ	Release 1	Page 3.10.1–2
FIGURE 3.10.1–2, 64K BY 4 MPDRAM IN ZIP	Release 1	Page 3.10.1–3
FIGURE 3.10.1–3, 256K BY 4 MPDRAM IN DIP, SOJ, & TSOP2	Release 3	Page 3.10.1–4
FIGURE 3.10.1–4, 256K BY 4 MPDRAM IN ZIP	Release 1	Page 3.10.1–5
FIGURE 3.10.1–5, 256K BY 4 TPDRAM IN SOJ	Release 2	Page 3.10.1–6
3.10.2 Byte Wide MPDRAM	**Release 1**	**Page 3.10.2–1**
3.10.2.1 – 128K AND 256K BY 8 MPDRAM IN DIP, SOJ, & TSOP2	Release 3	Page 3.10.2–1
FIGURE 3.10.2–1, 128K AND 256K BY 8 MPDRAM IN DIP & SOJ	Release 2	Page 3.10.2–2
FIGURE 3.10.2–2, 128K BY 8 MPDRAM IN TSOP2	Release 3	Page 3.10.2–3
3.10.3 Word Wide MPDRAM	**Release 1**	**Page 3.10.3–1**
3.10.3.1 – 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS	Release 2	Page 3.10.3–1
3.10.3.2 – 128K & 256K BY 16 MPDRAM IN TSOP–2 WITH MULTIPLE CLOCKS	Release 5	Page 3.10.3–1
3.10.3.3 – 256K BY 16 SGRAM IN TSOP2	Release 6	Page 3.10.3–1
3.10.3.4 – 256K BY 32 SGRAM IN QFP/TQFP	Release 6	Page 3.10.3–1
3.10.3.5 – 256K BY 32 GRAM IN TSOP–2	Release 6	Page 3.10.3–1
3.10.3.6 – 256K BY 32 SMPDRAM IN TSOP–2	Release 6	Page 3.10.3–2
3.10.3.7 – 256K BY 32 SMPDRAM IN TSOP–2	Release 7	Page 3.10.3–2
FIGURE 3.10.3–1, 128K & 256K BY 16 MPDRAM IN SOG with 2 W & 2 CE	Release 3	Page 3.10.3–3
FIGURE 3.10.3–2, 128K & 256K BY 16 MPDRAM IN TSOP–2 with 2 W & 2 CE	Release 5	Page 3.10.3–4
FIGURE 3.10.3–3, 256K BY 16 SGRAM IN TSOP–2	Release 6	Page 3.10.3–5
FIGURE 3.10.3–4, 256K BY 32 SGRAM IN QFP/TQFP	Release 6c7	Page 3.10.3–6
FIGURE 3.10.3–5, 256K BY 32 SGRAM IN TSOP–2	Release 6	Page 3.10.3–7
FIGURE 3.10.3–6, 256K BY 32 SYNCH. MPDRAM IN QFP/TQFP	Release 6	Page 3.10.3–8
FIGURE 3.10.3–7, 256K BY 32 SYNCH. MPDRAM IN QFP/TQFP	Release 7	Page 3.10.3–9
3.10.4 MPDRAM Optional Features	**Release 1**	**Page 3.10.4–1**
3.10.4.1 – 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4–3
3.10.4.2 – 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4–3
3.10.4.3 – MPDRAM BIT WRITE OPTIONAL FEATURE	Release 1	Page 3.10.4–3
3.10.4.4 – 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4–3
3.10.4.5 – 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4–3
3.10.4.6 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4–3
3.10.4.7 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4–3
3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM	Release 3	Page 3.10.4–3
3.10.4.9 – PIPELINED FAST PAGE MODE FOR MPDRAM	Release 2	Page 3.10.4–4
3.10.4.10 – EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM	Release 2	Page 3.10.4–4
3.10.4.11 – SAM LENGTH DEFINITION FOR 2/4M MPDRAM	Release 5	Page 3.10.4–4
3.10.4.12 – SYNCH GRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4–4
3.10.4.13 – SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4–4
3.10.4.14 – SYNCH. GRAM OPERATIONAL FUNCTION TRUTH TABLES	Release 6	Page 3.10.4–4
3.10.4.15 – 8Mb MPDRAM FEATURE SET FUNCTION TABLE	Release 7	Page 3.10.4–4
3.10.4.16 – EXTENDED FUNCTIONSFOR SGRAM & MPDRAM	Release 6r7	Page 3.10.4–4
TABLE 3.10.4–1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4–5
TABLE 3.10.4–2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4–6
FIGURE 3.10.4–1, BIT WRITE TIMING	Release 1	Page 3.10.4–7

Section	Release #	Page #
TABLE 3.10.4–3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4–8
FIGURE 3.10.4–2, SPLIT REGISTER WITH PROGRAMMABLE STOPS	Release 2	Page 3.10.4–9
FIGURE 3.10.4–3A, PIPELINED FAST PAGE MODE	Release 2	Page 3.10.4–10
FIGURE 3.10.4–3B, PIPELINED FAST PAGE MODE	Release 2	Page 3.10.4–11
FIGURE 3.10.4–4, MPDRAM EXTENDED DATA OUT FAST PAGE MODE	Release 4	Page 3.10.4–12
FIGURE 3.10.4–5A & 5B, SAM LENGTH DEFINITION FOR 4M MPDRAM	Release 5	Page 3.10.4–13, 14
FIGURE 3.10.4–6, SYNCH GRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4–15
FIGURE 3.10.4–7, SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4–16
TABLE 3.10.4–4 A,B, & C , SGRAM FUNCTION TRUTH TABLE	Release 6r7	Page 3.10.4–17⇒19
TABLE 3.10.4–5, 8Mb BURST MPDRAM FUNCTION TABLE	Release 7	Page 3.10.4–20
EXTENDED FUNCTIONS FOR SGRAM & MPDRAM	Release 7	Page 3.10.4–21
3.11 Synchronous Dynamic Random Access Memory (SDRAM)	**Release 4**	**Page 3.11–1**
3.11.1 Bit Wide SDRAM	**Release 4**	**Page 3.11.1–1**
FIGURE 3.11.1–1,	Release 4	Page 3.11.1–5
3.11.2 Nibble Wide SDRAM	**Release 4**	**Page 3.11.2–1**
3.11.2.1 – 4M BY 4 SDRAM IN TSOP2	Release 6r7	Page 3.11.2–1
3.11.2.2 – 16M BY 4 SDRAM IN TSOP2	Release 6	Page 3.11.2–1
3.11.2.3 – 64M BY 4 SDRAM IN TSOP2 PIN ROTATION	Release 7	Page 3.11.2–1
FIGURE 3.11.2–1, 4M X 4 SDRAM IN TSOP2	Release 6r7	Page 3.11.2–3
FIGURE 3.11.2–2, 16M X 4 SDRAM IN TSOP2	Release 6	Page 3.11.2–4
FIGURE 3.11.2–3, 64M X 4 SDRAM IN TSOP2 PIN ROTATION	Release 7	Page 3.11.2–5
3.11.3 BYTE WIDE SDRAM	**Release 4**	**Page 3.11.3–1**
3.11.3.1 – 2M BY 8 or 9 SDRAM IN TSOP2	Release 6r7	Page 3.11.3–1
3.11.3.2 – 8M BY 8 SDRAM IN TSOP2	Release 6	Page 3.11.3–1
FIGURE 3.11.3–1, 2M BY 8 OR 9 SDRAM IN TSOP2	Release 6r7	Page 3.11.3–3
FIGURE 3.11.3–2, 8M BY 8 SDRAM IN TSOP2	Release 6	Page 3.11.3–4
FIGURE 3.11.3–3, 32M BY 8 SDRAM IN TSOP2 PIN ROTATION	Release 7	Page 3.11.3–5
3.11.4 WORD WIDE SDRAM	**Release 5**	**Page 3.11.4–1**
3.11.4.1 – 256K BY 16 AND 1M BY 16/18 SDRAM IN TSOP–2	Release 6r7	Page 3.11.4–1
3.11.4.2 – 2M & 4M BY 16 SDRAM IN TSOP–2	Release 6r7	Page 3.11.4–1
3.11.4.3 – 16M BY 16 SDRAM IN TSOP–2 PIN ROTATION	Release 6	Page 3.11.4–1
3.11.4.4 – 256K BY 32 SDRAM IN QFP/TQFP	Release 6	Page 3.11.4–1
3.11.4.5 – 2M BY 32 SDRAM IN TSOP–2	Release 6	Page 3.11.4–1
3.11.4.6 – 8M BY 32 SDRAM IN TSOP–2 PIN ROTATION	Release 6	Page 3.11.4–1
3.11.4.7 – 2M BY 32 & 36 SDRAM IN TSOP–2	Release 7	Page 3.11.4–2
FIGURE 3.11.4–1, 256 BY 16 AND 1M BY 16/18 SDRAM IN TSOP–2	Release 6r7	Page 3.11.4–3
FIGURE 3.11.4–2, 4M BY 16 SDRAM IN TSOP–2	Release 6r7	Page 3.11.4–4
FIGURE 3.11.4–3, 16M BY 16 SDRAM IN TSOP–2	Release 6c7	Page 3.11.4–5
FIGURE 3.11.4–4, 256K BY 32 SDRAM IN QFP/TQFP	Release 6r7	Page 3.11.4–6
FIGURE 3.11.4–5, 2M BY 32 SDRAM IN TSOP–2	Release 6r7	Page 3.11.4–7
FIGURE 3.11.4–6, 8M BY 32 SDRAM IN TSOP–2 PIN ROTATION	Release 6c7	Page 3.11.4–8
FIGURE 3.11.4–7, 2M BY 32 & 36 SDRAM IN TSOP–2	Release 7	Page 3.11.4–9
3.11.5 SDRAM Architectural and Operational Features	**Release 4**	**Page 3.11.5–1**
3.11.5.1 – SDRAM FUNCTION TRUTH TABLE	Release 5	Page 3.11.5–3
3.11.5.2 – SDRAM FUNCTION TRUTH TABLE FOR CKE	Release 5	Page 3.11.5–3
3.11.5.3 – SDRAM MODE REGISTER ARCHITECTURE	Release 4	Page 3.11.5–3
3.11.5.4 → 3.11.5.15 — SDRAM OPERATIONAL CYCLES AND MODES	Release 4	Page 3.11.5–3
3.11.5.4 – POWER ON SEQUENCE (RECOMMENDED)	Release 4	Page 3.11.5–3
3.11.5.5 – AUTO PRECHARGE	Release 6	Page 3.11.5–3
3.11.5.6 – PRECHARGE ALL BANKS	Release 6	Page 3.11.5–3

Release 7

Section	Release #	Page #
3.11.5.7 – MODE REGISTER WRITE TIMING	Release 4	Page 3.11.5–3
3.11.5.8 – AUTO REFRESH	Release 4	Page 3.11.5–3
3.11.5.9 – WRITE LATENCY	Release 4c7	Page 3.11.5–3
3.11.5.10 – DQM LATENCY FOR READS AND WRITES	Release 4	Page 3.11.5–3
3.11.5.11 – PRECHARGE TIMING FOR READS	Release 4	Page 3.11.5–3
3.11.5.12 – COLUMN ADDRESS TO COLUMN ADDRESS DELAY	Release 4	Page 3.11.5–3
3.11.5.13 – CKE TIMING FOR POWER DOWN	Release 4	Page 3.11.5–3
3.11.5.14 – SELF REFRESH ENTRY AND EXIT	Release 4	Page 3.11.5–3
3.11.5.15 – CKE TIMING FOR CLOCK SUSPEND	Release 4	Page 3.11.5–3
TABLE 3.11.5–1, SDRAM FUNCTION TRUTH TABLE	Release 5	Page 3.11.5–5
TABLE 3.11.5–1, SDRAM FUNCTION TRUTH TABLE (Continued)	Release 5	Page 3.11.5–6
TABLE 3.11.5–2, SDRAM FUNCTION TRUTH TABLE for CKE	Release 5	Page 3.11.5–7
FIGURE 3.11.5–1, SDRAM MODE REGISTER ARCHITECTURE	Release 4	Page 3.11.5–8
3.11.5.4–Power On Sequence (Recommended)	Release 4	Page 3.11.5–9
3.11.5.5–Auto Precharge	Release 4	Page 3.11.5–9
3.11.5.6–Precharge All Banks	Release 4c7	Page 3.11.5–9
3.11.5.7–Mode Register Write Timing	Release 4	Page 3.11.5–10
3.11.5.8–Auto Refresh	Release 4	Page 3.11.5–11
3.11.5.9–Write Latency, (Write Latency = 0)	Release 4	Page 3.11.5–12
3.11.5.10–DQM Latency for Reads and Writes, (DQM Write Latency = 0)	Release 4	Page 3.11.5–13
3.11.5.11–Precharge Timing for Reads	Release 4	Page 3.11.5–14
3.11.5.12–Column Address to Column Address Delay	Release 4	Page 3.11.5–15
3.11.5.13–CKE Timing for Power Down	Release 4	Page 3.11.5–16
3.11.5.14–Self–Refresh Entry and Exit	Release 4	Page 3.11.5–17
3.11.5.15–CKE Timing for Clock Suspend	Release 4	Page 3.11.5–18
4. MULTI–CHIP MEMORY MODULES & CARDS	**Release 7**	**Page 4–1**
4.1. Memory Module Nomenclature and General Features	**Release 7**	**Page 4.1–1**
4.1.1 Memory Module Nomenclature	Release 1–7	Page 4.1–1
4.1.2 Serial Presence Detect General Standard	Release 1–7	Page 4.1–1
4.1.2.1 SPD Appendix A	Release 7	Page 4.1.2.1–1
4.1.2.2 SPD Appendix B	Release 7	Page 4.1.2.2–1
4.1.2.3 SPD Appendix C	Release 7	Page 4.1.2.3–1
4.1.2.4 SPD Appendix D	Release 7	Page 4.1.2.4–1
4.1.2.5 SPD Appendix E	Release 7	Page 4.1.2.5–1
4.1.2.6 SPD Appendix F	Release 7	Page 4.1.2.6–1
4.2. One BYTE Modules	**Release 7**	**Page 4.2–1**
4.2.1 – 22 PIN SIP/SIMM 4 bit DRAM MODULE	Release 1–7	Page 4.2–1
4.2.2 – 24 PIN SIP/SIMM 4 bit DRAM MODULE	Release 1–7	Page 4.2–1
4.2.3 – 30 PIN SIP/SIMM 8 or 9 bit DRAM MODULE	Release 4–7	Page 4.2–1
4.2.4 – 30 PIN SIP/SIMM 1, 2, 4, 5, or 8 bits DRAM MODULE FAMILY	Release 1–7	Page 4.2–1
4.2.5 – 23/25/26/28 PIN ZIP/SIMM 1 or 4 bit DRAM MODULE FAMILY	Release 1–7	Page 4.2–2
4.2.6 – 60 PIN ZIP/SIMM 4 bit SRAM MODULE	Release 1–7	Page 4.2–2
4.2.7 – 70 PIN ZIP/SIMM 9 bit SRAM MODULE	Release 1–7	Page 4.2–2
FIGURE 4.2–1, 22, 24,& 30 PIN DRAM MODULES	Release 4–7	Page 4.2–3
FIGURE 4.2–2, 30 PIN DRAM MODULE FAMILY	Release 1–7	Page 4.2–4
FIGURE 4.2–3, 23/25/26/28 PIN DRAM MODULE FAMILY	Release 1–7	Page 4.2–5
FIGURE 4.2–4, 2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY	Release 1–7	Page 4.2–6
FIGURE 4.2–5, 64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY	Release 1–7	Page 4.2–7

Section	Release #	Page #
4.3. Two BYTE Modules and Cards	Release 7	**Page 4.3–1**
4.3.1 – 76 PIN ZIP/SIMM 9 or 18 bit SRAM MODULE	Release 1–7	Page 4.3–1
4.3.2 – 40 PIN SIP/SIMM 1, 2, 4, 5, 8, 9, 16, or 18 DRAM MOD FAMILY	Release 1–7	Page 4.3–1
4.3.3 – 60 PIN DRAM 16 or 18 bit CARD FAMILY	Release 2–7	Page 4.3–1
4.3.4 – 68 PIN MULTIPLE TECHNOGY MEMORY 16 bit CARD FAMILY	Release 3–7	Page 4.3–1
FIGURE 4.3–1, 2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY	Release 1–7	Page 4.3–3
FIGURE 4.3–2, 40 PIN DRAM MODULE FAMILY	Release 1–7	Page 4.3–4
FIGURE 4.3–3A, 60 PIN DRAM CARD FAMILY PIN CONNECTIONS	Release 2–7	Page 4.3–5
FIGURE 4.3–3B, 60 PIN CARD FAMILY BLOCK DIAGRAMS	Release 2–7	Page 4.3–6
FIGURE 4.3–4A, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY	Release 3–7	Page 4.3–7
FIGURE 4.3–4B, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TRUTH TABLES	Release 3–7	Page 4.3–8
4.4. Four BYTE Modules and Cards	Release 7	**Page 4.4–1**
4.4.1 – 64 & 72 PIN ZIP/SIMM 32 bit SRAM MODULE	Release 6–7	Page 4.4.1–1
FIGURE 4.4.1–1, 16K TO 4M BY 32, 64 & 72 PIN SRAM MODULE FAMILY	Release 6–7	Page 4.4.1–2
4.4.2 – 72 PIN SIMM 32 or 36 bit DRAM MODULE FAMILY	Release 6–7	Page 4.4.2–1
– 72 PIN SIMM 36 or 39 DRAM ECC MODULE FAMILY	Release 6–7	Page 4.4.2–1
FIGURE 4.4.2–2, 256K TO 256M BY 36. 72 PIN DRAM MODULE FAMILY	Release 6–7	Page 4.4.2–3
FIGURE 4.4.2–2 B⇒K, 72 PIN 36 BIT DRAM SIMM BLOCK DIAGRAMS	Release 6–7	Page 4.4.2–4⇒13
FIGURE 4.4.2–3 A, 256K TO 256M BY 32, 36. & 40 BIT 72 PIN DRAM MODULE	Release 6–7	Page 4.4.2–14
FIGURE 4.4.2–3 B⇒C 72 PIN 32, 36, & 40 BIT DRAM SIMM BLOCK DIAGRAMS	Release 6–7	Page 4.4.2–15⇒16
4.4.3 – 88 PIN, 32/36/39 bit DRAM CARD FAMILY	Release 6–7	Page 4.4–1
FIGURE 4.4.3–1 A, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY	Release 6–7	Page 4.4.3–3
FIGURE 4.4.3–1 B, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY CONFIGURATION TABLES	Release 6–7	Page 4.4.3–4
FIGURE 4.4.3–1 C, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6–7	Page 4.4.3–5
FIGURE 4.4.3–1 D, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6–7	Page 4.4.3–6
FIGURE 4.4.3–1 E, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6–7	Page 4.4.3–7
FIGURE 4.4.3–1 F, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6–7	Page 4.4.3–8
– 88 PIN, 40 bit DRAM CARD FAMILY	Release 4–7	Page 4.4.3–1
FIGURE 4.4.3–2 A, 256K TO 128M BY 40 DRAM CARD	Release 4–7	Page 4.4.3–9
FIGURE 4.4.3–2 B, 256K TO 128M BY 40 DRAM CARD PD TRUTH TABLE	Release 4–7	Page 4.4.3–10
FIGURE 4.4.3–2 C, 256K TO 64M BY 40 DRAM CARDUSING BY 4 DEVICES	Release 4–7	Page 4.4.3–11
FIGURE 4.4.3–2 D, 512K TO 128M BY 40 DRAM CARD USING BY 4 DEVICES	Release 4–7	Page 4.4.3–12
FIGURE 4.4.3–2 E, 512K TO 32M BY 40 DRAM CARD USING BY 8 DEVICES	Release 4–7	Page 4.4.3–13
FIGURE 4.4.3–2 F, 1M TO 64M BY 40 DRAM CARD USING BY 8 DEVICES	Release 4–7	Page 4.4.3–14
4.4.4 – 72 PIN 32 or 36 bit DRAM SO–DIMM FAMILY	Release 5–7	Page 4.4.4–1
FIGURE 4.4.4– A 32 & 36 BIT 72 PIN DRAM SO–DIMM PINOUT, PRESENCE DETECT & CONFIGURATION TABLES	Release 6–7	Page 4.4.4–1
FIGURE 4.4.4–B–D 32 & 36 BIT DRAM SO–DIMM BLOCK DIAGRAMS	Release 5–7	Page 4.4.4–2⇒5
4.4.5 – 88 PIN 32 or 36 bit DRAM SO–DIMM FAMILY	Release 5–7	Page 4.4.5–1
FIGURE 4.4.5–A, 88 PIN 32 & 36 BIT DRAM SO–DIMM PINOUT	Release 6–7	Page 4.4.5–2
FIGURE 4.4.5–B, 88 PIN 32 & 36 BIT DRAM SO–DIMM PD TRUTH TABLES	Release 6–7	Page 4.4.5–3
FIGURE 4.4.5–C⇒F, 88 PIN 32 & 36 BIT DRAM SO–DIMM BLOCK DIAGRAMS	Release 6–7	Page 4.4.5–4⇒7
4.4.6 – 112 PIN 32 bits MPDRAM SO–DIMM FAMILY	Release 5–7	Page 4.4.6–1
FIGURE 4.4.6–A, 112 PIN 32 BIT MPDRAM DIMM PINOUT	Release 6–7	Page 4.4.6–2
FIGURE 4.4.6– B, C, 112 PIN 32 BIT MPDRAM DIMM PD TRUTH TABLES AND BLOCK DIAGRAMS	Release 6–7	Page 4.4.6–3, 4
4.4.7 – 80 PIN 32 bit EEPROM SIMM FAMILY	Release 4–7	Page 4.4.7–1
FIGURE 4.4.7–A, 128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES	Release 4–7	Page 4.4.7–3

Release 7

XILINX EXHIBIT 1010
Page 53

Section	Release #	Page #
FIGURE 4.4.7–B, 128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM	Release 4–7	Page 4.4.7–4
4.4.8 – 100 PIN 32, 36, or 40 BIT DRAM, SDRAM, ROM DIMM FAMILY	Release 7	Page 4.4.8–1
FIGURE 4.4.8–B & C, 32, 36, or 40 bit 100 PIN MODULE PINOUT	Release 7	Page 4.4.8–3, 4
FIGURE 4.4.8–D, 32, 36, or 40 bit 100 PIN MODULE PIN COMPARISON	Release 7	Page 4.4.8–5
FIGURE 4.4.8–E, 32, 36, or 40 bit 100 PIN MODULE CLOCK WIRING	Release 7	Page 4.4.8–6
FIGURE 4.4.8–F⇒AE, 32, 36, or 40 bit 100 PIN MODULE BLOCK DIAGRAMS	Release 7	Page 4.4.8–7⇒32
4.5. Eight BYTE Modules and Cards	**Release 7**	**Page 4.5–1**
4.5.1 – 168 PIN Buffered DRAM, 64, 72, or 80 Bit DIMM FAMILY	Release 6–7	Page 4.5.1–1
FIGURE 4.5.1–A–B, 64, 72, or 80 BIT SIMM PINOUT, TOP & BOTTOM HALVES	Release 4–7	Page 4.5.1–2,3
FIGURE 4.5.1–C, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 6–7	Page 4.5.1–4
FIGURE 4.5.1–D, 64, 72, & 80 BIT DRAM SIMM Capacity Table	Release 4–7	Page 4.5.1–5
FIGURE 4.5.1–E–AB, 64, 72, & 80 BIT CONFIGURATION BLOCK DIAGRAMS	Release 4–7	Page 4.5.1–6–29
4.5.2 – 200 PIN SDRAM, 64, 72, or 80 DIMM FAMILY	Release 5–7	Page 4.5.2–1
FIGURE 4.5.2–A, B, 8 –BYTE SDRAM DIMM PINOUT	Release 5–7	Page 4.5.2–3,4
FIGURE 4.5.2– C, 8–BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5–7	Page 4.5.2–5
FIGURE 4.5.2–D, E, 8–BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5–7	Page 4.5.2–6
FIGURE 4.5.2–F–M, 8–BYTE SDRAM DIMM BLOCK DIAGRAMS	Release 5–7	Page 4.5.2–7,14
4.5.3 – 168 PIN Unbuffered DRAM, 64, 72, or 80 DIMM FAMILY with SPD	Release 5–7	Page 4.5.3–1
FIGURE 4.5.3–A, B, 8 –BYTE DRAM DIMM PINOUT	Release 5–7	Page 4.5.3–2,3
FIGURE 4.5.3–D, 8–BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5–7	Page 4.5.3–5
FIGURE 4.5.3– F, 8–BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5–7	Page 4.5.3–7
FIGURE 4.5.2–G–S, 8–BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5–7	Page 4.5.3–8,20
4.5.4 – 168 PIN Unbuffered SDRAM, 64, 72, or 80 DIMM FAMILY with SPD	Release 5–7	Page 4.5.4–1
FIGURE 4.5.4–A, B, 8 –BYTE SDRAM DIMM PINOUT	Release 5–7	Page 4.5.4–2,3
FIGURE 4.5.4– C, 8–BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5–7	Page 4.5.4–4
FIGURE 4.5.4–E, 8–BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5–7	Page 4.5.4–6
FIGURE 4.5.4–I–Y, 8–BYTE SDRAM DIMM BLOCK DIAGRAMS	Release 5–7	Page 4.5.4–10,26
4.5.5 – 144 PIN Unbuffered DRAM, 64, or 72, SO–DIMM FAMILY with SPD	Release 5–7	Page 4.5.5–1
FIGURE 4.5.5–A, B, 8 –BYTE DRAM DIMM PINOUT	Release 5–7	Page 4.5.5–2,3
FIGURE 4.5.5–C, 8–BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5–7	Page 4.5.5–4
FIGURE 4.5.5– E, 8–BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5–7	Page 4.5.5–6
FIGURE 4.5.5–F–O, 8–BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5–7	Page 4.5.5–7,16
4.5.6 – 144 PIN Unbuffered SDRAM, 64, or 72 SO–DIMM FAMILY with SPD	Release 5–7	Page 4.5.6–1
FIGURE 4.5.6–A, B, 8 –BYTE DRAM DIMM PINOUT	Release 5–7	Page 4.5.6–2,3
FIGURE 4.5.6– C, 8–BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5–7	Page 4.5.5–6
FIGURE 4.5.6–D, 8–BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5–7	Page 4.5.6–4
FIGURE 4.5.2–G–P, 8–BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5–7	Page 4.5.6–7,17
4.6. Sixteen BYTE Modules	**Release 7**	**Page 4.6–1**
4.6.1 – 278 PIN Buffered SDRAM, 144 Bit DIMM FAMILY	Release 7	Page 4.6.1–1
FIGURE 4.6.1–A,B,C, 144 BIT SIMM PINOUT, TOP, MIDDLE, & BOTTOM PARTS	Release 7	Page 4.6.1–2,3,4
FIGURE 4.6.1–D, 144 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 7	Page 4.6.1–5
FIGURE 4.6.1–E, F, 144 BIT SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5–7	Page 4.6.1–6
FIGURE 4.6.1–G, H, 144 BIT SDRAM CONFIGURATION BLOCK DIAGRAMS	Release 7	Page 4.6.1–7, 8
5 PROGRAMMABLE LOGIC AND ASIC DEVICES	**Release 1**	**Page 5–1**
5.1 Pin Out Standards	**Release 1**	**Page 5–1**

Release 7

XILINX EXHIBIT 1010
Page 54

Section	Release #	Page #
5.1.1 PIN–OUT STANDARDS FOR PLD DIP TO SCC CONVERSION	Release 4	Page 5–1
5.1.1.1 – 20 PIN DIP to 20 TERMINAL SCC, 0.350" BY 0.350", Fig. 5–1	Release 1	Page 5–1
5.1.1.2 – 24 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5–2	Release 1	Page 5–1
5.1.1.3 – 28 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5–2	Release 1	Page 5–1
5.1.1.4 – 24 PIN FUNCTIONS IN 28 PIN DIP & 28 TERMINAL SCC, Fig. 5–9	Release 1	Page 5–1
5.1.1.5 – 20 PIN FUNCTIONS IN 28 TERMINAL SCC AND 24 PIN DIP FOR HIGH SPEED OPERATION, Fig. 5–11	Release 4	Page 5–1
5.1.2 POWER PIN LOCATIONS FOR PLD and ASIC DEVICES	Release 1	Page 5–1
5.1.2.1 – POWER PIN LOCATIONS FOR ECL PLD IN DIP	Release 1	Page 5–1
5.1.2.2 – POWER PIN LOCATIONS FOR TTL PLD IN DIP and CC	Release 1	Page 5–1
5.1.2.3 – POWER PIN LOCATIONS FOR TTL PROGRAMMABLE ASIC IN DIP and CC	Release 1	Page 5–1
5.1.2.4 – POWER PIN LOCATIONS FOR PLD IN 132 PIN QFP	Release 1	Page 5–1
5.1.3 Nomenclature for FPLD	Release 1	Page 5–1
5.1.4 PLD Data Transfer Format	Release 1	Page 5–1
5.1.5 PLD Standard OUTPUT LOADS	Release 5	Page 5–1
FIGURE 5–1, 20 PIN DIP TO 20 TERMINAL CC PLD CONVERSION	Release 1	Page 5–3
FIGURE 5–2, 24 & 28 PIN DIP TO 27 TERMINAL CC CONVERSION	Release 2	Page 5–4
FIGURE 5–3, POWER PIN PLACEMENT FOR ECL PLD	Release 1	Page 5–5
FIGURE 5–4, 40 PIN DIP PLD POWER PIN PLACEMENT	Release 1	Page 5–6
FIGURE 5–5, 44 TERMINAL CC POWER PIN PLACEMENT	Release 1	Page 5–7
FIGURE 5–6, 48 & 64 PIN DIP ASIC POWER PIN PLACEMENT	Release 1	Page 5–8
FIGURE 5–7, 52, 68, & 84 TERMINAL CC ASIC POWER PIN PLACEMENT	Release 1	Page 5–9
FIGURE 5–8A, PLD STANDARD LOADS, DEFINITIONS	Release5	Page 5–11
FIGURE 5–8B, PLD STANDARD LOAD CIRCUIT	Release 5	Page 5–12
FIGURE 5–8C, PLD OUTPUT LOAD CALCULATIONS	Release 5	Page 5–13
FIGURE 5–8D, PLD AC LOAD LINES	Release 5	Page 5–14
FIGURE 5–9, 24 PIN PLD FUNCTIONS IN 28 PIN DIP AND SCC	Release 3	Page 5–15
FIGURE 5–10, 132 PIN PQFP POWER PIN LOCATIONS	Release 3	Page 5–16
FIGURE 5–11, HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS	Release 4	Page 5–17
6 APPLICABLE OTHER DOCUMENTS	Release 1	Page 6–1
6.1 – Standard Manufacturers Identification Code., JEDEC Publication No. 106A	Release 1	Page 6–1
6.2 – Interface Standard for Low Voltage TTL–Compatible Devices (LVTTL), JEDEC Standard No. 8 and Addendum No. 1	Release 1	Page 6–1
6.3 – Package Outlines, JEDEC Publication 95	Release 1	Page 6–1
6.4 – PLD Data Transfer Format, JEDEC Standard 3–B	Release 1	Page 6–1
6.5 – Nomenclature for FPLD, EIA Standard RS–428	Release 1	Page 6–1

XILINX EXHIBIT 1010
Page 55

2.1.17 – DC, DIAGNOSTIC CLOCK
The input that, on some devices, invokes and controls any built–in diagnostic test features.

2.1.18 – DQ(n)(x), DATA INPUT/OUTPUT
The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state. On a devices having both serial and parallel access ports, these pins provide access to the parallel RAM port data channels. The suffix (n) is a numeric value indicating the number assignment of a particular pin with numbering starting at 0. In some situations the letters U or L are used to indicate that the pins are assigned to the upper or lower byte of a 2 byte data interface. In devices where the standard supports an optional 9th bit that may be used as a parity bit, the suffix P may be used in lieu of a numeric value. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.19 – DQM, INPUT/OUPUT DATA MASK
A control signal used primarily on SDRAMs that acts as as mask for reading and writing functions. In some instances, the DQM term will includes a prefix "U" or "L" indicating upper or lower byte control. In devices where more than two data bit groupings have a data mask applied, a "x" is applied where "x" takes the values of a, b, c, etc.

2.1.20 – E, CHIP ENABLE
The input that, when true, permits active operation including the input and/or output of data, and when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating.

2.1.21 – F, REFRESH
An input that, when true, causes the device to enter a data refresh mode.

2.1.22 – G(n), OE(n), OUTPUT ENABLE
The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.23 – GS, SYNCHRONOUS OUTPUT ENABLE
An output enable input that must be set in by a synchronizing clock signal, K (q.v.).

2.1.24 – $\overline{I}$, INITIALIZE INPUT
A control input that provides a preassigned Manufacturer or User defined code to be set into the data register. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.25 – ID(n), IDENTIFICATION
A group of output terminals, nominally used to convey information about the configuration or other attributes of the device when plugged into a system. The function of these outputs are similar to those of the PD(n) terminals but they often have different electrical interface chatacteristics.

2.1.26 – I/O, INPUT/OUTPUT
A generic term for otherwise undefined signal pins which can have either an input and/or an output function. This term is not used as a specific pin name, only as a generic indicatior of the nature of the function of the pin.

2.1.27 – $\overline{IS}$, INITIALIZE INPUT (SYNCHRONOUS)
A control input that provides a preassigned Manufacturer or User defined code to be presented to the data register for subsequent setting by a clock input. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.28 – K, INPUT CLOCK
The input that, on devices that contain input buffer registers, causes the address on the A(n), the data on the D(n) pins and/or certain control inputs to be set into the register.

2.1.29 – L, LATCH ENABLE or LOWER BYTE
An input that, on devices containing a latch register, causes the data to be latched into the register. When L is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. $\overline{LW}$).

2.1.30 – LB, LOWER BYTE ENABLE
An input, on wordwide devices, that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.

2.1.31 – LW, LOWER BYTE WRITE ENABLE
An input, on wordwide devices, that when true causes the data present on the lower byte input/output, terminals DQ0 through DQ7, to be written into the addressed cells of the device.

2.1.32 – M(n), M, MODE SELECT, MASK
Input signals that when true select an alternative mode of operation for the device. The alternative modes available must be defined in the applicable device standard. When M is used in conjuction with other symbols to create a new pin name, it signifies that the pin function is either MASK or MODE related.

2.1.33 – MA, MATCH
An output signal that when true indicates that there has been a match (logic compare equal) between data stored in the memory and data presented on a set of input pins as defined in the individual device standard.

2.1.34 – MCH, MUST CONNECT HIGH
A pin which must be connected to a voltage that is interpreted as logic high or "true" signal.

XILINX EXHIBIT 1010
Page 57

2.1.35 – MCL, MUST CONNECT LOW
A pin which must be connected to a voltage that is interpreted as logic low or "false" signal.

2.1.36 – NC, NO CONNECTION
A pin to which no internal electrical connection is present or allowed.

2.1.37 – NE, NON–VOLATILE ENABLE
The input, on a NVRAM, that enables the non–volatile functions ST & RC as determined by the states of S,E,G, and W.

2.1.38 – NF, NO FUNCTION
An input that is electrically connected to the device but for which the signal has no function in the device operation.

2.1.39 – NP, NO PIN
A pin position on a package where the pin has been purposely been left blank or removed after assembly. No physical pin is allowed in this position.

2.1.40 – NU, NOT USABLE
A device pin to which there may or may not be an internal connection but to which no external connections are allowed.

2.1.41 – OE,(n), G(n) OUTPUT ENABLE
The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.42 – OP, OPTIONAL
The designation for pins on which the manufacturer has the freedom to supply a specialized function not previously defined in the standard, and still have his part meet the requirements of the standard.

2.1.43 – P, PROGRAM or PROGRAM ENABLE, PARITY
The input on a non–volatile memory device that, when true, causes the data present on the D or DQ pins to be written into the addressed cell(s) of the device. The letter P may also be used as a suffix for data pins where an optional 9th bit, that may be used for parity, is allowed by the standard (e.g. DQP)

2.1.44 – PD(n), PRESENCE DETECT
A group of output pins, normally used on modules or cards, whose state is used to convey information about the capacity, speed, configuration, or other attributes of the device when plugged into a system.

2.1.45 – PR, PAGE RESET
The input on a page select memory that, when true, unconditionally causes the page select address register to be reset to zero and the corresponding page to be selected.

2.1.46 – PS, PAGE SELECT
The input on a page select memory that, when true, causes one of the pages of memory to be selected as identified by the inputs on the DQ pins (as defined in the appropriate function table) and for this page address to be stored in an internal register.

2.1.47 – Q(n)(x), DATA OUTPUT
The outputs whose state represents the data read from the selected cells. When the device is not selected or enabled, the outputs are usually in a floating (Z, high impedance) state. When the numbering of the data outputs is significant for device operation, the data outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.48 – RA, ROW ADDRESS INPUT
In an address multiplexed DRAM, the address field that is captured by the ROW ENABLE signal, RAS\. When the numbering of the row address numbering is significant for device operation, the RA are numbered beginning with 0

2.1.49 – RAS, (RE) ROW ENABLE INPUT
A chip enable signal that, on certain dynamic RAMs, actuates only row address oriented internal circuitry. In modules that have multiple RAS\s, the RAS\s are numbered beginning with 0.

2.1.50 – RC, RECALL
The input on a NVRAM, that transfers the non–volatile data into the RAM array.

2.1.51 – RFU, RESERVED FOR FUTURE USE
A terminal whose function is not currently defined, but which is intended to be defined in some future enhancement of this Standard. This terminal should not be used (either internally or externally) until it has been further defined.

2.1.52 – RSVD, RESERVED
In a family of standards where some devices in the family are subsets of others, terminals that are defined in some devices but not used in others. To allow for upgradeability, the unused terminals are "RESERVED" to prevent their being used. NC has often been used in similar situations.

2.1.53 – RY, READY
The output that, on some devices, signifies that no internal asynchronous operations are still in process, and that the device is available for normal functions. This signal is normally implemented so that multiple devices can be OR–tied. This signal is the inverse of BY (RY=$\overline{BY}$)

2.1.54 – S(n)(x), CHIP SELECT
The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating (Z) for MOS and TTL devices and low (L)

for ECL devices), and the device becomes insensitive to a write command. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.55 – ST, STORE
The input, on a NVRAM, that initiates the non–volatile data storage of the entire RAM array.

2.1.56 – Sxx, SYNCHRONOUS FUNCTION
On a synchronous memory device, any input terms that are synchronous with a clock should start with the letter S. For example: $\overline{SG}$ = Synchronous Output Enable, $\overline{SW}$ = Synchronous Write Enable.

2.1.57 – $\overline{TF}$, TEST FUNCTION
The input, on a MEMORY that, when true, causes built in on–chip test logic to be actuated and for the part to go into its test mode of operation.

2.1.58 – U, UPPER BYTE
When U is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. UW).

2.1.59 – UB, UPPER BYTE ENABLE
An input that, on wordwide devices, when true, enables the upper byte data input/outputs, pins DQ8 through DQ15.

2.1.60 – UW, UPPER BYTE WRITE ENABLE
An input, on wordwide devices, that, when true, causes the data present on the upper byte input/output, terminals DQ8 through DQ15, to be written into the addressed cells of the device.

2.1.61 – WE, W, WRITE ENABLE
The input that, when true, causes the data present on the D or the DQ pin(s) to be written into the address cell(s) of the device. In devices that have a WE per byte, the WEs are designated LWE & UWE for 2 byte devices. In devices that have a WE per byte and more that two bytes, the WE are numbered beginning with 0. In modules that have multiple WEs, the WEs are numbered beginning with 0.

2.2 MULTIPORT DRAM PIN NAMES

The following pin names apply primarily to specialized function pins for MPDRAM. In some situations, the names may also be applicable to other types of memories such as Graphics DRAMs.

2.2.1 – DSF, SPECIAL FUNCTION ENABLE INPUT
The input on a device, that when true, actuates certain special operational functions. In devices and modules that have multiple DSFs, the DSFs are numbered beginning with 0.

2.2.2 – DT/$\overline{OE}$(n), $\overline{TRG}$(n), DATA TRANSFER/OUTPUT ENABLE INPUT
The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

2.2.3 – QSF, QSY, TRANSFER ACKNOWLEDGE OUTPUT
The output on a device having both serial and parallel access ports which signifies that a transfer of data from the parallel to the serial port, in certain special transfer cycles, has been completed. In devices and modules that have multiple QSFs, the QSFs are numbered beginning with 0.

2.2.4 – SC, SERIAL CLOCK
An input, on devices having a serial data access port, that actuates the serial transfer of data, either in or out.

2.2.5 – SDQ(n)(x), SERIAL DATA INPUT/OUTPUT
The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode and as serial data inputs(s) when in the write mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data input/outputs is significant for device operation, the serial data input/outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.2.6 – SE, SERIAL PORT ENABLE
The input that, when true, actuates the device's serial access circuitry.

2.2.7 – SG, SERIAL PORT OUTPUT ENABLE
The input that, when true, actuates the device's serial data output circuitry.

2.2.8 – SQ(n), SERIAL DATA OUTPUT
The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode, When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data outputs is significant for device operation, the serial data outputs are numbered beginning with 0.

2.2.9 – $\overline{TRG}$(n), DT/$\overline{OE}$(n) DATA TRANSFER/OUTPUT ENABLE INPUT
The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

XILINX EXHIBIT 1010
Page 59

2.3 POWER PIN NAMES

The following symbols are used to designate the power pins in a memory device. When only a single pin is provided for a given supply, the pin name is used without suffix. When multiple pins are used, a suffix may be used to designate specific pins. A numeric suffix is used to indicate the preferred order of implementation when optional redundant pins are allowed. An alphabetic suffix is used to indicate pins which have a specific power circuit or loop connection. The use of a common suffix for different supplies indicates that those pins connect to a common power loop.

2.3.1 – VBB, SUBSTRATE POWER VOLTAGE

A bias voltage that maintains the substrate at a potential which is negative with respect to GND or VSS in an NMOS or CMOS part.

2.3.2 – VCC, LOGIC POWER VOLTAGE

The most positive potential of the two logic power supply pins. This is used for the memory device power voltage when the supply voltage is nominally 5 V. VCC is also commonly used to designate the ground reference power supply voltage for ECL interface devices.

2.3.3 – VCCQ, OUTPUT STAGE LOGIC POWER VOLTAGE

See VDDQ for definition. VCCQ is restricted to 5 V applications only

2.3.4 – VDD, DRAIN POWER VOLTAGE

The primary power voltage on MOS devices that require a potential that is different from the normal system logic voltage. This is used interchangeably with VCC on devices that use 5 V.

2.3.5 – VDDQ, OUTPUT STAGE DRAIN POWER VOLTAGE

The power pin that is intended to feed power to the output transistors of the device to supply the potential and energy to drive the load applied to the data output (Q) pins or data input/output (DQ) pins. Other, non–data, output pin transistors may also be designated to be fed by this power pin. VDDQ/VCCQ may be specified to have the same or a different potential from that feeding the primary device power pins (VDD/VCC) but is DC isolated on the chip from these and any other chip power pins.

2.3.6 – VEE, EMITTER POWER VOLTAGE

For ECL interface devices, the primary and most negative power supply terminal.

2.3.7 – VHH, SPECIAL FUNCTION ENABLE VOLTAGE

A special high voltage logic level (super voltage) that enables special on–chip functions.

2.3.8 – VPP, PROGRAMMING POWER VOLTAGE

A special high voltage supply that supplies the potential and energy for altering the state of certain non–volatile memory arrays. On some devices the presence of VPP also acts as a PROGRAM ENABLE signal (see P).

2.3.9 – VREF, REFERENCE POWER SUPPLY

A power supply that acts as a reference for determining internal threshold voltages but does not supply any substantial power to the device.

2.3.10 – VSS, (GND), GROUND REFERENCE or SOURCE POWER VOLTAGE

The ground reference voltage for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the symbol is often used interchangeably with GND.

2.3.11 – VSSQ, (GNDQ), OUTPUT STAGE SOURCE POWER VOLTAGE or OUTPUT STAGE GROUND REFERENCE

The ground reference voltage for the data output (Q) or input/output (DQ) pins. Other, non–data, output pin transistors may also be designated to be referenced to this ground pin. Internal to the device, this pin shall be DC isolated from the primary ground reference (VSS) pin and any other ground reference pin. External to the device it must be DC common with the primary ground reference.

2.4 DEVICE TYPE NAMES

2.4.1 – ASIC, Programmable Application Specific Device
A complex array of logic elements whocs interconnection pattern can be field programmed to fill the needs of specific applications.

2.4.2 – BDRAM, Burst DRAM
A DRAM that has BURST mode data capability.

2.4.3 – Bxxx,
Device names that have the prefix "B" are devices that have a "Burst" data capability.

2.4.4 – DPM, Dual Port Memory
Any memory that has two essentially identical data ports.

2.4.5 – DPSRAM, Dual Port Static RAM
A static RAM that contains two sets of identical random access address and data ports.

2.4.6 – DRAM, Dynamic Random Access Memory
These devices are made using Dynamic RAM circuit configurations that have data storage that must be refreshed periodically.

2.4.7 – FEEPROM, Flash EEPROM
An EEPROM in which clearing can be performed only on blocks or the entire array.
Note: there are no restrictions on the block archetecture in the fefinition of FEEPROM. the blocks within a device may be of various capacities ranging from a single address to the entire memory array.

2.4.8 – EEPROM, Electrically Erasable Programmable Read Only Memory
A reprogammable ROM in which cells may be erased electrically and in which each cell may be reprogrammed electrically.

2.4.9 – EPROM, Erasable Programmable Read Only Memory
A reprogrammable ROM in which all cells may be simultaneously erased using ultraviolet light and in which each cell may be reprogrammed electrically.

2.4.10 – GRAM, Gaphics DRAM
A DRAM that contains special graphics features, similar to those contained in a MPDRAM. When the term has a prefix "S", it becomes synchronous GRAM.

2.4.11 – LPROM, Latched PROM
A PROM that contains a latch register for the output data.

2.4.12 – MPDRAM, Multiport DRAM
A dynamic RAM that contains in addition to the conventional random access data and address port, a serial access port that allows serial access to a portion of the stored data in a way which is independent of the normal RAM data terminals and in which simultaneous serial and random operations may be executed. This type of memory has been referred to as "Video RAM" because of its primary field of application.

2.4.13 – MPM, Multiport Memory
Any memory array that has two or more data ports which do not have the same architecture. The most common form of MPM is one in which there is a random access port and a serial access port.

2.4.14 – MPRAM, Multiport RAM
A RAM that has more than one port for data, address, and control, that are not identical in nature. Normally at least one port provides parallel access while one other provides serial access. When the term has a prefix "S", it becomes s synchronous MPDRAM.

2.4.15 – NVRAM, Non–Volatile Random–Access Memory
An SRAM in which provisions exist on chip for the state of the cells to be saved when power is removed.

2.4.16 – PLD, Programmable Logic Array
An array of logic elements in which the interconnection pattern can be programmed (either mask or user programmed) to perform specific logic functions.

2.4.17 – PROM, Programmable Read–Only Memory
A field programmable ROM which can have the data content of each cell altered only once.

2.4.18 – PSRAM, Pseudo Static Random–Access Memory
A combinational form of dynamic RAM that incorporates various refresh and control circuits on–chip (e.g. refresh address counter and multiplexer, interval timer, and/or arbiter). These circuits allow the PSRAM operating characteristics to closely resemble those of a SRAM.

2.4.19 – RAM, Random–Access Memory
A memory in which access to all storage data can be achieved in essentially the same time, independent of the location. In a multiport memory, this term refers to that portion of the array which contains the memory cell array and its drivers, sense amplifiers, and control circuitry and the circuitry associated with the normal random access data port.

2.4.20 – ROM, Read–Only Memory
A memory in which the contents are not intended to be altered during operation.

2.4.21 – RPROM, Registered PROM
A PROM that contains a "D" type FF register for the output data.

XILINX EXHIBIT 1010
Page 61

2.4.21 – Sxxx
The prefix "S" on a device term can mean either "Static" as in SRAM, "Serial" as in SAM, or "Synchronous" as in SDRAM and SGRAM.

2.4.22 – SAM, Serial Access Memory
A memory (or serial port in a multiport memory) in which data is accessed sequentially and the time for access depends on the location of the data desired. In a multiport memory, this term refers to that portion of the device which is related to the serial access port and its associated functions.

2.4.23 – SDRAM, Synchronous DRAM
A DRAM that has a clocked synchronous interface.

2.4.24 – SGRAM, Synchronous Graphics DRAM
A GRAM that has a synchronous interface.

2.4.25 – SMPDRAM, SVRAM, Synchronous MPDRAM (VRAM)
An MPDRAM that has a synchronous interface on all ports.

2.4.26 – SRAM, Static Random Access Memory
A read/write memory in which the data is retained in the absence of control signals generated inside or outside the integrated circuit.

2.4.27 – SSRAM, Synchronous Static RAM
An SRAM that has input and/or output buffers (either register or latch), that are controlled by an externally supplied clock (or clocks).

2.4.28 – VRAM, Video Ram
A term commonly used in the Industry to describe the device class referred to in this standard as MPDRAM. It is a multi–ported DRAM that has features keyed to the video buffer application

XILINX EXHIBIT 1010
Page 62

2.5 MISCELLANEOUS DEVICE RELATED TERMS

2.5.1 – Bit Plane
In a semiconductor memory device having a data interface that is wider than 1 bit, those storage cells and associated circuitry which are associated with a given bit in the data interface.

2.5.2 – Bit Wide
A class of memory devices that have only a single–bit data interface.

2.5.3 – Byte Wide
A class of memory devices that have a parallel 8–bit or occasionally 9–bit data interface.

2.5.4 – K
When describing the storage capacity of a memory device the quantity K=1024 is used.

2.5.5 – M
When describing the storage capacity of a memory device, the quantity M=2 exp 20 or 1024 K is used.

2.5.6 – MX, Multiplexed
A term describing a device that has pins used for different purposes at different times as a function of one or more of its control inputs. The signal groups that are multiplexed onto a common pin set are given together as in: AA MX signifying ADDRESS, ADDRESS multiplex, OR ADQ MX signifying ADDRESS, DATA IN, DATA OUT multiplex.

2.5.7 – Nibble Wide
A class of memory devices that have a parallel 4–bit data interface. This term should not be confused with "nibble mode" (see 3.1.3.2), which refers to a serial data access mode in memories.

2.5.8 – Word Wide
A class of memory devices that have a parallel 16–bit or longer data interface.

2.6 Special Operational Cycles for MPDRAM

The following terms describe a series of special operational cycles for MPDRAM. They are presented in the order of their logical relationships rather than alphabetically.

2.6.1 LOGIC SETUP, (LS)

A special non-memory cycle in which the logic state of the device is set up to actuate the desired mode of operation for future memory cycles. The selected mode is normally persistent until canceled by some subsequent special control cycle.

2.6.2 INTERNAL REFRESH, (CBR)

Defined in 3.9.2.3.

2.6.3 WRITE TRANSFER, (WT)

An operation in which the data to be written is introduced through the serial port and is then transferred internally to the memory array data bus for writing into the cells. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial register into which data is entered. Data is entered serially from this point with wrap around when the end of the register is reached. The contents of the full serial register are transferred in parallel. In addition to the normal write transfer, there are numerous other types of special write transfers defined in the following paragraphs.

2.6.4 PSEUDO WRITE TRANSFER, (PWT)

This is a non-memory cycle in which the operational mode of the serial port is changed from output to input. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial data register into which data is entered. Data is entered serially from this point with wrap around when the end is reached.

2.6.5 MASKED WRITE TRANSFER, (MWT)

A write transfer in which the transfer of new data from the serial register into the memory array is controlled by a "Write Mask" that is supplied on the DQ(n) terminals. This mask allows the selective writing of new data into one or more of the data bit planes of the storage array corresponding to the data bits of the parallel array. In a normal implementation, a high M value enables the writing of new data while a low M inhibits the writing and leaves the existing data unchanged. A new mask value must be supplied for each masked write cycle.

2.6.6 FLASH WRITE WITH MASK, (FWM)

A write cycle in which the contents of an entire row of the memory array can be selectively set to a stated value. The "mask" value determines which bit planes are to be altered while the "color register" (qv) contains the data value to be written. The color register is loaded in a previous "Load Color Register" cycle with a persistent value. The mask value is supplied during the cycle on the DQ(n) terminals. A new mask value must be supplied for each cycle performed. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.7 SPECIAL WRITE TRANSFER

A write transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal SAM to RAM data transfers. These variations are defined in the following paragraphs.

2.6.8 SPLIT WRITE TRANSFER, (SWT)

A write transfer in which the SAM data register is split into two halves and the data is transferred to the RAM data bus separately after each half of the SAM register is filled.

2.6.9 AUTO-LOAD WRITE TRANSFER, (AWT)

A split SAM data register transfer in which the transfer from each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is filled.

2.6.10 READ TRANSFER, (RT)

A read operation in which the contents of one row of the memory array is transferred into the SAM data register in parallel.

2.6.11 SPECIAL READ TRANSFER

A read transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal RAM to SAM data transfers. These variations are defined in the following paragraphs.

2.6.12 SPLIT READ TRANSFER, (SRT)

A read transfer in which the SAM data register is split into two halves and the data is transferred from the RAM data bus separately into each half of the SAM register as it is needed for transfer to the SDQn terminals.

2.6.13 AUTO-LOAD READ TRANSFER, (ART)

A split SAM data register transfer in which the transfer into each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is emptied.

XILINX EXHIBIT 1010
Page 64

3.5.1.10 - 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
PACKAGE--32 LEAD TSOP-1, 8 mm X 18.4 mm
PIN ASSIGNMENT--Fig. 3.5.1-10

3.5.1.11 - EXTENDED FEATURE SET FOR 256K BIT EEPROM

This standard specifies features beyond the existing pinout standards that need to be standardized for 32K X 8 EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.1..

3.5.1.11.1 - REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 32K Byte EEPROMs and must be implemented to be in compliance with this standard:
-Operate with a primary power supply of 5.0 V nominal
-Operate in conformance with the standard truth table
-Have read and write timing cycles which are consistent with the standard timing diagrams
-Contain Data & Address Latches for Write cycles
-Operate with self timed write cycles
-Operate with input levels between 0 and 5 Volts.

3.5.1.11.2 - OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:
-Page Write Mode with standard write cycle timings
-Minimum page size of 16 Byte in page write mode
-DATA\ Polling
-Software Data Protect Option
-Hardware Mass Erase (All 1's)
-Software Mass Erase (All 1's)

3.5.1.12 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM

This Standard provides an optional command set for DUAL-SUPPLY EEPROM devices (commonly known as FLASH EEPROM). This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.2-4

3.5.1.13 - 512K BY 8 DUAL-SUPPLY EEPROM IN RCC

CAPACITY--512K WORDS OF 8 BITS,
PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
PIN ASSIGNMENT--Fig. 3.5.1-12

3.5.1.14 - 128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP-1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
THESE DEVICES ARE APPROVED IN THREE PACKAGES:
DIP PACKAGE--32 LEAD DIP, 15.24 mm (0.6") WIDE WITH 2.54 mm (0.1") PP
PIN ASSIGNMENT--Fig. 3.5.1-13
RCC PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
PIN ASSIGNMENT--Fig. 3.5.1-14
TSOP-1 PACKAGE--32 LEAD TSOP-1, 8 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT--Fig. 3.5.1-15

3.5.1.15 – 256K, 512K, & 1M BY 8 DUAL–SUPPLY EEPROM IN TSOP–1

CAPACITY—256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE—40 LEAD TSOP–1, 10 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT—256K, 512K, Fig. 3.5.1–18
PIN ASSIGNMENT—1M, Fig. 3.5.1–16

The 256K & 512K devices have a different pin assignment pattern from the 1M device, therefor are not backward compatible with the 1M device.

3.5.1.16 – 1M TO 8M BY 8 SINGLE–SUPPLY EEPROM FAMILY IN TSOP–1

CAPACITY—1M, 2M, 4M, & 8M WORDS OF 8 BITS,
PACKAGE—48 LEAD TSOP1, 12 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–17

3.5.1.17 – 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP–2

CAPACITY—8K WORDS OF 256 OR 264 BYTES, SERIALLY ACCESSED
PACKAGE—44/40 LEAD TSOP2, 10.16 mm WIDE WITH 0.8 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–19 A
CONTROL & LOGIC TABLES—Figs. 3.5.1–19 B & C

3.5.1.18 – 1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM FAMILY IN PSOP

CAPACITY—1M & 2M WORDS OF 8 BITS,
PACKAGE—44 LEAD PSOP 16 mm wide WITH 1.27 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–20

XILINX EXHIBIT 1010
Page 66

Logic Table

Function	CL	AL	$\overline{E}$	$\overline{W}$	$\overline{R}$	$\overline{WP}$
Command Input	H	L	L	⌐‾⌐	H	·
Data Input	L	L	L	⌐‾⌐	H	·
Address Input	L	H	L	⌐‾⌐	H	·
Address Output	L	H	L	H	⌐‾⌐	·
Serial Read & Output	L	L	L	H	⌐‾⌐	·
During Auto Program	·	·	·	·	·	H
During Auto Erase	·	·	·	·	·	H
During Busy State	·	·	·	·	·	H
Program/Erase Protect	·	·	·	·	·	L

Serial Address Input

	ADQ0	ADQ1	ADQ2	ADQ3	ADQ4	ADQ5	ADQ6	ADQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	A15
3rd Cycle	A16	A17	A18	A19	A20	RFU	RFU	RFU

A0 ⇒ A7 : Column Address
A8 ⇒ A11 : NAND Address
A12 ⇒ A20 : Block Address

PIN DEFINITIONS

The following pin terms are used in this device, but some may not appear in Sec. 2 on terminology of this Standard,

CL: Command Latch Enable
$\overline{E}$: Chip Enable
$\overline{R}$: Read Enable
RY: Ready
AL: Address Latch Enable
$\overline{W}$: Write Enable
$\overline{WP}$: Write Protect
ADQn: Address/Data/Command Multiplex

FIGURE 3.5.1–19 C
8K BY 256B or 8K BY 264B SERIAL ACCESS EEPROM LOGIC TABLE

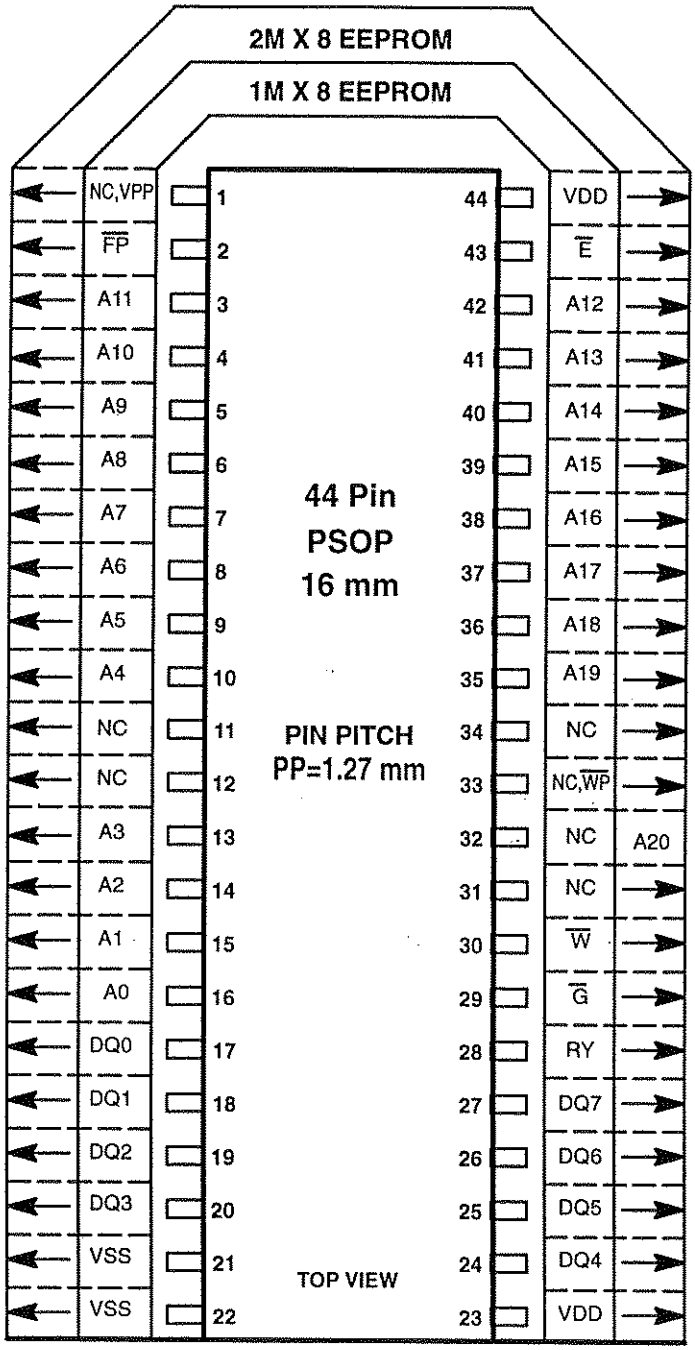


FIGURE FIGURE 3.5.1–20
1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP

Release 7

3.5.2.1 – 4K TO 32K BY 16 EEPROM IN DIP

CAPACITY—4K TO 32K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.5.2–1

3.5.2.2 – 4K TO 256K BY 16 EEPROM IN SCC

CAPACITY—4K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.5.2–2

3.5.2.3 – 256K TO 128M BY 16 EEPROM IN DIP AND SOP

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, and 128M WORDS OF 16 BITS
PACKAGE—44, 48 or 52 PIN DIP and SOP, 0.600" WIDE
PIN ASSIGNMENTS—256K TO 2M, Fig. 3.5.2–4
PIN ASSIGNMENTS—4M TO 128M, Fig. 3.5.2–3

3.5.2.4 – 1M TO 4M BY 16 DUAL SUPPLY EEPROM IN SSOP

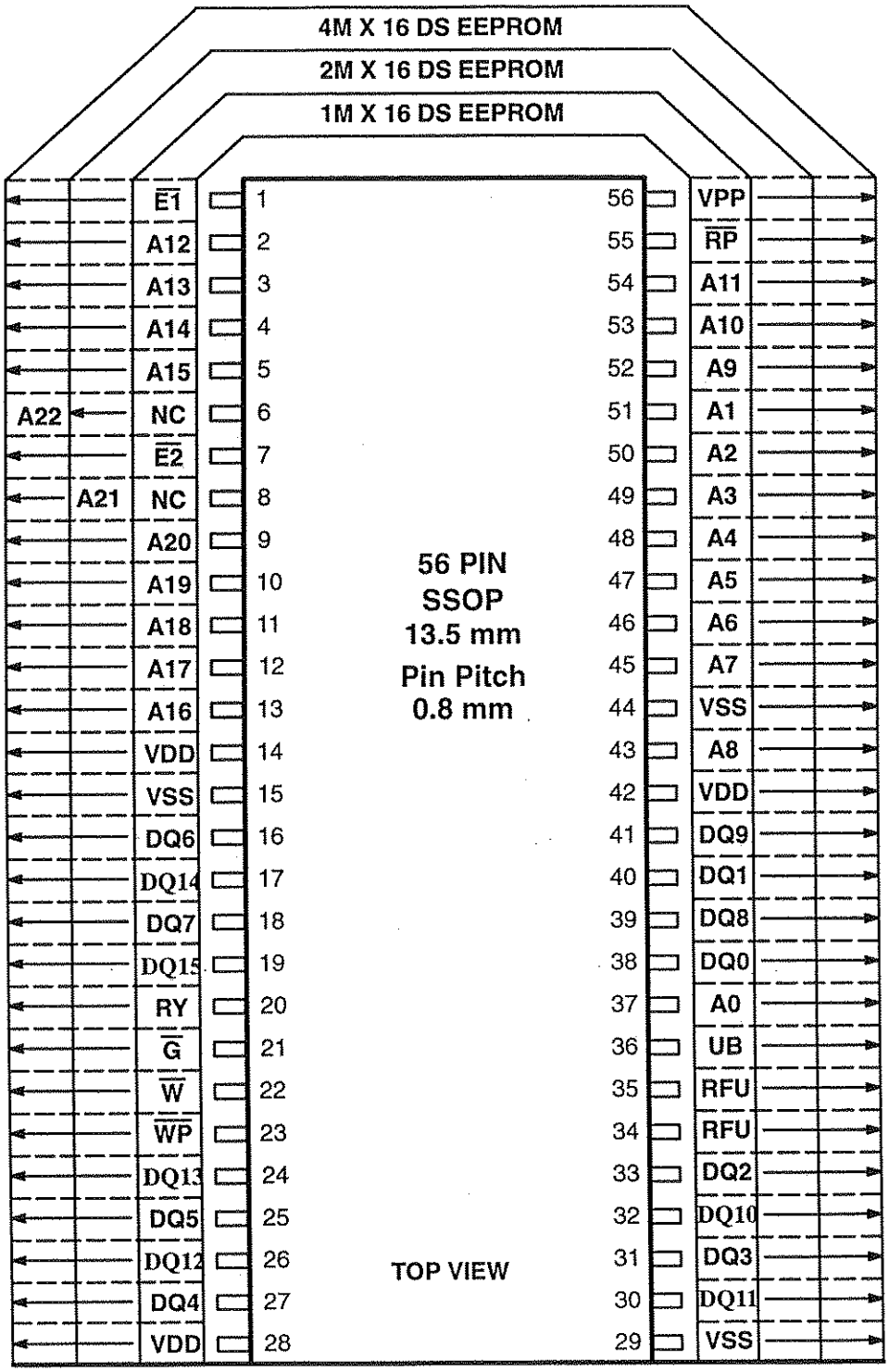
CAPACITY—1M, 2M, 4M WORDS OF 16 BITS,
PACKAGE—56PIN SSOP, 13.5 mm WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.5.2–5

3.5.2.5 – 1M, 2M, & 4M DENSITY, BY 8 & 16 FEEPROM IN PSOP

CAPACITY—1M, 2M, & 4M, BITS WITH x8 OR x16 DATA INTERFACE.
—128K, 256K, OR 512K WORDS OF 8 BITS
—64K, 128, OR 256K WORDS OF 16 BITS
PACKAGE—44 PIN PSOP, 16 mm WIDE
PIN ASSIGNMENTS—Fig. 3.5.2–6
POWER SUPPLIES—SINGLE OR DUAL SUPPLY DESIGN

3.5.2.6 – 1M TO 32M DENSITY, BY 8 & 16 FEEPROM IN TSOP1

CAPACITY—1M, 2M, 4M, 8M, 16M, & 32M BITS WITH x8 OR x16 DATA INTERFACE.
—128K, 256K, 512K, 1M, 2M, OR 4M WORDS OF 8 BITS
—64K, 128, 256K, 512K, 1M, OR 2M WORDS OF 16 BITS
PACKAGE—44 PIN TSOP1, 20 mm X 16 mm with 0.5 mm PP.
PIN ASSIGNMENTS—Fig. 3.5.2–7
POWER SUPPLIES—SINGLE OR DUAL SUPPLY DESIGN



	UB	A0	DQ0 ⇒ DQ7	DQ8 ⇒ DQ15
Word Access	VIH	X	Even Byte	Odd Byte
Odd Byte Access	VIL	VIH	Odd Byte	High Z
Even Byte Access	VIL	VIL	Even Byte	High Z

FIGURE 3.5.2–5
1M TO 4M BY 16 DUAL SUPPLY EEPROM IN SOP

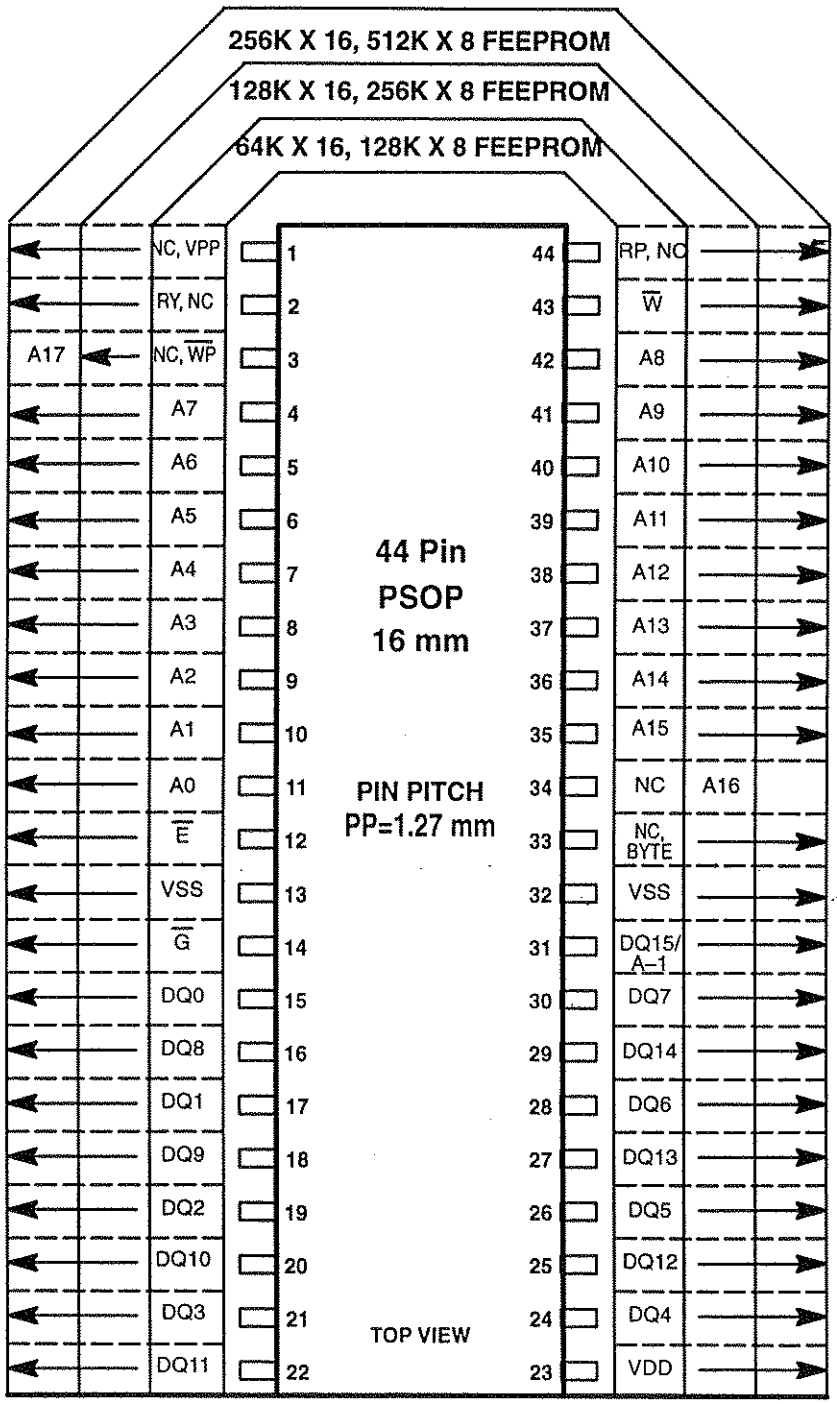
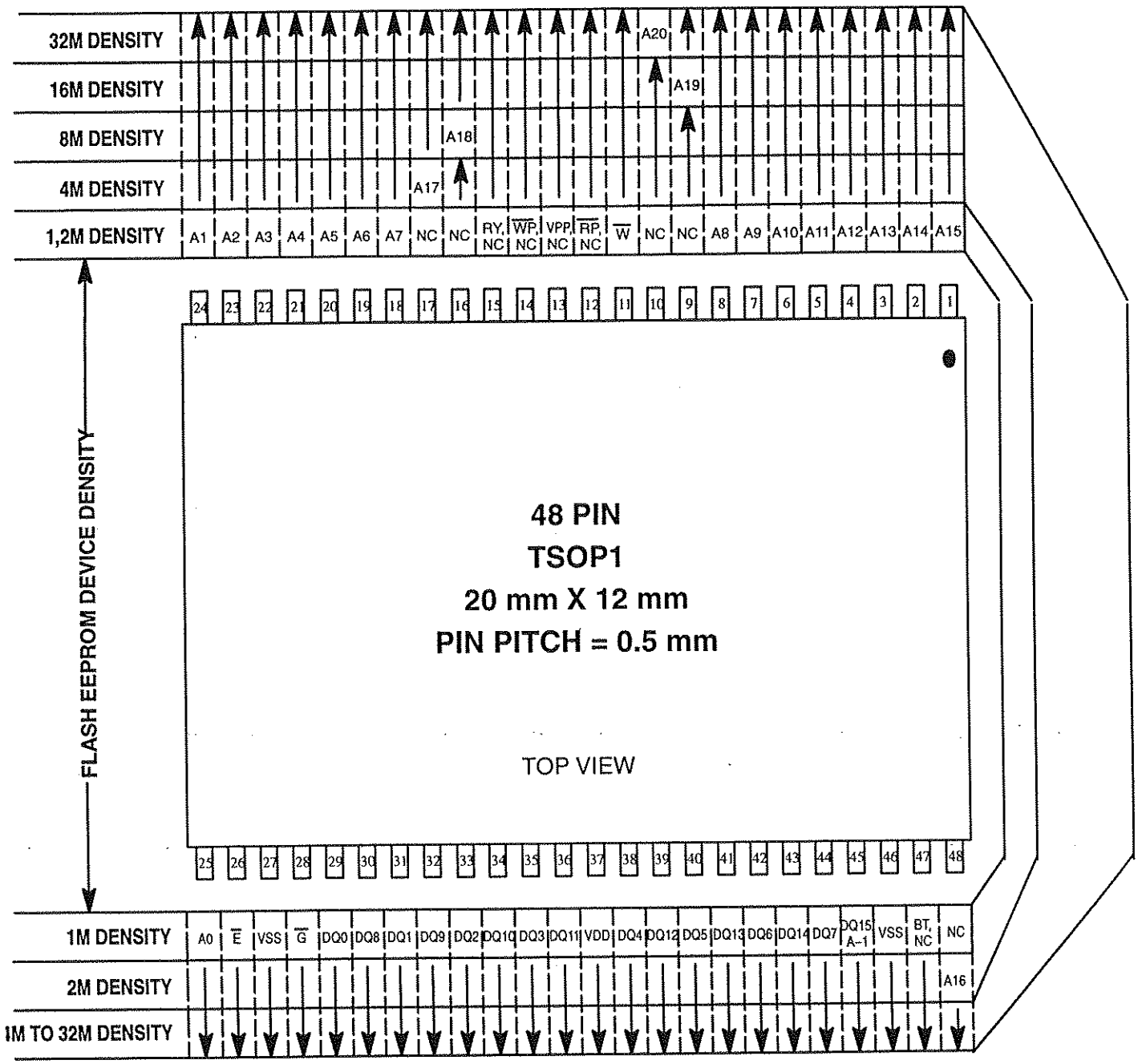


FIGURE 3.5.2–6
1M, 2M, & 4M DENSITY BY 8 & 16 SINGLE OR DUAL SUPPLY FEEPROM IN PSOP, 128K TO 512K BY 8 OR 64K TO 256K BY 16

Release 7



ORGANIZATION VS. DENSITY TABLE

DENSITY	X16	X8
1Mb	64K X 16,	128K X 8
2Mb	128K X 16	256K X 8
4Mb	256K X 16	512K X 8
8Mb	512K X 16	1M X 8
16Mb	1M X 16	2M X 8
32Mb	2M X 16	4M X 8

FIGURE 3.5.2–7
1M TO 32M DENSITY BY 8 & 16 SINGLE OR DUAL SUPPLY FEEPROM IN TSOP1, 64K TO 2M BY 16 OR 128K TO 4M BY 8

3.5.3 EEPROM EXTENDED FEATURES

There are a number of extended feature standards for EEPROMS that depend on the capacity and number of power supplies used in the design. The various standards and their location are listed as follows:

– 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARDS. PP 3.5.1–15 to 22

– DUAL POWER SUPPLY EEPROM COMMAND SET. Fig. 3.5.3.2, P 3.5.3–13

– EXTENDED FEATURE SET FOR EEPROM (256Kb and larger) . Sec. 3.5.3.1 following

– SINGLE POWER SUPPLY EEPROM COMMAND CODES. SEC. 3.5.3.3

– EEPROM TOGGLE BIT FEATURE (larger than 256 Kb) . Sec. 3.5.3.4

3.5.3.1 – EXTENDED FEATURE SET FOR EEPROM (256Kb and larger)

This standard specifies features beyond the existing pinout standards that need to be standardized for EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.3.2

3.5.3.1.1 – REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 256Kb and larger EEPROMs and must be implemented to be in compliance with this standard:

–Operate with a primary power supply of 5.0 V and lower nominal
–Operate in conformance with the defines standard command set
–Operate in conformance with the standard truth table
–Have read and write timing cycles which are consistent with the standard timing diagrams
–Contain Data & Address Latches for Write cycles
–Operate with self timed write cycles
–Operate with input levels between 0 and 5 Volts.
–DATA\ Polling

3.5.3.1.2 – OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:

–Page Write Mode with standard write cycle timings
–Minimum page size of 16 Byte in page write mode
–Software Data Protect Option
–Hardware Mass Erase (All 1's)
–Software Mass Erase (All 1's)

3.5.3.2 – OPTIONAL COMMAND SET FOR DUAL–SUPPLY EEPROM

This Standard provides an optional command set for DUAL–SUPPLY EEPROM devices. This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.1–11

3.5.3.3 – SINGLE POWER SUPPLY EEPROM COMMAND CODES

These tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

3.5.3.4 – EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies. The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

EEPROM EXTENDED FEATURE STANDARD (256Kb and greater)

The mandatory features, whlch are the minimum set necessary to achieve functional compability for 256Kb and larger EEPROMs, must be implemented to be in compliance with this standard. Any, all, or none of the optlonal features may be implemented at the manufacturers discretlon. However, if an optional feature deflned In thls standard is implemented, it must operate as specltied in this standard to be in compllance with the standard.

Other features not described in the standard may be incorporated and the device still be in compliance as long as they are compatible wlth the required and optlonal features in this standard.

BYTEWIDE EEPROM REQUIRED STANDARD FEATURES (256Kb and larger)

1. VDD SUPPLY IS 5 V OR LESS NOMINAL
2. STANDARD LOGIC TRUTH TABLE (FIG. A1–1)
3. STANDARD COMMAND SET (Fig. A1–2)
4. STANDARD READ CYCLE TIMING (FIG. A1–3)
5. STANDARD BYTE WRITE CYCLE FEATURES
   –TIMING (FIG. A1–4)
   –DATA AND ADDRESS LATCHES
   –SELF–TIMED WRITE CYCLES
   –ALL INPUT LEVELS IN RANGE BETWEEN 0 V AND 5 V.
6. DATA POLLING (FIG. A1–5)
   MUST MEET NORMAL READ CYCLE AND WRITE CYCLE TIMING

OPTIONAL FEATURES

1. PAGE WRITE MODE (FIG. A1–6)
   –STANDARD PAGE WRITE CYCLE TIMING
   –16 BYTE MINIMUM PAGE SIZE (A0 – A3)
2. SOFTWARE DATA PROTECT OPTION (FIGS. A1–7 & A1–8)
3. HARDWARE MASS ERASE (ALL 1'S) (FIG. A1–9)
4. SOFTWARE MASS ERASE (ALL 1'S) (FIG. A1–10)

EEPROM TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
L	L	H	READ	Q	ACTIVE
L	H	L	WRITE	D	ACTIVE
H	X	X	STANDBY AND WRITE INHIBIT	HIGH Z	STANDBY
L	L	L	WRITE INHIBIT	HIGH Z	ACTIVE
L	H	H	WRITE INHIBIT	HIGH Z	ACTIVE

~NOTE: $\overline{G}$ functions as both an output control and a write Inhibit control in this EEPROM Standard.

FIGURE A1–1

SINGLE–SUPPLY EEPROM COMMAND SET

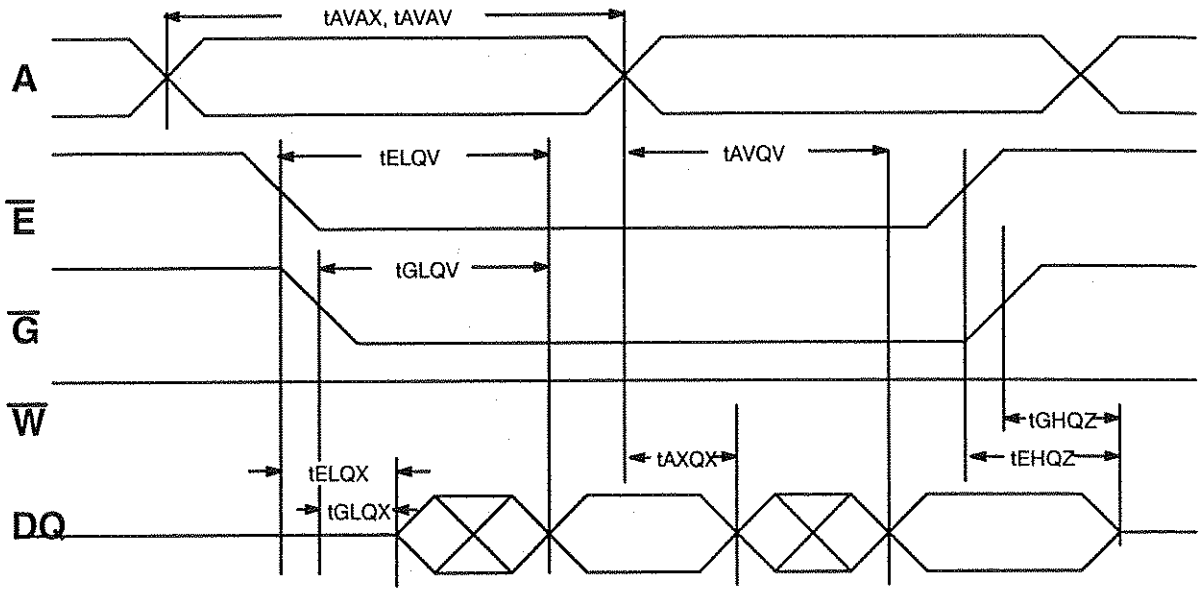
Bus Command Table

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	FOH										
Rearl/Reset	4	5555H	AAH	2AAAH	55H	5555H	FOH	RA	RD				
Autoselect	4	5555H	AAH	2AMH	55H	5555H	90H						
Fyte Program	4	5555H	AAH	2AMH	55H	5555H	AOH	PA	Data				
Chip Erase	6	5555H	AAH	2AMH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	1OH
Sector Erase	6	5555H	AAH	2AMH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don~t rare), Data (BOH)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don~t care), Data (30H)											

Note: A0 is always LSB regardless of data width.

FIGURE A1–2

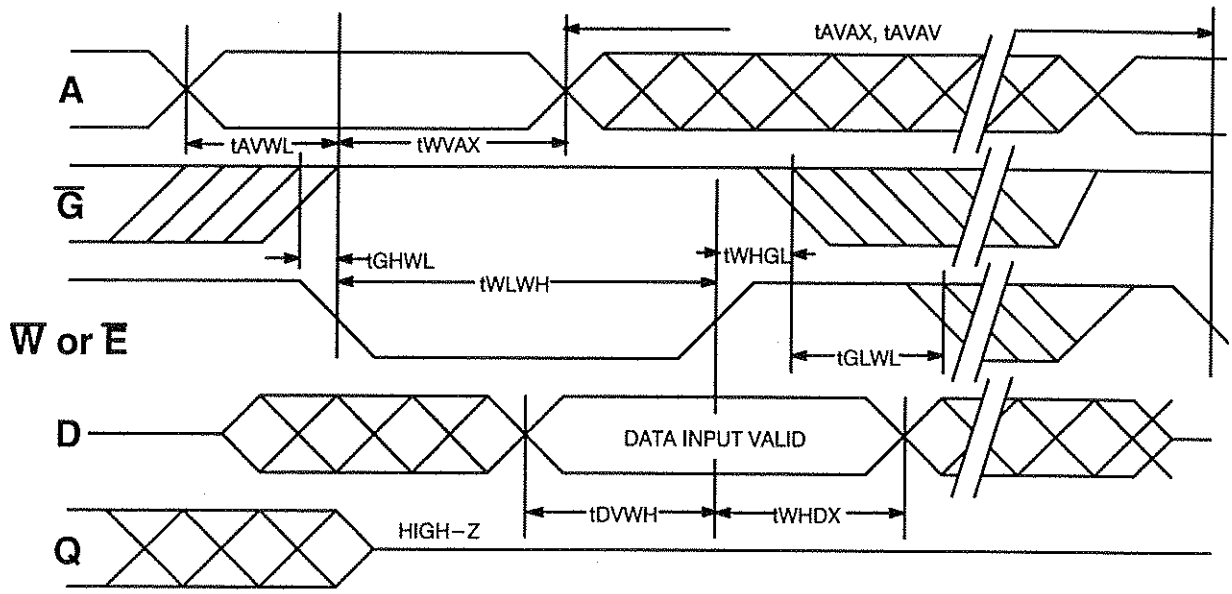
SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL	DESCRIPTION
tAVAX, tAVAV	ADDRESS VALID TO ADDRESS CHANGE (READ CYCLE TIME)
tELQV	$\overline{E}$ LOW TO OUTPUT VALID (CHIP ENABLE ACCESS TIME)
tAVQV	ADDRESS VALID TO OUTPUT VALID (ADDRESS ACCESS TIME) tGLQV
tELQX	$\overline{E}$ LOW TO ACTIVE OUTPUT
tGLQX	$\overline{G}$ LOW TO ACTIVE OUTPUT
tEHQZ	$\overline{E}$ HIGH TO HIGH–Z OUTPUT
tGHQZ	$\overline{G}$ HIGH TO HIGH–Z OUTPUT
tAXQX	ADDRESS INVALID TO DATA OUT INVALID

FIGURE A1–3

SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
tWLWL, tELEL	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (WRIITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SETUP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tGLWL, tGLEL	$\overline{G}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW ($\overline{G}$ LOW WRITE INHIBIT SETUP TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1–4

SINGLE SUPPLY EEPROM DATA BAR POLLING AND AUTOMATIC WRITE OPERATION STATUS

IN PROGRESS	AUTO PROGRAMMING	DQ7	TOGGLE	0	0	0	RFU
	PROGRAMMING IN AUTO–ERASE	0	TOGGLE	0	0	1	
	ERASING IN AUTO–ERASE	0	TOGGLE	0	1	1	
EXCEEDED TIME LIMITS	AUTO PROGRAMMING	DQ7	TOGGLE	1	0	0	RFU
	PROGRAMMING IN AUTO–ERASE	0	TOGGLE	1	0	1	
	ERASING IN AUTO–ERASE	0	TOGGLE	1	1	1	

FIGURE A1–5

Definition of Automatic Algorithm

Automated Write
Data Command = 10h/ Byte Address and Data (1st/2nd bus cycle)

Write the automated program set–up command (10h) and program command (Byte address and program data). The device automatically times the program pulse width, provides the program verify to guarantee adequate data retention, and counts the number of pulses required for complete programming.

A data polling status bit (output pin DQ7) and a toggle bit status (output pin DQ6) provide feedback to the system as to the status of the programming operation. Either DQ7 or DQ6 can be used.

Data Polling– DQ7

While the automated algorithms are in operation, an attempt to read the device (address = don't care) will produce the compliment of the intended valid program or erase data on DQ7. Upon completion of the automated algorithm, an attempt to read the device will produce the valid data expected from DQ7.

The data polling feature is valid after the rising edge of the second W pulse of the two write pulse sequence.

Toggle Bit– DQ6

While the automated algorithms are in progress, successive attempts to read data (address = don't care) from the device will result in DQ6 toggling between the logic levels "1" and "O". Once the automated operation is complete, DQ6 will stop toggling and valid data will be read.

The toggle bit is valid after the rising edge of the first W pulse of the two write pulse sequence, unlike data polling which is valid after the rising edge of the second W pulse. This

feature allows the user to determine if the device is partially through the two write pulse sequence.

Exceeded Timing Limits – DQ5

DQ5 will indicate if the program or erase pulse counts have exceeded the specified limits. Under this condition, DQ5 will provide a logic "1 " output.

Hardware Sequence Flash – DQ4

If the device has exceeded the specified erase or program time and DQ5 is at logic level "1", then DQ4 will indicate which step in the algorithm the device exceeded limits. A logic level "O" in DQ4 indicates that the programming limits were exceeded. A logic level "1" indicates erase limits were exceeded.

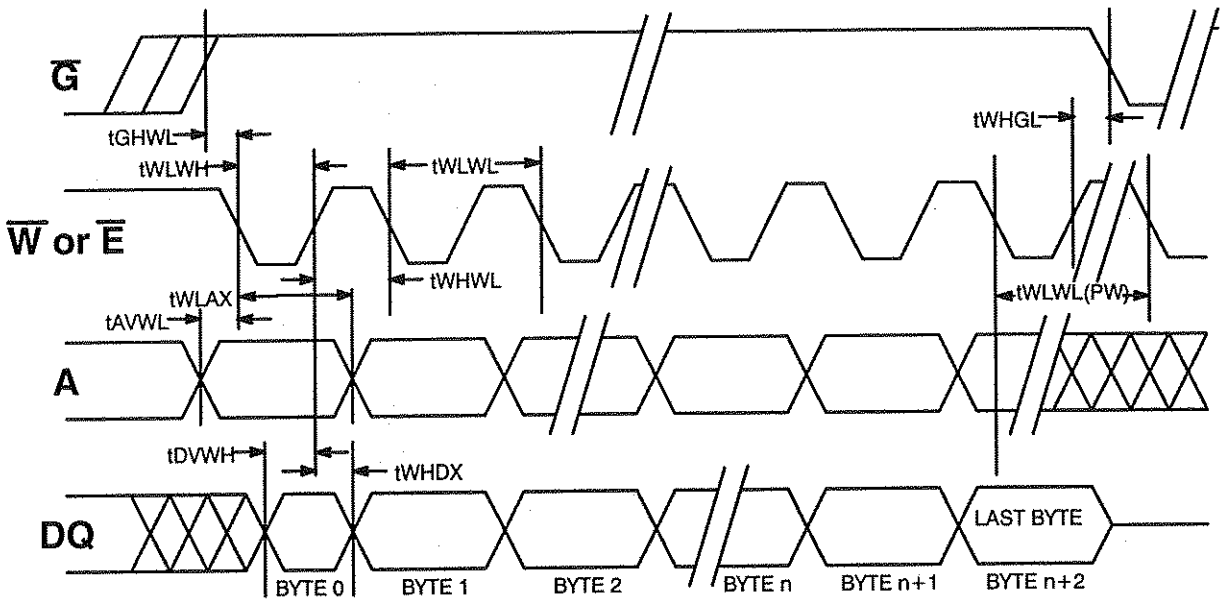
Sector Erase Timer– DQ3

After the compietion of the initial sector erase command sequence, the sector erase time–out of 100μs will begin. If another sector erase command is written within the 100μs time–out window, the timer is reset.

If Data Polling or the Toggle bit (DQ6) indicates that the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is at logic level "1" the internally controlled erase cycle has begun. Any further attempts to write subsequent commands to the device will be ignored untilthe erase operation is completed which is indicated by Data Polling or the Toggle bit. If DQ3 is at logic level "0", the device will accept additional sector erase commands.

DQ0–DQ2 are reserved for future use.

SINGLE SUPPLY EEPROM PAGE MODE WRITE CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
tWLWL(PW)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (PAGE WRIITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SETUP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)
tWLWL, tELEL	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW (BYTE LOAD CYCLE TIME)

FIGURE A1–6

SINGLE SUPPLY EEPROM OPTIONAL SOFTWARE DATA PROTECTION

–SOFTWARE DATA PROTECTION IS A DIFFERENT METHOD OF PREVENTING INADVERTANT WRITE OPERATIONS IN A NONVOLATILE MEMORY COMPARED TO THE "HARDWAREU METHODS, SUCH AS: E, G, AND W LOGIC COMBINATIONS, VCC LEVEL DETECTORS, AND POWER UP TIMERS.

–A SPECIFIC DATA AND ADDRESS SOFTWARE SEQUENCE MUST BE ISSUED TO ENABLE A SINGLE PAGE OR BYTE WRITE.

–DATA INPUT FORMAT: D7/D6/D5/D4/D3/D2/D1/D0

–ADDRESS FORMAT: A14/A13/A12/A11/A10/A9/A8/A7/A6/A5/A4/A3/A2/A1/A0

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS WRITE"	5555H	AAH
2	"ACCESS WRITE"	2AAAH	55H
3	"ACCESS WRITE"	5555H	A0H
4	"PAGE WRITE"	Address	Data

–ALL WRITES MUST CONFORM TO THE PAGE MODE TIMING REQUIREMENTS FOR THE PART.

–SINCE THE PAGE ADDRESS IS CHANGED (A VIOLATION OF THE NORMAL PAGE MODE WRITE CYCLE), THE FIRST THREE "ACCESS" WRITES (STEPS 1–3) ARE USED ONLY FOR SOFTWARE ACCESS, NO DATA IS ACTUALLY WRITTEN TO THE EEPROM.

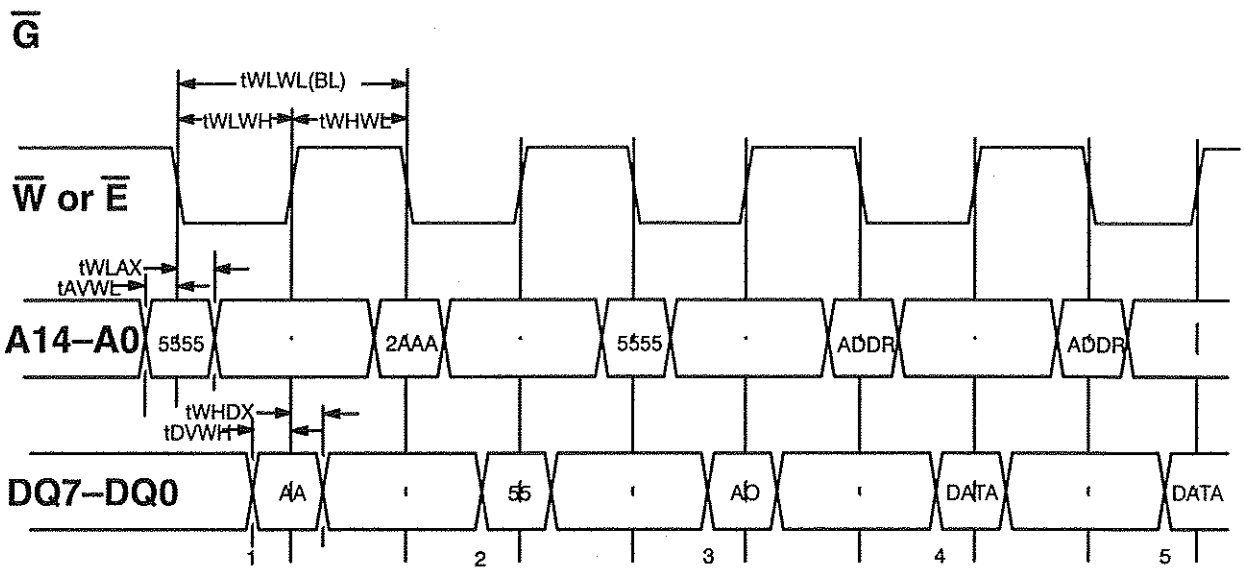
–THE FIRST TIME THIS SEQUENCE IS APPLIED TO THE PART A NON–VOLATILE BIT IS SET, WHICH RECONFIGURES THE PART FROM HARDWARE PROTECTED ONLY TO HARDWARE AND SOFTWARE SEQUENCE PROTECTED. ONCE THIS BIT IS SET, THE SOFTWARE SEQUENCE MUST BE USED TO WRITE TO THE PART.

–THE SOFTWARE PROTECTION CAN BE DISABLED AND THE PART RECONFIGURED TO HARDWARE–ONLY PROTECTION, BY APPLYING THE SIX STEP SOFTWARE SEQUENCE BELOW:

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	20H

FIGURE A1–7

SINGLE SUPPLY EEPROM SOFTWARE DATA PROTECTION TIMING



NOTE 5: Software Data Protection Timings are referenced to $\overline{W}$ or $\overline{E}$ Inputs, whichever is last going LOW, and the $\overline{W}$ or $\overline{E}$ Inputs, whichever is first going HIGH.

SYMBOL (NOTE 5)	DESCRIPTION
tWLWL(BL), tELEL(BL)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW BYTE LOW CYCLE TIME
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tWHWL, tEHEL	$\overline{W}$ OR $\overline{E}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME (WRITE HIGH RECOVERY)
tAVWL tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SET–UP TIME)
tWLAX, ELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID TIME (ADDRESS HOLD TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX. tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1–8

SINGLE SUPPLY EEPROM OPTIONAL HARDWARE MASS ERASE (ALL 1'S) FEATURE

– IF A HARDWARE MASS ERASE MODE IS IMPLEMENTED ON THE 256K EEPROM, THE FOLLOWING CONVENTIONS MUST BE FOLLOWED:

– $\overline{E}$ = LOW LOGIC LEVEL

– $\overline{W}$ = LOW LOGIC LEVEL

– $\overline{G}$ = SUPER VOLTAGE (WAVEFORM, LEVEL AND TIMING TO BE DETERMINED BY THE MANUFACTURER).

– DQ0 – DQ7 = ALL HIGH LOGIC LEVEL (FFH)

– A0 – A14 = DON'T CARE (EITHER HIGH OR LOW LOGIC LEVELS)

FIGURE A1–9

SINGLE SUPPLY BIT EEPROM OPTIONAL SOFTWARE MASS ERASE (ALL 1'S) FEATURE

IF A SOFTWARE MASS ERASE FEATURE IS IMPLEMENTED IN THE SINGLE SUPPLY EEPROM, IT MUST OPERATE BY APPLYING THE FOLLOWING SIX DATA/ADDRESS SEQUENCE TO THE PART.

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	10H

–ALL ACCESS WRITES MUST FOLLOW THE STANDARD PAGE MODE WRITE CYCLE TIMING SPECIFIED FOR THE PART,

–NO DATA IS ACTUALLY WRITTEN TO THE EEPROM DURING THE "ACCESS" WRITES. ONCE THE 6 STEP SEQUENCE IS COMPLETED, THE PART AUTOMATICALLY COMPLETES A MASS ERASE CYCLE INTERNALLY.

FIGURE A1–10

3.5.3.2 – DUAL POWER SUPPLY EEPROM COMAND SET

The following command set is applicable to dual power supply EEPROMs of any capacity.

COMAND CODES		
1st CYCLE	2nd CYCLE	OPERATION DESCRIPTION
00		RESERVED
10		Automated Write
20	20	Automated Block Erase
20	D0	Automated Block Erase
30	30	Automated Chip Erase
40		Algorithmic Write
50		Reserved
60	60	Algorithmic Block Erase
70		Reserved
80		Reserved
90		Read ID
A0		Algorithmic Erase Verify
B0		Reserved
C0		Algorithmic Write Verify
D0		Reserved
E0		Reserved
F0		

NOTE: All operands are in HEX.

This Standard provides an optional command set for use with the dual supply voltage EEPROM devices. This command set comprehends algorithmic commands and adds a set of automatic codes. A device may respond to either or both operating modes.

The Standard is applicable to devices with all data interface widths..

3.5.3.3 – SINGLE POWER SUPPLY EEPROM COMMAND CODES

The following tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

Three cycle Command Codes

Command	1st Cycle		2nd Cycle		3rd Cycle	
	Address	Data	Address	Data	Address	Data
SDP Write Disable	5555	AA	2AAA	55	5555	A0
Product Identification Entry	5555	AA	2AAA	55	5555	90
Reset/Product Identification Exit	5555	AA	2AAA	55	5555	F0
Note: All operands are in HEX.						

Six Cycle Command Codes

	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
Command	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
SDP Write Disable	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	20
Chip Clear (Erase)	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Note: All operands are in HEX												

All timings are per the EEPROM Software Data Protect Timing shown in Fig. A1–7

The address space required is encompassed by A0–A14; other address lines, e.g., A15, A16, can be at any level between VSS minimum and VCC maximum. The data space required is encompassed by DQ0–DQ7; other I/O lines, DQ8, DQ9, can be at any level between VSS minimum and VCC maximum.

3.5.3.4 – EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies.

–The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

–Whenever the part is read during a nonvolatile write cycle, the data on DQ6 will toggle, i.e., alternate between high and low, on alternate read cycles. Any address can be used when reading to get the Toggle Bit output. Typically, the first toggle out is high (logic "1").

–When the nonvolatile write cycle automatically times out, normal valid data is read at the outputs for any provided address.

–A software routine uses this feature to determine when the nonvolatile write cycle is complete.

–The normal read cycle timing specified for the part must be used for Toggle Bit read cycles.

–An additional parameter, tWHGL (tEHGL), must also be specified for the toggle bit cycle. tWHGL (tEHWL) is the minimum time the system must wait from the last rising edge of $\overline{W}$ ($\overline{WE}$) or $\overline{E}$ until the Toggle Bit read cycle is initiated by the falling edge of $\overline{G}$ ($\overline{OE}$).

–The actual completion of the nonvolatile write cycle is asynchronous with the system; therefore, a Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system will possibly get an erroneous result, i.e., valid data may appear to conflict with DQ6. In order to prevent spurious rejections, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the reject is valid.

3.7.5.10 – 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ

CAPACITY—32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES—SEPARATE DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE
PACKAGE—40 PIN DIP, 0.6" wide
—40 PIN SOJ, UNDEFINED
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–10

3.7.5.11 – 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC

CAPACITY—2K, 8K, 32K WORDS OF 9 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—68 PAD (PIN) SCC, 0.950" X 0.950"
PIN ASSIGNMENT—Fig. 3.7.5–11
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.12 – 32K BY 9 CACHE SRAM IN 44 SCC

CAPACITY—32K WORDS OF 9 BITS,
LOGIC FEATURES—Internal CACHE data compare logic
PACKAGE—44 TERMINAL SCC, 0.500" X 0.500"
PIN ASSIGNMENT—Fig. 3.7.5–12
This part contains specialized logic functions which allow it to be used to implement the CACHE memory function conveniently.

3.7.5.13 – 128K BY 8 SRAM IN TSOP1

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 20 mm X 8 mm, 0.5 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.7.5–13

3.7.5.14 – 128K BY 8 & 9 SSRAM IN SOJ

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN SOJ, 0.400"
PIN ASSIGNMENTS—Fig. 3.7.5–14

3.7.5.15 – 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP

CAPACITY—1K, 2K WORDS OF 8 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—48 PIN DIP, 0.600"
PIN ASSIGNMENT—Fig. 3.7.5–15
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.16 – 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO–N

CAPACITY—128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN LEADLESS CERAMIC SO, 0.400"
PIN ASSIGNMENT—Fig. 3.7.5–16
This family of parts is based on the evolutionary SRAM pinout family described in Sec. 3.7.5.7

3.7.5.17 – 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP, TSOP2, AND SOJ

CAPACITY—128K & 512K WORDS OF 8 OR 9 BITS,
LOGIC FEATURES—Both Synchronous and Asynchronous versions of the 128K part
PACKAGE—36 PIN DIP, TSOP2, or SOJ, 0.400" or 0.600",
— See Fig. 3.7.5–17 for specific package approvals and dimensions.
PIN ASSIGNMENT—Fig. 3.7.5–17

Release 7

3.7.5.18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5–18
These parts contain BURST addressing capability.

3.7.5.19 – 128K TO 2M BY 8/9 SSRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5–19
Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.5–20

3.7.5.20 – 32K BY 8 SRAM IN TSOP1

CAPACITY—32K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 8 mm X 11.8 mm, 0.55 mm PP
PIN ASSIGNMENTS—Fig. 3.7.5–21

3.7.5 Byte Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.5.1 – 64 BY 9 TTL SRAM IN SCC

CAPACITY—64 WORDS OF 9 BITS
PACKAGE—28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS—Fig. 3.7.5–1
This standard was developed by Committee 42.1.

3.7.5.2 – 1K & 2K BY 8 TTL SRAM IN DIP

CAPACITY—1K, 2K WORDS OF 8 BITS
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–2

3.7.5.3 – 2K & 4K BY 8 TTL SRAM IN RCC

CAPACITY—2K, 4K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–3
These parts are CC equivalents of 24 Pin DIP devices.

3.7.5.4 – 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,

CAPACITY—2K, 4K, 8K, 16K, & 32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
—28 PIN DIP, 0.3" WIDE OPTIONAL FOR 8K & 32K DEVICES
PIN ASSIGNMENT—Fig. 3.7.5–4

3.7.5.5 – .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

CAPACITY—.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–5

3.7.5.6 – 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP–2,

CAPACITY—32K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.3", 0.4" WIDE OR NOT DEFINED
—32 PIN TSOP–2 (see Fig. 3.7.5–6 for package approvals)
PIN ASSIGNMENT—Fig. 3.7.5–6

3.7.5.7 – 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,

CAPACITY—64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–7

3.7.5.8 – 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
—OPTIONAL 32 PIN DIP & SOJ, 0.3" WIDE FOR 32K DEVICE
PIN ASSIGNMENT—Fig. 3.7.5–8

3.7.5.9 – 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—32K, 128K, 512K, 2M WORDS OF 8 BIT AND 512K, 2M WORDS OF 9 BITS
LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–9

SSRAM Boundry Scan Order					
X9 Part					
Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		22	NC, $\overline{SA}$	3B
2	SA	6T		23	NC, SE2 SA#	2B
3	SA	4P		24	SA	3A
4	SA	4T		25	SA	3C
5	SA	6R		26	SA	2C
6	SA	5T		27	SA	2A
7	NC, ZZ	7T				
				28	DQ	2G
8	DQ	6L				
				29	DQ	1H
9	DQ	7K				
				30	ZQ, NC	4D
10	$\overline{K}$, NC	4L		31	$\overline{SS}$	4E
11	K	4K		32	$\overline{C}$, NC	4G
12	$\overline{G}$	4F		33	C, NC	4H
				34	$\overline{SW}$	4M
13	DQ	6H				
14	DQ	7G		35	DQ	2K
				36	DQ	1L
15	DQ, NC	7E				
16	SA	6A				
17	SA	6C		37	SA	3T
18	SA	5C		38	SA	2R
18	SA	5A		39	SA	4N
20	NC, $\overline{SE2}$ SA◇	6B		40	SA	2T
21	NC, SA*	5B		41	M1, NC	3R

FIGURE 3.7.5-20

128K TO 2M BY 8/9 SSRAM IN BGA BOUNDRY SCAN ORDER

Release 4

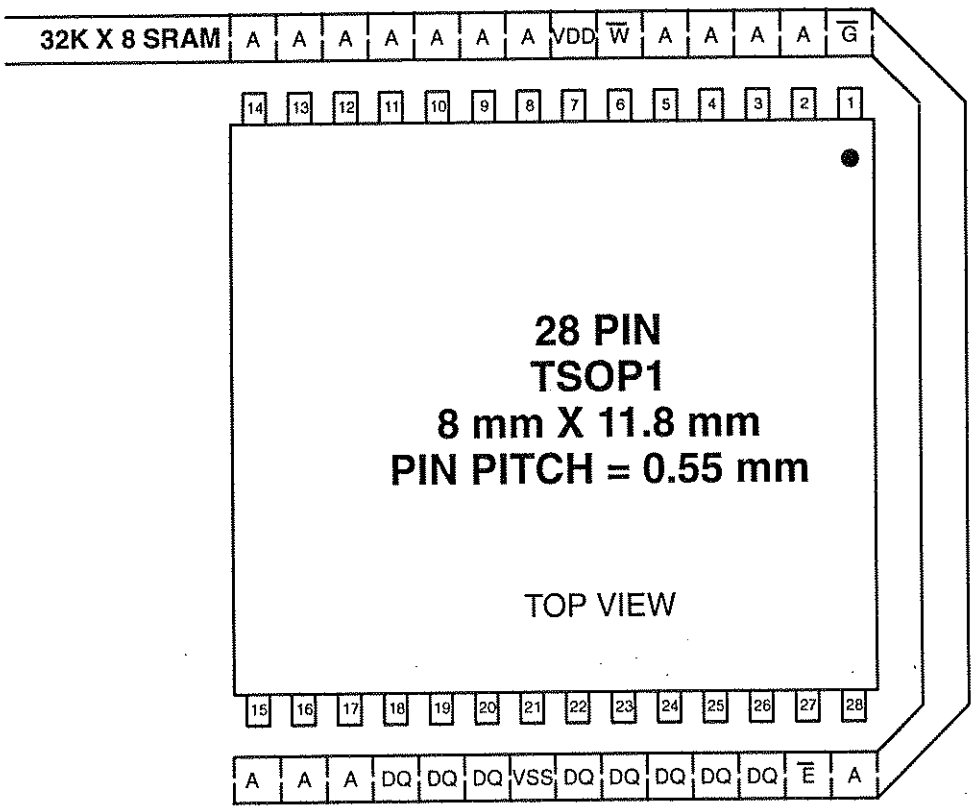


FIGURE 3.7.5–21
32K BY 8 SRAM IN TSOP–1

Synchronous SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X18	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA~	NC	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	VSS	NC, ZQ	VSS	DQa, NC	NC
E	NC	DQb	VSS	$\overline{SS}$, $\overline{SE}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{G}$, $\overline{SG}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{SBb}$	NC, $\overline{C}$	VSS	NC	DQa
H	DQb	NC	VSS	NC, C	VSS	DQa	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQb	VSS	CK, K	VSS	NC	DQa
L	DQb	NC	VSS	$\overline{CK}$, $\overline{K}$, NC	$\overline{SBa}$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{SW}$	VSS	NC	VDDQ
N	DQb	NC	VSS	SA	VSS	DQa	NC
P	NC	DQb, NC	VSS	SA	VSS	NC	DQa
R	NC	SA	M1, NC	VDD	M2, NC	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (64K X 18)	Basic SA	14 mm X 22 mm
2M (128K X 18)	~	14 mm X 22 mm
4M (256K X 18)	~, *	14 mm X 22 mm
8M (512K X 18)	~, *, ◇	TBD
16 M (1M X 18)	~, *. ◇, #	TBD

Mode Truth Table	M1	M2
Single Clock, Register Flow Through	VSS	VSS
Single Clock, Register–Register	VSS	VDD
Single Clock, Register–Latch	VDD	VSS
Dual Clock	VDD	VDD

FIGURE 3.7.7–10
64K TO 1M BY 16 & 18 SSRAM IN BGA

Release 5

SSRAM Boundry Scan Order						
X18 Part						
Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		26	NC, SA~	3B
2	SA			27	NC, SE2 SA#	2B
3	SA	6T		28	SA	3A
		4P		29	SA	3C
4	SA	6R		30	SA	2C
5	SA	5T		31	SA	2A
6	NC, ZZ	7T				
				32	DQB	1D
7	DQa	7P		33	DQb	2E
8	DQa	6N				
				34	DQb	2G
9	DQa	6L				
				35	DQb	1H
10	DQa	7K		36	$\overline{SBb}$	3G
11	$\overline{SBa}$	5L		37	ZQ, NC	4D
12	$\overline{K}$, NC	4L		38	$\overline{SS}$	4E
13	K	4K		39	$\overline{C}$, NC	4G
14	G	4F		40	C, NC	4H
				41	$\overline{SW}$	4M
15	DQa	6H				
16	DQa	7G		42	DQb	2K
				43	DQb	1L
17	DQa	6F				
18	DQa	7E		44	DQb	2M
				45	DQb	1N
19	DQa, NC	6D				
20	SA	6A		46	DQb, NC	2P
21	SA	6C		47	SA	3T
22	SA	5C		48	SA	2R
23	SA	5A		49	SA	4N
24	NC, $\overline{SE2}$ SA◇	6B		50	SA	2T
25	NC, SA*	5B		51	M1, NC	3R

FIGURE 3.7.7–11
64K TO 1M BY 16 & 18 SSRAM IN BGA BOUNDRY SCAN ORDER

Release 5c7

3.7.8.1 – 32K TO 128K BY 32 & 36 BURST SSRAM IN TQFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE—100 PIN TQFP, 20 mm X 14 mm WITH 0.65 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–1
These parts combine the features of Synchronous SRAM with BURST addressing capability. This standard modifies the one published previously in Release 5 ab adding new functions and deleting some that were not used.

3.7.8.2 – 32K TO 128K BY 32 & 36 SRAM AND SSRAM FAMILIES IN 100 TQFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
LOGIC FEATURES —There are two version of this part available:
—SYNCHRONOUS WITH ADDRESS LATCH OR ASYNCHRONOUS
—UPPER BYTE AND LOWER BYTE SELECTABLE
—COMMON DATA I/O
PACKAGE—100 PIN TQFP, 20 mm X 14 mm 0.65 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–2

3.7.8.3 – 32K TO 512K BY 32 & 36 BURST SRAM IN BGA

CAPACITY—32K, 64K,128K, 256K, OR 512K WORDS OF 32 OR 36 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–3
These parts contain BURST addressing capability.

3.7.8.4 – 32K TO 512K BY 16 & 18 SSRAM IN BGA

CAPACITY—32K, 64K, 128K, 256K, OR 512K WORDS OF 32 OR 36 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–4
.Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.8–5

3.7.8.5 – 16K TO 64K BY 64 & 72 BURST SSRAM IN QFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE—120 PIN TQFP, 20 mm X 14 mm WITH 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–6
These parts combine the features of Synchronous SRAM with BURST addressing capability.

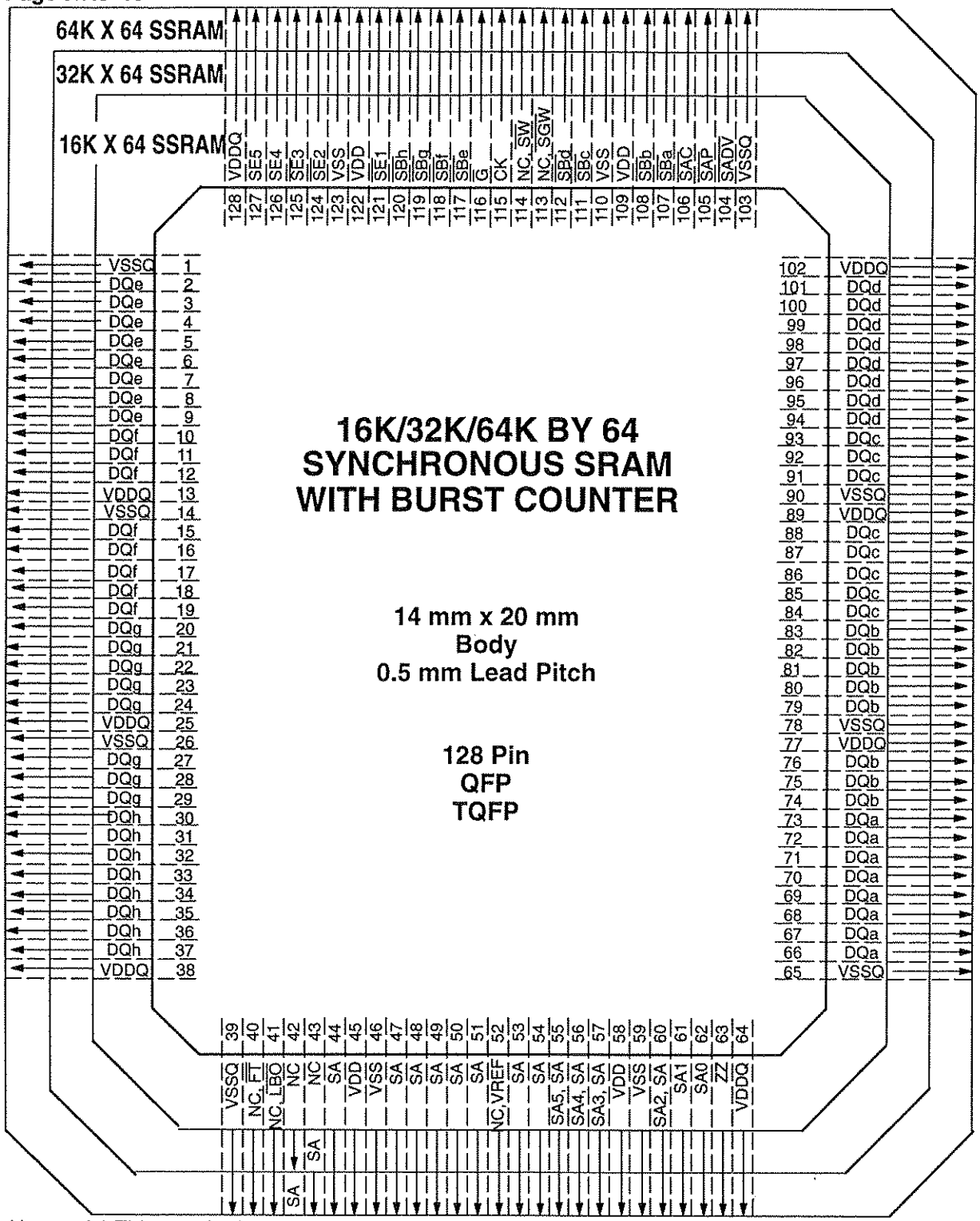
3.7.8.6 – 16K TO 256K BY 64 & 72 BURST SSRAM IN BGA

CAPACITY—16K, 32K, 64K, 128K, OR 256K WORDS OF 64 OR 72 BITS,
PACKAGE—11 X 19 BALL BGA 20 mm X 25 mm OR UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–7
These parts combine the features of Synchronous SRAM with BURST addressing capability.

SSRAM Boundry Scan Order					
X36 Part					
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2, NC	5R	36	NC, $\overline{SA}$	3B
			37	NC, SE2 SA#	2B
2	SA	4P	38	SA	3A
3	SA	4T	39	SA	3C
4	SA	6R	40	SA	2C
5	SA	5T	41	SA	2A
6	NC, ZZ	7T	42	DQc,NC	2D
7	DQa, NC	6P	43	DQc	1D
8	DQa	7P	44	DQc	2E
9	DQa	6N	45	DQc	1E
10	DQa	7N	46	DQc	2F
11	DQa	6M	47	DQc	2G
12	DQa	6L	48	DQc	1G
13	DQa	7L	49	DQc	2H
14	DQa	6K	50	DQc	1H
15	DQa	7K	51	$\overline{SBc}$	3G
16	$\overline{SBa}$	5L	52	ZQ, NC	4D
17	$\overline{K}$, NC	4L	53	$\overline{SS}$	4E
18	K	4K	54	$\overline{C}$, NC	4G
19	$\overline{G}$	4F	55	C, NC	4H
20	$\overline{SBb}$	5G	56	$\overline{SW}$	4M
21	DQb	7H	57	$\overline{SBd}$	3L
22	DQb	6H	58	DQd	1K
23	DQb	7G	59	DQd	2K
24	DQb	6G	60	DQd	1L
25	DQb	6F	61	DQd	2L
26	DQb	7E	62	DQd	2M
27	DQb	6E	63	DQd	1N
28	DQb	7D	64	DQd	2N
29	DQb, NC	6D	65	DQd	1P
30	SA	6A	66	DQd, NC	2P
31	SA	6C	67	SA	3T
32	SA	5C	68	SA	2R
33	SA	5A	69	SA	4N
34	NC, $\overline{SE2}$ SA◇	6B			
35	NC, SA*	5B	70	M1, NC	3R

FIGURE 3.7.8-5
32K TO 512K BY 32 & 36 SSRAM IN BGA BOUNDRY SCAN ORDER

Release 5



Notes: (1) This standard accommodates synchronous burst address fields ranging from 2 to 6 address b
(2) An 8-word (3 address bits) interleaved burst sequence is currently specified in commercial data sheets

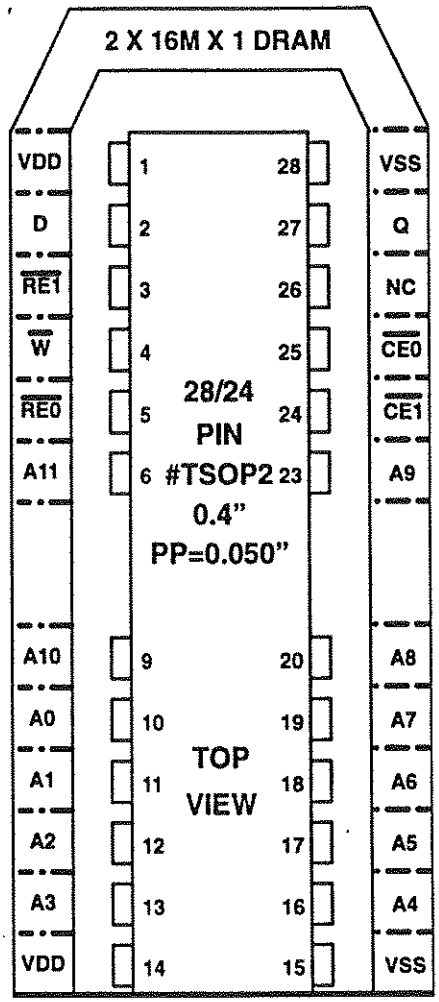
FIGURE 3.7.8–6
16K/32K/64K BY 64 SYNCHRONOUS SRAM WITH BURST COUNTER

Burst SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View											
X72	1	2	3	4	5	6	7	8	9	10	11
A	DQe	DQe	NC, SA#	SA	SA	$\overline{SS}$, $\overline{SE1}$	SA	SA	NC, SA$	DQd	DQd
B	DQe	DQe	NC, SA~	SA	SA	$\overline{G}$	SA	SA	NC, SA◇	DQd	DQd
C	DQe	DQe	NC, SE2	VDD, VDDQ	VDD, VDDQ	ND, $\overline{SGW}$	VDD, VDDQ	VDD, VDDQ	NC, $\overline{SE3}$	DQd	DQd
D	DQe	DQe	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{ADV}$	VSS, VSSQ	VDD	VDD, VDDQ	DQd	DQD
E	DQe, NC	DQf, NC	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{SAC}$	VSS, VSSQ	VDD	VDD, VDDQ	DQc, NC	DQd, NC
F	DQf	DQf	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{SAP}$	VSS, VSSQ	VDD	VDD, VDDQ	DQc	DQc
G	DQf	DQf	VDD, VDDQ	VDD	VSS, VSSQ	VSS, VSSQ	VSS, VSSQ	VDD	VDD, VDDQ	DQc	DQc
H	DQf	DQf	VDD, VDDQ	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	VDD, VDDQ	DQc	DQc
J	DQf	DQf	$\overline{SWe}$, $\overline{SBe}$	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	$\overline{SWd}$, $\overline{SBd}$	DQc	DQc
K	$\overline{SWf}$, $\overline{SBf}$	$\overline{SWg}$, $\overline{SBg}$	NC, VREF	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	NC, VREF	$\overline{SWb}$, $\overline{SBb}$	$\overline{SWc}$, $\overline{SBc}$
L	DQg	DQg	$\overline{SWh}$, $\overline{SBh}$	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	$\overline{SWa}$, $\overline{SBa}$	DQb	DQb
M	DQg	DQg	VDD, VDDQ	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	VDD, VDDQ	DQb	DQb
N	DQg	DQg	VDD, VDDQ	VDD	VSS, VSSQ	VSS, VSSQ	VSS, VSSQ	VDD	VDD, VDDQ	DQb	DQb
P	DQg	DQg	VDD, VDDQ	VDD	VSS, VSSQ	NC, $\overline{CK}$, K	VSS, VSSQ	VDD	VDD, VDDQ	DQb	DQb
R	DQg, NC	DQh, NC	VDD, VDDQ	VDD	VSS, VSSQ	CK, K	VSS, VSSQ	VDD	VDD, VDDQ	DQa, NC	DQb, NC
T	DQh	DQh	VDD, VDDQ	VDD	VSS, VSSQ	NC, $\overline{SW}$	VSS, VSSQ	VDD	VDD, VDDQ	DQa	DQa
U	DQh	DQh	$\overline{LBO}$, NC	VDD, VDDQ	VDD, VDDQ	SA1	VSS, VSSQ	VDD, VDDQ	NC, $\overline{FT}$	DQa	DQa
V	DQh	DQh	NC	SA	SA	SA0	SA	SA	NC	DQa	DQa
W	DQh	DQh	NC, ZQ	NC, TMS	NC, TDI	NC, TCK	NC, TDO	NC, TRST	NC, ZZ	DQa	DQa

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (16K X 64, 72)	Basic SA	21 mm X 25 mm
2M (32K X 64, 74)	~	21 mm X 25 mm
4M (64K X 64, 72)	~, *	21 mm X 25 mm
8M (128K X 64, 72)	~, *, ◇	TBD
16 M (256K X 64, 72)	~, *. ◇, #	TBD

FIGURE 3.7.8–7
16K TO 256K BY 64 & 72 BURST SRAM IN BGA

Release Release 7

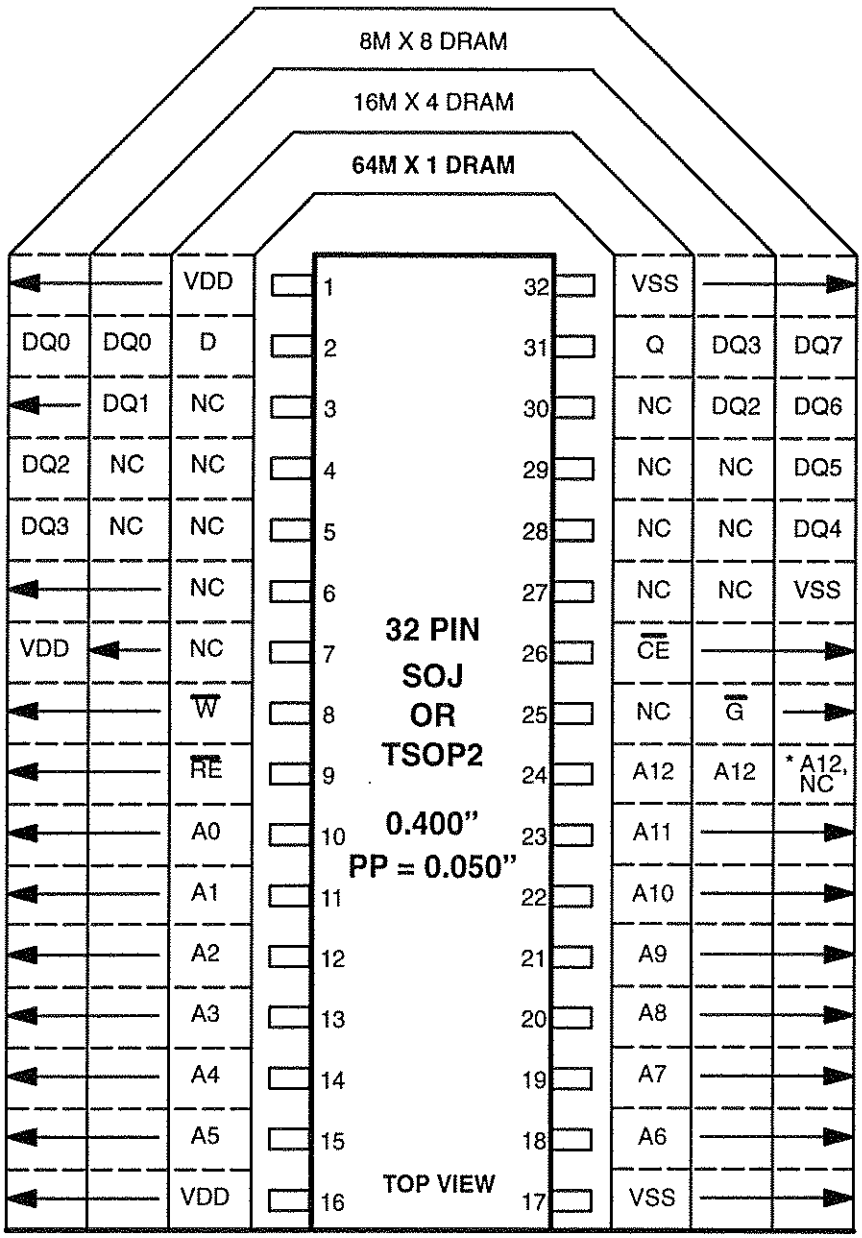


The JEDEC approved term for this package is PDSO–G

ROW, REFRESH, & COLUMN ADDRESS CONFIGURATION

DEVICE CONFIGURATION	2 X 16M X 1	2 X 16M X 1
REFRESH COUNT	2048 Refresh	4096 Refresh
ROW ADDRESS	A0 → A11	A0 → A11
REFRESH ADDRESS	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A11	A0 → A11

FIGURE 3.9.1–11
2 X 16M BY 1 DRAM IN TSOP2



* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4	16M X 4	8M X 8	8M X 8
ROW COUNT		4K Rows	8K Rows	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.1–12
64M BY 1 DRAM IN SOJ & TSOP2

Release 5r7

3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP

CAPACITY—16K, 64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—18 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2–1

3.9.2.2 – 16K BY 4 DRAM IN DIP

CAPACITY—16K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Separate DATA I/O
PACKAGE—20 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2–1
NOTE: At the time that this document was published, this standard was in the process of being rescinded by the Committee.

3.9.2.3 – 64K BY 4 DRAM IN RCC

CAPACITY—64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with Common DATA I/O
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.9.2–2

3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN DIP, Width: 0.3" for 256K & 1M,
PIN ASSIGNMENT—Fig. 3.9.2–3

3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 256K
—26/20 PIN SOJ or TSOP2: 0.3" or 0.35" by 0.675" for 1M
—26/24 PIN SOJ OR TSOP–2: 0.3" for 4M
—28/24 PIN SOJ: 0.4" by 0.725 for 4M
PIN ASSIGNMENT—Fig. 3.9.2–4

3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP

CAPACITY—64K, 256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR 64K, 256K, & 1M PARTS
—24 PIN ZIP, 0.475" WIDE FOR 4M PART
PIN ASSIGNMENT—Fig. 3.9.2–5

3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with 4 CE clocks controlling the 4 data bits
PACKAGE—26/24 PIN SOJ, Width: 0.3"
—26/24 PIN TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–6

3.9.2.8 – 256K BY 4 DRAM IN TSOP1

CAPACITY—256K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1, 14.4 mm x 6.0 mm, 0.5 mm LEAD PITCH
PIN ASSIGNMENT—Fig. 3.9.2–7

Release 4

3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.2–8

3.9.2.10 – 256K TO 4M BY 4 NON–MUX DRAM FAMILY IN SOJ

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Non–Multiplexed Address
PACKAGE—28, 32, OR 34 PIN SOJ, WIDTH Not yet defined
PIN ASSIGNMENT—Fig. 3.9.2–9

3.9.2.11 – 4M BY 4 DRAM WITH 1 $\overline{CE}$ AND 4 $\overline{CE}$ IN TSOP2

CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—There are two versions of this part, one with 1 $\overline{CE}$ and one with 4 $\overline{CE}$ controlling each of the data bits
PACKAGE—28/24 PIN TSOP2, 0.4" WIDE FOR THE 1 $\overline{CE}$ PART
— 28 PIN TSOP2, 0.4" WIDE FOR THE 4 $\overline{CE}$ PART
PIN ASSIGNMENT—Fig. 3.9.2–10

3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
This part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.
PACKAGE—34 PIN SOJ, WIDTH: 0.5"
—34PIN TSOP2, WIDTH: 0.5", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–11
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP.
PIN ASSIGNMENT—Fig. 3.9.1–12

3.9.2.13 – 1M, 2M, & 4M BY 2 DRAM IN SOJ & TSOP2

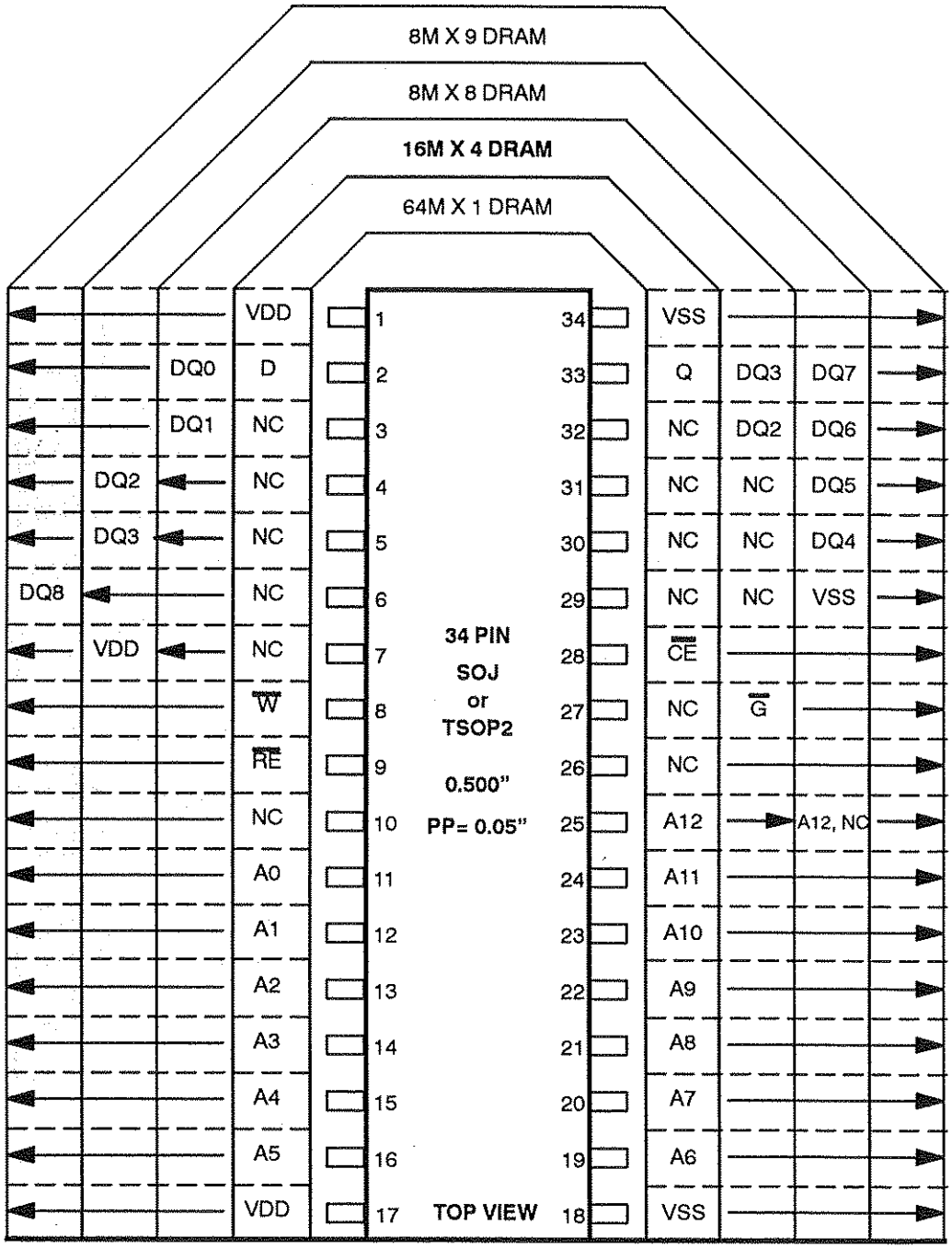
CAPACITY—1M, 2M, & 4M WORDS OF 2 BITS
LOGIC FEATURES—Multiplexed Address and a separate $\overline{CE}$ control for each data bit.
PACKAGE—26/20, 26/24, & 28/24 PIN SOJ or TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–12

3.9.2.14 – 16M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ OR TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—The part, has 4 $\overline{CE}$, one controlling each of the data bits.
PACKAGE— 34 PIN TSOP2, 12.7 mm WIDE, PP = 1.27 mm
— 34 PIN SOJ, 12.7 mm WIDE, PP = 1.27 mm
PIN ASSIGNMENT—Fig. 3.9.2–14
PACKAGE—32 PIN SOJ, 10.16 mm Wide
—32 PIN TSOP2, 10.16 mm Wide, 1.27 mm PP
PIN ASSIGNMENT—Fig. 3.9.2–14

3.9.2.15 – 64M X 4 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 64M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.2–15
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.



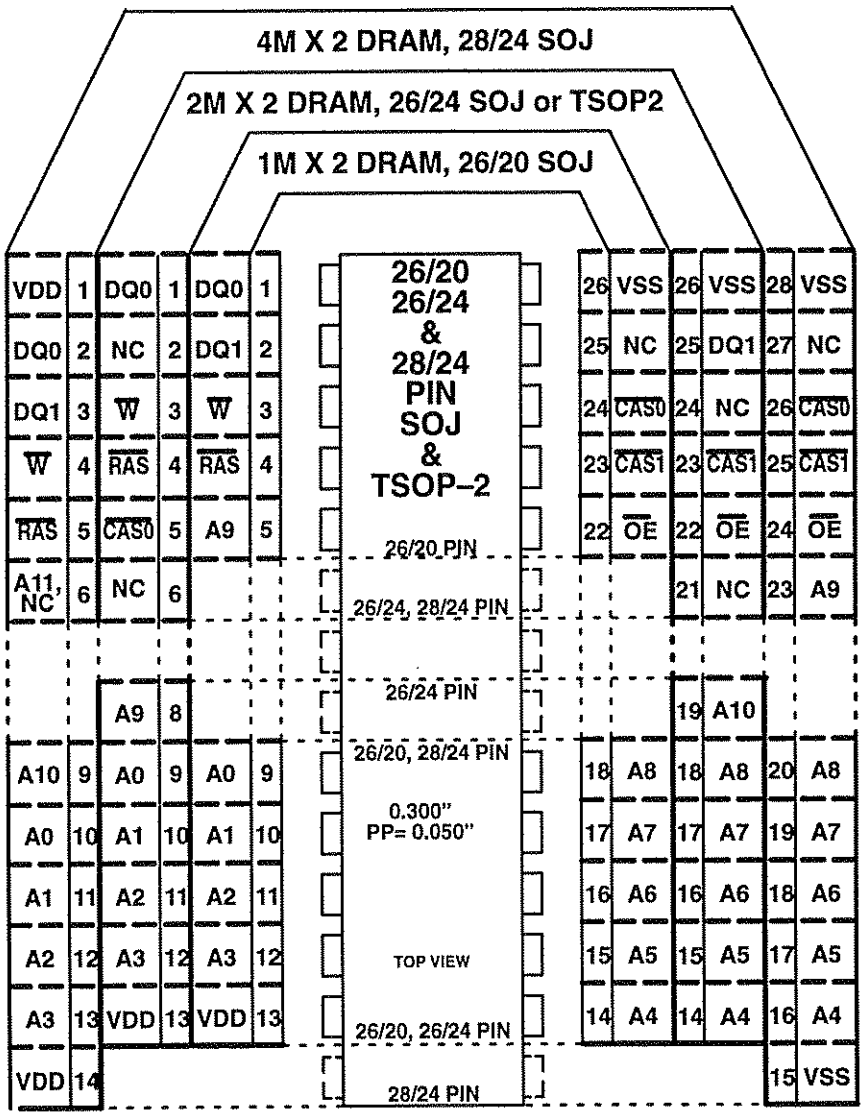
ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

▌This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.2-11
16M BY 4 DRAM IN SOJ & TSOP2

Release 4 a

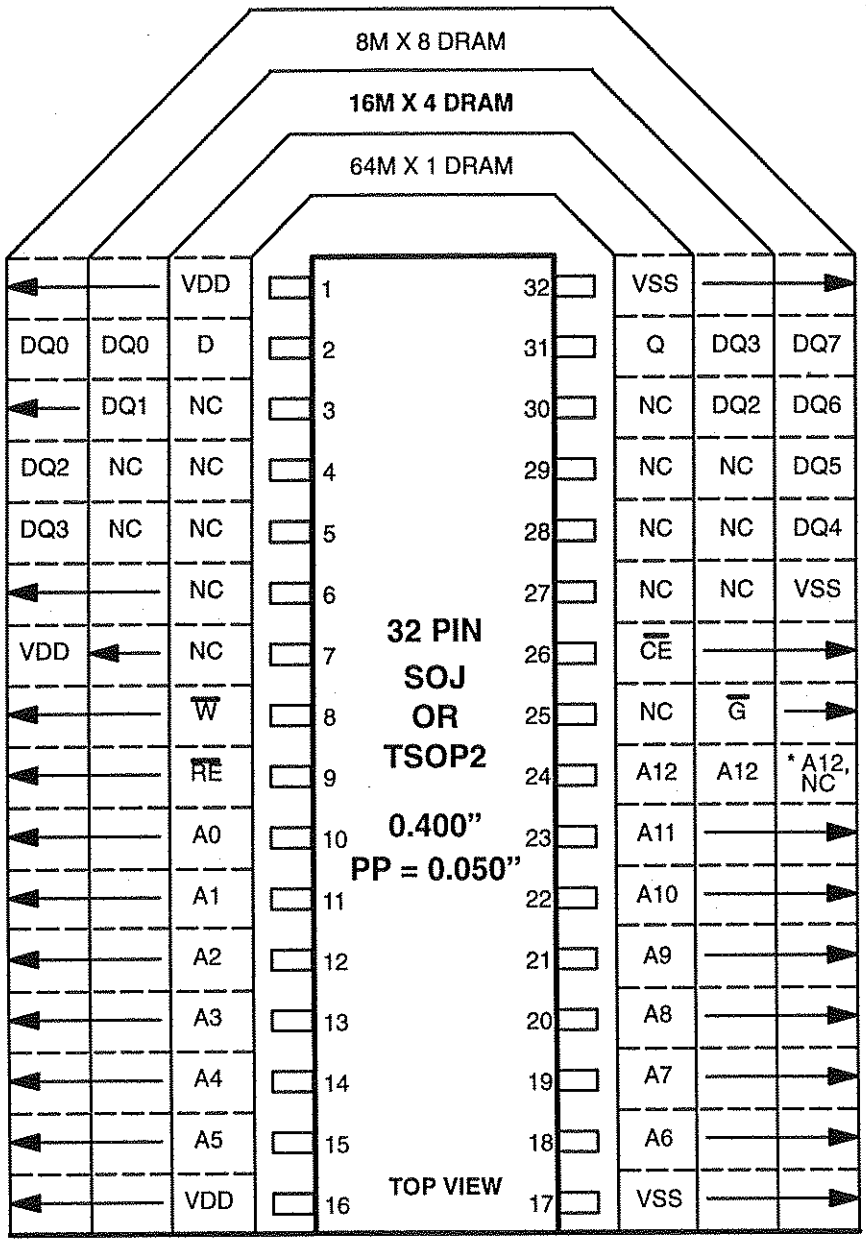


ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	1M X 2	2M X 2	4M X 2	4M X 2
ROW COUNT	1K Rows	1K Rows	2K Rows	4K Rows
ROW ADDRESSES	A0 → A9	A0 → A10	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A9	AO → A9	A0 → A10	A0 → A9

FIGURE 3.9.2–12
1M TO 4M BY 2 DRAM WITH 2 CAS IN SOJ & TSOP2

Release 4r7

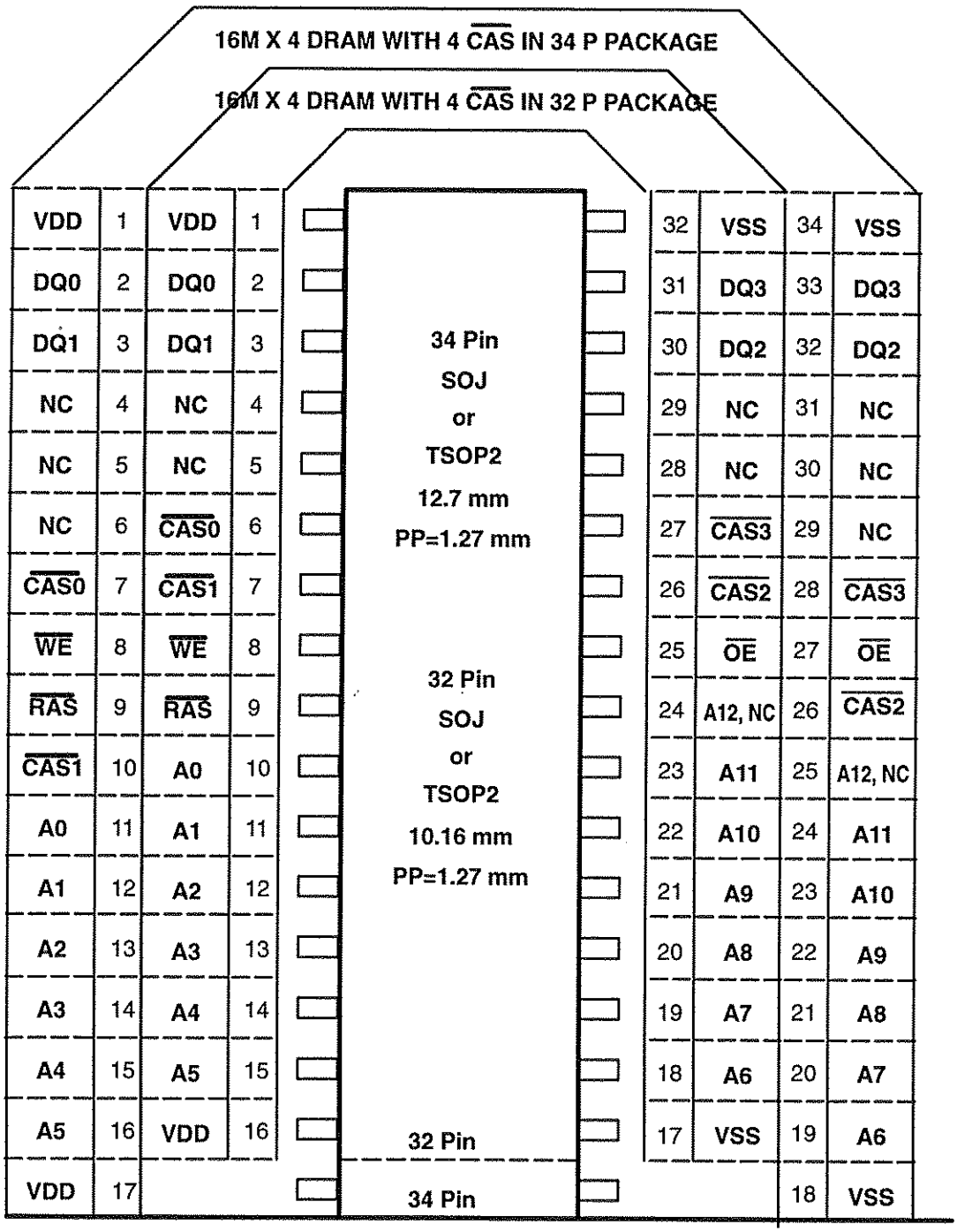


* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4	16M X 4	8M X 8	8M X 8
ROW COUNT		4K Rows	8K Rows	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.2–13
16M BY 4 DRAM IN SOJ & TSOP2



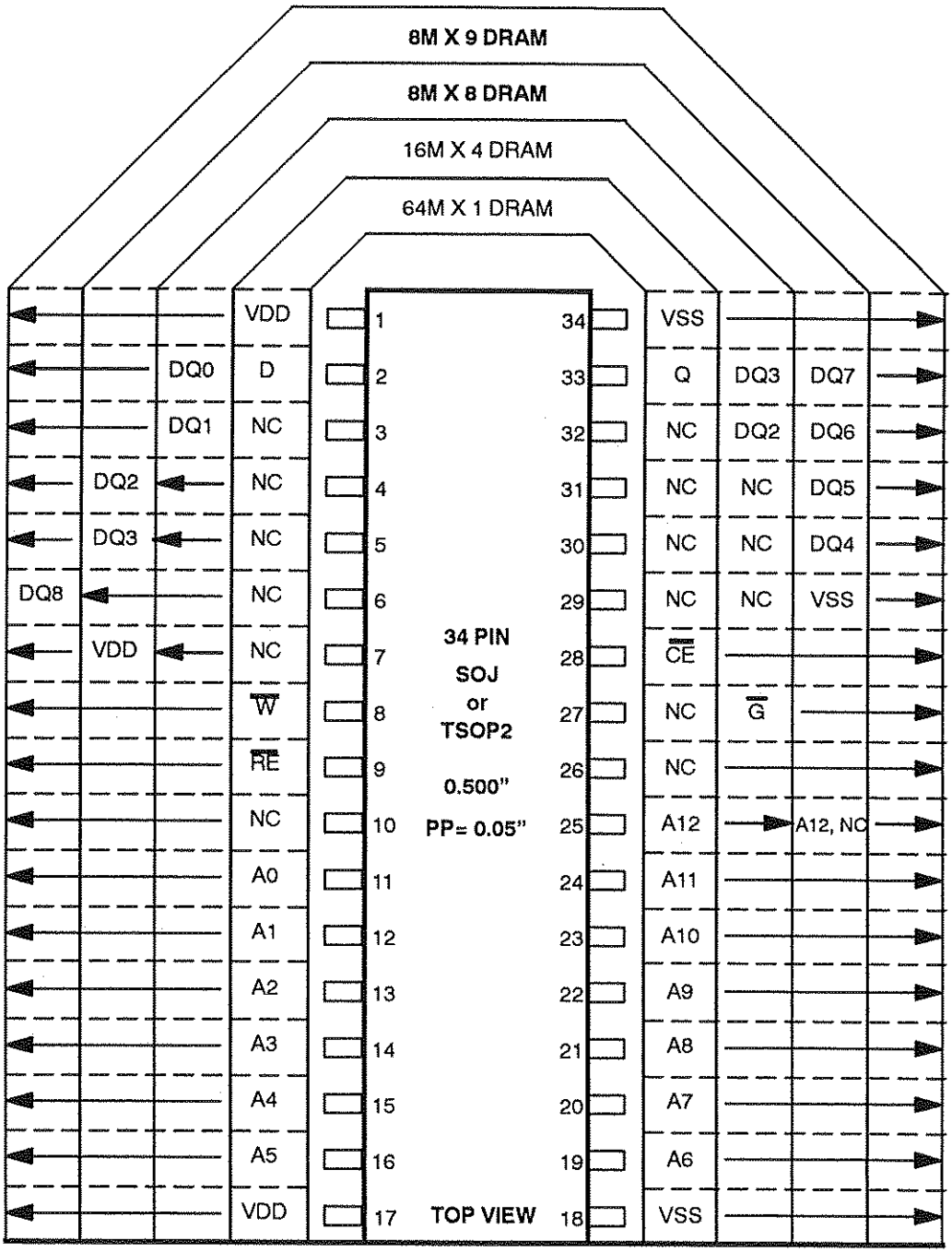
ADDRESS CONFIGURATIONS

ROW COUNT	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A11	A0 ⇒ 12
COLUMN ADDRESSES	A0 ⇒ A11	A0 ⇒ 10

*NOTE: The JESD30 approved term for the TSOP2 package is PDSO–G, for the SOJ is PDSO–J

FIGURE 3.9.2–14
16M BY 4 DRAM WITH 4 CAS IN SOJ & TSOP2

Release 6r7



ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

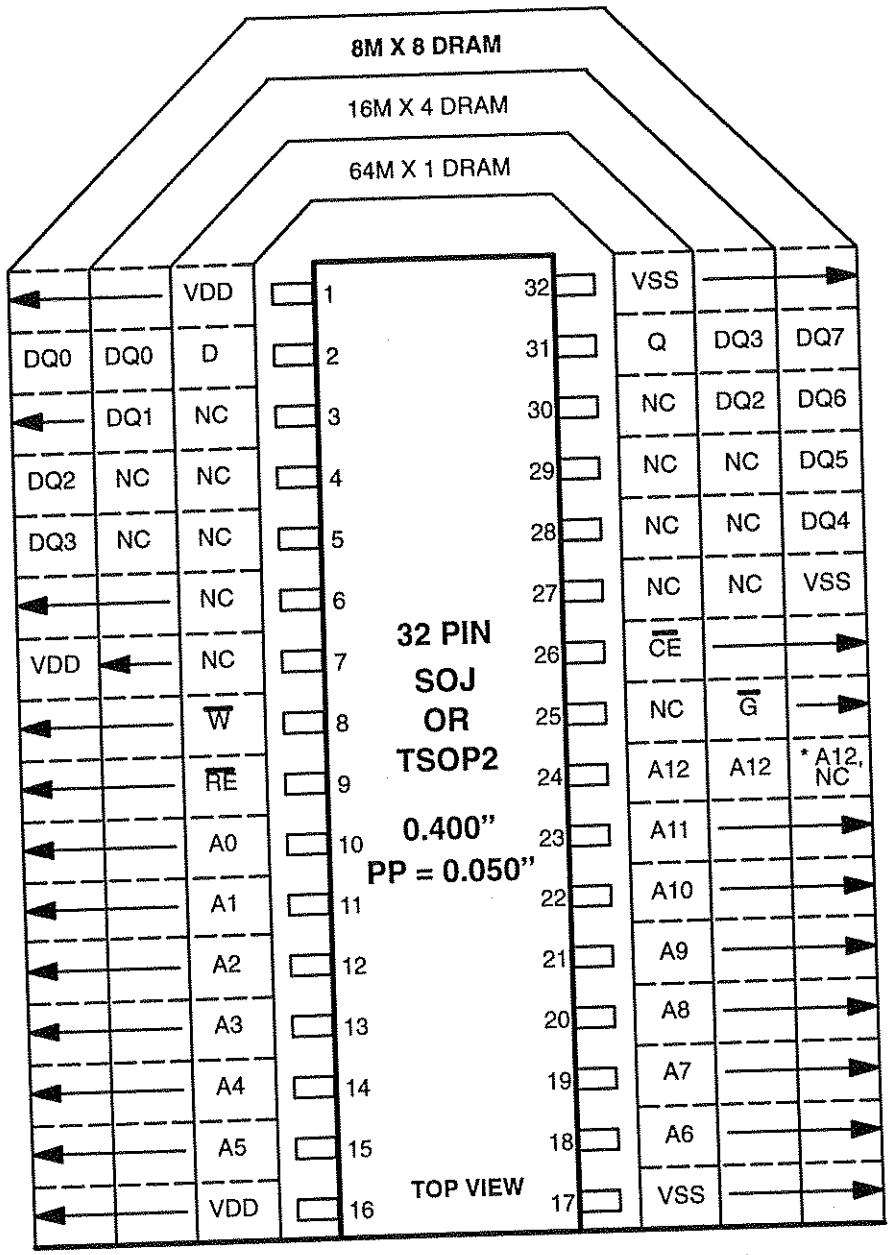
DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.3-7

8M BY 8 & 9 DRAM IN SOJ & TSOP2

Release 4 a



* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4 4K Rows	16M X 4 8K Rows	8M X 8 4K Rows	8M X 8 8K Rows
ROW COUNT					
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.3–8

8M BY 8 DRAM IN SOJ & TSOP2

3.9.4.1 – 64K BY 16 DRAM WITH 2 $\overline{W}$ IN SOJ & TSOP2

CAPACITY—64K WORDS OF 16 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—40 PIN SOJ, 0.400" WIDE
—44/40 PIN TSOP2, 0.400" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–1 (SOJ)
—Fig. 3.9.4–6 (TSOP2)

3.9.4.2 – 256K & 1M BY 16 & 18 WITH 2 $\overline{CE}$ OR 2 $\overline{W}$ DRAM IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 16 & 18 BITS,
The standard for the 2 $\overline{W}$ versions of the 1M part has been rescinded and removed from Figs. 3.9.4–4 & 3.9.4–5 in Release 5.
LOGIC FEATURES—MULTIPLEXED ADDRESS
—There are two versions of these parts, one with 2 $\overline{W}$ and the other with 2 $\overline{CE}$.
—The two clocks control the LOWER BYTE and UPPER BYTE data bits.
—The 1M part allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—256K in 40 PIN SOJ, 0.400" WIDE
—256K in 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
—1M IN 42 PIN SOJ, 0.400" WIDE
—1M in 50/44 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–2 (256K SOJ)
—Fig. 3.9.4–3 (256K TSOP2)
—Fig. 3.9.4–4 (1M SOJ)
—Fig. 3.9.4–5 (1M TSOP2)

3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—This part contains multiple logic functions that are similar to those used in MPDRAMS and that are keyed for VIDEO memory applications. All devices meeting this standard must contain all functions which must be implemented as defined in the TRUTH TABLE.
PACKAGE—40 PIN DIP, 0.400" WIDE, 0.100" PIN PITCH
—40 PIN SOJ, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–7A
FUNCTION TRUTH TABLE—Fig. 3.9.4–7B

3.9.4.4 – 2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP2

CAPACITY—2M & 4M WORDS OF 16 or 4M WORDS OF18 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts utilizes 4K or 8K refresh cycles
PACKAGE—50 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH, X16 parts only
PACKAGE—54 PIN TSOP2, 0.500" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–8

3.9.4.5 – 128K & 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, OR ZIP

CAPACITY—128K OR 256K WORDS OF 16 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts have BURST data out capability
PACKAGE—40 PIN SOJ, 10.16 mm WIDE, 1.27 mm PIN PITCH
PACKAGE—44/40 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH
PACKAGE—40 PIN ZIP, 1.27 mm PIN PITCH (256K only)
PIN ASSIGNMENT—SOJ, Fig. 3.9.4–9
PIN ASSIGNMENT—TSOP2, Fig. 3.9.4–10
PIN ASSIGNMENT—ZIP, Fig. 3.9.4–11, (256K ONLY)

Release 7

3.9.4.6 – 16M X 16 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 16M WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.4–12
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.7 – 128K AND 256K BY 32 DRAM WITH 4 $\overline{CE}$ IN SSOP

CAPACITY—128K OR 256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—The part, has 4 $\overline{CE}$, one controlling each group of 8 data bits.
PACKAGE— 64 PIN SSOP, 0.525" WIDE, PP = 0.8 mm
PIN ASSIGNMENT—Fig. 3.9.4–13

3.9.4.8 – 512K & 2M BY 32 & 36 DRAM WITH 4 $\overline{CE}$ IN SOJ & TSOP2

CAPACITY—512K, 2M WORDS OF 32 & 36 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—The part, has 4 $\overline{CE}$, one controlling each group of 8 or 9 data bits.
—The standard allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—70 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PP
—70 PIN TSOP2, 10.16 mm WIDE, 0.65 mm PP, 512K only.
—70 PIN SOJ, 10.16 mm WIDE, 0.8 mm PP
PIN ASSIGNMENT—Fig. 3.9.4–14

3.9.4.9 – 8M X 32 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 8M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.4–15
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.10 – 2M X 32 DRAM IN TSOP2

CAPACITY— 8M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—86 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.9.4–16

MANDATORY TRUTH TABLE FOR 256K BY 16 DRAM with EXTENDED FUNCTIONS

Mnem.	Function	Valid at RE					Valid at CE
		CE	G	W	DSF(1)	*DSF2	DSF(1)
RW	READ/WRITE	1	1	1	0	0	0
BW	BLOCK WRITE	1	1	1	0	0	1
LMR	LOAD MASK REGISTER	1	1	1	1	0	0
LCR	LOAD COLOR REGISTER	1	1	1	1	0	1
RWM	WRITE, MASKED	1	1	0	0	0	0
BWM	BLOCK WRITE, MASKED	1	1	0	0	0	1
CBR	CBR REFRESH (1)	0	X	1	0	0	X
CBRN	CBR REFRESH (2)	0	X	1	1	0	X
FWT	FLASH WRITE	1	1	0	1	0	X

* IF DSF2 IS PRESENT

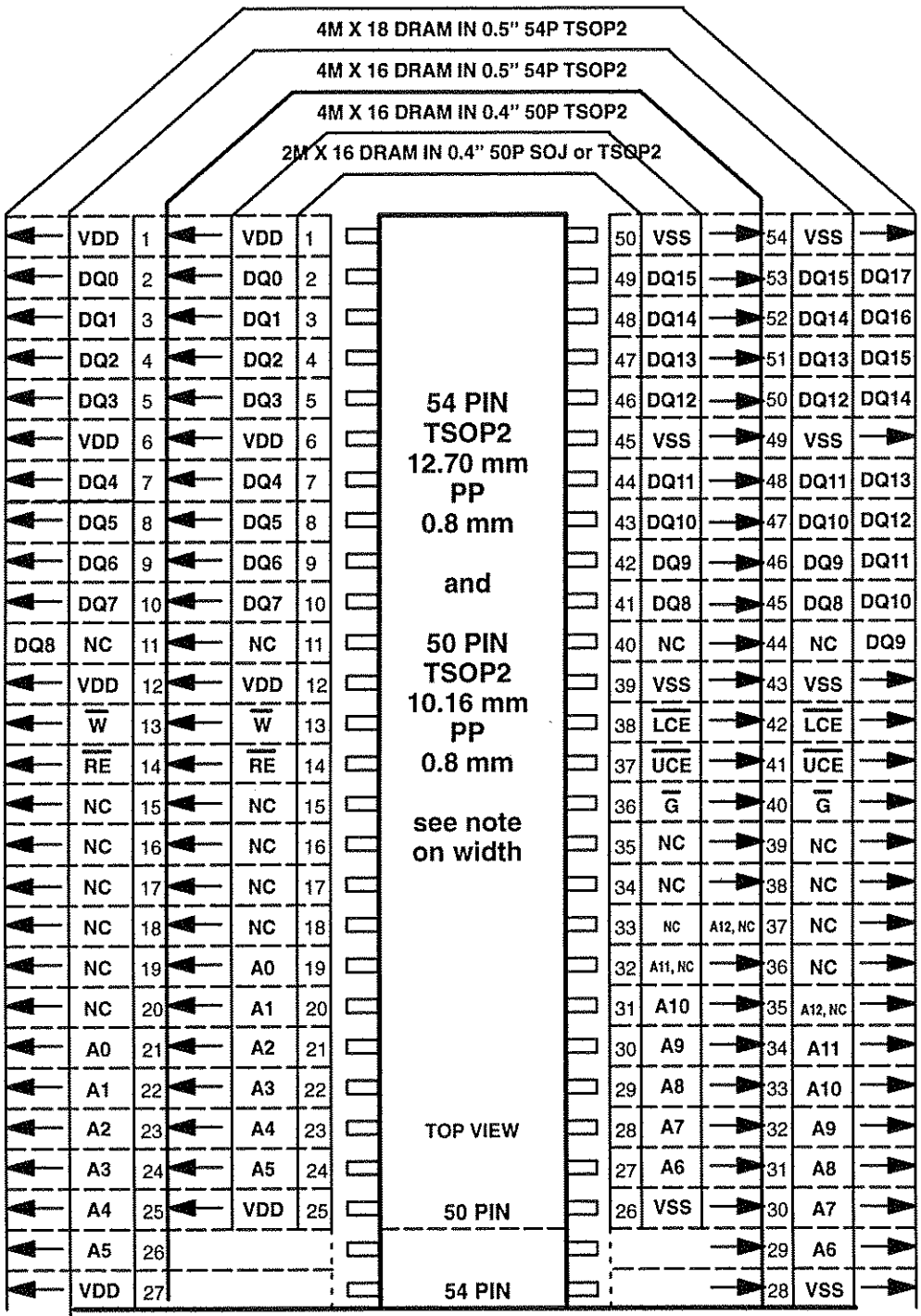
CBR(1) – All optional modes reset

CBR(2) – Any optional modes remain active

FIGURE 3.9.4–7 B

256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE

Release 4



54 P ADDRESS CONFIGURATION

	4K ROWS	8K ROWS
4M X 16/18		
ROW ADDRESSES	A0 → A11	A0 → A12
COLUMN ADDRESSES	A0 → A9	A0 → A8

50 P ADDRESS CONFIGURATION

	2K ROWS	4K ROWS	8K ROWS
2M X 16			
ROW ADDRESS	A0 ⇒ A10	A0 ⇒ A11	
COLUMN ADDRESS	A0 ⇒ A9	A0 ⇒ A8	
4M X 16	2K ROWS	4K ROWS	8K ROWS
ROW ADDRESS	A0 ⇒ A10	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESS	A0 ⇒ A10	A0 ⇒ A9	A0 ⇒ A8

* NOTES:
For 54P parts, Pin 35 is A12 for 8K rows and NC for 4K rows.

For 50P 4M parts, Pin 33 is A12 for 8K rows and NC for 4K rows. Pin 32 is NC for devices with 11 row & 11 columns and A11 for other Refresh/Address options..

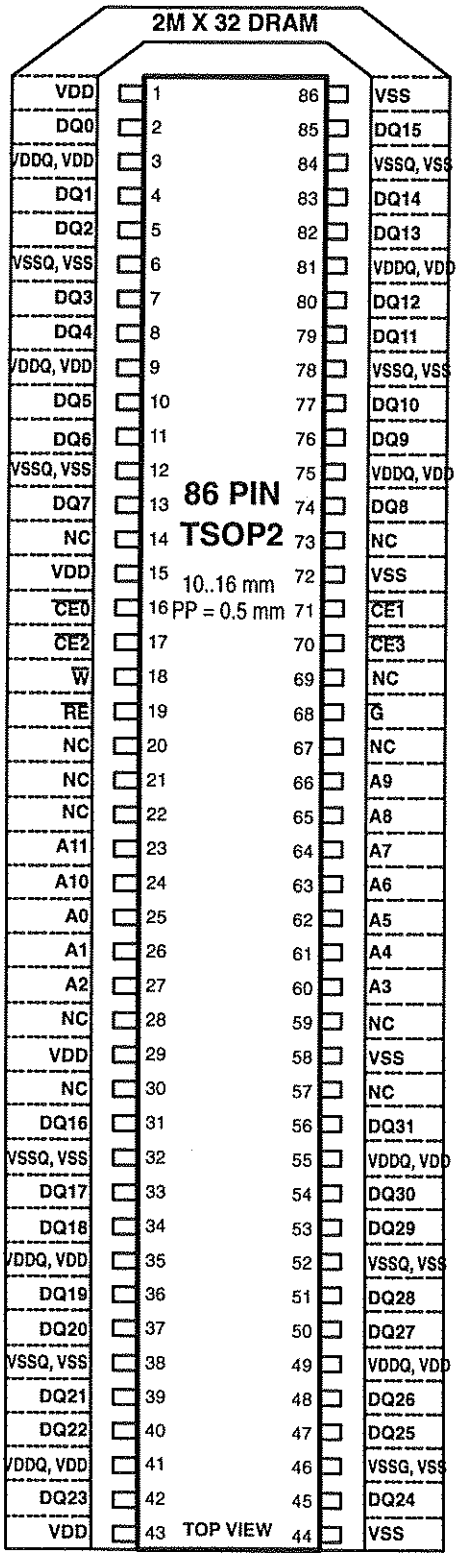
For 50P 2M parts, Pin 32 is A11 for devices with 4K rows and NC for devices with 2K rows.

The use of CBR for Refresh is strongly recommended for these devices.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

This standard recognizes that some early deliveries of the 54P parts may have to be in a 0.6"wide package

FIGURE 3.9.4–8
2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP–2



NOTES
1. The standard refresh period is 64 ms.
2. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally DC isolated from the VDD power supply pins.
3. The VSSQ designator is used when the ground reference pins

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	2M X 32
ROW COUNT	4K Rows
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.9.4–16
2M BY 32 DRAM IN TSOP2

3.9.5.1 – OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM

The definitions for serial data access, bit write, and refresh control included in Release 1 of this standard have been replaced by the more general definitions of Optional Operational Modes and Cycles beginning on page 3.9.5–11

3.9.5.2 – 1M DRAM BUILT IN TEST FUNCTION

An approved option for 1M DRAM (1M X 1 or 256K X 4) is the inclusion of a built in manufacturer defined "Test Mode". This mode is enabled using a dedicated pin which is optional NC or TF. When the optional mode is implemented, the manufacturer should include notes on his data sheet as follows:

(A) Normal operation requires the "TF" pin be connected to a VSS or logic low level or left unconnected.

(B) When the "TF" pin is connected to the manufacturer defined positive voltage, the internal test mode will be actuated. Contact the manufacturer for specific operational details of the Test Mode.

3.9.5.3 – ON–CHIP REFRESH CONTROL FOR X8 DRAM

This standard describes an optional feature that is applicable to the non–address multiplexed byte wide dynamic RAMs described in this publication. The standard establishes the clock timing sequence needed to invoke an on–chip refresh feature.

3.9.5.4 – $\overline{G}$ BEFORE $\overline{E}$ REFRESH

If G is low when E falls, a refresh cycle is executed. During this type of refresh cycle, an internal counter/register provides the refresh address and the external address is ignored

3.9.5.5 – DRAM SPECIAL TEST AND OPERATIONAL MODES

This standard defines a scheme for controlling a series of special operational modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control and exit from the special modes. In addition, it defines a basic test mode plus a series of other special test and operational modes. The details of this standard are given on pages 3.9.5–7 through 3.9.5–10.

3.9.5.6 – NON–MULTIPLEXED DRAM OPERATION

This standard defines multiple aspects of the address and clock relationships for DRAMs that have a non–multiplexed address architecture. It also defines the relationships between the address bits of multiplexed and non–multiplexed devices. The details of the standard are given on page 3.9.5–13

3.9.5.7 – DRAM EXTENDED DATA OUT

This standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part encorporating "EDO" must satisfy all of the following criteria to conform to the Standard. The details of the EDO standard are given on P 3.9.5–14

3.9.5.8 – 256M DRAM TEST MODE DATA AND ADDRESS COMPRESSION

This standard defines the algorithms for data and address compression when 256M DRAMs are operated in the built in special test mode. The detaild of the Compression standard are given on P 3.9.5–15

3.9.5.9 – PIPELINED NIBBLE MODE DEFINITION

This standard defines the output characteristics of the Pipelined Nibble Mode feature for DRAMs. Any part encorporating Pipelined Nibble Mode must satisfy all of the following criteria to conform to the Standard. The details of the standard are given on P 3.9.5–16

Release 7

Pipelined Nibble Mode Definition

Devices that operate in the Pipelined Nibble Mode are required to meet the following criteria to conform to this Standard.

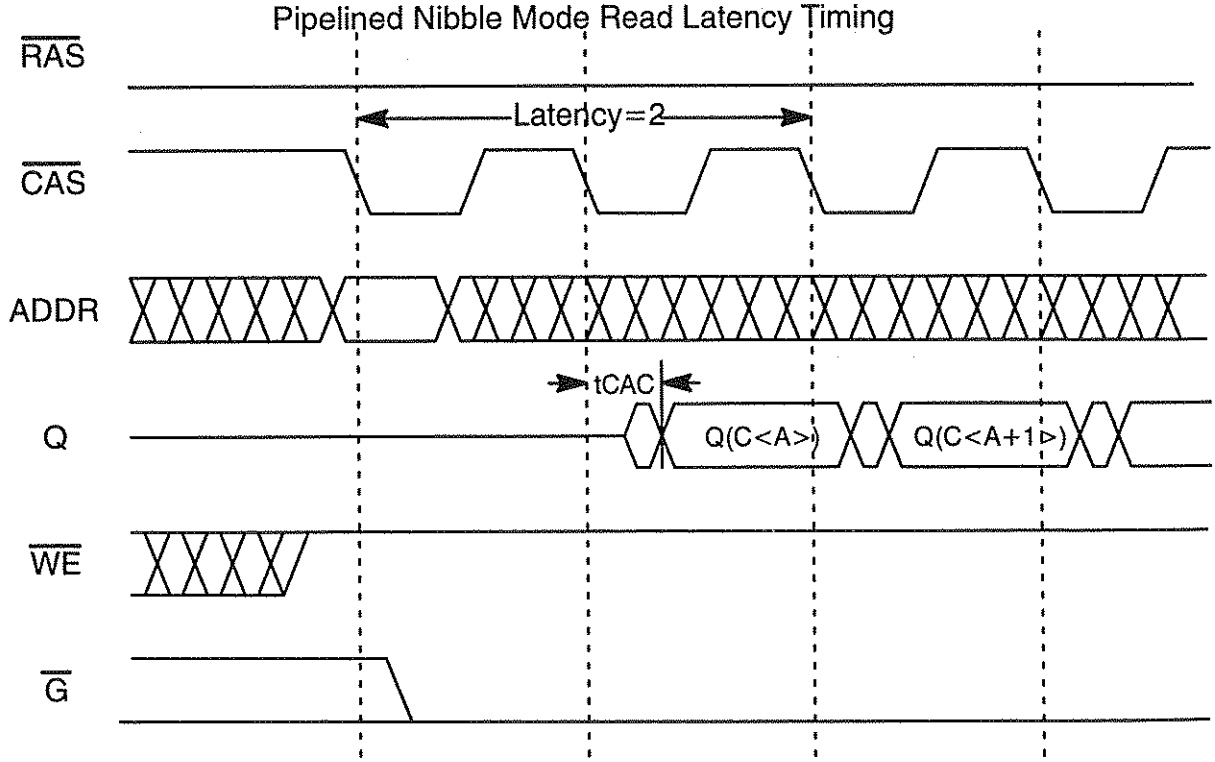
1. Burst Length shall be 4
2. Read Latency shall be 2 (refer to attached timing diagram for clarification)
3. Write Latency shall be 0
4. A WCBR, with the address keys shown below, is used to program the burst sequence. It is persistant until it is reprogrammed.

Address Sequence	A0	A1	A2	A3	A4	A5	A6	A7
Linear	0	0	0	0	0	1	0	0
Interleaved	1	0	0	0	0	1	0	0

5. $\overline{WE}$ transition during $\overline{CAS}$ precharge time causes burst to terminate
6. $\overline{WE}$ transition during $\overline{CAS}$ low, which remains through the $\overline{CAS}$ rising edge, causes burst to terminate.
7. $\overline{WE}$ pulse which is fully enclosed by a $\overline{CAS}$ low will be ignored and not cause a burst terminate.
8. Same output enable function as in EDO definition.
9. Read–modify–write cycle within $\overline{CAS}$ active cycle is not supported.
10. A Pipelined Nibble Mode device may not be reconfigured by the user to operate in the standard EDO (non–burst) mode.

FOR REFERENCE ONLY

Pipelined Nibble Mode Read Latency Timing



Release 7

256M DRAM Address Compression for Test–Mode

Devices		16K Refresh cycles (RA0–RA13)			8K Refresh cycles (RA0–RA12)		
		Normal Mode Input Addr.	Test Mode		Normal Mode Input Addr.	Test Mode	
			Input Address	Compress. Address		Input Address	Compress. Address
256M	64M X 4	RA0–RA13 CA0–CA11	RA0–RA13 CA0–CA7	CA8–11	RA0–RA12 CA0–CA12	RA0–RA12 CA0–CA8	CA9–12
	32M X 8	RA0–RA13 CA0–CA11	RA0–RA13 CA0–CA7	CA8–10	RA0–RA12 CA0–CA11	RA0–RA12 CA0–CA8	CA9–11
	16M X 16	RA0–RA13 CA0–CA9	RA0–RA13 CA0–CA7	CA8–9	RA0–RA12 CA0–CA10	RA0–RA12 CA0–CA8	CA9–10
	8M X 32	RA0–RA13 CA0–CA8	RA0–RA13 CA0–CA7	CA8	RA0–RA12 CA0–CA9	RA0–RA12 CA0–CA8	CA9

256M DRAM Data Space Compression for Test–Mode

When the memory device is operating in the compression mode, the data space is compressed with four DQn circuits supplying test data and receiving test results as defined in the following table.

Devices		Normal Mode Data Interface	Test Mode Data Interface	
			Active Data Bits	Data Bits Served
256M	64M X 4	DQ0–DQ3	DQ0	DQ0
			DQ1	DQ1
			DQ2	DQ2
			DQ3	DQ3
	32M X 8	DQ0–DQ7	DQ0	DQ0, DQ1
			DQ3	DQ2, DQ3
			DQ5	DQ4, DQ5
			DQ6	DQ6, DQ7
	16M X 16	DQ0–DQ15	DQ0	DQ0⇒DQ3
			DQ7	DQ4⇒DQ7
			DQ11	DQ8⇒DQ11
			DQ12	DQ12⇒DQ15
	8M X 32	DQ0–DQ31	DQ0	DQ0⇒DQ7
			DQ15	DQ8⇒DQ15
			DQ23	DQ16⇒DQ23
			DQ24	DQ24⇒DQ31

256M DRAM ADDRESS AND DATA SPACE COMPRESSION FOR TEST MODE

Release 7

3.10.3 Word Wide MPDRAM & GRAM

3.10.3.1 – 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—SERIAL and RAM data ports
There are two versions of these parts: One with 2 $\overline{W}$ and the other with 2 $\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with 2 W, 256K with 2 CE. .
PACKAGE—64 PIN SOG, 12 mm wide, 0.8 mm pin pitch
PIN ASSIGNMENTS—FIG. 3.10.3–1

3.10.3.2 – 128K & 256K BY 16 MPDRAM IN TSOP–2 WITH MULTIPLE CLOCKS

CAPACITY—128K AND 256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—SERIAL and RAM data ports
There are two versions of these parts: One with 2 $\overline{W}$ and the other with 2 $\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with 2 $\overline{W}$, 128K & 256K with 2 $\overline{CE}$. .
PACKAGE—70 PIN TSOP–2 10.16 mm wide (0.400"), 23.49 mm long. 0.65 mm pin pitch
NOTE: These parts have essentially the same pin rotation as the parts defined in Par. 3.10.3.1 with the exception of the addition of NC pins in the middle.
PIN ASSIGNMENTS—FIG. 3.10.3–2

3.10.3.3 – 256K BY 16 SGRAM IN TSOP–2

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—50 PIN TSOP–2, 10.16 mm wide (0.400"), 0.8 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–3
NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4–1 with the exception of the DSF function on P 33.

3.10.3.4 – 256K BY 32 SGRAM IN QFP or TQFP

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–4
NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4–4 with the exception of the DSF function on P 33.

3.10.3.5 – 256K BY 32 SGRAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—80 PIN TSOP2, 10.16 mm wide (0.400"), 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–5

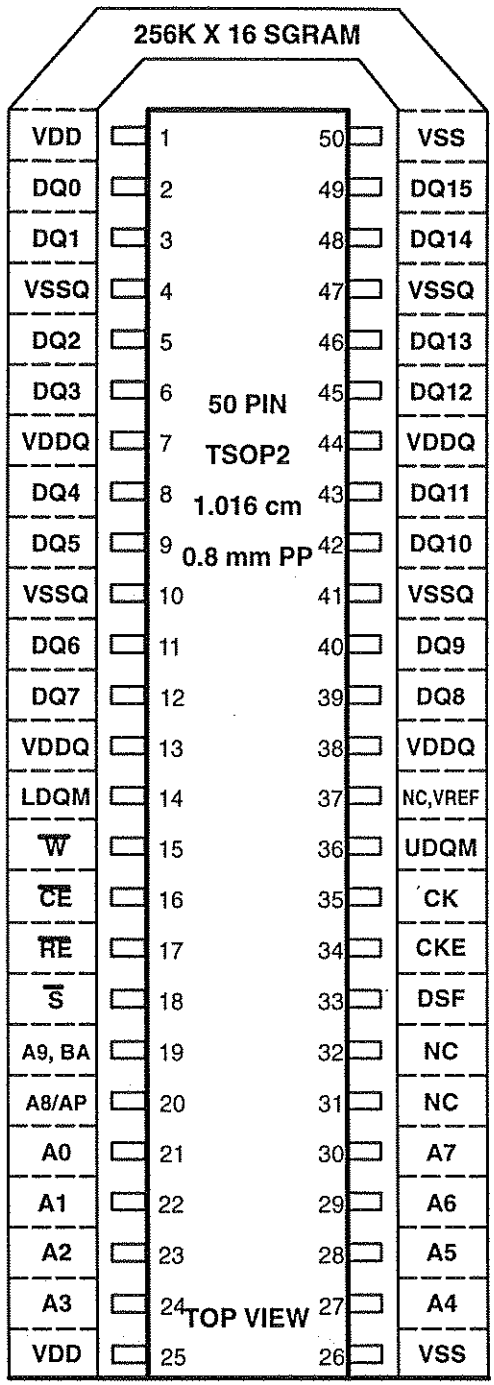
3.10.3.6 – 256K BY 32 SYNCHRONOUS MPDAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A multiple data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—120 PIN QFP or TQFP, 20 mm X 14 mm, 0.5 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–5

3.10.3.7 – 256K BY 32 SYNCHRONOUS MPDAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A multiple data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–6

XILINX EXHIBIT 1010
Page 126



This pinout is the same as the one for the 256K X 16 SDRAM shown in Fig. 3.11.4–1 except for the DSF function on pin 33.

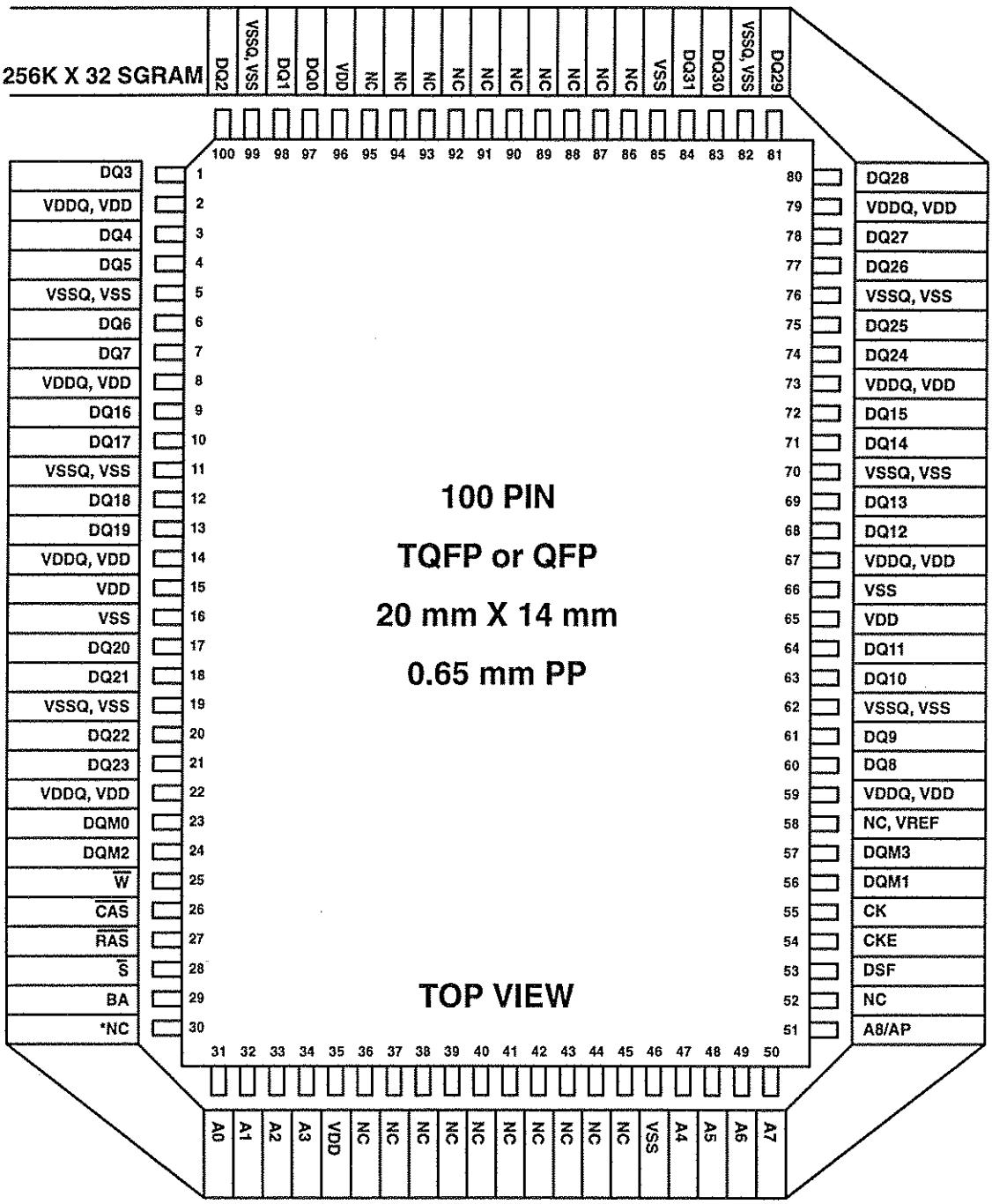
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

* NOTE—All VDDQ and VSSQ pins may be VDD and VSS at the option of the supplier.

ADDRESS STRUCTURE

RA	A0 ⇒ A8
CA	A0 ⇒ A7

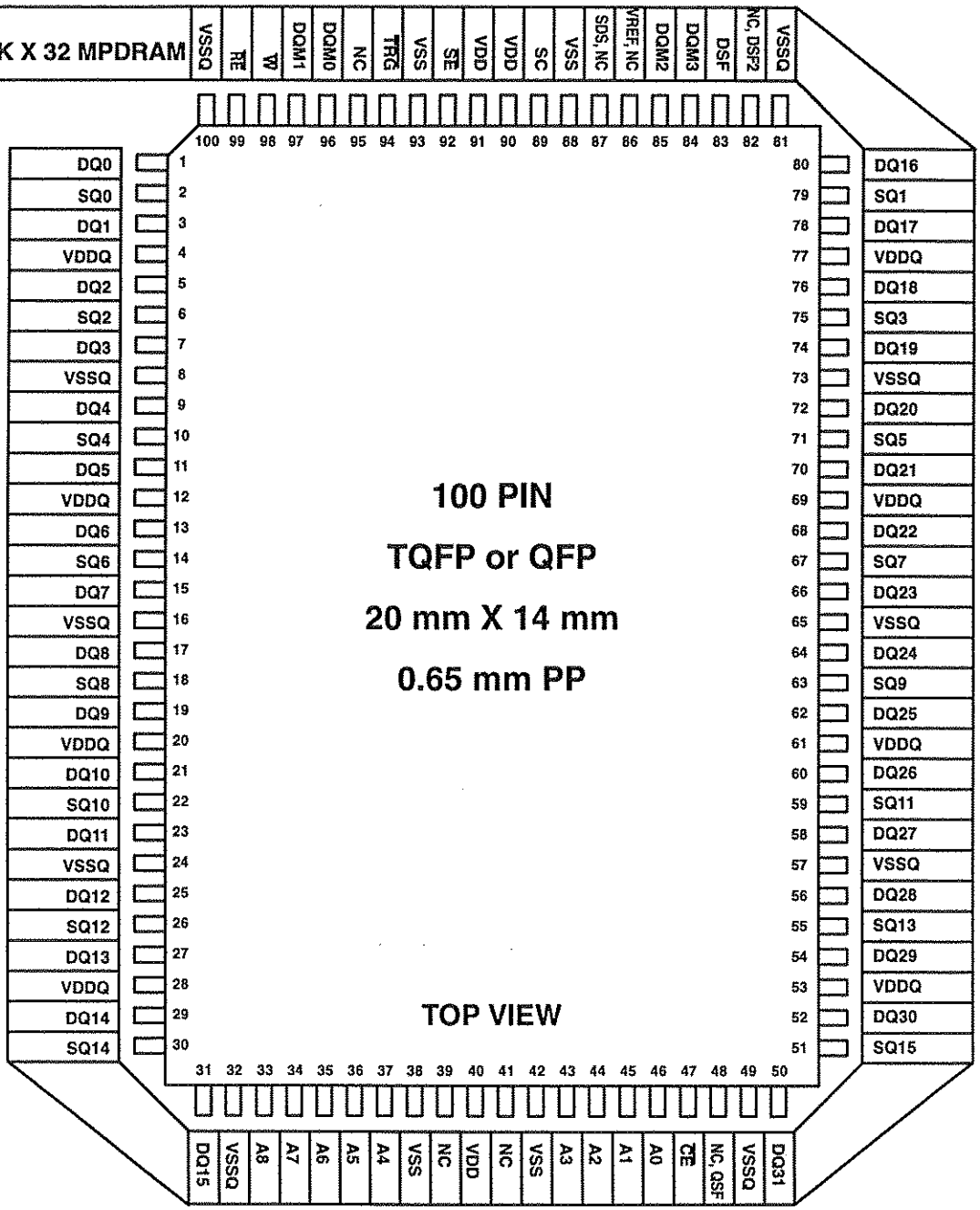
FIGURE 3.10.3–3
256K BY 16 SGRAM IN TSOP2



* In Release 6, Pin 30 had an optional VREF. This was deleted by action of the Committee in Release 7.

FIGURE 3.10.3–4
256K BY 32 SGRAM IN QFP

Release 6c7



Configuration
DRAM = 256K X 32
SAM = 512 X 16
ROW ADDRESS A0⇒A8
COLUMN ADDRESS A0⇒A8

FIGURE 3.10.3–7
256K BY 32 MPDRAM IN QFP

Release 7

3.10.4.1 - 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4-1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.2 - 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard, in addition to the minimum feature set defined in Table 3.10.4-1, may contain any of the features described in the Table, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.3 - MPDRAM BIT WRITE OPTIONAL FEATURE

This feature allows individual data bits of a memory array with a multi bit data interface to be selectively modified during a write cycle while other bits remain unchanged. The timing sequence used to control the feature is shown in figure 3.10.4-1 and operates as follows:

1-If W\ is low at the time that RE\ goes low, the state of the individual DQ pins determines if that data bit is to be written.

2-If DQ is HIGH write is ENABLED for that bit and the data present on DQ at the time that CE\ goes low is written.

3-If DQ is LOW, write is DISABLED for that bit and no subsequent writing can occur during that RE\ cycle.

4-If W\ is high at the time that RE\ goes low but goes low later in the cycle, a normal write cycle will be performed and all data bits will be written.

3.10.4.4 - 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 128K BY 8 MPDRAM described in this standard must contain, as a minimum, the feature set described in Table 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.5 - 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 128K X 8 MPDRAM described in this Standard may, in addition to the minimum feature set defined, contain any of the other features described in Table 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.6 - 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 2Mb & 4Mb density MPDRAMs described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.7 - 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE INCLUDING REQUIRED MINIMUM OPTIONAL FEATURE SET

The 2Mb & 4Mb density MPDRAMs described in this Standard must, in addition to the minimum basic feature set defined in Par. 3.10.4.6, contain all of the minimum defined set of optional features if any of them are included. In addition, any of the other features described may be included. The basic and optional features are shown in Table 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. These logic features must operate exactly as defined in the table to conform to the Standard. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.8 - SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4-2.

3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4–2.

3.10.4.9 – PIPELINED FAST PAGE MODE FOR MPDRAM

This standard describes the operational characteristics of an optional serial access data mode for the RAM PORT of MPDRAMs. The details and timing diagrams are given in Figures 3.10.4–3A and 3.10.4–3B.

3.10.4.10 – EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM

The EXTENDED DATA OUT FAST PAGE MODE defined in Sec. 3.9.5, DRAM OPTIONAL Features, on Page 3.9.5–11, Par. 1.4 is also applicable to MPDRAM as is needed. The mode is further defined with timing diagrams in Fig. 3.10.4–4.

3.10.4.11 – SAM OPTIONS FOR 4Mb MPDRAM

For 4 Mb MPDRAMs organized as 256K x 16, there are two options for the length of the SAM (Serial Access Memory). It may be either (1), 256 (Half SAM) or (2), 512 bits (Full SAM) for a 512 Column Page Depth. The details of these two options are described in Figs. 3.10.4–5A and 3.10.4–5B.

3.10.4.12 – Synchronous GRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Graphics DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–6 on Page 3.10.4–15.

3.10.4.13 – Synchronous MPDRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Multiport DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–7 on Page 3.10.4–16.

3.10.4.14 – Synchronous GRAM OPERATIONAL FUNCTION TABLES

This standard gives a set of functional truth tables for Synchronous Graphics DRAM. Three truth tables are given that define all standard operational functions. They are given in Tables 3.10.4–4A⇒C on Pages 3.10.4–17⇒19.

3.10.4.15 – 8Mb MPDRAM FEATURE SET FUNCTION TABLE

The 8Mb MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–15 on Page 3.10.4–8. This standard applies to devices with any interface data word length.

3.10.4.16 – Extended Functions for SGRAM and MPDRAM.

These standards define two special write function operations for SGRAM and MPDRAM. The functions defined are:

Write–Per–Bit
Block Write

These logic features must operate exactly as defined in the table to conform to the Standard. Details of the standards are given on Page 3.10.4–6.

XILINX EXHIBIT 1010
Page 132

SGRAM FUNCTION TABLE

CURRENT STATE	$\overline{S}$	$\overline{TR}$	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	X	H	L	X	BA, CA	ILLEGAL[2]
	L	L	X	H	L	H	CA	Latch Tap Address[7]
	L	H	L	L	H	H	BA, RA	Row (&Bank) active; Latch Row Address; No Mask
	L	H	H	L	H	H	BA, RA	Row (&Bank) active; Latch Row Address; Use Mask
	L	L	L	L	H	H	BA, RA	Read Transfer; Latch Row Address ⇒ Precharge
	L	L	H	L	H	H	BA, RA	Split Read Transfer; Latch Row Address ⇒ Precharge
	L	H	L	L	H	L	BA, AP	NOP[4]
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	H	L	L	L	H	X	Auto–Refresh[6]
	L	H	H	L	L	H	X	ILLEGAL
	L	L	X	L	L	H	X	ILLEGAL
	L	H	L	L	L	L	Op–code	Mode Register Access[6]
	L	H	H	L	L	L	Op–code	Special Register Access[5]
	L	L	X	L	L	L	X	ILLEGAL
ROW ACTIVE	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	L	H	L	H	BA, CA, AP	Begin Read; Latch CA; Determine AP
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Begin Write; Latch CA; Determine AP
	L	H	H	H	L	L	BA, CA, AP	Block Write; Latch CA; Determine AP
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Precharge
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	X	X	L	L	H	X	ILLEGAL
	L	H	L	L	L	L	Op–code	ILLEGAL
	L	H	H	L	L	L	Op–code	Special Register Access[5]
	L	L	X	L	L	L	X	ILLEGAL

TABLE 3.10.4–4 A
SGRAM FUNCTION TABLE

SGRAM FUNCTION TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{TR}$	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
READ	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Row Active)
	L	X	X	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	L	H	H	L	X	RESERVED (Term. Burst);⇒Row Active
	L	H	H	H	H	L	X	ILLEGAL
	L	L	X	H	H	L	X	ILLEGAL
	L	H	L	H	L	H	BA, CA, AP	Term Burst, New Read, Determine AP[3]
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Term Burst, Start Write, Determine AP[3]
	L	H	H	H	L	L	BA, CA, AP	Term Burst, Start Write, Determine AP[3]
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Term Burst, Precharge Timing for Reads
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	X	X	L	L	X	X	ILLEGAL
WRITE	H	X	X	X	X	X	X	NOP(Continue Burst to End;⇒Row Active)
	L	X	X	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	L	H	H	L	X	RESERVED (Term Burst);⇒Row Active
	L	H	H	H	H	L	X	ILLEGAL
	L	L	X	H	H	L	X	ILLEGAL
	L	H	L	H	L	H	BA, CA, AP	Term Burst, Start Read, Determine AP[3]
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Term Burst, New Write, Determine AP[3]
	L	H	H	H	L	L	BA, CA, AP	Term Burst, Block Write, Determine AP[3]
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Term Burst, Precharge[3]
	L	X	X	L	L	X	X	ILLEGAL
READ with AUTO Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	H	BA, CA, AP	ILLEGAL[2]
	L	X	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	X	BA, RA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
WRITE with AUTO Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	H	BA, CA, AP	ILLEGAL[2]
	L	X	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	X	BA, RA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL

TABLE 3.10.4–4 B
SGRAM FUNCTION TABLE (Continued)

SGRAM FUNCTION TABLE (continued)

CURRENT STATE	$\overline{S}$	TR	$\overline{DSF}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H	X	X	X	X	X	X	NOP⇒idle after tRP
	L	X	X	H	H	H	X	NOP⇒idle after tRP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	X	H	L	X	BA, CA, AP	ILLEGAL[2]
	L	L	X	H	L	H	CA	Latch Tap Address[7]
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	X	X	L	H	L	BA, AP	NOP[4]
	L	X	X	L	L	X	X	ILLEGAL
ROW Activating	H	X	X	X	X	X	X	NOP⇒Row Active after tRCD
	L	X	X	H	H	H	X	NOP⇒Row Active after tRCD
	L	X	X	H	H	H	X	ILLEGAL[2]
	L	X	X	H	L	X	BA, CA, AP	ILLEGAL[2]
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	X	X	L	H	L	BA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
WRITE Recovering	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	X	BA, CA, AP	ILLEGAL[2]
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	X	X	L	H	L	BA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	X	NOP⇒idle after tRP
	L	X	X	H	H	X	X	NOP⇒idle after tRP
	L	X	X	H	L	X	X	ILLEGAL
	L	X	X	L	H	X	X	ILLEGAL
	L	X	X	L	L	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL
	L	X	X	H	L	X	X	ILLEGAL
	L	X	X	L	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address — BA = Bank Address — Term = Terminate

CA = Column Address — AP = Auto Precharge — NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n–rule", bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and AP).
5. Legal only if all banks are in idle or row active state.
6. Illegal if any bank is not idle.
7. Illegal if any bank is not idle or precharging.

ILLEGAL = Device operation and/or data–integrity are not guaranteed

TABLE 3.10.4–4 C
SGRAM FUNCTION TABLE (Continued)

8 Mb BURST MPDRAM FUNCTION TRUTH TABLE

CYCLE	$\overline{CE}$	RE Fall				$\overline{CE}$		A(n)		DQ(n)			FUNCTION
CODE	$\overline{CE}$	TRG	W	DSF1	DSF2	DSF1	DSF2	RE	$\overline{CE}$.	RE	$\overline{CE}$	DQM	
OPTION	0	0	0	0	0	—	0	MODE	—	X	—	X	OPTIONAL
CBRR	0	X	1	0	0	—	0	X	—	X	—	X	CBR REFRESH (OPTION RESET)
CBRS	0	X	0	1	0	—	0	STOP Addr	—	X	—	X	CBR REFRESH STOP POINT SET
CBRSD	0	X	0	1	1	—	0	X	—	X	—	X	CBR REFRESH SDS MODE SET
CBRN	0	X	1	1	0	—	0	X	—	X	—	X	CBR REFRESH NO RESET
RT	1	0	1	0	0	0	0	ROW	TAP	X	X	X	READ TRANSFER CYCLE
SRT	1	0	1	1	0	0	0	ROW	TAP	X	X	X	SPLIT READ TRANSFER CYCLE
RWM	1	1	0	0	0	0	0	ROW	COL	WPBM	DATA IN	DQM	READ MASKED WRITE CYCLE
BRWM	1	1	0	0	1	0	0	ROW	COL	WPBM	DATA IN	DQM	BURST READ MASKED WRITE CYCLE
BWM	1	1	0	0	0	1	0	ROW	CA3–CA8 CA0=CR	WPBM	COL ADDR MASK	DQM	MASKED BLOCK WRITE CYCLE
RW	1	1	1	0	0	0	0	ROW	COL	X	DATA IN	DQM	READ WRITE CYCLE (NO MASK)
BRW	1	1	1	0	1	0	0	ROW	COL	X	DATA IN	DQM	BURST READ WRITE CYCLE (NO MASK)
BI	—	—	—	—	—	0	1	ROW	COL	X	X	X	BURST INTERRUPT
BW	1	1	1	0	0	1	0	ROW	CA3–CA8 CA0 = CR	X	COL ADDR. MASK	DQM	BLOCK WRITE
LCR	1	1	1	1	0	1	0	ROW	CA0 = CR	X	COLOR	DQM	LOAD COLOR REGISTER
LMR	1	1	1	1	0	0	0	ROW	X	X	WPBM	DQM	LOAD MASK REGISTER

X = Don't care 0 or 1 — = NOT APPLICABLE

NOTES: CR = 0 selects Color Register 0 CR = 1 selects Color Register 1
All states not defined are illegal. If used, device operation and/or data integrity are not guaranteed.

BYTE ENABLE TRUTH TABLE			
		$\overline{CE}$ FALLING	
DQM0–DQM3			
DQM0	0	Byte Write Enable (DQ0–DQ7)	
	1	Byte Write Disable (DQ0–DQ7)	
DQM1	0	Byte Write Enable (DQ8–DQ15)	
	1	Byte Write Disable (DQ8–DQ15)	
DQM2	0	Byte Write Enable (DQ16–DQ23)	
	1	Byte Write Disable (DQ16–DQ23)	
DQM3	0	Byte Write Enable (DQ24–DQ31)	
	1	Byte Write Disable (DQ24–DQ31)	

8M BURST MPDRAM FUNCTION TABLE

8MB BURST MPDRAM FUNCTION TABLE
TABLE 3.10.4–5

Extended Functions for SGRAM and SVRAM

WRITE–PER–BIT WPB, for Synchronous Video RAMs (SVRAM), and Synchronous Graphics RAMs (SGRAM) is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enabled.

1) A Bank Active Command with DSF = 1 (high) enables Write–per–bit for the associated bank. A bank active command with DSF = O (low) disables Write–Per–Bit for the associated bank.

2) The mask used for Write per–bit operations is stored in the Mask Register accessed by Special Register Access command. When a mask bit = 1 (high), the associated data bit is written when a Write Command is executed and Write–per–bit has been enabled for the bank being written. When a mask bit = O (low) the associated data bit is unaltered when a Write Command is executed and Write–per–bit has been enabled for the bank being written.

3) No additional, timing conditions are required for Write per–bit operations. Write–per–bit writes can be either single writes, burst writes, or block writes.

4) DQM masking is the same for WPB and non–WPB writes.

BLOCK WRITE for Synchronous Multi–port DRAMs (SMPRAM), and Synchronous Graphics RAMs (SGRAM). A feature allowing the simultaneous writing of consecutive columns of data within RAM device during a single access cycle. During block write the data to be written comes from an internal "color" register and the DQ I/O pins are used for independent column selection. The block of columns to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB's ignored.

1) A Write Command with DSF = 1 (high) enables Block Write for the associated bank. A Write Command with DSF = O (low) disables Block Write for the associated bank.

2) The block size is 8 columns. Where column = "n" bits for by "n" part.

3) The Color Register is the same width as the data port of the part. It is written via a special register access where data present on the DQ pins is copied into the internal color register. The color register provides the data to be copied to the 8 column locations during a block write cycle as masked by the DQ column select, WPB mask (if enabled), and DQM byte mask.

4) Column data masking is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per byte basis (i.e. DQ[0:7] provides the column mask for data byte [0;7], DQ[8.15] provides the column mask for data byte [8:15] and so on). A DQ column mask of 1 (high) enables the particular column to be written while a value of 0 (low) disables writing of the data. The relationship between DQ bits and column within the block is logically equivalent within each byte (i.e. DQ[0] masks column [0] for data bits [0:7] DQ[8] masks column [0] for data bits [8:15], DQ[1] masks column [1] for data bits [0:7], DQ[9] masks column [1] for data bits 18:15], etc.).

5) Block Writes are always non–burst, independent of the burst length that has been programmed into the Mode Register. Back–to–back Block Writes are allowed provided that the specified Block Write cycle time is satisfied.

6) If Write–per–bit was enabled to the bank by executing a Bank Active Command with DSF=1 (high), then write–per–bit masking of the Color Register data is enabled. If Write–per–bit was disabled to the bank by executing a Bank Active Command with DSF=O (Low), then write–per–bit masking of the color Register data is disabled.

7) DQM masking provides independent data byte masking during block write exactly the same as It does during normal write operations, except that the control is extended to the 8 consecutive columns of the block write.

3.11.2 NIBBLE WIDE SDRAM

3.11.2.1 – 4M BY 4 SDRAM IN TSOP2

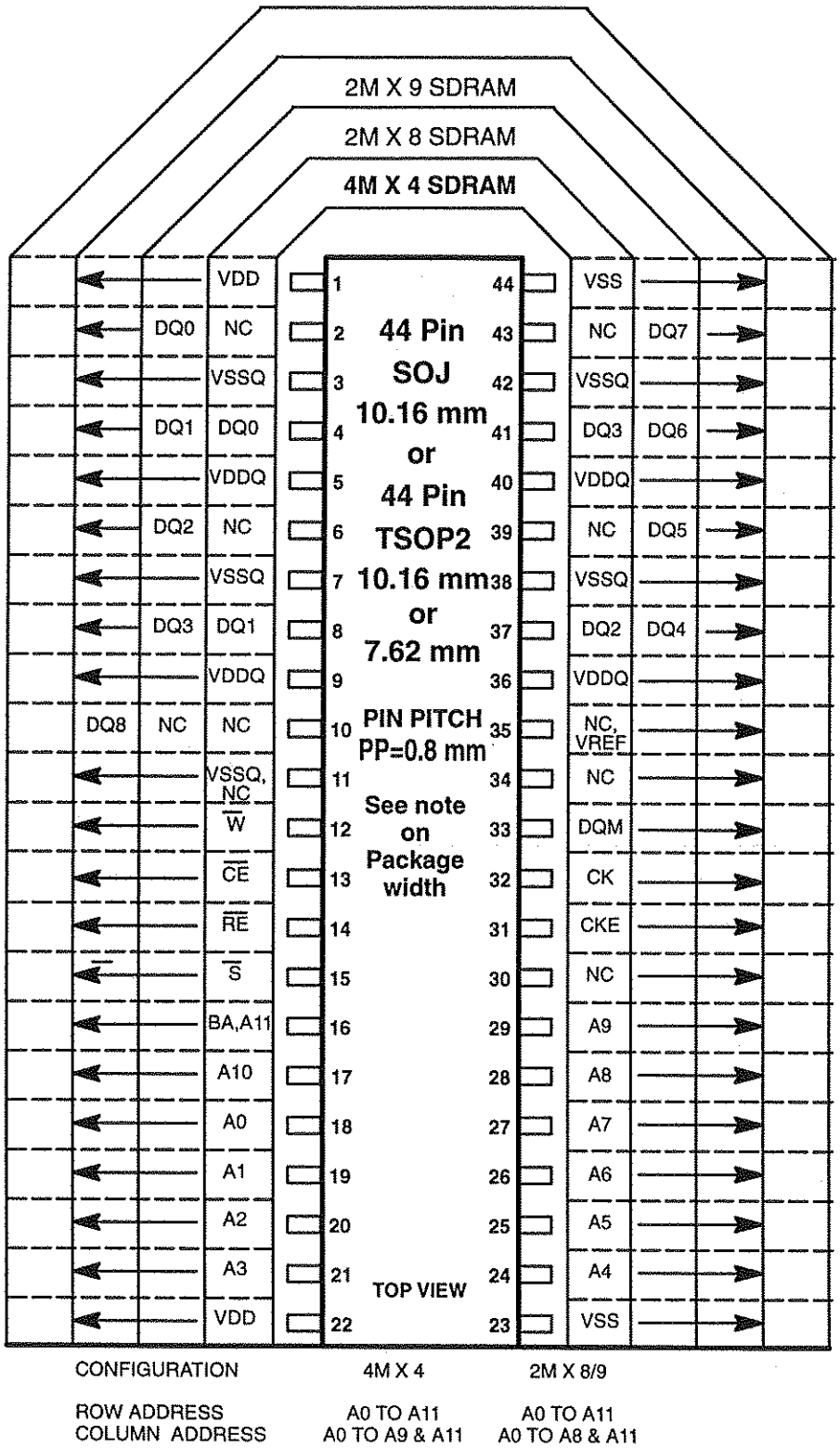
CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—44 Pin TSOP2, 7.62 mm or 10.16 mm WIDE, 0.8mm PIN PITCH
—44 Pin SOJ 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1

3.11.2.2 – 16M BY 4 SDRAM IN TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1

3.11.2.3 – 64M BY 4 SDRAM PIN ROTATION

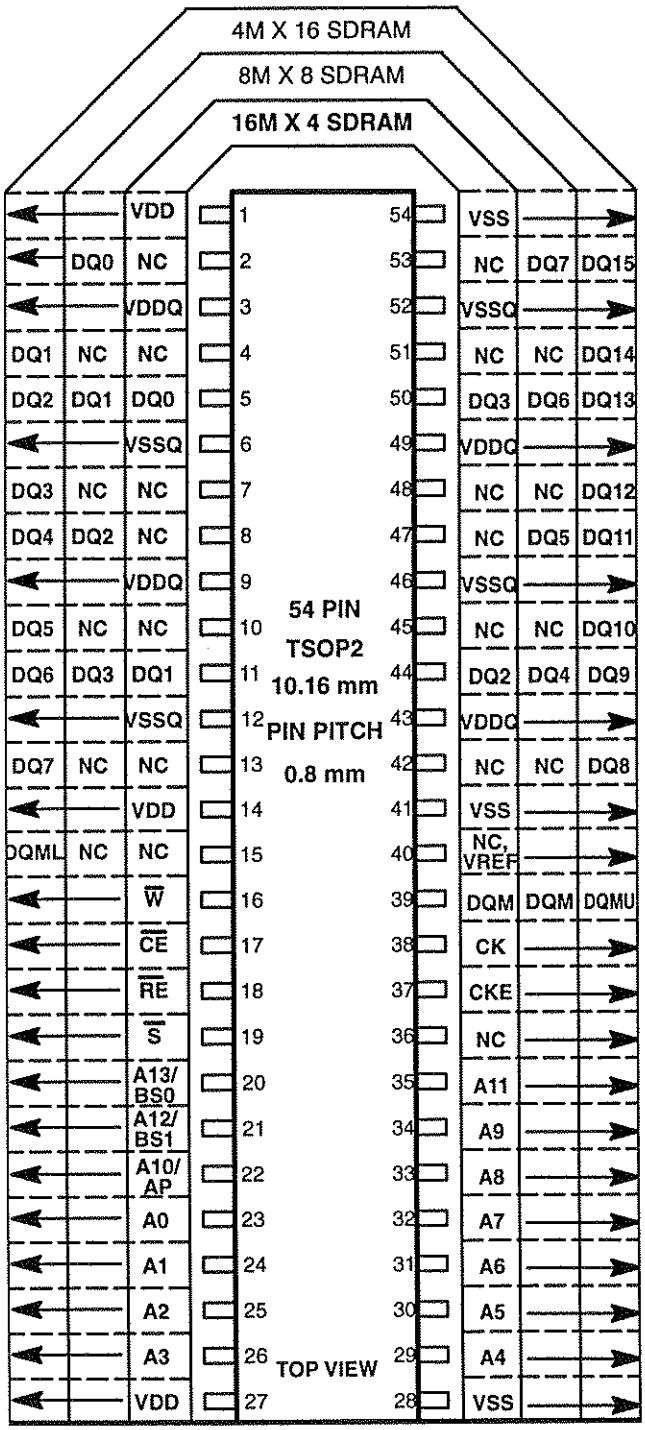
CAPACITY—64M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.2–5
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.



Notes:
1) The VREF option on P35 was added when the 0.3" package was approved.

2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.2–1
4M X 4 SDRAM IN TSOP2



	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

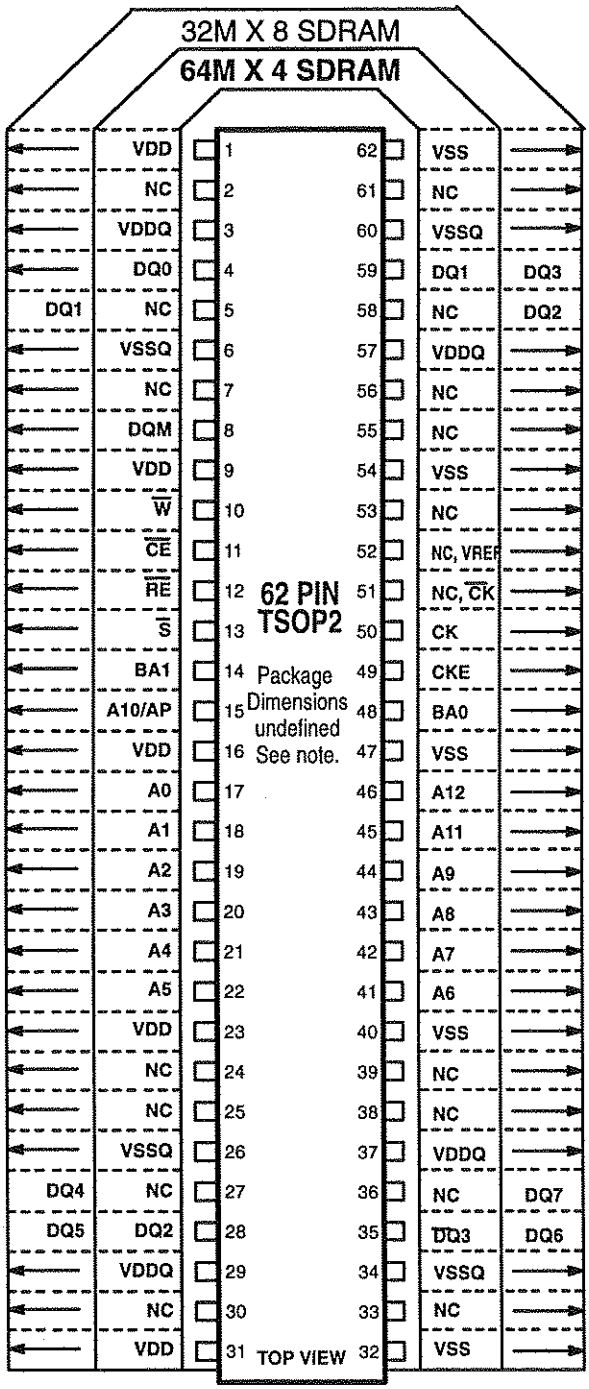
A10	AUTO PRECHARGE

BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.2–2
16M BY 4 SDRAM IN TSOP2



Configuration	64M X 4	32M X 8
ROW ADDRESS	A0⇒A12	A0⇒A12
COLUMN ADDRESS	A0⇒A9,A11	A0⇒A9

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).

7. BA0 is the Least Significant Bank Addr.

8. BA1 is the Most Significant Bank Addr.

9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.2–3
64M BY 4 SDRAM PIN ROTATION IN TSOP2

3.11.3 BYTE WIDE SDRAM

3.11.3.1 – 2M BY 8 or 9 SDRAM IN TSOP2

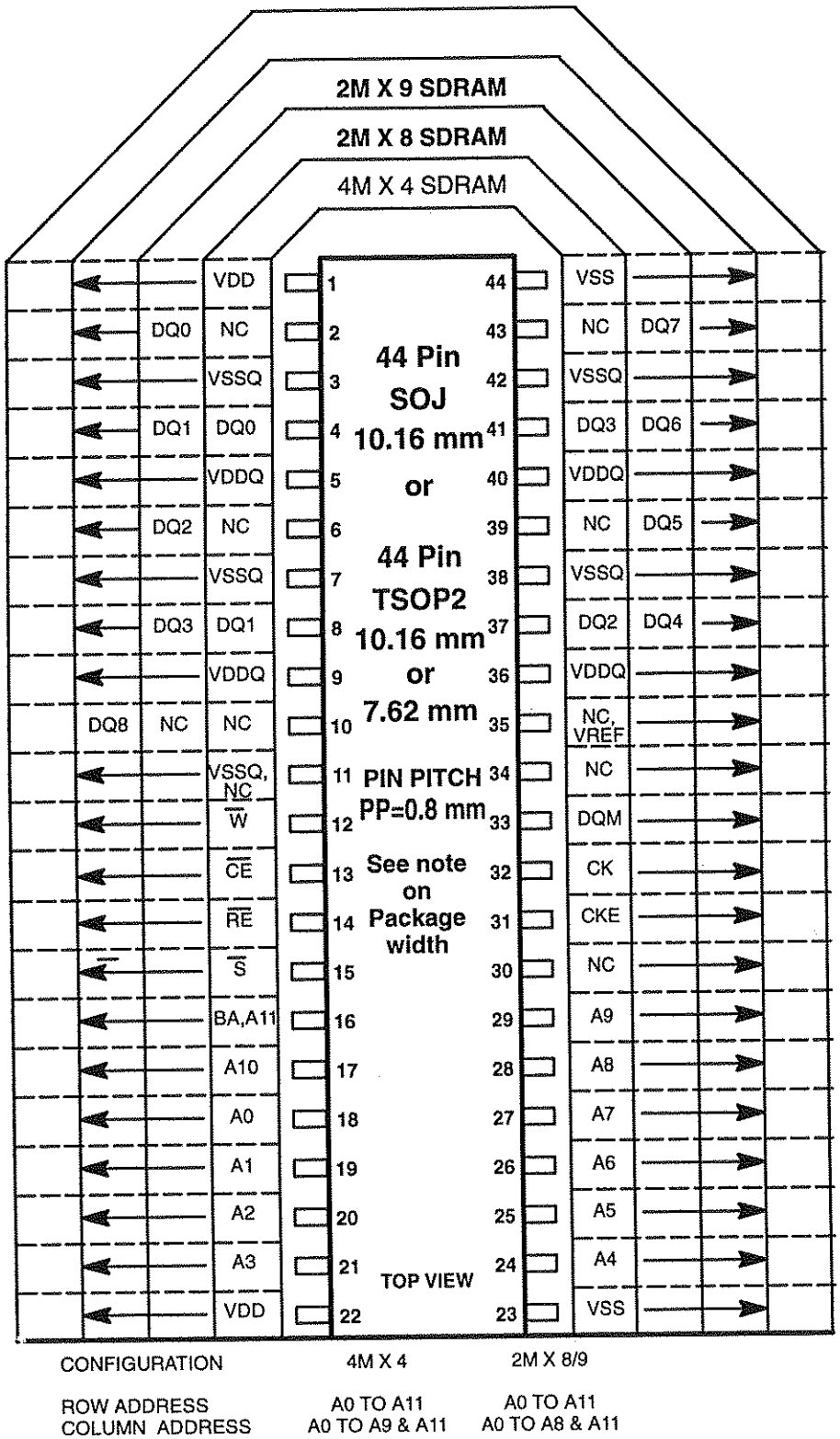
CAPACITY—2M WORDS OF 8 or 9 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LVTTL
PACKAGE—44 Pin TSOP2, 7.62 mm WIDE, 0.8mm PIN PITCH (2M X 8 part only)
PACKAGE—44 Pin TSOP2, 10.16 WIDE, 0.8mm PIN PITCH
PACKAGE—44 Pin SOJ, 10.16 WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.3–1

3.11.3.2 – 8M BY 8 SDRAM IN TSOP2

CAPACITY—8M WORDS OF 8 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.3–2

3.11.3.3 – 32M BY 8 SDRAM PIN ROTATION

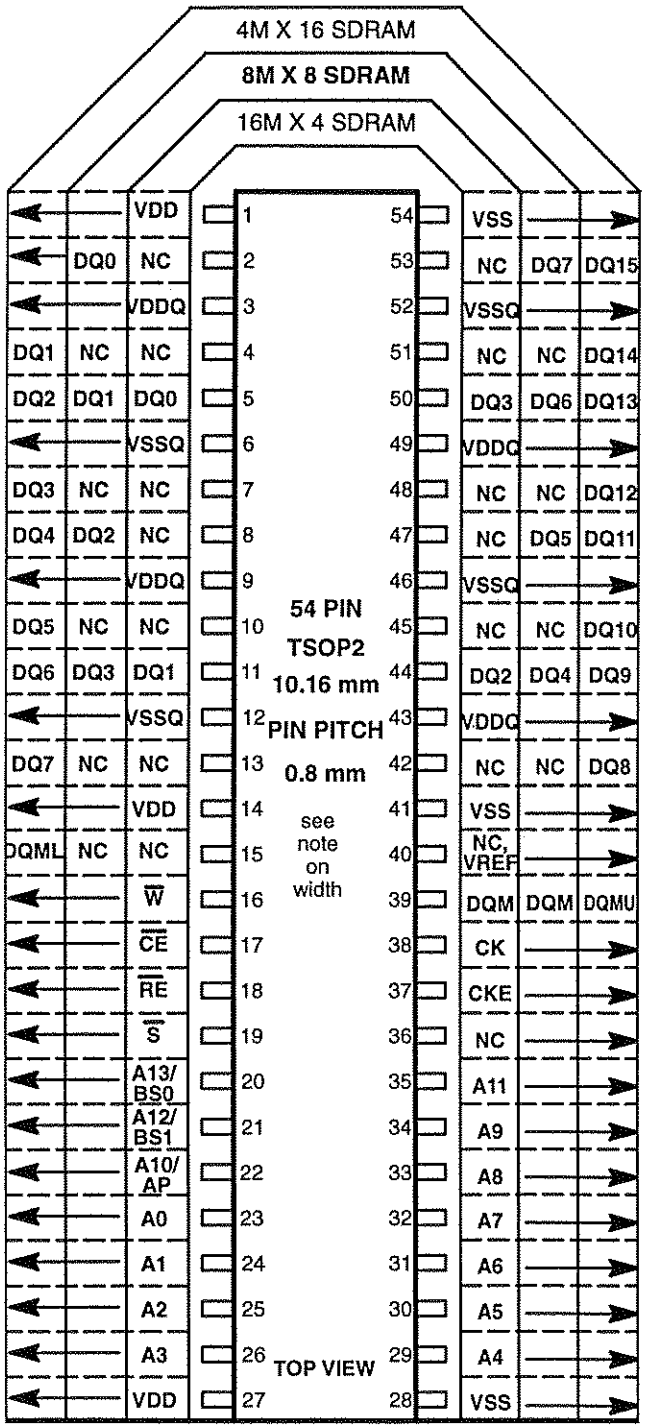
CAPACITY—32M WORDS OF 8 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.3–5
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.



Notes:
1) The VREF option on P35 was added when the 0.3" package was approved.

2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.3–1
2M BY 8 OR 9 SDRAM IN TSOP2



	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

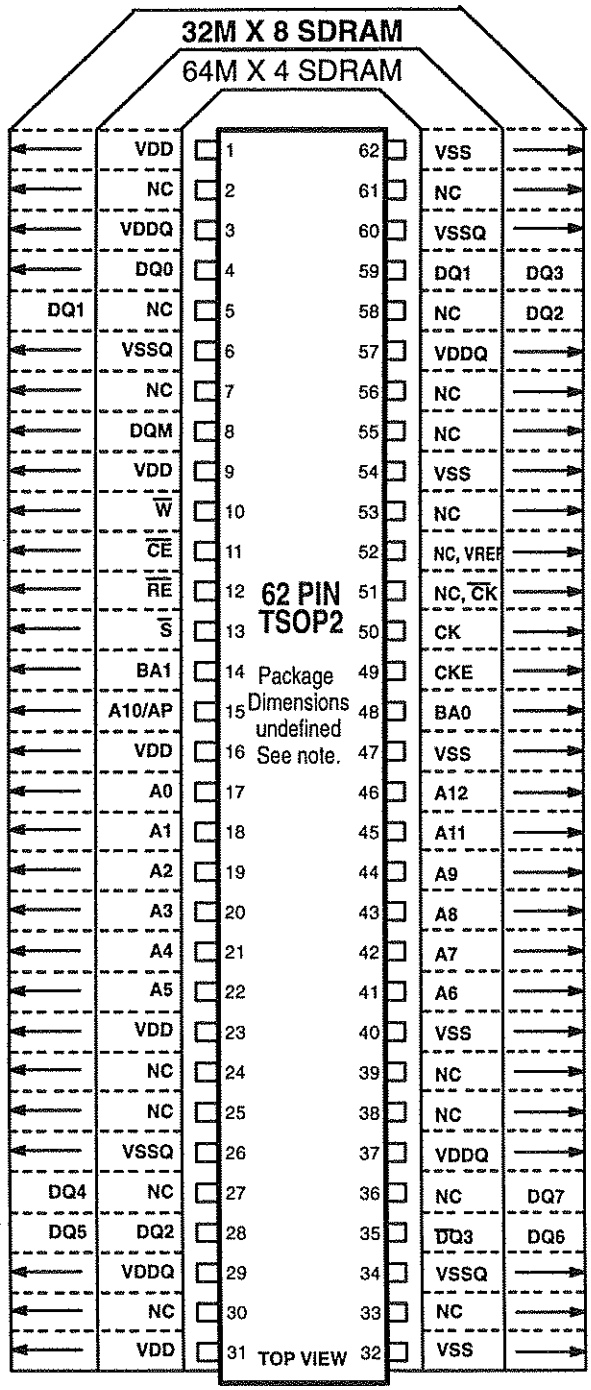
A10	AUTO PRECHARGE

BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.3–2
8M BY 8 SDRAM IN TSOP2



Configuration	64M X 4	32M X 8
ROW ADDRESS	A0⇒A12	A0⇒A12
COLUMN ADDRESS	A0⇒A9,A11	A0⇒A9

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).

7. BA0 is the Least Significant Bank Addr.

8. BA1 is the Most Significant Bank Addr.

9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.3–3
32M BY 8 SDRAM PIN ROTATION IN TSOP2

3.11.4 WORD WIDE SDRAM

3.11.4.1 – 256K BY 16 AND 1M BY 16 & 18 SDRAM IN TSOP2

CAPACITY—256K WORDS OF 16 BITS AND 1M WORDS OF 16 OR 18
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LOWER LEVEL INTERFACE CONSISTENT WITH THE VALUE OF VDD CHOSEN.
PACKAGE—50 Pin SOJ, 10.16 mm WIDE, 0.8mm PIN PITCH
PACKAGE—50 Pin TSOP2, 0.400" WIDE (10.16 mm), 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.4–1

NOTE: The 256K part has the same pinout as the SGRAM part shown in Fig. 3.10.3–3 with the exception of the DSF function on P 33.

3.11.4.2 – 2M & 4M BY 16 SDRAM IN TSOP2

CAPACITY—2M or 4M WORDS OF 16 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.4–2

3.11.4.3 – 16M BY 16 SDRAM IN TSOP2 PIN ROTATION

CAPACITY—16M WORDS OF 16 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.4–3

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.11.4.4 – 256K BY 32 SDRAM IN QFP or TQFP

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.11.4–4

NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.10.3–4 with the exception of the DSF function on P 33.

3.11.4.5 – 2M BY 32 SDRAM IN TSOP2

CAUTION: See note in Fig. 3.11.4–5 regarding the use of this device.
CAPACITY—2M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—Synchronous address & control interface.
PACKAGE—84 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP
PIN ASSIGNMENTS—FIG. 3.11.4–5

3.11.4.6 – 8M BY 32 SDRAM IN TSOP2 PIN ROTATION

CAPACITY—8M WORDS OF 32 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.4–6

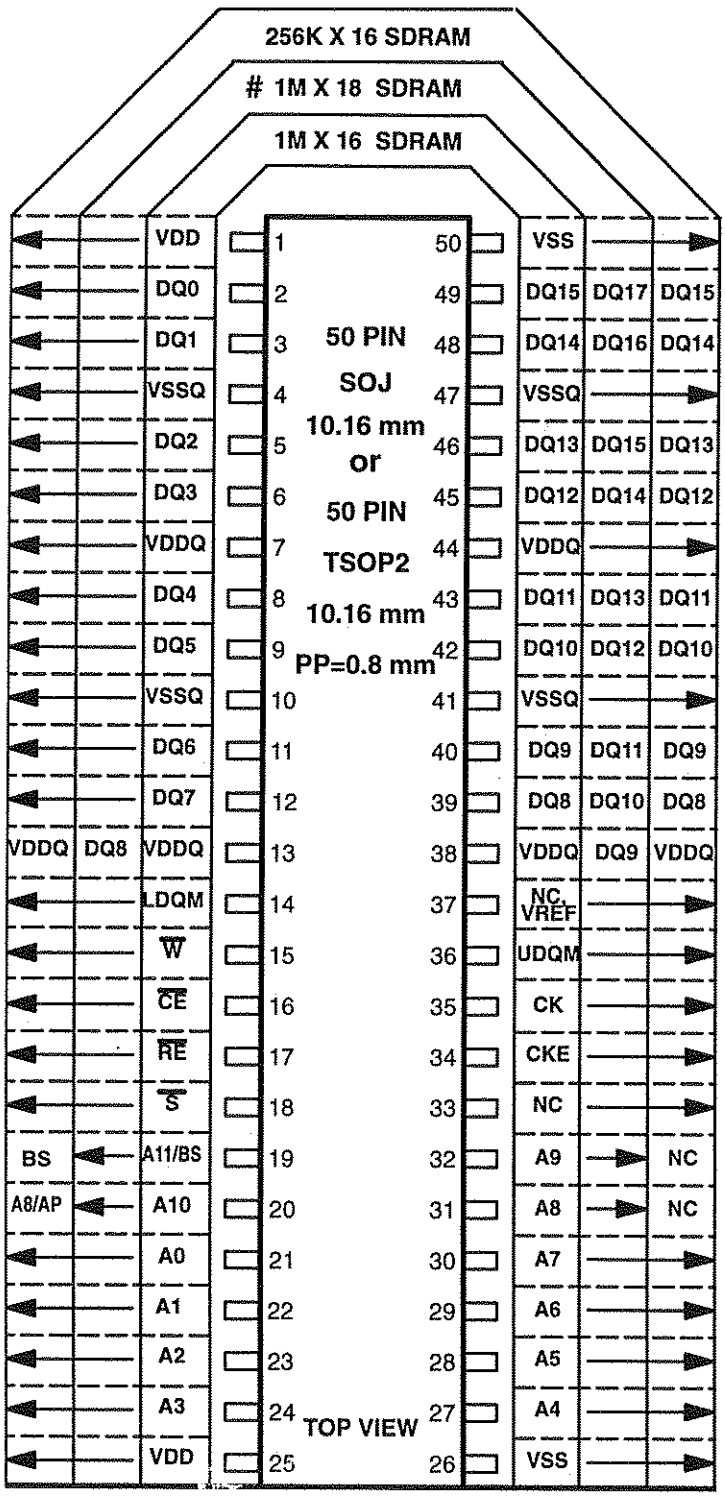
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

XILINX EXHIBIT 1010
Page 151

3.11.4.7 – 2M BY 32 & 36 SDRAM IN TSOP2

CAPACITY—8M WORDS OF 32 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—86 PIN TSOP2, 10.16 mm Wide, 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.11.4–7

XILINX EXHIBIT 1010
Page 152



	256K	1M 1K RFSH	1M 4K RFSH
ROW/REFRESH ADDRESSES	A0 ⇒ A8	A0 ⇒ A9	A0 ⇒ A11
COLUMN ADDRESSES	A0 ⇒ A7	A0 ⇒ A9	A0 ⇒ A7

* Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

1) Pin 20 (A10) id the auto–precharge input during read and write commands.

2) Pin 37 (NC, VREF) is VREF on devices that need an external voltage reference. On other devices, it is a NC.

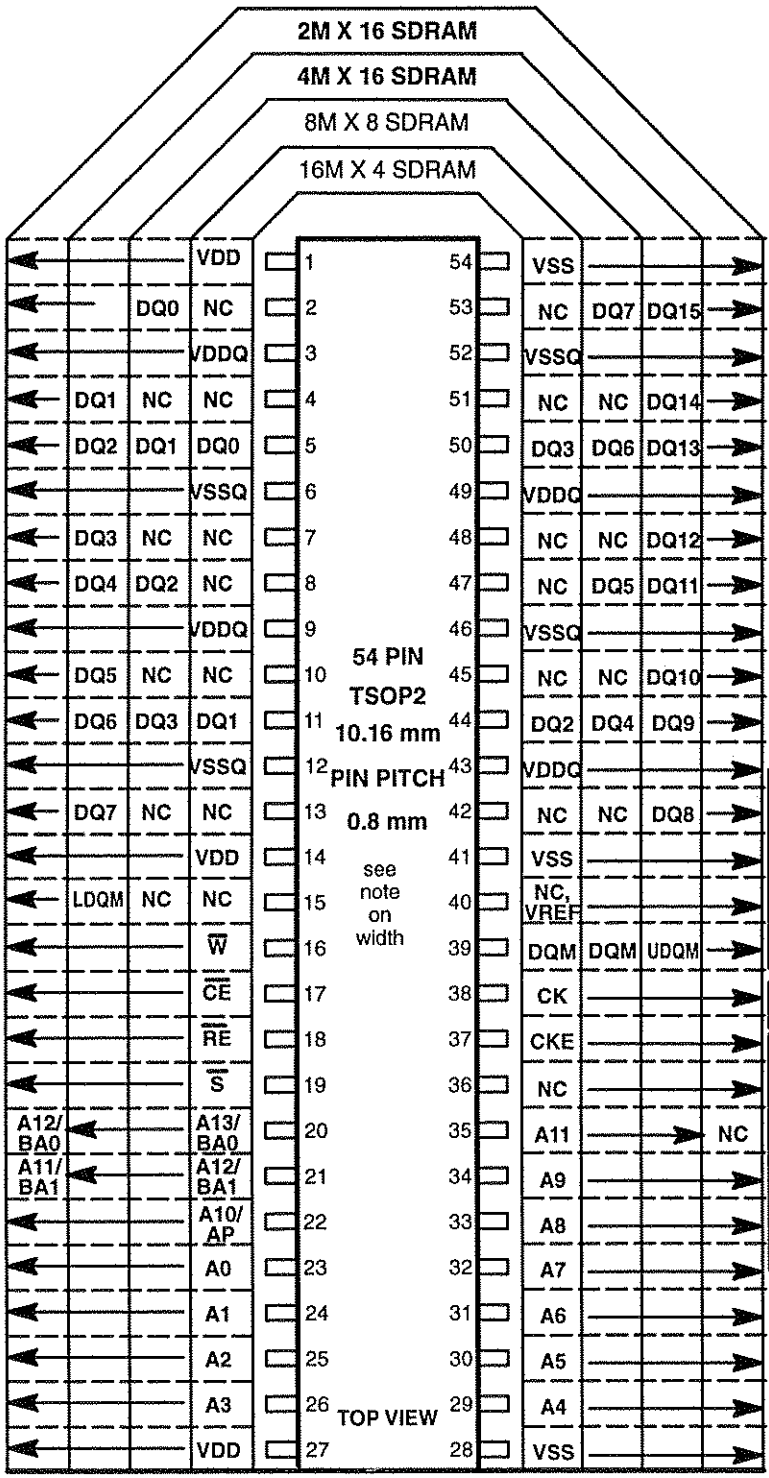
3) All VDDQ and VSSQ pins may be VDD and VSS at the option of the supplier

4) BS is the Bank Select Address

5) The 256K device has the same pinout as the 256K X 16 SGRAM shown in Fig 3.10.3–3 except for the lack of a DSF function on pin 33.

\# The 1M X 18 device is approved for use in the TSOP2 package only.

FIGURE 3.11.4–1
256K X 16 & 1M X 16/18 SDRAM IN SOJ & TSOP–2



Device	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16, 4M	A0⇒A13	A0⇒A7
X16, 2M	A0⇒A12	A0⇒A7

A10	AUTO PRECHARGE

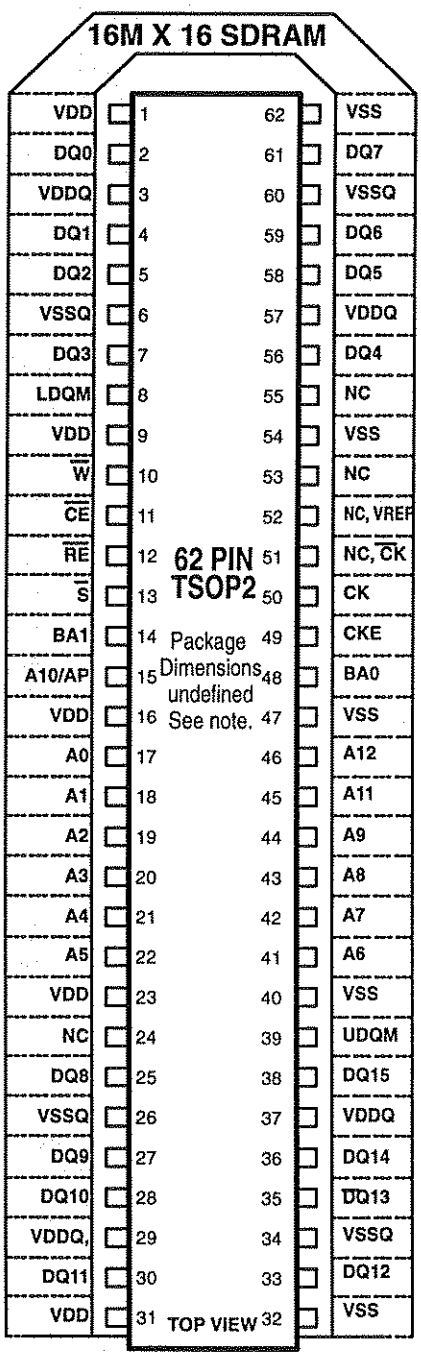
BANKS	BANK SELECT ADDRESS
4	A13/A12
4 #	A12/A11
2	A13
2 #	A12

2M X 16

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.4–2
2M & 4M BY 16 SDRAM IN TSOP2



Configuration	16M X 16
ROW ADDRESS	A0–A12
COLUMN ADDRESS	A0–A8

NOTES

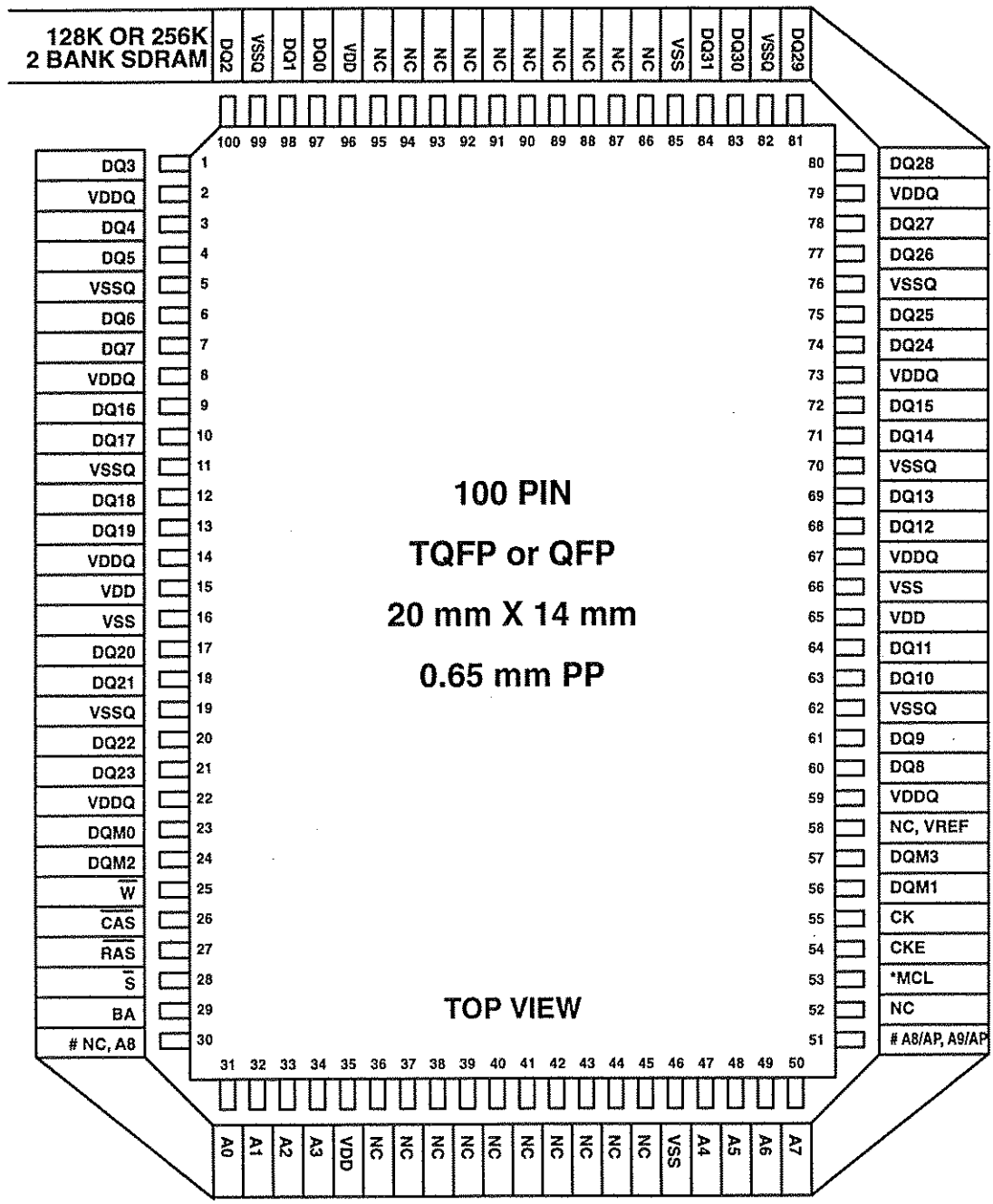
1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.
3. (NC, VREF) is VREF on devices that require an external voltage reference.
4. BA0 is the least significant bank address
5. BA1 is the most significant bank address
6. A10/AP is row address A10, autoprecharge and precharge all banks.
7. (NC, $\overline{CK}$) is NC for devices using a single ended clock. $\overline{CK}$ is used for devices using a differential clock.
8. (NC, VREF) is VREF on devices that require an external voltage reference.
9. This standard is for a 4 Bank version only.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4–3
16M BY 16 SDRAM PIN ROTATION IN TSOP2



Note: This pinout is for both 128K and 256K parts. The Pin assignments are as follows

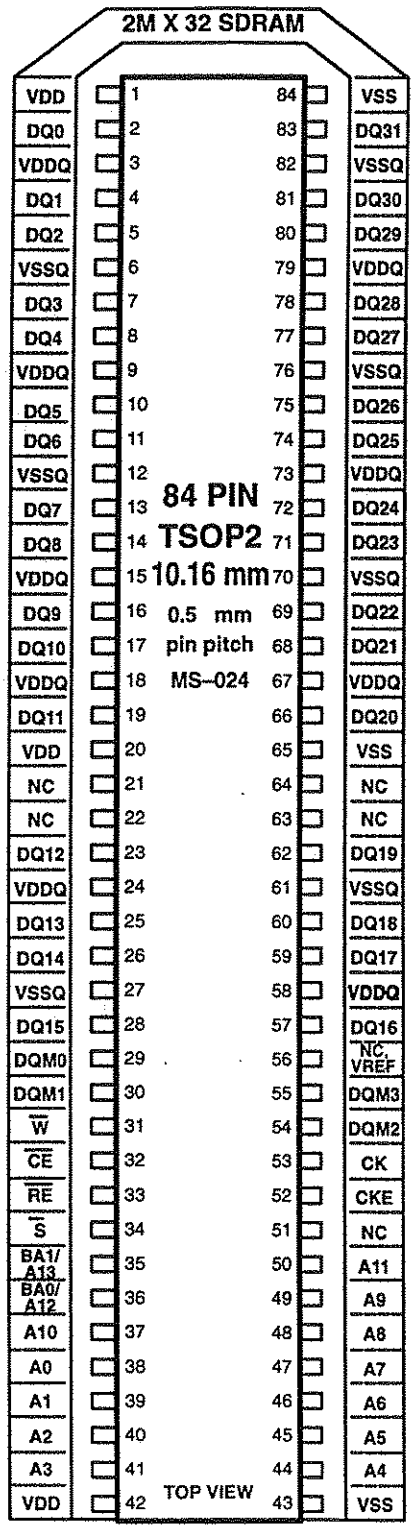
Configuration	P30	P51
128K x 2 Bank	NC	A8/AP;
256K X 2 Bank	A8	A9/AP

* Note: This part is a subset of the SGRAM shown in Fig. 3.10.3–4. P53 is DSF for the SGRAM version and MCL for the SDRAM.
MCL = Must Connect to Logic Low

Configuration	128K X 2	256K X 2
ROW ADDRESS	A0⇒A8,BA	A0⇒A9,BA
COLUMN ADDRESS	A0⇒A7	A0⇒A7
BANK SELECT		A9
REFRESH PERIOD	16 ms	32 ms
# ROWS REFRESH	1024	2048

FIGURE 3.11.4–4
128K & 256K BY 32, 2 BANK SDRAM IN QFP

Release 6r7



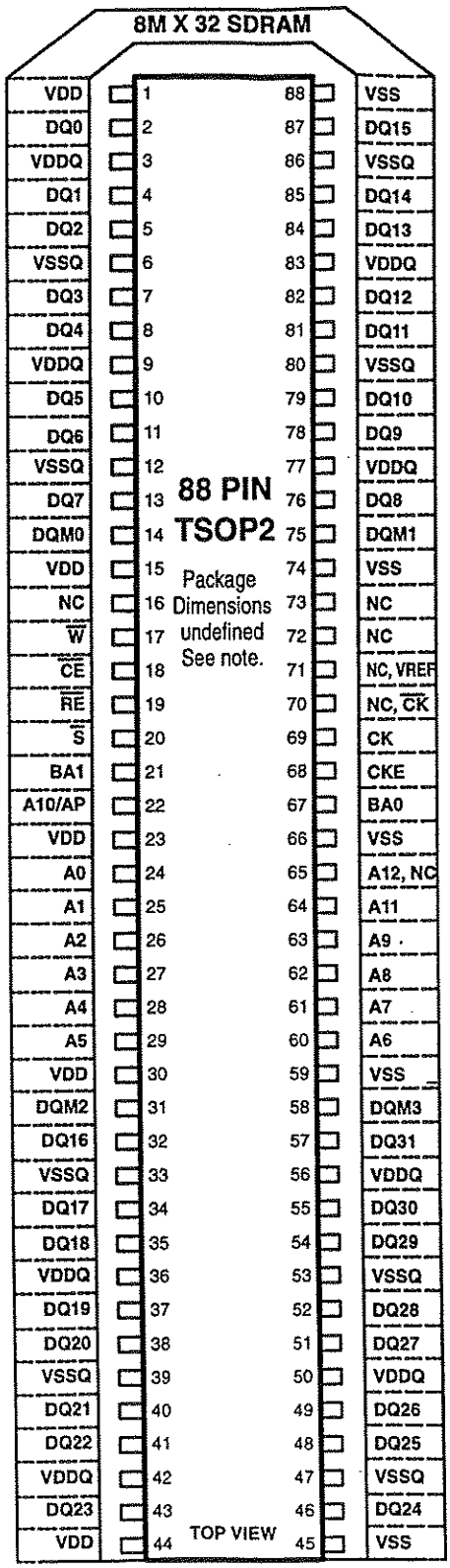
NOTE:
In addition to this pinout for a 2M X 32 SDRAM, there is another one that has the DQ pins at the outer ends of the package and the control pins in the center and superceeds this one. The other device should be used for all new designs. It is found in figure 3.11.4–7.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

ADDRESS ORGANIZATION

	2	4
NUMBER BANKS		
ROW ADDR.	A0⇒A13	A0⇒A13
COL. ADDR.	A0⇒A6	A0⇒A6
AUTO–PRECHARGE	A10	A10
BANK ADDRESS	A13	A12, A13

FIGURE 3.11.4–5
2M BY 32 SDRAM IN TSOP2



NOTES
1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.
2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.
3. (NC, VREF) is VREF on devices that require an external voltage reference.
4. BA0 is the least significant bank address
5. BA1 is the most significant bank address
6. A10/AP is row address A10, autoprecharge and precharge all banks.
7. (NC, $\overline{CK}$) is NC for devices using a single ended clock. $\overline{CK}$ is used for devices using a differential clock.
8. (NC, VREF) is VREF on devices that require an external voltage reference.
9. This standard is for a 4 Bank version only.

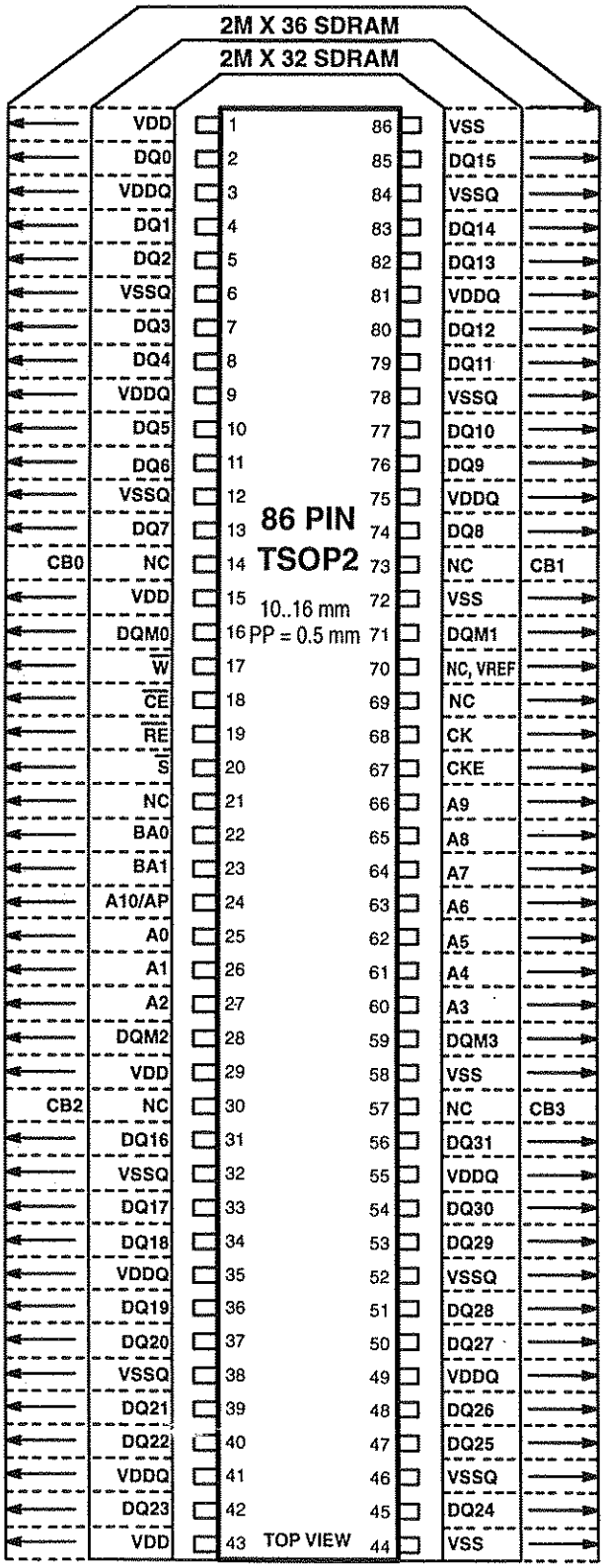
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	8M X 32	8M X 32
Number RA	13	12
ROW ADDRESS	A0⇒A12	A0⇒A11
COLUMN ADDRESS	A0⇒A7	A0⇒A8

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4–6
8M BY 32 SDRAM PIN ROTATION IN TSOP2

Release 6c7



NOTES

1. A10/AP Is Row Address A10, Autopre charge And Precharge All Banks Input.

2. (NC,VREF) is VREF on devices that require an external voltage reference.

3. The VDDQ designator is used when t power supply pins for the DQ I/O drivers are internally DC isolated from the VDD power supply pins.

4. The VSSQ designator is used when tl ground reference pins for the DQ I/O drivers are internally DC isolated from th primary ground reference (VSS) power supply pins.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	2M X 32
REFRESH ADDR.	A0 ⇒ A11
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.11.4–7
2M BY 32 & 36 SDRAM IN TSOP2

SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE_{n-1}	CKE_n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Self–refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self–Refresh)
Power–Down	H	X *	X	X	X	X	X	INVALID
	L	H *	H	X*	X*	X*	X	EXIT Power Down⇒ABI
	L	H *	L	H	H	H	X	EXIT Power Down⇒ABI
	L	H *	L	H	H*	L*	X	ILLEGAL
	L	H *	L	H*	L*	X*	X	ILLEGAL
	L	H*	L	L	X*	X*	X	ILLEGAL
	L	L	X	X*	X*	X	X	NOP(Maintain Low–Power Mode)
All Banks Idle[7]	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power–Down
	H	L	L	H	H	H	X	Enter Power–Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self–Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8]
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS
ABI = All Banks Idle
NOTES:

6. CKE Low–to–High transition will re–enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power–Down and Self–Refresh can be entered only from the All Banks Idle State.
8. Must be legal command.
* Elements of the table that were in error in the first printing of Release 4

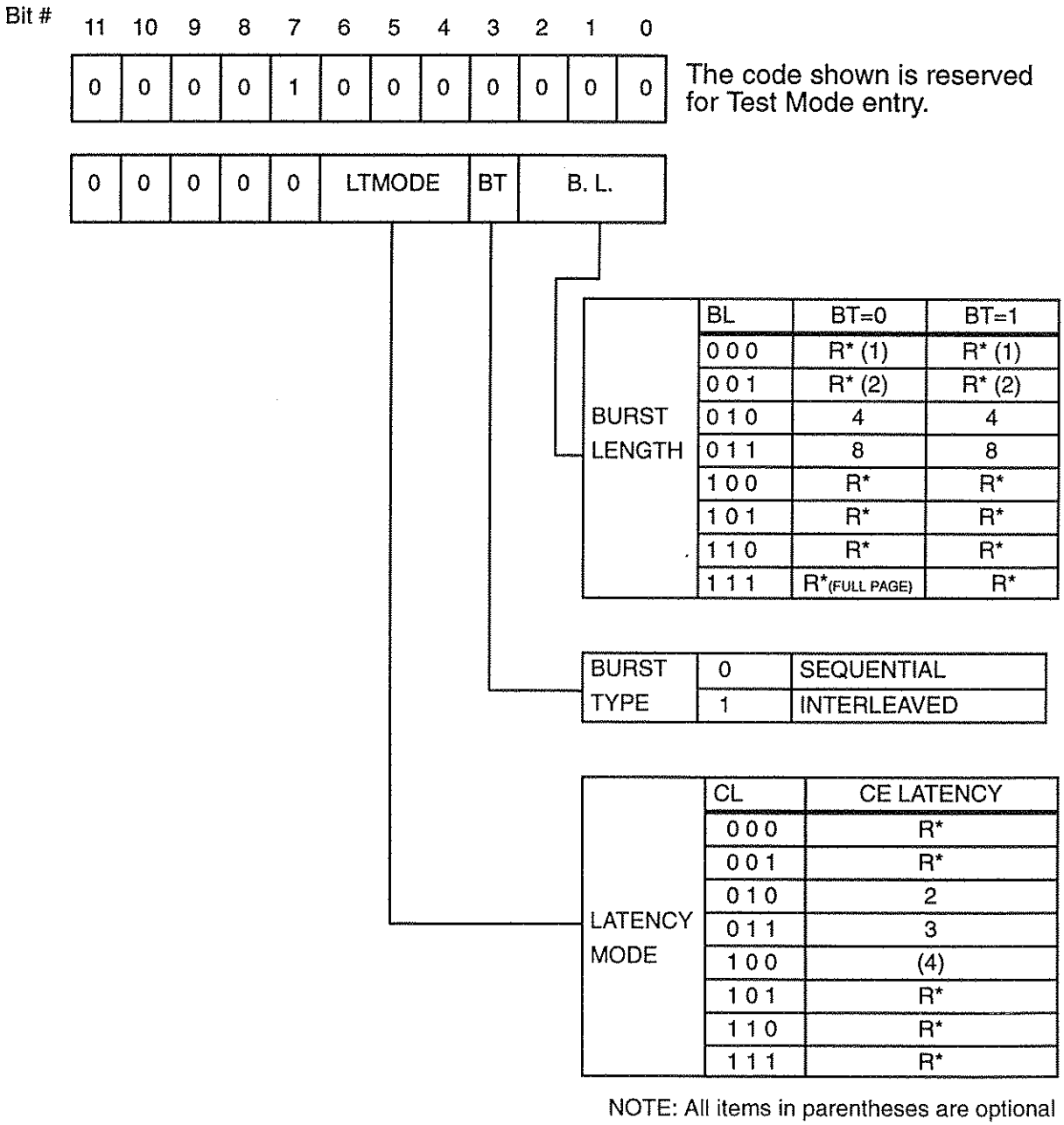
TABLE1 3.11.5–2

SDRAM FUNCTION TRUTH TABLE for CKE

SDRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM) chip. Its purpose is to store the mode–of–operation data. This data is written after power–on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{CE}$ Latency, and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode–Register–Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

SDRAM Mode Register architecture:



NOTE: All items in parentheses are optional

FIGURE 3.11.5–1
SDRAM MODE REGISTER ARCHITECTURE

3.11.5.4–Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High–Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High–Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μS.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

3.11.5.5–Auto Precharge

The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle. The following table defines the options available from AP during the column address portion of any cycle.

AP	Option
0	Do not auto precharge, leave bank active at end of burst.
1	Auto precharge bank specified by BA at end of burst.

The user must wait until the precharge is completed before issuing another command to the device. Timing for auto precharge is required to be the same as or less than the minimum requirement of external precharge.

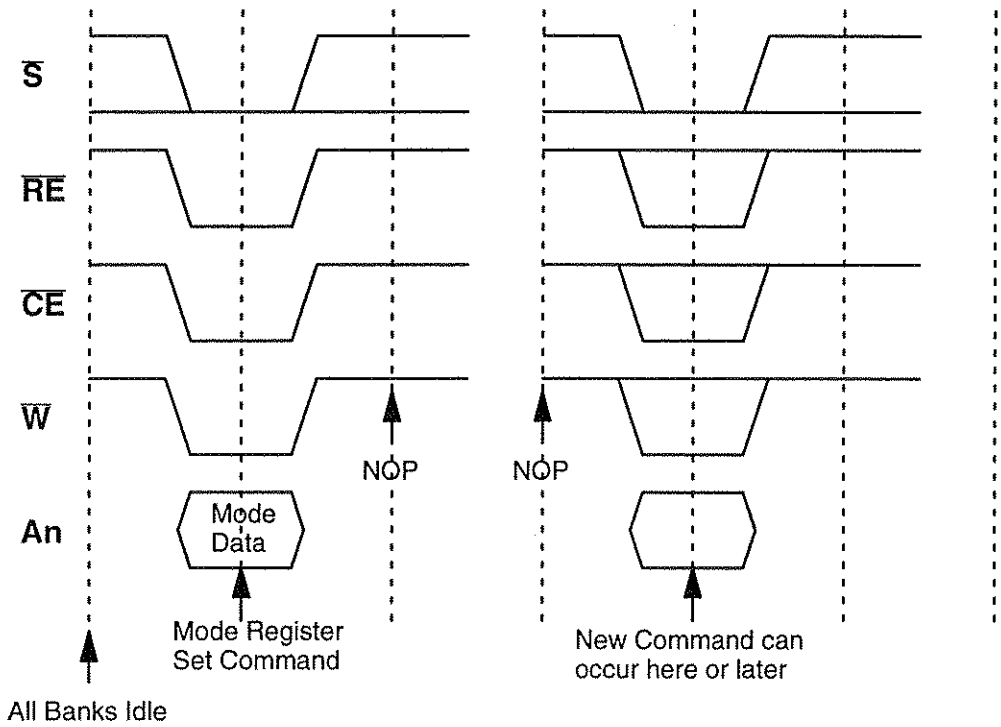
3.11.5.6–Precharge All Banks

The user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks. BA is used to specify the bank to be precharge, and AP is used to indicate the precharge option. The following table defines the options available from AP during the precharge cycle.

PA	Option
0	Precharge bank specified by BA
1	Precharge All banks

3.11.5.7–Mode Register Write Timing

The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.



Note: Clock Low–to–high transitions occur at the dotted lines.

4 MEMORY MODULES AND CARDS

The following standards for MODULES and CARDS were developed by Committee JC–42.5. In earlier releases of JESD 21–C, the individual standards were intermixed and appeared in one section, 4, in the order in which they were approved with no regard for the module structure or organization. In Release 7, the section has been reorganized and the individual standards grouped in sub–sections by the data word length. A separate section is included (4.1) for those standards that describe features that are generic in nature and independent of the module organization.

The standards establish pin assignments for a series of multi–chip modules. The package configurations and dimensions are as defined in JEDEC Publication 95. The modules will normally be made using surface mount devices described in section 3 of this standard. The initial standards were for DRAM modules, but the since the publication of Std. 21–B, a standard for a families of SRAM and non–volatile modules have been approved. In addition to the device standards, there is a standard that addresses special nomenclature related to the modules.

The sub–sections are as follows:

4.1 Module & Card Features
4.2 One Byte Modules
4.3 Two Byte Modules and Cards
4.4 Four Byte Modules and Cards
4.5 Eight Byte Modules
4.6 Sixteen Byte Modules

4.1 Module Features & Properties

The following standards are applicable to modules and cards without regard to the data word length except as where specifically indicated.

4.1.1 Memory Module Nomenclature

4.1.2 Memory Module Serial Presence Detect (SPD) General Standard

4.1.2.1 SPD Appendix A

4.1.2.2 SPD Appendix B

4.1.2.3 SPD Appendix C

4.1.2.4 SPD Appendix D

4.1.2.5 SPD Appendix E

4.1.2.6 SPD Appendix F

4.1.1 Memory Module Nomenclature

4.1.1.1 – Purpose

The purpose of this standard is to establish a format for a number system which defines the format of a number which is an architectural description of multi–chip memory modules. It is intended to be used with but not restricted to modules made with DRAM devices.

4.1.1.2 – Number Format

The description number designation shall consist of 8 fields with the form nnSccbbDttlpp where :
nn = the number of longitudinal positions on the module: 4, 5, 8, 9.
S = the number of sides on the module stated as "single or double" : S, D
cc = the capacity of the memory chip stated in terms of the log(2) of the capacity (i.e.–the number of address bits needed for the chip): 16, 18, 20, 22
bb = the number of data bits in the interface: 1, 2, 4, 5, 8, 9, 10, 17
D = the data interface configuration, common, separate, or mixed: C, S, M
tt = total number of words stated as log(2) of the capacity: 16—26
l = mechanical interface: P = pins, E = edge card connector
pp = number of pins or pads

4.1.1.3 – Number Example

A module with the following attributes:
9 chips long
Double sided
18 bit data interface
Separate I/O for parity bits, common I/O for other bits
1M X 1 memory chips
Pin interface
Architectural number: 9D2018M20P40

XILINX EXHIBIT 1010
Page 169

4.1.2 – SERIAL PRESENCE DETECT STANDARD, General Standard

Introduction: New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident; consequently, new memory technologies are being incorporated onto existing module form factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module form factor; hence the parallel Presence Detect method did not allow for these newer technologies. Given that memory modules do not regularly change form factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

1 **Scope:** This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g. Fast Page Mode DRAM), an appendix to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each appendix.

When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD Interface protocol (see section 2 herein)
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing
- Acceptable error checking schemes (ECC, Parity...)
- SPD Wiring diagram and pinout to module.

2 **Interface Protocol.** Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include IIC, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

3 **Data Order and PD Size:** This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technologies' PD bits are defined, then the entire address map for those SPDs must also be defined.

4 **SPD Data Types:** SPD data is stored in a non–volatile serial memory device. The different types of data include, but are not limited to:

- Look Up Table entries
- Binary data
- Optional data (Binary, ASCII, etc. data)
- Checksums

4.1 **Look Up Table (LUT) Entries:** Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g. fast page mode DRAM will have specific tables for tRAC, tCAC, # of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a look–up– table specified within an appendix within this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its appendices.

4.2 **Optional Data:** The current Jedec Standard allows for manufacturers to insert some of their own specific data into the SPD ROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

4.3 **Checksums:** In various cases, checksums are required. Checksum calculation method is currently being proposed at time of publication of this standard.

XILINX EXHIBIT 1010
Page 171

5 **SPD Content:** The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the following must be addressed in any SPD implementation:

Description	Data Type	Address Map Byte #
SPD size	LUT Entry	0
Total SPD memory size	LUT Entry	1
Fundamental memory type	LUT Entry, Appendix A	2
Definition of features specific to the fundamental memory	See pertinent appendix	3–31
(Optional) Superset memory type	See appendix B	32
(Optional) definition of features specific to the superset memory	See pertinent appendix	33–61
SPD Revision designator	LUT	62
Checksum for bytes 0–62	Checksum	63
Manufacturers Jedec ID code per JEP–106	LUT	64–71
Manufacturing location	Supplier Unique	72
Manufacturer's Part Number	Supplier Unique	73–90
Revision Code	Supplier Unique	91–92
Manufacturing date	BCD	93–94
Assembly Serial Number	Supplier Unique	95–98
Manufacturer Specific Data	Supplier Unique	99–125
Reserved	N/A	126–127
Open free–form area	Application Specific	128–255

Detailed descriptions follow in paragraphs 5.x

5.1 **Byte 0,** Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data:

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

5.2 **Byte 1, Total SPD Memory Size:** This field describes the total size of the serial memory (often an EEPROM) used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

5.3 **Byte 2,** Fundamental Memory Type: This field will identify the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in **appendix A** herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre–existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5) within this standard.

5.4 **Bytes 3–31:** Descriptions of Module Specific Features: Appendices to this standard detail the tables for the features specific to each of the fundamental memory types as described above. For example, see appendix C for details of SPD features for Fast Page Mode and Extended Data Out DRAM Modules.

5.5 **Byte 32:** Superset Memory Type: When a new technology is developed which is completely backward compatible to an already specified (fundamental) technology, then it may be considered a $Superset' technology. The benefits of specifying a technology as a superset are obvious; if a system is capable of operating in a $fundamental' mode only and a superset module is inserted, then the system can still use the module. The memory superset type or technology is specified in appendix B to this standard. Appendix B provides the decode of specific superset technologies. It references other appendices where the specific superset PDs are further detailed. As new supersets are created, appendices must also be added. Presence Detects for a superset technology are specified just as for any given fundamental technology except that any and all backward compatible fundamental technologies must be referenced.

5.6 **Bytes 33–63:** Superset Features: Appendices to this standard detail the tables for the features specific to each of the superset memory types as described above. A new appendix must be added to this standard detailing the PDs for that superset technology detailed in appendix B and represented in byte 32. Appendix B would identify the superset technology type and would also reference the appropriate appendix where the superset is detailed.

5.9.0 **Bytes 64–127:** Module manufacturers may include information which is pertinent to their particular modules. This information is detailed below in paragraph 5.9.X:

5.9.1 **Bytes 64–71**: Manufacturers Jedec ID code per JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FF indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes would be FFh.

5.9.2 **Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

XILINX EXHIBIT 1010
Page 173

5.9.3 **Bytes 73–90:** Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.9.4 **Bytes 91–92:** Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.9.5 **Bytes 93–94:** Date of Module Manufacture: The module manufacturer may include a date code for the module. If this is done, then specifically, byte 93 must contain the year in Binary and byte 94 must contain the week in Binary.

5.9.6 **Bytes 95–98:** Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.9.7 **Bytes 99–125:** Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.9.8 **Bytes 126–127:** Reserved. These bytes are reserved and cannot be later allocated.

5.10 **Bytes 128–255:** System Integrators specific information: The system integrator may choose to use the SPD ROM for various items. If so, then bytes 128–255 may be used.

XILINX EXHIBIT 1010
Page 174

4.1.2.1 – Appendix A: Table of Fundamental Memory Types:

This table is modified/appended whenever a new fundamental memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new fundamental type. The following table details the fundamental memory types.

Byte 2, Fundamental Memory Type: This field identifies the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in this Appendix herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre–existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5 of the General Standard) within this standard.

The fundamental memory types are identified as follows:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See Appndx
Reserved	0	0	0	0	0	0	0	0	N/A
Standard FPM DRAM	0	0	0	0	0	0	0	1	C
EDO	0	0	0	0	0	0	1	0	C
PNEDO									
	0	0	0	0	0	0	1	1	TBD
Sync Dram	0	0	0	0	0	1	0	0	E
Multiplexed ROM	0	0	0	0	0	1	0	1	F
TBD	0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	0	1	TBD
TBD	1	1	1	1	1	1	1	0	TBD
TBD									
	1	1	1	1	1	1	1	1	TBD

4.1.2.2 – Appendix B: Table(s) of Superset Memory Types:

This table is modified/appended whenever a new Superset memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new superset memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new superset type. The following table identifies the Superset memory types and their pertinent fundamental technologies.

The Superset memory types are identified as follows:

Superset Mem. Type Appndx	Fundamental memory type. (note 1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See
Reserved		0	0	0	0	0	0	0	0	N/A
TBD		0	0	0	0	0	0	0	1	TBD
TBD		0	0	0	0	0	0	1	0	TBD
TBD		0	0	0	0	0	0	1	1	TBD
TBD		0	0	0	0	0	1	0	0	TBD
TBD		0	0	0	0	0	1	0	1	TBD
TBD		0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
TBD		1	1	1	1	1	1	0	1	TBD
TBD		1	1	1	1	1	1	1	0	TBD
TBD		1	1	1	1	1	1	1	1	TBD

Note 1: The fully backward compatible Fundamental memory type must be referenced when a superset is specified.

4.1.2.3 – Appendix C: Specific PD's for Fast Page Mode or Extended Data Out DRAM.

1 **Introduction:** This appendix describes the Presence Detects for Fast Page Mode DRAM and Extended Data Out (EDO) DRAM Modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 **Address map:** The following is the SPD address map for FPM and EDO. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# DRAM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	RAS# access time of this assembly	4
10	CAS# access time of this assembly	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	DRAM width, Primary DRAM	
14	Error Checking DRAM data width	
15–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	6
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for FPM and EDO DRAM

2) This will be 256 bytes, represented as 08h. See below.

3) High order bit defines is assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)

4) From data sheet.

5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.

6) Per the JEDEC spec, these are optional.

2 **Bytes 0–2,** For Reference: Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in **appendix A** to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0,** From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1,** From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3 Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing Fast Page Mode and EDO DRAM technology. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 Byte #3, Number of ROW Addresses: This first field describes the number of Row Addresses in the DRAM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

4.2 **Byte #4, Number of COLUMNs Addresses:** This field describes the number of COLUMN addresses in the module's DRAM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte #5, Number of Banks:** This field describes the number of banks on the DRAM Module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 182

4.4 **Bytes 6 & 7,** Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
576	0000 0010	0100 0000

Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.1 **Byte 7, Module Data Width Continued:** This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 **Byte 8, Module Interface Levels:** This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL ! 5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 183

4.6 **Byte 9, RAS Access Time (tRAC):** This field describes the module's RAS access time:

RAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
50ns	0	0	1	1	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
60ns	0	0	1	1	1	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
70ns	0	1	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80ns	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.7 **Byte 10, CAS Access Time (tCAC):** This field describes the module's CAS access time:

CAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
10ns	0	0	0	0	1	0	1	0
11ns	0	0	0	0	1	0	1	1
12ns	0	0	0	0	1	1	0	0
13ns	0	0	0	0	1	1	0	1
14ns	0	0	0	0	1	1	1	0
15ns	0	0	0	0	1	1	1	1
16ns	0	0	0	1	0	0	0	0
17ns	0	0	0	1	0	0	0	1
18ns	0	0	0	1	0	0	1	0
19ns	0	0	0	1	0	0	1	1
20ns	0	0	0	1	0	1	0	0
21ns	0	0	0	1	0	1	0	1
22ns	0	0	0	1	0	1	1	0
23ns	0	0	0	1	0	1	1	1
24ns	0	0	0	1	1	0	0	0
25ns	0	0	0	1	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.8 **Byte 11, Module Configuration type:** This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 **Byte 12, Refresh Rate/Type:** This field describes the module's refresh rate and type:

Refresh Period	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 Byte 13, DRAM width, Primary DRAM: This field describes the width of the primary DRAMs used on the module. The primary DRAM is that which is used for data; examples of primary (data) DRAM widths are x4, x8, x16, x32. Note that if the module is made with DRAMs which provide extra bits for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using x72 modules include:

Module width	Primary Data DRAM Width	Error Checking DRAM Width	Qty Primary Data DRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x1	4	0001 0000

DRAM Width, Primary DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 Byte 14, Error Checking DRAM data width: If the module incorporates error checking and if the primary data DRAM does not include these bits; i.e. there are separate error checking DRAMs, then the error checking DRAM's width is expressed in this byte. Examples of error checking DRAM widths include x1, x4, x8. For Example:

Module width	Primary DRAM Width	Error Checking DRAM Width	Qty of Error Checking DRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x1	8	0000 0001

DRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.12 **Bytes 15–31:** Open. There are no defined PD settings for these bytes.

4.13 **Bytes 32 through 62, Superset information:** If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.14 **Byte 63, Checksum for bytes 0–62:** At time of the publish of this standard, the checksum method is currently in ballot and is not yet incorporated, suggested method is modulo 256.

5 **From the general SPD standard:** The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 **Bytes 64–71:** Manufacturers ID code per EIA/JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 **Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 **Bytes 73–90:** Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4: **Bytes 91–92:** Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 **Bytes 93–94:** Date of Module Manufacture: The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 **Bytes 95–98:** Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 **Bytes 99–125:** Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.8 **Bytes 126–127:** Reserved. These bytes are reserved and cannot be later allocated.

4.1.2.4 – Appendix D: Table not yet defined

Table D is not yet defined. It will be placed in this location when it is published.

4.1.2.5 – Appendix E: Specific PD's for Synchronous DRAM (SDRAM).

Date of last update: 11/25/96

1. **Introduction:** This appendix describes the Presence Detects for Synchronous DRAM Modules. These PD's are those referenced in the SPD standard document for "Specific Features". The following PD fields will occur, in the order presented, in table 1.1. Further descriptions of bytes 0 and 1 are found in the SPD standard. Further description of byte 2 is found in appendix A of the SPD standard.

1.1 **Address map:** The following is the SPD address map for SDRAM. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# Module Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	SDRAM Cycle time at Max. Supported CAS Latency (CL), CL=X	4
10	SDRAM Access from Clock	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	SDRAM width, Primary DRAM	
14	Error Checking SDRAM data width	
15	Minimum Clock Delay, Back to Back Random Column Addresses	
16	Burst Lengths Supported	
17	# Banks on Each SDRAM device	4
18	CAS# Latencies Supported	4
19	CS# Latency	4
20	Write Latency	4
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	
23–31	TBD	
32–62	Superset information	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106E	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	
126–127	Reserved	
128–255	Open for Customer use.	7

notes:

1) This will be programmed as 128 bytes for the 168 pin DIMM Module.
2) This must be programmed as 256 bytes, 256 byte EEPROM's will be used for SPD on 168 pin SDRAM DIMMs.
3) High order bit defines if assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)
4) From data sheet.
5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.
6) The JEDEC spec specifies that these bytes are optional.
7) Module suppliers will need to assure that these bytes are open for reads/writes by Customer.

Release 7

2 **For Reference, Bytes 1–3:** Descriptions of bytes 1 and 2 can be found in the main body of the SPD standard, and byte 3 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0:** From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1:** From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
SDRAM	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3. Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4. The following PD bytes are those specific to modules implementing Synchronous DRAM technology. Note that these full descriptions start at byte 3 below and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology

4.1 Byte 3: Number of ROW Addresses: This first field describes the number of row Addresses in the SDRAM array. This does not include the Bank Select pin. For example, the number of Row Addresses used on a 2MX64 SDRAM DIMM is

Decimal 11 Binary 0000 1011 Addresses (for RA0 through RA10):

No. of Row Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
14(redundant)	1	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

XILINX EXHIBIT 1010
Page 193

4.2 **Byte 4: Number of COLUMN Addresses:** This field describes the number of COLUMN Addresses in the module's SDRAM array:

Number of Columns	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte 5: Number of Banks on module:** This field describes the number of physical banks on the SDRAM Module. This is not to be confused with the number of logical banks on a given SDRAM device :

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 194

4.4 Bytes 6 & 7, Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte 7. Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 Byte 8, Module Interface Levels: This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 195

4.6 **Byte 9, SDRAM Cycle time (tCYC):** This byte defines the minimum cycle time for the SDRAM Module at the highest CAS Latency, CAS Latency=X, defined in byte 18. If other CAS latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate cycletimes at lower CAS Latencies. Byte 9, Cycle time for CAS Latency = X, is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are	and bits 3:0 are	then the cycle time is
1010	0101	
(10ns) +	(0.5ns)	= 10.5ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Cycle Time Subfield A:								
Units of nanoseconds (bits 4 through 7)					SEE Subfield Table B			
Undefined	0	0	0	0				
1ns/16ns	0	0	0	1				
2ns	0	0	1	0				
3ns	0	0	1	1				
4ns	0	1	0	0				
5ns	0	1	0	1				
6ns	0	1	1	0				
7ns	0	1	1	1				
8ns	1	0	0	0				
9ns	1	0	0	1				
10ns	1	0	1	0				
11ns	1	0	1	1				
12ns	1	1	0	0				
13ns	1	1	0	1				
14ns	1	1	1	0				
15ns	1	1	1	1				
SDRAM Cycle Time Subfield B:								
Tenths of ns (bits 0 through 3)	SEE Subfield table A							
+0ns					0	0	0	0
+0.1ns					0	0	0	1
+0.2ns					0	0	1	0
+0.3ns					0	0	1	1
+0.4ns					0	1	0	0
+0.5ns 1						0	1	0
+0.6ns					0	1	1	0
+0.7ns					0	1	1	1
+0.8ns					1	0	0	0
+0.9ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 196

4.7 Byte 10, SDRAM Access time from Clock (tAC): This byte defines the maximum clock to data out for the module. This is the Clock to data out specification at the highest given CAS Latency specified/depicted in byte 18 of this SPD specification/ standard. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate tAC's at lower CAS Latencies. The byte is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are 1001 (9ns) + and bits 3:0 are 0000 (0.0ns) = then the cycle time is 9.0ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Access time from Clock:								
Subfield A: Units of nanoseconds (bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1ns	0	0	0	1				
2ns	0	0	1	0				
3ns	0	0	1	1				
4ns	0	1	0	0				
5ns	0	1	0	1				
6ns	0	1	1	0				
7ns	0	1	1	1				
8ns	1	0	0	0				
9ns	1	0	0	1				
10ns	1	0	1	0				
11ns	1	0	1	1				
12ns	1	1	0	0				
13ns	1	1	0	1				
14ns	1	1	1	0				
15ns	1	1	1	1				
SDRAM Access time from CLK								
Subfield B: Tenths of ns (bits 0 through 3)								
+0ns	SEE Subfield Table A				0	0	0	0
+0.1ns					0	0	0	1
+0.2ns					0	0	1	0
+0.3ns					0	0	1	1
+0.4ns					0	1	0	0
+0.5ns					0	1	0	1
+0.6ns					0	1	1	0
+0.7ns					0	1	1	1
+0.8ns					1	0	0	0
+0.9ns					1	0	0	1
RFU					1	0	1	0
.					.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.8 Byte 11, Module Configuration type: This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 197

4.9 **Byte 12, Refresh Rate/Type:** This field describes the module's refresh rate and type:

Refresh Period Bit 0	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 **Byte 13, SDRAM width, Primary SDRAM:** This field describes the width of the primary SDRAMs used on the module. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, x32. Note that if the module is made with SDRAMs which provide for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using (1 bank) x72 modules include:

Module width	Primary Data SDRAM Width	Error Checking SDRAM Width	Qty Primary Data SDRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x4	4	0001 0000

SDRAM Width, Primary SDRAM Bit 0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 Byte 14, Error Checking SDRAM data width: If the module incorporates error checking and if the primary data SDRAM does not include these bits; i.e. there are separate error checking SDRAMs, then the error checking SDRAM's width is expressed in this byte. Examples of error checking SDRAM widths include x4, x8, x16. For Example:

Module width	Primary SDRAM Width	Error Checking SDRAM Width	Qty of Error Checking SDRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x4	8	0000 0100

SDRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.12 Byte 15, as determined by the limiting part on the assembly, SDRAM Device Attributes: Minimum Clock Delay, Back to Back Random Column Accesses. Note that SDRAM architecture can be gained with this parameter. A latency of 1 for random writes denotes Pipelined SDRAM and a latency of 2 for random writes denotes Prefetch SDRAMs:

Number of Clocks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
.	.					.		
255	1	1	1	1	1	1	1	1

4.13 Byte 16, SDRAM Device Attributes, Burst Lengths Supported: This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is "1", then that Burst Length is supported on the module; If the bit is "0", then that burst length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

4.14 Byte 17, SDRAM Device Attributes, Number of Banks on the discrete SDRAM Device: This byte details how many banks are on each discrete SDRAM installed onto the module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
.	.					.		
255	1	1	1	1	1	1	1	1

4.15 **Byte 18, SDRAM Device Attributes, CAS# Latency:** This byte describes which of the programmable CAS# Latencies are supported by the Module. If the bit is "1", then that CAS# Latency is supported on the module; If the bit is "0", then that CAS# Latency is not supported by the module. Bytes 9,10,23–26 all relate CAS Latency dependent timings.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CAS# Latency = 7	CAS# Latency = 6	CAS# Latency = 5	CAS# Latency = 4	CAS# Latency = 3	CAS# Latency = 2	CAS# Latency = 1
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.16 **Byte 19, SDRAM Device Attributes, CS# Latency:** This byte describes which of the programmable CS# Latencies are acceptable for the Module. If the bit is "1", then that CS# Latency is supported on the module; If the bit is "0", then that CS# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CS# Latency = 6	CS# Latency = 5	CS# Latency = 4	CS# Latency = 3	CS# Latency = 2	CS# Latency = 1	CS# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.17 **Byte 20, SDRAM Device Attributes, WE# Latency:** This byte describes which of the programmable WE# Latencies are acceptable for the Module. If the bit is "1", then that WE# Latency is supported on the module; If the bit is "0", then that WE# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	WE# Latency = 6	WE# Latency = 5	WE# Latency = 4	WE# Latency = 3	WE# Latency = 2	WE# Latency = 1	WE# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.18 **Byte 21, SDRAM Module Attributes:** This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, then the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On–Card PLL (Clock)	*Registered Address/Control Inputs	*Buffered Address/Control Inputs
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

* Address, RAS, CAS, WE, CKE, CS

4.19 **Byte 22, SDRAM Device Attributes, General:** This byte depicts various aspects of the SDRAMs on the module. It details various unrelated but critical elements pertinent to the SDRAMs. A given SDRAM characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, then the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	Supports Write1/Read Burst	Supports Precharge All	Supports Auto–Precharge	Supports Early RAS# Precharge
0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

4.1.2.6 – Appendix F: Specific PD's for Address Multiplexed ROMs (MXROM).

1.0 Introduction: This appendix describes the Presence Detects for Multiplexed ROM modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 Address map: The following is the SPD address map for Multiplexed ROM. It describes where the individual LUT–Entries/ bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	
4	# Column Addresses on this assembly	
5	# ROM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	Address Access Time of this assembly$	3
10	$Address Access Time continuation	3
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Reserved	
13	Page Mode Access Time of this assembly	3
14	Output Enable Access Time of this assembly	3
15	Chip Enable Access Time of this assembly$	3
16	$Chip Enable Access Time continuation	3
17	Burst Length of this assembly	
18–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	4
72	Manufacturing location	4
73–90	Manufacturer's Part Number	4
91–92	Revision Code	4
93–94	Manufacturing date	4
95–98	Assembly Serial Number	4
99–125	Manufacturer Specific Data	4
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for Multiplexed ROM assemblies.
2) This will be 256 bytes, represented as 08h. See below.
3) From data sheet.
4) Per the JEDEC spec, these are optional.

2 **Bytes #0–2, For Reference:** Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE #0, From General SPD Standard, Number of Bytes used by Module Manufacturer:** This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte #1, From General SPD Standard, Total SPD Memory Size:** This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 **Byte #2, From Appendix A, Memory Type:** This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
Multiplexed ROM	0	0	0	0	0	1	0	1

3 **Data Type(s):** Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing ROM devices with a multiplexed address interface. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 **Byte #3, Number of ROW Addresses:** This first field describes the number of Row Addresses in the ROM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 203

4.2 **Byte #4, Number of COLUMN Addresses:** This field describes the number of COLUMN addresses in the module's ROM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte #5, Number of Banks:** This field describes the number of banks on the ROM Module.

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

XILINX EXHIBIT 1010
Page 204

4.4 Bytes 6 & 7, Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte #7, Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 Byte #8, Module Interface Levels: This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6 **Bytes #9 & #10, Address Access Time (t_{AA}):** Bytes 9 and 10 are used to designate the address access time of the module. This access time is presented as a 16 bit word; bit 0 of byte 9 becomes the LSB of the 16 bit access time identifier and bit 7 of byte 10 becomes the MSB. Consequently, if the module has an address access time of less than 256ns, byte 10 will have a value of 00h. If the address access time is 256ns or greater, byte 10 is used in conjunction with byte 9 to designate the total access time.

4.6.1 **Byte 9:**

Address Access Time (LSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 (+x0A) ns	0	0	0	0	0	0	0	1
2 (+x0A) ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
254 (+x0A) ns	1	1	1	1	1	1	0	1
255 (+x0A) ns	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6.2 **Byte #10, Address Access Time Continued:** This byte will be left at 00h if the address access time of the module is less than 256 nanoseconds. If the address access time of the module is 256 nanoseconds or greater, byte 10 is used in conjunction with byte 9 to determine the access time of the assembly.

Address Access Time (MSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (+x09) ns	0	0	0	0	0	0	0	0
256 (+x09) ns	0	0	0	0	0	0	0	1
512 (+x09) ns	0	0	0	0	0	0	1	0
1024 (+x09) ns	0	0	0	0	0	0	1	1
2048 (+x09) ns	0	0	0	0	0	1	0	0
4096 (+x09) ns	0	0	0	0	0	1	0	1
8192 (+x09) ns	0	0	0	0	0	1	1	0
16384 (+x09) ns	0	0	0	0	0	1	1	1
–	–	–	–	–	–	–	–	–

4.7 **Byte #11, Module Configuration type:** This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.8 **Byte #12, Reserved:** This byte is reserved for future offerings.

XILINX EXHIBIT 1010
Page 206

4.9 Byte #13, Page Mode Access Time (t_{PA}): Byte 13 represents the page mode access time from chip enable of the device (t_{PA}) in nanoseconds.

Page Mode Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 ns	0	0	0	0	0	0	0	1
2 ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
253 ns	1	1	1	1	1	1	0	1
254 ns	1	1	1	1	1	1	1	0
New Table	1	1	1	1	1	1	1	1

4.10 Byte #14, Output Enable Access Time (t_{OE}): Byte x14 represents the access time from output enable of the device (t_{OE}) in nanoseconds.

Output Enable Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 ns	0	0	0	0	0	0	0	1
2 ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
253 ns	1	1	1	1	1	1	0	1
254 ns	1	1	1	1	1	1	1	0
New Table	1	1	1	1	1	1	1	1

4.11 Bytes #15 & #16, Chip Enable Access Time (t_{OE}): Bytes 15 and 16 are used to designate the access time from chip enable of the module. This access time is presented as a 16 bit word; bit 0 of byte 15 becomes the LSB of the 16 bit access time identifier and bit 7 of byte 16 becomes the MSB. Consequently, if the module has a chip enable access time of less than 256ns, byte 16 will have a value of 00h. If the chip enable access time is 256ns or greater, byte 16 is used in conjunction with byte 15 to designate the total chip enable access time.

4.11.1 Byte #15:

Chip Enable Access Time (LSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 (+x0F) ns	0	0	0	0	0	0	0	1
2 (+x0F) ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
254 (+x0F) ns	1	1	1	1	1	1	0	1
255 (+x0F) ns	1	1	1	1	1	1	1	1

4.11.2 Byte #16, Chip Enable Access Time Continued: This byte will be left at 00h if the chip enable access time of the module is less than 256 nanoseconds. If the chip enable access time of the module is 256 nanoseconds or greater, byte 16 is used in conjunction with byte 15 to determine the chip enable access time of the assembly.

Chip Enable Access Time (MSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (+x0F) ns	0	0	0	0	0	0	0	0
256 (+x0F) ns	0	0	0	0	0	0	0	1
512 (+x0F) ns	0	0	0	0	0	0	1	0
1024 (+x0F) ns	0	0	0	0	0	0	1	1
2048 (+x0F) ns	0	0	0	0	0	1	0	0
4096 (+x0F) ns	0	0	0	0	0	1	0	1
8192 (+x0F) ns	0	0	0	0	0	1	1	0
16384 (+x0F) ns	0	0	0	0	0	1	1	1
–	–	–	–	–	–	–	–	–

4.12 **Byte #17, Burst Length:** Byte 17 is an 8 bit mask which indicates all burst lengths supported by the device. If a bit in byte 17 is "1" then the associated burst length is supported by the module. If the bit is "0", then that burst length is not supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length 8	Burst Length 4	Burst Length 2	Burst Length 1
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.13 **Bytes 18–31:** Open. There are no defined PD settings for these bytes.

4.14 **Bytes 32 through 62, Superset information:** If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.15 **Byte 63, Checksum for bytes 0–62:** At time of the publish of this standard, the checksum method is currently in ballot and is not yet incorporated, suggested method is modulo 256.

5 **From the general SPD standard:** The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 **Bytes 64–71, Manufacturers ID code per EIA/JEP106.** Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 **Byte 72, Manufacturing Location.** Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 **Bytes 73–90, Manufacturer's Part Number:** Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4 **Bytes 91–92, Revision Code:** This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 **Bytes 93–94, Date of Module Manufacture:** The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 **Bytes 95–98, Module Serial Number:** The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 **Bytes 99–125, Manufacturers specific data, open area:** The module manufacturer may add any additional information desired into the module within these locations.

5.8 **Bytes 126–127, Reserved:** These bytes are reserved and cannot be later allocated.

XILINX EXHIBIT 1010
Page 208

4.2 One Byte Memory Modules

4.2.1 – 22 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K WORDS OF 4 BITS
CONFIGURATION—SINGLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—22 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 24 PIN SIP/SIMM DRAM MODULE

CAPACITY—128K, 512K WORDS OF 4 BITS
CONFIGURATION—DOUBLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—24 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 30 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K, 1M, 4M WORDS OF 8 OR 9 BITS, & 16M WORDS OF 8 BITS
CONFIGURATION—SINGLE SIDED MODULE
—USING 64K, 256K, 1M, 4M, OR 16M MEMORY DEVICES
LOGIC FEATURES—Some of the modules contain a "presence detect" feature which conists of outputs that supply an encoded value which defines the storage capacity of the module.
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

4.2.2 – 30 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 8M WORDS OF 4 OR 5 BITS
—128K TO 16M WORDS OF 2 BITS
—256K TO 32M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENT Fig. 4.2–2

4.2.3 – 23/25/26/28 PIN ZIP/SIMM DRAM MODULE FAMILY

CAPACITY —256K TO 16M WORDS OF 4 BIT
—1M TO 64M WORDS OF 1 BIT
CONFIGURATION—DOUBLE SIDED, USING 1M, 4M, 16M, OR 64M DEVICES
PACKAGE—THE X4 MODULES, 26 PIN ZIP/SIP MODULE
THE X1 MODULES, 23 PIN ZIP/SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–3
NOTE: At the highest density using 64M memory devices, the modules must be expanded to 25 or 28 pins to provide the needed addresses. These modules will be defined in more detail when the packages for the 64M memory devices have been defined.

4.2.4 – 60 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 4 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 8, 128K, 512K, OR 2M BY 4
PACKAGE—60 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–4

– 70 PIN ZIP/SIMM SRAM MODULE

CAPACITY—64K, 256K, 1M WORDS OF 9 BITS
CONFIGURATION—SINGLE BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 9
LOGIC FEATURE—SEPARATELY CONTROLLABLE BIT FOR USE AS PARITY BIT
PACKAGE—70 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–5

PHYSICAL CONFIGURATION	4 DEVICES LONG				8 OR 9 DEVICES LONG			
	SINGLE BANK		DOUBLE BANK		SINGLE BANK			DOUBLE BANK
VERSION	N X 4	@ 4N X 1	2N X 4	N X 8	* N X 8(9)	* N X 8(9)	16M X 8	* 2N X 8(9)
[1] 1	$ A8	VSS	** NC	% NC	VDD	VDD	VDD	VDD
[2] 2	VDD	VDD	A8	A8	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
[3] 3	D0	$\overline{RE0}$	VDD	VDD	DQ0	DQ0	DQ0	DQ0
[4] 4	Q0	Q	D0	DQ0	A0	A0	A0	A0
[5] 5	$\overline{CE}$	A3	Q0	DQ1	A1	A1	A1	A1
[6] 6	A7	A6	$\overline{CE}$	$\overline{CE}$	DQ1	DQ1	DQ1	DQ1
[7] 7	A5	D	A7	A7	A2	A2	A2	A2
[8] 8	A4	$\overline{W}$	A5	A5	A3	A3	A3	A3
[9] 9	D1	$\overline{RE1}$	A4	A4	VSS	VSS	VSS	VSS
[10] 10	Q1	A0	D1	DQ2	DQ2	DQ2	DQ2	DQ2
[11] 11	$\overline{W}$	A7	Q1	DQ3	A4	A4	A4	A4
[12] 12	A1	A8	$\overline{W}$	$\overline{W}$	A5	A5	A5	A5
[13] 13	A3	$\overline{CE}$	A1	A1	DQ3	DQ3	DQ3	DQ3
[14] 14	A6	$\overline{RE2}$	A3	A3	A6	A6	A6	A6
[15] 15	Q2	A2	A6	A6	A7	A7	A7	A7
[16] 16	D3	A1	Q2	DQ4	DQ4	DQ4	DQ4	DQ4
[17] 17	A2	@ A9	D2	DQ5	A8	A8	A8	A8
[18] 18	A0	A4	A2	A2	* A9	* A9	A9	* A9
[19] 19	$\overline{RE}$	$\overline{RE3}$	A0	A0	* A10	NC	A10	$\overline{RE2}$
[20] 20	D3	A5	$\overline{RE1}$	$\overline{RE}$	DQ5	DQ5	DQ5	DQ5
[21] 21	Q0	VDD	D3	DQ6	$\overline{W}$	$\overline{W}$	$\overline{W}$	$\overline{W}$
[22] 22	VSS	VSS	Q3	DQ7	VSS	VSS	VSS	VSS
[23] 23			VSS	VSS	DQ6	DQ6	DQ6	DQ6
[24] 24			*** $\overline{RE2}$	NC	# NC ·	PD1	A11	PD1
[25] 25					DQ7	DQ7	DQ7	DQ7
[26] 26					Q8	PD2	NC	PD2
[27] 27					$\overline{RE}$	$\overline{RE}$	$\overline{RE}$	$\overline{RE1}$
[28] 28					$\overline{CE8}$	NC	NC	NC
[29] 29					D8	DQ8	NC	DQ8
[30] 30					VDD	VDD	VDD	VDD

TOP VIEW

* ON THE 30 PIN MODULE, 1M & 4M DEVICES MAY BE USED. PINS 18 & 19 ARE USED TO PROVIDE ADDRESS EXPANSION. THE OTHER MODULES WILL ACCOMIDATE 64K & 256K DEVICES ONLY.

** OPTIONAL VSS

*** NC FOR SINGLE BANK VERSION

$ OPTIONAL VSS WHEN A8 NOT NEEDED

OPTIONAL REFRESH (F) FUNCTION

@ ON THE 22 PIN 4N X 1 MODULE, 1 MB & 4 MB DEVICES MAY BE USED. PIN 17 IS USED FOR ADDRESS EXPANSION

% POTENTIAL VSS

PRESENCE DETECT TRUTH TABLE			
SIZE	256K	512K	1M
PIN			
PD1	L	H	L
PD2	H	L	L

CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED.

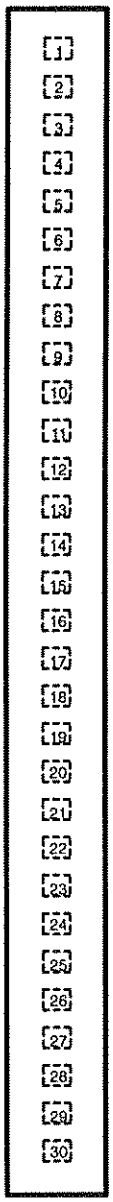
VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

FIGURE 4.2–1

22, 24,& 30 PIN DRAM MODULES

XILINX EXHIBIT 1010
Page 211

PHYSICAL CONFIGURATION	4 OR 5 DEVICES LONG SINGLE SIDED			4 OR 5 DEVICES LONG DOUBLE SIDED		
VERSION	N X 4(5)	2N X 2	4N X 1	2N X 4(5)	4N X 2	8N X 1
1	VDD					
2	D4	NC	NC	D4	NC	NC
3	Q4	NC	NC	Q4	NC	NC
4	A8					
5	A9					
6	*A10					
7	D3	D1	NC	D3	D1	NC
8	Q3	Q1	NC	Q3	Q1	NC
9	VSS					
10	A6					
11	A7					
12	A2					
13	A1					
14	D2	NC	D	D2	NC	D
15	Q2	NC	Q	Q2	NC	Q
16	A4					
17	A5					
18	A3					
19	A0					
20	D1	D0	NC	D1	D0	NC
21	Q1	Q0	NC	Q1	Q0	NC
22	VSS					
23	$\overline{W}$					
24	$\overline{CE}$	$\overline{CE1}$				
25	NC	$\overline{CE2}$				
26	$\overline{RE}$			$\overline{RE1}$		
27	NC	NC	NC	$\overline{RE2}$		
28	D0	NC	$\overline{CE3}$	D0	NC	$\overline{CE3}$
29	Q0	NC	$\overline{CE4}$	Q0	NC	$\overline{CE4}$
30	VDD					



30 PIN SIP MODULE TOP VIEW

* PIN 6 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

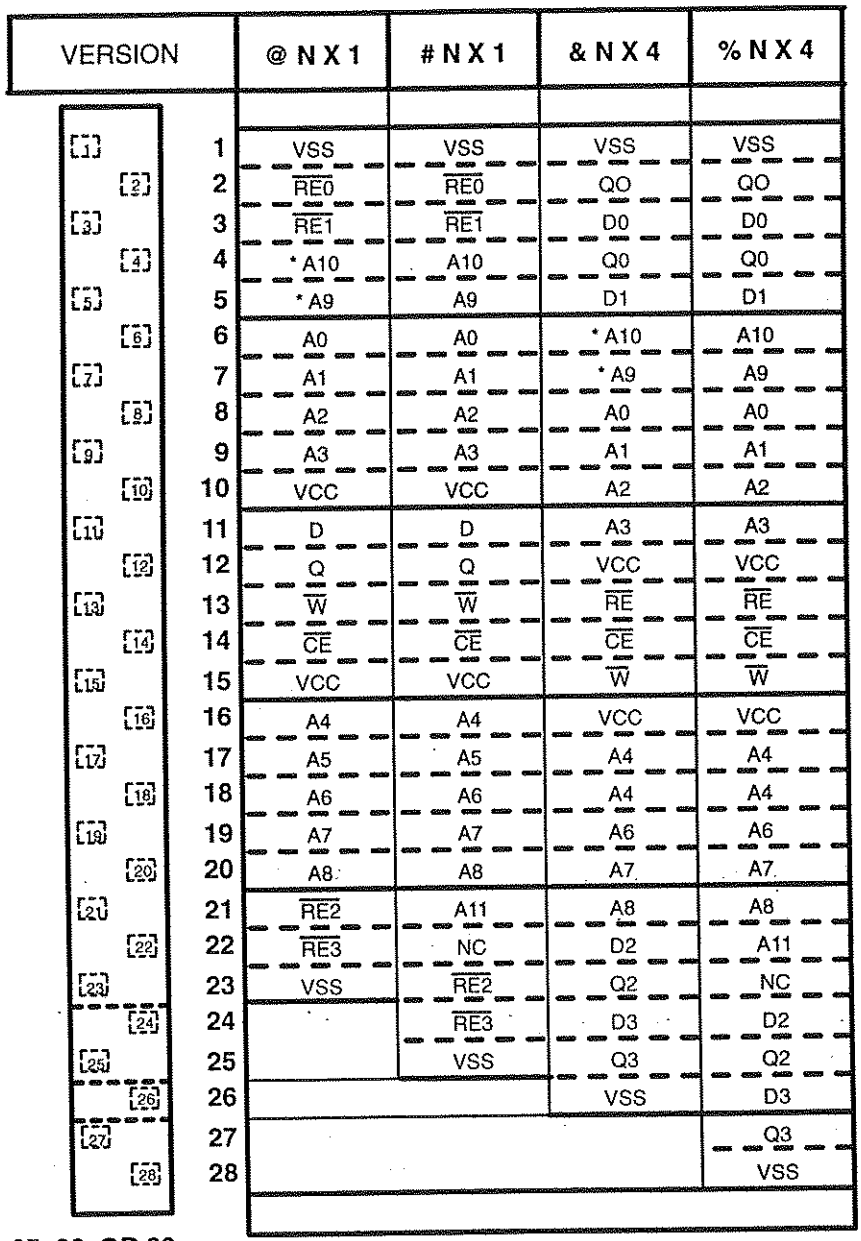
CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEFICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED

MEMORY DEVICES WITH A CAPACITY OF UP TO 4Mb BY 1 CAN BE ACCOMIDATED ON THE MODULES DEFINED IN THIS STANDARD

FIGURE 4.2–2

30 PIN DRAM MODULE FAMILY



VERSION	@ N X 1	# N X 1	& N X 4	% N X 4
1	VSS	VSS	VSS	VSS
2	$\overline{RE0}$	$\overline{RE0}$	QO	QO
3	$\overline{RE1}$	$\overline{RE1}$	D0	D0
4	* A10	A10	Q0	Q0
5	* A9	A9	D1	D1
6	A0	A0	* A10	A10
7	A1	A1	* A9	A9
8	A2	A2	A0	A0
9	A3	A3	A1	A1
10	VCC	VCC	A2	A2
11	D	D	A3	A3
12	Q	Q	VCC	VCC
13	$\overline{W}$	$\overline{W}$	$\overline{RE}$	$\overline{RE}$
14	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
15	VCC	VCC	$\overline{W}$	$\overline{W}$
16	A4	A4	VCC	VCC
17	A5	A5	A4	A4
18	A6	A6	A4	A4
19	A7	A7	A6	A6
20	A8	A8	A7	A7
21	$\overline{RE2}$	A11	A8	A8
22	$\overline{RE3}$	NC	D2	A11
23	VSS	$\overline{RE2}$	Q2	NC
24		$\overline{RE3}$	D3	D2
25		VSS	Q3	Q2
26			VSS	D3
27				Q3
28				VSS

23, 25, 26, OR 28 PIN ZIP SIMM TOP VIEW

N = THE ADDRESS CAPACITY OF THE MEMORY DEVICE USED

@ THIS CONFIGURATION IS APPLICABLE TO 1M, 4M, & 16M X 1 DEVICES.

THIS CONFIGURATION IS APPLICABLE TO A 64M X 1 DEVICE

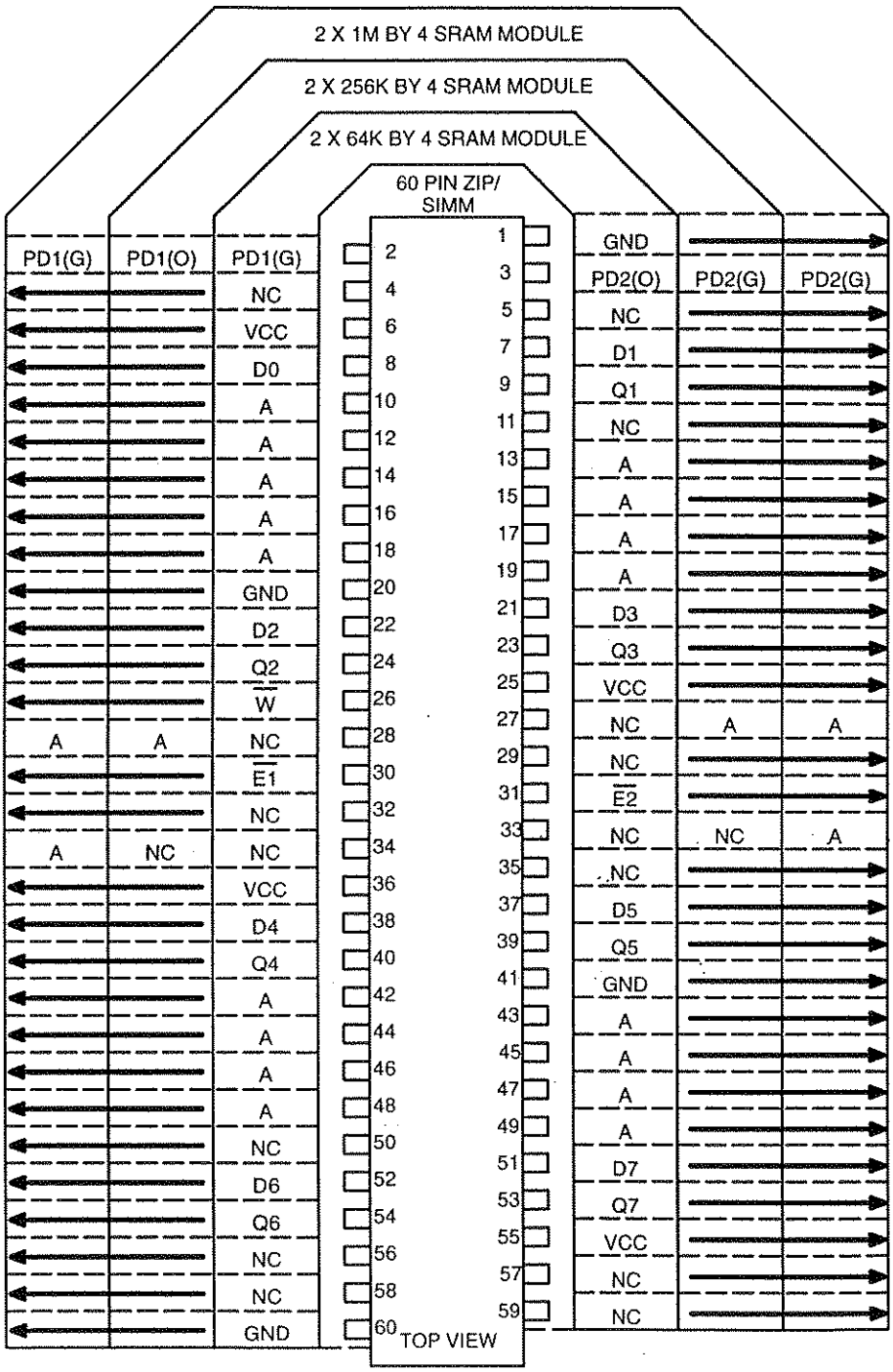
& THIS CONFIGURATION IS APPLICABLE TO 256K, 1M, & 4M X 4 DEVICES.

% THIS CONFIGURATION IS APPLICABLE TO A 16M X 4 DEVICE

* THESE ADDRESS PINS ARE NC WHEN NOT NEEDED FOR THE MEMORY DEVICE USED.

FIGURE 4.2–3

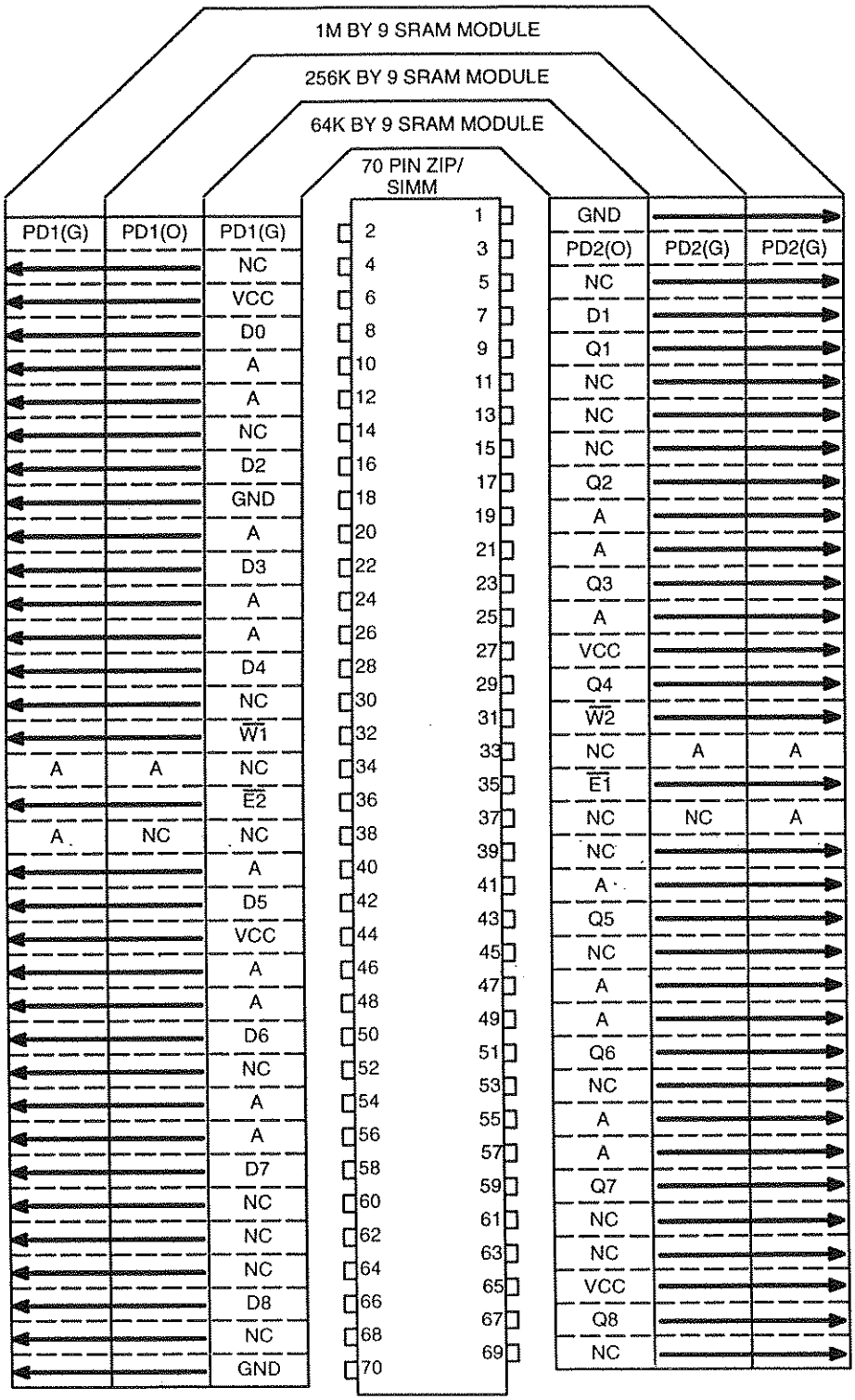
23/25/26/28 PIN DRAM MODULE FAMILY



The PD(n) pins are connected to GND (G) or left open (O).

E1 ENABLES Q0, Q2, Q4, & Q6
E2 ENABLES Q1, Q3, Q5, & Q7

FIGURE 4.2–4
2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY



The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q1, Q2, Q3, Q5, Q6, Q7, Q8
E2 & W2 CONTROL Q4

FIGURE 4.2–5

64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY

4.3 Two Byte Modules & Cards

4.3.1 – 76 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 9 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 18
128K, 512K, OR 2M BY 9
LOGIC FEATURE—2 SEPARATELY CONTROLLABLE BITS FOR USE AS PARITY BITS
PACKAGE—76 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.3–1

4.3.2 – 40 PIN SIP/SIMM DRAM MODULE FAMILY

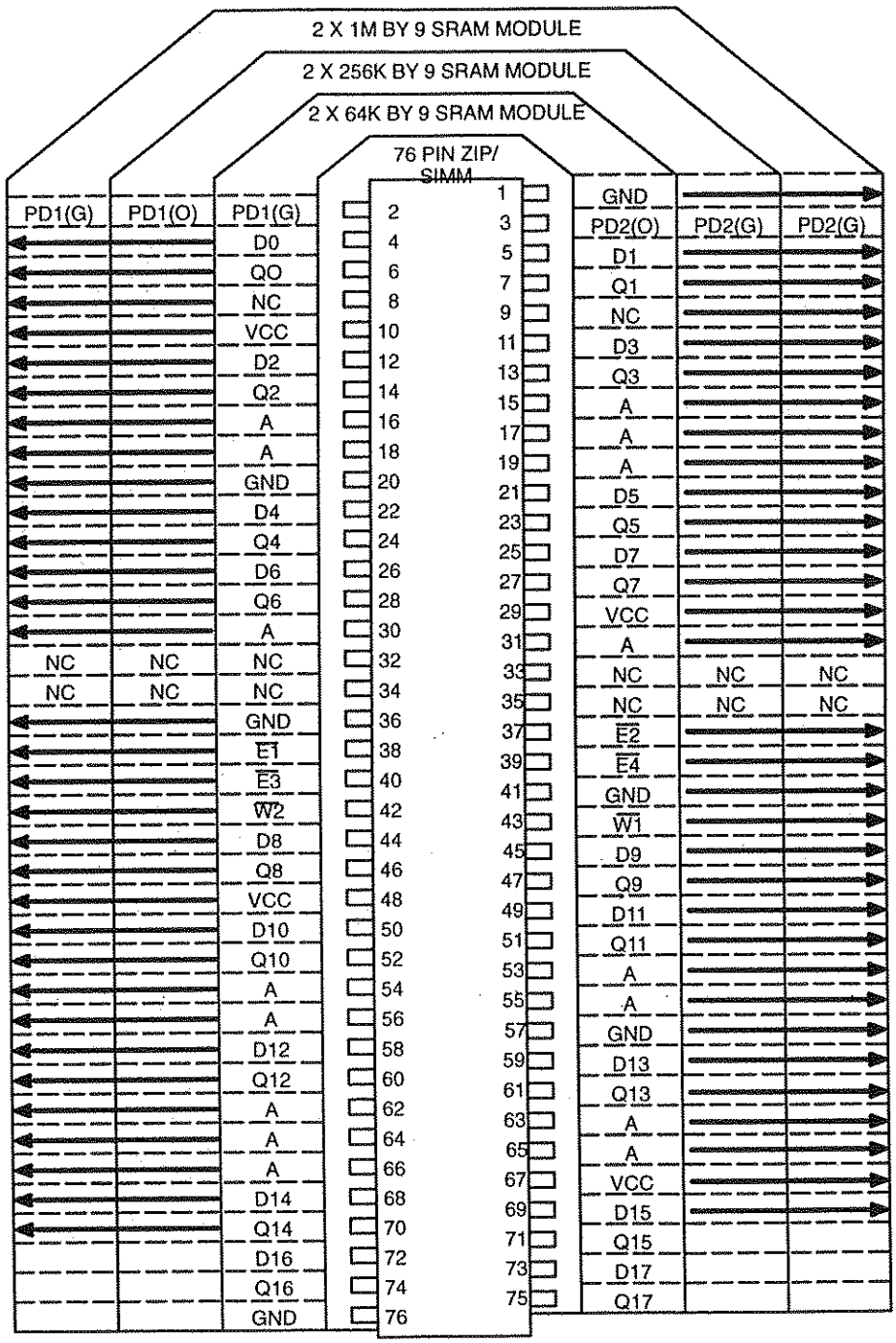
CAPACITY —64K TO 4M WORDS OF 16 OR 18 BITS
—64K TO 8M WORDS OF 8 OR 9 BITS
—128K TO 16M WORDS OF 4 BITS
—256K TO 32M WORDS OF 2 BITS
—512K TO 64M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
PACKAGE—40 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.3–2

4.3.3 – 60 PIN DRAM CARD FAMILY

CAPACITY—512K, 1M, 2M, 4M, & 8M WORDS OF 16 OR 18 BITS
CONFIGURATION—SEVEN DIFFERENT CONFIGURATIONS
—USING 1Mb & 4Mb DEVICES AND WITH 1, 2, OR 4 RE CLOCKS.
LOGIC FEATURES, The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—60 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3–3A
CONFIGURATION BLOCK DIAGRAMS—Fig. 4.3–3B

4.3.4 – 68 PIN MULTIPLE TECHNOLOGY MEMORY CARD FAMILY

CAPACITY—UP TO 32M WORDS OF 16 BITS
CONFIGURATION—ONE BASIC CONFIGURATION that allows the use of SRAM, EEPROM, EPROM, or ROM memory devices with software or firmware control to accomidate the device characteristic differences.
LOGIC FEATURES,
—The card contains an internal MEMORY called the "ATTRIBUTE MEMORY"; the contents describe the hardware and software characteristics, and use of the card.
— The card contains a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—68 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3–4A
MEMORY CARD OPERATION TRUTH TABLE— Page 4.3–4B
MEMORY CARD SPECIFIC TERMINOLOGY— Sec. 2.8, Page 2–13

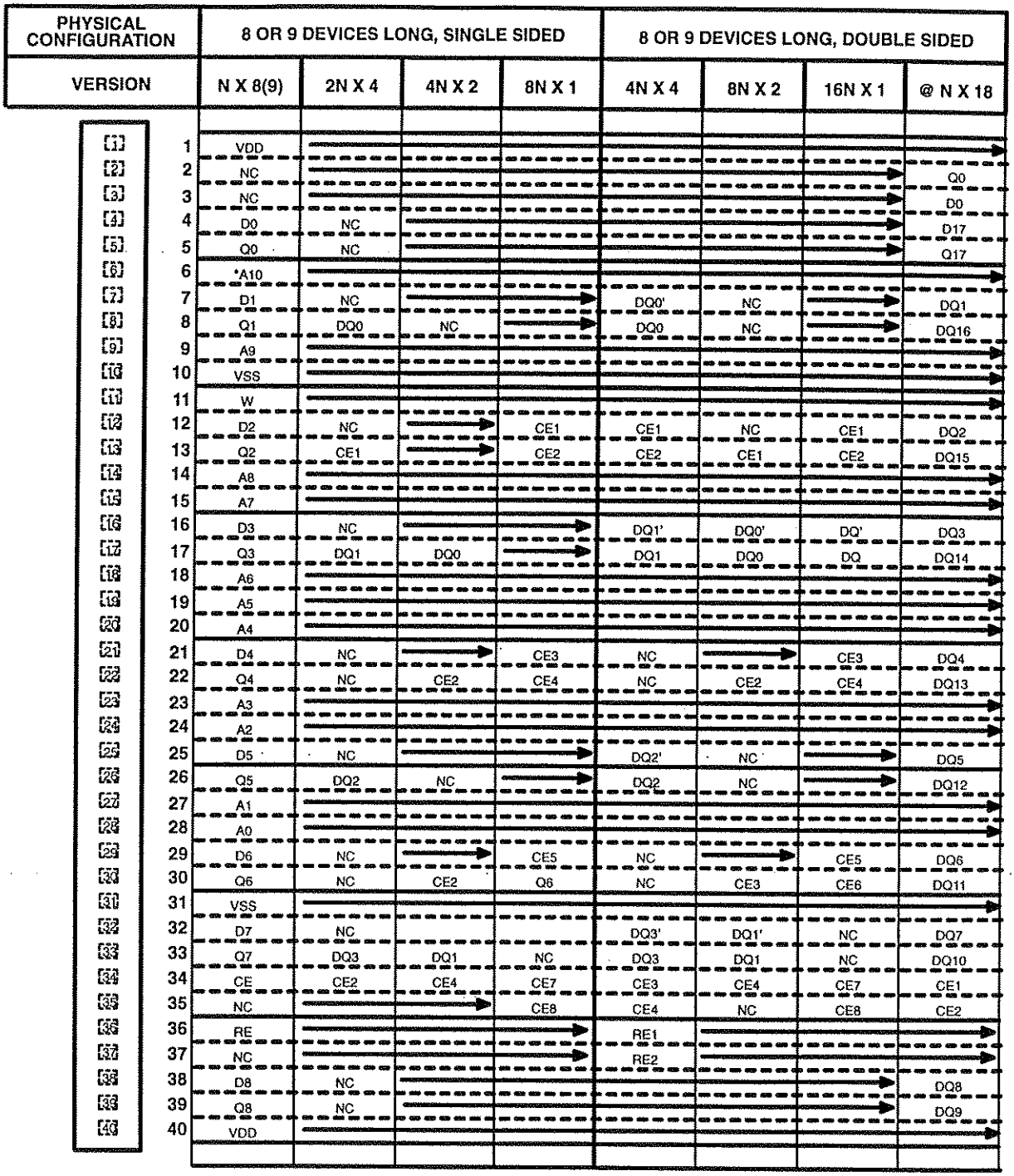


The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q2, Q4, Q6, Q10, Q12, Q14, Q16
E2 & W1 CONTROL Q1, Q3, Q5, Q7, Q11, Q13, Q15, Q17
E3 & W2 CONTROL Q8
E4 & W2 CONTROL Q9

FIGURE 4.3–1

2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY



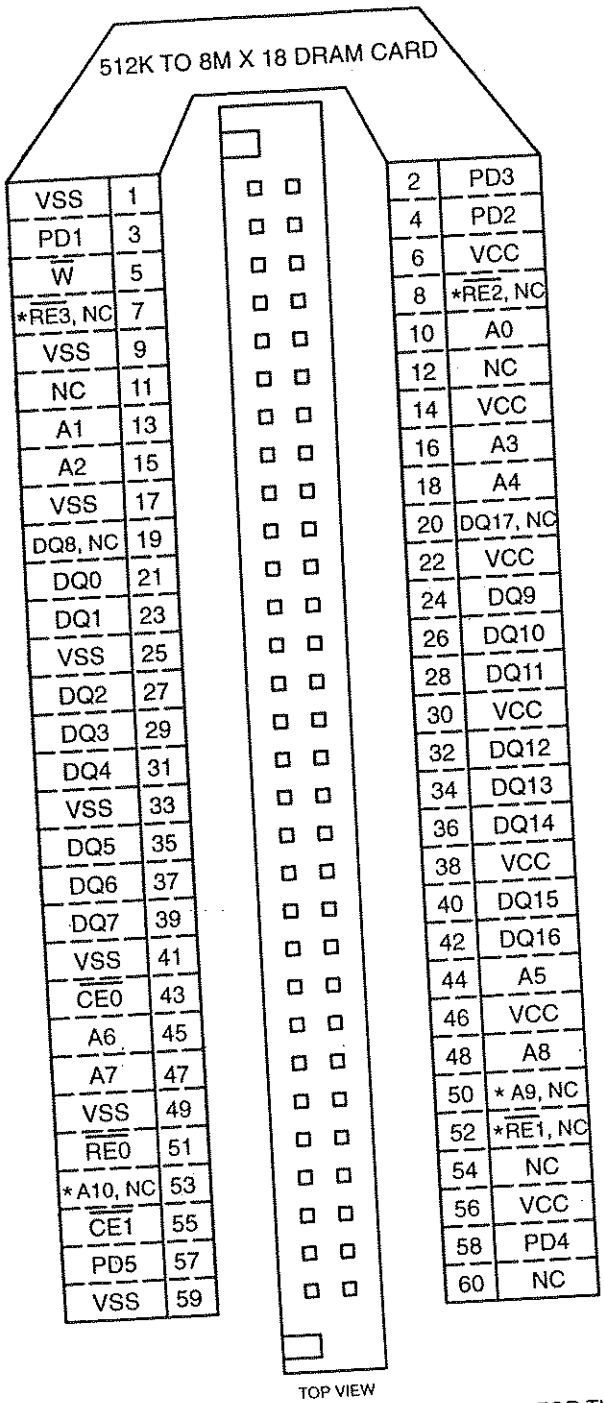
* PIN 5 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

@ N X 18 MODULE CAN BE USED AS A 2N X 9 BY CONNECTING ADJACENT D, Q, & DQ PINS TOGETHER

CONFIGURATION GIVES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE GIVING LENGTH AND NUMBER OF SIDED POPULATED, VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

THOSE PIN NAMES LABELED "'" (PRIME) ARE CONNECTED TO THE BACK SIDE OF THE MODULE ON THE DOUBLE SIDED CONFIGURATIONS.

FIGURE 4.3–2
40 PIN DRAM MODULE FAMILY



* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

	PD4	PD5
SPEED (tRAC)	58	57
80 NS	VSS	VSS
70 NS	VSS	NC
60 NS	NC	VSS
50 NS	NC	NC

PD SPEED TABLE

	PD1	PD2	PD3
CONFIGURATION	3	4	2
512K X 16/18 2 $\overline{RE}$	VSS	NC	VSS
1M X 16/18 4 $\overline{RE}$	VSS	NC	NC
2M X 16/18 2 $\overline{RE}$	NC	VSS	VSS
4M X 16/18 4 $\overline{RE}$	NC	VSS	NC
1M X 16/18 1 $\overline{RE}$	VSS	VSS	VSS
4M X 16/18 1 $\overline{RE}$	NC	NC	VSS
8M X 16/18 2 $\overline{RE}$	VSS	VSS	NC
NO CARD	NC	NC	NC

PD CONFIGURATION TABLE

	PIN NUMBER				
CONFIGURATION	50	53	52	8	7
512K X 16/18 2 $\overline{RE}$	NC	NC	RE1	NC	NC
1M X 16/18 4 $\overline{RE}$	NC	NC	RE1	RE2	RE3
2M X 16/18 2 $\overline{RE}$	A9	NC	RE1	NC	NC
4M X 16/18 4 $\overline{RE}$	A9	NC	RE1	RE2	RE3
1M X 16/18 1 $\overline{RE}$	A9	NC	NC	NC	NC
4M X 16/18 1 $\overline{RE}$	A9	A10	NC	NC	NC
8M X 16/18 2 $\overline{RE}$	A9	A10	RE1	NC	NC

CONFIGURATION PIN ASSIGNMENT TABLE

Pins 19 & 20 (DQ8 & DQ 17) are NC for X16 Versions

FIGURE 4.3–3A
60 PIN x16 or 18 DRAM CARD FAMILY PIN CONNECTIONS

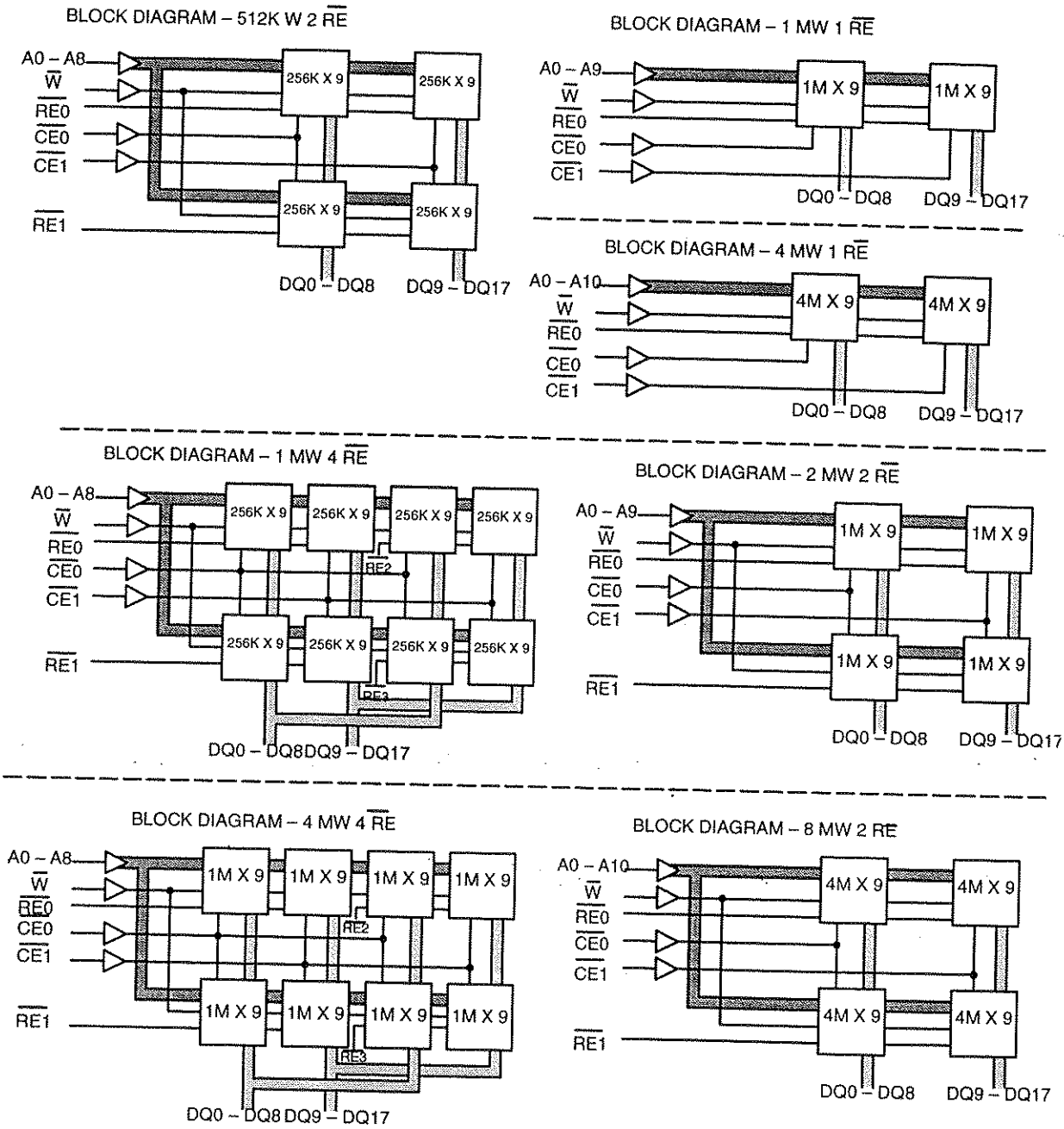
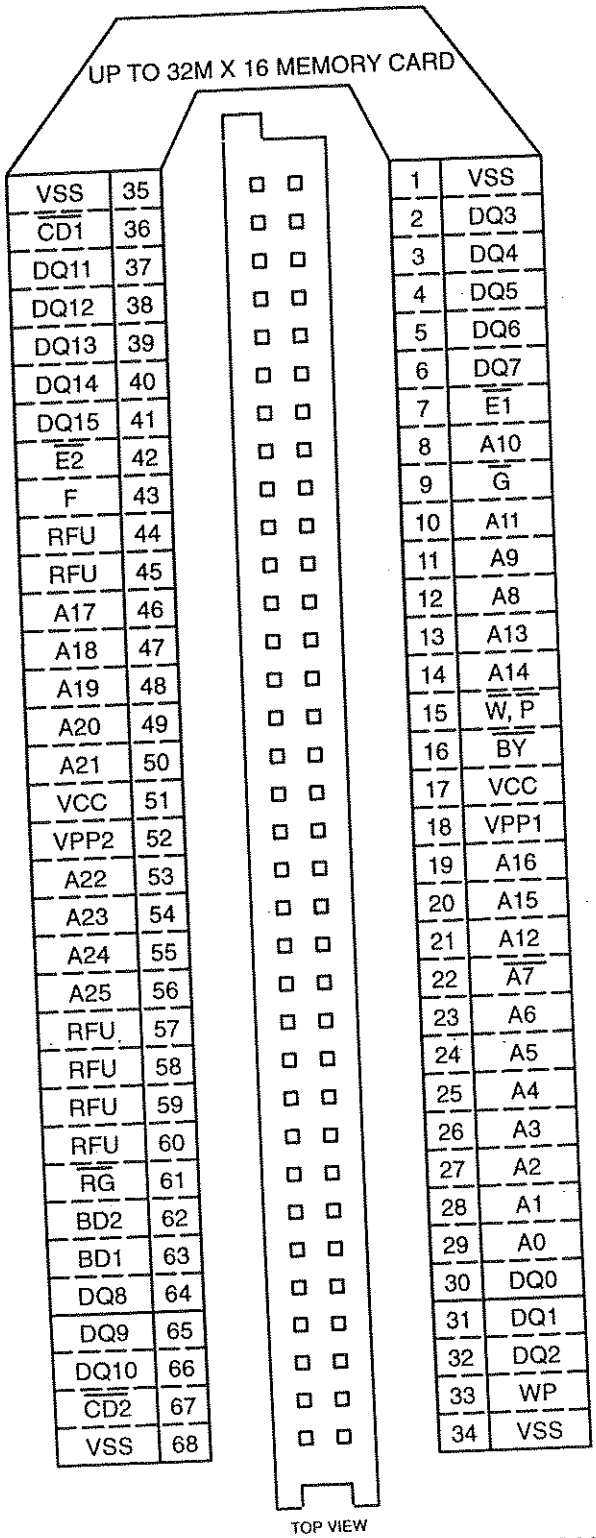


FIGURE 4.3–3B
60 PIN x16 or 18 DRAM CARD FAMILY BLOCK DIAGRAMS



* NOTE: This Standard is applicable to SRAM, EPROM, OTPROM, EEPROM, and FLASH Memory. It is not applicable to DRAM.

FIGURE 4.3–4A

68 PIN MULTIPLE TECHNOLOGY CARD FAMILY

Main Memory Read Function for all types of Memory Card except DRAM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	H	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	H	H	L	H	L	H	VCC	VCC	High–Z	Odd–Byte
Word Access (16 bits)	H	L	L	X	L	H	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	L	H	VCC	VCC	Odd–Byte	High–Z
Main Memory Write Function for SRAM and EEPROM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	H	H	L	H	H	L	VCC	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VCC	VCC	Odd–Byte	High–Z
Main Memory Write Function for OTPROM, EPROM, and FLASH Memory										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	H	H	L	H	H	L	VPP	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VPP	VPP	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VPP	VCC	Odd–Byte	XXX
Attribute Memory Read Function										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	L	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	L	H	L	H	L	H	VCC	VCC	High–Z	Not Valid
Word Access (16 bits)	L	L	L	X	L	H	VCC	VCC	Not Valid	Even–Byte
Odd–Byte Only Access	L	L	H	X	L	H	VCC	VCC	Not Valid	High–Z
Attribute Memory Write Function for SRAM and EEPROM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VCC	VCC	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VCC	VCC	XXX	XXX
Attribute Memory Write Function for OTPROM, EPROM, and FLASH Memory										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	XXX	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VPP	VPP	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VPP	VCC	XXX	XXX

NOTE: For those pins in the above tables where "VCC, VPP" is specified, either supply may be used for programming at the option of the manufacturer. However those cards which use VCC must be able to withstand VPP without damage.

FIGURE 4.3–4B

68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TABLES

4.4 Four Byte Modules & Cards

4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

– 72 PIN SIMM DRAM ECC MODULE FAMILY

4.4.3 – 88 PIN DRAM CARD FAMILY

4.4.4 – 72 PIN DRAM SO–DIMM FAMILY

4.4.5 – 88 PIN DRAM SO–DIMM FAMILY

4.4.6 – 112 PIN MPDRAM DIMM FAMILY

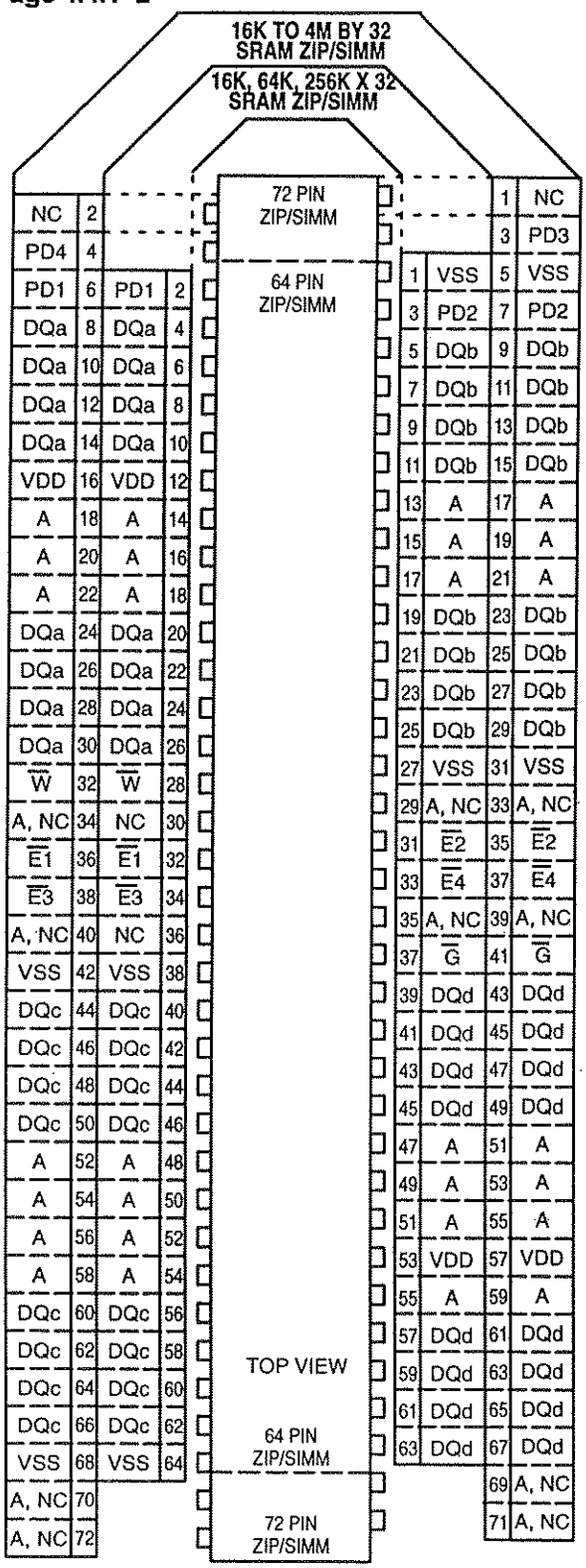
4.4.7 – 80 PIN EEPROM SIMM FAMILY

4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

CAPACITY—16K, 32K, 64K, 128K, 256K, 512K, 1M, 2M, or 4M WORDS OF 32 BITS
CONFIGURATION—FOUR BANK MODULE
—SELECTABLE BY BYTE GROUPS
LOGIC FEATURE—The 72 pin modules are supersets of the 64 pin family with added capacity.
PACKAGE—64 and 72 PIN SIP MODULEWITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.4.1–1

XILINX EXHIBIT 1010
Page 227



NOTES for 72–pin ZIP/SIMM module pinout:
1. $\overline{E1}$ enables DQa pins 8, 10, 12, 14, and 24, 26, 28, 30; $\overline{E2}$ enables DQb pins 9, 11, 13, 15, and 23, 25, 27, 29; $\overline{E3}$ enables DQc pins 44, 46, 48, 50, and 60, 62, 64, 66; $\overline{E4}$ enables DQd pins 43, 45, 47, 49, and 61, 63, 65, 67.
2. $\overline{W}$ enables writing into all enabled devices.
3. $\overline{G}$ enables outputs from any and all enabled devices.
4. This footprint is a superset of the 64–pin JEDEC standard. Any 64 pin JEDEC standard module may be used in the 72–pin footprint. PD3 and PD4 become NC (OPEN) in this case.
5. Two pins (1 & 2) are available for future definition.

PRESENCE DETECT TRUTH TABLE				
MOD CONFIG	PD4	PD3	PD2	PD1
72P MOD	PIN 68	PIN 67	PIN 66	PIN 11
# 16K X 32	O	O	O	S
32K X 32	S	S	O	O
# 64K X 32	O	O	S	O
128K X 32	S	O	O	O
# 256K X 32	O	O	S	S
512K X 32	O	S	O	O
1M X 32	O	S	O	S
2M X 32	O	S	S	O
4M X 32	O	S	S	S

O = OPEN CIRCUIT (NO CONNECTION)
S = CONNECTED TO VSS

Indicates configurations duplicated in 64P package. Use PD1 & PD2 only.

PRESENCE DETECT NOTES
1. Compatibility has been maintained with existing 64–pin standard
2. PD signature has been added for 32K X 32 & 128K X 32 configurations that were not implemented in the 64–pin standard.
3. Six PD signatures are left undefined for future definition.

ADDRESS PIN ASSIGNMENTS								
CONFIGURATION	ADDRESS PIN NUMBER							
72 P MODULES	33	34	40	39	69	70	71	72
16K X 32	NC	NC	NC	NC	NC	NC	NC	NC
32K X 32	A	NC	NC	NC	NC	NC	NC	NC
64K X 32	A	A	NC	NC	NC	NC	NC	NC
128K X 32	A	A	A	NC	NC	NC	NC	NC
256K X 32	A	A	A	A	NC	NC	NC	NC
512K X 32	A	A	A	A	A	NC	NC	NC
1M X 32	A	A	A	A	A	A	NC	NC
2M X 32	A	A	A	A	A	A	A	NC
4M X 32	A	A	A	A	A	A	A	A
64 P MODULES	29	30	35	36				
16K X 32	NC	NC	NC	NC				
64K X 32	A	A	NC	NC				
256K X 32	A	A	A	A				

FIGURE 4.4.1–1
16K TO 4M BY 32 SRAM ZIP/SIMM MODULE

NOTE: The 72 pin module standards that follow describe two separate devices. Both have a 4 byte data interface. One is intended to be used with or without parity bits while the other contains error correction bits ECC). The one with ECC is similar to the parity module but is not completely pin compatible

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 32 or 36 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES
LOGIC FEATURES, These modules contain a "presence detect" feature which conists of output pins which supply an encoded value which defines the storage capacity and speed of the module.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4.4.2–2A
BLOCK DIAGRAMS—Fig. 4.4.2–2 A⇒K. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–2 B⇒K
POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

– 72 PIN SIMM DRAM ECC MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 36 or 39 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES
LOGIC FEATURES, These modules are optimized for ECC applications. They are similar to but not the same as the modules described in Fig. 4–6. The Standard defines a "presence detect" feature which consists of output pins which supply an encoded value which defines the storage capacity and speed of the module. The PD code identifies the presence of an ECC module as well as the speed and organization of the module. The Standard also defines the logic organization of the modules in Figs. 4.4.2–3B & 4.4.2–3C.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4.4.2–3A
BLOCK DIAGRAMS—Figs. 4.4.2–3 B & C. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–3 B & C
POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

72 Pin SIMM Block Diagrams

The block diagrams given in the 12 pages, Figs 4.4.2–2 B ⇒ K and Figs 4.4.2–3 B & C), are applicable to the 72 Pin SIMM pinouts shown in Figures 4.4.2–2 A and 4.4.2–3 A. These block diagrams are provided for guidance only. **Other implementations with different block configurations are also acceptable**.

The following table shows the applicability of the block configurations given to the 5 V and 3.3 V Non–ECC and ECC modules.

Configuration	# Banks	Applies to: 5 V SIMM	Applies to: 3.3 V SIMM
Parity, Non–Parity			
X32/36 W/X4, X1 (X36)	1 or 2	X	X
X32/36 W/X16, X18	1 or 2	X	X
X36 W/X4, X4/4CE	1 or 2	X	X
X36 W/X4, X2/2CE	1 or 2	X	X
X36 W/X16, X4/4CE	1 or 2	X	X
X36 W/X16, X2/2CE	1 or 2	X	X
X32 W/X8	1 or 2		X
X36 W/X8, X2/2CE	1 or 2		X
X32 W/X32	1 or 2		X
X36 W/X32, X2/2CE	1 or 2		X
ECC			
X36/40 W/X4	1 or 2	X	X (X36 only)

Note: To reduce the number of diagrams, only 2 bank versions are shown. In addition, in cases where one SIMM I/O width can be described as a depopulation of another SIMM (i.e. X36⇒X32), the depopulated devices are shown by a "dashed" outline.

$\overline{RE}$ AND $\overline{G}$ WIRING FOR BYTE WRITE SIMMS.		
SIGNAL NAME	5 V SIMMs	3.3 V SIMMs
$\overline{G}$	Tied to GND	Wired to Pin 46
$\overline{RE0}$	Connected as shown. Tied to pin 44 ($\overline{RE0}$)	$\overline{RE0}$, $\overline{RE2}$ nets connected together and tied to pin 44 ($\overline{RE0}$)
$\overline{RE1}$	Connected as shown. Tied to pin 45 ($\overline{RE1}$)	$\overline{RE1}$, $\overline{RE3}$ nets connected together and tied to pin 45 ($\overline{RE1}$)
$\overline{RE2}$	Connected as shown. Tied to pin 34 ($\overline{RE2}$)	$\overline{RE0}$, $\overline{RE2}$ nets connected together and tied to pin 44 ($\overline{RE0}$)
$\overline{RE3}$	Connected as shown. Tied to pin 33 ($\overline{RE3}$)	$\overline{RE1}$, $\overline{RE3}$ nets connected together and tied to pin 45 ($\overline{RE1}$)

FIGURE 4.4.2–1
72 PIN DRAM SIMM APPLICABILITY TABLE

	5 V Byte Write	3.3 V Byte Write
PIN #	PIN NAME	PIN NAME
1	VSS	VSS
2	DQ0	DQ0
3	DQ18	DQ18
4	DQ1	DQ1
5	DQ19	DQ19
6	DQ2	DQ2
7	DQ20	DQ20
8	DQ3	DQ3
9	DQ21	DQ21
10	VDD	VDD
11	NU	PD5
12	A0	A0
13	A1	A1
14	A2	A2
15	A3	A3
16	A4	A4
17	A5	A5
18	A6	A6
19	NC, A10	NC, A10
20	DQ4	DQ4
21	DQ22	DQ22
22	DQ5	DQ5
23	DQ23	DQ23
24	DQ6	DQ6
25	DQ24	DQ24
26	DQ7	DQ7
27	DQ25	DQ25
28	A7	A7
29	NC, A11	NC, A11
30	VDD	VDD
31	A8	A8
32	NC, A9	NC, A9
33	NC, $\overline{RE3}$	NC, A12
34	$\overline{RE2}$	NC, A13
35	PDQ26, NC	PDQ26, NC
36	PDQ8, NC	PDQ8, NC

	5 V Byte Write	3.3 V Byte Write
PIN #	PIN NAME	PIN NAME
37	PDQ17, NC	PDQ17, NC
38	PDQ35,, NC	PDQ35,, NC
39	VSS	VSS
40	$\overline{CE0}$	$\overline{CE0}$
41	$\overline{CE2}$	$\overline{CE2}$
42	$\overline{CE3}$	$\overline{CE3}$
43	$\overline{CE1}$	$\overline{CE1}$
44	$\overline{RE0}$	$\overline{RE0}$
45	NC, $\overline{RE1}$	NC, $\overline{RE1}$
46	NC	$\overline{G}$
47	$\overline{W}$	$\overline{W}$
48	PD(ECC)	PD(ECC)
49	DQ9	DQ9
50	DQ27	DQ27
51	DQ10	DQ10
52	DQ28	DQ28
53	DQ11	DQ11
54	DQ29	DQ29
55	DQ12	DQ12
56	DQ30	DQ30
57	DQ13	DQ13
58	DQ31	DQ31
59	VDD	VDD
60	DQ32	DQ32
61	DQ14	DQ14
62	DQ33	DQ33
63	DQ15	DQ15
64	DQ34	DQ34
65	DQ16	DQ16
66	NC	$\overline{EDO}$
67	PD1	PD1
68	PD2	PD2
69	PD3	PD3
70	PD4	PD4
71	NC	PD(REF)
72	VSS	VSS

PRESENCE DETECT TRUTH TABLE

CONFIGURATION	tRAC	ECC	PD1	PD2	PD3	PD4
1MB (256K X 36) 64MB (16M X 32/36)	100 nS	O	S	O	S	S
	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
2MB (512K X 36) 128MB (32M X 32/36)	100 nS	O	O	S	S	S
	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O
4MB (1M X 36) 256MB (64M X 32/36)	100 nS	O	S	S	S	S
	80 nS	O	S	S	O	S
	70 nS	O	S	S	S	O
	60 nS	O	S	S	O	O
8MB (2M X 36) 0.5GB (128M X 32/36)	100 nS	O	O	O	S	S
	80 nS	O	O	O	O	S
	70 nS	O	O	O	S	O
	60 nS	O	O	O	O	O
16MB (4M X 36) 1GB (256M X 32/36)	50 nS	O	S	O	S	S
	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
32MB (8M X 36) 2GB (512M X 36)	50 nS	O	O	S	S	S
	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O

O = NO CONNECTION S = CONNECTED TO VSS

$\overline{EDO}$ Pin: VSS for EDO, NC for Fast Page.

Note: The $\overline{ECC}$ Function (Pin 48) is not a defined function for the devices in this standard, however, it is used in a companion Standard for 72 pin ECC modules shown in Fig. 4–10. The presence of a VSS connection on this pin signifies that an ECC module has been inserted.

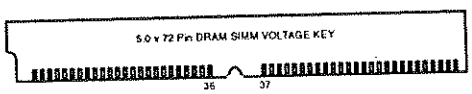
CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 BIT WORDS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{RE3}$	NC	$\overline{RE3}$	NC	$\overline{RE3}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	RE1

* A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.

NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.

See Figure 4–18 for applicable block diagrams



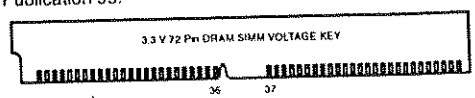


FIGURE 4.4.2–2 A

256K TO 256M BY 36, 72 PIN DRAM MODULE PINOUT

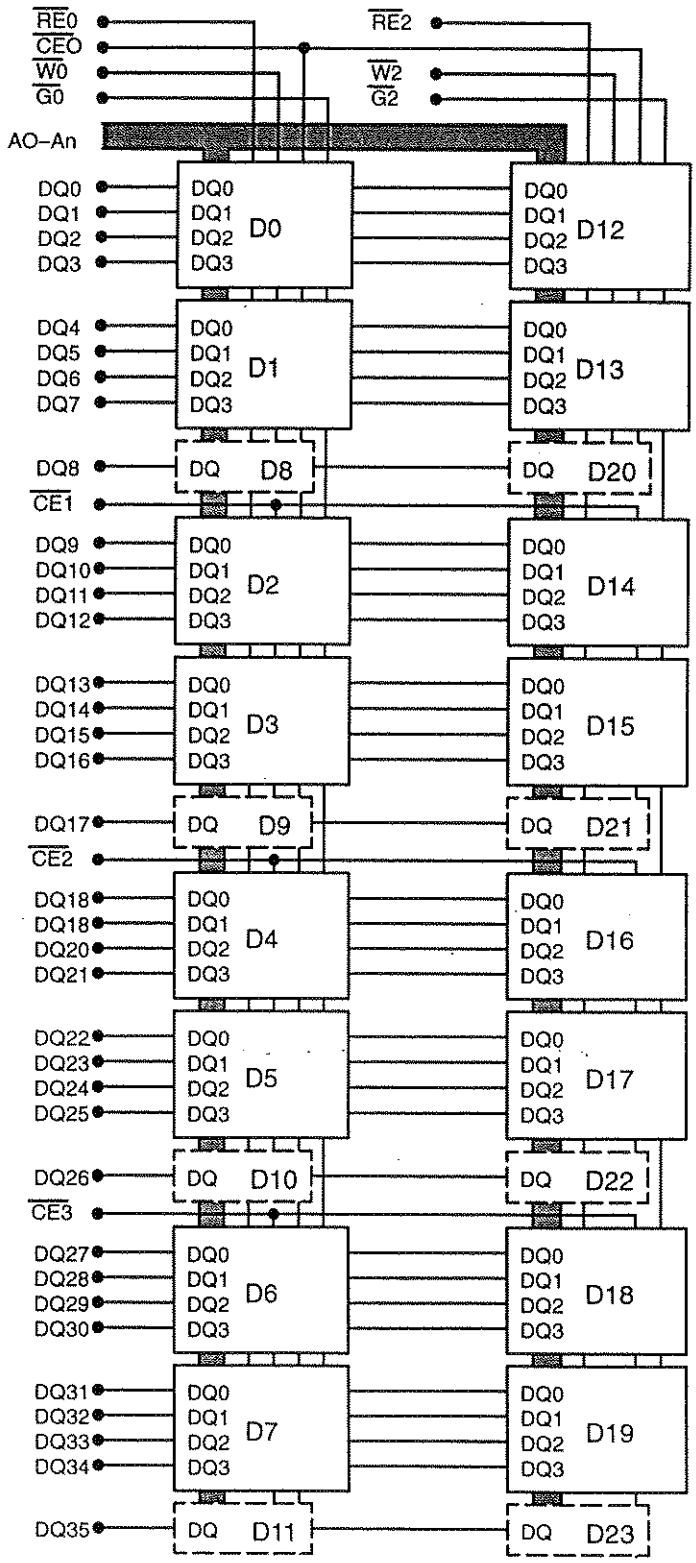
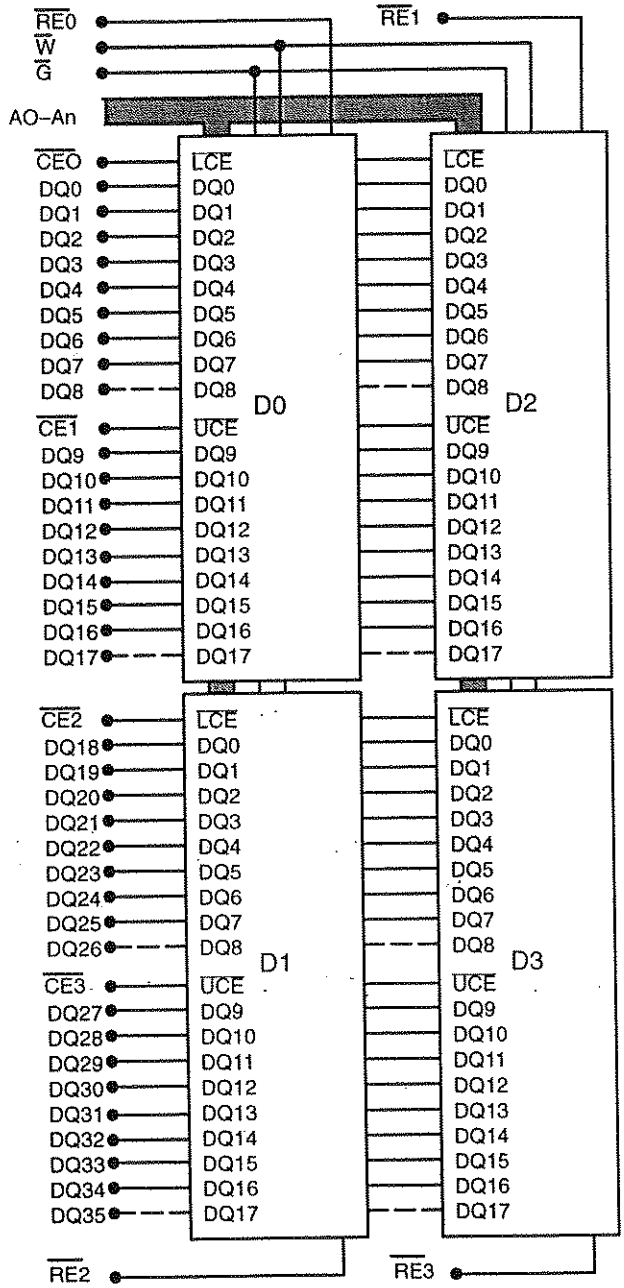


FIGURE 4.4.2–2 B
X32/36 DRAM SIMM, 2 Banks with X4 & X1 DRAMs



DQ8, DQ17, DQ26, & DQ35 ARE NOT USED
ON THE X32 MODULE USING X16 DRAM

FIGURE 4.4.2–2 C
X32/36 DRAM SIMM, 2 Banks with X16/18 DRAMs

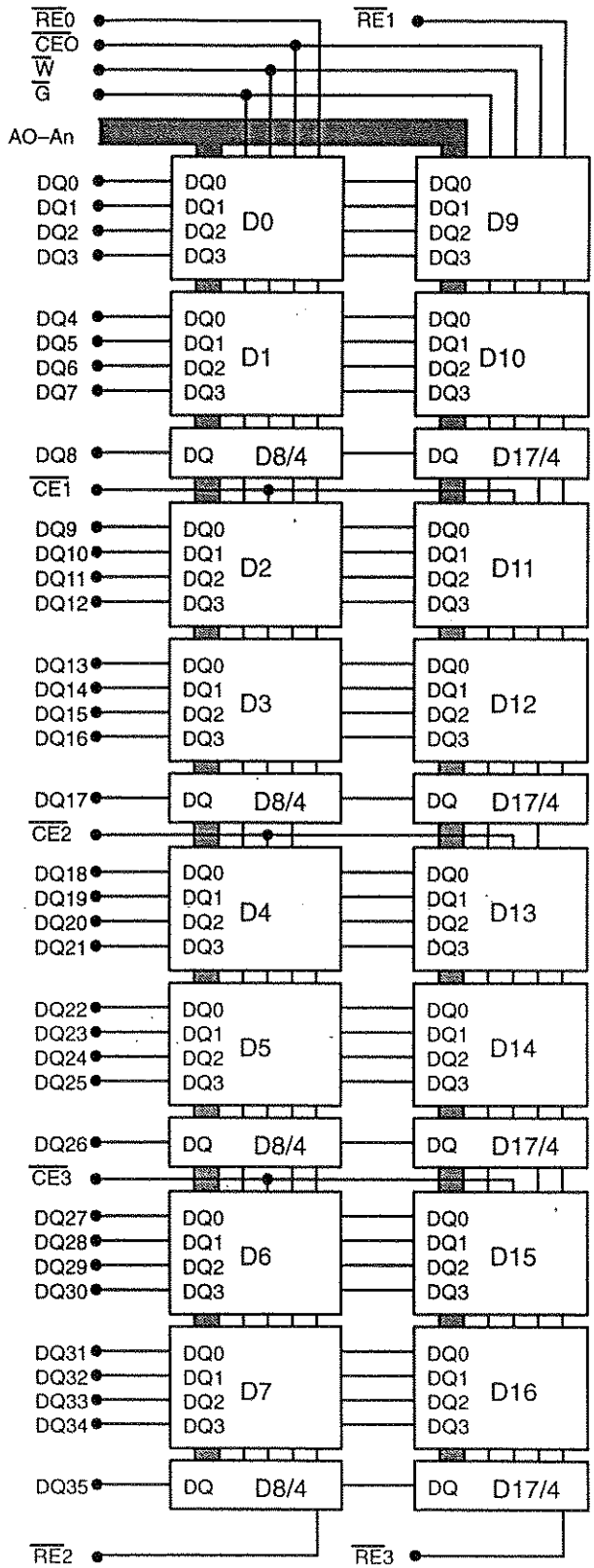


FIGURE 4.4.2–2 D
X36 DRAM SIMM, 2 Banks with X4 & X4 W/4 $\overline{CE}$ DRAMs

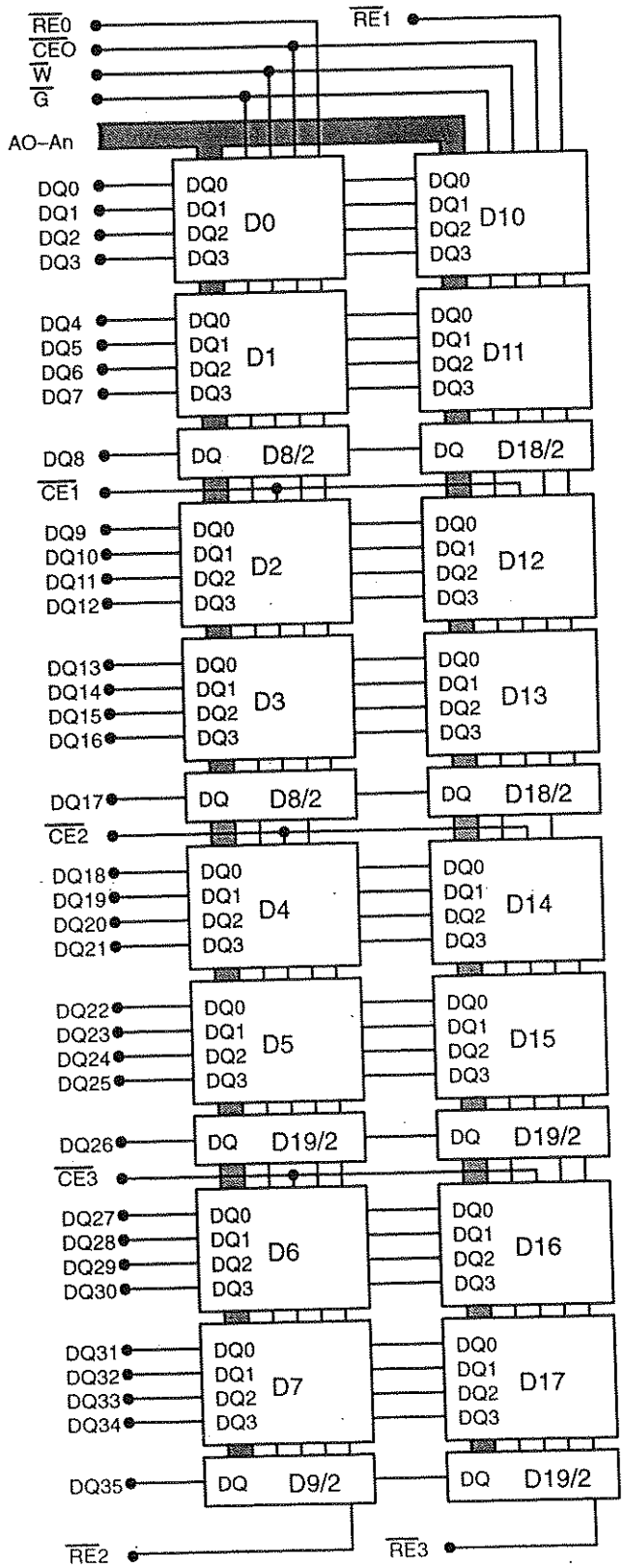


FIGURE 4.4.2–2 E

X36 DRAM SIMM, 2 Banks with X4 & X2 W/2 $\overline{CE}$ DRAMs

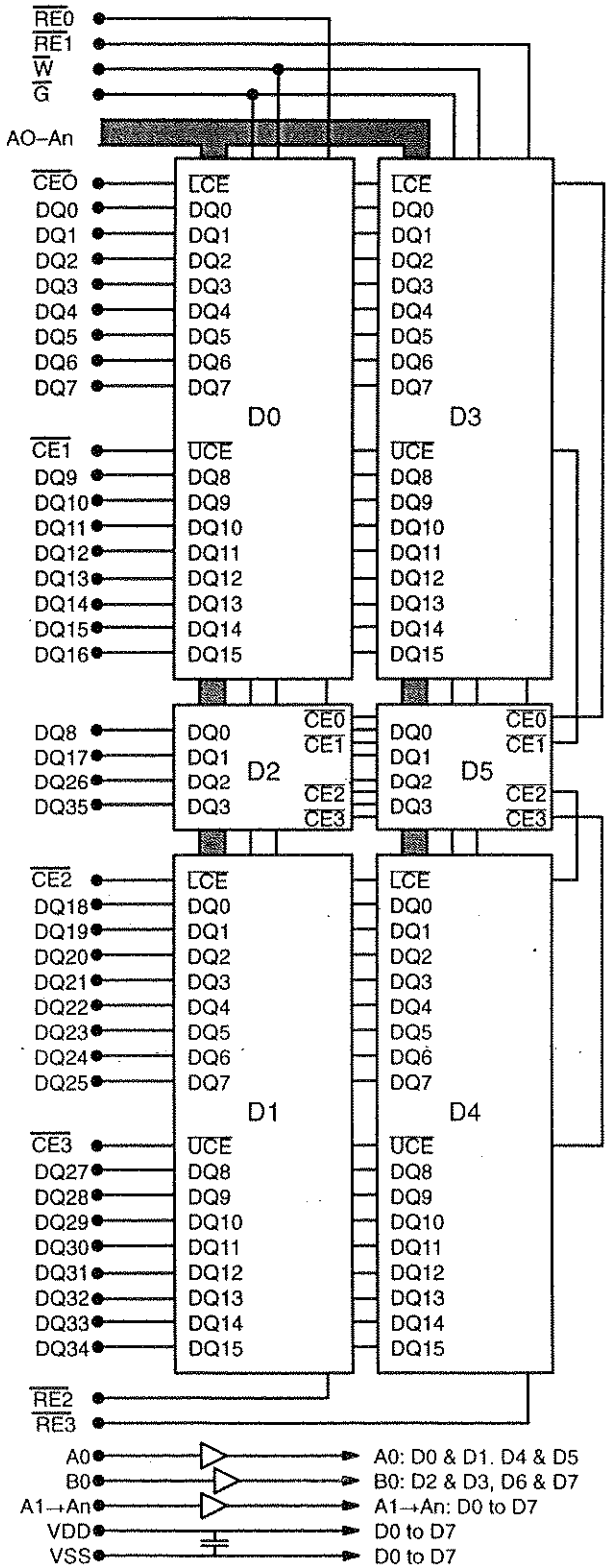


FIGURE 4.4.2–2 F
X36 DRAM SIMM, 2 Banks with X16 & X4 W/4 $\overline{CE}$ DRAMs

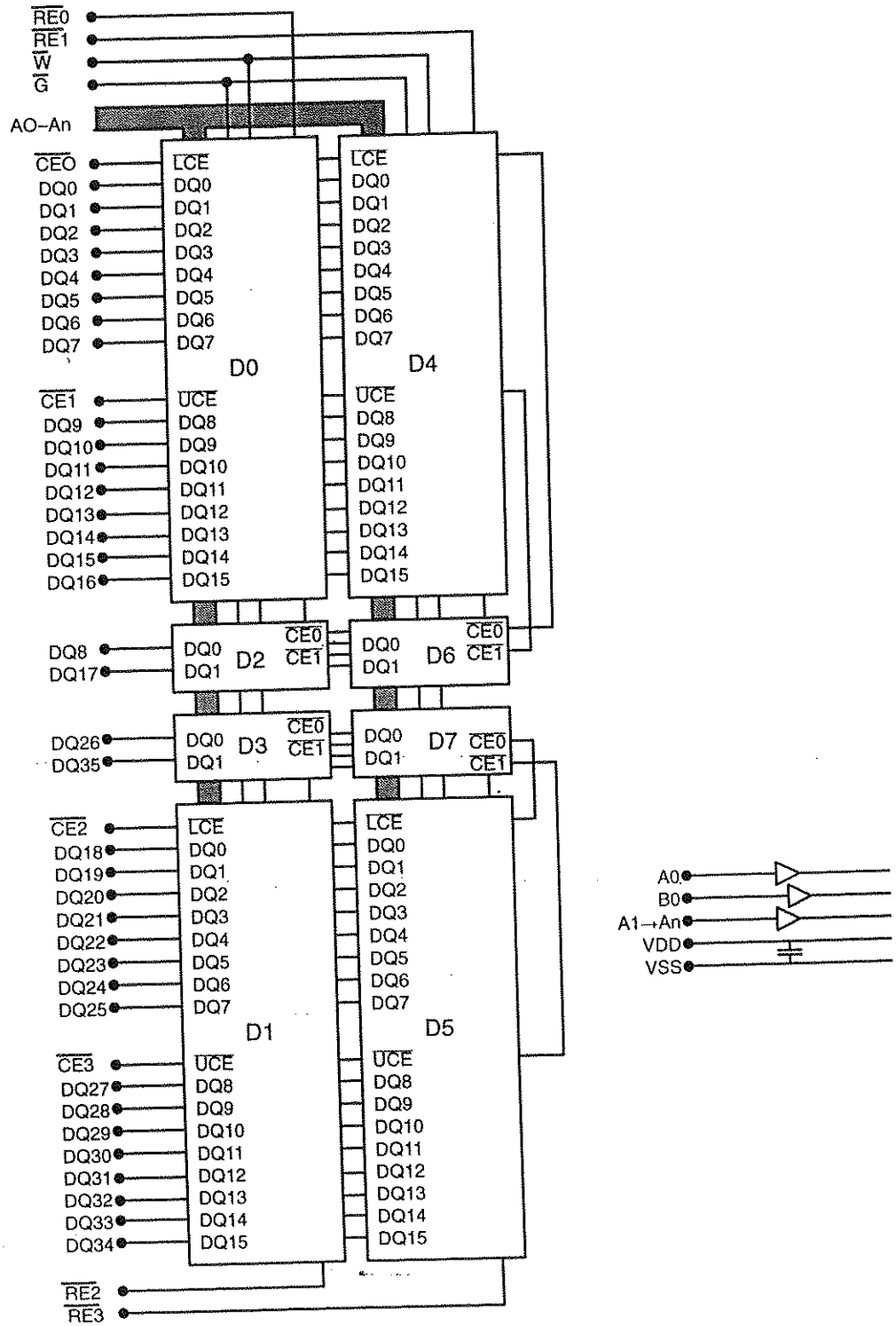


FIGURE 4.4.2–2 G

X36 DRAM SIMM, 2 bank with X16 & X2 W/2 $\overline{CE}$ DRAMs

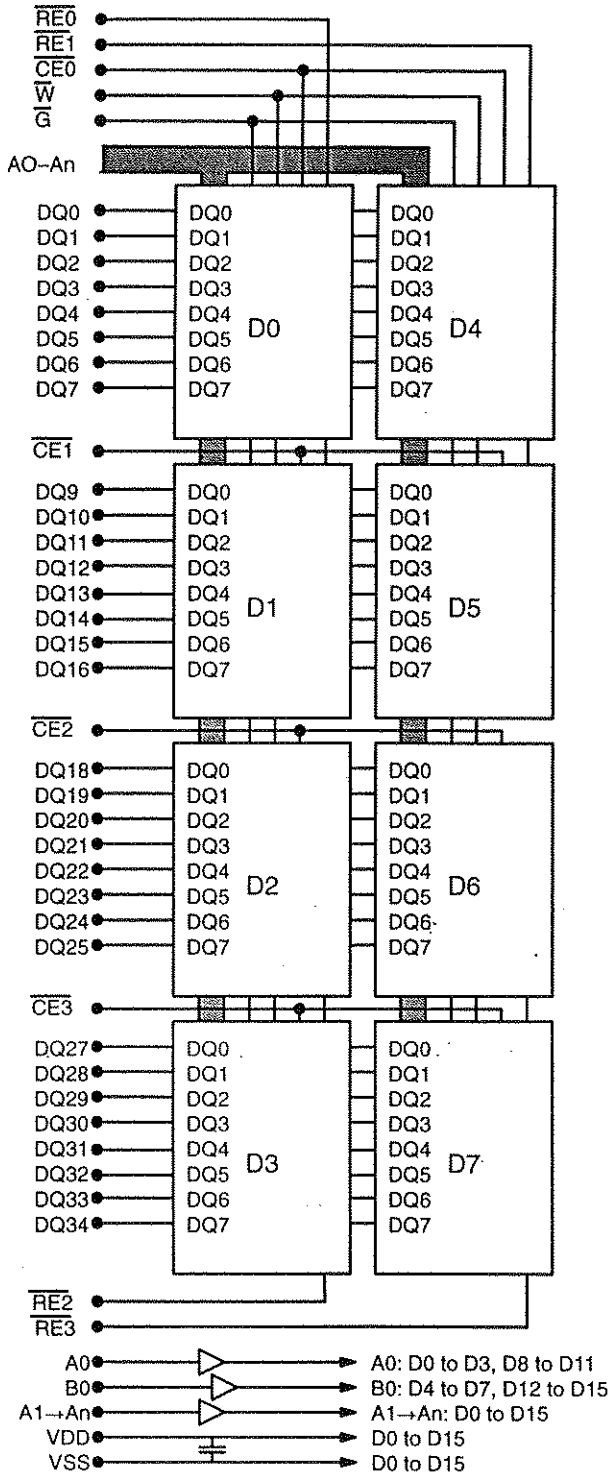


FIGURE 4.4.2–2 H
X32 DRAM SIMM, 2 Banks with X8 DRAMs

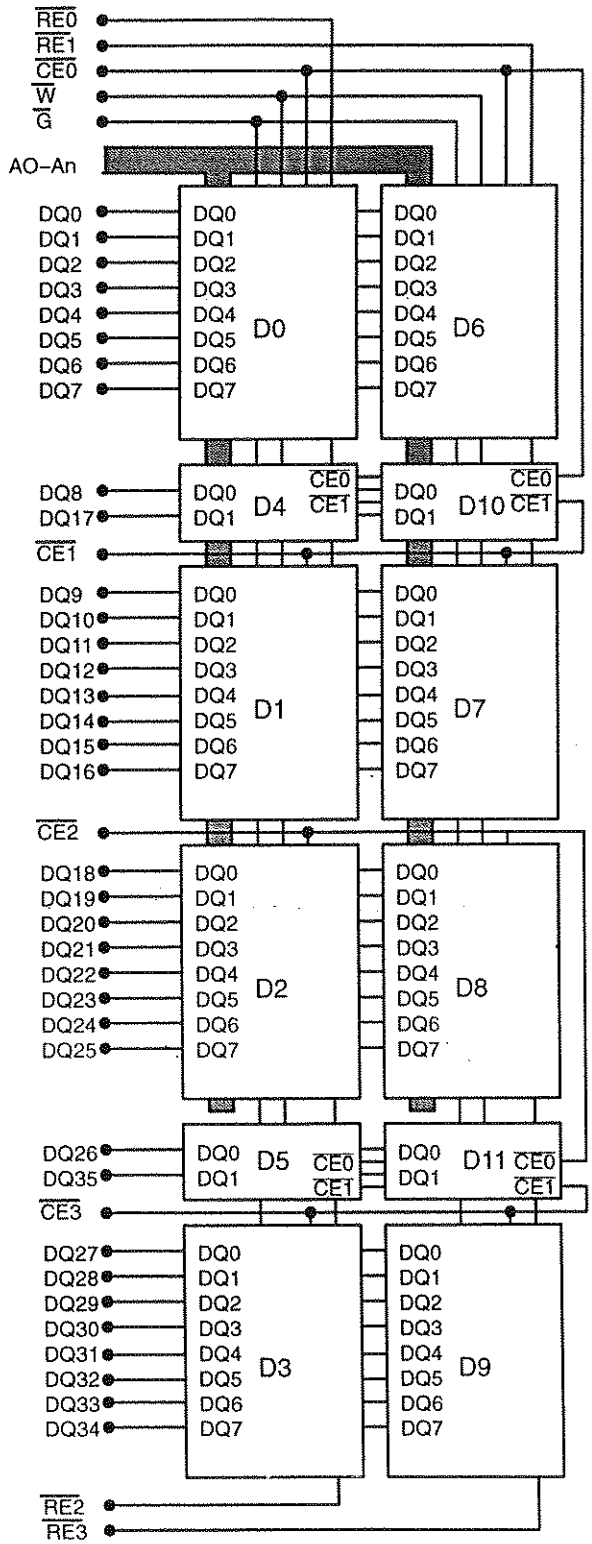


FIGURE 4.4.2–2 I

X36 DRAM SIMM, 2 Banks with X8 & X2 W/2 $\overline{CE}$ DRAMs

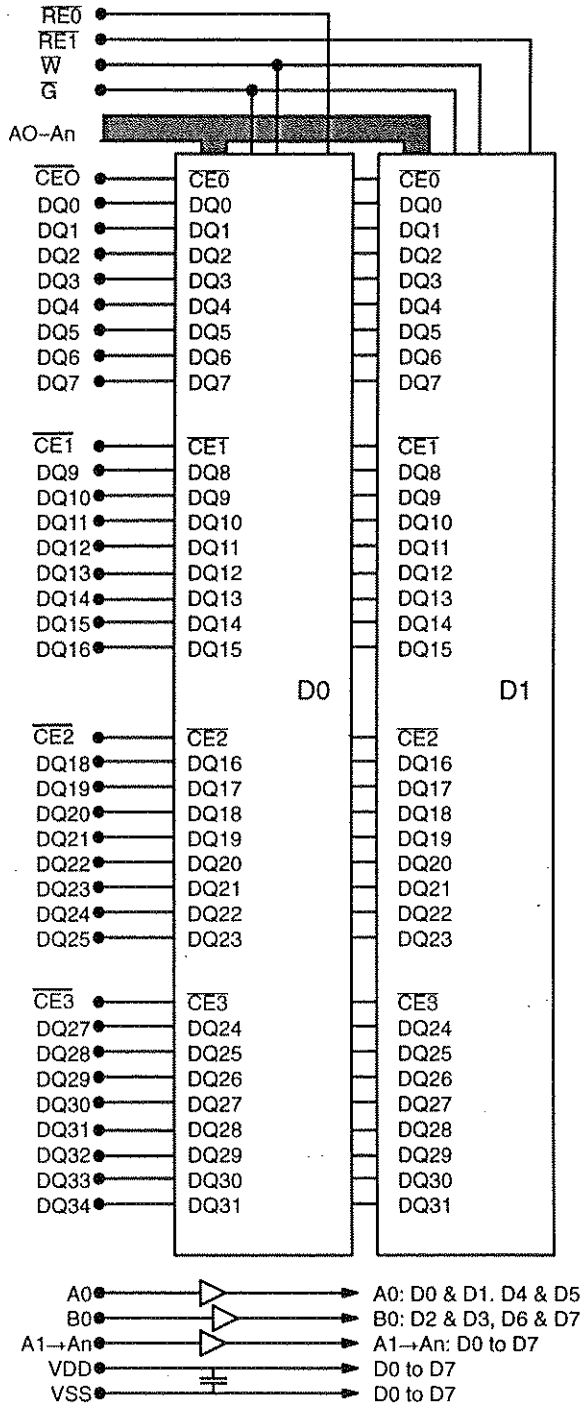


FIGURE 4.4.2–2 J
X32 DRAM SIMM, 2 bank with X32 DRAMs

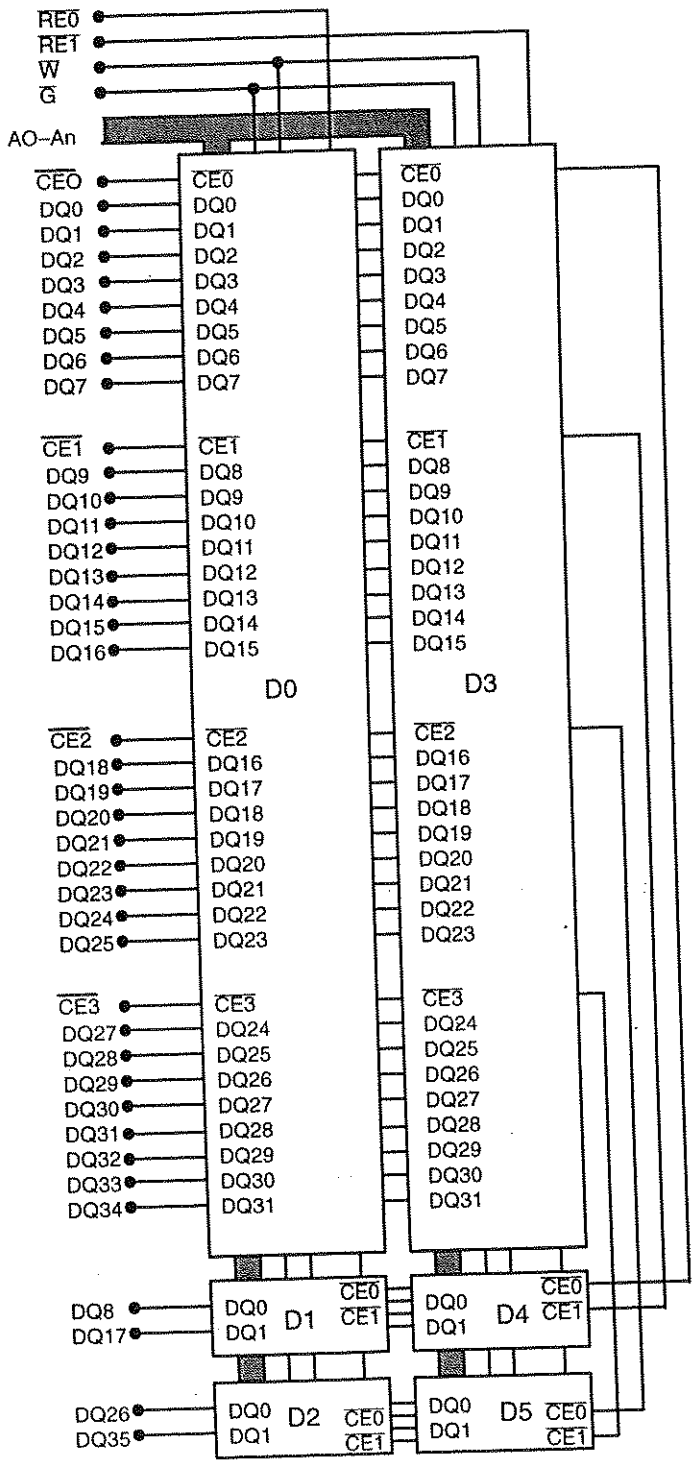


FIGURE 4.4.2–2 K

X36 DRAM SIMM, 2 bank with X32 & X2 W/2 $\overline{CE}$ DRAMs

	5 V ECC	3.3 V ECC
PIN #	PIN NAME	PIN NAME
1	VSS	VSS
2	DQ0	DQ0
3	DQ1	DQ1
4	DQ2	DQ2
5	DQ3	DQ3
6	DQ4	DQ4
7	DQ5	DQ5
8	DQ6	DQ6
9	DQ7	DQ7
10	VDD	VDD
11	PD5	PD5
12	A0	A0
13	A1	A1
14	A2	A2
15	A3	A3
16	A4	A4
17	A5	A5
18	A6	A6
19	$\overline{G}$	$\overline{G}$
20	DQ8	DQ8
21	DQ9	DQ9
22	DQ10	DQ10
23	DQ11	DQ11
24	DQ12	DQ12
25	DQ13	DQ13
26	DQ14	DQ14
27	DQ15	DQ15
28	A7	A7
29	DQ16	DQ16
30	VDD	VDD
31	A8	A8
32	A9	A9
33	NC	NC, A12
34	NC	NC, A13
35	DQ17	DQ17
36	DQ18	DQ18

	5 V ECC	3.3 V ECC
PIN #	PIN NAME	PIN NAME
37	DQ19	DQ19
38	DQ20	DQ20
39	VSS	VSS
40	$\overline{CE0}$	$\overline{CE0}$
41	NC, A10	A10
42	NC, A11	A11
43	NC, $\overline{CE1}$	$\overline{CE1}$
44	$\overline{RE0}$	$\overline{RE0}$
45	NC, $\overline{RE1}$	$\overline{RE1}$
46	DQ21	DQ21
47	$\overline{W}$	$\overline{W}$
48	$\overline{ECC}$	$\overline{ECC}$
49	DQ22	DQ22
50	DQ23	DQ23
51	DQ24	DQ24
52	DQ25	DQ25
53	DQ26	DQ26
54	DQ27	DQ27
55	DQ28	DQ28
56	DQ29	DQ29
57	DQ30	DQ30
58	DQ31	DQ31
59	VDD	VDD
60	DQ32	DQ32
61	DQ33	DQ33
62	DQ34	DQ34
63	DQ35	DQ35
64	DQ36,NC	NC
65	DQ37,NC	NC
66	DQ38,NC	$\overline{EDO}$
67	PD1	PD1
68	PD2	PD2
69	PD3	PD3
70	PD4	PD4
71	DQ39,NC	PD(REF)
72	VSS	VSS

PRESENCE DETECT TRUTH TABLE

TYPE	tRAC	$\overline{ECC}$	PD1	PD2	PD3	PD4	#PD5
256K X 36 or 40	100 nS	S	S	O	S	S	O
16M X 36/39	80 nS	S	S	O	O	S	O
	70 nS	S	S	O	S	O	O
	60 nS	S	S	O	O	O	O
512K X 36 or 40	100 nS	S	O	S	S	S	O
32M X 36/39	80 nS	S	O	S	O	S	O
	70 nS	S	O	S	S	O	O
	60 nS	S	O	S	O	O	O
1M X 36 or 40	100 nS	S	S	S	S	S	O
64M X 36/39	80 nS	S	S	S	O	S	O
	70 nS	S	S	S	S	O	O
	60 nS	S	S	S	O	O	O
2M X 36 or 40	100 nS	S	O	O	S	S	O
128M X 36/39	80 nS	S	O	O	O	S	O
	70 nS	S	O	O	S	O	O
	60 nS	S	O	O	O	O	O
4M X 36 or 40	80 nS	S	S	O	O	S	S
256M X 36/39	70 nS	S	S	O	S	O	S
	60 nS	S	S	O	O	O	S
	50 nS	S	S	O	S	S	S
8M X 36 or 40	80 nS	S	O	S	O	S	S
512M X 36/39	70 nS	S	O	S	S	O	S
	60 nS	S	O	S	O	O	S
	50 nS	S	O	S	S	S	S

O = NC CONNECTION) S = CONNECTED TO VSS
$\overline{EDO}$ Pin: VSS FOR EDO, NC for Fast Page.
$\overline{ECC}$ Pin: VSS for ECC Module, OPEN for NON ECC Module
The connection of PD5 to VSS must be made through a 2..6 KΩ resistor

CONFIGURATION PIN ASSIGNMENT TABLE

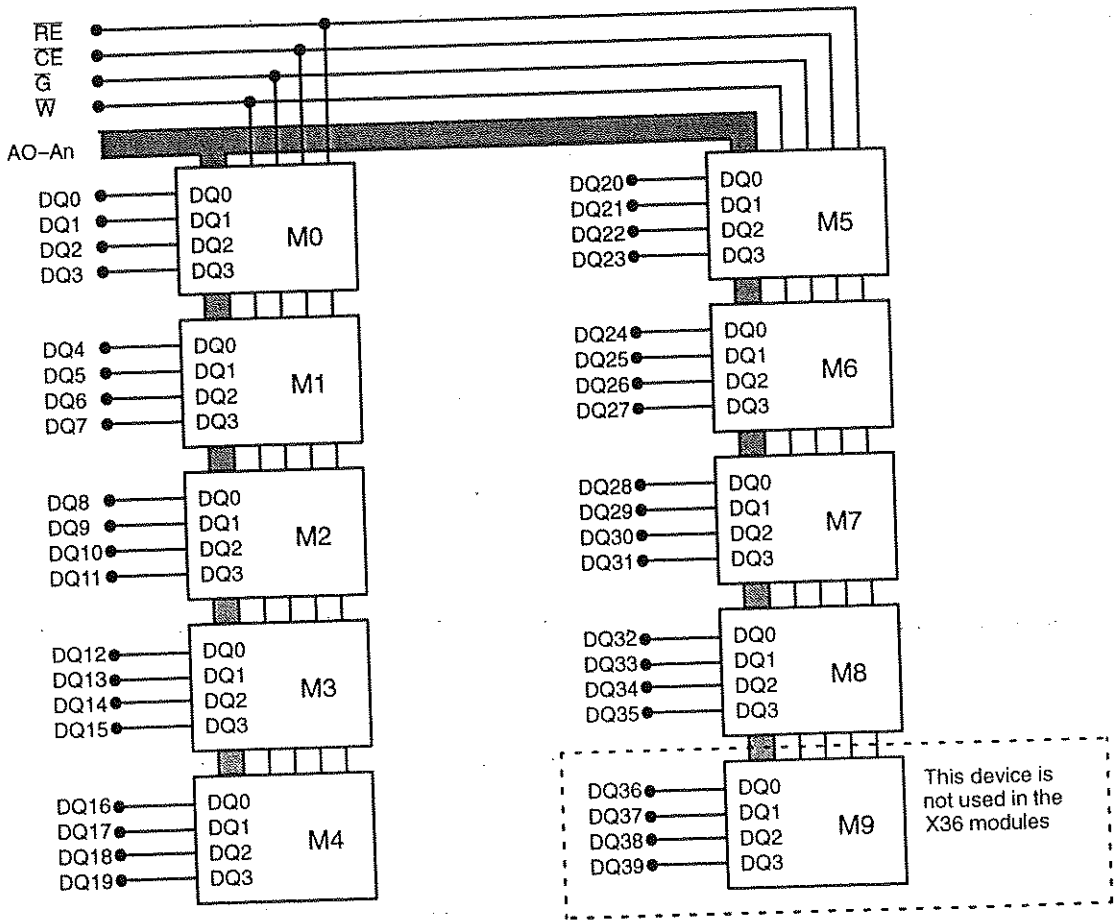
	MODULE SIZE, 36 or 39/40 BITS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{RE3}$	NC	$\overline{RE3}$	NC	$\overline{RE3}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	RE1

*A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.
NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.



FIGURE 4.4.2–3 A
256K TO 8M BY 36 or 40, 72 PIN ECC DRAM MODULE PINOUT

XILINX EXHIBIT 1010
Page 242



BLOCK DIAGRAM for 256K/1M/4M X 36 or 40 USING X4 DRAM

FIGURE 4.4.2–3 B
36/40 BIT 72 PIN ECC DRAM SIMM, 1 Bank with X4 DRAMs

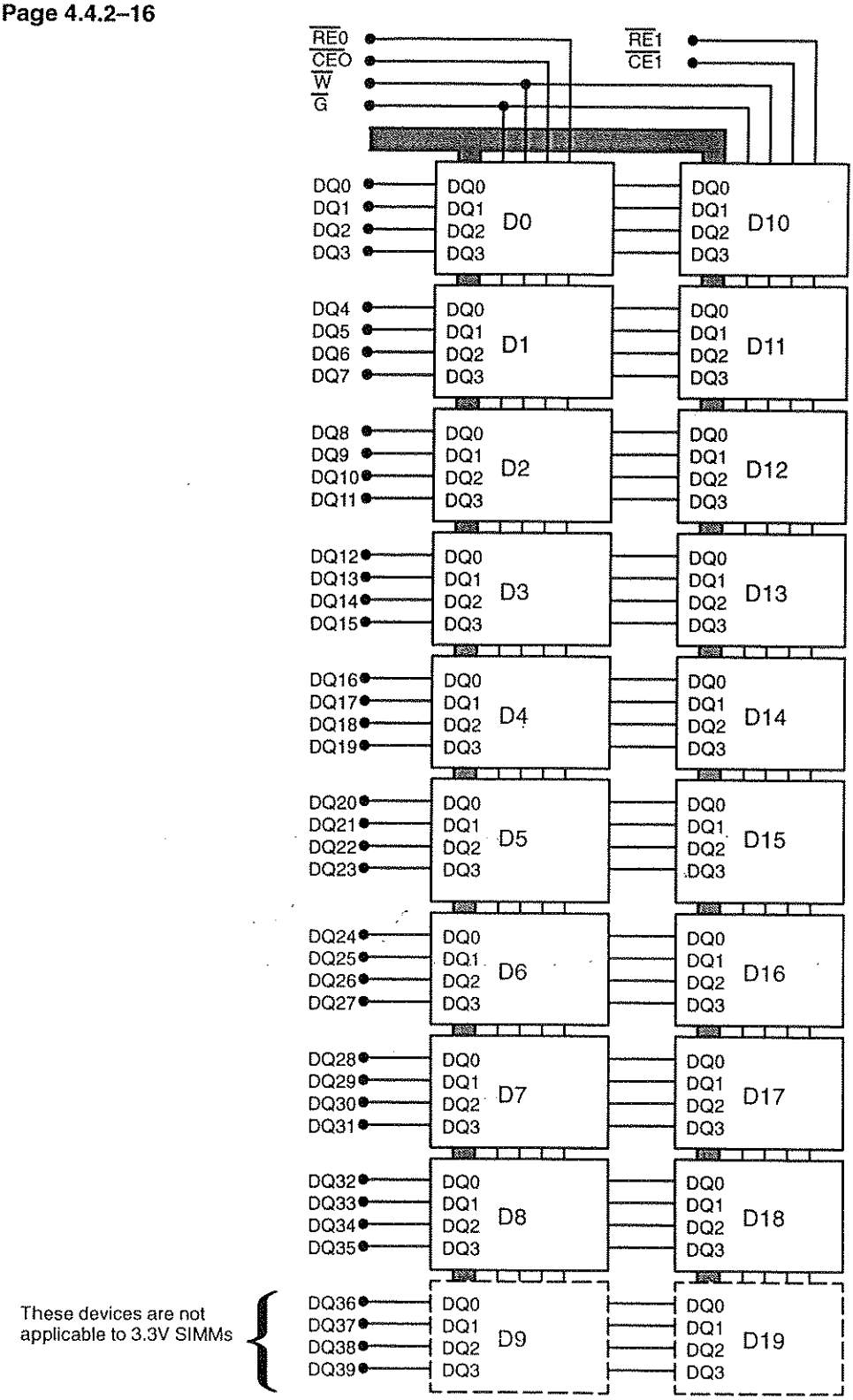


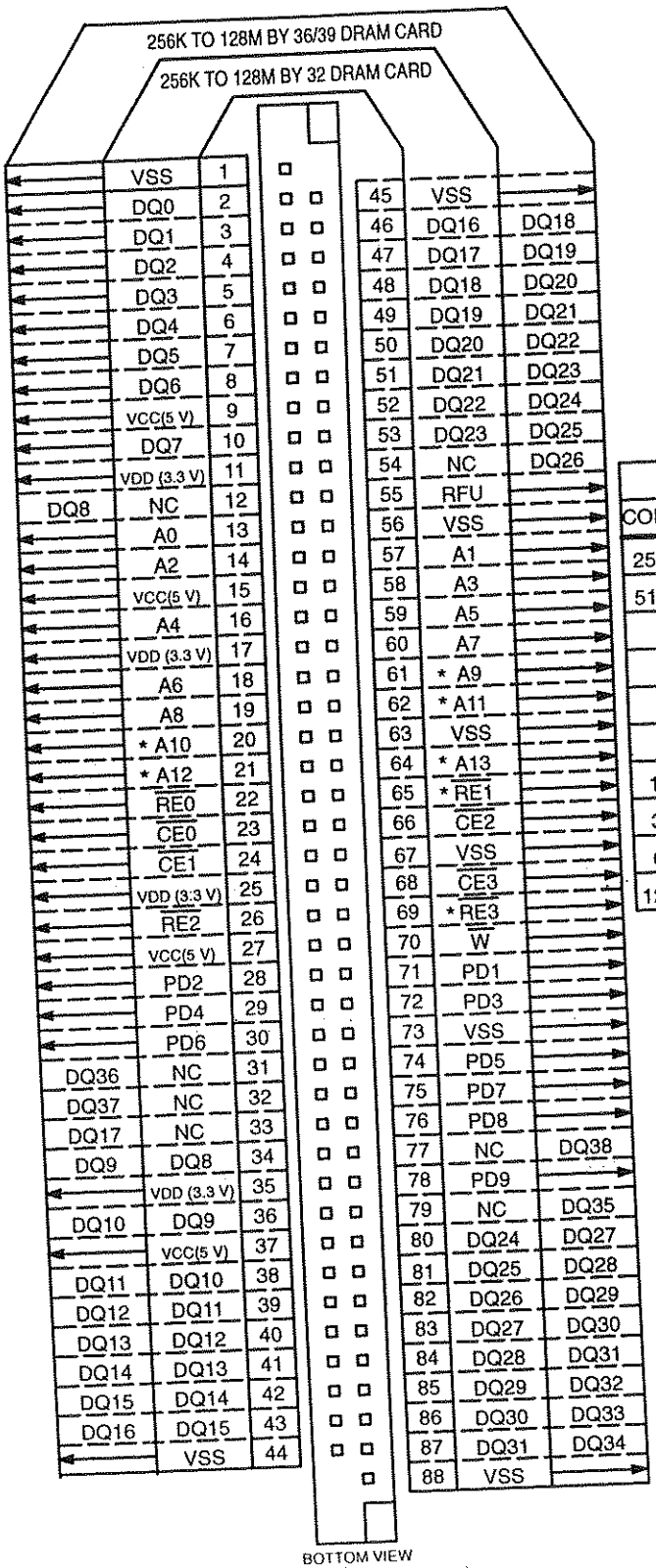
FIGURE 4.4.2–3 C
36/40 BIT 72 PIN ECC DRAM SIMM, 2 Banks with X4 DRAMs

4.4.3 – 88 PIN DRAM CARD FAMILIES

NOTE: There are two versions of this Card, shown in Figure 4.4.3–1 describing X 32 & 36/39 configurations, & 4.4.3–2 describing a X 40 configuration. They are similar but not fully compatible. Caution should be exercised in using these standards.

CAPACITY—256K TO 128M WORDS OF 32, 36, 39 OR 40 BITS
CONFIGURATION—16 Different Configurations Using 1mb, 4mb, 16mb, 64mb, & 256mb Devices
And With 2, Or 4 $\overline{\text{Re}}$ Clocks.
LOGIC FEATURES—The cards may be used with DATA BUS widths of X16/18 or X32/36 or X39— The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PIN ASSIGNMENTS, 32, 36, & 39 bit—Fig. 4.4.3–1 A
PRESENCE DETECT TABLE 32, 36, & 39 bit—Fig. 4.4.3–1 B
CONFIGURATION BLOCK DIAGRAMS 32, 36, & 39 bit—Figs. 4.4.3–1 C, 4.4.3–1 D, 4.4.3–1 E, & 4.4.3–1 F
PIN ASSIGNMENTS, 40 bit—Fig. 4.4.3–2 A
PRESENCE DETECT TABLE 40 bit—Fig. 4.4.3–2 B
CONFIGURATION BLOCK DIAGRAMS 40 bit—Figs. 4.4.3–2 C, 4.4.3–2 D, 4.4.3–2 E, & 4.4.3–2 F
PACKAGE—88 PIN JEDEC MEMORY CARD

XILINX EXHIBIT 1010
Page 246



	PD7	PD6
SPEED (tRAC)	75	30
100 nS	VSS	VSS
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PIN NUMBER						
CONFIGURATION	20	21	61	62	64	65	69
256K X 36, 2 $\overline{RE}$	NC	NC	NC	NC	NC	NC	NC
512K X 36, 4 $\overline{RE}$	NC	NC	NC	NC	NC	RE1	RE3
1M X 36, 2 $\overline{RE}$	NC	NC	A9	NC	NC	NC	NC
2M X 36, 4 $\overline{RE}$	NC	NC	A9	NC	NC	RE1	RE3
4M X 36, 2 $\overline{RE}$	A10	NC	A9	A11	NC	NC	NC
8M X 36, 4 $\overline{RE}$	A10	NC	A9	A11	NC	RE1	RE3
16M X 36, 2 $\overline{RE}$	A10	A12	A9	A11	NC	NC	NC
32M X 36, 4 $\overline{RE}$	A10	A12	A9	A11	NC	RE1	RE3
64M X 36, 2 $\overline{RE}$	A10	A12	A9	A11	A13	NC	NC
128M X 36, 4 $\overline{RE}$	A10	A12	A9	A11	A13	RE1	RE3

ADDRESS AND CLOCK PIN ASSIGNMENTS

Data Access Mode	PD9
FAST PAGE	NC
EDO	VSS

* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

FIGURE 4.4.3–1 A
88 PIN, BY 32 and 36/39 DRAM CARD PINOUT

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	CARD ADDR. REQ'D	RE ADDR.	CE ADDR.	AVAIL. PAGE DEPTH	AVERAGE REFRESH INTERVAL	NOTES
1 1 1 1 1	NO CARD							NO CARD INSTALLED
1 0 0 0 0	1 MB	256K X 1, 4, 16, 18	18	9	9	512	125 mS	
0 0 0 0 0	2 MB	256K X 1, 4, 16, 18	18	9	9	512	125 mS	
1 0 0 0 1	2 MB	512K X 8, 9	19	10	9	512	125 mS	
0 0 0 0 1	4 MB	512K X 8, 9	19	10	9	512	125 mS	
1 0 0 1 0	4 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 mS	
0 0 0 1 0	8 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 mS	
1 1 0 1 0	4 MB	1M X 16, 18	20	12	8	256	62 mS	
0 1 0 1 0	8 MB	1M X 16, 18	20	12	8	256	62 mS	
1 0 0 1 1	8 MB	2M X 8, 9	21	11	10	1024	125 mS	
0 0 0 1 1	16 MB	2M X 8, 9	21	11	10	1024	125 mS	
1 0 1 0 0	16 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 mS	SUPPORT 12/10 AND 11/11 ADDRESS
0 0 1 0 0	32 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 mS	SUPPORT 12/10 AND 11/11 ADDRESS
1 0 1 0 1	32 MB	8M X 8, 9	23	13	*11	**1024	62 mS	SUPPORT 13/10 AND 12/11 ADDRESS
0 0 1 0 1	64 MB	8M X 8, 9	23	13	*11	**1024	62 mS	SUPPORT 13/10 AND 12/11 ADDRESS
1 0 1 1 0	64 MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 mS	SUPPORT 13/11 AND 14/10 ADDRESS
0 0 1 1 0	128MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 mS	SUPPORT 13/11 AND 14/10 ADDRESS

* INDICATES REDUNDANT ADDRESS THAT MUST BE PROVIDED AT CE\ TIME (TO ALLOW USE OF MIXED DRAM ADDRESSING)
** PAGE DEPTH DETERMINED BY THE SMALLEST CE\ ADDRESS DRAM
*** ALL DENSITIES ASSUME 4 BYTE CARD DATA WIDTH (32 OR 36 BITS)
FOR THE PDn PINS, 1 = NC, 0 = VSS

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

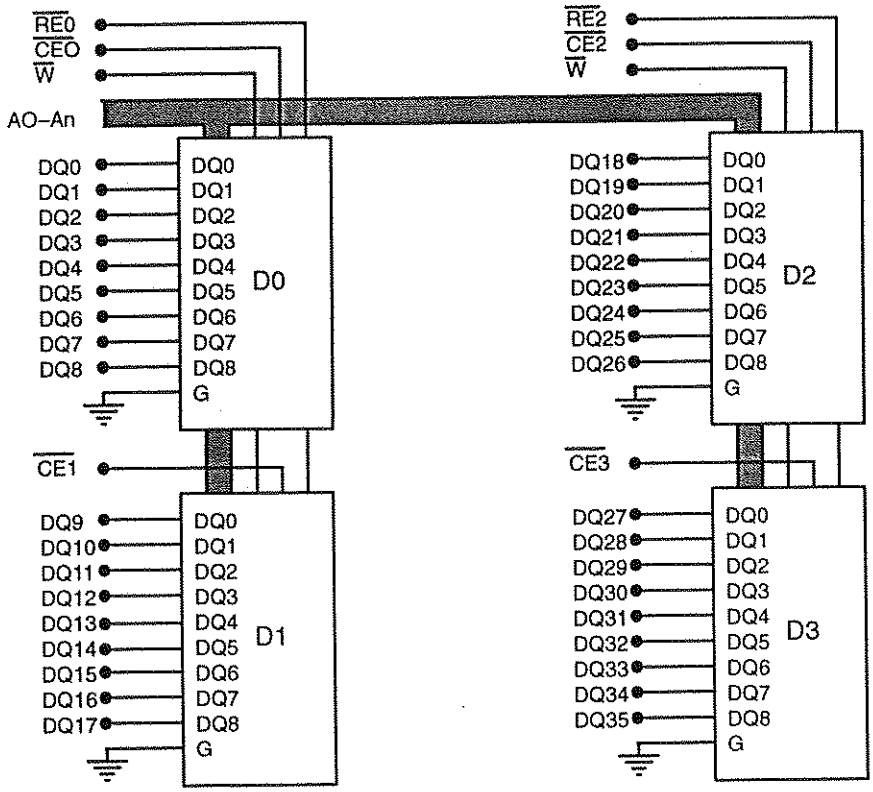
BASE DEVICE	CONFIG'N	PIN NUMBER 9	11	15	17	25	27	35	37
1M	256K X 36, 2 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
1M	512K X 36, 4 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
4M	1M X 36, 2 $\overline{RE}$	5 V,NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
4M	2M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	4M X 36, 2 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	8M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
64M	16M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
64M	32M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	64M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	128M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC

VDD POWER PIN ASSIGNMENT TABLE

FIGURE 4.4.3–1 B
88 PIN, BY 32 AND 36/39 DRAM CARD CONFIGURATION TABLES

Release 6–7

BLOCK DIAGRAM for 512K /2M/8M/32M X 36 or 1M/4M/16M/64M X 18 USING X8 or X9 DRAM



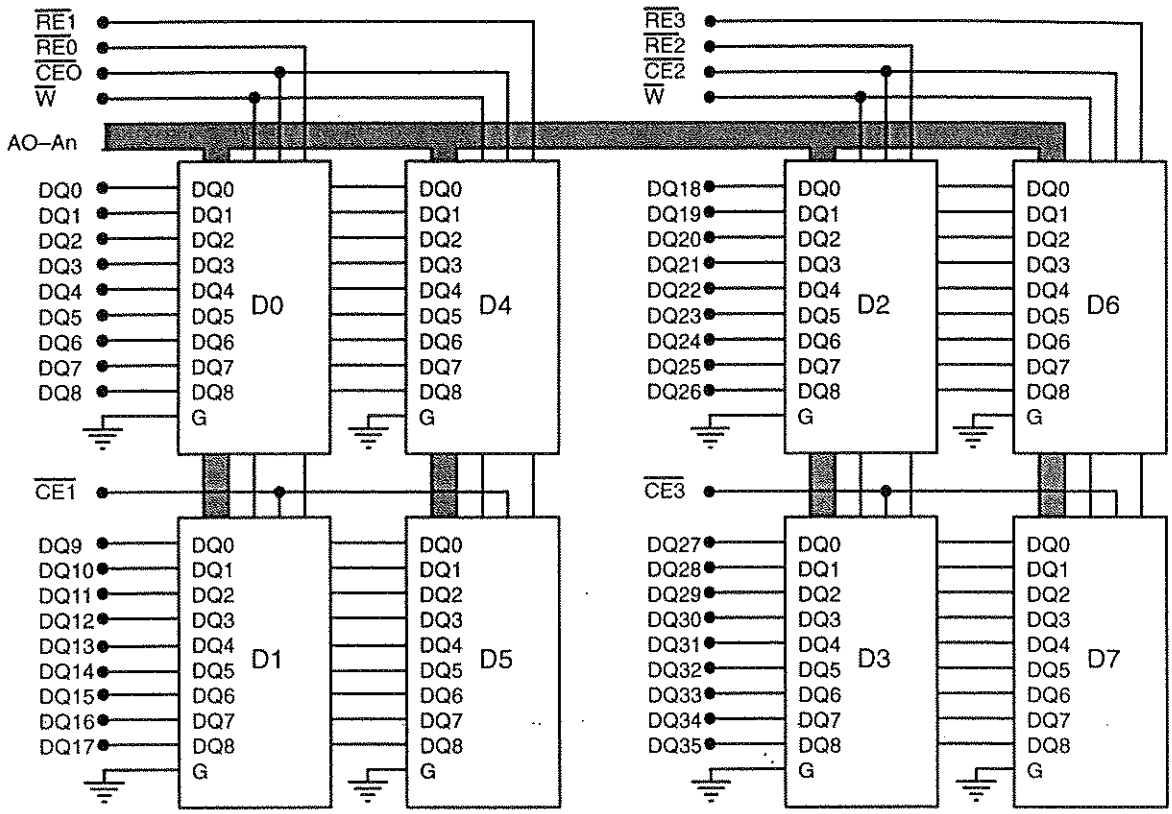
WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D3	ADDRESS
512K X 36 or 1M X 18	4M (X9)	A0 – A9
2M X 36 or 4M X 18	16M (X9)	A0 – A10
8M X 36 or 16M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 C
88 PIN, BY 36, DRAM CARD 1 BANK USING BY 9 DEVICES

BLOCK DIAGRAM for 1M /4M/16M/64M X 36 or 2M/8M/32M/128M X 18 USING X8 or X9 DRAM



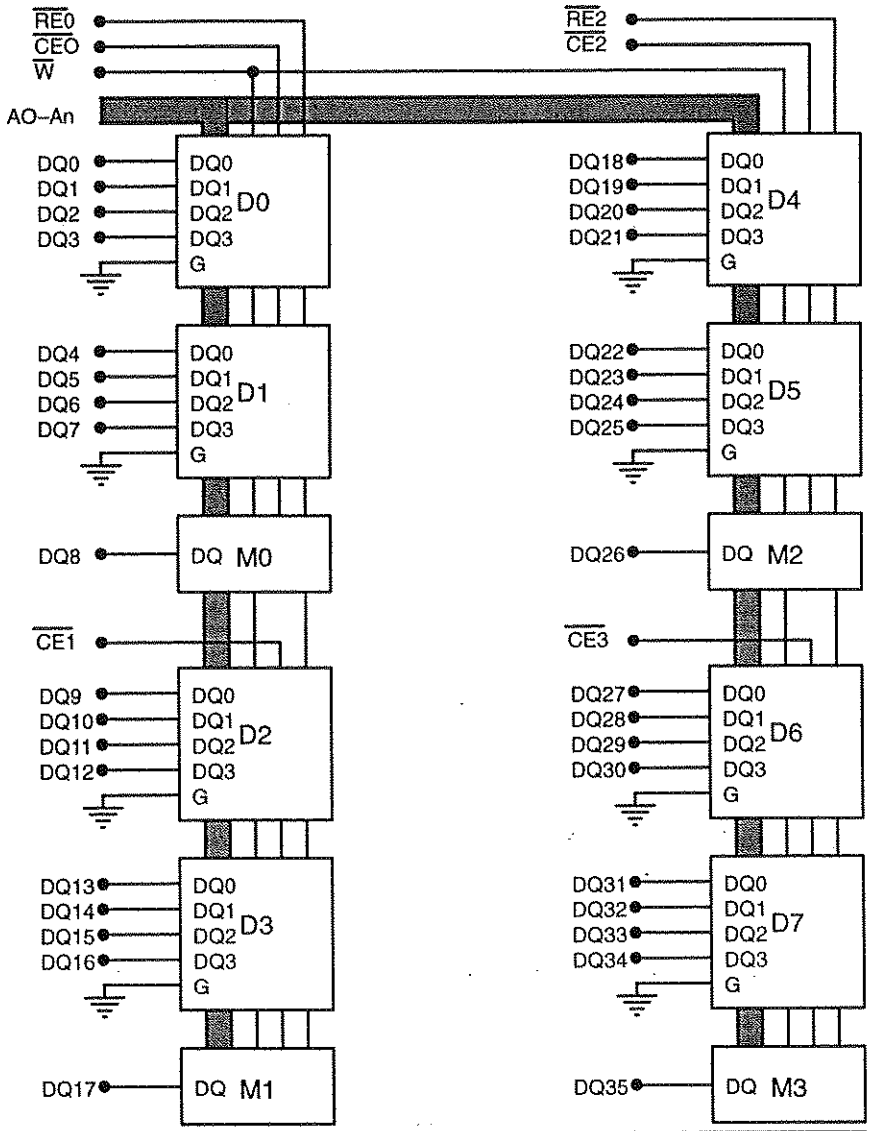
WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D7	ADDRESS
1M X 36 or 2M X 18	4M (X9)	A0 – A9
4M X 36 or 8M X 18	16M (X9)	A0 – A10
16M X 36 or 32M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ and $\overline{RE3}$) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ and $\overline{RE3}$) will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 D
88 PIN, BY 36, DRAM CARD 2 BANK USING BY 9 DEVICES

BLOCK DIAGRAM for 256K /1M/4M/16M/64M X 36 or 512K/2M/8M/32M/128M X 18 USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D7	M0 – M3	ADDRESS
256K X 36 or 512K X 18	1M (X4)	256K (X1)	A0 – A8
1M X 36 or 2M X 18	4M (X4)	1M (X1)	A0 – A9
4M X 36 or 8M X 18	16M (X4)	4M (X1)	A0 – A11
16M X 36 or 32M X 18	64M (X4)	16M (X1)	A0 – A13

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

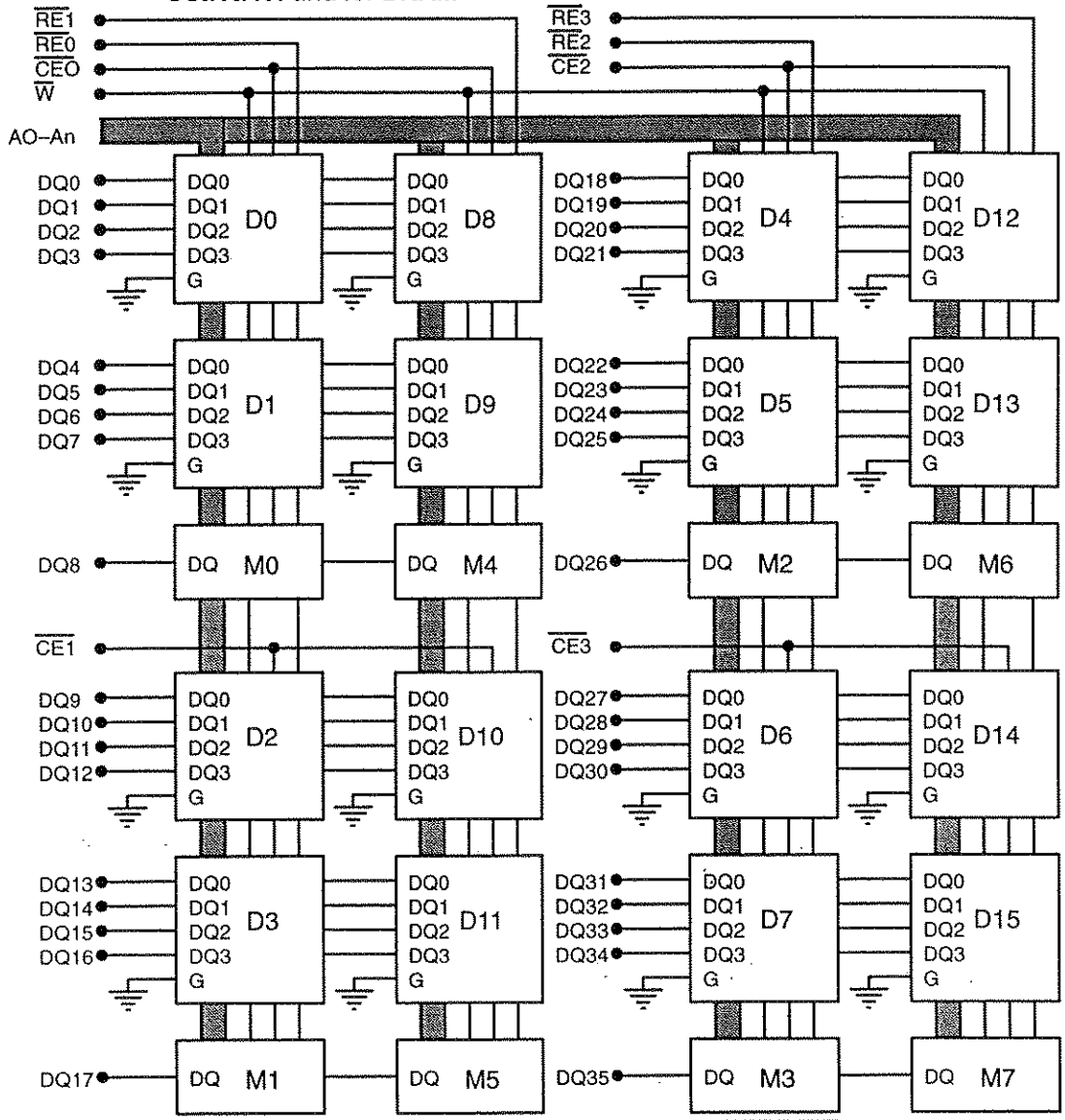
note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 E

88 PIN, 36, DRAM CARD 1 BANK USING BY 4 & BY 1 DEVICES

BLOCK DIAGRAM for 512K/2M/8M/32M/32M/128M X 36 or 1M/4M/16M/256M X 18 USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D15	M0 – M7	ADDRESS
512K X 36 or 1M X 18	1M (X4)	256K(X1)	A0 – A8
2M X 36 or 4M X 18	4M (X4)	1M (X1)	A0 – A9
8M X 36 or 16M X 18	16M (X4)	4M (X1)	A0 – A11
32M X 36 or 64M X 18	64M (X4)	16M (X1)	A0 – A13

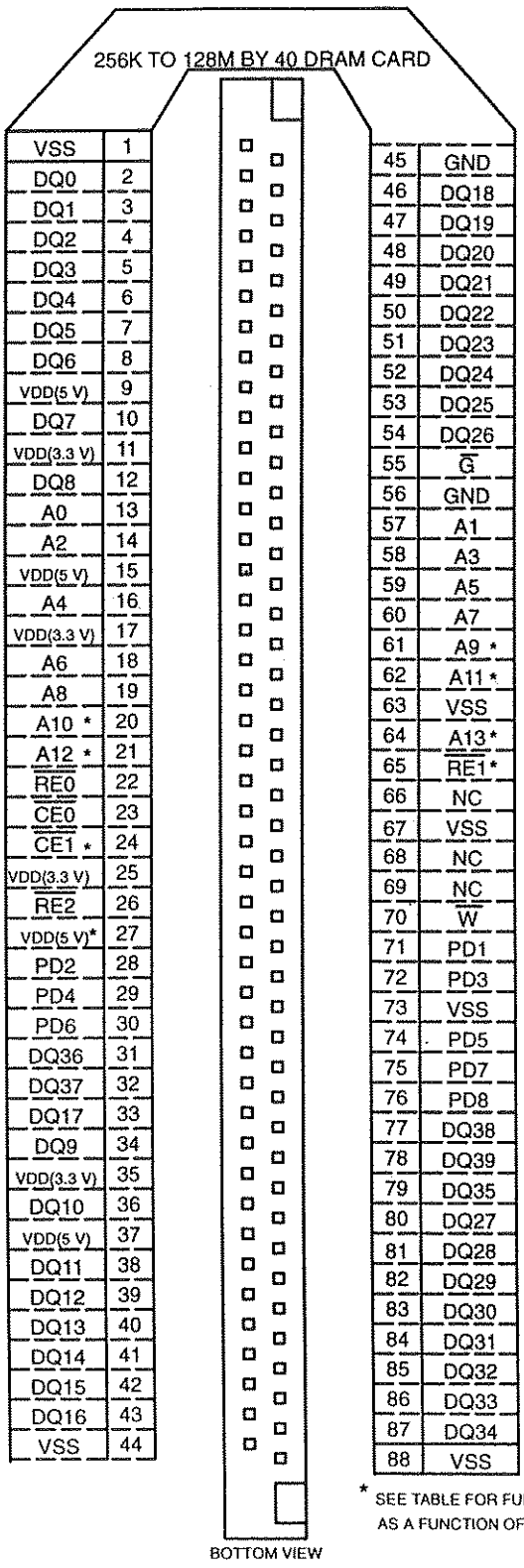
* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ AND $\overline{RE3}$) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card,
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ and $\overline{RE3}$) will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 F

88 PIN, BY 36 DRAM CARD 2 BANK USING BY 4 & BY 1 DEVICES



* SEE TABLE FOR FUNCTIONAL ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

Pin Assignment, Cards based on X4 DRAM

	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
256K X 40 (1M)	NC	NC	NC	5 V, NC	NC	NC	NC	NC
512K X 40 (1M)	NC	NC	$\overline{CE1}$	5 V, NC	NC	NC	NC	$\overline{RE1}$
1M X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
2M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
4M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
8M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
16M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
32M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
64M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
128M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

Pin Assignment, Cards based on X8 DRAM

	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
512K X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
1M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
2M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
4M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
8M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
16M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
32M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
64M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

ADDRESS AND CLOCK PIN ASSIGNMENTS

FIGURE 4.4.3–2 A
88 PIN, BY 40 DRAM CARD

XILINX EXHIBIT 1010
Page 253

	PD7	PD6
SPEED (tRAC)	P 75	P 30
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PD8
REFRESH MODE	P 76
80 nS	VSS
70 nS	NC

PD REFRESH MODE TABLE

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	RE ADDR.	CE ADDR.	REFRESH PERIOD (mS) NORMAL	SLOW
1 1 1 1 1	NO CARD					
1 0 0 0 0	1 MB	256K X 4	9	9	8	64
0 0 0 0 0	2 MB	256K X 4	9	9	8	64
1 0 0 0 1	2 MB	512K X 8	10	9	16	128
0 0 0 0 1	4 MB	512K X 8	10	9	16	128
1 0 0 1 0	4 MB	1M X 4	10	10	16	128
0 0 0 1 0	8 MB	1M X 4	10	10	16	128
1 0 0 1 1	8 MB	2M X 8	11	10	32	256
0 0 0 1 1	16 MB	2M X 8	11	10	32	256
1 0 1 0 0	16 MB	4M X 4	11/12	11/10	64	256
0 0 1 0 0	32 MB	4M X 4	11/12	11/10	64	256
1 0 1 0 1	32 MB	8M X 8	12/13	11/10	TBD	TBD
0 0 1 0 1	64 MB	8M X 8	12/13	11/10	TBD	TBD
1 0 1 1 0	64 MB	16M X 4	13	11	TBD	TBD
0 0 1 1 0	128 MB	16M X 4	13	11	TBD	TBD
1 0 1 0 1	128 MB	32M X 8	TBD	TBD	TBD	TBD
0 0 1 0 1	256 MB	32M X 8	TBD	TBD	TBD	TBD
1 0 1 1 0	256 MB	64M X 4	TBD	TBD	TBD	TBD
0 0 1 1 0	512 MB	64M X 4	TBD	TBD	TBD	TBD

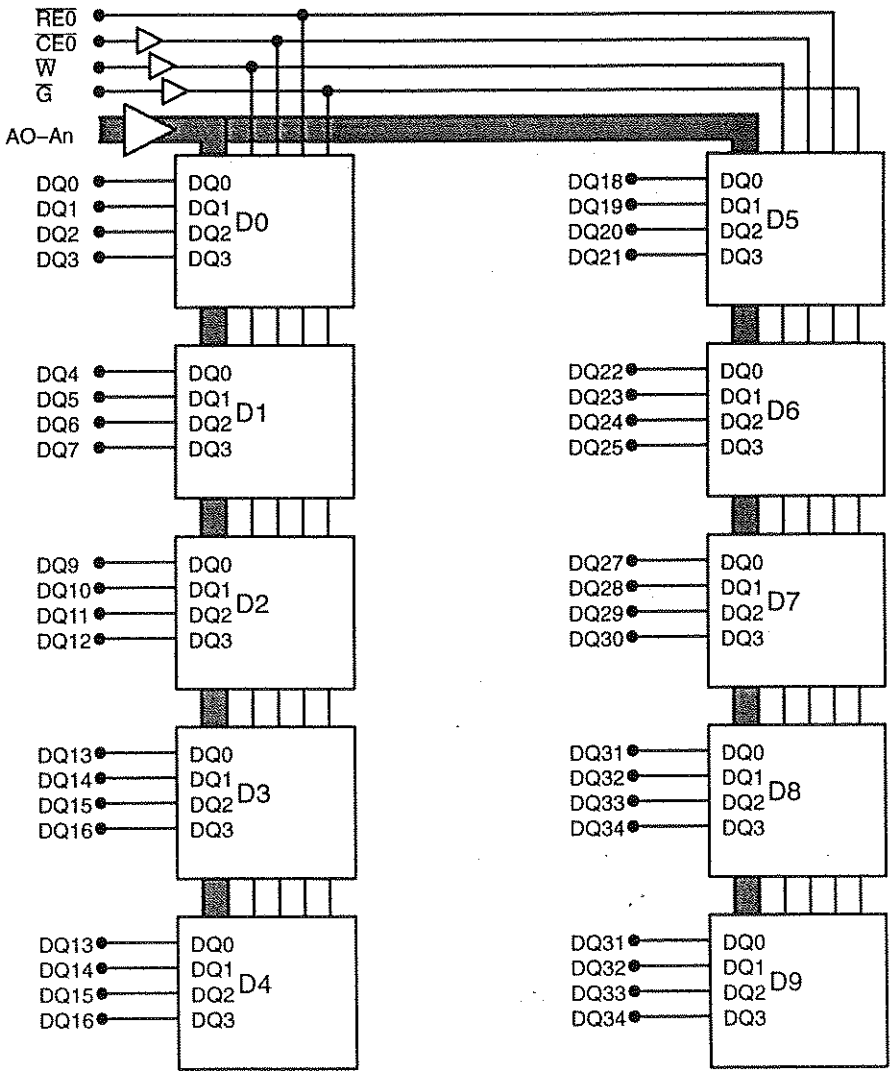
FOR THE PDn PINS, 1 = NC, 0 = VSS
NOTE: In the above address table, optional address configurations are given for some devices to allow for different approved refresh counts.

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

NOTE: The DRAM densities are shown in parentheses (xxxM)

FIGURE 4.4.3–2 B
88 PIN, BY 40 DRAM CARD PD TRUTH TABLE

BLOCK DIAGRAM for 256K/1M/4M/16M/64M X 40 USING X4 DRAM



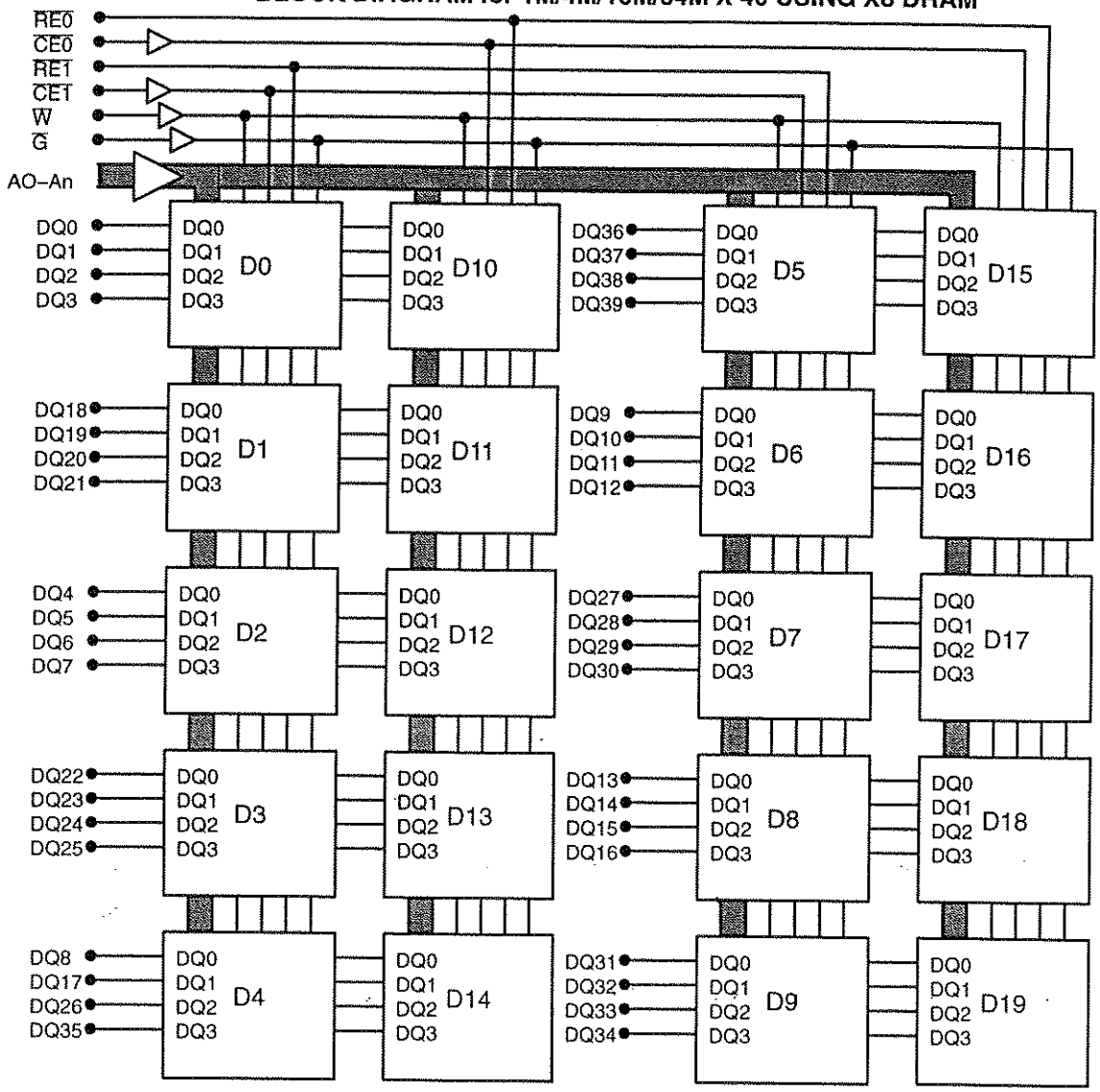
WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD	OPTIONAL ADDRESS
256K X 40	1M (X4)	A0 – A8	NA
1M X 40	4M (X8)	A0 – A9	NA
4M X 40	16M (X8)	A0 – A10	A0–A11
16M X 40	64M (X8)	A0 – A11	A0–A12
64M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card.

FIGURE 4.4.3–2 C
88 PIN, BY 40 DRAM CARD 1 BANK USING BY 4 DEVICES

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



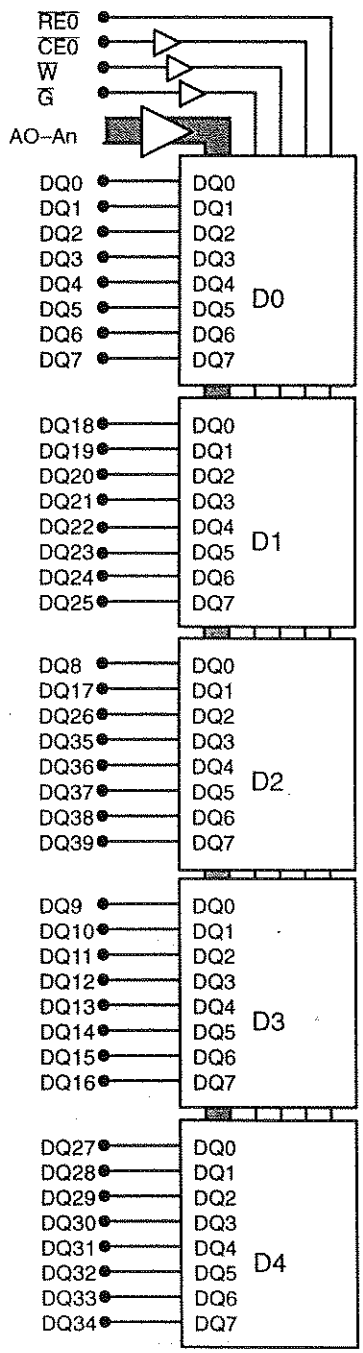
WORD ORGANIZATION	*Base Memory Device D0 to D19	ADDRESS FIELD	OPTIONAL ADDRESS
512K X 40	1M (X4)	A0 – A8	NA
2M X 40	4M (X8)	A0 – A9	NA
8M X 40	16M (X8)	A0 – A10	A0–A11
32M X 40	64M (X8)	A0 – A11	A0–A12
128M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 D
88 PIN, BY 40 DRAM CARD 2 BANK USING BY 4 DEVICES

BLOCK DIAGRAM for 512K/2M/8M/32M X 40 USING X8 DRAM



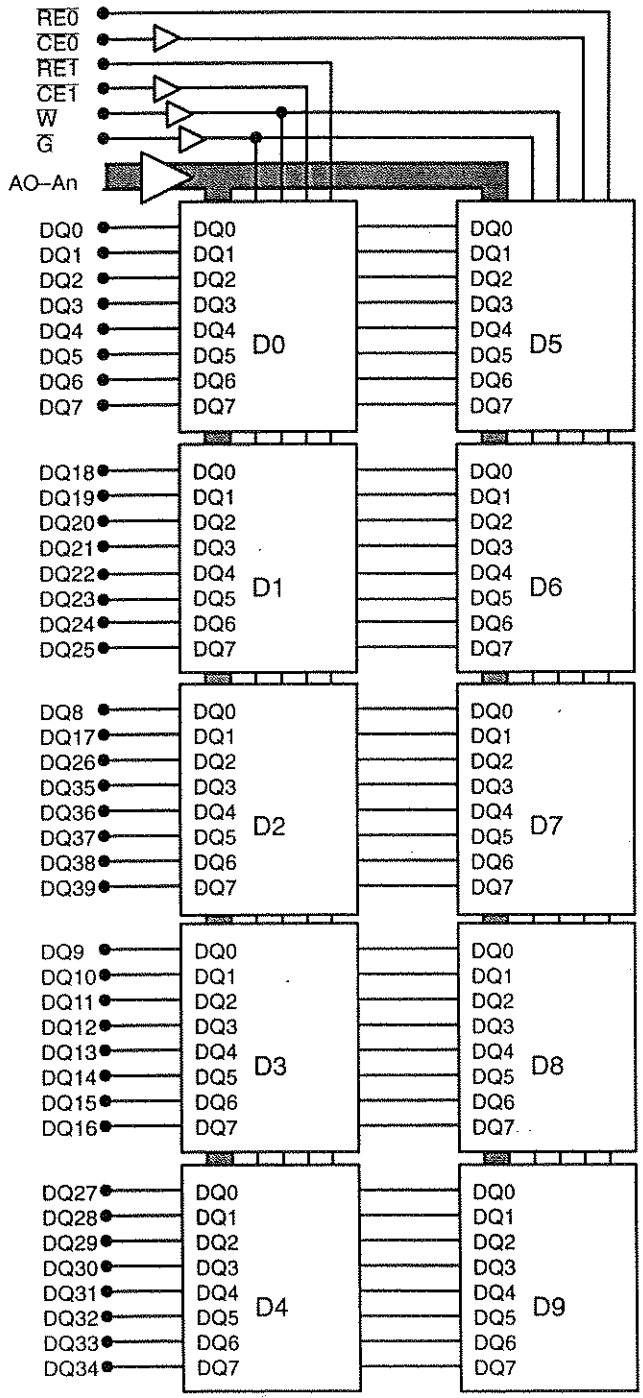
WORD ORGANIZATION	*Base Memory Device D0 to D4	ADDRESS FIELD
512K X 40	4M (X8)	A0 – A9
2M X 40	16M (X8)	A0 – A10
8M X 40	8M (X8)	A0 – A11
32M X 40	32M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 E
88 PIN, BY 40 DRAM CARD 1 BANK USING BY 8 DEVICES

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD
1M X 40	4M (X8)	A0 – A9
4M X 40	16M (X8)	A0 – A10
16M X 40	64M (X8)	A0 – A11
64M X 40	256M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 F
88 PIN, BY 40 DRAM CARD 2 BANK USING BY 8 DEVICES

4.4.4 – 72 PIN DRAM SO–DIMM FAMILY

CAPACITY—512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 32, OR 36 BITS
DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—32 BIT
—36 BIT
CONFIGURATION—3 Different Configurations are defined using various combinationa of X4, X8, X9 memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" features that consist of output pins in the PDn field that supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
VDD CHOICE—The choice of VDD value will be determined by the memory device used and defined by a mechanical interlock KEY
ENHANCEMENTS: In Release 6 Refresh was defined and new configurations were added.
PACKAGE—72 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.4–A
CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.4.4–A
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.4–B through 4.4.4–D

PIN NAME	PIN #	PIN #	PIN NAME
VSS	1	2	DQ0
DQ1	3	4	DQ2
DQ3	5	6	DQ4
DQ5	7	8	DQ6
DQ7	9	10	&VDD
PD1	11	12	A0
A1	13	14	A2
A3	15	16	A4
A5	17	18	A6
A10	19	20	@ DQ8, NC
DQ9	21	22	DQ10
DQ11	23	24	DQ12
DQ13	25	26	DQ14
DQ15	27	28	A7
A11	29	30	&VDD
A8	31	32	A9
$\overline{RE3}$	33	34	$\overline{RE2}$
DQ16	35	36	@ DQ17, NC
DQ18	37	38	DQ19
VSS	39	40	$\overline{CE0}$
$\overline{CE2}$	41	42	$\overline{CE3}$
$\overline{CE1}$	43	44	$\overline{RE0}$
$\overline{RE1}$	45	46	A12
$\overline{W}$	47	48	A13
DQ20	49	50	DQ21
DQ22	51	52	DQ23
DQ24	53	54	DQ25
@ DQ26, NC	55	56	DQ27
DQ28	57	58	DQ29
DQ31	59	60	DQ30
&VDD	61	62	DQ32
DQ33	63	64	DQ34
@ DQ35, NC	65	66	PD2
PD3	67	68	PD4
PD5	69	70	PD6
PD7	71	72	VSS

TOP VIEW

PRESENCE DETECT TRUTH TABLE								Ave Refresh Interval (µs)	
MOD CONFIG	DEVICE	ADDR		PD4	PD3	PD2	PD1		
		ROW	COL	Pin 68	Pin 67	Pin 66	Pin 11	Normal	Long
NO MODULE				O	O	O	O		
512K X 32/36	512K X 8/9	10	9	O	S	S	S	15.6	125
1M X 32/36	512K X 8/9	10	9	S	S	S	S	15.6	125
1M X 32/36	1M X 2/4/16/18	10	10	O	S	S	O	15.6	125
1M X 32/36	1M X 16/18	12	8	O	O	S	O	15.6	31.2
2M X 32/36	1M X 2/4/16/18	10	10	S	S	S	O	15.6	125
2M X 32/36	1M X 16/18	12	8	S	O	S	O	15.6	31.2
2M X 32/36	2M X 8/9	11	10	O	S	O	S	15.6	62.4
4M X 32/36	2M X 8/9	11	10	S	S	O	S	15.6	62.4
4M X 32/36	4M X 2/416/18	12*	10*	O	S	O	O	15.6	31.2
	or	11*	11*						62.4
8M X 32/36	4M X 2/4/16/18	12*	10*	S	S	O	O	15.6	31.2
	or	11*	11*						62.4
8M X 32/36	8M X 8/9	12	11	O	O	S	S	15.6	31.2
16M X 32/36	8M X 8/9	12	11	S	O	S	S	15.6	31.2
16M X 32/36	16M X 2/4/16/18	13	11	O	O	O	S	15.6	TBD
32M X 32/36	16M X 2/4/16/18	13	11	S	O	O	S	15.6	TBD
32M X 32/36	32M X 8/9	TBD	TBD	O	S	S	S	TBD	TBD
64M X 32/36	32M X 8/9	TBD	TBD	S	S	S	S	TBD	TBD
64M X 32/36	64M X 2/4	TBD	TBD	O	S	S	O	TBD	TBD

* Indicates that 12/10 or 11/11 may be used on this assembly. The application must determine the appropriate addressing version or provide redundant (12/11) addressing to allow the use of either.

** The DRAM organization is provided for reference and clarification only. X2 implies X2 DRAM with 2 $\overline{CE}$s. X4 can be either X4 or X4 with 4 CEs. X1 options are allowed if approved dimensions are met.

O = OPEN CIRCUIT (NO CONNECTION)

S = CONNECTED TO VSS

	PD6	PD5
SPEED (tRAC)	Pin 70	Pin 69
80 ns	S	O
70 ns	O	S
60 ns	O	O
50 ns	S	S
PD SPEED TABLE		

	PD7
REFRESH MODE	Pin 71
NORMAL	O
* SELF-REFRESH	S
REFRESH MODE	

*SELF-REFRESH/LONG INTERVA

&Note: This standard allows for the use of different values of VDD depending on the memory device requirements. A mechanical key is used to define the voltage as described in the package registration document, MO–160.

@ These Pins are NC for X32, and DQn for X36 modules

FIGURE 4.4.4–A
32 OR 36 BIT DRAM SO–DIMM PINOUT

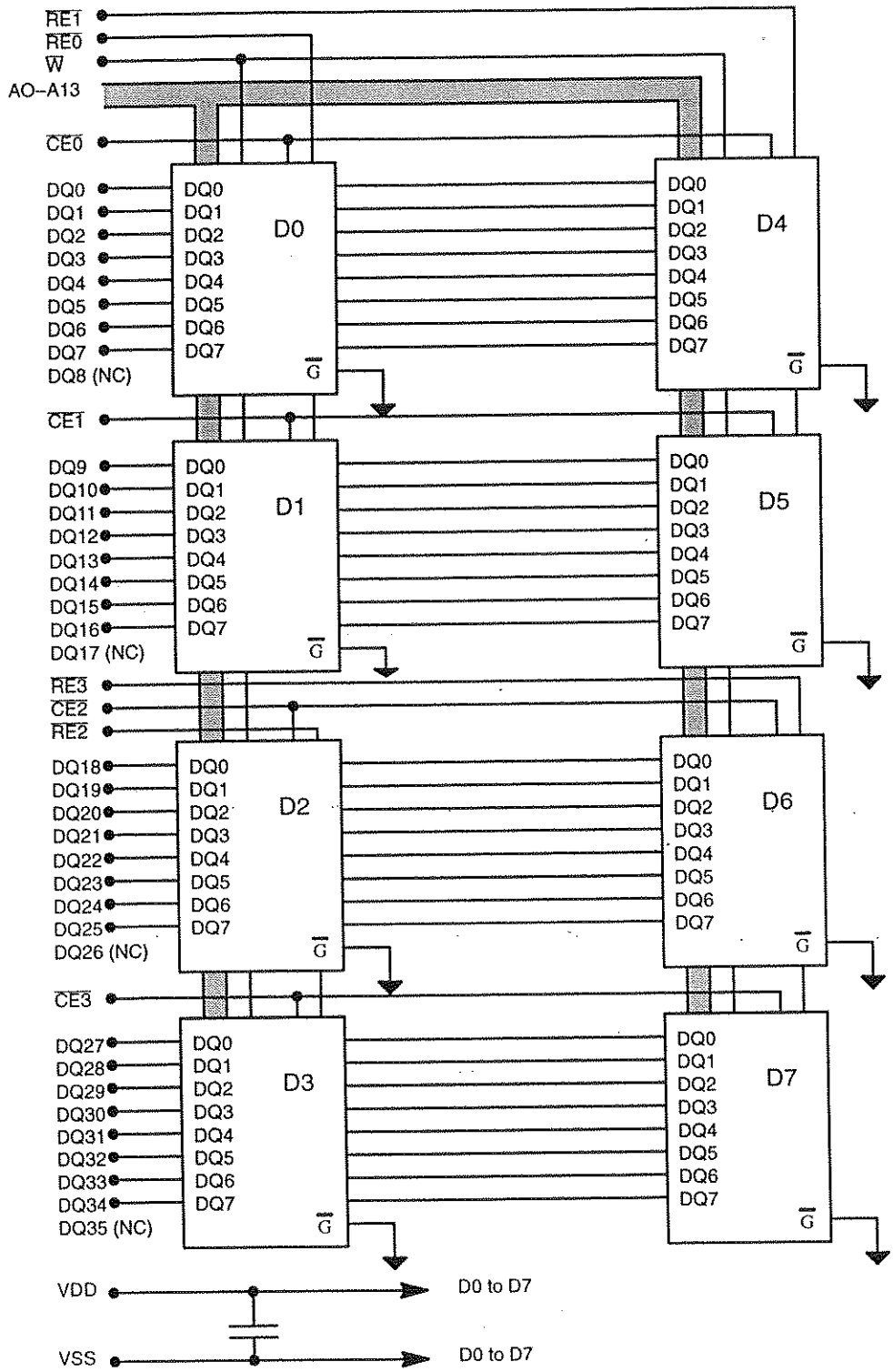


FIGURE 4.4.4–B
BLOCK DIAGRAM for X 32 DRAM SO–DIMM USING X8 DRAM
Release 5c7

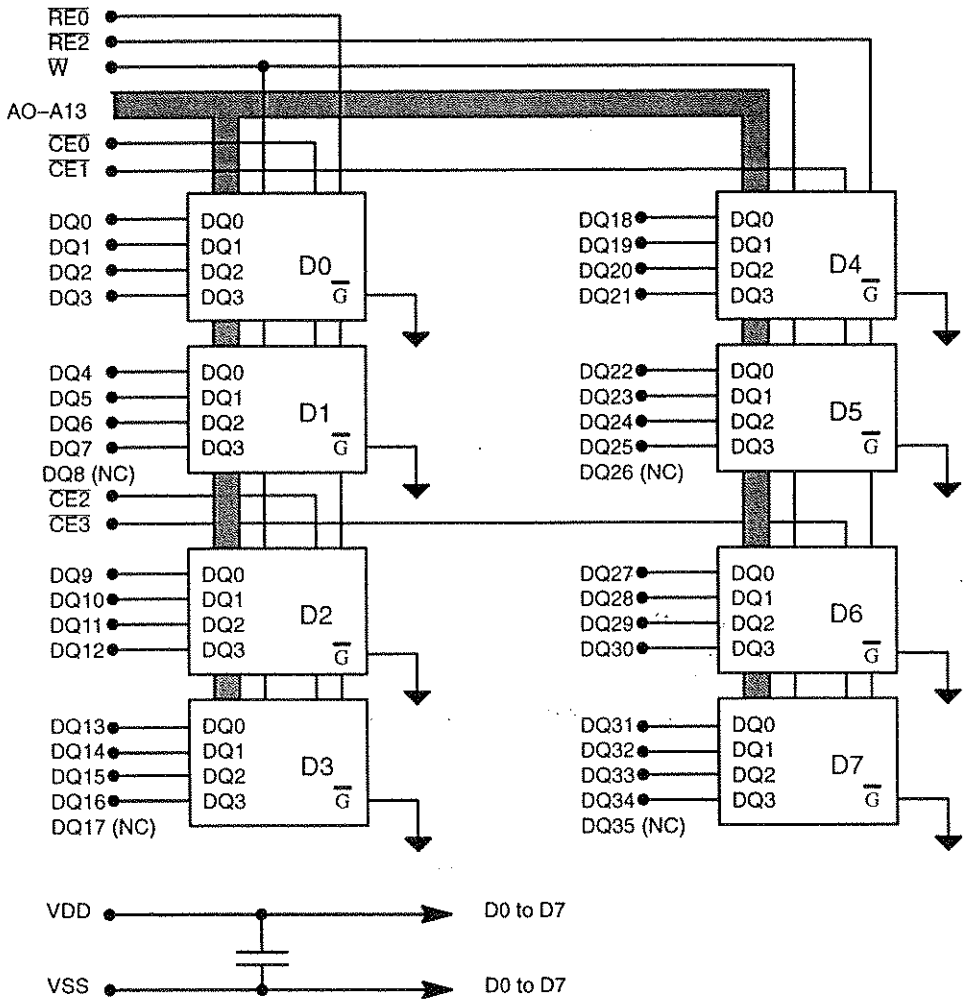


FIGURE 4.4.4–C
BLOCK DIAGRAM for X 32 DRAM SO–DIMM USING X4 DRAM

Release 5c7

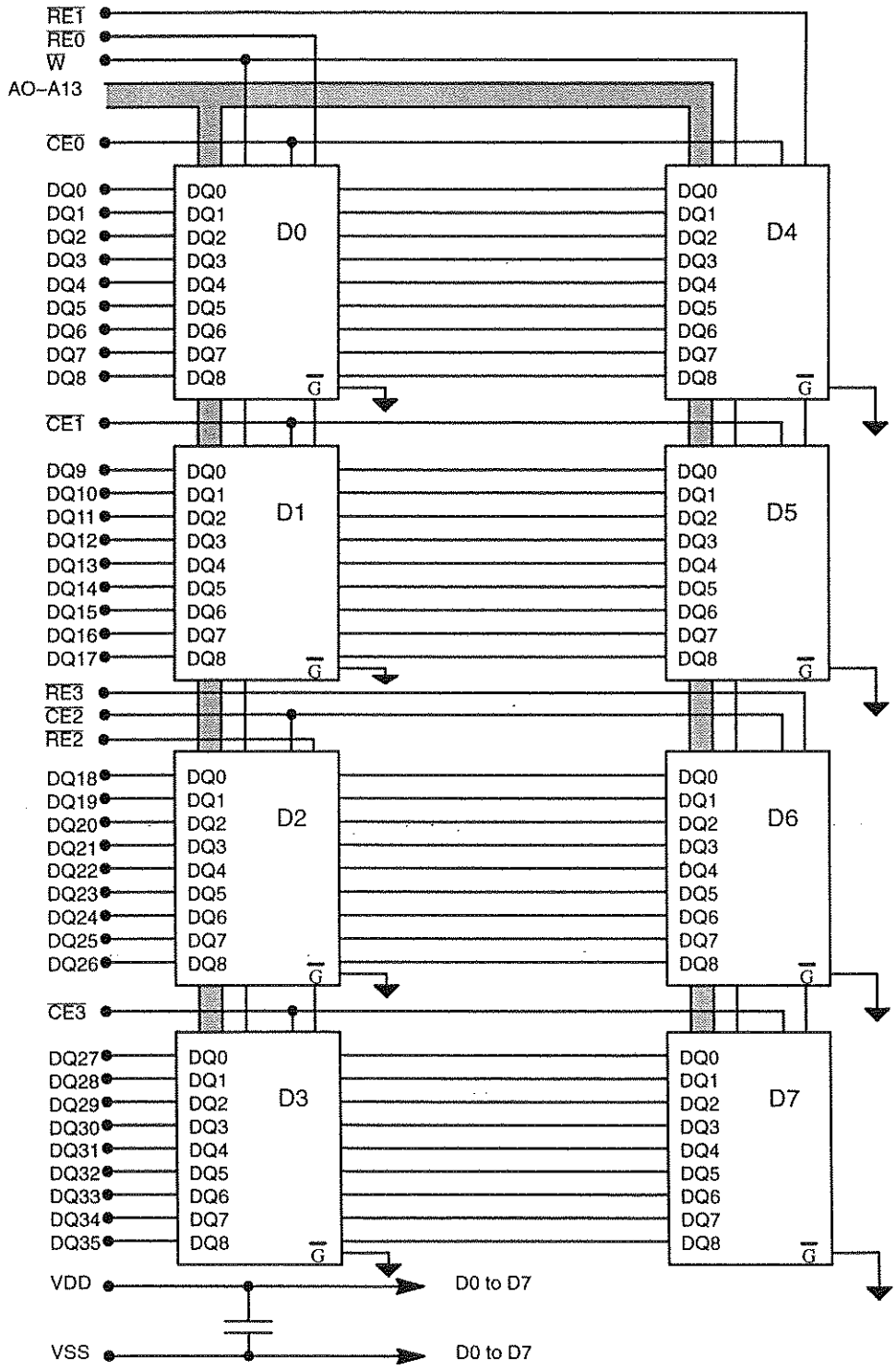


FIGURE 4.4.4–D
BLOCK DIAGRAM for X 36 DRAM SO–DIMM USING X9 DRAM
Release 5c7

4.4.5 – 88 PIN DRAM SO–DIMM FAMILY

CAPACITY—512K TO 128M WORDS OF 32, OR 36 BITS
DATA CONFIGURATIONS—Two DATA Word configurations are defined: X32 & X36
CONFIGURATION—4 Different Configurations are defined using various combinationa of X1, X4, X8, memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" features that consist of output pins in the PDn field that supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
VDD CHOICE—The choice of VDD value will be determined by the memory device used and defined by a mechanical interlock KEY
PACKAGE—88 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.4.5–A
PD, CAPACITY / DEVICE CONFIGURATION TABLES—Fig. 4.4.5–B
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.5–C through 4.4.5–F

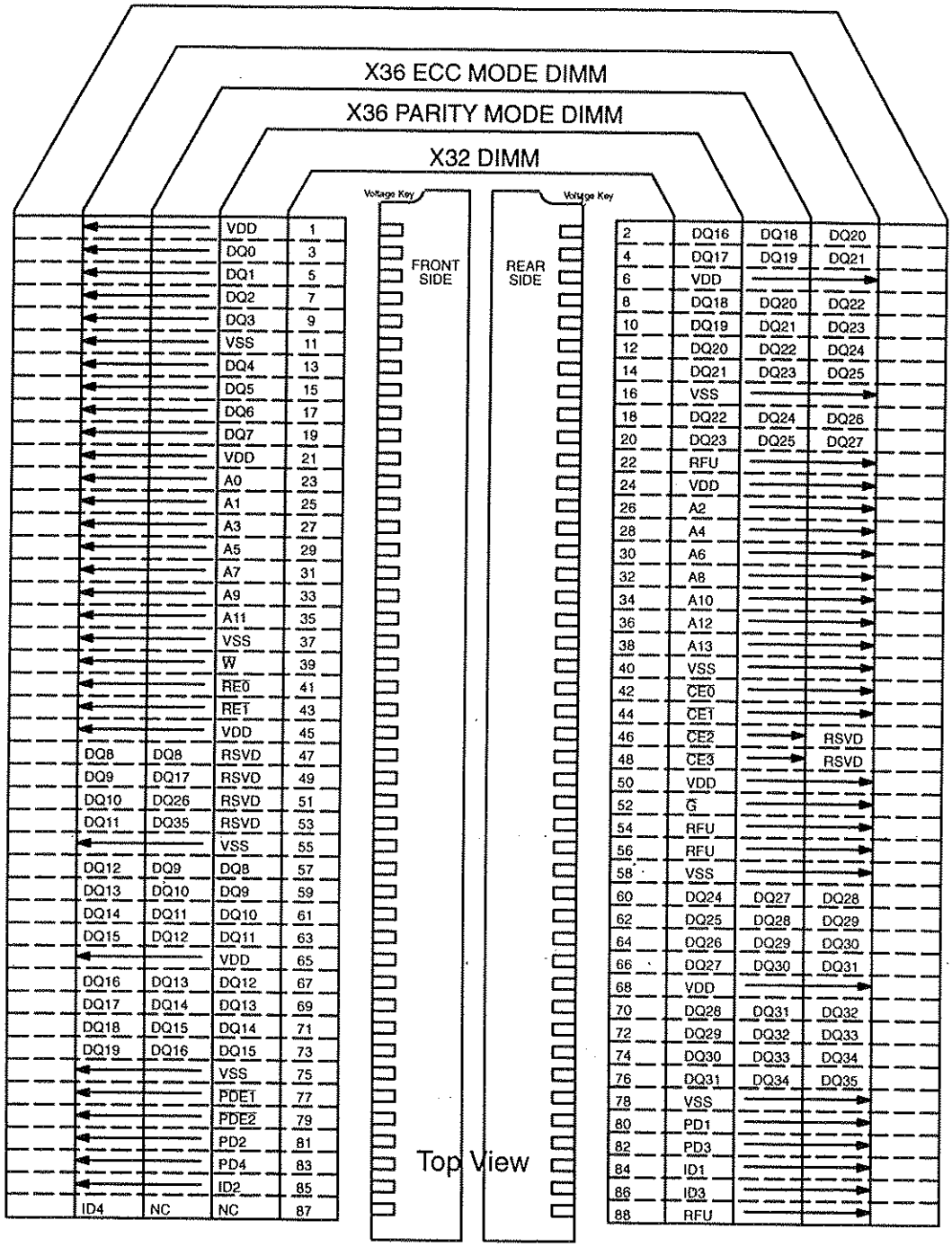


FIGURE 4.4.5–A
X32 and X36 DRAM SO–DIMM PINOUT

Release 6c7

PREOENCE DETECT TRUTH TABLE							
MOD CONFIG	DEVICE	ADDR		PD14	PD13	PD12	PD11
		ROW	COL				
NO MODULE				1	1	1	1
512K X 32/36	512K X 8/9	10	9	1	0	0	0
1M X 32/36	512K X 8/9	10	9	0	0	0	0
1M X 32/36	1M X 1/4/16/18	10	10	1	0	0	1
1M X 32/36	1M X 16/18	12	8	1	0	1	0
2M X 32/36	1M X 1/4/16/18	10	10	0	0	0	1
2M X 32/36	1M X 16/18	12	8	0	0	1	0
2M X 32/26	2M X 1/2/8/9	11	10	1	0	1	1
4M X 32/36	2M X 1/2/8/9	11	10	0	0	1	1
4M X 32/36	4M X 4/16/18	12	10	1	1	0	0
4M X 32/36	4M X 1/4/16/18	11	11	1	1	0	1
8M X 32/36	4M X 4/16/18	12	10	0	1	1	1
8M X 32/36	4M X 1/4/16/18	11	11	0	1	0	1
8M X 32/36	8M X 1/2/8/9	12	11	1	1	1	0
16M X 32/36	8M X 1/2/8/9	12	11	0	1	1	0
16M X 32/36	16M X 1/4/16/18	13/12	11/12	1	0	0	0
32M X 32/36	16M X 1/4/16/18	13/12	11/12*	0	0	0	0
32M X 32/36	32M X 1/2/8/9	TBD	TBD	1	0	0	1
64M X 32/36	32M X 1/2/8/9	TBD	TBD	0	0	0	1
64M X 32/36	64M X 1/4	TBD	TBD	1	0	1	0
128M X 32/36	64M X 1/4	TBD	TBD	0	0	1	0

NOTE 1 – * This addressing includes a redundant address to allow mixing of 13/11 and 12/12 devices.

NOTE 2 – The PDmn & IDn values given in the tables have the following significance: 1 = Driven to LOGIC HIGH for PD, OPEN CIRCUIT FOR ID
0 = Driven to LOGIC LOW for PD, SHORT TO VSS FOR ID

NOTE 3 – #The PDmn values are multiplexed onto the PDn pins under the control of $\overline{PDE1}$ and $\overline{PDE2}$ as follows:
PD11 ⇒ PD14 to PD1 ⇒ PD4 WITH $\overline{PDE1}$ = LOW
PD21 ⇒ PD24 to PD1 ⇒ PD4 WITH $\overline{PDE2}$ = LOW

NOTE4: This standard allows for the use of different values of VDD depending on the memory device requirements. A mechanical key is used to define the voltage as described in the package registration document.

	ID3
PARITY	
X32 NO–PAR.	0
X36 PARITY	1
PARITY STRUCTURE	

	ID2
REFRESH MODE	
NORMAL	0
SELF–REFRESH	1
REFRESH MODE	

	ID1
REFRESH	
NORMAL	0
SLOW	1
REFRESH PERIOD	

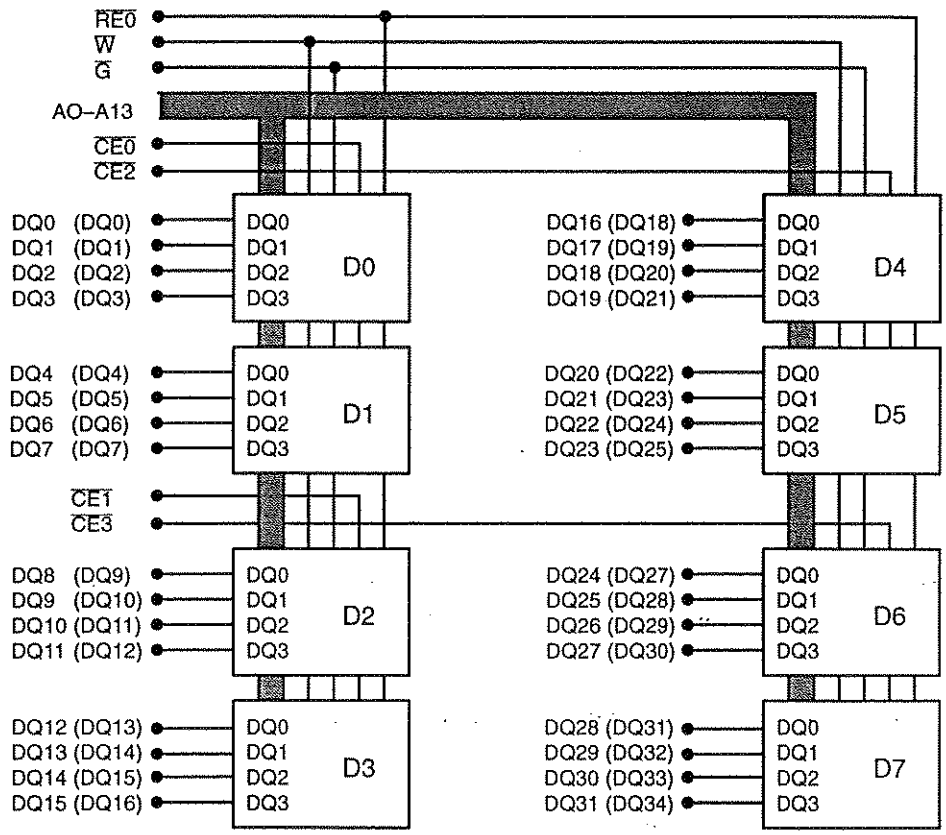
	PD24
ECC	
X32/X36 PARITY	1
X36 ECC	0
DATA STRUCTURE	

	PD23
MODE	
FAST PAGE	1
EDO/BURST EDO	0
DATA I/O MODE	

	PD22	PD21
SPEED (tRAC)	81	80
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

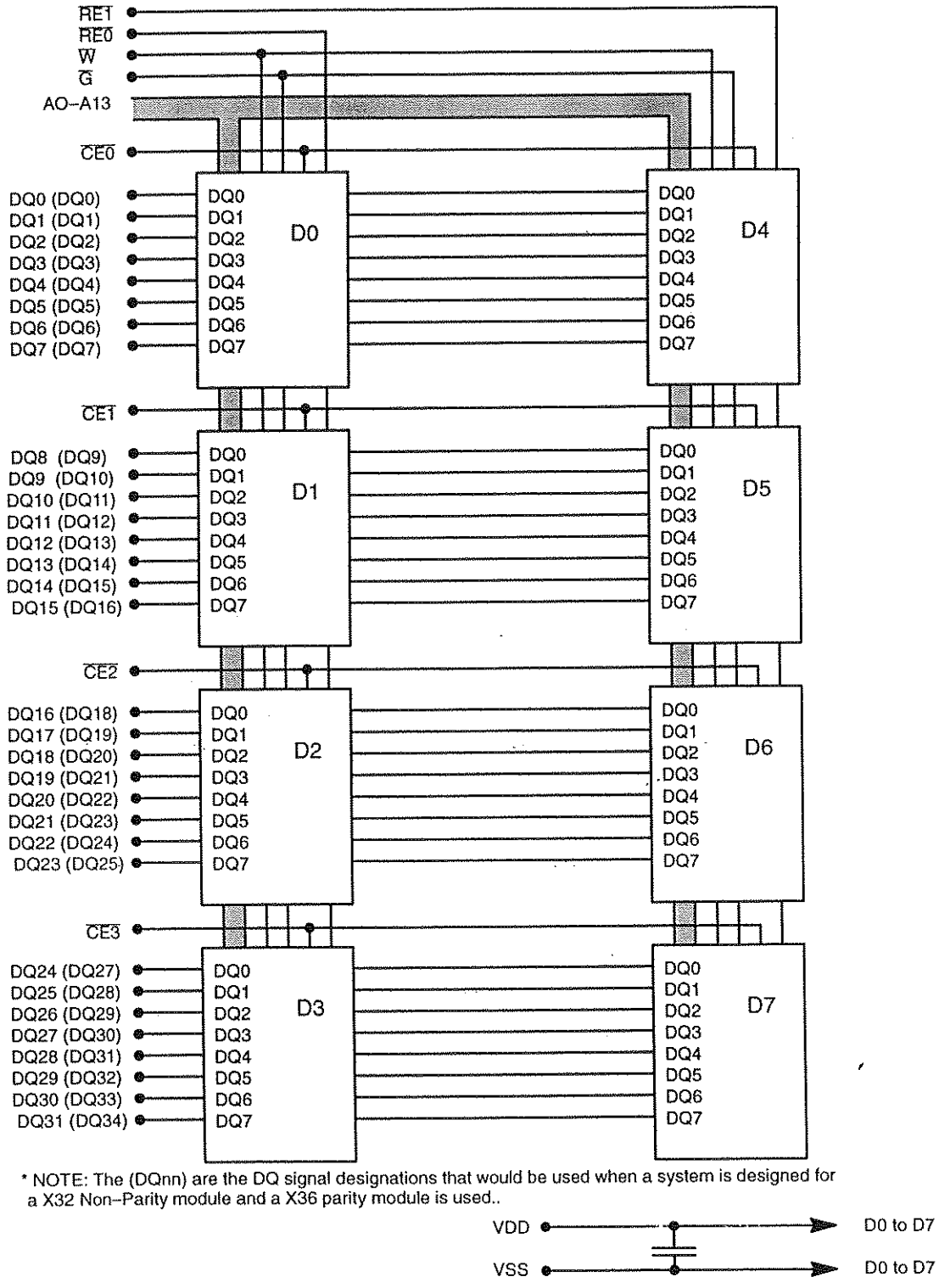
&

FIGURE 4.4.5–B
X32 and X36 DRAM SO–DIMM PD and ID TRUTH TABLES



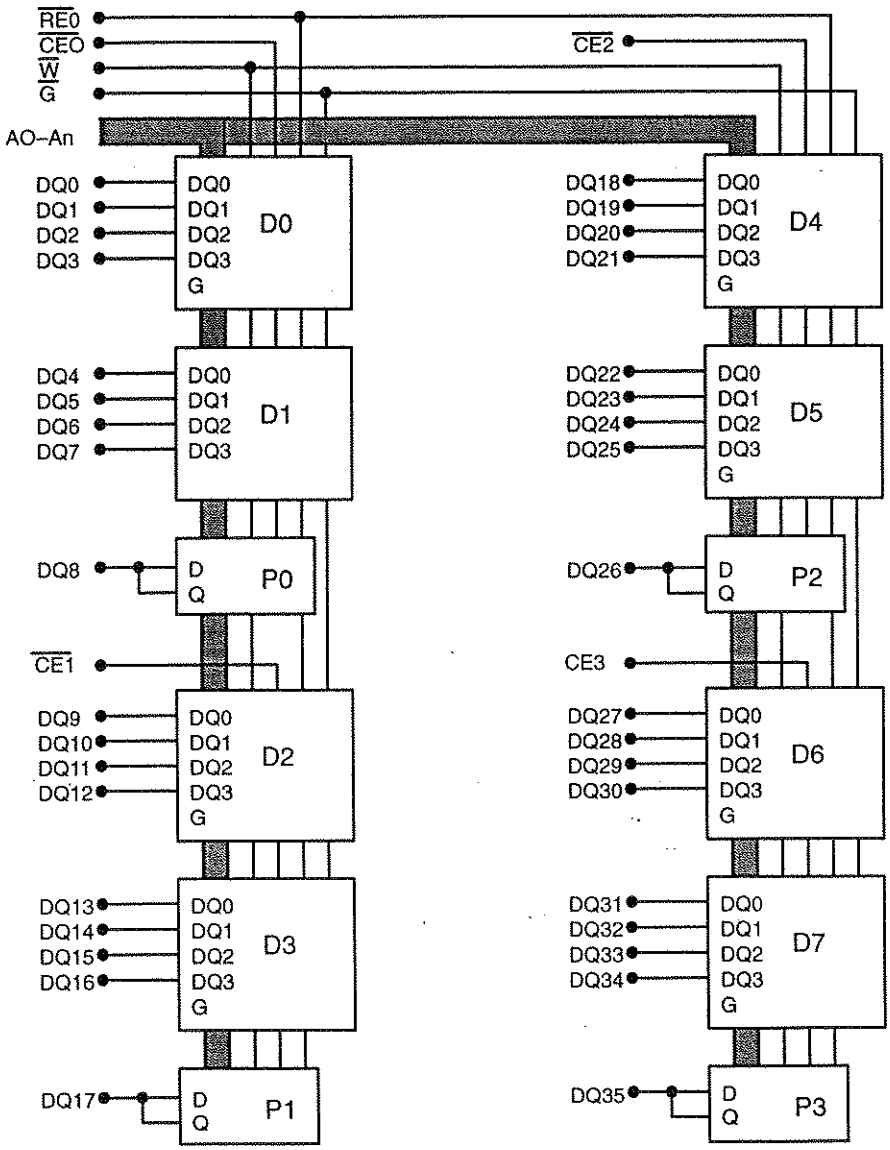
* NOTE: The (DQnn) are the DQ signal designations that would be used when a system is designed for a X32 Non–Parity module and a X36 parity module is used..

FIGURE 4.4.5–C
X 32 DRAM SO–DIMM USING X4 DEVICES



* NOTE: The (DQnn) are the DQ signal designations that would be used when a system is designed for a X32 Non–Parity module and a X36 parity module is used..

FIGURE 4.4.5–D
X 32 DRAM SO–DIMM USING X8 DEVICES



* NOTE: For the parity bit devices, P0 ⇒ P3, X1 DRAMs are showed, but Multi $\overline{CE}$ DRAM may be used.

FIGURE 4.4.5–E
X 36 DRAM PARITY SO–DIMM USING X4/X1 DEVICES

Release 6–7

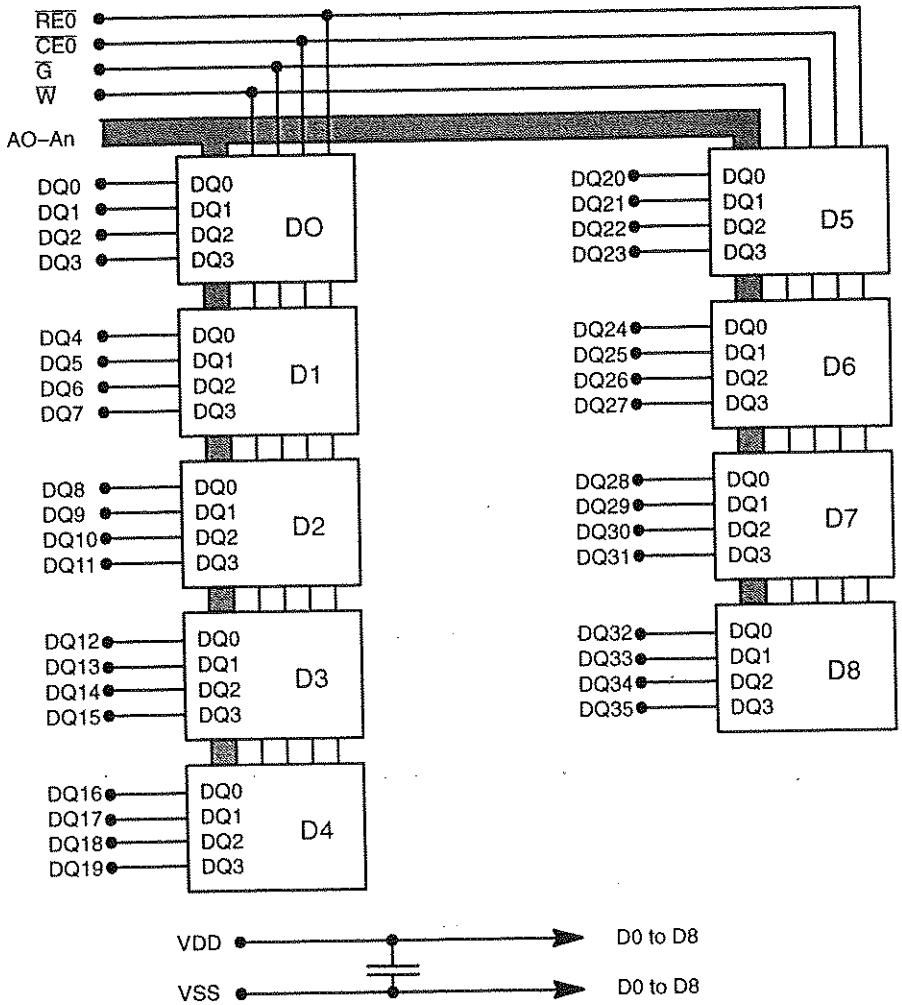
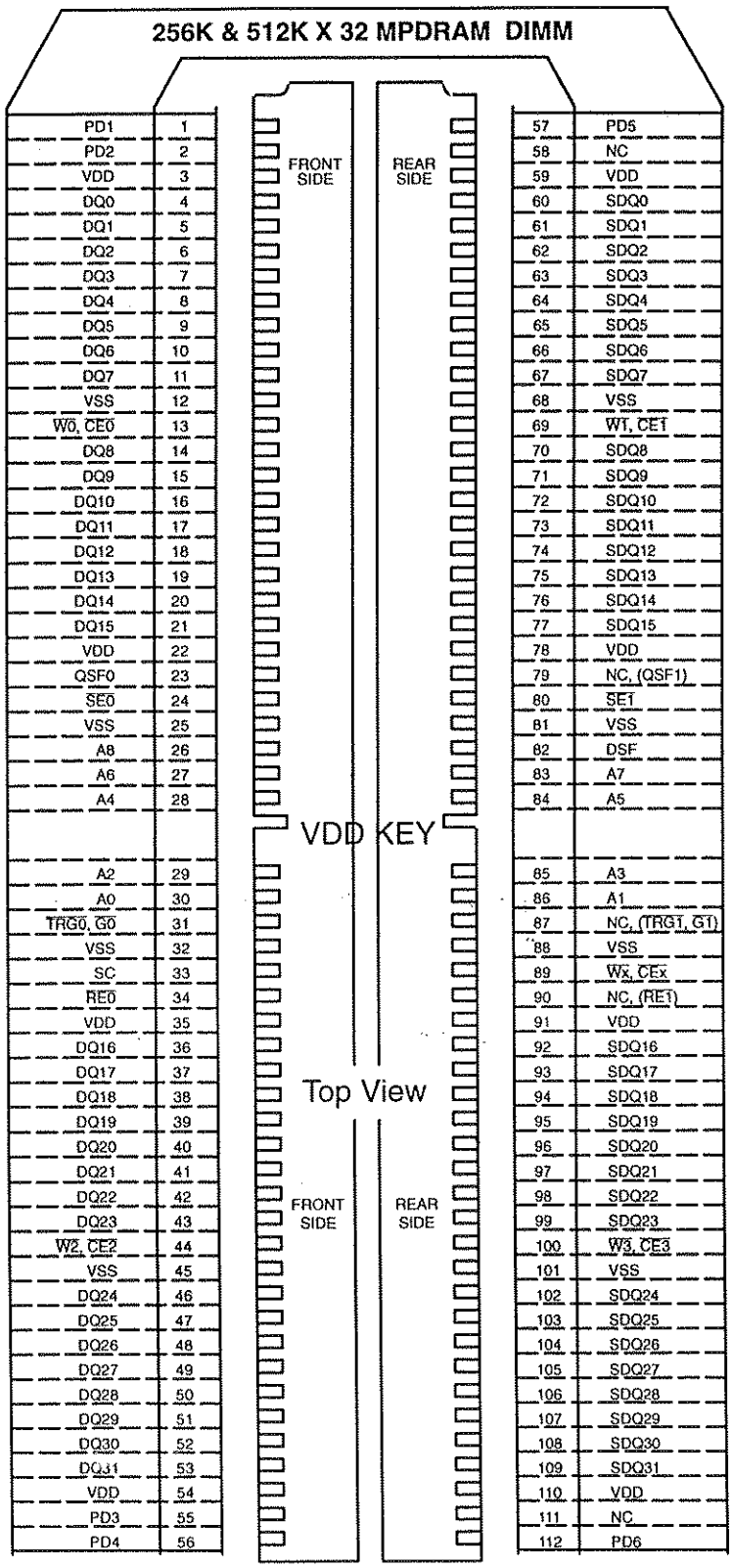


FIGURE 4.4.5–F
X 36 DRAM ECC SO–DIMM USING X4 DEVICES

4.4.6 – 112 PIN MPDRAM DIMM FAMILY

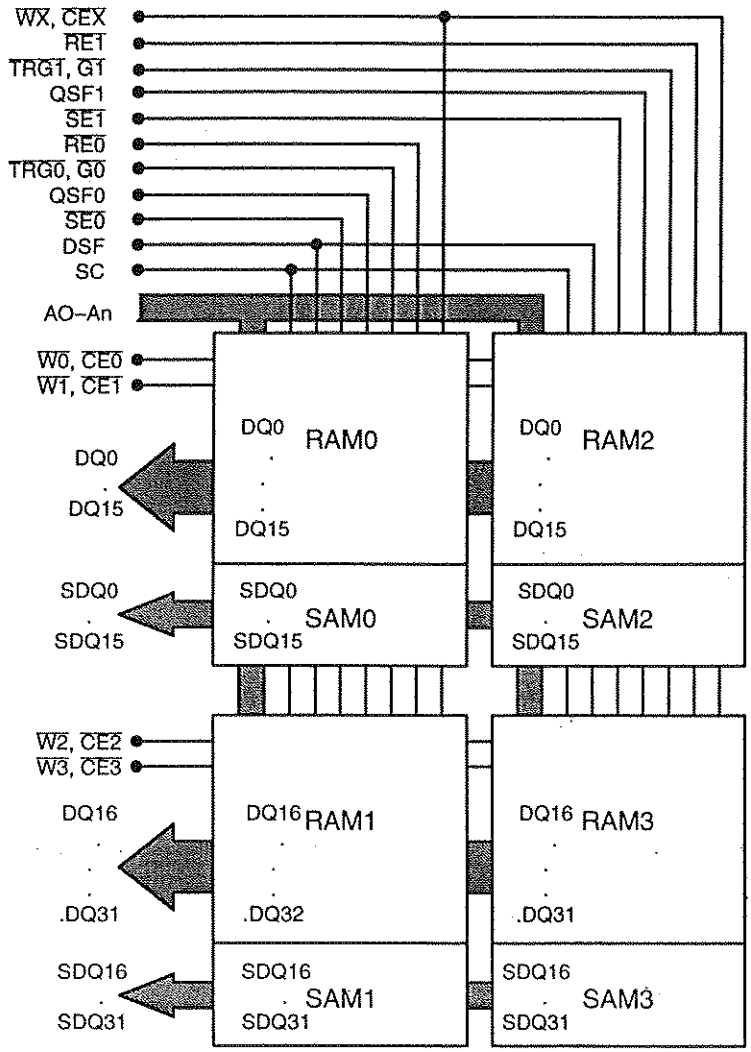
CAPACITY—256K, and 512K WORDS OF 32 BITS ON THE SERIAL AND PARALLEL PORTS.
DATA CONFIGURATIONS—Two DEVICE configurations are defined: using X8 and X16 MPDRAM
CONFIGURATION—2 Different Configurations are defined using X4 & X8 memories with 2 banks.
LOGIC FEATURES—The modules contain independent clock control of the 4 separate BYTE groups of data bits and "PRESENCE DETECT" features that consists of output pins in the PDn field which supplies encoded values that define the storage capacity, SAM length, read mode, refresh mode, $\overline{CE}$/W logic configuration, and speed of the module.
PACKAGE—112 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.6–A
PRESENCE DETECT TABLES—Fig. 4.4.6–B
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.6–B & 4.4.6–C

XILINX EXHIBIT 1010
Page 273



NOTE: Pin functions in ( ) may be re;quired on certain 2–bank 512K X 32 module implementations

FIGURE 4.4.6–A
256K & 512K MPDRAM DIMM



BLOCK DIAGRAM for 256K/512K X 32 DIMM WITH 256K BY 16 MPDRAM

CAPACITY	
	PD1
	Pin 1
1MB	S
2MB	O

SAM LENGTH	
	PD2
	Pin 2
256	S
512	O

OPERATIONAL MODE	
	PD3
	Pin 55
Fast Page	S
EDO	O

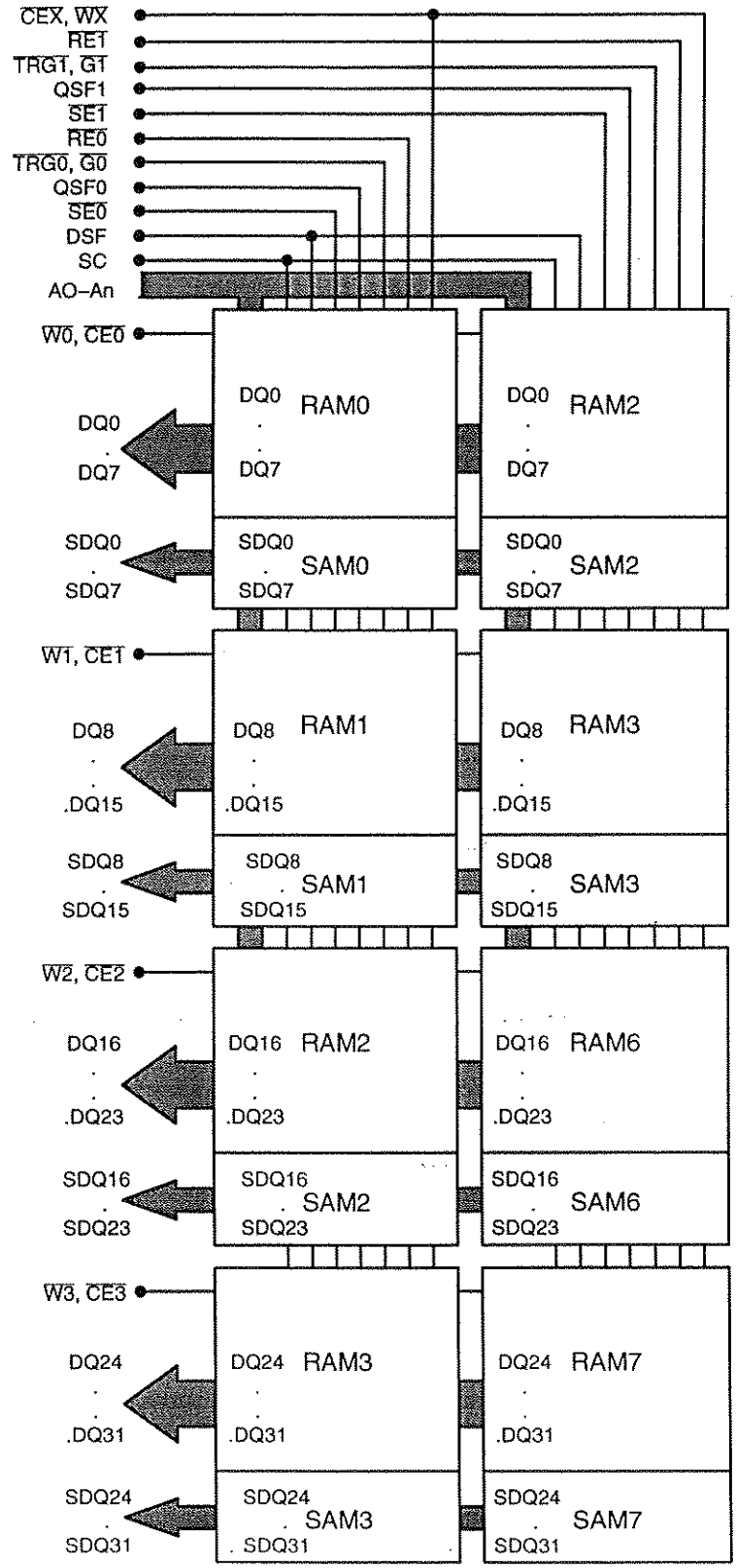
BYTE CONTROL	
	PD6
	Pin 112
4 $\overline{CE}$	S
4 $\overline{W}$	O

PD SPEED TABLE		
	PD4	PD5
SPEED (tRELQV)	Pin 56	Pin 57
80 ns	O	O
70 ns	S	O
60 ns	O	S
50 ns	S	S

S = CONNECTED TO VSS
O = NO CONNECTION

PD TRUTH TABLES for 256K/512K X 32 DIMM WITH 256K BY 8 or 16 MPDRAM

FIGURE 4.4.6–B
256K/512K BY 32 MPDRAM DIMM WITH 256K BY 16 MPDRAM



BLOCK DIAGRAM for 256K/512K X 32 DIMM WITH 256K BY 8 MPDRAM

FIGURE 4.4.6–C

256K/512K BY 32 MPDRAM DIMM WITH 256K BY 8 MPDRAM

4.4.7 – 80 PIN EEPROM SIMM FAMILY

CAPACITY—128K, 256K, 512K, 1M, 2M, 4M, & 8M WORDS OF 32 BITS
CONFIGURATION—Fifteen Different Configurations Using 1mb, 4mb, & 16mb Devices.
LOGIC FEATURES—The modules contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the module.
PACKAGE—88 PIN JEDEC MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Fig. 4.4.7–A
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.7–B

XILINX EXHIBIT 1010
Page 278

PIN #	PIN NAME	PIN #	PIN NAME
1	VSS	41	A11
2	VDD	42	A10
3	VPP/NC	43	A9
4	$\overline{G}$	44	A8
5	$\overline{W0}$	45	A7
6	$\overline{W1}$	46	A6
7	RFU	47	A5
8	DQ16	48	A4
9	DQ17	49	A3
10	DQ18	50	A2
11	DQ19	51	A1
12	DQ20	52	A0
13	DQ21	53	$\overline{W3}$
14	DQ22	54	VSS
15	DQ23	55	DQ15
16	DQ24	56	DQ14
17	DQ25	57	DQ13
18	DQ26	58	DQ12
19	DQ27	59	DQ11
20	DQ28	60	DQ10
21	$\overline{E3}$	61	DQ9
22	$\overline{E2}$	62	DQ8
23	$\overline{E1}$	63	DQ7
24	$\overline{E0}$	64	DQ6
25	VSS	65	DQ5
26	DQ29	66	DQ4
27	DQ30	67	DQ3
28	DQ31	68	DQ2
29	$\overline{W2}$	69	DQ1
30	A22	70	DQ0
31	A21	71	VPP/NC
32	A20	72	VDD
33	A19	73	PD1
34	A18	74	PD2
35	A17	75	PD3
36	A16	76	PD4
37	A15	77	PD5
38	A14	78	PD6
39	A13	79	PD7
40	A12	80	VSS

PRESENCE DETECT TRUTH TABLE

Module Organization	Device Density	# of Dev.	Module Capacity	PD1	PD2	PD3	PD4
No Module				1	1	1	1
.128K X 32	1M	4	512KB	0	1	1	1
256K X 32	1M	8	1MB	1	0	1	1
512K X 32	1M	16	2MB	0	0	1	1
256K X 32	2M	4	1MB	1	1	0	1
512K X 32	2M	8	2MB	0	1	0	1
1M X 32	2M	16	4MB	1	0	0	1
512K X 32	4M	4	2MB	0	0	0	1
1M X 32	4M	8	4MB	1	1	1	0
2M X 32	4M	16	8MB	0	1	1	0
1M X 32	8M	4	4MB	1	0	1	0
2M X 32	8M	8	8MB	0	0	1	0
4M X 32	8M	16	16MB	1	1	0	0
2M X 32	16M	4	8MB	0	1	0	0
4M X 32	16M	8	16MB	1	0	0	0
8M X 32	16M	16	32MB	0	0	0	0

1 = OPEN CIRCUIT (NO CONNECTION)
0 = CONNECTED TO VSS

MODULE SPEED IDENTIFICATION

MAX ACCESS TIME	PRESENCE DETECT PIN		
	PD5	PD6	PD7
NOT DEFINED	1	1	1
45 nS	0	1	1
55 nS	1	0	1
70 nS	0	0	1
90 nS	1	1	0
120 nS	0	1	0
150 nS	1	0	0
200 nS	0	0	0

NOTE – This family of pinouts is approved for use in SIMM package that is nominally 4.65" long and a height of 0.85" See JEDEC Publication 95, section MO–XXX.

FIGURE 4.4.7–A
128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES

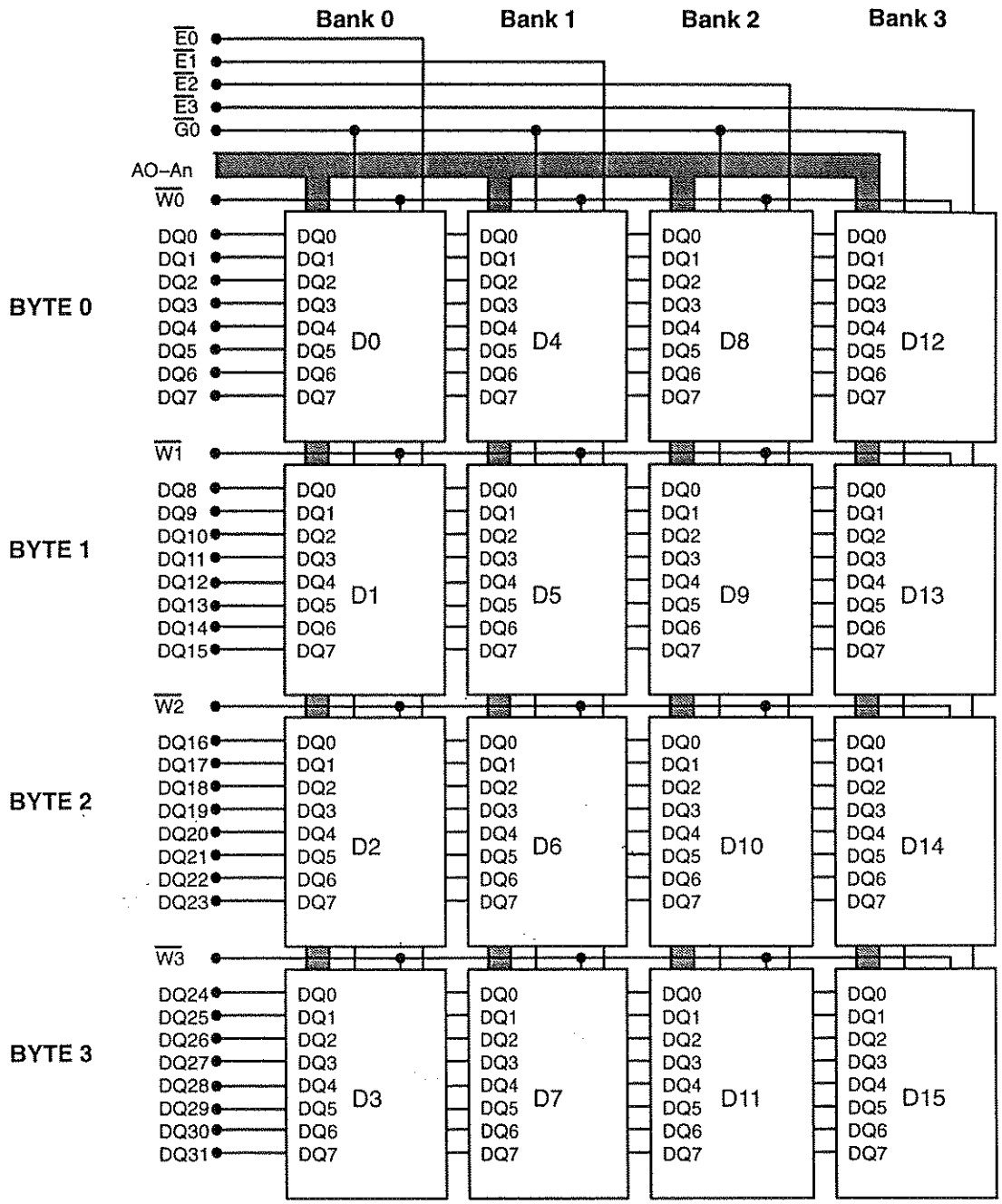


FIGURE 4.4.7–B
128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM

4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Seven DATA Word configurations are defined:

—32 BIT DRAM & SDRAM without PARITY
—36 BIT DRAM & SDRAM for ECC CODES
—40 BIT DRAM & SDRAM for ECC CODES
—32 BIT MULTIPLEXED ROM without PARITY.

CONFIGURATION—26 Different Configurations are defined using various combinationa of X1, X4, X8, and X16 DRAM & SDRAM memories including 2 bank configurations, 5 for DRAM and 21 for SDRAM.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—100 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.4.8–A & 4.4.8–B

TECHNOLOGY COMPARISON TABLE — Fig. 4.4.8–C

SDRAM CLOCK WIRING DIAGRAMS — Fig. 4.4.8–D

SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–E through 4.4.8–Z

DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–AA through 4.4.8–AE

XILINX EXHIBIT 1010
Page 281

XILINX EXHIBIT 1010
Page 282

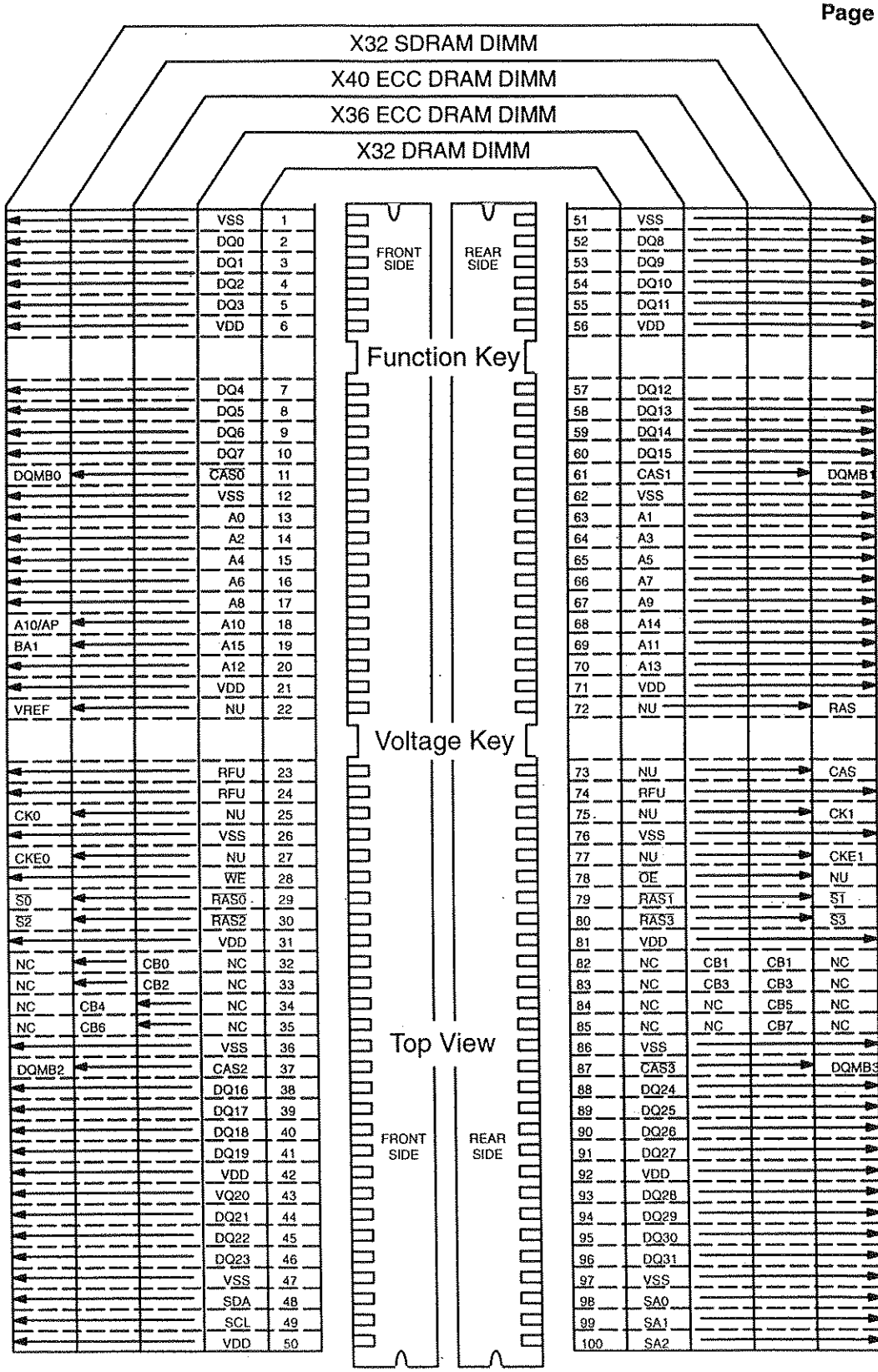


FIGURE 4.4.8– B

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

Release 7

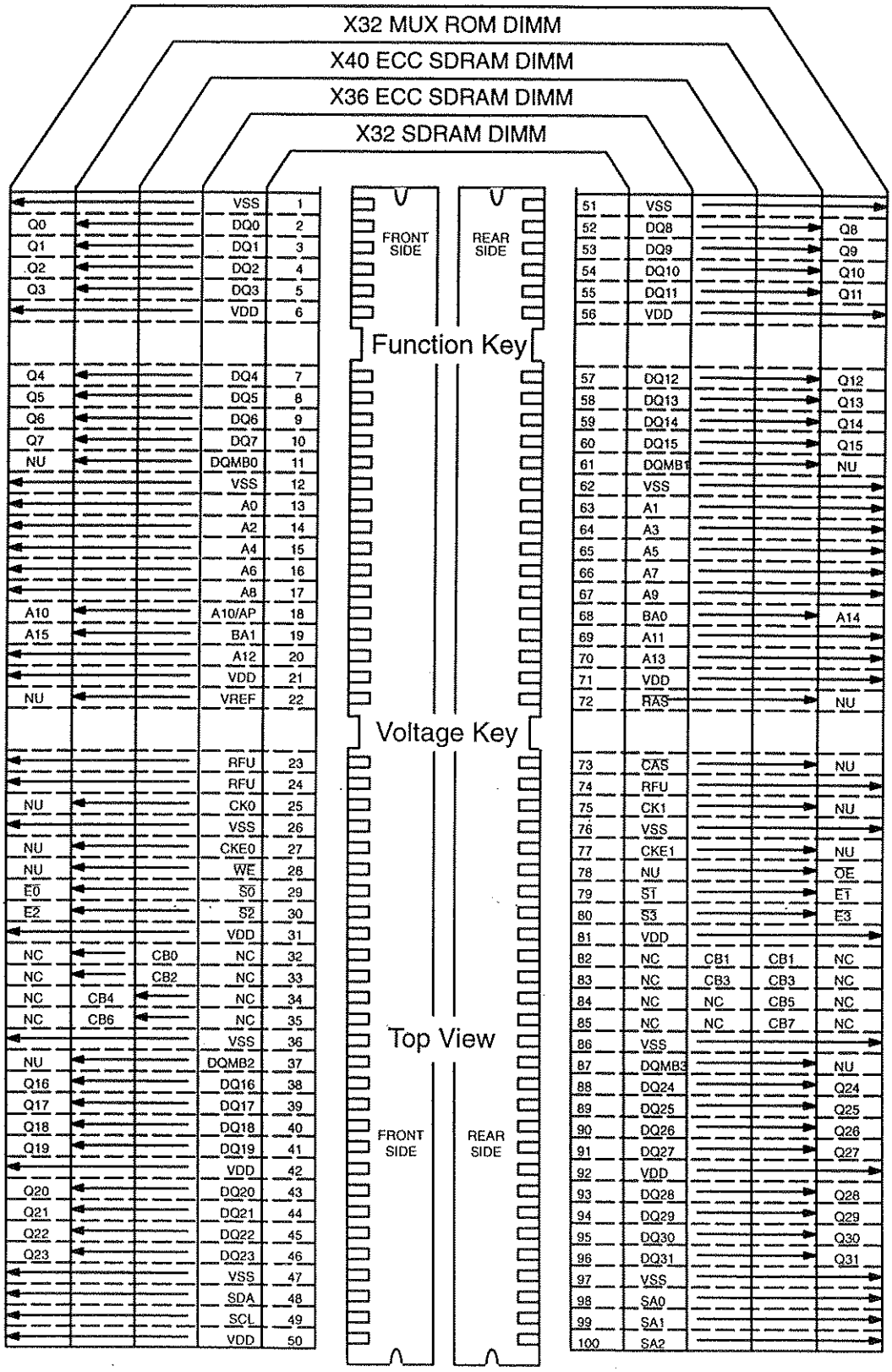


FIGURE 4.4.8– C

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

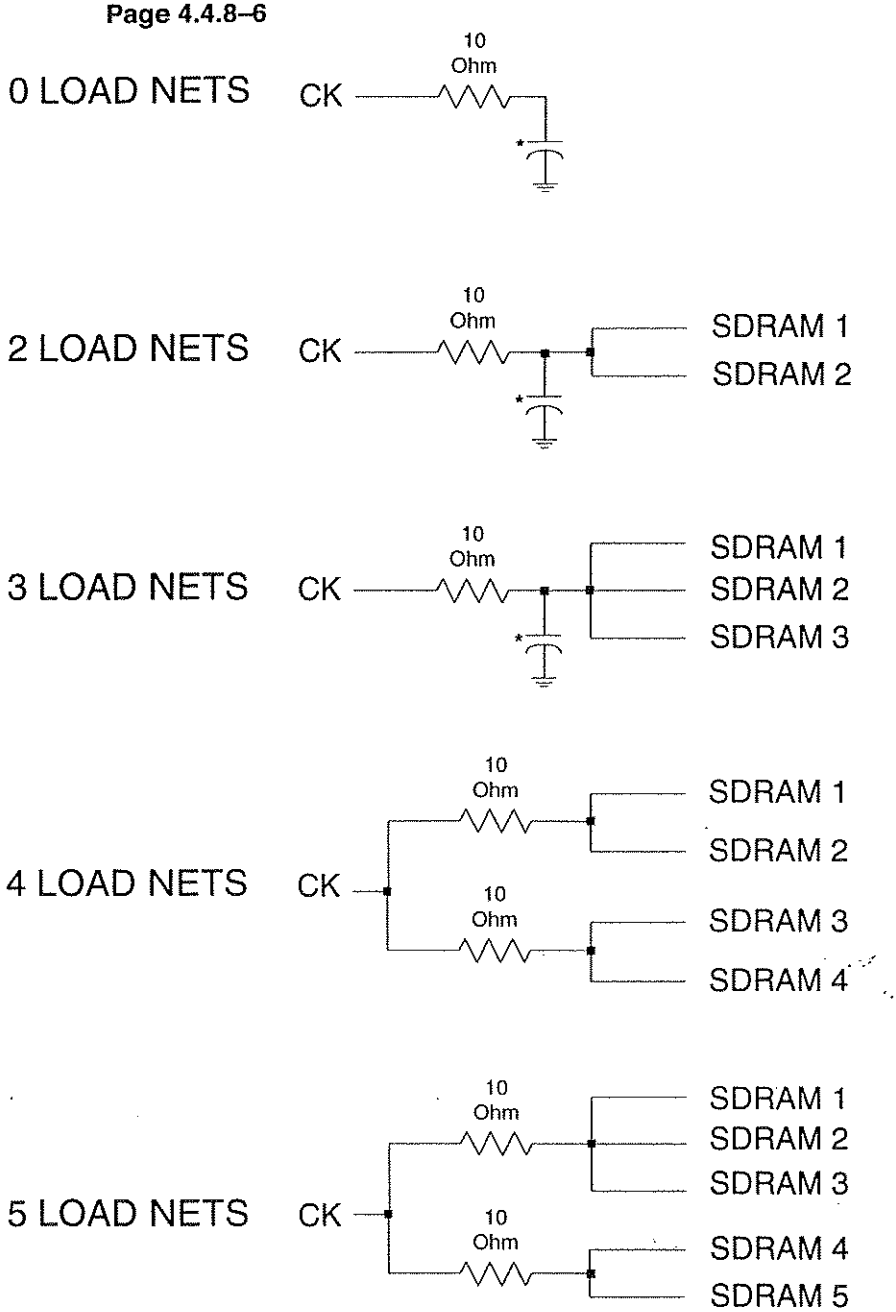
100 PIN DRAM/SDRAM DIMM PINOUT COMPARISON

PIN	DRAM DIMM	SDRAM DIMM	MUX ROM
11	$\overline{CAS0}$	DQMB0	NU
18	A10	A10/AP	A10
19	A12	BA1	A12
20	NU	A12	A14
22	NU	Vref	NU
25	NU	CK0	NU
27	NU	CKE0	NU
28	$\overline{WE}$	$\overline{WE}$	NU
29	$\overline{RAS0}$	$\overline{S0}$	$\overline{E0}$
30	$\overline{RAS2}$	$\overline{S2}$	$\overline{E2}$
37	$\overline{CAS2}$	DQMB2	NU
61	$\overline{CAS1}$	DQMB1	NU
68	A11	BA0	A11
69	A13	A11	A13
70	NU	A13	A15
72	NU	$\overline{RAS}$	NU
73	NU	$\overline{CAS}$	NU
75	NU	CK1	NU
77	NU	CKE1	NU
78	$\overline{OE}$	NU	$\overline{OE}$
79	$\overline{RAS1}$	$\overline{S1}$	$\overline{E1}$
80	$\overline{RAS3}$	$\overline{S3}$	$\overline{E3}$
87	$\overline{CAS3}$	DQMB3	NU

Notes:

1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A14 on DRAM DIMM is also BA0 on SDRAM DIMM
3. A15 on DRAM DIMM is also BA1 on SDRAM DIMM (for 4 Bank SDRAM).

Figure 4.4.8–D
100 Pin DRAM, SDRAM, & ROM DIMM, PIN COMPARISON

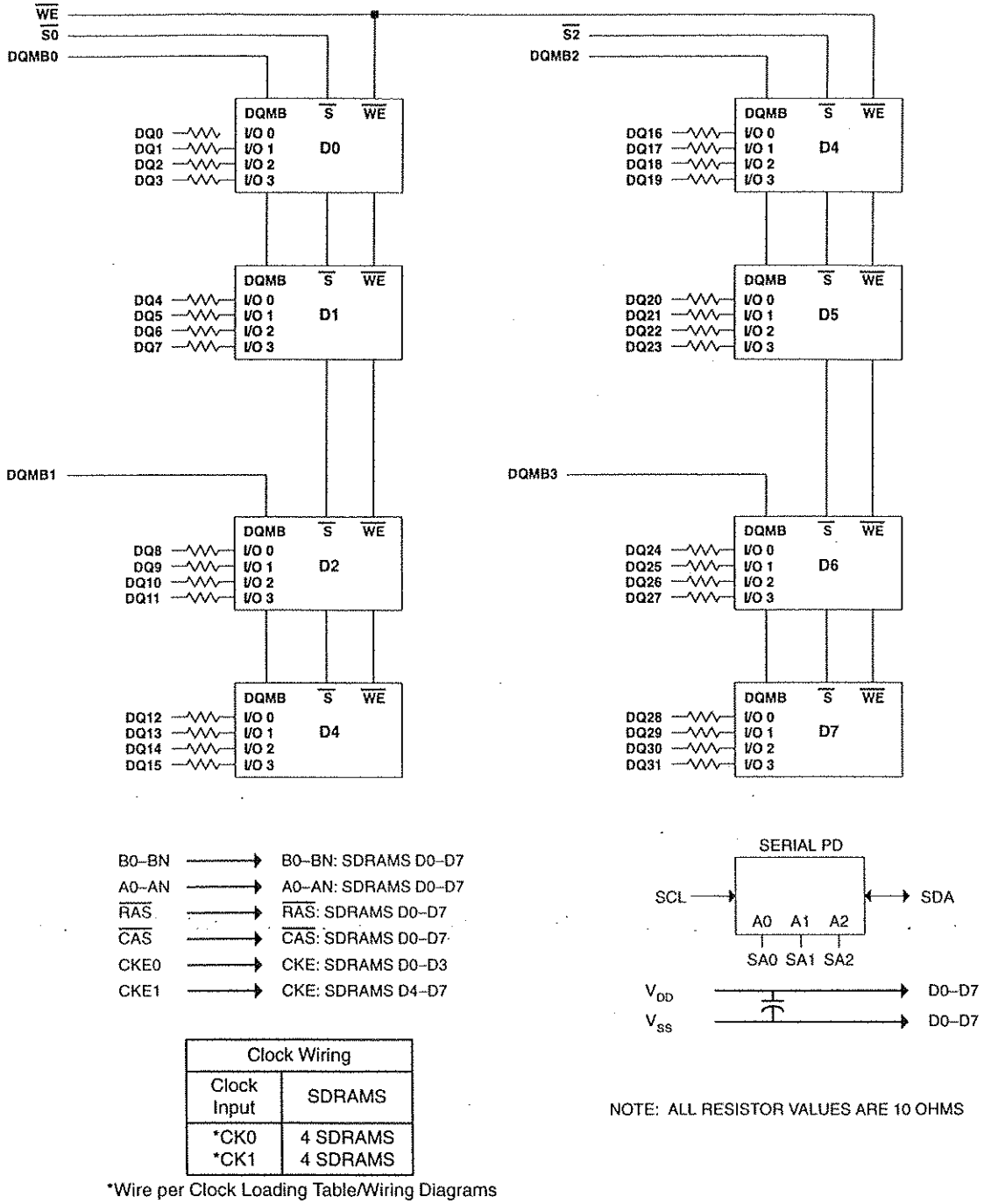


Notes:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .4ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PADDING CAPACITOR). (EG: THIS IS APPROXIMATELY 2" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2.) THE VARIATION OF CK INPUT DELAY WILL BE +/– .1NS FOR BOTH CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/– 3pf IN TOTAL CK INPUT CAPACITANCE).

Figure 4.4.8–E
100 Pin SDRAM DIMM, CLOCK WIRING



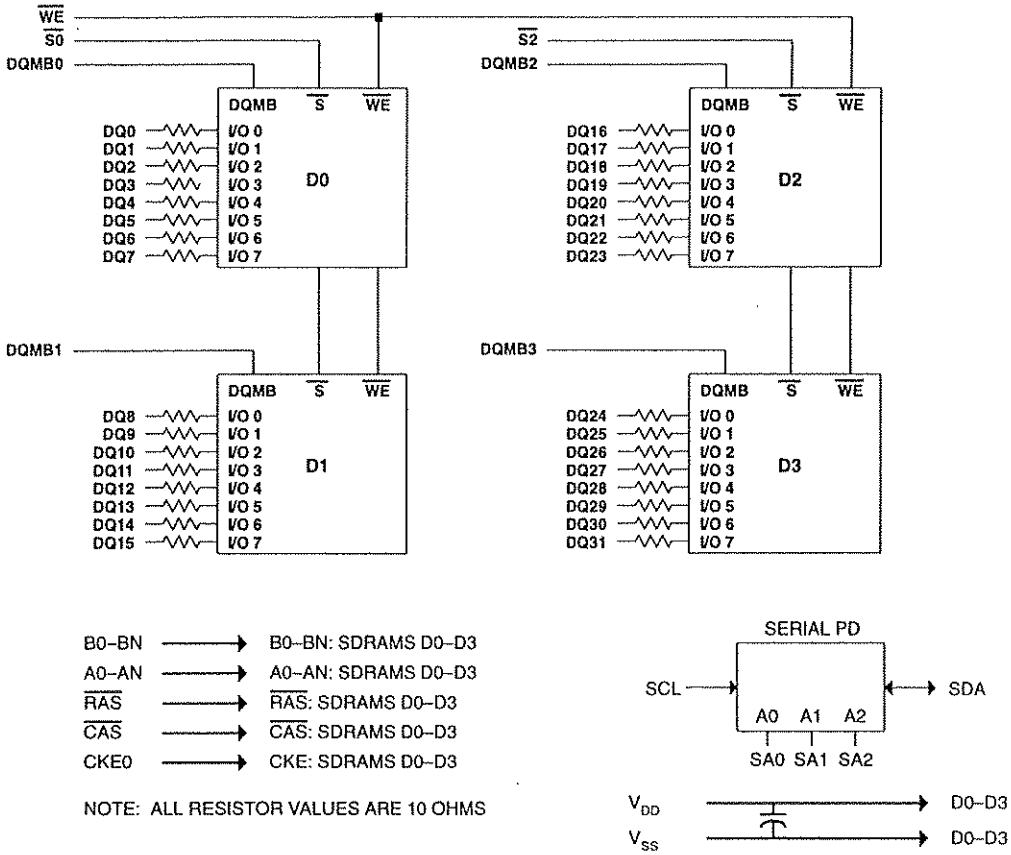
Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Figure 4.4.8–F
100 Pin X32 SDRAM DIMM, 1 Bank with X4 SDRAMs

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Page 287

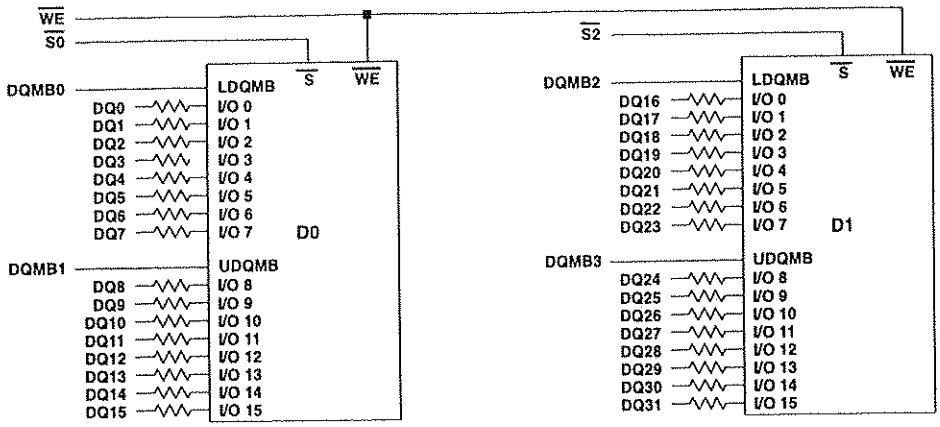


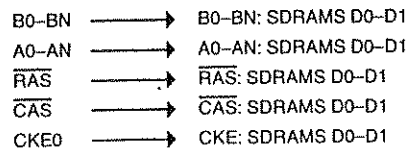
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	4 SDRAMS

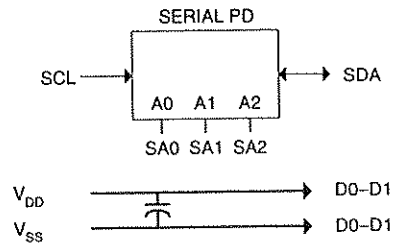
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–G
100 Pin X32 SDRAM DIMM, 1 Bank with X8 SDRAMs





NOTE: ALL RESISTOR VALUES ARE 10 OHMS

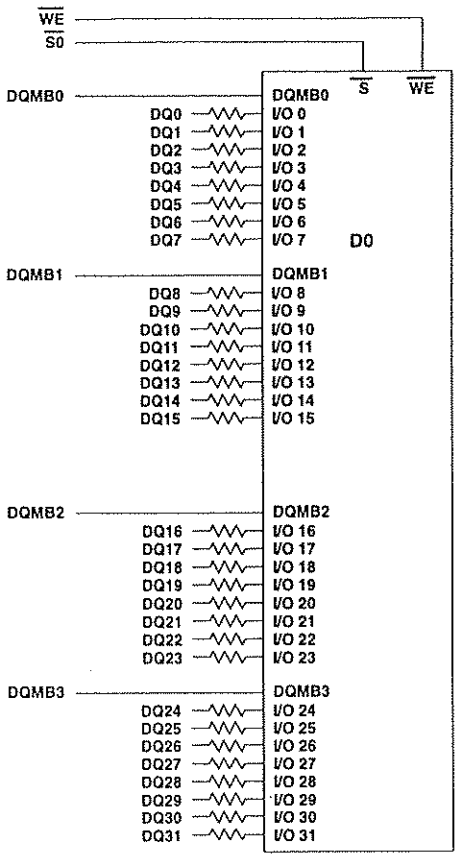


Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

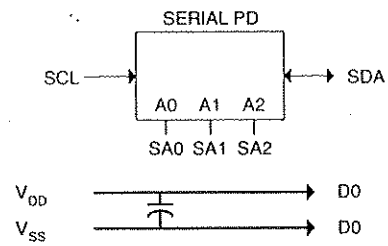
Figure 4.4.8–H
100 Pin X32 SDRAM DIMM, 1 Bank with X16 SDRAMs

XILINX EXHIBIT 1010
Page 289



B0–BN → B0–BN: SDRAMS D0
A0–AN → A0–AN: SDRAMS D0
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0
CKE0 → CKE: SDRAMS D0

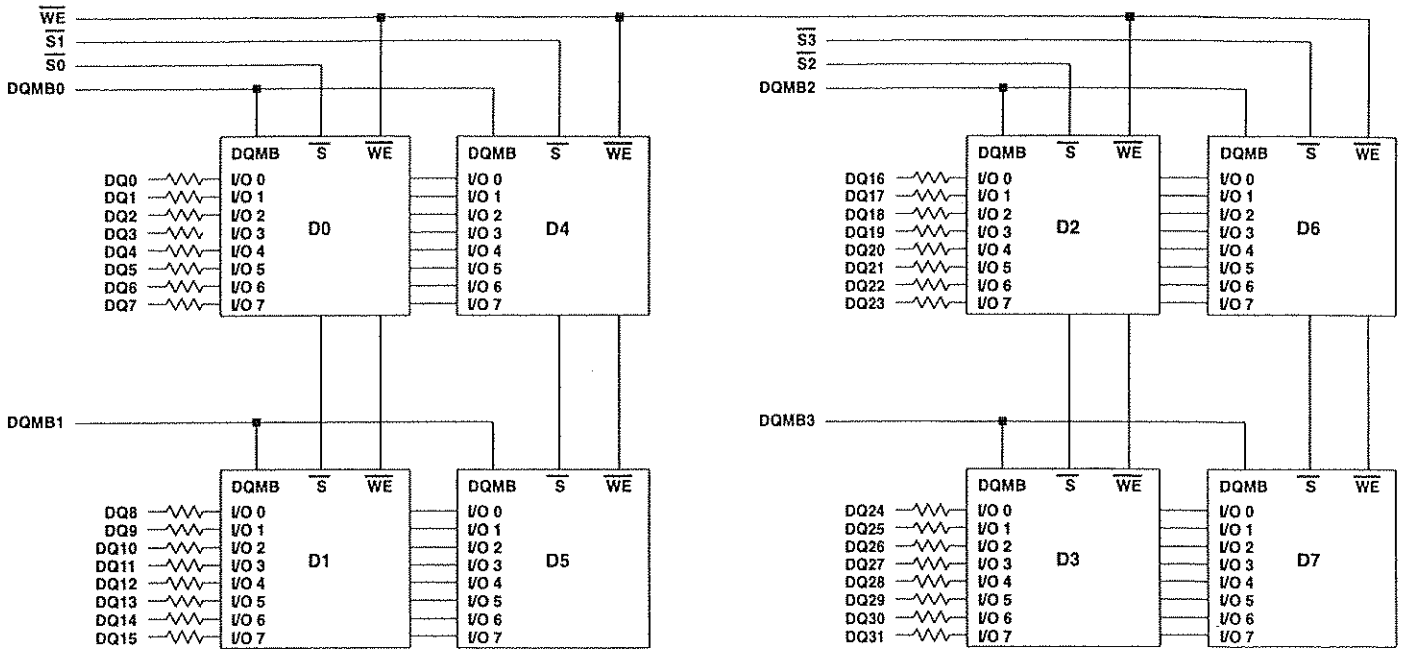
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	1 SDRAMS

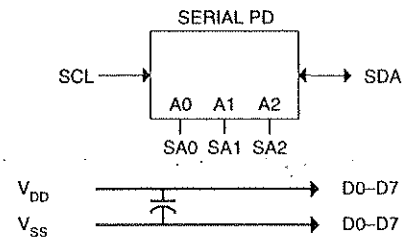
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–I
100 Pin X32 SDRAM DIMM, 1 Bank with X32 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D7
A0–AN → A0–AN: SDRAMS D0–D7
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D7
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D7
CKE0 → CKE: SDRAMS D0–D3
CKE1 → CKE: SDRAMS D4–D7

NOTE: ALL RESISTOR VALUES ARE 10 OHMS



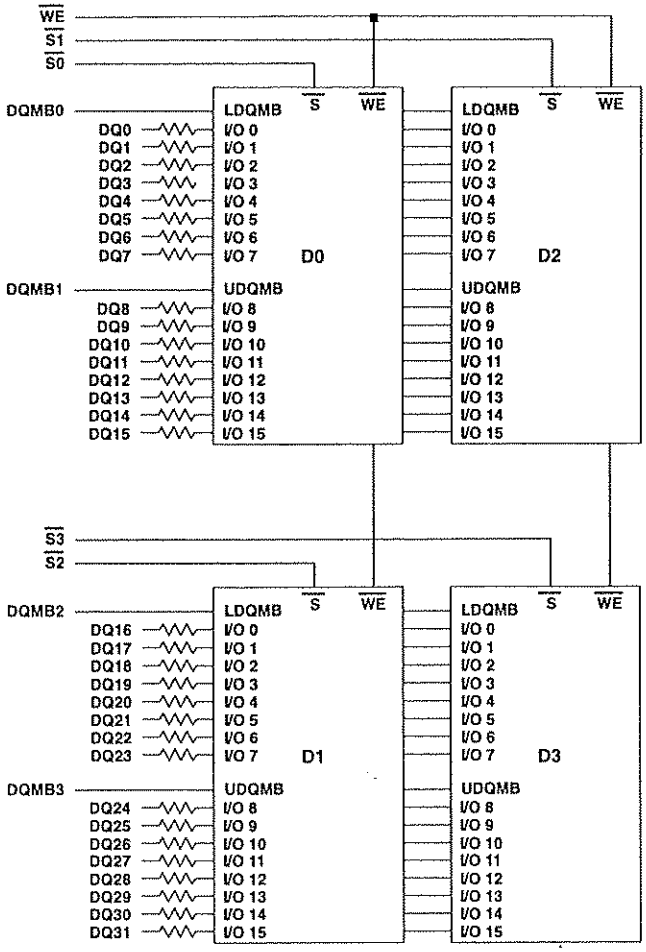
Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–J
100 Pin X32 SDRAM DIMM, 2 Bank with X8 SDRAMs

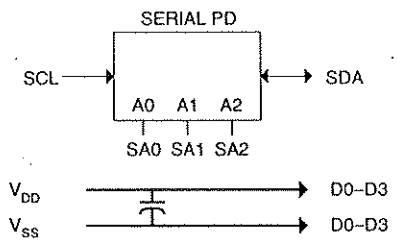
XILINX EXHIBIT 1010
Page 291

4.4.6–1



B0–BN → B0–BN: SDRAMS D0–D3
A0–AN → A0–AN: SDRAMS D0–D3
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D3
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D3
CKE0 → CKE: SDRAMS D0–D1
CKE1 → CKE: SDRAMS D2–D3

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

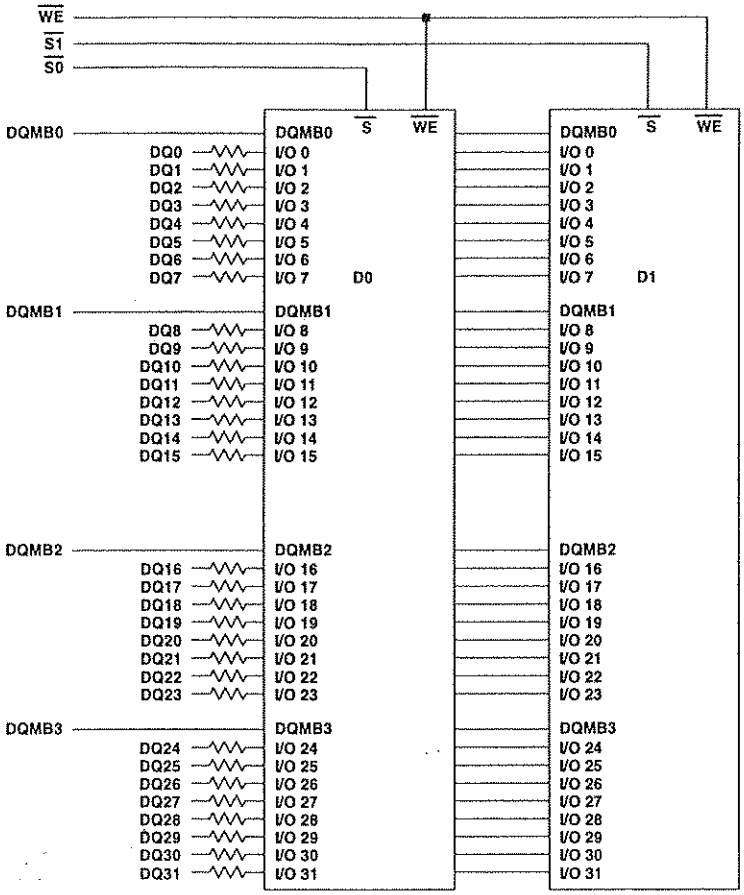


Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

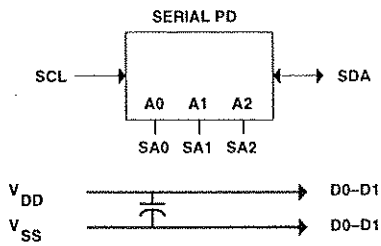
Figure 4.4.8–K
100 Pin X32 SDRAM DIMM, 2 Bank with X16 SDRAMs

XILINX EXHIBIT 1010
Page 292



B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0
CKE1 → CKE: SDRAMS D1

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

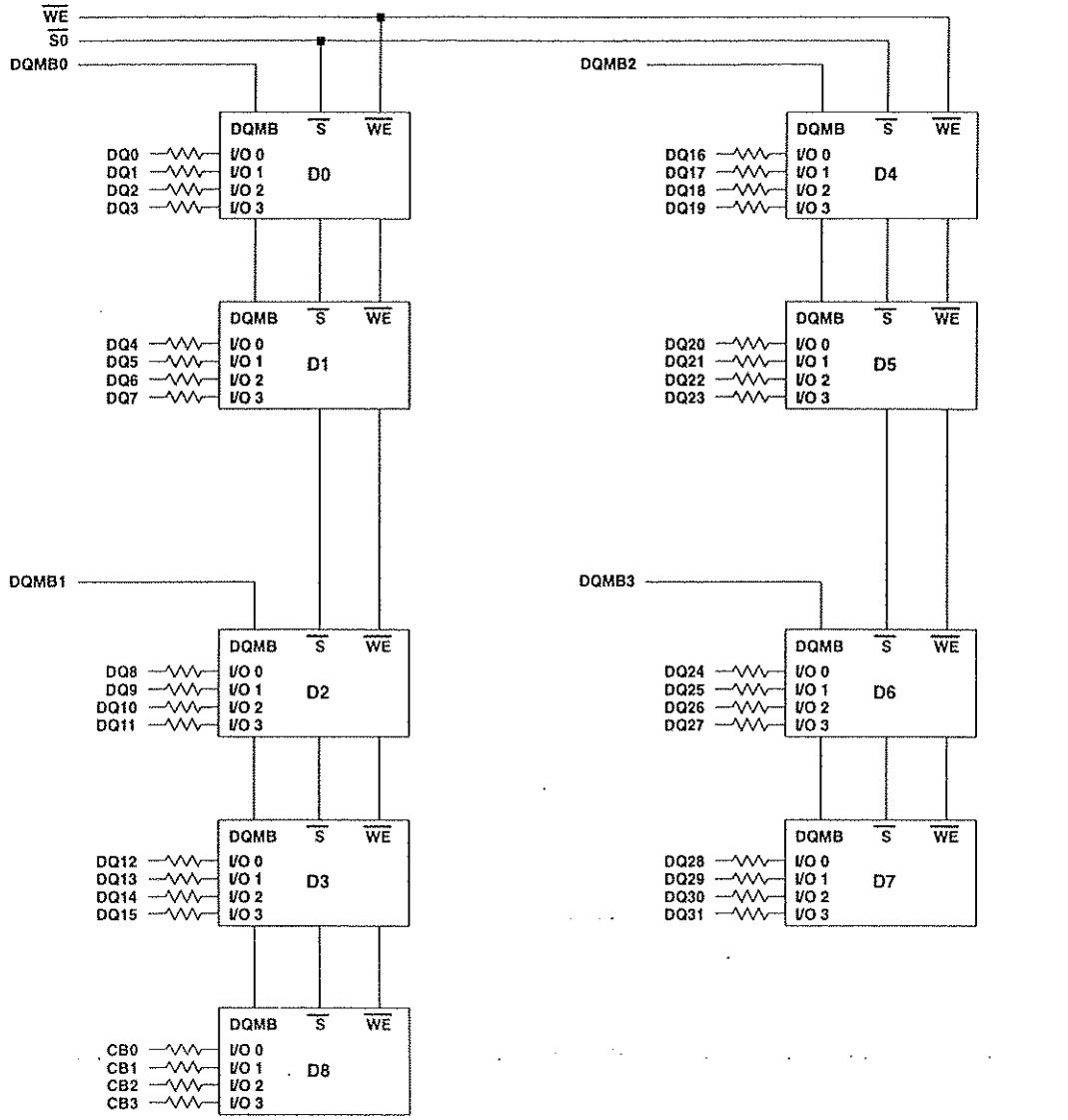


Clock Wiring	
Clock Input	SDRAMS
*CK0	1 SDRAM
*CK1	1 SDRAM

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–L
100 Pin X32 SDRAM DIMM, 2 Bank with X32 SDRAMs

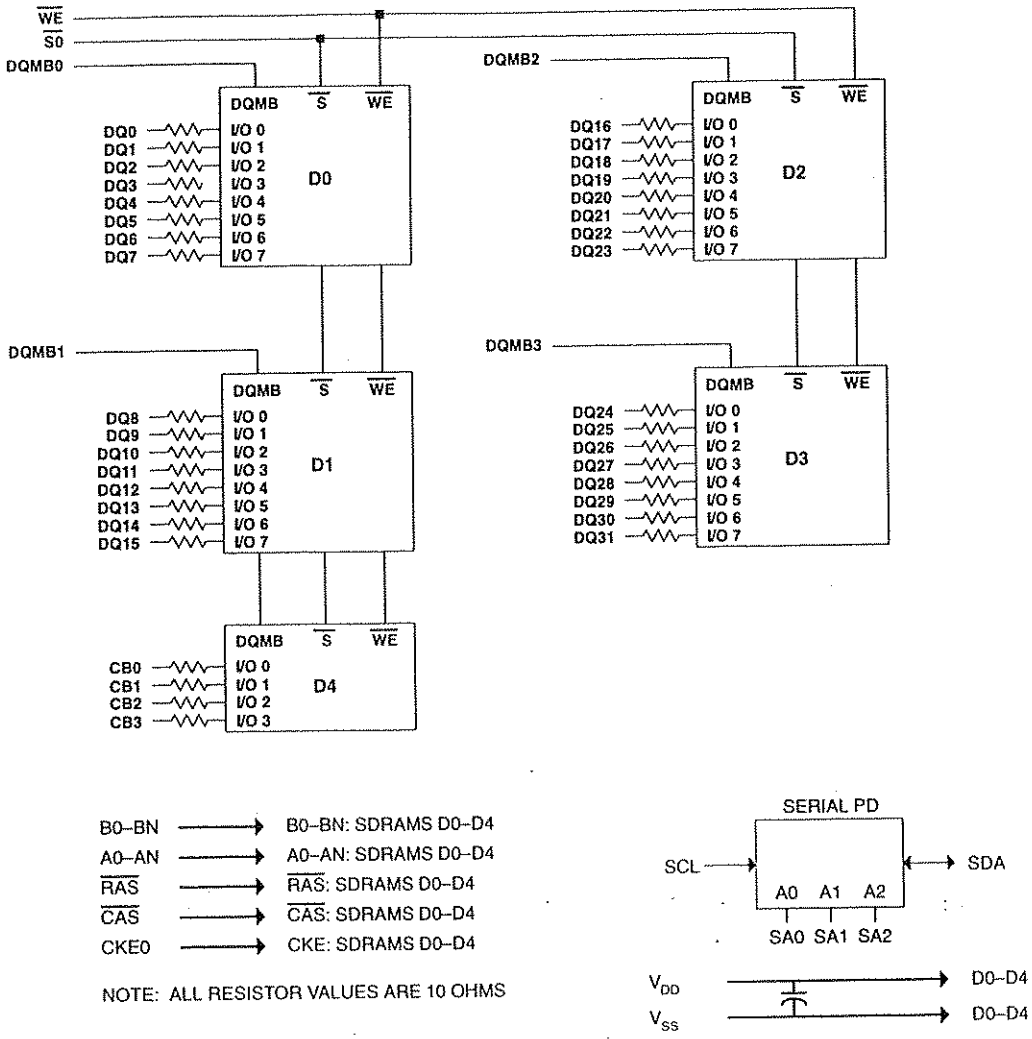
XILINX EXHIBIT 1010
Page 293



Clock Wiring	
Clock Input	SDRAMS
*CK0	4 or 5 SDRAMS
*CK1	4 or 5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–M
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs

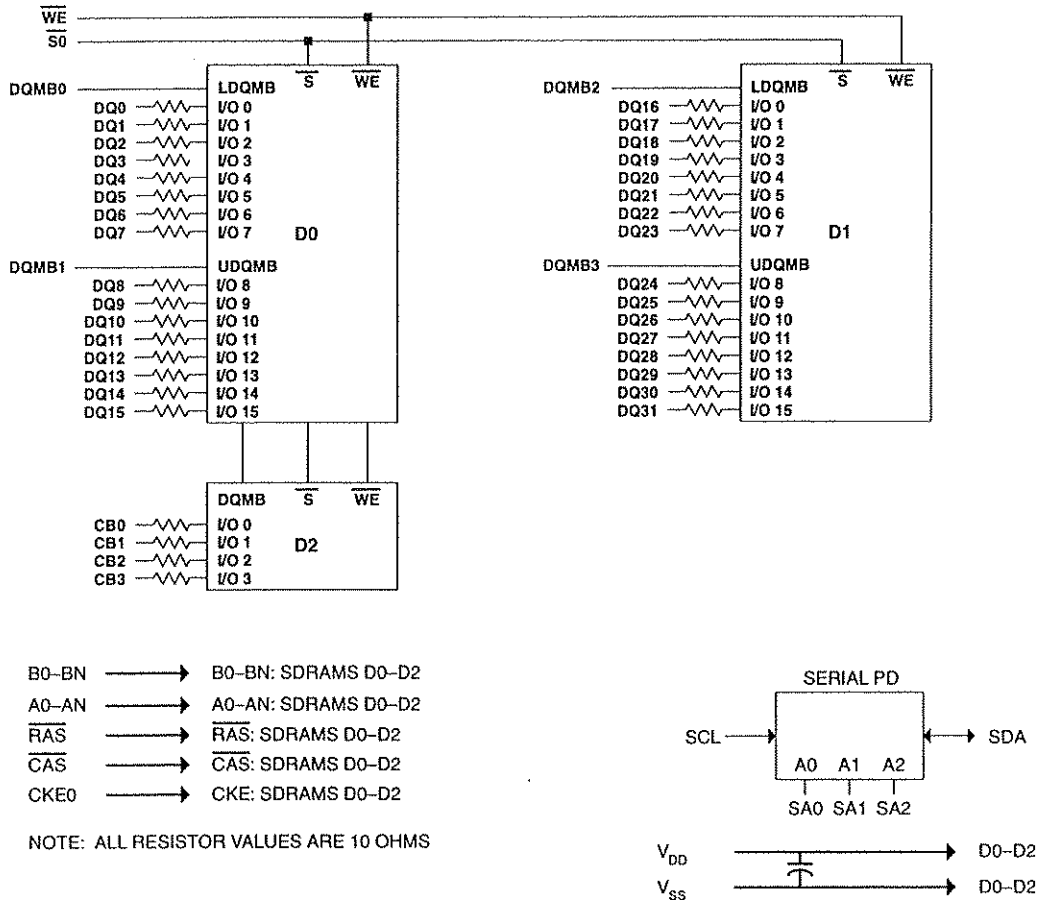


Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–N
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X8 SDRAMs

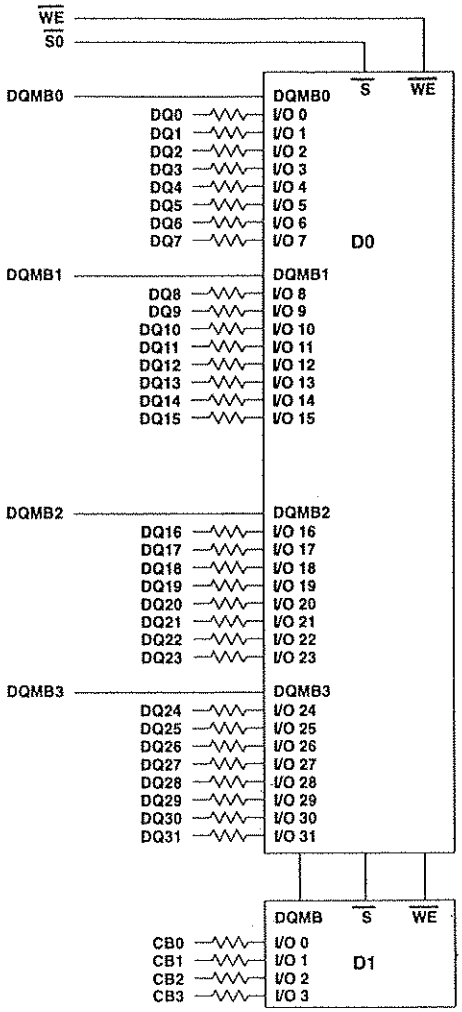
XILINX EXHIBIT 1010
Page 295



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

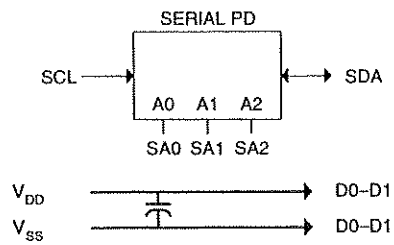
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–O
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0–D1

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

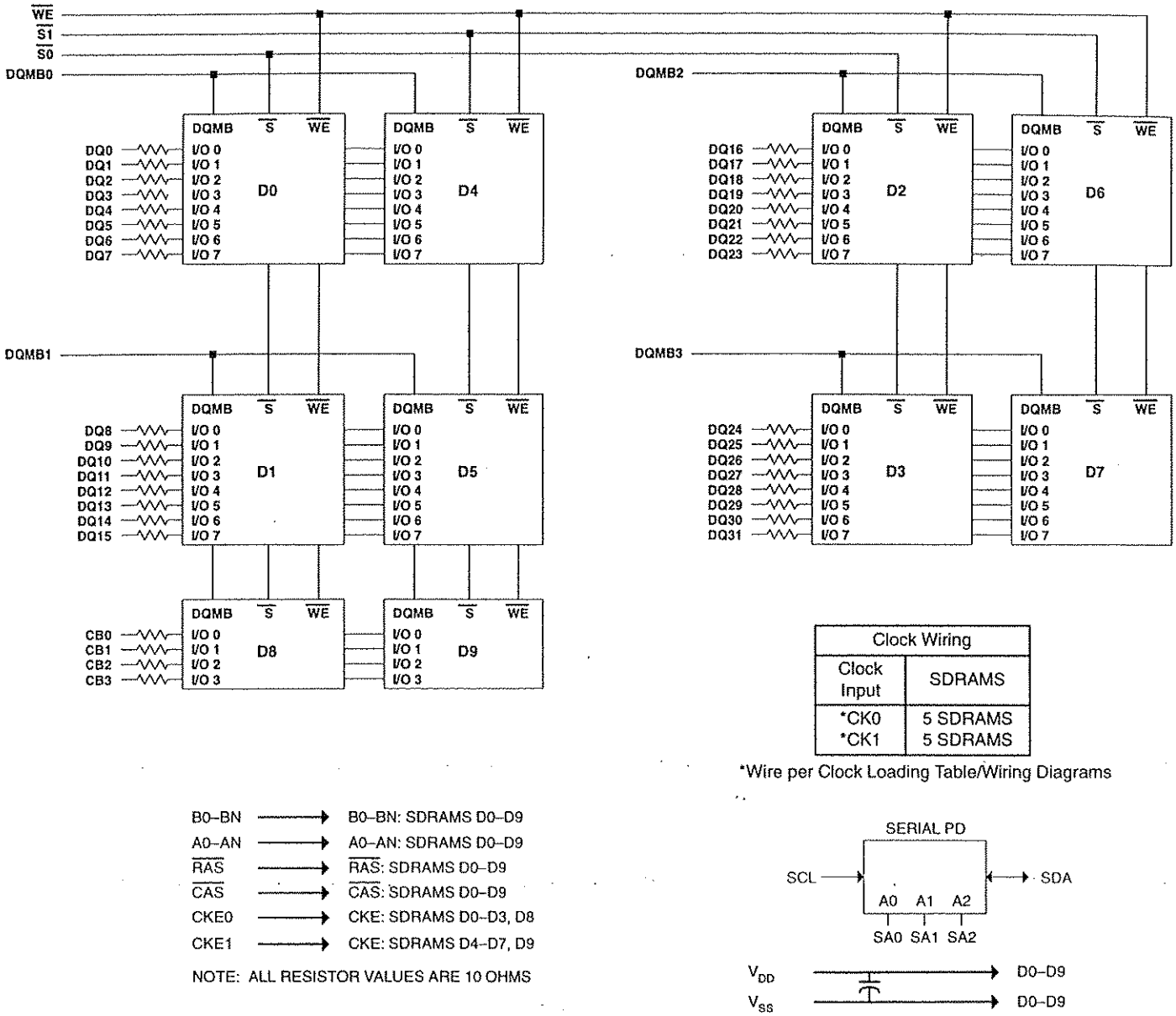


Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–P
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X32 SDRAMs

Release 7



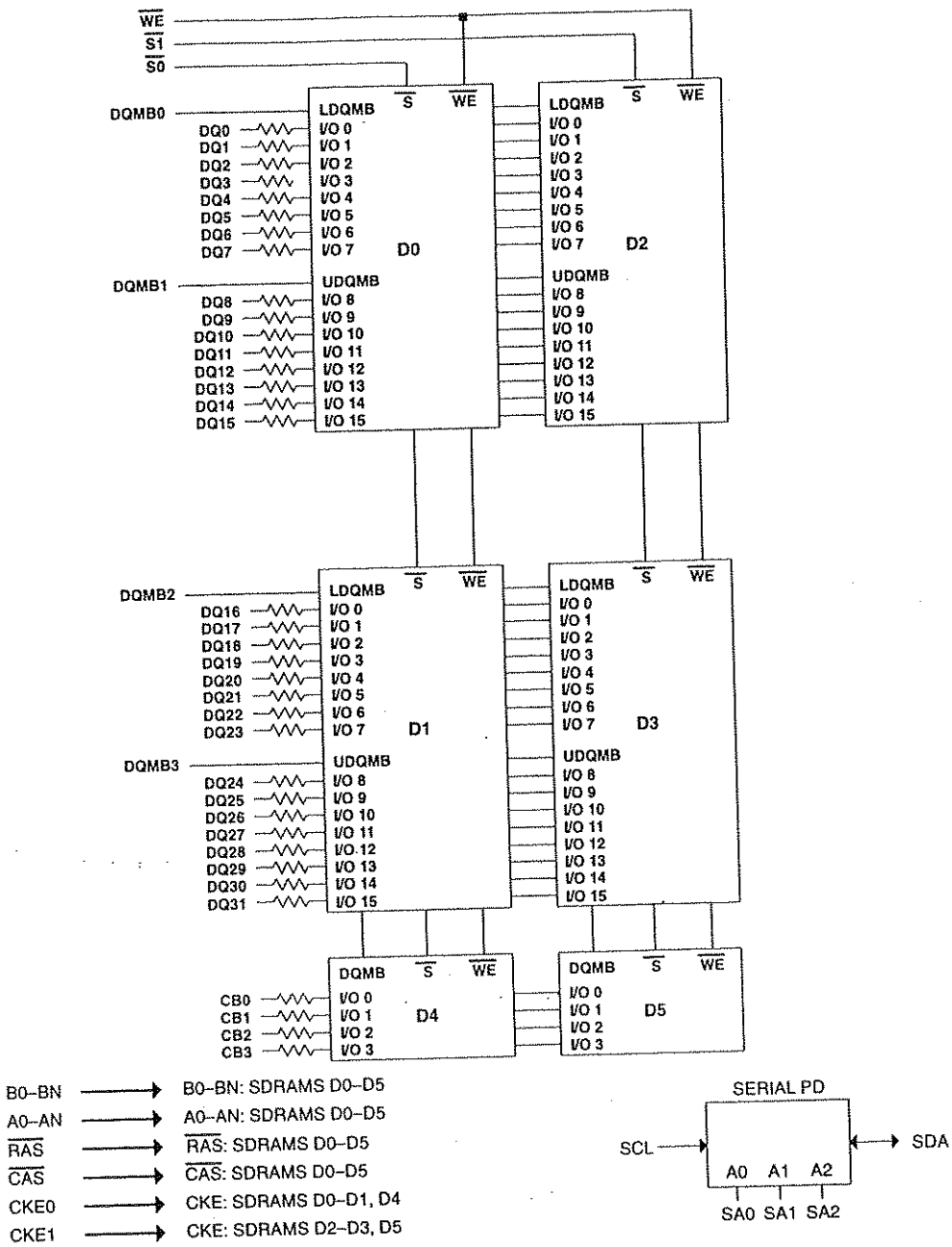
Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

B0–BN → B0–BN: SDRAMS D0–D9
A0–AN → A0–AN: SDRAMS D0–D9
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D9
CKE0 → CKE: SDRAMS D0–D3, D8
CKE1 → CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Figure 4.4.8–Q
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X8 SDRAMs

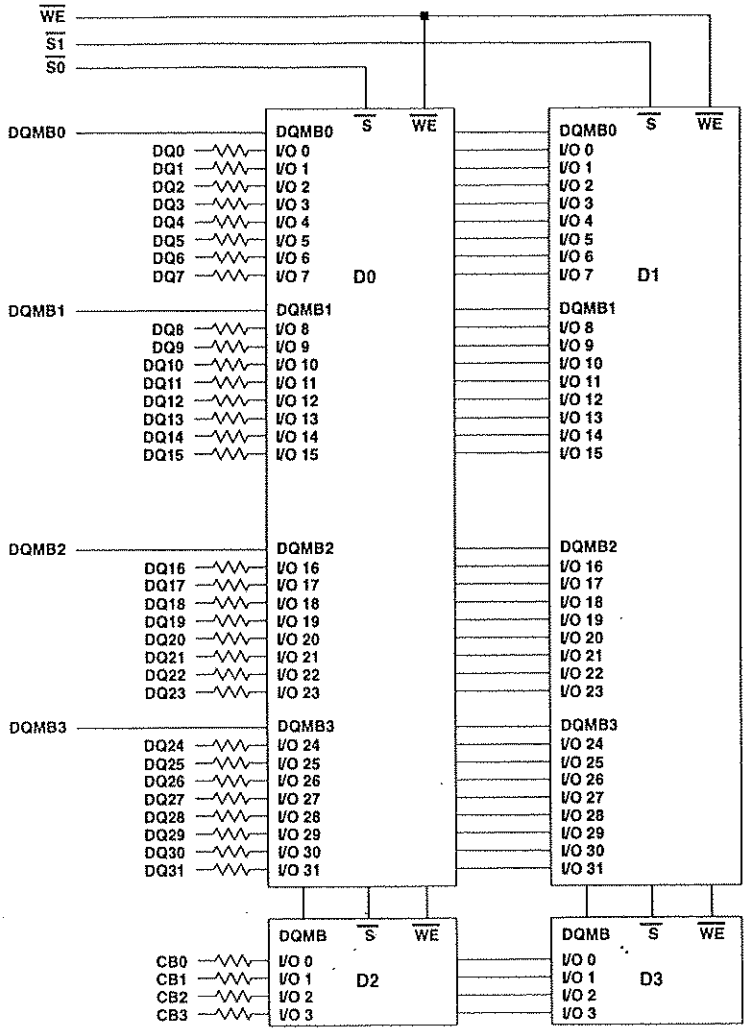


Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

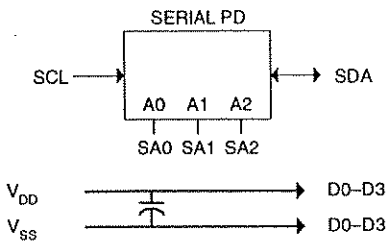
Figure 4.4.8–R
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X16 SDRAMs

Release 7



B0–BN → B0–BN: SDRAMS D0–D3
A0–AN → A0–AN: SDRAMS D0–D3
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D3
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D3
CKE0 → CKE: SDRAMS D0, D2
CKE1 → CKE: SDRAMS D1, D3

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

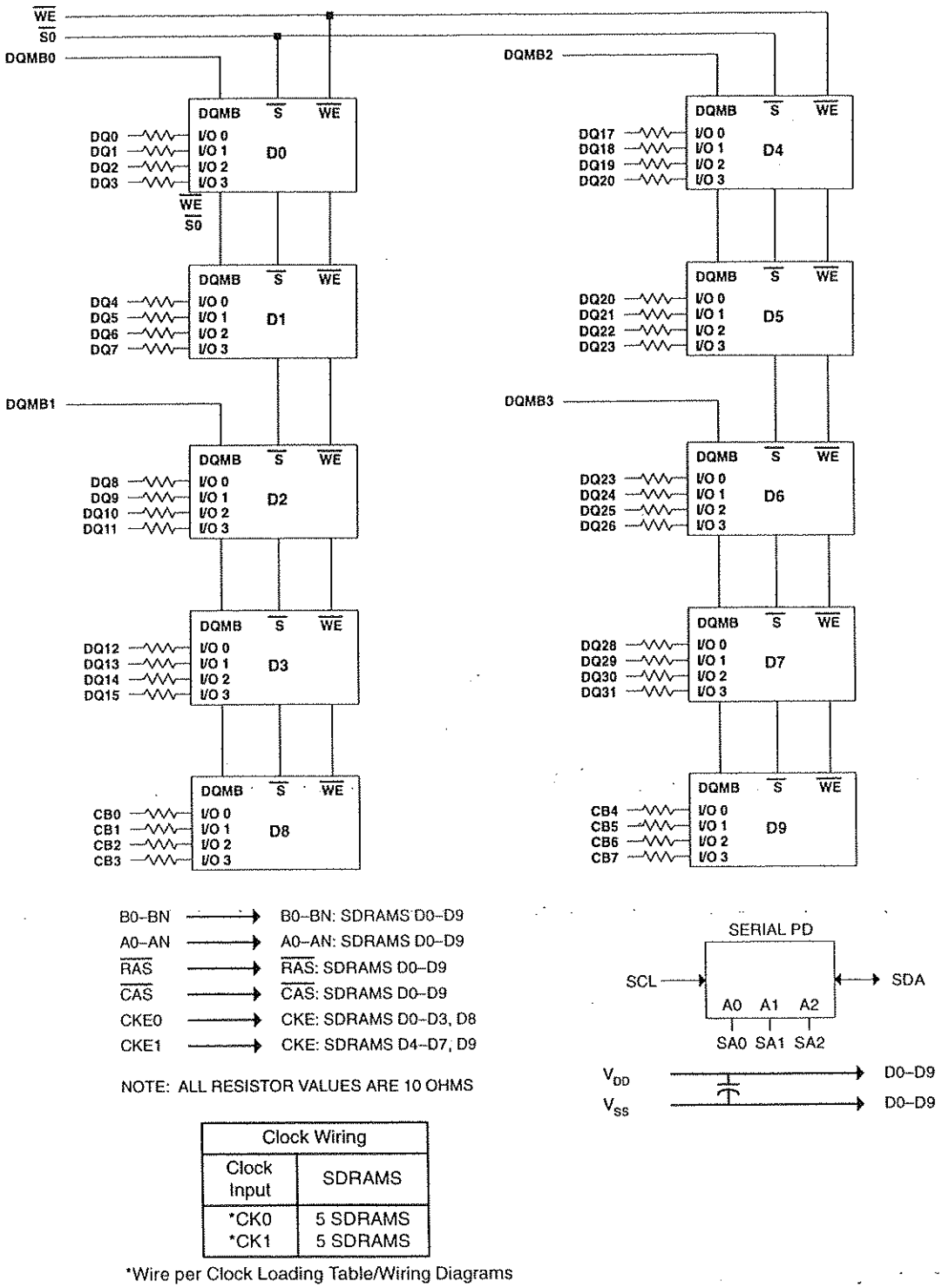


Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–S
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X32 SDRAMs

Release 7



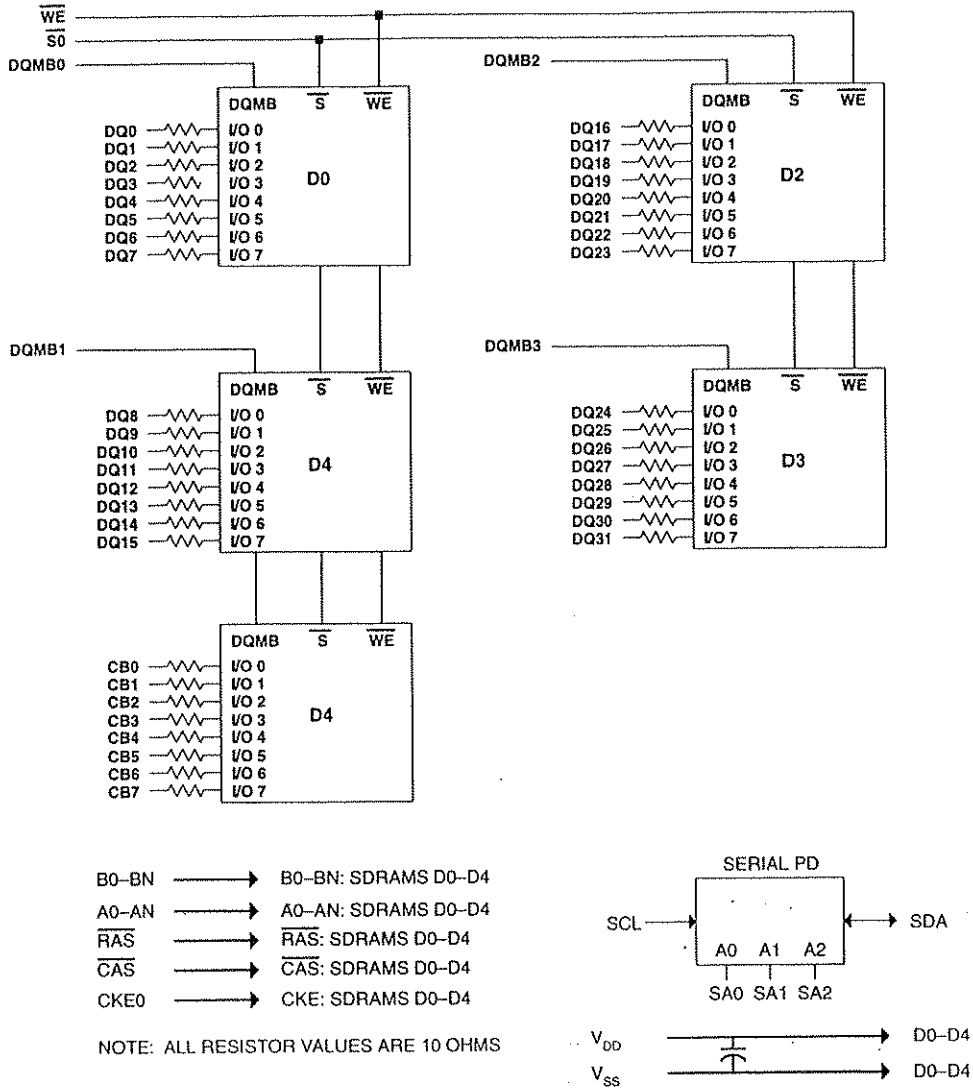
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–T
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs

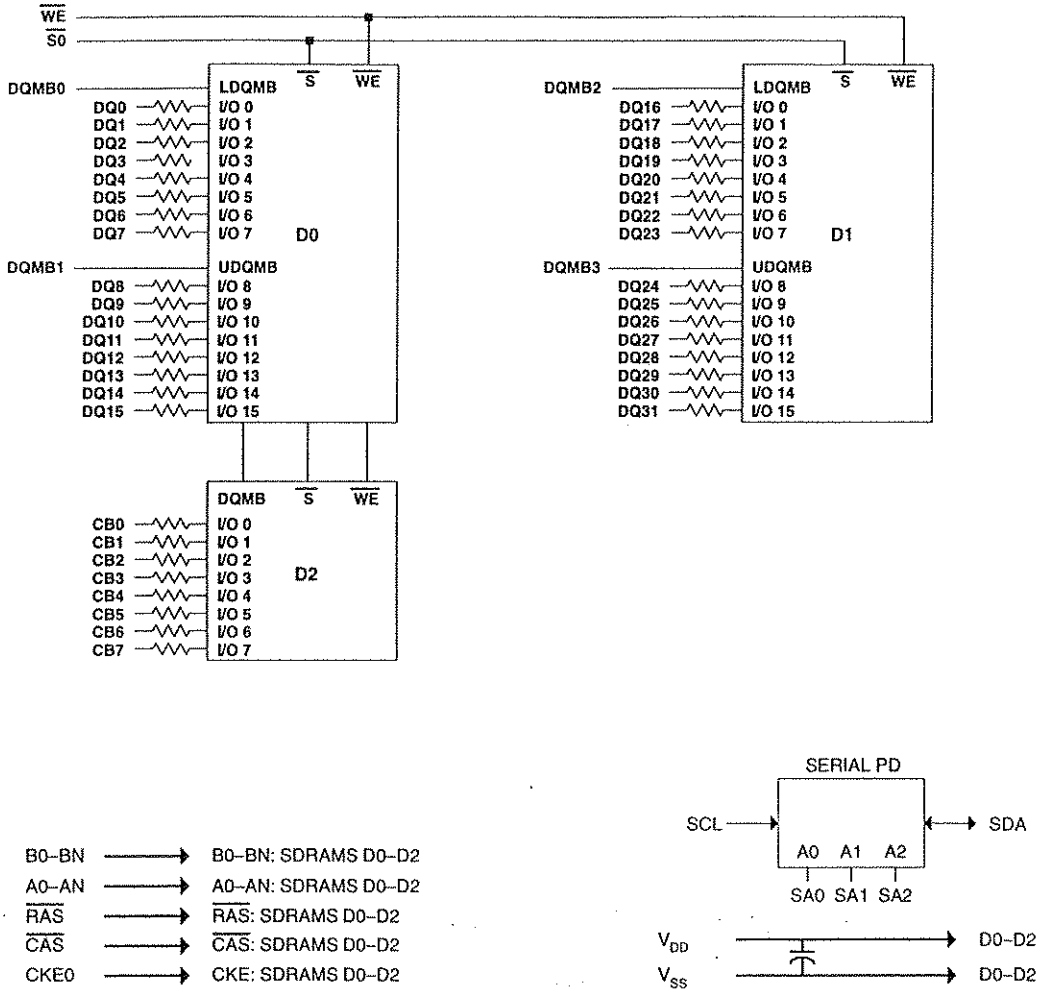
Release 7



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

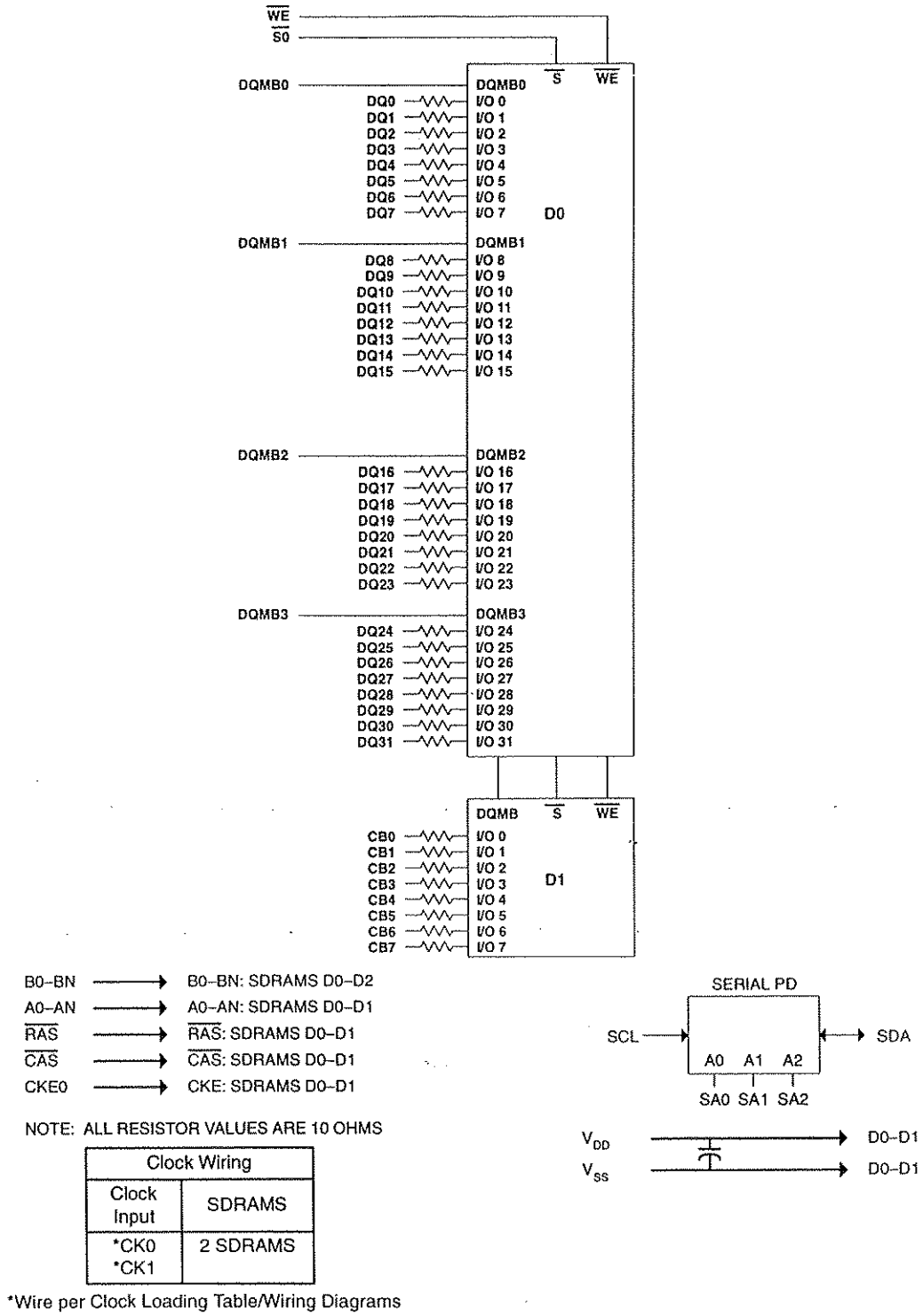
Figure 4.4.8–U
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–V
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X16 SDRAMs



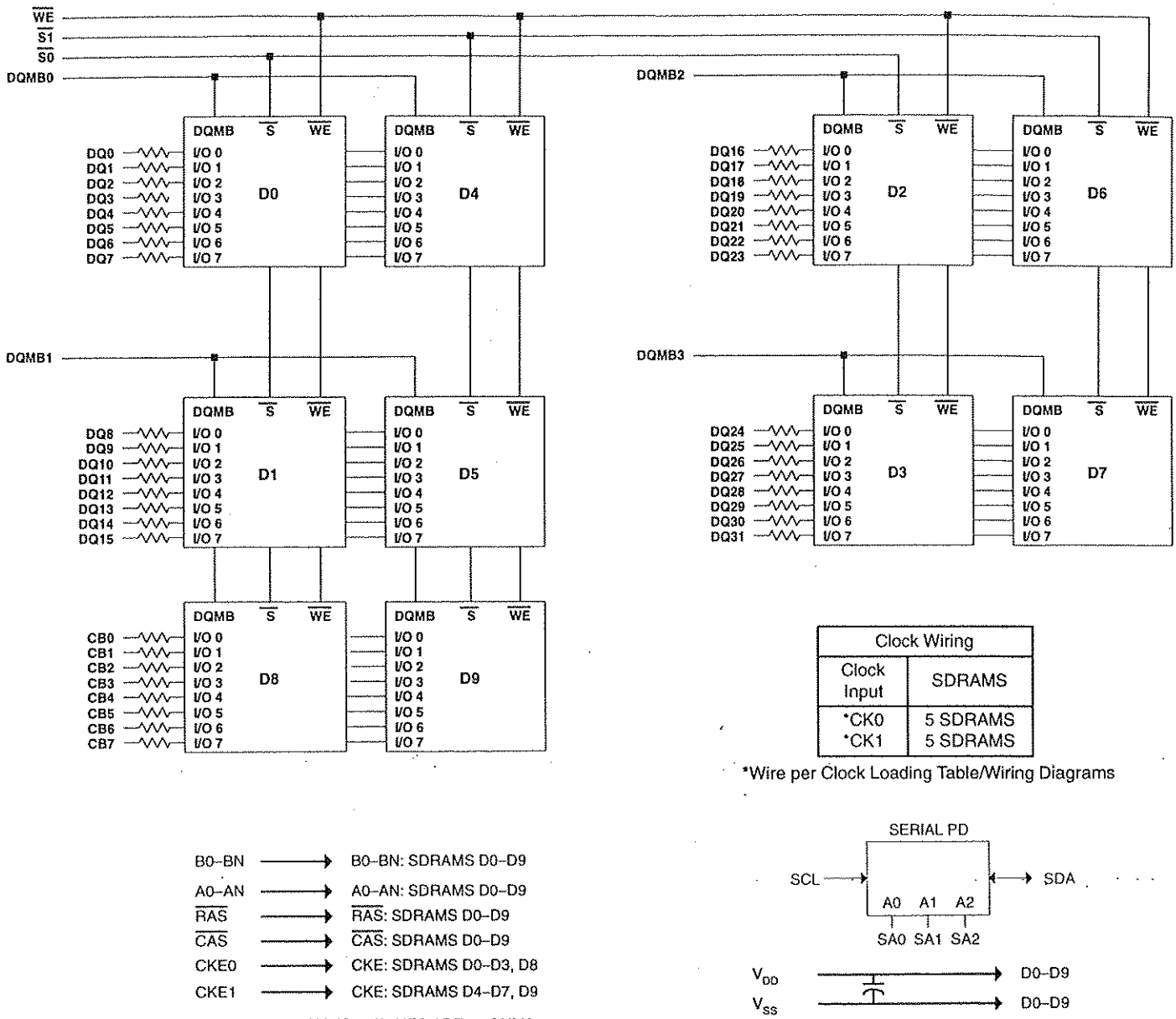
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–W
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X32 SDRAMs

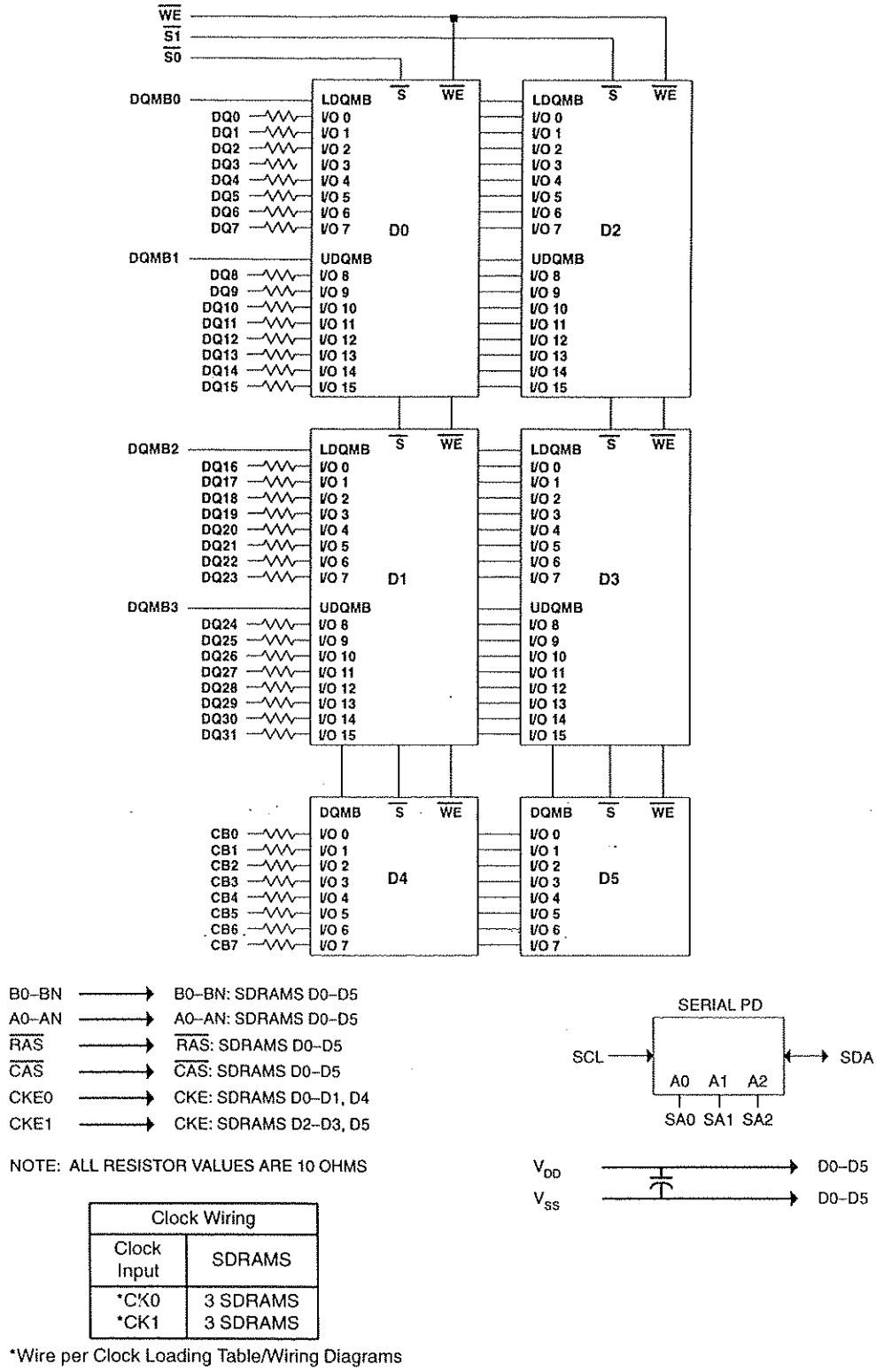
Release 7



Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–X
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 SDRAMs



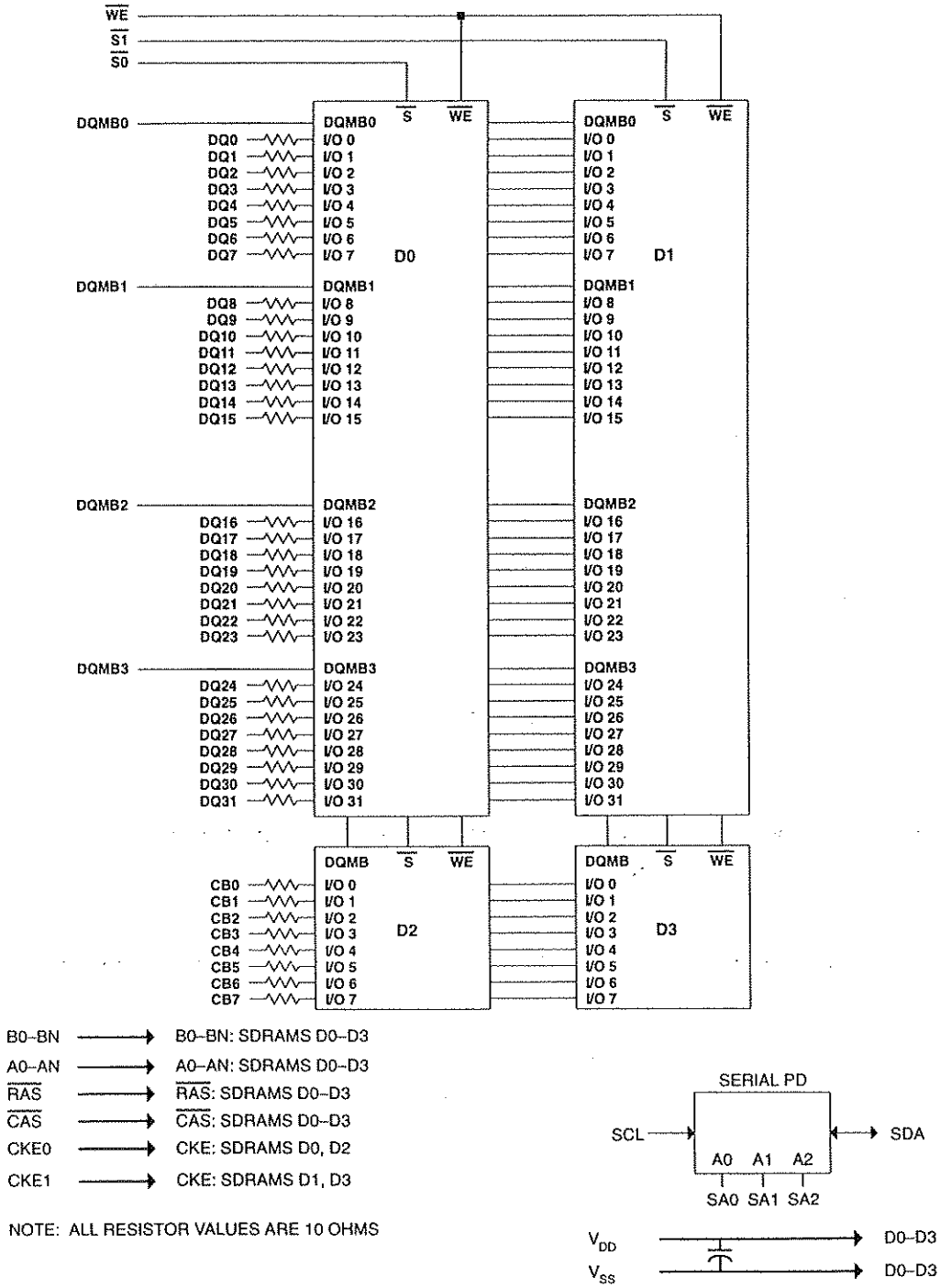
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Y
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X16 SDRAMs

Release 7



Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Z
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X32 SDRAMs

Release 7

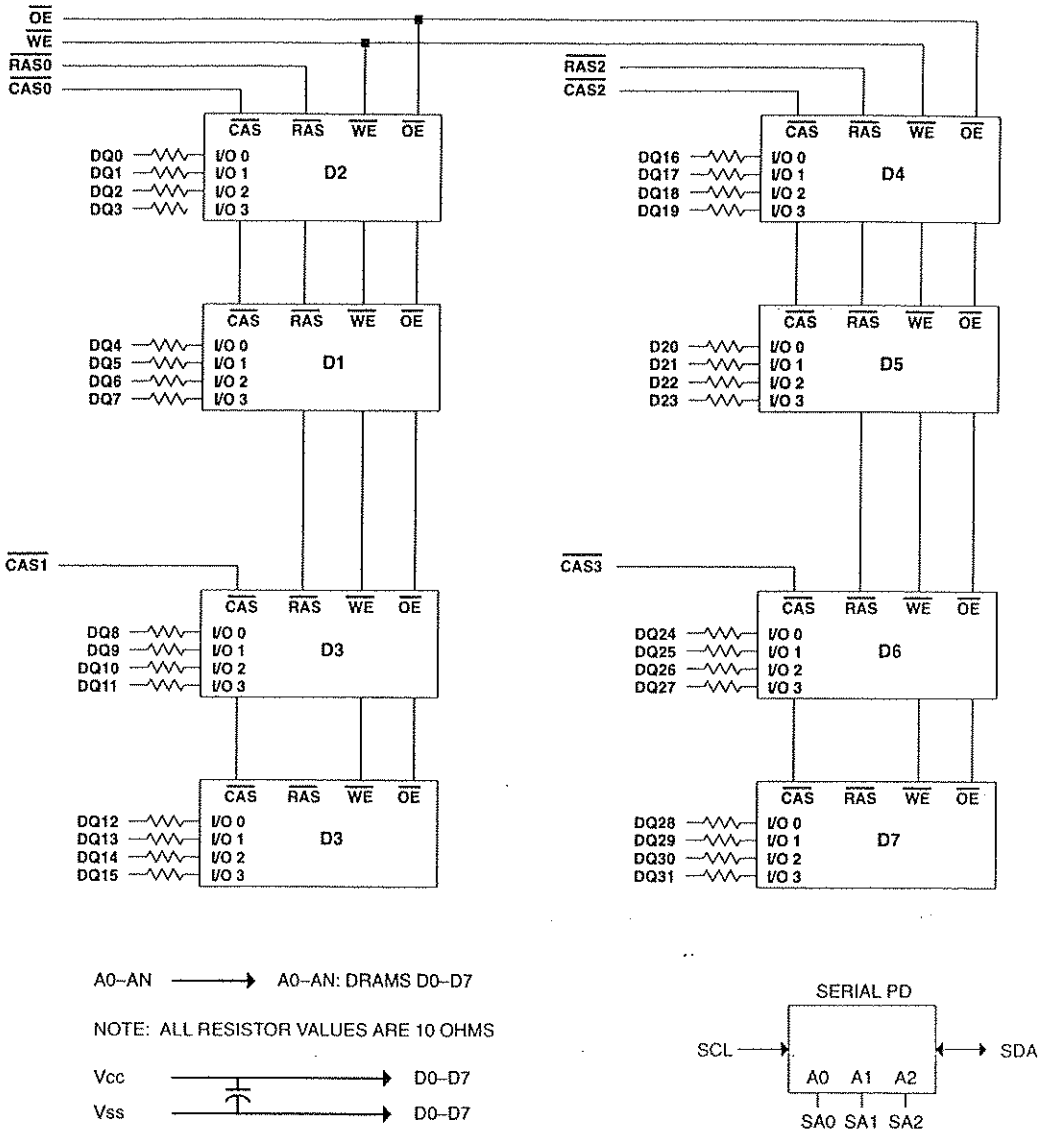


Figure 4.4.8–AA
100 Pin X32 DRAM DIMM, 1 Bank with X4 DRAMs

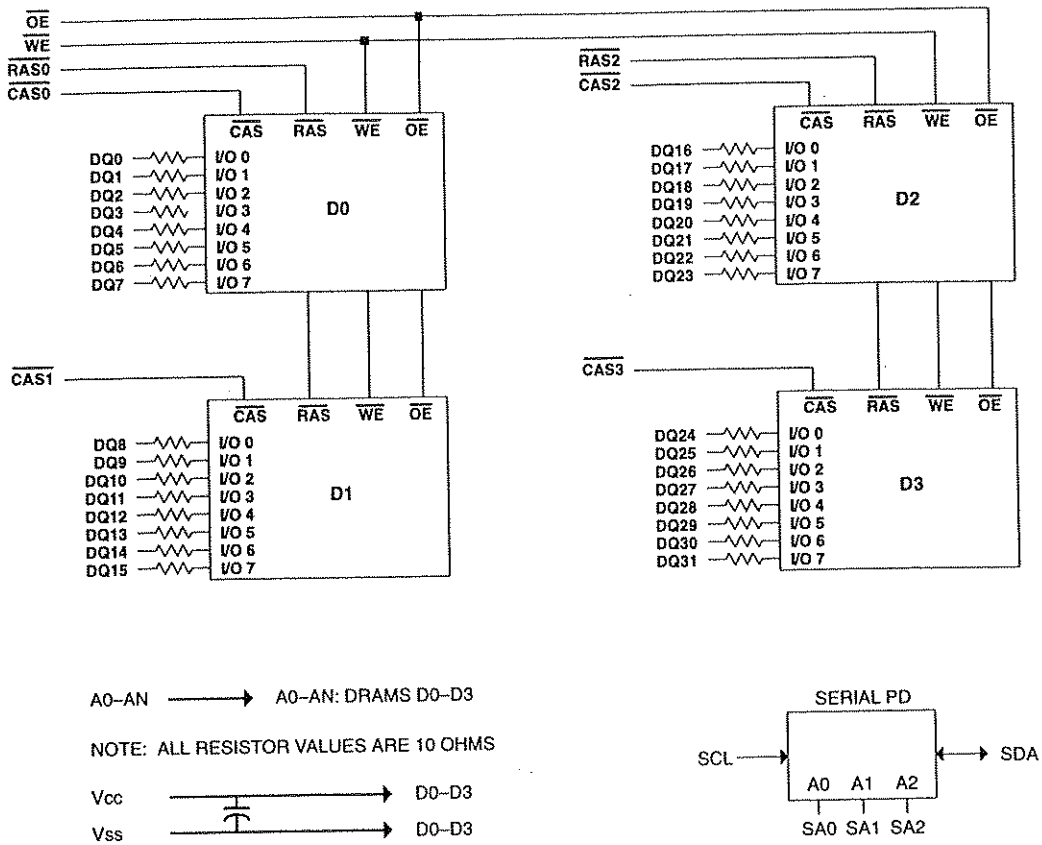


Figure 4.4.8–AB
100 Pin X32 DRAM DIMM, 1 Bank with X8 DRAMs

XILINX EXHIBIT 1010
Page 309

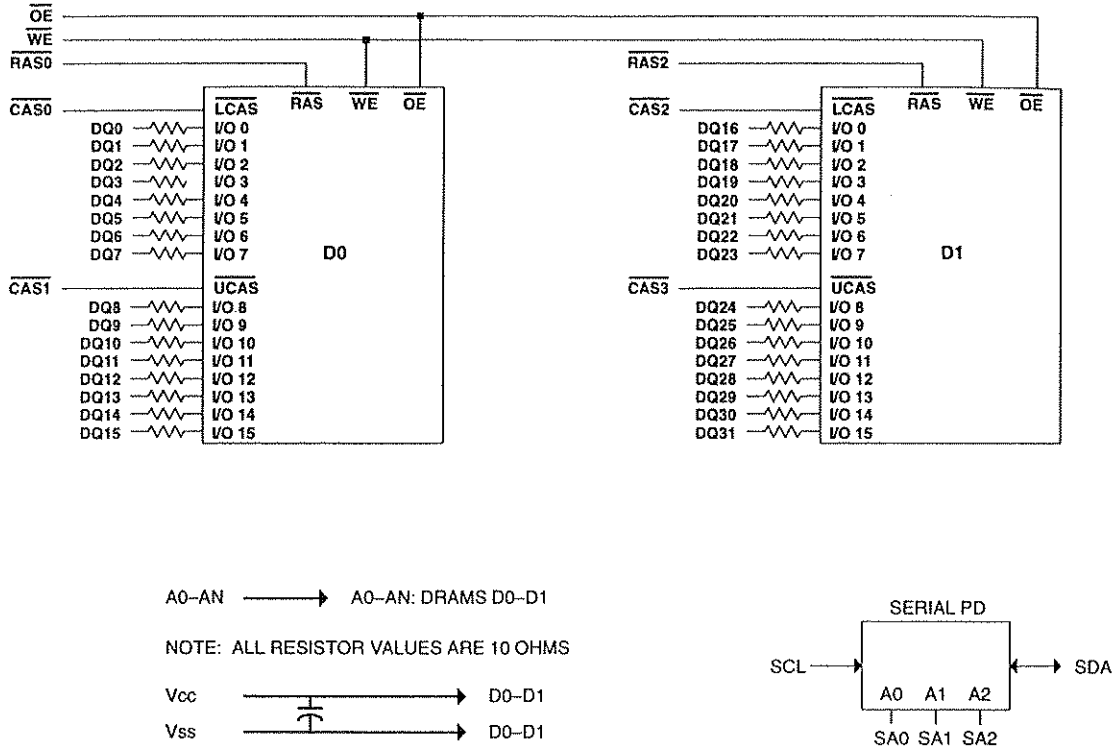


Figure 4.4.8–AC
100 Pin X32 DRAM DIMM, 1 Bank with X16 DRAMs

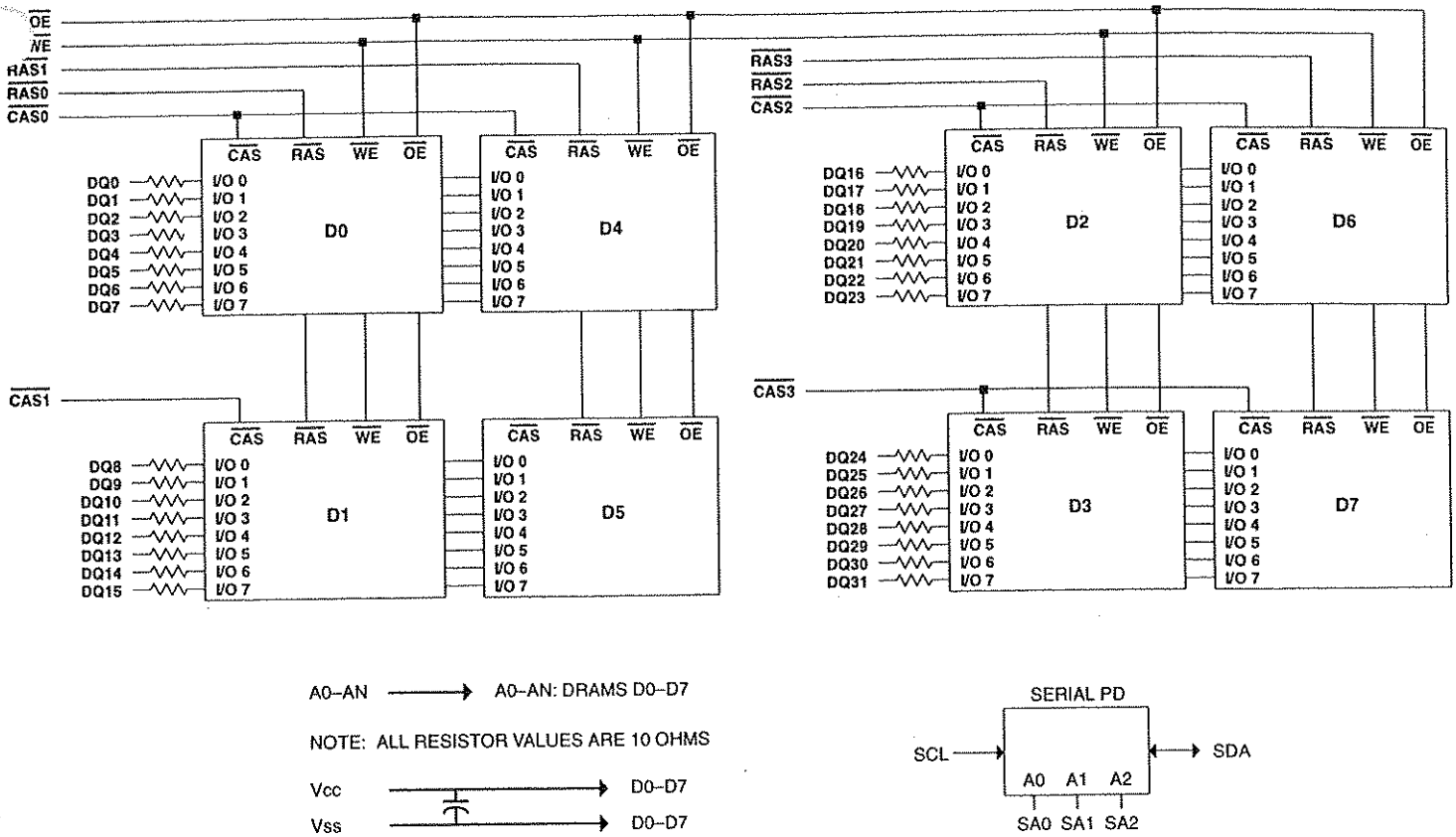


Figure 4.4.8–AD
100 Pin X32 DRAM DIMM, 2 Bank with X8 DRAMs

XILINX EXHIBIT 1010
Page 311

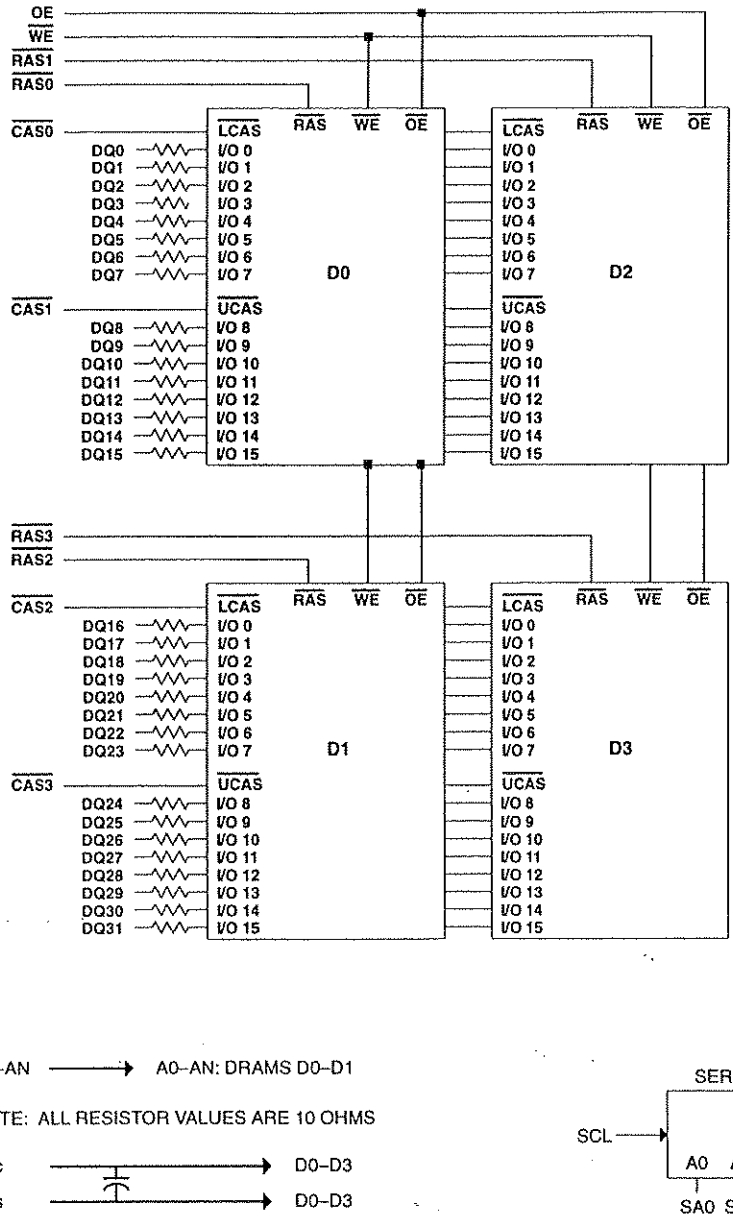


Figure 4.4.8–AE
100 Pin X32 DRAM DIMM, 2 Bank with X16 DRAMs

4.5 Eight Byte Memory Modules

4.5.1 – 168 PIN DRAM DIMM FAMILY

4.5.2 – 200 PIN DRAM DIMM FAMILY

4.5.3 – 168 PIN UNBUFFERED DRAM DIMM FAMILY

4.5.4 – 168 PIN UNBUFFERED SDRAM DIMM FAMILY

4.5.5 – 144 PIN DRAM SO–DIMM FAMILY

4.5.6 – 144 PIN SDRAM SO–DIMM FAMILY

4.5.1 – 168 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.

LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.1–A, 4.5.1–B, & 4.5.1–C

CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.5.1–D

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.1–E through 4.5.1–AB

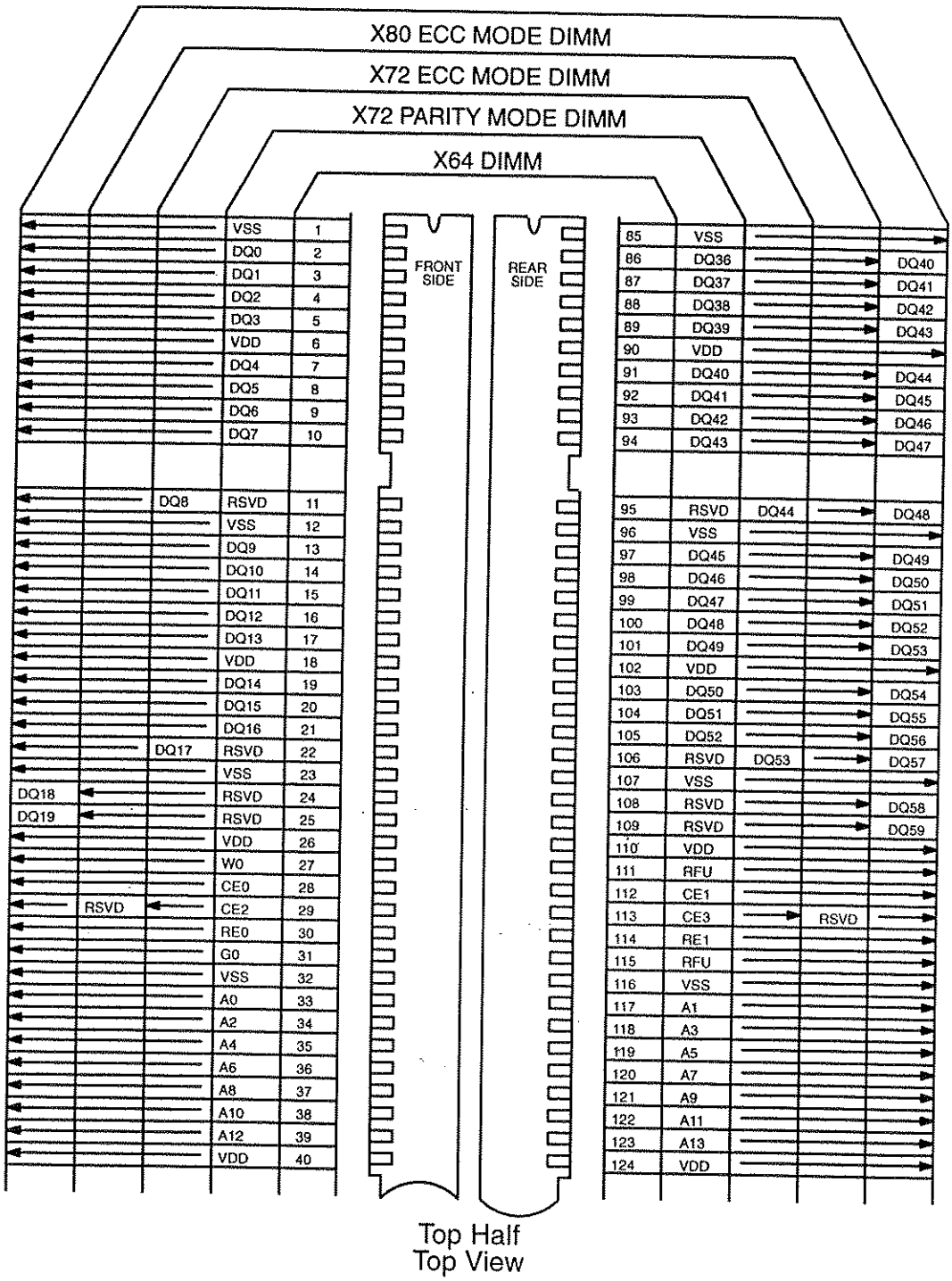


Figure 4.5.1–A
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, TOP HALF

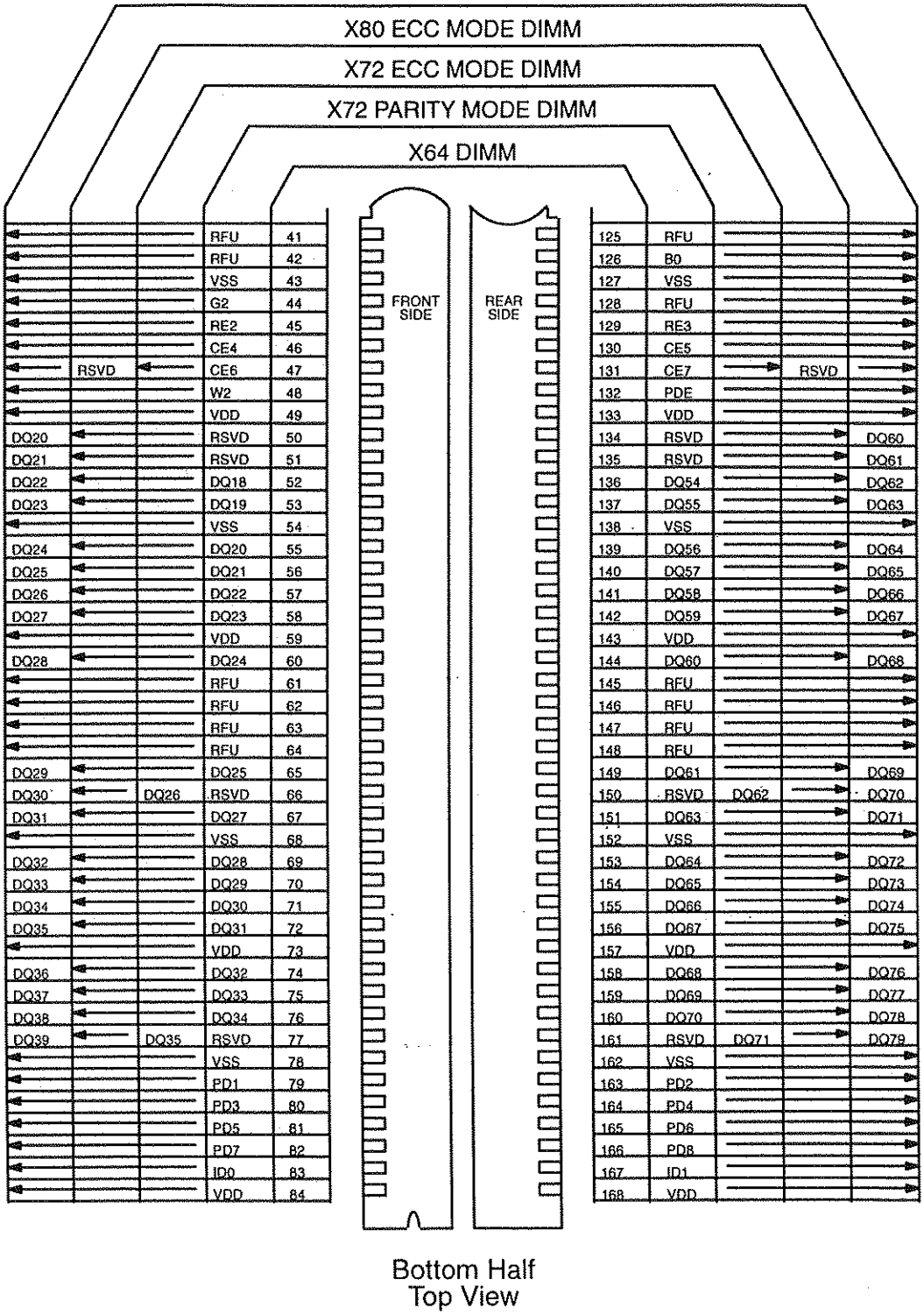


Figure 4.5.1–B
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

JEDEC Standard No. 21–C
Page 4.5.1–4

PD 4	PD 3	PD 2	PD 1	DIMM CONFIGURATION (Parity, ECC)	# BANKS	DRAM CONFIGURATION	DRAM ROW ADDR.	DRAM COL. ADDR.	Av. REFRESH INTERVAL NORMAL (µS)	SLOW
0	0	0	0	256K X 64/72, 72	1	256K X 16/18	9	9	15.6	125
0	0	0	1	512K X 64/72, 72	2	256K X 16/18	9	9	15.6	125
0	0	1	0	512K X 64/72, 72/80	1	512K X 8/9	10	9	15.6	125
0	0	1	1	1M X 64/72, 72/80	2	512K X 8/9	10	9	15.6	125
0	1	0	0	1M X 64/72, 72/80	1	1M X 4/16/18	10	10#	15.6	125
0	1	0	1	2M X 64/72, 72/80	2	1M X 4/16/18	10	10#	15.6	125
0	1	1	0	1M X 64/72, 72	1	1M X 16/18	12	8	15.6	31.2
1	0	0	0	2M X 64/72, 72	2	1M X 16/18	12	8	15.6	31.2
1	0	0	1	2M X 64/72, 72/80	1	2M X 8	11	10	15.6	62.5
1	0	1	0	4M X 64/72, 72/80	2	2M X 8	11	10	15.6	62.5
1	0	1	1	4M X 72	1	4M X 1/4	12**	11**	15.6	31.2
1	0	1	1	4M X 64, 72/80	1	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	0	8M X 64/72, 72/80	2	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	1	8M X 64/72, 72/80	1	8M X 8	12	11	15.6	31.2
1	1	1	0	16M X 64/72, 72/80	2	8M X 8	12	11	15.6	31.2
1	1	1	1	16M X 64/72, 72/80	1	16M X 4	13/12	11/12	15.6	TBD/31.2
0	0	0	0	16M X 64/72, 72	1	16M X 16	13/12	11/12	15.6	TBD/31.2
0	0	0	1	32M X 64/72, 72/80	2	16M X 4/16	13/12	11/12	15.6	TBD/31.2
0	0	1	0	32M X 64/72, 72/80	1	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	0	1	1	64M X 64/72, 72/80	2	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	1	0	0	64M X 64/72, 72/80	1	64M X 4	14/13	12/13	7.8/15.6	TBD*
0	1	1	1	Expansion						

Note 1) * These modules using 256M devices are for reference only and will be further defined in the future.
Note 2) 1 = Logic high ; 0 = Logic low; In Table Information.
Note 3) ** This addressing includes a redundant address to allow mixing of 12/10(X4) and 11/11(X1) DRAMs
Note 4) # 1M X 16/18 DRAMS with 10/10 addressing may dissipate excessive power in many applications. Care must be taken to ensure device thermal limits are not exceeded. 12/8 addressing is provided as a lower power option.
PD Note: PD & ID terminals must each be pulled up through a resistor to VDD at the next higher level assembly. PDs will either be open or driven to VOH or driven to VOL via on–board buffer circuits.
ID Note: IDs will either be open (NC) or connected directly to VSS without a buffer.

	PD7	PD6
SPEED (tRAC)	82	165
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

	PD8	ID0
CONFIGURATION	166	83
X64	1	0
X72 PARITY	1	1
X72 ECC	0	0
X80 ECC	0	1
DATA CONFIGURATION		

	ID1
REFRESH MODE	167
NORMAL	0
SELF–REFRESH	1
REFRESH MODE	

DATA ACCESS MODE	PD5
	81
FAST PAGE	0
FP W/EDO	1
EDO DETECTION	

Figure 4.5.1–C
168 PIN, 64, 72, or 80 BIT DIMM PRESENCE DETECT & CONFIGURATION TABLES

64, 72, & 80 BIT DRAM DIMM CAPACITY IN M BYTE																				
Memory Device / DIMM Configuration	4M DRAM					16M DRAM					64M DRAM					256M DRAM				
	256K		512K		1M	1M		2M		4M	4M		8M		16M	16M		32M		64M
	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4
256K X 64		4																		
256K X 72	4																			
256K X 72 (ECC)	4																			
256K X 80 (ECC)																				
512 X 64		8		8																
512K X 72	8		8																	
512K X 72 (ECC)	8		8	9																
512K X 80 (ECC)				10																
1M X 64				16	16		4													
1M X 72			16		18	4														
1M X 72 (ECC)			16	18	18	4														
1M X 80 (ECC)				20	20															
2M X 64							8		8											
2M X 72						8		8												
2M X 72 (ECC)						8		8	9											
2M X 80 (ECC)									10											
4M X 64									16	16		4								
4M X 72								16		18	4									
4M X 72 (ECC)								16	18	18	4									
4M X 80 (ECC)									20	20										
8M X 64												8		8						
8M X 72											8		8							
8M X 72 (ECC)											8		8	9						
8M X 80 (ECC)														10						
16M X 64														16	16		4			
16M X 72													16		18	4				
16M X 72 (ECC)													16	18	18	4				
16M X 80 (ECC)														20	20					
32M X 64																	8		8	
32M X 72																8		8		
32M X 72 (ECC)																8		8	9	
32M X 80 (ECC)																			10	
64M X 64																			16	16
64M X 72																		16		18
64M X 72 (ECC)																		16	18	18
64M X 80 (ECC)																			20	20

Figure 4.5.1–D
168 PIN, 64, 72, & 80 BIT DRAM DIMM Capacity Table

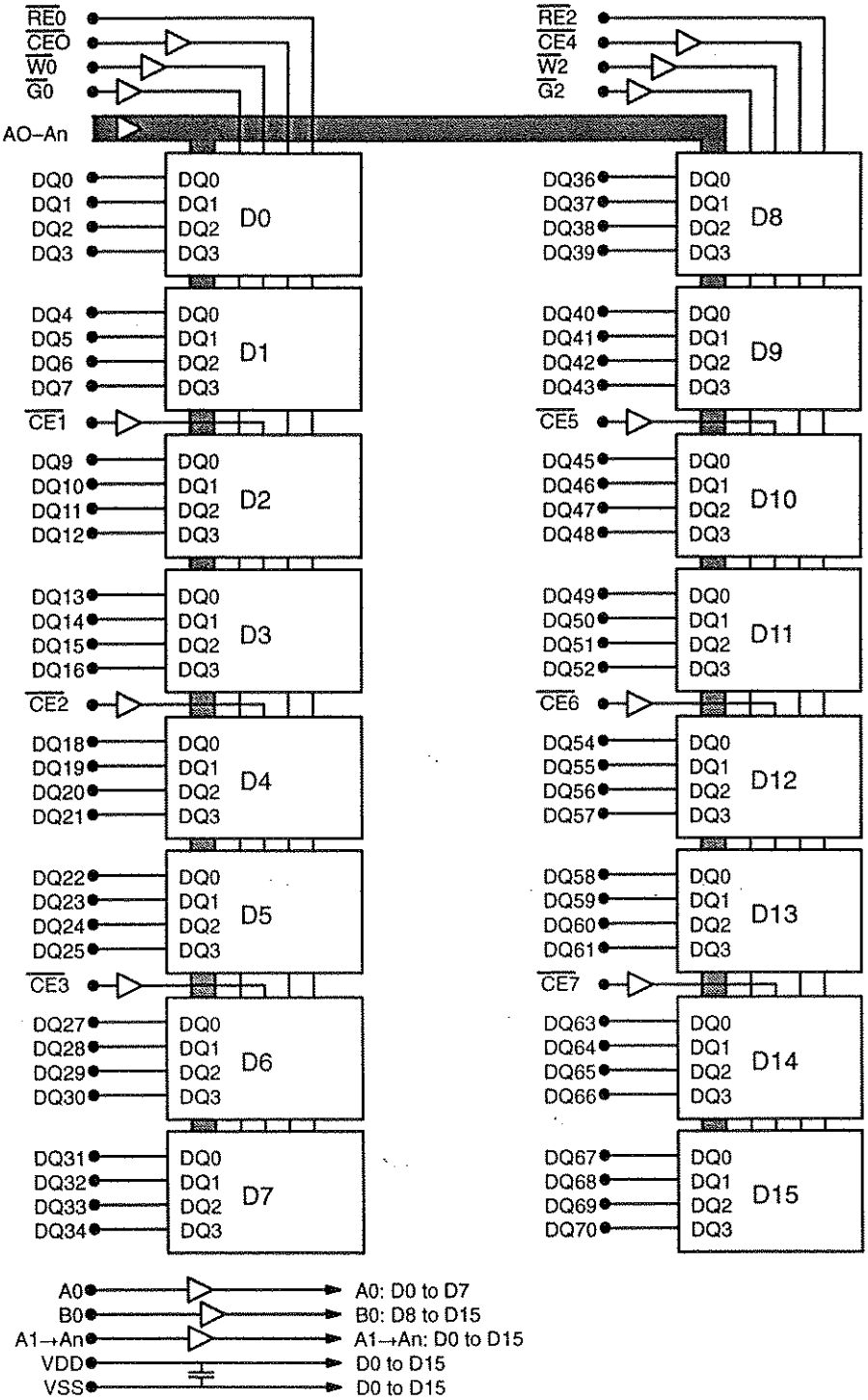


Figure 4.5.1–E
168 PIN, X64 DRAM DIMM, 1 bank with X4 DRAMs

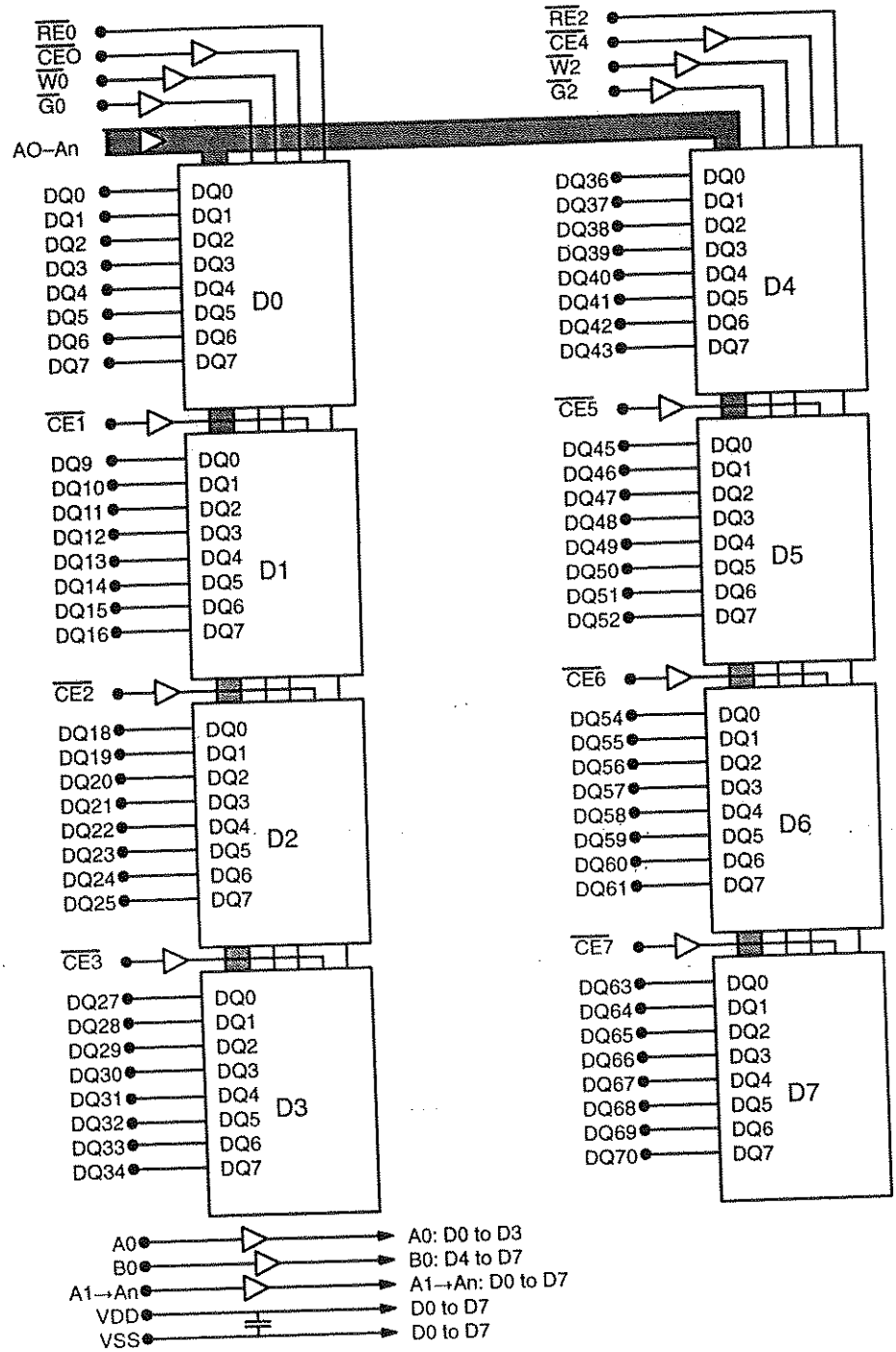


Figure 4.5.1–F
168 PIN, X64 DRAM DIMM, 1 bank with X8 DRAMs

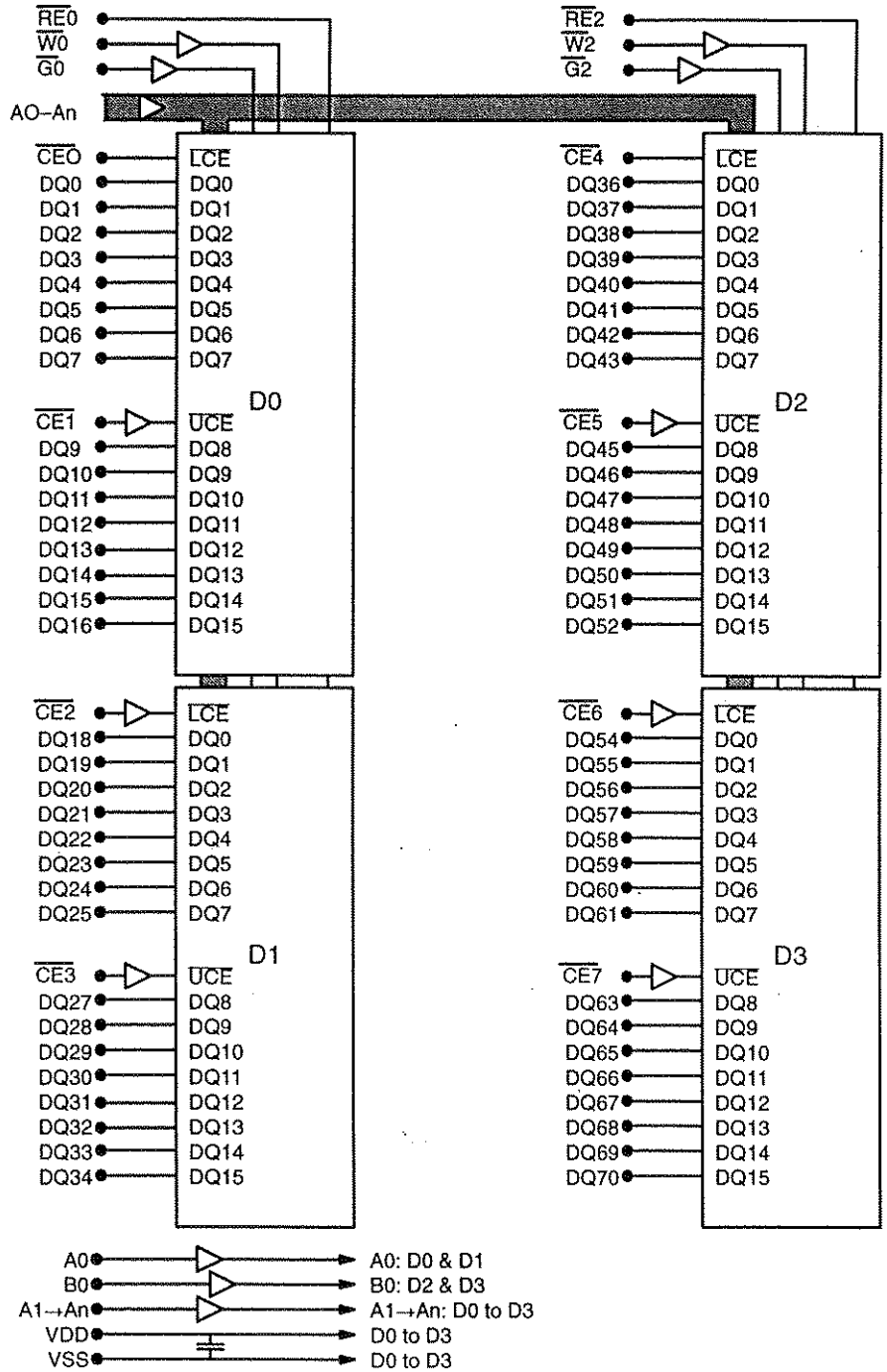


Figure 4.5.1–G
168 PIN, X64 DRAM DIMM, 1 bank with X16 DRAMs

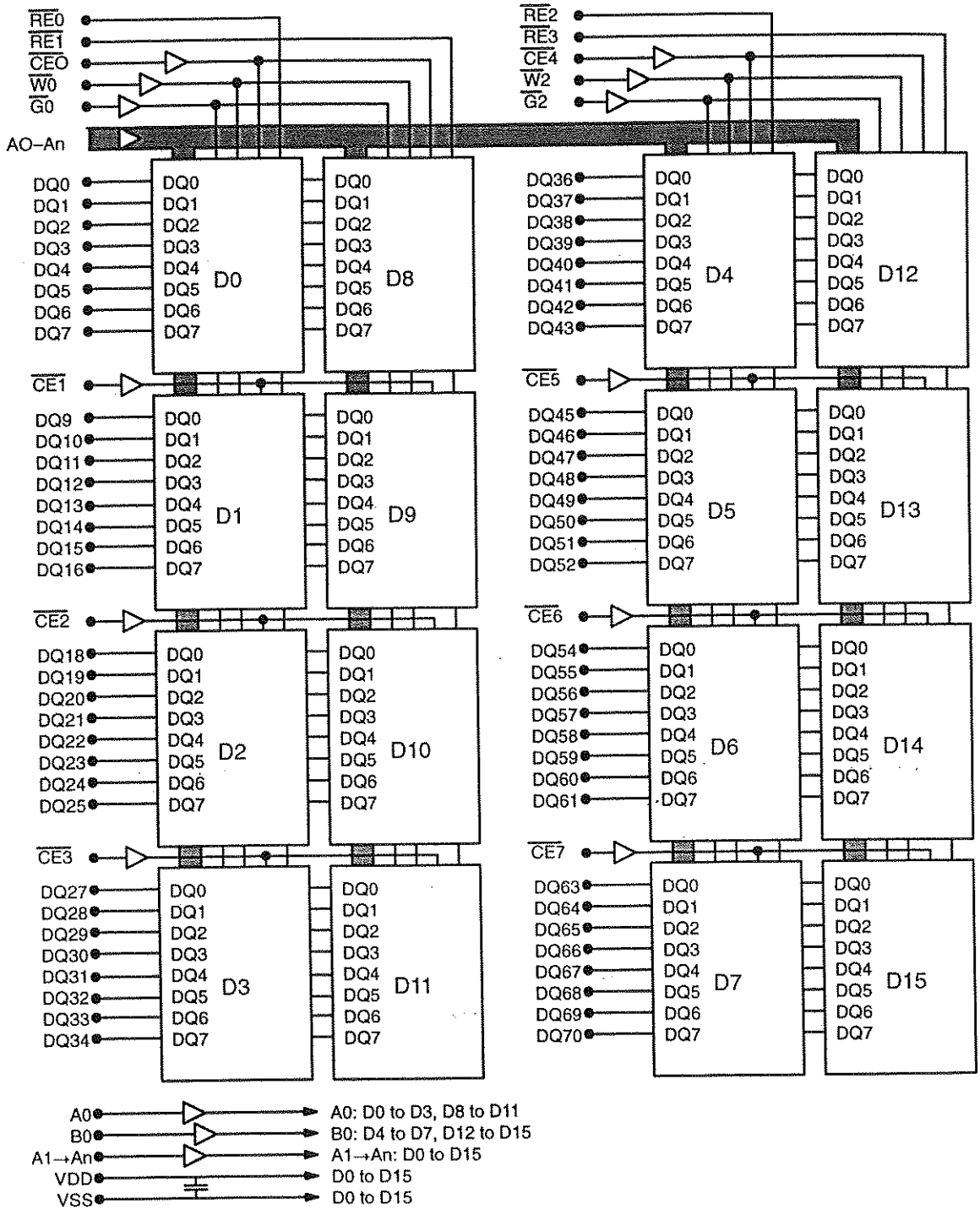


Figure 4.5.1–H
168 PIN, X64 DRAM DIMM, 2 banks with X8 DRAMs

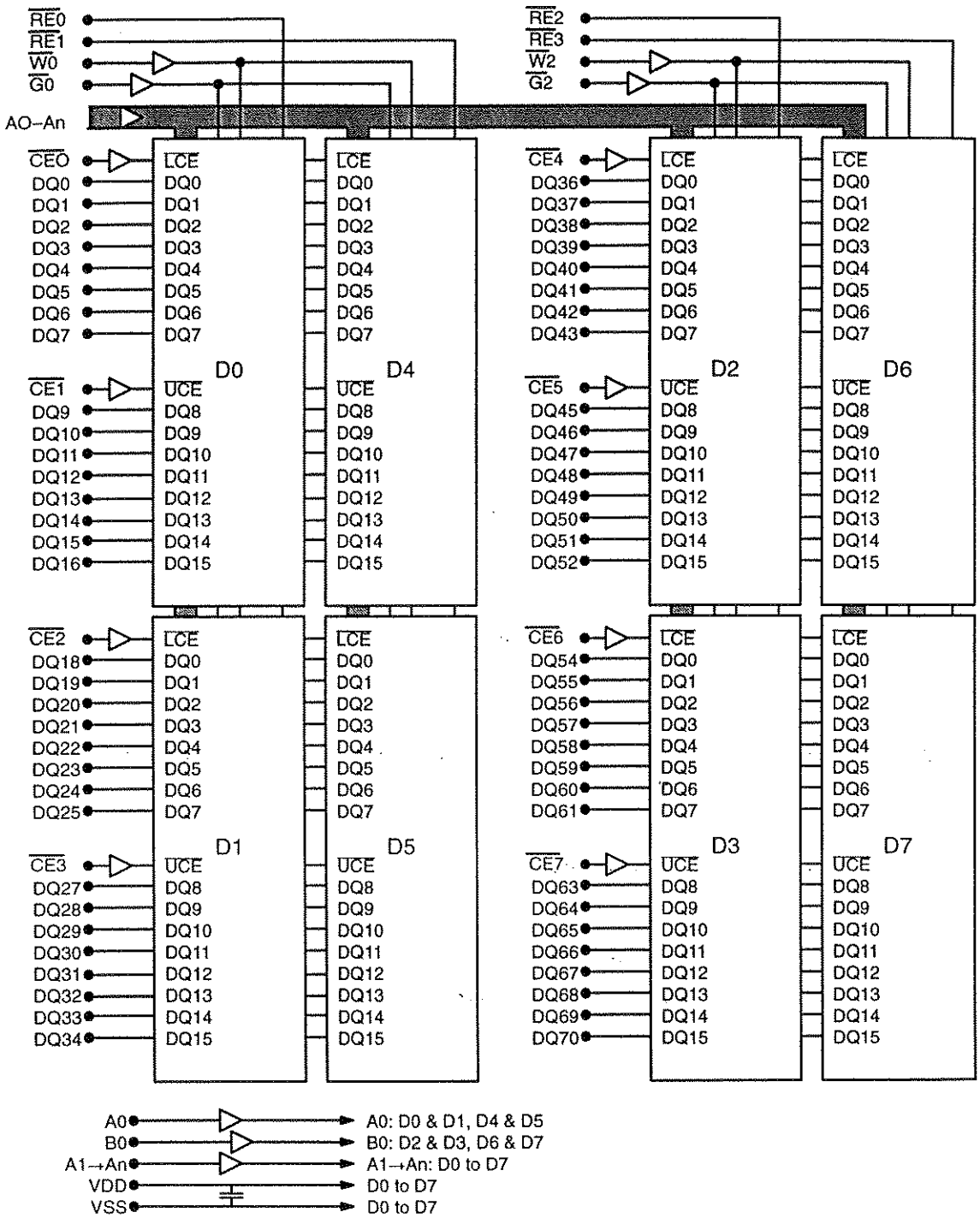


Figure 4.5.1–I
168 PIN, X64 DRAM DIMM, 2 banks with X16 DRAMs

Release 4c7

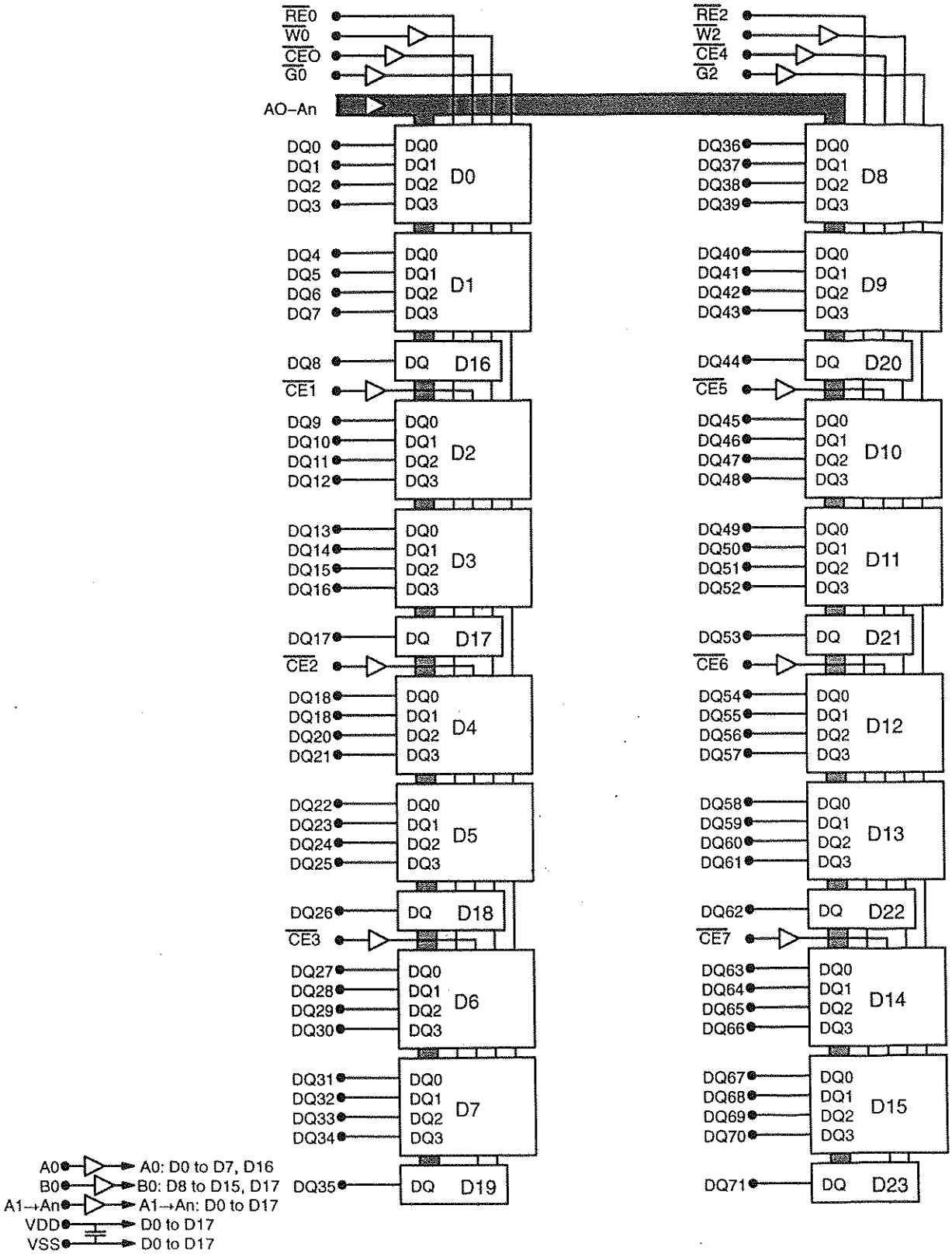


Figure 4.5.1–J

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X1 DRAMs

Release 4c7

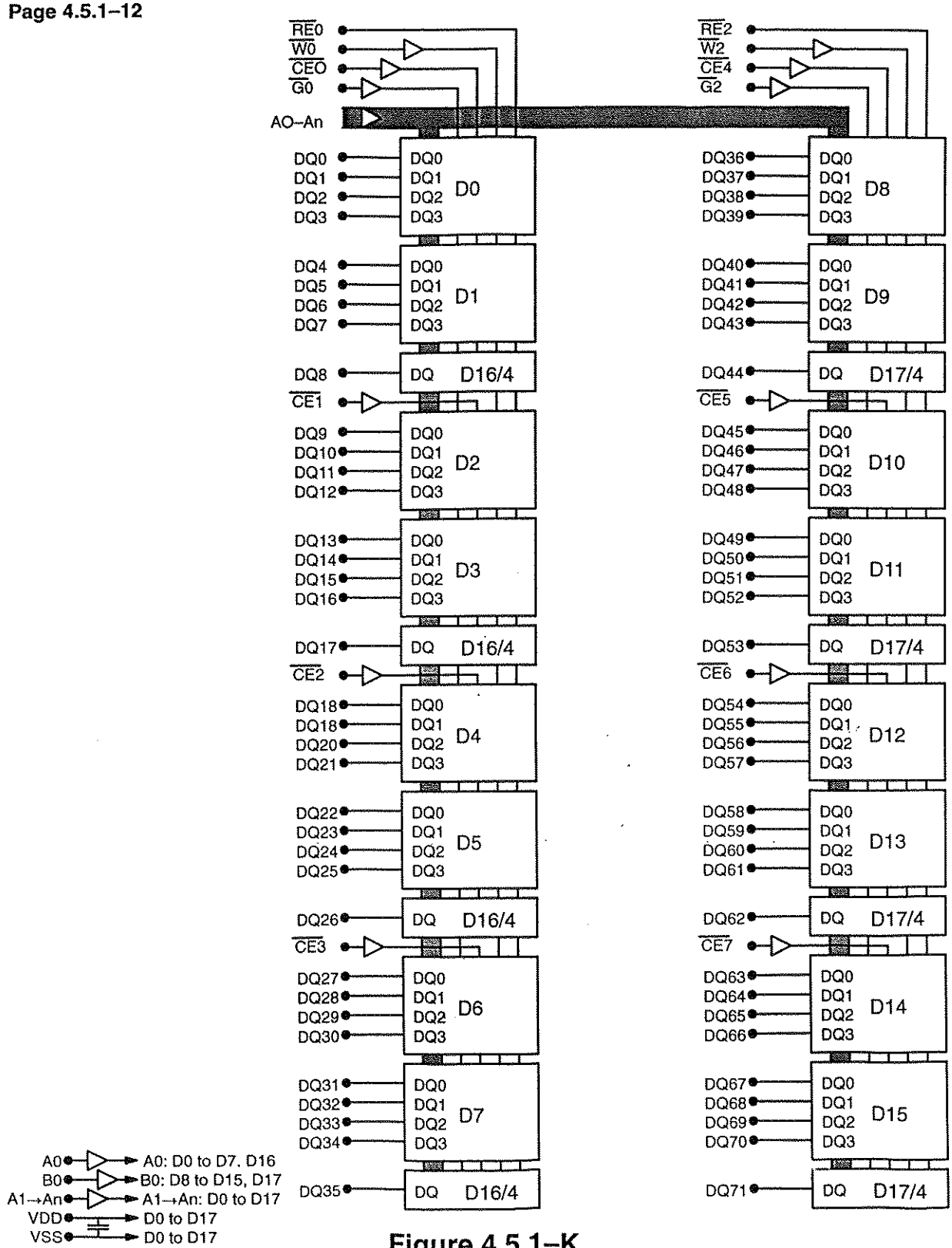


Figure 4.5.1–K
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X4 W/4 $\overline{CE}$ DRAMs

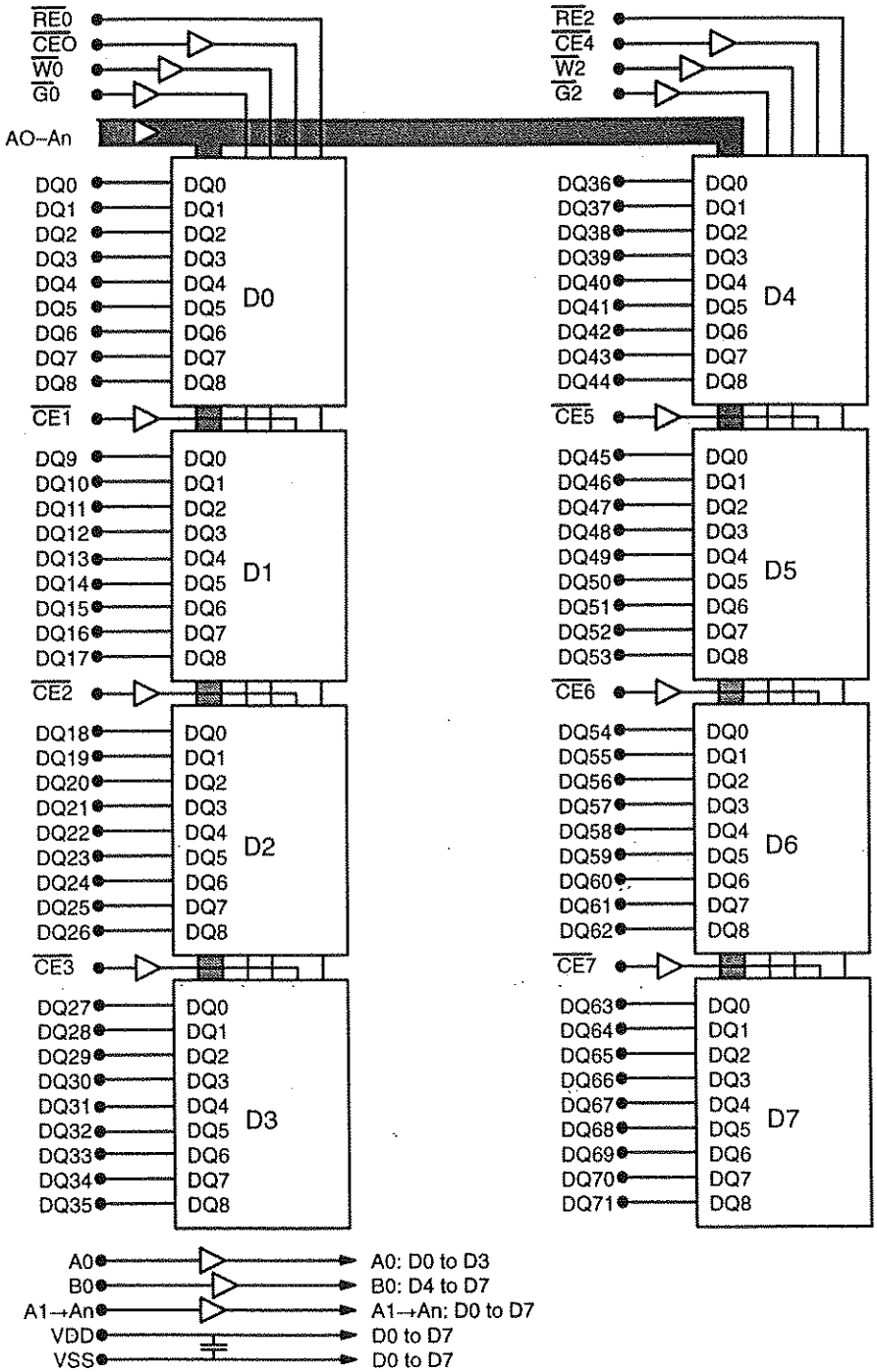


Figure 4.5.1–L
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X9 DRAMs

Release 4–7

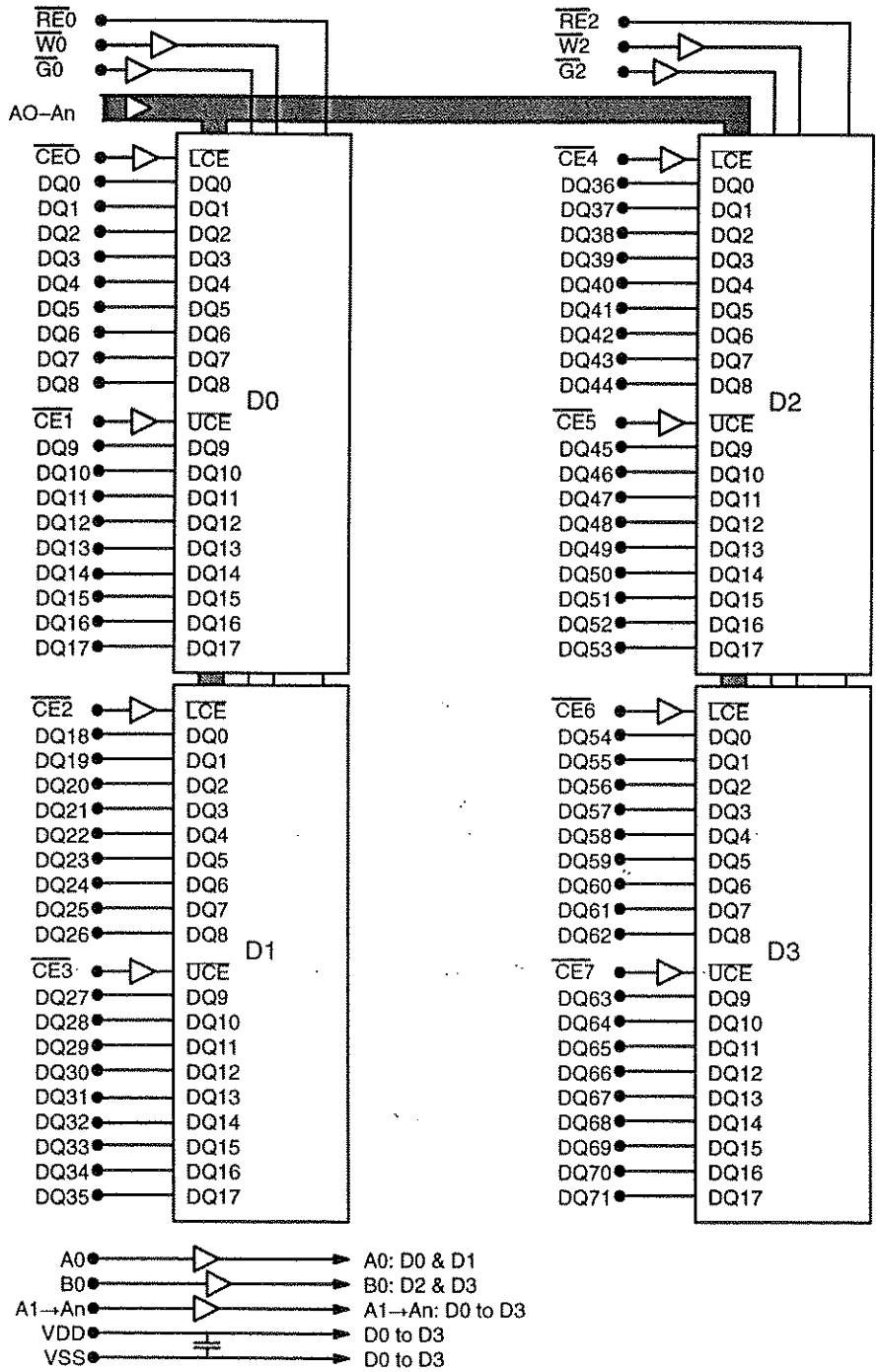


Figure 4.5.1–M
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X18 DRAMs
Release 4c7

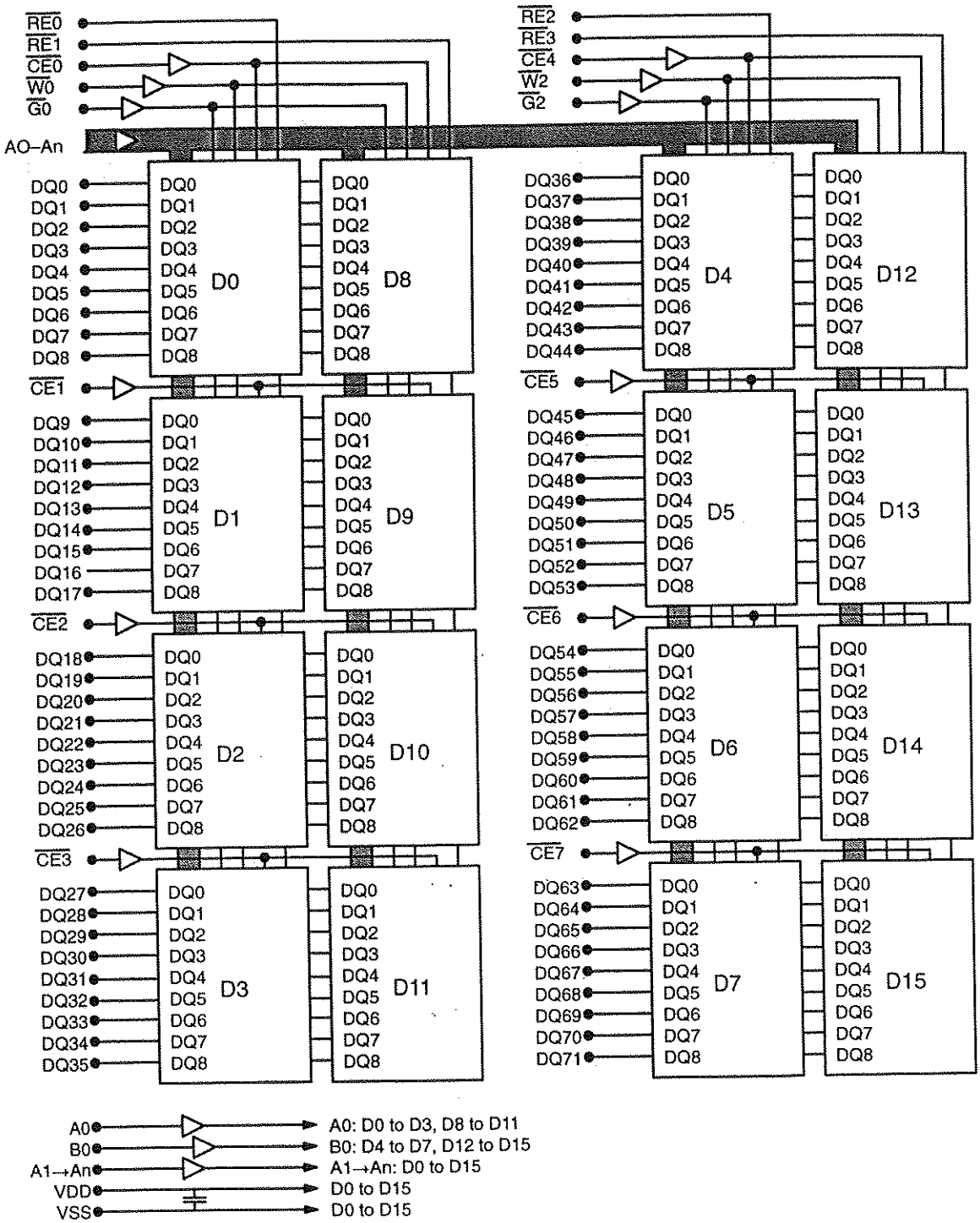


Figure 4.5.1–N
168 PIN, X72 (Parity mode) DRAM DIMM, 2 banks with X9 DRAMs

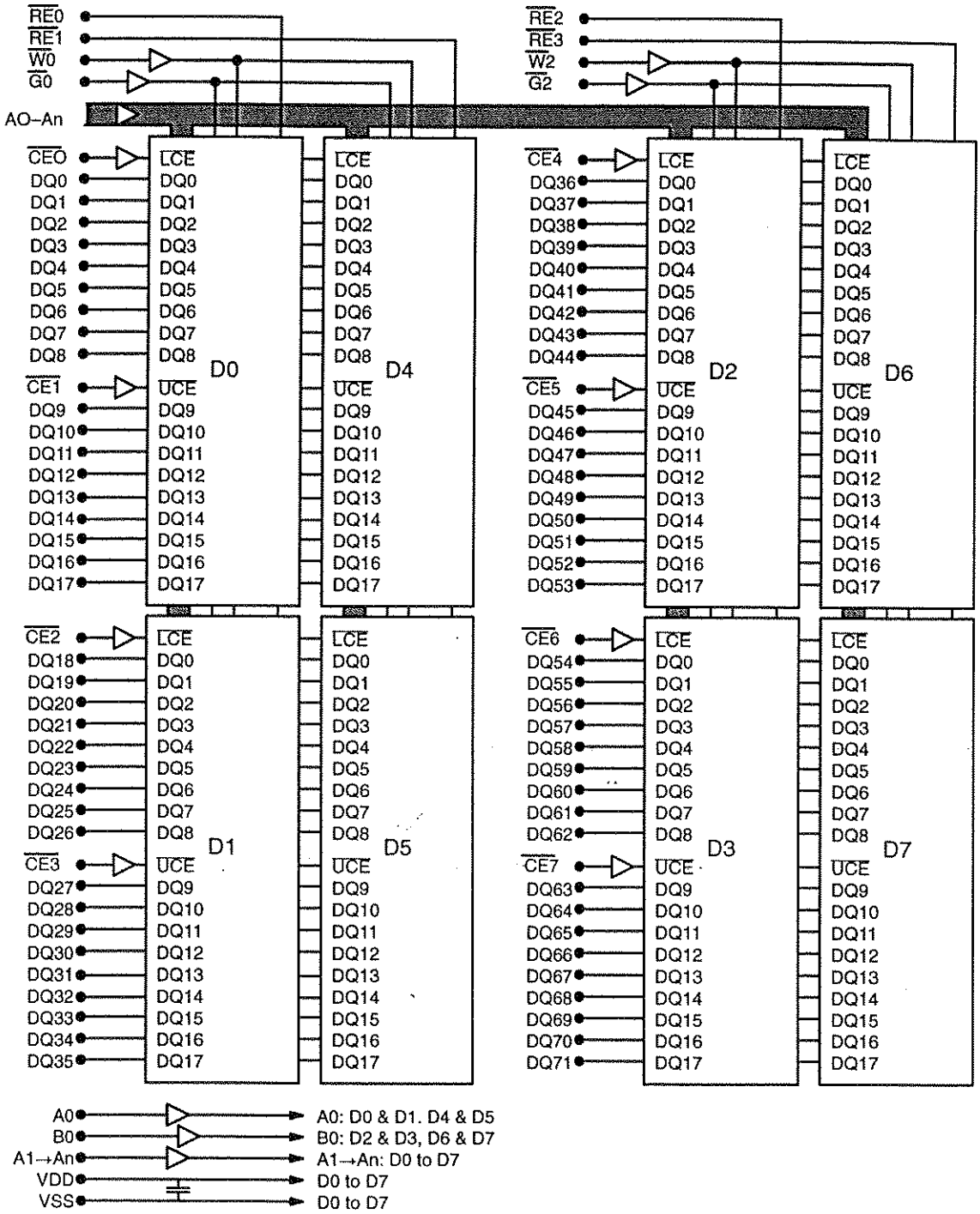


Figure 4.5.1–O
168 PIN, X72 (Parity mode) DRAM DIMM, 2 bank with X18 DRAMs
Release 4–7

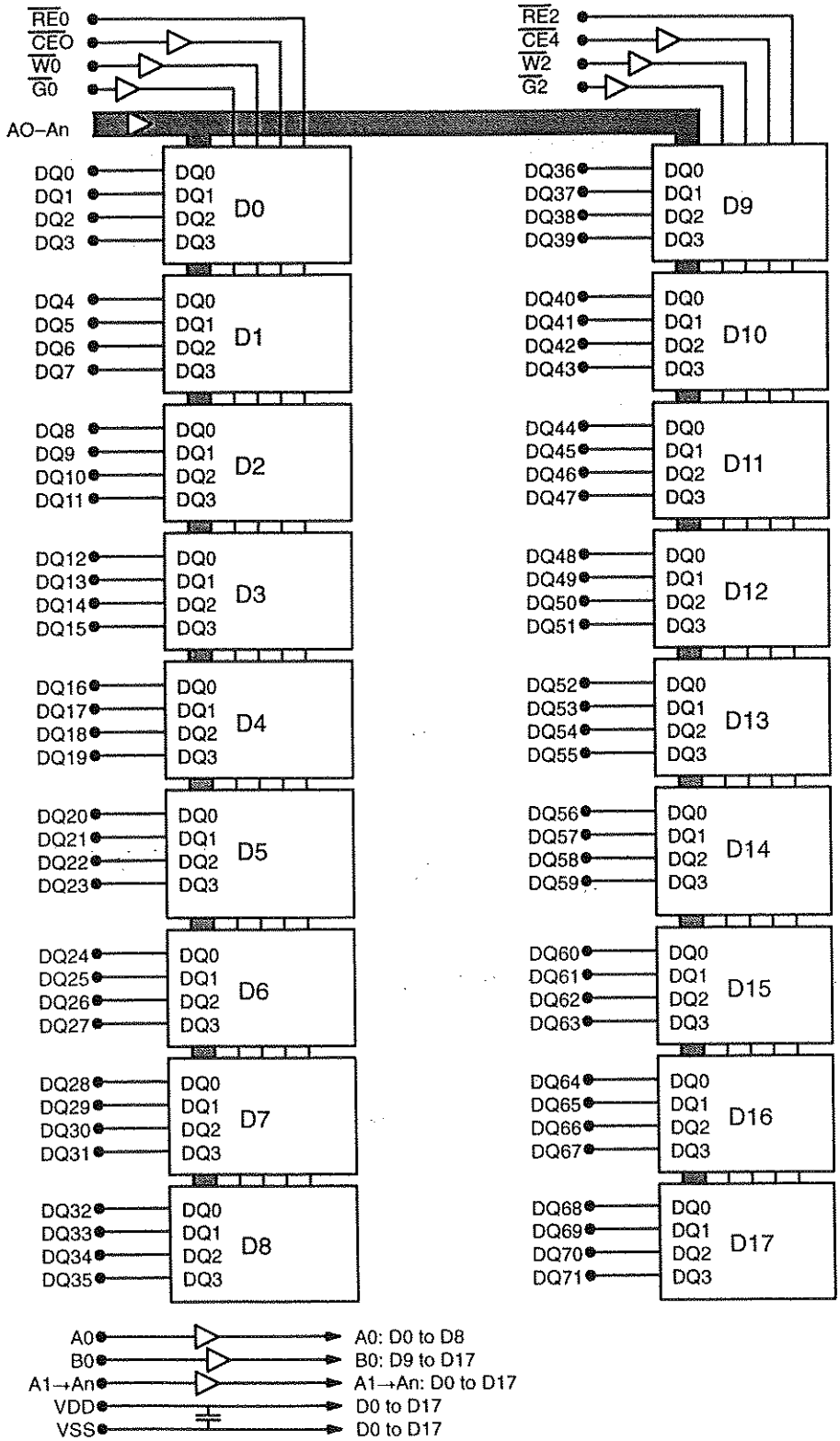
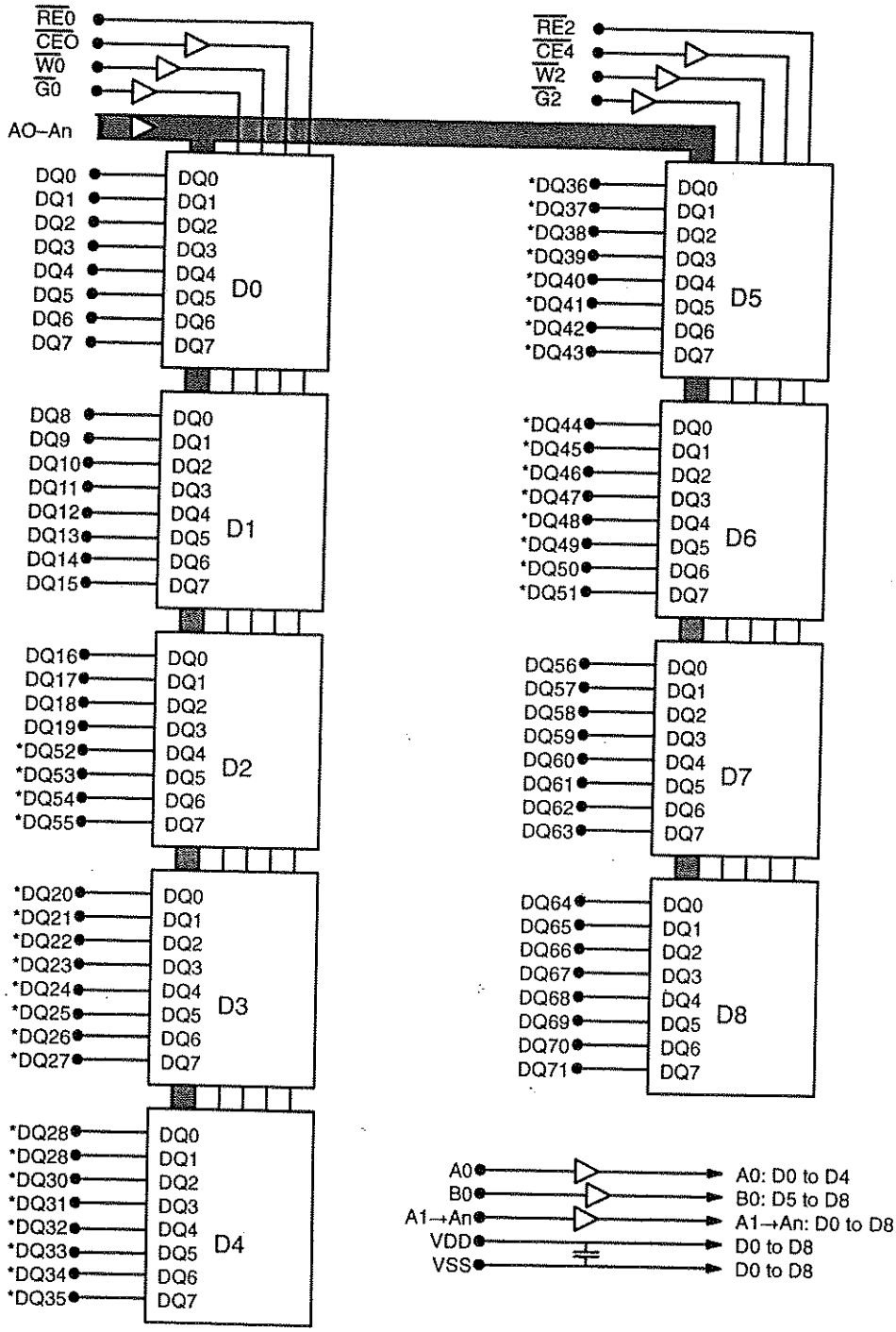


Figure 4.5.1–P
168 PIN, X 72 (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs
Release 4c7



* Note: The location of data pins DQ–20 through DQ–55 have been changed in Release 7

Figure 4.5.1–Q
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs

Release 4–r7

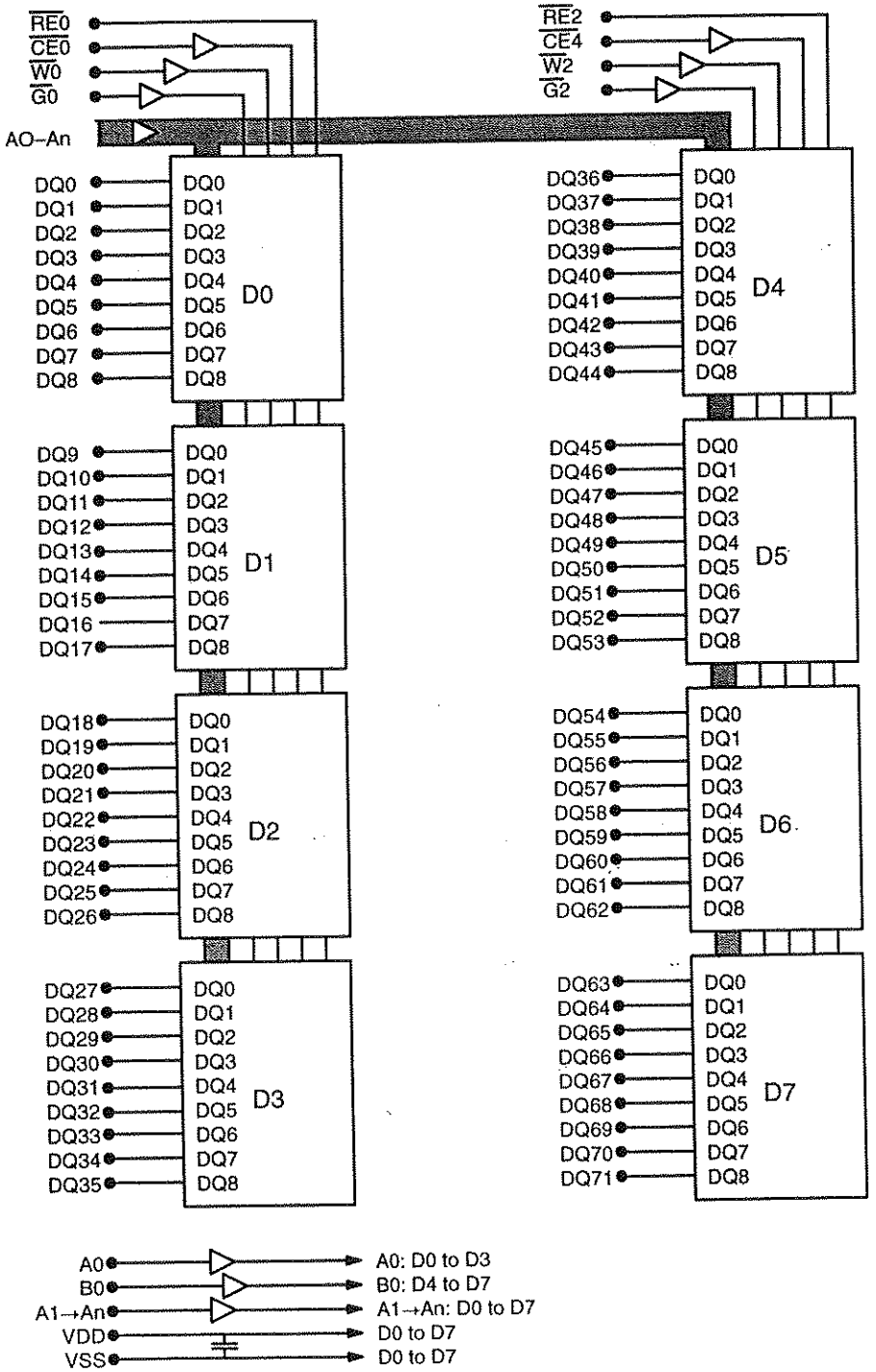


Figure 4.5.1–R
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X9 DRAMs

Release 4c7

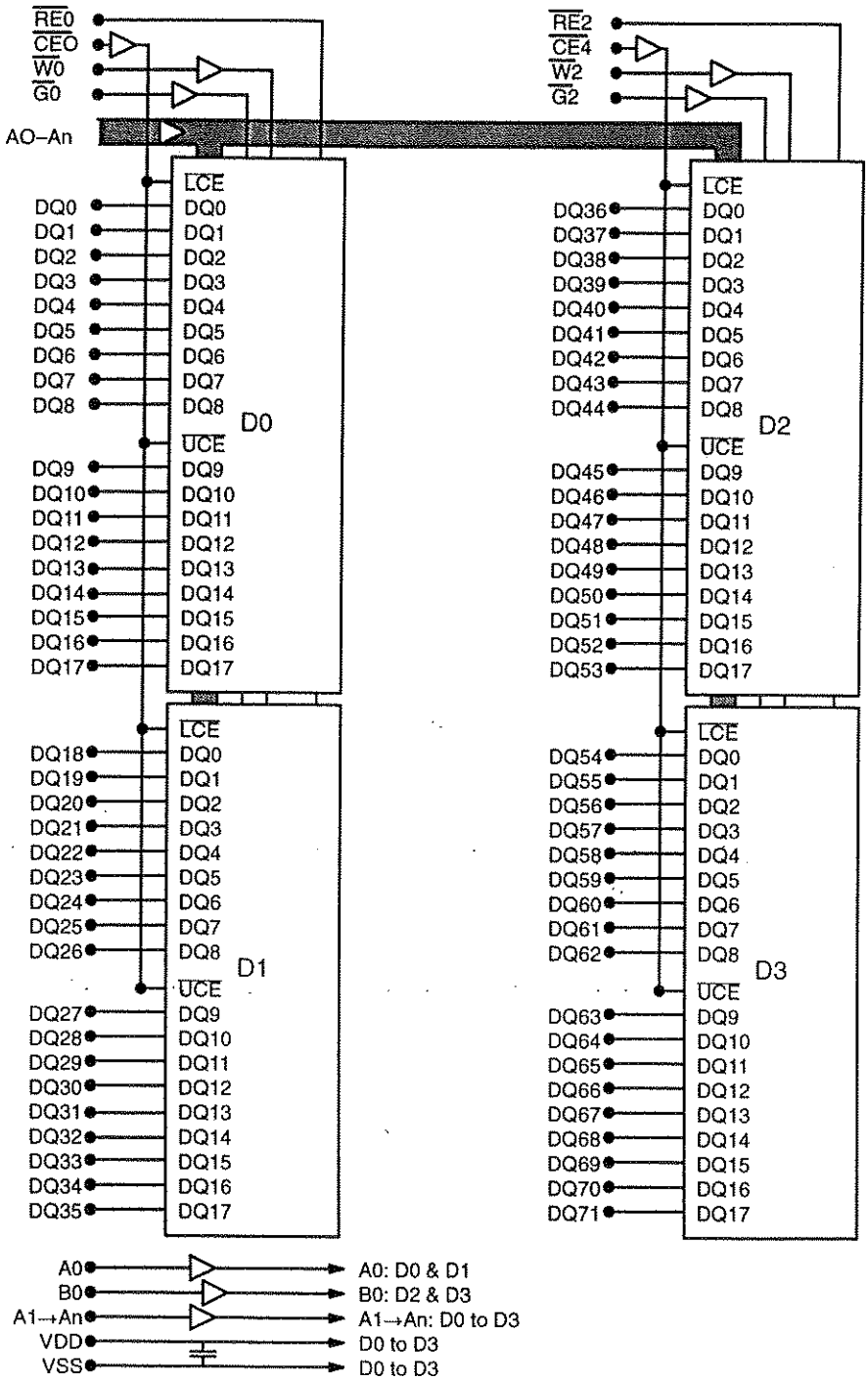


Figure 4.5.1–S
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X18 DRAMs

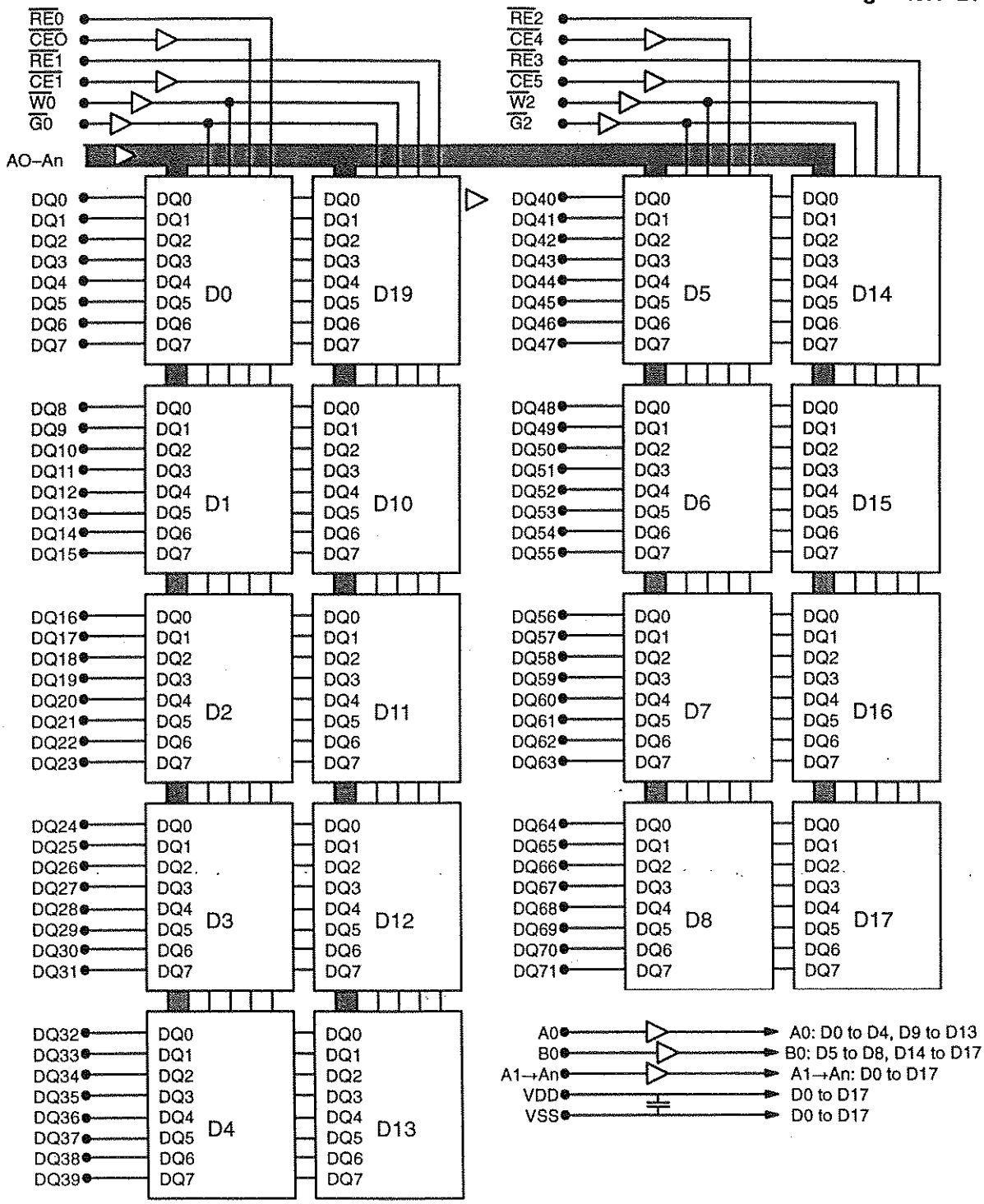


Figure 4.5.1–T
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

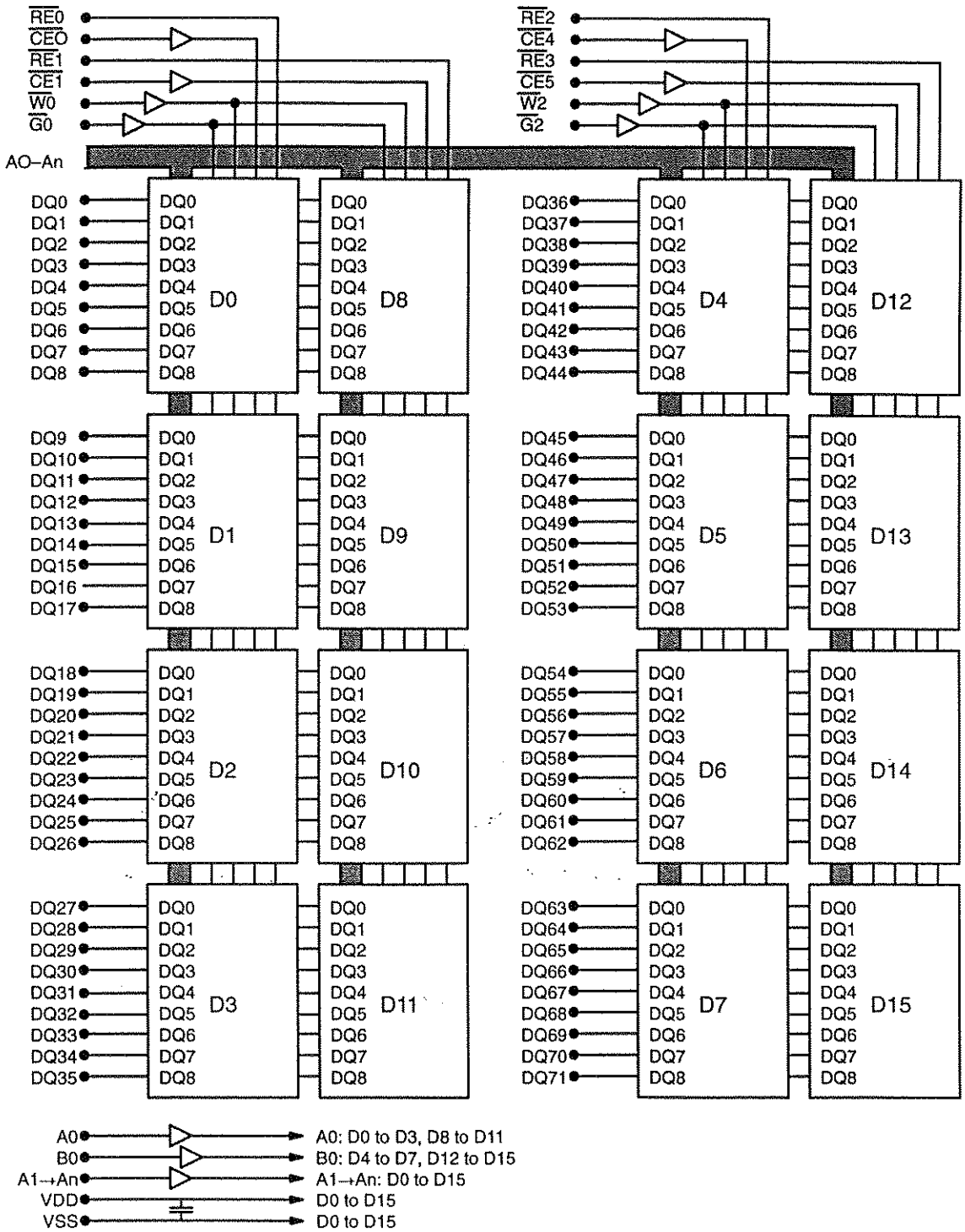


Figure 4.5.1–U
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X9 DRAMs
Release 4–7

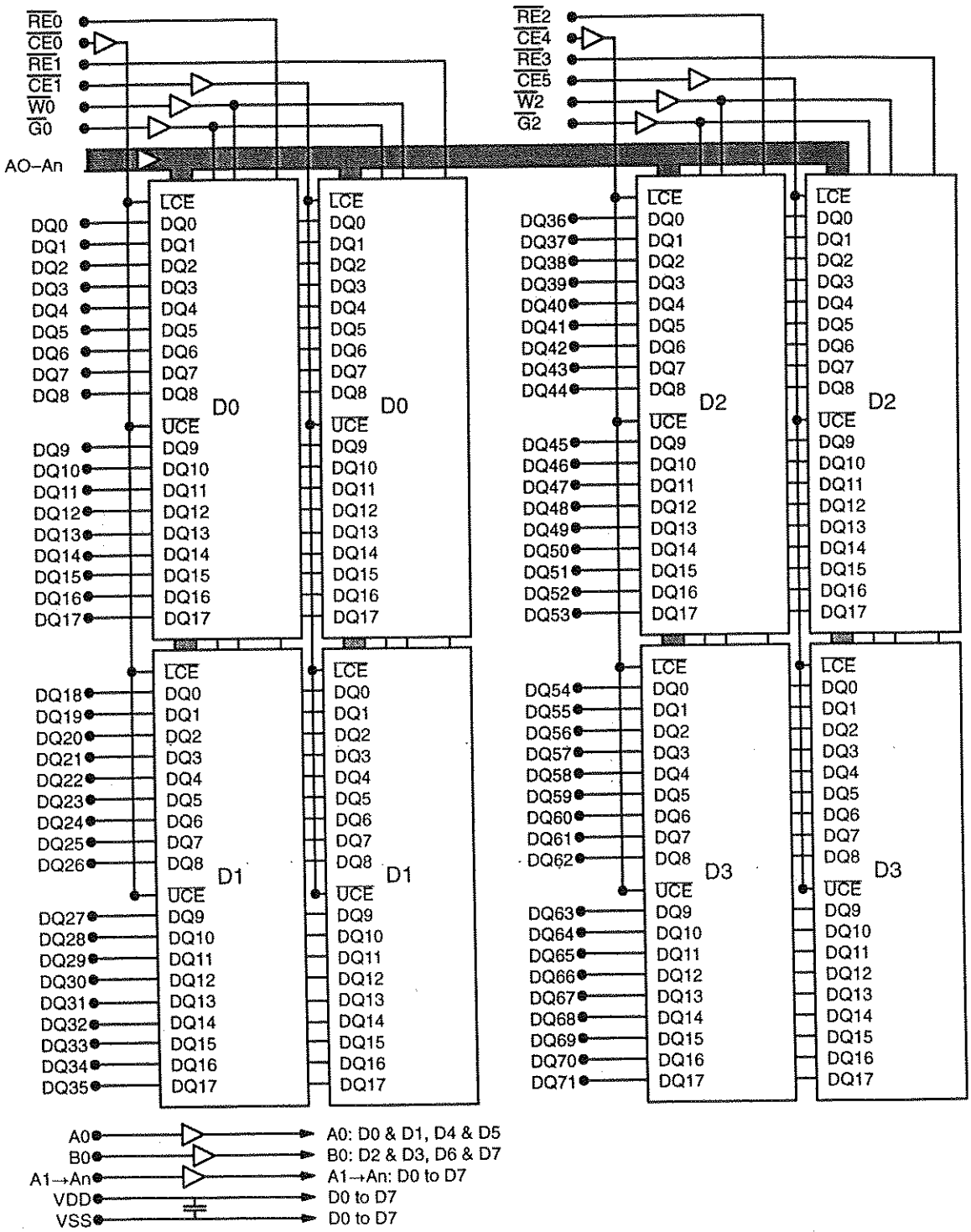


Figure 4.5.1–V
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X18 DRAMs

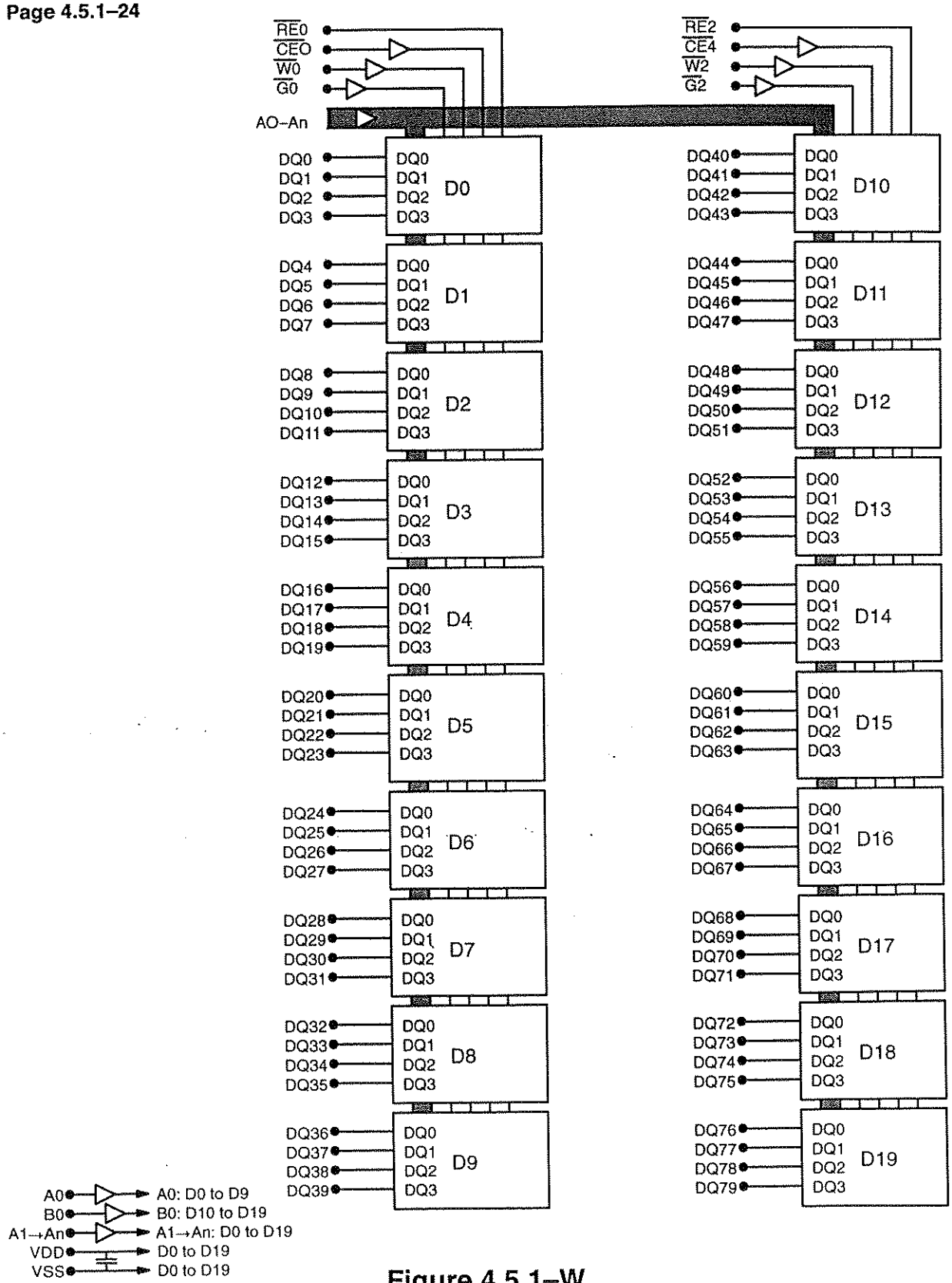


Figure 4.5.1–W
168 PIN, 80 BIT (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs

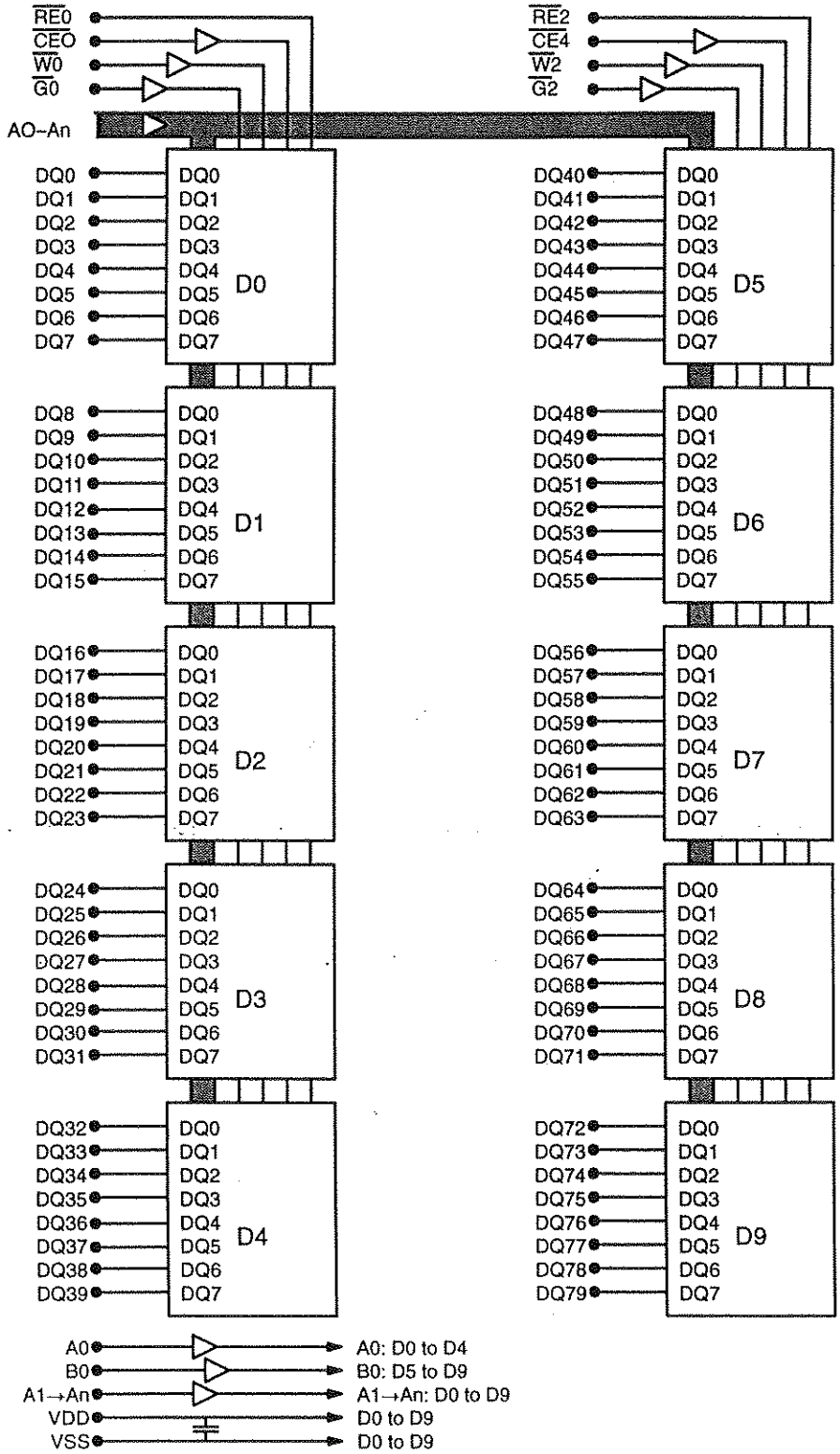


Figure 4.5.1–X
168 PIN, X80 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs

Release 4–7

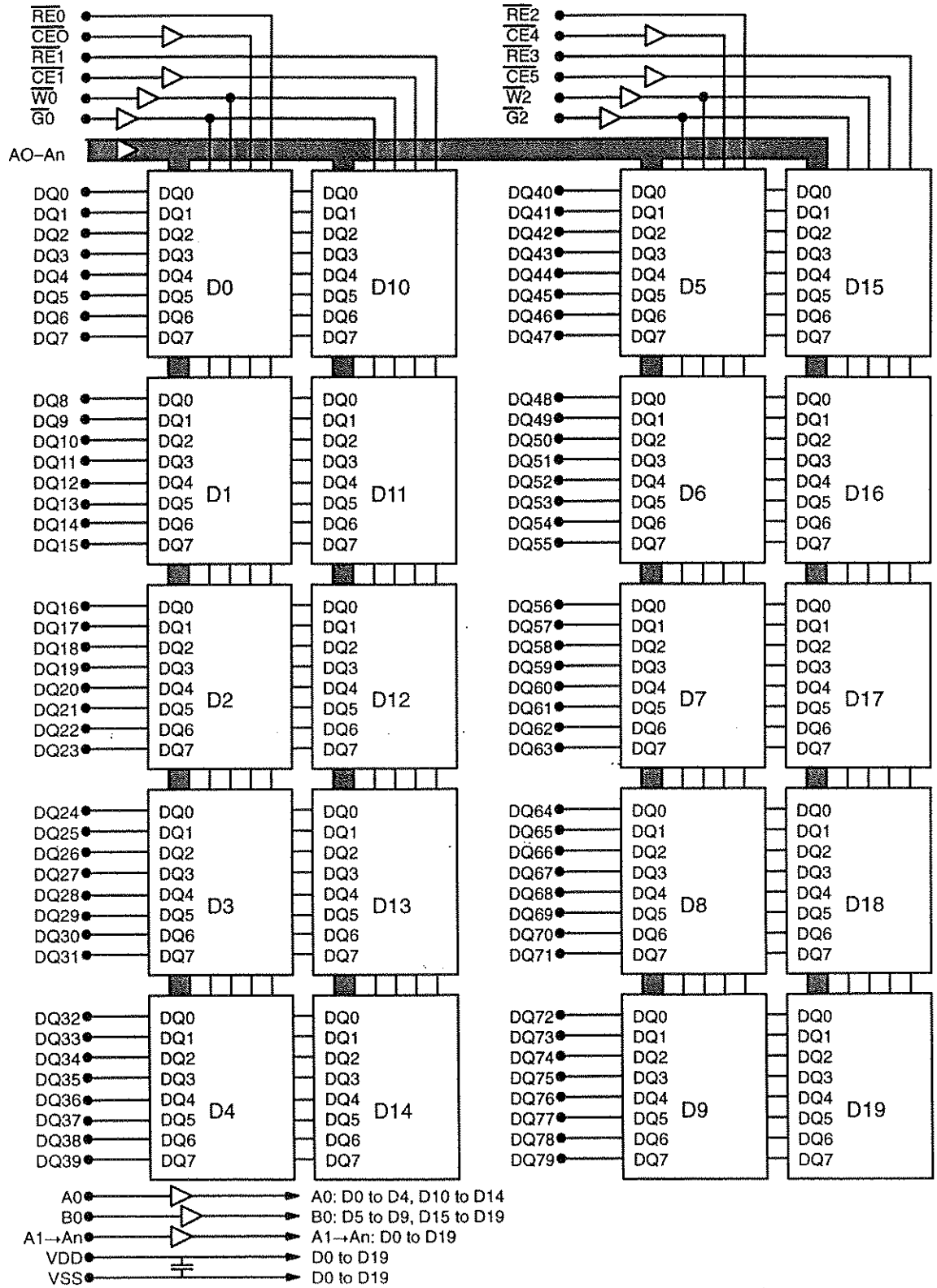


Figure 4.5.1–Y
168 PIN, X80 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

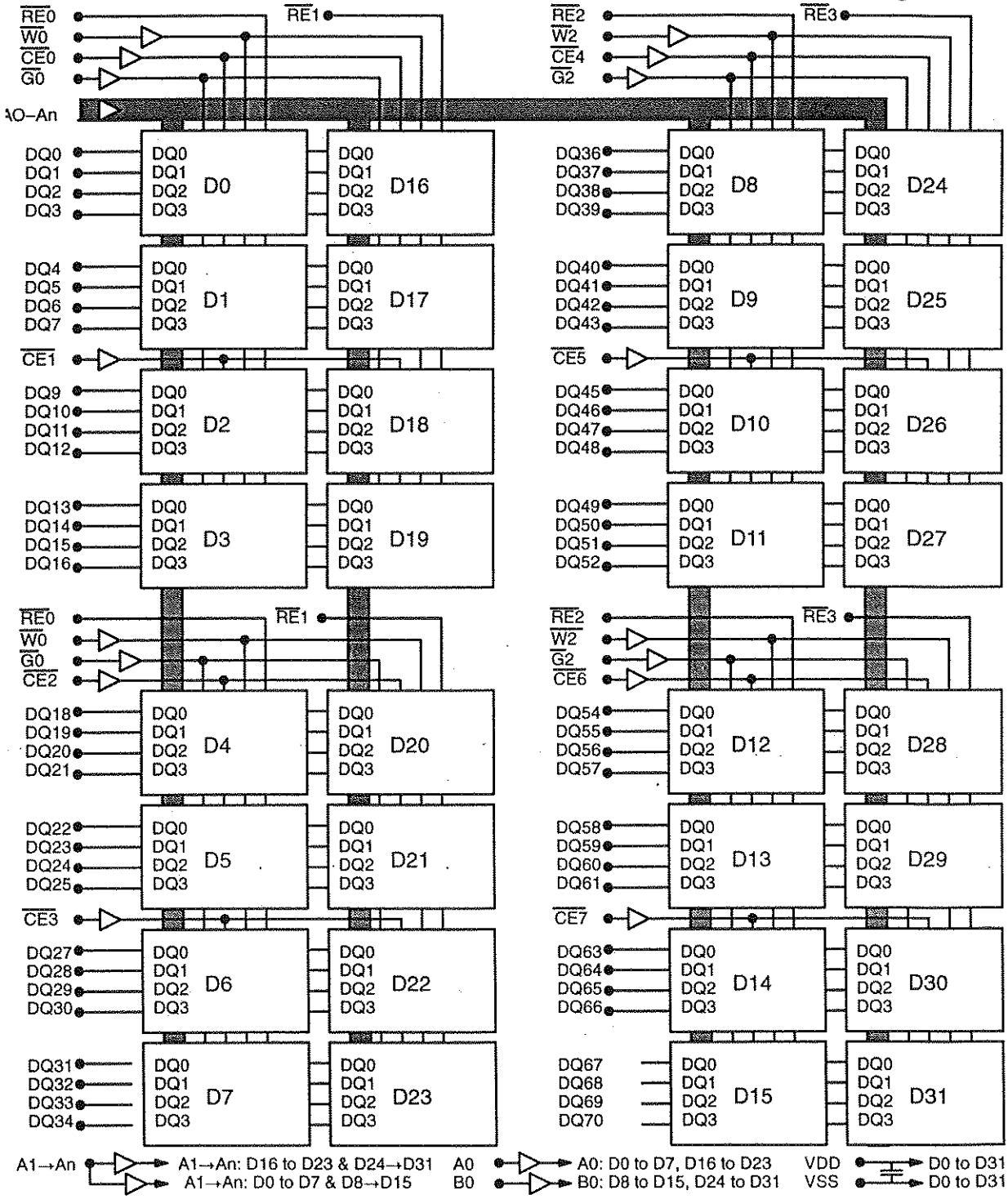


Figure 4.5.1–Z
168 PIN, X64 DRAM DIMM, 2 BANK with X4 DRAMs

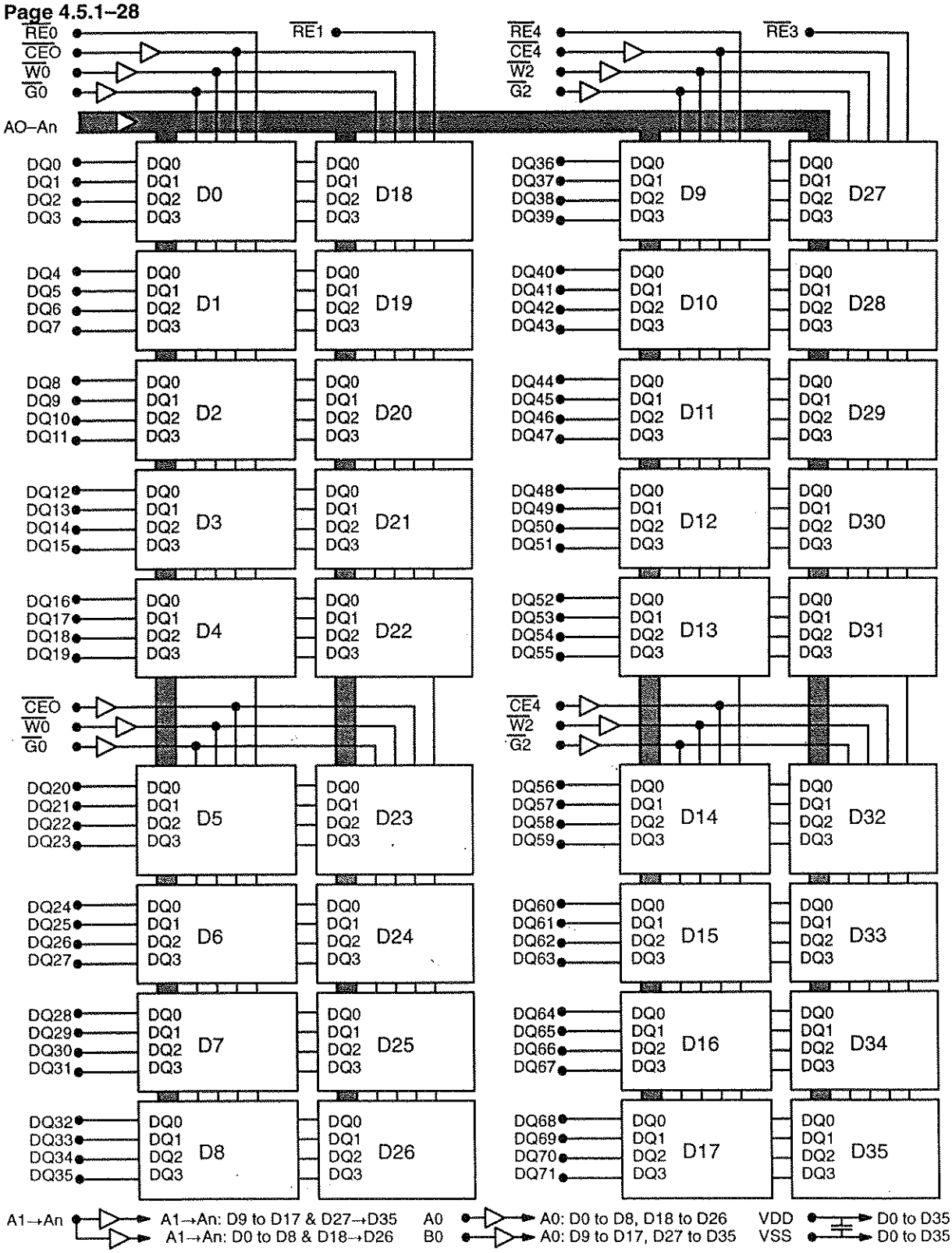


Figure 4.5.1–AA
168 PIN, X72 ECC DRAM DIMM, 2 BANK, X4 DRAMs
Release 6c7

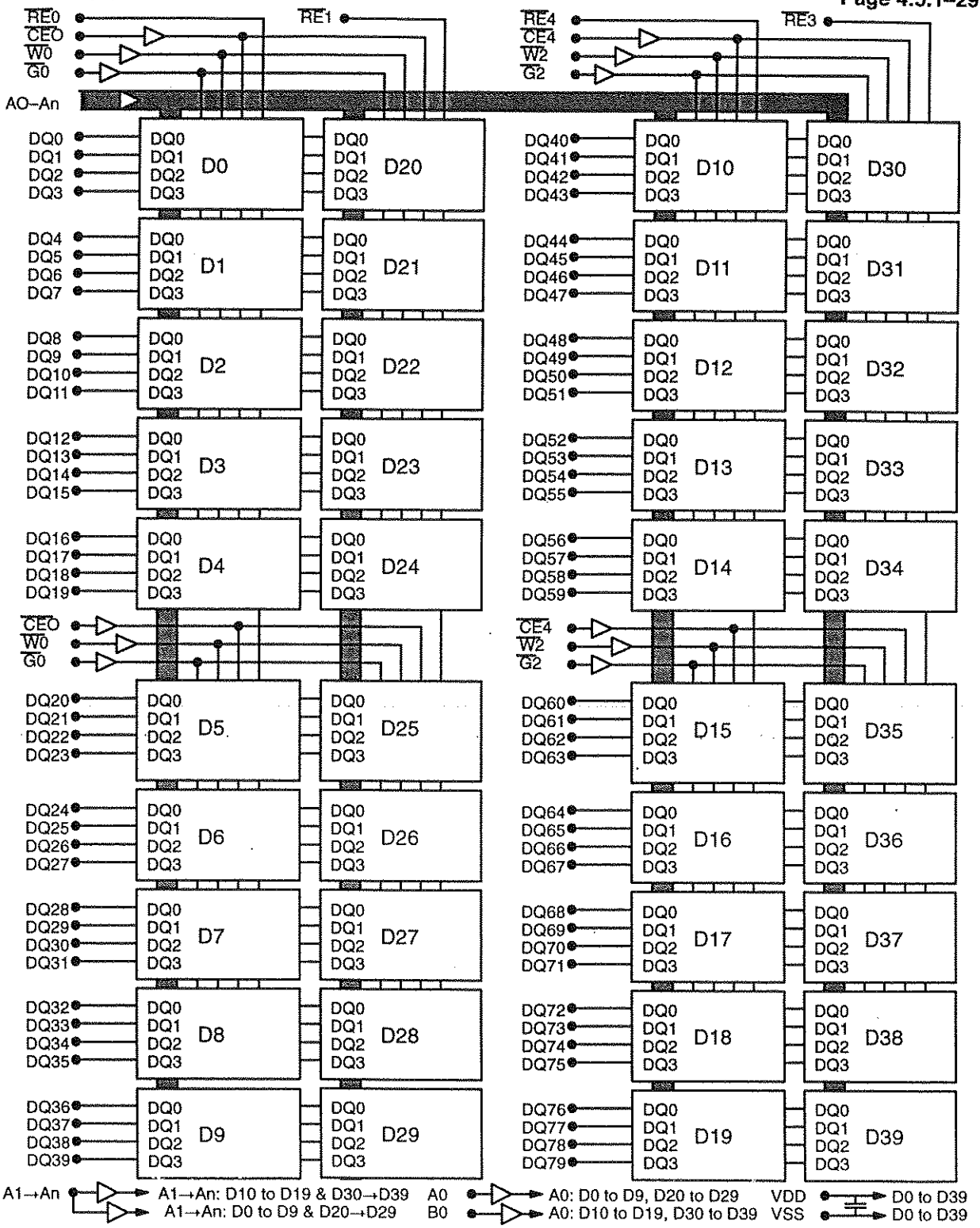


Figure 4.5.1–AB
168 PIN, X80 ECC DRAM DIMM, 2 BANK, X4 DRAMs

Release 6c7

4.5.2 – 200 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memory devices.

LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.2–A, 4.5.2–B, & 4.5.2–C

MECHANICAL KEY DEFINITION—Fig. 4.5.2–D

PIN DEFINITIONS—Fig. 4.5.2–E

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.2–F through 4.5.2–M

XILINX EXHIBIT 1010
Page 346

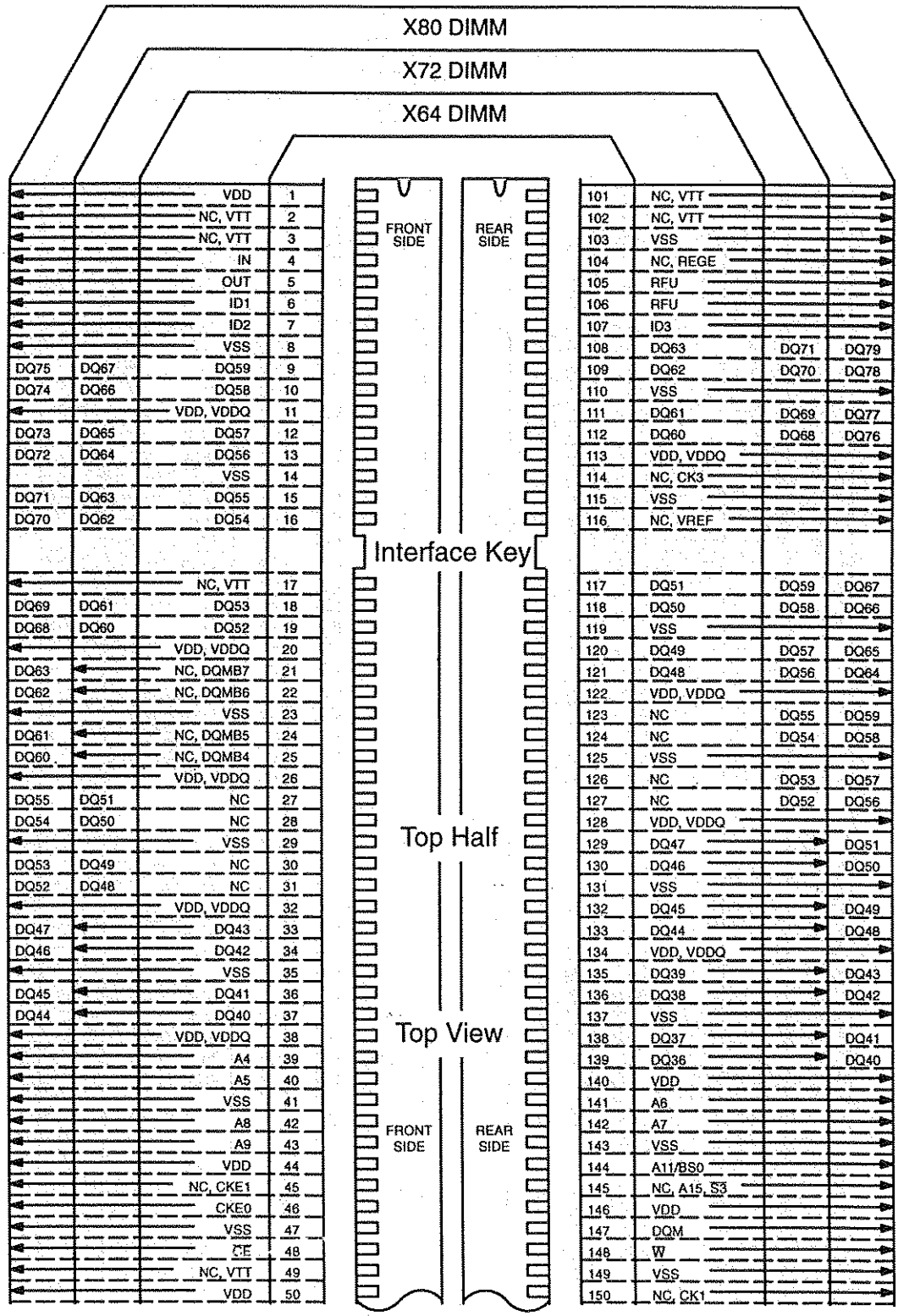


Figure 4.5.2–A
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

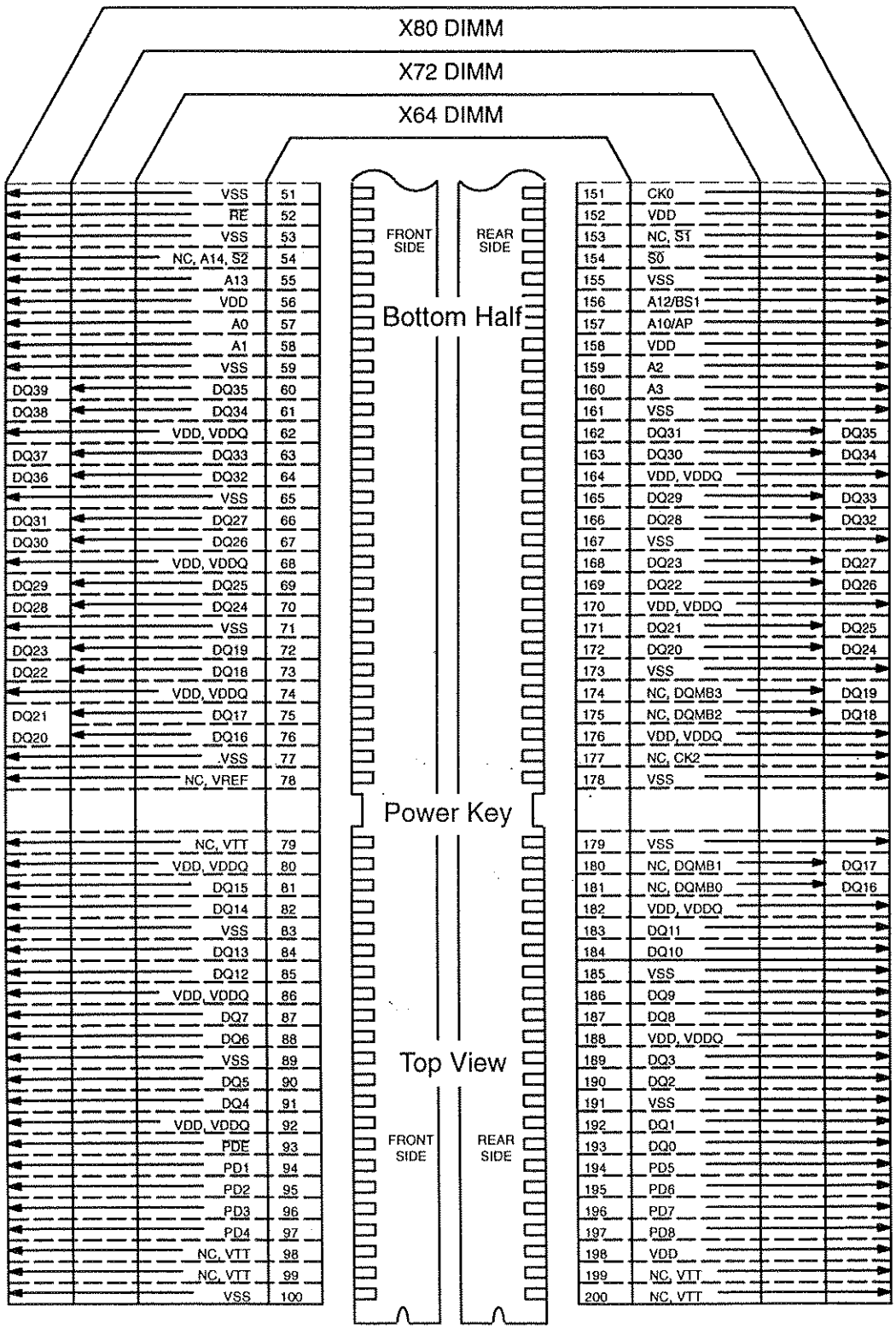


Figure 4.5.2–B
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

Release 6–7

PD BITS 4 3 2 1	MODULE CONFIGURATION	SDRAM ORGANIZATION	RE ADDR.	CE ADDR
1 1 1 1	NO MODULE			
1 0 0 0 0 0 0 0	1M X 64/72/80 2M X 64/72/80	1M X 16 1M X 16	12 12	8 8
1 0 0 1 0 0 0 1	2M X 64/72/80 4M X 64/72/80	2M X 8 2M X 8	12 12	9 9
1 0 1 0 0 0 1 0	4M X 64/72/80 8M X 64/72/80	4M X 4/16 4M X 4/16	12 12	10 10
1 0 1 1 0 0 1 1	8M X 64/72/80 16M X 64/72/80	8M X 8 8M X 8	TBD TBD	TBD TBD
1 1 0 0 0 1 0 0	16M X 64/72/80 32M X 64/72/80	16M X 4 16M X 4	TBD TBD	TBD TBD
1 1 0 1 0 1 0 1	RFU RFU	TBD TBD	TBD TBD	TBD TBD
1 1 1 0 0 1 1 0	RFU RFU	TBD TBD	TBD TBD	TBD TBD
0 1 1 1	Expansion			

Note 1 Presence Detect pins PD1—PD8 are buffered and enabled by $\overline{PDE}$. The "1" outputs are NC and the "0" outputs are driven low by on–module drivers when $\overline{PDE}$ is asserted active low.

Note 2 Buffered DIMMs (PD7=1) with PD8=0 (Byte–Write) shall be capable of both Word–Write and Byte–Write operations

	PD6	PD5
SPEED (tCYC)	195	194
15 ns	1	1
12 ns	1	0
10 ns	0	1
8 ns	0	0
PD SPEED TABLE		

	PD7
INTERFACE	196
UNBUFFERED	0
BUFFERED	1
MODULE INTERFACE	

	PD8
WRITE MODE	197
BYTE	0
WORD	1
WRITE MODE DETECT	

	ID3
POWER	107
NORMAL	0
LOW–POWER	1
POWER LEVEL DETECT	

	ID2
RAS TIMING	7
NO EARLY RAS	0
EARLY RAS	1
READ PRECHARGE TIMING	

	ID1
INTERVAL	6
2 CLOCKS	0
1 CLOCK	1
COMMAND INTERVAL	

Figure 4.5.2–C

200 PIN, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES

Release 5–7

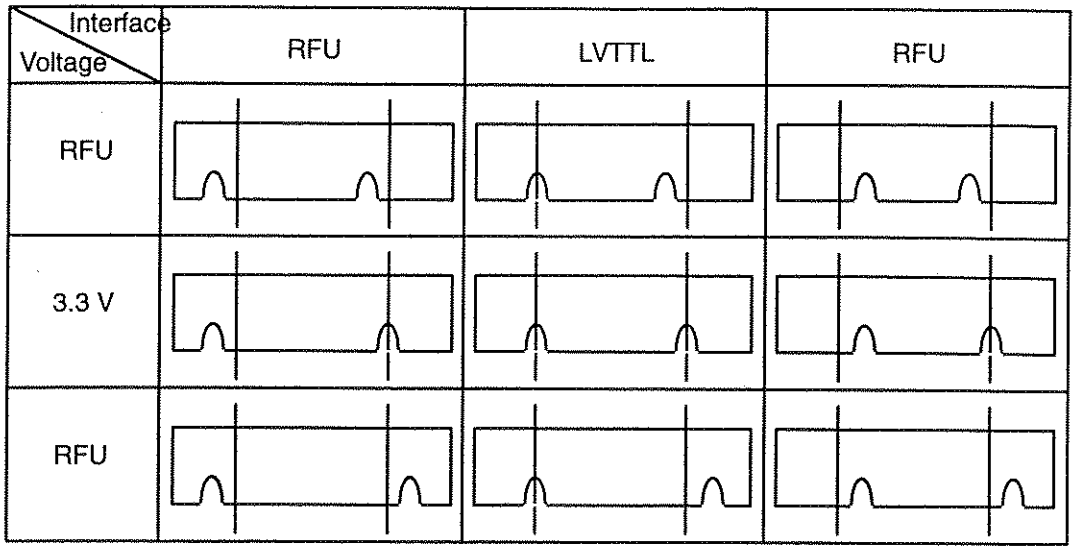


Figure 4.5.2–D

200 PIN, 8 BYTE SDRAM DIMM MECHANICAL KEY DEFINITION

Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ79	80	Data Input/Output (common)
CK0....CK3	4	Clock Input
CKE0....CKE1	2	Clock Enable Input
$\overline{S0}$....$\overline{S3}$	4	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB7	8	Byte Data Mask
REGE	1	Buffer/Register Enable
$\overline{PDE}$	1	Presence Detect Enable
PD1....PD8	8	Buffered Logic Presence Detect Output
ID1....ID3	3	Identification Output
IN, OUT	2	Unbuffered Physical Detect Input/Output
VDD	9	Primary Positive Power Supply
VDDQ	20	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	33	Ground
VTT	11	Termination Power Supply
RFU	2	Reserved for Future Use

Notes:

1. Pin A14 is shared with S2, and pin A15 is shared with pin S3.
2 Pins DQMB0...DQMB7 are shared with pins defined as NC for X64 and X72 configurations.
3 REGE (Register Enable) operates similarly to the SAB pin on the 74AC11652 "Octal Bus Transceiver and Register with 3–State Outputs". When it is asserted, active high, the buffer–register operates in Register mode, as opposed to when it is de–asserted, inactive low, the buffer –register operates in "real–time" buffer mode.
4. The unbuffered physical detect pins IN and OUT are shorted together on the DIMM.

Figure 4.5.2–E

8 BYTE SDRAM DIMM PIN DEFINITIONS

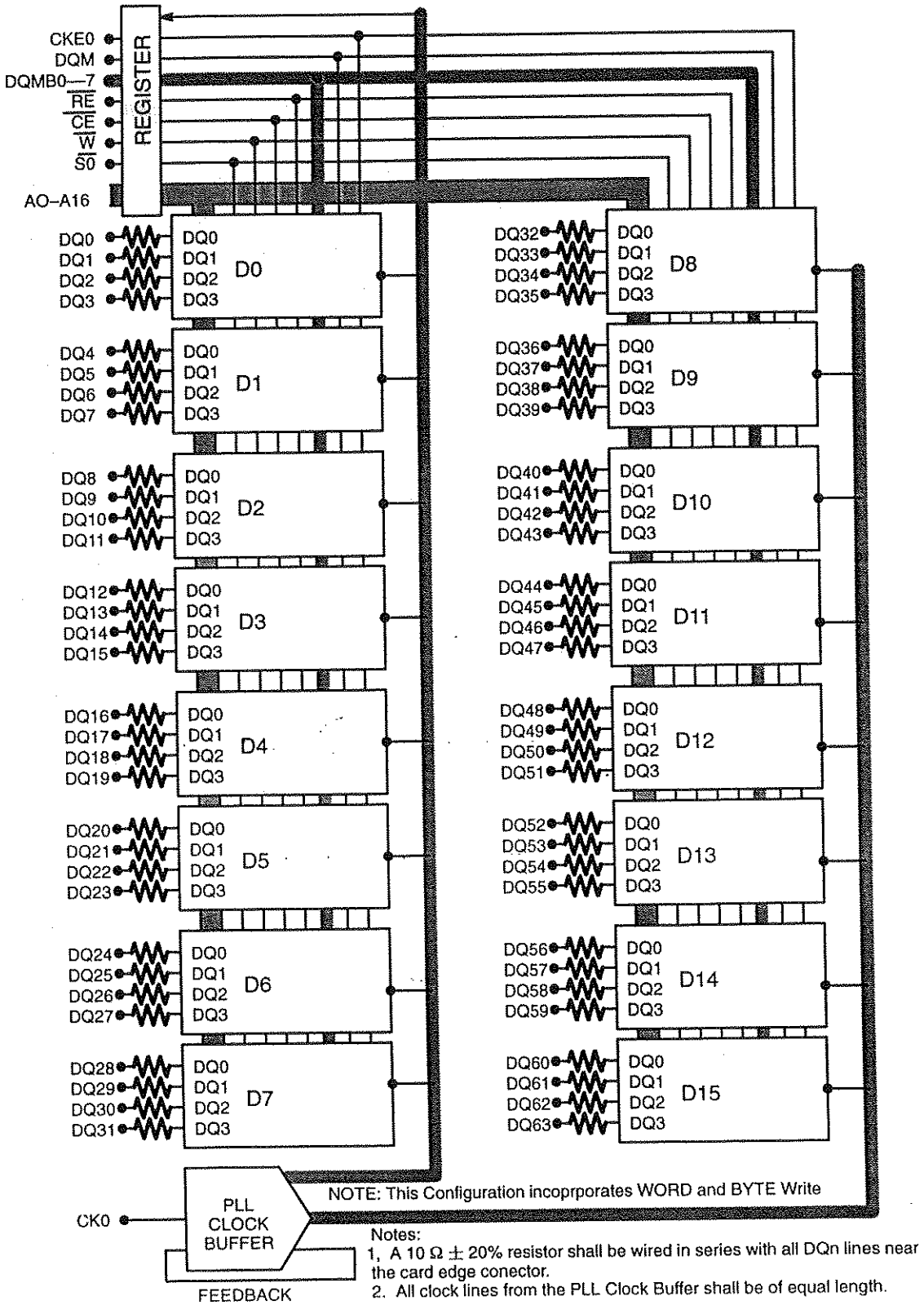


Figure 4.5.2–F

200 PIN, X64 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

XILINX EXHIBIT 1010
Page 351

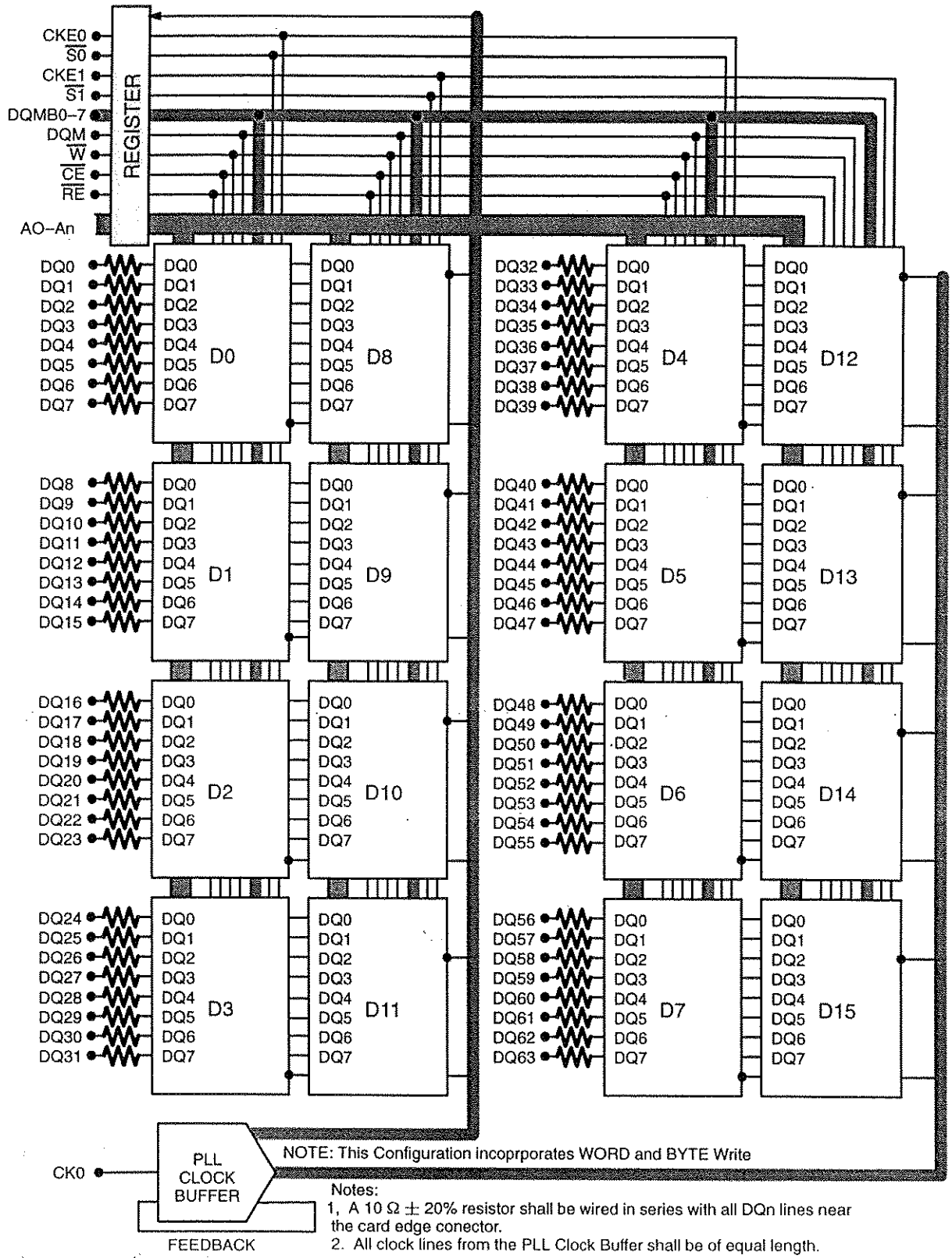


Figure 4.5.2–G

200 PIN, X64 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

Release 5–7

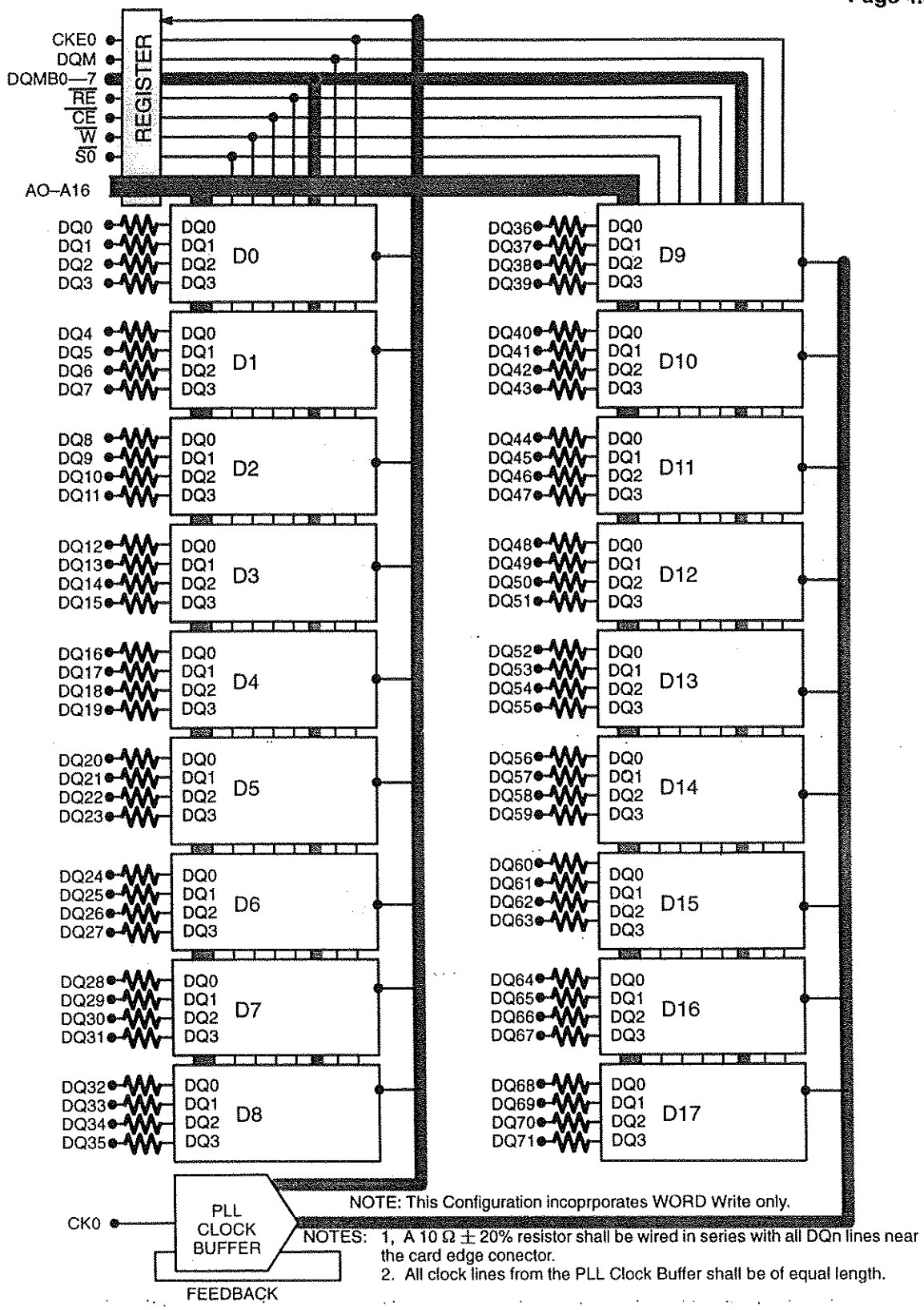
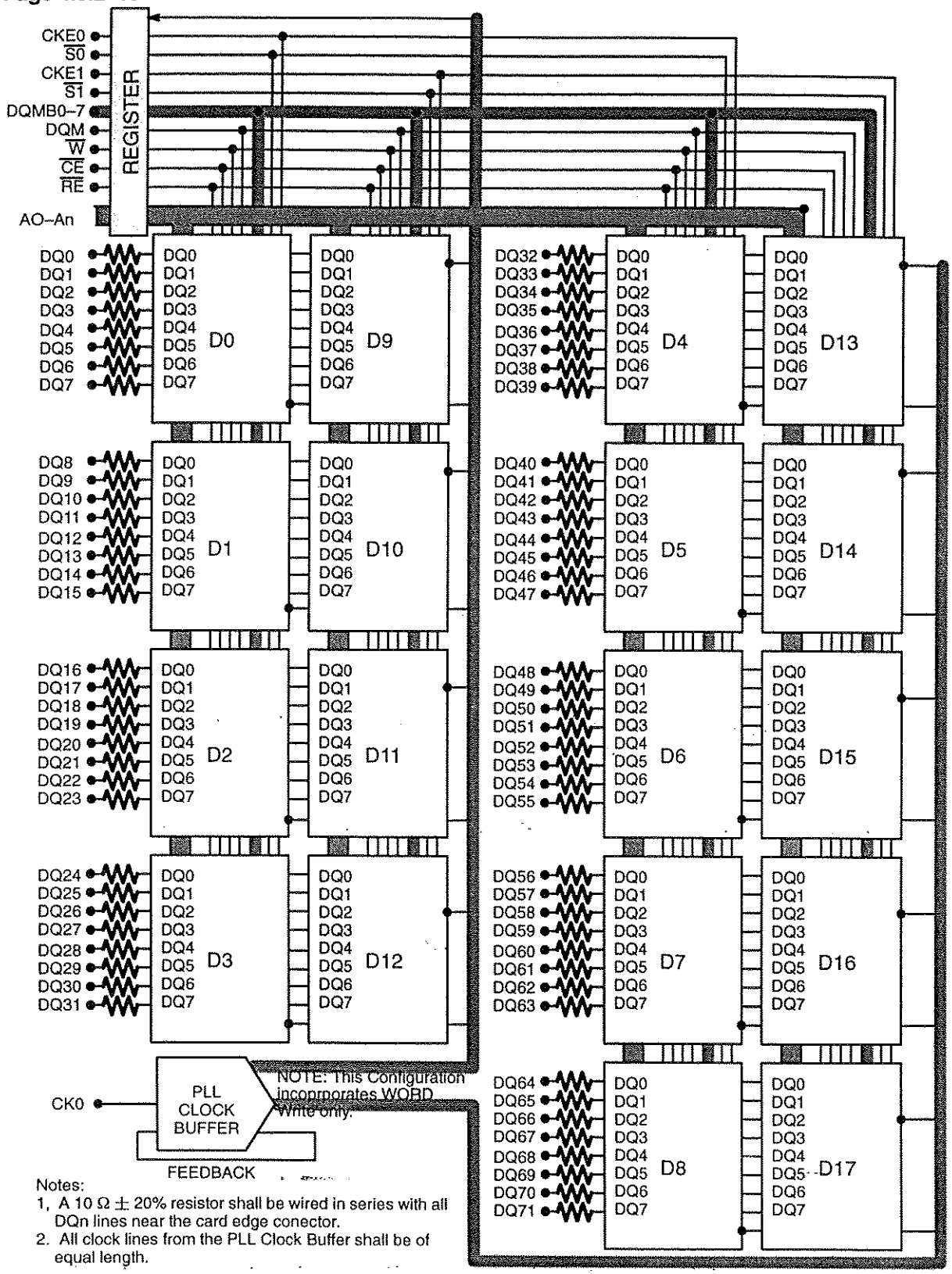


Figure 4.5.2–H

200 PIN, X72 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs



Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–I

200 PIN, X72 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

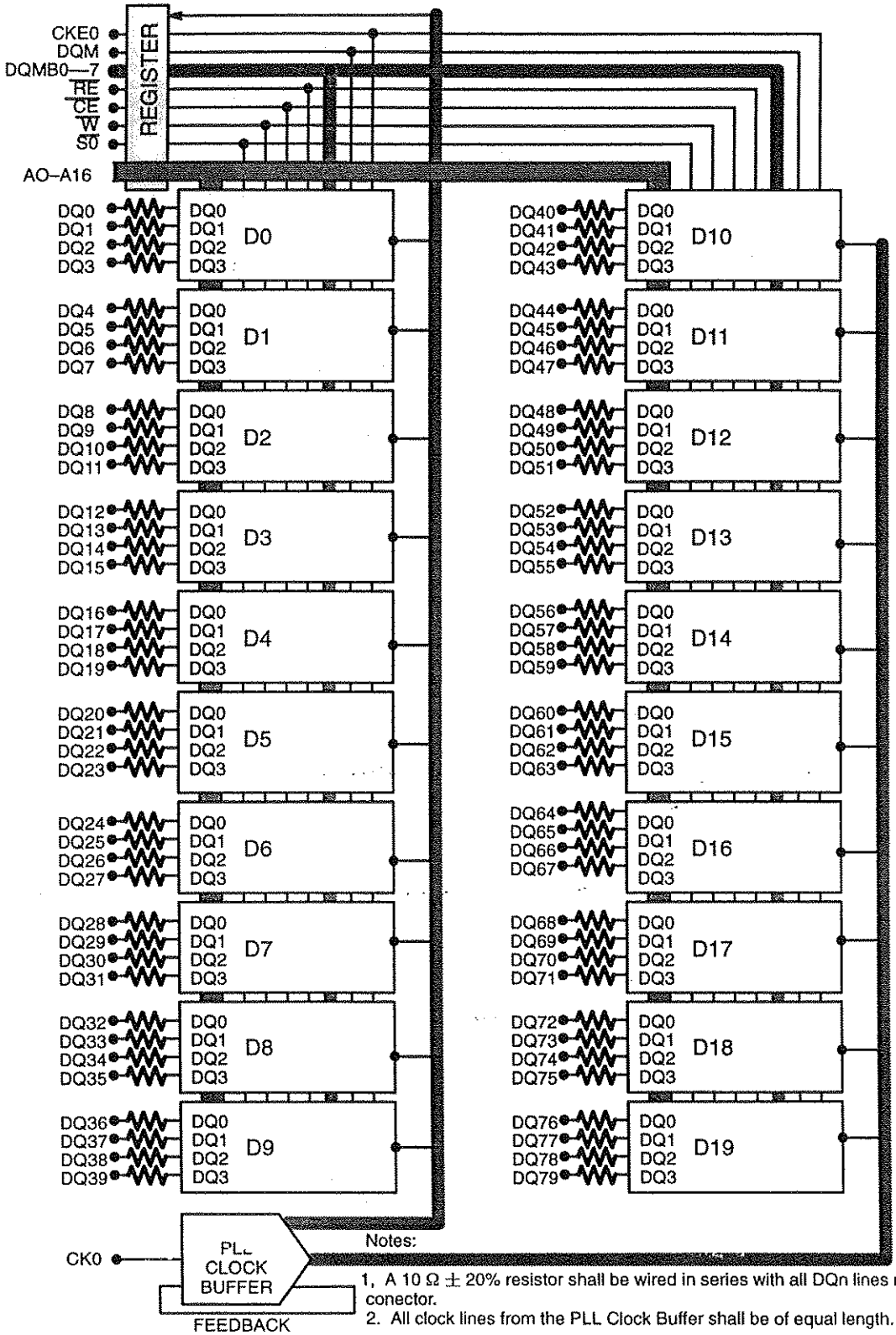
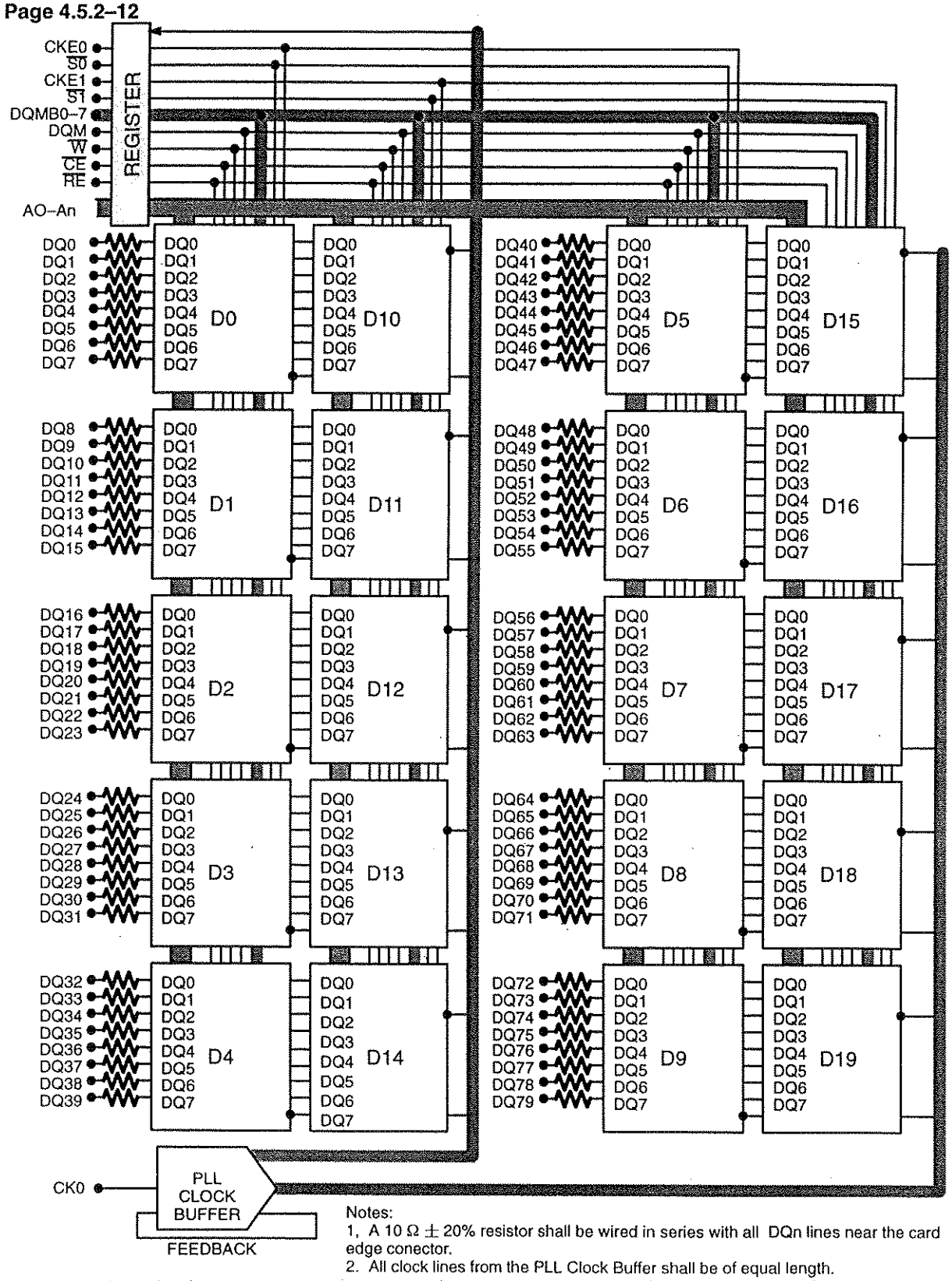


Figure 4.5.2–J

200 PIN, X80 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

Release 5–7

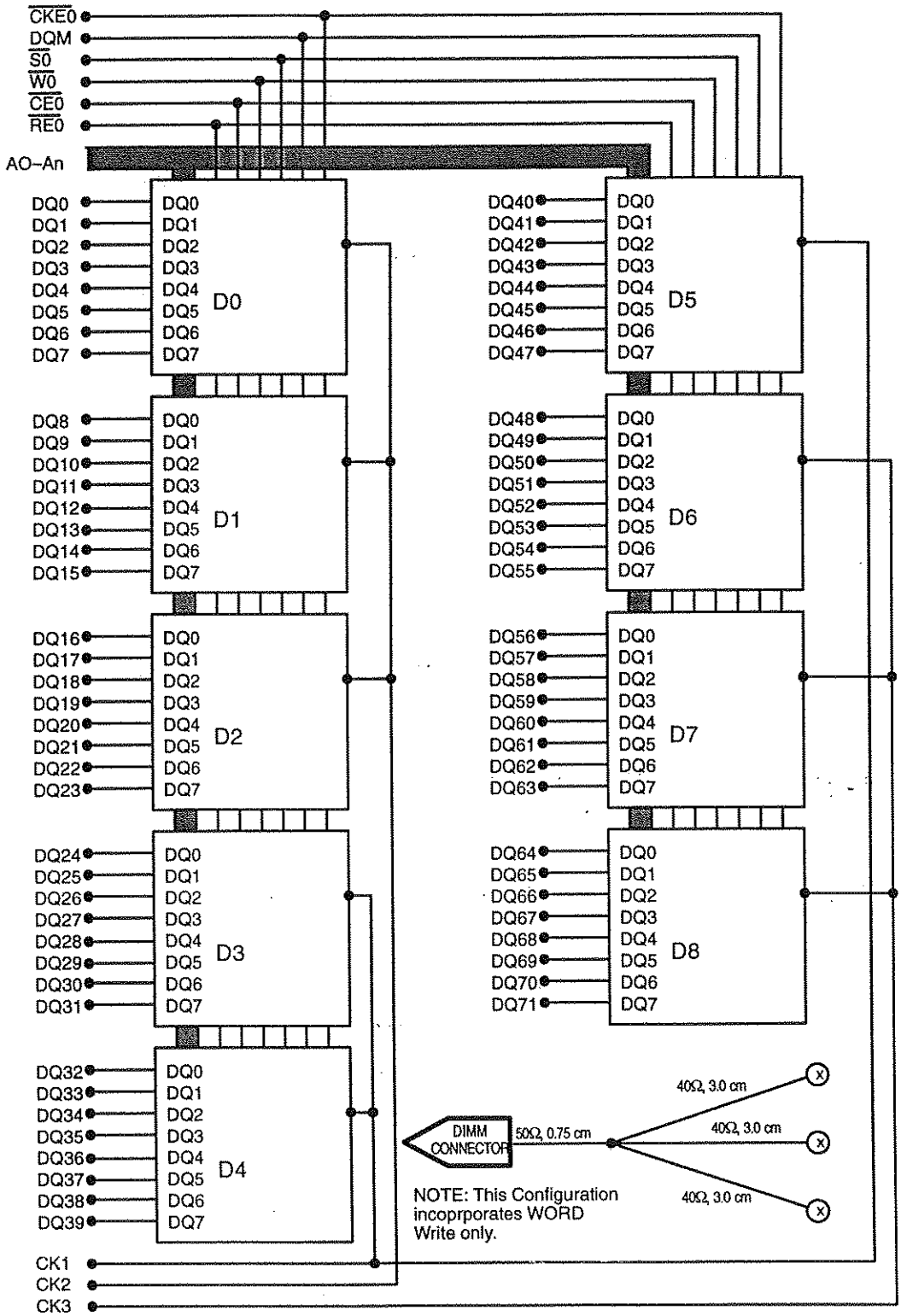


Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–K

200 PIN, X80 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

Release 5–7



Note: All clock trees shall be routed as equal–length "stars" from CK1, CK2, & CK3 inputs as shown in the diagram above.

Figure 4.5.2–L

200 PIN, X72 UNBUFFERED SDRAM DIMM, 1 bank with X8 DRAMs

Release 5–7

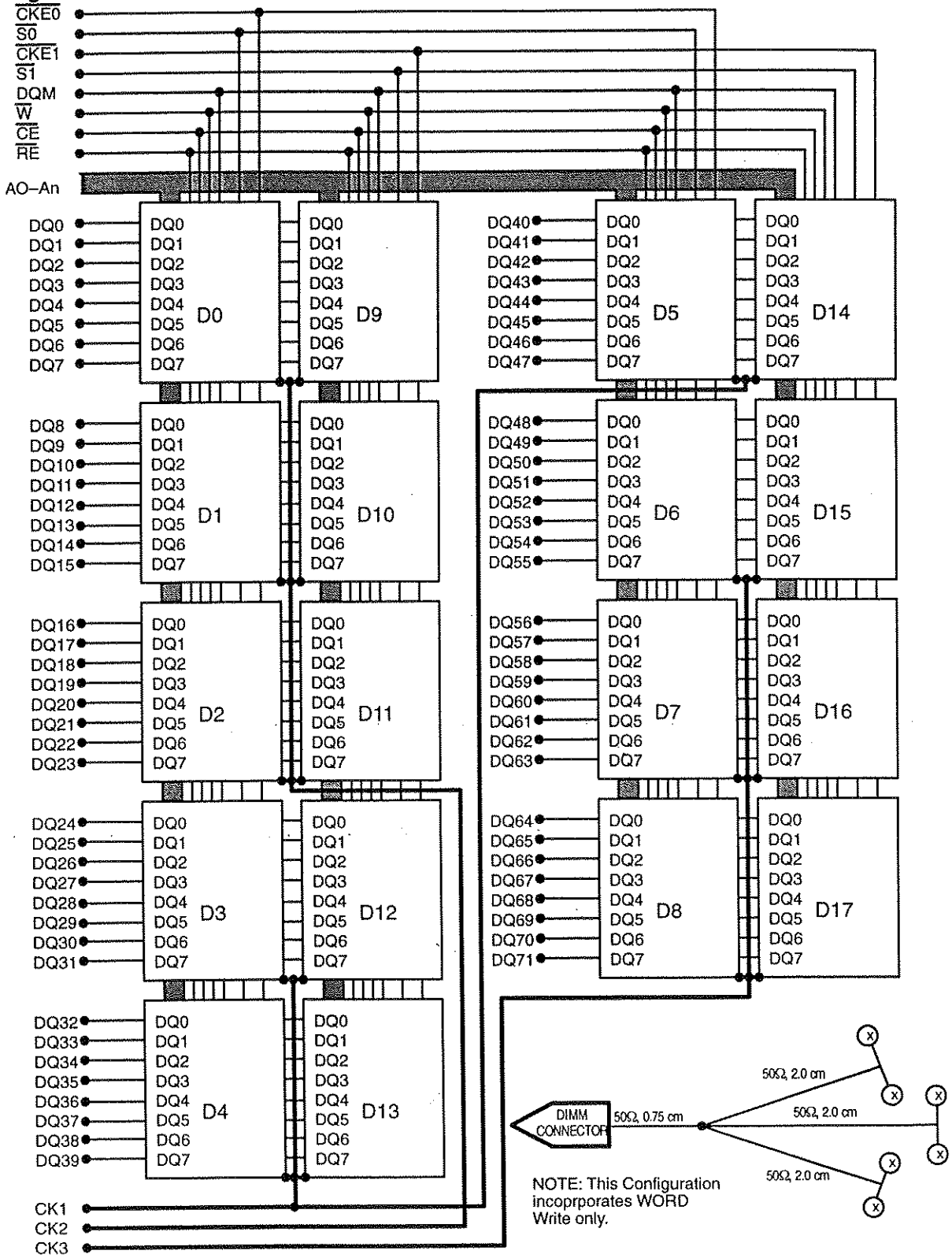


Figure 4.5.2–M

200 PIN, X72 UNBUFFERED SDRAM DIMM, 2 banks with X8 DRAMs

Release 5–7

4.5.3 – 168 PIN UNBUFFERED DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—13 Different Configurations are defined using various combinationa of X1, X4, X8, X16 and X18 memories.

LOGIC FEATURES—The modules contain "SERIAL PRESENCE DETECT" features using EEPROM stored information that profided a variety of encoded information regarding the module such as storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
—Check Bit locations are pre–assigned

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS—Figs. 4.5.3–A, & 4.5.3–B

SPD TABLES—Figs. 4.5.3–C

KEYING METHODOLOGY—Fig. 4.5.3–D

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.3–E through 4.5.3–S

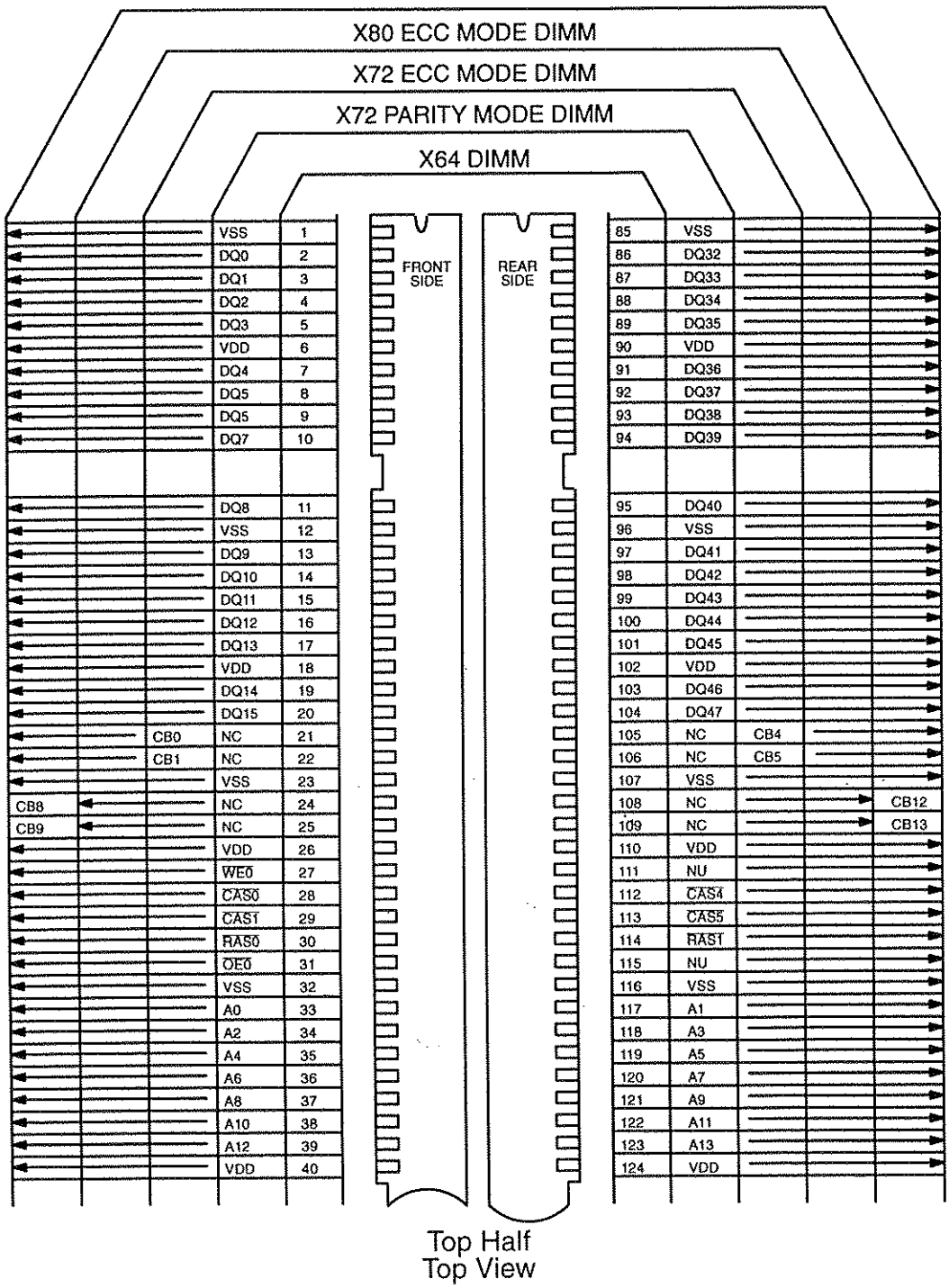


FIGURE 4.5.3–A
64, 72, or 80 BIT DIMM PINOUT, TOP HALF

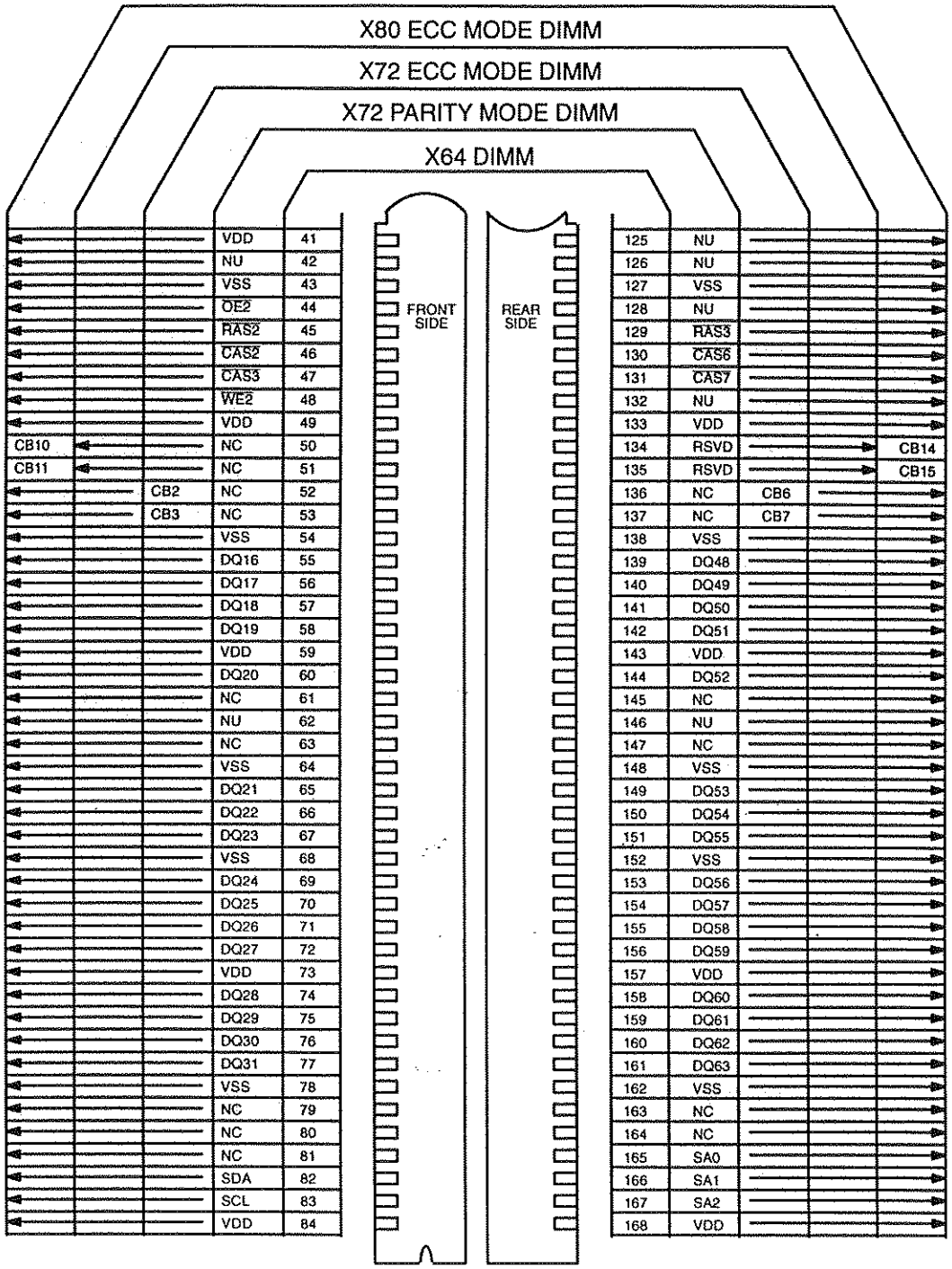
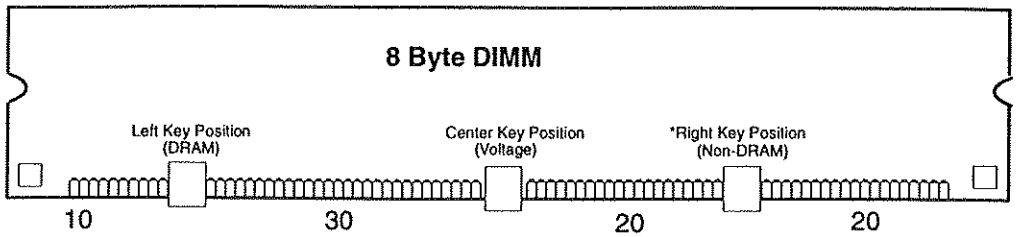


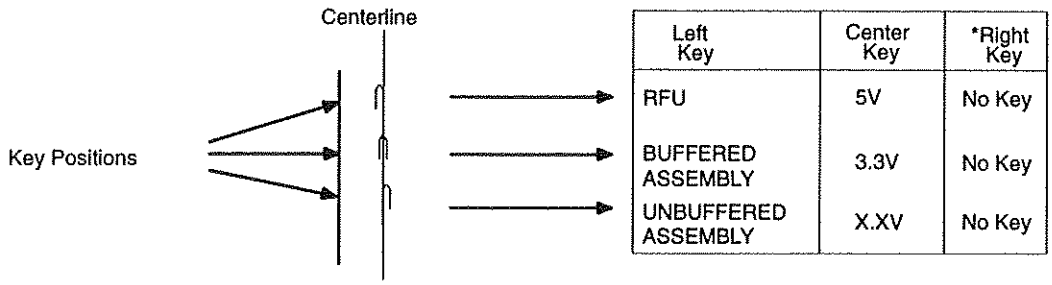
FIGURE 4.5.3–B
64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins V_{CC} - 16 V_{SS} - 16	35 Power/Gnd Pins V_{CC} - 17 (1 additional pin) V_{SS} - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

FIGURE 4.5.3–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM

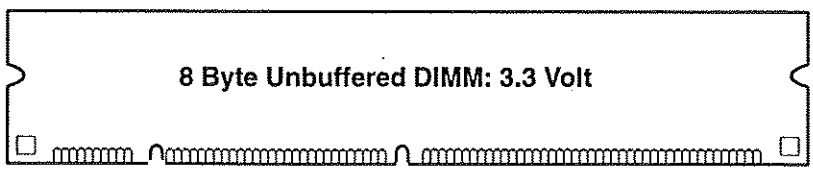
XILINX EXHIBIT 1010
Page 362





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.



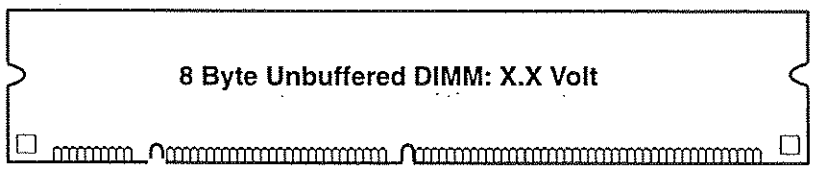


FIGURE 4.5.3–D
168 Pin DRAM DIMM Keying Methodology

31	$\overline{OE0}$	DU
42	DU	CK0
44	$\overline{OE2}$	DU
45	$\overline{RAS2}$	$\overline{S2}$
46	$\overline{CAS2}$	DQMB2
47	$\overline{CAS3}$	DQMB3
48	$\overline{WE2}$	DU
62	DU	V_{REF} (IF APPLICABLE)
111	DU	$\overline{CAS}$
112	$\overline{CAS4}$	DQMB4
113	$\overline{CAS5}$	DQMB5
114	$\overline{RAS1}$	$\overline{S1}$
115	DU	$\overline{RAS}$
125	DU	CK1
126	DU	A14
128	DU	CKE
129	$\overline{RAS3}$	$\overline{S3}$
130	$\overline{CAS6}$	DQMB6
131	$\overline{CAS7}$	DQMB7
132	DU	A15
146	DU	V_{REF} (IF APPLICABLE)

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A11 on DRAM DIMM is also BS0 on SDRAM DIMM
3. A12 on DRAM DIMM is also BS1 on SDRAM DIMM (for 4 Bank SDRAMs)

FIGURE 4.5.3–E
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

8 Byte Presence Detect Information

- Serial PD Interface Protocol: IIC (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:

a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
256K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	512K x 8	10	9				
1M x 64/72/80	512K x 8	10	9				
1M x 64/72/80	1M x 4/16	10	10	12	8		
2M x 64/72/80	1M x 4/16	10	10	12	8		
2M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	4M x 4/16	11	11	12	10	*13	9
8M x 64/72/80	4M x 4/16	11	11	12	10	*13	9
8M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	16M x 4/16	12	12	13	11	*14	10
32M x 64/72/80	16M x 4/16	12	12	13	11	*14	10
32M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	64M x 4	TBD	TBD				

(Note: All options possible with DRAM standards are shown)
* This addressing option applies to x16 DRAM configuration

b. Allowable configurations: (Byte 11)
- x64 (Non-parity, Byte controls)
- x72 (Parity, Byte controls)
- x72 (ECC-optimized, Byte controls)
- x80 (ECC-optimized, Byte controls)

c. Functional Attributes:
- Power Supply Voltage/Interface levels (Byte 8)
- $\overline{RAS}$ access (Byte 9)
- $\overline{CAS}$ access (Byte 10)
- Refresh rate/type (Byte 12)

Figure 4.5.3–F
168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

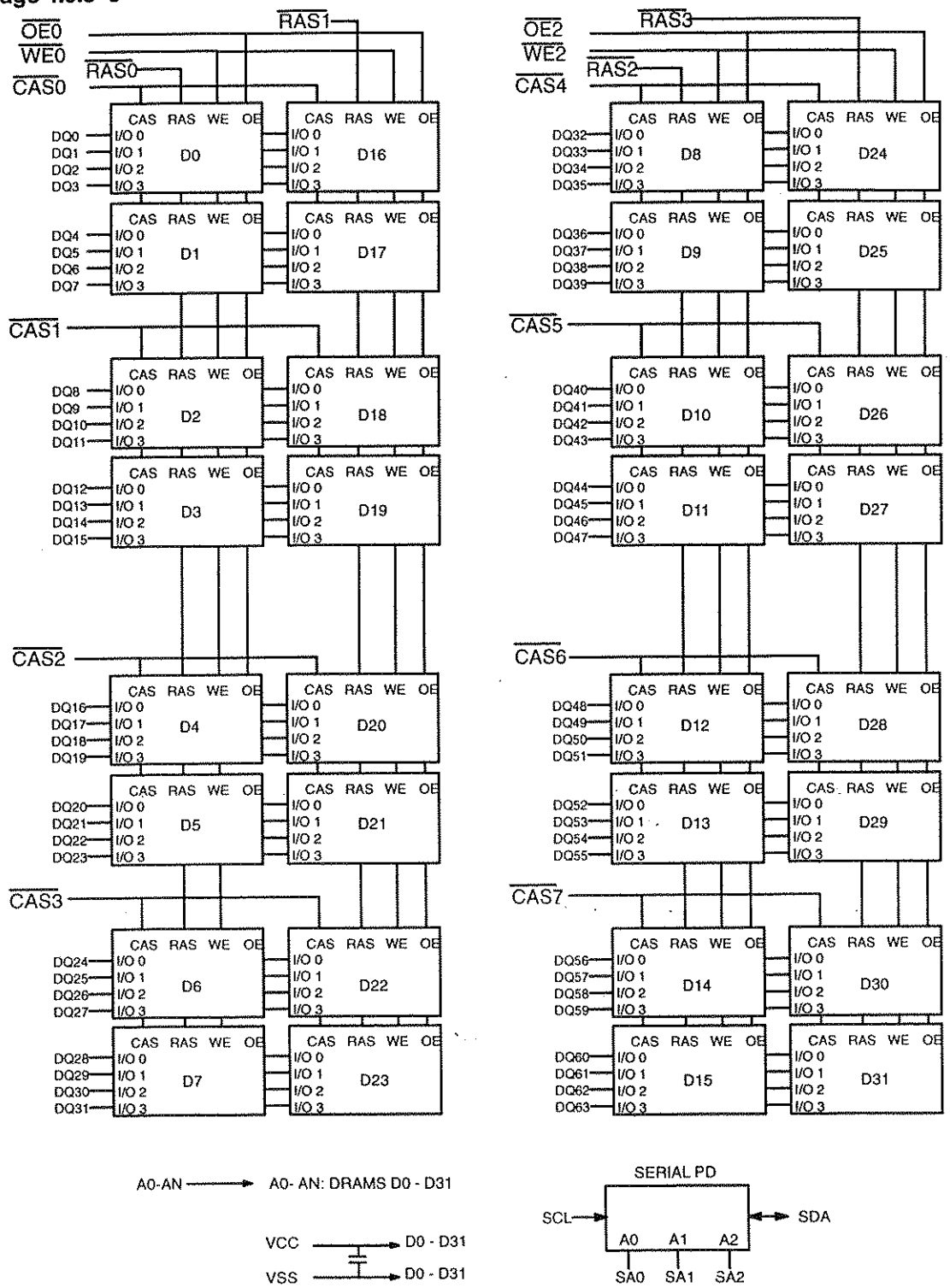


Figure 4.5.3–G
X64 DRAM DIMM, 2 Banks with X4 DRAMs

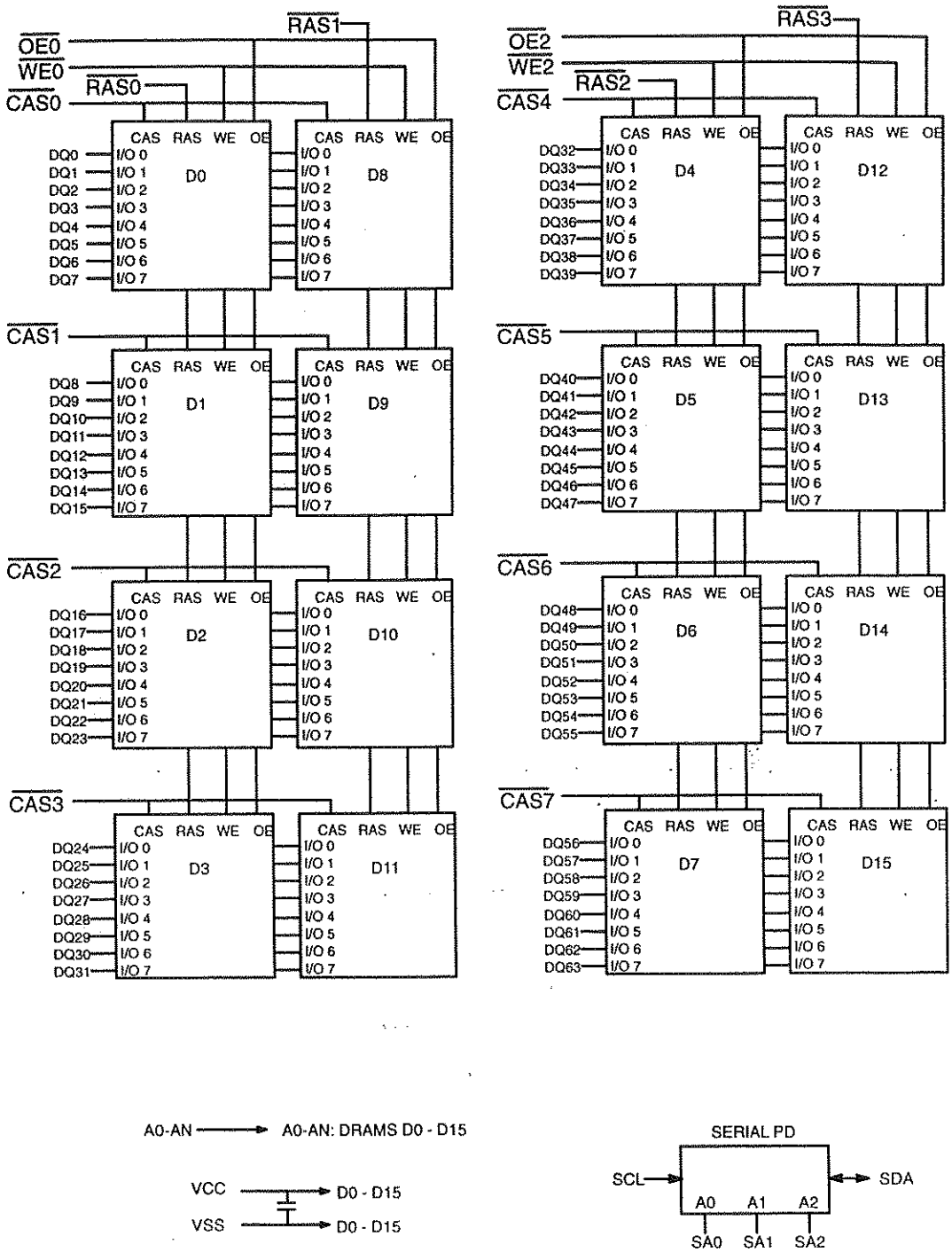


Figure 4.5.3–H
X64 DRAM DIMM, 2 Banks with X8 DRAMs

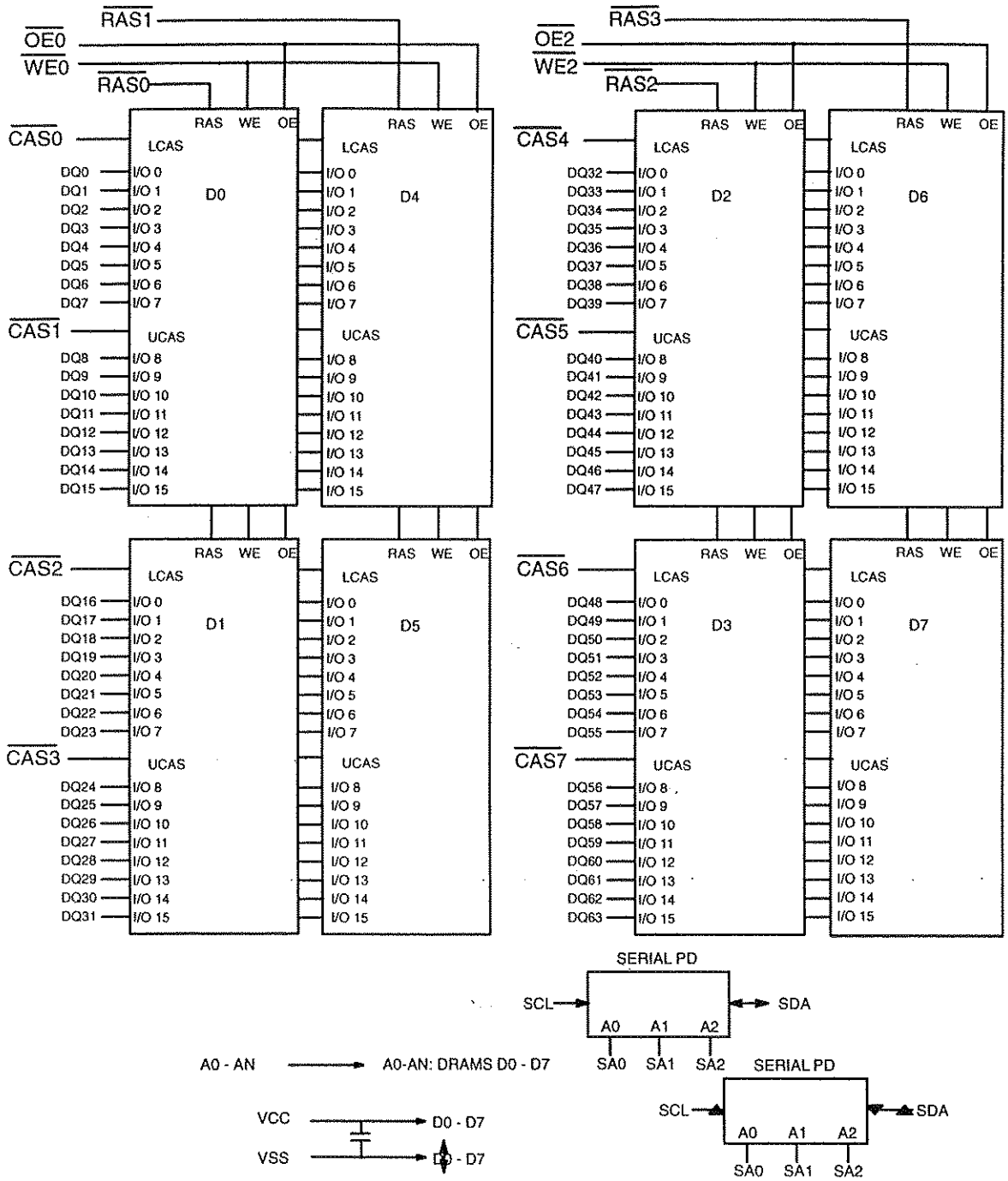


Figure 4.5.3–I
X64 DRAM DIMM, 2 Banks with X16 DRAMs

Release 7

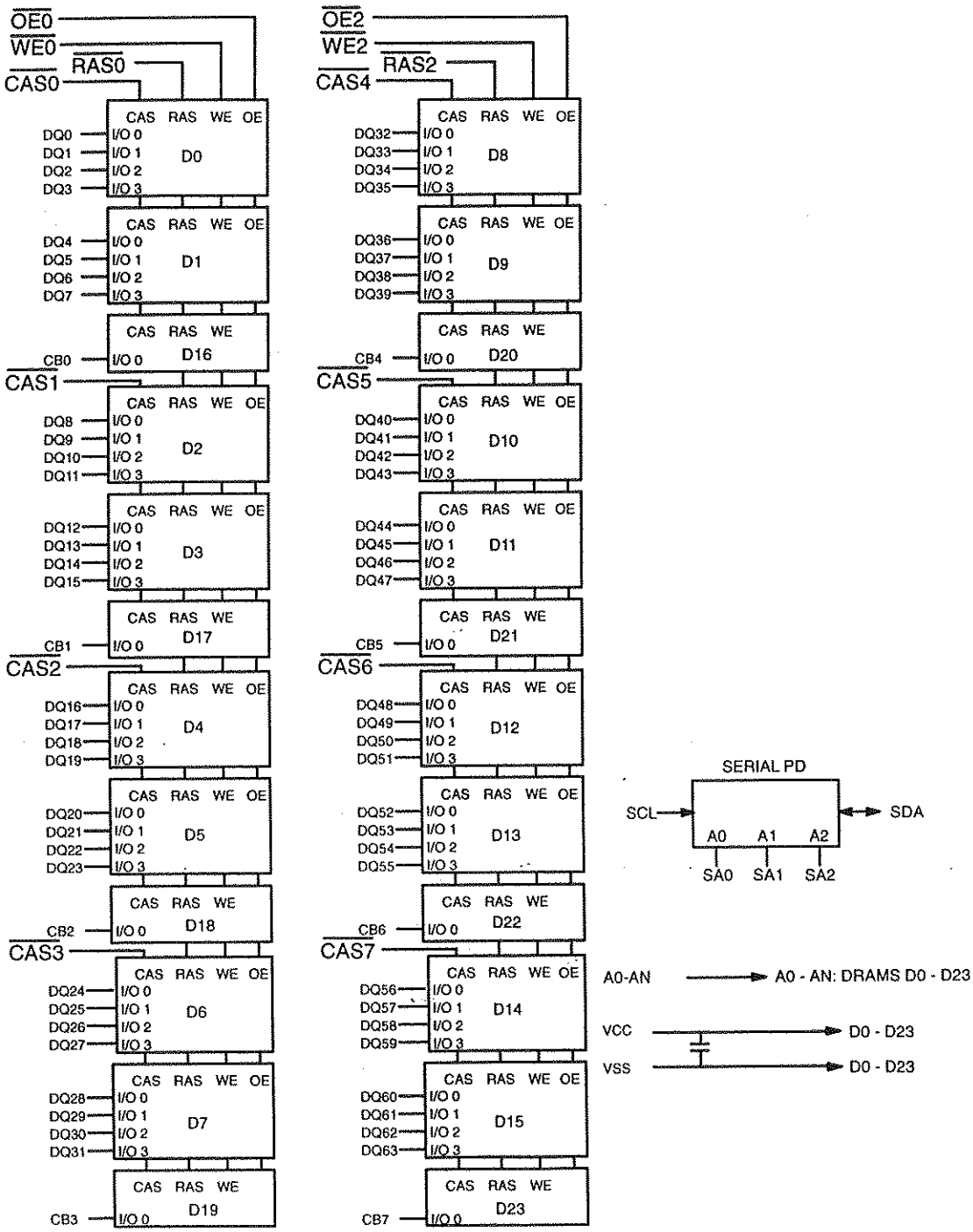


Figure 4.5.3–J
X64 DRAM DIMM, 2 Banks with X4/X1 DRAMs

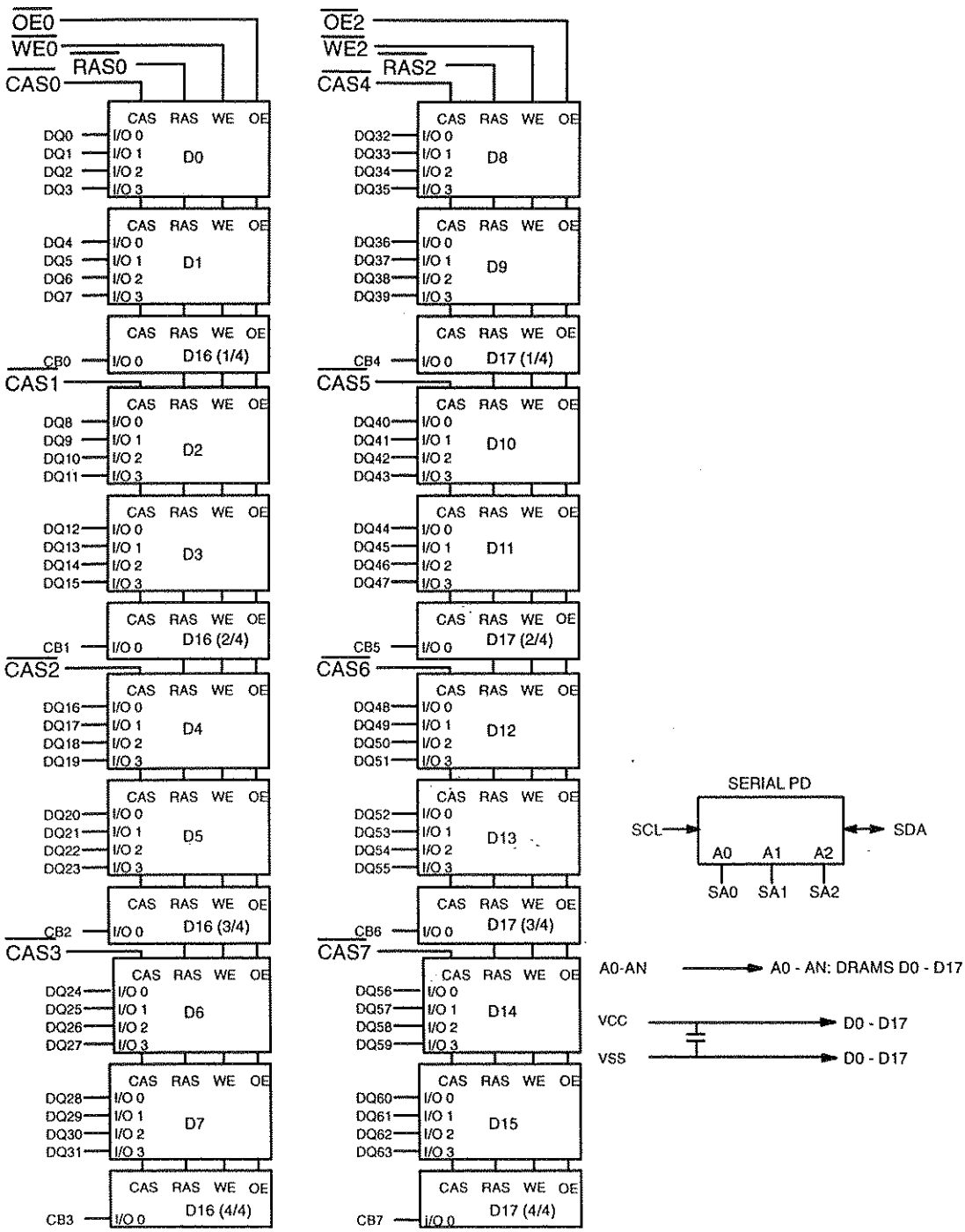


Figure 4.5.3–K
X72 Parity DRAM DIMM, 2 Banks with X4 & X4 W/4 CAS DRAMs

XILINX EXHIBIT 1010
Page 370

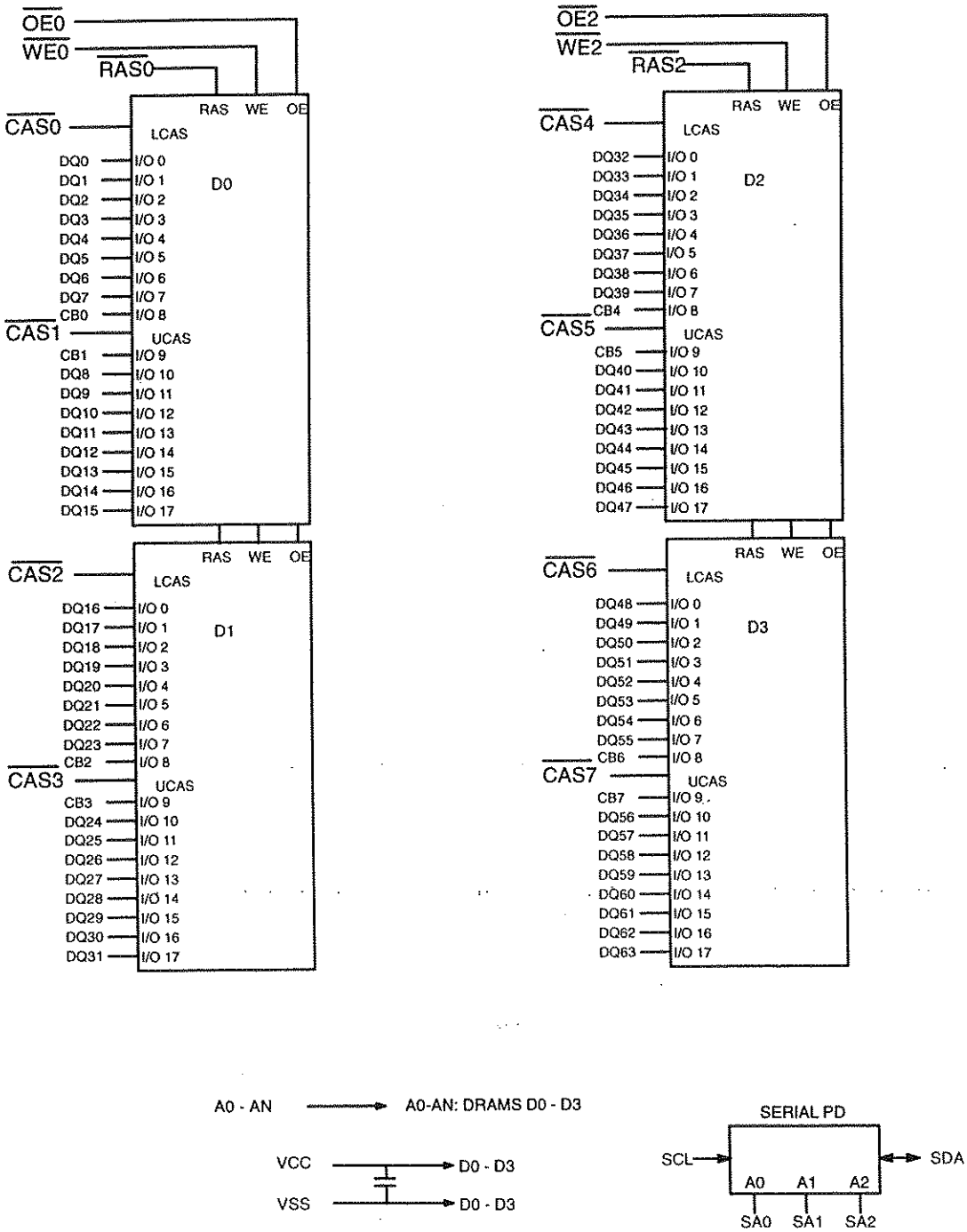


Figure 4.5.3–L
X72 Parity DRAM DIMM, 2 Banks with X16 DRAMs

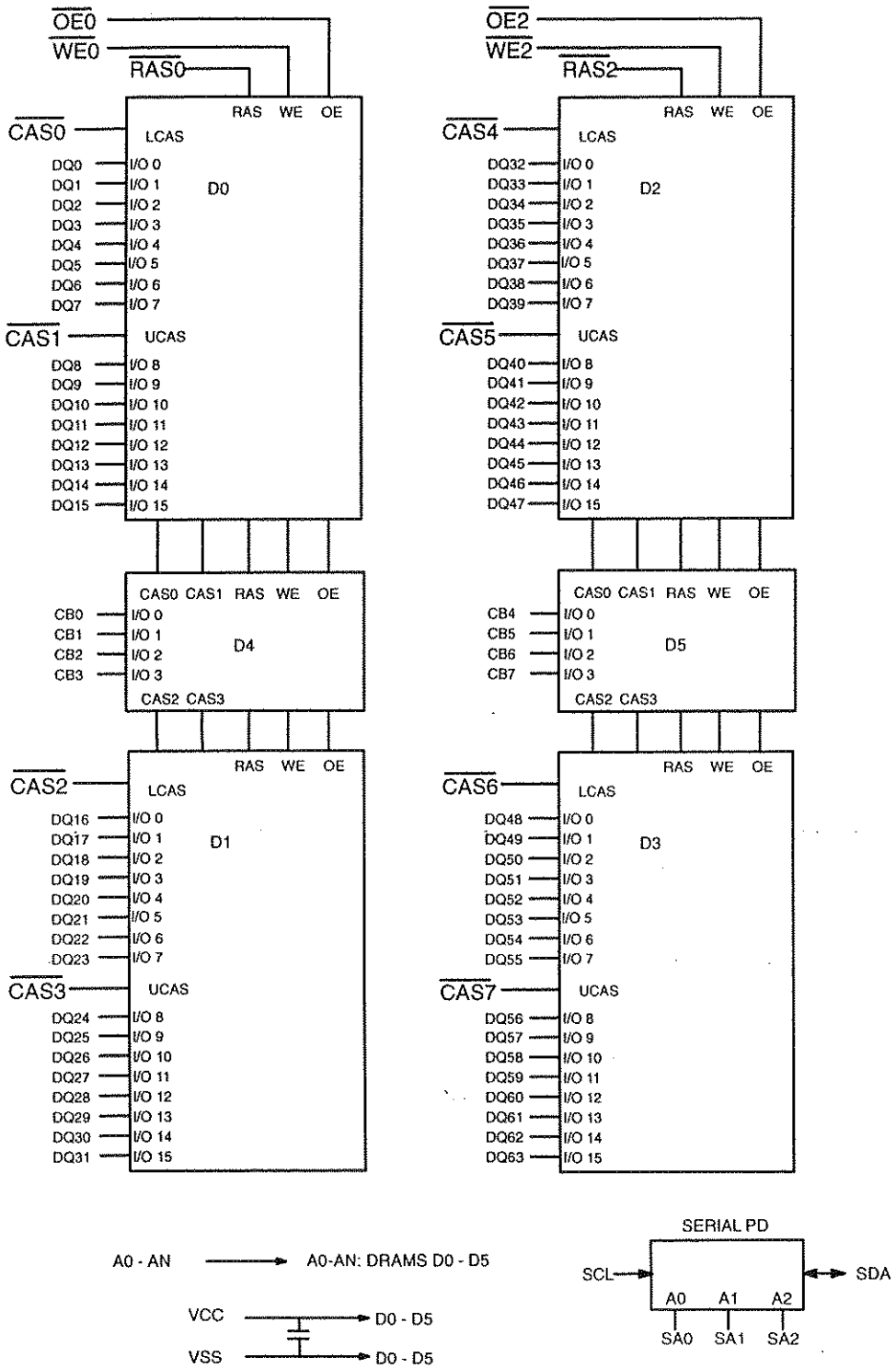


Figure 4.5.3–M
X72 Parity DRAM DIMM, 2 Banks with X16 & X4 W/4 CAS DRAMs

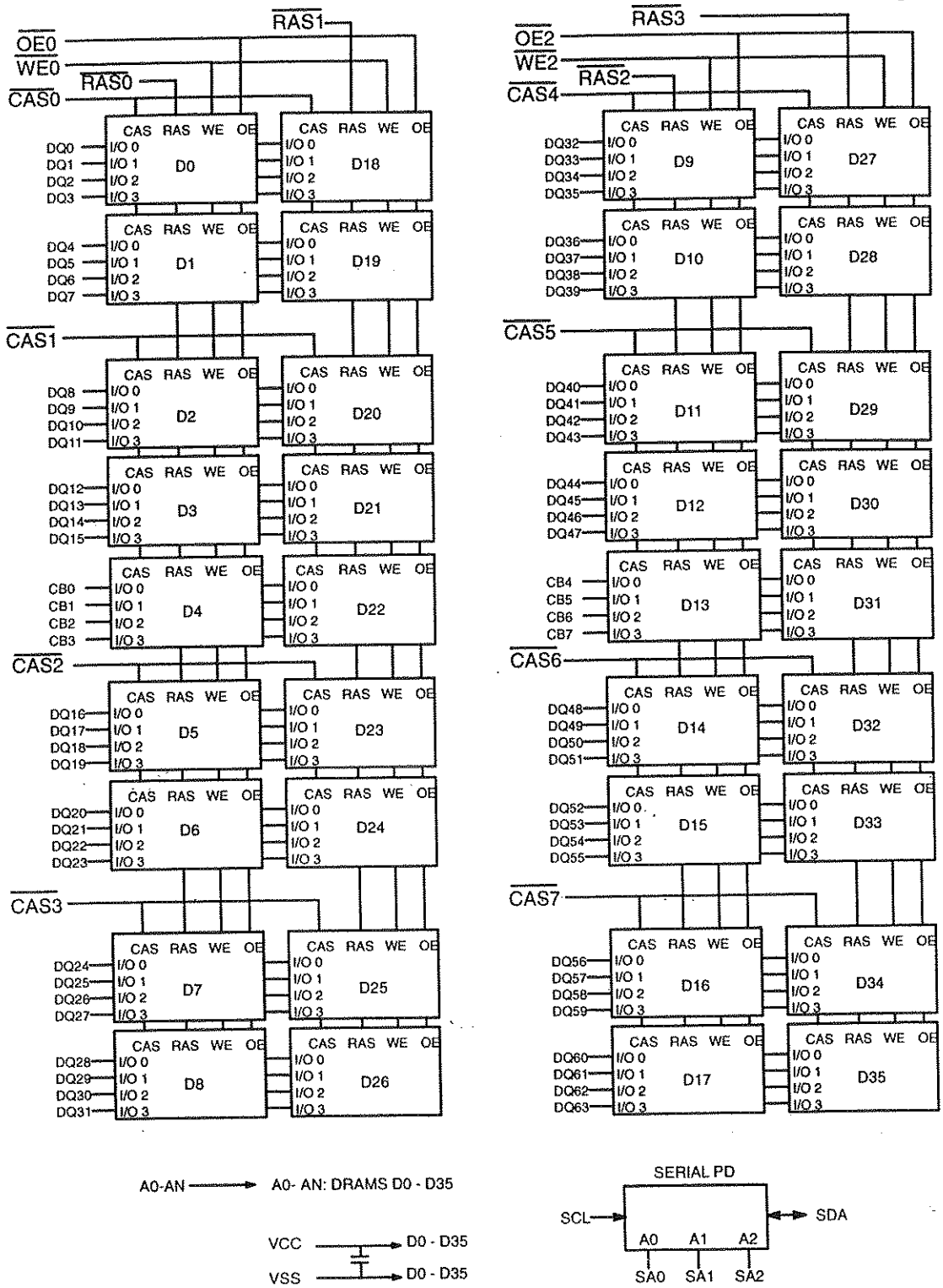


Figure 4.5.3–N
X72 ECC DRAM DIMM, 2 Banks with X4 DRAMs

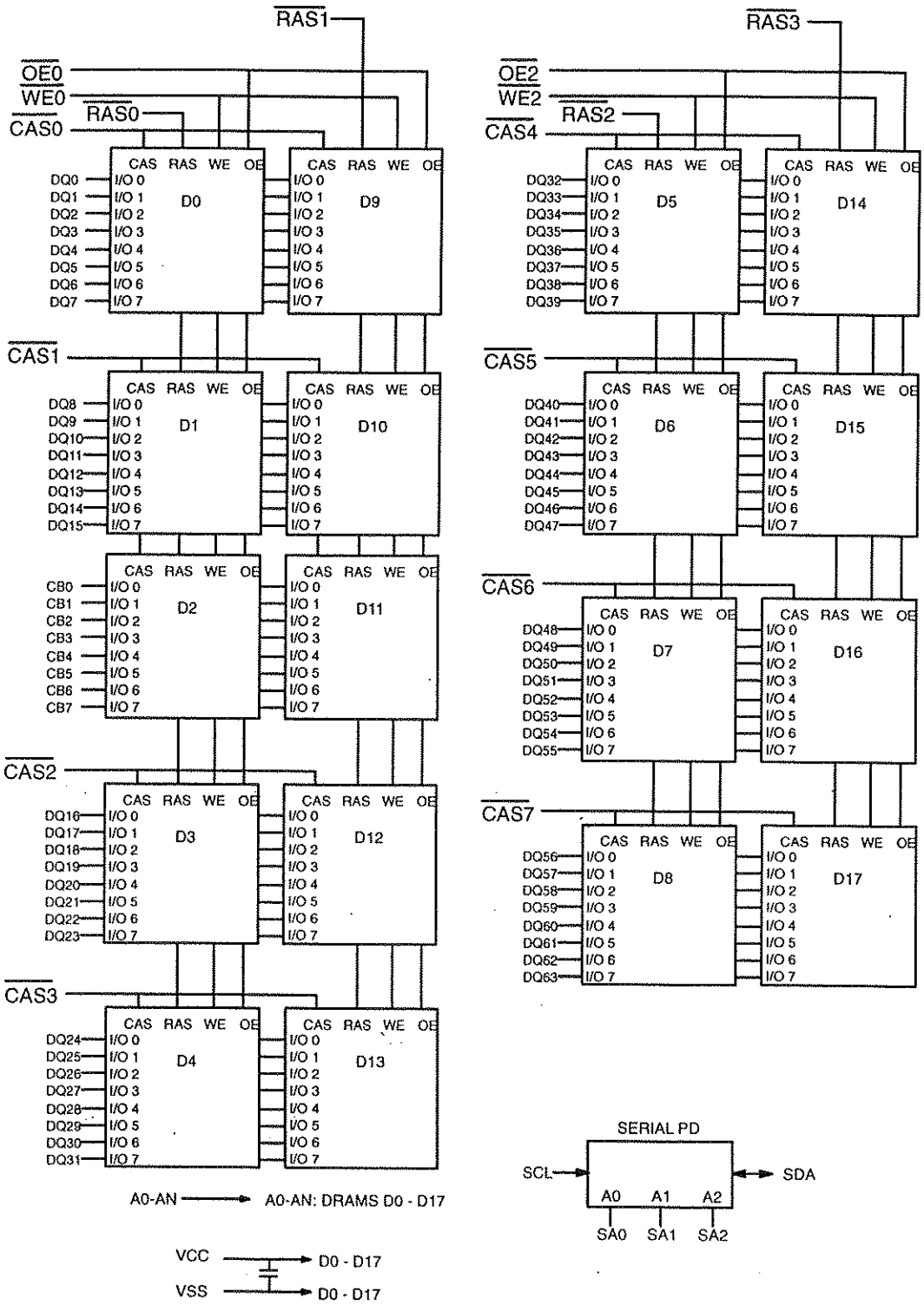


Figure 4.5.3–O
X72 ECC DRAM DIMM, 2 Banks with X8 DRAMs

XILINX EXHIBIT 1010
Page 374

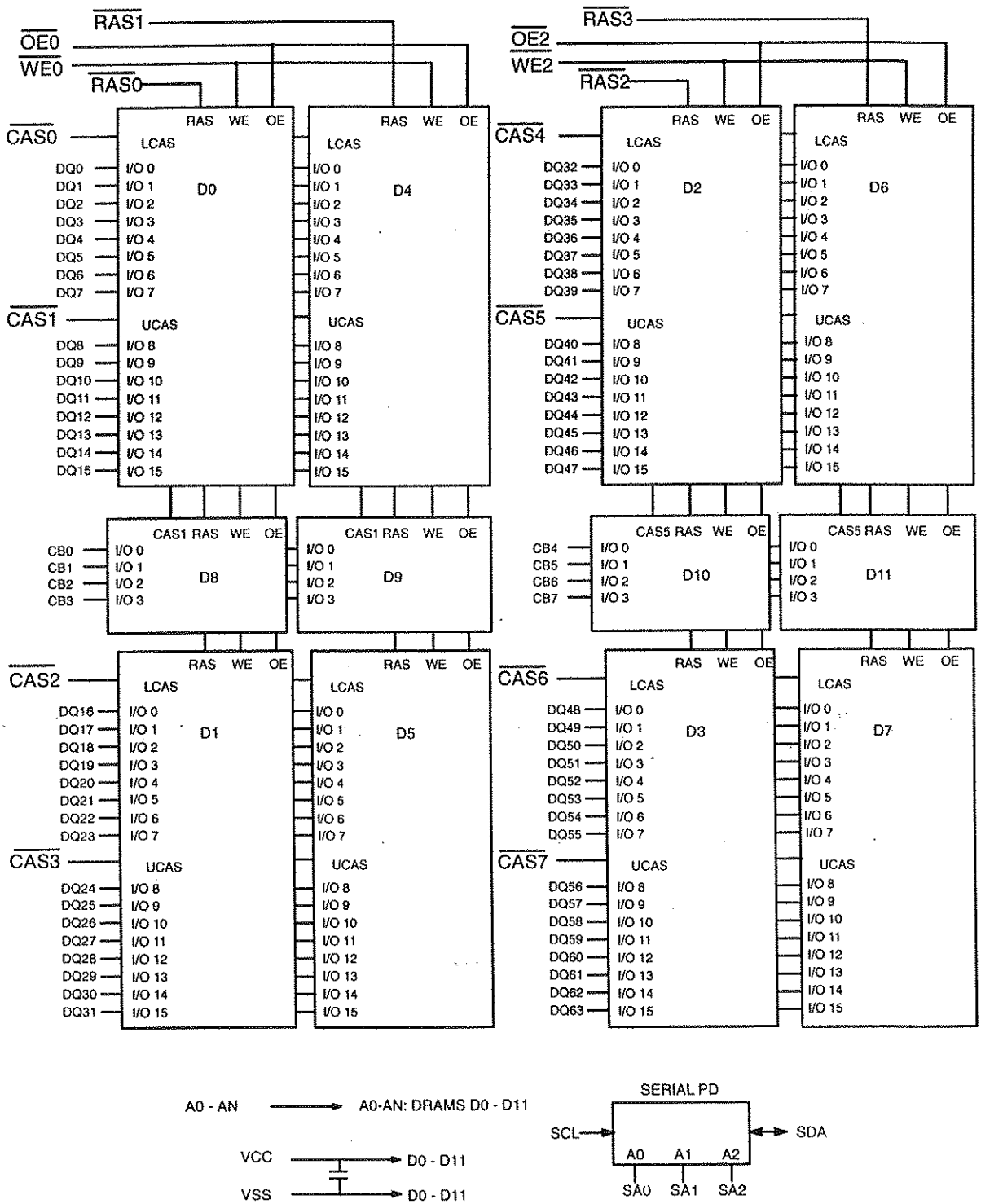


Figure 4.5.3–P
X72 ECC DRAM DIMM, 2 Banks with X16 & X4 DRAMs

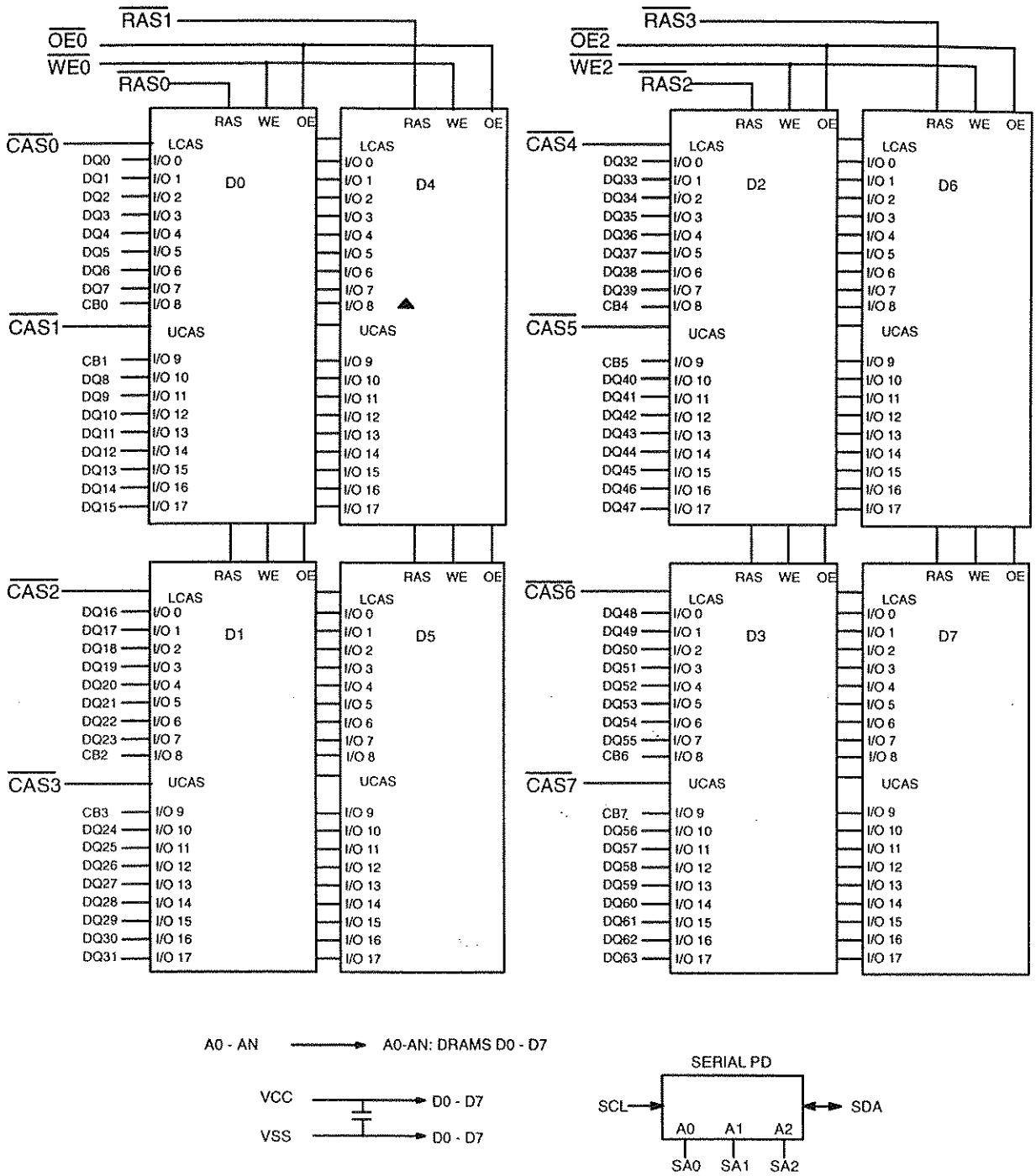


Figure 4.5.3–Q
X72 ECC DRAM DIMM, 2 Banks with X18 DRAMs

XILINX EXHIBIT 1010
Page 376

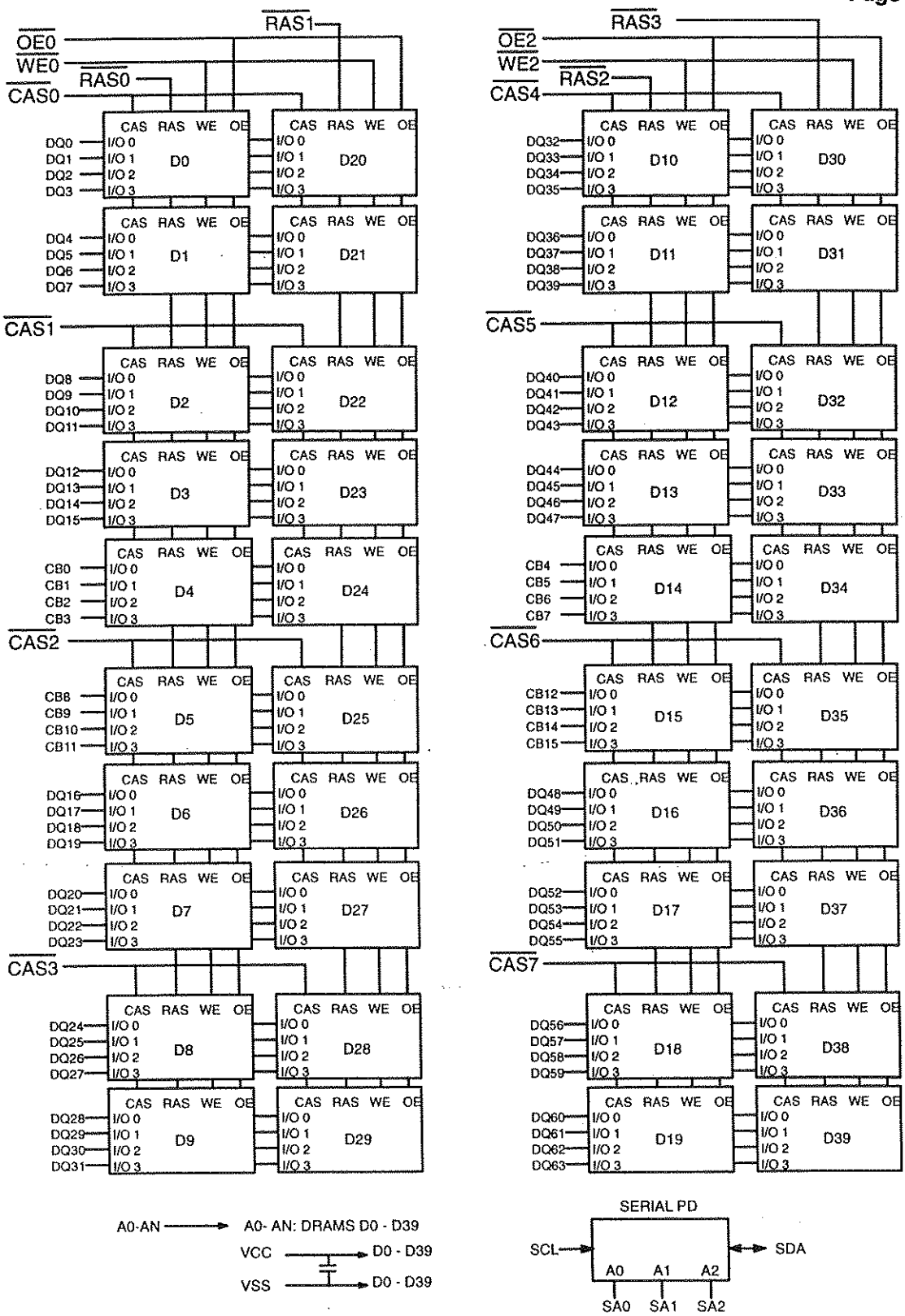


Figure 4.5.3–R
X80 DRAM DIMM, 2 Banks with X4 DRAMs

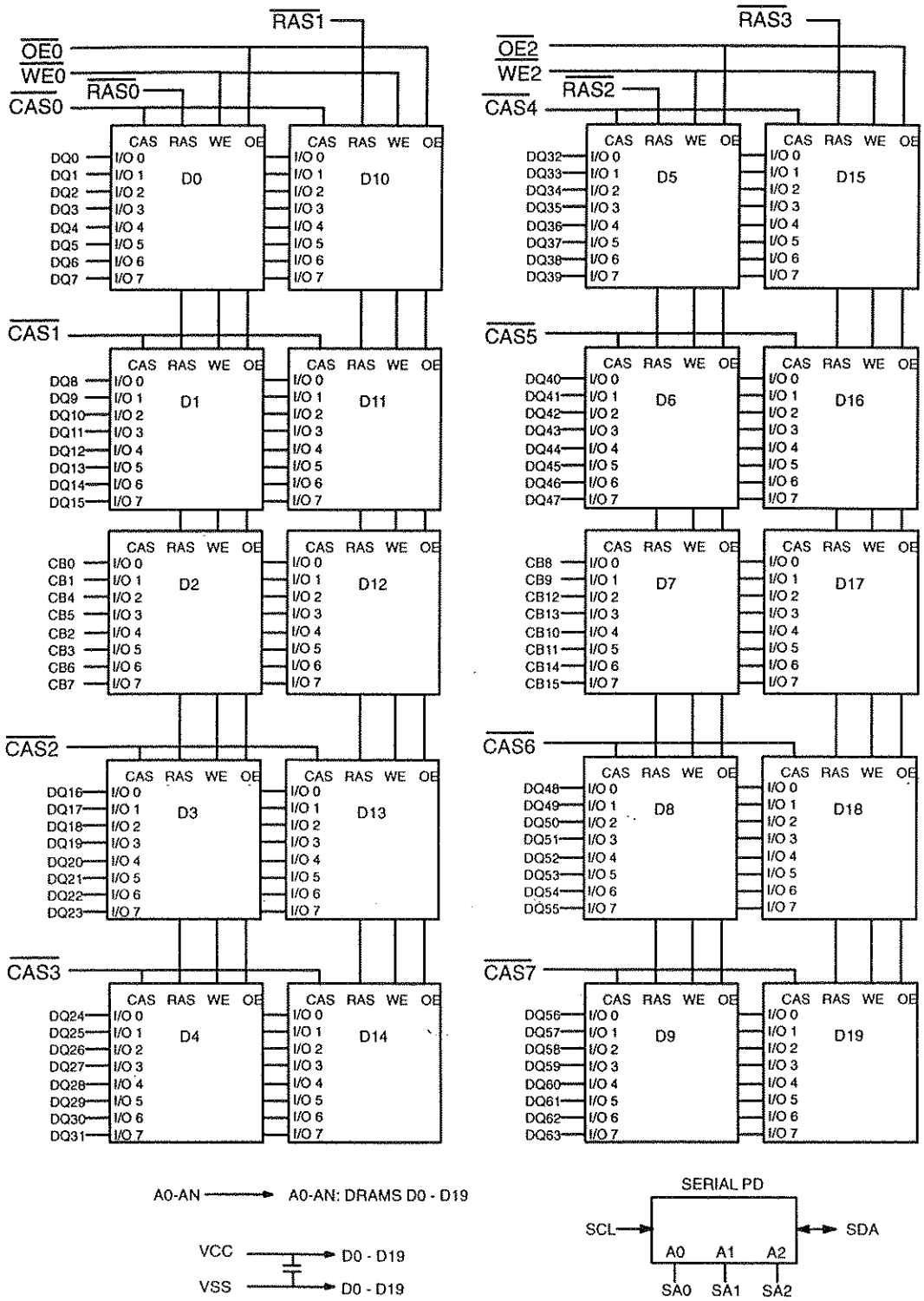


Figure 4.5.3–S
X80 ECC DRAM DIMM, 2 Banks with X8 DRAMs

4.5.4 – 168 PIN UNBUFFERED SDRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS—Figs. 4.5.4–A, & 4.5.4–B,
SPD TABLE & INFORMATION—Fig. 4.5.4–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM—Fig. 4.5.4–D
KEYING METHODOLOGY—Fig. 4.5.4–E
PINOUT COMPARISON DRAM & SDRAM DIMM—Fig. 4.5.4–F
SDRAM CLOCK LOADING—Fig. 4.5.4–G
SDRAM CLOCK WIRING—Fig. 4.5.4–H
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.4–I through 4.5.4–Y

XILINX EXHIBIT 1010
Page 379

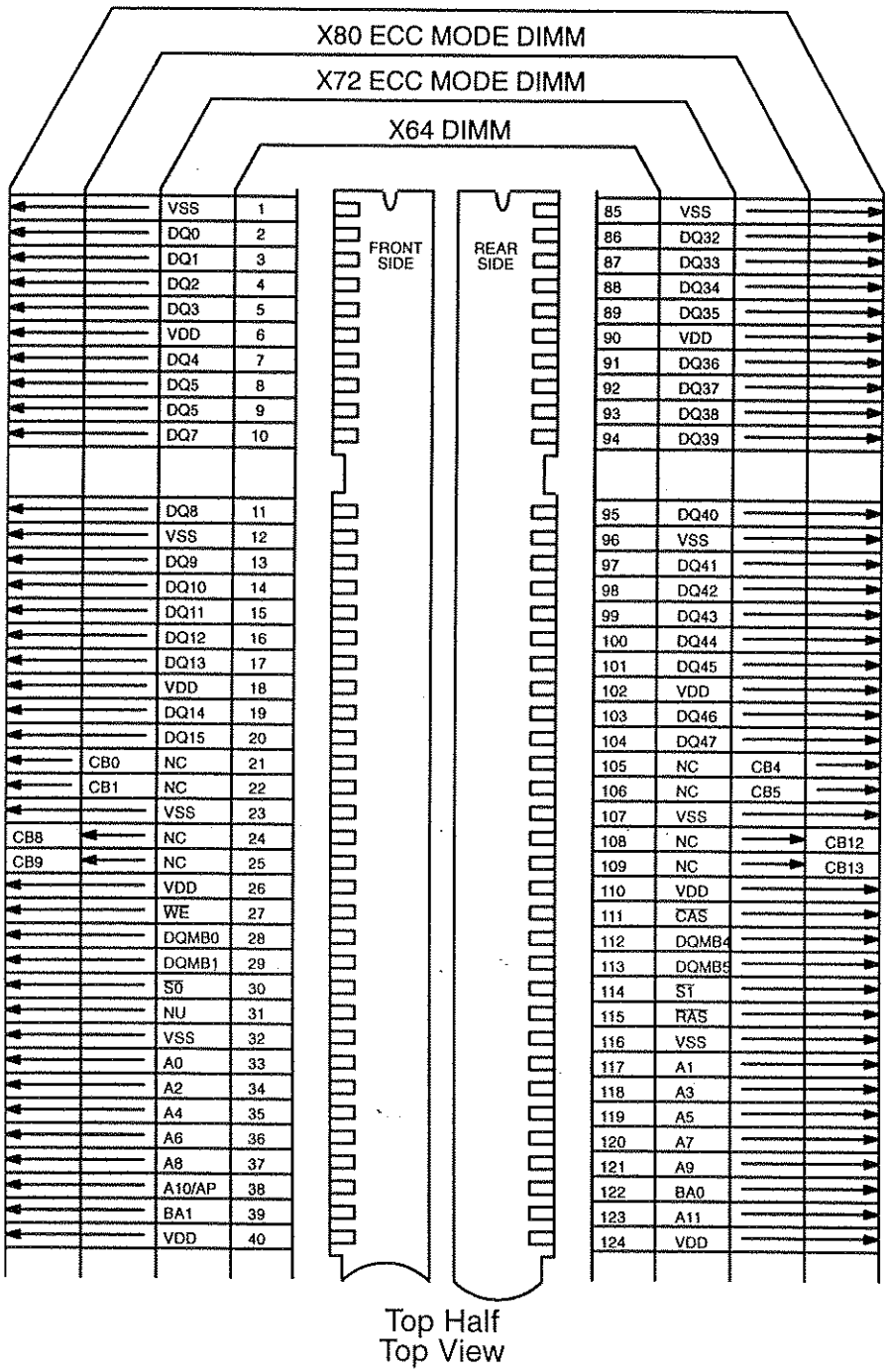


FIGURE 4.5.4–A
168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

Release 7

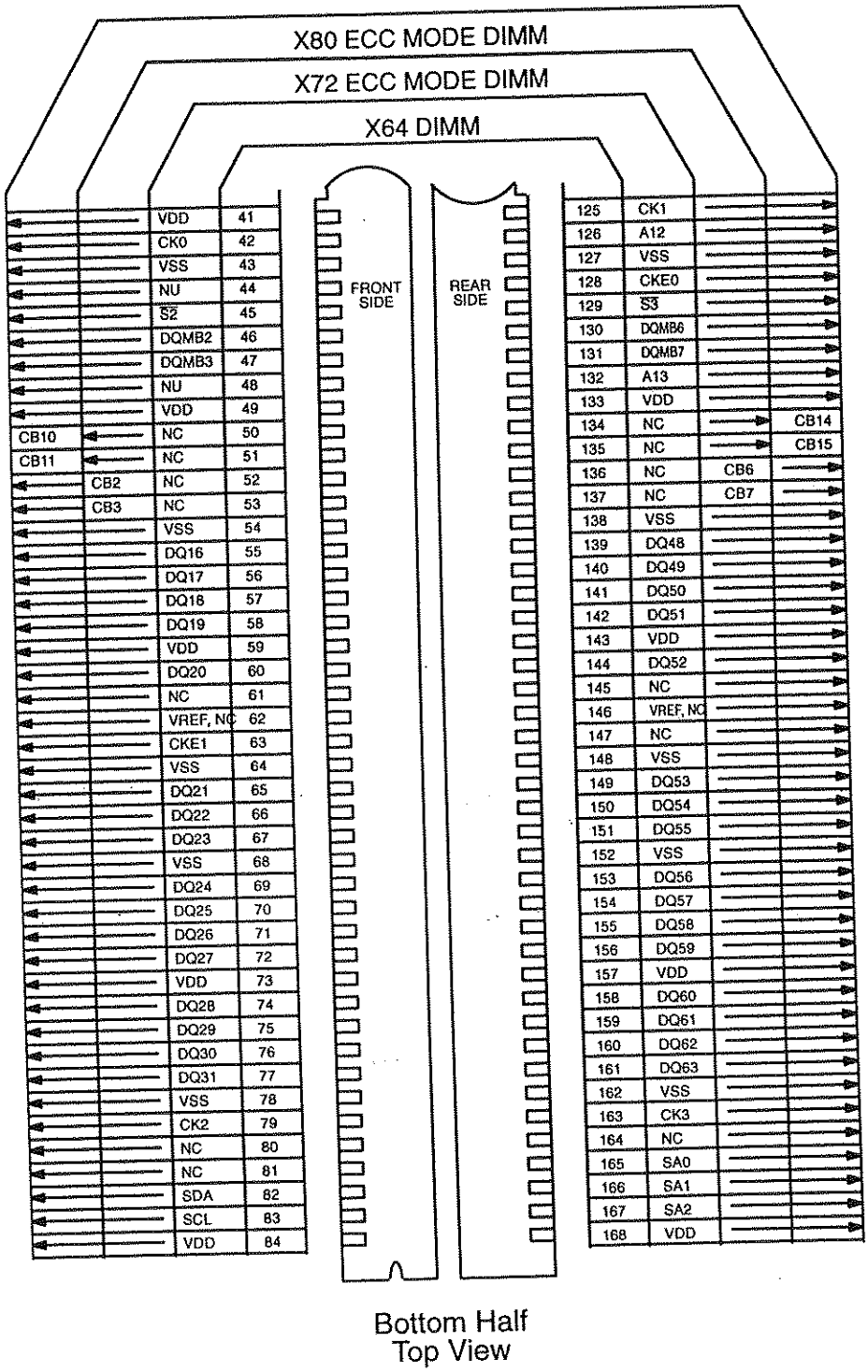


FIGURE 4.5.4–B
168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.
1M x 64/72/80	1M x 16	1	11	8						
2M x 64/72/80	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72/80	2M x 8	1	11	9						
4M x 64/72/80	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72/80	4M x 4	1	11	10						
4M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72/80	16M x 4	2	12	10	1	13	10			
16M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	64M x 4	2	13	11						
(Note: All options possible with SDRAM standards are shown)										

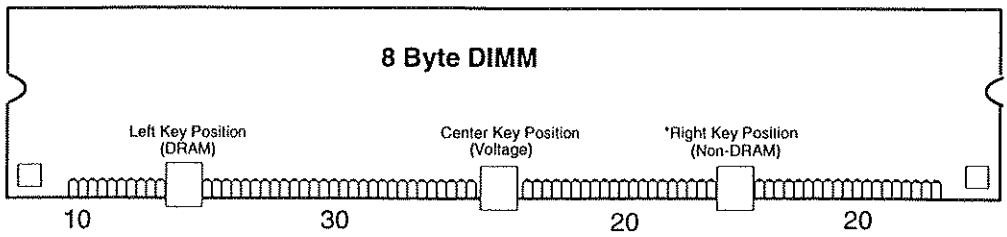
b. Allowable configurations: (Byte 11)
   - x64 (Non-parity, Byte controls)
   - x72 (ECC-optimized, Byte controls)
   - x80 (ECC-optimized, Byte controls)

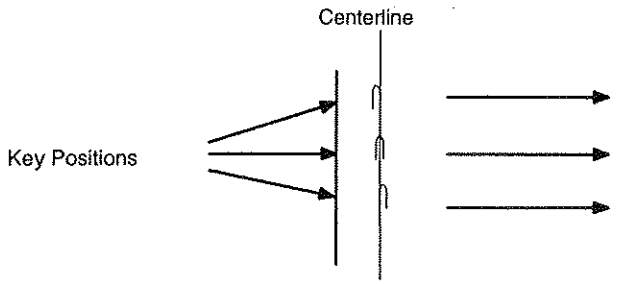
c. Functional Attributes:
   - Power Supply Voltage/Interface levels (Byte 8)
   - SDRAM cycle time (Byte 9)
   - SDRAM access from Clock (Byte 10)
   - Refresh rate/type (Byte 12)
   - SDRAM module attributes (Byte 13)
   - SDRAM device attributes (Bytes 14 - 20)
   - Primary/Secondary DRAM (Bytes 21 - 22)

Figure 4.5.4–C
168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins VCC - 16 VSS - 16	35 Power/Gnd Pins VCC - 17 (1 additional pin) VSS - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

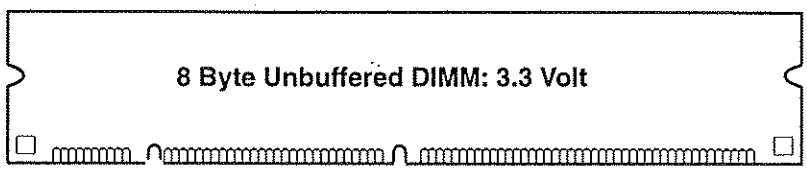
FIGURE 4.5.4–D
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.



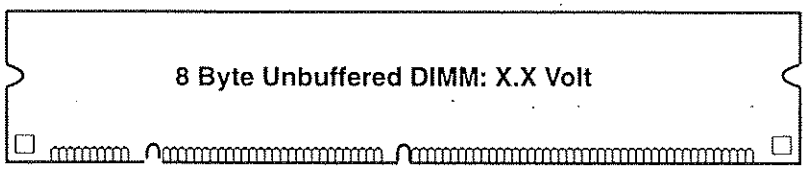


FIGURE 4.5.4–E
168 Pin DRAM DIMM Keying Methodology

Pin number	DRAM DIMM	SDRAM DIMM
39	A12	BA1
42	DU	CK0
44	$\overline{OE2}$	DU
45	$\overline{RAS2}$	$\overline{S2}$
46	$\overline{CAS2}$	DQMB2
47	$\overline{CAS3}$	DQMB3
48	$\overline{WE2}$	DU
62	DU	V_{REF}, NC
63	NC	CKE1
79	NC	CK2
111	DU	$\overline{CAS}$
112	$\overline{CAS4}$	DQMB4
113	$\overline{CAS5}$	DQMB5
114	$\overline{RAS1}$	$\overline{S1}$
115	DU	$\overline{RAS}$
122	A11	BA0
123	A13	A11
125	DU	CK1
126	DU	A12
128	DU	CKE0
129	$\overline{RAS3}$	$\overline{S3}$
130	$\overline{CAS6}$	DQMB6
131	$\overline{CAS7}$	DQMB7
132	DU	A13
146	DU	V_{REF}, NC
163	NC	CK3

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM

FIGURE 4.5.4–F
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

X 64 (Non–parity)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
x4	1	16	4	4	4	4
x8	1	8	4	4	*	*
x16	1	4	4	*	*	*
x32	1	2	*2	*	*	*
x8	2	16	4	4	4	4
x16	2	8	4	4	*	*
x32	2	4	4	*	*	*

X 72 (ECC)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
x4	1	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
x8	1	9	** 4 or 5	** 4 or 5	*	*
x16/x4	1	6	4 (MAX)	4 (MAX)	*	*
x32/x8	1	3	*3	*	*	*
x8	2	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
x16/x4	2	12	4	4	4	
x32/x8	2	6	4 (MAX)	4 (MAX)	*	*

X 80 (ECC)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
x4	1	20	5	5	5	5
x8	1	10	5	5	*	*
x16	1	5	5	*	*	*
x32/x8	1	4	4	*	*	*
x8	2	20	5	5	5	5
x16	2	10	5	5	*	*
x32/x8	2	8	4	4	*	*

Notes:

* add padding capacitance per clock wiring detail.

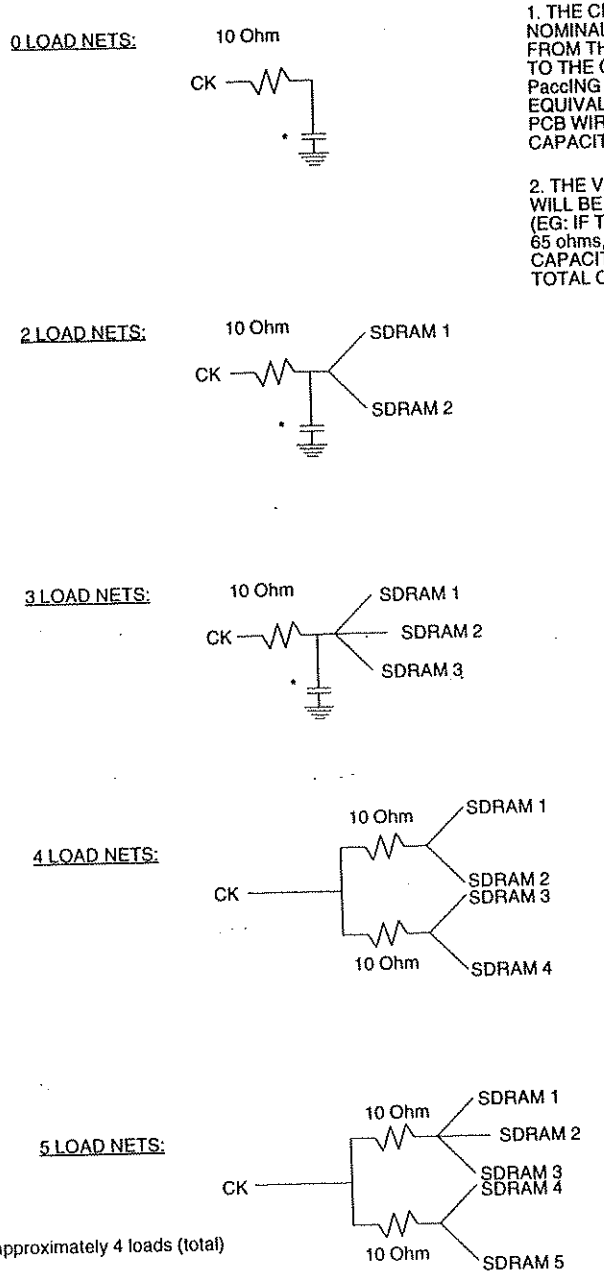
** CK0 + CK2 must total 9 SDRAMs, CK1 + CK3 must total 9 SDRAMs (to allow clock "dotting" at system).

Figure 4.5.4–G
168 Pin UNBUFFERED SDRAM DIMM CLOCK LOADING

TARGET CLOCK (CK) SPECIFICATION:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .6ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PaccING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 3" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. THE VARIATION OF CK INPUT DELAY WILL BE +/- .1ns FOR ALL FOUR CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/- 3pf IN TOTAL CK INPUT CAPACITANCE).



* add padding capacitance to approximately 4 loads (total)

Figure 4.5.4–H
168 Pin UNBUFFERED DRAM DIMM CLOCK WIRING

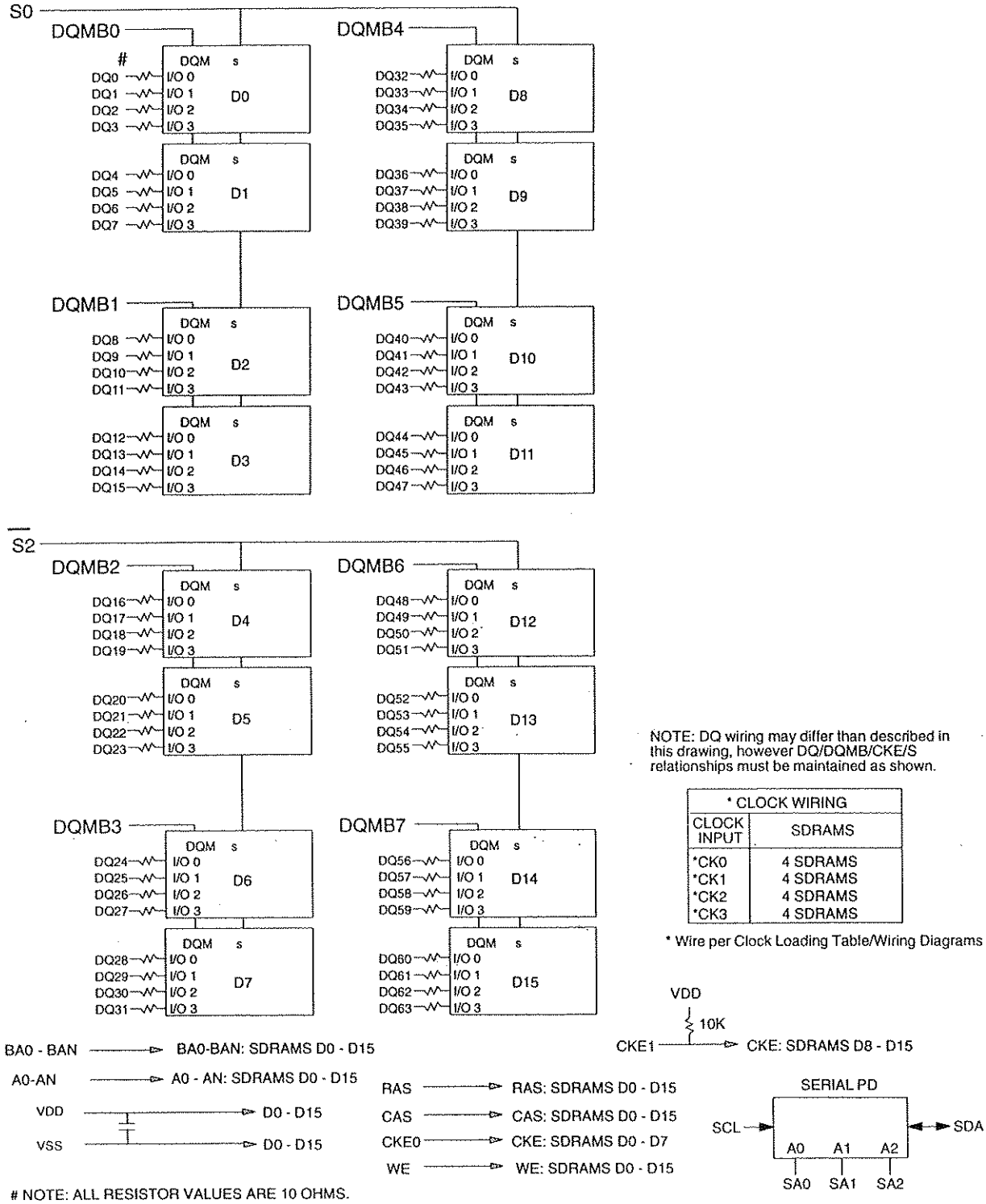


Figure 4.5.4–I
X64 SDRAM DIMM, 1 Bank with X4 SDRAMs

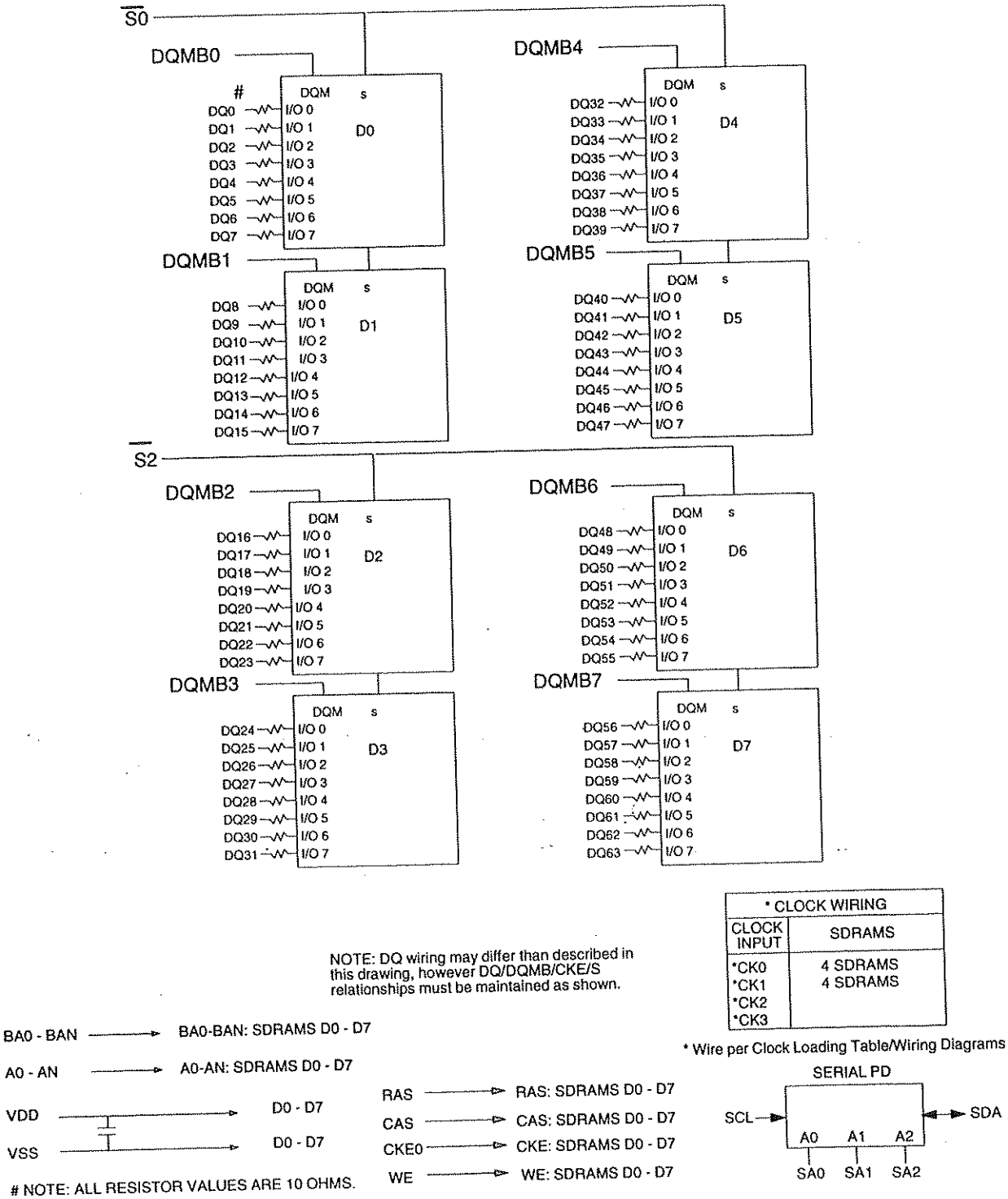
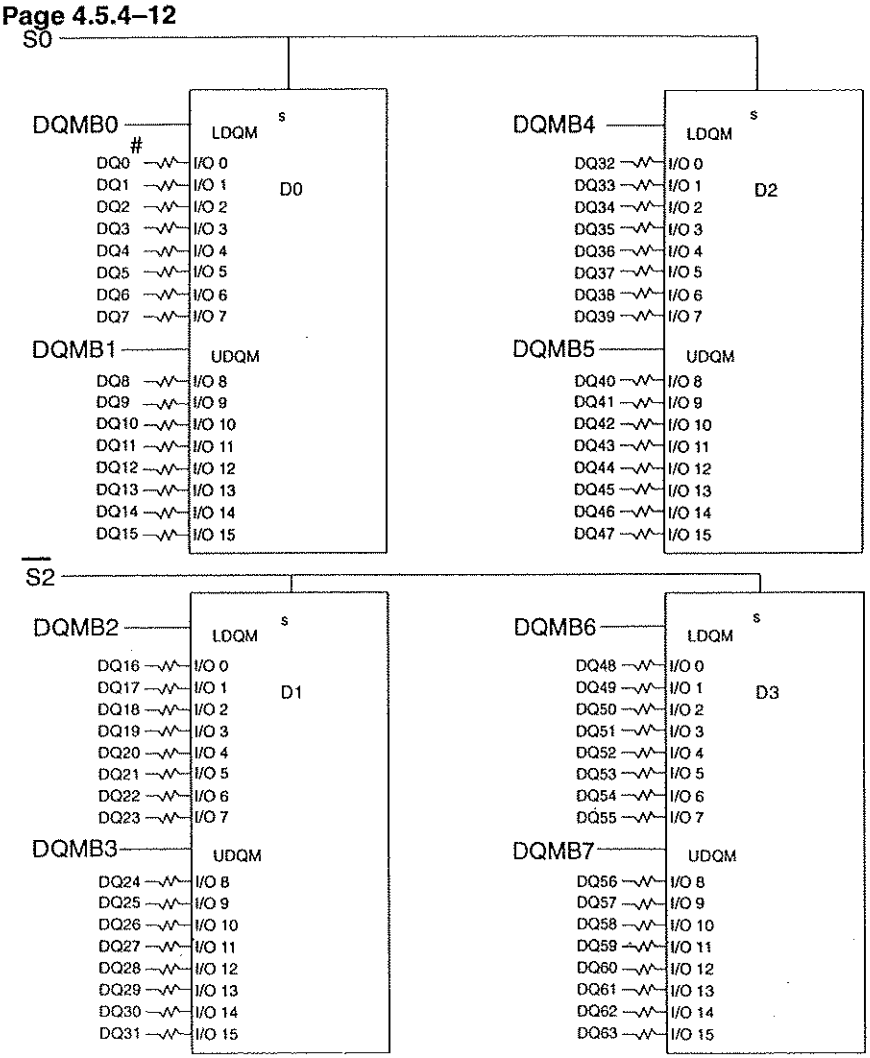
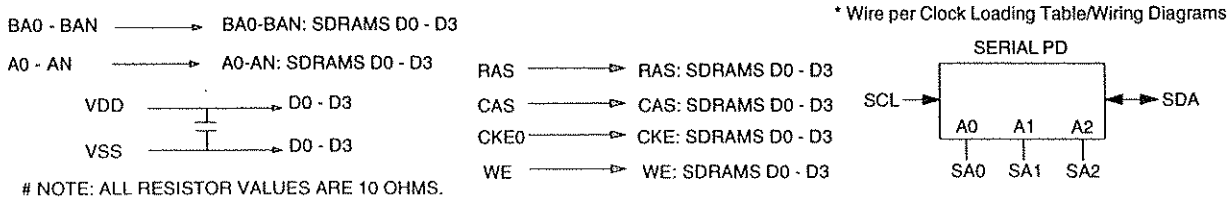


Figure 4.5.4–J
X64 SDRAM DIMM, 1 Bank with X8 SDRAMs



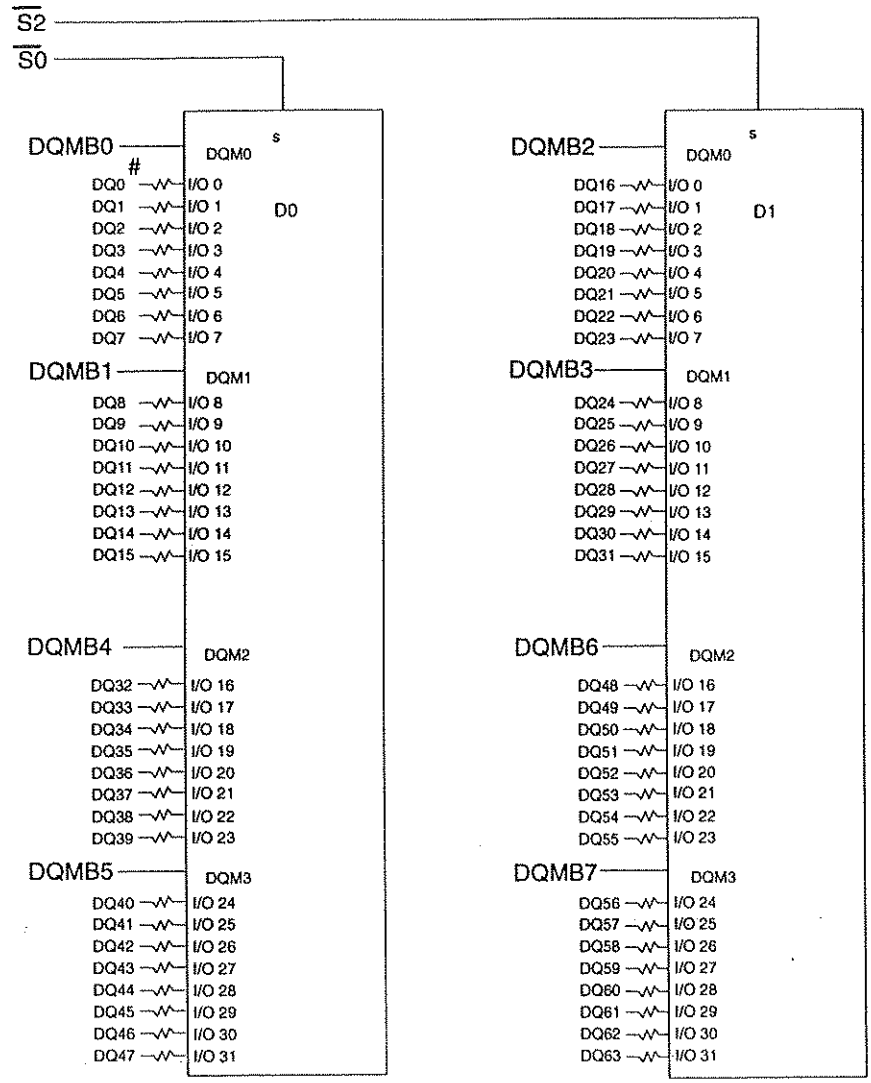
NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	4 SDRAMS



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

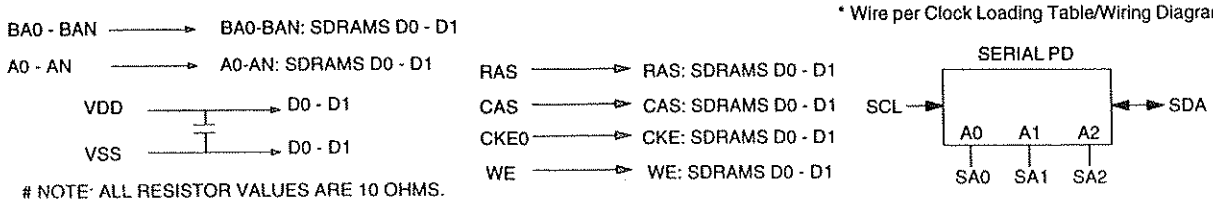
Figure 4.5.4–K
X64 SDRAM DIMM, 1 Bank with X16 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

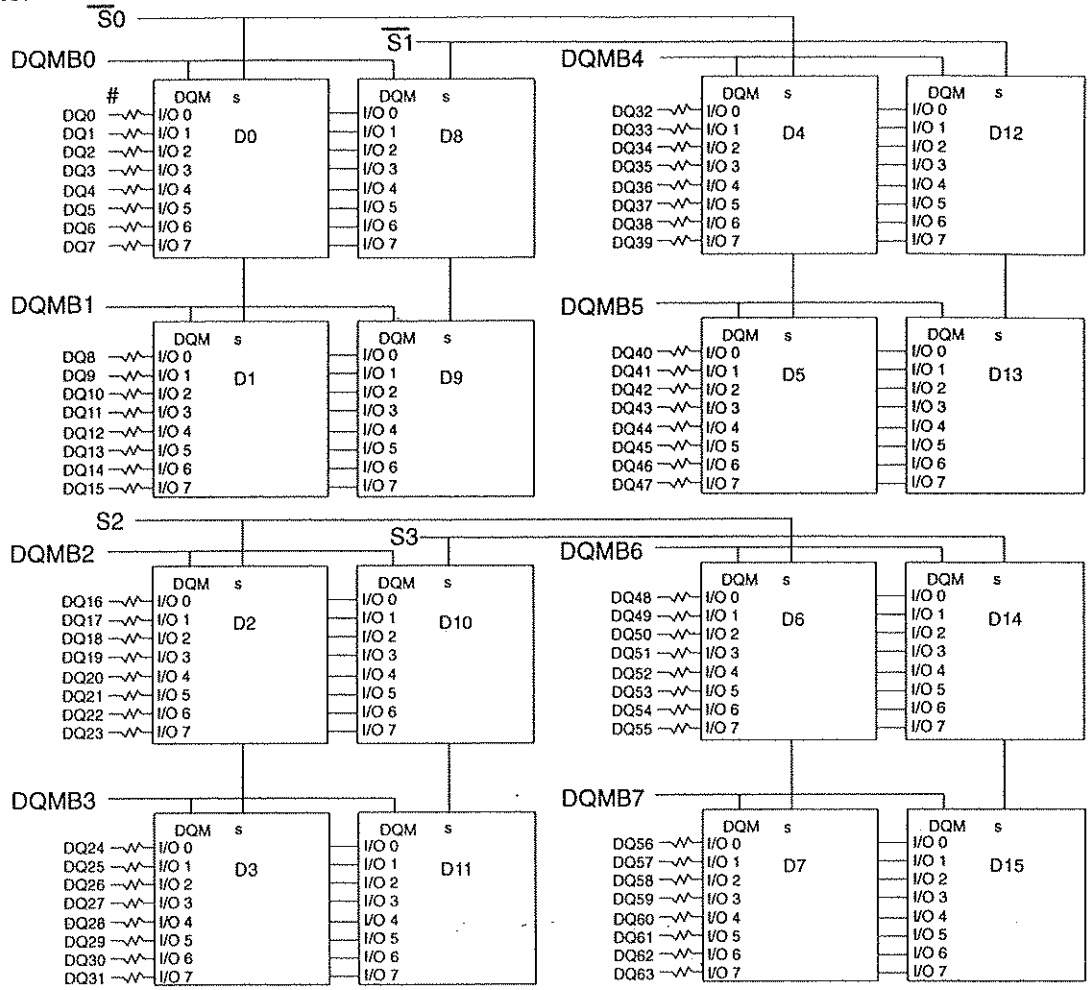
* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	2 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–L
X64 SDRAM DIMM, 1 Bank with X32 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS
*CK2	4 SDRAMS
*CK3	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

VDD — 10K — CKE1 → CKE: SDRAMS D8 - D15

BA0 - BAN → BA0-BAN: SDRAMS D0 - D15

A0 - AN → A0-AN: SDRAMS D0 - D15

VDD → D0 - D15

VSS → D0 - D15

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

RAS → RAS: SDRAMS D0 - D15

CAS → CAS: SDRAMS D0 - D15

CKE0 → CKE: SDRAMS D0 - D7

WE → WE: SDRAMS D0 - D15

* Wire per Clock Loading Table/Wiring Diagrams

SERIAL PD: SCL, SDA, A0, A1, A2, SA0, SA1, SA2

VDD — 10K — CKE1 → CKE: SDRAMS D4 - D7, D9, D11

Figure 4.5.4–M
X64 SDRAM DIMM, 2 Banks with X8 SDRAMs

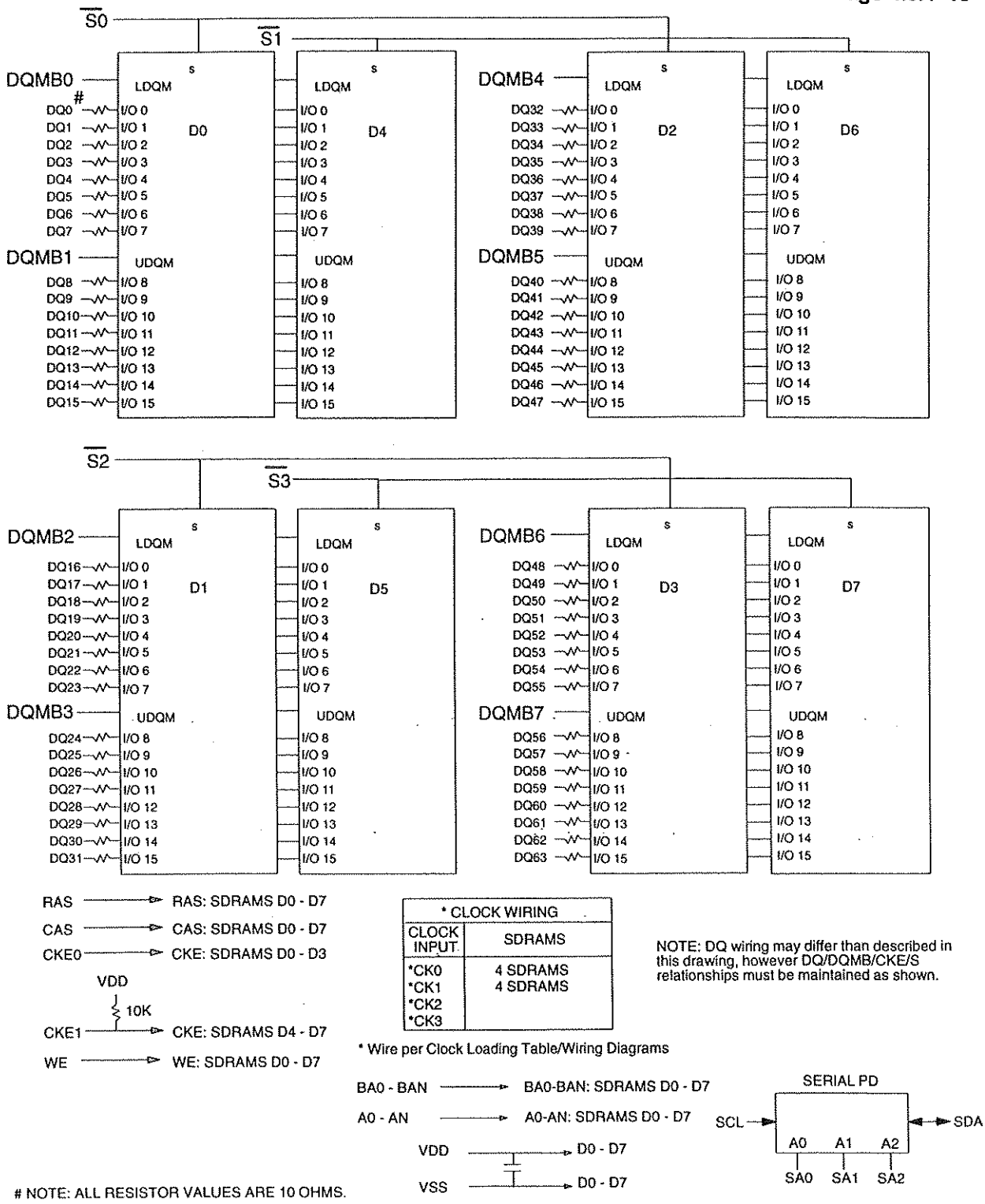


Figure 4.5.4–N
X64 SDRAM DIMM, 2 Banks with X16 SDRAMs

Release 7

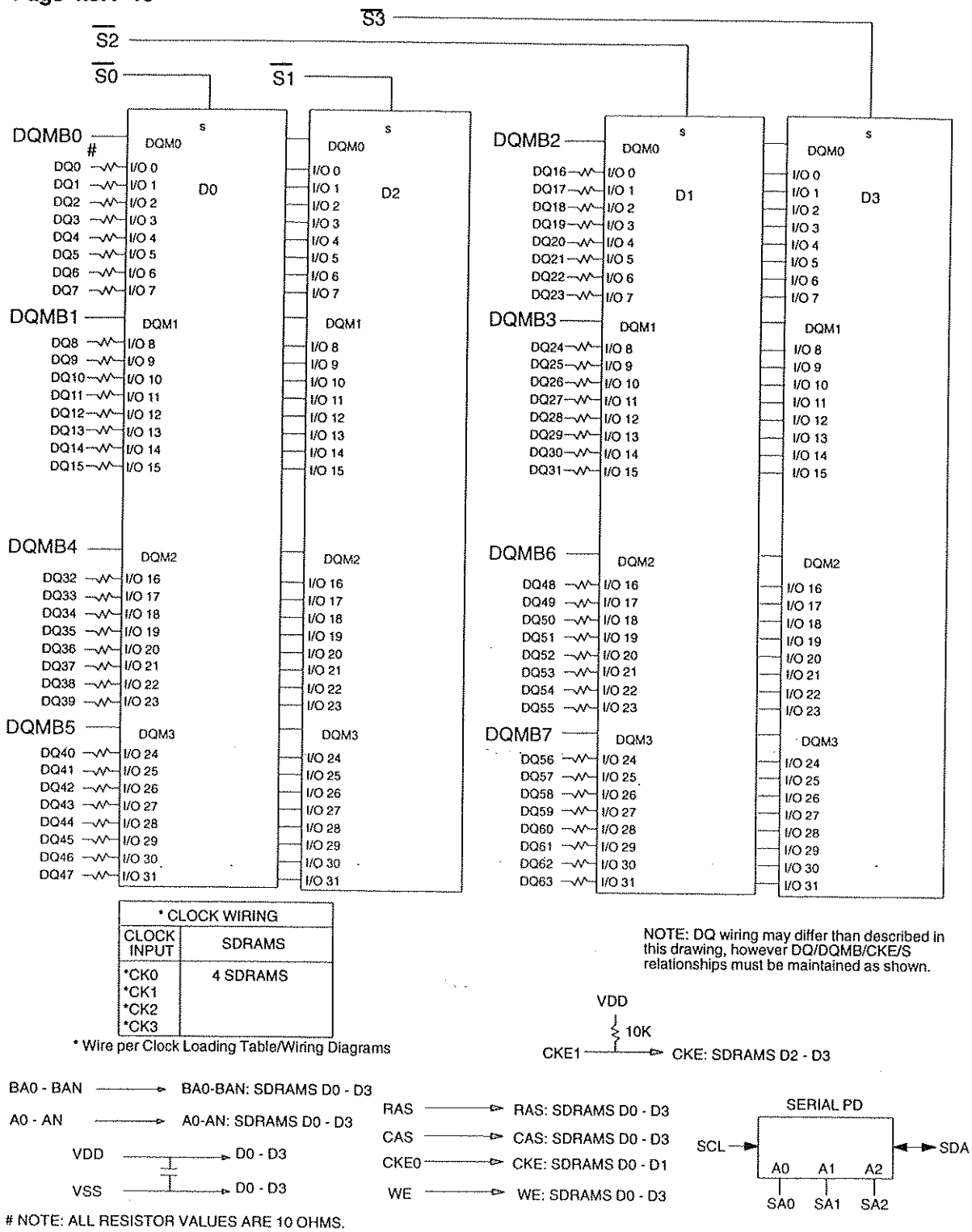


Figure 4.5.4–O
X64 SDRAM DIMM, 2 Banks with X32 SDRAMs

Release 7

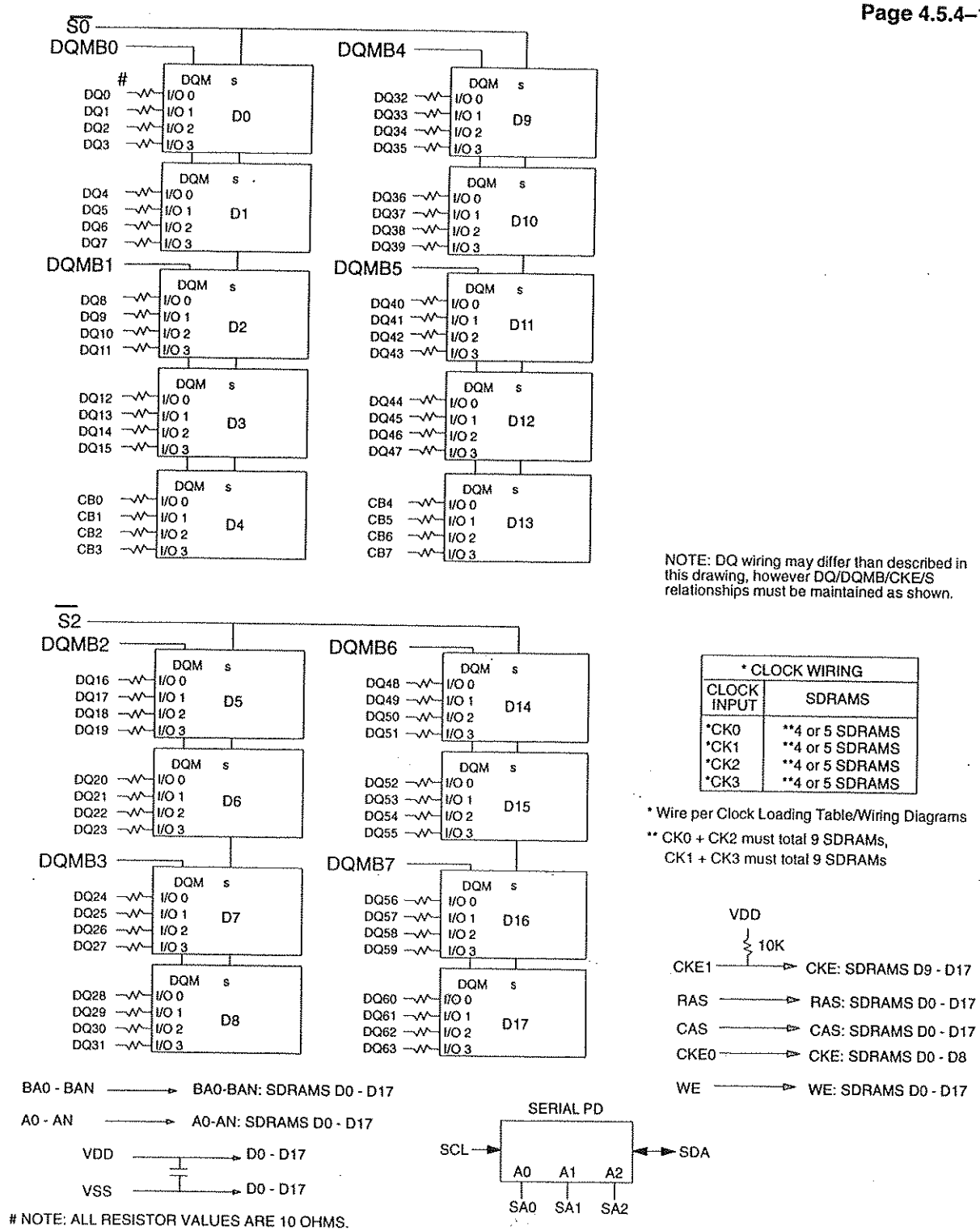
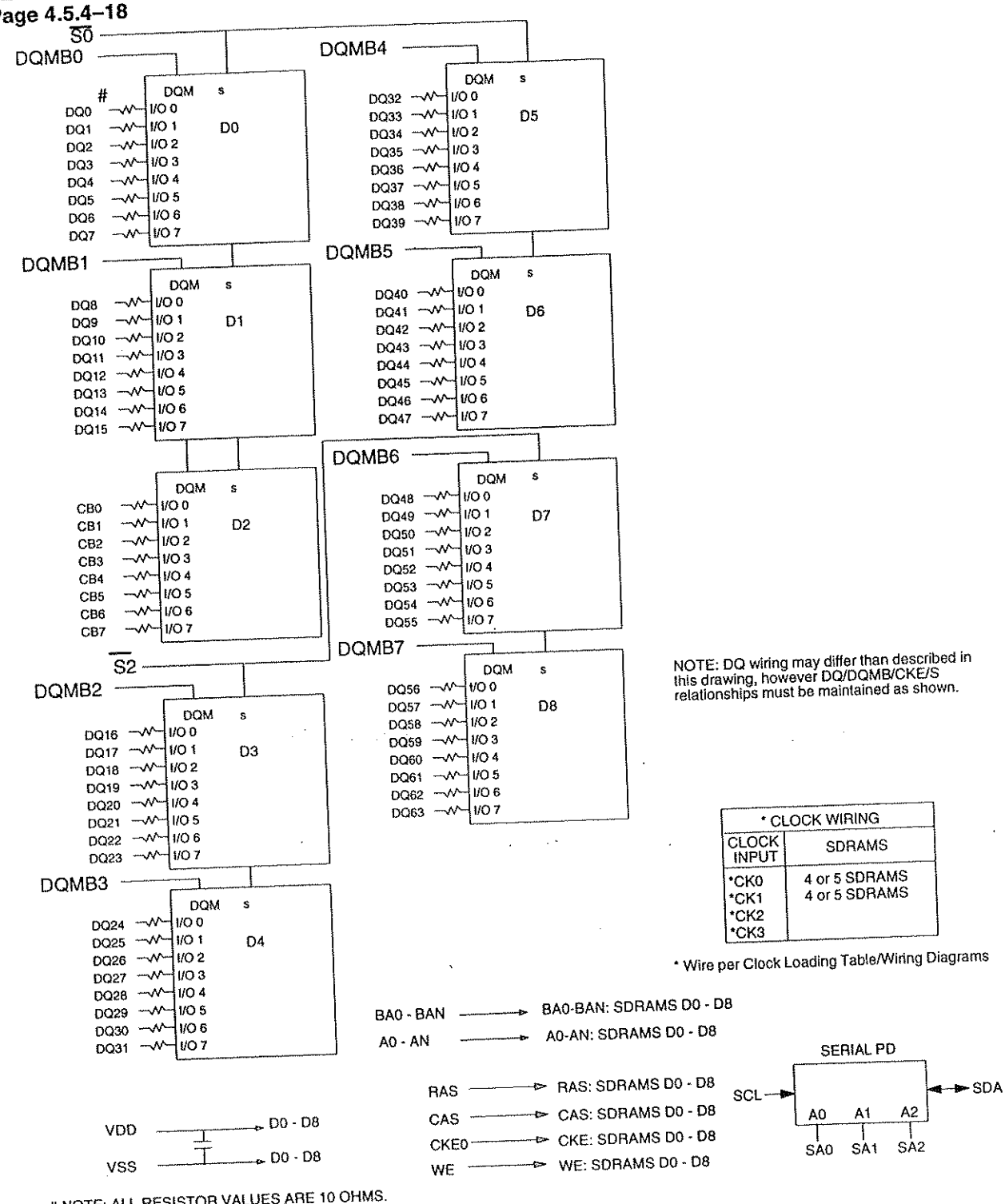


Figure 4.5.4–P
X72 ECC SDRAM DIMM, 1 Banks with X4 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 or 5 SDRAMS
*CK1	4 or 5 SDRAMS
*CK2	
*CK3	

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–Q
X72 ECC SDRAM DIMM, 1 Banks with X8 SDRAMs

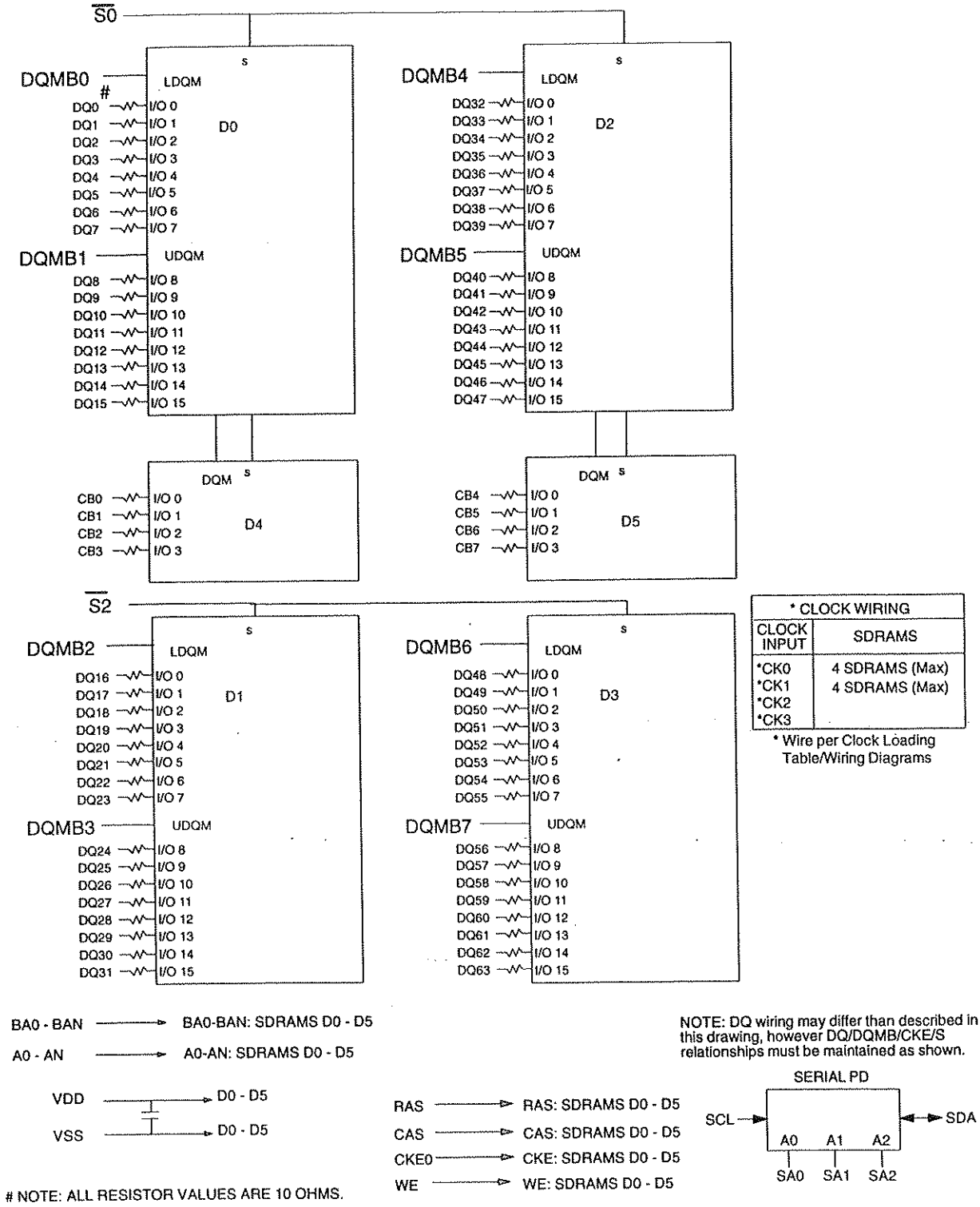


Figure 4.5.4–R
X72 ECC SDRAM DIMM, 1 Bank with X16 & X4 SDRAMs

XILINX EXHIBIT 1010
Page 397

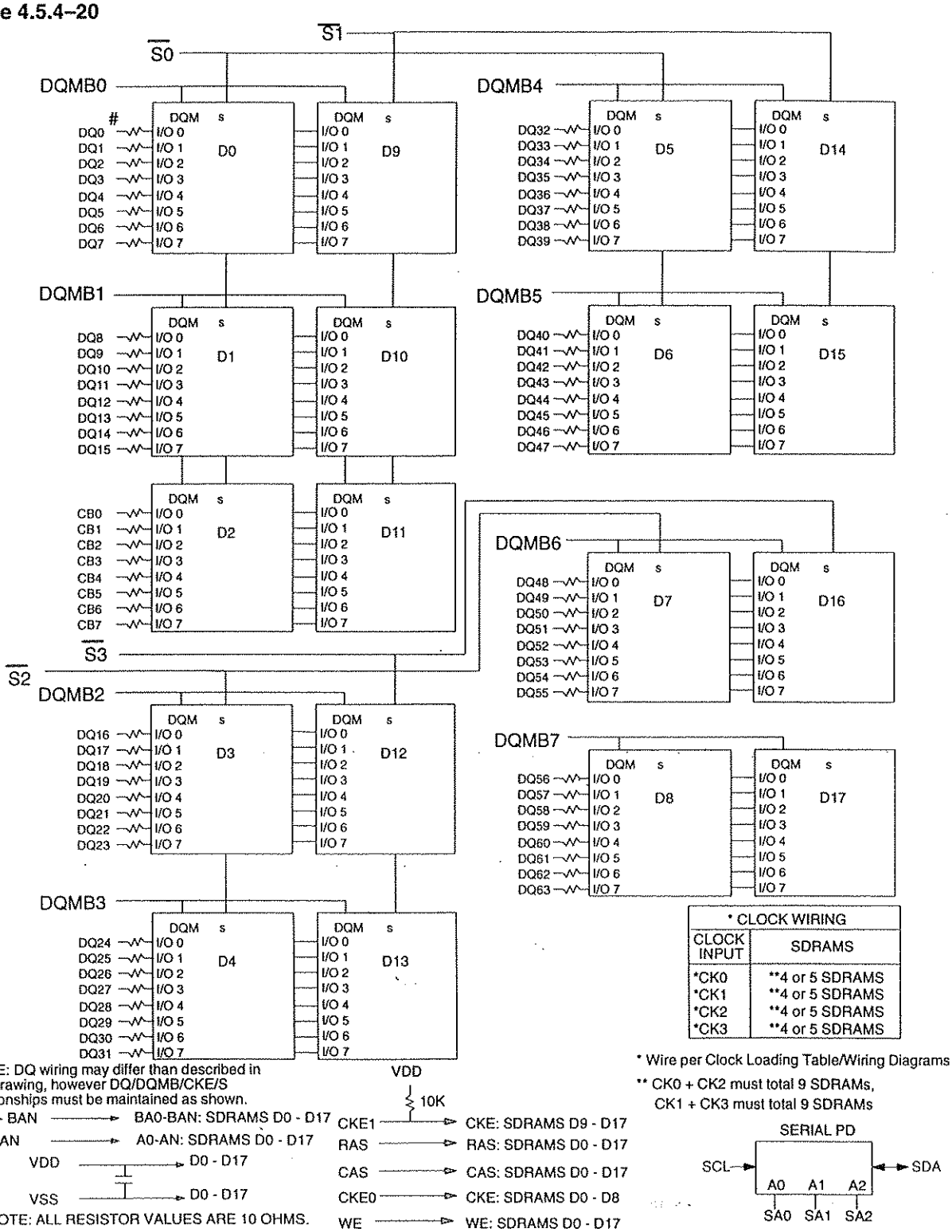


Figure 4.5.4–S
X72 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs

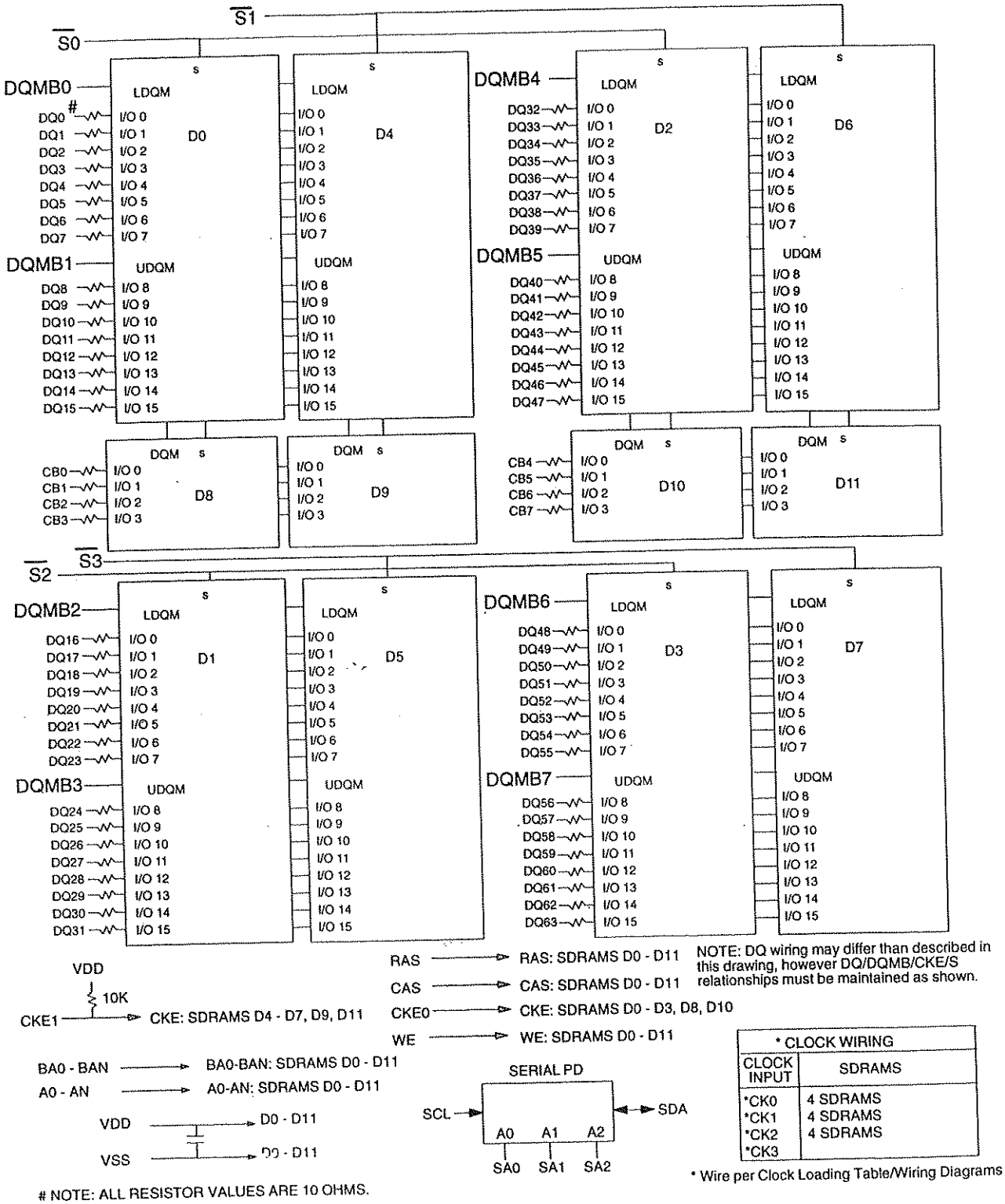


Figure 4.5.4–T
X72 ECC SDRAM DIMM, 2 Banks with X16 & X4 SDRAMs

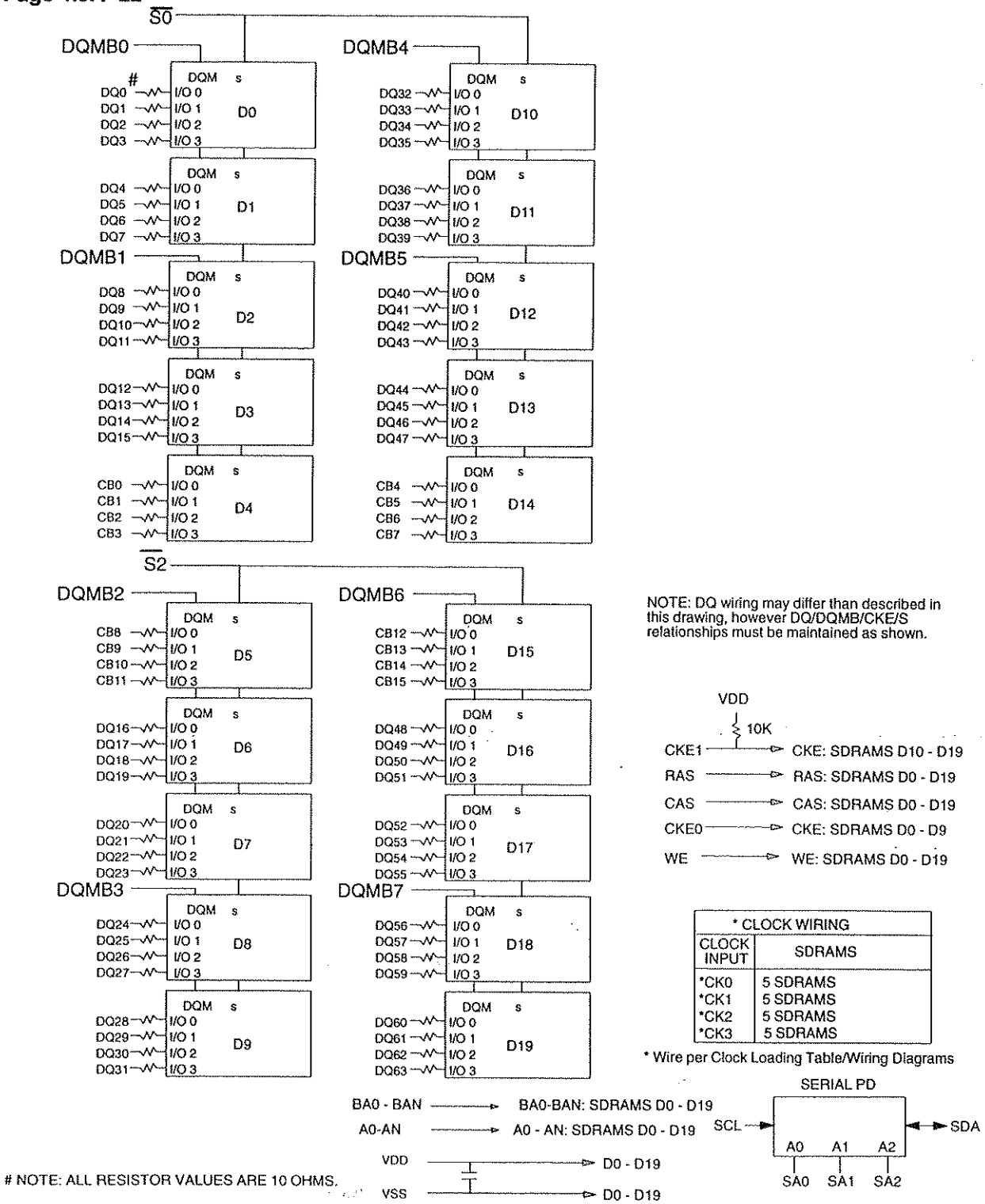


Figure 4.5.4–U
X80 SDRAM DIMM, 1 Bank with X4 SDRAMs

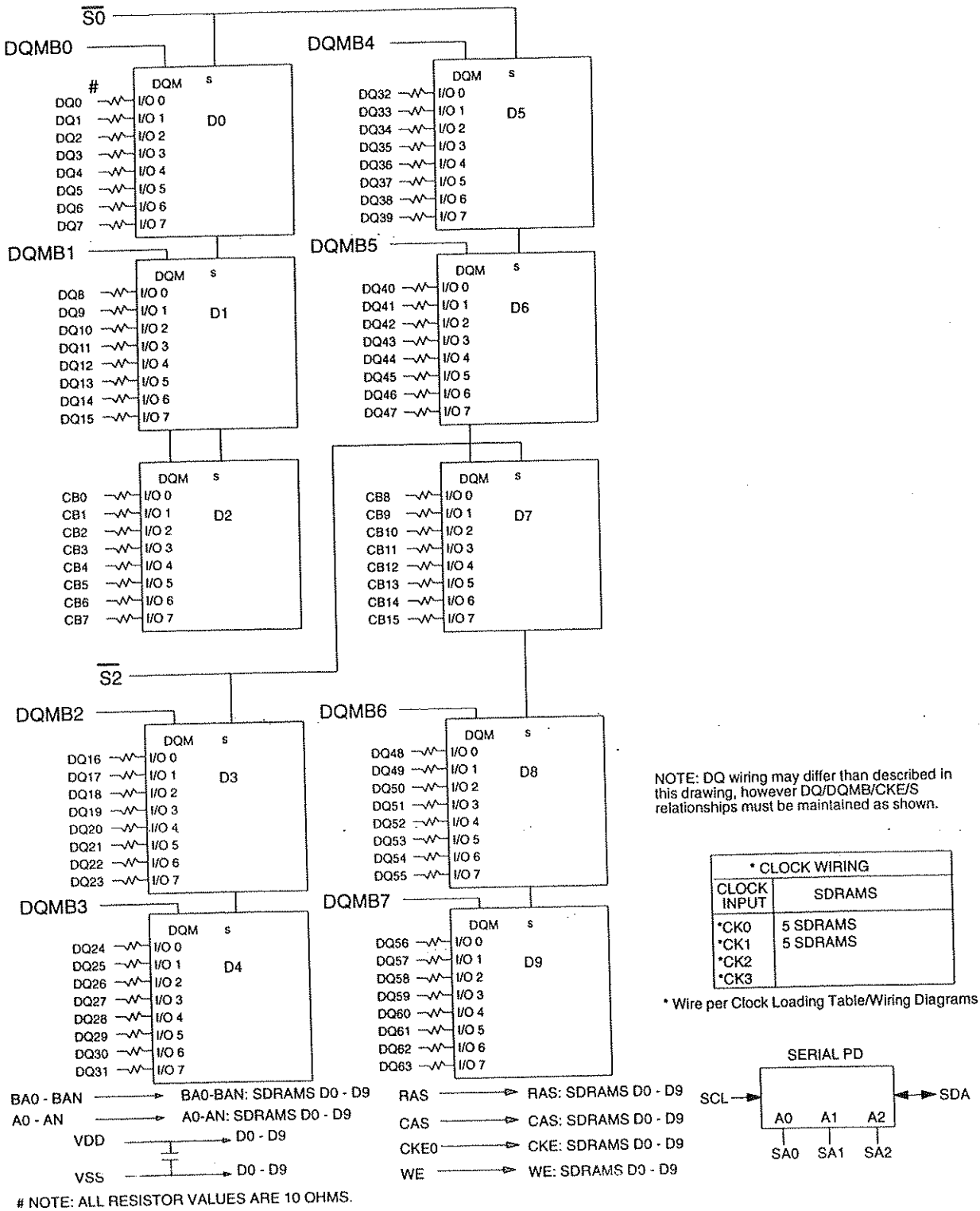


Figure 4.5.4–V
X80 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs

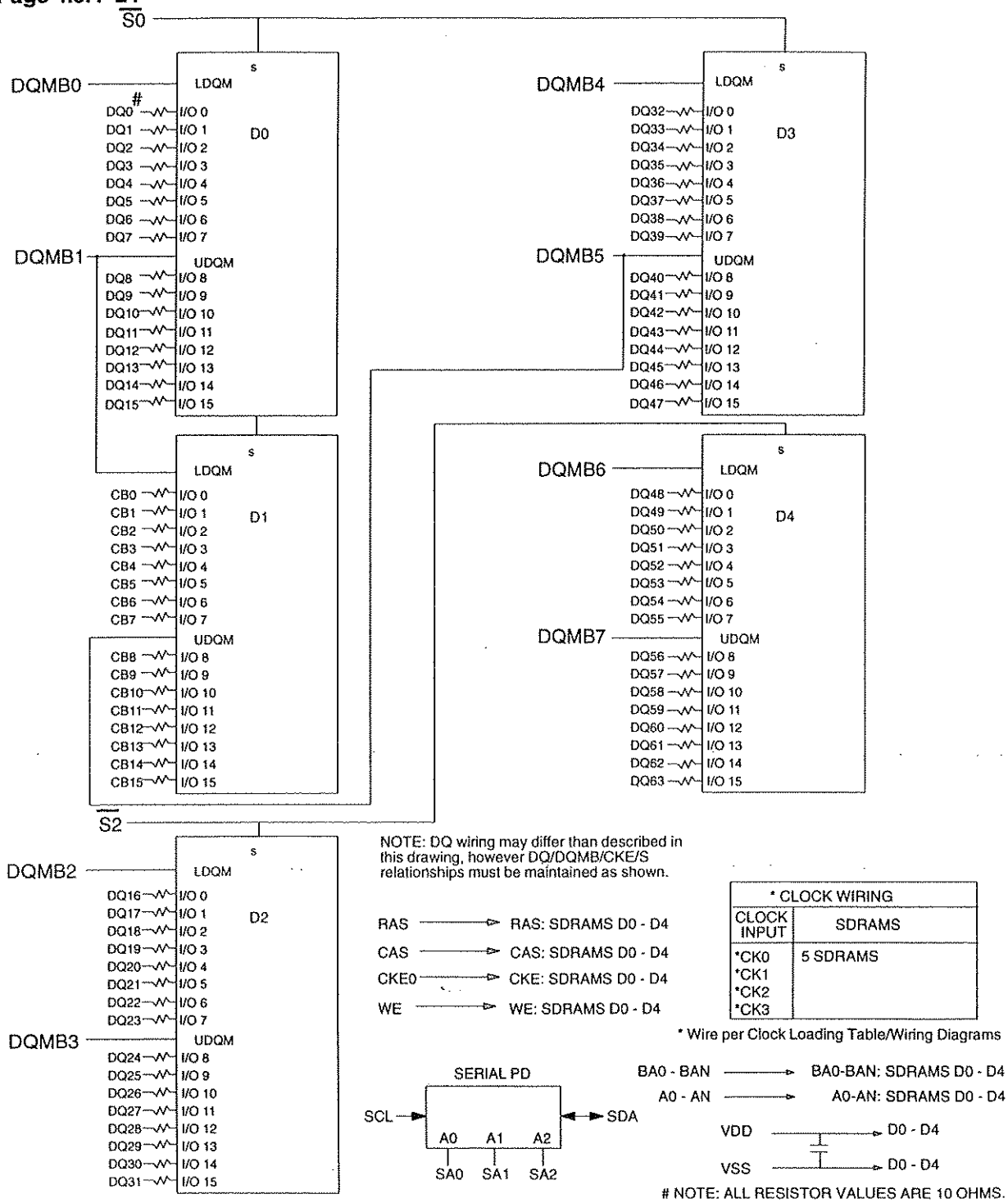


Figure 4.5.4–W
X80 ECC SDRAM DIMM, 1 Bank with X16 SDRAMs

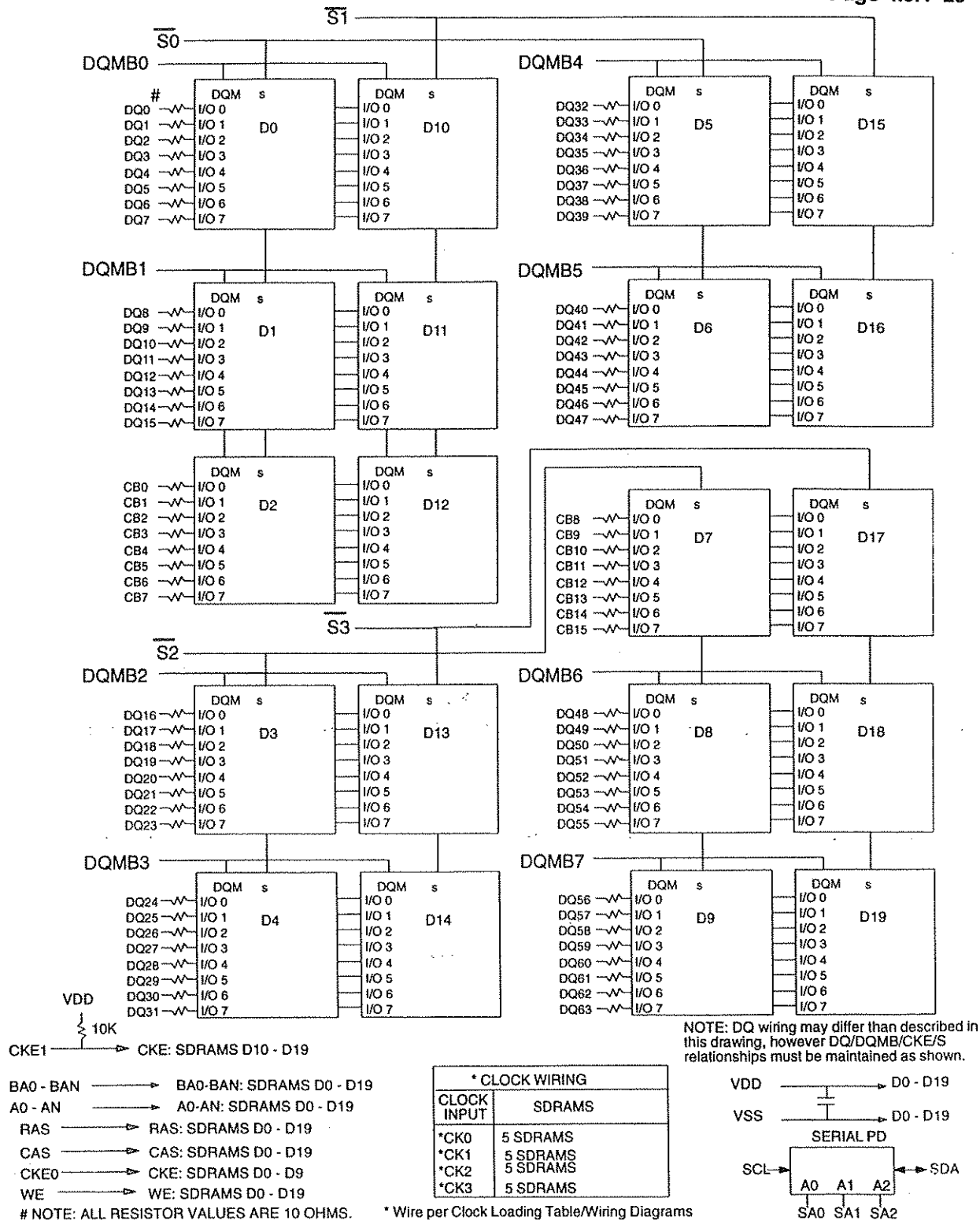


Figure 4.5.4–X
X80 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs

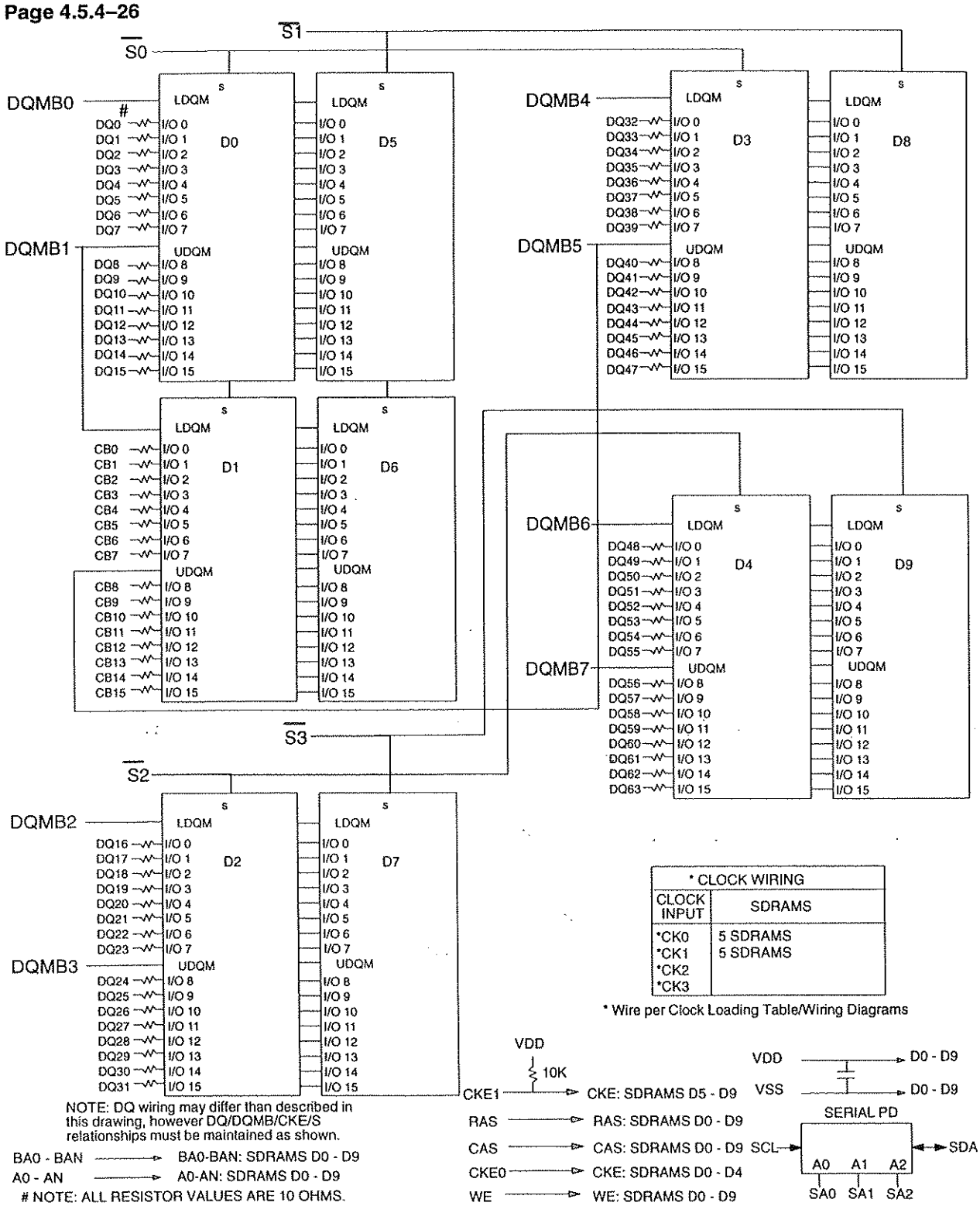


Figure 4.5.4-Y
X80 ECC SDRAM DIMM, 2 Banks with X16 SDRAMs

4.5.5 – 144 PIN DRAM SO–DIMM FAMILY

NOTE: It is recommended that this module be used primarily for main memory applications. At the time this standard was published, the Committee was working on a standard for a Graphics 144 Pin Module to be published in the near future.

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—64 BIT DRAM without PARITY
—72 BIT DRAM for ECC CODES

CONFIGURATION—10 Different Configurations are defined using various combinationa of X4, X8, and X16 DRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that consist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.5.5–A & 4.5.5–B

MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.5–C

TECHNOLOGY COMPARISON TABLE — Fig. 4.5.5–D

DRAM SPD INFORMATOION — Fig. 4.5.5–E

X64 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5–F through 4.5.5–J

X72 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5–K through 4.5.5–O

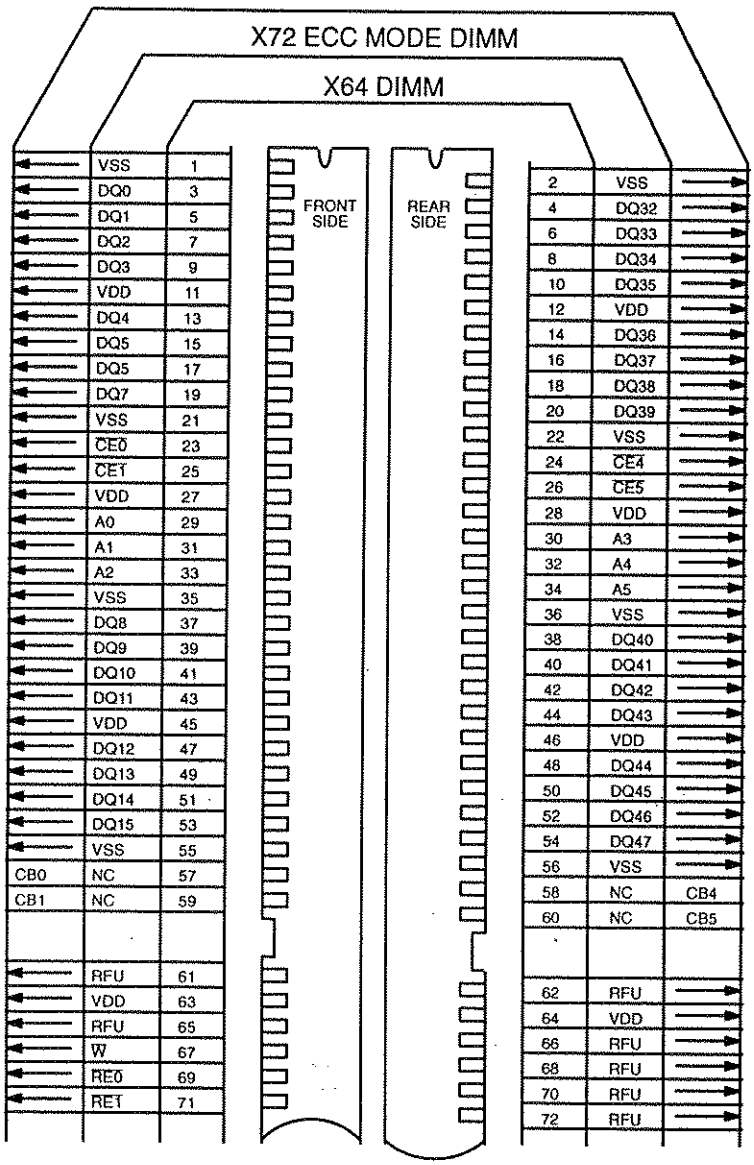


Figure 4.5.5–A
144 Pin X64 & X72 DRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF

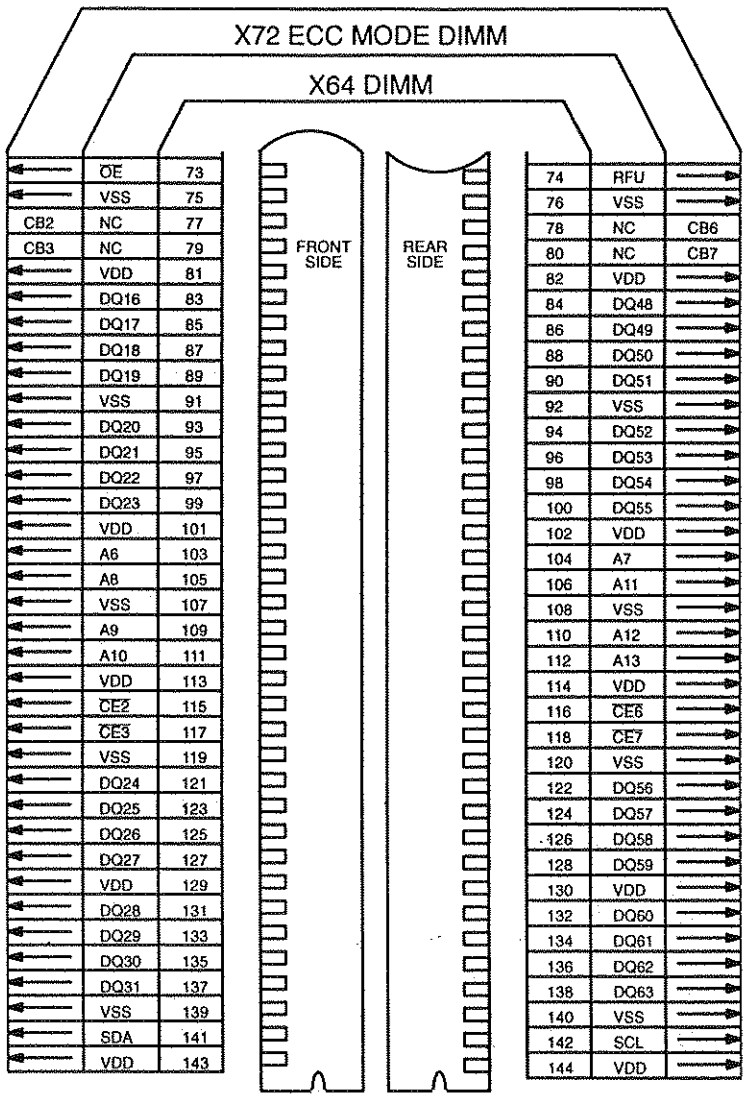


Figure 4.5.5–B
144 Pin X64 & X72 DRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

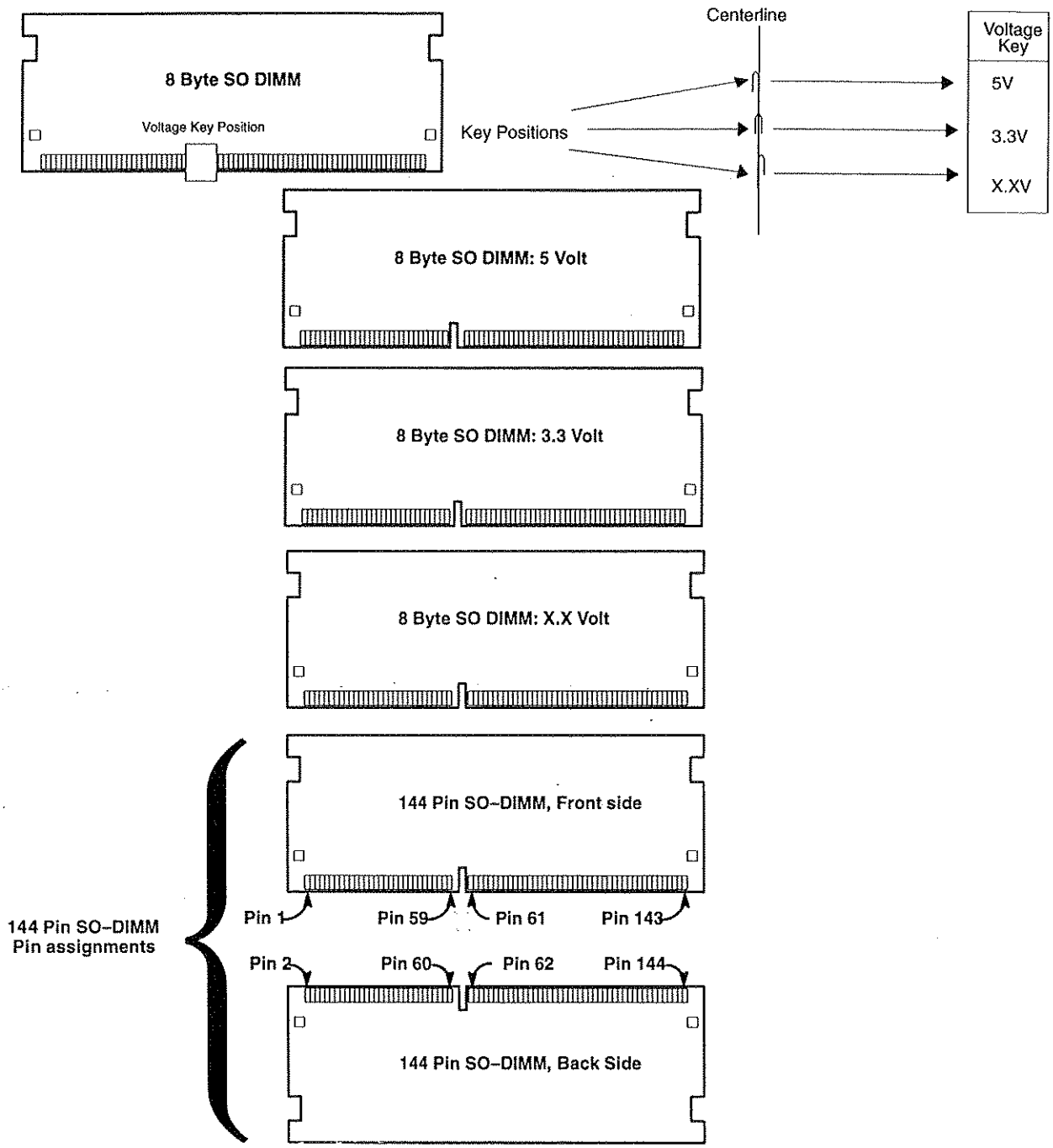


Figure 4.5.5–C
144 Pin SO–DRAM DIMM Keying Methodology

Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{CAS0}$	DQMB0
25	$\overline{CAS1}$	DQMB1
61	DU	CK0
65	DU	$\overline{RAS}$
69	$\overline{RAS0}$	$\overline{S0}$
71	$\overline{RAS1}$	$\overline{S1}$
73	$\overline{OE}$	DU
111	A10	A10/AP
115	$\overline{CAS2}$	DQMB2
117	$\overline{CAS3}$	DQMB3
24	$\overline{CAS4}$	DQMB4
26	$\overline{CAS5}$	DQMB5
62	DU	CKE0
66	DU	$\overline{CAS}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{CAS6}$	DQMB6
118	$\overline{CAS7}$	DQMB7

Figure 4.5.5–D
Pinout Comparison, 144 Pin DRAM & SDRAM SO–DIMM

8 Byte DRAM SO–DIMM PD Information

- Serial PD Interface Protocol: I^2C (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:
  a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
512K x 64/72	512K x 8	10	9				
1M x 64/72	512K x 8	10	9				
1M x 64/72	1M x 4/16	10	10	12	8		
2M x 64/72	1M x 16	10	10	12	8		
2M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	4M x 4/16	11	11	12	10	*13	9
8M x 64/72	4M x 16	11	11	12	10	*13	9
8M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	16M x 4/16	12	12	13	11	*14	10
32M x 64/72	16M x 16	12	12	13	11	*14	10
32M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	64M x 4	13	13	14	12		
(Note: All options possible with DRAM standards are shown) * This addressing option applies to x16 DRAM configuration							

  b. Allowable configurations: (Byte 11)
     - x64 (Non-parity, Byte controls)
     - x72 (ECC-optimized, Byte controls)
  c. Functional Attributes:
     - Power Supply Voltage/Interface levels (Byte 8)
     - $\overline{RAS}$ access (Byte 9)
     - $\overline{CAS}$ access (Byte 10)
     - Refresh rate/type (Byte 12)

For Detailed Serial PD Byte data see section 4–?–?, DRAM Serial Presence Detect Definitions.

1. Serial PD interface is standard I^2C architecture
2. Pull-up resistors (4.7K typical value) are required on all open drain/open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA source (I_{OL} max) must be at least 3ma to maintain a valid "low level".
4. I^2C Bus specification:

Figure 4.5.5–E
144 Pin X64 DRAM SO–DIMM, SPD TABLE AND INFORMATION

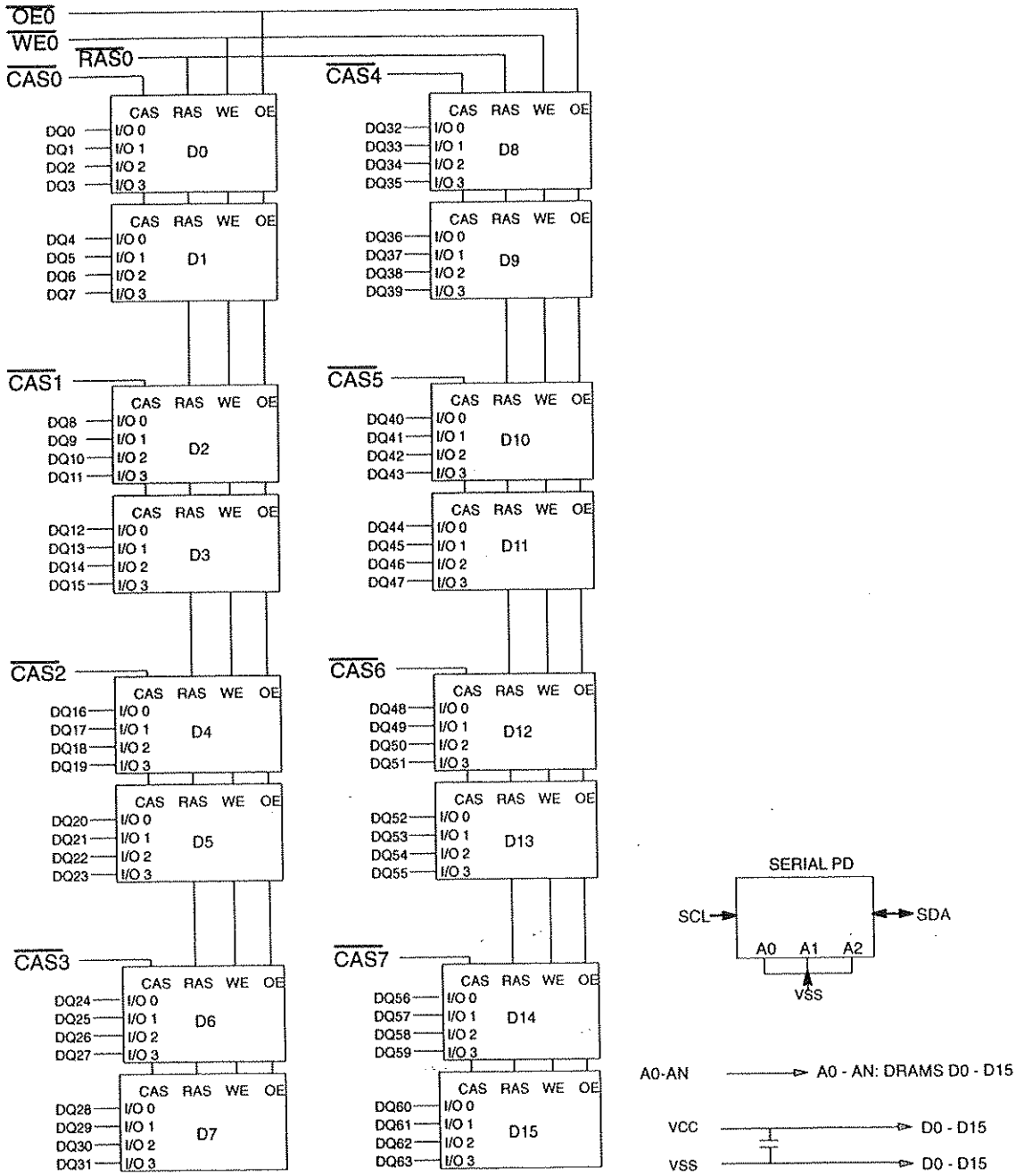


Figure 4.5.5–F
144 Pin X64 DRAM SO–DIMM, 1 Bank with X4 DRAMs

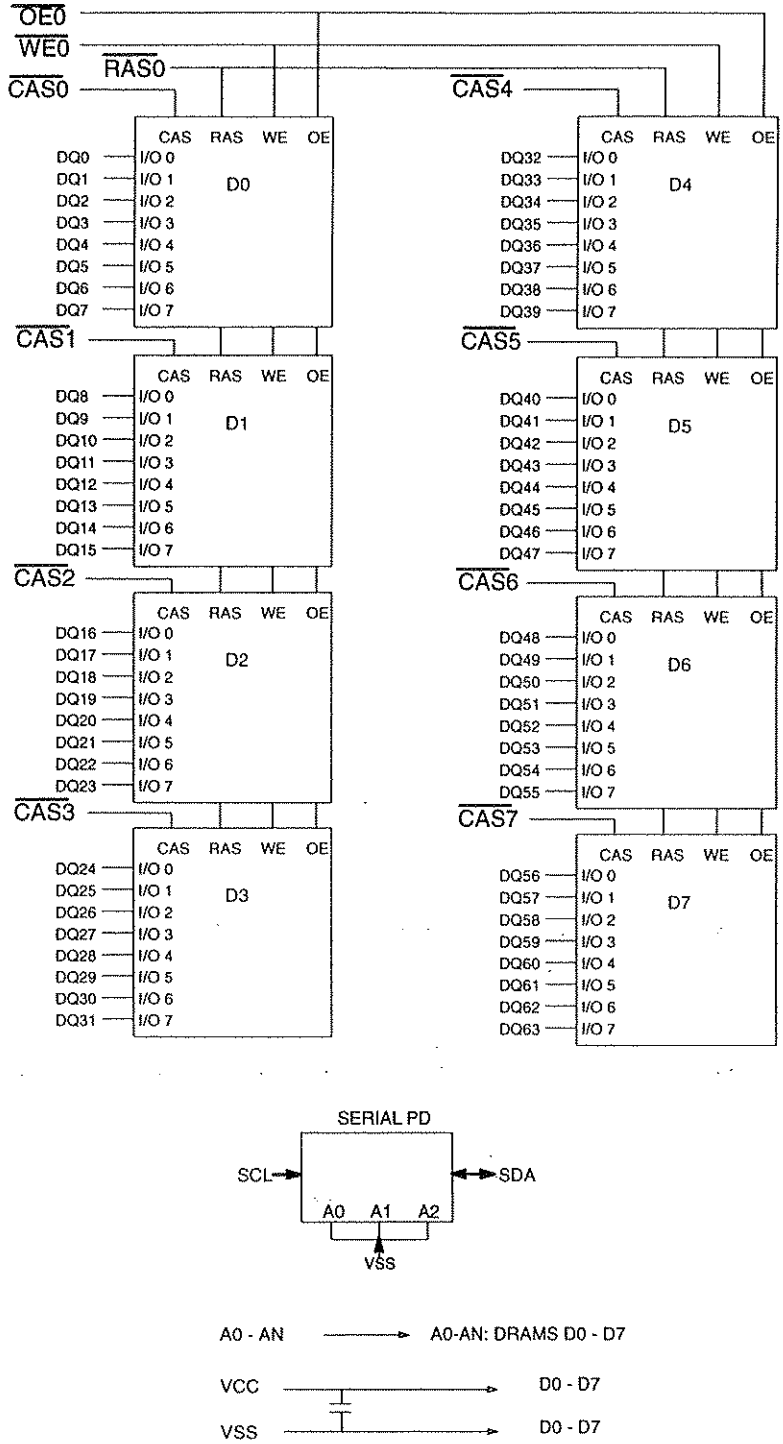


Figure 4.5.5–G
144 Pin X64 DRAM SO–DIMM, 1 Bank with X8 DRAMs

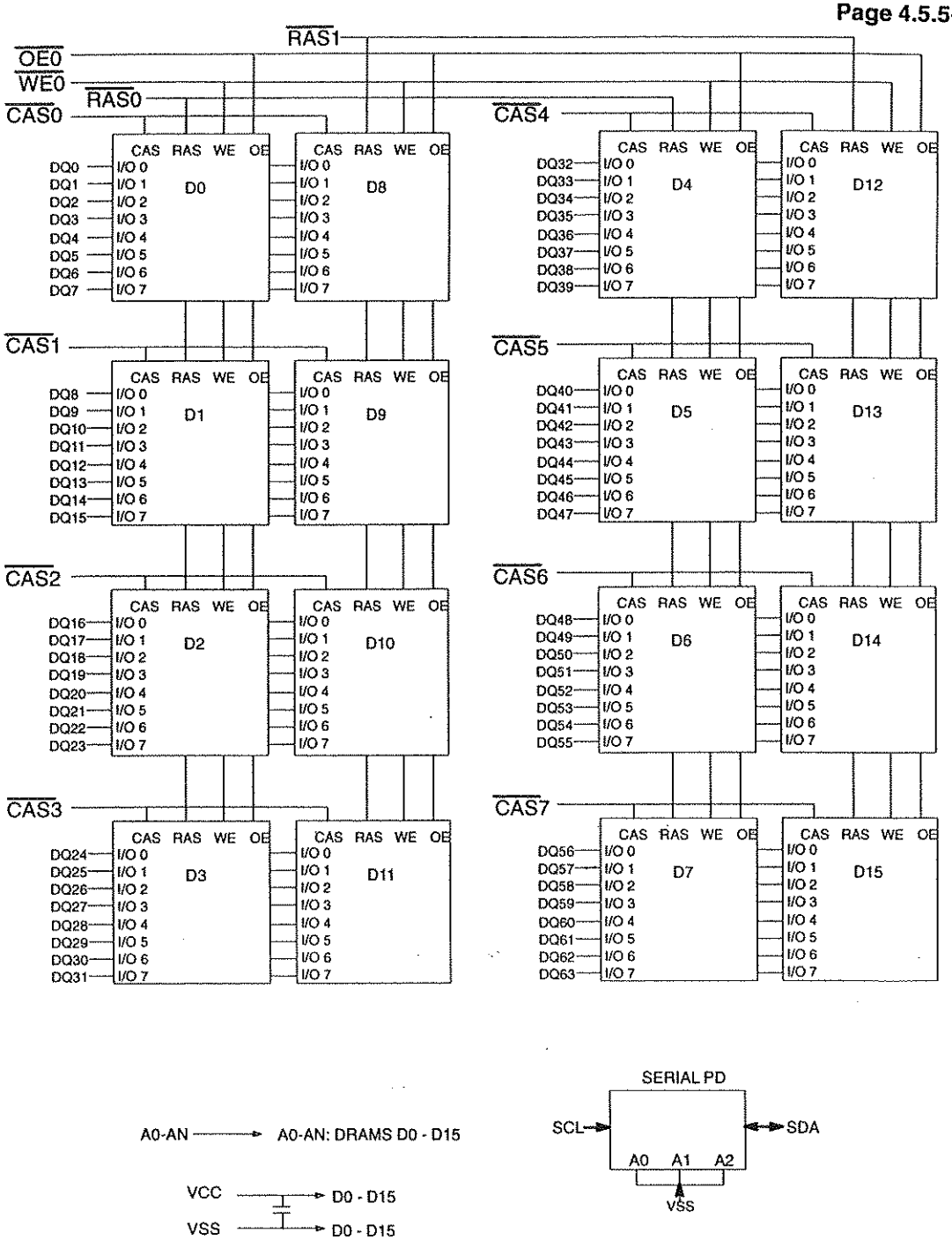


Figure 4.5.5–H
144 Pin X64 DRAM SO–DIMM, 2 Bank with X8 DRAMs

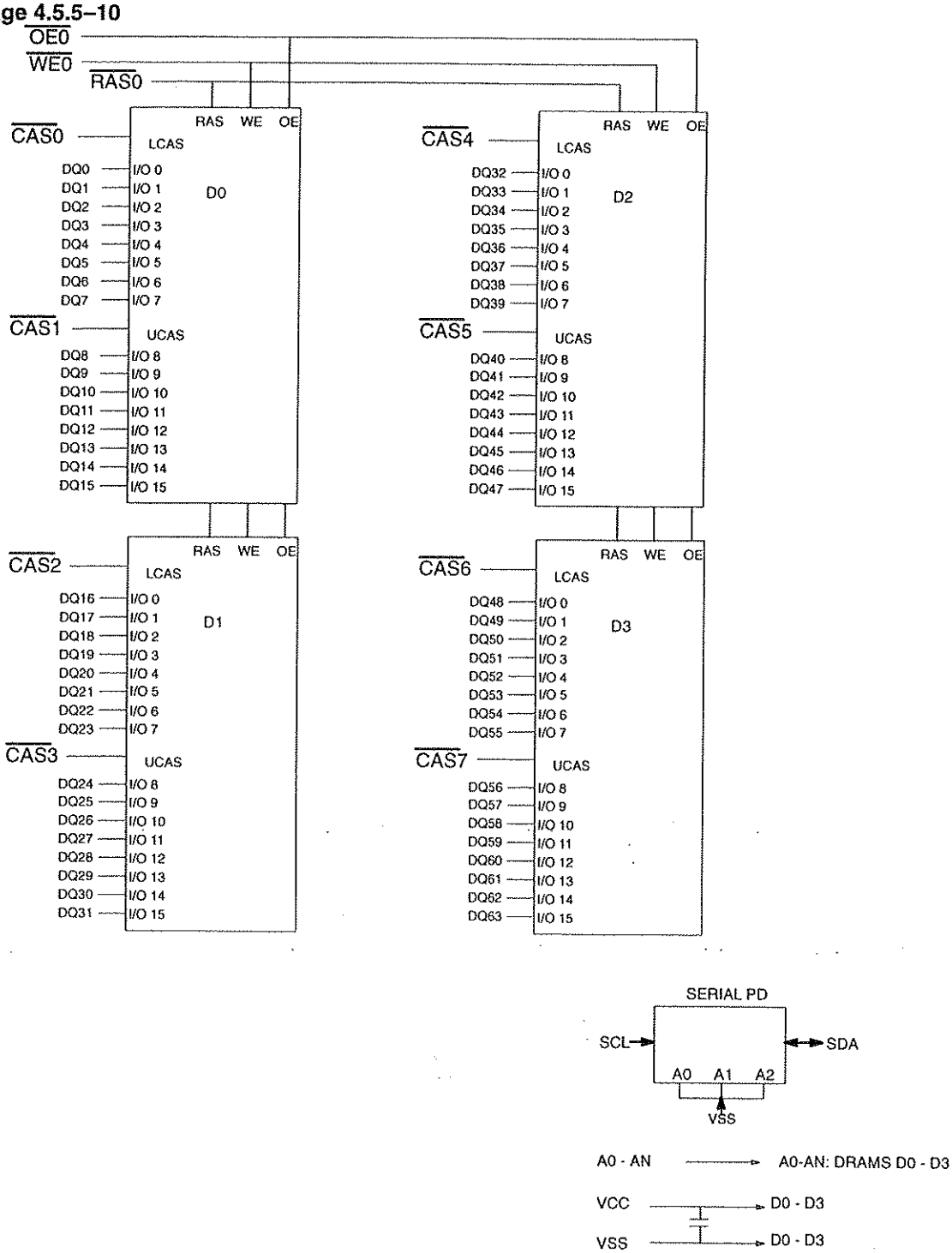


Figure 4.5.5–I
144 Pin X64 DRAM SO–DIMM, 1 Bank with X16 DRAMs

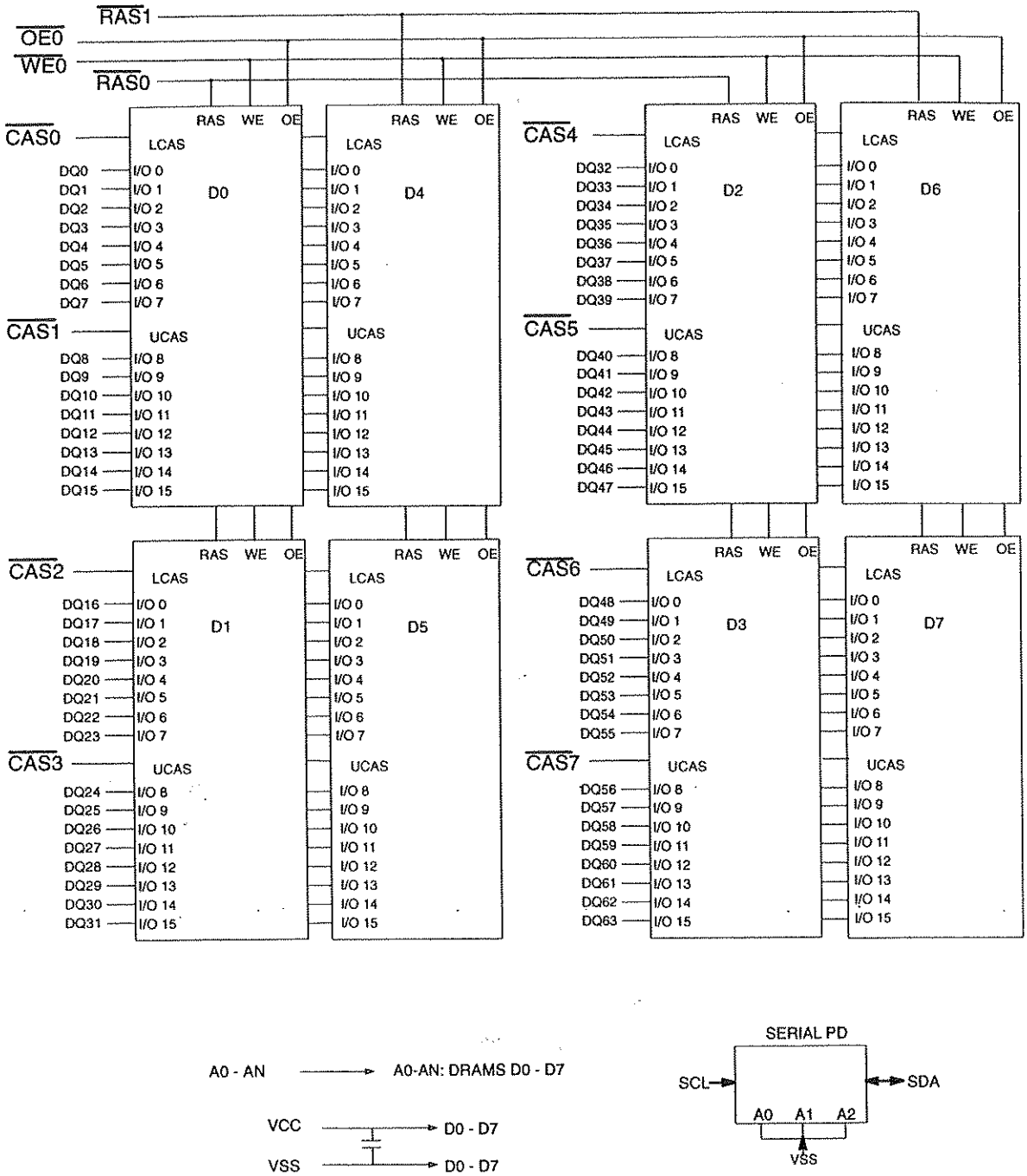


Figure 4.5.5–J
144 Pin X64 DRAM SO–DIMM, 2 Bank with X16 DRAMs

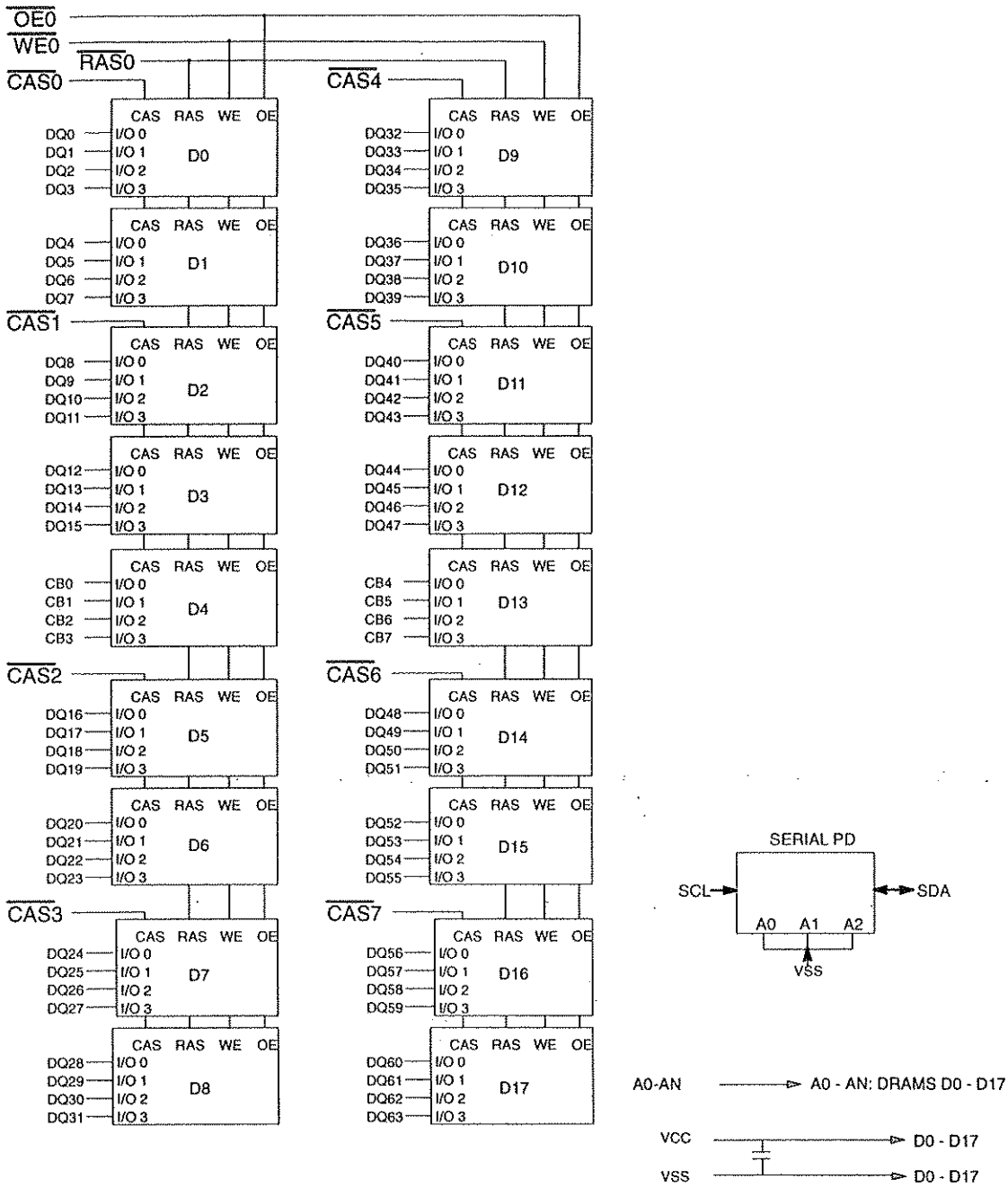


Figure 4.5.5–K
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X4 DRAMs

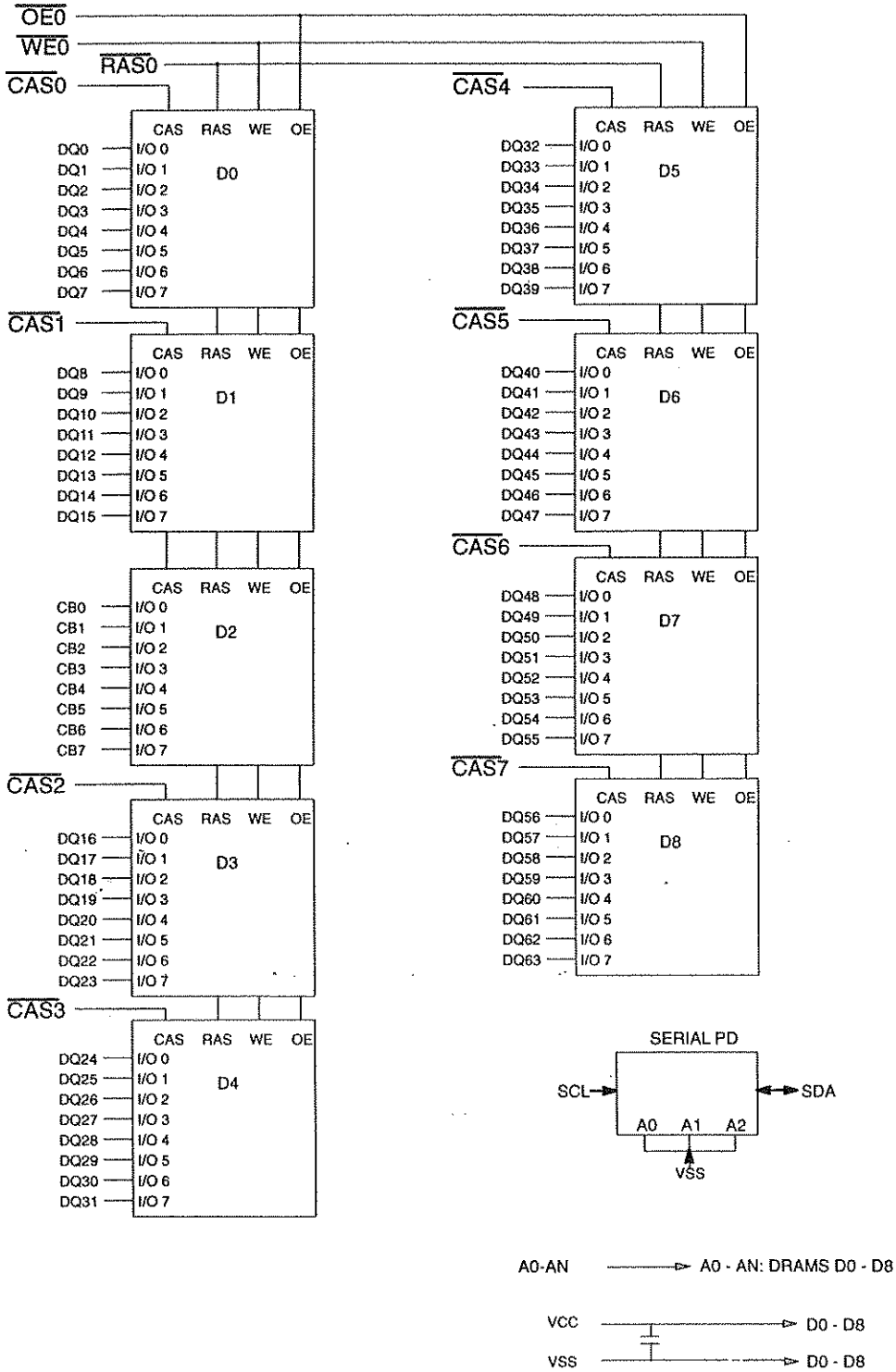


Figure 4.5.5–L
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X8 DRAMs

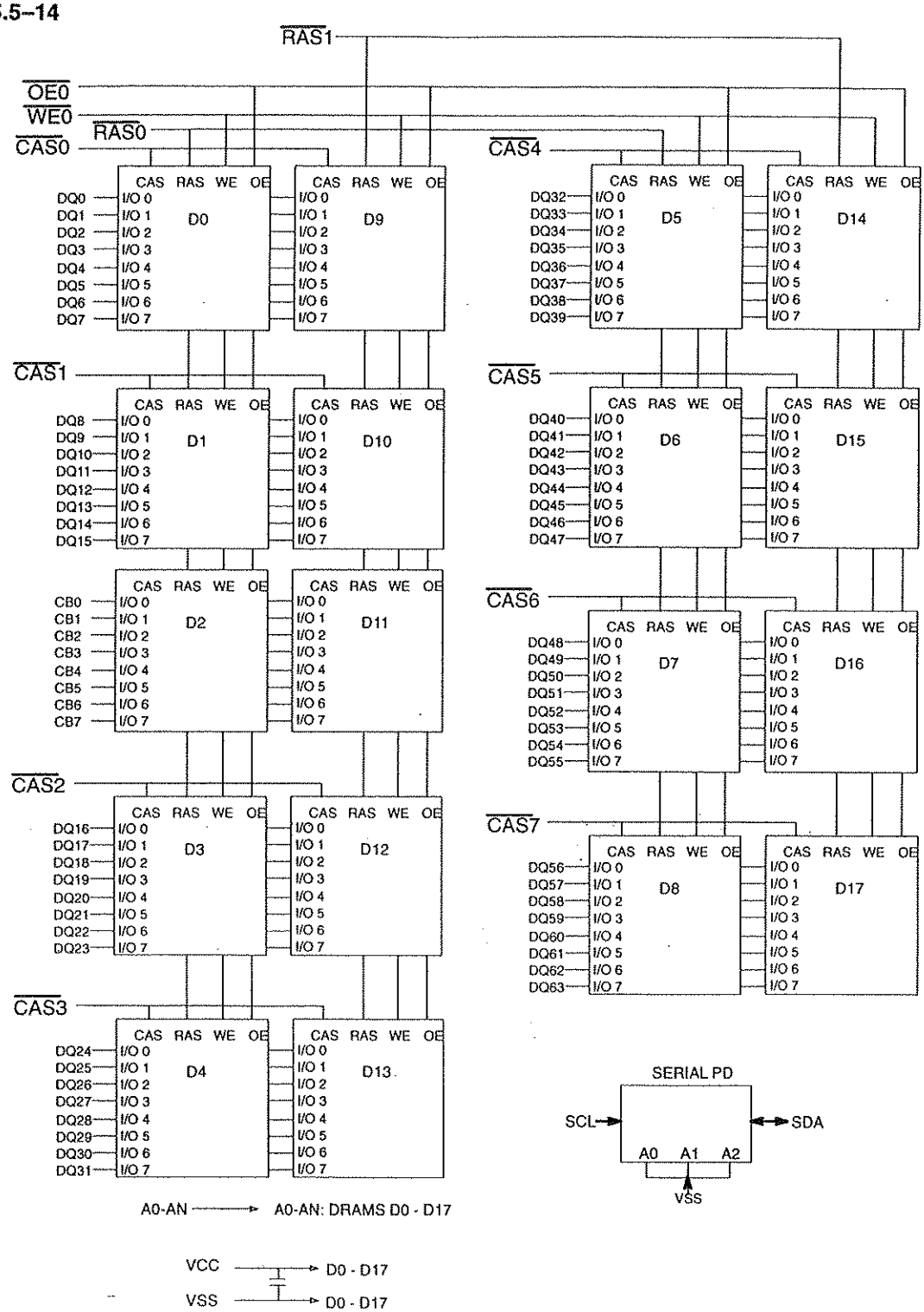


Figure 4.5.5–M
144 Pin X72 ECC DRAM SO–DIMM, 2 Bank with X8 DRAMs

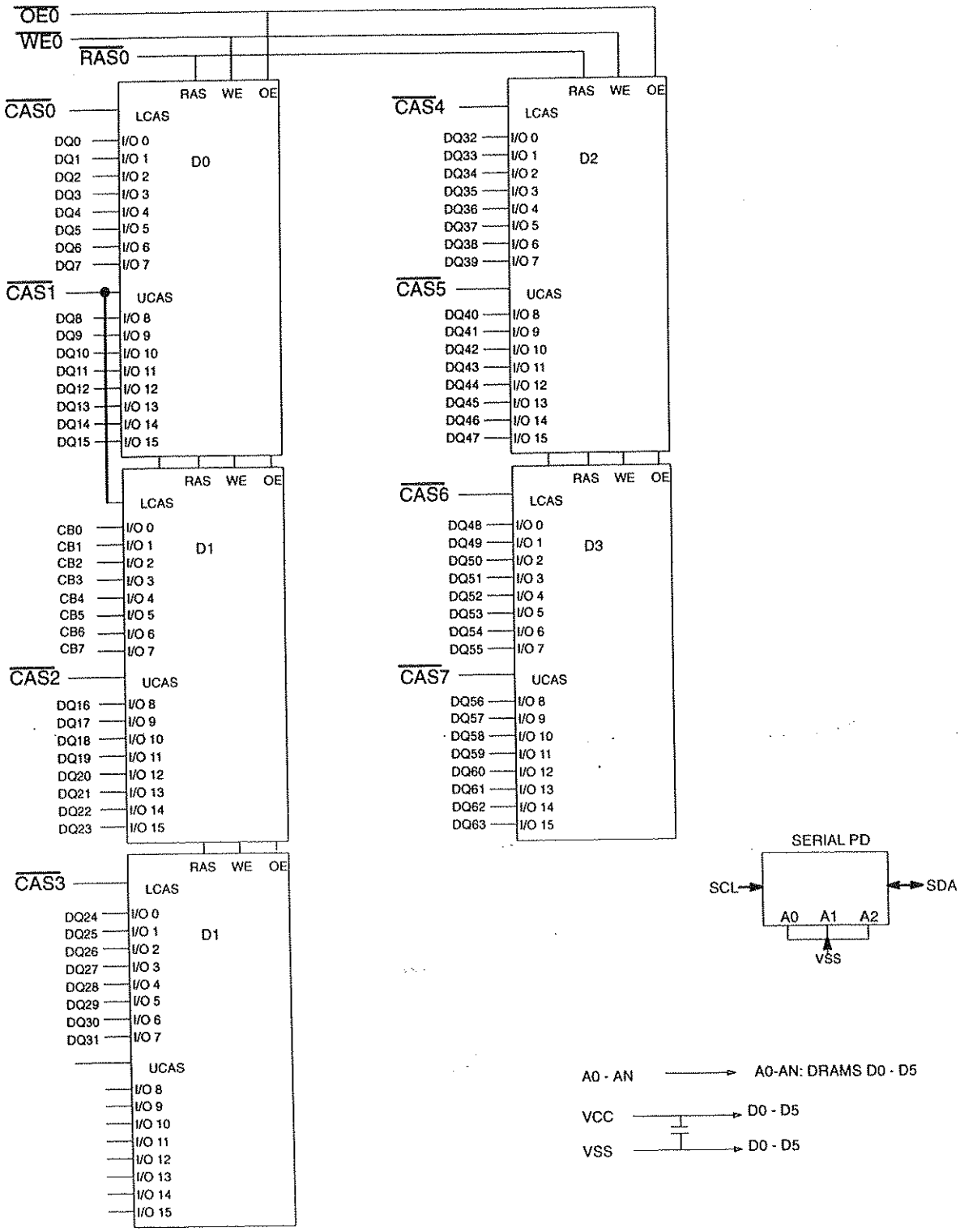


Figure 4.5.5–N
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X16 DRAMs

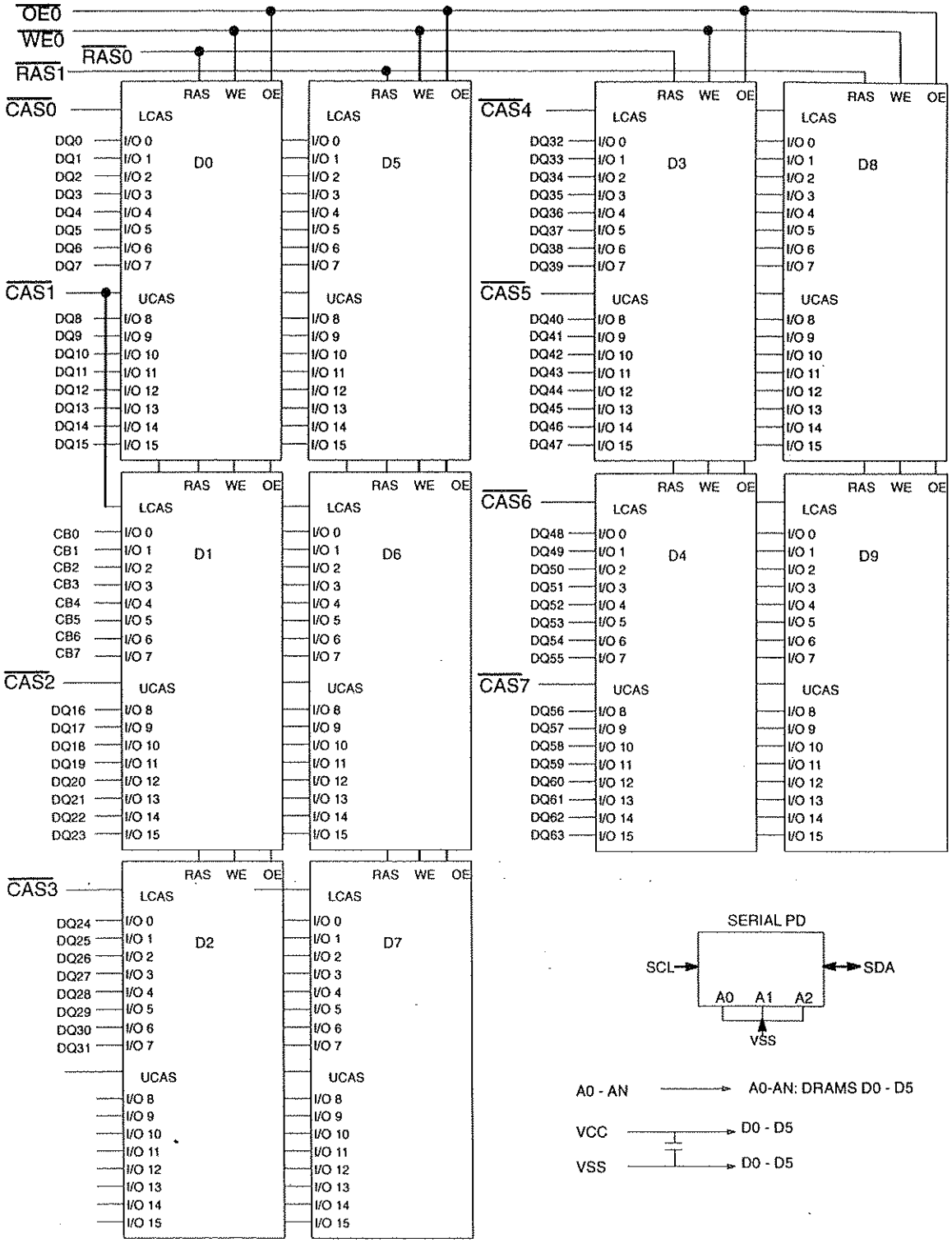


Figure 4.5.5–O
144 Pin X72 ECC DRAM SO–DIMM, 2 Bank with X16 DRAMs

4.5.6 – 144 PIN SDRAM SO–DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.
DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—64 BIT SDRAM without PARITY
—72 BIT SDRAM for ECC CODES
CONFIGURATION—10 Different Configurations are defined using various combinationa of X4, X8, and X16 SDRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.5.6–A & 4.5.6–B
SDRAM SPD INFORMATOION — Fig. 4.5.6–C
MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.6–D
TECHNOLOGY COMPARISON TABLE — Fig. 4.5.6–E
SDRAM CLOCK LOADING & WIRING—Figs. 4.5.6–F
X64 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6–G through 4.5.6–L
X72 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6–M through 4.5.6–P

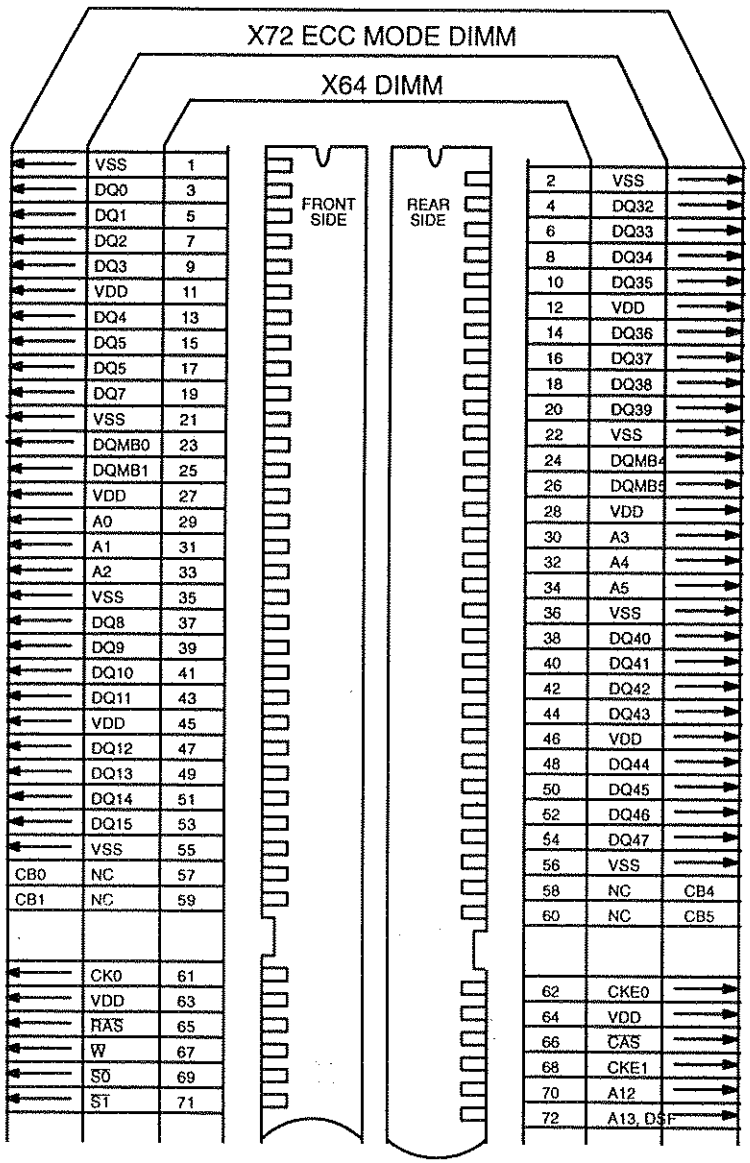


Figure 4.5.6–A
144 Pin X64 & X72 SDRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF

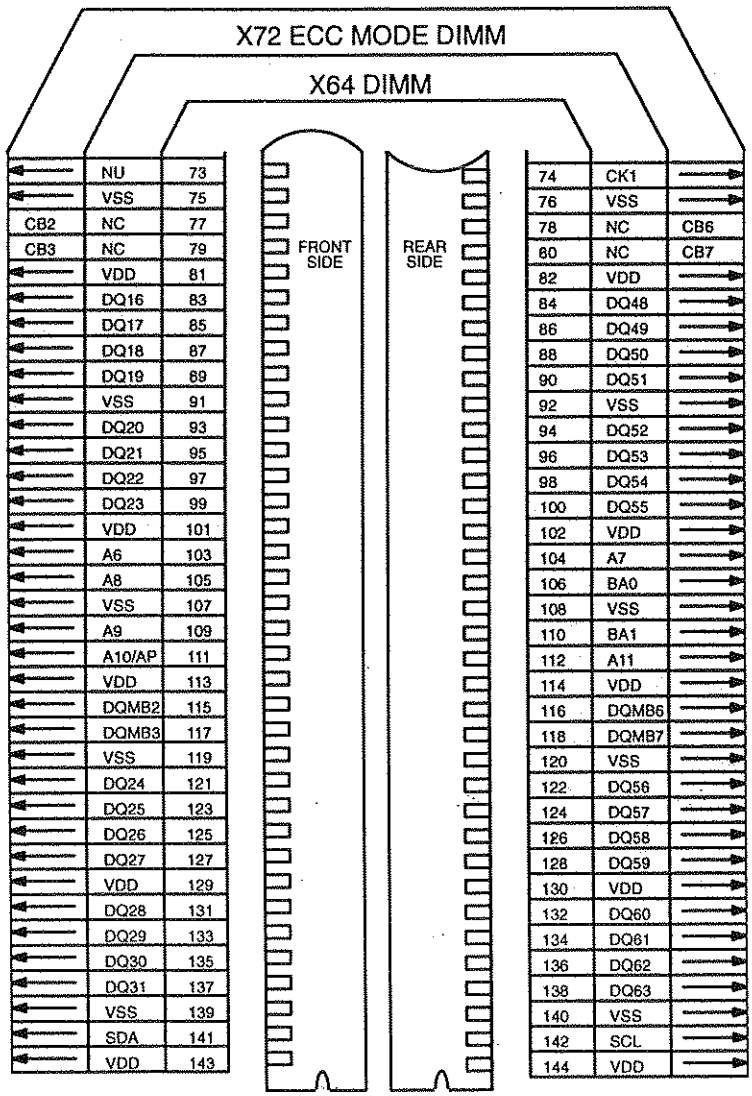


Figure 4.5.6–B
144 Pin X64 & X72 SDRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.
1M x 64/72	1M x 16	1	11	8						
2M x 64/72	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72	2M x 8	1	11	9						
4M x 64/72	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72	16M x 16	2	13	9						
32M x 64/72	16M x 16	2	13	9						
32M x 64/72	32M x 8	2	13	10						
64M x 64/72	32M x 8	2	13	10						
(Note: All options possible with SDRAM standards are shown)										

b. Allowable configurations: (Byte 11)
   - x64 (Non-parity, Byte controls)
   - x72 (ECC-optimized, Byte controls)

c. Functional Attributes:
   - Power Supply Voltage/Interface levels (Byte 8)
   - SDRAM cycle time (Byte 9)
   - SDRAM access from Clock (Byte 10)
   - Refresh rate/type (Byte 12)
   - SDRAM module attributes (Byte 13)
   - SDRAM device attributes (Bytes 14 - 20)
   - Primary/Secondary SDRAM (Bytes 21 - 22)

Figure 4.5.6–C
144 Pin SDRAM SO–DIMM, PD INFORMATION

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

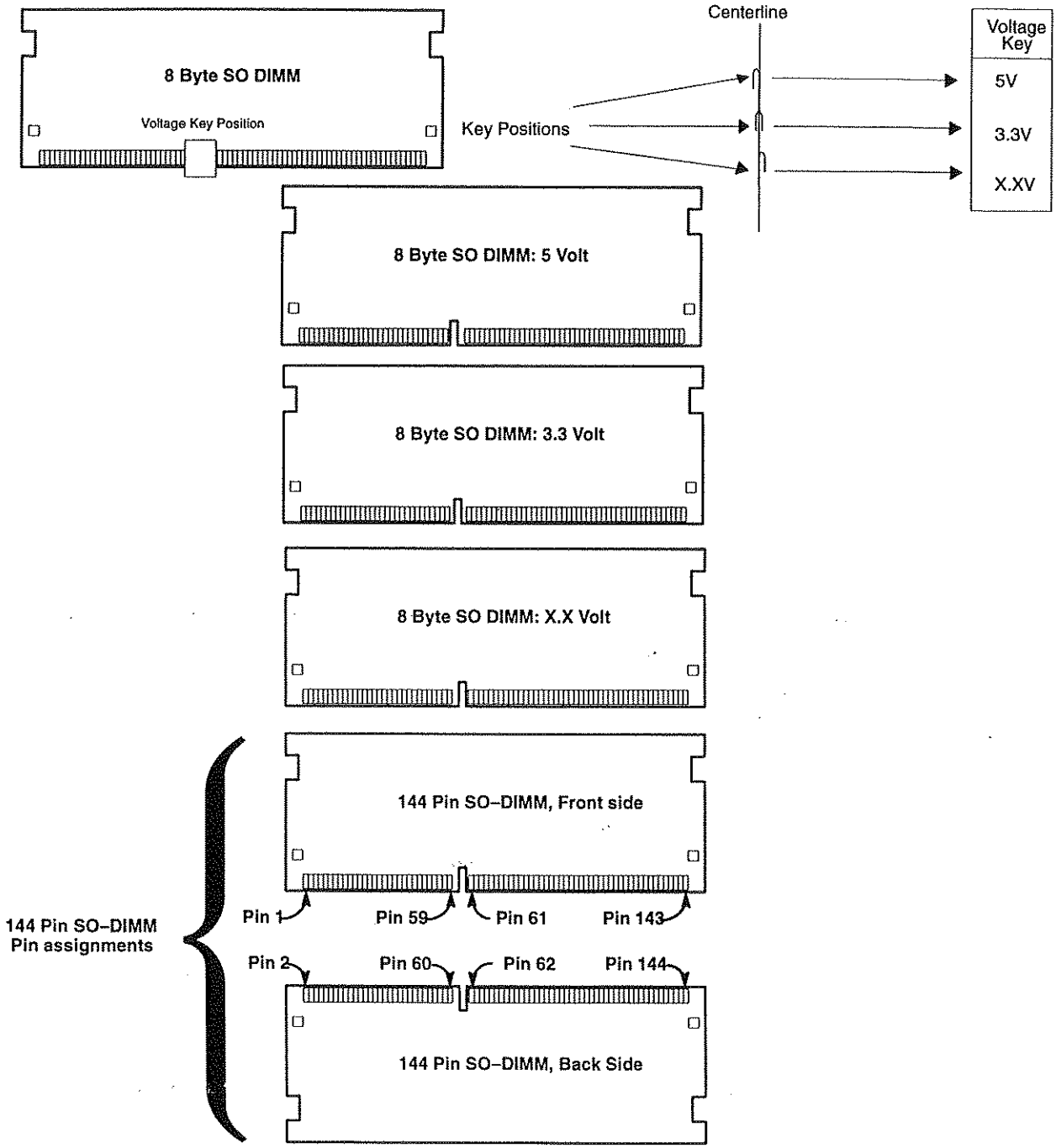


Figure 4.5.6–D
144 Pin SDRAM DIMM Keying Methodology

Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{CAS0}$	DQMB0
25	$\overline{CAS1}$	DQMB1
61	DU	CK0
65	DU	$\overline{RAS}$
69	$\overline{RAS0}$	$\overline{S0}$
71	$\overline{RAS1}$	$\overline{S1}$
73	$\overline{OE}$	DU
111	A10	A10/AP
115	$\overline{CAS2}$	DQMB2
117	$\overline{CAS3}$	DQMB3
24	$\overline{CAS4}$	DQMB4
26	$\overline{CAS5}$	DQMB5
62	DU	CKE0
66	DU	$\overline{CAS}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{CAS6}$	DQMB6
118	$\overline{CAS7}$	DQMB7

FIGURE 4.5.6–E
Pinout Comparison, 144 Pin DRAM & SDRAM SO–DIMM

XILINX EXHIBIT 1010
Page 426

Configuration	CK0	CK1
x8 (1 bank)	4	4
x16 (1 bank)	4	*
x8 (2 bank)	*1 (PLL)	*
x16 (2 bank)	4	4

Configuration	CK0	CK1
x8 (1 bank)	*4 OR 5	*4 OR 5
x16/x4 (1 bank)	*4 (MAX)	*4 (MAX)
x8 (2 bank)	*1 (PLL)	*
x16/x4 (2 bank)	*1 (PLL)	*

- add padding capacitance per clock wiring diagram.

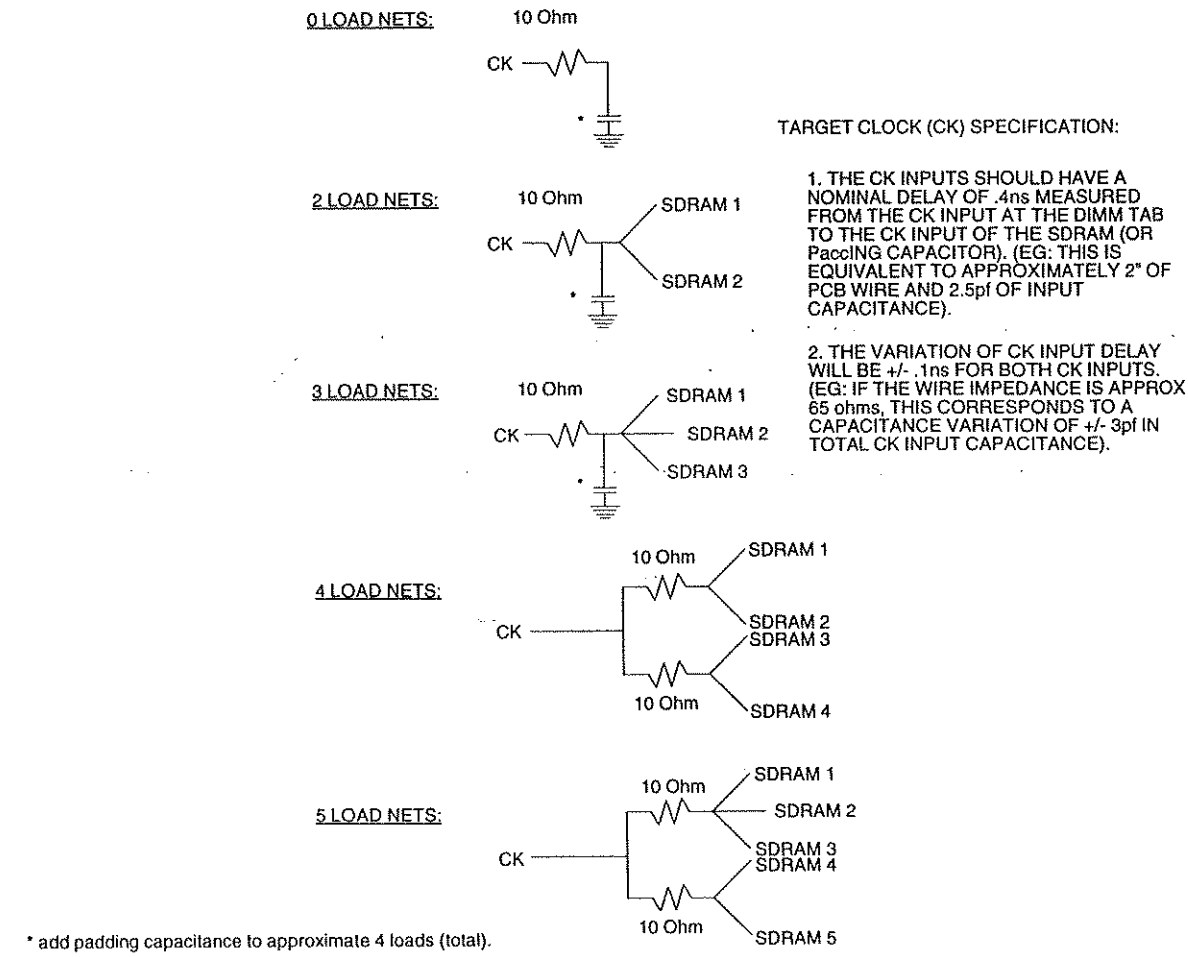
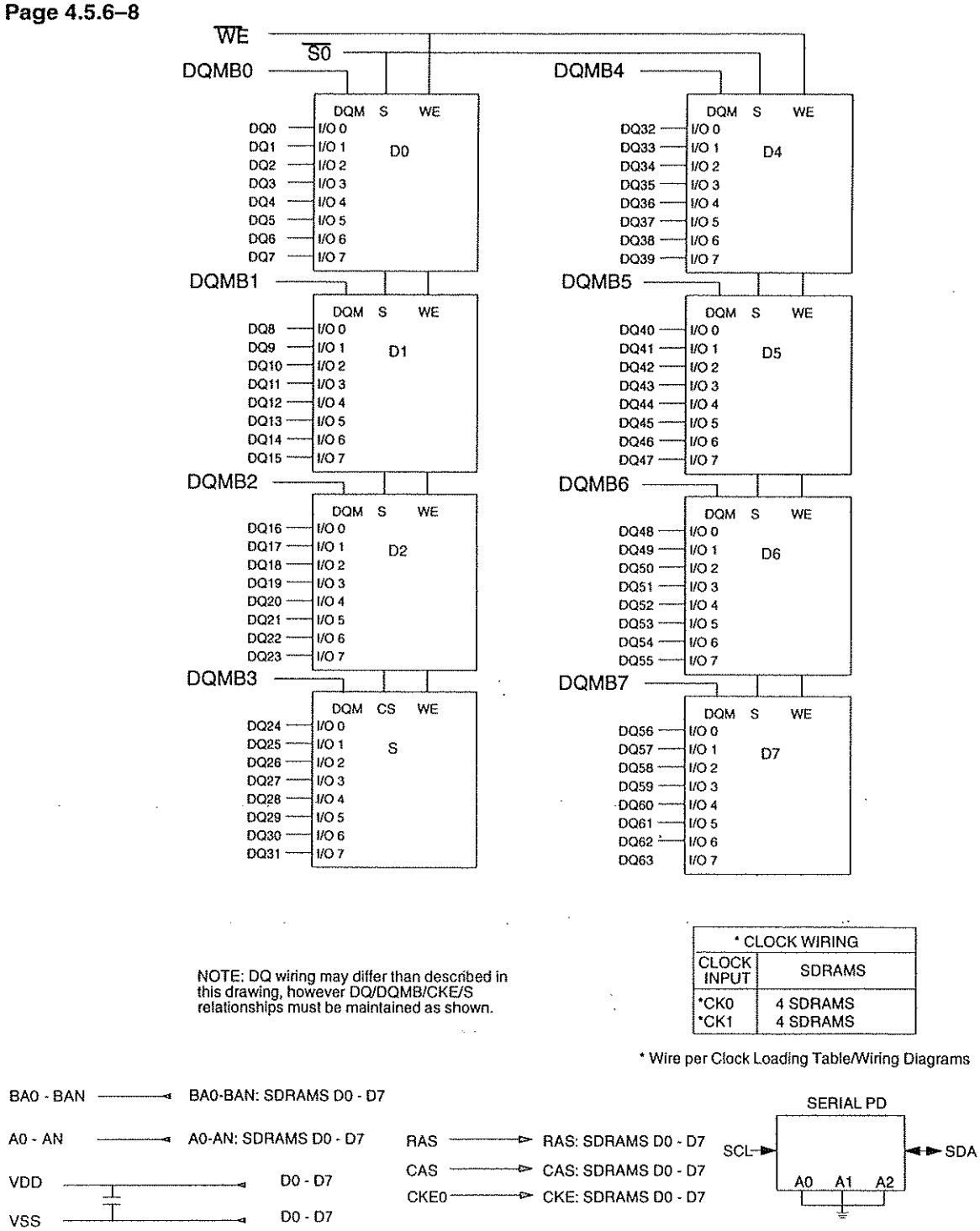


Figure 4.5.6–F
144 Pin SDRAM SO–DIMM, CLOCK LOADING AND WIRING

Release 7



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–G
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X8 SDRAMs

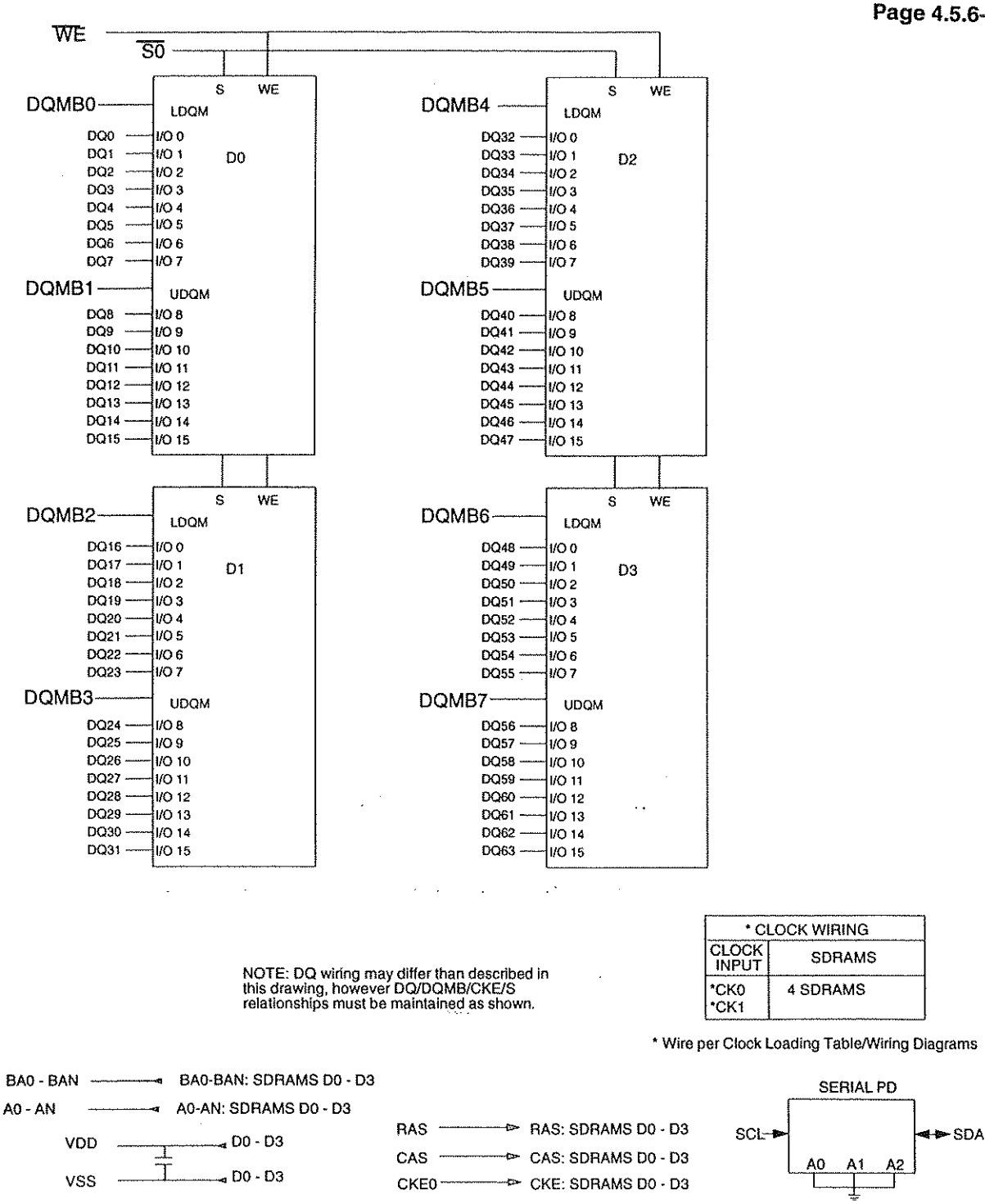
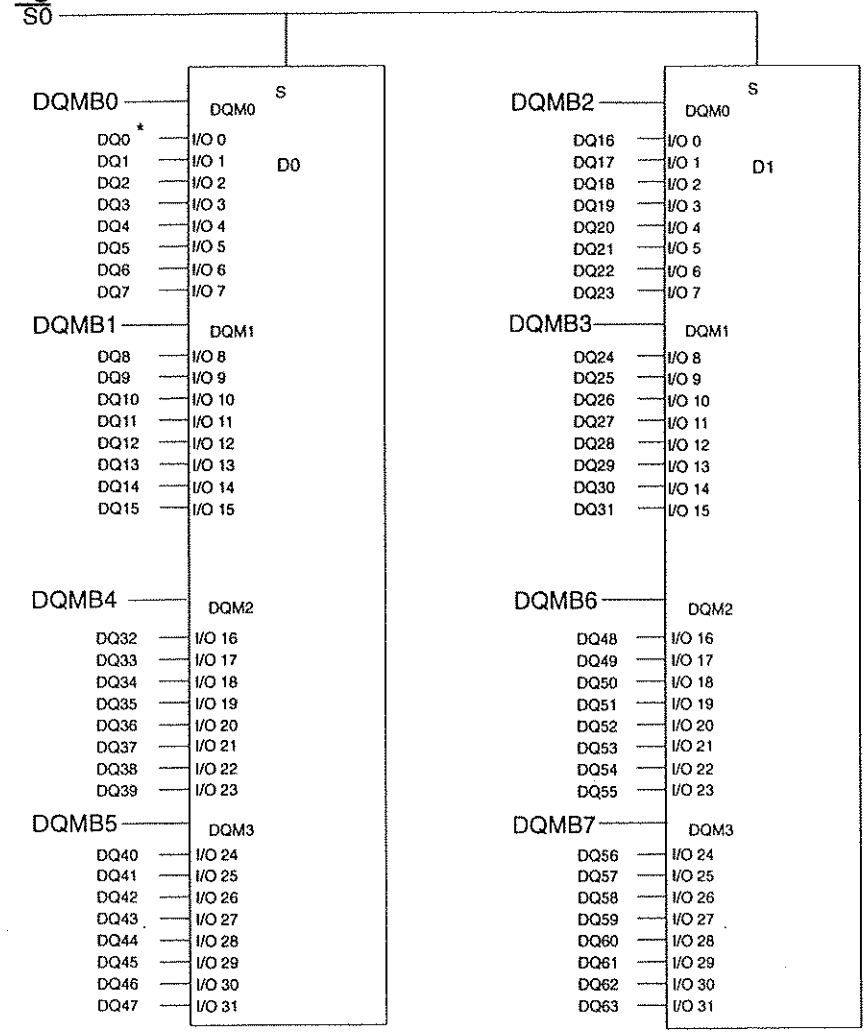


Figure 4.5.6–H
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X16 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	2 SDRAMS

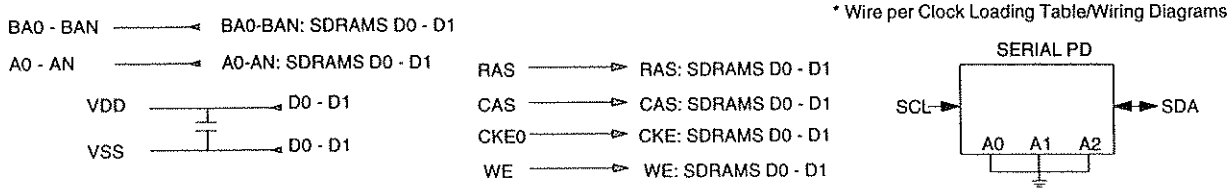
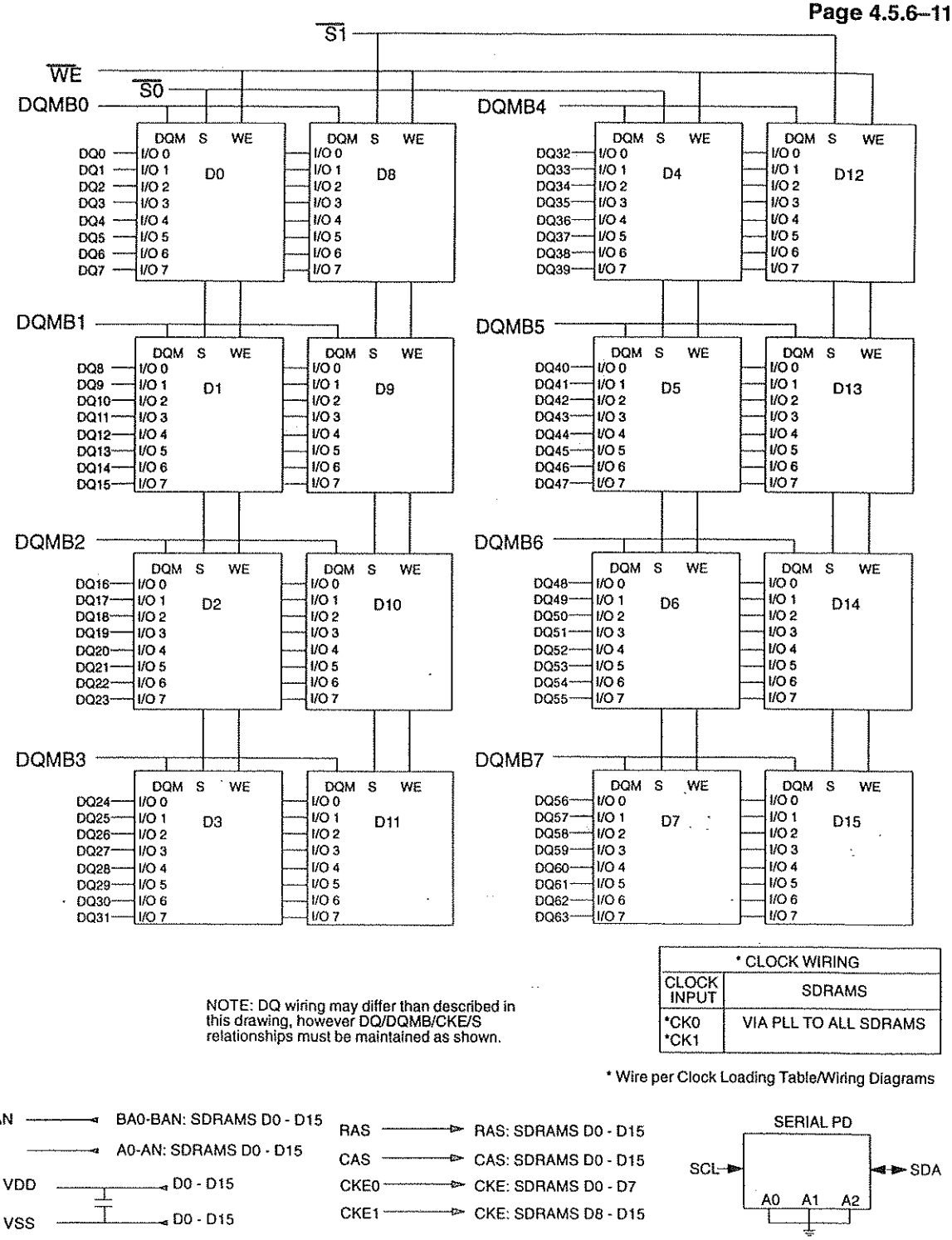


Figure 4.5.6–I
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X32 SDRAMs

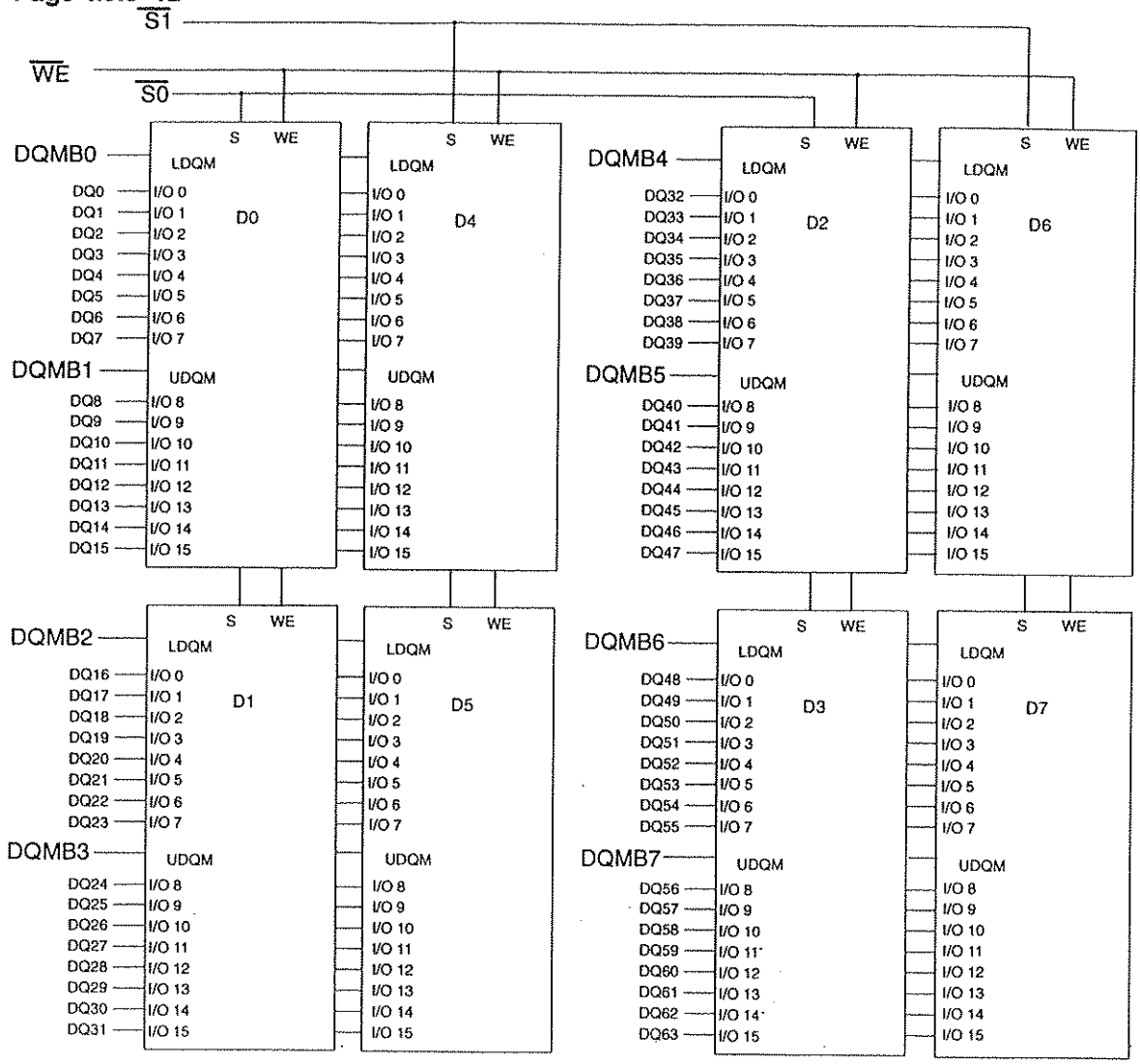


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	VIA PLL TO ALL SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

Figure 4.5.6–J
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

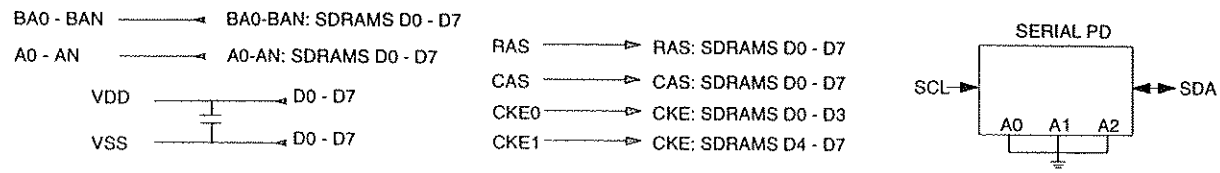
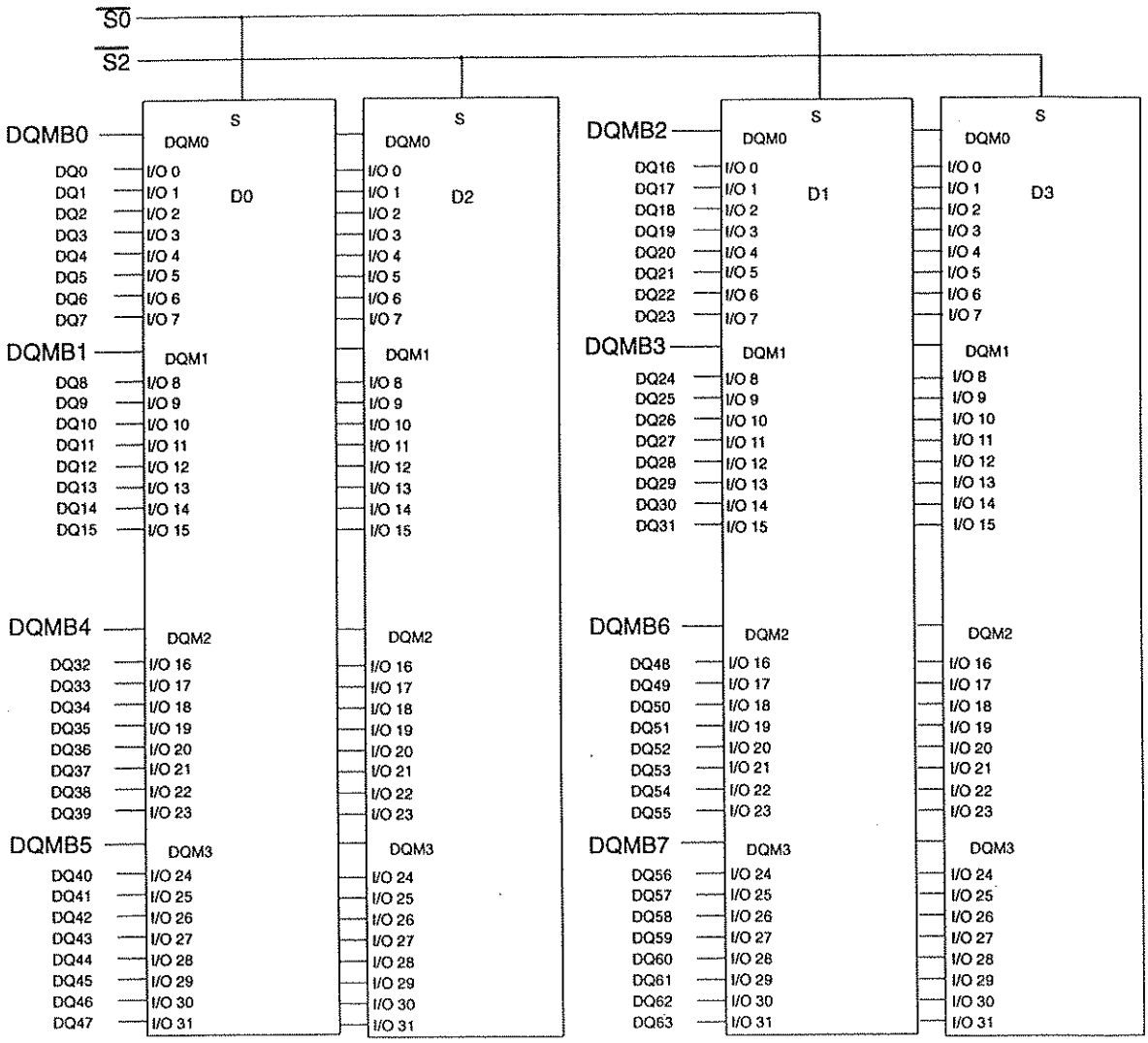


Figure 4.5.6–K
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X16 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

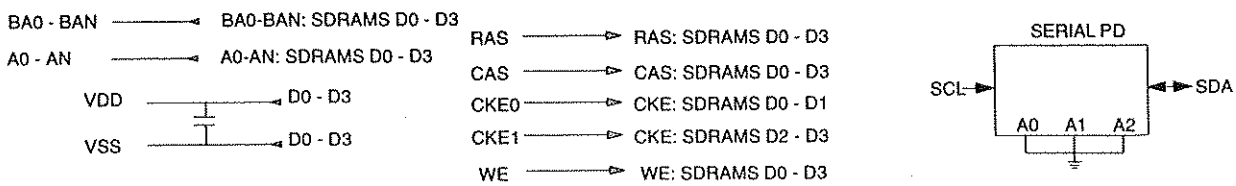
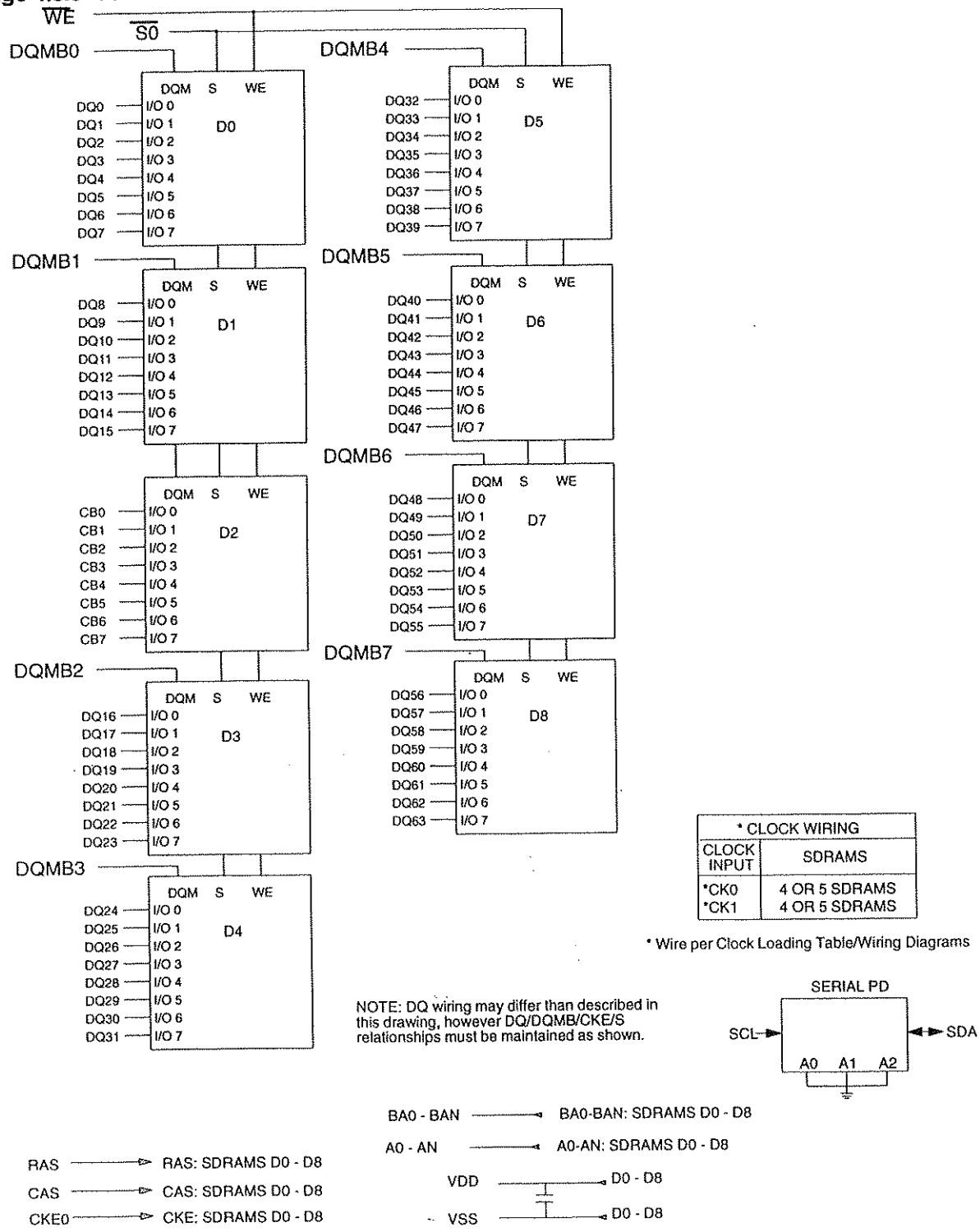


Figure 4.5.6–L
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X32 SDRAMs



* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 OR 5 SDRAMS
*CK1	4 OR 5 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

Figure 4.5.6–M
144 Pin X72 ECC SDRAM SO–DIMM, 1 Bank with X8 SDRAMs

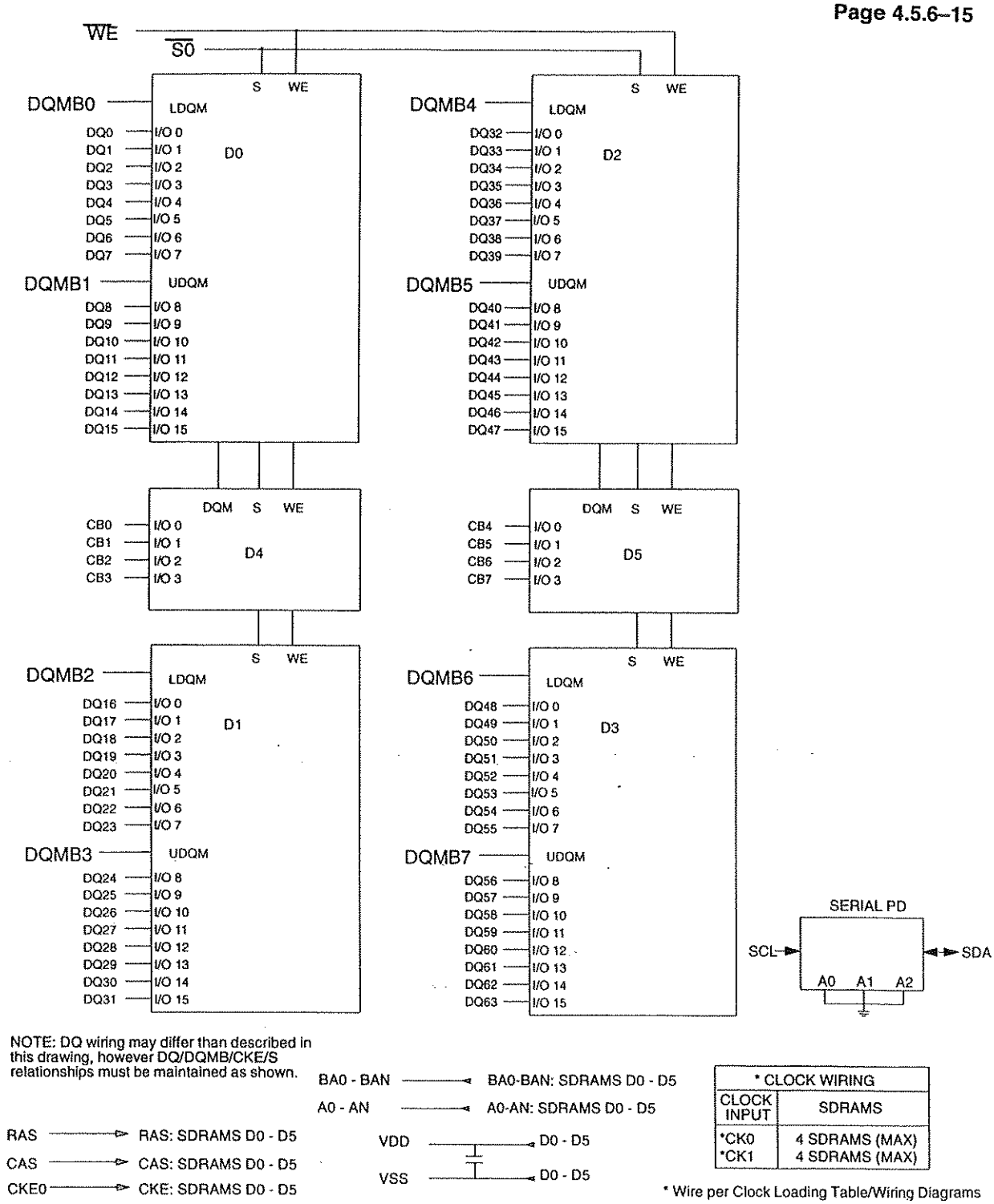


Figure 4.5.6–N
144 Pin X72 ECC SDRAM SO–DIMM, 1 Bank with X16 & X4 SDRAMs

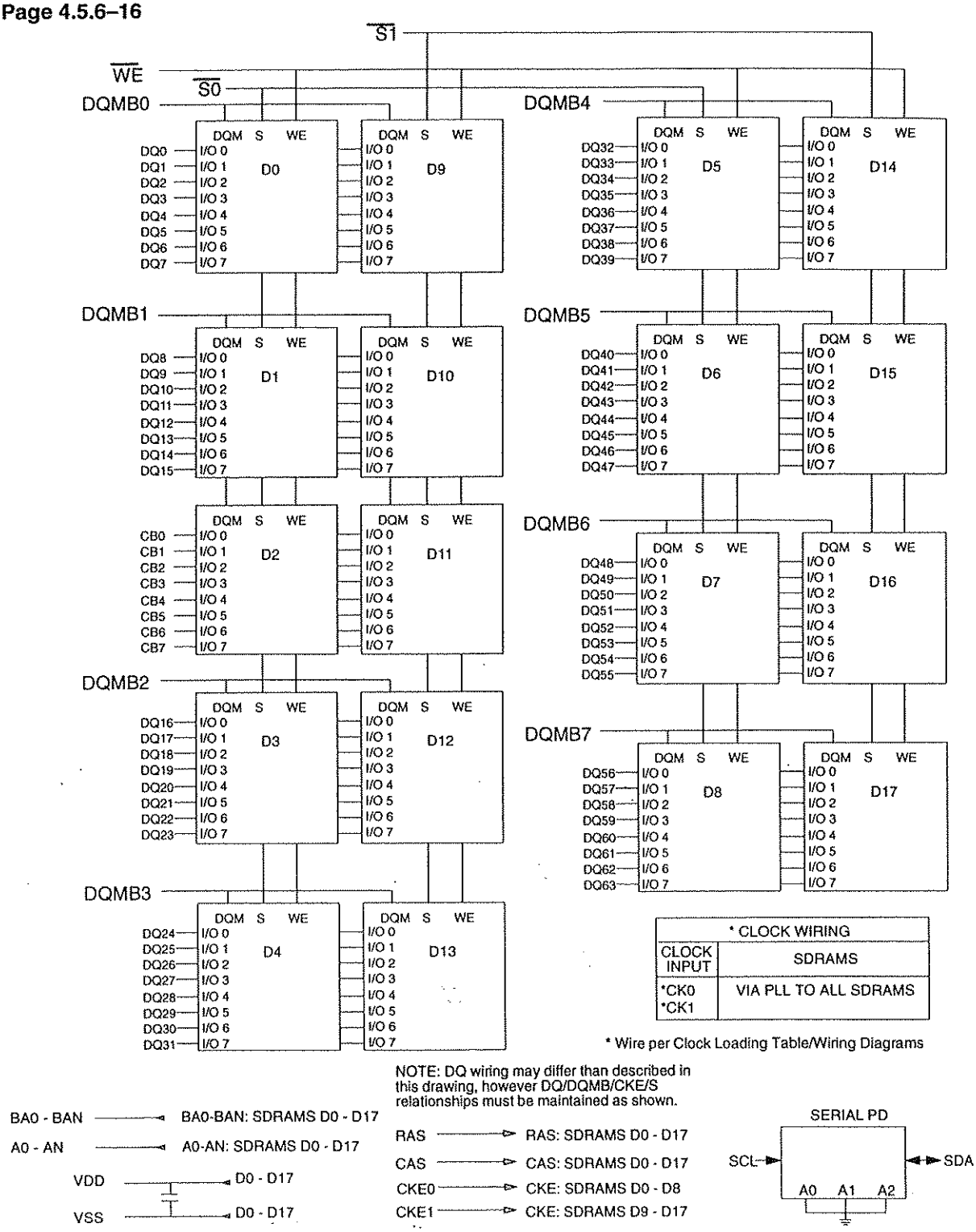


Figure 4.5.6–O
144 Pin X72 ECC SDRAM SO–DIMM, 2 Bank with X8 SDRAMs

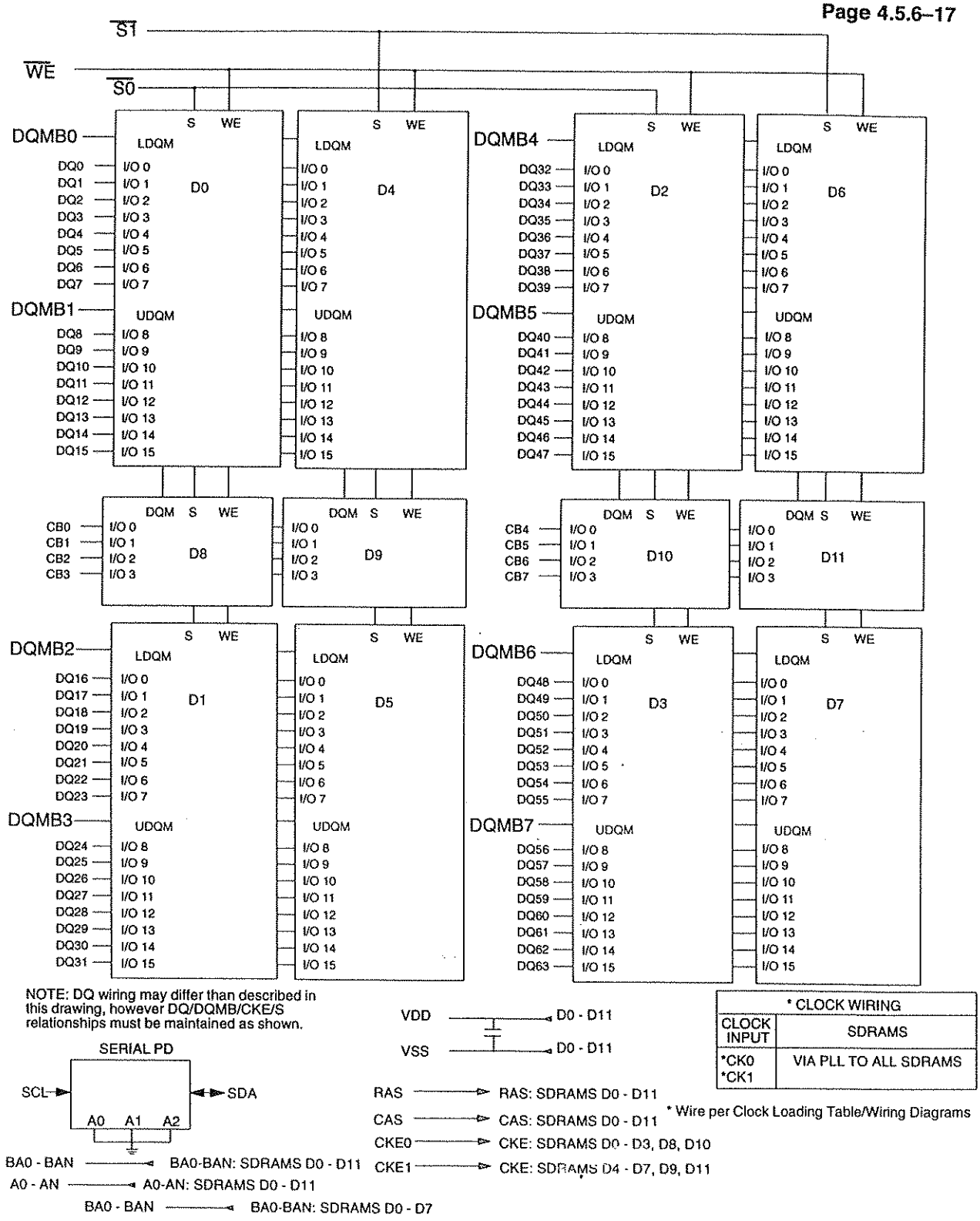


Figure 4.5.6–P
144 Pin X72 ECC SDRAM SO–DIMM, 2 Bank with X16 & X4 DRAMs

Release 7

4.6 Sixteen Byte Memory Modules

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

XILINX EXHIBIT 1010
Page 439

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 16 bytes (144 bits).
DATA CONFIGURATIONS—Only one DATA Word configurations is defined in the initial release:
—144 BIT SDRAM with the location of CHECKBITS undefined
CONFIGURATION—2 Different Configurations are defined using X16 SDRAM memories with 1 and 2 banks
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—278 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.6.1–A, 4.6.1–B, & 4.6.1–C
DRAM SPD INFORMATOION — Fig. 4.6.1–D
MODULE KEYING DEFINITION — Fig. 4.6.1–E
MODULE PIN DEFINITIONS — Fig. 4.6.1–F
X144 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.6.1–G and 4.6.1–H

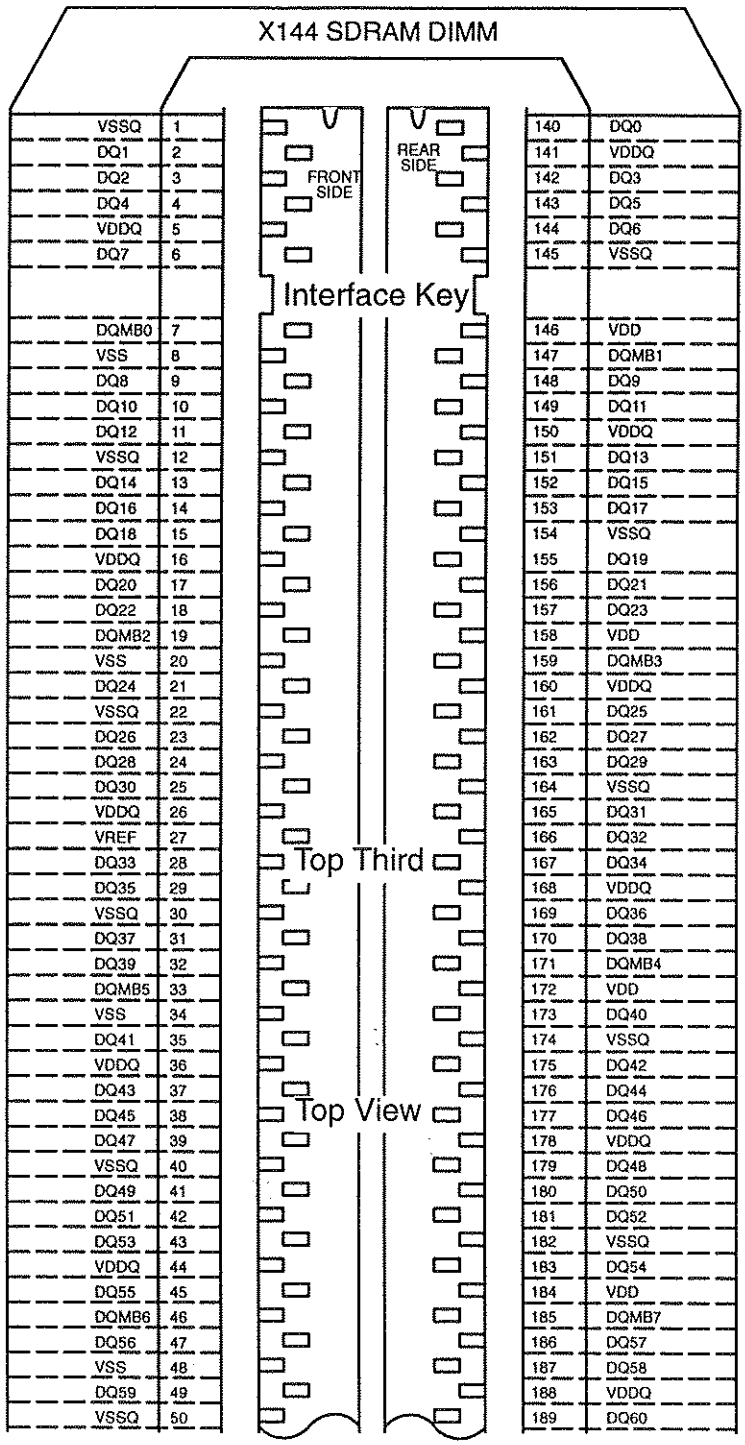


Figure 4.6.1–A
278 PIN X144 SDRAM DIMM PINOUT (TOP THIRD)

Release 7

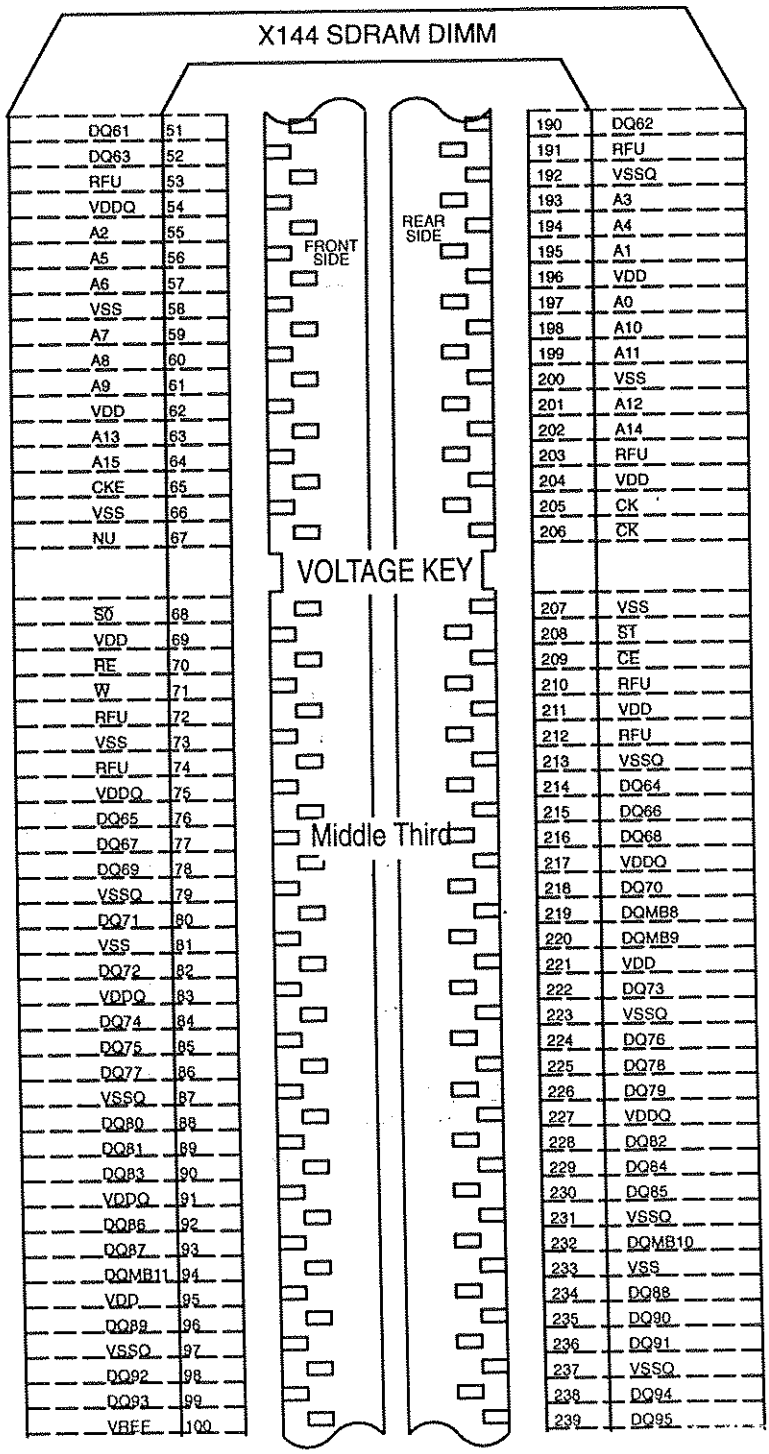


Figure 4.6.1–B
278 PIN X144 SDRAM DIMM PINOUT (MIDDLE THIRD)

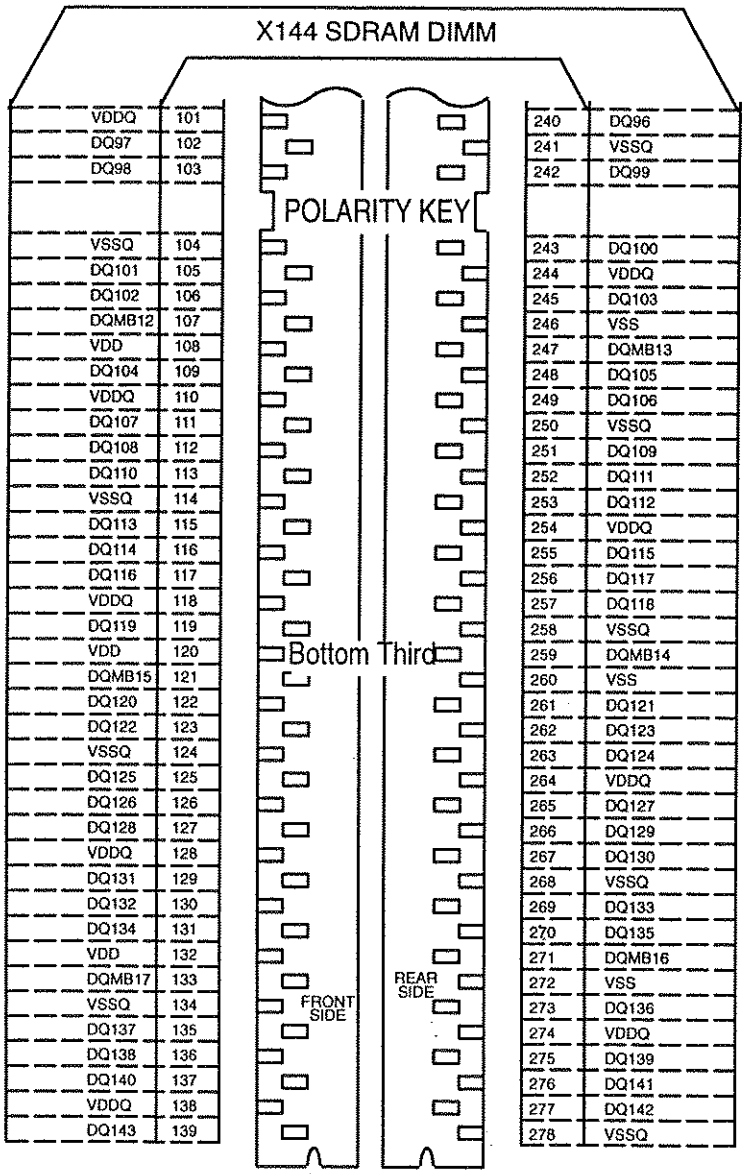


Figure 4.6.1–C
278 PIN X144 SDRAM DIMM PINOUT (BOTTOM THIRD)
Release 7

This page is reserved for the future addition of serial presence detect tables.

Figure 4.6.1–D
278 PIN X144 SDRAM DIMM PD AND CONFIGURATION TABLES
Release 7

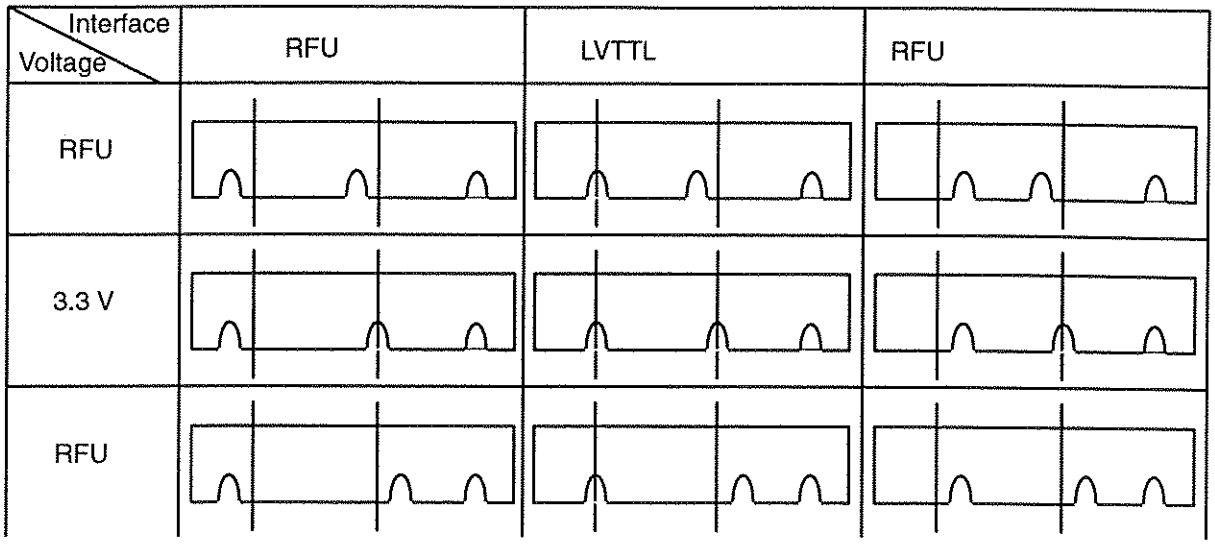
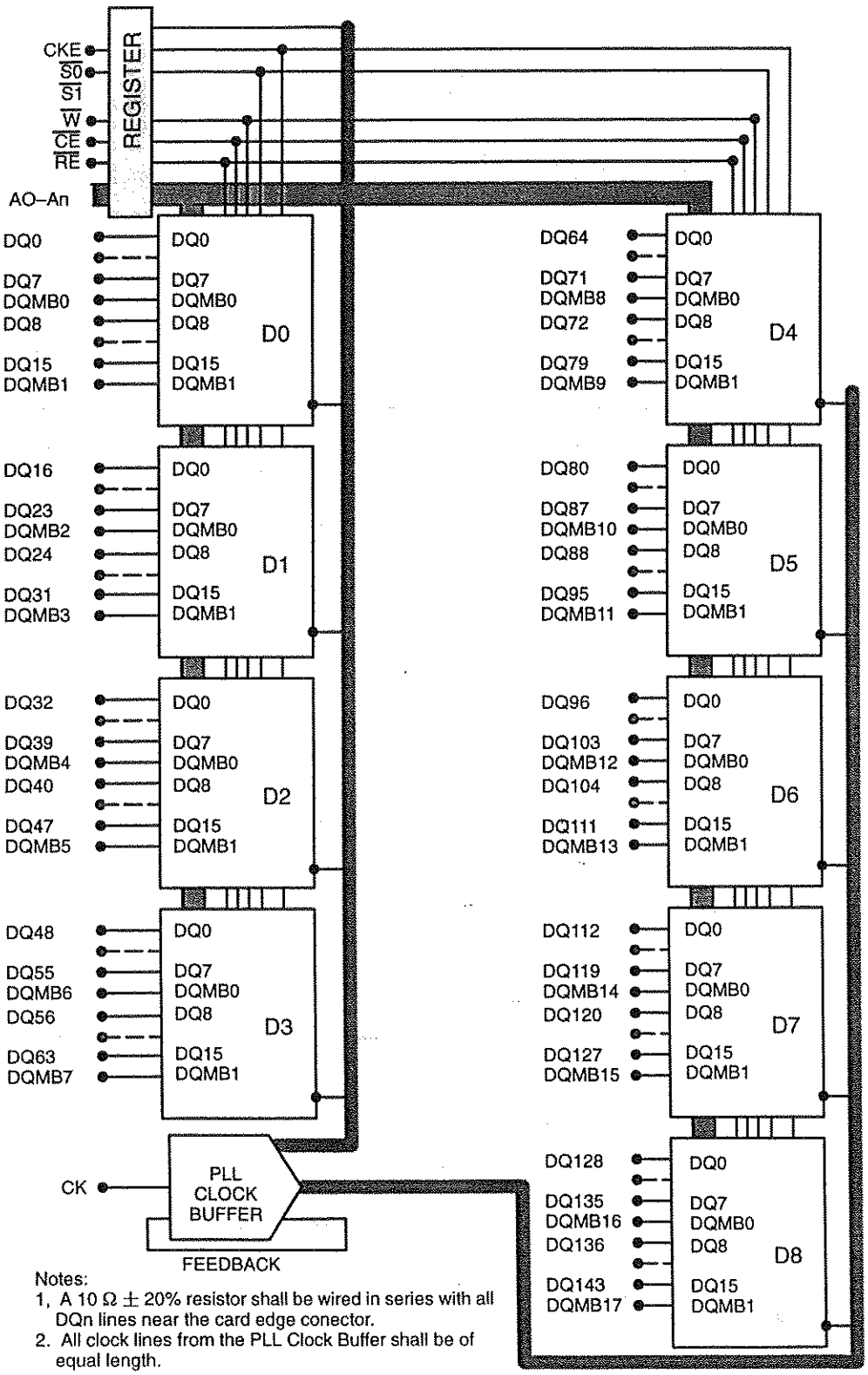


Figure 4.6.1-E
278 PIN 144 BIT SDRAM DIMM MECHANICAL KEY DEFINITION

Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ143	144	Data Input/Output (common)
CK, $\overline{CK}$	2	Clock Input
CKE	1	Clock Enable Input
$\overline{S0}$, $\overline{S1}$	2	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB17	18	Byte Data Mask input
VDD	14	Primary Positive Power Supply
VDDQ	27	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	14	Ground
VSSQ	27	Ground for data Input/Output
NU	1	Reserved for board test of PLL
RFU	7	Reserved for Future Use

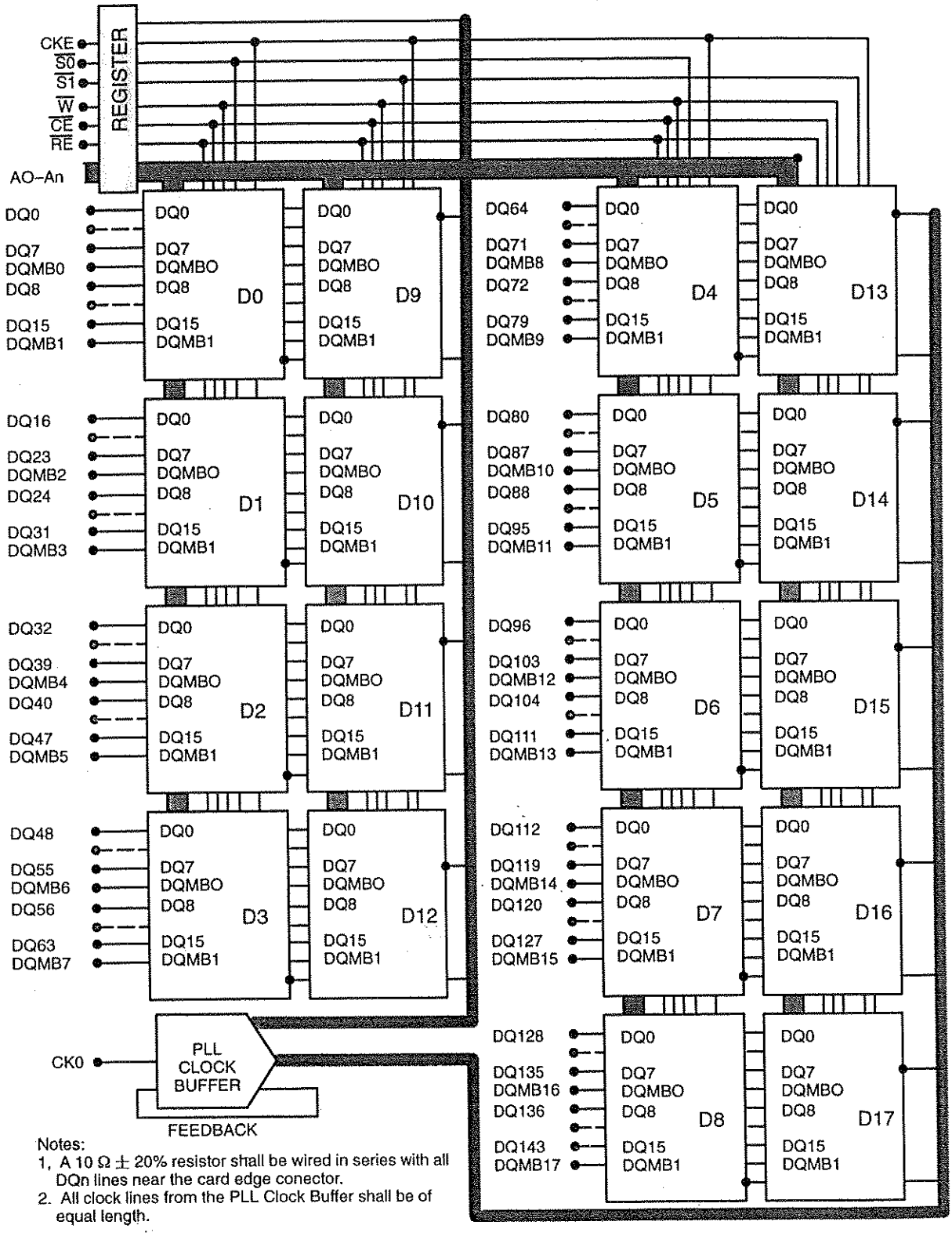
Notes:
1. NU pin is reserved for board test control of PLL, Make no connection at system level.
2 RFU pins are available for future standardization of serial Presence Detect and VTT.

Figure 4.6.1-F
278 PIN 144 BIT SDRAM DIMM PIN DEFINITIONS



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.6.1–G
278 PIN X144 BUFFERED SDRAM DIMM 1 BANK with X16 SDRAM
Release 7



Notes:
1. A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.6.1–H
278 PIN X144 BUFFERED SDRAM DIMM 2 BANKS with X16 SDRAM
Release 7

Exhibit E

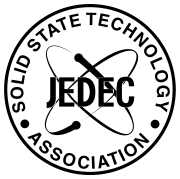
JEDEC STANDARD

Double Data Rate (DDR) SDRAM Specification

JESD79

JUNE 2000

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION





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Double Data Rate (DDR) SDRAM Specification

(The material contained in this standard was formulated under the cognizance of the JC-42.3 Subcommittee on RAM Memories and approved by the JEDEC Board of Directors. The text in this standard is from the following BoD Ballots: JCB-99-70, JCB-99-84, JCB-00-08, JCB-00-10 JCB-00-11, JCB-00-12, JCB-00-13, and JCB-00-23.)

1 Purpose

To define the minimum set of requirements for JEDEC-compliant 64M x4/x8/x16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

2 Scope

This comprehensive standard defines all required aspects of 64M x4/x8/x16 DDR SDRAMs, including features, functionality, AC and DC parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

XILINX EXHIBIT 1010
Page 453

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M x4 (4 M x4 x4 banks), 8 M x8 (2 M x8 x4 banks), 4 M x16 (1 M x16 x4 banks)

FEATURES

- Double–data–rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge–aligned with data for READs; center–aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 15.6 μs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ = +2.5 V ±0.2 V
- VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V

GENERAL DESCRIPTION

The 64 Mb DDR SDRAM is a high–speed CMOS, dynamic random–access memory containing 67,108,864 bits. It is internally configured as a quad–bank DRAM.

The 64 Mb DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM effectively consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half–clock–cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge–aligned with data for READs and center–aligned with data for WRITEs.

The 64 Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW will be referred to as the postive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self–timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power–saving, power–down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices will have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

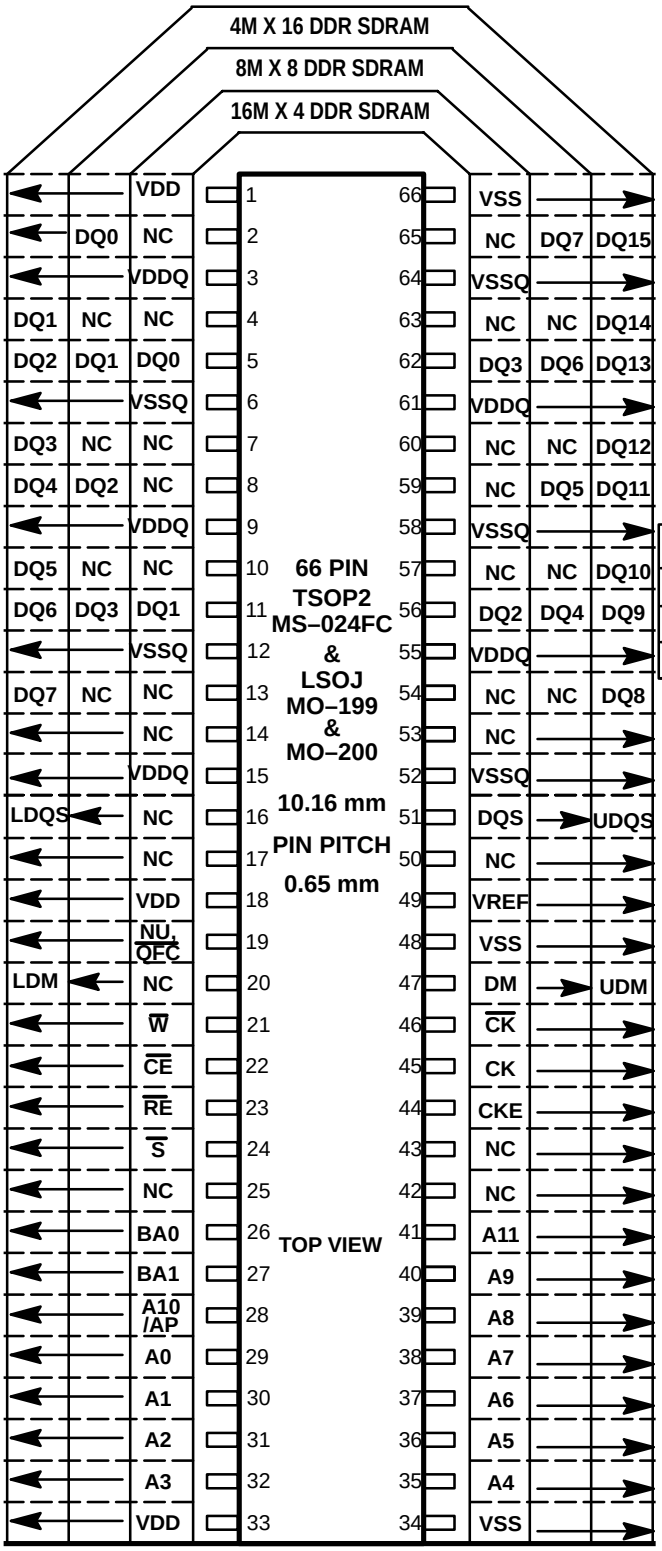
This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC 64 M x4/x8/x16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

CONTENTS

Pin Assignment Diagram 3
Functional Block Diagram – 16 M x4 4
Functional Block Diagram – 8 M x8 5
Functional Block Diagram – 4 M x16 6
Pin Descriptions 7
Functional Description 8
Initialization 8
Register Definition 8
Mode Register 8
Burst Length 8
Fig. 1, Mode Register Definition 9
Table 1, Burst Definition 9
Burst Type 10
Read Latency 10
Operating Mode 10
Table 2, CAS Latency & Frequency 10
Fig. 2, Required CAS Latencies 11
Extended Mode Register 12
DLL Enable/Disable 12
Output Drive Strength 12
QFC\ Enable/Disable 12
Fig. 3, Extended Mode Register Definition 12
Ternibology Definitions
DDR–200 12
DDR–266 12
Commands 13
Truth Table 1a (Commands) 13
Truth Table 1b(DM Operation) 13
Deselect 14
No Operation (NOP) 14
Mode Register Set 14
Active 14
Read 14
Write 14
Precharge 14
Auto Precharge 14
Burst Terminate 14
Auto Refresh 14
Self Refresh 15
Operation 16
Bank/Row Activation 16
Fig. 4, Activating a Specific Row 16
Fig. 5, tRCD & tRRD Definition 16
Reads 17
Fig. 6, Read Command 17
Fig. 7, Read Burst 18
Fig. 8, Consecutive Read Bursts 19
Fig. 9, Nonconsecutive Read Bursts 20
Fig. 10, Random Read Accesses 21
Fig. 11, Terminating a Read Burst 23
Fig. 12, Read to Write 24
Fig. 13, Read to Precharge 25
Writes 26
Fig. 14, Write Command 26
Figs. 15 & 16, Write Burst 27
Fig. 17, Write to Write–Max tDQSS 28
Fig. 18, Write to Write–Min tDQSS 29
Fig. 19a, Write to Write–Max tDQSS, Nonconsecutive 30
Fig. 19b, Write to Write–Min tDQSS, Nonconsecutive 31
Fig. 20, Random Writes–Max tDQSS 32
Fig. 21, Random Writes–Min tDQSS 33
Fig. 22, Write to Read–Max tDQSS, Noninterrupting 34
Fig. 23, Write to Read–Min tDQSS, Noninterrupting 35
Fig. 24, Write to Read–Max tDQSS, Interrupting 36
Fig. 25, Write to Read–Min tDQSS, Interrupting 37
Fig. 26, Write to Read–Min tDQSS, Odd, Interrupting 38
Fig. 27, Write to Read–Nominal tDQSS, Interrupting 39
Fig. 28, Write to Precharge–Max tDQSS, Noninterrupting . . 40
Fig. 29, Write to Precharge–Min tDQSS, Noninterrupting . . 41
Fig. 30, Write to Precharge–Max tDQSS, Interrupting 42
Fig. 31, Write to Precharge–Min tDQSS, Interrupting 43
Fig. 32, Write to Precharge–Min tDQSS, Odd, Interrupting . 44
Fig. 33, Write to Precharge – Nominal tDQSS,Interrupting . . 45
Precharge 46
Fig. 34, Precharge Command 46
Fig. 35, Power–Down 47
Truth Table 2 (CKE) 48
Truth Table 3 (Current State, Same Bank) 49
Truth Table 4 (Current State, Different Bank) 51
Simplified State Diagram 53
Absolute Maximum Ratings 54
Capacitance 54
DC Electrical Characteristics and Operating Conditions 54
Output V–I Characteristics . . . . . 55 & 56
AC Operating Conditions 57
Idd Specifications and Conditions 57
AC Electrical Characteristics (Timing Table) . . . . . 58 & 59
Fig. 36, Test Reference Load 60
Timing Waveforms
Fig. 37, Data Input Timing 61
Fig. 38, Data Output Timing 61
Fig. 39, Initialize and Mode Register Set 62
Fig. 40, Power–Down Mode 63
Fig. 41, Auto Refresh Mode 64
Fig. 42, Self Refresh Mode 65
Reads
Fig. 43, Read – Without Auto Precharge 66
Fig. 44, Read – With Auto Precharge 67
Fig. 45, Bank Read Access 68
Writes
Fig. 46, Write – Without Auto Precharge 69
Fig. 47, Write – With Auto Precharge 70
Fig. 48, Bank Write Accesses 71
Fig. 49, Write – DM Operation 72



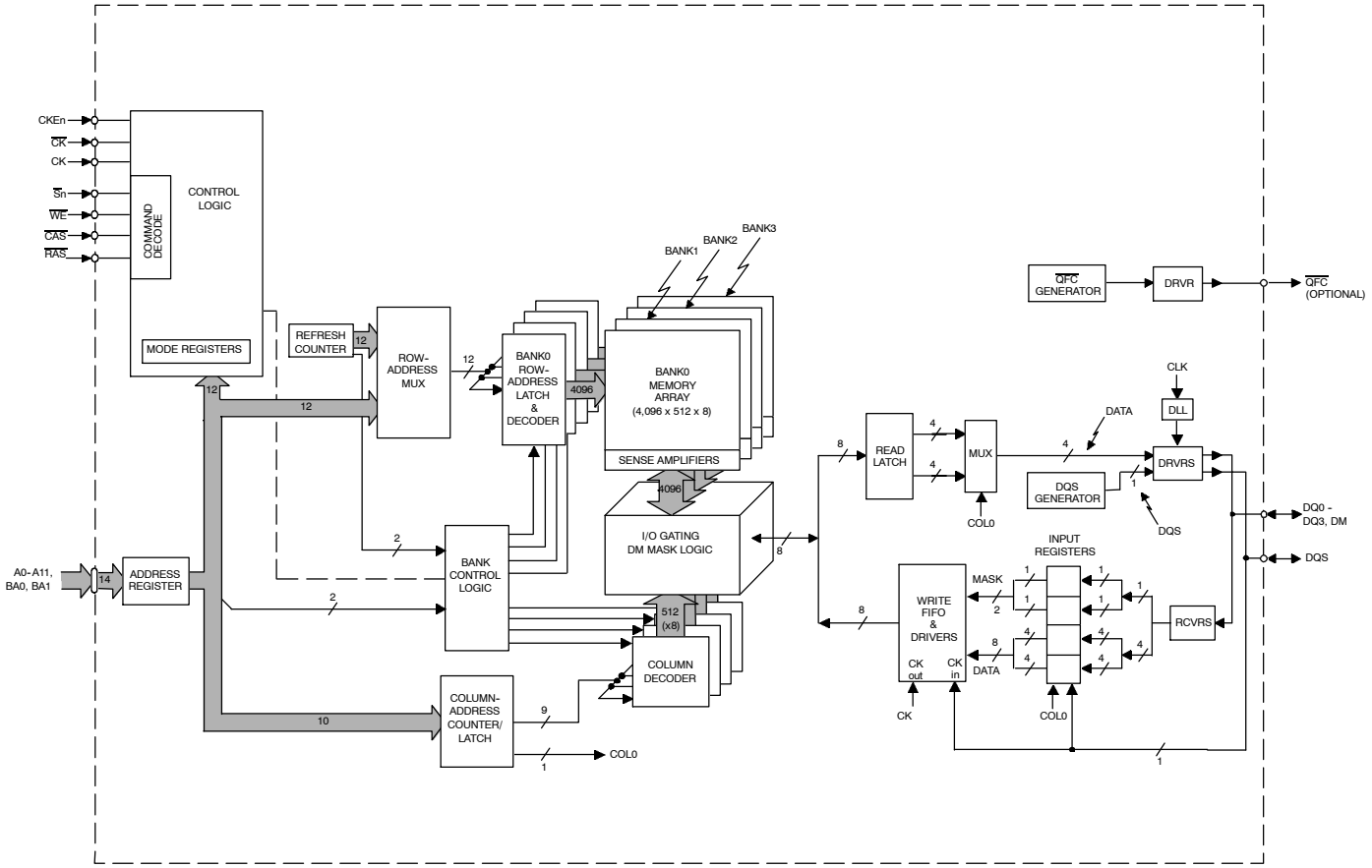
ADDRESS ASSIGNMENT TABLE

	DENSITY	BANKS	ROW ADDR.	COL ADDR	BANK ADDR
16M X 4	64 Mb	4	A0⇒A11	A0⇒A9	BA0, BA1
8M X 8	64 Mb	4	A0⇒A11	A0⇒A8	BA0, BA1
4M X 16	64 Mb	4	A0⇒A11	A0⇒A7	BA0, BA1

64 M DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ

Release 1

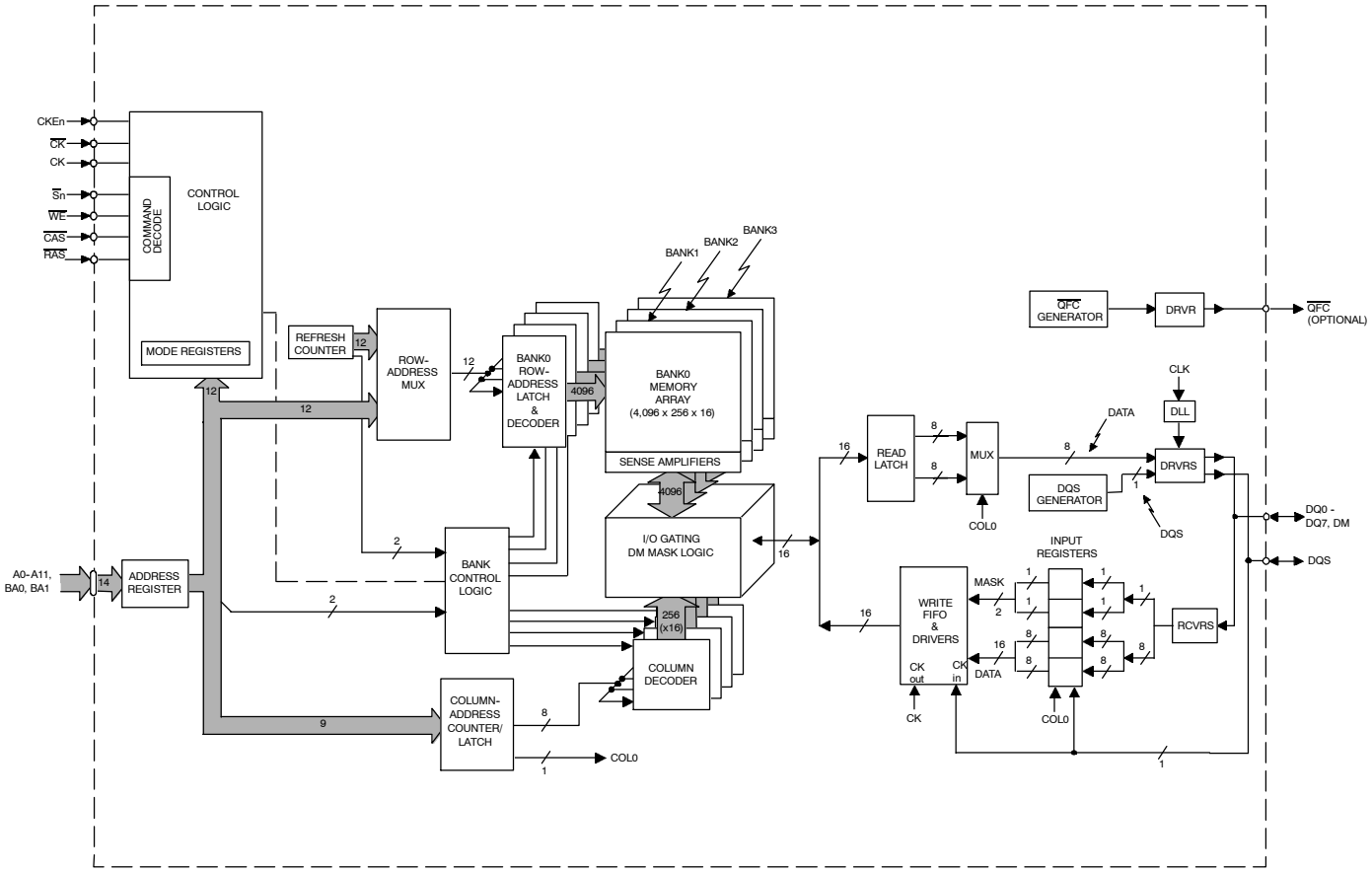
FUNCTIONAL BLOCK DIAGRAM – x4 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

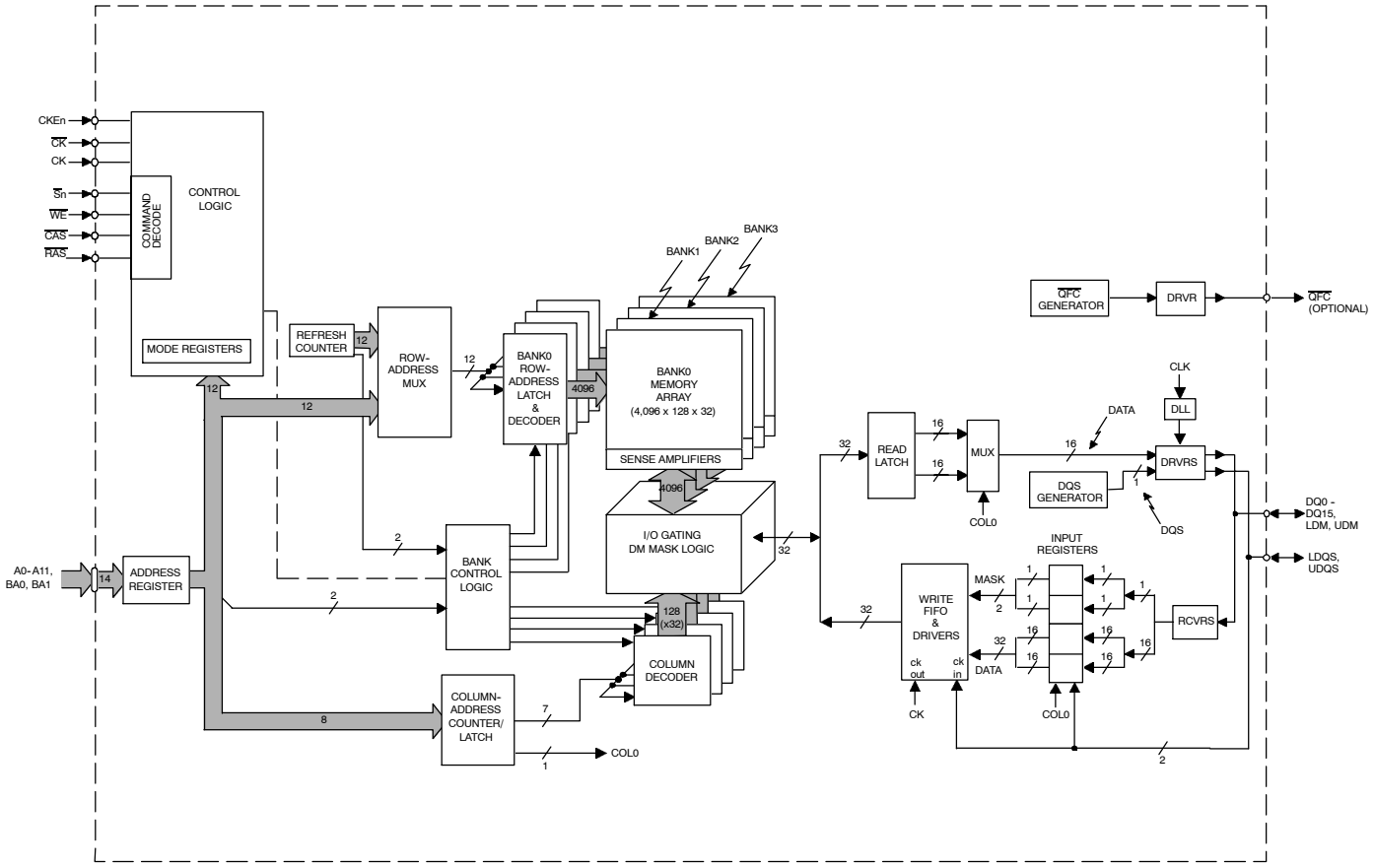
FUNCTIONAL BLOCK DIAGRAM – x8 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

FUNCTIONAL BLOCK DIAGRAM – x16 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: LDM and UDM are unidirectional signals (input only) but are internally loaded to match the load of the bidirectional DQ and DQS signals.

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE(n)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER–DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER–DOWN (row ACTIVE in any bank). CKE is synchronous for POWER–DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER–DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied. The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{S}$(n)	Input	Chip Select: All commands are masked when $\overline{S}$ is registered high. $\overline{S}$ provides for external bank selection on systems with multiple banks. $\overline{S}$ is considered part of the command code. The standard pinout includes one $\overline{S}$ pin. Optional pinouts include $\overline{S}$0 and $\overline{S}$1 on different pins, to facilitate device stacking.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{S}$) define the command being entered.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0–DQ7; UDM corresponds to the data on DQ8–DQ15.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.–
A0–A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op–code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Input/Output: Data bus
DQS	I/O	Data Strobe: Output with read data, input with write data. Edge–aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0–DQ7; UDQS corresponds to the data on DQ8–DQ15.
$\overline{QFC}$	Output	FET Control: Optional. Output during every Read and Write access. Can be used to control isolation switches on modules. Open drain output.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V ±0.2 V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V ±0.3 V or +2.5 V ±0.2 V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

FUNCTIONAL DESCRIPTION

The 64 Mb DDR SDRAM is a high–speed CMOS, dynamic random–access memory containing 67,108,864 bits. The 64 Mb DDR SDRAM is internally configured as a quad–bank DRAM.

The 64 Mb DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double–data–rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch–up, which may cause permanent damage to the device. Vref can be applied any time after VDDQ, but is expected to be nominally coincident with Vtt. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power–up is required to guarantee that the DQ and DQS outputs will be in the High–Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 µs delay prior to applying an executable command.

Once the 200 µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the ”all banks idle” state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 1. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self–clearing).

Mode Register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–Ai when the burst length is set to two, by A2–Ai when the burst length is set to four and by A3–Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

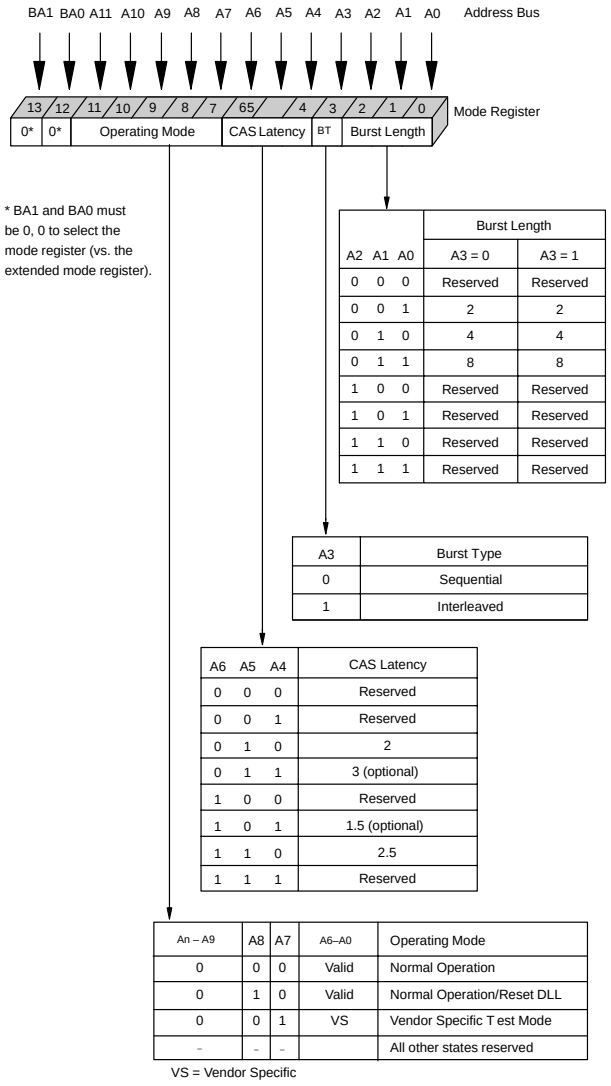


Figure 1
MODE REGISTER DEFINITION

Table 1

BURST DEFINITION

Burst Length	Starting Coumn Adress:	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0–1	0–1
	1	1–0	1–0
4	A1 A0		
	0 0	0–1–2–3	0–1–2–3
	0 1	1–2–3–0	1–0–3–2
	1 0	2–3–0–1	2–3–0–1
	1 1	3–0–1–2	3–2–1–0
8	A2 A1 A0		
	0 0 0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0 0 1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0 1 0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0 1 1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1 0 0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1 0 1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1 1 0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1 1 1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0

Note:
1. For a burst length of two, A1–Ai selects the two–data–element block; A0 selects the first access within the block.
2. For a burst length of four, A2–Ai selects the four–data–element block; A0–A1 selects the first access within the block.
3. For a burst length of eight, A3–Ai selects the eight–data–element block; A0–A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A11 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is inititated by issuing a Mode Register Set command with bits A7 and A9–A11 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7–A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Table 2

CAS LATENCY AND FREQUENCY

	MAXIMUM OPERATING FREQUENCY (MHz)*		
	DDR–266A	DDR–266B	DDR–200
CL2	133	100	100
CL2.5	143	133	125

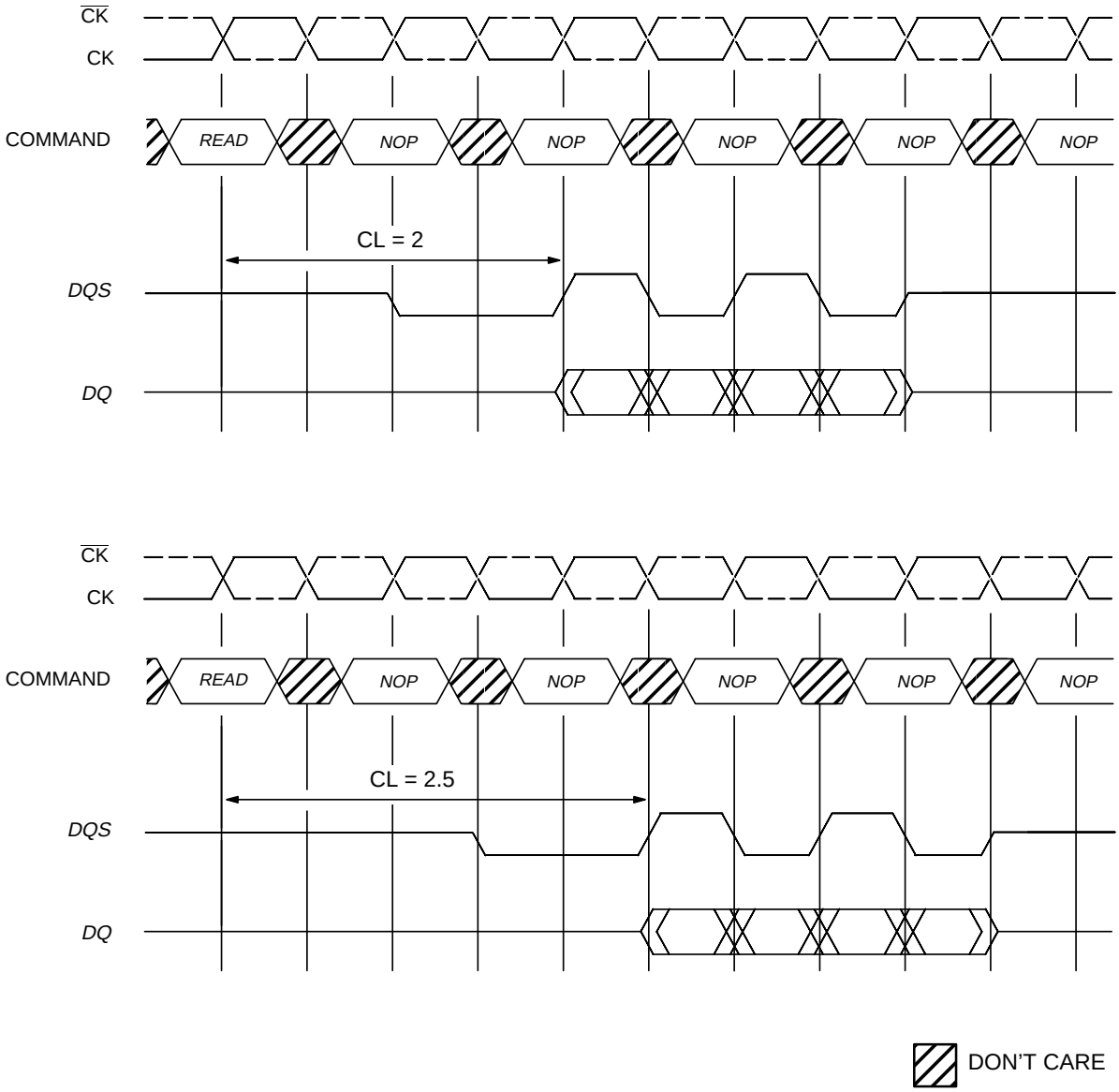
* Values are nominal (i.e., may have been rounded off; exact tCK should be used).

Terminology Definitions. The following are definitions of the terms DDR–200 & DDR–266 as used in this specification

DDR–200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The corresponding nominal data rate is 200 MHz.

DDR–266n: Speed grades for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is 266 MHz. Devices designated as DDR–266B will operate with CAS Latency = 2.5 clock periods at a 133 MHz clock frequency. Devices designated as DDR–266A will operate with CAS Latency = 2 clock periods at a 133 MHz clock frequency.

XILINX EXHIBIT 1010
Page 463



Burst Length = 4 in the cases shown
Shown with nominal tDQSCK, and tDQSQ

Figure 2
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional), and $\overline{\text{QFC}}$ output enable/disable (optional). These functions are controlled via the bits shown in Figure 3. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power–up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point–to–point environments. I–V curves for the normal drive strength are included in this document; the curves for the weak drive strength will be included in a future revision.

$\overline{\text{QFC}}$ Enable/Disable

The $\overline{\text{QFC}}$ signal might be provided by certain vendors to control FET switches used to isolate module loads from the system memory bus at times when the given module is not being accessed.

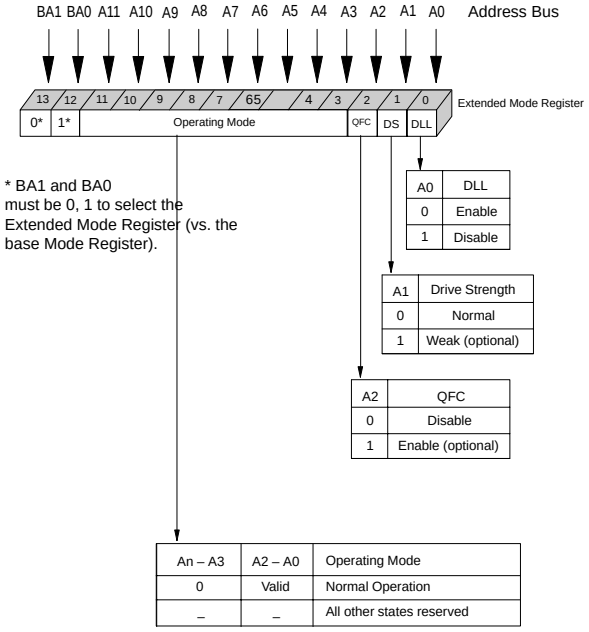


Figure 3
EXTENDED MODE REGISTER DEFINITION

COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a _ Commands

(Notes: 1)

NAME (Function)	**$\overline{S}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**ADDR**	**NOTES**
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7
MODE REGISTER SET	L	L	L	L	Op–Code	2

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0–BA1 are reserved; A0–A11 provide the op–code to be written to the selected Mode Register.
3. BA0–BA1 provide bank address and A0–A11 provide row address.
4. BA0–BA1 provide bank address; A0–Ai provide column address (where i = 7 for x16, 8 for x8 and 9 for x4); A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are ”Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are ”Don’t Care” except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.

TRUTH TABLE 1b _ DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

NOTE: 1. Used to mask write data, provided coincident with the corresponding data.

DESELECT

The DESELECT function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an DDR SDRAM which is selected ($\overline{S}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A11. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as ”Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual–bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to /CAS–BEFORE–/RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an AUTO REFRESH command. The 64 Mb DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of 15.6 µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 * 15.6 µs (140.4 µs).

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are ”Don’t Care” during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be ”opened.” This is accomplished via the ACTIVE command (Figure 4), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been ”closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row–access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

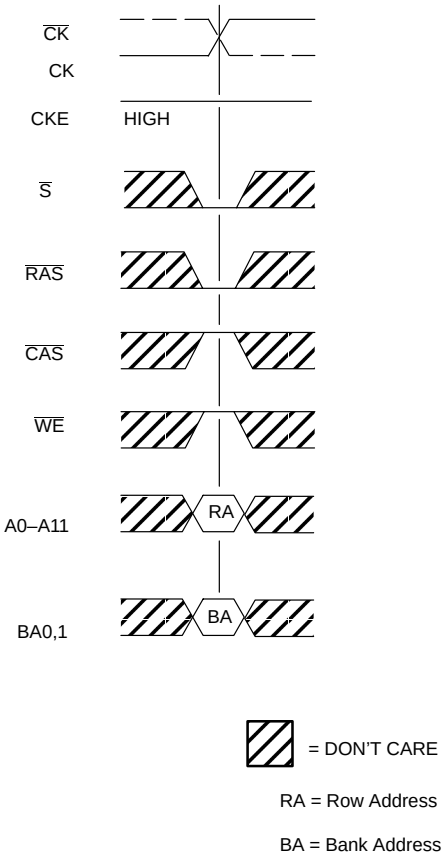


Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

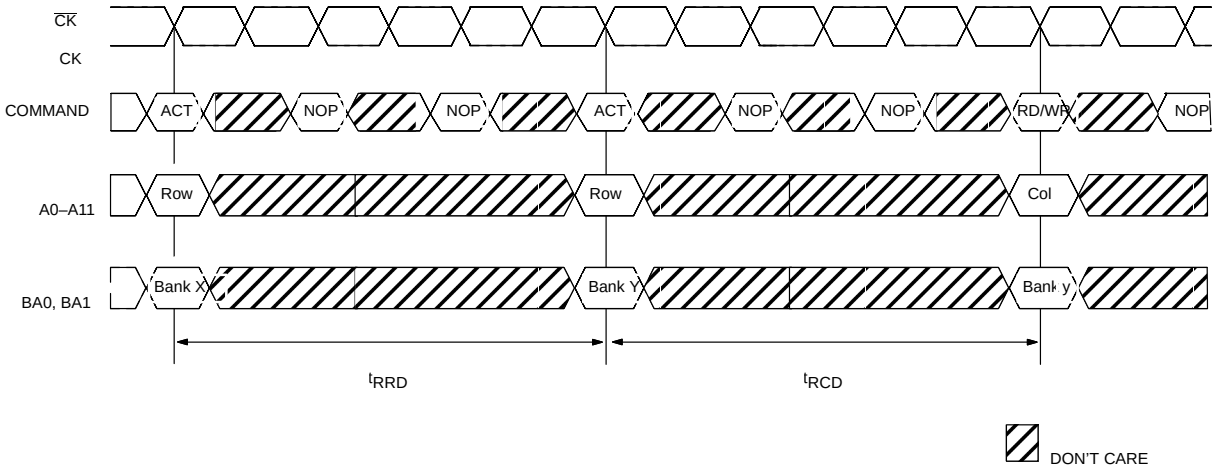


Figure 5
tRCD and tRRD Definition

Reads

READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data–out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data–out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 7 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data–out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High–Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 8. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 9. Full–speed random read accesses within a page (or pages) can be performed as shown in Figure 10.

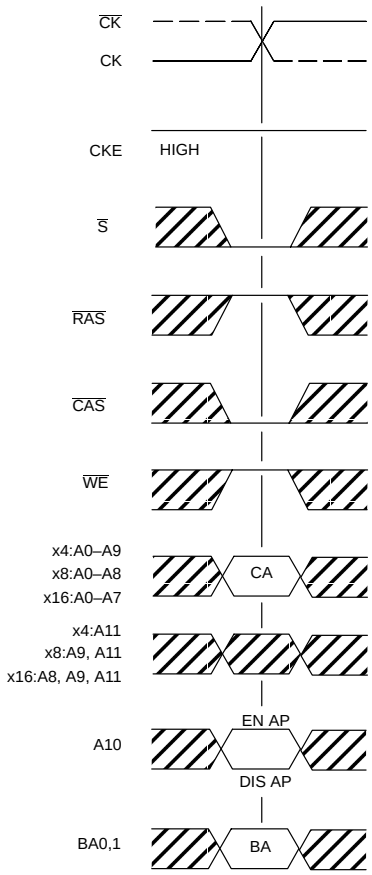
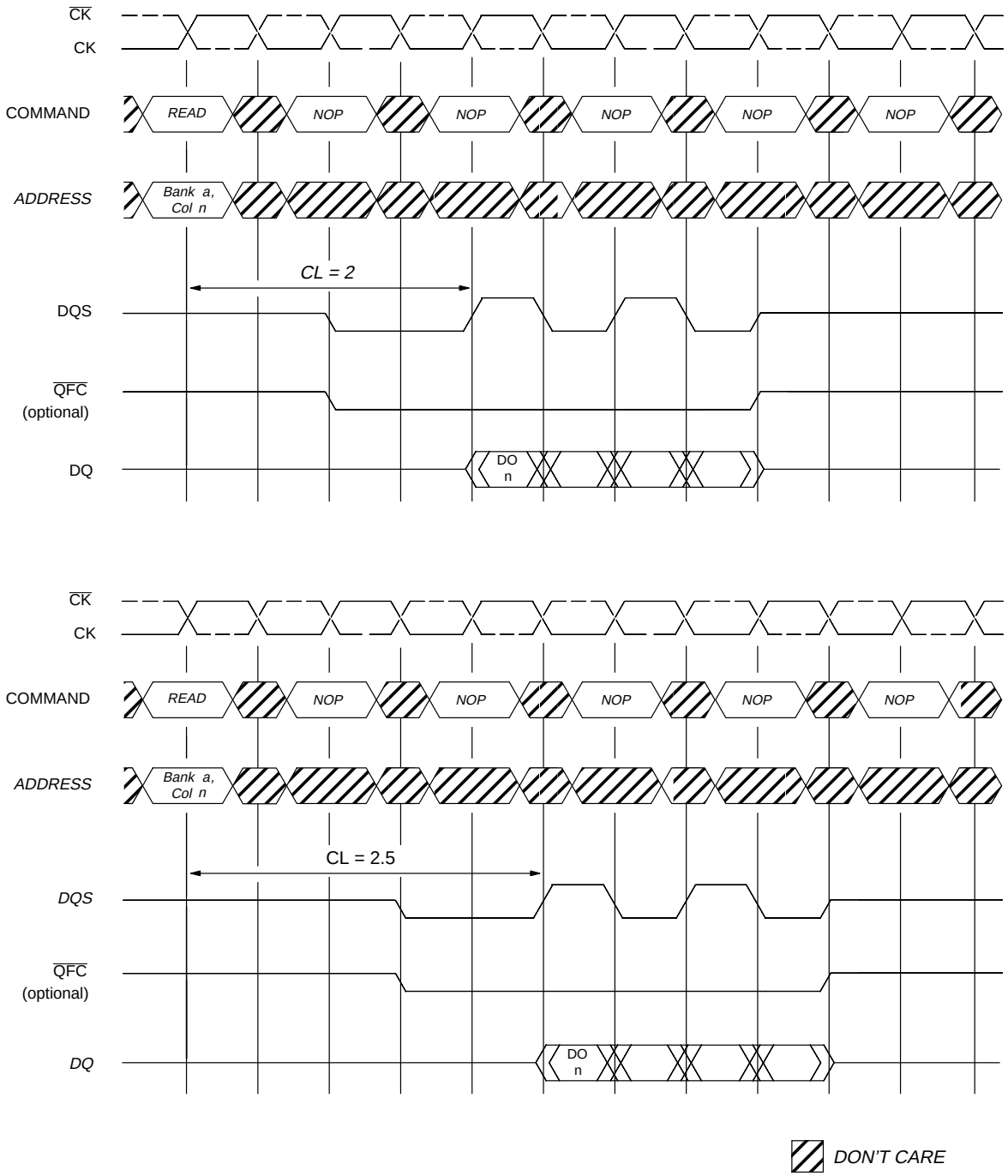
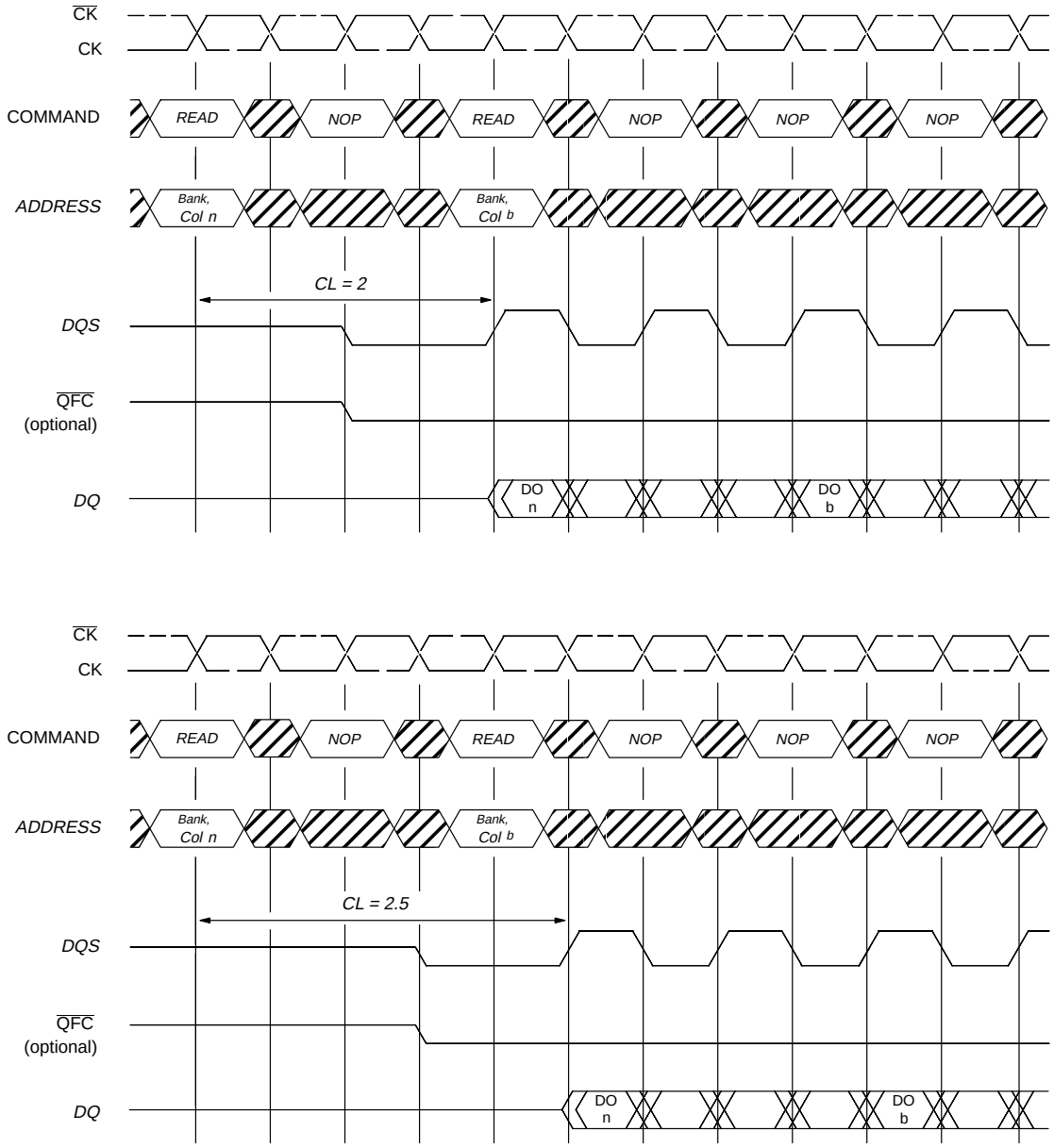


Figure 6
READ COMMAND



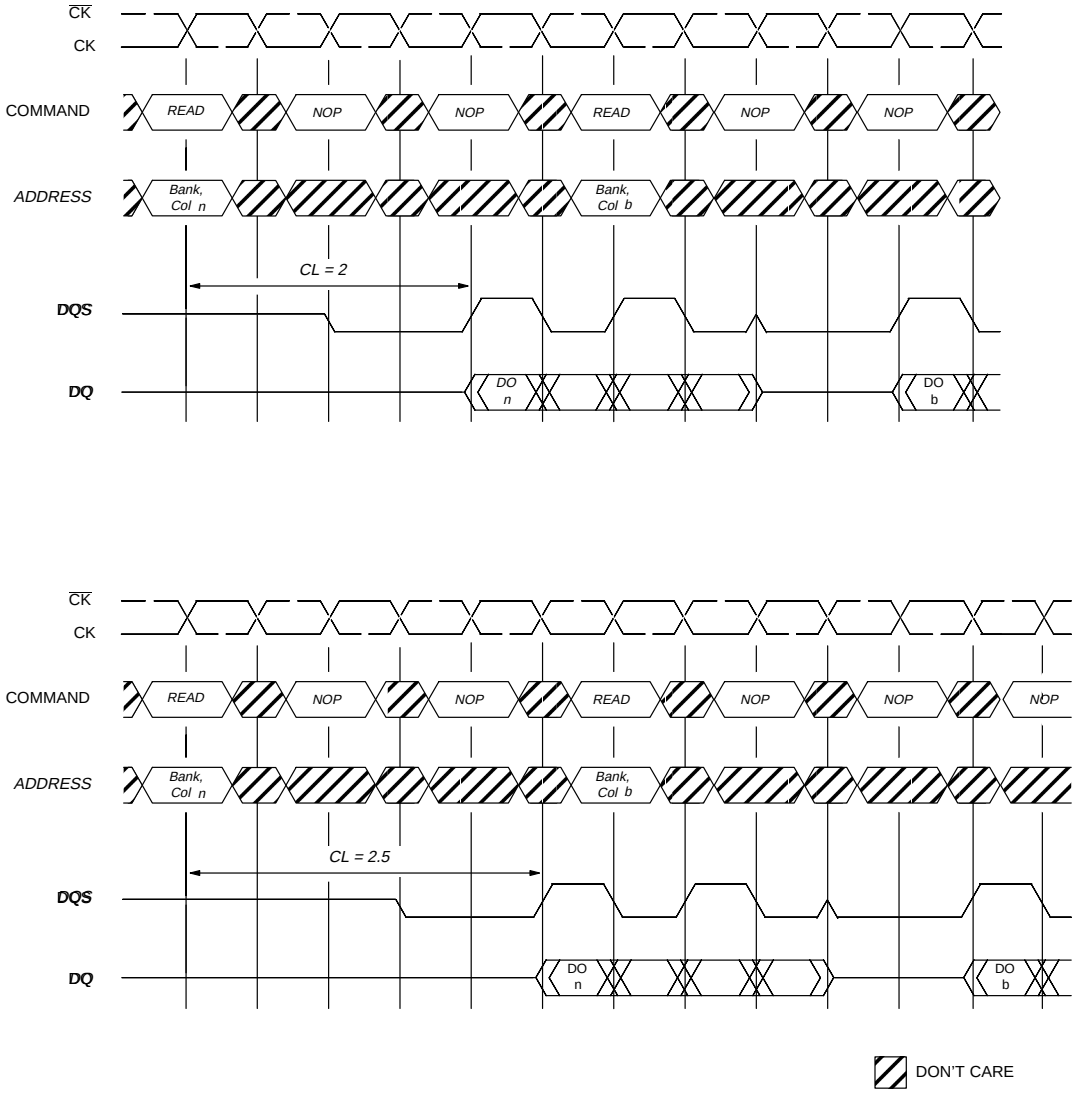
DO n = Data Out from column n
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 7
READ BURST – REQUIRED CAS LATENCIES



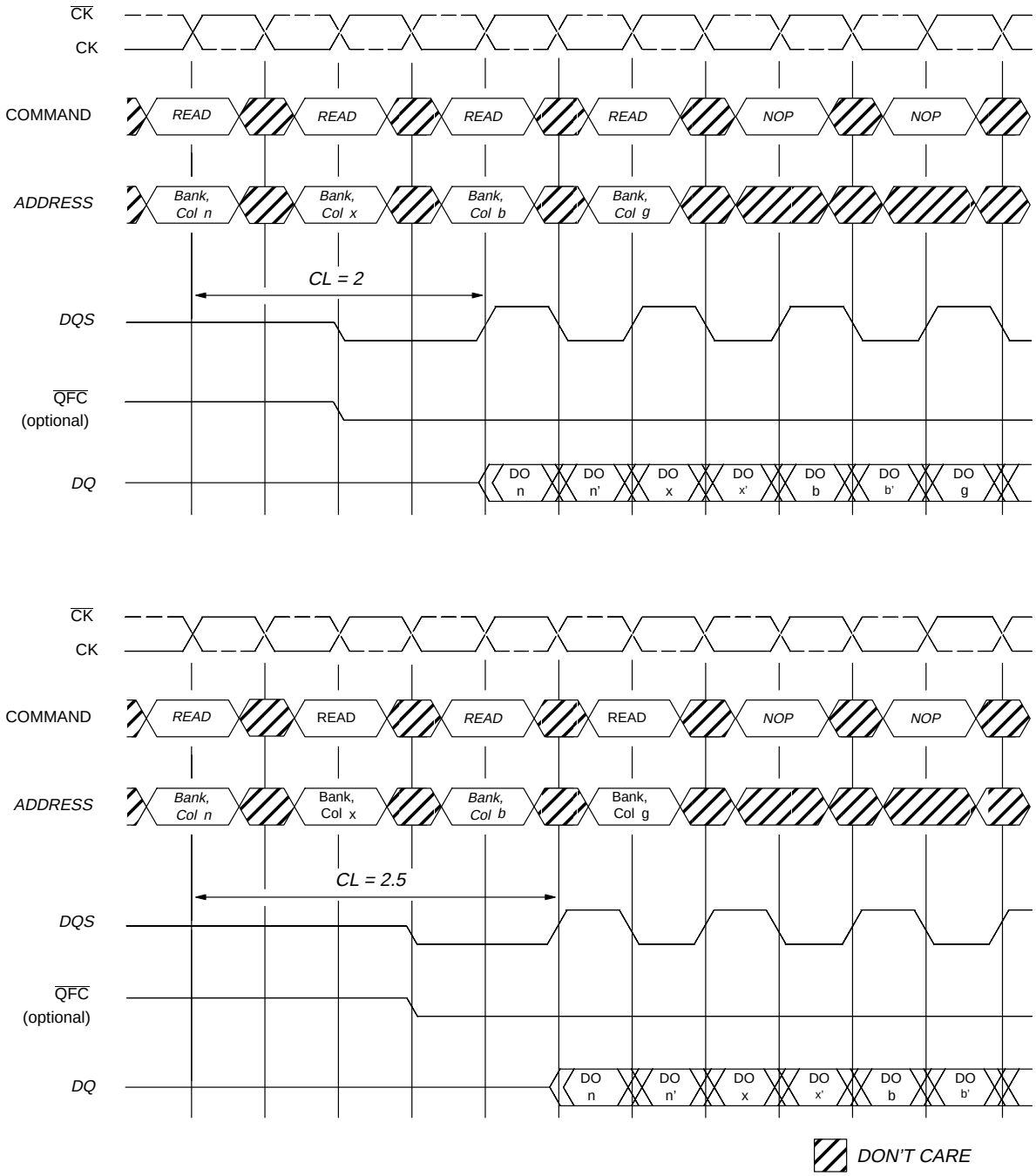
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b
Shown with nominal tDQSCK, and tDQSQ
Read commands shown must be to the same device

Figure 8
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)
Shown with nominal tDQSCK, and tDQSQ

Figure 9
NONCONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n, etc. = Data Out from column n, etc.
n' , etc. = the next Data Out following DO n, etc. according to the programmed burst order
Burst Length = 2, 4 or 8 in cases shown
Reads are to active rows in any banks
Shown with nominal tDQSCK, and tDQSQ

Figure 10
RANDOM READ ACCESSES – REQUIRED CAS LATENCIES

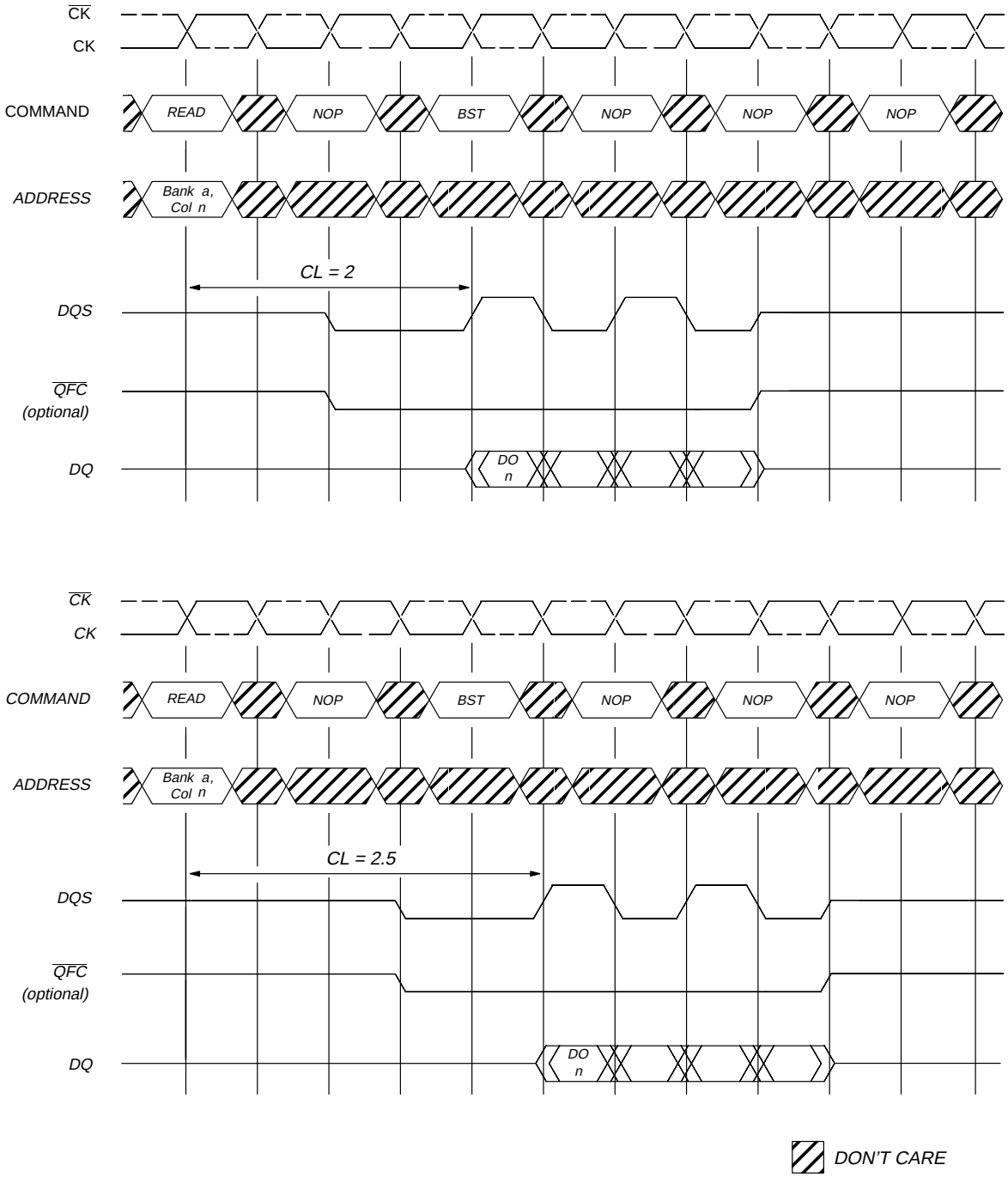
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs.

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued.

If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITEs).

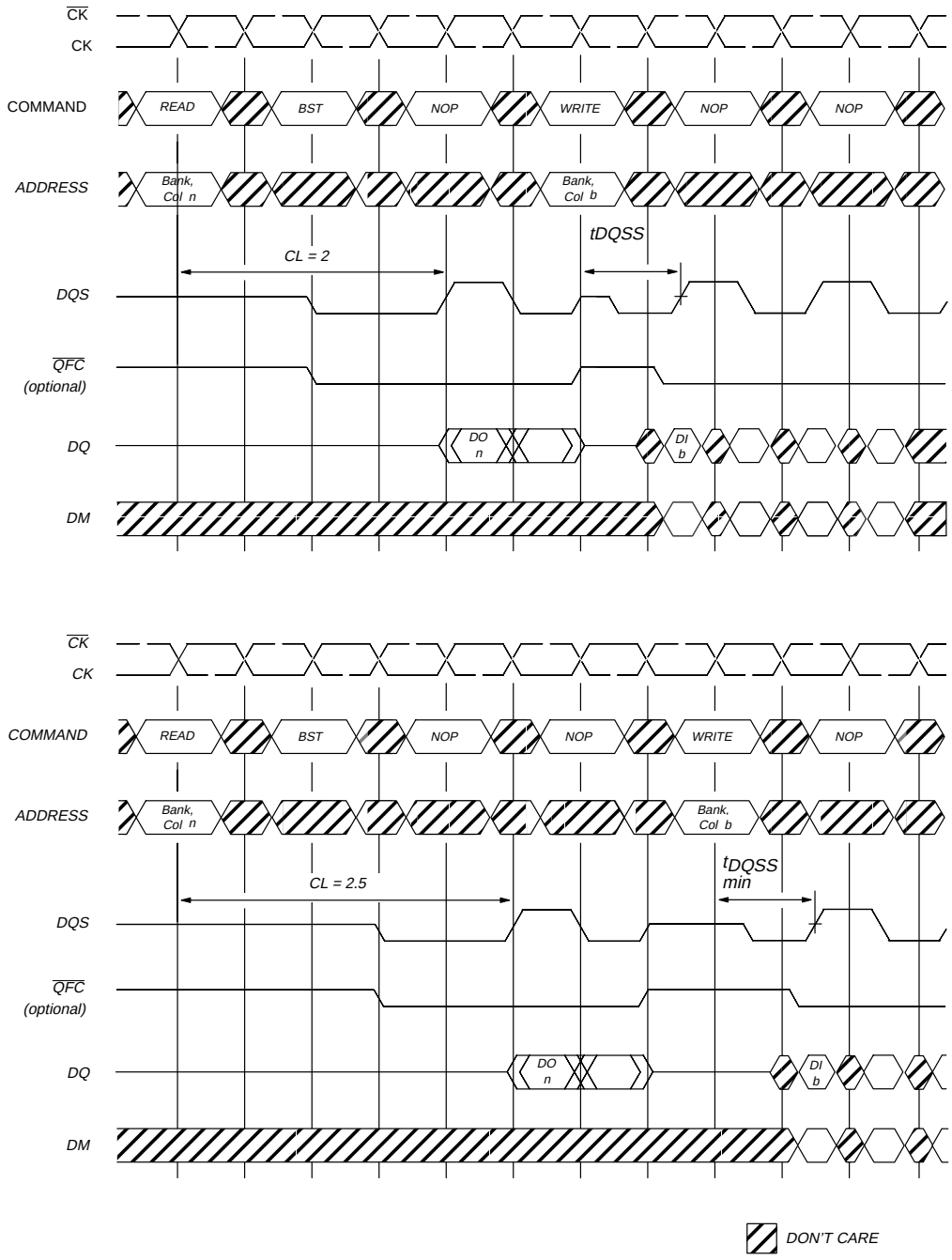
A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 13 for READ latencies of 2, and 2.5. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



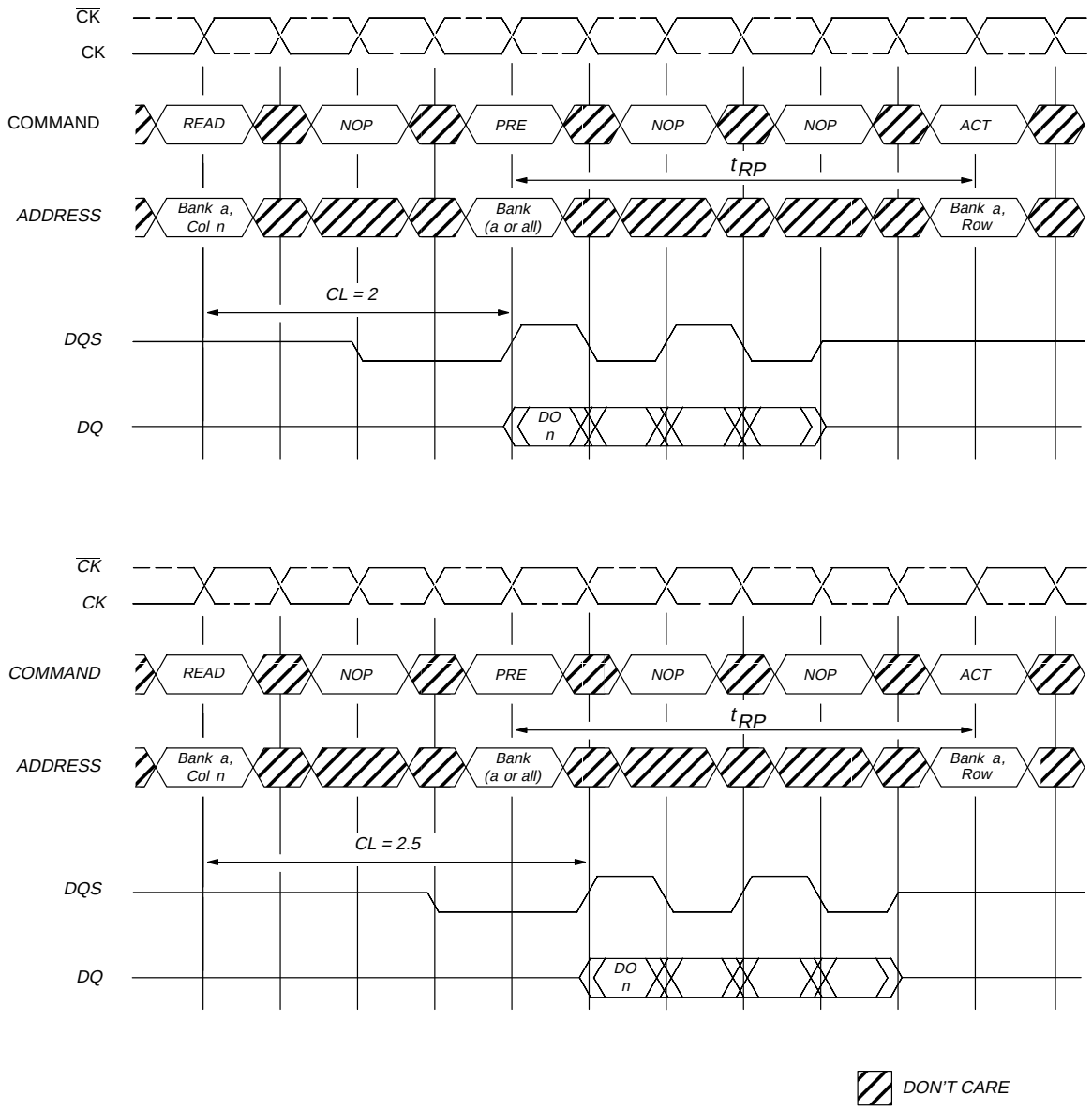
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 11
TERMINATING A READ BURST – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
1 subsequent element of Data Out appears in the programmed order following DO n
Data In elements are applied following DI b in the programmed order
Shown with nominal tDQSCK, and tDQSQ

Figure 12
READ TO WRITE – REQUIRED CAS LATENCIES



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 13
READ TO PRECHARGE – REQUIRED CAS LATENCIES

Writes

WRITE bursts are initiated with a WRITE command, as shown in Figure 14.

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data–in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data–in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle), so most of the WRITE diagrams that follow are drawn for the two extreme cases (i.e., tDQSS MIN and tDQSS MAX). Figures 15 and 16 show the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High–Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figures 17 and 18 show concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 19. Full–speed random write accesses within a page or pages can be performed as shown in Figures 20 and 21.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figures 22 and 23.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 24–27. Note that only the data–in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data–in must be masked with DM, as shown in Figures 24–27.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, tWR should be met as shown in Figures 28 and 29.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 30–33.

Note that only the data–in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data–in should be masked with DM, as shown in Figures 30–33. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

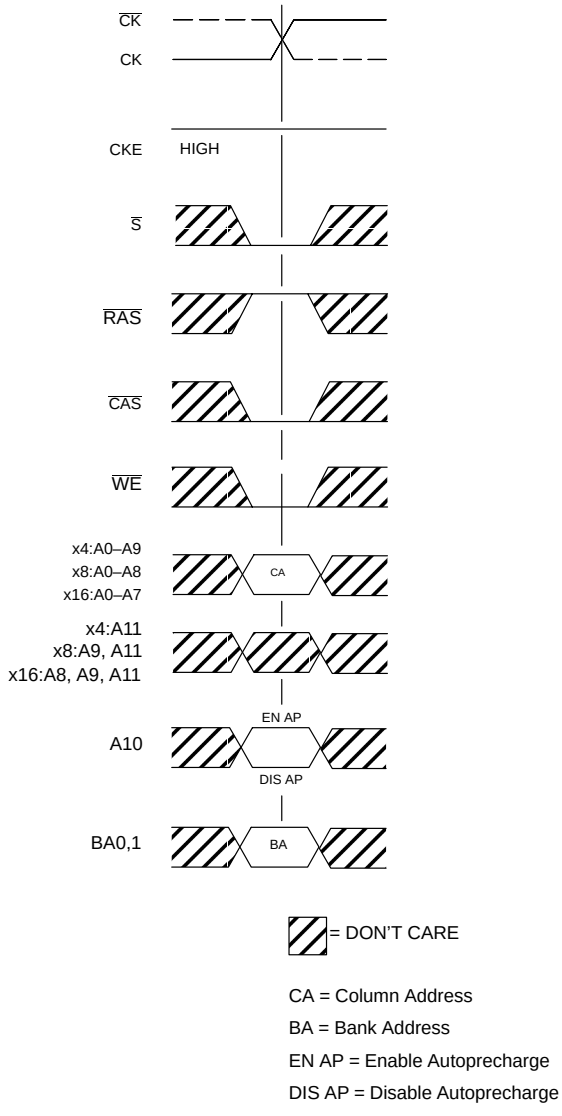
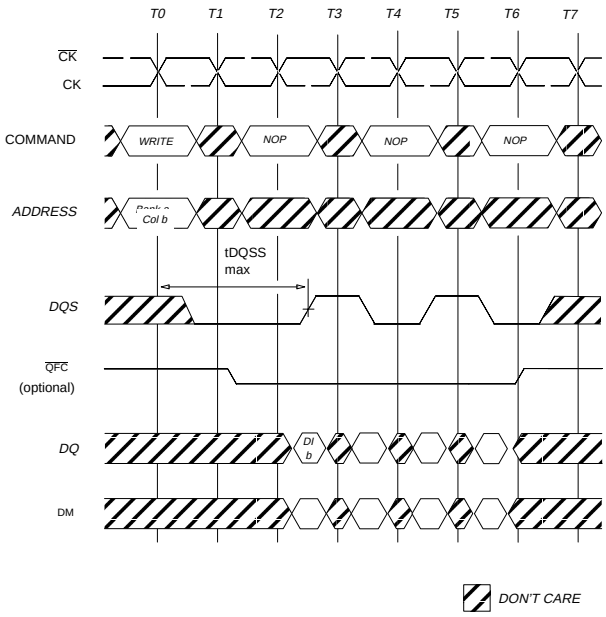
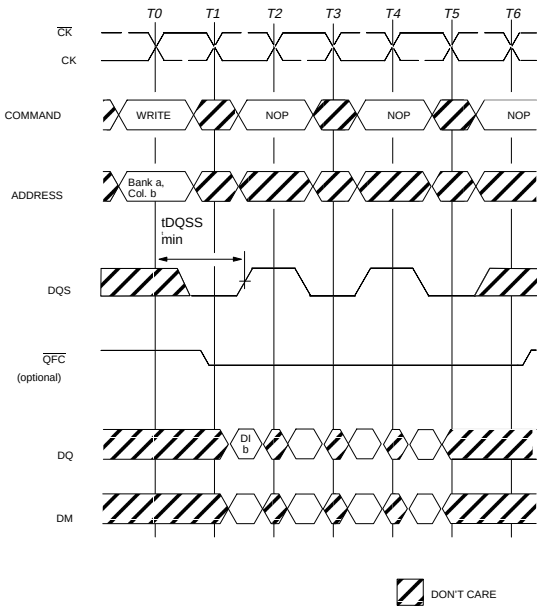


Figure 14
WRITE COMMAND



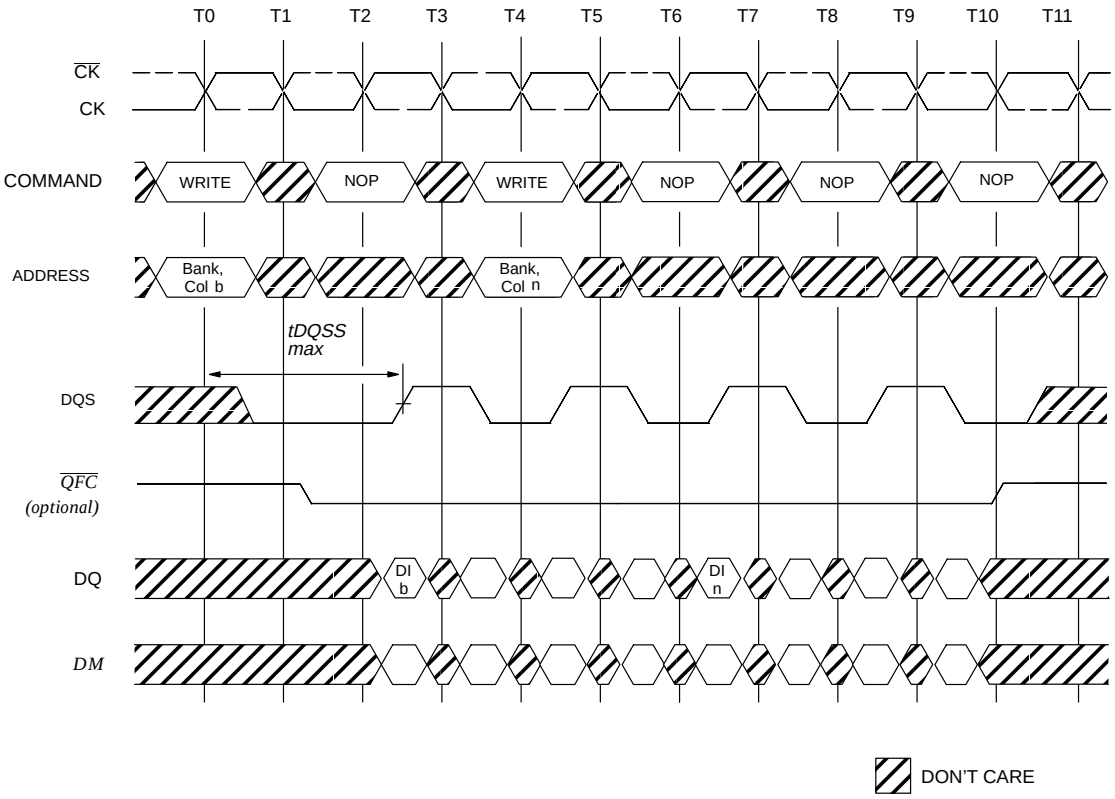
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI
A non–interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 15
WRITE TO WRITE – MAX DQSS



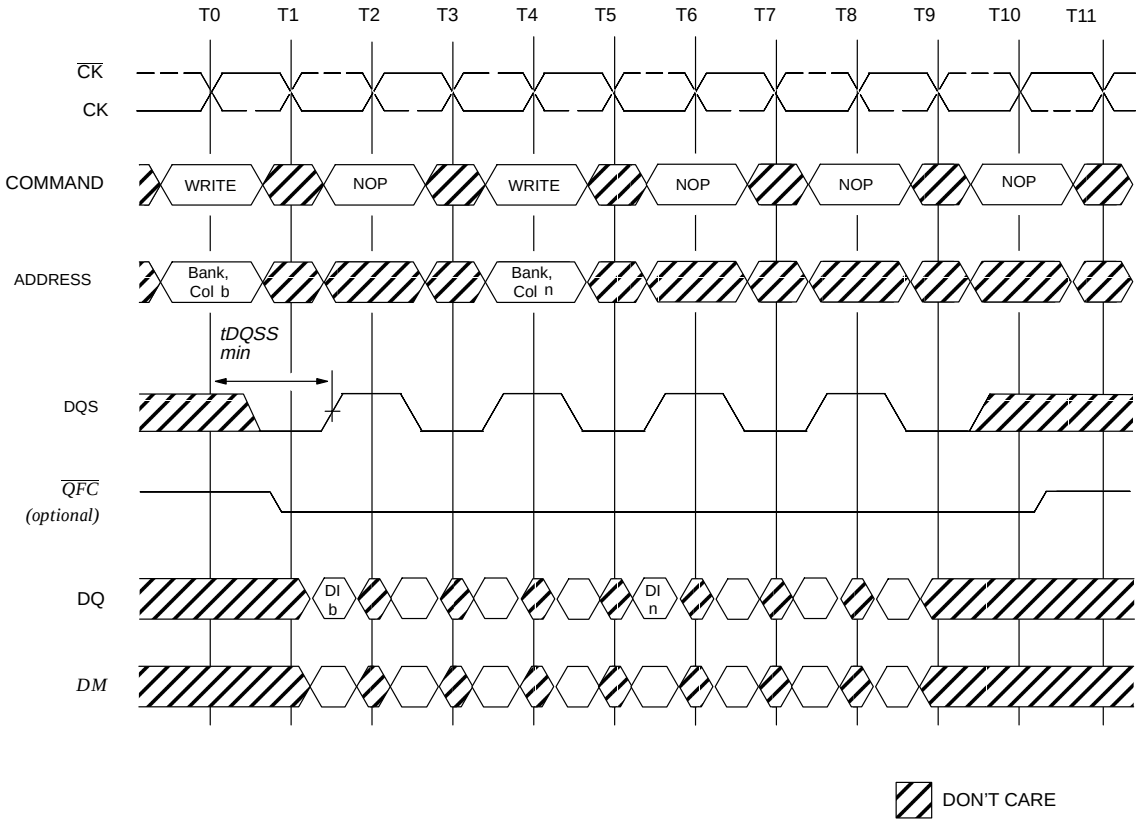
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non–interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 16
WRITE TO WRITE – MIN DQSS



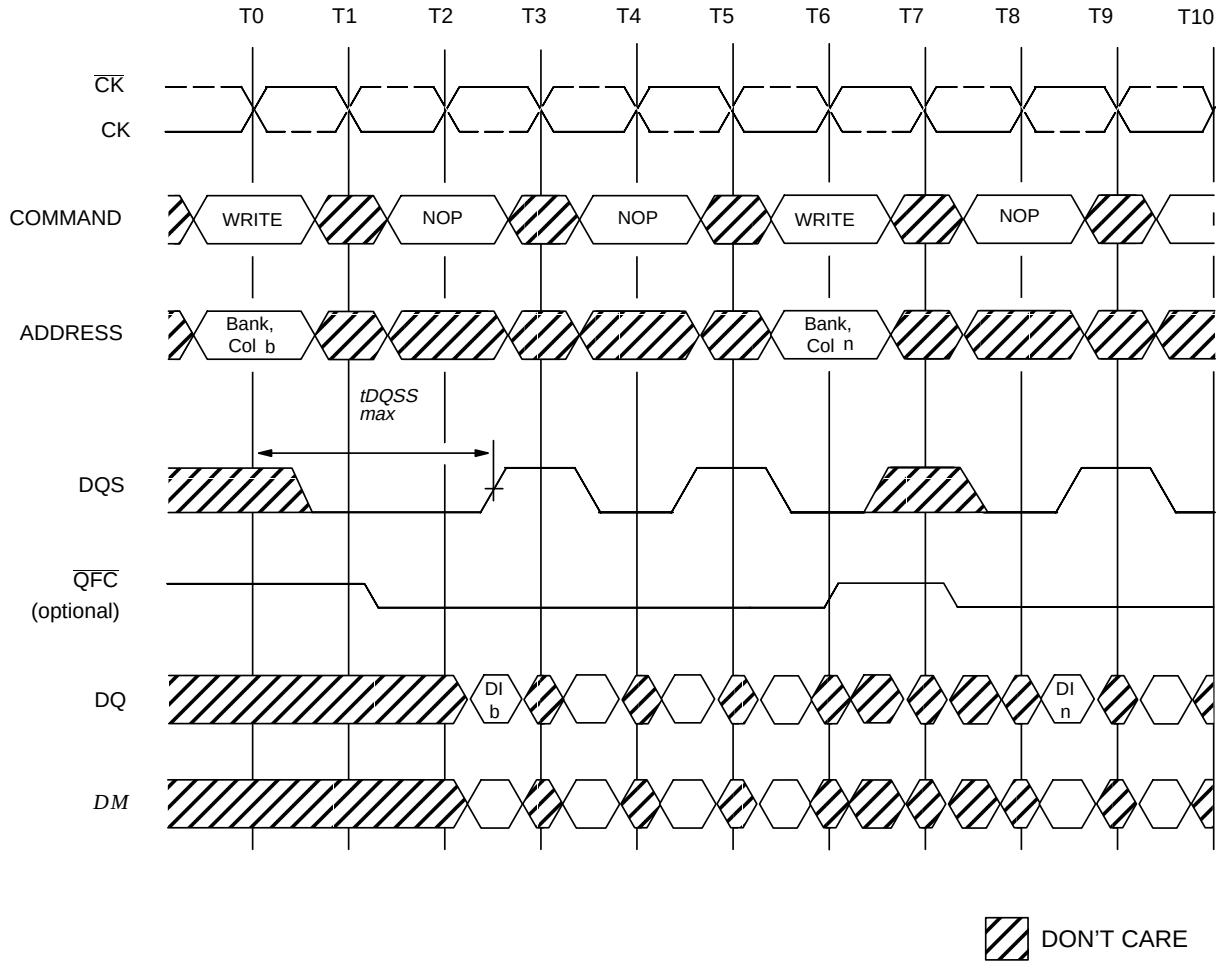
DI b, etc = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)
For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 17
WRITE TO WRITE – MAX DQSS



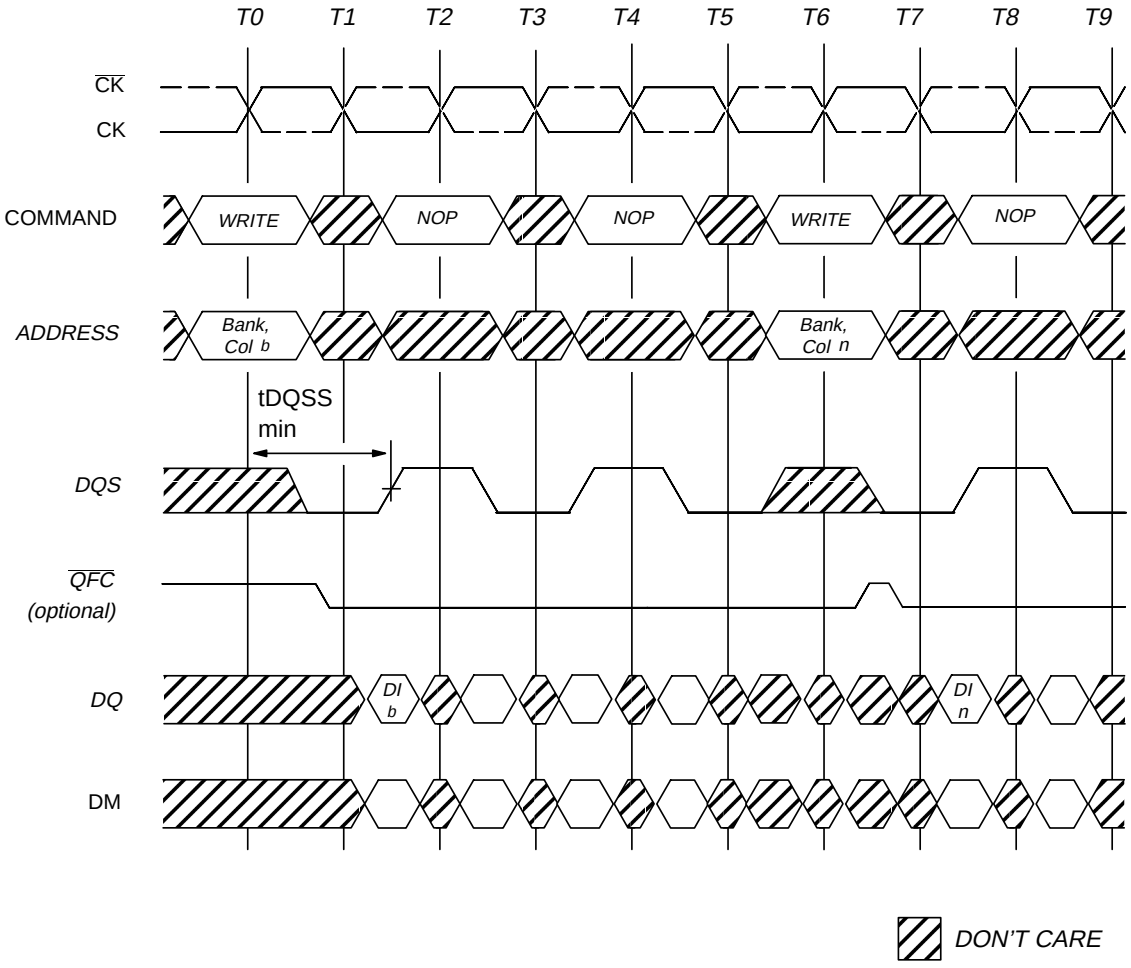
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
For system configurations using $\overline{\text{QFC}}$: the Write commands shown must be to the same device (but can be to any bank within the device)
Depending on external components, $\overline{\text{QFC}}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device
For system configurations not using $\overline{\text{QFC}}$: each Write command may be to any bank and may be to the same or different devices

Figure 18
WRITE TO WRITE – MIN DQSS,



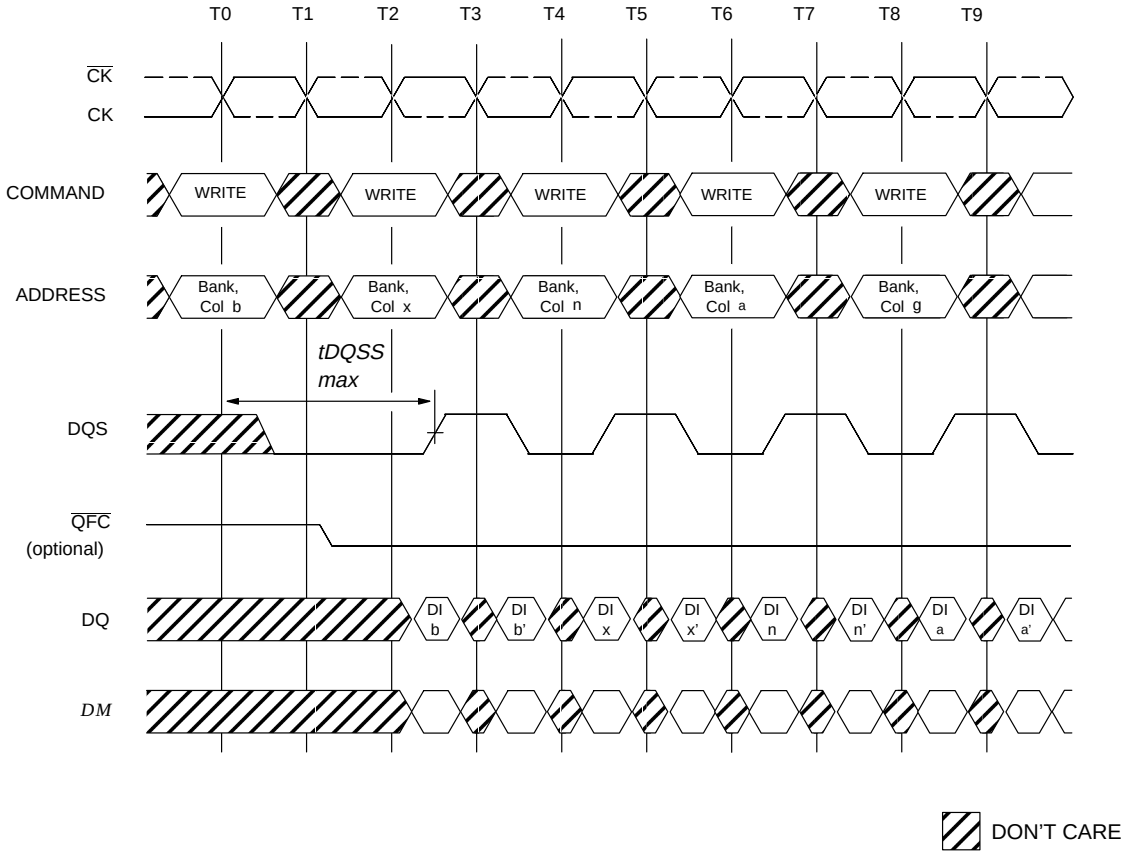
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
Each Write command may be to any bank and may be to the same or different devices

Figure 19 a
WRITE TO WRITE – MAX DQSS, NONCONSECUTIVE



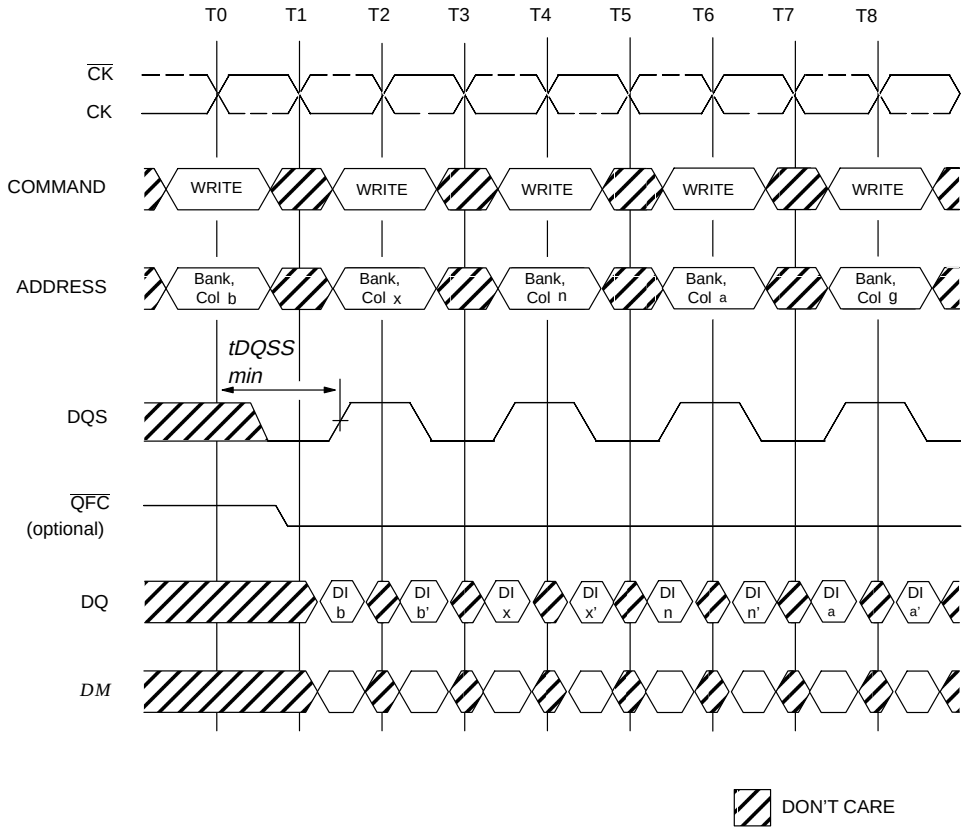
DI b, etc. = Data In for column b. etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
Each Write command may be to any bank, and may be to the same or different devices
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 19 b
WRITE TO WRITE – MIN DQSS, NONCONSECUTIVE



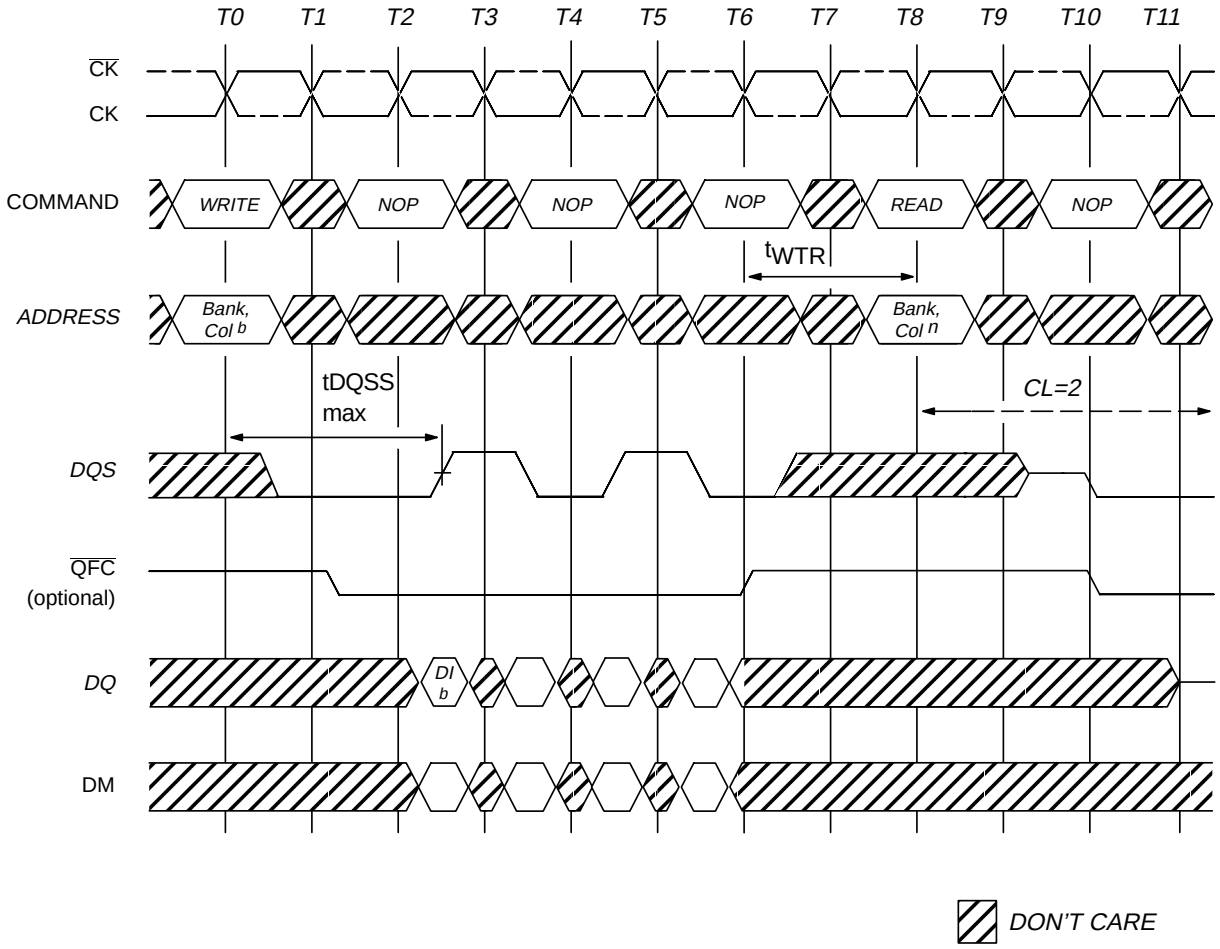
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order
Programmed Burst Length = 2, 4 or 8 in cases shown
For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)
For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 20
RANDOM WRITE CYCLES – MAX DQSS



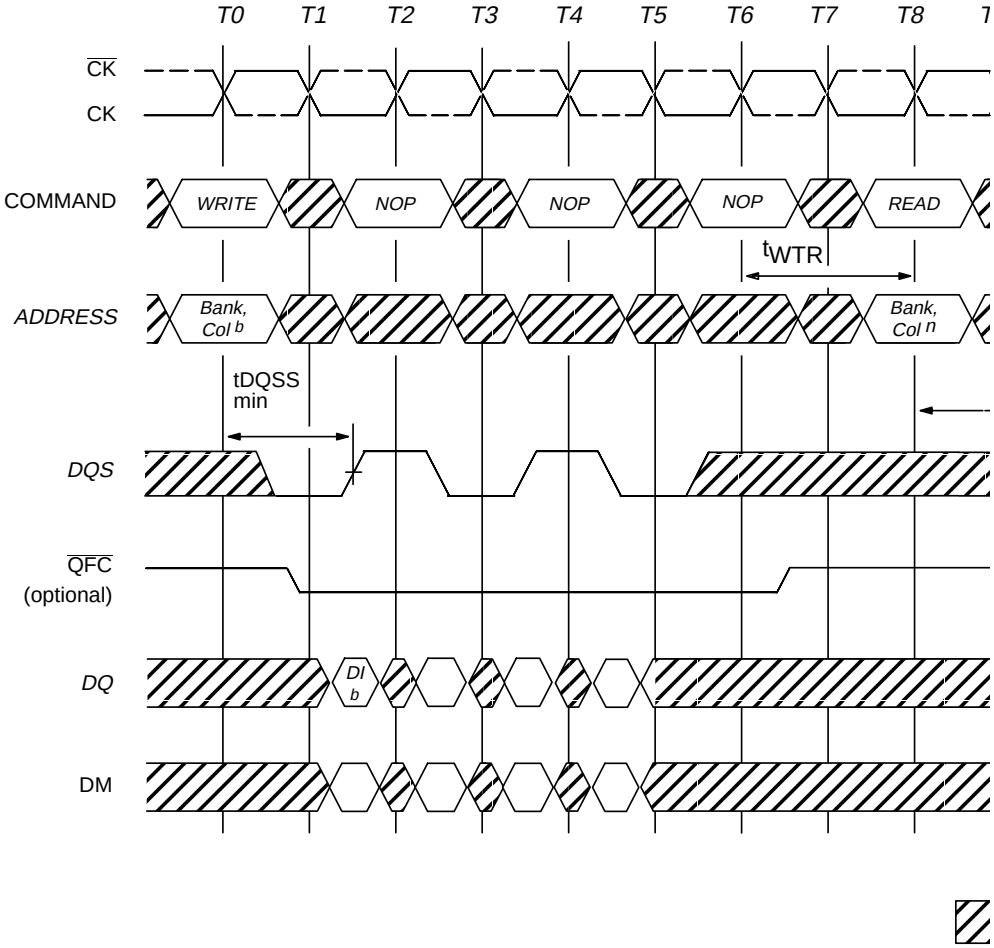
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b , etc., according to the programmed burst order
Programmed Burst Length = 2, 4 or 8 in cases shown
For system configurations using QFC: the Write commands shown must be to the same device (but can be to any bank within the device)
Depending on external components, QFC operation with min tDQSS might not be possible at the maximum operating frequency of the device
For system configurations not using QFC: each Write command may be to any bank and may be to the same or different devices

Figure 21
RANDOM WRITE CYCLES – MIN DQSS



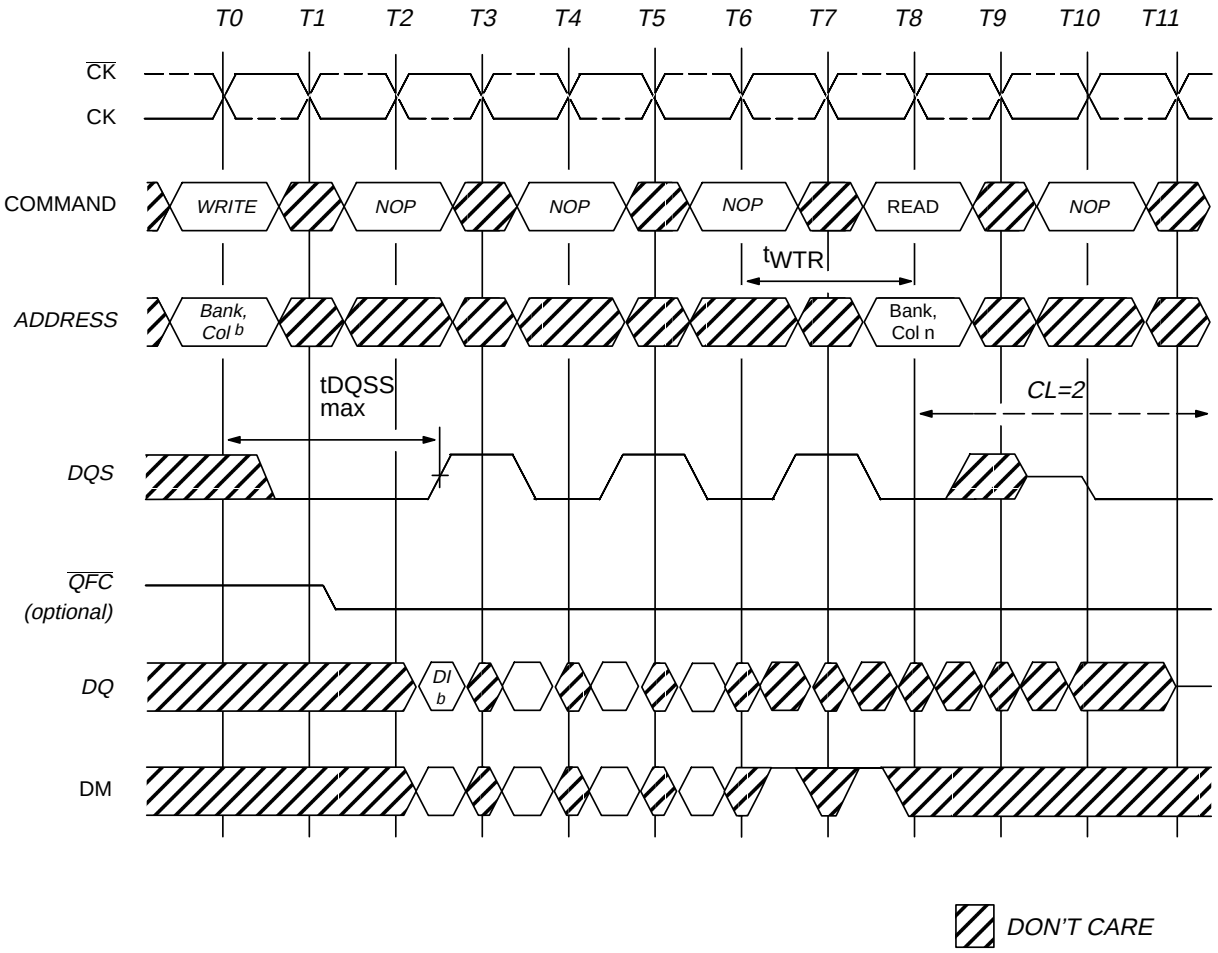
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non–interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands may be to any bank, and may be to the same or different devices
In the case where the READ and WRITE commands are to different devices, tWTR need not be met, and the READ command can be applied earlier
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)

Figure 22
WRITE TO READ – MAX DQSS, NONINTERRUPTING



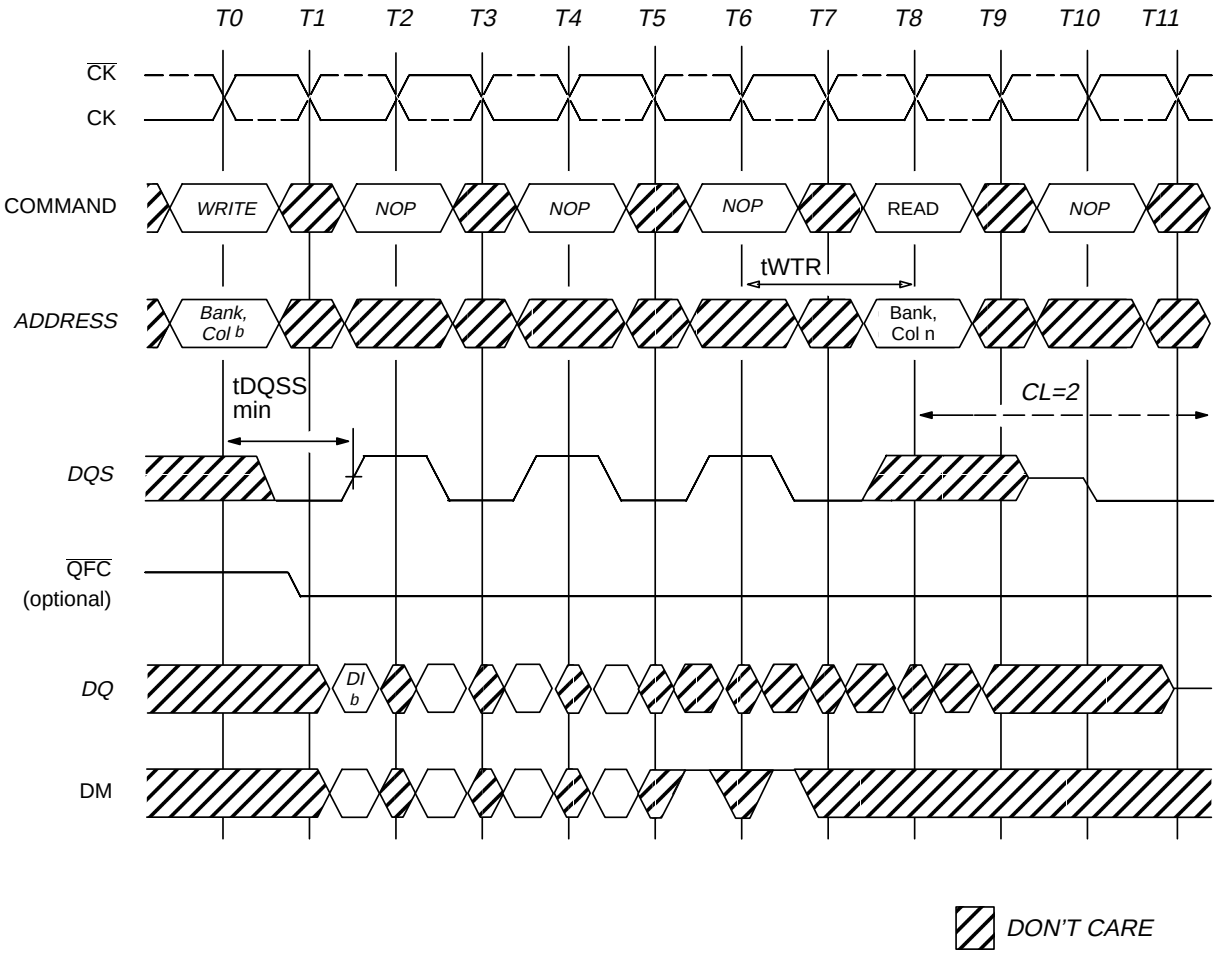
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following D
A non–interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands may be to any bank, and may be to the same o
In the case where the READ and WRITE commands are to different devices, tWTR
and the READ command can be applied earlier
tWTR = 2 tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be p
at the maximum operating frequency of the device

Figure 23
WRITE TO READ – MIN DQSS, NON–INTERRUPTING



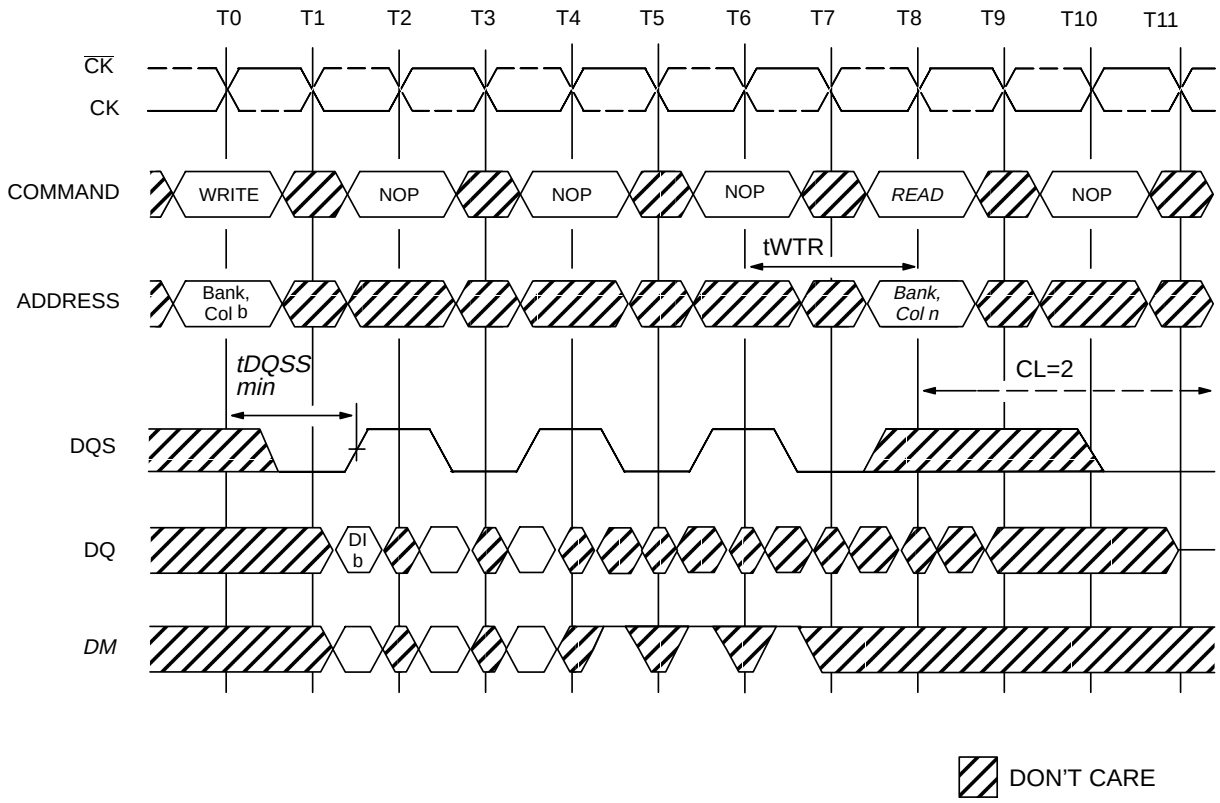
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank

Figure 24
WRITE TO READ – MAX DQSS, INTERRUPTING



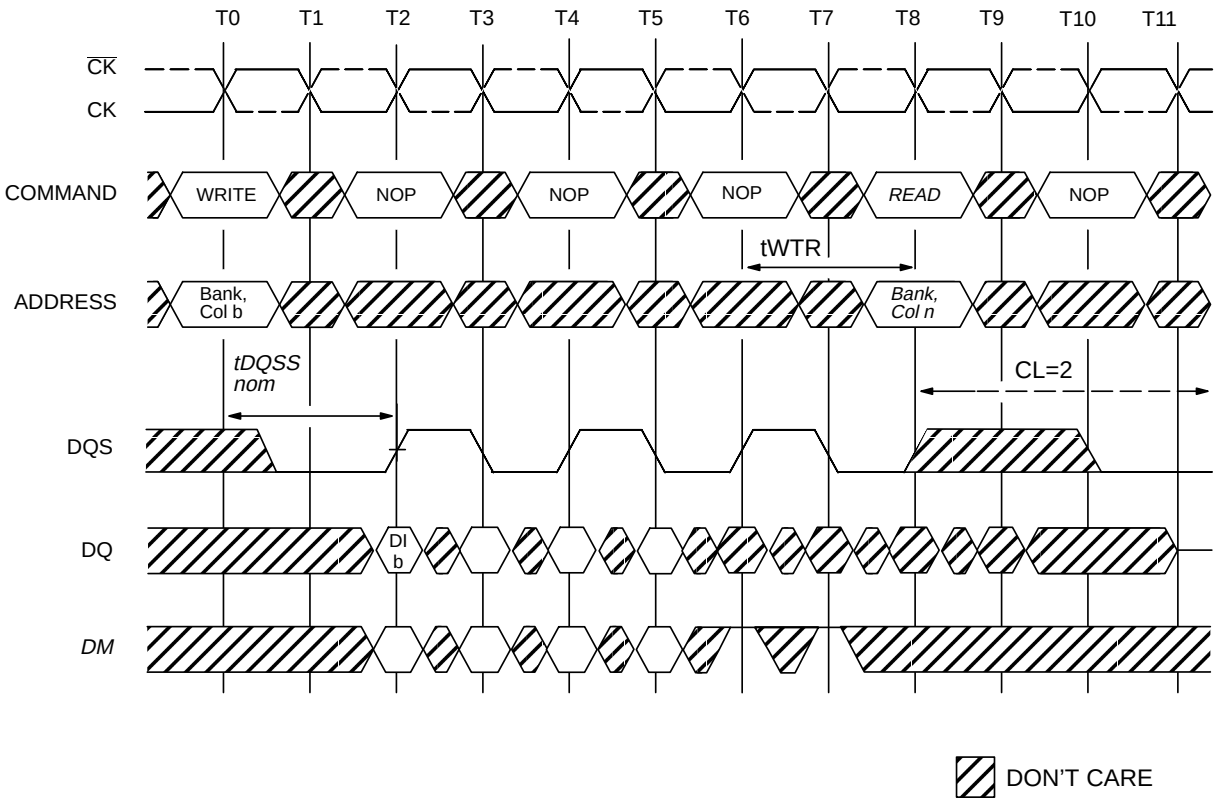
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last desired Data In pair
tWTR = 2 tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device, but not necessarily to the same bank
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 25
WRITE TO READ – MIN DQSS, INTERRUPTING



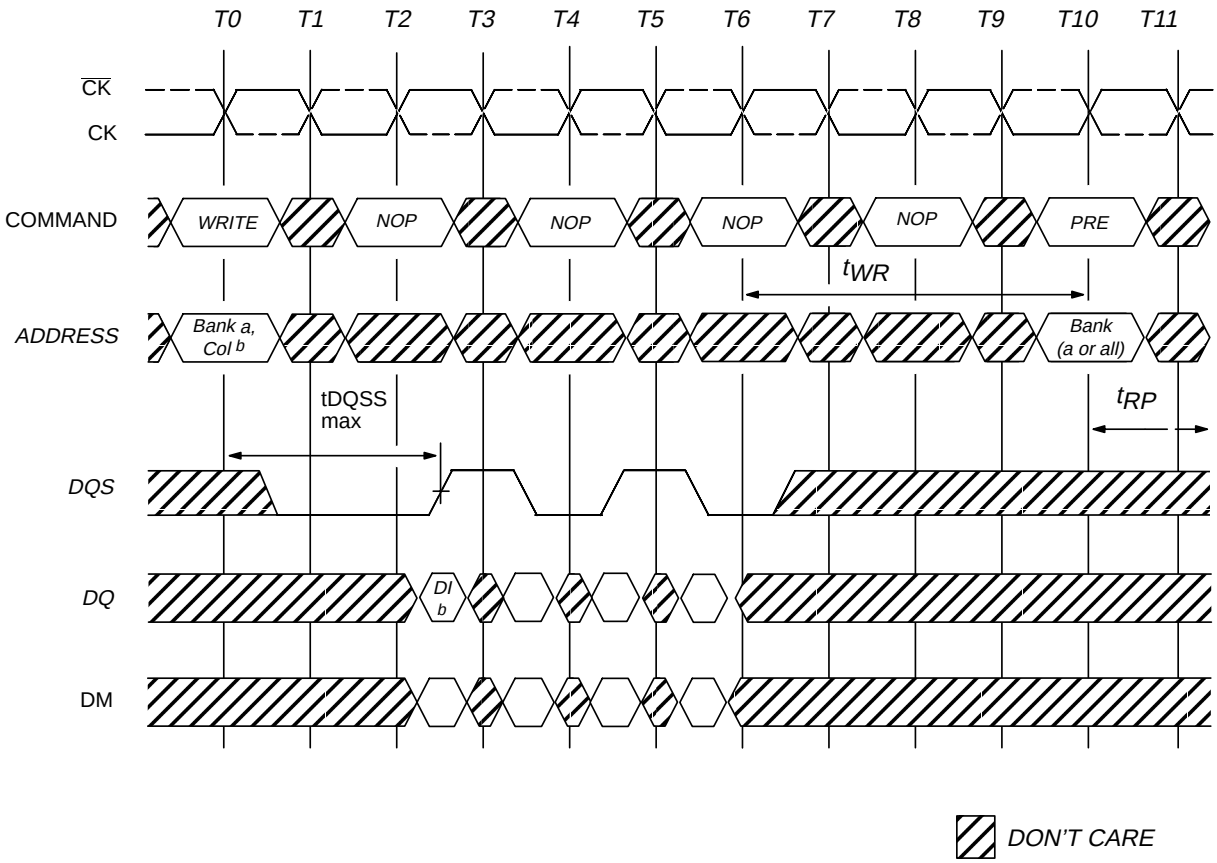
DI b = Data In for column b
An interrupted burst of 8 is shown, 3 data elements are written
2 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last desired Data In pair (not the last desired data in element)
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 26
WRITE TO READ – MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



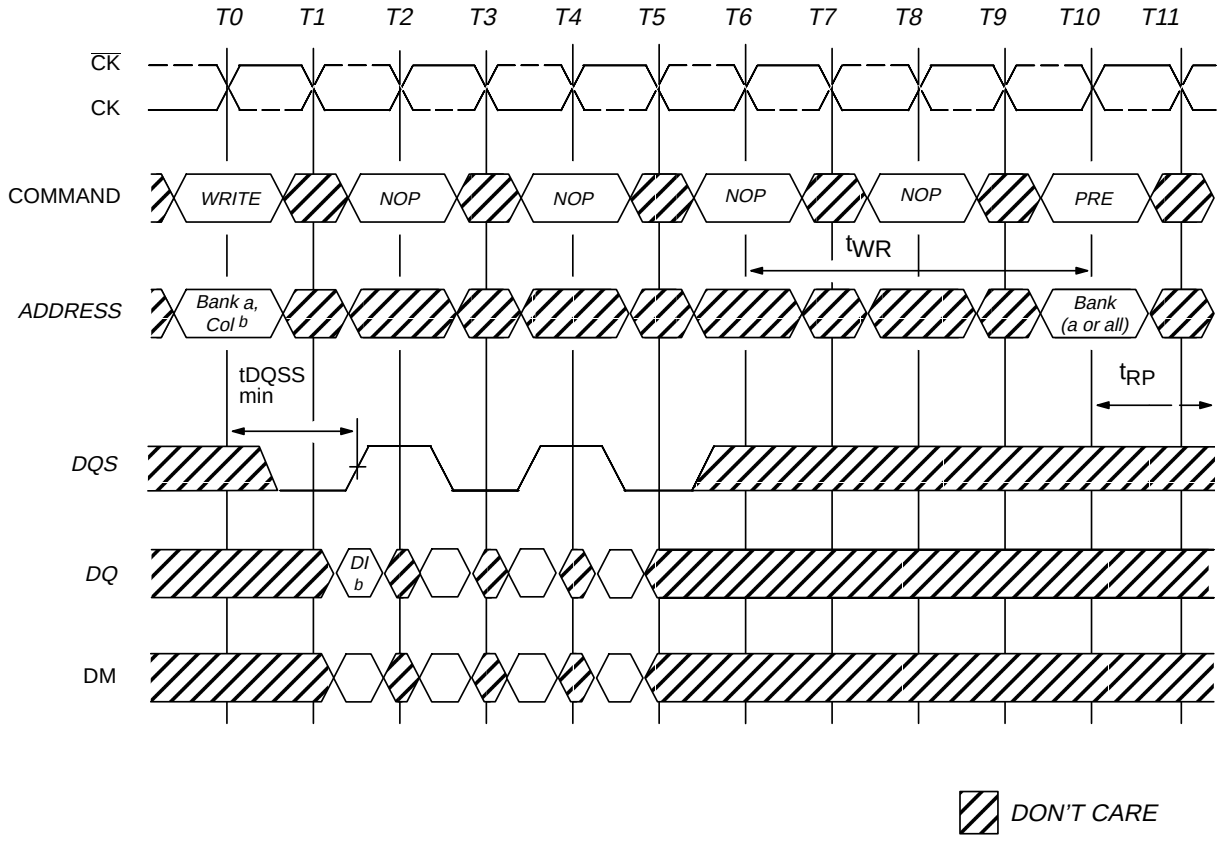
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last desired Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 27
WRITE TO READ – NOMINAL DQSS, INTERRUPTING



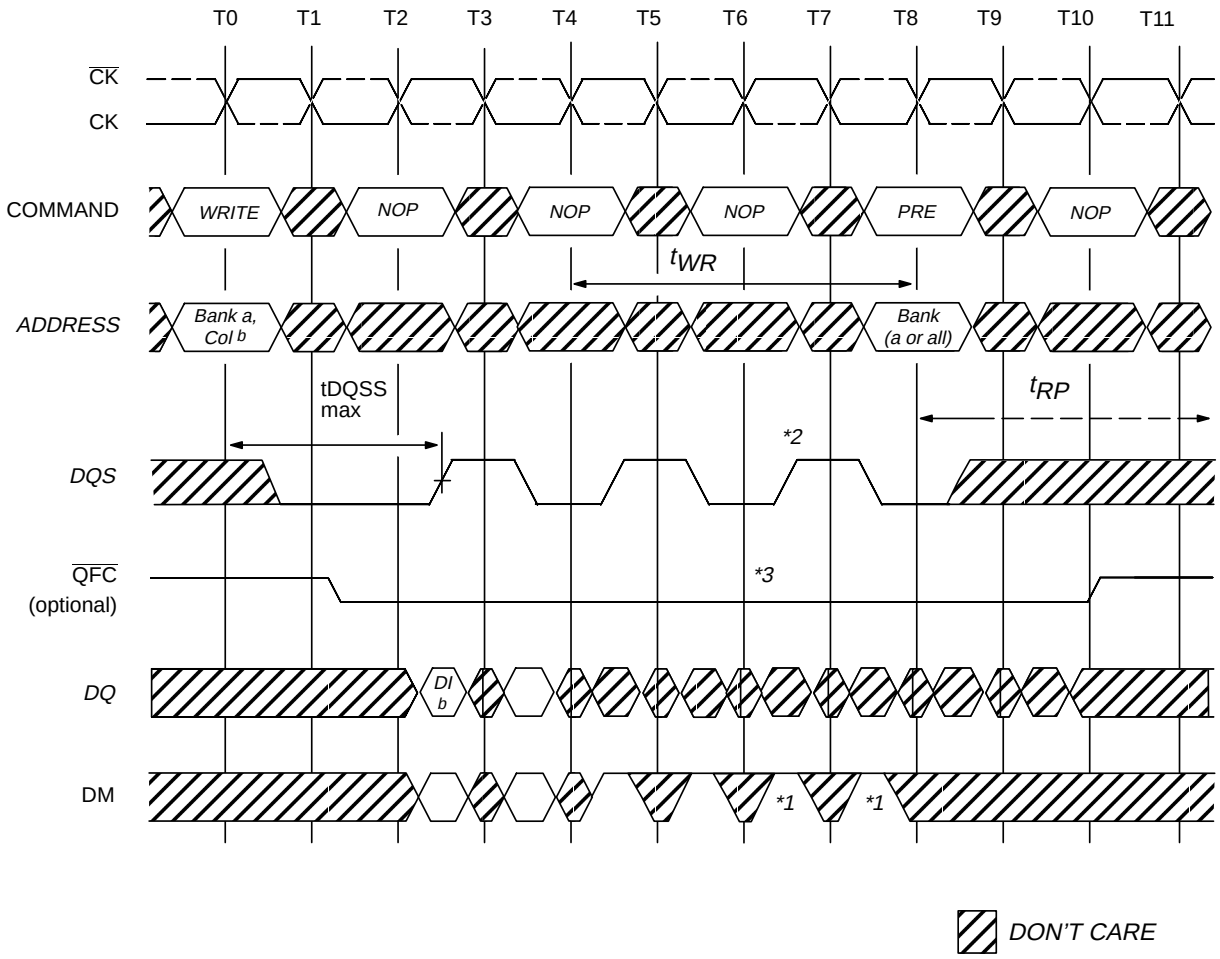
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A noninterrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 28
WRITE TO PRECHARGE – MAX DQSS, NON–INTERRUPTING



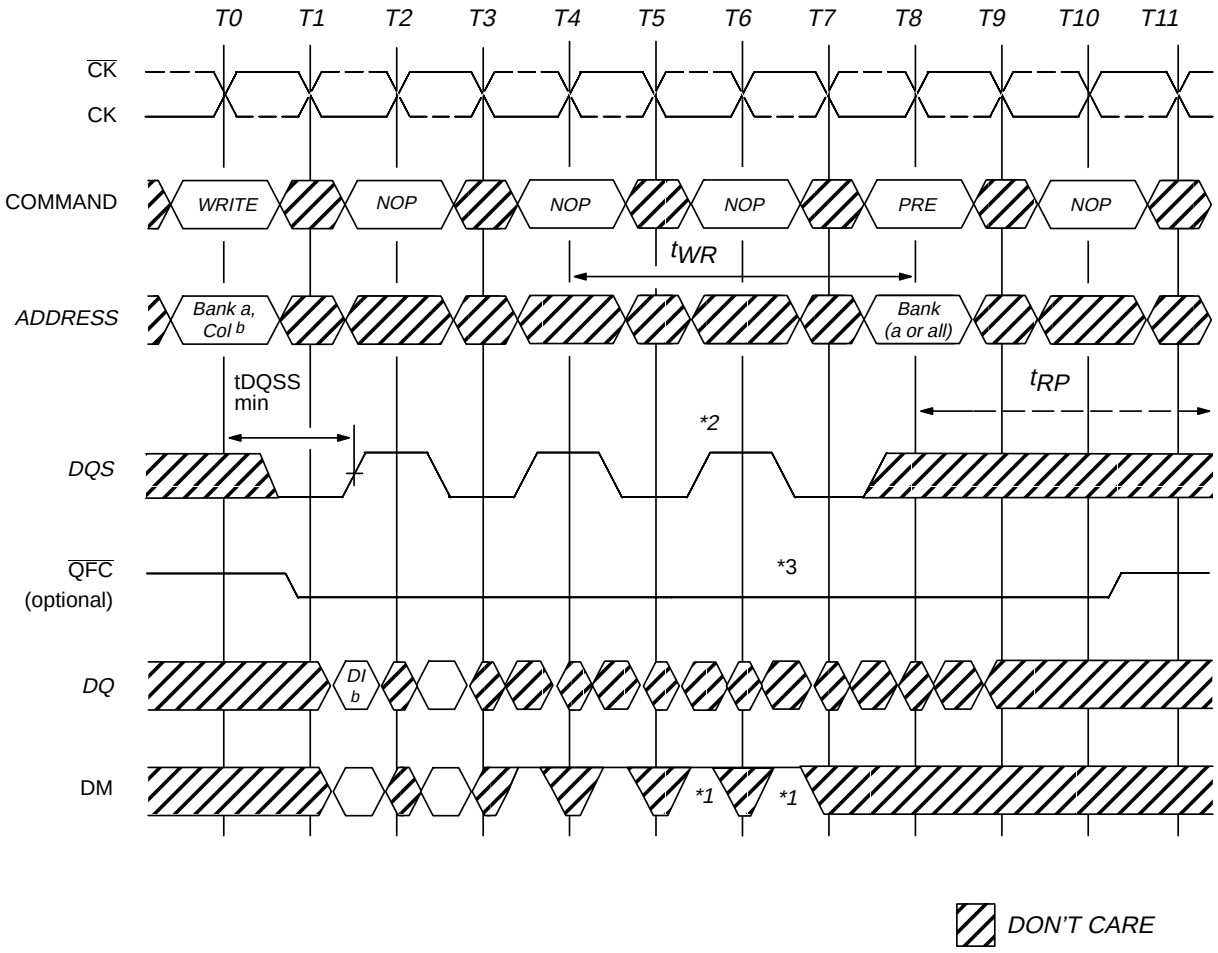
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A noninterrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 29
WRITE TO PRECHARGE – MIN DQSS, NON–INTERRUPTING



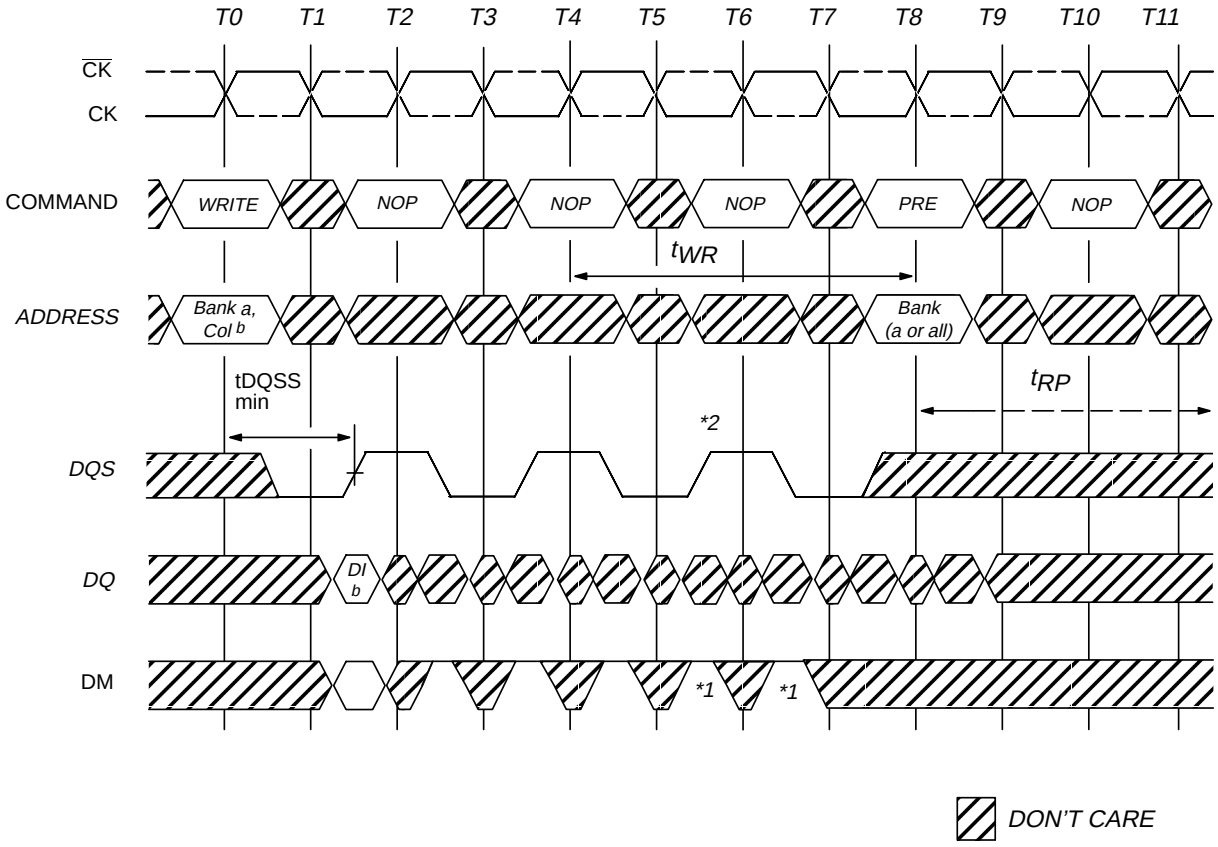
DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
**1 = can be don't care for programmed burst length of 4*
**2 = for programmed burst length of 4, DQS becomes don't care at this point*
**3 = for programmed burst length of 4, $\overline{QFC}$ becomes High–Z at this point*

Figure 30
WRITE TO PRECHARGE – MAX DQSS, INTERRUPTING



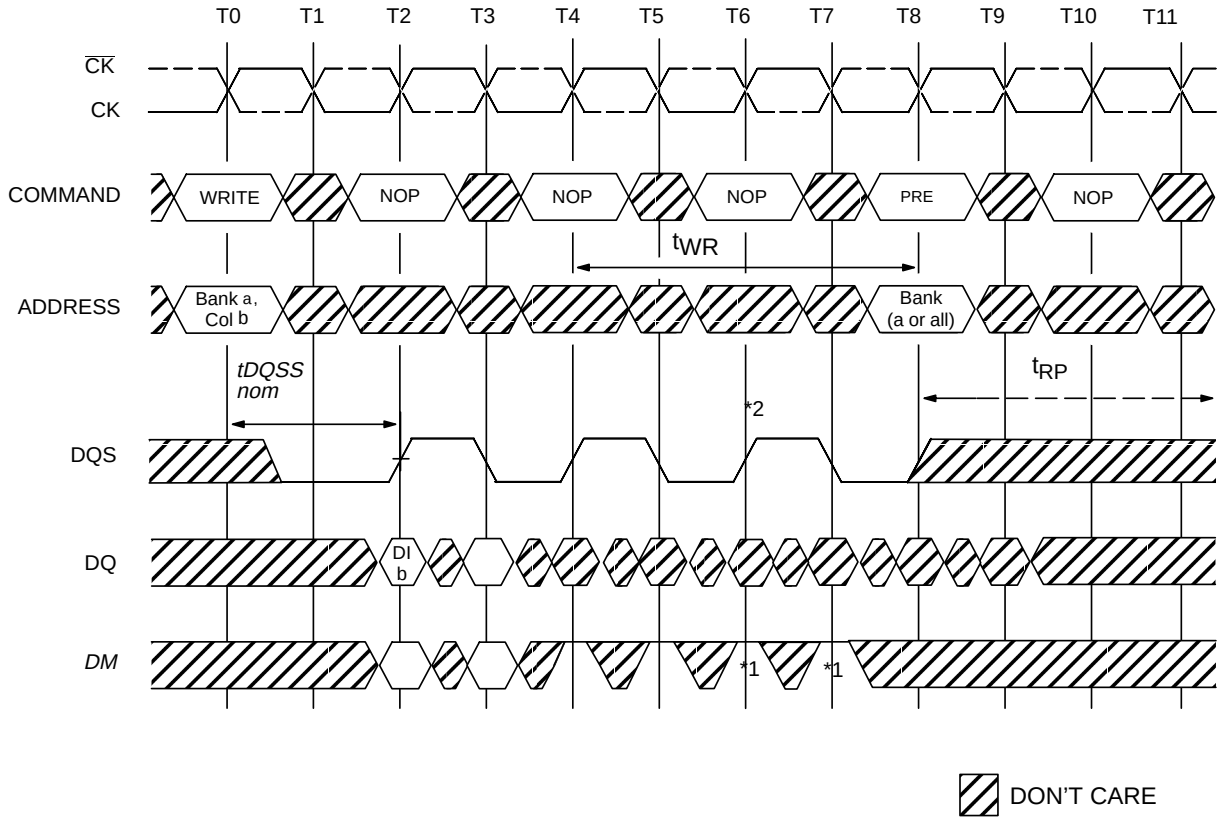
DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
**1 = can be don't care for programmed burst length of 4*
**2 = for programmed burst length of 4, DQS becomes don't care at this point*
**3 = for programmed burst length of 4, $\overline{QFC}$ becomes High–Z at this point*
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 31
WRITE TO PRECHARGE – MIN DQSS, INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
**1 = can be don't care for programmed burst length of 4*
**2 = for programmed burst length of 4, DQS becomes don't care at this point*

Figure 32
WRITE TO PRECHARGE – MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point

Figure 33
WRITE TO PRECHARGE – NOMINAL DQSS, INTERRUPTING

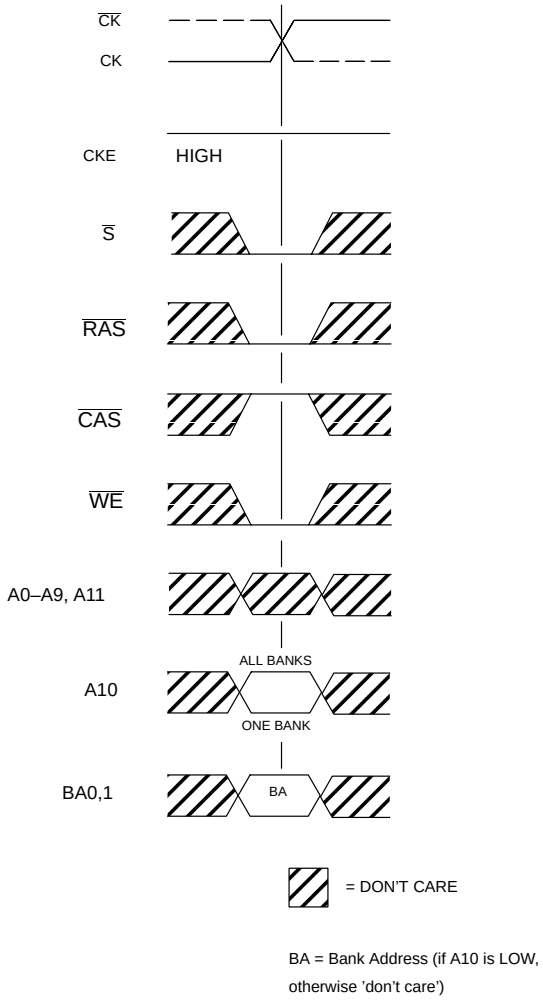


Figure 34
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as ”Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER–DOWN

Power–down is entered when CKE is registered low (no accesses can be in progress). If power–down occurs when all banks are idle, this mode is referred to as precharge power–down; if power–down occurs when there is a row active in any bank, this mode is referred to as active power–down. Entering power–down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power–down. In that case, the DLL must be enabled after exiting power–down, and 200 clock cycles must occur before a READ command can be issued. However, power–down duration is limited by the refresh requirements of the device, so in most applications, the self–refresh mode is preferred over the DLL–disabled power–down mode.

In power–down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are ”Don’t Care”.

The power–down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

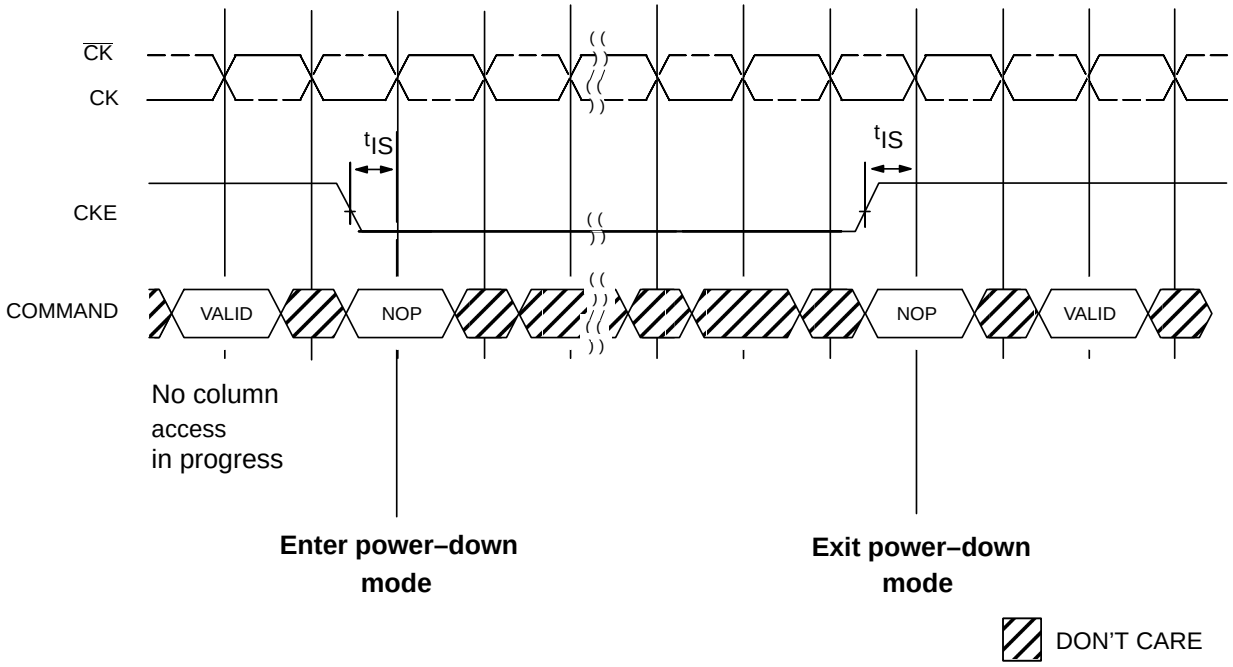


Figure 35
POWER–DOWN

(Notes: 1–4)

TRUTH TABLE 2 – CKE

CKEn–1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power–Down	X	Maintain Power–Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power–Down	DESELECT or NOP	Exit Power–Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power–Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power–Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn–1 was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.

4. All states and sequences not shown are illegal or reserved.

5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3 – Current State Bank n – Command to Bank n

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION(NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table is bank–specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and tRP has been met.
   - Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the ”row active” state.
   - Read w/Auto–Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE eabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
   - Write w/Auto–Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the ”all banks idle” state.

   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMTC is met, the DDR SDRAM will be in the ”all banks idle” state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank–specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank–specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank–specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.

TRUTH TABLE 4 – Current State Bank n – Command to Bank m

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto–Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	L	H	L	PRECHARGE	
Write (Auto–Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto–Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto–Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst) 3a,	7
	L	H	L	L	WRITE (select column and start new WRITE burst) 3a,	7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

NOTE: (continued)

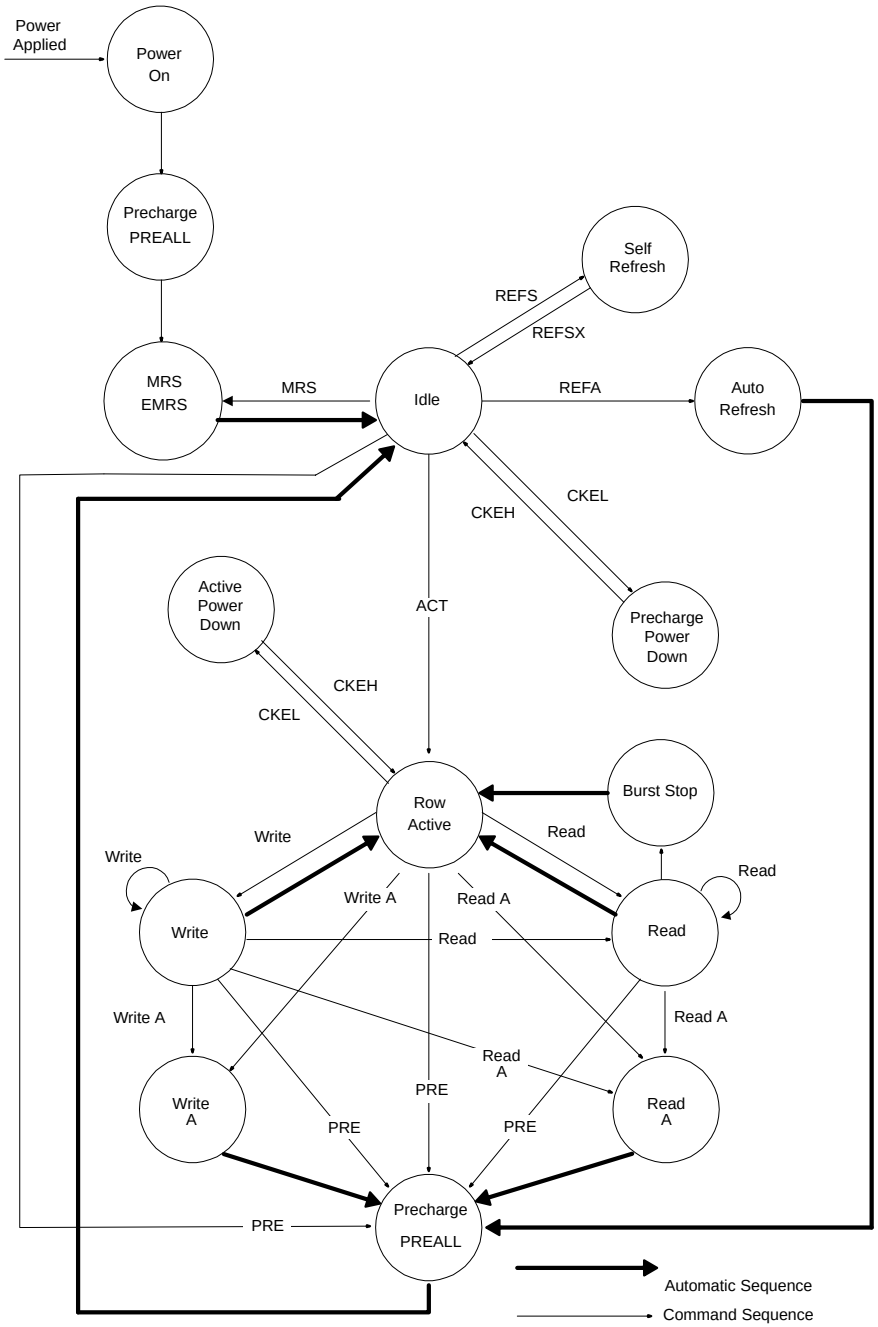
3. Current state definitions:

Idle:	The bank has been precharged, and tRP has been met.
Row Active:	A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
Read with Auto Precharge Enabled:	See following text
Write with Auto Precharge Enabled:	See following text

3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHAGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output.

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vdd Supply (For devices with nominal Vdd of 3.3 V)
Relative to Vss –1 V to +4.6 V
Voltage on Vdd Supply (For devices with nominal Vdd of 2.5 V)
Relative to Vss –1 V to +3.6 V
Voltage on VddQ Supply
Relative to Vss –1 V to +3.6 V
Voltage on Inputs
Relative to Vss –1 V to +3.6 V
Voltage on I/O Pins
Relative to Vss –0.5 V to VddQ+0.5 V

Operating Temperature, TA (ambient)	0 °C to +70 °C
Storage Temperature (plastic)	–55 °C to +150 °C
Power Dissipation	1 W
Short Circuit Output Current	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance:CK, $\overline{CK}$	Ci1	2.5	3.5	pF	13
Input Capacitance: All other input–only pins	Ci2	2.5	3.5	pF	13
Input/Output Capacitance: DQ, DQS, DM	Cio	4.0	5.0	pF	13
Delta Input/Output Capacitance: DQ, DQS, DM	Cdio	–	0.5	pF	13
Output Capacitance: ($\overline{QFC}$)	Co	TBD	TBD	pF	13

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.18	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	–0.3	VREF–0.18	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN(DC)	–0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	8
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	II	–2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	–5	5	µA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	 IOH IOL	 –15.2 15.2		 mA mA	

1) The full variation in driver pulldown current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of Figure a.
2) It is recommended that the ”typical” IBIS pulldown V–I curve lie within the shaded region of the V–I curve of Figure a.

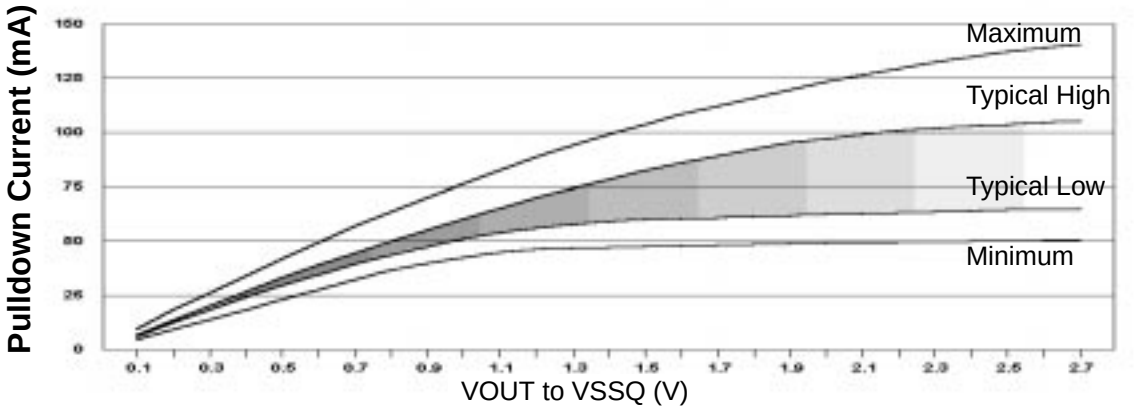


Figure a: Pulldown Characteristics

3) The full variation in driver pullup current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of Figure b.
4) It is recommended that the ”typical” IBIS pullup V–I curve lie within the shaded region of the V–I curve of Figure b.

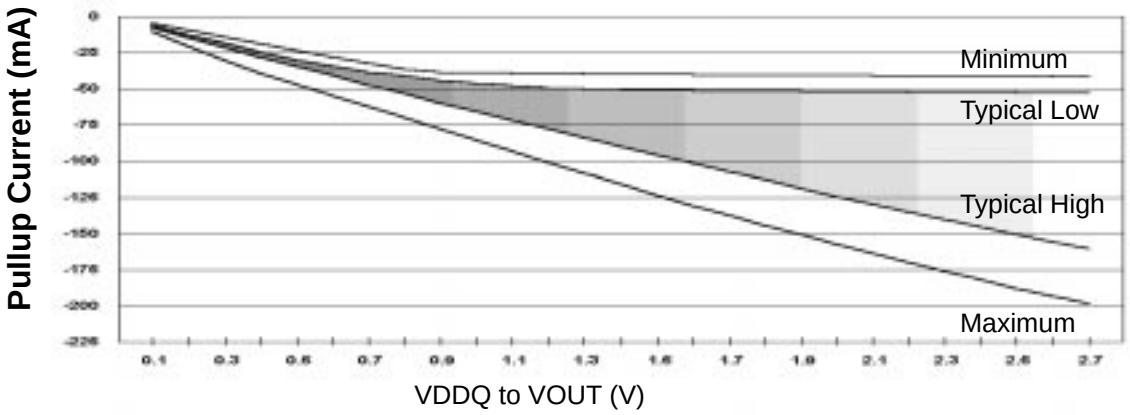


Figure b: Pull Up Characteristics

5) The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.
6) The full variation in the ratio of the ”typical” IBIS pullup to ”typical” IBIS pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.
7) These characteristics obey the SSTL_2 class II standard.
8) This specification is intended for DDR SDRAM only.

DATA DRIVER OUTPUT CHARACTERISTIC CURVES

	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.9	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	–155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	–160.1	–41.2	–198.2

Evaluation conditions:

Typical 25° C ($T_{Ambient}$), VDDQ=2.5 V, typical process

Minimum 70° C ($T_{Ambient}$), VDDQ=2.3 V, slow–slow process

Maximum 0° C ($T_{Ambient}$), VDDQ=2.7 V, fast–fast process

DATA DRIVER OUTPUT CHARACTERISTIC V–I DATA POINTS

AC OPERATING CONDITIONS

(Notes: 1–5, 14, 16) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(ac)	VREF + 0.35		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(ac)		VREF –.35	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(ac)	0.7	VDDQ + 0.6	V	8
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(ac)	0.5*VDDQ–0.2	0.5*VDDQ+0.2	V	9

IDD SPECIFICATIONS AND CONDITIONS

(Notes: 1–5, 12, 14) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

		MAX		
PARAMETER/CONDITION	SYMBOL		UNITS	NOTES
OPERATING CURRENT: One Bank; Active–Precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cyle; address and control inputs changing once per clock cycle	IDD0	V/DS*	mA	
OPERATING CURRENT: One Bank; Active–Read–Precharge; Burst = 2; tRC = tRC MIN; CL = 2.5; tCK = tCK MIN; Iout = 0 mA; Address and control inputs changing once per clock cycle	IDD1	V/DS*	mA	
PRECHARGE POWER–DOWN STANDBY CURRENT: All banks idle; power–down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD2P	V/DS*	mA	
IDLE STANDBY CURRENT: $\overline{S}$ ≥ Vih (MIN); All banks idle; CKE ≥ Vih (MIN); tCK = tCK MIN; Address and other control inputs changing once per clock cycle	IDD2N	V/DS*	mA	
ACTIVE POWER–DOWN STANDBY CURRENT: One bank active; power–down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD3P	V/DS*	mA	
ACTIVE STANDBY CURRENT: $\overline{S}$ ≥ Vih (MIN); CKE ≥ Vih (MIN); One bank; Active–Precharge; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	V/DS*	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = tCK MIN; Iout = 0 mA	IDD4R	V/DS*	mA	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle	IDD4W	V/DS*	mA	
AUTO REFRESH CURRENT: tRC = tRFC (MIN)	IDD5	V/DS*	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2 V	IDD6	V/DS*	mA	11

V/DS* = Vendor/Device Specific

ELECTRICAL CHARACTERISTICS AND AC TIMING for DDR–266/DDR–200 –

Absolute Specifications

(Notes: 1–5, 14–17) (0°C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		DDR–266A		DDR–266B		DDR–200			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQ output access time from CK/$\overline{CK}$	tAC	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	
CK high–level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low–level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)		min(tCL, tCH)		min(tCL, tCH)		ns	29
Clock cycle time CL = 2.5	tCK	7	15	7.5	15	8	15	ns	
CL = 2	tCK	7.5	15	10	15	10	15	ns	
DQ and DM input hold time	tDH	0.5		0.5		0.6		ns	
DQ and DM input setup time	tDS	0.5		0.5		0.6		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.5		ns	27
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		2		ns	27
Data–out high–impedance time from CK/$\overline{CK}$	tHZ	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	18
Data–out low–impedance time from CK/$\overline{CK}$	tLZ	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	18
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5		+0.5		+0.6	ns	
DQS–DQ Skew (for DQS and all DQ signals)	tDQSQA		+0.5		+0.5		+0.6	ns	
DQ/DQS output hold time from DQS	tQH	tHP–0.75		tHP–0.75		tHP–1.0		ns.	30
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	15		15		16		ns	
Write preamble setup time	tWPRES	0		0		0		ns	22
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.40	0.60	tCK	19
Write preamble	tWPRE	0.25		0.25		0.25		tCK	
Address and Control input hold time (fast slew rate)	tIH	0.9		0.9		1.2		ns	24,26,27
Address and Control input setup time (fast slew rate)	tIS	0.9		0.9		1.2		ns	25,26,27
Address and Control input hold time (slow slew rate)	tIH	1.0		1.0		1.2		ns	25,26,27
Address and Control input setup time (slow slew rate)	tIS	1.0		1.0		1.2		ns	25,26,27
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
$\overline{QFC}$ preamble during reads	tQPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
$\overline{QFC}$ postamble during reads	tQPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
$\overline{QFC}$ output access time from CK/$\overline{CK}$, for writes	tQCK		4		4		4	ns	
$\overline{QFC}$ output hold time for writes	tQOH	1.25	2.0	1.25	2.0	1.25	2.0	ns	
ACTIVE to PRECHARGE command	tRAS	45	120,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	65		65		70		ns	
Auto Refresh to Active/Auto Refresh command period	tRFC	75		75		80		ns	
ACTIVE to READ or WRITE delay	tRCD	20		20		20		ns	
PRECHARGE command period	tRP	20		20		20		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	15		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	35		35		35		ns	
Internal Write to Read Command Delay	tWTR	1		1		1		tCK	
Exit self refresh to non–READ command	tXSNR	75		75		80		ns	
Exit self refresh to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval	tREFI		15.6		15.6		15.6	µs	23

ELECTRICAL CHARACTERISTICS AND AC TIMING for DDR–266 –

Applicable Specifications Expressed in Clock Cycles

(Notes: 1–5, 14–17) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V,
VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		tCK = 7.5 ns			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQ output access time from CK/$\overline{CK}$	tAC	–0.75	+0.75	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	–0.75	+0.75	ns	
CK high–level width	tCH	3.4	4.1	ns	
CK low–level width	tCL	3.4	4.1	ns	
CK half period	tHP	min(tCL, tCH)		ns	29
DQ and DM input hold time	tDH	0.5		ns	
DQ and DM input setup time	tDS	0.5		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		ns	27
DQ and DM input pulse width (for each input)	tDIPW	1.75		ns	27
Data–out high–impedance time from CK/$\overline{CK}$	tHZ	–0.75	+0.75	ns	18
Data–out low–impedance time from CK/$\overline{CK}$	tLZ	–0.75	+0.75	ns	18
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5	ns	
DQS–DQ Skew (for DQS and all DQ signals)	tDQSQA		+0.5	ns	
DQ/DQS output hold time	tQH	tHP–0.75		ns	30
Write command to first DQS latching transition	tDQSS	5.6	9.4	ns	
DQS input high pulse width	tDQSH	2.63		ns	
DQS input low pulse width	tDQSL	2.63		ns	
DQS falling edge to CK setup time	tDSS	1.5		ns	
DQS falling edge hold time from CK	tDSH	1.5		ns	
MODE REGISTER SET command cycle time	tMRD	2		tCK	
Write preamble setup time	tWPRES	0		ns	22
Write postamble	tWPST	3	4.5	ns	19
Write preamble	tWPRE	0.25			
Address and Control input hold time (fast slew rate)	tIH	0.9		ns	24,26,27
Address and Control input setup time (fast slew rate)	tIS	0.9		ns	24,26,27
Address and Control input hold time (slow slew rate)	tIH	1.0		ns	25,26,27
Address and Control input setup time (slow slew rate)	tIS	1.0		ns	25,26,27
Read preamble	tRPRE	6.75	8.25	ns	
Read postamble	tRPST	3	4.5	ns	
$\overline{QFC}$ preamble during reads	tQPRE	6.75	8.25	ns	
$\overline{QFC}$ postamble during reads	tQPST	3	4.5	ns	
$\overline{QFC}$ output access time from CK/$\overline{CK}$, for writes	tQCK		4	ns	
$\overline{QFC}$ output hold time for writes	tQOH	1.25	2.0	ns	
ACTIVE to PRECHARGE command	tRAS	6	16000	tCK	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	9		tCK	
Auto Refresh to Active/Auto Refresh command period	tRFC	10		tCK	
ACTIVE to READ or WRITE delay	tRCD	3		tCK	
PRECHARGE command period	tRP	3		tCK	
ACTIVE bank A to ACTIVE bank B command	tRRD	2		tCK	
Write recovery time	tWR	2		tCK	
Auto Precharge write recovery + precharge time	tDAL	5		tCK	
Internal Write to Read Command Delay	tWTR	1		tCK	
Exit self refresh to non–READ command	tXSNR	10		tCK	
Exit self refresh to READ command	tXSRD	200		tCK	
Average Periodic Refresh Interval	tREFI	15.6		µs	23

NOTES

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 36 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

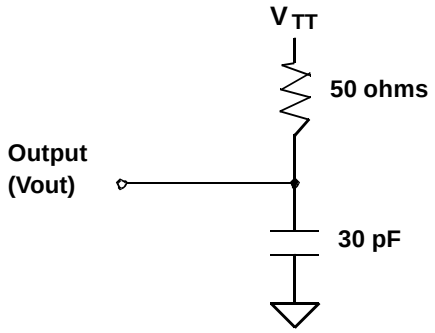
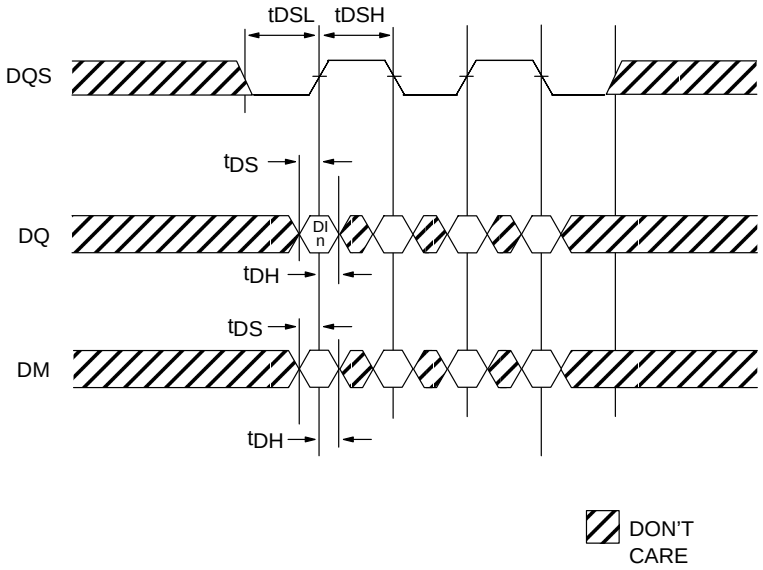


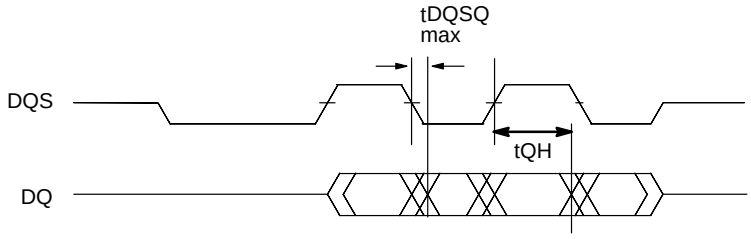
Figure 36: Timing Reference Load

4. ac timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/$\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak–to–peak noise on VREF may not exceed +/–2% of the dc value.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
8. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
9. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
11. Enables on–chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. This parameter is sampled. VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V , f = 100 MHz, tA = 25 °C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2 V. DM inputs are grouped with I/O pins – reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
15. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$, is VREF.
16. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.2VDDQ is recognized as LOW.
17. The output timing reference voltage level is VTT.
18. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
22. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High–Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
23. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
24. For command/address input slew rate ≥ 1.0 V/ns
25. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
26. For CK & $\overline{CK}$ slew rate ≥ 1.0 V/ns
27. These parameters guarantee device timing, but they are not necessarily tested on each device.
28. Slew Rate is measured between VOH(ac) and VOL(ac).
29. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
30. tQH = tHPmin – X where:
    tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
    X consists of tDQSQmax, the pulse width distortion of on–chip clock circuits, data pin to pin skew and output pattern effects, and p–channel to n–channel variation of the output drivers.



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n

Figure 37 – DATA INPUT (WRITE) TIMING

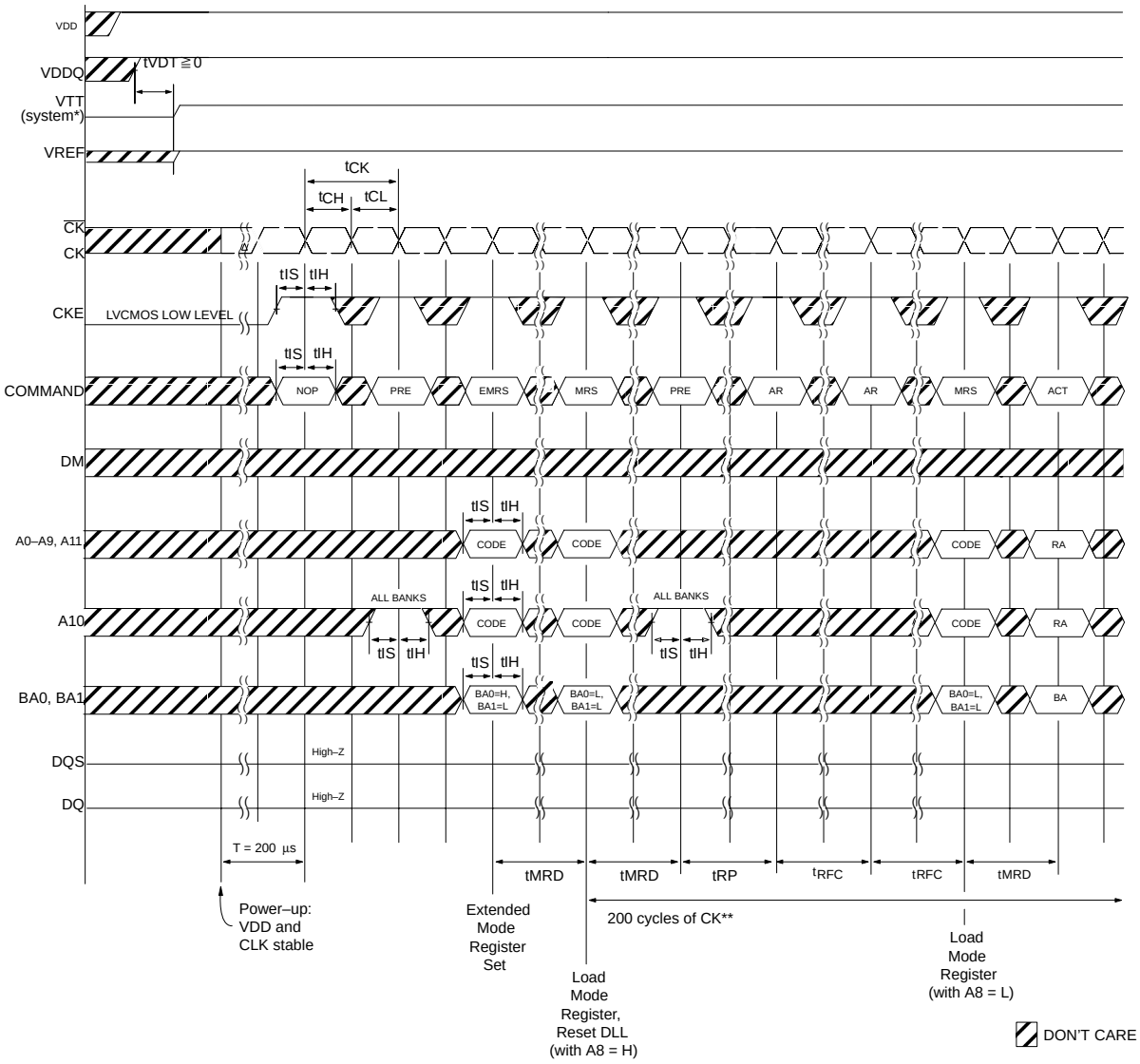


Burst of 4 is shown.

tDQSQ and tQH are only shown once, and are shown referenced to different edges of DQS, only for clarity of illustration.
tDQSQ and tQH both apply to each of the four relevant edges of DQS.

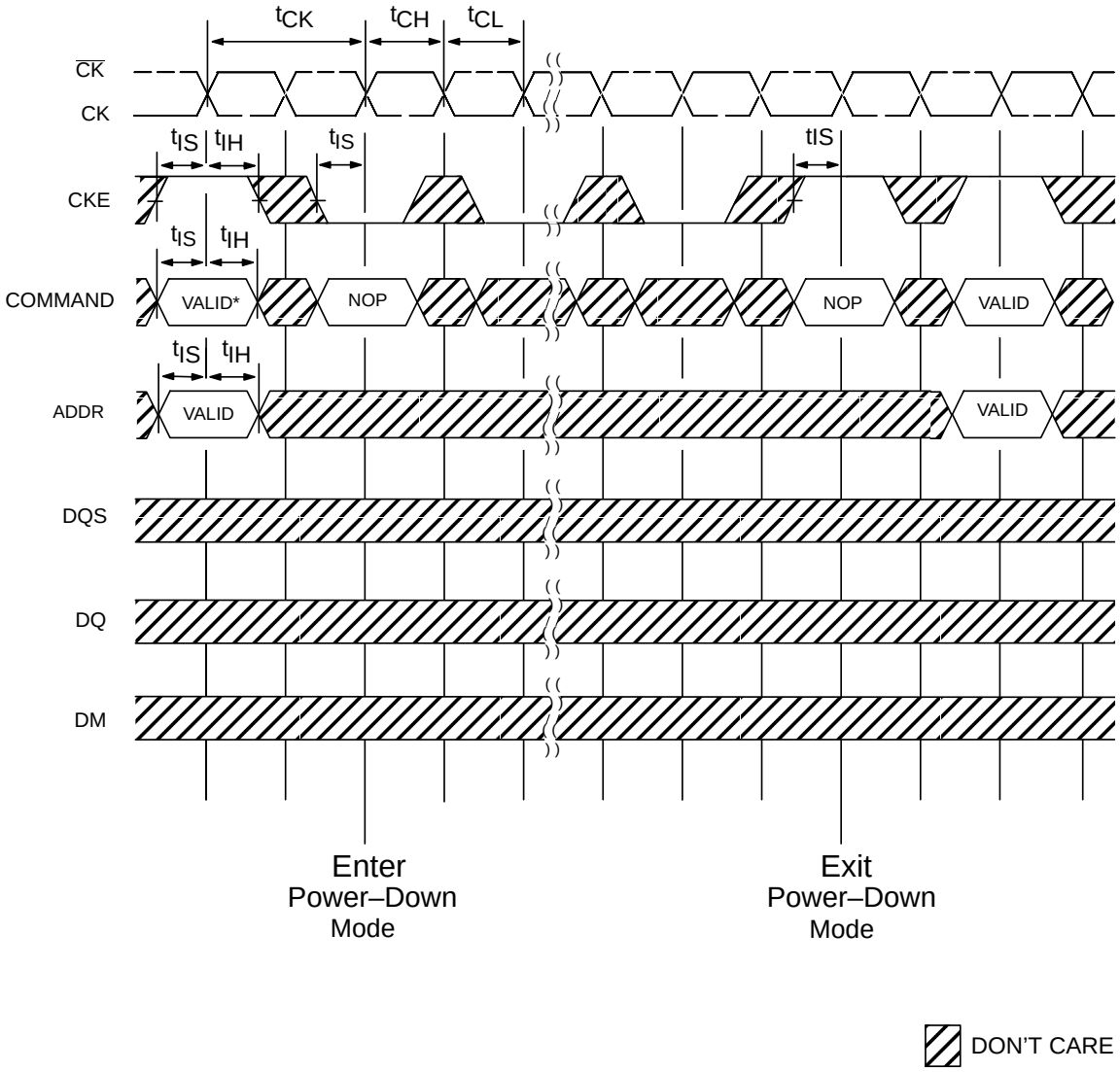
tQHmin = tHPmin – X where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
X consists of tDQSQmax, the pulse width distortion of on–chip clock circuits, data pin to pin skew and output pattern effects, and p–channel to n–channel variation of the output drivers.

Figure 38 – DATA OUTPUT (READ) TIMING



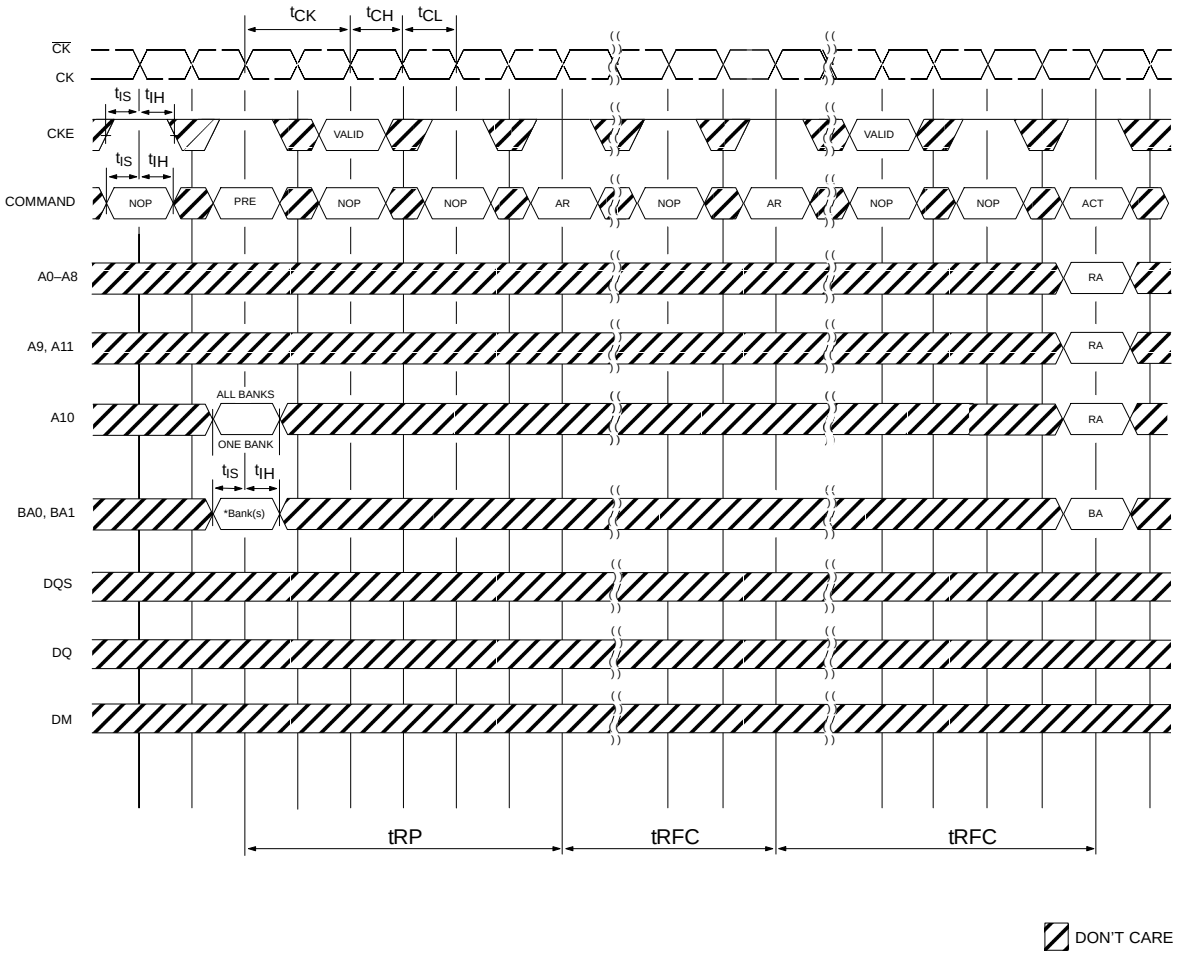
* = VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch–up.
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied
The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

Figure 39 – INITIALIZE AND MODE REGISTER SETS



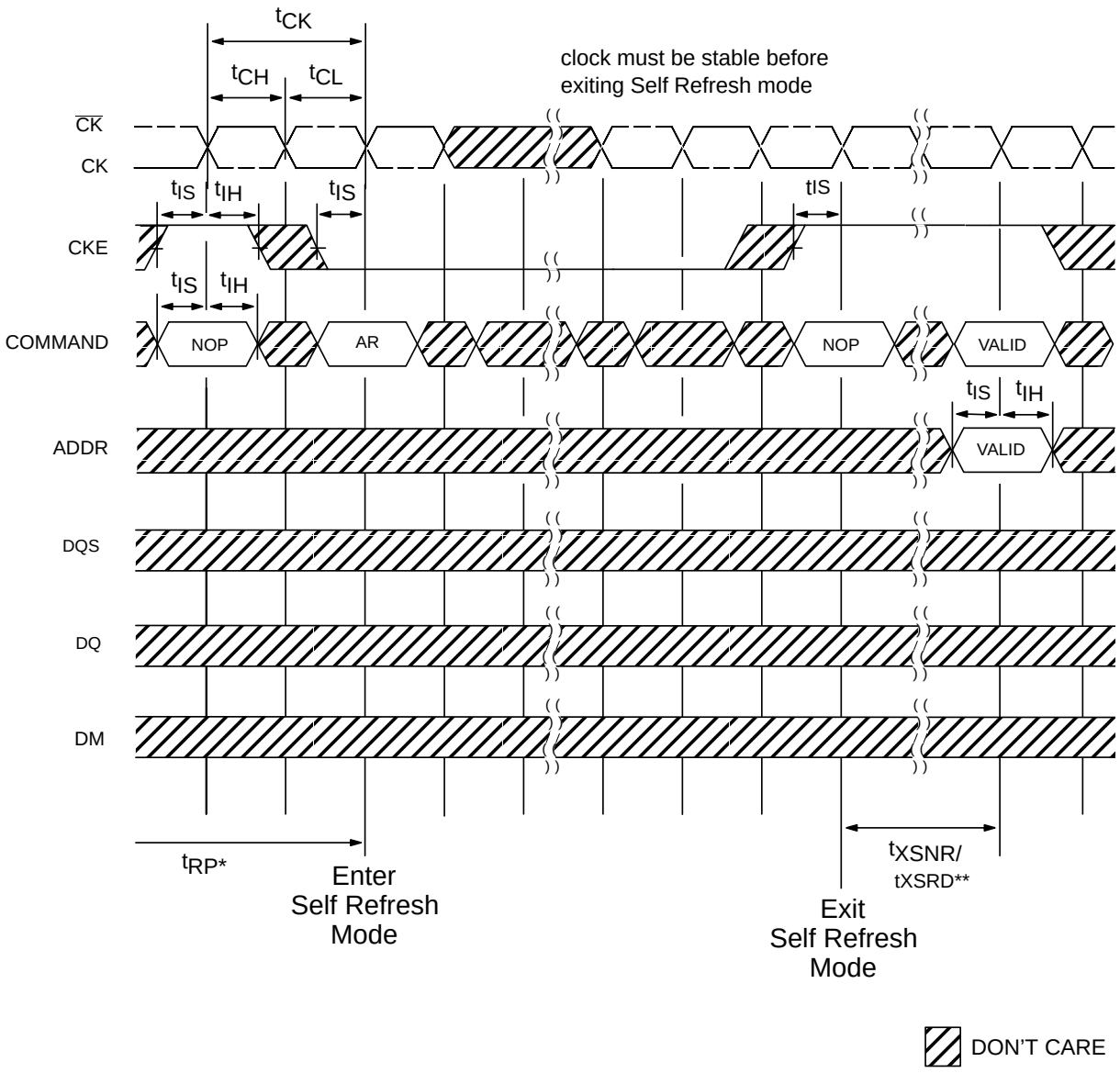
No column accesses are allowed to be in progress at the time Power–Down is entered
* = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power–Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power–Down mode shown is Active Power Down.

Figure 40 – POWER–DOWN MODE



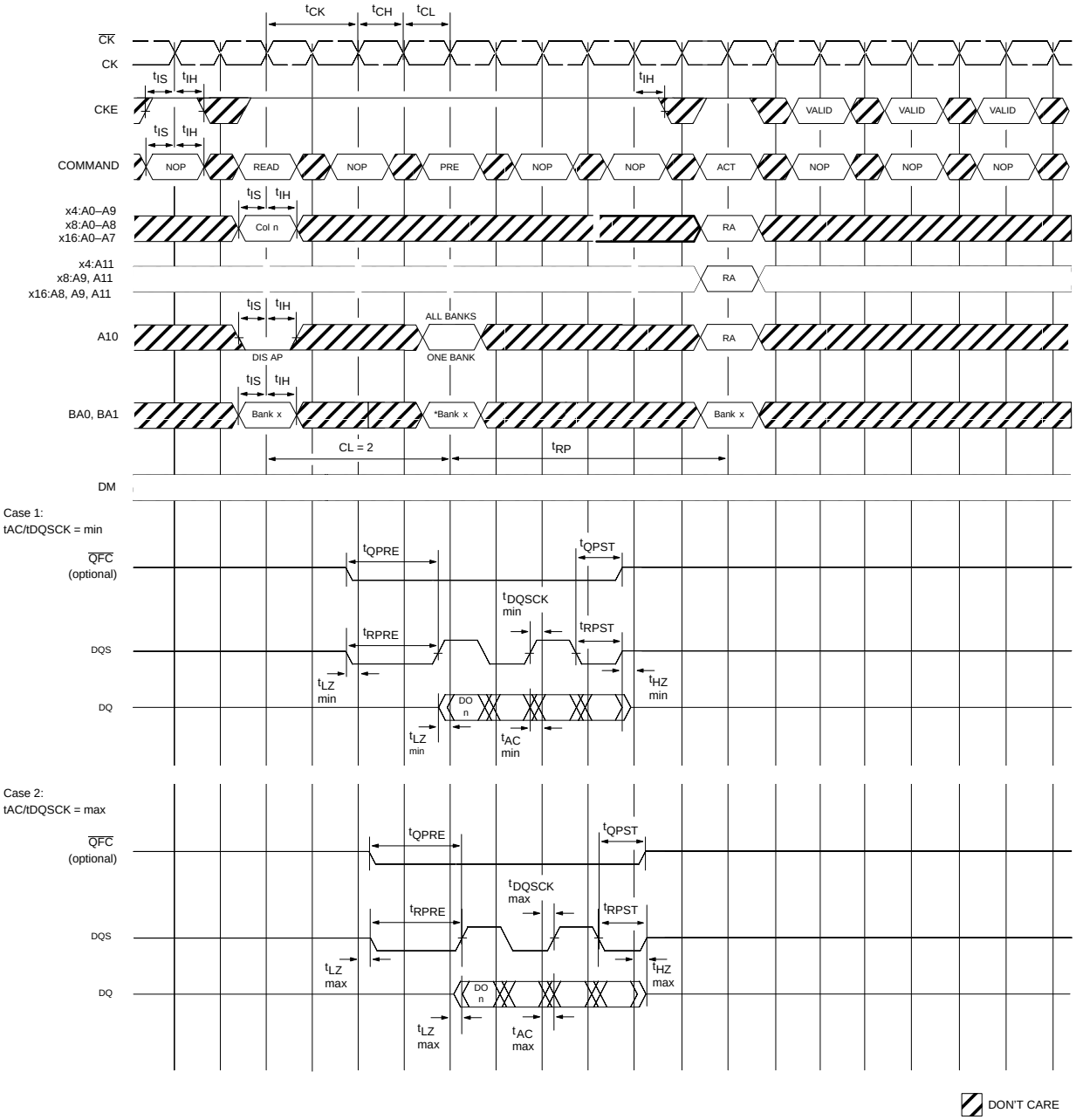
* = ”Don’t Care”, if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
DM, DQ and DQS signals are all ”Don’t Care”/High–Z for operations shown

Figure 41 – AUTO REFRESH MODE



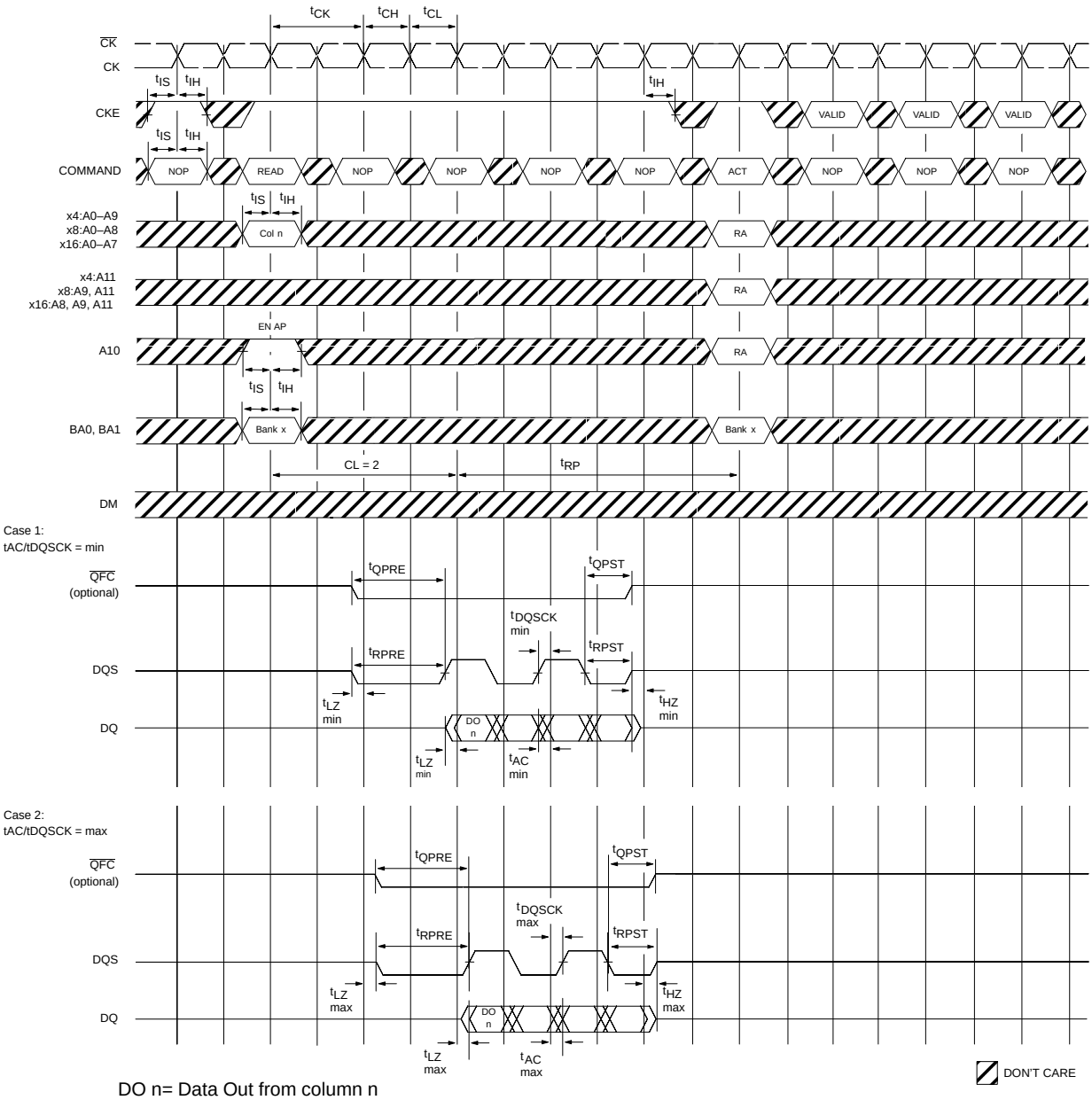
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non–READ command can be applied, and tXSRD (200 cycles of CK) are required before a READ command can be applied.

Figure 42 – SELF REFRESH MODE



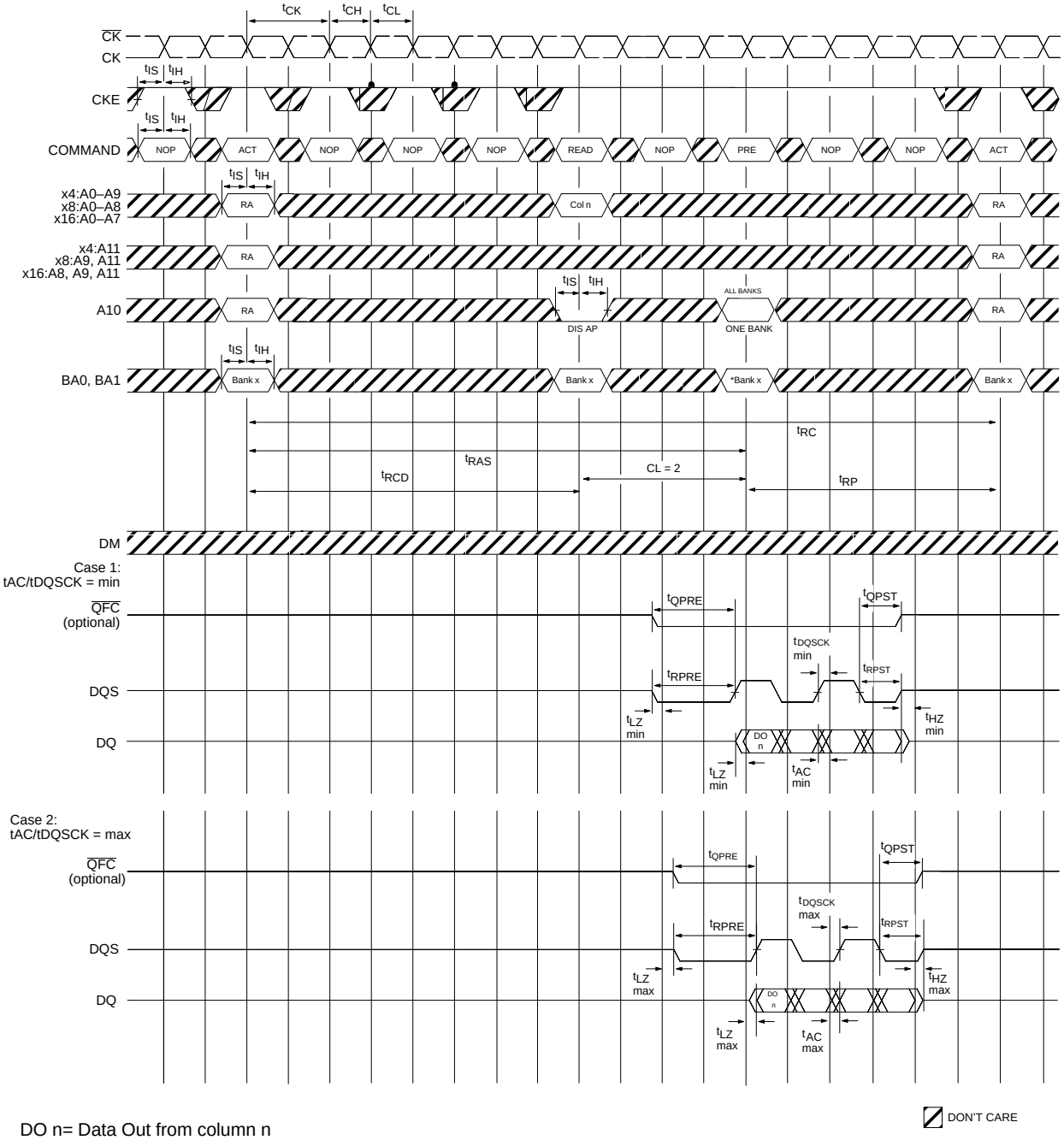
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 43 – READ _ WITHOUT AUTO PRECHARGE



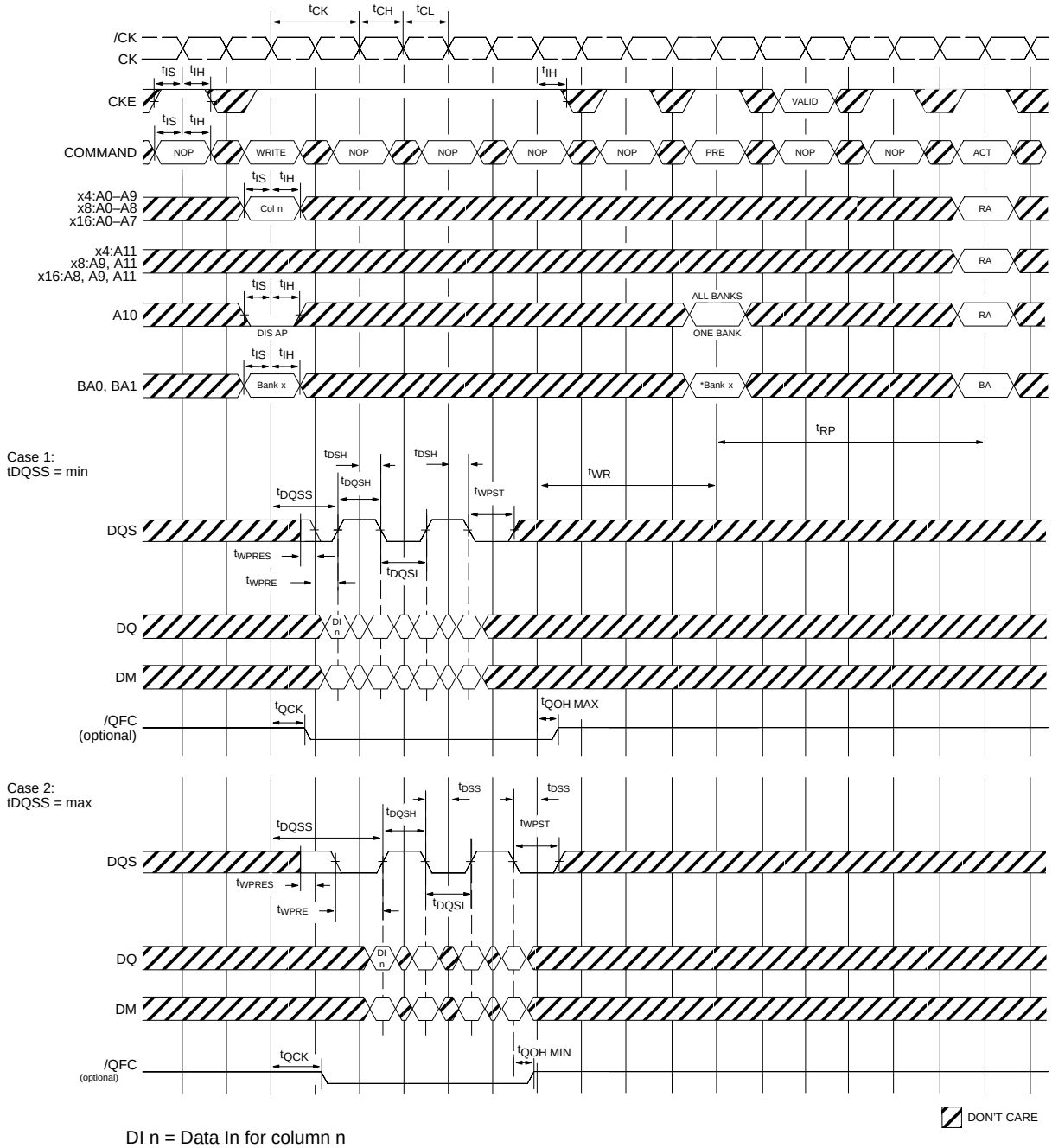
DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP = Enable Autoprecharge
ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 44 – READ _ WITH AUTO PRECHARGE



DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

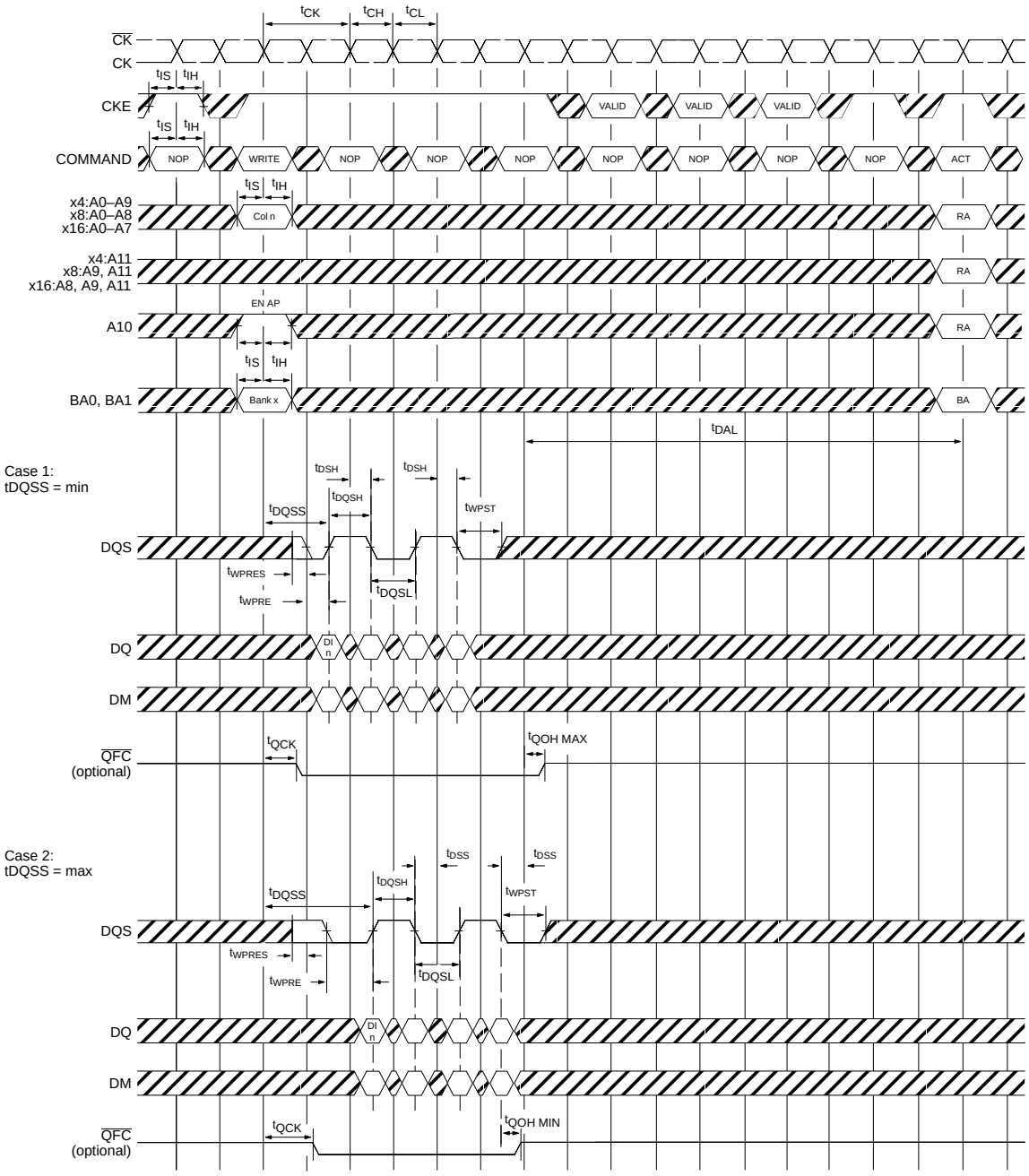
Figure 45 – BANK READ ACCESS



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 46 – WRITE – WITHOUT AUTO PRECHARGE

Release 1



DI n = Data In for column n

DON'T CARE

Burst Length = 4 in the case shown

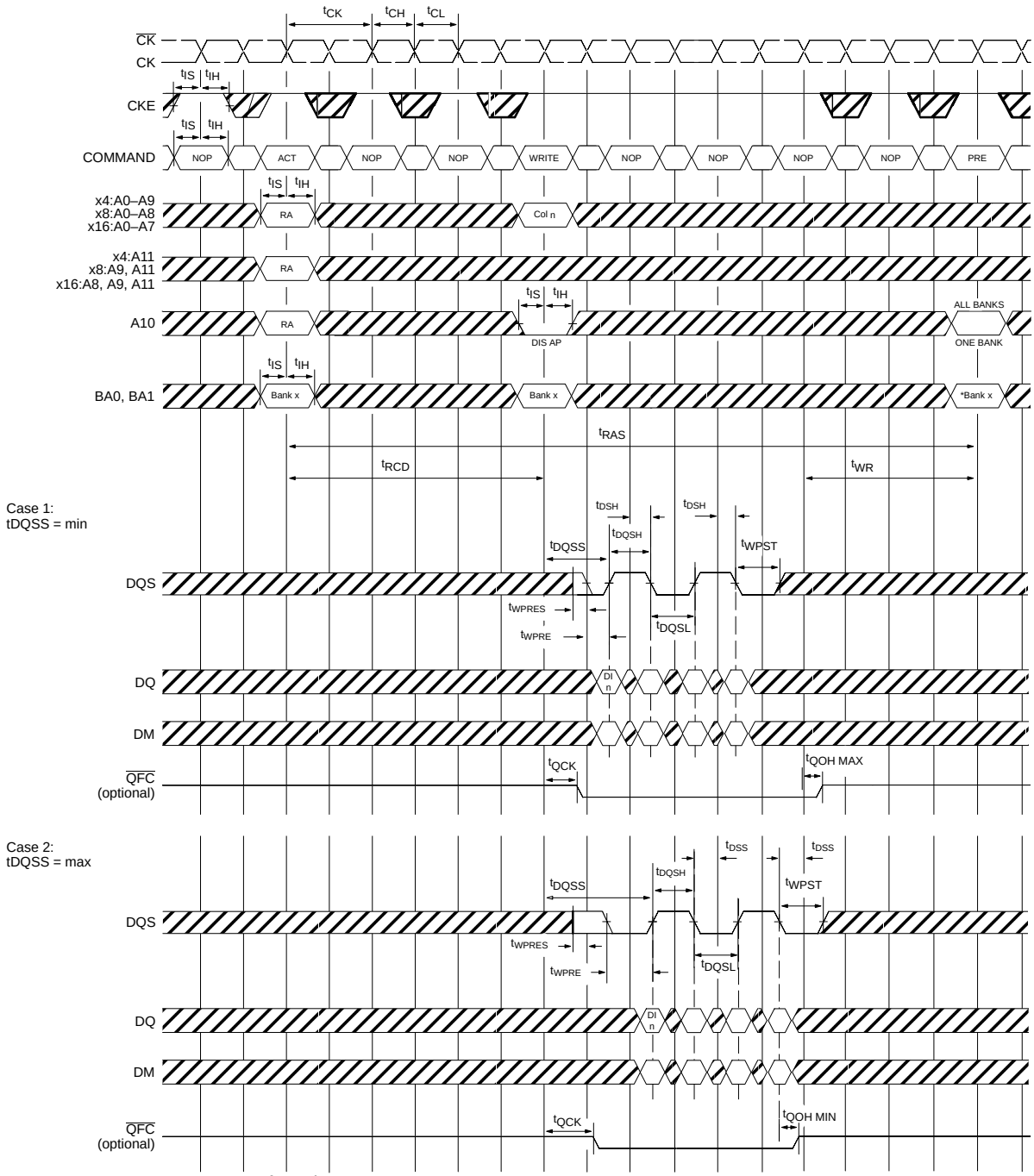
3 subsequent elements of Data In are applied in the programmed order following DI n

EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

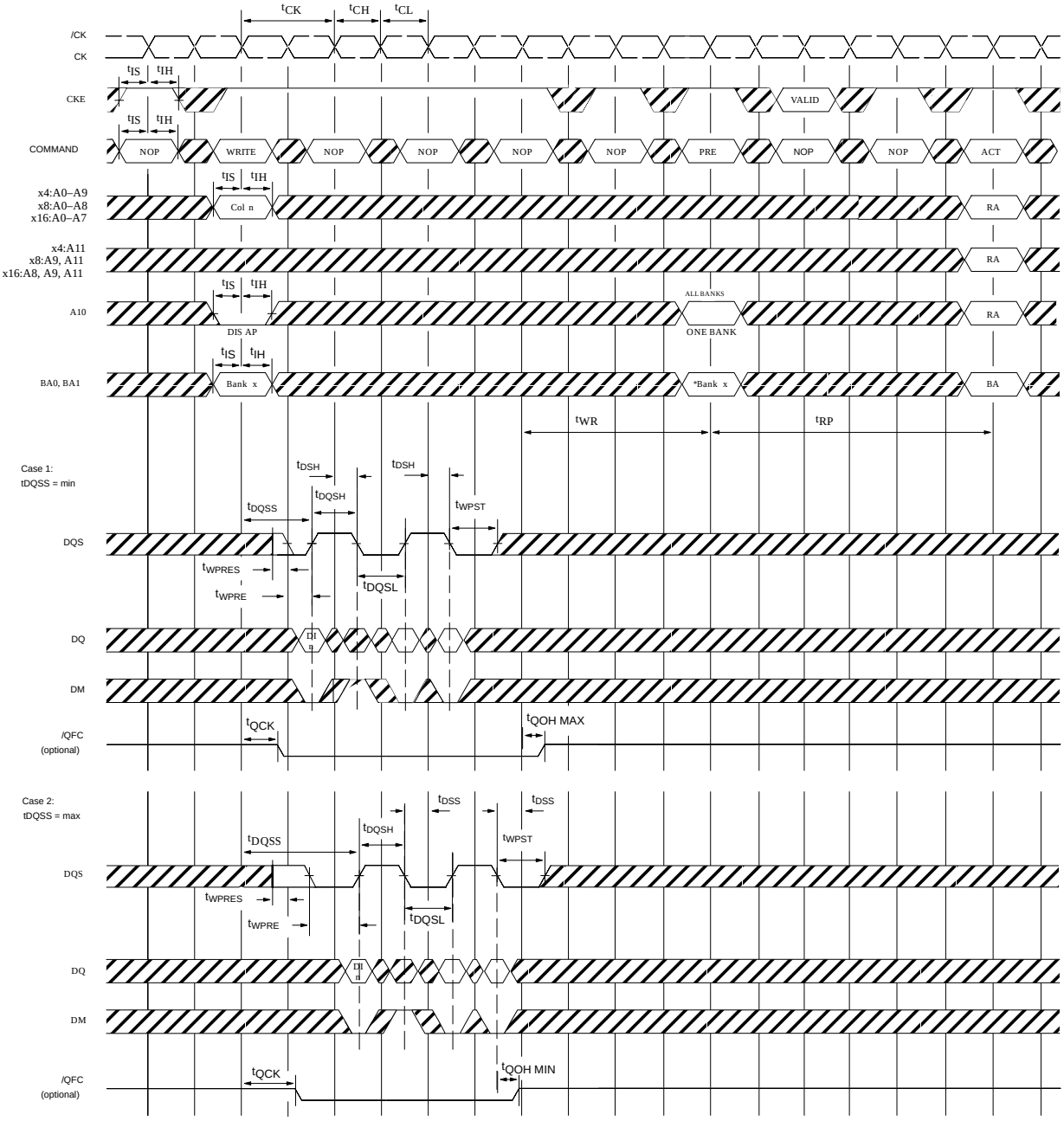
Figure 47 – WRITE – WITH AUTO PRECHARGE



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 48 – BANK WRITE ACCESS

Release 1



DON'T CARE

DI n= Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n (the second element of the four is masked)
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 49 – WRITE _ DM OPERATION

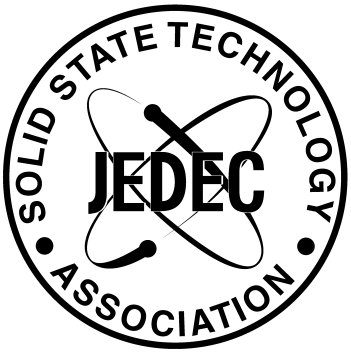

SOLID STATE TECHNOLOGY
JEDEC
ASSOCIATION

Exhibit F

JEDEC STANDARD

Double Data Rate (DDR) SDRAM Specification

JESD79

(Release 2)

MAY 2002

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

XILINX EXHIBIT 1010
Page 528

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DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

(From JEDEC Board Ballot JCB-99-70, and modified by numerous other Board Ballots, formulated under the cognizance of Committee JC-42.3 on DRAM Parametrics.)

Standard No. 79 Revision Log.
Release 1, June 2000
Release 2, May 2002

Scope

This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

XILINX EXHIBIT 1010
Page 532

XILINX EXHIBIT 1010
Page 533

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M X4 (4 M X4 X4 banks), 8 M X8 (2 M X8 X4 banks), 4 M X16 (1 M X16 X4 banks)
32 M X4 (8 M X4 X4 banks), 16 M X8 (4 M X8 X4 banks), 8 M X16 (2 M X16 X4 banks)
64 M X4 (16 M X4 X4 banks), 32 M X8 (8 M X8 X4 banks), 16 M X16 (4 M X16 X4 banks)
128 M X4 (32 M X4 X4 banks), 64 M X8 (16 M X8 X4 banks), 32 M X16 (8 M X16 X4 banks)
256 M X4 (64 M X4 X4 banks), 128 M X8 (32 M X8 X4 banks), 64 M X16 (16 M X16 X4 banks)

FEATURES

- Double–data–rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge–aligned with data for READs; center–aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ = +2.5 V ±0.2 V
- VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V

GENERAL DESCRIPTION

The DDR SDRAM is a high–speed CMOS, dynamic random–access memory internally configured as a quad–bank DRAM. These devices contain the following number of bits:
64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits

The DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half–clock–cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge–aligned with data for READs and center–aligned with data for WRITEs.

The DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self–timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power–saving, power–down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices may have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

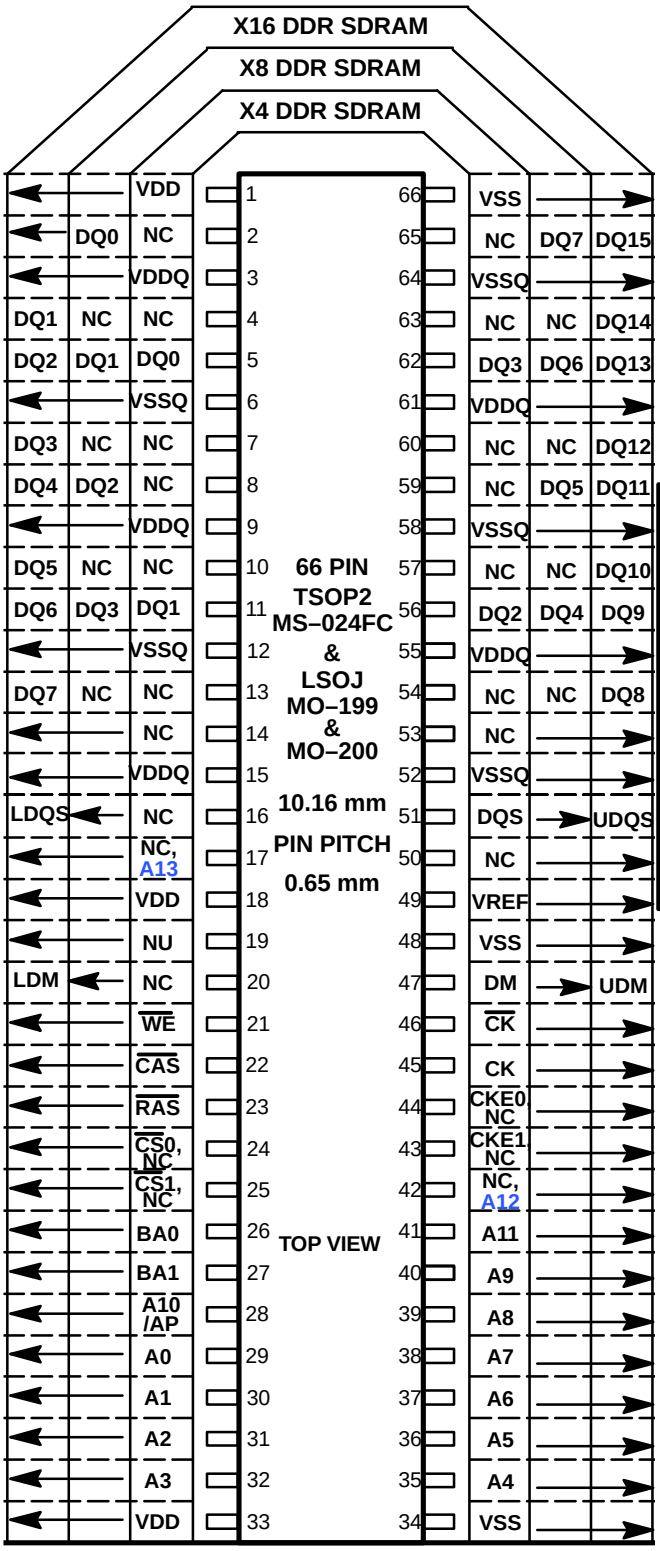
This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC X4/X8/X16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

CONTENTS

Features 1
General Description 1
Pin Assignment Diagram, TSOP2 Package 3
Address Assignment Table 1a TSOP2 Package 3
Pin Assignment Diagram, BGA Package 4
Address Assignment Table 1b BGA Package 5
Functional Block Diagram – X4/X8/X16 5
Pin Descriptions, Table 2 6
Functional Description 7
Initialization 7
Register Definition 7
Mode Register 7
Burst Length 8
Table 3, Burst Definition 8
Fig. 4, Mode Register Definition 8
Burst Type 9
Read Latency 9
Operating Mode 9
Terminology Definitions
DDR200 9
DDR266 9
DDR333 9
Fig. 5, Required CAS Latencies 10
Extended Mode Register 11
DLL Enable/Disable 11
Output Drive Strength 11
Fig.6, Extended Mode Register Definitions 11
Commands 12
Truth Table 1a (Commands) 12
Truth Table 1b (DM Operation) 12
Truth Table 2 (CKE) 13
Truth Table 3 (Current State, Same Bank) . . . . . 14 & 15
Truth Table 4 (Current State, Different Bank) . . . . . 16 & 17
Fig. 7, Simplified State Diagram 18
Command definitions . . . . . 19 & 20
DESELECT 19
NO OPERATION (NOP) 19
MODE REGISTER SET 19
ACTIVE 19
READ 19
WRITE 19
BURST TERMINATE 19
PRECHARGE 20
AUTO PRECHARGE 20
REFRESH REQUIREMENTS 20
AUTO REFRESH 20
SELF REFRESH 20
Table 4, Row–Column Organization by Density 19
Operations 21
Bank/Row Activation 21
Fig. 8, Activating a Specific Row 21
Fig. 9, tRCD & tRRD Definition 21
Reads . . . . . 22 & 23
Fig. 10, Read Command 22
Fig. 11, Read Burst 24
Fig. 12, Consecutive Read Bursts 25
Fig. 13, Nonconsecutive Read Bursts 26
Fig. 14, Random Read Accesses 27
Fig. 15, Terminating a Read Burst 28
Fig. 16, Read to Write 29
Fig. 17, Read to Precharge 30
Writes 31
Fig. 18, Write Command 31
Fig. 19, Write to Write–Max tDQSS 32
Fig. 20, Write to Write–Min tDQSS 32
Fig. 21, Write Burst – Nom., Min., and Max tDQSS 33
Fig. 22, Write To Write – Max tDQSS 34
Fig., 23, Write To Write – Max tDQSS, Non Consecutive . 35
Fig., 24, Random Write Cycles – Max tDQSS 36
Fig., 25, Write To Read – Max tDQSS, Non–Interrupting . 37
Fig., 26, Write To Read – Max tDQSS, Interrupting 38
Fig., 27, Write To Read – Max tDQSS, Odd Number of Data, Interrupting 39
Fig., 28, Write To Precharge – Max tDQSS, Non–Interrupting 40
Fig., 29, Write To Precharge – Max tDQSS, Interrupting 41
Fig., 30, Write To Precharge – Max tDQSS, Odd Number of Data, Interrupting 42
Precharge 43
Fig. 31, Precharge Command 43
Powerdown 43
Fig. 32, Power–Down 44
Absolute Maximum Ratings 45
Capacitance, Table 5 45
DC Electrical Characteristics and Operating Conditions, Tab. 6 . . . 45
AC Operating Conditions, Table 7 46
Idd Specifications and Conditions, Table 8 . . . . . 46 & 47
Fig. 33, IDD7 Measurement Timing Waveforms 47
AC Electrical Characteristics (Timing Table), Table 9 48
AC Timing Variations, DDR200, DDR266, DDR333, Table 10 49
Fig. 34, Test Reference Load 49
Component Specification Notes . . . . . 49 & 50
System Characteristics, DDR200, DDR266, & DDR333 51
Signal Derating Specifications, Tables 11–17 51
Figs. 35 & 36, AC Overshoot/Undershoot Specification, Tables 18 & 19, ... 52 & 53
System Characteristics Notes . . . . . 54 & 55
Full Strength Output V–I Characteristics . . . . . 56 & 57
Weak Output V–I Characteristics . . . . . 58 & 59
DDR SDRAM Output Driver V–I Characteristics 60
Timing Waveforms
Fig. 41, Data Input Timing 61
Fig. 42, Data Output Timing 61
Fig. 43, Initialize and Mode Register Set 62
Fig. 44, Power–Down Mode 63
Fig. 45, Auto Refresh Mode 64
Fig. 46, Self Refresh Mode 65
Reads
Fig. 47, Read – Without Auto Precharge 66
Fig. 48, Read – Without Auto Precharge (CL=1.5, BL=4) 67
Fig. 49, Read – With Auto Precharge 68
Fig. 50, Bank Read Access 69
Writes
Fig. 51, Write – Without Auto Precharge 70
Fig. 52, Write – With Auto Precharge 71
Fig. 53, Bank Write Accesses 72
Fig. 54, Write – DM Operation 73
Revision Log . . . . . 74 & 75



ADDRESS ASSIGNMENT TABLE

Density	Org.	Bank	Row Addr.	Col Addr	Bank Addr
64 Mb	16M X 4	4	A0⇒A11	A0⇒A9	BA0, BA1
	8M X 8	4	A0⇒A11	A0⇒A8	BA0, BA1
	4M X 16	4	A0⇒A11	A0⇒A7	BA0, BA1
128 Mb	32M X 4	4	A0⇒A11	A0⇒A9, A11	BA0, BA1
	16M X 8	4	A0⇒A11	A0⇒A9	BA0, BA1
	8M X 16	4	A0⇒A11	A0⇒A8	BA0, BA1
256 Mb	64M X 4	4	A0⇒A12	A0⇒A9, A11	BA0, BA1
	32M X 8	4	A0⇒A12	A0⇒A9	BA0, BA1
	16M X 16	4	A0⇒A12	A0⇒A8	BA0, BA1
512 Mb	128M X 4	4	A0⇒A12	A0⇒A9,A11,A12	BA0, BA1
	64M X 8	4	A0⇒A12	A0⇒A9, A11	BA0, BA1
	32M X 16	4	A0⇒A12	A0⇒A9	BA0, BA1
1 Gb	256M X 4	4	A0⇒A13	A0⇒A9,A11,A12	BA0, BA1
	128M X 8	4	A0⇒A13	A0⇒A9,A11	BA0, BA1
	64M X 16	4	A0⇒A13	A0⇒A9	BA0, BA1

TABLE 1a: TSOP2 Device Address Assignment Table

The following pin assignments apply for $\overline{CS}$ and CKE pins for Stacked and Non–stacked devices.

Pin	Non–Stacked	Stacked	
24	$\overline{CS}$	$\overline{CS}$0	
25	NC	$\overline{CS}$1	
43	NC	CKE1	
44	CKE	CKE0	

Figure 1
64 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ

(x4)

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	A13,NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12,NC	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

X4 Device Ball Pattern

(x8)

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DM	F	NC	VDD	A13,NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12,NC	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

X8 Device Ball Pattern

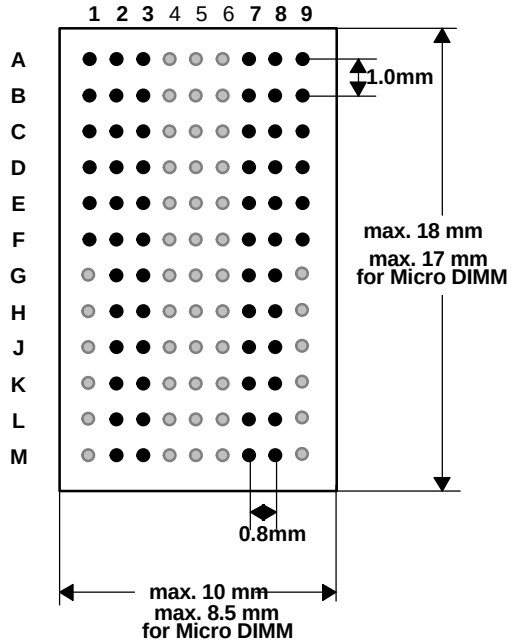
(x16)

1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VDDQ	DQ7
VREF	VSS	UDM	F	LDM	VDD	A13,NC
	CK	$\overline{CK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12,NC	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

X16 Device Ball Pattern

● : Ball Existing [For Reference Only]
○ : Depopulated Ball

Top View(See the balls through the Package)

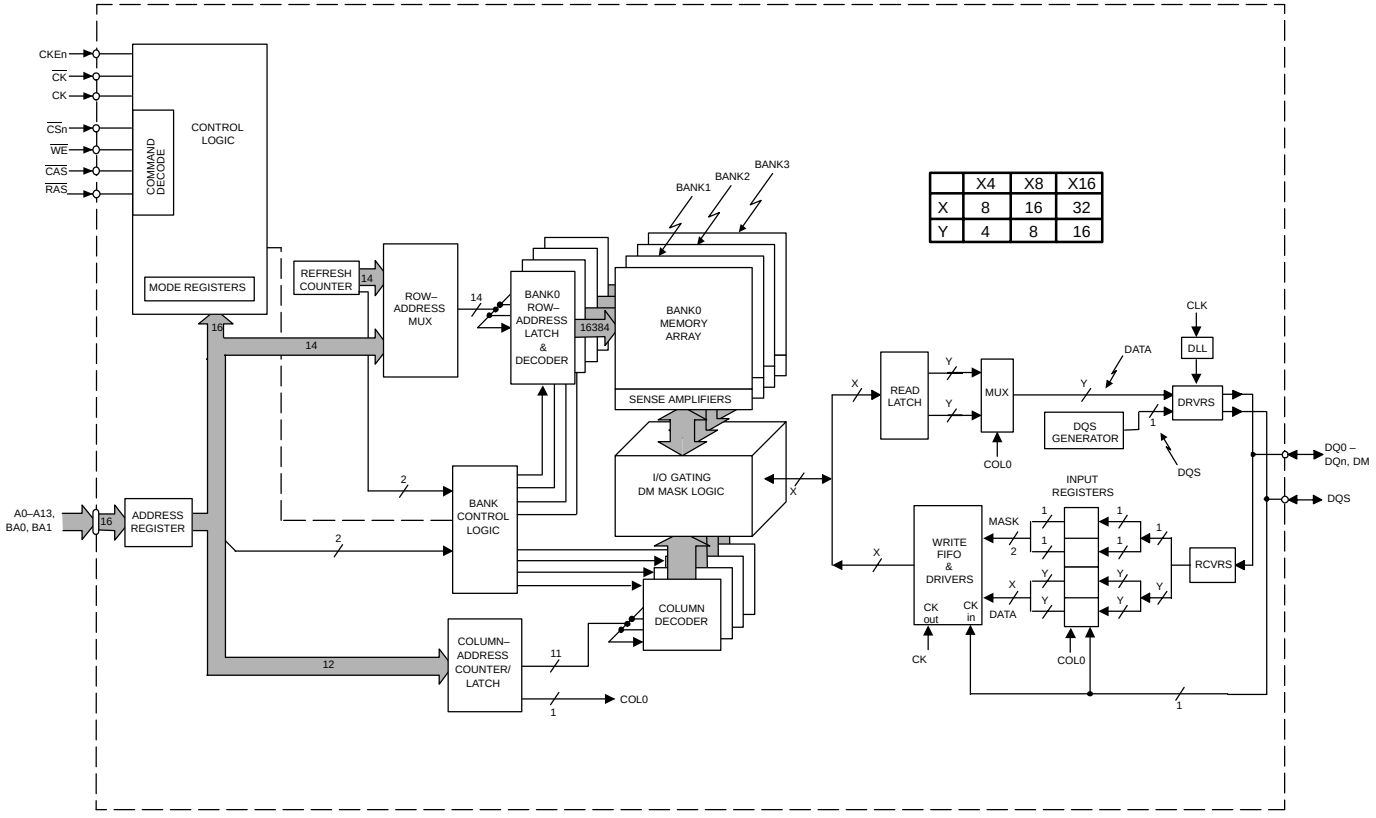


BGA Package Ball Pattern, Top View

Figure 2
128 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN BGA

Item	128Mb	256Mb	512Mb	1Gb	Note
Number of banks	4	4	4	4	
Bank Address Pins	BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1	
Autoprecharge Pins	A10/AP	A10/AP	A10/AP	A10/AP	
Row Addresses	A0-A11	A0-A12	A0-A12	A0-A13	
Column Addresses x4 x8 x16	A0-A9,A11 A0-A9 A0-A8	A0-A9,A11 A0-A9 A0-A8	A0-A9,A11,A12 A0-A9,A11 A0-A9	A0-A9,A11,A12 A0-A9,A11 A0-A9	
H2 pin function	NC	A12	A12	A12	
F13 pin function	NC	NC	NC	A13	
JC11 MO #	MO-233A	MO-233A	MO-233A	MO-233A	
JC11 Variation #	AA	AA	AA	AA	
JC11 Package Name	DSBGA	DSBGA	DSBGA	DSBGA	
Pin Pitch	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	

TABLE 1b: BGA Device Address Assignment and Package Table



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

FIGURE 3: FUNCTIONAL BLOCK DIAGRAM OF DDR SDRAM

Release 2

TABLE 2: PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE (CKE0) (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER–DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER–DOWN (row ACTIVE in any bank). CKE is synchronous for POWER–DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER–DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied. The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{CS}$ ($\overline{CS}$0) ($\overline{CS}$1)	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin. Optional pinouts include $\overline{CS}$0 and $\overline{CS}$1 on different pins, to facilitate device stacking.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (LDM) (UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the X16, LDM corresponds to the data on DQ0–DQ7; UDM corresponds to the data on DQ8–DQ15. DM may be driven high, low, or floating during READs.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0–A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op–code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). A12 is used on device densities of 256Mb and above; A13 is used on device dendities of 1Gb.
DQ	I/O	Data Bus: Input/Output.
DQS (LDQS) (UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge–aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0–DQ7; UDQS corresponds to the data on DQ8–DQ15.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V ±0.2 V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V ±0.3 V or +2.5 V ±0.2 V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

XILINX EXHIBIT 1010

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high–speed CMOS, dynamic random–access memory internally configured as a quad–bank DRAM. These devices contain the following number of bits:
64Mb has 67,108,864 bits
128Mb has 134,217,728 bits
256Mb has 268,435,456 bits
512Mb has 536,870,912 bits
1Gb has 1,073,741,824 bits

The DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double–data–rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half clock cycle data transfers at the I/O pins. DQ, DQS, & DM may be floated when no data is being transferred

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A13 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. No power sequencing is specified during power up and power down given the following criteria:

- VDD and VDDQ are driven from a single power converter output, AND
- VTT is limited to 1.35 V, AND
- VREF tracks VDDQ/2

OR, the following relationships must be followed:

- VDDQ is driven after or with VDD such that VDDQ < VDD + 0.3 V AND
- VTT is driven after or with VDDQ such that VTT < VDDQ + 0.3 V, AND
- VREF is driven after or with VDDQ such that VREF < VDDQ + 0.3 V.

At least one of these two conditions must be met.

Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power–up is required to guarantee that the DQ and DQS outputs will be in the High–Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μs delay prior to applying an executable command.

Once the 200 μs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the ”all banks idle” state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 4. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self–clearing).

Mode Register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A13 or (A12 on 256Mb/512Mb, A13 on 1Gb see figure 4) specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Table 3
BURST DEFINITION

Burst Length	Starting Coumn Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0–1	0–1
	1	1–0	1–0
4	A1 A0		
	0 0	0–1–2–3	0–1–2–3
	0 1	1–2–3–0	1–0–3–2
	1 0	2–3–0–1	2–3–0–1
	1 1	3–0–1–2	3–2–1–0
8	A2 A1 A0		
	0 0 0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0 0 1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0 1 0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0 1 1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1 0 0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1 0 1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1 1 0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1 1 1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0

Notes:
1. For a burst length of two, A1–Ai selects the two–data–element block; A0 selects the first access within the block.
2. For a burst length of four, A2–Ai selects the four–data–element block; A0–A1 selects the first access within the block.
3. For a burst length of eight, A3–Ai selects the eight–data–element block; A0–A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–Ai when the burst length is set to two, by A2–Ai when the burst length is set to four and by A3–Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

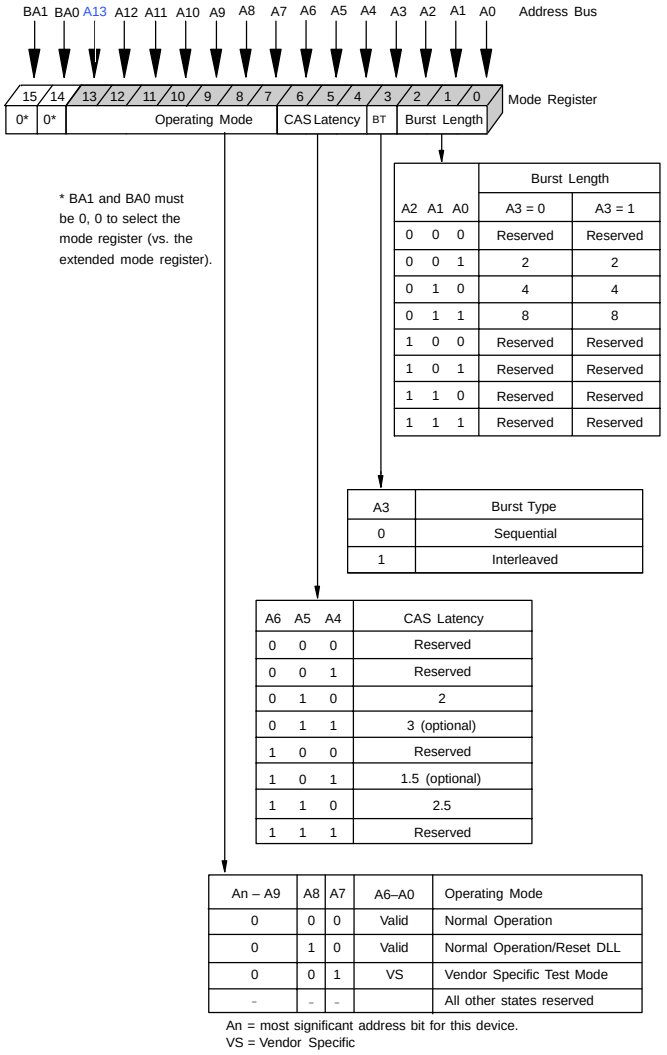


Figure 4
Mode Register Definition

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 3.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A13 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9–A13 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7–A13 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Terminology Definitions.

The following are definitions of the terms DDR200, DDR266, & DDR333, as used in this specification.

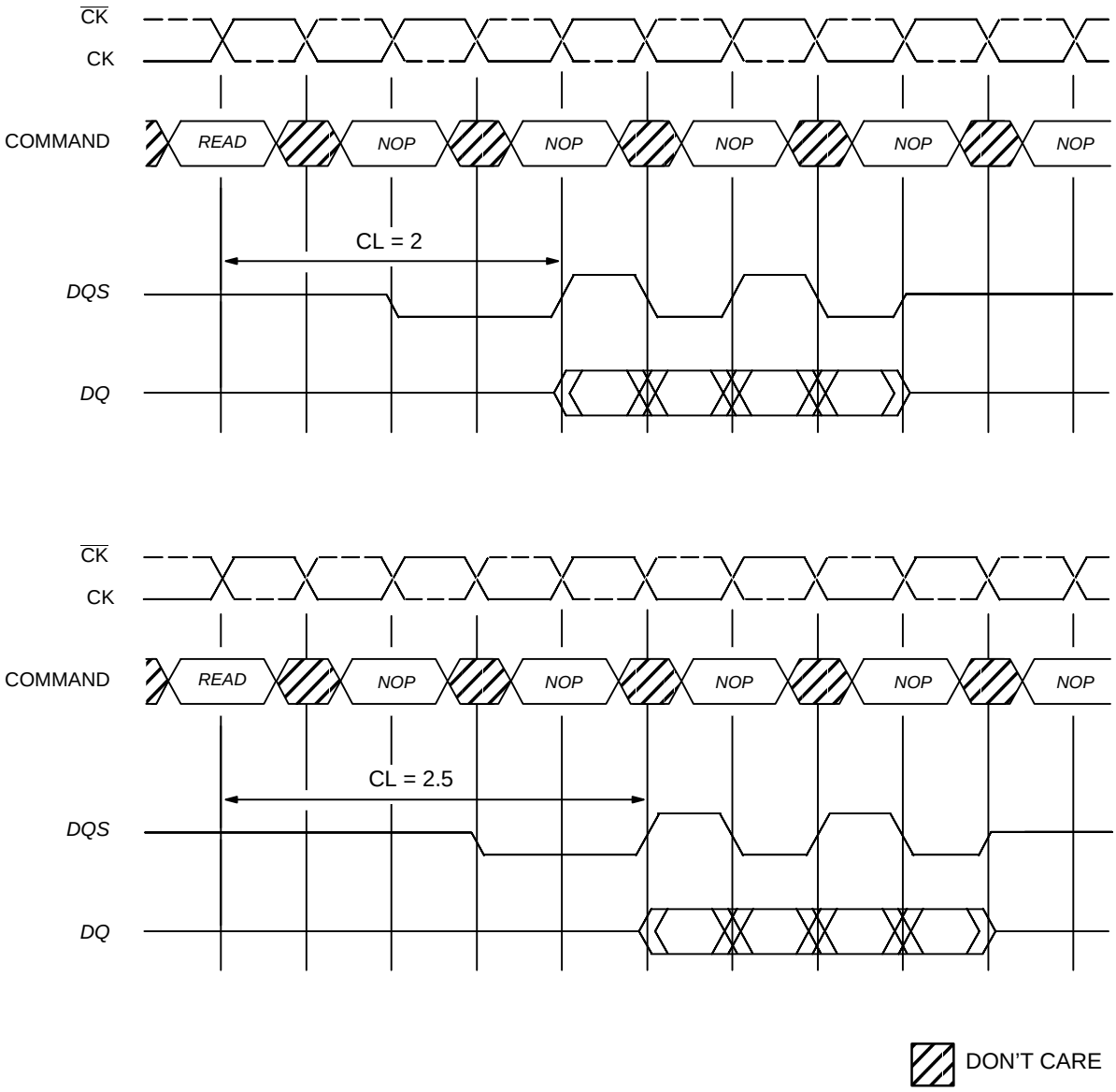
DDR200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The corresponding nominal data rate is *200 MHz.

DDR266: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is *266 MHz.

DDR333: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 167 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 167 MHz clock frequency). The corresponding nominal data rate is *333 MHz.

In addition to the above DDRxxx specification, a letter modifier may be applied to indicate special timing characteristics for these devices in various market applications. For example, DDR266A and DDR266B classifications define distinct sorts for operation as a function of CAS latency. These differences between sorts are described in Table 10, ”AC Timing Variations”.

* In this context, the term MHz is used loosely. A more technically precise definition is ”million transfers per second per data pin”



Burst Length = 4 in the cases shown
Shown with nominal tDQSCK

Figure 5
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional). These functions are controlled via the bits shown in Figure 6. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power–up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point–to–point environments. I–V curves for the normal drive strength and weak drive strength are included in this document.

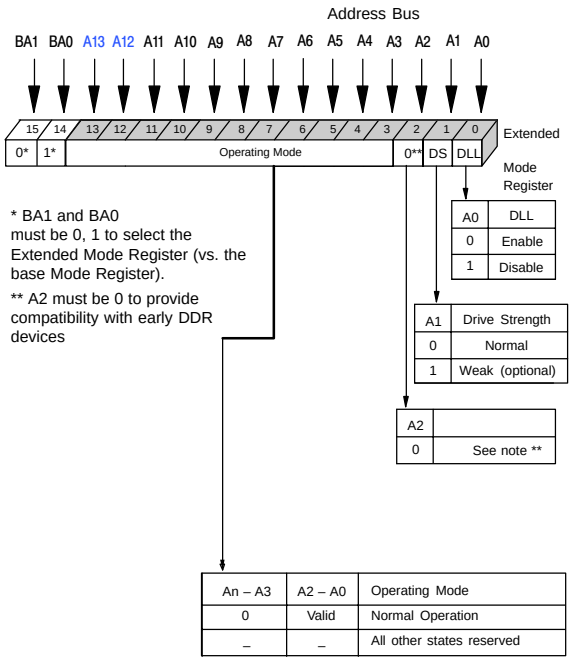


Figure 6
EXTENDED MODE REGISTER DEFINITION

COMMANDS

Truth Table 1a provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a – Commands

(Notes: 1)

NAME (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7
MODE REGISTER SET	L	L	L	L	Op–Code	2

TRUTH TABLE 1b – DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0–BA1 are reserved; A0–A13 provide the op–code to be written to the selected Mode Register.
3. BA0–BA1 provide bank address and A0–A13 provide row address.
4. BA0–BA1 provide bank address; A0–Ai provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are ”Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are ”Don’t Care” except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data, provided coincident with the corresponding data.

TRUTH TABLE 2 – CKE

(Notes: 1–4)

CKEn–1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power–Down	X	Maintain Power–Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power–Down	DESELECT or NOP	Exit Power–Down	
L	H	Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power–Down Entry	
H	L	Bank(s) Active	DESELECT or NOP	Active Power–Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn–1 was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.

4. All states and sequences not shown are illegal or reserved.

5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3 – Current State Bank n – Command to Bank n

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table is bank–specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and tRP has been met.
   - Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the ”row active” state.
   - Read w/Auto–Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
   - Write w/Auto–Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the ”all banks idle” state.

   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM will be in the ”all banks idle” state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank–specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank–specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank–specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,

TRUTH TABLE 4 – Current State Bank n – Command to Bank m

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto–Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto–Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto–Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto–Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	3a, 7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

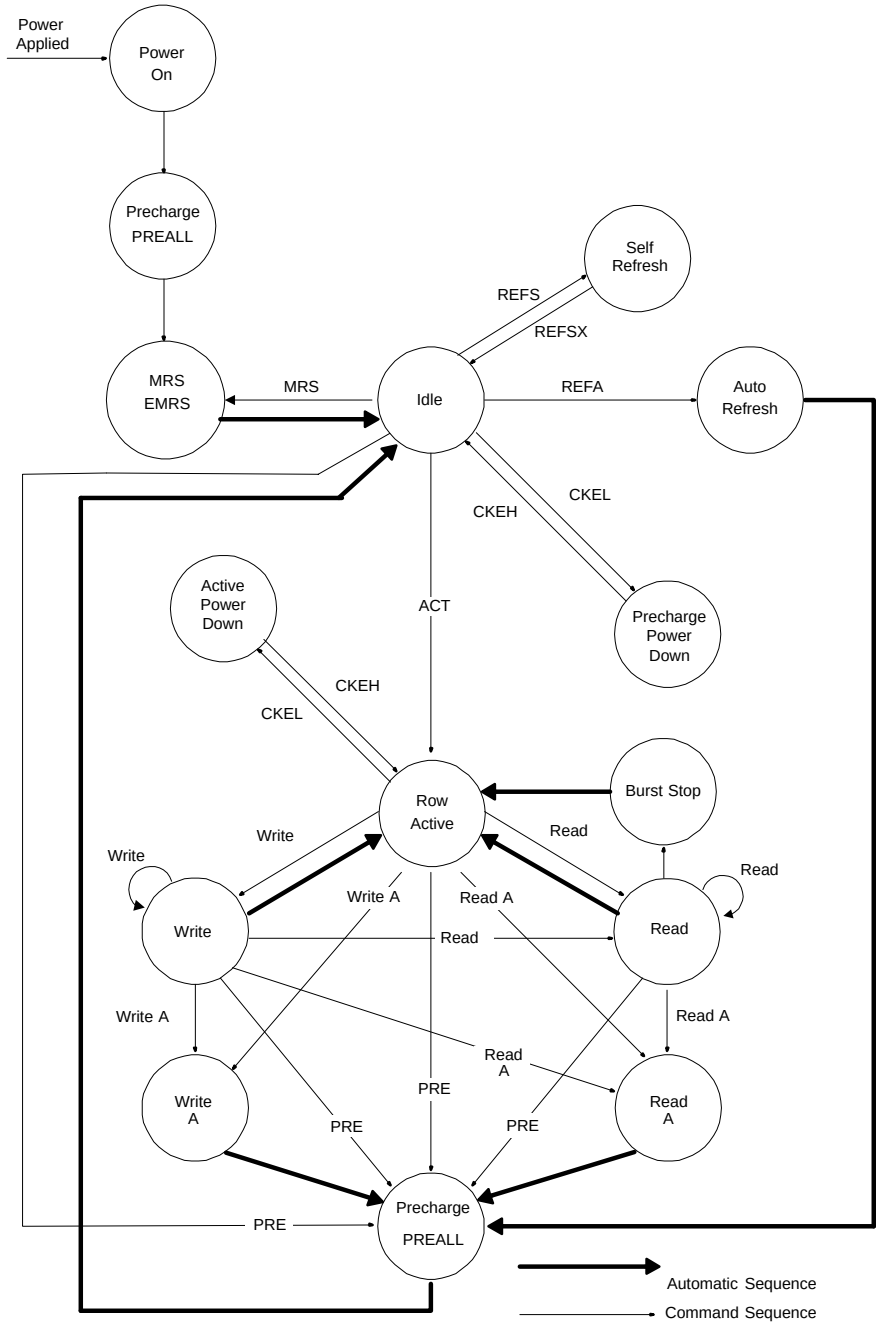
NOTE: (continued)

3. Current state definitions:

Idle:	The bank has been precharged, and tRP has been met.
Row Active:	A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
Read with Auto Precharge Enabled:	See following text
Write with Auto Precharge Enabled:	See following text

3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command..



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

Figure 7
SIMPLIFIED STATE DIAGRAM

DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to a DDR SDRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A13. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A13 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

Density	Column Address			Row Address
	X16	X8	X4	
64 Mb	A0⇒A7	A0⇒A8	A0⇒A9	A0⇒A11
128 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A11
256 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A12
512 Mb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A12
1 Gb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A13

Table 4

ROW–COLUMN ORGANIZATION BY DENSITY

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as ”Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual–bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

REFRESH REQUIREMENTS

DDR SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 256 Mb DDR SDRAM has 8192 rows resulting in a tREFI of 7.8 μs. To avoid excessive interruptions to the memory controller, higher density DDR SDRAMs maintain the 7.8 μs average refresh time and perform multiple internal refresh bursts. In these cases, the refresh recovery times, tRFC and tXSNR, are extended to accomodate these internal operations.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS–BEFORE–RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of tREFI (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 * tREFI.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are ”Don’t Care” during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNRC because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be ”opened.” This is accomplished via the ACTIVE command (Figure 8), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been ”closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row–access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

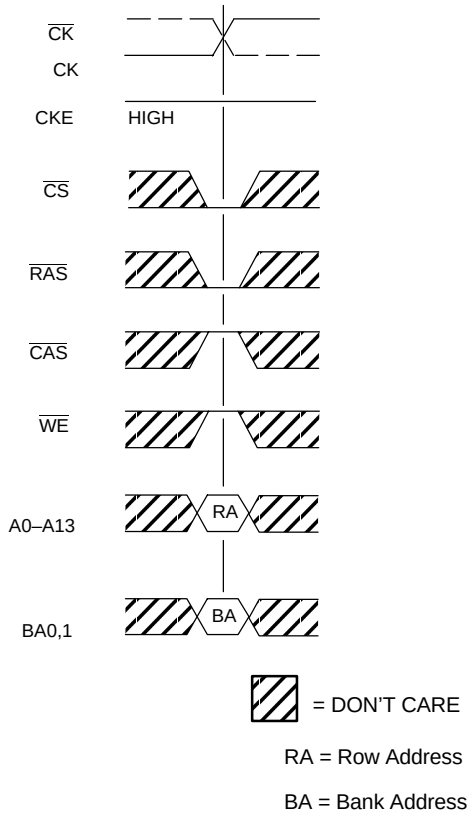


Figure 8
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

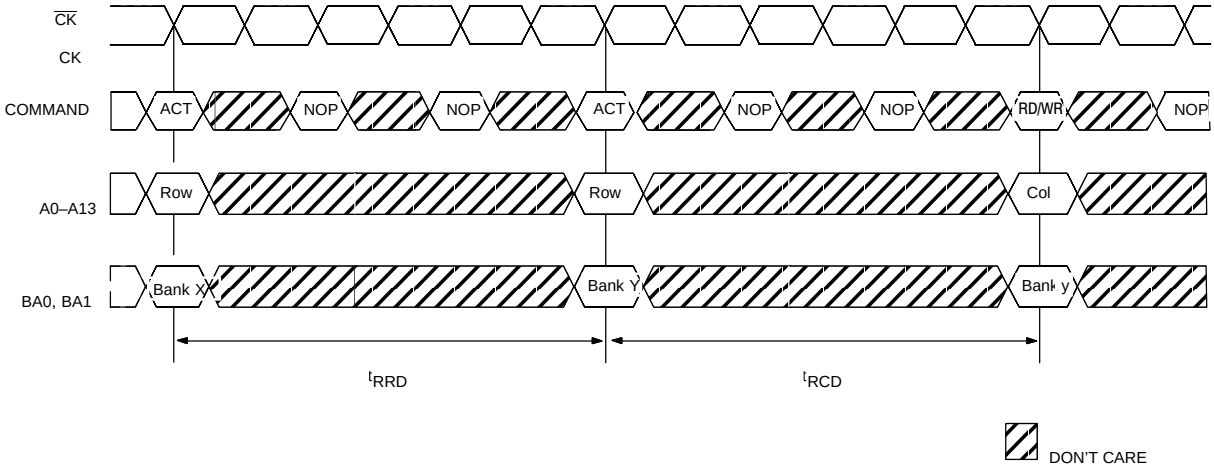


Figure 9
tRCD and tRRD Definition

Reads

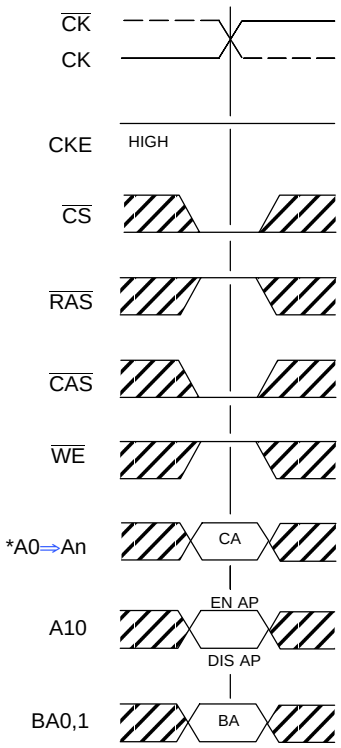
READ bursts are initiated with a READ command, as shown in Figure 10.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data–out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data–out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 11 shows general timing for each required (CL=2 and CL=2.5) CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data–out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High–Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 12. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 13. Full–speed random read accesses within a page (or pages) can be performed as shown in Figure 14.



= DON'T CARE
CA = Column Address
BA = Bank Address
EN AP = Enable Autoprecharge
DIS AP = Disable Autoprecharge
* See Address tables on PP 3 & 5

Figure 10
READ COMMAND

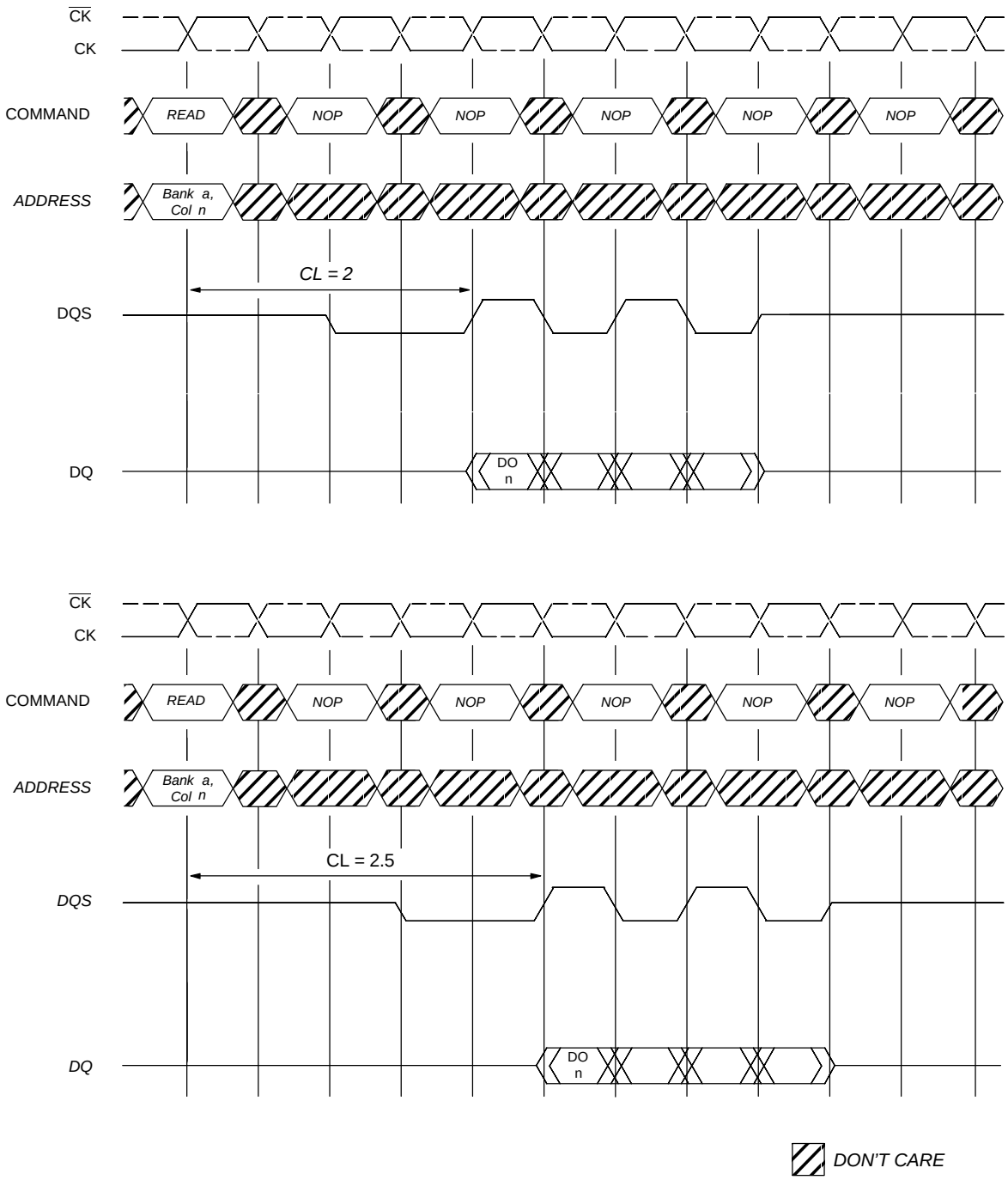
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 15. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs.

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued.

If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 16. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITEs).

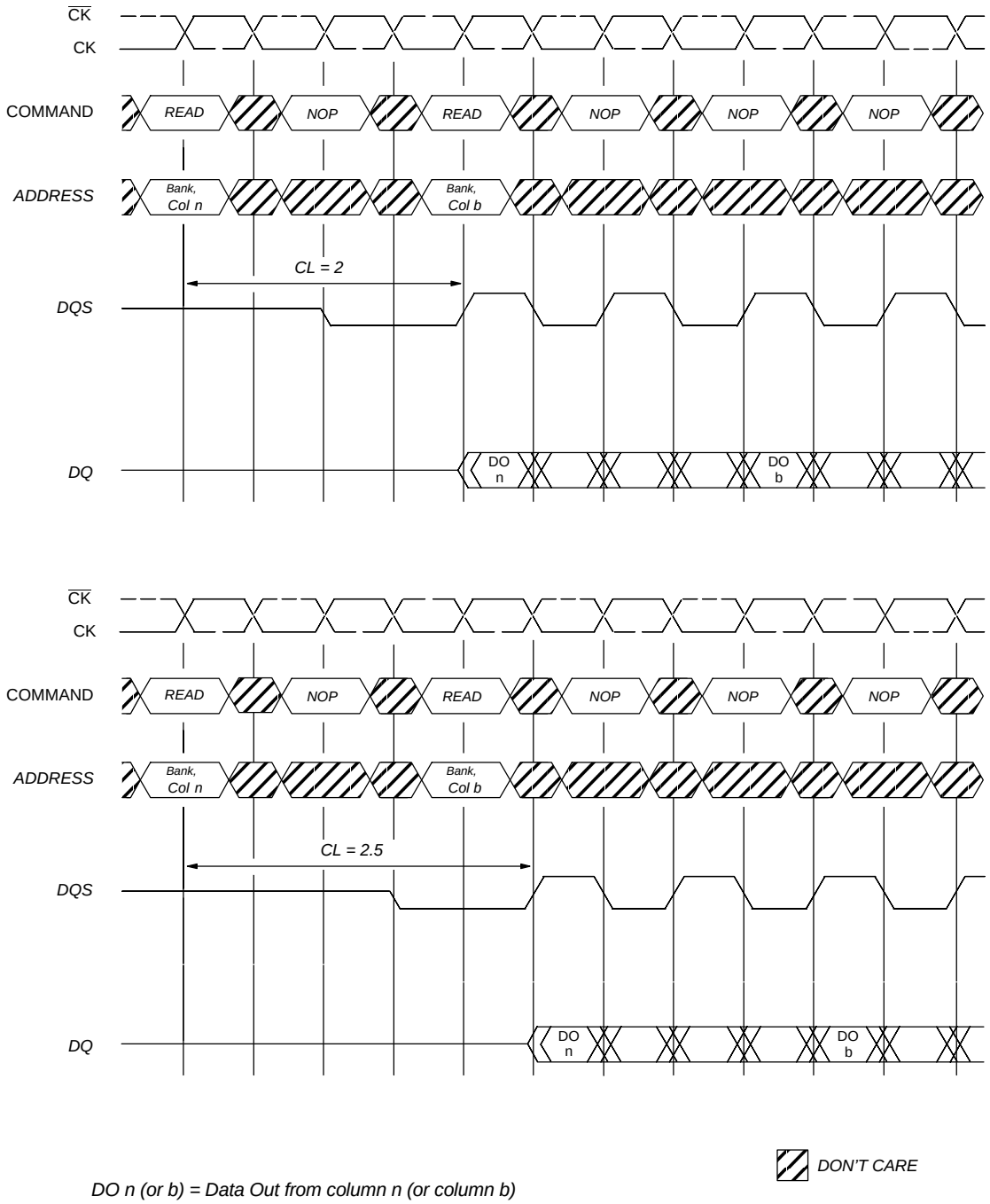
A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 17 for READ latencies of 2 and 2.5. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



DO n = Data Out from column n
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 11
READ BURST – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)

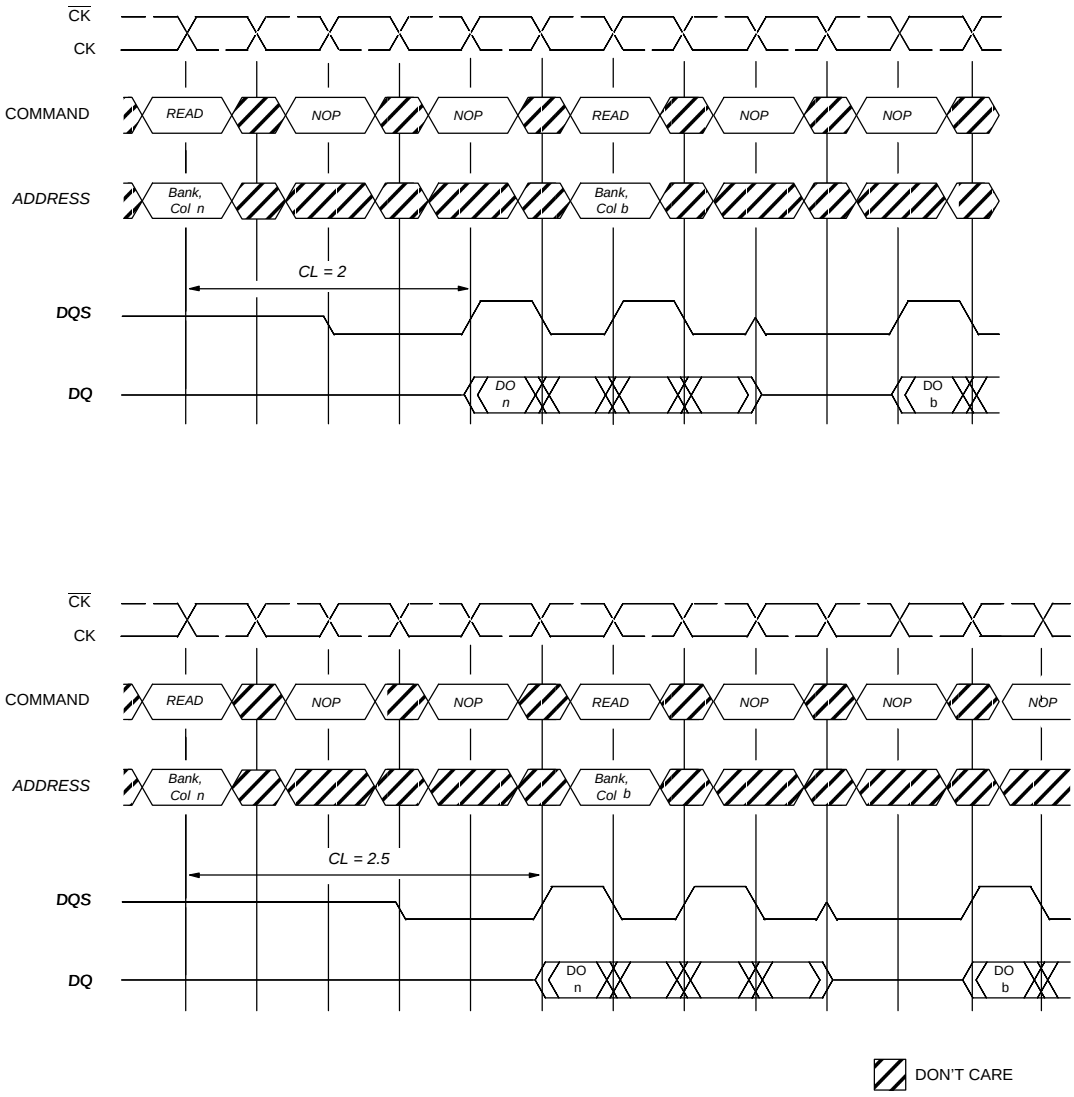
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

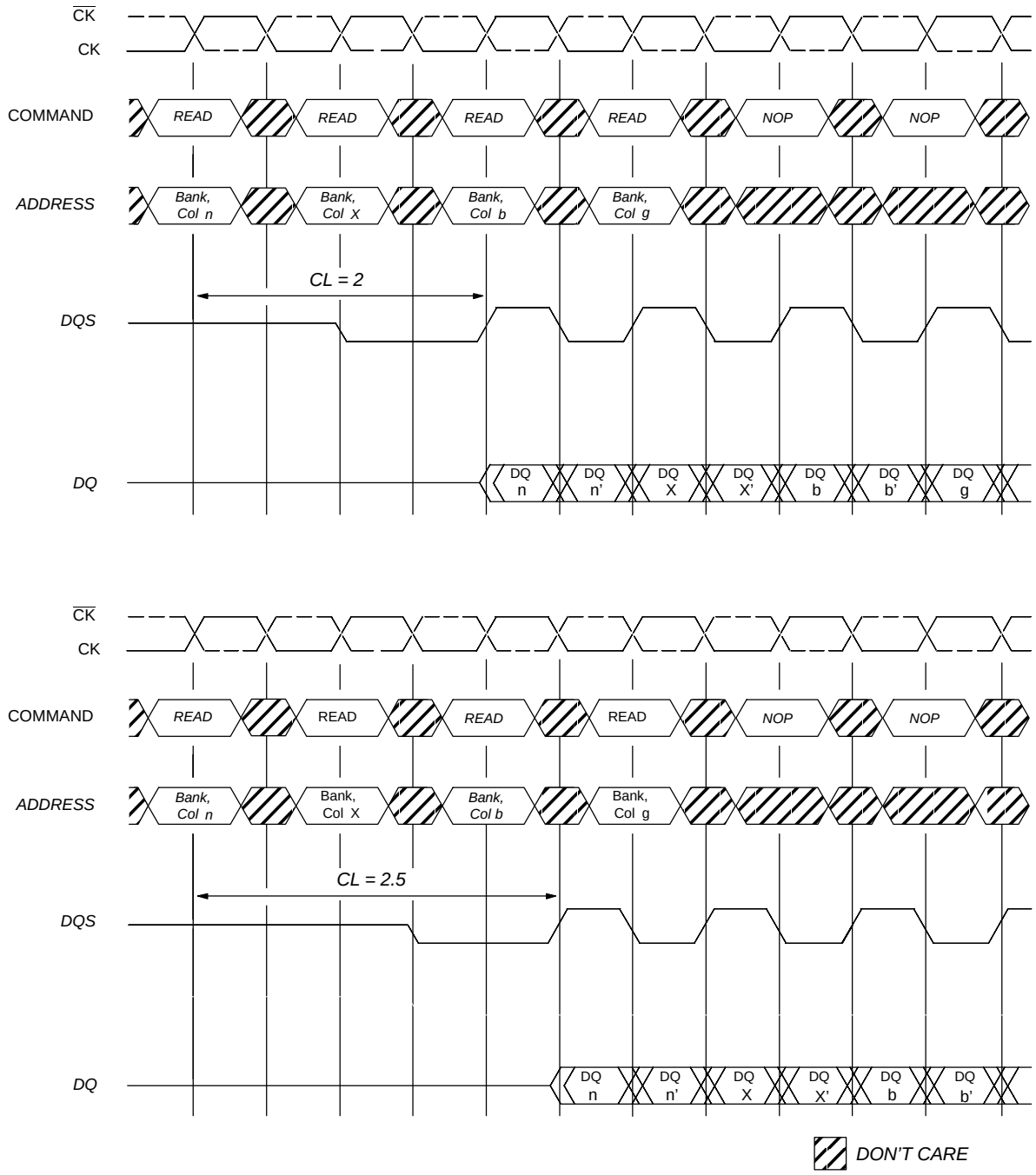
Read commands shown must be to the same device

Figure 12
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



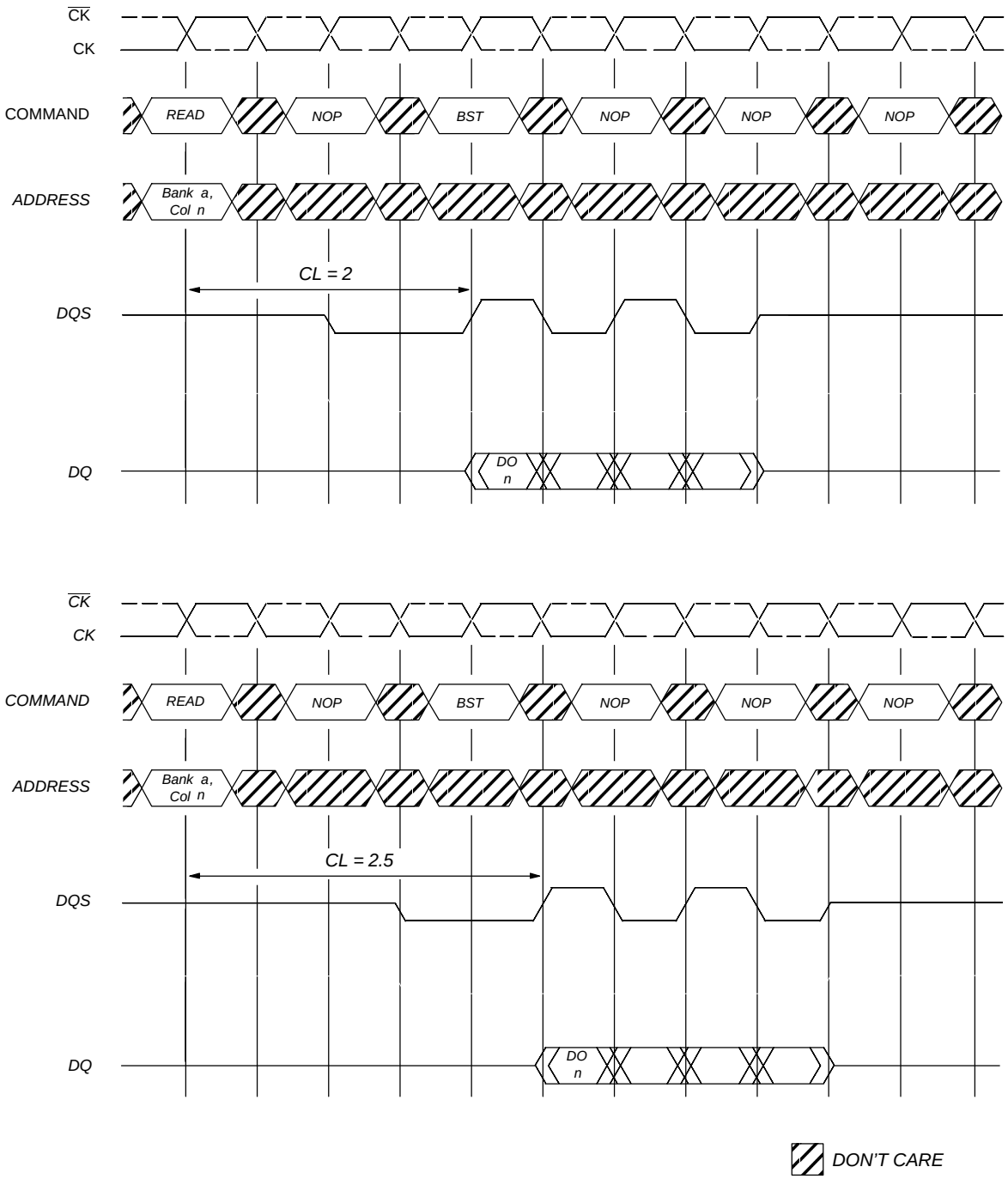
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Figure 13
NONCONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



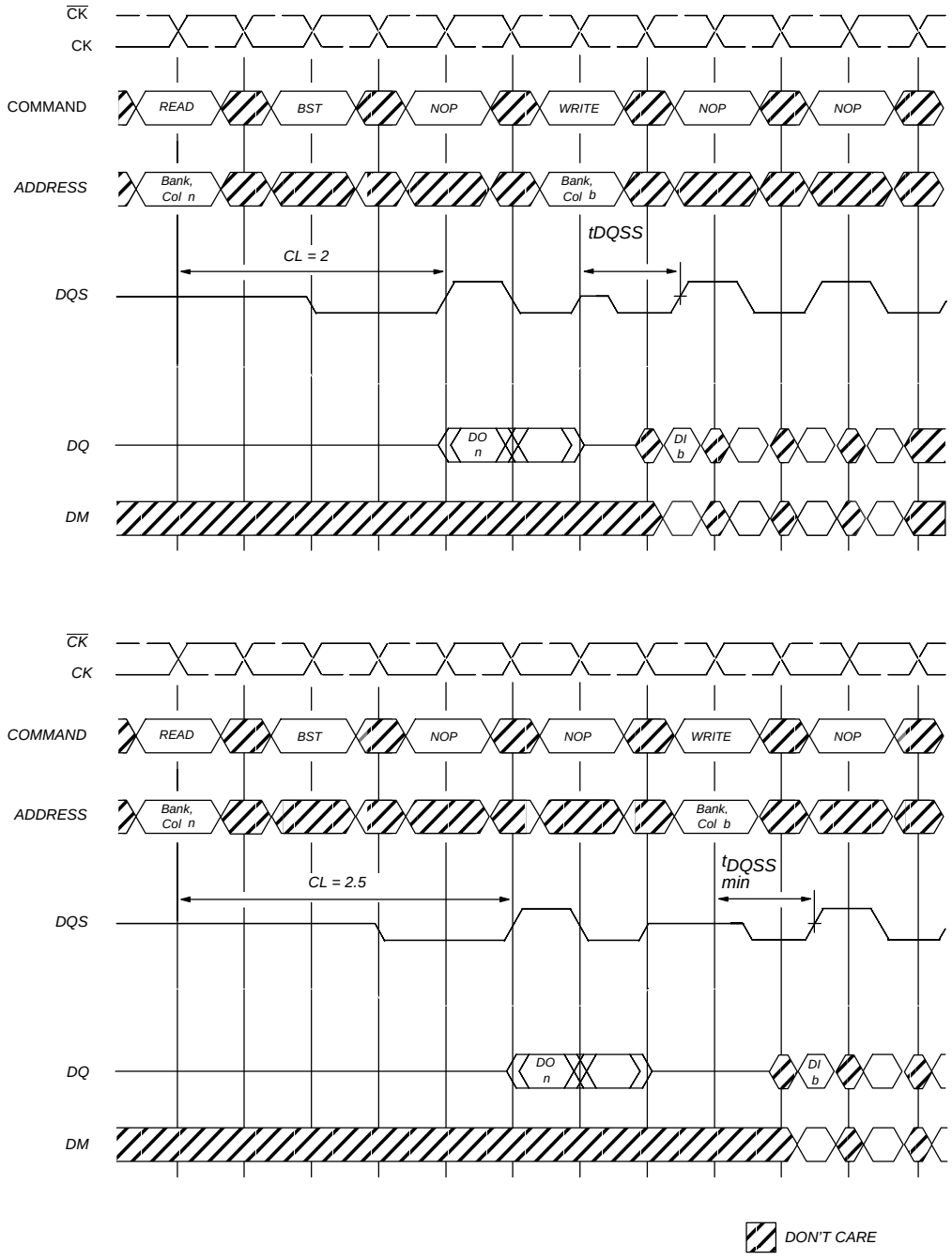
DO n, etc. = Data Out from column n, etc.
n' , etc. = the next Data Out following DO n, etc. according to the programmed burst order
Burst Length = 2, 4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted,
Reads are to active rows in any banks

Figure 14
RANDOM READ ACCESSES – REQUIRED CAS LATENCIES



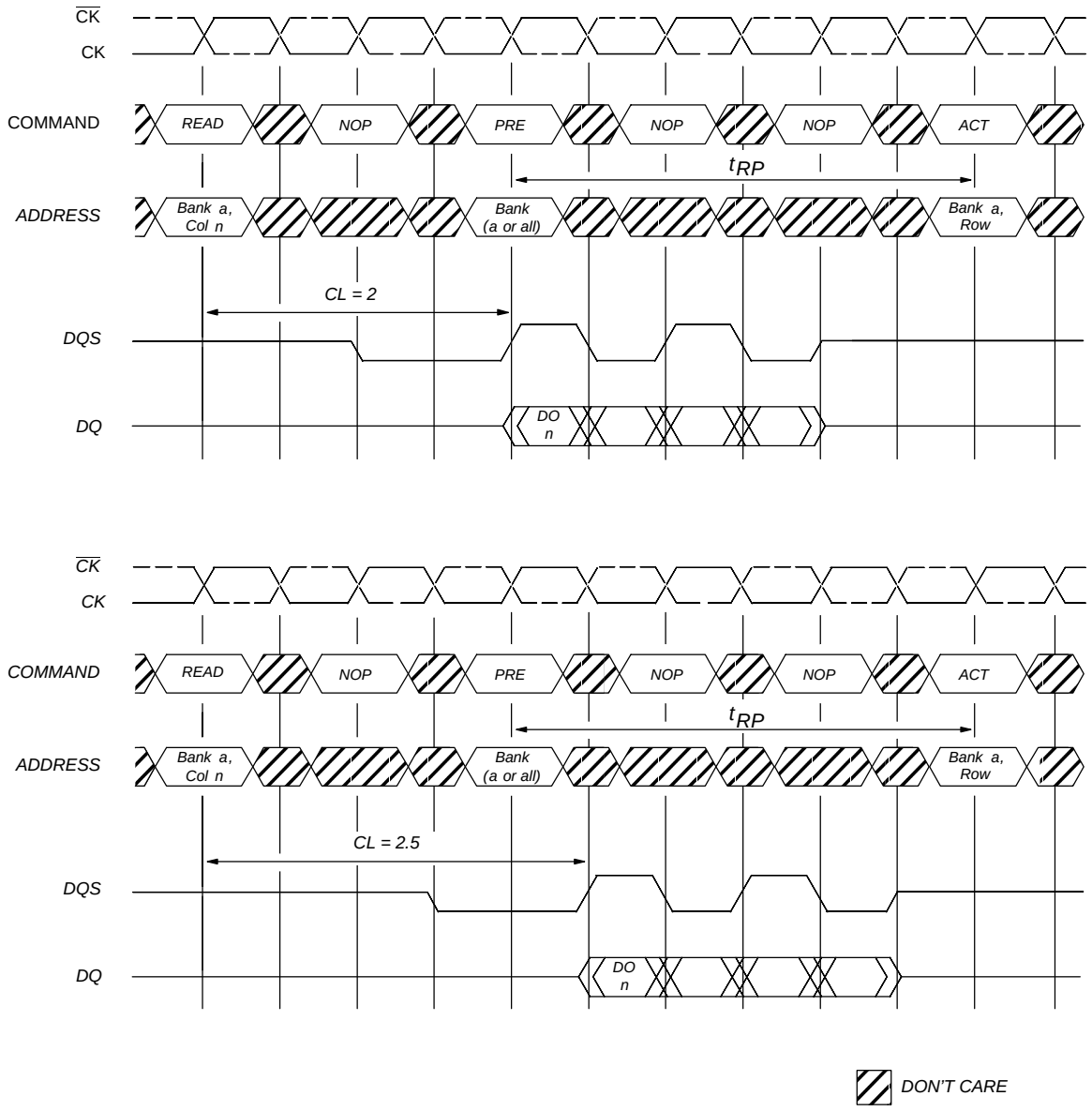
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 15
TERMINATING A READ BURST – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
1 subsequent element of Data Out appears in the programmed order following DO n
Data In elements are applied following DI b in the programmed order

Figure 16
READ TO WRITE – REQUIRED CAS LATENCIES



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Precharge may be applied at (BL/2) tCK after the READ command.
Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
The Active command may be applied if tRC has been met.

Figure 17
READ TO PRECHARGE – REQUIRED CAS LATENCIES

Writes

WRITE bursts are initiated with a WRITE command, as shown in Figure 18.

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data–in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data–in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle). Figures 19 and 20 show the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High–Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figure 22 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 23. Full–speed random write accesses within a page or pages can be performed as shown in Figure 24.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figure 25

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 26. and 27 Note that only the data–in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data–in must be masked with DM, as shown in Figures 26 and 27.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, tWR should be met as shown in Figure 28.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 29 and 30.

Note that only the data–in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data–in should be masked with DM, as shown in Figures 29 and 30. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

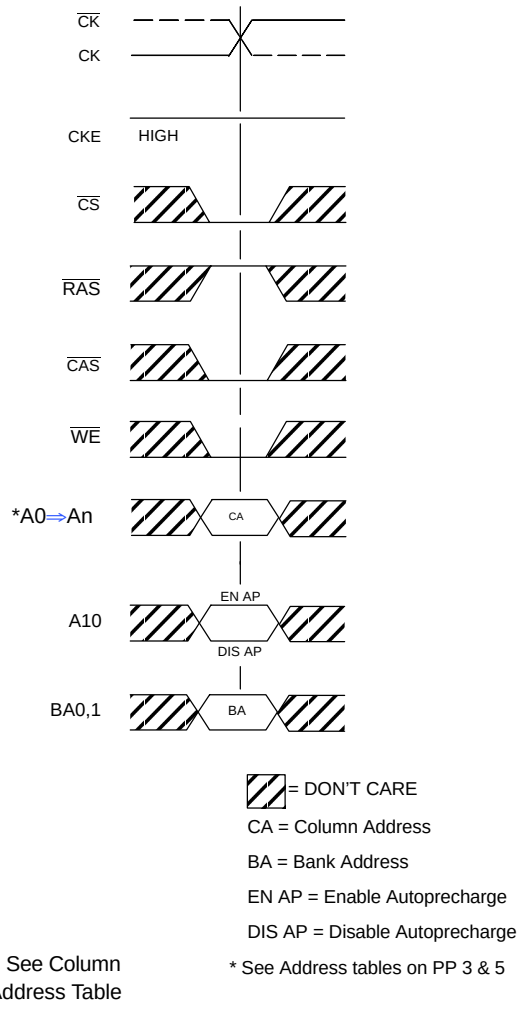
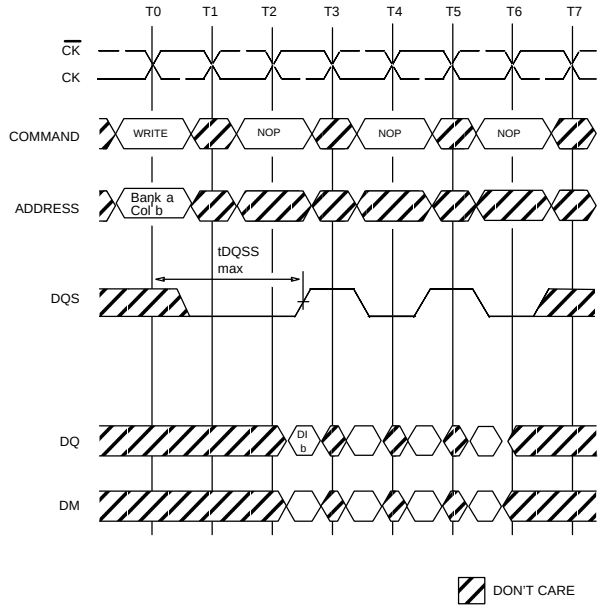
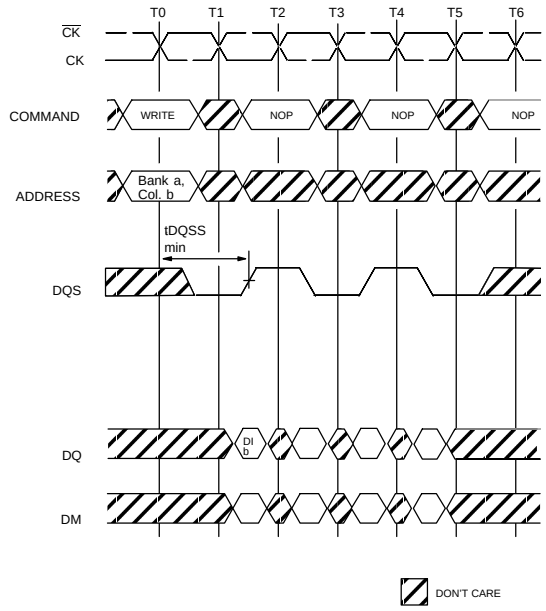


Figure 18
WRITE COMMAND



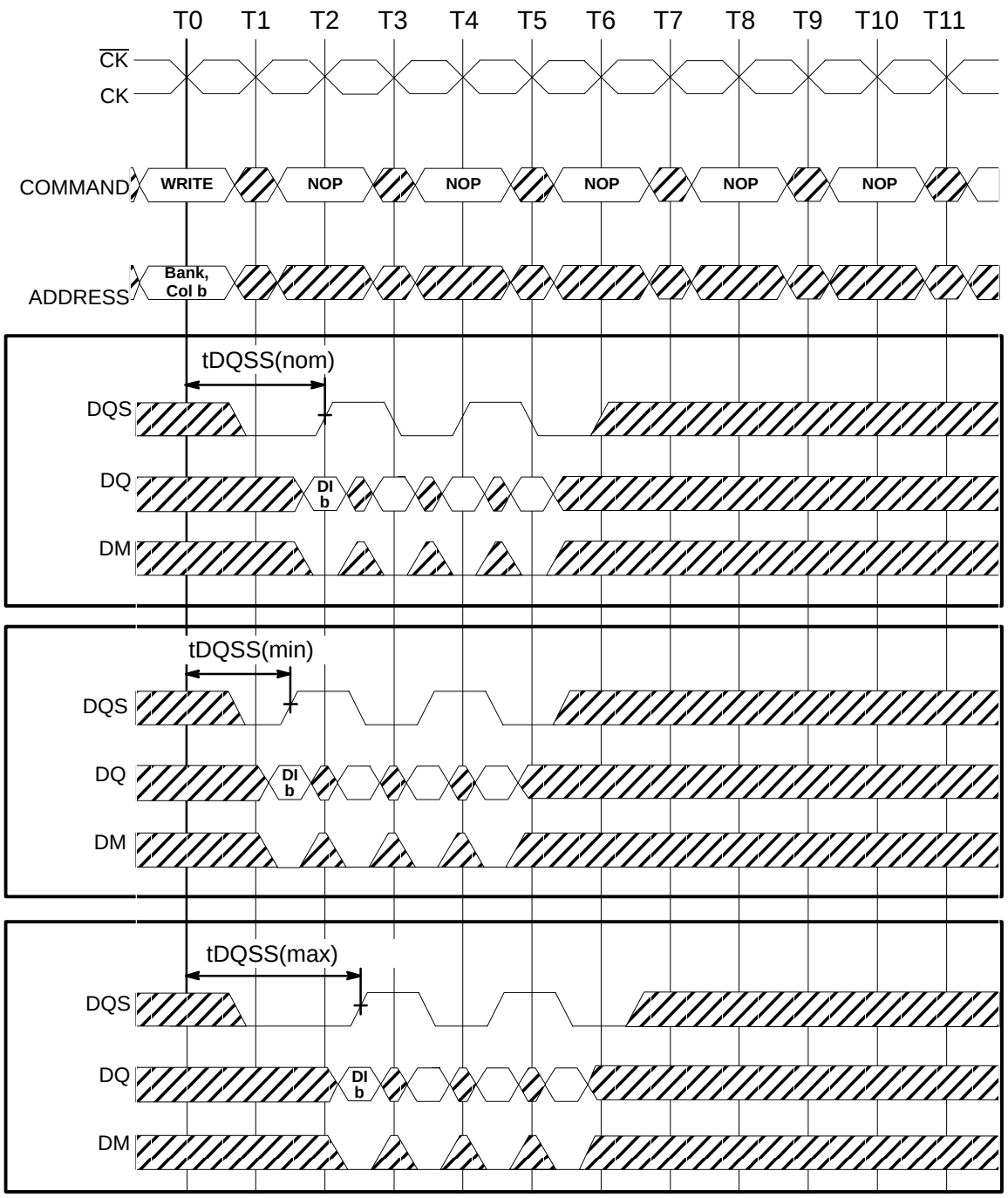
DI b = Data in for column b
3 subsequent elements of Data IN are applied in the programmed order following Di b
A non–interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Figure 19
WRITE – MAX DQSS



DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non–interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

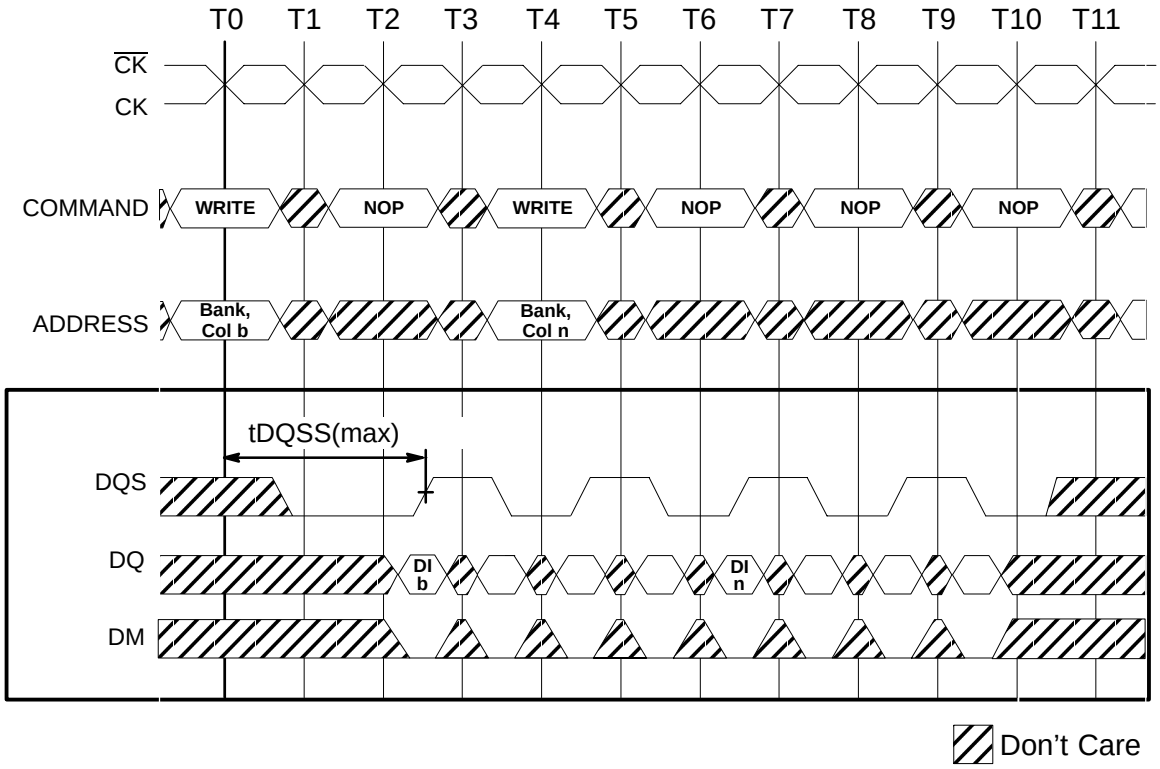
Figure 20
WRITE – MIN DQSS



DI b = Data In for column b
Three elements of data are applied in the programmed order following DI
A noninterrupted burst of 4 is shown
A10 is low with the WRITE command (autoprecharge is disabled)
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

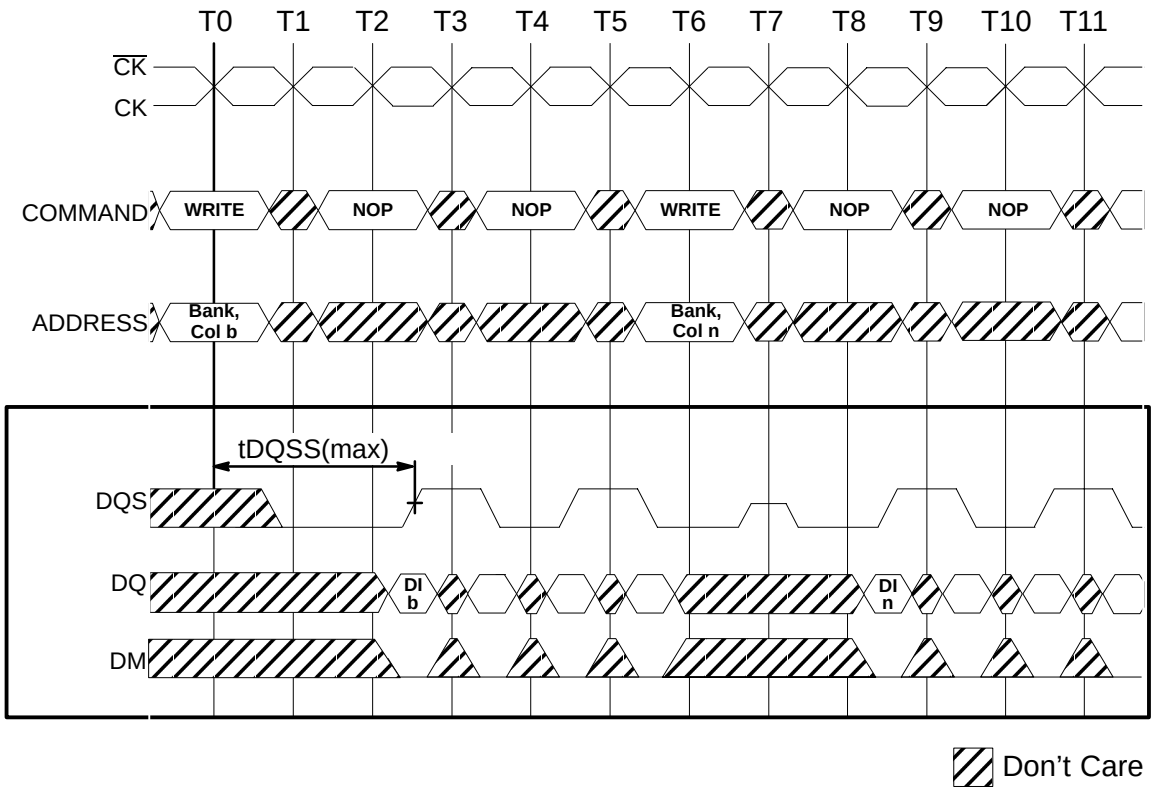
Don't Care

Figure 21
WRITE BURST – Nom., Min., and Max tDQSS



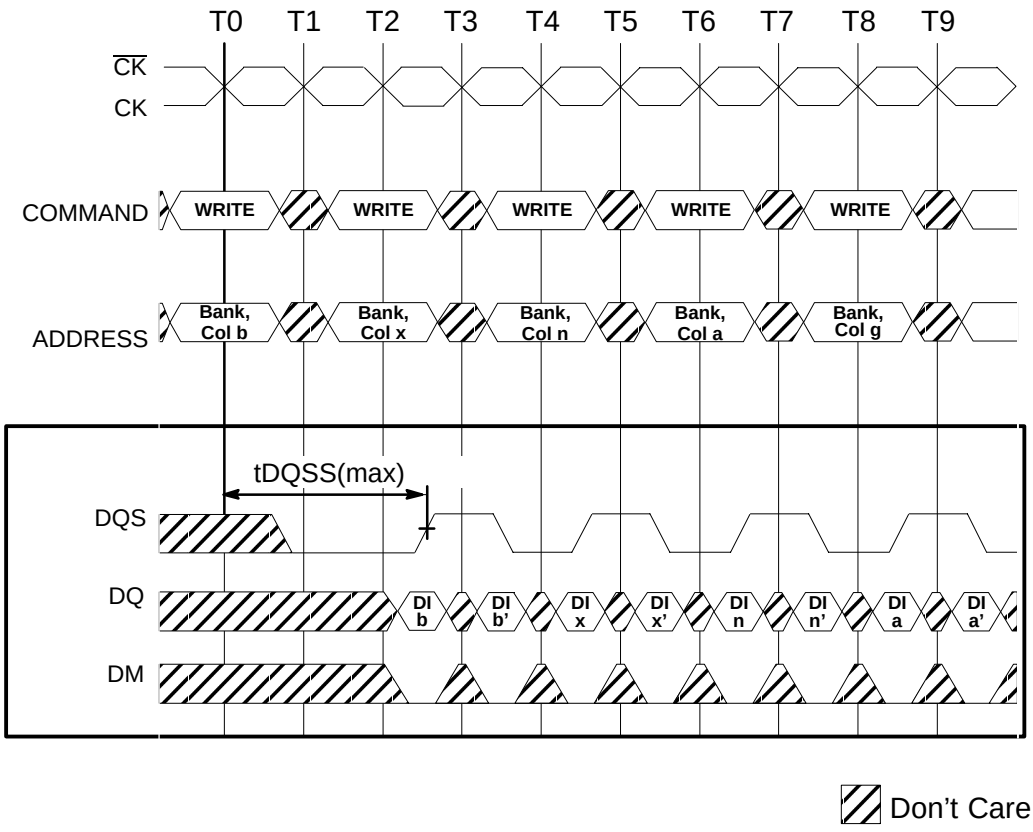
DI b, etc. = Data In for column b, etc.
Three subsequent elements of Data In are applied in the programmed order following DI b
Three subsequent elements of Data In are applied in the programmed order following DI n
Noninterrupted bursts of 4 are shown
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 22
WRITE TO WRITE – Max tDQSS



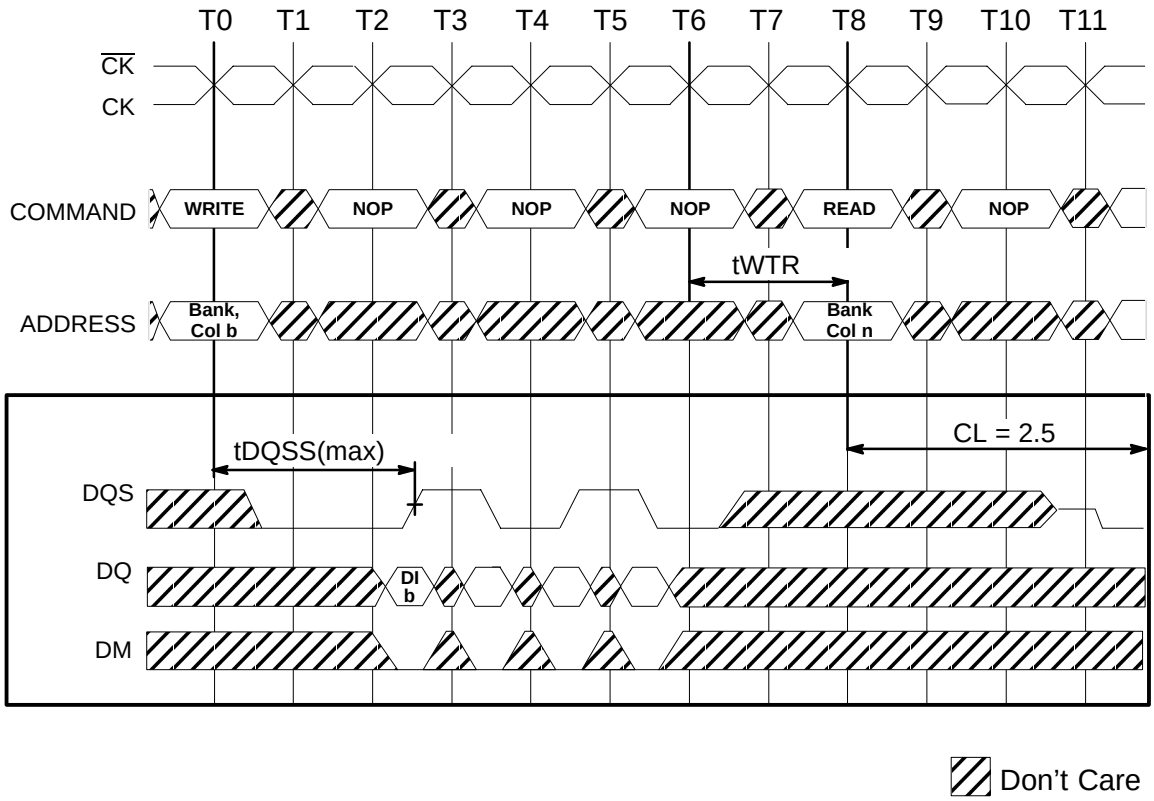
DI b, etc. = Data In for column b, etc.
Three subsequent elements of Data In are applied in the programmed order following DI b
Three subsequent elements of Data In are applied in the programmed order following DI n
Noninterrupted bursts of 4 are shown
Each WRITE command may be to any bank and may be to the same or different devices
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 23
WRITE TO WRITE – Max tDQSS, NON CONSECUTIVE



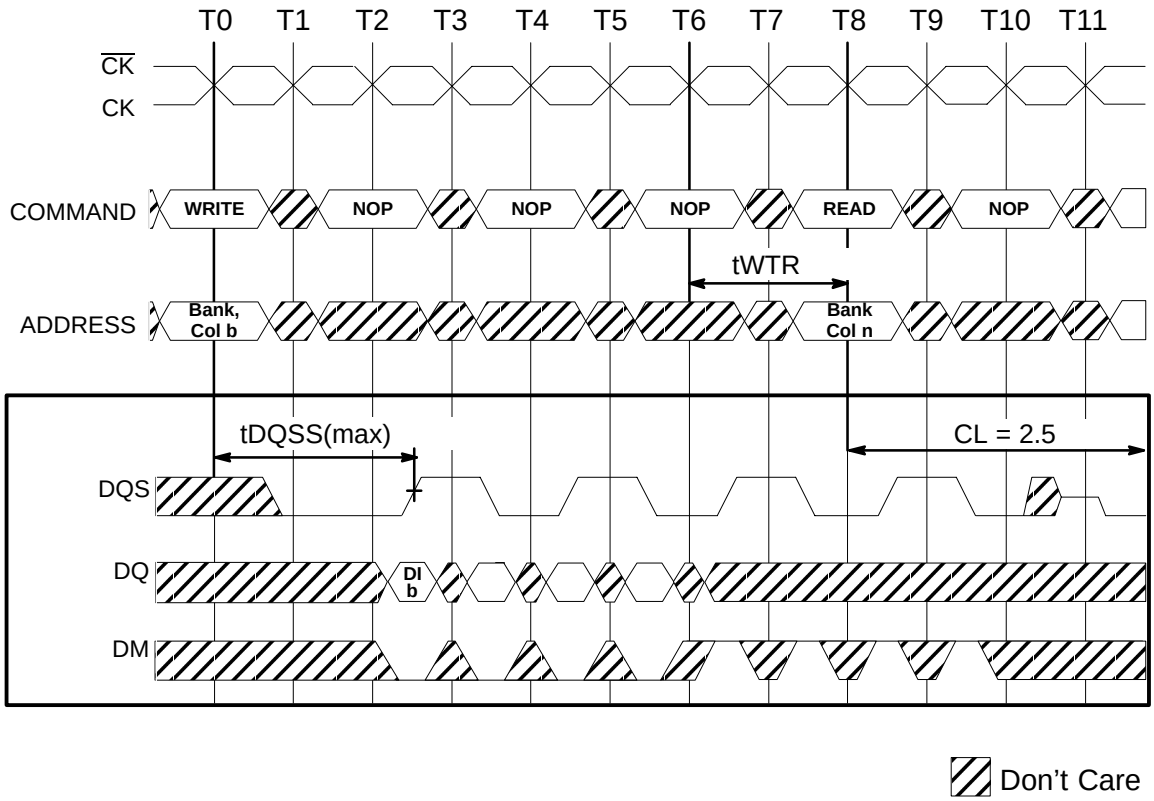
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order.
Programmed Burst Length = 2, 4, or 8 in cases shown.
If burst of 4 or 8, the burst would be truncated.
Each WRITE command may be to any bank and may be to the same or different devices.
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 24
RANDOM WRITE CYCLES – Max tDQSS



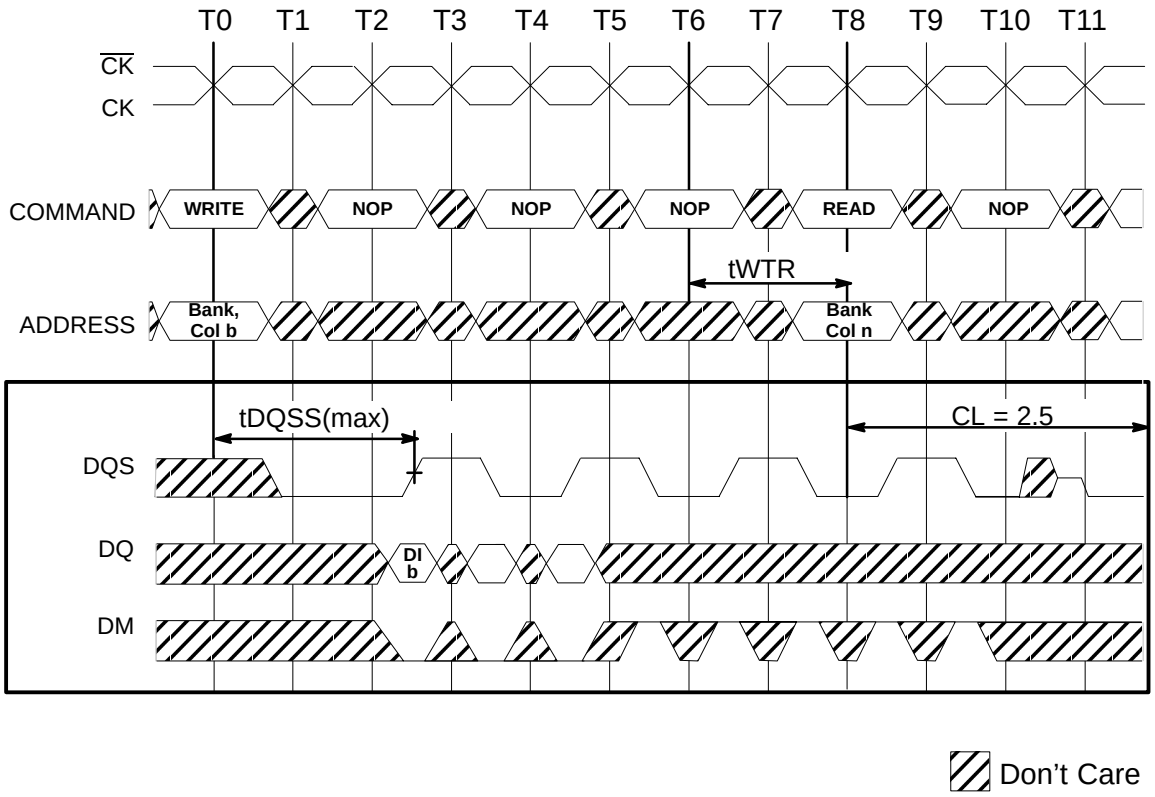
DI b = Data In for column b
Three subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 25
WRITE TO READ – Max tDQSS, NON–INTERRUPTING



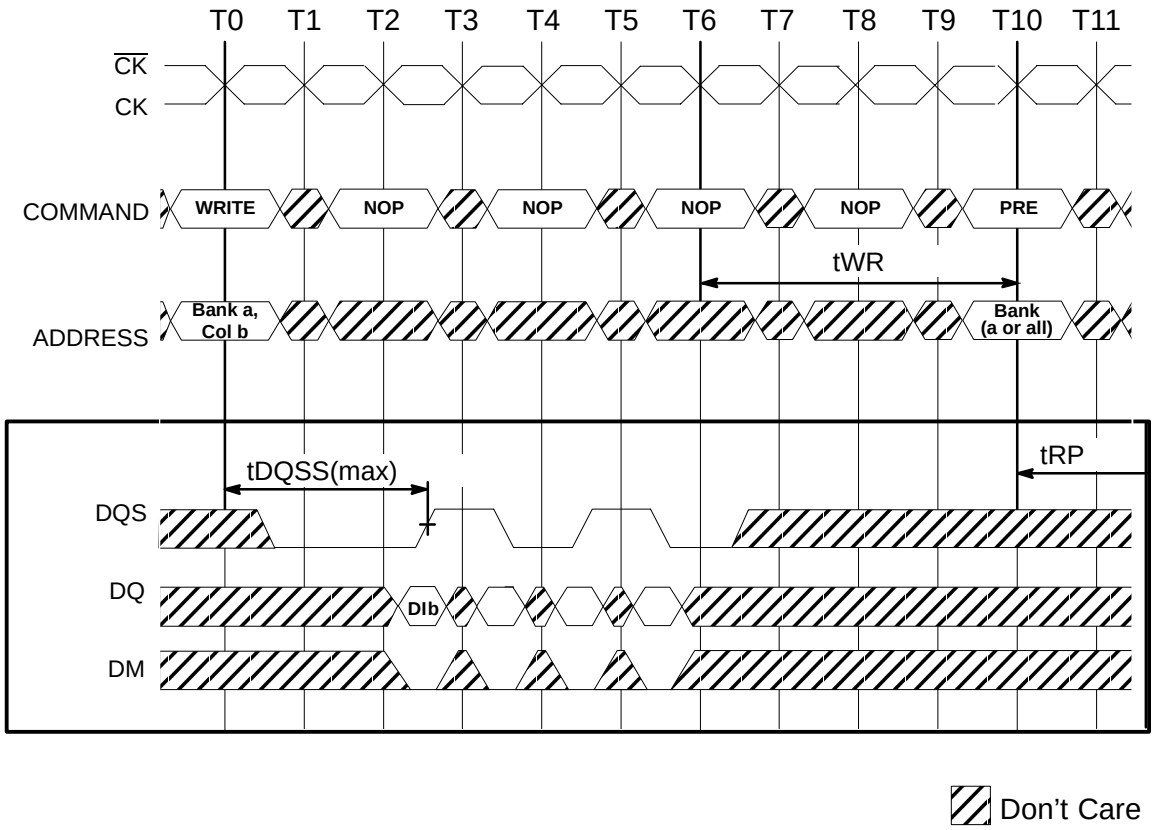
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
Three subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 26
WRITE TO READ – Max tDQSS, INTERRUPTING



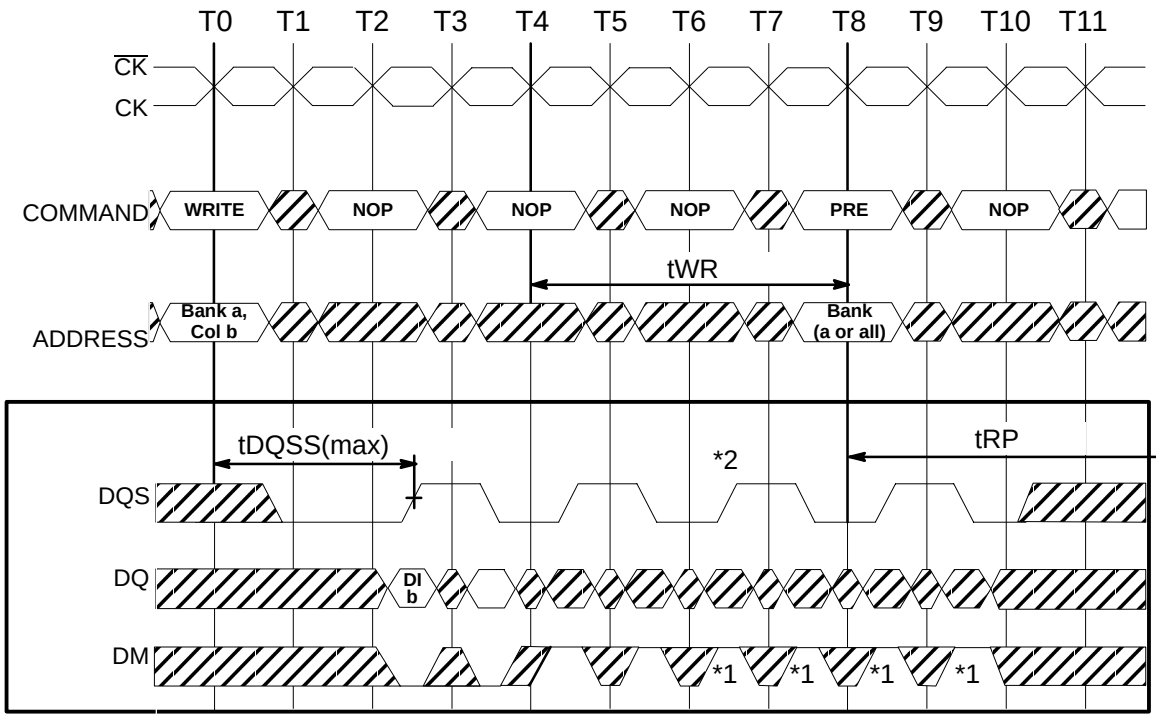
DI b = Data In for column b
An interrupted burst of 8 is shown, 3 data elements are written
Two subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair (not the last desired Data In element)
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Example is for x4 or x8 devices where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.
The READ and WRITE commands are to the same device but not necessarily to the same bank.

Figure 27
WRITE TO READ – Max tDQSS, ODD NUMBER OF DATA, INTERRUPTING



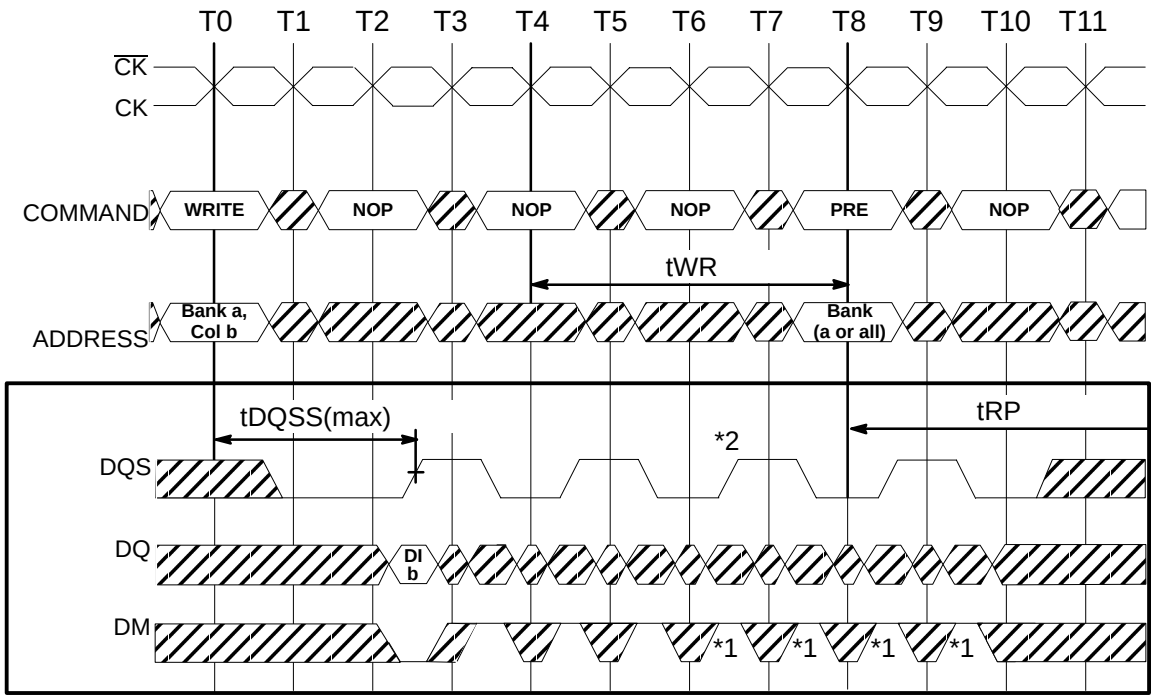
DI b = Data In for column b
Three subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 28
WRITE TO PRECHARGE – Max tDQSS, NON–INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
tWR is referenced from the first positive CK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 29
WRITE TO PRECHARGE – Max tDQSS, INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last desired Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 30
WRITE TO PRECHARGE – Max tDQSS,
ODD NUMBER OF DATA, INTERRUPTING

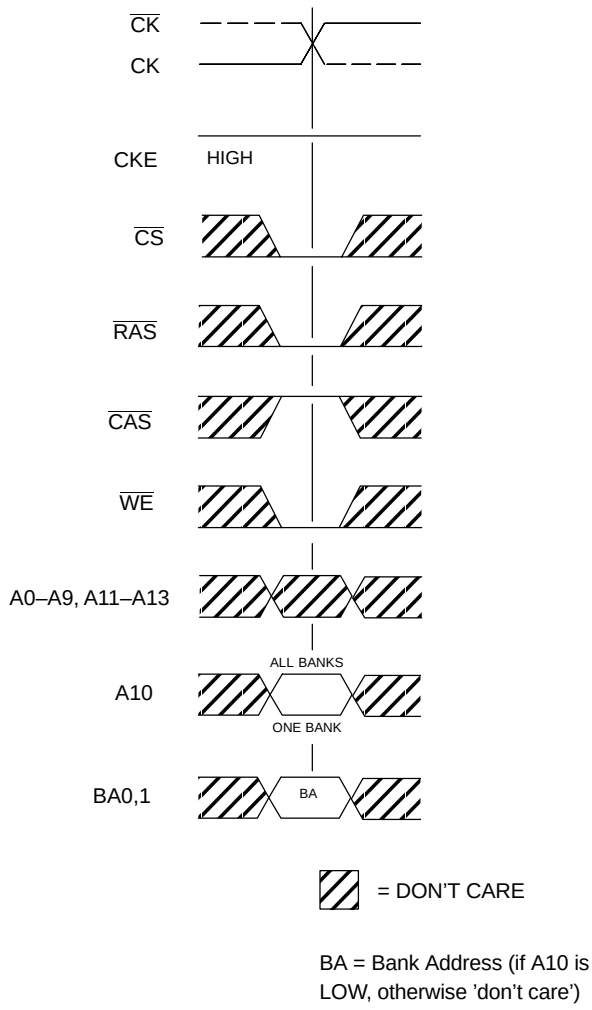


Figure 31
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER–DOWN

Power–down is entered when CKE is registered low (no accesses can be in progress and Table 2 criteria must be met). If power–down occurs when all banks are idle, this mode is referred to as precharge power–down; if power–down occurs when there is a row active in any bank, this mode is referred to as active power–down. Entering power–down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power–down. In that case, the DLL must be enabled after exiting power–down, and 200 clock cycles must occur before a READ command can be issued. However, power–down duration is limited by the refresh requirements of the device, so in most applications, the self–refresh mode is preferred over the DLL–disabled power–down mode.

In power–down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care".

The power–down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

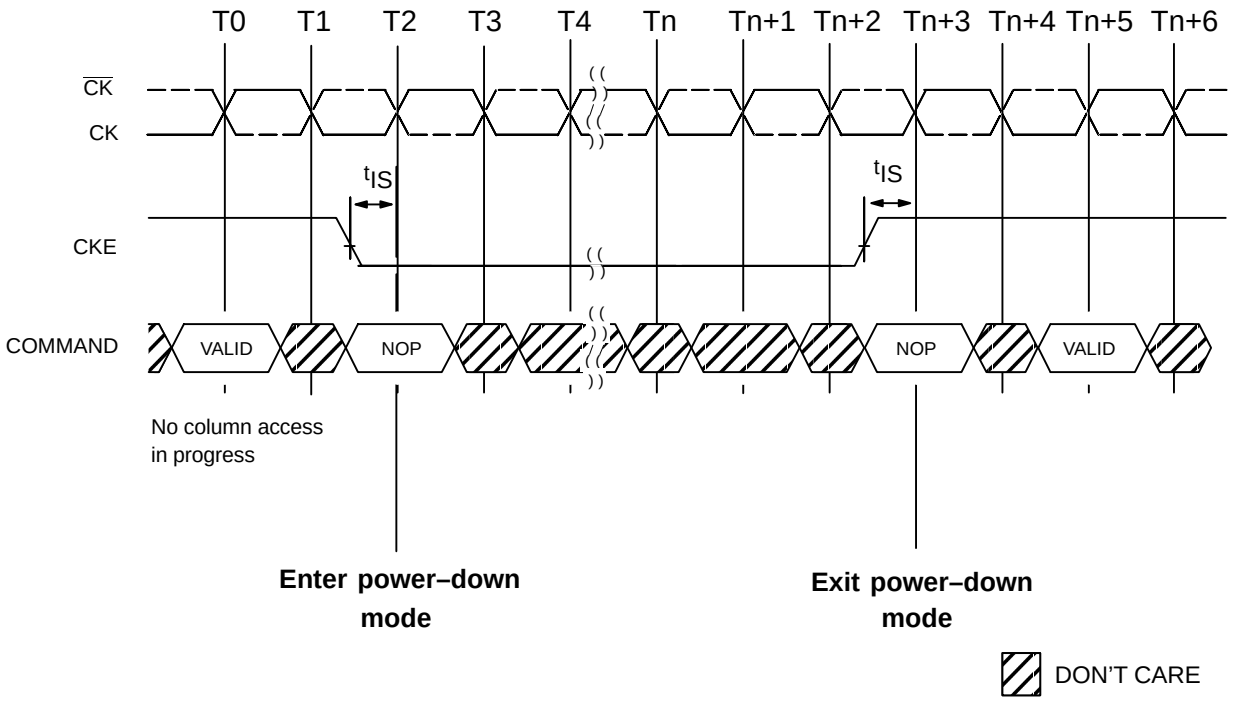


Figure 32
POWER–DOWN

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vdd Supply (For devices with nominal Vdd of 3.3 V)
Relative to Vss: –1 V to +4.6 V
Voltage on Vdd Supply (For devices with nominal Vdd of 2.5 V)
Relative to Vss: –1 V to +3.6 V
Voltage on VddQ Supply Relative to Vss: –1 V to +3.6 V
Voltage on Inputs Relative to Vss: –1 V to +3.6 V
Voltage on I/O Pins Relative to Vss: –0.5 V to VddQ+0.5 V

Operating Temperature, TA (ambient)	0 °C to +70 °C
Storage Temperature (plastic)	–55 °C to +150 °C
Power Dissipation	1 W
Short Circuit Output Current	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: CAPACITANCE

PARAMETER	PACKAGE	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance:CK, $\overline{CK}$	TSOP	Ci1	2.0	3.0	pF	a,d
	BGA		1.5	2.5		a,d
Delta Input Capacitance:CK, $\overline{CK}$	TSOP	Cdi1	–	0.25	pF	a,d
	BGA		–	0.25		a,d
Input Capacitance: All other input–only pins	TSOP	Ci2	2	3	pF	a,d
	BGA		1.5	2.5		a,d
Delta Input Capacitance: All other input–only pins	TSOP	Cdi2	–	0.5	pF	a,d
	BGA		–	0.5		a,d
Input/Output Capacitance: DQ, DQS, DM	TSOP	Cio	4.0	5.0	pF	a,b,c,d
	BGA		3.5	4.5		a,b,c,d
Delta Input/Output Capacitance: DQ, DQS, DM	TSOP	Cdio	–	0.5	pF	a,b,c,d
	BGA		–	0.5		a,b,c,d

a) These values are guaranteed by design and are tested on a sample basis only.
b) Although DM is an input–only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
c) Unused pins are tied to ground.
d).This parameter is sampled. VDDQ = +2.5 V +0.2 V, VDD = +3.3 V +0.3 V or +2.5 V +0.2 V , f = 100 MHz, tA = 25 5C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2 V. DM inputs are grouped with I/O pins – reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
e) The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25 V to 1.0 V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

TABLE 6: ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	7
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	8
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.15	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	–0.3	VREF–0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN(DC)	–0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	9
V–I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	–	e
INPUT LEAKAGE CURRENT, Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	IL	–2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	–5	5	µA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	IOH IOL	–16.2 16.2		mA mA	

TABLE 7: AC OPERATING CONDITIONS

(Notes: 1–6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(ac)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(ac)		VREF – 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(ac)	0.7	VDDQ + 0.6	V	9
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(ac)	0.5*VDDQ–0.2	0.5*VDDQ+0.2	V	10

TABLE 8: IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

This table is provided for the users of this Standard so that suppliers use a common format for parameter definitions of their individual IDD specifications. Values will be specific to each supplier.

Conditions	Symbol	Typ	Max
Operating current for one bank active-precharge; $t_{RC} = t_{RC}(min)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; $\overline{CS}$ = high between valid commands.	IDD0	-	-
Operating current for one bank operation; one bank open, BL = 4, reads - Refer to the following page for detailed test conditions: $\overline{CS}$ = high between valid commands.	IDD1	-	-
Precharge power-down standby current; all banks idle; power-down mode; CKE ≤ $V_{IL}(max)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266A, DDR266B, 6 ns for DDR333; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2P	-	-
Precharge floating standby current; $\overline{CS}$ ≥ $V_{IH}(min)$; all banks idle; CKE ≥ $V_{IH}(min)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2F	-	-
Precharge quiet standby current; $\overline{CS}$ ≥ $V_{IH}(min)$; all banks idle; CKE ≥ $V_{IH}(min)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; address and other control inputs stable at ≥ $V_{IH}(min)$ or ≤ V_{IL} (max); $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2Q	-	-
Active power-down standby current ; one bank active; power-down mode; CKE ≤ $V_{IL}(max)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD3P	-	-
Active standby current; $\overline{CS}$ ≥ $V_{IH}(min)$; CKE ≥ $V_{IH}(min)$; one bank active; $t_{RC} = t_{RAS}(max)$; t_{CK} = 10 ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	-	-
Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; CL = 2 at t_{CK} = 10 ns for DDR200, CL = 2 at t_{CK} = 7.5 ns for DDR266A, CL = 2.5 at t_{CK} = 7.5 ns for DDR266B, 6 ns for DDR333; 50% of data changing on every transfer; I_{OUT} = 0 mA	IDD4R	-	-
Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; CL = 2 at t_{CK} = 10 ns for DDR200, CL = 2 at t_{CK} = 7.5 ns for DDR266A, CL = 2.5 at t_{CK} = 7.5 ns for DDR266B, 6 ns for DDR333; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	IDD4W	-	-
Auto refresh current; $t_{RC} = t_{RFC}(min)$ which is 8 * t_{CK} for DDR200 at t_{CK} = 10 ns, 10 * t_{CK} for DDR266 at t_{CK} = 7.5 ns; 12 * t_{CK} for DDR333 at t_{CK} = 6ns;	IDD5	-	-
Self refresh current; CKE ≤ 0.2 V; external clock on; t_{CK} = 10 ns for DDR200, t_{CK} = 7.5 ns for DDR266, 6 ns for DDR333	IDD6	-	-
Operating current for four bank operation; four bank interleaving with BL = 4 - Refer to the following page for detailed test condition	IDD7	-	-
Typical case : V_{DD} = 2.5 V, T = 25 °C Worst case : V_{DD} = 2.7 V, T = 10 °C Self refresh: normal/low power respectively Measured values for all items will be averaged from repeated cycles with the above description			

Detailed test conditions for DDR SDRAM IDD1 and IDD7

Typical Case: V_{DD} = 2.5 V, T = 25° C, Worst Case: V_{DD} = 2.7 V, T = 10° C
Legend: A = Active, R = Read, RA = Read with Autoprecharge, P = Precharge, N = DESELECT

IDD1 : Operating current: One bank operation

Only one bank is accessed with t_{RC}(min), Burst Mode, Address and Control inputs change logic state once per Deselect cycle. I_{OUT} = 0 mA

Timing patterns

- DDR200 (100 MHz, CL = 2): t_{CK} = 10 ns, BL = 4, t_{RCD} = 2 * t_{CK}, **t_{RC} = 7 * t_{CK},** t_{RAS} = 5 * t_{CK}
  Setup: A0 N R0 N N P0 N
  Read: A0 N R0 N N P0 N - repeat the same timing with random address changing 50% of data changing at every transfer

- DDR266B (133 MHz, CL = 2.5): t_{CK} = 7.5 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 9 * t_{CK}, **t_{RAS} = 6 * t_{CK}**
- DDR266A (133 MHz, CL = 2): t_{CK} = 7.5 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 9 * t_{CK}, **t_{RAS} = 6 * t_{CK}**
  Setup: A0 N N R0 N N P0 N N
  Read: A0 N N R0 N N P0 N N - repeat the same timing with random address changing 50% of data changing at every transfer

- DDR333B (167 MHz, CL = 2.5): t_{CK} = 6 ns, BL = 4, t_{RCD} = 3 * t_{CK}, t_{RC} = 10 * t_{CK}, t_{RAS} = 7 * t_{CK}
  Setup: A0 N N R0 N N N P0 N N
  Read: A0 N N R0 N N N P0 N N - repeat the same timing with random address changing 50% of data changing at every transfer

IDD7 : Operating current: Four bank operation

Four banks are being interleaved with t_{RC}(min), Burst Mode, Address and Control inputs on Deselect edge are not changing. I_{OUT} = 0 mA

Timing patterns

- DDR200 (100 MHz, CL = 2): t_{CK} = 10 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 5 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2
  Read: A0 RA3 A1 RA0 A2 RA1 A3 RA2 - repeat the same timing with random address changing 50% of data changing at every transfer

- DDR266B (133 MHz, CL = 2.5): t_{CK} = 7.5 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 6 * t_{CK}
- DDR266A (133 MHz, CL = 2): t_{CK} = 7.5 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 6 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer

- DDR333B (167 MHz, CL = 2.5): t_{CK} = 6 ns, BL = 4, t_{RRD} = 2 * t_{CK}, t_{RCD} = 3 * t_{CK}, t_{RAS} = 7 * t_{CK}
  Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
  Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer

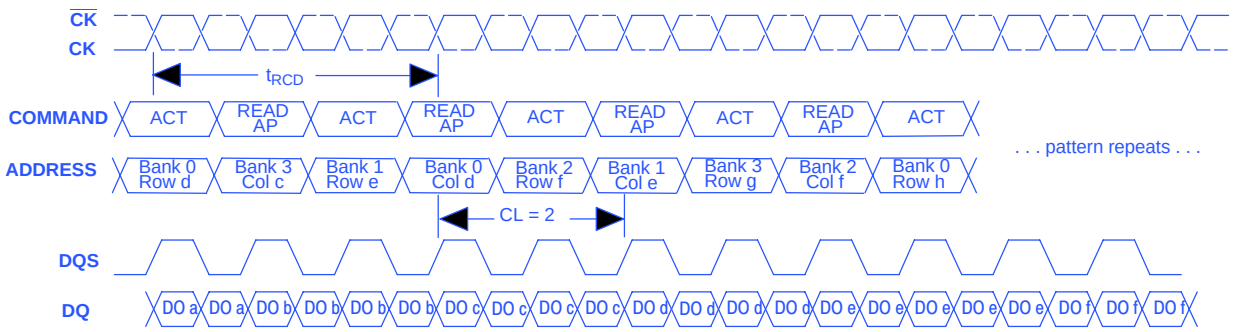


FIGURE 33: Timing waveform for IDD7 measurement at 100 MHz Ck operation

TABLE 9: ELECTRICAL CHARACTERISTICS AND AC TIMING

All specification parameters are guaranteed by the supplier, but it is not implied that this table represents a test specification.

Absolute Specifications (Notes: 1–6, 13, 14) (0°C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		DDR333		DDR266		DDR200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ output access time from CK/$\overline{CK}$	tAC	–0.70	+0.70	–0.75	+0.75	–0.8	+0.8	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	–0.60	+0.60	–0.75	+0.75	–0.8	+0.8	ns	
CK high–level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low–level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	24, 25
Clock cycle time CL = 2.5	tCK	6	12	7.5	12	10	12	ns	30
CL = 2	tCK	7.5	12	7.5	12	10	12	ns	30
DQ and DM input hold time	tDH	0.45		0.5		0.6		ns	j, k
DQ and DM input setup time	tDS	0.45		0.5		0.6		ns	j, k
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.5		ns	22
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		2		ns	22
DQ & DQS high–impedance time from CK/$\overline{CK}$	tHZ		+0.70		+0.75		+0.8	ns	15
DQ & DQS low–impedance time from CK/$\overline{CK}$	tLZ	–0.70	+0.70	–0.75	+0.75	–0.8	+0.8	ns	15
DQS–DQ Skew (for DQS and associated DQ signals) TSOP Package	tDQSQ		+0.45		+0.5		+0.6	ns	26
BGA Package	tDQSQ		+0.4		+0.5		+0.6	ns	26
DQ/DQS output hold time from DQS	tQH	tHP-tQHS		tHP-tQHS		tHP-tQHS		ns.	25
Data Hold Skew Factor (for DQS and associated DQ Signals) TSOP Package	tQHS		+0.55		+0.75		+1.0	ns	25
BGA Package	tQHS		+0.5		+0.75		+1.0	ns	25
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	2		2		2		tCK	
Write preamble setup time	tWPRES	0		0		0		ns	17
Write postamble	tWPST	0.40	0.60	0.4	0.6	0.40	0.60	tCK	16
Write preamble	tWPRE	0.25		0.25		0.25		tCK	
Address and Control input hold time (fast slew rate)	tIH	0.75		0.9		1.1		ns	i, 19, 21-23
Address and Control input setup time (fast slew rate)	tIS	0.75		0.9		1.1		ns	i, 19, 21-23
Address and Control input hold time (slow slew rate)	tIH	0.80		1.0		1.1		ns	i, 20-23
Address and Control input setup time (slow slew rate)	tIS	0.80		1.0		1.1		ns	i, 20-23
Read preamble CL=2.5	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	28
CL = 2.0		0.9	1.1	0.9	1.1	0;9	1.1	tCK	28
CL = 1.5		N/A	N/A	N/A	N/A	–	1.1	tCK	28
Read preamble setup time (Optional CL=1.5)	tRPRES		N/A		N/A		1.5	ns	28
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE to PRECHARGE command	tRAS	42	70,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	60		65		70		ns	
Auto Refresh to Active/Auto Refresh command period 64Mb, 512Mb	tRFC	72		75		80		ns	
1Gb		120		120		120		ns	
ACTIVE to READ or WRITE delay	tRCD	18		20		20		ns	
PRECHARGE command period	tRP	18		20		20		ns	
Active to Autoprecharge Delay	tRAP	tRCD or tRASmin		tRCD or tRASmin		tRCD or tRASmin		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	12		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	—		—		—		tCK	27
Internal Write to Read Command Delay CL=2.5	tWTR	1		1		1		tCK	
CL=2.0		1		1		1		tCK	
CL=1.5		N/A		N/A		2		tCK	
Exit self refresh to non–READ command 64Mb to 512 Mb	tXSNR	75		75		80		ns	29
1Gb		126		127.5		130			
Exit self refresh to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval 64Mb, 128Mb	tREFI		15.6		15.6		15.6	µs	18
256Mb. 1Gb			7.8		7.8		7.8	µs	18

TABLE 10: AC TIMING VARIATIONS FOR DDR333, DDR266, & DDR200

This table defines several parameters that differ from those given in Table 9 to establish A & B variants of the primary speed sort specifications for DDR200, DDR266, & DDR333.

	DDR333B		DDR266A		DDR266B		DDR200		DDR200B		Units
Parameter	min	max	min	max	min	max	min	max	min	max	ns
tAC	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
tDQSCK	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
tCK CL = 2.5	6	12	7.5	12	7.5	12	10	12	10	12	ns
tCK CL = 2.0	7.5	12	7.5	12	10	12	10	12	10	12	ns
tRRD	12		15		15		15		20		ns
tWR	15		15		15		15		20		ns

Component Notes

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 34 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

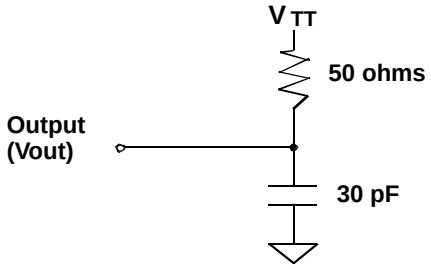


Figure 34: Timing Reference Load

4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/$\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.2VDDQ is recognized as LOW.
7. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak–to–peak noise on VREF may not exceed +/–2% of the dc value.
8. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
9. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
10. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
11. Enables on–chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$, is VREF.
14. The output timing reference voltage level is VTT.
15. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

17. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High–Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
18. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
19. For command/address input slew rate $\geq$1.0 V/ns
20. For command/address input slew rate $\geq$0.5 V/ns and $<$1.0 V/ns
21. For CK & $\overline{CK}$ slew rate $\geq$1.0 V/ns
22. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
23. Slew Rate is measured between VOH(ac) and VOL(ac).
24. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
25. tQH = tHP – tQHS, where:
    tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on–chip clock circuits; and 2) The worst case push–out of DQS on one transition followed by the worst case pull–in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p–channel to n–channel variation of the output drivers.
26. **tDQSQ**
    Consists of data pin skew and output pattern effects, and p–channel to n–channel variation of the output drivers for any given cycle.
27. **tDAL = (tWR/tCK) + (tRP/tCK)**
    For each of the terms above, if not already an integer, round to the next highest integer.
    Example: For DDR266B at CL=2.5 and tCK=7.5 ns
    tDAL = ((15 ns / 7.5 ns) + (20 ns / 7.5 ns)) clocks
    = ((2) + (3)) clocks
    = 5 clocks

28 Optional CAS Latency, 1.5, is only defined for DDR200 speed grade

29 In all circumstances, tXSNR can be satisfied using tXSNR = tRFCmin + 1*tCK

30 The only time that the clock frequency is allowed to change is during self–refresh mode.

SYSTEM CHARACTERISTICS for DDR SDRAMS

The following specification parameters are required in systems using DDR333, DDR266 & DDR200 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

Table 11: Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR333		DDR266		DDR200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	0.5	4.0	V/ns	a, m

Table 12: Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	ΔtIS	ΔtIH	UNITS	NOTES
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 13: Input/Output Setup & Hold Time Derating for Slew Rate

I/O Input Slew Rate	ΔtDS	ΔtDH	UNITS	NOTES
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 14: Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	ΔtDS	ΔtDH	UNITS	NOTES
±0.0 ns/V	0	0	ps	j
±0.25 ns/V	+50	+50	ps	j
±0.5 ns/V	+100	+100	ps	j

Table 15: Output Slew Rate Characteristics (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 – 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown Slew Rate	1.2 – 2.5	1.0	4.5	b,c,d,f,g,h

Table 16: Output Slew Rate Characteristics (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 – 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown Slew Rate	1.2 – 2.5	0.7	5.0	b,c,d,f,g,h

Table 17: Output Slew Rate Matching Ratio Characteristics

Slew Rate Characteristic	DDR266A		DDR266B		DDR200		
PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Output Slew Rate Matching Ratio (Pullup to Pulldown)	–	–	–	–	0.71	1.4	e,m

Table 18: AC Overshoot/Undershoot Specification for Address and Control Pins
This specification is intended for devices with no clamp protection and is guaranteed by design

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot (See Figure 35):	TBD	1.5 V
Maximum peak amplitude allowed for undershoot (See Figure 35):	TBD	1.5 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 35):	TBD	4.5 V–ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 35):	TBD	4.5 V–ns

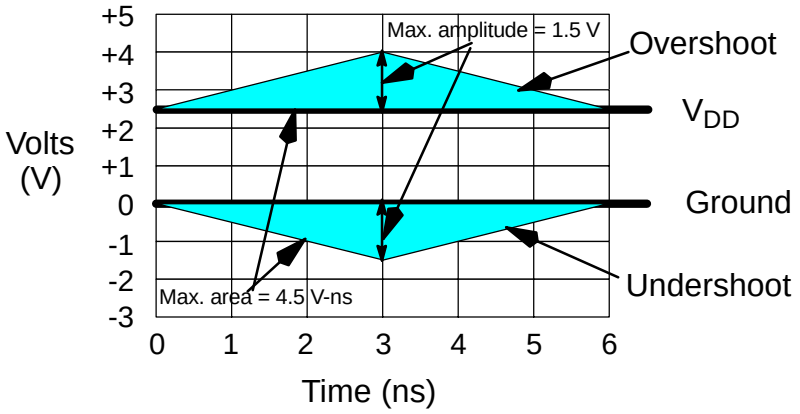


Figure 35: Address and Control AC Overshoot and Undershoot Definition

TABLE 19: Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot (See Figure 36):	TBD	1.2 V
Maximum peak amplitude allowed for undershoot (See Figure 36):	TBD	1.2 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 36):	TBD	2.4 V–ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 36):	TBD	2.4 V–ns

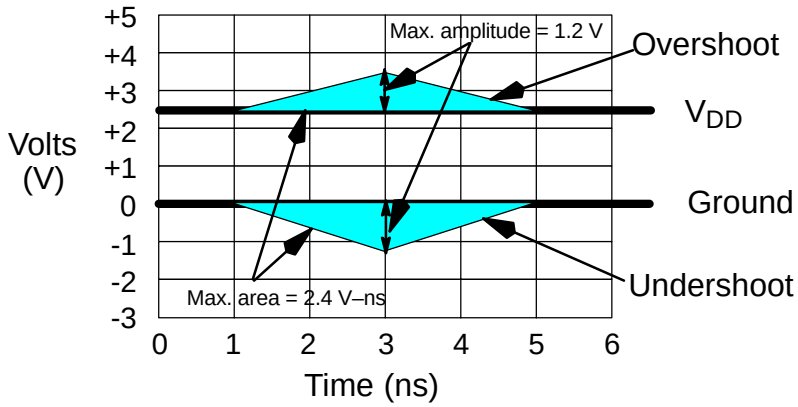


Figure 36: DQ/DM/DQS AC Overshoot and Undershoot Definition

TABLE 20. Clamp V–I Characteristics for Address, Control and Data Pins

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0.1
0.8	0.1	0.6
0.9	1.0	1.8
1.0	2.5	3.4
1.1	4.7	5.6
1.2	6.8	7.6
1.3	9.1	10.0
1.4	11.0	13.0
1.5	13.5	15.4
1.6	16.0	18.0
1.7	18.2	21.6
1.8	21.0	25.0
1.9	23.3	28.0
2.0	26.0	31.0
2.1	28.2	34.4
2.2	31.0	38.0
2.3	33.0	42.0
2.4	35.0	46.0
2.5	37.0	50.0

Power & Ground Clamp V–I Characteristics

System Notes:

a. Pullup slew rate is characteristized under the test conditions as shown in Figure 37.

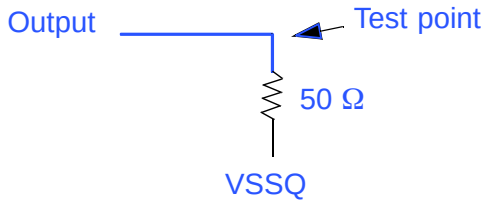


Figure 37: Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 38.

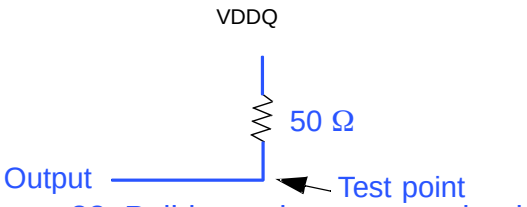


Figure 38: Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 – 320 mV ± 250 mV)
Pulldown slew rate is measured between (VDDQ/2 + 320 mV ± 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew rate, DQ0 is switching
For minimum slew rate, all DQ bits are switching worst case pattern
For maximum slew rate, only one DQ is switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical: 25 °C (T Ambient), VDDQ = 2.5 V, typical process
Minimum: 70 °C (T Ambient), VDDQ = 2.3 V, slow–slow process
Maximum: 0 °C (T Ambient), VDDQ = 2.7 V, fast–fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table 12. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 13 & 14. Input slew rate is based on the larger of AC–AC delta rise, fall rate and DC–DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as:
{1/(Slew Rate1)}–{1/(slew Rate2)}
For example: If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise,fall rate is –0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

XILINX EXHIBIT 1010
Page 587

k. Table 13 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC–AC slew rate and the DC–DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

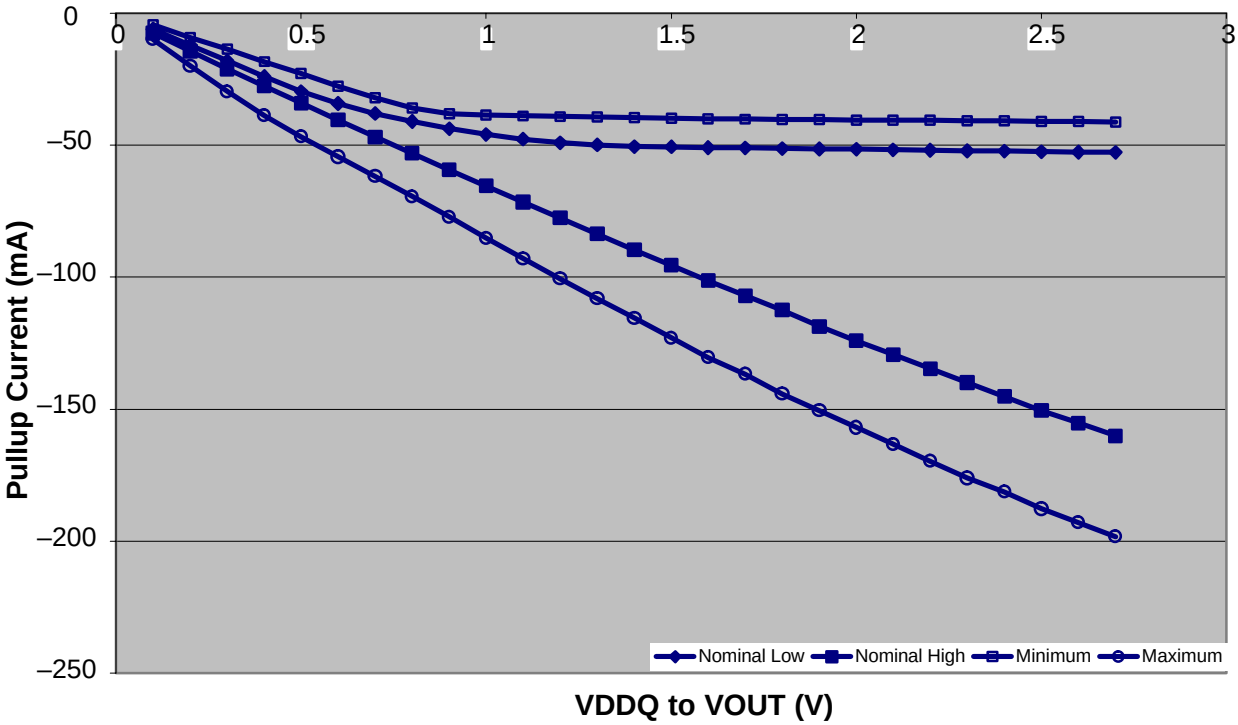


Figure 39a: Pullup characteristics for Full Strength Output Driver

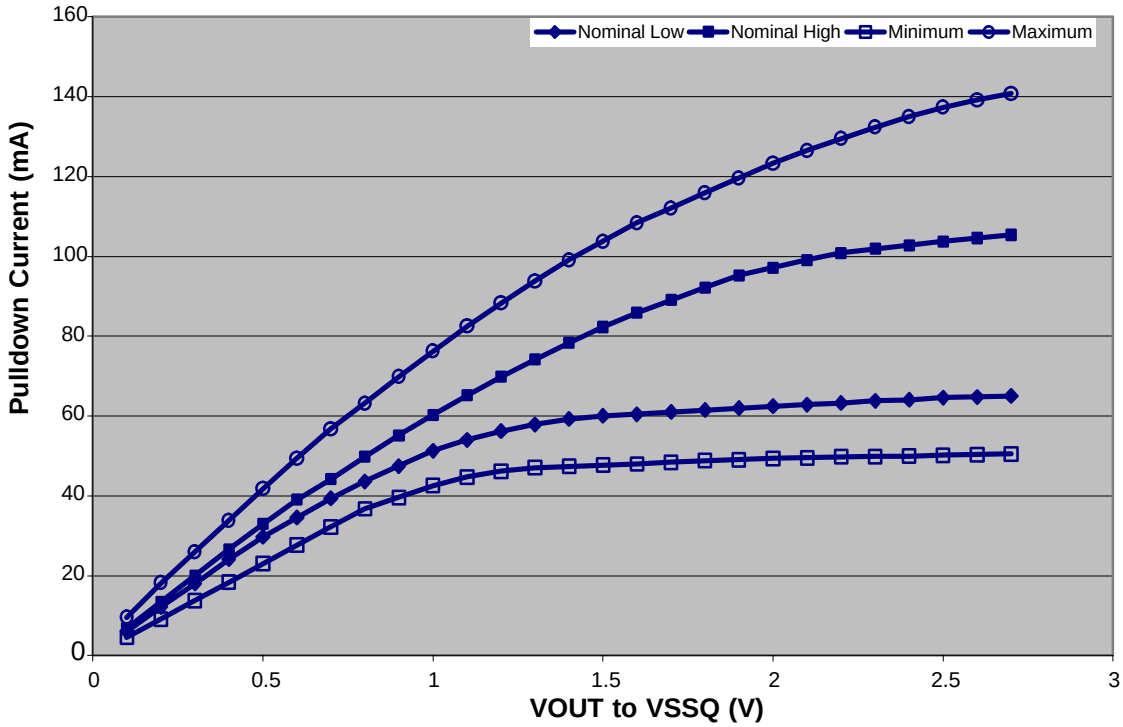


Figure 39b: Pulldown characteristics for Full Strength Output Driver

FIGURE 39: FULL STRENGTH OUTPUT DRIVER CHARACTERISTIC CURVES

TABLE 21: Full Strength Driver Characteristics

Voltage (V)	Pull–Down Current (mA)				Pull–Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.9	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	160.1	–41.2	–198.2

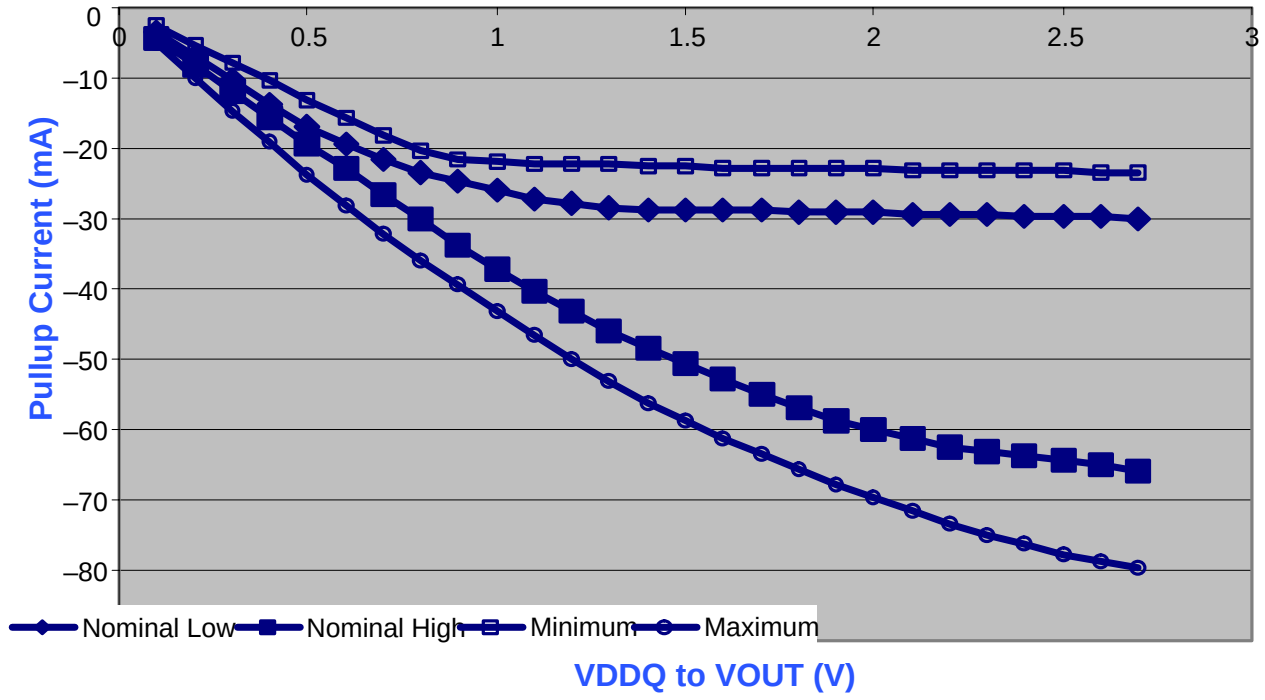


Figure 40a: Pullup Characteristics for Weak Output Driver

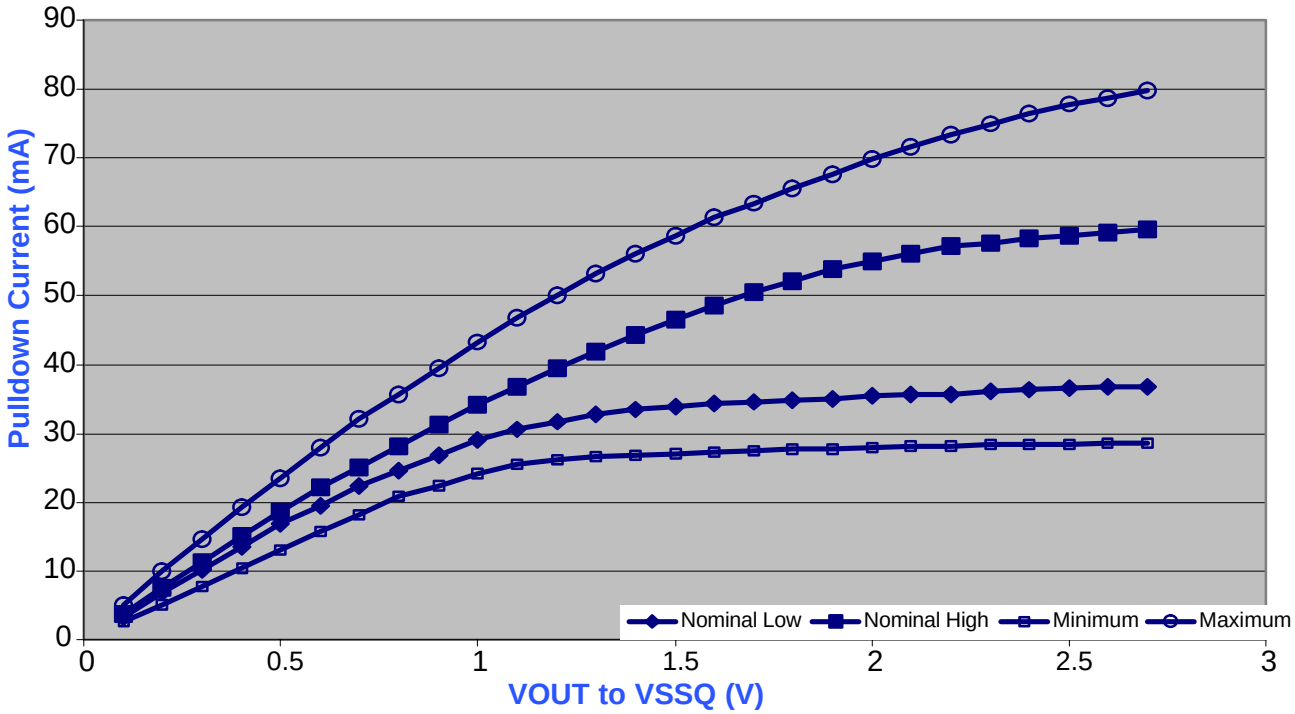


Figure 40b: Pulldown Characteristics for Weak Output Driver

FIGURE 40: WEAK OUTPUT DRIVER CHARACTERISTIC CURVES

TABLE 22: Weak Driver Characteristics

Voltage (V)	Pull–Down Current (mA)				Pull–Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5	–3.5	–4.3	–2.6	–5
0.2	6.9	7.6	5.2	9.9	–6.9	–8.2	–5.2	–9.9
0.3	10.3	11.4	7.8	14.6	–10.3	–12	–7.8	–14.6
0.4	13.6	15.1	10.4	19.2	–13.6	–15.7	–10.4	–19.2
0.5	16.9	18.7	13	23.6	–16.9	–19.3	–13	–23.6
0.6	19.6	22.1	15.7	28	–19.4	–22.9	–15.7	–28
0.7	22.3	25	18.2	32.2	–21.5	–26.5	–18.2	–32.2
0.8	24.7	28.2	20.8	35.8	–23.3	–30.1	–20.4	–35.8
0.9	26.9	31.3	22.4	39.5	–24.8	–33.6	–21.6	–39.5
1	29	34.1	24.1	43.2	–26	–37.1	–21.9	–43.2
1.1	30.6	36.9	25.4	46.7	–27.1	–40.3	–22.1	–46.7
1.2	31.8	39.5	26.2	50	–27.8	–43.1	–22.2	–50.0
1.3	32.8	42	26.6	53.1	–28.3	–45.8	–22.3	–53.1
1.4	33.5	44.4	26.8	56.1	–28.6	–48.4	–22.4	–56.1
1.5	34	46.6	27	58.7	–28.7	–50.7	–22.6	–58.7
1.6	34.3	48.6	27.2	61.4	–28.9	–52.9	–22.7	–61.4
1.7	34.5	50.5	27.4	63.5	–28.9	–55	–22.7	–63.5
1.8	34.8	52.2	27.7	65.6	–29	–56.8	–22.8	–65.6
1.9	35.1	53.9	27.8	67.7	–29.2	–58.7	–22.9	–67.7
2	35.4	55	28	69.8	–29.2	–60	–22.9	–69.8
2.1	35.6	56.1	28.1	71.6	–29.3	–61.2	–23	–71.6
2.2	35.8	57.1	28.2	73.3	–29.5	–62.4	–23	–73.3
2.3	36.1	57.7	28.3	74.9	–29.5	–63.1	–23.1	–74.9
2.4	36.3	58.2	28.3	76.4	–29.6	–63.8	–23.2	–76.4
2.5	36.5	58.7	28.4	77.7	–29.7	–64.4	–23.2	–77.7
2.6	36.7	59.2	28.5	78.8	–29.8	–65.1	–23.3	–78.8
2.7	36.8	59.6	28.6	79.7	–29.9	–65.8	–23.3	–79.7

DDR SDRAM Output Driver V–I Characteristics

DDR SDRAM output driver characteristics are defined for full and half strength operation as selected by the EMRS bit A1. Figures 39 and 40 show the driver characteristics graphically, and tables 21 and 22 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

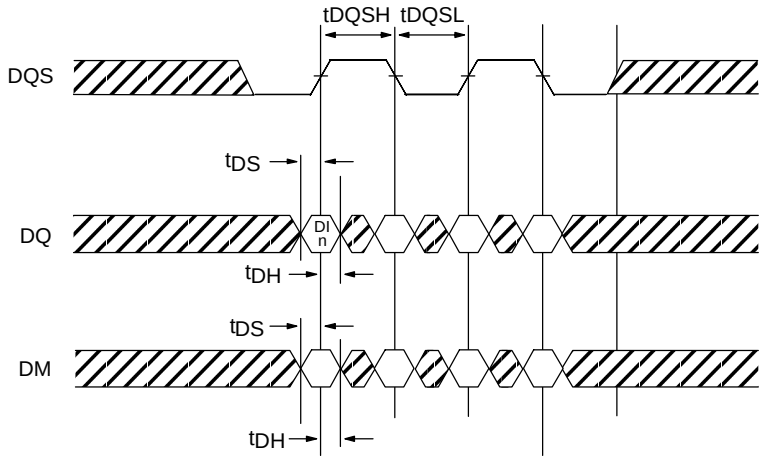
Typical	25 ^{O}C (T ambient),	VDDQ = 2.5 V,	typical process
Minimum	70 ^{O}C (T ambient),	VDDQ = 2.3 V,	slow–slow process
Maximum	0 ^{O}C (T ambient),	VDDQ = 2.7 V,	fast–fast process

Output Driver Characteristic Curves Notes:

1) The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of Figures 39 and 40.

2) It is recommended that the ”typical” IBIS V–I curve lie within the inner bounding lines of the V–I curves of Figures 39 and 40.

3) The full variation in the ratio of the “typical” IBIS pullup to “typical” IBIS pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n

Figure 41 – DATA INPUT (WRITE) TIMING

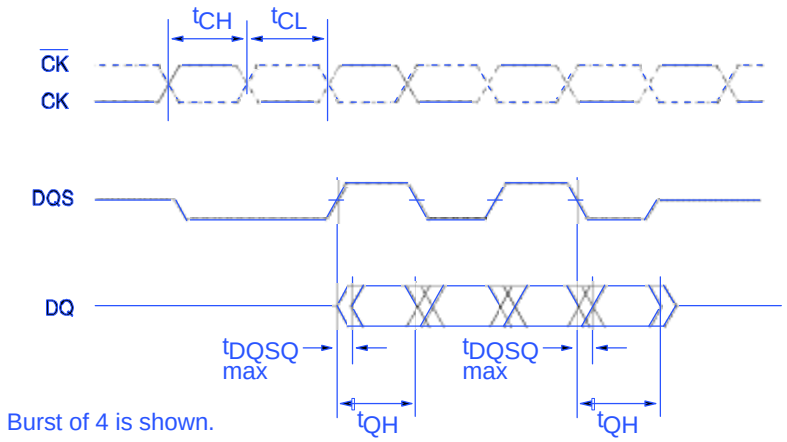
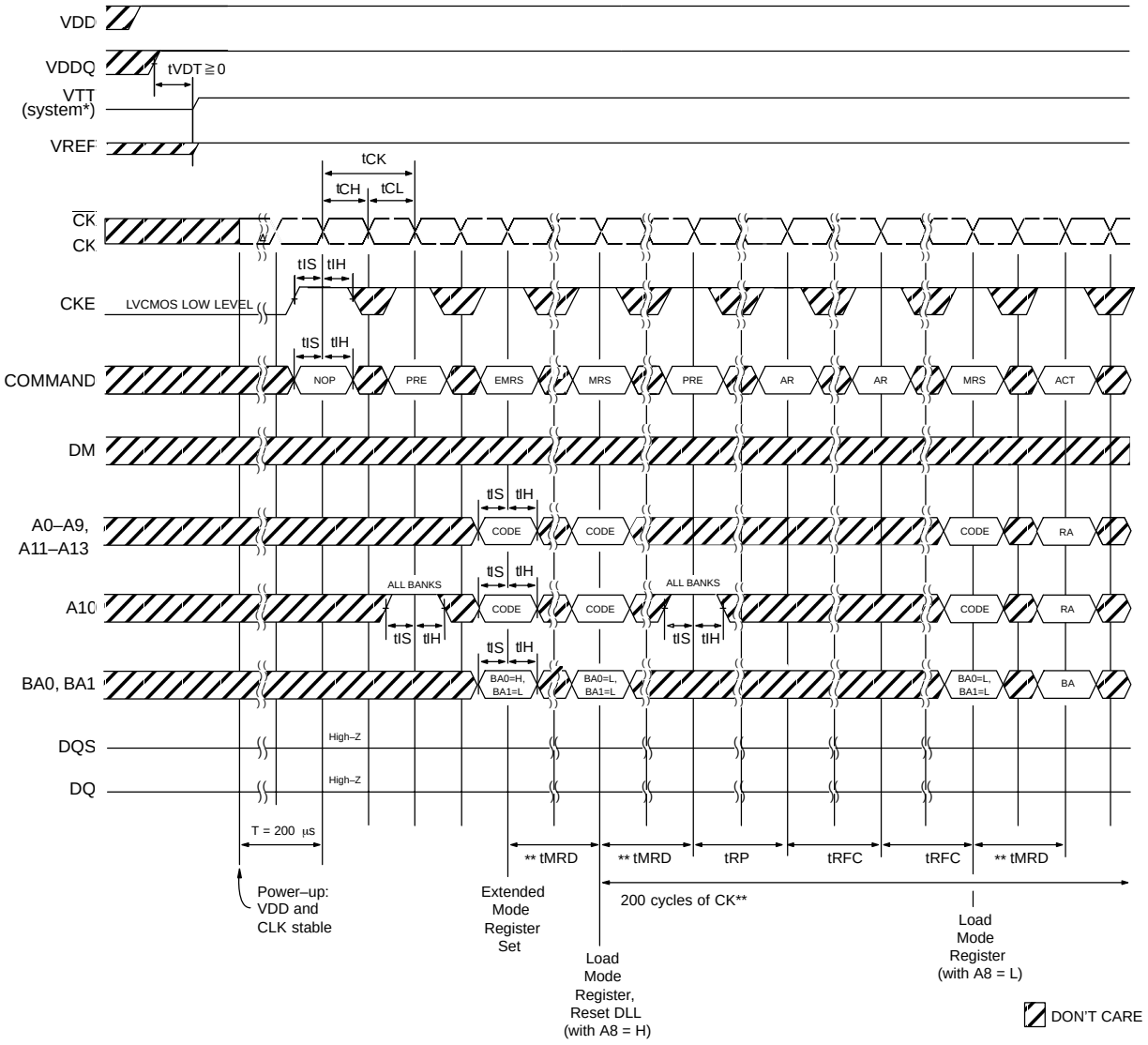


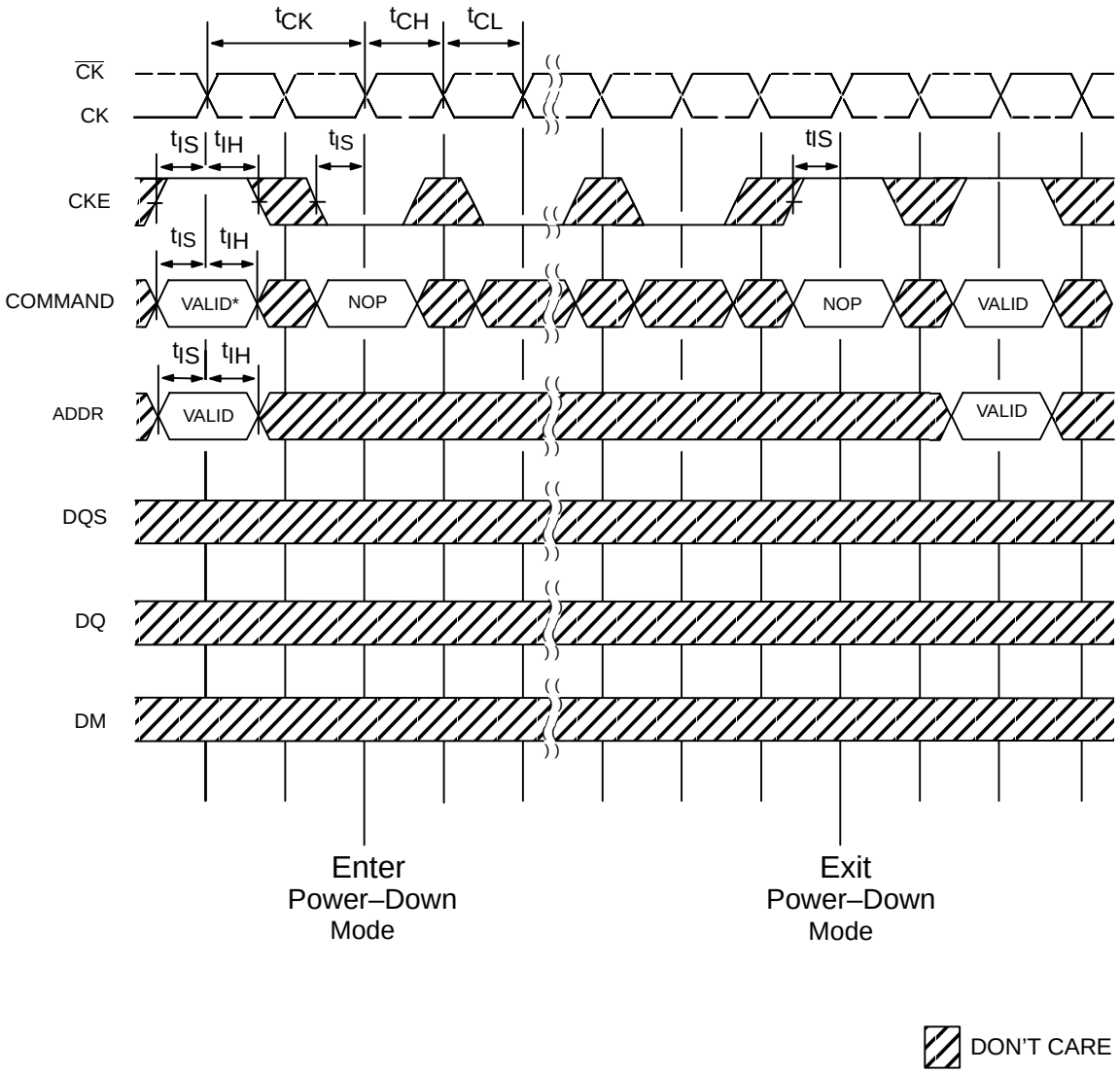
Figure 42 – DATA OUTPUT (READ) TIMING



* = VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch–up.

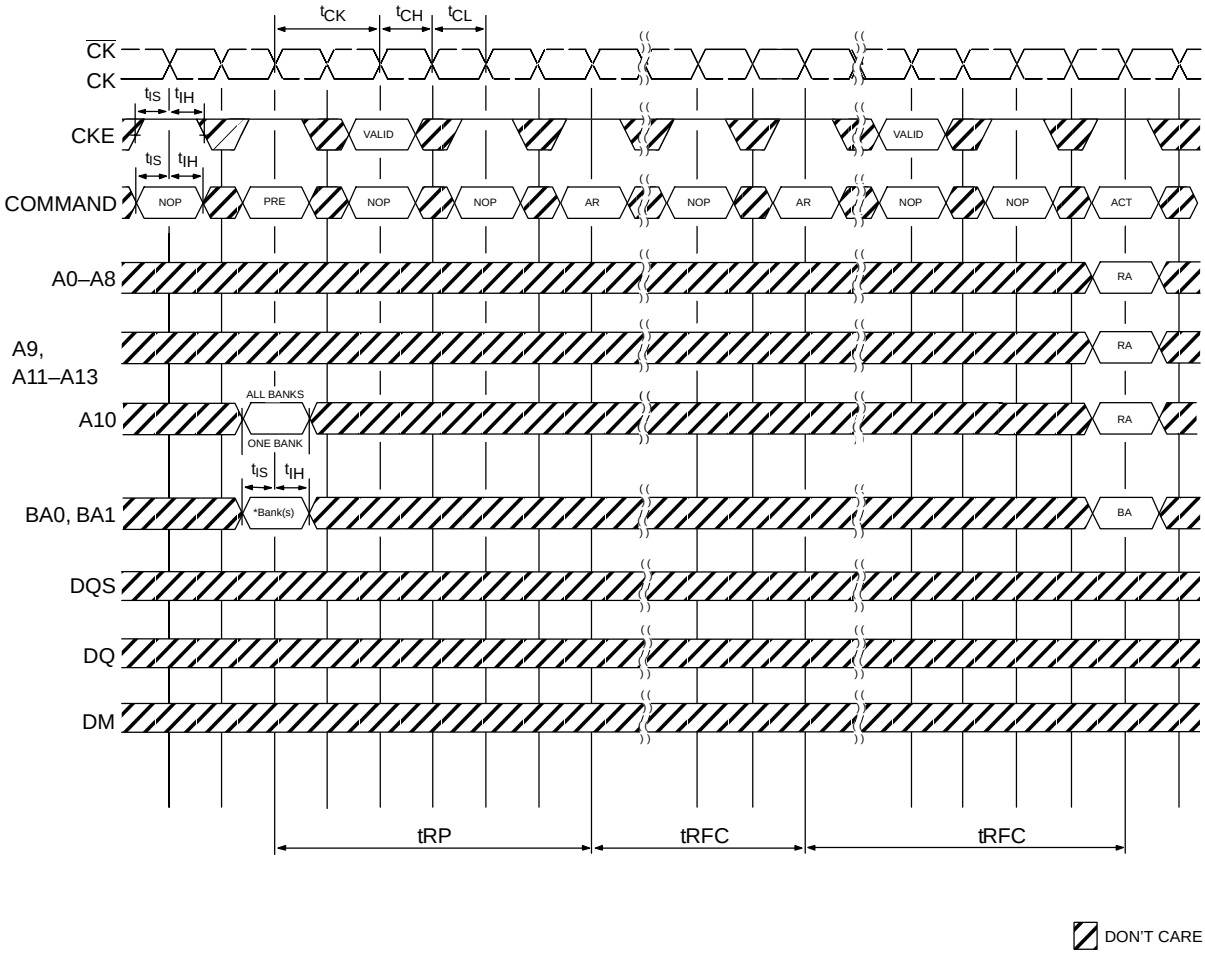
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied
The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

Figure 43 – INITIALIZE AND MODE REGISTER SETS



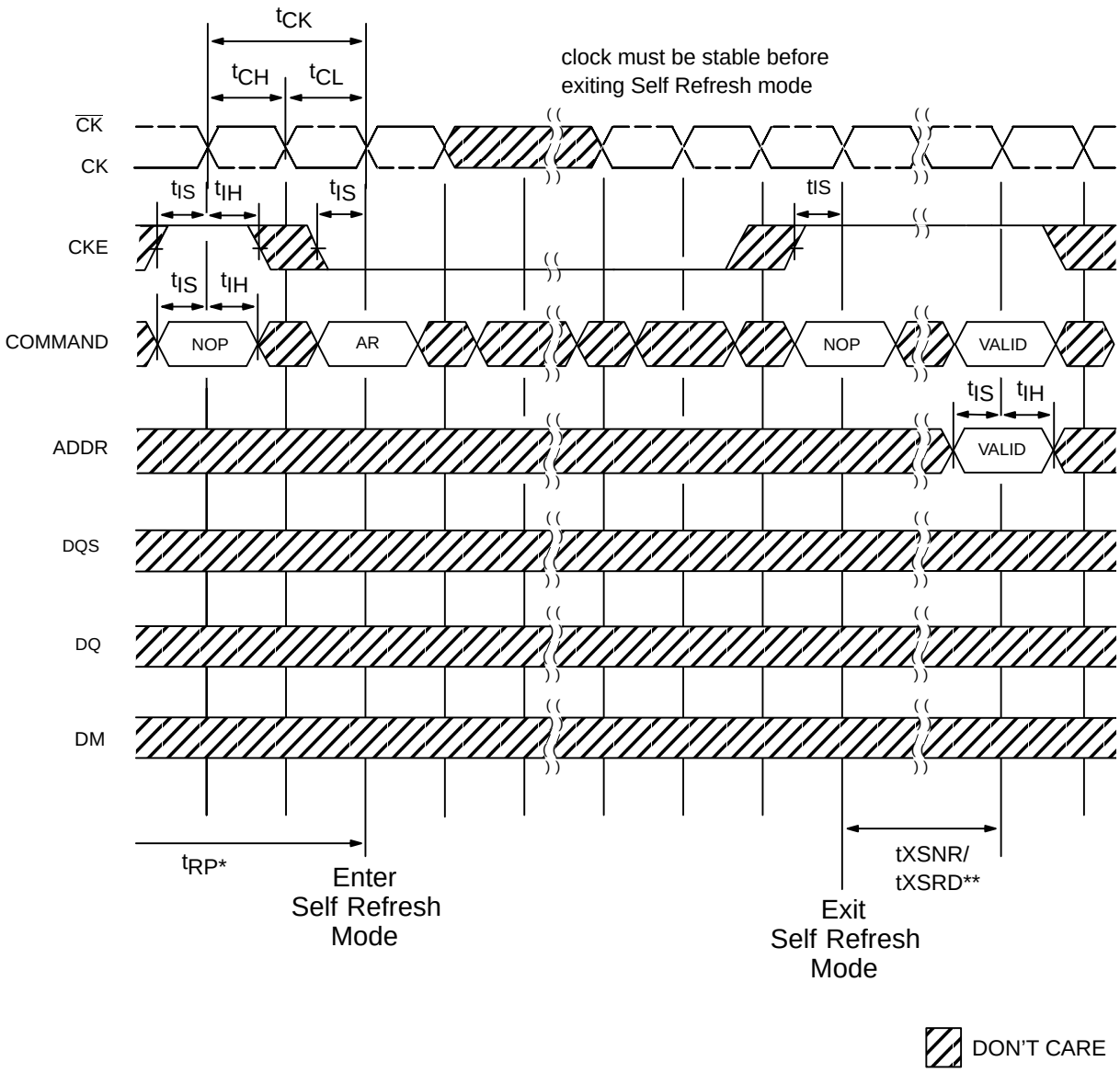
No column accesses are allowed to be in progress at the time Power–Down is entered
* = If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power–Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power–Down mode shown is Active Power Down.

Figure 44 – POWER–DOWN MODE



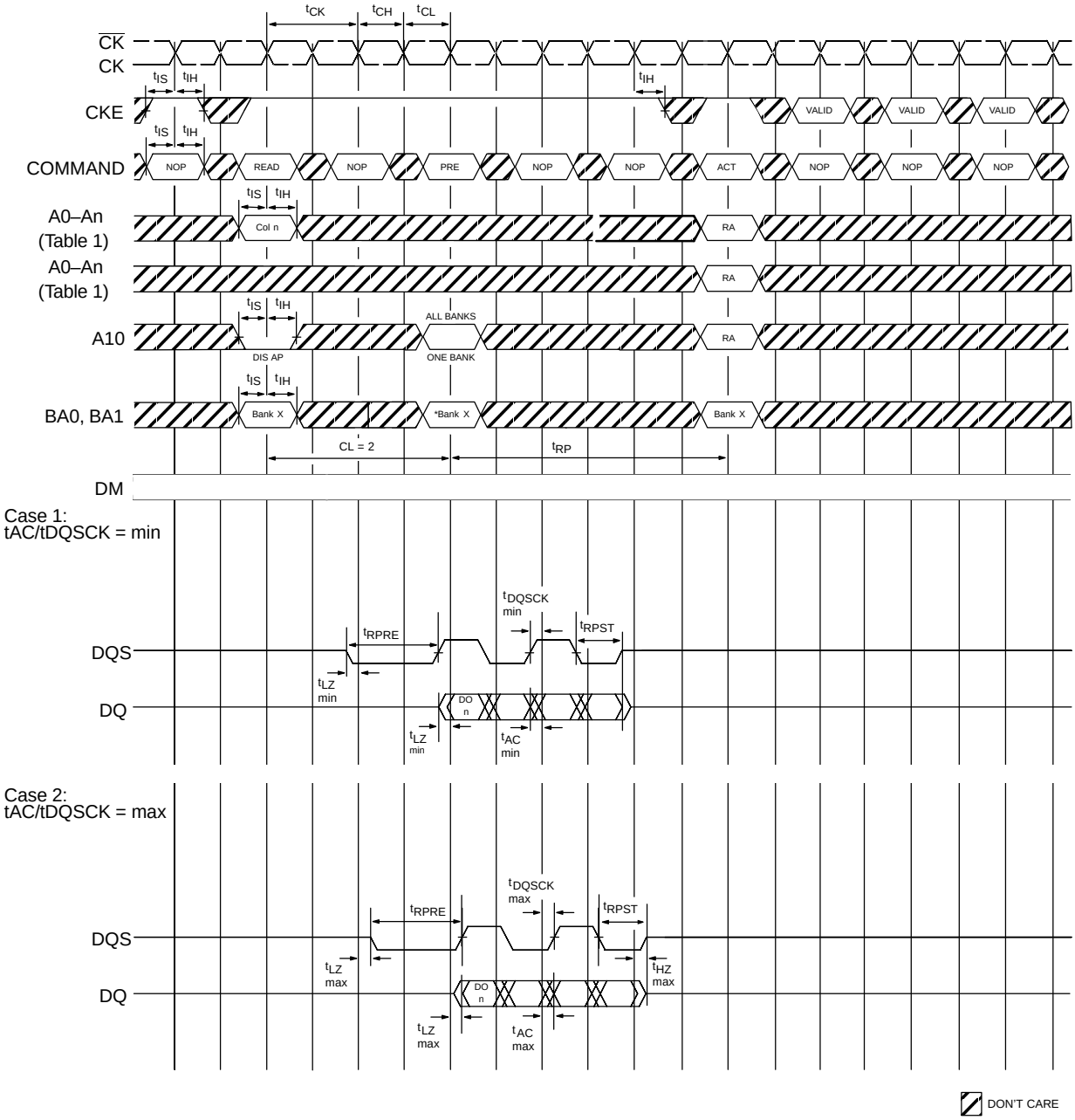
* = ”Don’t Care”, if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC.
DM, DQ and DQS signals are all ”Don’t Care”/High–Z for operations shown

Figure 45 – AUTO REFRESH MODE



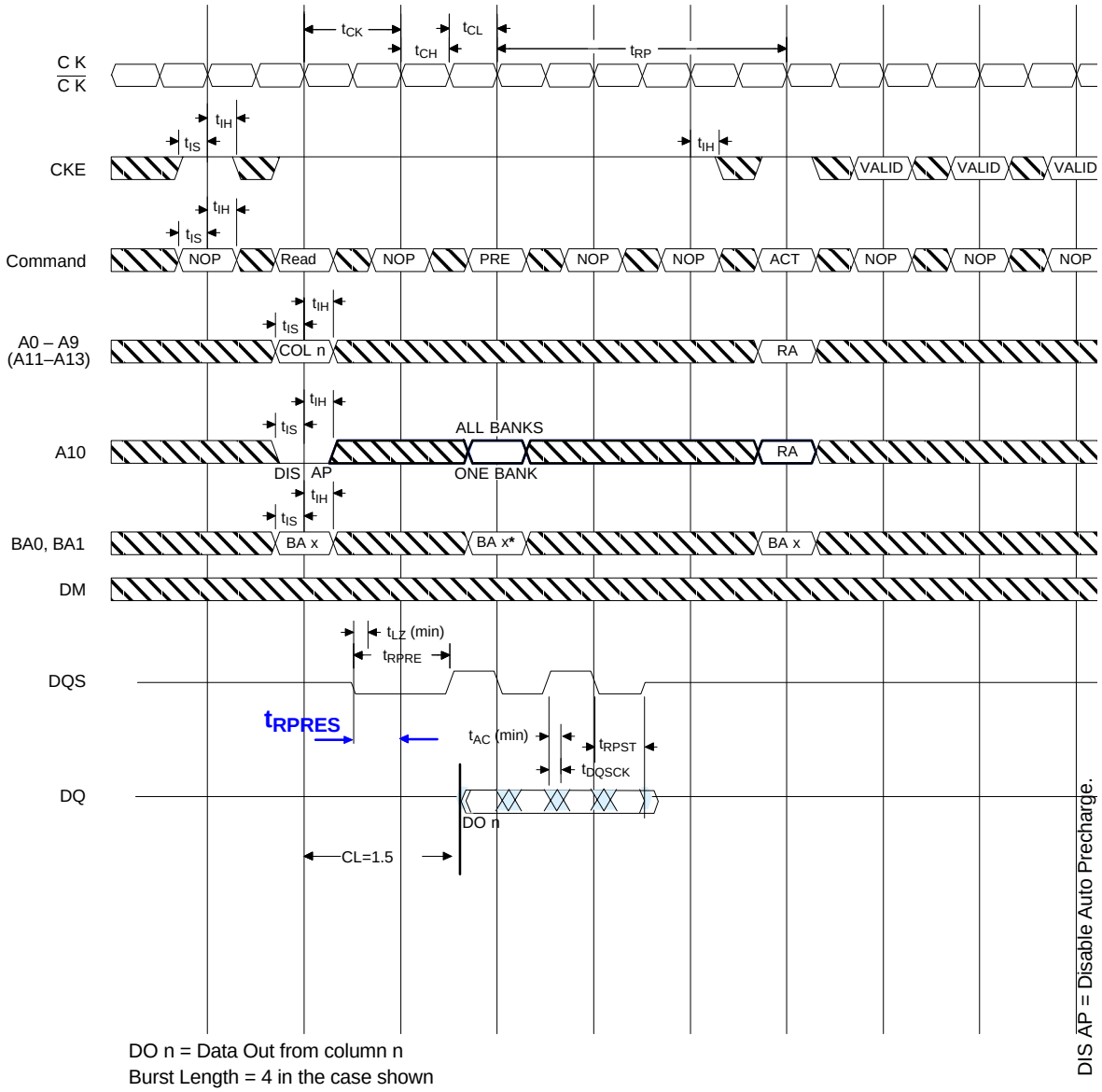
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non–READ command can be applied, and tXSRD is required before a READ command can be applied.

Figure 46 – SELF REFRESH MODE



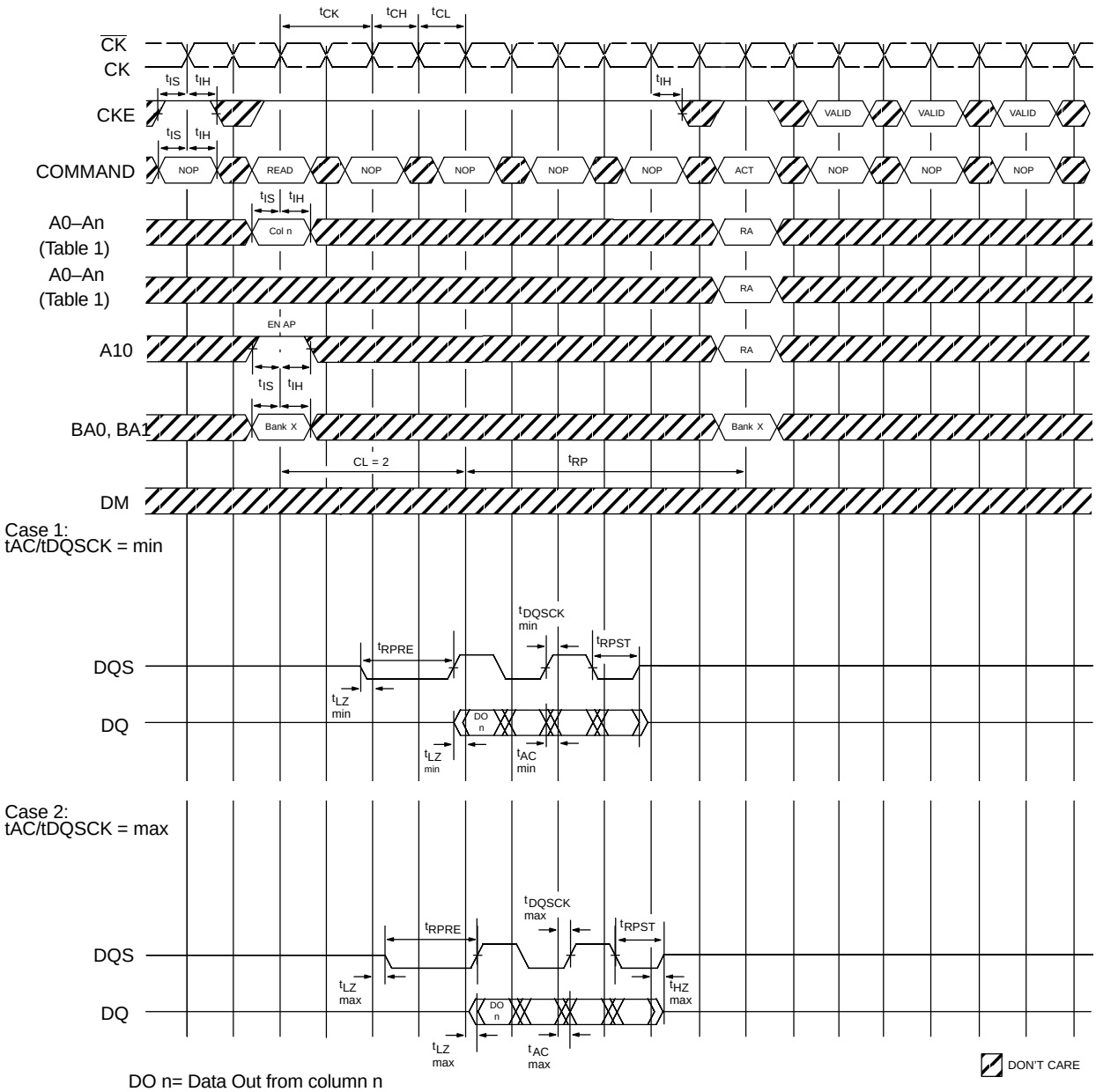
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

Figure 47 – READ – WITHOUT AUTO PRECHARGE



DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

Figure 48 – READ WITHOUT AUTOPRECHARGE (CL=1.5, BL=4)



DO n= Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

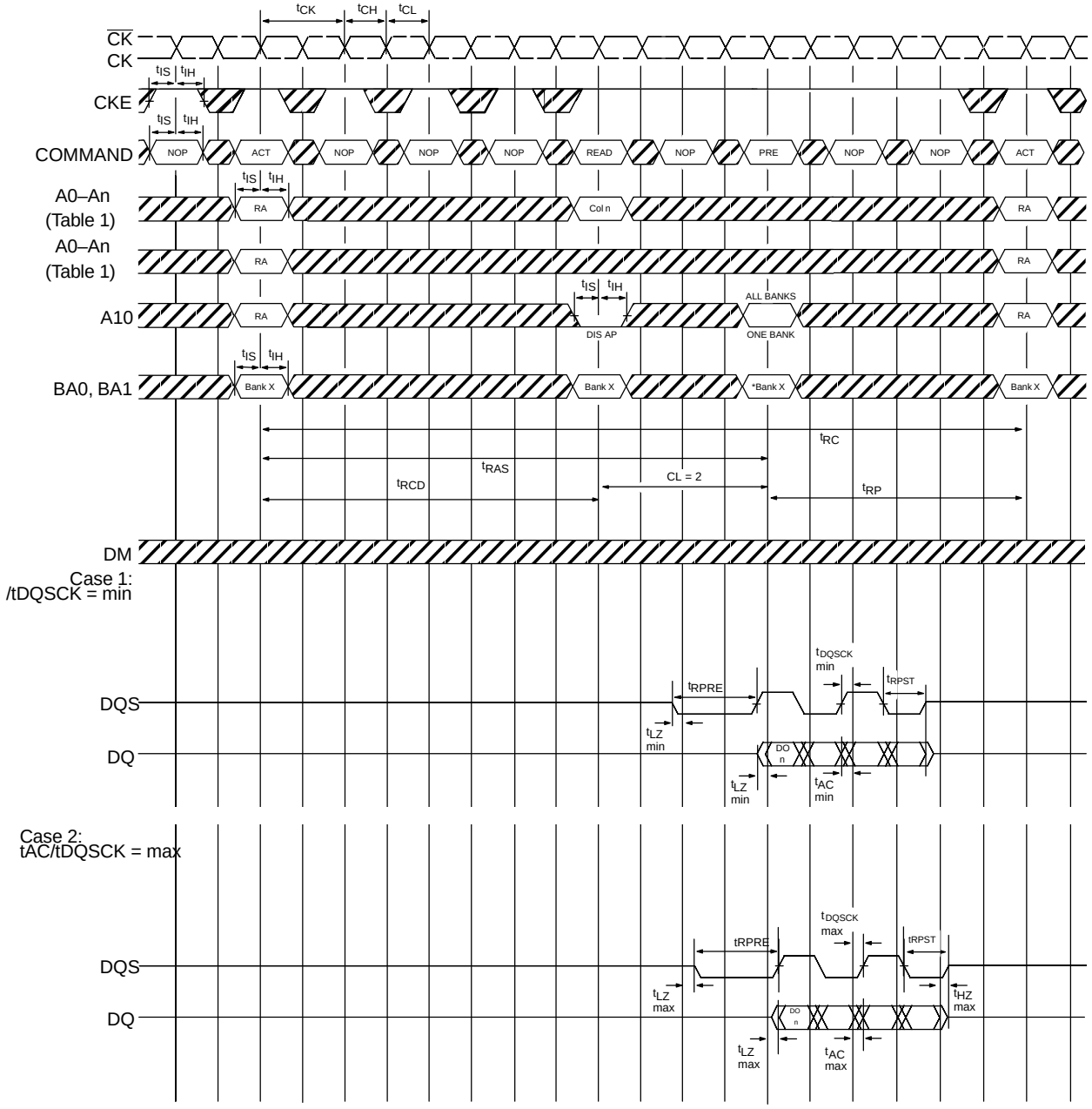
EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

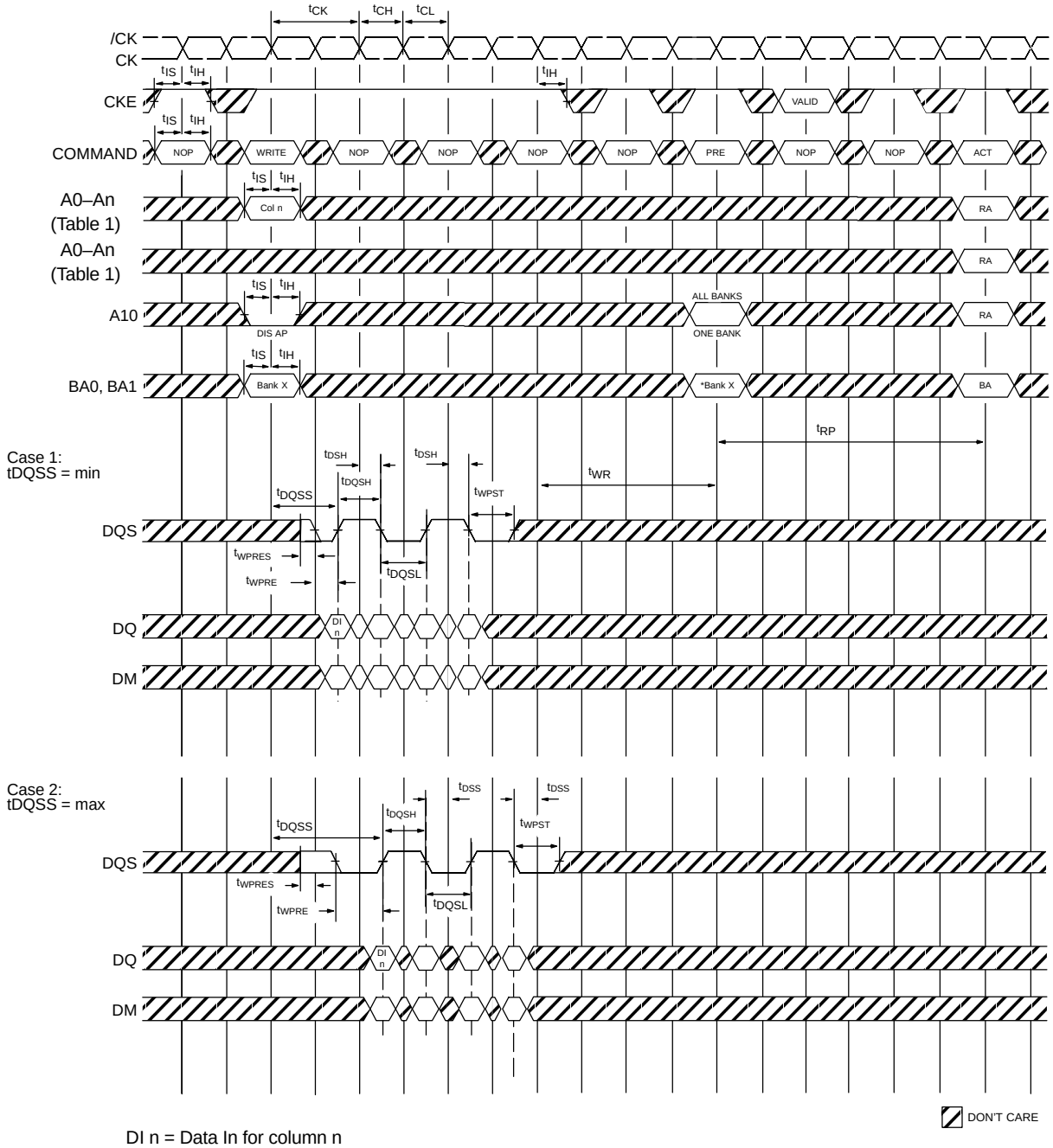
The READ command may not be issued until tRAP has been satisfied. If Fast Autoprecharge is supported, tRAP = tRCD, else the READ may not be issued prior to tRASmin – (BL*tCK/2).

Figure 49 – READ – WITH AUTO PRECHARGE



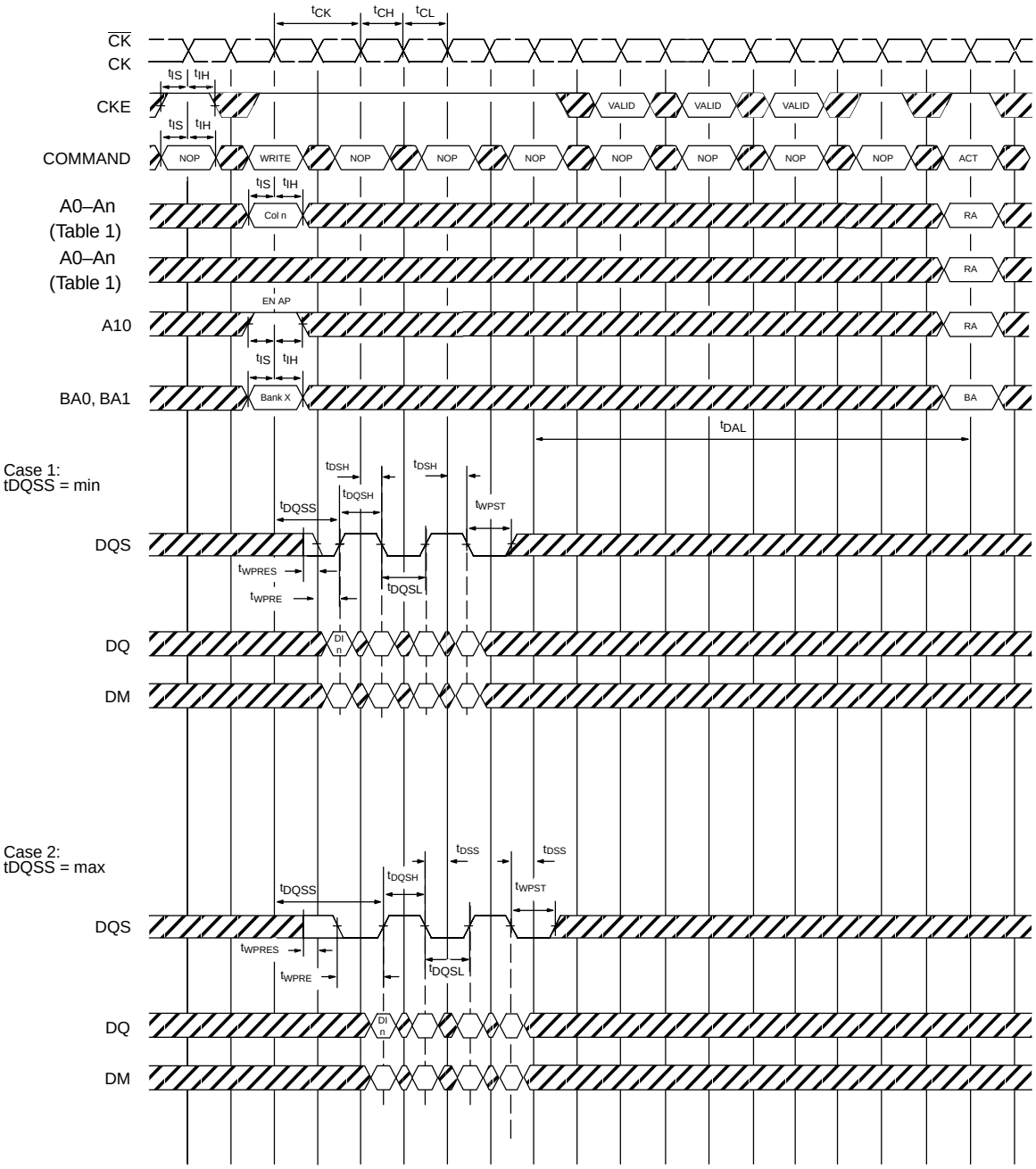
DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Figure 50 – BANK READ ACCESS



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

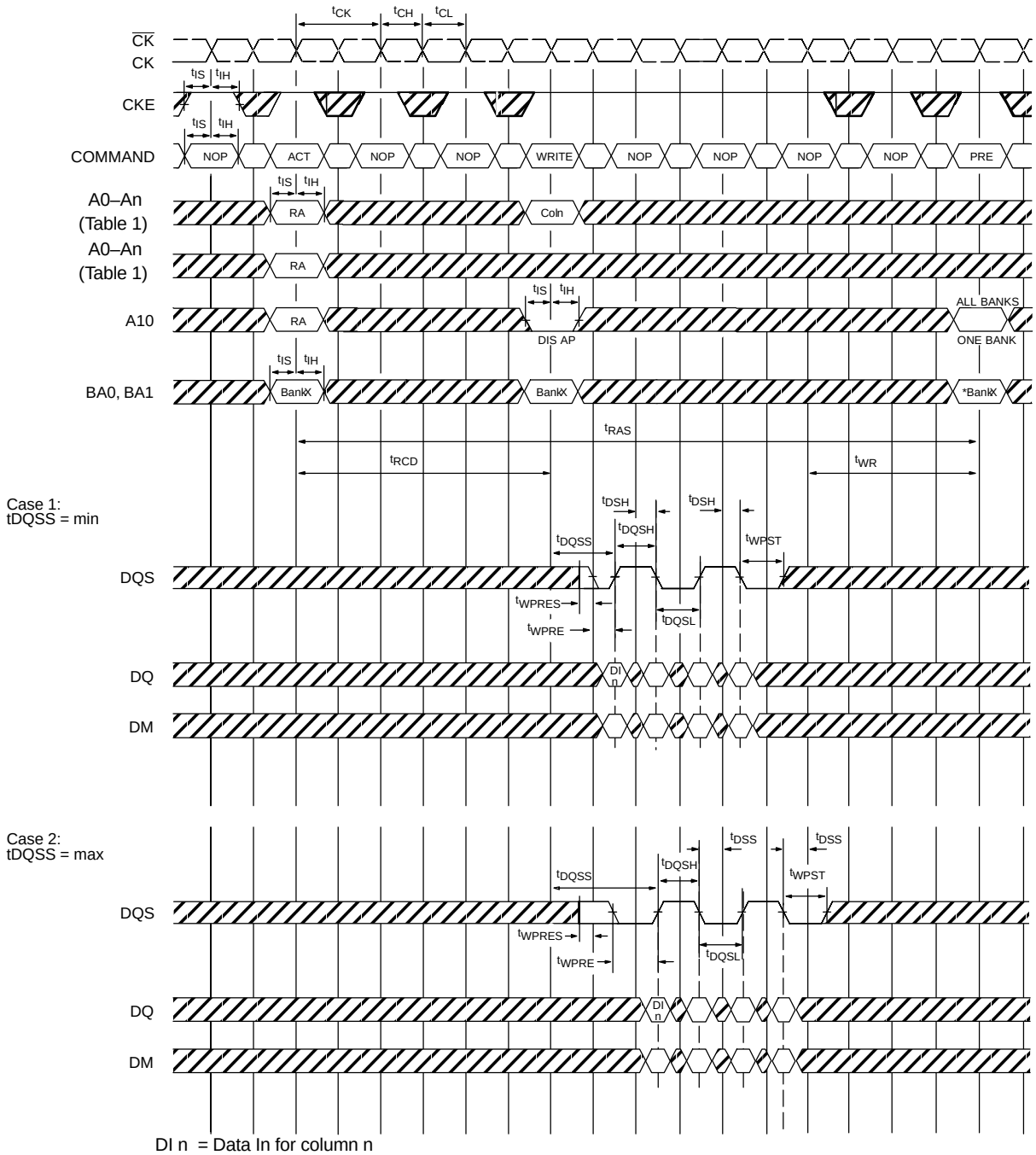
Figure 51 – WRITE – WITHOUT AUTO PRECHARGE



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
EN AP = Enable Autoprecharge
ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.

DON'T CARE

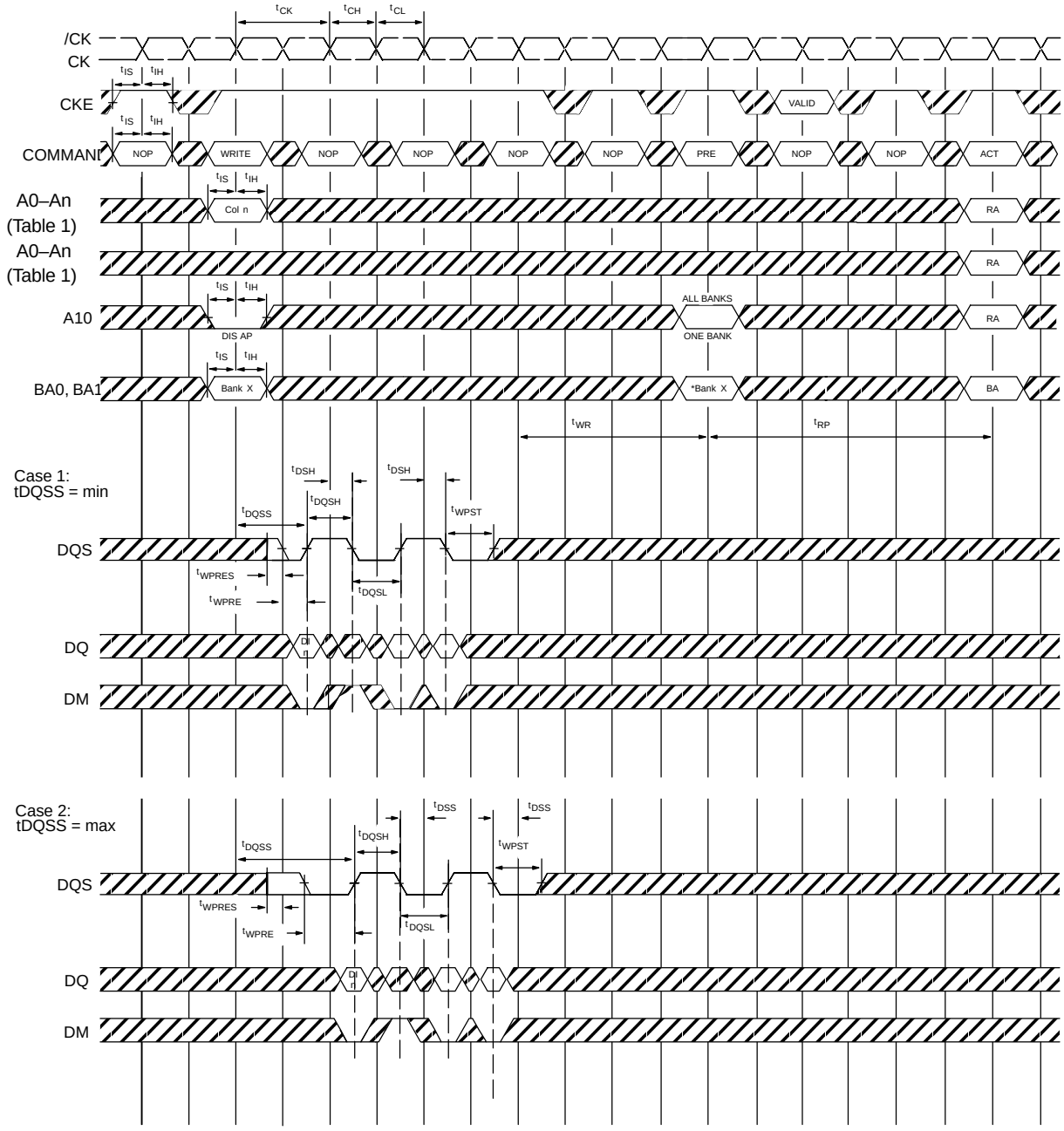
Figure 52 – WRITE – WITH AUTO PRECHARGE



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.
Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

DON'T CARE

Figure 53 – BANK WRITE ACCESS



DI n= Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n (the second element of the four is masked)
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.

Figure 54 – WRITE – DM OPERATION


JEDEC

Exhibit G

JEDEC STANDARD

DDR2 SDRAM SPECIFICATION

JESD79-2A

(Revision of JESD79-2)

January 2004

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

XILINX EXHIBIT 1010
Page 609

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DDR2 SDRAM SPECIFICATION

Contents

Page

1 Package Pinout & Addressing 1
1.1 DDR2 SDRAM Package Ballout 1
1.2 Input/Output Functional Description 6
1.3 DDR2 SDRAM Addressing 7

2 Functional Description 9
2.1 Simplified State Diagram 9
2.2 Basic Functionality 10
2.2.1 Power-Up and Initialization 10
2.2.2 Programming the Mode and Extended Mode Registers 11
2.2.3 Bank Activate Command 23
2.2.4 Read and Write Access Modes 24
2.2.5 Precharge Operation 33
2.2.6 Auto Precharge Operation 37
2.2.7 Refresh Command 41
2.2.8 Self Refresh Operation 42
2.2.9 Power-Down 43
2.2.10 Asynchronous CKE Low Event 47
2.2.11 Input Clock Frequency Change during Precharge Power Down 48
2.2.12 No Operation Command 48
2.2.13 Deselect Command 48

3 Truth Tables 49

4 Absolute Maximum DC Ratings 51

5 AC & DC Operating Conditions 51

Figures

1 DDR2 SDRAM x4 Ballout Using MO-207 1
2 DDR2 SDRAM x8 Ballout Using MO-207 2
3 DDR2 SDRAM x16 Ballout Using MO-207 3
4 Stacked/Dual-Die DDR2 SDRAM x4 Ballout Using MO-TBD. 4
5 Stacked/Dual-Die DDR2 SDRAM x8 Ballout Using MO-TBD 5
6 DDR2 SDRAM Simplified State Diagram 9
7 Initialization Sequence after Power Up 11
8 DDR2 SDRAM Mode Register Set (MRS) 12
9 EMRS(1) Programming 14
10 EMRS(2) Programming: Reserved 15
11 EMRS(3) Programming: Reserved 15
12 OCD Impedance Adjustment 16
13 OCD Adjust Mode 17
14 OCD Drive Mode 18
15 Functional Representation of ODT 19
16 ODT Timing for Active/Standby Mode 19
17 ODT Timing for Powerdown Mode 20
18 ODT Timing Mode Switch at Entering Power Down Mode 21
19 ODT Timing Mode Switch at Exiting Power Down Mode 22
20 Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2 23
21 Example 1: Read Followed by a Write to the Same Bank 24

XILINX EXHIBIT 1010
Page 613

DDR2 SDRAM SPECIFICATION

Contents (cont'd)

		Page
22	Example 2: Read Followed by a Write to the Same Bank	25
23	Data Output (Read) Timing	26
24	Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)	27
25	Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)	27
26	Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4	28
27	Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4	28
28	Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)	29
29	Data Input (Write) Timing	30
30	Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL = 4	30
31	Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4	30
32	Burst Write Followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4	31
33	Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4	31
34	Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)	32
35	Write Data Mask	33
36	Example 1: Burst Read Operation Followed by Precharge: RL = 1, CL = 3, BL = 4, tRTP <= 2 clocks	34
37	Example 2: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, tRTP <= 2 clocks	35
38	Example 3: Burst Read Operation Followed by Precharge: RL = 5, AL = 2, CL = 3, BL = 4, tRTP <= 2 clocks	35
39	Example 4: Burst Read Operation Followed by Precharge: RL = 6, AL = 2, CL = 4, BL = 4, tRTP <= 2 clocks	36
40	Example 5: Burst Read Operation Followed by Precharge: RL = 4, AL = 0, CL = 4, BL = 8, tRTP > 2 clocks	36
41	Example 1: Burst Write followed by Precharge: WL = (RL-1) =3	37
42	Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4	37
43	Example 1: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 8, tRTP <= 2 clocks	38
44	Example 2: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 4, tRTP > 2 clocks	39
45	Example 3: Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRC Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, tRTP <= 2 clocks)	39
46	Example 4: Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, tRTP <= 2 clocks)	40
47	Burst Write with Auto-Precharge (tRC Limit): WL = 2, tWR =2, BL = 4, tRP=3	40
48	Burst Write with Auto-Precharge (tWR + tRP): WL = 4, tWR =2, BL = 4, tRP=3	41
49	Refresh Command	41
50	Self Refresh Operation	42
51	Basic Power Down Entry and Exit Timing Diagram	43
52	Read to Power Down Entry	44
53	Read with Autoprecharge to Power Down Entry	45
54	Write to Power Down Entry	45
55	Write with Autoprecharge to Power Down Entry	46
56	Refresh Command to Power Down Entry	46
57	Active Command to Power Down Entry	46
58	Precharge/Precharge all Command to Power Down Entry	47

XILINX EXHIBIT 1010
Page 614

DDR2 SDRAM SPECIFICATION

Contents (cont'd)

		Page
59	MRS/EMRS Command to Power Down Entry	47
60	Asynchronous CKE Low Event	47
61	Clock Frequency Change in Precharge Power Down Mode	48
62	AC Input Test Signal Waveform	53
63	Differential signal levels	53
64	AC Overshoot and Undershoot Definition for Address and Control Pins	54
65	AC Overshoot and Undershoot Definition for Clock, Data, Strobe, and Mask Pins	55
66	DDR2 Default Pulldown Characteristics for Full Strength Driver	58
67	DDR2 Default Pullup Characteristics for Full Strength Output Driver	59
68	AC Timing Reference Load	69
69	Slew Rate Test Load	69
70	Data Input (Write) Timing	70
71	Data Output (Read) Timing	70

Tables

1	256Mb Addressing	7
2	512Mb Addressing	7
3	1Gb Addressing	7
4	2Gb Addressing	7
5	4 Gb Addressing	8
6	OCD Drive Mode Program	15
7	OCD Adjust Mode Program	17
8	Burst Length and Sequence	25
9	Bank Selection for Precharge by Address Bits	34
10	Command Truth Table.	49
11	Clock Enable (CKE) Truth Table for Synchronous Transitions	50
12	DM Truth Table	50
13	Recommended DC Operating Conditions (SSTL_1.8)	51
14	ODT DC Electrical Characteristics	52
15	Input DC Logic Level	52
16	Input AC Logic Level	52
17	AC Input Test Conditions	52
18	Differential Input DC Logic Level	53
19	Differential Input AC Logic Level	53
20	Differential AC output parameters	54
21	AC Overshoot/Undershoot Specification for Address and Control Pins A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT	54
22	AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins DQ, DQS, DM, CK, CK	54
23	Characteristics for Input Only Pins with Clamps	55
24	Output AC Test Conditions	56
25	Output DC Current Drive	56
26	OCD Default Characteristics	56
27	Full Strength Default Pulldown Driver Characteristics	57
28	Full Strength Default Pullup Driver Characteristics	58
29	Full Strength Calibrated Pulldown Driver Characteristics	60

XILINX EXHIBIT 1010
Page 615

DDR2 SDRAM SPECIFICATION

Contents (cont'd)

		Page
30	Full Strength Calibrated Pullup Driver Characteristics	60
31	IDD Specification Parameters and Test Conditions (IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5)	60
32	IDD Testing Parameters	62
33	Input/Output capacitance	63
34	Refresh Parameters by Device Density	63
35	DDR2 SDRAM Standard Speed Bins and tRCD, tRP and tRC for Corresponding Bin	64
36	Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)	64
37	Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)	67
Annex A (informative)	**Differences Between JESD79-2 and JESD79-2A**	**72**

DDR2 SDRAM SPECIFICATION

1 Package Pinout & Addressing

1.1 DDR2 SDRAM Package Ballout

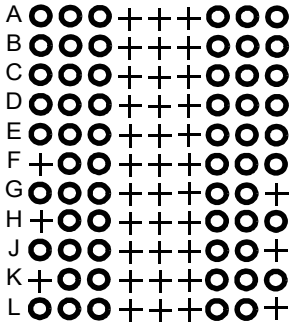
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NC	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	NC	VSSQ	DM				DQS	VSSQ	NC	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

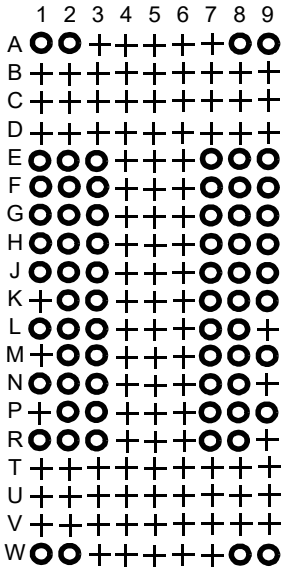
Variation DJ-z without support balls

Variation DM-z with support balls

Variation DJ-z (x4 x8)



Variation DM-z (x4/x8) with support balls



O Populated ball
\+ Ball not populated

Figure 1 — DDR2 SDRAM x4 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

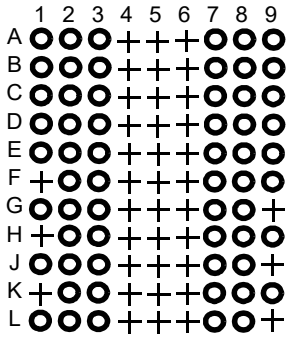
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
A	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
B	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
C	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
D	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
E	VDDL	VREF	VSS				VSSDL	CK	VDD	J
F		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	K
G	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		L
H		A10/AP	A1				A2	A0	VDD	M
J	VSS	A3	A5				A6	A4		N
K		A7	A9				A11	A8	VSS	P
L	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

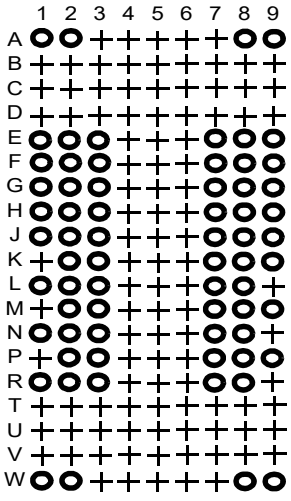
Variation DJ-z without support balls

Variation DM-z with support balls

Variation DJ-z (x4 x8)



Variation DM-z (x4/x8)
with support balls



Populated ball

Ball not populated

Figure 2 — DDR2 SDRAM x8 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

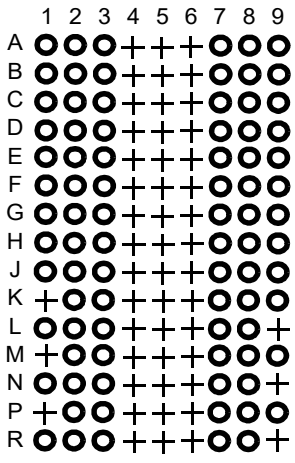
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
A	VDD	NC	VSS				VSSQ	$\overline{\text{UDQS}}$	VDDQ	D
B	DQ14	VSSQ	UDM				UDQS	VSSQ	DQ15	E
C	VDDQ	DQ9	VDDQ				VDDQ	DQ8	VDDQ	F
D	DQ12	VSSQ	DQ11				DQ10	VSSQ	DQ13	G
E	VDD	NC	VSS				VSSQ	$\overline{\text{LDQS}}$	VDDQ	H
F	DQ6	VSSQ	LDM				LDQS	VSSQ	DQ7	J
G	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	K
H	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	L
J	VDDL	VREF	VSS				VSSDL	CK	VDD	M
K		CKE	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT	N
L	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS}}$		P
M		A10/AP	A1				A2	A0	VDD	R
N	VSS	A3	A5				A6	A4		T
P		A7	A9				A11	A8	VSS	U
R	VDD	A12	NC, A14				NC, A15	NC, A13		V
										W
										X
	NC	NC						NC	NC	AA

Variation DK-z without support balls

Variation DL-z with support balls

Variation DK-z (x16)



Populated ball

Ball not populated

Variation DL-z (x16) with support balls

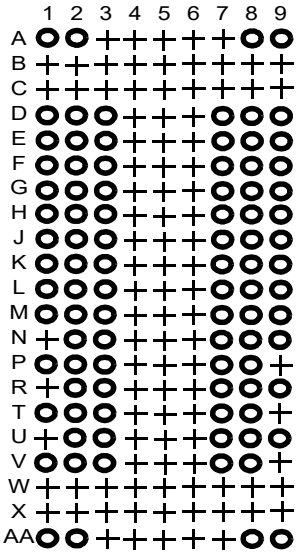


Figure 3 — DDR2 SDRAM x16 Ballout Using MO-207

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
Variation tbd. without support balls	VDD	NC	VSS				VSSQ	$\overline{DQS}$	VDDQ	E
A	NC	VSSQ	DM				DQS	VSSQ	NC	F
B	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
C	NC	VSSQ	DQ3				DQ2	VSSQ	NC	H
D	VDDL	VREF	VSS				VSSDL	CK	VDD	J
E		CKE0	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT0	K
F	NC, BA2	BA0	BA1				$\overline{CAS}$	$\overline{CS0}$	$\overline{CS1}$	L
G	CKE1	A10/AP	A1				A2	A0	VDD	M
H	VSS	A3	A5				A6	A4	ODT1	N
J		A7	A9				A11	A8	VSS	P
K	VDD	A12	NC, A14				NC, A15	NC, A13		R
L										T
										U
										V
	NC	NC						NC	NC	W

Variation tbd. with support balls

NOTE This stacked ballout does not represent the nonstacked ballout; it is intended only for use in a stacked package.

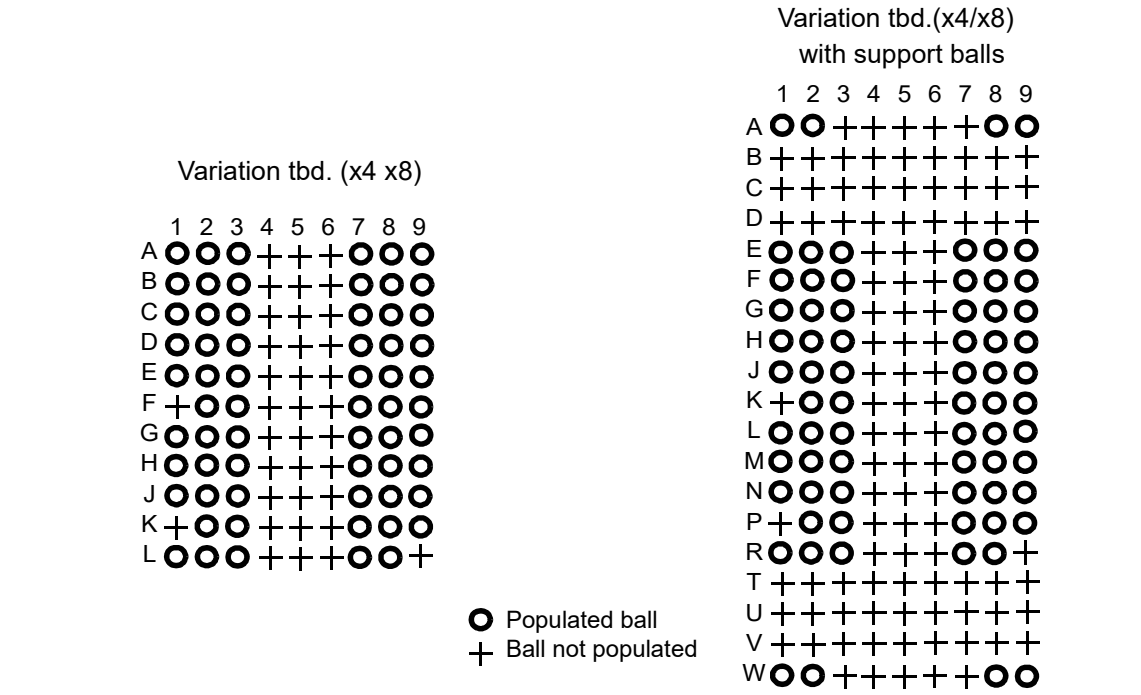


Figure 4 — Stacked/Dual-Die DDR2 SDRAM x4 Ballout Using MO-TBD.

1 Package Pinout & Addressing (cont'd)

1.1 DDR2 SDRAM Package Ballout (cont'd)

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	
	NC	NC						NC	NC	A
										B
										C
										D
Variation tbd. without support balls	VDD	NU/$\overline{\text{RDQS}}$	VSS				VSSQ	$\overline{\text{DQS}}$	VDDQ	E
	DQ6	VSSQ	DM/RDQS				DQS	VSSQ	DQ7	F
	VDDQ	DQ1	VDDQ				VDDQ	DQ0	VDDQ	G
	DQ4	VSSQ	DQ3				DQ2	VSSQ	DQ5	H
	VDDL	VREF	VSS				VSSDL	CK	VDD	J
		CKE0	$\overline{\text{WE}}$				$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0	K
	NC, BA2	BA0	BA1				$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	L
	CKE1	A10/AP	A1				A2	A0	VDD	M
	VSS	A3	A5				A6	A4	ODT1	N
		A7	A9				A11	A8	VSS	P
	VDD	A12	NC, A14				NC, A15	NC, A13		R
										T
										U
										V
	NC	NC						NC	NC	W

Variation tbd. with support balls

NOTE This stacked ballout is intended for use only in a stacked package, it does not represent the nonstacked package.

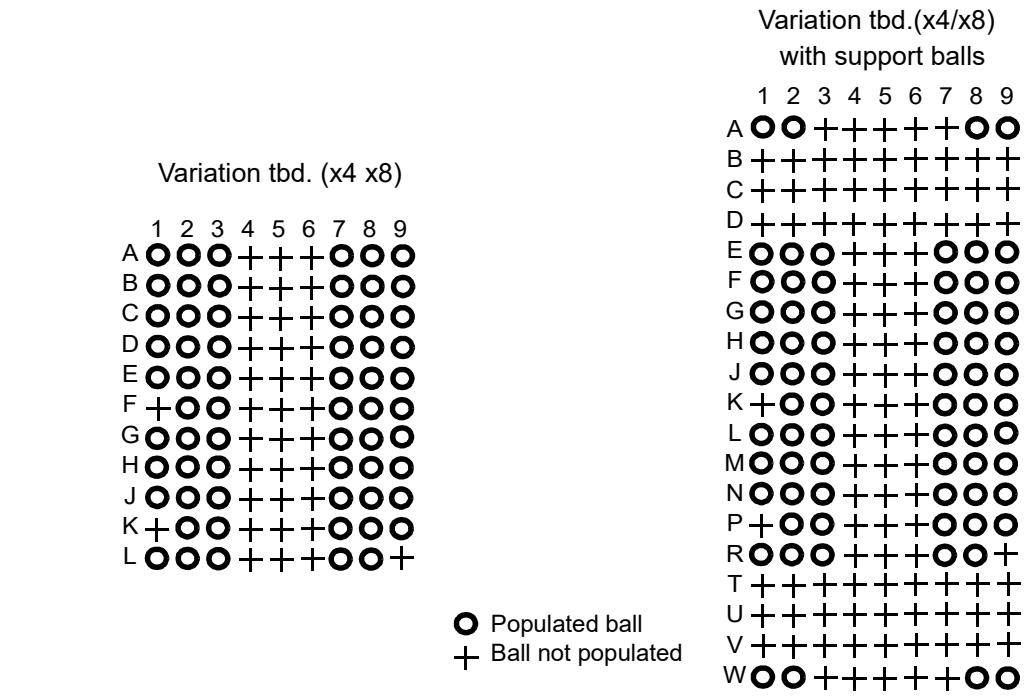


Figure 5 — Stacked/Dual-Die DDR2 SDRAM x8 Ballout Using MO-TBD

1 Package Pinout & Addressing (cont'd)

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1)

x4 DQS/$\overline{DQS}$
x8 DQS/$\overline{DQS}$ if EMRS(1)[A11] = 0
x8 DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, if EMRS(1)[A11] = 1
x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$

"single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1)

x4 DQS
x8 DQS if EMRS(1)[A11] = 0
x8 DQS, RDQS, if EMRS(1)[A11] = 1
x16 LDQS and UDQS

1 Package Pinout & Addressing (cont'd)

1.3 DDR2 SDRAM Addressing

Table 1 — 256Mb Addressing

Configuration	64Mb x4	32Mb x 8	16Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A8
Page size*1	1 KB	1 KB	1 KB

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

1 Package Pinout & Addressing (cont'd)

1.3 DDR2 SDRAM Addressing (cont'd)

Table 5 — 4 Gb Addressing

Configuration	1 Gb x4	512Mb x 8	256Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	tbd	tbd	tbd
Column Address	tbd	tbd	tbd
Page size *1	tbd	tbd	tbd

NOTE Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size = $2^{COLBITS} * ORG \div 8$

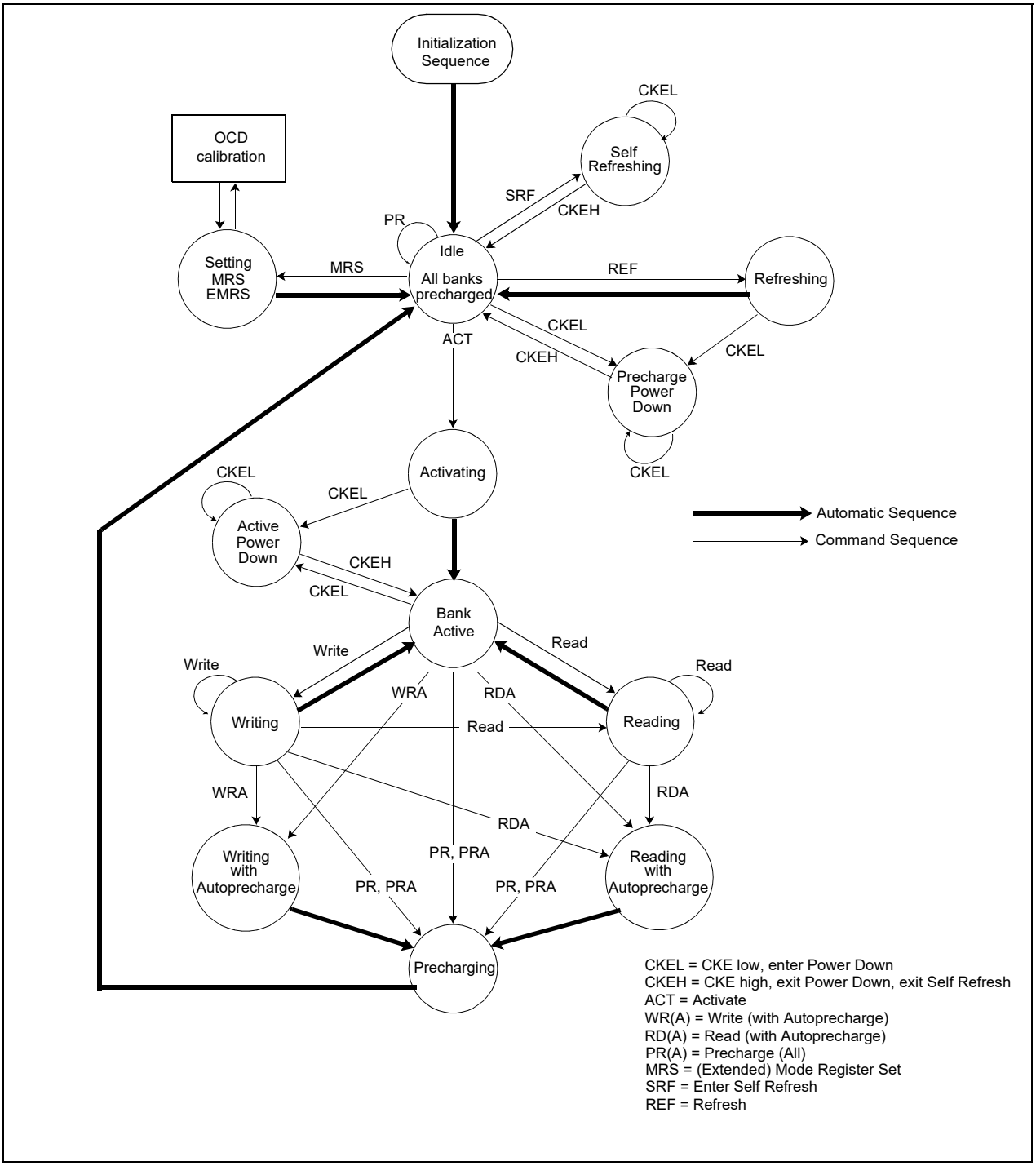
where

COLBITS = the number of column address bits

ORG = the number of I/O (DQ) bits

2 Functional Description

2.1 Simplified State Diagram



NOTE Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down entry/exit - among other things - are not captured in full detail.

Figure 6 — DDR2 SDRAM Simplified State Diagram

2 Functional Description (cont'd)

2.2 Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.2.1 Power-Up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/Extended Mode Register Set commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

2.2.1.1 Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

2. Start clock and maintain stable condition.
3. For the minimum of 200 us after stable power and clock (CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide "Low" to BA0 and BA2, "High" to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide "Low" to BA2, "High" to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-2 and A13~A15.)

2.2.1 Power up and Initialization (cont'd)

2.2.1.1 Power-up and Initialization Sequence (cont'd)

8. Issue a Mode Register Set command for "DLL reset".
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2, and A13~15.)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after Step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

*1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

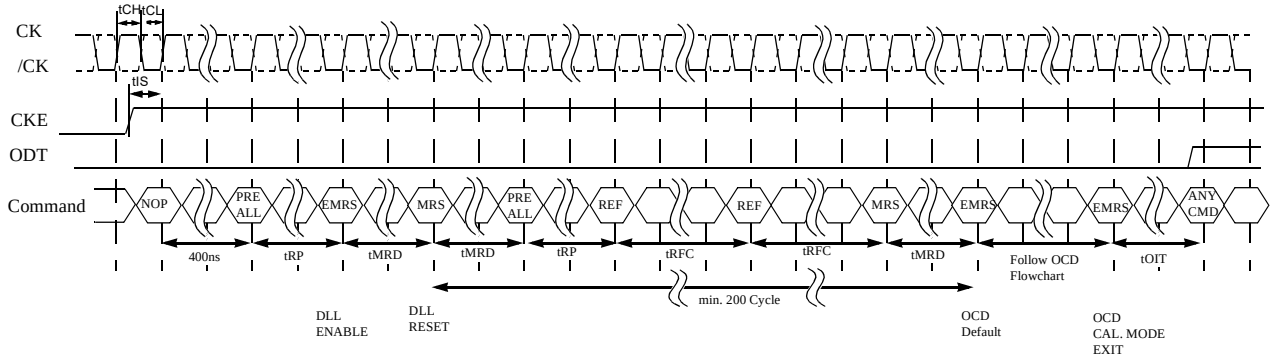


Figure 7 — Initialization Sequence after Power Up

2.2.2 Programming the Mode and Extended Mode Registers

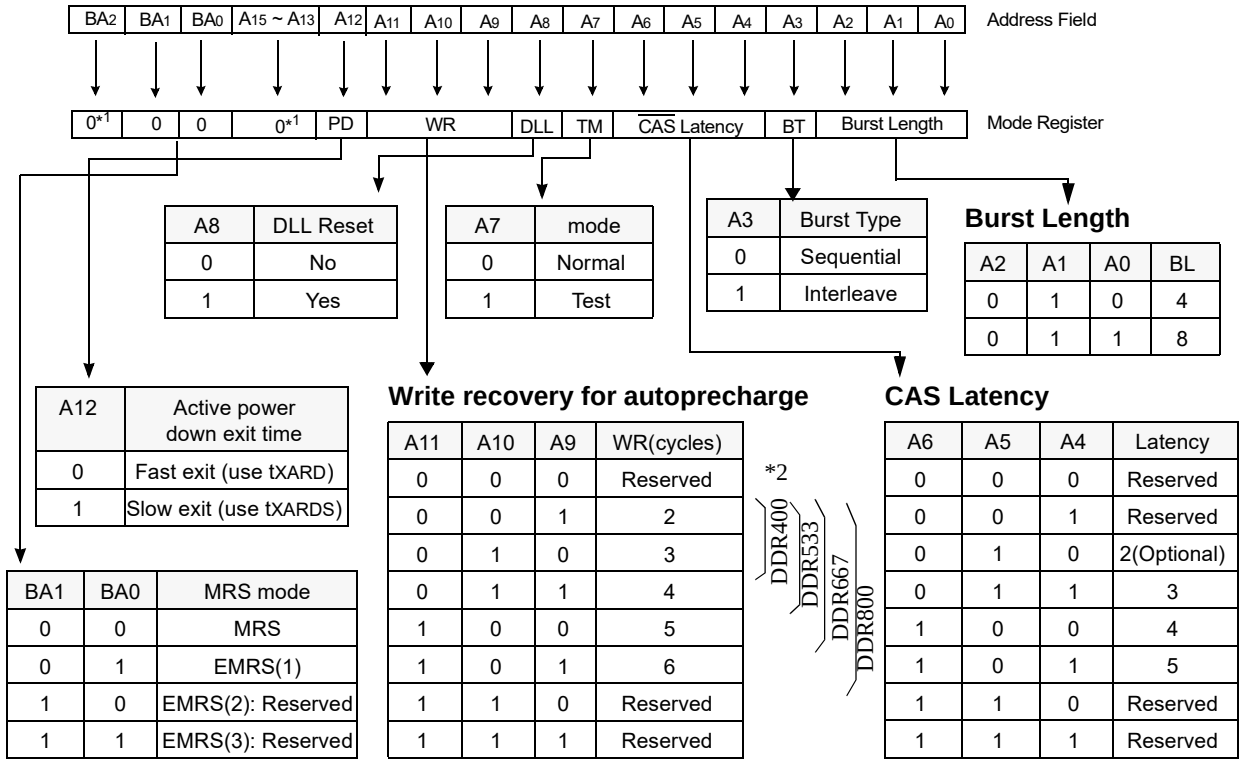
For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.2.2 Programming the Mode and Extended Mode Registers (cont'd)

2.2.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to Figure 8 for specific codes.



1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

2. WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Figure 8 — DDR2 SDRAM Mode Register Set (MRS)

2.2.2 Programming the Mode and Extended Mode Registers (cont'd)

2.2.2.2 DDR2 SDRAM Extended Mode Register Set

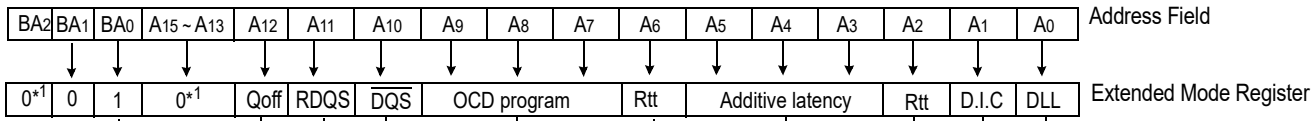
EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, DQS disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be written after power-up for proper operation. The extended mode register(1) is written by asserting low on CS, RAS, CAS, WE, high on BA0 and low on BA1, while controlling the states of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3~A5 determines the additive latency, A7~A9 are used for OCD control, A10 is used for DQS disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)



BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (NOMINAL)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[a]
1	1	1	OCD Calibration default [b]

a: When Adjust mode is issued, AL from previously set value must be applied.
b: After setting to default, OCD mode needs to be exited by setting A9-A7 to 000. Refer to the following 2.2.2.3 section for detailed information

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff (Optional)[a]
0	Output buffer enabled
1	Output buffer disabled

a. Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s, RDQS, $\overline{\text{RDQS}}$. This feature is used in conjunction with dimm IDD meaurements when IDDQ is not desired to be included.

A1	Output Driver Impedance Control	Driver Size
0	Normal	100%
1	Weak	60%

A10	$\overline{\text{DQS}}$
0	Enable
1	Disable

A11	RDQS Enable
0	Disable
1	Enable

* If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

A11 (RDQS Enable)	A10 ($\overline{\text{DQS}}$ Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS	DQS	DQS
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS	DQS	DQS
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

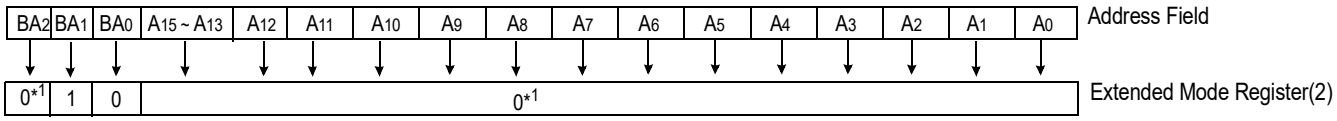
* BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

Figure 9 — EMRS(1) Programming

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)

EMRS(2)

1

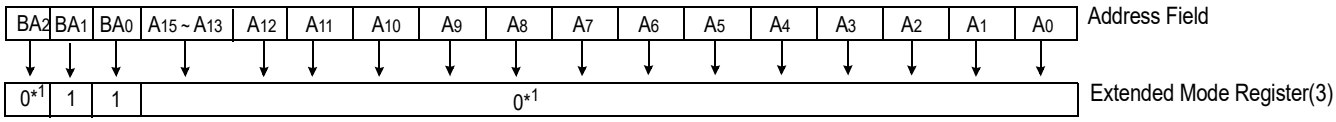


EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Figure 10 — EMRS(2) Programming: Reserved

EMRS(3)

1



EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

Figure 11 — EMRS(3) Programming: Reserved

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart in Figure 12 is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On DieTermination) should be carefully controlled depending on system environment.

Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{\text{DQS}}$ signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{\text{DQS}}$ signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in Table 6. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default output driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Table 6 — OCD Drive Mode Program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{\text{DQS}}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{\text{DQS}}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

.

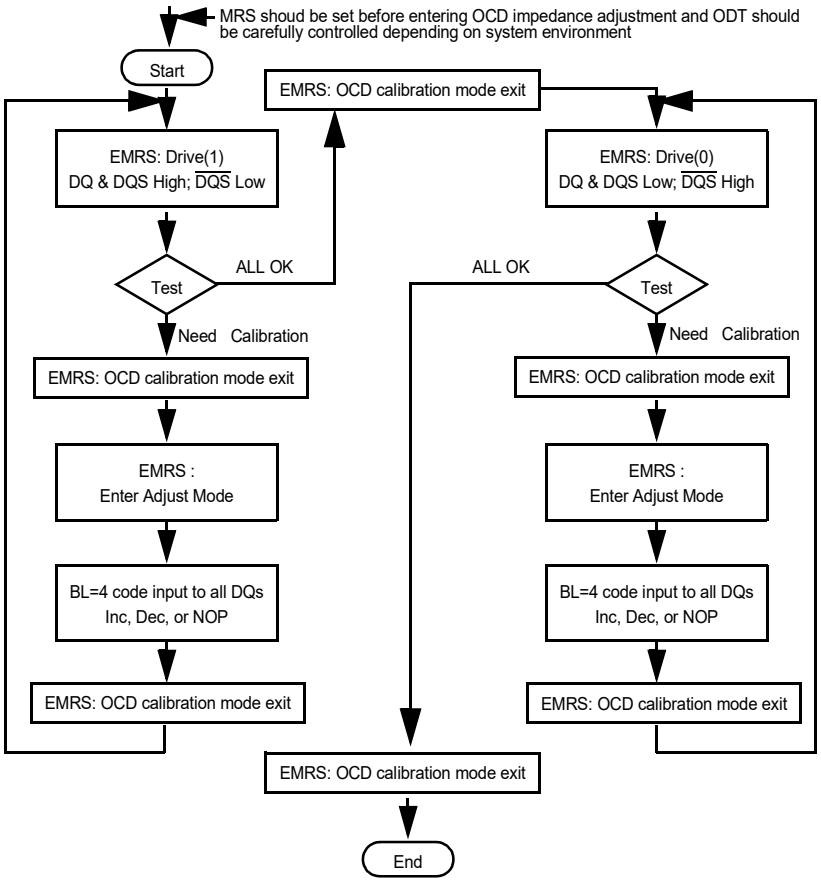


Figure 12 — OCD Impedance Adjustment

OCD Impedance Adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in Table 7. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in Table 7 means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

Table 7 — OCD Adjust Mode Program

4bit burst code inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as shown in Figure 13. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by MRS addressing mode (i.e. sequential or interleave).

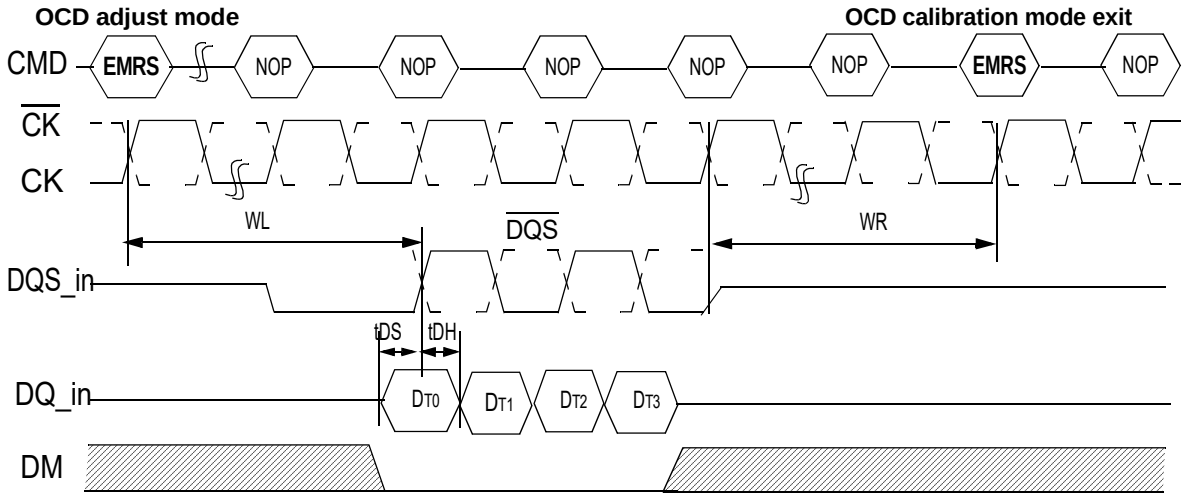


Figure 13 — OCD Adjust Mode

Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after "enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as shown in Figure 14.

2.2.2.3 Off-Chip Driver (OCD) Impedance Adjustment (cont'd)

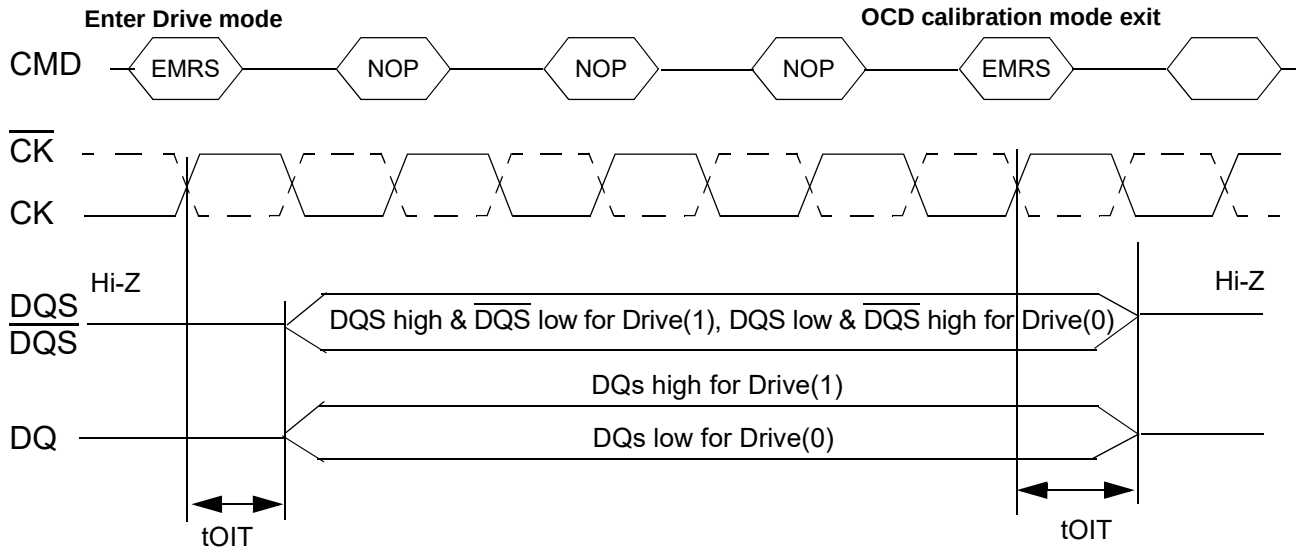


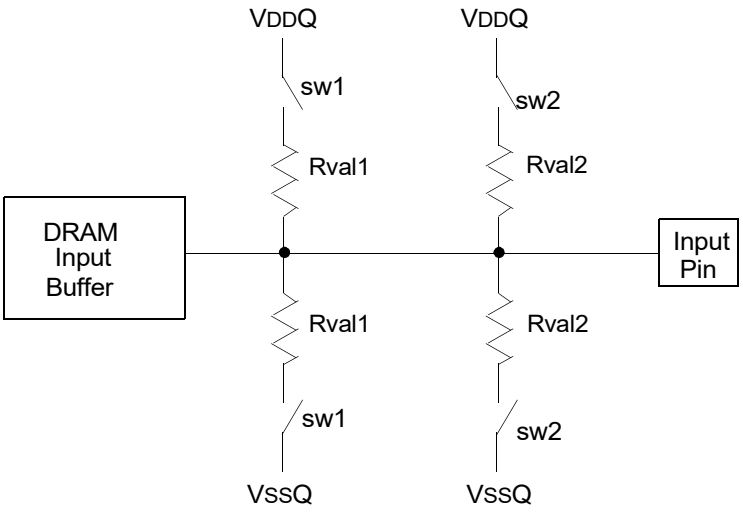
Figure 14 — OCD Drive Mode

2.2.2.4 ODT (On Die Termination)

On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

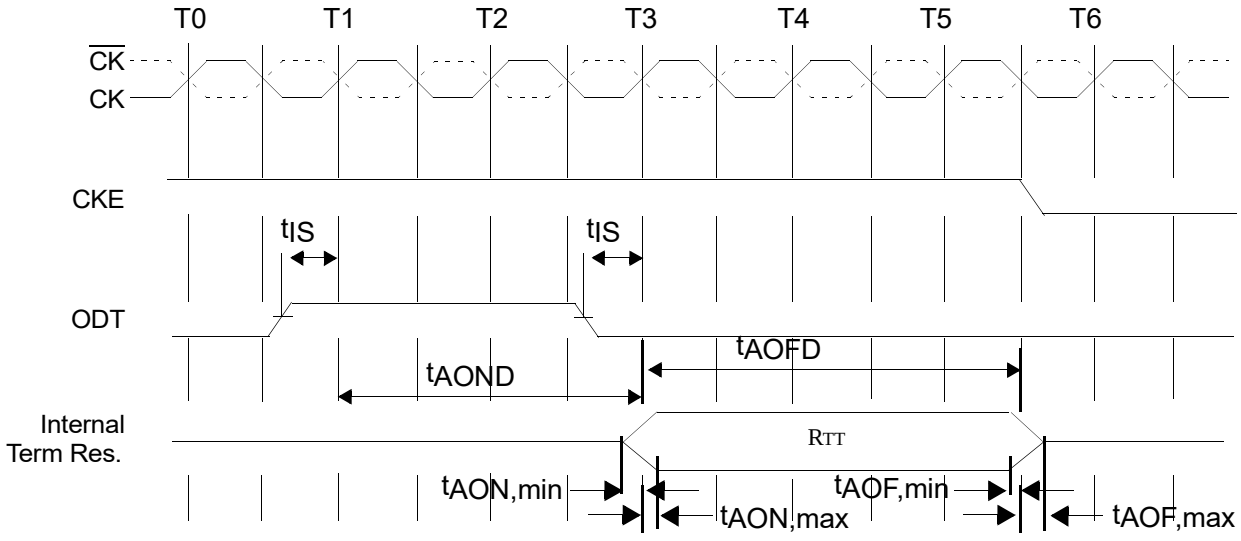


Figure 16 — ODT Timing for Active/Standby Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

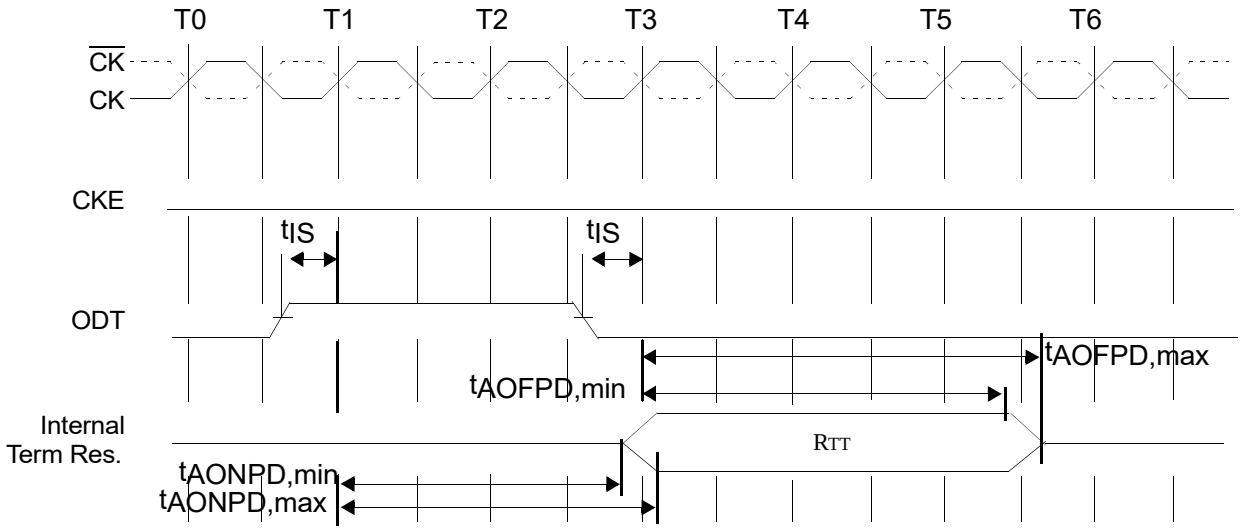


Figure 17 — ODT Timing for Powerdown Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

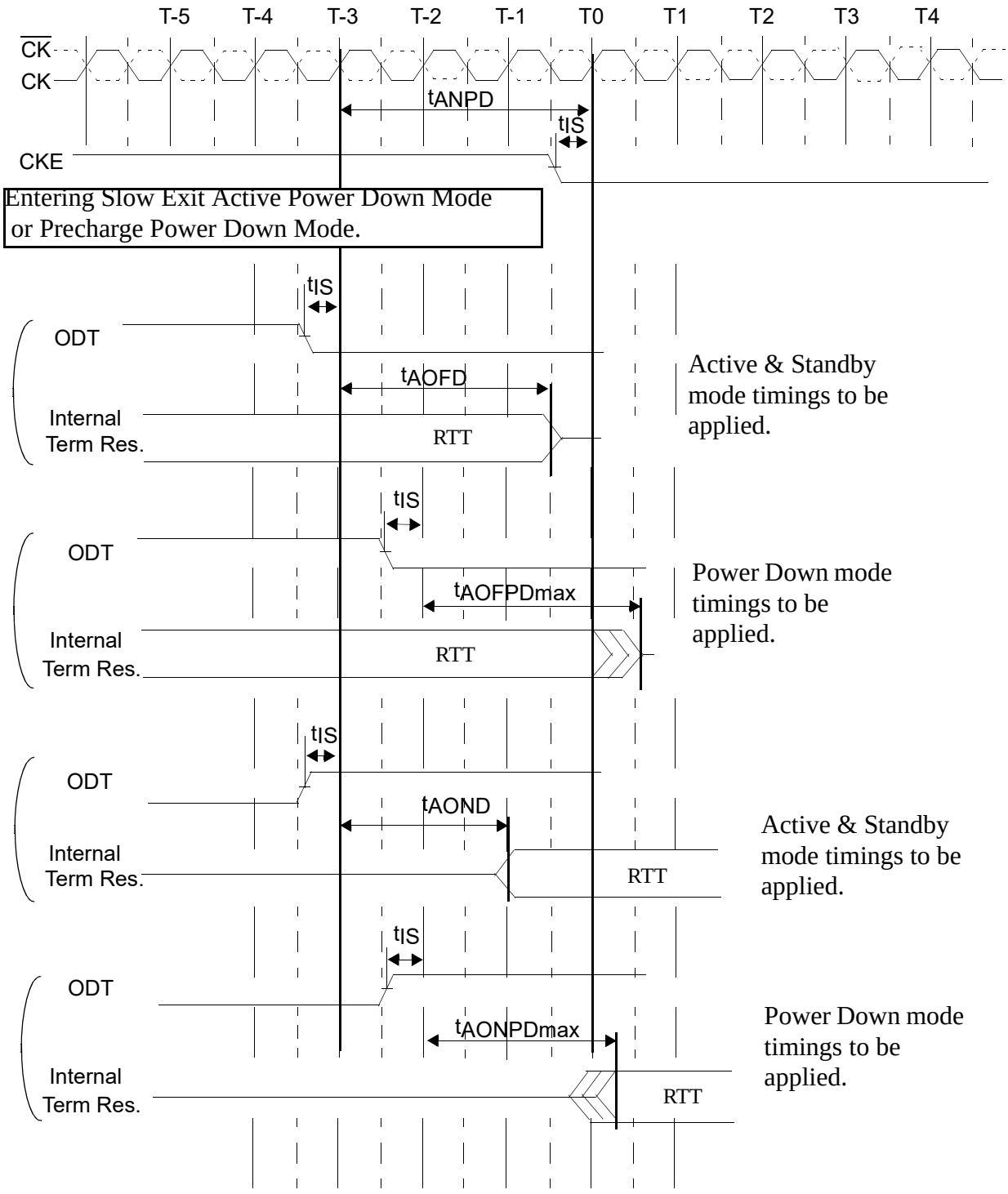


Figure 18 — ODT Timing Mode Switch at Entering Power Down Mode

2.2.2.4 ODT (On Die Termination) (cont'd)

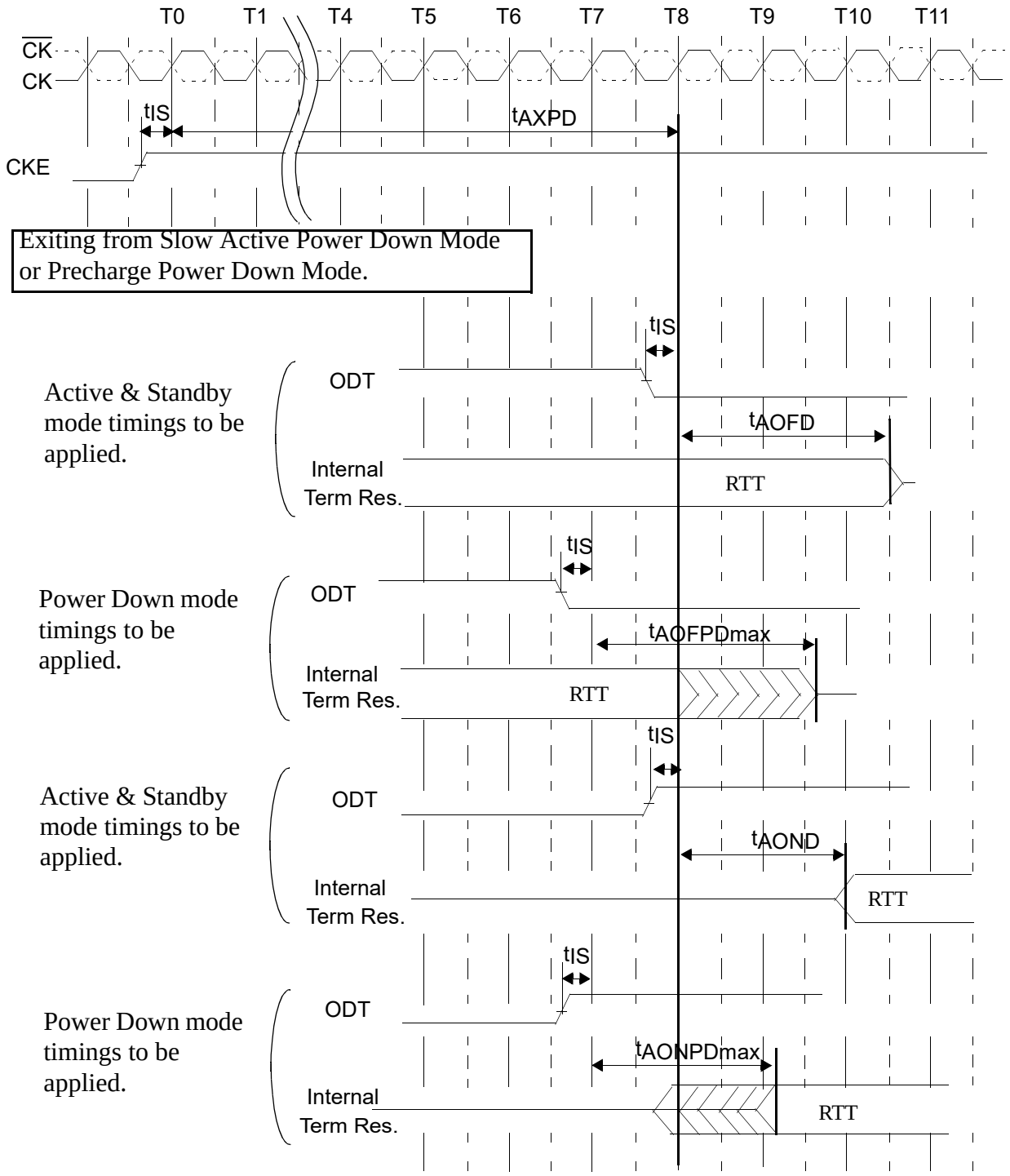


Figure 19 — ODT Timing Mode Switch at Exiting Power Down Mode

2.2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD}.

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules, one for restricting the number of sequential ACT commands that can be issued and another for allowing more time for $\overline{RAS}$ precharge for a Precharge All command. The rules are as follows:

1. 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling 4 * tRRD + 2 * tCK window. tRRD must be converted to clocks prior to multiplying by 4 and prior to adding 2*tCK. Converting to clocks is done by dividing tRRD(ns) by tCK(ns) and rounding up to next integer value.
2. 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will equal to tRP + 1 * tCK, where tRP is the value for a single bank pre-charge.

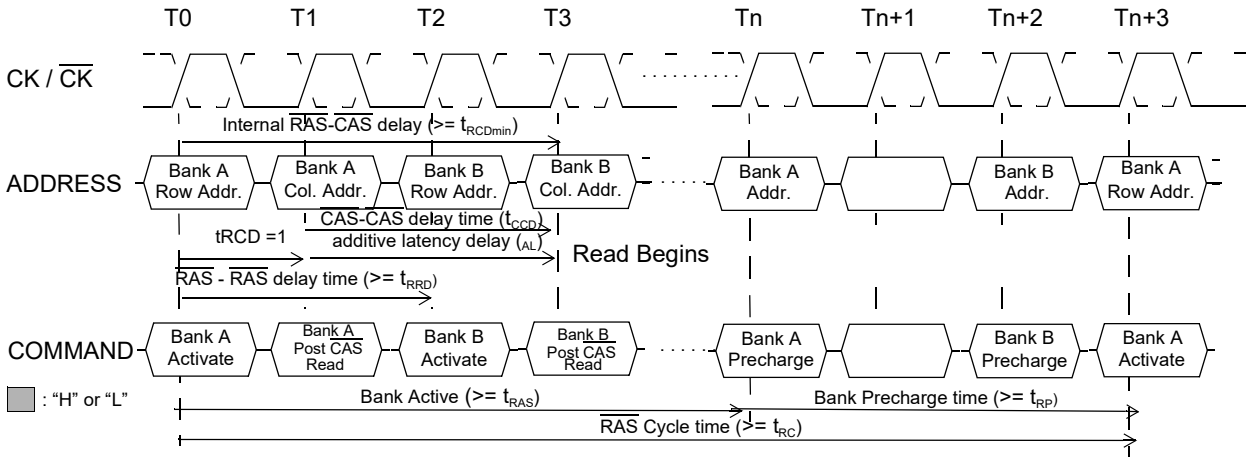


Figure 20 — Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

2.2.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting RAS high, CS and CAS low at the clock's rising edge. WE must also be defined at this time to determine whether the access cycle is a read operation (WE high) or a write operation (WE low).

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 2048 bits (defined by CA0-CA9, CA11). The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8 bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum CAS to CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

2.2.4.1 Posted CAS

Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a CAS read or write command to be issued immediately after the RAS bank activate command (or any time during the RAS-CAS-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCDmin, then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section).

Examples of posted CAS operation

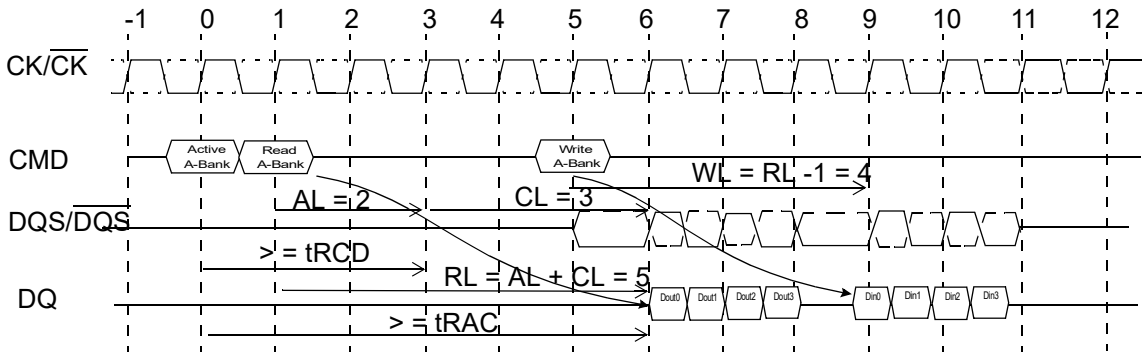


Figure 21 — Example 1: Read Followed by a Write to the Same Bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

2.2.4 Read and Write Access Modes (cont'd)

2.2.4.1 Posted $\overline{CAS}$ (cont'd)

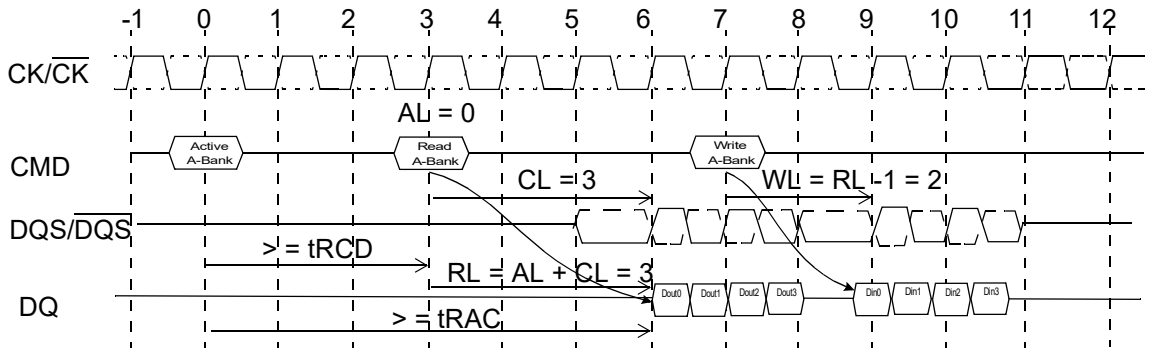


Figure 22 — Example 2: Read Followed by a Write to the Same Bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

2.2.4.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bit burst and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR SDRAM operation. Seamless burst read or write operations are supported. Unlike DDR devices, interruption of a burst read or write cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Table 8 — Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

NOTE Page length is a function of I/O organization and column addressing.

2.2.4 Read and Write Access Modes (cont'd)

2.2.4.3 Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs. The AL is defined by the Extended Mode Register Set (1)(EMRS(1)).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single-ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

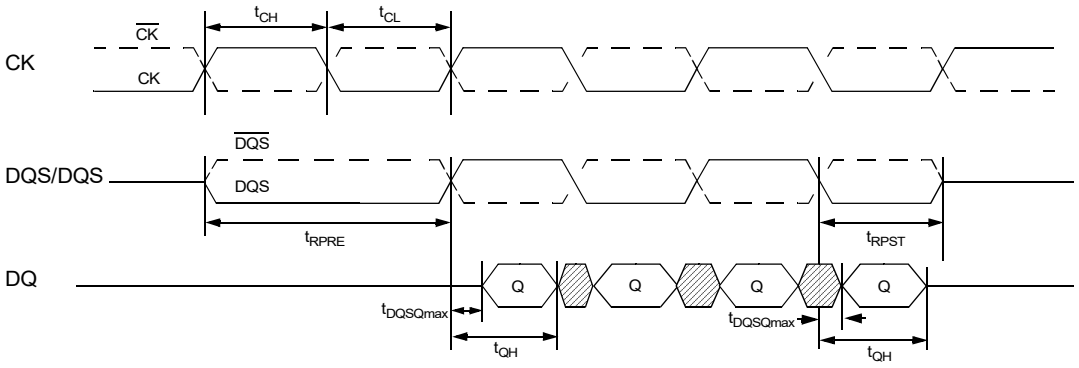


Figure 23 — Data Output (Read) Timing

2.2.4.3 Burst Read Command (cont'd)

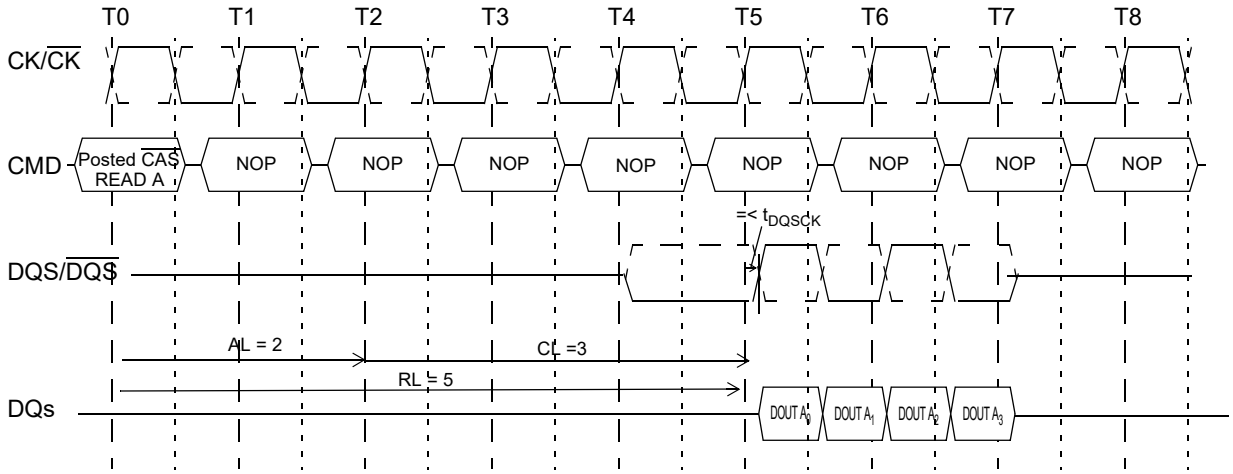


Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

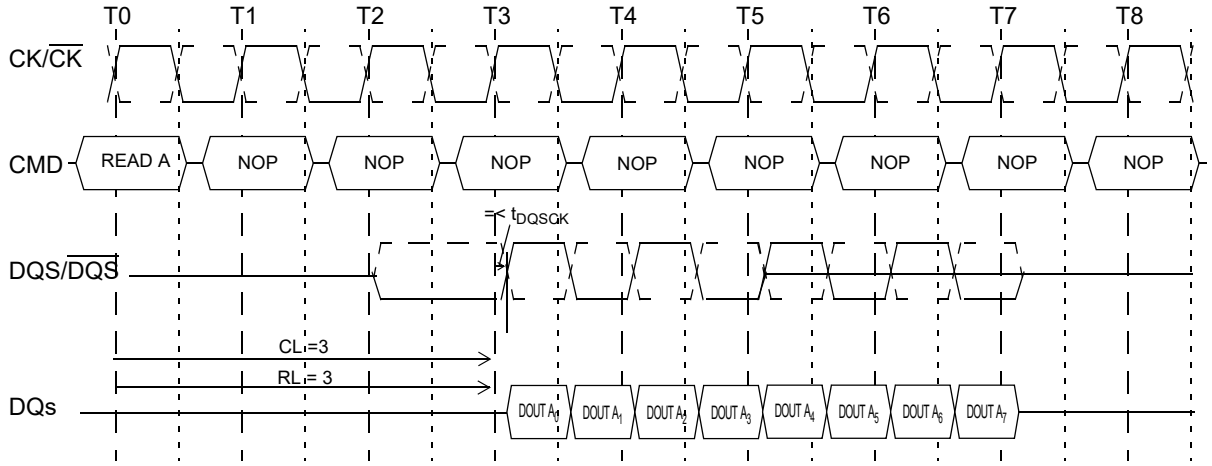
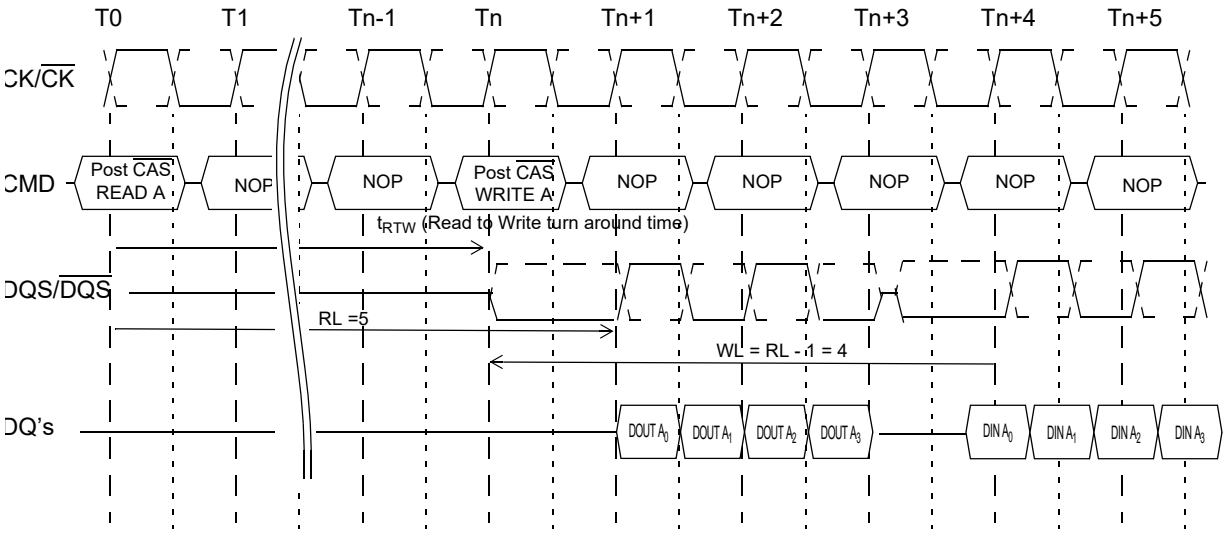


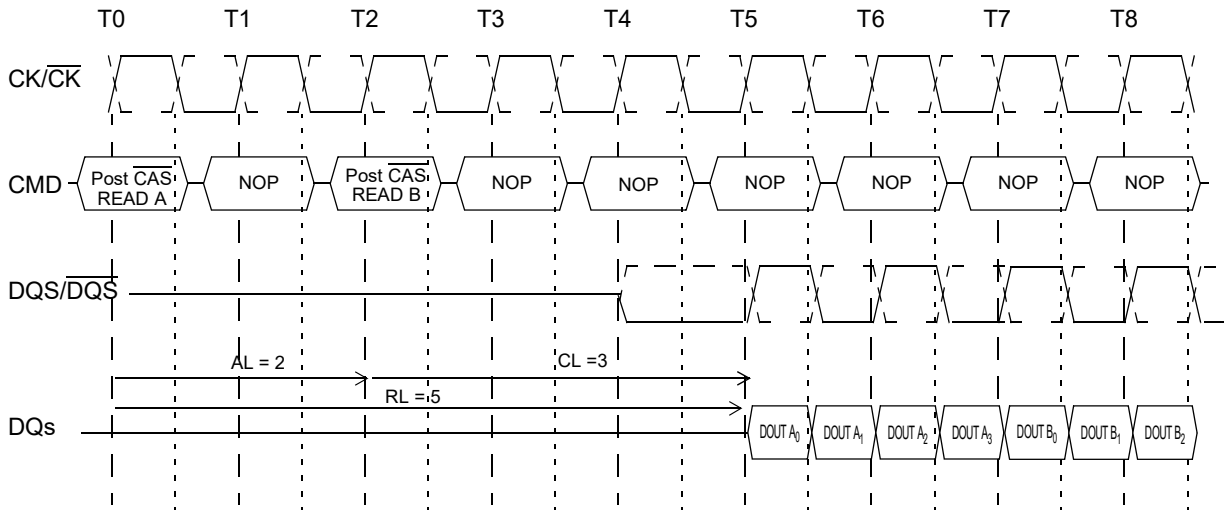
Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

2.2.4.3 Burst Read Command (cont'd)



The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Figure 26 — Burst Read Followed by Burst Write: RL = 5, WL = (RL-1) = 4, BL = 4



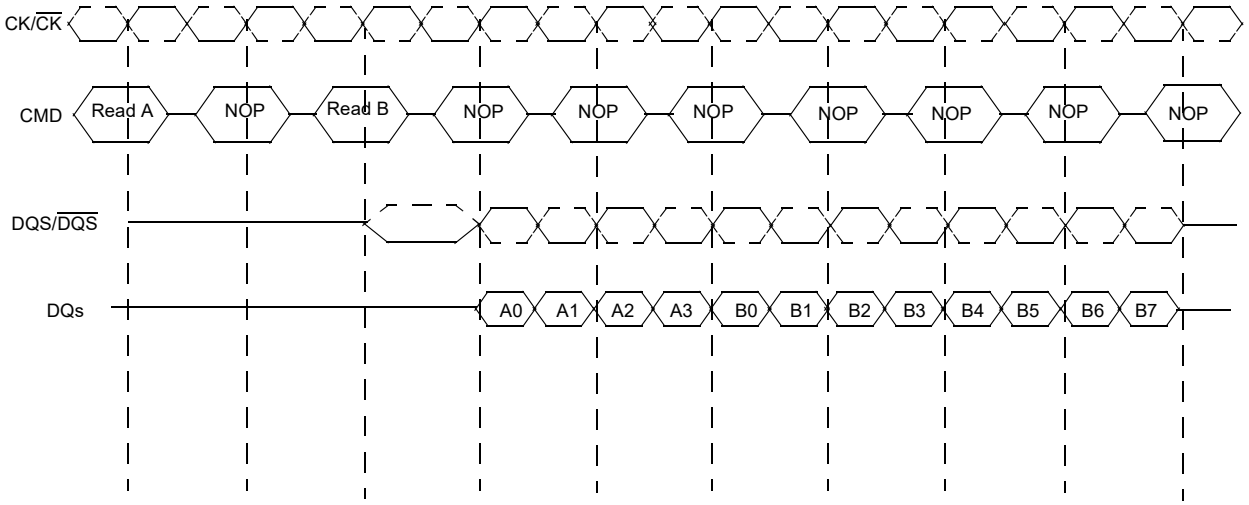
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

Reads Interrupted by a Read

Burst read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

2.2.4.3 Burst Read Command (cont'd)



NOTE 1 Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
NOTE 2 Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
NOTE 3 Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
NOTE 4 Read burst interruption is allowed to any bank inside DRAM.
NOTE 5 Read burst with Auto Precharge enabled is not allowed to interrupt.
NOTE 6 Read burst interruption is allowed by another Read with Auto Precharge command.
NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

Figure 28 — Read Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, BL=8)

2.2.4.4 Burst Write Operation

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR).

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 Kohm resistor to insure proper operation.

2.2.4.4 Burst Write Operation (cont'd)

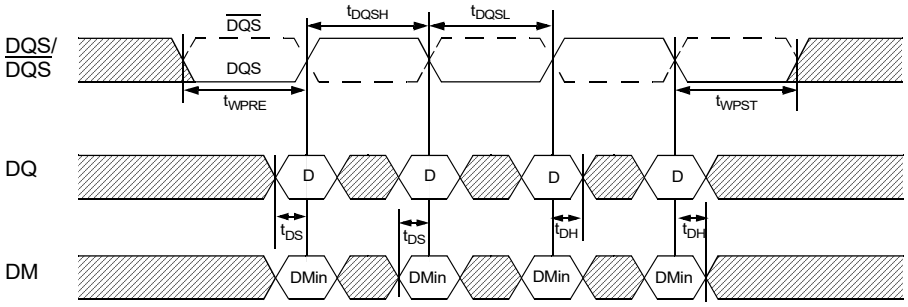


Figure 29 — Data Input (Write) Timing

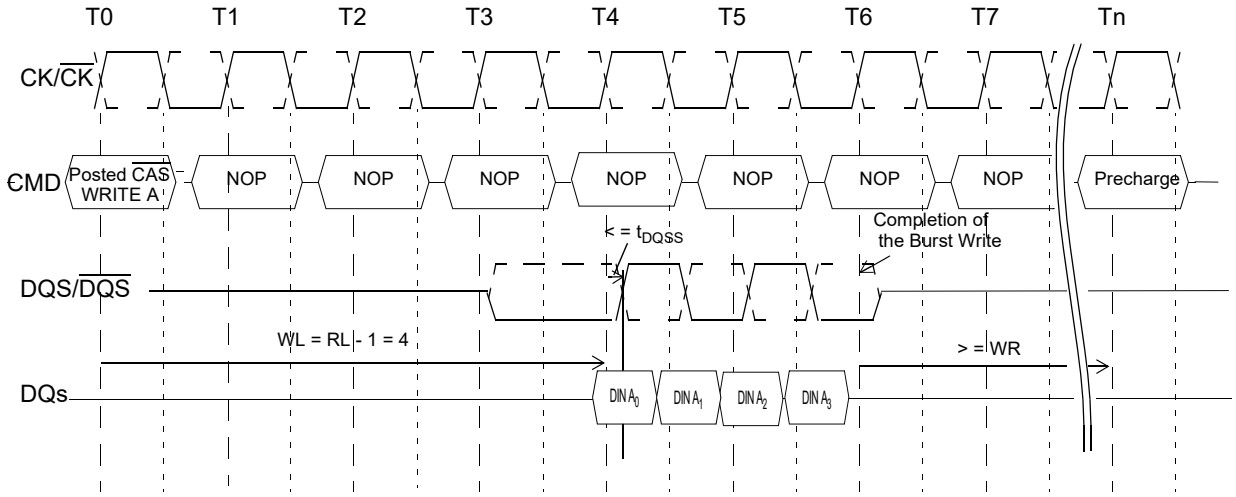


Figure 30 — Burst Write Operation: RL = 5, WL = 4, tWR = 3 (AL=2, CL=3), BL = 4

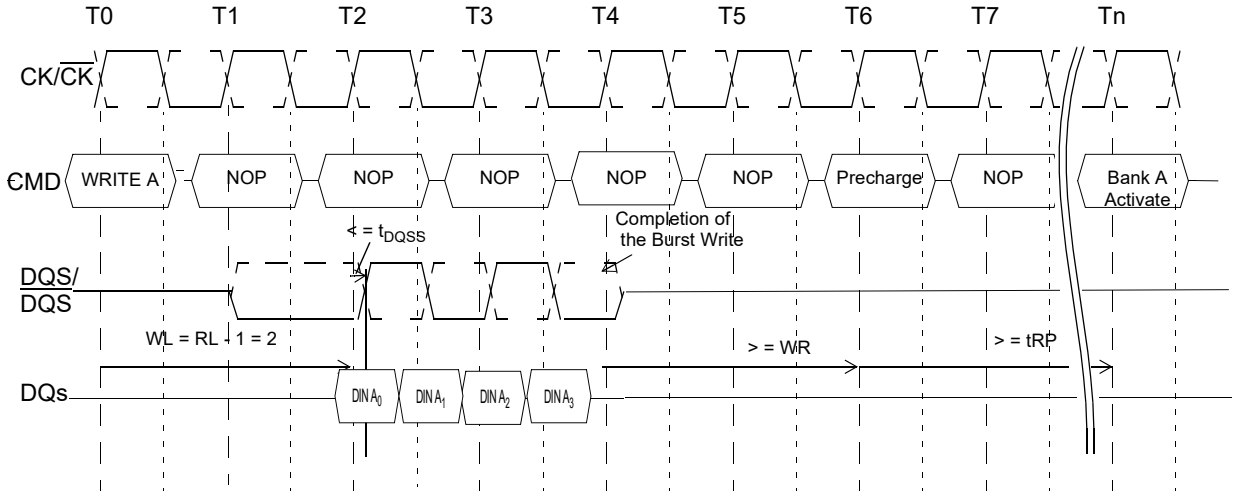
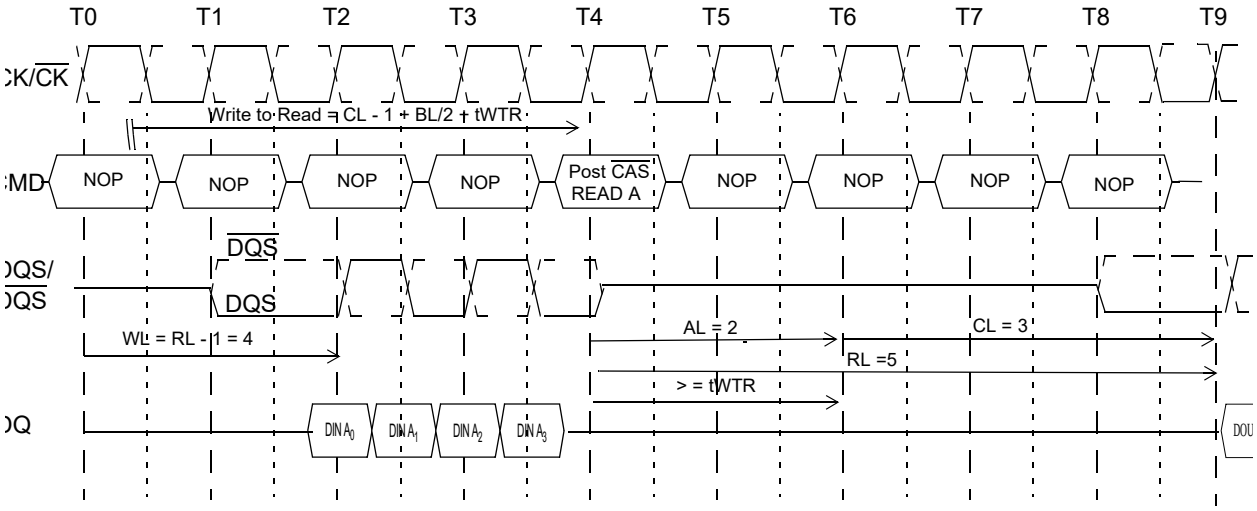


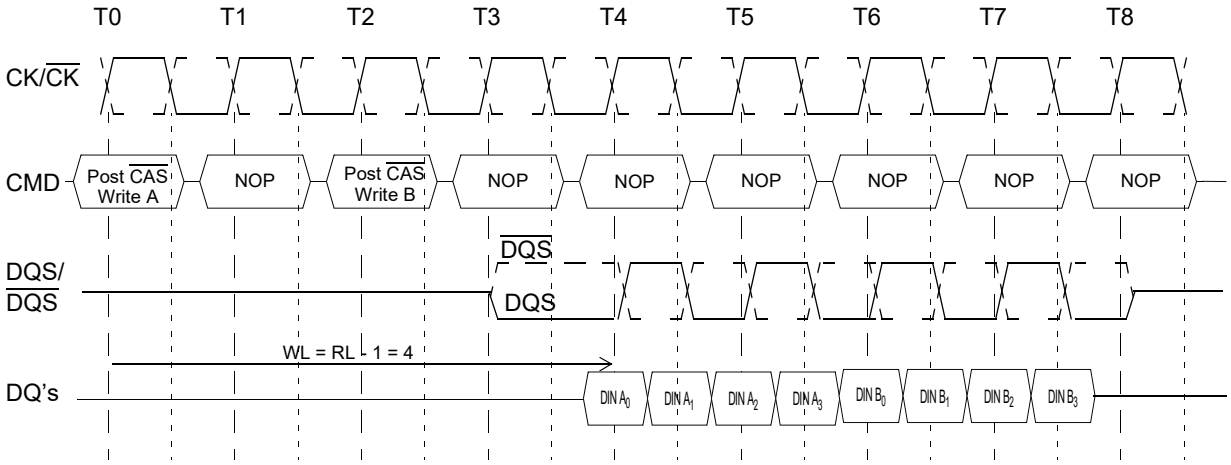
Figure 31 — Burst Write Operation: RL = 3, WL = 2, tWR = 2 (AL=0, CL=3), BL = 4

2.2.4.4 Burst Write Operation (cont'd)



The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

Figure 32 — Burst Write Followed by Burst Read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4



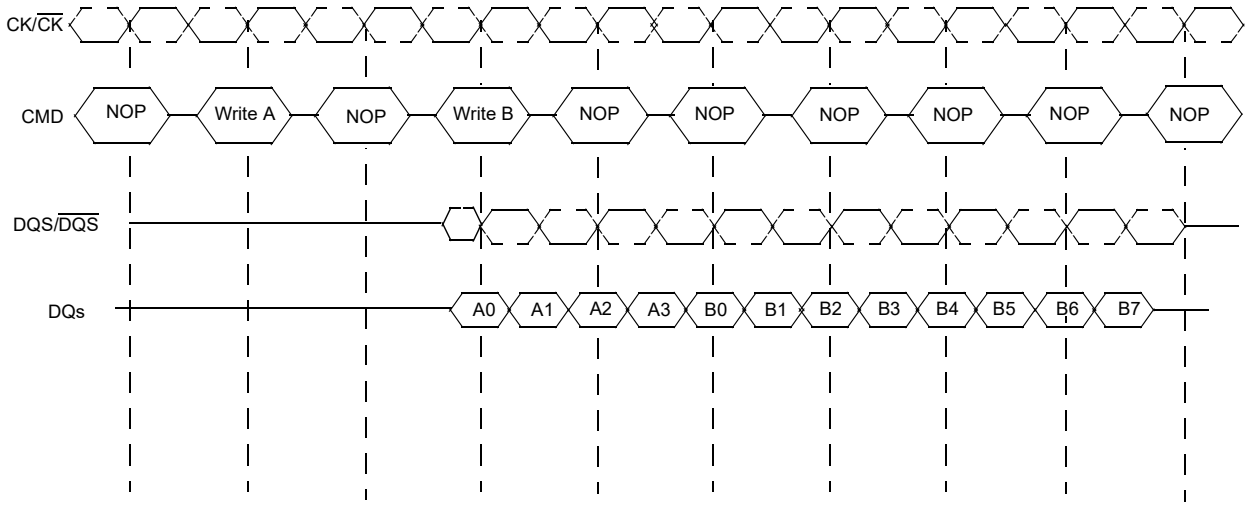
The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for
BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 33 — Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

Writes Interrupted by a Write

Burst write can only be interrupted by another write with 4 bit burst boundary. Any other case of write interrupt is not allowed.

2.2.4.4 Burst Write Operation (cont'd)



NOTE 1 Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

NOTE 2 Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.

NOTE 3 Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.

NOTE 4 Write burst interruption is allowed to any bank inside DRAM.

NOTE 5 Write burst with Auto Precharge enabled is not allowed to interrupt.

NOTE 6 Write burst interruption is allowed by another Write with Auto Precharge command.

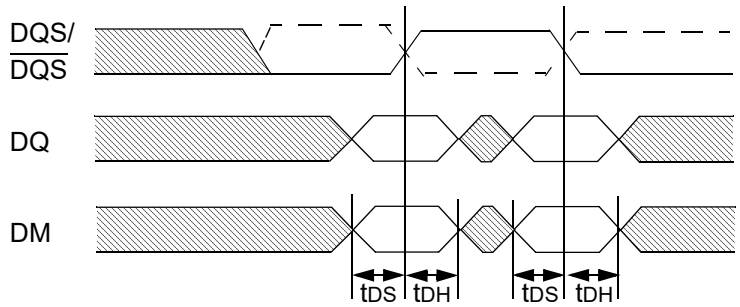
NOTE 7 All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

Figure 34 — Write Burst Interrupt Timing Example: (CL=3, AL=0, RL=3, WL=2, BL=8)

2.2.4.5 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However DM of x8 bit organization can be used as RDQS during read cycles by EMRS(1) setting.

Data Mask Timing



Data Mask Function, WL=3, AL=0, BL = 4 shown

Case 1: min t_{DQSS}

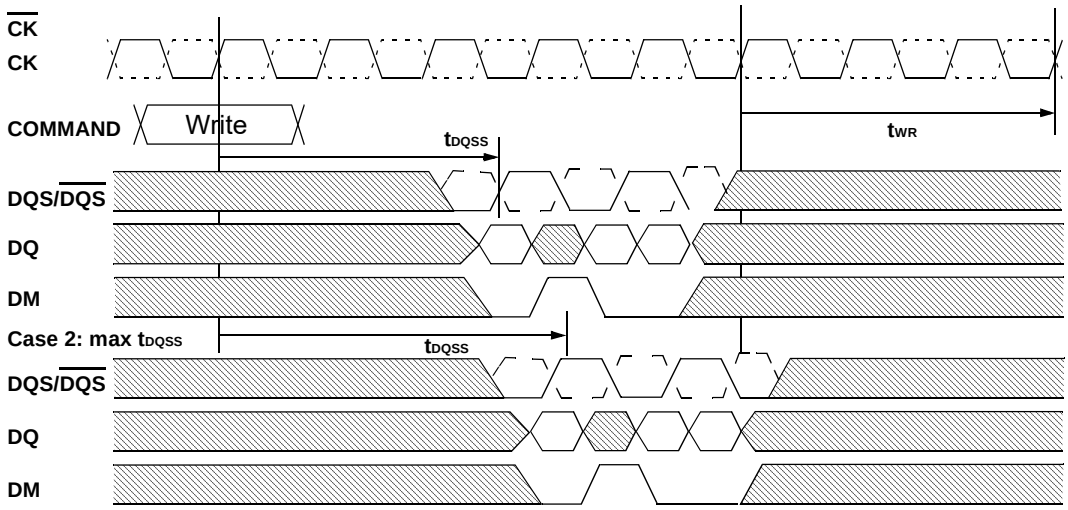


Figure 35 — Write Data Mask

2.2.5 Precharge Operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 for 256Mb and 512Mb and four address bits A10, BA0 ~ BA2 for 1Gb and higher densities are used to define which bank to precharge when the command is issued. For 8 bank devices, refer to Section 2.2.3 of this data sheet.

2.2.5 Precharge Operation (cont'd)

Table 9 — Bank Selection for Precharge by Address Bits

A10	BA2	BA0	BA1	Precharged Bank(s)	Remarks
LOW	LOW	LOW	LOW	Bank 0 only	
LOW	LOW	LOW	HIGH	Bank 1 only	
LOW	LOW	HIGH	LOW	Bank 2 only	
LOW	LOW	HIGH	HIGH	Bank 3 only	
LOW	HIGH	LOW	LOW	Bank 4 only	1 Gb and higher
LOW	HIGH	LOW	HIGH	Bank 5 only	1 Gb and higher
LOW	HIGH	HIGH	LOW	Bank 6 only	1 Gb and higher
LOW	HIGH	HIGH	HIGH	Bank 7 only	1 Gb and higher
HIGH	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	

2.2.5.1 Burst Read Operation Followed by Precharge

Minimum Read to precharge command spacing to the same bank = AL + BL/2 clocks
For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive latency(AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (t_{RP}). A precharge command cannot be issued until t_{RAS} is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command.

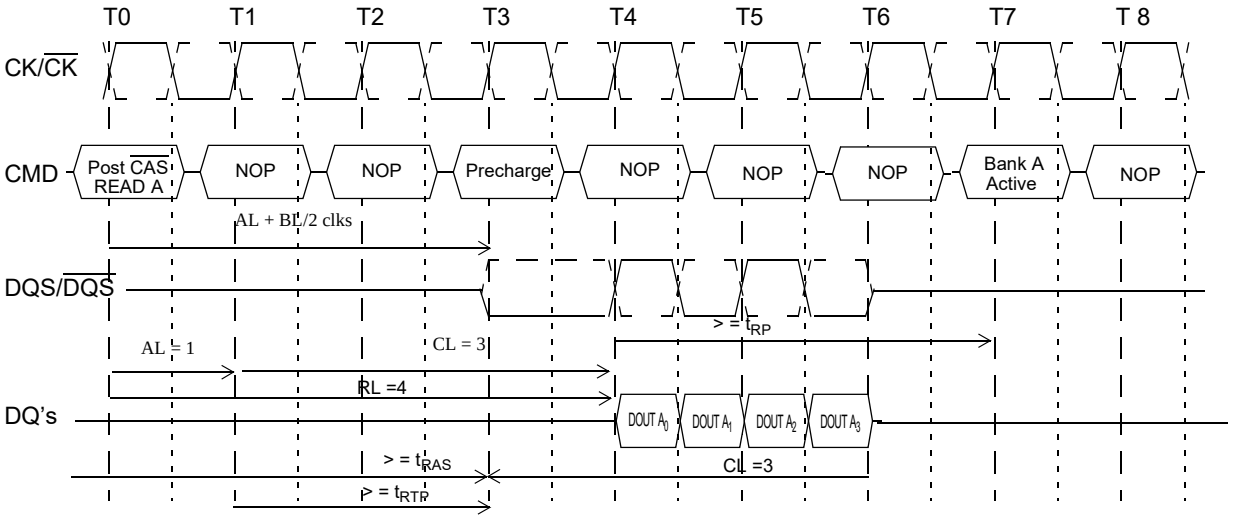


Figure 36 — Example 1: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.2.5.1 Burst Read Operation Followed by Precharge (cont'd)

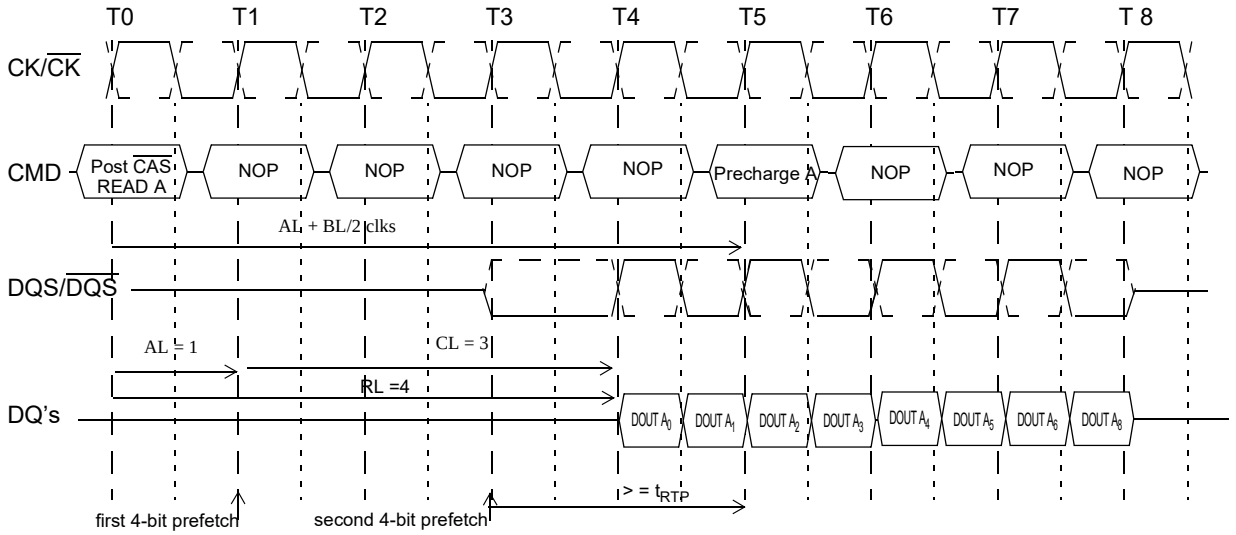


Figure 37 — Example 2: Burst Read Operation Followed by Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

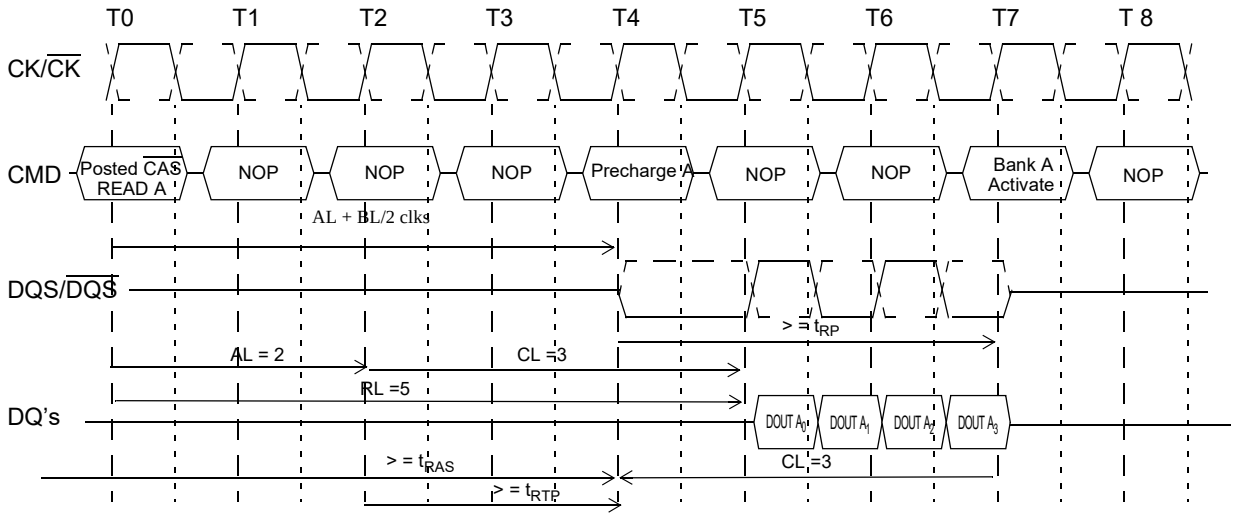


Figure 38 — Example 3: Burst Read Operation Followed by Precharge: RL = 5, AL = 2, CL = 3, BL = 4, t_{RTP} <= 2 clocks

2.2.5.1 Burst Read Operation Followed by Precharge (cont'd)

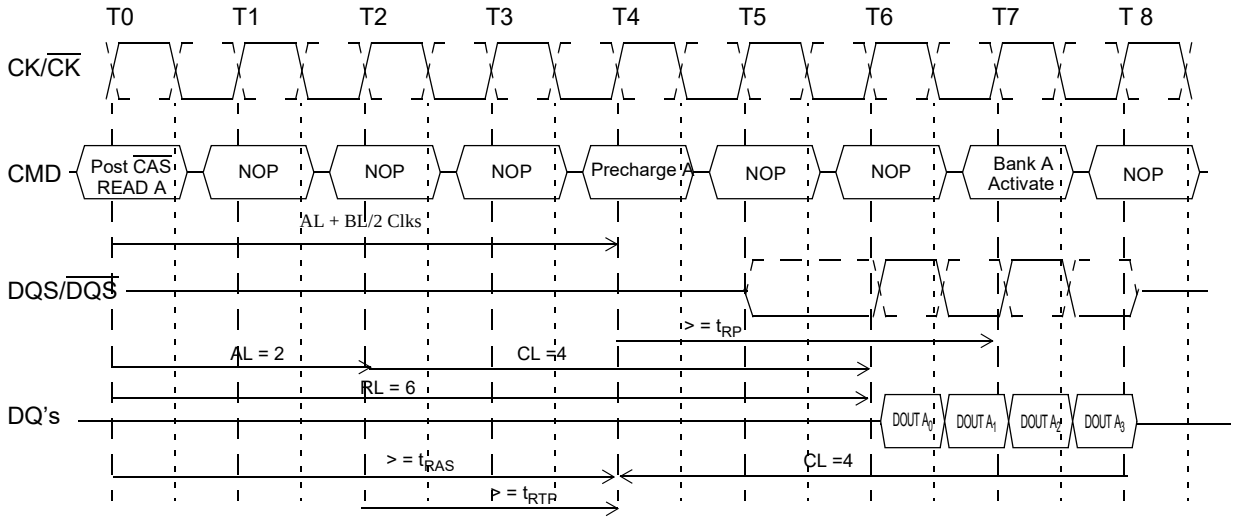
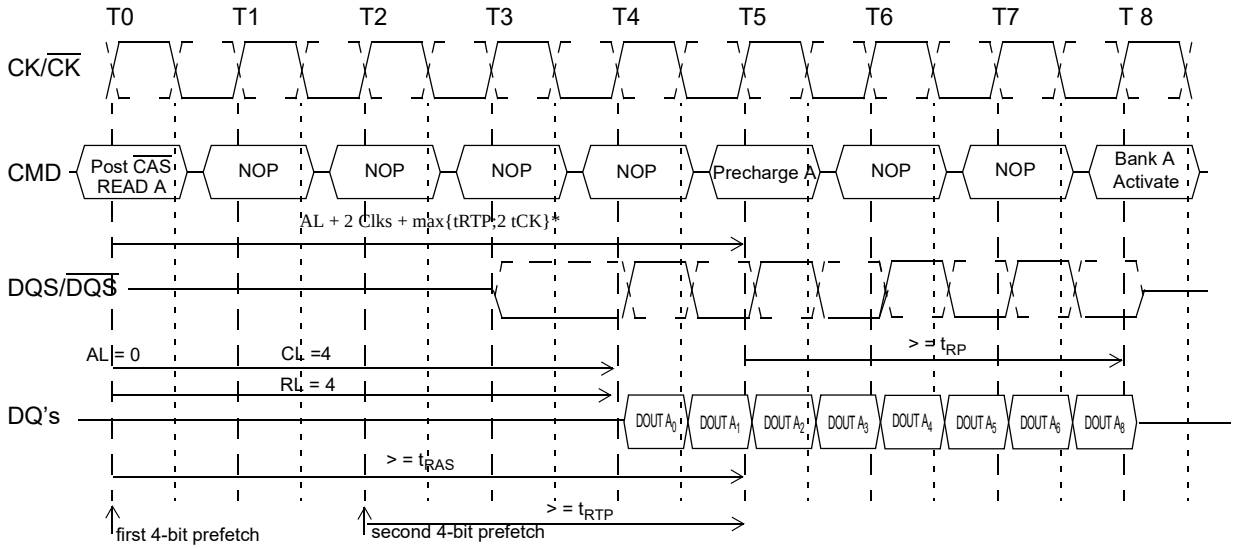


Figure 39 — Example 4: Burst Read Operation Followed by Precharge: RL = 6, AL = 2, CL = 4, BL = 4, t_{RTP} <= 2 clocks



*: rounded to next integer

Figure 40 — Example 5: Burst Read Operation Followed by Precharge: RL = 4, AL = 0, CL = 4, BL = 8, t_{RTP} > 2 clocks

2.2.5.2 Burst Write followed by Precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay.

2.2.5.2 Burst Write followed by Precharge (cont'd)

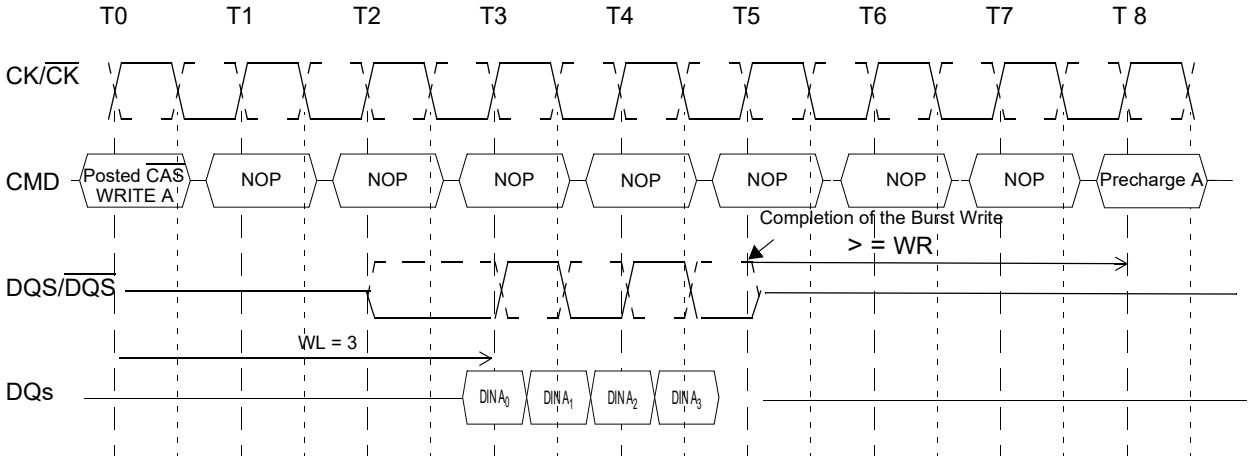


Figure 41 — Example 1: Burst Write followed by Precharge: WL = (RL-1) =3

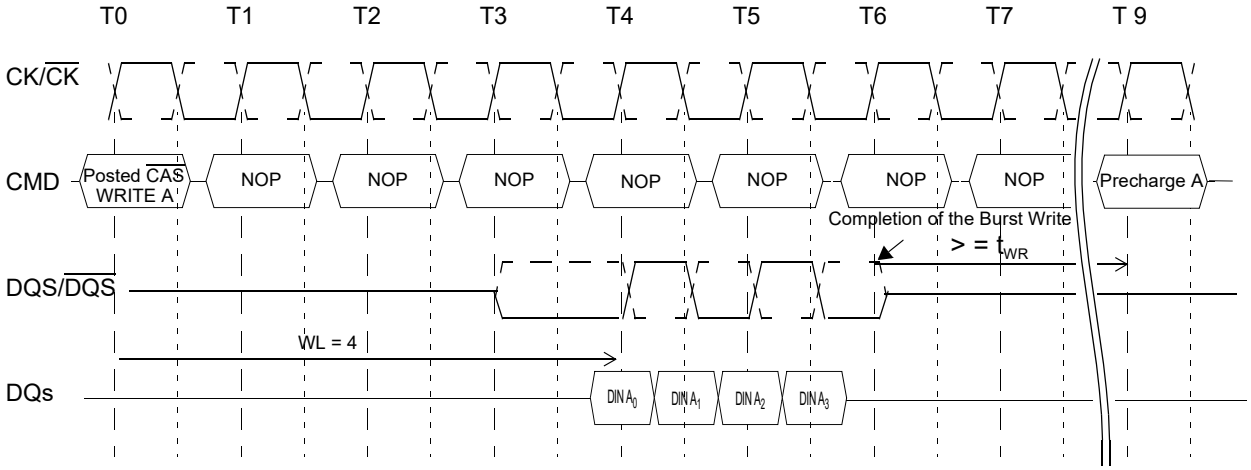


Figure 42 — Example 2: Burst Write followed by Precharge: WL = (RL-1) = 4

2.2.6 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS latency (CL) clock cycles before the end of the read burst.

Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

2.2.6 Auto Precharge Operation (cont'd)

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ latency) thus improving system performance for random data access. The $\overline{RAS}$ lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read or write command.

2.2.6.1 Burst Read with Auto Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP(min) are satisfied.

If tRAS(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRAS(min) is satisfied.

If tRTP(min) is not satisfied at the edge, the start point of auto-precharge operation will be delayed until tRTP(min) is satisfied.

In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read_AP to the next Activate command becomes AL + (tRTP + tRP)* (see example 2) for BL = 8 the time from Read_AP to the next Activate is AL + 2 + (tRTP + tRP)*, where "*" means: "rounded up to the next integer". In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.
(1) The $\overline{RAS}$ precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

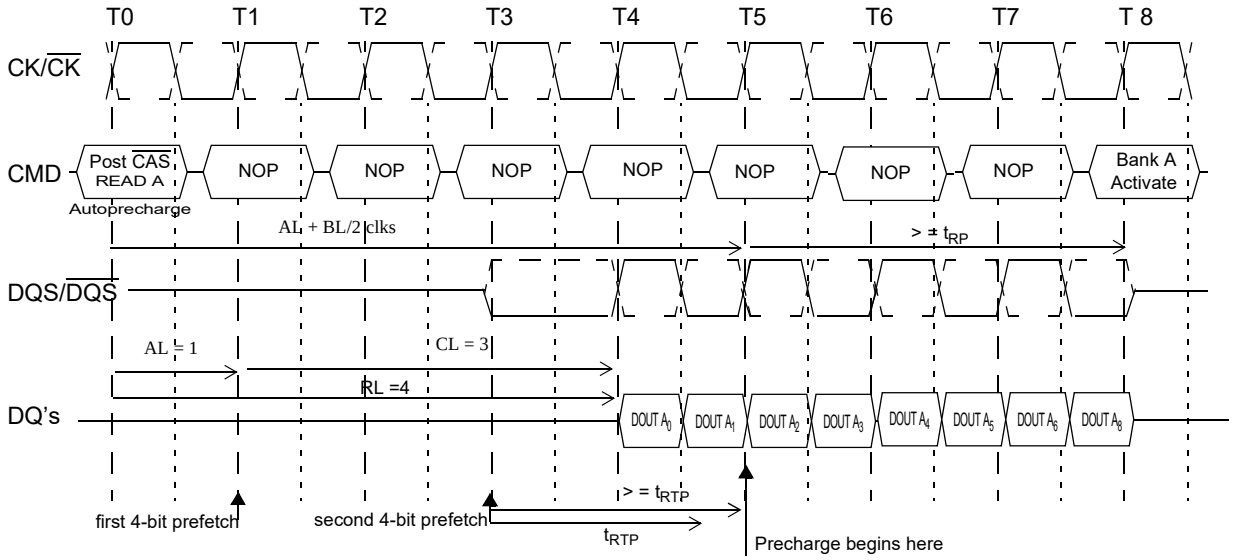


Figure 43 — Example 1: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

2.2.6.1 Burst Read with Auto Precharge (cont'd)

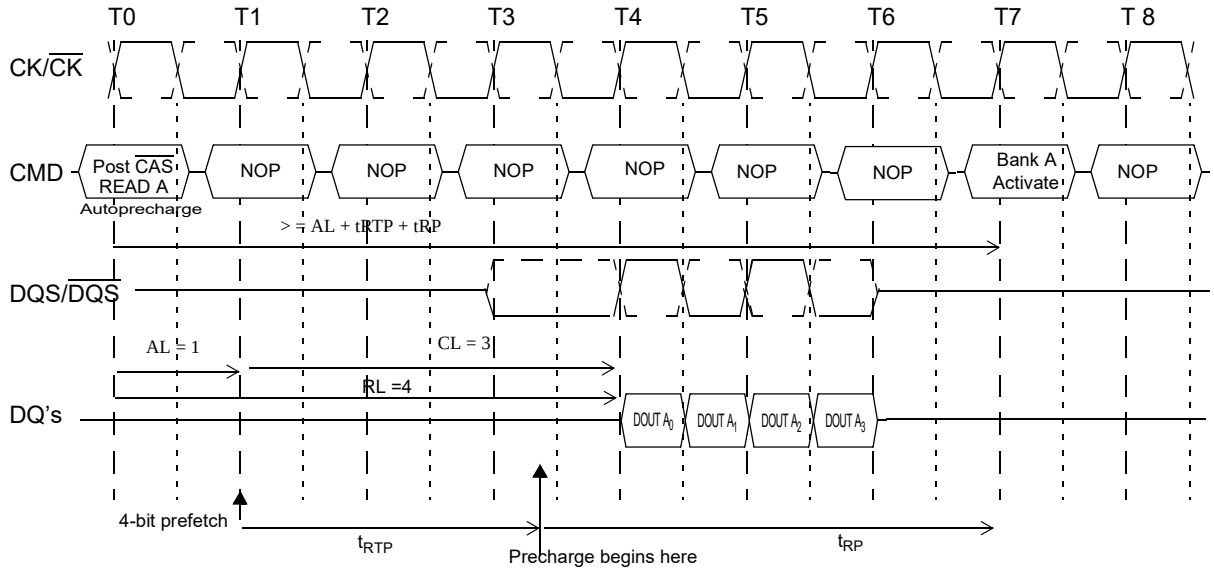


Figure 44 — Example 2: Burst Read Operation with Auto Precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} > 2 clocks

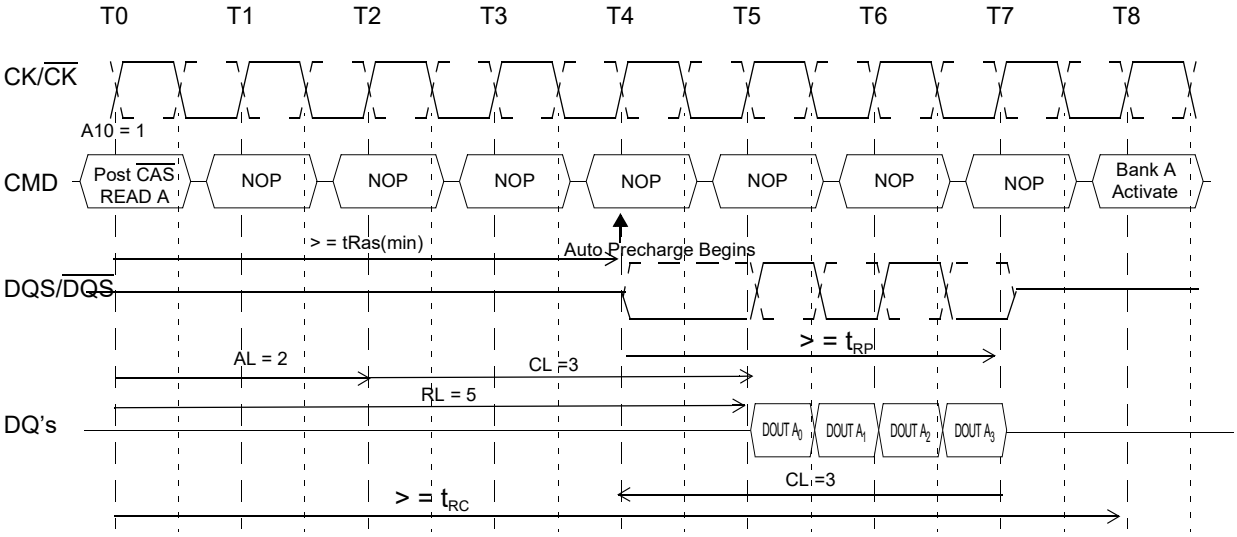


Figure 45 — Example 3: Burst Read with Auto Precharge Followed by an Activation to the Same Bank(tRC Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.2.6.1 Burst Read with Auto Precharge (cont'd)

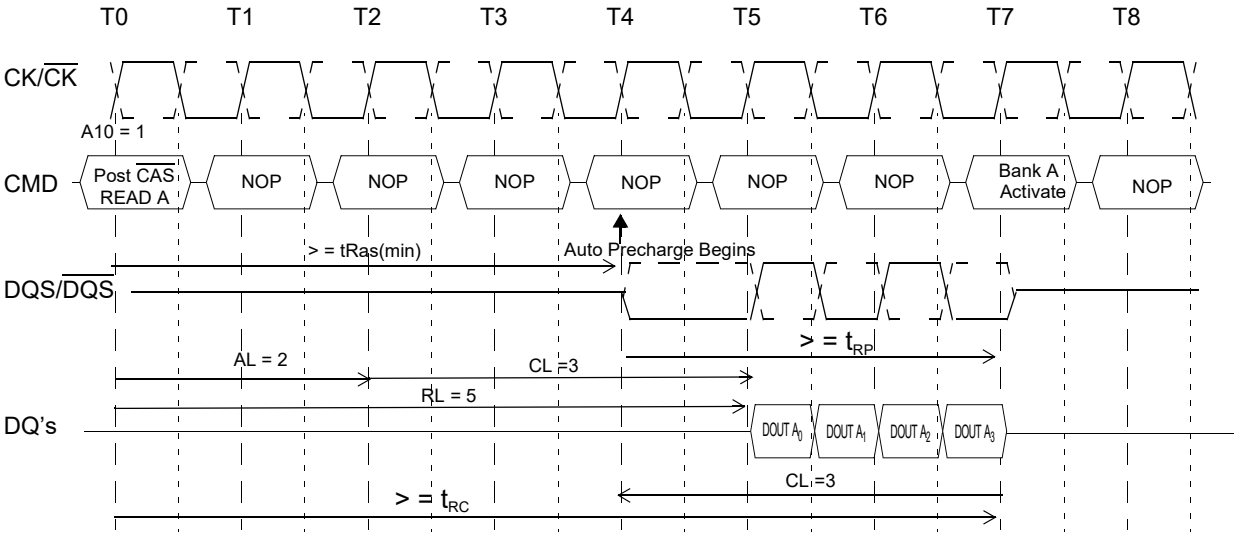


Figure 46 — Example 4: Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP Limit): RL = 5 (AL = 2, CL = 3, internal tRCD = 3, BL = 4, t_{RTP} <= 2 clocks)

2.2.6.2 Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

1) The data-in to bank activate delay time (WR + tRP) has been satisfied.
2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

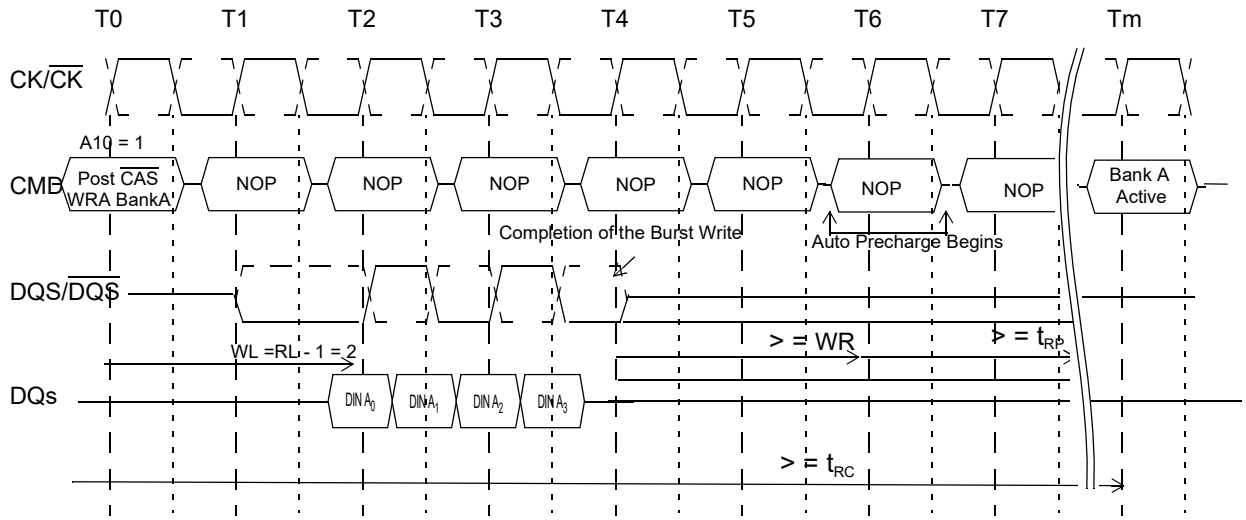


Figure 47 — Burst Write with Auto-Precharge (tRC Limit): WL = 2, tWR =2, BL = 4, tRP=3

2.2.6.2 Burst Write with Auto-Precharge (cont'd)

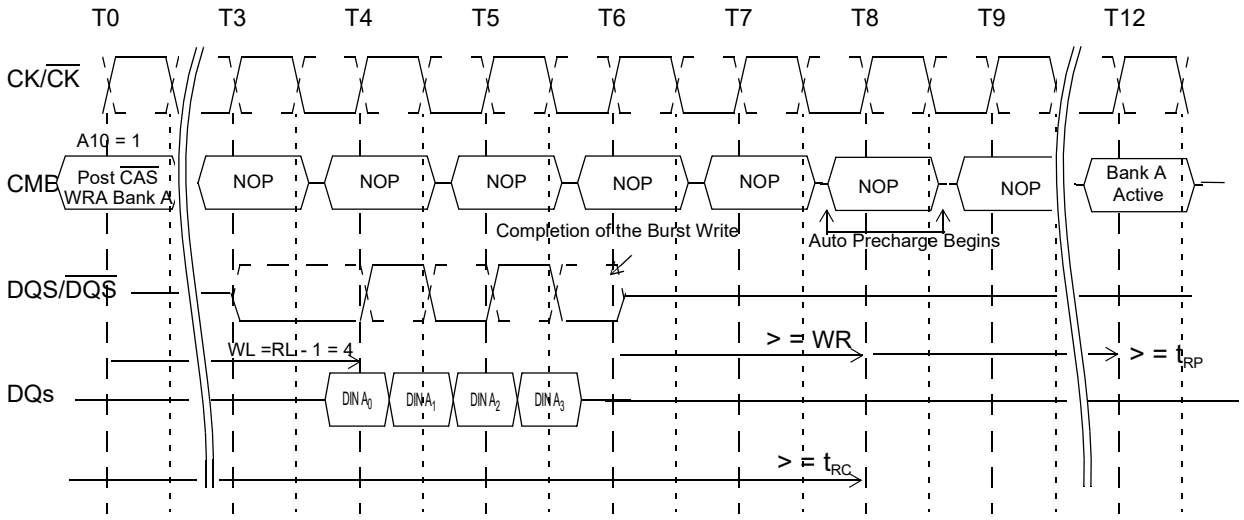


Figure 48 — Burst Write with Auto-Precharge (tWR + tRP): WL = 4, tWR =2, BL = 4, tRP=3

2.2.7 Refresh Command

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.
When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * tREFI.

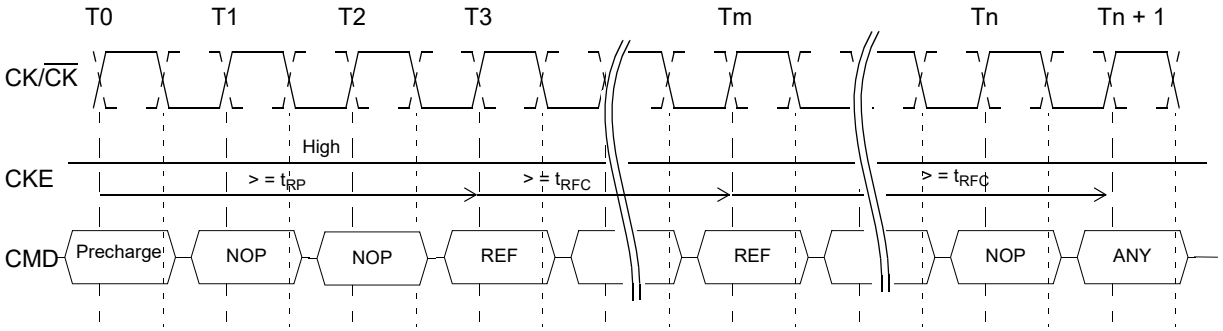
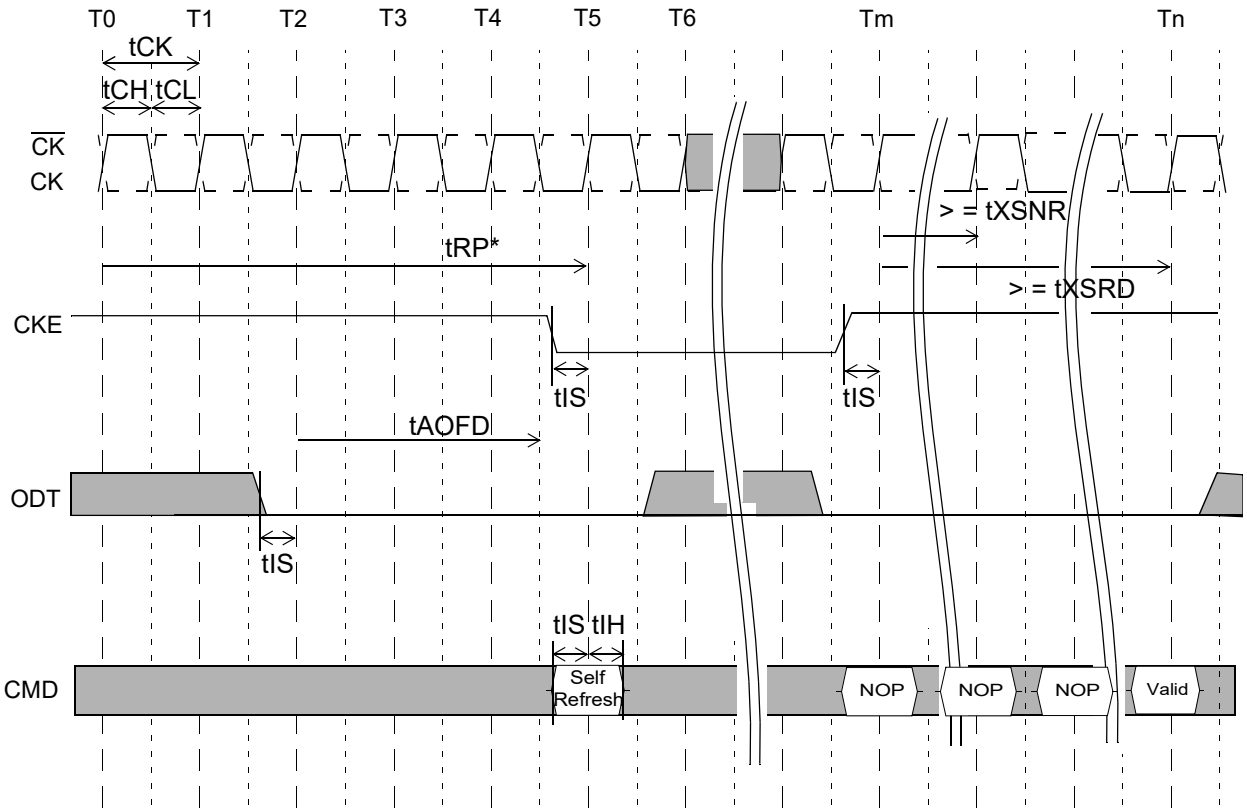


Figure 49 — Refresh Command

2.2.8 Self Refresh Operation

The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the Command is registered, CKE must be held low to keep the device in Self Refresh mode. When the DDR2 SDRAM has entered Self Refresh mode all of the external signals except CKE, are “don’t care”. The clock is internally disabled during Self Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation. Once Self Refresh Exit command is registered, a delay equal to or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self Refresh exit period tXSRD for proper operation. NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval. ODT should also be turned off during tXSRD.



- Device must be in the “All banks idle” state prior to entering Self Refresh mode.
- ODT must be turned off tAOFD before entering Self Refresh mode, and can be turned on again when tXSRD timing is satisfied.
- tXSRD is applied for a Read or a Read with autoprecharge command
- tXSNR is applied for any command except a Read or a Read with autoprecharge command.

Figure 50 — Self Refresh Operation

2.2.9 Power-Down

Power-down is synchronously entered when CKE is registered low (along with Nop or Deselect command). CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or autoprecharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 51 through 59 with details for entry into power down.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes high. Power-down exit latency is defined at AC spec table of this data sheet.

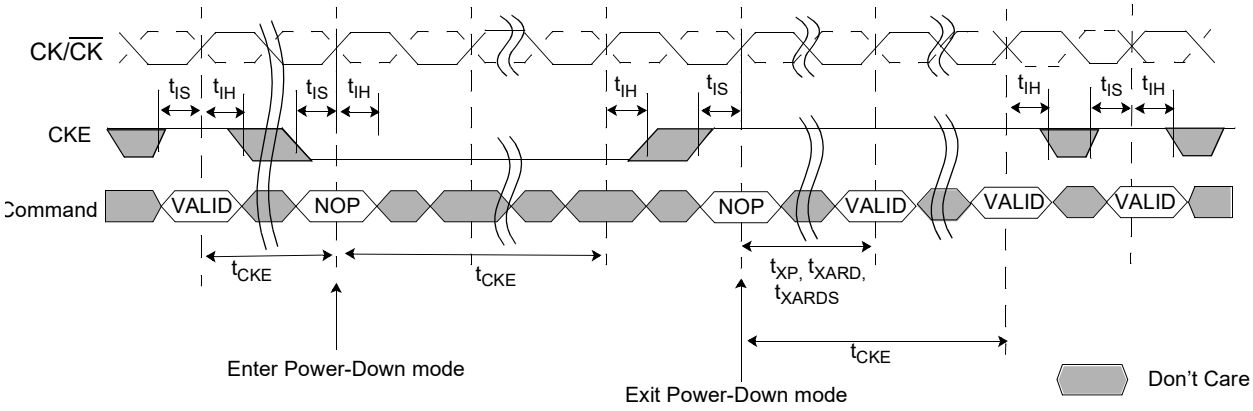


Figure 51 — Basic Power Down Entry and Exit Timing Diagram

2.2.9 Power-Down (cont'd)

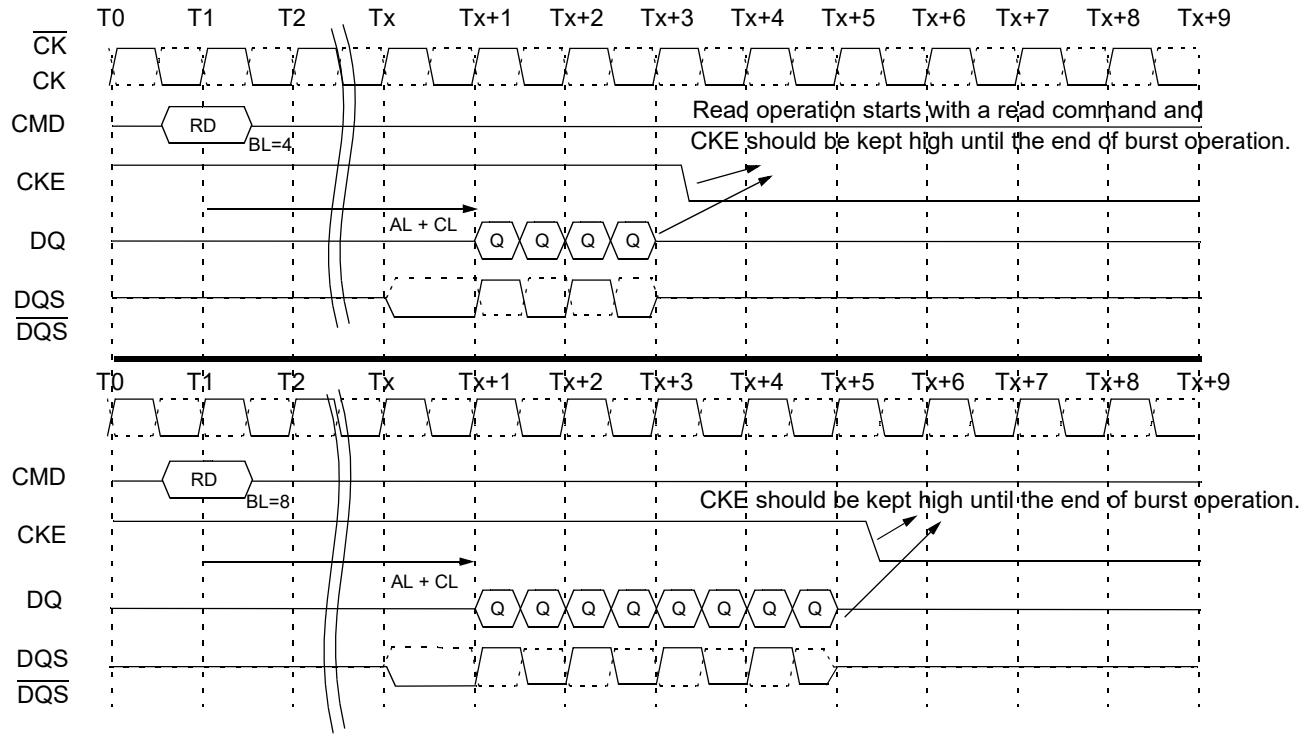


Figure 52 — Read to Power Down Entry

2.2.9 Power-Down (cont'd)

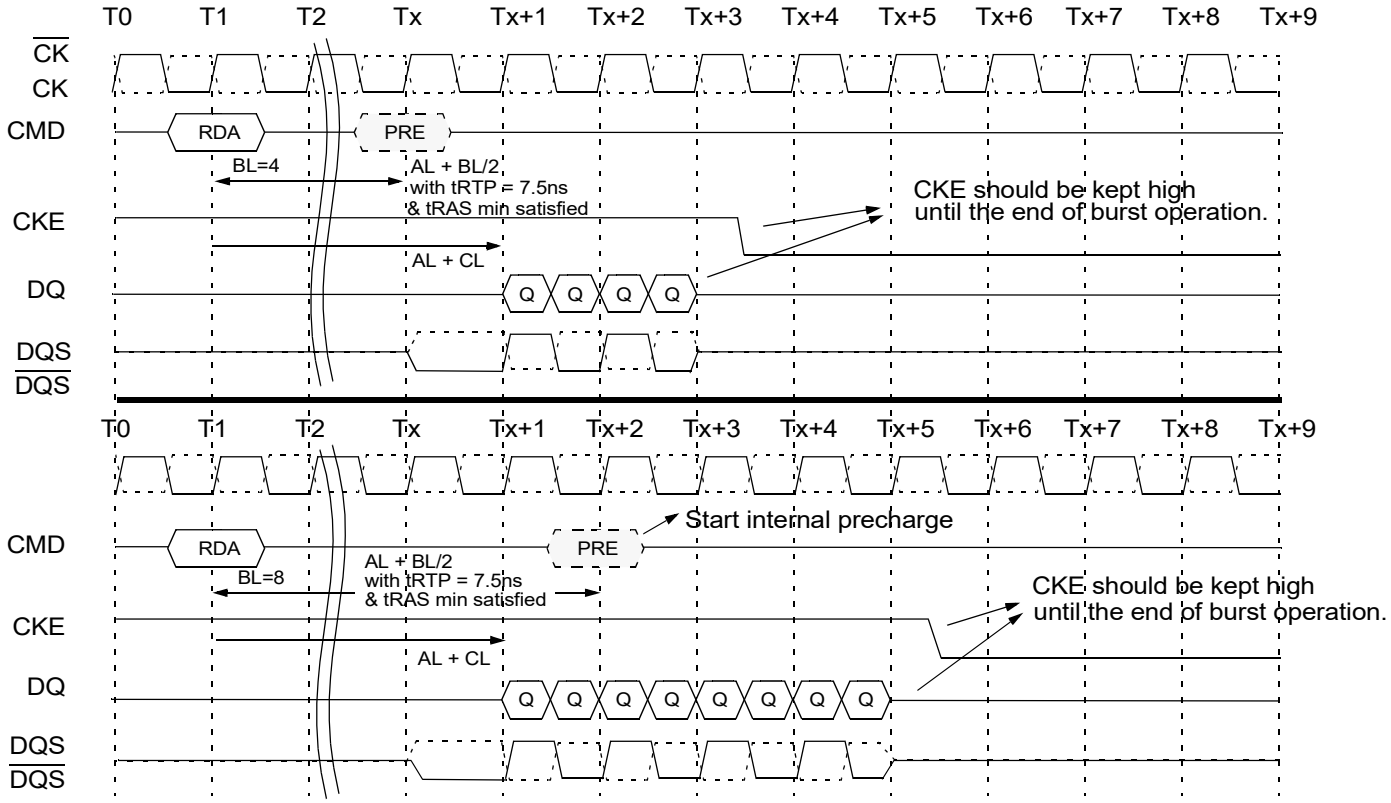


Figure 53 — Read with Autoprecharge to Power Down Entry

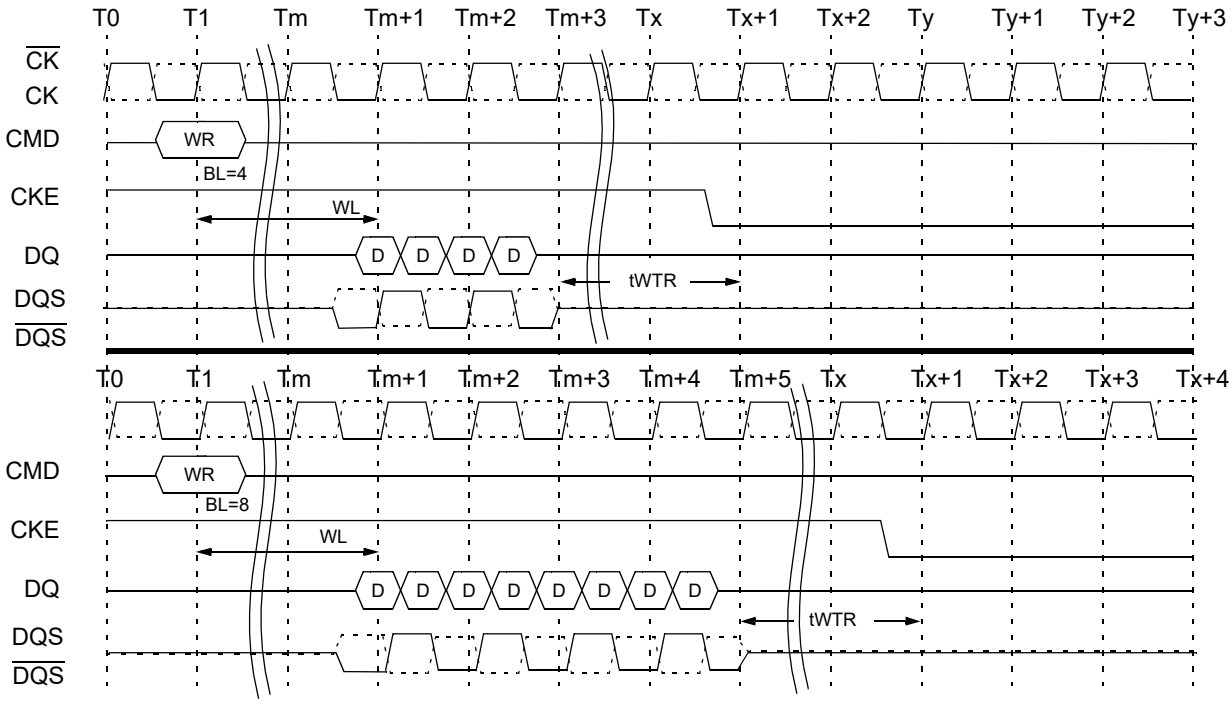


Figure 54 — Write to Power Down Entry

2.2.9 Power-Down (cont'd)

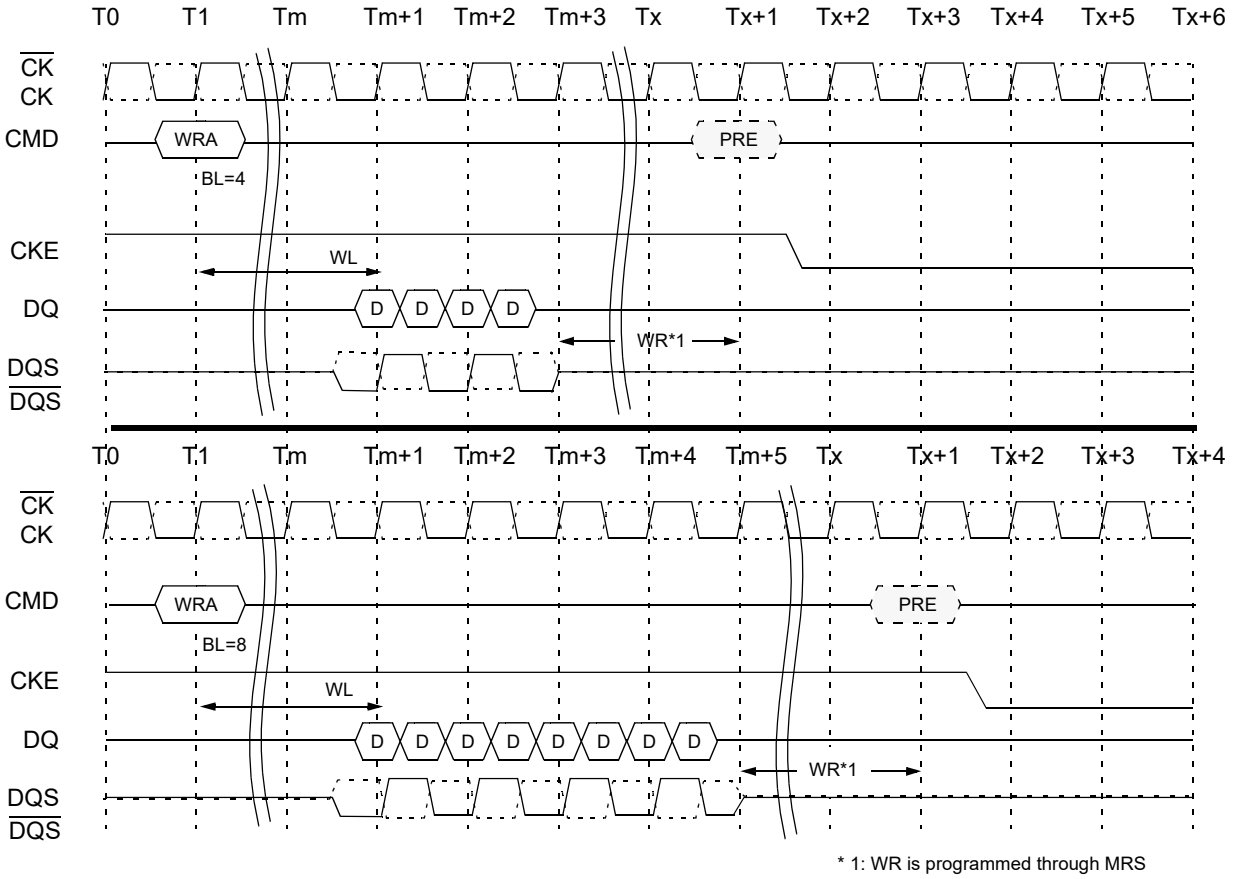


Figure 55 — Write with Autoprecharge to Power Down Entry

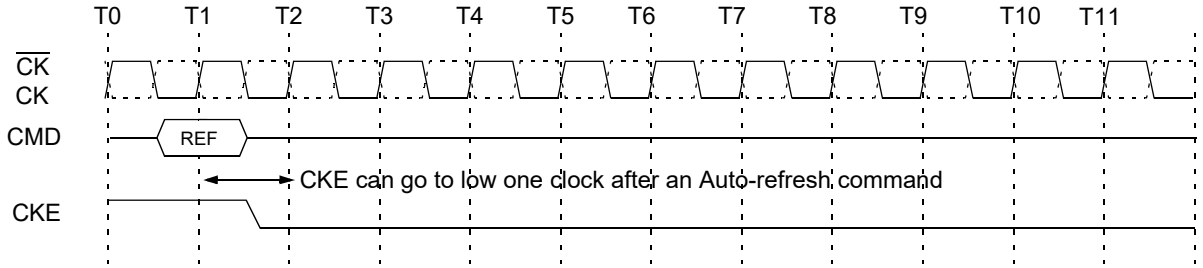


Figure 56 — Refresh Command to Power Down Entry

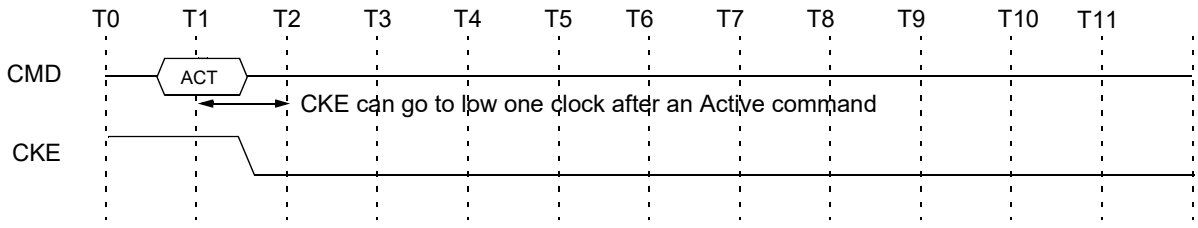


Figure 57 — Active Command to Power Down Entry

2.2.9 Power-Down (cont'd)

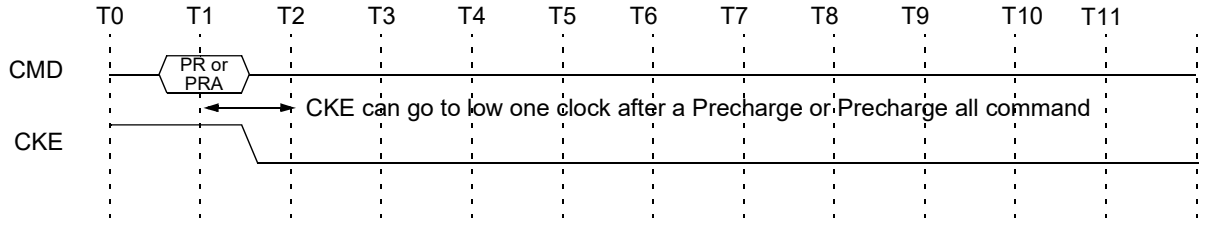


Figure 58 — Precharge/Precharge all Command to Power Down Entry

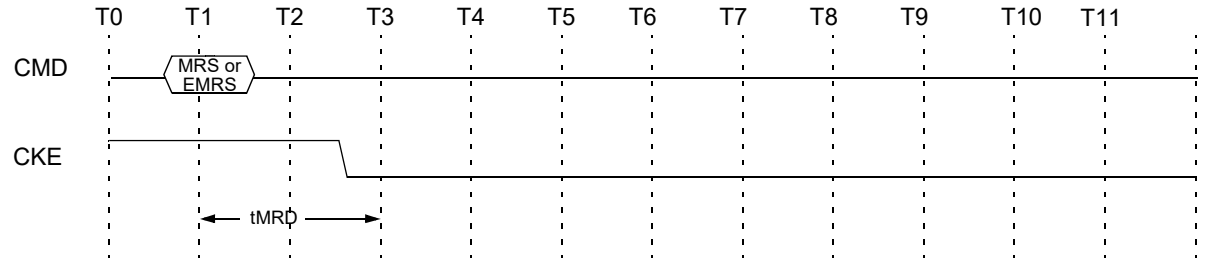


Figure 59 — MRS/EMRS Command to Power Down Entry

2.2.10 Asynchronous CKE Low Event

DRAM requires CKE to be maintained "HIGH" for all valid operations as defined in this data sheet. If CKE asynchronously drops "LOW" during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDelay before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised "HIGH" again. DRAM must be fully re-initialized (steps 4 thru 13) as described in initialization sequence. DRAM is ready for normal operation after the initialization sequence. See Table 35 for tDelay specification.

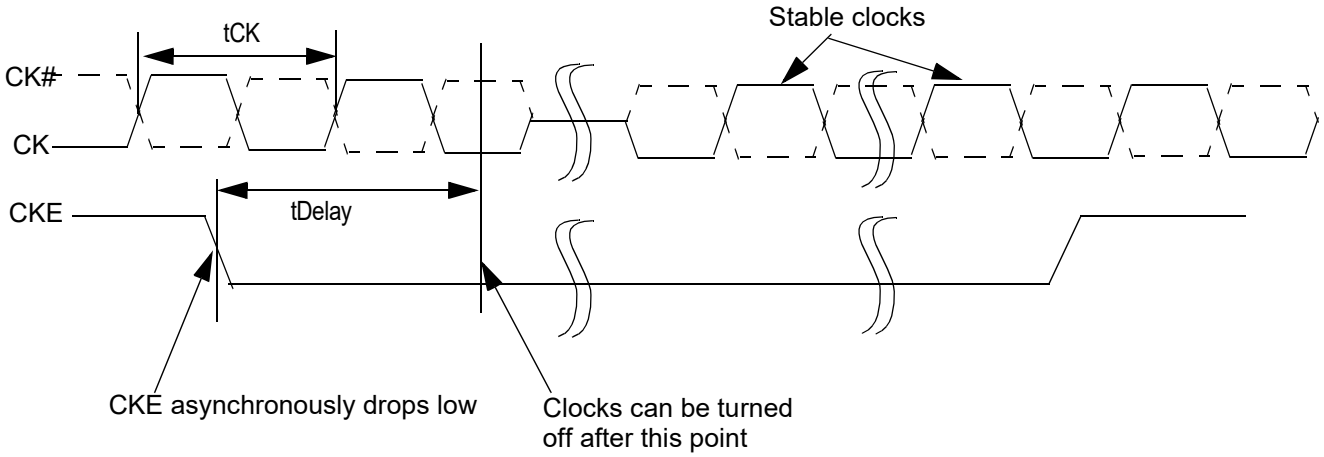


Figure 60 — Asynchronous CKE Low Event

2.2.11 Input Clock Frequency Change during Precharge Power Down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc. During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

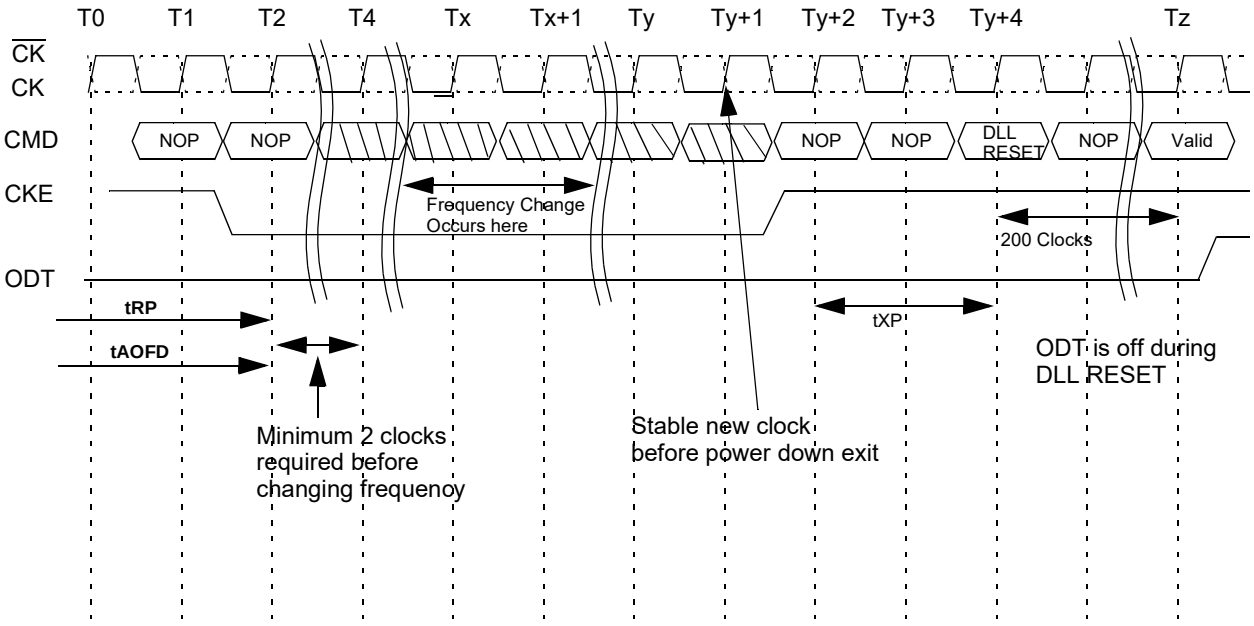


Figure 61 — Clock Frequency Change in Precharge Power Down Mode

2.2.12 No Operation Command

The No Operation command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A No Operation command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.2.13 Deselect Command

The Deselect command performs the same function as a No Operation command. Deselect command occurs when $\overline{CS}$ is brought high at the rising edge of the clock, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't cares.

3 Truth Tables

Operation or timing that is not specificed is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specficed initialization sequence before normal operation can continue.

Table 10 — Command Truth Table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 “X” means “H or L (but a defined logic level)”.

NOTE 7 Self refresh exit is asynchronous.

3 Truth Tables (cont'd)

Table 11 — Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [2]	CKE		Command (N) [3]	Action (N) [3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power Down Exit	4, 8, 11,13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5,9
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4, 8, 10,11,13
	H	L	REFRESH	Self Refresh Entry	6, 9, 11,13
	H	H	Refer to the Command Truth Table		7

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is the state of the DDR SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.

NOTE 6 Self Refresh mode can only be entered from the All Banks Idle state.

NOTE 7 Must be a legal command as defined in the Command Truth Table.

NOTE 8 Valid commands for Power Down Entry and Exit are NOP and DESELECT only.

NOTE 9 Valid commands for Self Refresh Exit are NOP and DESELECT only.

NOTE 10 Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See section 2.2.9 "Power Down" and 2.2.8 "Self Refresh Command" for a detailed list of restrictions.

NOTE 11 Minimum CKE high time is three clocks.; minimum CKE low time is three clocks.

NOTE 12 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 13 The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 14 CKE must be maintained high while the SDRAM is in OCD calibration mode.

NOTE 15 "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).

Table 12 — DM Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE 1 Used to mask write data, provided coincident with the corresponding data

4 Absolute Maximum DC Ratings

Operation or timing that is not specificed is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specficed initialization sequence before normal operation can continue.

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 AC & DC Operating Conditions

Operation or timing that is not specificed is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specficed initialization sequence before normal operation can continue.

Table 13 — Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	4
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	4, 5
VDD	Supply Voltage	2.3	2.5	2.7	V	4, 6
VDDL	Supply Voltage for DLL	2.3	2.5	2.7	V	4, 5, 6
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	5, 6
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	1.2
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically, the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).

NOTE 4 VTT of transmitting device must track VREF of receiving device.

NOTE 5 DDR2 parts with 2.5 V Vdd may exist in the market, but devices with 1.8 V Vdd are expected to be the preferred mass production parts

NOTE 6 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

NOTE 7 Note 5 does not apply when Vdd = 2.5 V nominal

5 AC & DC Operating Conditions (cont'd)

Table 14 — ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Deviation of VM with respect to VDDQ/2	delta VM	-3.75		+3.75	%	1

NOTE 1 Test condition for Rtt measurements

Measurement Definition for Rtt(eff): Apply V_{IH} (ac) and V_{IL} (ac) to test pin separately, then measure current I(V_{IH} (ac)) and I(V_{IL} (ac)) respectively. V_{IH} (ac), V_{IL} (ac), and VDDQ values defined in SSTL_18

$$Rtt(eff) = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$$\text{delta VM} = \left(\frac{2 \times Vm}{VDDQ} - 1 \right) \times 100\%$$

Table 15 — Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic high	VREF + 0.125	VDDQ + 0.3	V	
V_{IL}(dc)	dc input logic low	- 0.3	VREF - 0.125	V	

Table 16 — Input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (ac)	ac input logic high	VREF + 0.250	-	V	
V_{IL} (ac)	ac input logic low	-	VREF - 0.250	V	

Table 17 — AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
NOTE 2 The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
NOTE 3 AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

5 AC & DC Operating Conditions (cont'd)

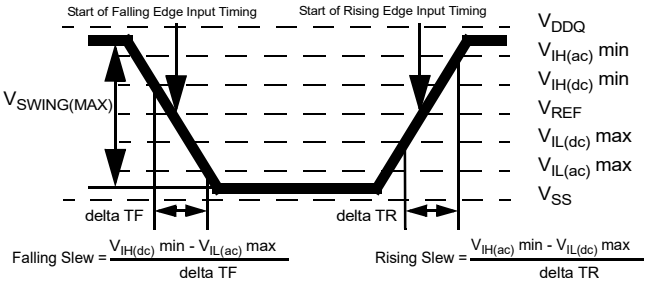


Figure 62 — AC Input Test Signal Waveform

Table 18 — Differential Input DC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IN} (dc)	dc differential signal voltage	-0.3	VDDQ + 0.3	V	1
V_{ID} (dc)	dc differential input voltage	0.25	VDDQ + 0.6	V	2

NOTE 1 VIN(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.

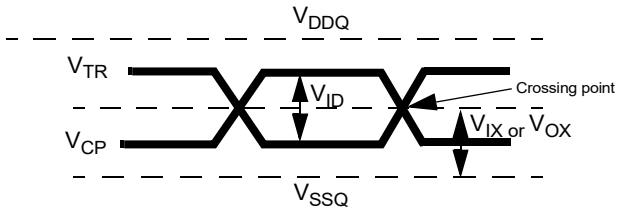
NOTE 2 VID(DC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to VIH(DC) - V IL(DC).

Table 19 — Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

NOTE 1 VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to VIH(AC) - V IL(AC).

NOTE 2 The typical value of VIX(DC) is excpected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.



NOTE 1 VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as CK, DQS, LDQS or UDQS). The minimum value is equal to V IH(AC) - V IL(AC).

NOTE 2 The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.

Figure 63 — Differential signal levels

5 AC & DC Operating Conditions (cont'd)

Table 20 — Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

NOTE 1 The typical value of VOX(AC) is expected to be about 0.5 * V DDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

Overshoot/Undershoot Specification

Table 21 — AC Overshoot/Undershoot Specification for Address and Control Pins A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT

Parameter	Specification		
	DDR2-400	DDR2-533	DDR2-667
Maximum peak amplitude allowed for overshoot area (See Figure 64):	0.9V	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 64):	0.9V	0.9V	0.9V
Maximum overshoot area above VDD (See Figure 64).	0.75 V-ns	0.56 V-ns	0.45 V-ns
Maximum undershoot area below VSS (See Figure 64).	0.75 V-ns	0.56 V-ns	0.45 V-ns

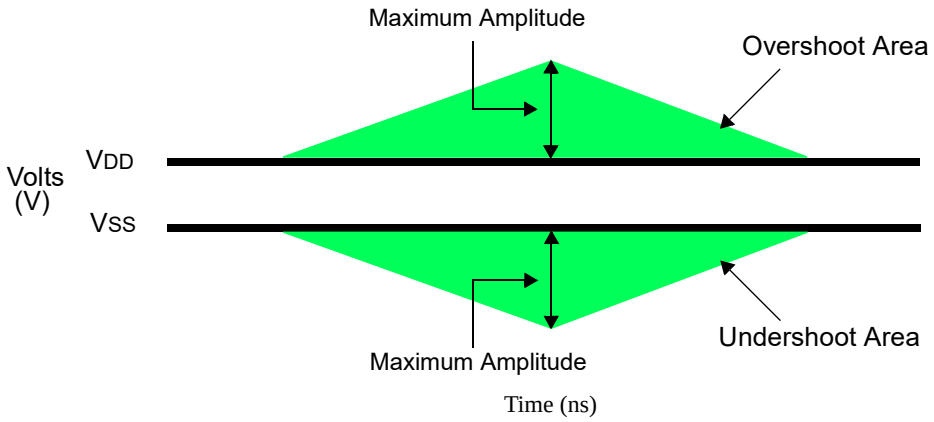


Figure 64 — AC Overshoot and Undershoot Definition for Address and Control Pins

Table 22 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe, and Mask Pins DQ, DQS, DM, CK, CK

Parameter	Specification		
	DDR2-400	DDR2-533	DDR2-667
Maximum peak amplitude allowed for overshoot area (See Figure 65):	0.9V	0.9V	0.9V
Maximum peak amplitude allowed for undershoot area (See Figure 65):	0.9V	0.9V	0.9V
Maximum overshoot area above VDDQ (See Figure 65).	0.38 V-ns	0.28 V-ns	0.23 V-ns
Maximum undershoot area below VSSQ (See Figure 65).	0.38 V-ns	0.28 V-ns	0.23 V-ns

5 AC & DC Operating Conditions (cont'd)

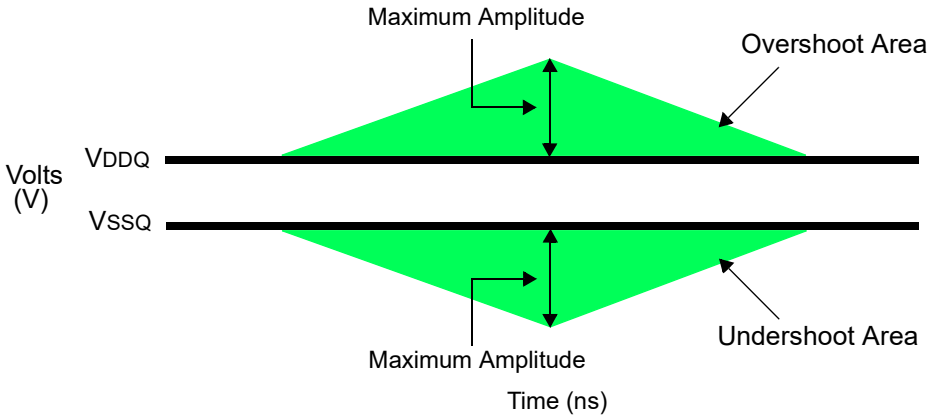


Figure 65 — AC Overshoot and Undershoot Definition for Clock, Data, Strobe, and Mask Pins

Power and ground clamps are required on the following input only pins:

1. BA0-BA2
2. A0-A15
3. $\overline{\text{RAS}}$
4. $\overline{\text{CAS}}$
5. $\overline{\text{WE}}$
6. $\overline{\text{CS}}$
7. ODT
8. CKE

Table 23 — Characteristics for Input Only Pins with Clamps

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

5 AC & DC Operating Conditions (cont'd)

Output Buffer Levels

Table 24 — Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

NOTE 1 The VDDQ of the device under test is referenced.

Table 25 — Output DC Current Drive

Symbol	Parameter	SSTl_18 Class II	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

NOTE 1 V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

NOTE 2 V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.

NOTE 3 The dc value of V_{REF} applied to the receiving device is set to V_{TT}

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Table 12) along a 21 ohm load line to define a convenient driver current for measurement.

Table 26 — OCD Default Characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		12.6	18	23.4	ohms	1,2
Output impedance for step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate		tbd		tbd	V/ns	1,4,5

NOTE 1 Absolute Specifications (0°C £ TCASE £ +tbd°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)

NOTE 2 Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.

NOTE 3 Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.

NOTE 4 Slew rate measured from vil(ac) to vih(ac).

NOTE 5 The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

NOTE 6 This represents the step size when the OCD is near 18 ohms at nominal conditions across all process and represents only the DRAM uncertainty. A zero-ohm value (no calibration) can only be achieved if the OCD impedance is 18 ohms ±0.75 ohms under nominal conditions.

5 AC & DC Operating Conditions (cont'd)

DDR2 SDRAM Default Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS1 bits A7-A9 = '111'. Figures 66 and 67 show the driver characteristics graphically, while Tables 26 and 27 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

- Nominal Default 25 °C (T case), VDDQ = 1.8 V, typical process
- Minimum TBD °C (T case), VDDQ = 1.7 V, slow–slow process
- Maximum 0 °C (T case), VDDQ = 1.9 V, fast–fast process

Default Output Driver Characteristic Curves Notes:

1. The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of the Figures.
2. It is recommended that the "typical" IBIS V–I curve lie within the inner bounding lines of the V–I curves of the Figures.

Table 27 — Full Strength Default Pulldown Driver Characteristics

	Pulldown Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8		37.9	60.9	99.1
1.9				101.1

5 AC & DC Operating Conditions (cont'd)

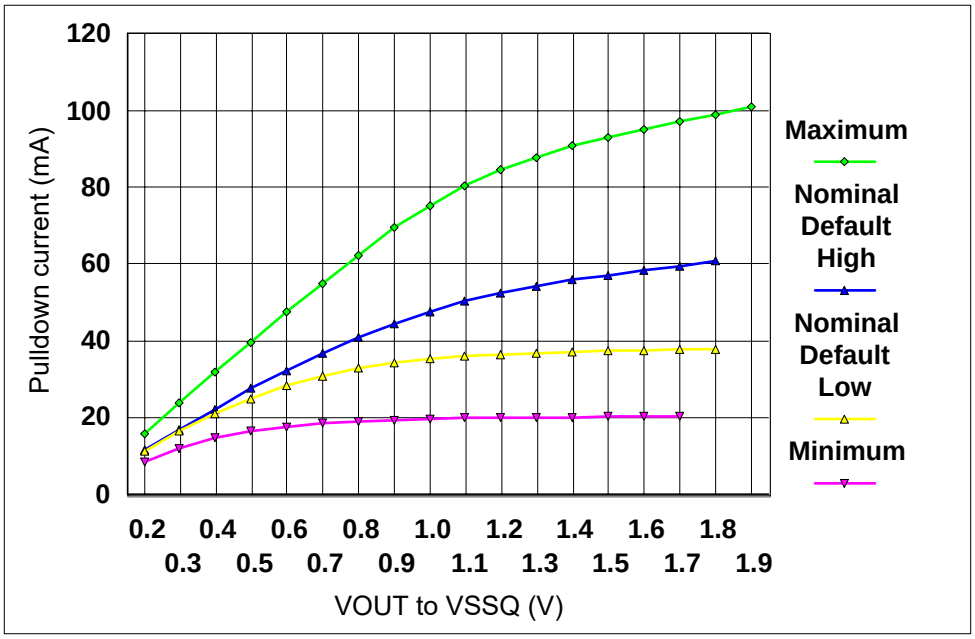


Figure 66 — DDR2 Default Pulldown Characteristics for Full Strength Driver

Table 28 — Full Strength Default Pullup Driver Characteristics

	Pullup Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	-8.5	-11.1	-11.8	-15.9
0.3	-12.1	-16.0	-17.0	-23.8
0.4	-14.7	-20.3	-22.2	-31.8
0.5	-16.4	-24.0	-27.5	-39.7
0.6	-17.8	-27.2	-32.4	-47.7
0.7	-18.6	-29.8	-36.9	-55.0
0.8	-19.0	-31.9	-40.8	-62.3
0.9	-19.3	-33.4	-44.5	-69.4
1.0	-19.7	-34.6	-47.7	-75.3
1.1	-19.9	-35.5	-50.4	-80.5
1.2	-20.0	-36.2	-52.5	-84.6
1.3	-20.1	-36.8	-54.2	-87.7
1.4	-20.2	-37.2	-55.9	-90.8
1.5	-20.3	-37.7	-57.1	-92.9
1.6	-20.4	-38.0	-58.4	-94.9
1.7	-20.6	-38.4	-59.6	-97.0
1.8		-38.6	-60.8	-99.1
1.9				-101.1

5 AC & DC Operating Conditions (cont'd)

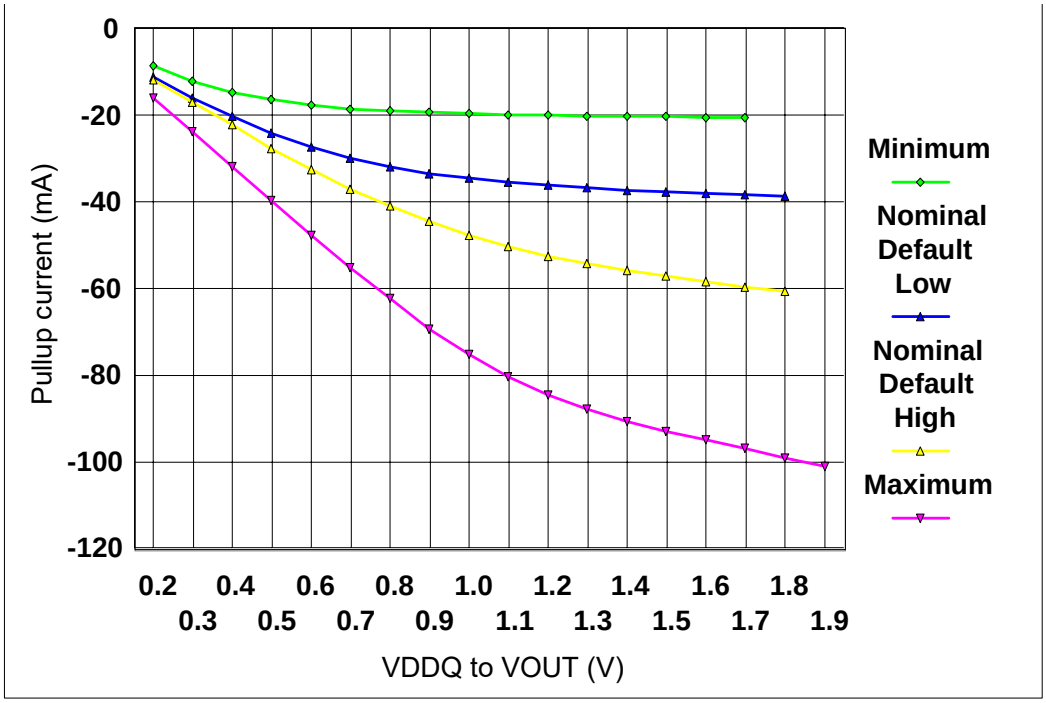


Figure 67 — DDR2 Default Pullup Characteristics for Full Strength Output Driver

DDR2 SDRAM Calibrated Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in Section 2.2.2.3, Off-Chip Driver (OCD) Impedance Adjustment. Tables 28 and 29 show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohm step size with no calibration error at the exact nominal conditions only (i.e., perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa. The driver characteristics evaluation conditions are:

- Nominal 25 ^{o}C (T case), VDDQ = 1.8 V, typical process
- Nominal Low and Nominal High 25 ^{o}C (T case), VDDQ = 1.8 V, any process
- Nominal Minimum TBD ^{o}C (T case), VDDQ = 1.7 V, any process
- Nominal Maximum 0 ^{o}C (T case), VDDQ = 1.9 V, any process

5 AC & DC Operating Conditions (cont'd)

Table 29 — Full Strength Calibrated Pulldown Driver Characteristics

	Calibrated Pulldown Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.25 ohms)	Nominal Maximum (15 ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

Table 30 — Full Strength Calibrated Pullup Driver Characteristics

	Calibrated Pullup Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.25 ohms)	Nominal Maximum (15 ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.7	-21.0	-21.2	-23.0	-27.0

Table 31 — IDD Specification Parameters and Test Conditions
(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

Symbol	Conditions	Max	Units	Notes
IDD0	**Operating one bank active-precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	

Table 31 — IDD Specification Parameters and Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

Symbol	Conditions		Max	Units	Notes
IDD2N	**Precharge standby current;** All banks idle; $^{t}CK = {}^{t}CK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD3P	**Active power-down current;** All banks open; $^{t}CK = {}^{t}CK(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0		mA	
		Slow PDN Exit MRS(12) = 1		mA	
IDD3N	**Active standby current;** All banks open; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RAS = {}^{t}RASmax(IDD)$, $^{t}RP = {}^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RAS = {}^{t}RASmax(IDD)$, $^{t}RP = {}^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RAS = {}^{t}RASmax(IDD)$, $^{t}RP = {}^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W			mA	
IDD5B	**Burst refresh current;** $^{t}CK = {}^{t}CK(IDD)$; Refresh command at every $^{t}RFC(IDD)$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING			mA	
IDD6	**Self refresh current;** CK and $\overline{CK}$ at 0V; CKE £ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING			mA	
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $^{t}RCD(IDD)-1*{}^{t}CK(IDD)$; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RC = {}^{t}RC(IDD)$, $^{t}RRD = {}^{t}RRD(IDD)$, $^{t}RCD = 1*{}^{t}CK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions			mA	

Table 31 — IDD Specification Parameters and Test Conditions
(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5

NOTE 1 IDD specifications are tested after the device is properly initialized

NOTE 2 Input slew rate is specified by AC Parametric Test Condition

NOTE 3 IDD parameters are specified with ODT disabled.

NOTE 4 Data bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS, and $\overline{\text{UDQS}}$. IDD values must be met with all combinations of EMRS bits 10 and 11.

NOTE 5 Definitions for IDD

LOW	=	Vin £ VILAC(max)
HIGH	=	Vin Š VIHAC(min)
STABLE	=	inputs stable at a HIGH or LOW level
FLOATING	=	inputs at VREF = VDDQ/2
SWITCHING	=	inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

IDD Testing Parameters

For purposes of IDD testing, the following parameters are to be utilized.

Table 32 — IDD Testing Parameters

	DDR2-667	DDR2-533			DDR2-400		
Parameter	**4-4-4**	**3-3-3**	**4-4-4**	**5-5-5**	**3-3-3**	**4-4-4**	**Units**
CL(IDD)	4	3	4	5	3	4	tCK
^{t}RCD(IDD)	12	11.25	15	18.75	15	20	ns
^{t}RC(IDD)	57	56.25	60	63.75	60	65	ns
^{t}RRD(IDD)-x4/x8	7.5	7.5	7.5	7.5	7.5	7.5	ns
^{t}RRD(IDD)-x16	10	10	10	10	10	10	ns
^{t}CK(IDD)	3	3.75	3.75	3.75	5	5	ns
^{t}RASmin(IDD)	45	45	45	45	45	45	ns
^{t}RASmax(IDD)	70000	70000	70000	70000	70000	70000	ns
^{t}RP(IDD)	12	11.25	15	18.75	15	20	ns
^{t}RFC(IDD)-256Mb	75	75	75	75	75	75	ns
^{t}RFC(IDD)-512Mb	105	105	105	105	105	105	ns
^{t}RFC(IDD)-1Gb	127.5	127.5	127.5	127.5	127.5	127.5	ns
^{t}RFC(IDD)-2Gb	197.5	197.5	197.5	197.5	197.5	197.5	ns

5 AC & DC Operating Conditions (cont'd)

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation
All banks are being interleaved at minimum ^{t}RC(IDD) without violating ^{t}RRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

Timing Patterns for 4 bank devices x4/ x8/ x16
-DDR2-400 4/4/4: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D D

-DDR2-400 3/3/3: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D

-DDR2-533 5/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

-DDR2-533 4/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D

Timing Patterns for 8 bank devices x4/x8
-DDR2-400 and DDR2-533 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

Timing Patterns for 8 bank devices x16
-DDR2-400 all bins: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

-DDR2-533 all bins: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D

Table 33 — Input/Output capacitance

Parameter	Symbol	DDR2-400 DDR2-533		DDR2-667 DDR2-800		Units
		Min	Max	Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	4.0	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	x	0.5	pF

Electrical Characteristics & AC Timing for DDR2-400/533/667 - Absolute Specification

(0 °C ≤ T_{CASE} ≤ xx °C; V_{DDQ} = 1.8V +/– 0.1V; V_{DD} = 1.8V +/– 0.1V)

Table 34 — Refresh Parameters by Device Density

Parameter	Symbol	256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC	75	105	127.5	195	tbd	ns
Average periodic refresh interval	tREFI	7.8	7.8	7.8	7.8	7.8	µs

Note: If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

5 AC & DC Operating Conditions (cont'd)

Table 35 — DDR2 SDRAM Standard Speed Bins and tRCD, tRP and tRC for Corresponding Bin

Speed	DDR2-667	DDR2-533	DDR2-533	DDR2-533	DDR2-400	DDR2-400	Units
Bin (CL - tRCD - tRP)	4 - 4 - 4	3 - 3 - 3	4 - 4 - 4	5 - 5 - 5	3 - 3 - 3	4 - 4 - 4	
Parameter	min	min	min	min	min	min	
$\overline{CAS}$ Latency	4	3	4	5	3	4	tCK
tRCD	12	11.25	15	18.75	15	20	ns
tRP Note1	12	11.25	15	18.75	15	20	ns
tRC	57	56.25	60	63.75	60	65	ns

NOTE 1 8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will be equal to tRP + 1 * tCK, where tRP are the values for a single bank pre-charge, which are shown in the above table.

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
DQ and DM input hold time	tDH	400	x	350	x	ps	6,7,8,18
DQ and DM input setup time	tDS	400	x	350	x	ps	6,7,8,18
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13
DQ hold skew factor	tQHS	x	450	x	400	ps	12

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
Write preamble setup time	tWPRES	0	x	0	x	ps	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.25	x	0.25	x	tCK	
Address and control input hold time	tIH	600	x	500	x	ps	5,7,9
Address and control input setup time	tIS	600	x	500	x	ps	5,7,9
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Active to precharge command	tRAS	45	70000	45	70000	ns	3
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	10	x	ns	4
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tCK	14
Internal write to read command delay	tWTR	10	x	7.5	x	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)
(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	^{t}CKE	3		3		tCK	
ODT turn-on delay	^{t}AOND	2	2	2	2	tCK	
ODT turn-on	^{t}AON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	^{t}AONPD	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	^{t}AOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

5 AC & DC Operating Conditions (cont'd)

Table 37 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-667		DDR2-SS800		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	450			ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	400			ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	3000	8000	2500		ps	15
DQ and DM input hold time	tDH		x		x	ps	6,7,18
DQ and DM input setup time	tDS		x		x	ps	6,7,18
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/$\overline{CK}$	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x		x		ps	13
DQ hold skew factor	tQHS	x		x	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
Write preamble setup time	tWPRES	0	x	0	x	ps	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.25	x	0.25	x	tCK	
Address and control input hold time	tIH		x		x	ps	5,7,9
Address and control input setup time	tIS		x		x	ps	5,7,9

Table 37 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)
(Refer to notes for information related to this table at the bottom)

Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Activate to precharge command	tRAS	45	70000		70000	ns	3
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP*	x	tWR+tRP*	x	tCK	14
Internal write to read command delay	tWTR	7.5	x	7.5		ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refreh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		TBD		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		tCK	
ODT turn-on delay	^{t}AOND	2	2	2	2	tCK	
ODT turn-on	^{t}AON	tAC(min)	tAC(max)+ 0.7	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	^{t}AONPD	tAC(min)+2	2tCK+tAC (max)+1	tAC(min)+2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	^{t}AOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns	17
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+2	2.5tCK+tAC (max)+1	tAC(min)+2	2.5tCK+tA C(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT Power Down Exit Latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	

Table 37 — Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800)

(Refer to notes for information related to this table at the bottom)

Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

General Notes, Which May Apply for all AC Parameters

NOTE 1 Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between VTT - 250 mV & VTT + 250 mV for single ended signals. For differential signals (e.g., DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input slew rate for single ended signals is measured from dc-level to ac-level: from VREF - 125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV and VREF - 250 mV for falling edges. For differential signals (e.g., CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV (250mV to -500 mV for falling edges).

c) VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

NOTE 2 DDR2 SDRAM AC timing reference load. Figure 68 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

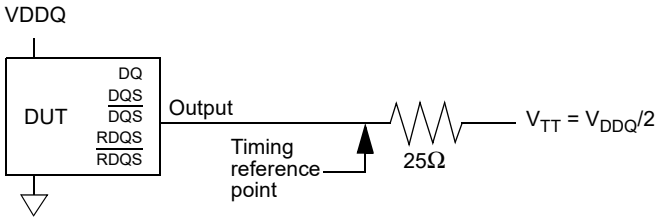


Figure 68 — AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g., DQS) and the complement (e.g., DQS) signal.

NOTE 3 DDR2 SDRAM output slew rate test load. Output slew rate is characterized under the test conditions as shown in Figure 69.

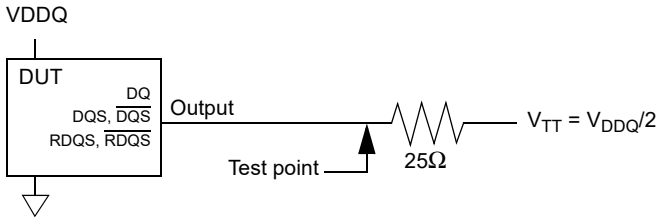


Figure 69 — Slew Rate Test Load

NOTE 4 Differential data strobe. DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. When differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10K Ω resistor to insure proper operation.

5 AC & DC Operating Conditions (cont'd)

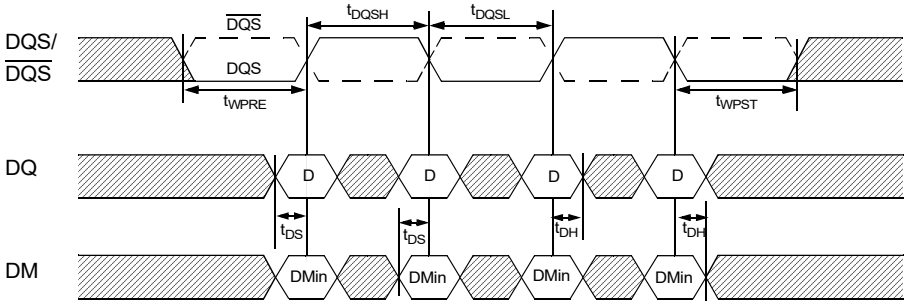


Figure 70 — Data Input (Write) Timing

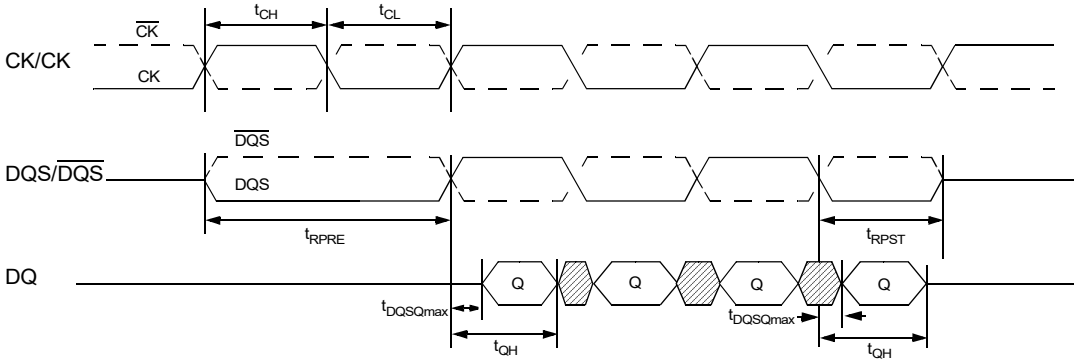


Figure 71 — Data Output (Read) Timing

NOTE 5 AC timings are for linear signal transitions. See System Derating for other signal transitions.

NOTE 6 These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

NOTE 7 All voltages referenced to VSS.

NOTE 8 Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/ supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for Dedicated AC Parameters

NOTE 1 User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

NOTE 2 AL = Additive Latency

NOTE 3 This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

NOTE 4 A minimum of two clocks (2 * tCK) is required irrespective of operating frequency

NOTE 5 Timings are guaranteed with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

NOTE 6 Timings are guaranteed with data, mask, and (DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ ns. See System Derating for other slew rate values.

NOTE 7 Timings are guaranteed with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.

Specific Notes for Dedicated AC Parameters Cont'd)

NOTE 8 tDS and tDH (data setup and hold) derating: TBD

NOTE 9 tIS and tIH (input setup and hold) derating: TBD

NOTE 10 The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

NOTE 11 MIN (t CL, t CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t CL and t CH). For example, t CL and t CH are = 50% of the period, less the half period jitter (t JIT(HP)) of the clock source, and less the half period jitter due to crosstalk (t JIT(crosstalk)) into the clock traces.

NOTE 12 t QH = t HP – t QHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).

tQHS accounts for:

a. The pulse duration distortion of on-chip clock circuits; and

b. The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

NOTE 13 tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

NOTE 14 t DAL = (nWR) + (tRP/tCK): For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period. nWR refers to the t WR parameter stored in the MRS.

Example: For DDR533 at t CK = 3.75 ns with t WR programmed to 4 clocks. tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 +(4)clocks=8clocks.

NOTE 15 The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in Section 2.2.9.

NOTE 16 ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

NOTE 17 ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

NOTE 18 If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

Annex A (informative) Differences between JESD79-2 and JESD79-2A

This table briefly describes most of the changes made to this standard, JESD79-2A, compared to its predecessor, JESD79-2 (September 2003). Some punctuation changes are not included.

Page	Description of Change
10	Per JCB-03-045 In Section 2.2.1, Power Up and Initialization Added second paragraph: “For DDR2SDRAMS...in any order.”
15	In Section 2.2.2.3, Off-Chip Driver (OCD) Impedance Adjustment Replaced “...the flow chart below...” with “...the flow chart in Figure 12...”
16	In paragraph **OCD Impedance Adjust**, Replaced “DTO in table X...” with “DTO in Table 7...”
49	Per JCB-02-130 Added text to Section 3, Truth Tables “Operation or timing that is not specified is illegal...before normal operation can continue.”
51	Per JCB-02-130 Added text to Section 4, Absolute Maximum DC Ratings “Operation or timing that is not specified is illegal...before normal operation can continue.”
51	Per JCB-02-130 Added text to Section 5, AC and DC Operating Conditions “Operation or timing that is not specified is illegal...before normal operation can continue.”
53	Per JCB-02-126 Added Table 18, Differential DC Input Logic Levels. Renumbered subsequent Tables. Paired the Notes with the appropriate Table.
56	Per JCB-03-080 Added to Table 26 - OCD Default Characteristics Entry: Output Impedancestep size for OCD calibration Note 6
63	Per JCB-03-076 Modfied Table 33 - Input/Output Capacitance Added columns for DDR2-667 and DDR2-800. Changed the Min value of CIO for DDR2-400 and DDR2-533 from 3.0 to 2.5
63	Per JCB-03-077 Modfied Table 33 - Input/Output Capacitance For DDR2-400 and DDR2-533: Changed the Min and Max values of CCK from 1.5 and 2.5 to 1.0 and 2.0. Changed the Min and Max values of CI from 1.5 and 2.5 to 1.0 and 2.0.
63	Per JCB-02-130 Added Note to Table 34 - Refresh Parameters by Device Density
64	Per JCB-02-130 In Table 36 - Timing Parmaeters by Speed Grade (DDR2-400 and DDR2-533) For tDH and tDS, added a reference to Note 18

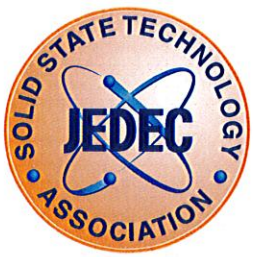
Annex A (informative) Differences between JESD79-2 and JESD79-2A

This table briefly describes most of the changes made to this standard, JESD79-2A, compared to its predecessor, JESD79-2 (September 2003). Some punctuation changes are not included.

Page	Description of Change
67	Per JCB-03-074 In Table 37 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800) For DDR2-667 Added Min and Max values for tAC: -450 ps and 450 ps Added Min and Max values for tDQSCK: -400 ps and 400 ps
67	Per JCB-02-130 In Table 37 - Timing Parmaeters by Speed Grade (DDR2-667 and DDR2-SS800) For tDH and tDS, added a reference to Note 18
68	Per JCB-03-073 In Table 37 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-SS800) For DDR2-667 Changed the Max value for tAON from tAC(max)+1 to tAC(max)+0.7
71	Per JCB-02-130 Added Note 18.
72	Updated Annex A


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Release 14

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JANUARY 2005

XILINX EXHIBIT 1010
Page 694

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CONFIGURATIONS FOR SOLID STATE MEMORIES

JEDEC Standard No. 21-C
Release 14

JANUARY 2005

JEDEC Solid State Technology Association

XILINX EXHIBIT 1010
Page 695

Contents

Section	Release #	Page #
1 BACKGROUND	Release 1	Page 1 - 1
2 TERMS AND DEFINITIONS	Release 1	Page 2 - 1
2.1 Conventional Device Pin Names	Release 9r10	Page 2 - 2
2.2 Multiport DRAM Pin Names	Release 3	Page 2 - 5
2.3 Power Pin Names	Release 9	Page 2 - 6
2.4 Device Type Names	Release 9r11	Page 2 - 7
2.5 Miscellaneous Device Related Terms	Release 1	Page 2 - 9
2.6 Special Operational Cycles for MPDRAM	Release 1	Page 2 - 10
2.7 Package-Related Terms	Release 5	Page 2 - 12
2.8 Memory Card Pin Names	Release 3	Page 2 - 13
2.9 SRAM and SSRAM special Pin Names	Release 6r11	Page 2-14
2.10 SLDRAM SPECIAL PIN NAMES	Release 9	Page 2-15
3 MEMORY DEVICE STANDARDS	Release 1	Page 3 - 1
3.1 General Standards	Release 1	Page 3 .1 -1
3.1.1 Bytewide	Release 1	Page 3 .1 -1
3.1.1.1 - 32K TO 256K BY 8 A/A MX FAMILY IN DIP	Release 1	Page 3 .1 -1
FIGURE 3.1-1, 32K TO 256K A/A MULTIPLEXED MEMORY IN DIP	Release 1	Page 3 .1 -2
3.2 Read Only Memory (ROM)	Release 1	Page 3.2-1
3.2.0 ROM General Standards	Release 5	Page 3.2-2
3.2.0.1 - Mask ROM Fast Address Mode Definition	Release 5	Page 3.2-2
3.2.1 ROM, Byte Wide	Release 1	Page 3.2.1-1
3.2.1.1 - 2K TO 8K BY 8 ROM FAMILY IN DIP, TYPE A	Release 1	Page 3.2.1-1
3.2.1.2 - 4K BY 8 ROM IN DIP, Type B	Release 1	Page 3.2.1-1
3.2.1.3 - 8K TO 128K BY 8 ROM FAMILY IN DIP,	Release 1	Page 3.2.1-1
3.2.1.4 - 2K TO 32K BY 8 ROM FAMILY IN RCC	Release 1	Page 3.2.1-1
3.2.1.5 - 32K TO 512K BY 8 ROM FAMILY IN SOJ,	Release 1	Page 3.2.1-1
3.2.1.6 - 128K TO 1M BY 8 ROM IN DIP,	Release 1	Page 3.2.1-1
3.2.1.7 - 64K TO 512K BY 9 ROM IN DIP,	Release 1	Page 3.2.1-1
3.2.1.8 - 2 TO 64 X 16K BY 8 PAGE SELECT ROM IN DIP,	Release 1	Page 3.2.1-1
3.2.1.9 - 512K and 1M BY 8 ROM IN QFP,	Release 2	Page 3.2.1-1
FIGURE 3.2.1-1, 2K TO 8K BY 8 ROM IN DIP, TYPES A & B	Release 1	Page 3.2.1-2
FIGURE 3.2.1-2, 8K TO 128K BY 8 ROM IN DIP	Release 1	Page 3.2.1-3
FIGURE 3.2.1-3, 2K TO 32K BY 8 ROM IN CC	Release 1	Page 3.2.1-4
FIGURE 3.2.1-4, 32K TO 512K BY 8 ROM IN SOJ	Release 1	Page 3.2.1-5
FIGURE 3.2.1-5, 128K TO 1M BY 8 ROM IN DIP	Release 1	Page 3.2.1-6
FIGURE 3.2.1-6, 64K TO 512K BY 9 ROM IN DIP	Release 1	Page 3.2.1-7
FIGURE 3.2.1-7, 2 TO 64 X 16K BY 8 PAGE SELECT	Release 1	Page 3.2.1-8
FIGURE 3.2.1-8, 512K AND 1M BY 8 ROM IN QFP	Release 2	Page 3.2.1-9
3.2.2 ROM, Word Wide	Release 1	Page 3.2.2-1
3.2.2.1 - 32K TO 256K BY 16 ROM IN DIP	Release 1	Page 3.2.2-3
3.2.2.2 - 32K TO 256K BY 16 ROM IN SCC	Release 1	Page 3.2.2-3
3.2.2.3 - 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN DIP	Release 1	Page 3.2.2-3
3.2.2.4 - 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN RCC	Release 1	Page 3.2.2-3
3.2.2.5 - 256K and 512K BY 16 ROM IN QFP	Release 2	Page 3.2.2-3
3.2.2.6 - 512K TO 128M BY 16 ROM IN DIP AND SOP	Release 6	Page 3.2.2-3
3.2.2.7 - 512K and 1M BY 16 ROM IN SCC	Release 3	Page 3.2.2-3

Section	Release #	Page #
FIGURE 3.2.2-1, 32K TO 256K BY 16 ROM IN DIP	Release 1	Page 3.2.2-5
FIGURE 3.2.2-2, 32K TO 256K BY 16 ROM IN CC	Release 1	Page 3.2.2-6
FIGURE 3.2.2-3, 16K TO 256K BY 16 AQ MX ROM IN DIP	Release 1	Page 3.2.2-7
FIGURE 3.2.2-4, 16K TO 256K BY 16 AQ MX ROM IN CC	Release 1	Page 3.2.2-8
FIGURE 3.2.2-5, 256K AND 512K BY 16 ROM IN QFP	Release 2	Page 3.2.2-9
FIGURE 3.2.2-6, 4M TO 128M BY 16 ROM IN DIP AND SOP	Release 2	Page 3.2.2-10
FIGURE 3.2.2-7, 512K & 1M BY 16 ROM IN SCC	Release 3	Page 3.2.2-11
FIGURE 3.2.2-8, 512K TO 2M BY 16 ROM IN DIP AND SOG	Release 6	Page 3.2.2-12
3.3 Programmable Read Only Memory (PROM)	**Release 1**	**Page 3.3-1**
3.3.1 PROM, Nibble Wide	**Release 1**	**Page 3.3.1-1**
3.3.1.1 - .25K & .5K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1-3
3.3.1.2 - .25K BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1-3
3.3.1.3 - 1K & 2K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1-3
3.3.1.4 - 1K & 2K BY 4 TTL PROM IN SOP	Release 1	Page 3.3.1-3
3.3.1.5 - 4K TO 8K BY 4 TTL PROM IN DIP	Release 2	Page 3.3.1-3
3.3.1.6 - .25K TO 2K BY 4 TTL PROM FAMILY IN RCC	Release 1	Page 3.3.1-3
3.3.1.7 - 4K BY 4 TTL PROM, 4K BY 4 TTL RPROM IN SCC	Release 1	Page 3.3.1-3
3.3.1.8 - 1K TO 8K TTL BY 4 PROM FAMILY IN RCC	Release 1	Page 3.3.1-3
3.3.1.9 - 1K TO 8K TTL BY 4 PROM FAMILY IN SCC	Release 1	Page 3.3.1-3
3.3.1.10 - 1K TO 4K BY 4 DPROM FAMILIES IN DIP & SCC	Release 1	Page 3.3.1-4
3.3.1.11 - 1K TO 16K BY 4 ECL PROM FAMILY IN DIP	Release 1	Page 3.3.1-4
FIGURE 3.3.1-1, .25K TO 2K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1-5
FIGURE 3.3.1-2, 256 BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1-6
FIGURE 3.3.1-3, 1K & 2K BY 4 TTL PROM IN SOG	Release 1	Page 3.3.1-7
FIGURE 3.3.1-4, 4K AND 8K BY 4 TTL PROM IN DIP	Release 2	Page 3.3.1-8
FIGURE 3.3.1-5, .25K TO 4K BY 4 TTL PROM FAMILY IN CC	Release 1	Page 3.3.1-9
FIGURE 3.3.1-6, 1K TO 8K BY 4 TTL PROM IN RCC	Release 1	Page 3.3.1-10
FIGURE 3.3.1-7, 1K TO 8K BY 4 TTL PROM IN SCC	Release 1	Page 3.3.1-11
FIGURE 3.3.1-8, 1K TO 4K BY 4 TTL DPROM IN DIP	Release 1	Page 3.3.1-12
FIGURE 3.3.1-9, 1K TO 4K BY 4 DPROM IN CC	Release 1	Page 3.3.1-13
FIGURE 3.3.1-10, 1K TO 16K BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1-14
3.3.2 PROM, Bytewide	**Release 1**	**Page 3.3.2-1**
3.3.2.1 - 32 BY 8 TTL PROM IN DIP & SCC	Release 1	Page 3.3.2-3
3.3.2.2 - 32 BY 8 ECL PROM IN DIP & SCC	Release 1	Page 3.3.2-3
3.3.2.3 - .25K & .5K BY 8 TTL PROM IN DIP & SCC	Release 1	Page 3.3.2-3
3.3.2.4 - .25K TO 8K BY 8 TTL PROM FAMILY IN DIP	Release 1	Page 3.3.2-3
3.3.2.5 - .5K TO 4K BY 8 TTL LPROM FAMILY IN DIP	Release 1	Page 3.3.2-3
3.3.2.6 - .5K TO 4K BY 8 TTL RPROM FAMILY IN DIP	Release 1	Page 3.3.2-3
3.3.2.7 - .5K TO 8K BY 8 TTL PROM FAMILIES IN RCC & SCC	Release 1	Page 3.3.2-3
3.3.2.8 - .5K TO 2K BY 8 TTL RPROM FAMILY IN SCC	Release 1	Page 3.3.2-4
3.3.2.9 - 16K TO 64K BY 8 TTL PROM FAMILY IN DIP	Release 1	Page 3.3.2-4
3.3.2.10 - 512 BY 8 ECL RPROM IN DIP & SCC	Release 2	Page 3.3.2-4
FIGURE 3.3.2-1, 32 BY 8 TTL & ECL PROM IN DIP	Release 1	Page 3.3.2-5
FIGURE 3.3.2-2, 32, 256, & 512 BY 8 TTL PROM IN CC, 32 BY 8 ECL PROM IN CC	Release 1	Page 3.3.2-6
FIGURE 3.3.2-3, 256 & 512 BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2-7
FIGURE 3.3.2-4, .25K TO 8K BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2-8
FIGURE 3.3.2-5, .5K TO 4K BY 8 TTL LPROM IN DIP	Release 1	Page 3.3.2-9
FIGURE 3.3.2-6, .5K TO 4K BY 8 TTL RPROM IN DIP	Release 1	Page 3.3.2-10
FIGURE 3.3.2-7, .5K TO 8K BY 8 TTL PROM IN SCC	Release 1	Page 3.3.2-11
FIGURE 3.3.2-8, .5K TO 8K BY 8 TTL PROM IN RCC	Release 1	Page 3.3.2-12
FIGURE 3.3.2-9, .5K TO 2K BY 8 RPROM IN CC	Release 1	Page 3.3.2-13

Section	Release #	Page #
FIGURE 3.3.2-10, 16K TO 64K BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2-14
FIGURE 3.3.2-11, 512 BY 8 10K & 100K ECL RPROM IN DIP AND SCC	Release 2	Page 3.3.2-15
3.3.3 PROM, Word Wide	**Release 1**	**Page 3.3.3-1**
3.3.3.1 - 32 AND 64 BY 16 PROM IN DIP AND SCC	Release 1	Page 3.3.3-3
FIGURE 3.3.3-1, 32 AND 64 BY 16 TTL PROM IN DIP	Release 1	Page 3.3.3-5
FIGURE 3.3.3-2, 32 AND 64 BY 16 TTL PROM IN CC	Release 1	Page 3.3.3-6
3.3.4 PROM Package Conversion	**Release 1**	**Page 3.3.4-1**
3.3.4.1 - PROM DIP TO SO CONVERSION, 16, 18, 20, 24 DIP	Release 1	Page 3.3.4-1
FIGURE 3.3.4-1, 1K AND 2K TTL PROM 18 DIP TO 20 SO CONVERSION	Release 1	Page 3.3.4-3
3.4 Erasable Programmable Read Only Memory (EPROM)	**Release 1**	**Page 3.4-1**
3.4.1 EPROM, Byte Wide	**Release 1**	**Page 3.4.1-1**
3.4.1.1 - 4K BY 8 EPROM IN DIP, TYPE A	Release 1	Page 3.4.1-3
3.4.1.2 - 4K AND 8K BY 8 EPROM IN DIP,	Release 1	Page 3.4.1-3
3.4.1.3 - 8K TO 64K BY 8 EPROM FAMILY IN DIP,	Release 1	Page 3.4.1-3
3.4.1.4 - 2K TO 512K BY 8 EPROM FAMILY IN RCC	Release 1	Page 3.4.1-3
3.4.1.5 - 32K TO 512K BY 8 EPROM FAMILY IN SOJ;	Release 1	Page 3.4.1-3
3.4.1.6 - 128K TO 1M BY 8 EPROM FAMILY IN DIP,	Release 1	Page 3.4.1-3
3.4.1.7 - 64K TO 512K BY 9 EPROM FAMILY IN DIP,	Release 1	Page 3.4.1-3
3.4.1.8 - 2 TO 64 X 16K BY 8 PAGE SELECT EPROM FAMILY IN DIP,	Release 1	Page 3.4.1-3
3.4.1.9 - 128K TO 512K BY 8 EPROM FAMILY IN TSOP-1,	Release 4	Page 3.4.1-3
FIGURE 3.4.1-1, 4K AND 8K BY 8 EPROM IN DIP, TYPES A & B	Release 1	Page 3.4.1-5
FIGURE 3.4.1-2, 8K TO 64K BY 8 EPROM IN DIP	Release 1	Page 3.4.1-6
FIGURE 3.4.1-3, 2K TO 512K BY 8 EPROM IN CC	Release 1	Page 3.4.1-7
FIGURE 3.4.1-4, 32K TO 512K BY 8 EPROM IN SOJ	Release 1	Page 3.4.1-8
FIGURE 3.4.1-5, 128K TO 1M BY 8 EPROM IN DIP	Release 1	Page 3.4.1-9
FIGURE 3.4.1-6, 64K TO 512K BY 9 EPROM IN DIP	Release 1	Page 3.4.1-10
FIGURE 3.4.1-7, 2 TO 64 X 16K BY 8 PAGE SELECT EPROM IN DIP	Release 1	Page 3.4.1-11
FIGURE 3.4.1-8, 128K TO 512K BY 8 EPROM IN TSOP-1	Release 4	Page 3.4.1-12
3.4.2 EPROM, Word Wide	**Release 1**	**Page 3.4.2-1**
3.4.2.1 - 32K TO 256K BY 16 EPROM IN DIP	Release 1	Page 3.4.2-3
3.4.2.2 - 32K TO 256K BY 16 EPROM IN SCC	Release 1	Page 3.4.2-3
3.4.2.3 - 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP	Release 1	Page 3.4.2-3
3.4.2.4 - 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC	Release 1	Page 3.4.2-3
3.4.2.5 - 512K TO 128M BY 16 EPROM or OTP IN DIP AND SOP	Release 6	Page 3.4.2-3
3.4.2.6 - 512K and 1M BY 16 EPROM IN SCC	Release 3	Page 3.4.2-3
3.4.2.7 - 64K TO 256K BY 16 EPROM IN TSOP-1	Release 4	Page 3.4.2-3
FIGURE 3.4.2-1, 32K TO 256K BY 16 EPROM IN DIP	Release 1	Page 3.4.2-5
FIGURE 3.4.2-2, 32K TO 256K BY 16 EPROM IN SCC	Release 1	Page 3.4.2-6
FIGURE 3.4.2-3, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP	Release 1	Page 3.4.2-7
FIGURE 3.4.2-4, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC	Release 1	Page 3.4.2-8
FIGURE 3.4.2-5, 4M TO 128M BY 16 EPROM OR OTP IN DIP AND SOP	Release 1	Page 3.4.2-9
FIGURE 3.4.2-6, 512K & 1M BY 16 EPROM IN CC	Release 3	Page 3.4.2-10
FIGURE 3.4.2-7, 64K BY 256K BY 16 EPROM IN TSOP-1	Release 4	Page 3.4.2-11
FIGURE 3.4.2-8, 512K TO 2M BY 16 EPROM IN DIP AND SOG	Release 6	Page 3.4.2-12
3.5 Electrically Erasable Programmable Read Only Memory (EEPROM)	**Release 1**	**Page 3.5-1**
3.5.1 EEPROM, Byte Wide	**Release 1**	**Page 3.5.1-1**
3.5.1.1 - .5K TO 2K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-2
3.5.1.2 - 2K & 4K BY 8 EEPROM IN RCC	Release 1	Page 3.5.1-2
3.5.1.3 - 1K TO 32K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-2
3.5.1.4 - .5K TO 32K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1-2

Release 14

XILINX EXHIBIT 1010
Page 698

Section	Release #	Page #
3.5.1.5 - 32K TO 256K BY 8 EEPROM FAMILY IN SOJ,	Release 1	Page 3.5.1-2
3.5.1.6 - 32K TO 512K BY 8 EEPROM FAMILY IN DIP,	Release 1	Page 3.5.1-2
3.5.1.7 - 32K TO 256K BY 8 EEPROM FAMILY IN RCC,	Release 1	Page 3.5.1-2
3.5.1.8 - 32K TO 256K BY 9 EEPROM FAMILY IN DIP,	Release 1	Page 3.5.1-2
3.5.1.9 - 128K TO 1M BY 8 EEPROM FAMILY IN SCC,	Release 1	Page 3.5.1-2
3.5.1.10 - 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1	Release 2	Page 3.5.1-3
3.5.1.11 - EXTENDED FEATURE SET FOR 256K BIT EEPROM	Release 2	Page 3.5.1-3
3.5.1.12 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM	Release 3	Page 3.5.1-3
3.5.1.13 - 512K BY 8 DUAL-SUPPLY EEPROM IN RCC	Release 5	Page 3.5.1-3
3.5.1.14 - 128K to 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP1	Release 5	Page 3.5.1-3
3.5.1.15 - 256K, 512K, &1M BY 8 DUAL-SUPPLY EEPROM IN TSOP1	Release 6	Page 3.5.1-4
3.5.1.16 - 1M TO 8M BY 8 SINGLE-SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1-4
3.5.1.17 - 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2	Release 6	Page 3.5.1-4
3.5.1.18 - 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP2	Release 7	Page 3.5.1-4
3.5.1.19 - 4Mb TO 32Mb DENSITY BY 8 Dual Supply Flash EEPROM in 8 X 5 GRID Micro BGA Package	Release 9	Page 3.5.1-4
3.5.1.20 - 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG	Release 9	Page 3.5.1-4
3.5.1.21 - 2-WIRE EEPROM IN SMALL FOOTPRINT PACKAGE	Release 14	Page 3.5.1-4
FIGURE 3.5.1-1, .5K TO 2K BY 8 EEPROM IN DIP	Release 1	Page 3.5.1-5
FIGURE 3.5.1-2, 2K & 4K BY 8 EEPROM IN RCC	Release 1	Page 3.5.1-6
FIGURE 3.5.1-3, 1K TO 32K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-7
FIGURE 3.5.1-4, .5K TO 32K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1-8
FIGURE 3.5.1-5, 32K TO 256K BY 8 EEPROM FAMILY IN SOJ	Release 1	Page 3.5.1-9
FIGURE 3.5.1-6, 32K TO 512K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-10
FIGURE 3.5.1-7, 32K TO 256K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1-11
FIGURE 3.5.1-8, 32K TO 256K BY 9 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-12
FIGURE 3.5.1-9, 128K TO 1M BY 8 EEPROM FAMILY IN SCC	Release 1	Page 3.5.1-13
FIGURE 3.5.1-10, 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1	Release 2	Page 3.5.1-14
ADDENDUM 1, 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARD	Release 2	Page 3.5.1-15
FIGURE 3.5.1-11, DUAL SUPPLY EEPROM COMMAND SET	Release 3	Page 3.5.1-23
FIGURE 3.5.1-12, 512K BY 8 DUAL-SUPPLY EEPROM IN RCC	Release 5	Page 3.5.1-24
FIGURE 3.5.1-13, 128K to 512K SINGLE-SUPPLY EEPROM FAMILY IN DIP	Release 5	Page 3.5.1-25
FIGURE 3.5.1-14, 128K to 512K SINGLE-SUPPLY EEPROM FAMILY IN RCC	Release 5	Page 3.5.1-26
FIGURE 3.5.1-15, 128K to 512K SINGLE-SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1-27
FIGURE 3.5.1-16, 1M BY 8 DUAL-SUPPLY EEPROM IN TSOP1	Release 5	Page 3.5.1-28
FIGURE 3.5.1-17. 1M TO 8M SINGLE-SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1-29
FIGURE 3.5.1-18, 256K & 512K BY 8 DUAL-SUPPLY EEPROM IN TSOP1	Release 6	Page 3.5.1-30
FIGURE 3.5.1-19 A⇒C 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2	Release 6	Page 3.5.1-31⇒33
FIGURE 3.5.1-20. 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP1	Release 7	Page 3.5.1-34
FIGURE 3.5.1-512K TO 4096K X 8 Dual Supply Flash EEPROM IN 8 X 5 GRID Micro BGA Package	Release 9	Page 3.5.1-35
FIGURE 3.5.1-22 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG	Release 9	Page 3.5.1-36
FIGURE 3.5.1-23 2-WIRE EEPROM, MLP 2X3 MM PINOUT	Release 14	Page 3.5.1-37
3.5.2 EEPROM, Word Wide	**Release 1**	**Page 3.5.2-1**
3.5.2.1 - 4K TO 32K BY 16 EEPROM IN DIP	Release 1	Page 3.5.2-2
3.5.2.2 - 4K TO 256K BY 16 EEPROM IN SCC	Release 1	Page 3.5.2-2
3.5.2.3 - 256K TO 128M BY 16 EEPROM IN DIP AND SOG	Release 6	Page 3.5.2-2
3.5.2.4 - 1M TO 4M BY 16 DS EEPROM IN SSOP	Release 6	Page 3.5.2-2
3.5.2.5 - 1M TO 4M DENSITY, BY 8 OR 16 FEEPROM IN PSOP	Release 7	Page 3.5.2-2
3.5.2.6 - 1M TO 32M DENSITY, BY 8 OR 16 FEEPROM IN TSOP1	Release 7	Page 3.5.2-2
3.5.2.7 - 4Mb TO 32Mb DENSITY BY 8 & 16 Dual Supply Flash EEPROM in 8 X 6 GRID Micro BGA Package	Release 9	Page 3.5.2-2

Release 14

XILINX EXHIBIT 1010
Page 699

Section	Release #	Page #
3.5.2.8 - 16Mb TO 64Mb DENSITY BY 8 & 16, Dual supply Flash EEPROM in 8 X 9 GRID Micro BGA Package	Release 9	Page 3.5.2-3
3.5.2.9 - 8Mb TO 128Mb Density FEEPROM/SRAM in BGA	Release 10	Page 3.5.2-3
3.5.2.10 - 4M TO 64M BY 16 FEEPROM IN TSOP1	Release 11	Page 3.5.2-3
3.5.2.11 - 2M TO 64M BY 16 FEEPROM IN FBGA	Release 11	Page 3.5.2-3
3.5.2.12 - 4M, 8M, & 16M BY 16 FEEPROM with SDRAM Interface	Release 11	Page 3.5.2-3
3.5.2.13 - 128Mb TO 4Gb Density FEEPROM, User Selectable as X8 OR X16 in SSOP	Release 11	Page 3.5.2-4
3.5.2.14 - SINGLE-SUPPLY 16Mb AND 32Mb (x16/x32) FEEPROM IN 80-PIN PQFP	Release 12	Page 3.5.2-4
3.5.2.15 - 128Mb TO1Gb(x8/x16) FEEPROM IN 64-BALL LBGA	Release 14	Page 3.5.2-4
3.5.2.16 - 28Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL LBGA	Release 14	Page 3.5.2-4
3.5.2.17 - 16Mb TO 512Mb (x8/x16) FEEPROM IN 52-PIN TSOP II	Release 14	Page 3.5.2-4
FIGURE 3.5.2-1, 4K TO 32K BY 16 EEPROM FAMILY IN DIP	Release 1	Page 3.5.2-5
FIGURE 3.5.2-2, 4K TO 256K BY 16 EEPROM FAMILY IN SCC	Release 1	Page 3.5.2-6
FIGURE 3.5.2-3, 4M TO 128M BY 16 EEPROM FAMILY IN DIP AND SOG	Release 2	Page 3.5.2-7
FIGURE 3.5.2-4, 256K TO 2M BY 16 EEPROM FAMILY IN DIP AND SOG	Release 6	Page 3.5.2-8
FIGURE 3.5.2-5, 1M TO 4M BY 16 DS EEPROM IN SSOP	Release 6	Page 3.5.2-9
FIGURE 3.5.2-6, 1M TO 4M DENSITY BY 8 OR16 FEEPROM IN PSOP	Release 7	Page 3.5.2-10
FIGURE 3.5.2-7, 1M TO 32M DEBSITY BY 8 OR16 FEEPROM IN PSOP	Release 7	Page 3.5.2-11
FIGURE 3.5.2-8, 512K TO 2048K X 8, 256K TO 2048K X 16, Dual Supply Flash EEPROM IN 8 X 6 GRID Micro BGA Package	Release 9	Page 3.5.2-12
FIGURE 3.5.2-9, 2048K & 8192K X 8, 1024K & 4096K X 16, Dual supply Flash EEPROM IN 8 X 9 GRID Micro BGA Package	Release 9	Page 3.5.2-13
FIGURE 3.5.2-10, FEEPROM/SRAM Mixed Technology, Multi Chip Device	Release 10r11	Page 3.5.2-14⇒19
FIGURE 3.5.2-11, 4M TO 64M BY 16 FEEPROM IN TSOP1	Release 11	Page 3.5.2-20
FIGURE 3.5.2-12, 32Mb TO 1Gb Density BY 16 FEEPROM IN BGA	Release 11	Page 3.5.2-21
FIGURE 3.5.2-13, 4MTO 16M BY 16 FEEPROM With SDRAM Interface In TSOP2	Release 11	Page 3.5.2-22
FIGURE 3.5.2-14, 4M TO 16M BY 16 FEEPROM With SDRAM Interface in FGBA	Release 11	Page 3.5.2-23
FIGURE 3.5.2-15, 128Mb TO 4Gb FEEPROM, user selectable as X8 or X16 in SSOP	Release 11	Page 3.5.2-24
FIGURE 3.5.2-16, SINGLE-SUPPLY 16Mb AND 32Mb (x16/x32) FEEPROM IN 80-PIN PQFP	Release 12	Page 3.5.2-25
FIGURE 3.5.2-17, 128Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL LBGA	Release 14	Page 3.5.2-26
FIGURE 3.5.2-18, 128Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL TFBGA	Release 14	Page 3.5.2-27
FIGURE 3.5.2-19, 16Mb TO 256Mb (x8/x16) FEEPROM IN 56-PIN TSOP II	Release 14	Page 3.5.2-28
3.5.3 EEPROM EXTENDED FEATURES	**Release 1**	**Page 3.5.3-1**
3.5.3.1 - EXTENDED FEATURE SET FOR 256Kb EEPROM	Release 1	Page 3.5.3-3
3.5.3.2 - DUAL SUPPLY EEPROM COMMAND SET	Release 7	Page 3.5.3-13
3.5.3.3 - SINGLE SUPPLY EEPROM COMMAND CODES	Release 7	Page 3.5.3-14
3.5.3.4 - EEPROM TOGGLE BIT FEATURE	Release 7	Page 3.5.3-15
3.5.3.5 - SYNCHRONOUS DRAM INTERFACE EEPROM (FLASH) IN 86-PIN TSOP-2 AND 90-BALL FBGA	Release 12	Page 3.5.3-16
3.5.3.6 - EEPROM with Two SPD Software Write Protect Methods	Release 14	Page 3.5.3-19
3.6 Non volatile Random Access Memory (NVRAM)	**Release 1**	**Page 3.6-1**
3.6.1 NVRAM, Nibble Wide	**Release 1**	**Page 3.6-3**
3.6.1.1 - .25K & 1K BY 4 NVRAM IN DIP	Release 1	Page 3.6-3
3.6.2 NVRAM, BYTE WIDE	**Release 1**	**Page 3.6-3**
3.6.2.1 - .5K, 1K BY 8 NVRAM IN DIP	Release 1	Page 3.6-3
3.6.2.2 - .5K & 1K BY 8 NVRAM IN RCC	Release 1	Page 3.6-3
3.6.2.3 - .5K TO 16K BY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6-3
3.6.2.4 - .5K TO 16K BY 8 NVRAM FAMILY IN RCC	Release 1	Page 3.6-3
3.6.2.5 - 32K TO 256K BY 8 NVRAM FAMILY IN SOJ,	Release 1	Page 3.6-3
3.6.2.6 - 32K TO 256K BY 8 NVRAM FAMILY IN DIP,	Release 1	Page 3.6-3
3.6.2.7 - 16K TO 128K BY 9 NVRAM FAMILY IN DIP,	Release 1	Page 3.6-3

Release 14

XILINX EXHIBIT 1010
Page 700

Section	Release #	Page #
FIGURE 3.6-1, .25K & 1K BY 4 NVRAM IN DIP	Release 1	Page 3.6-5
FIGURE 3.6-2, .5K & 1K BY 8 NVRAM IN DIP	Release 1	Page 3.6-6
FIGURE 3.6-3, .5K & 1K BY 8 NVRAM IN RCC	Release 1	Page 3.6-7
FIGURE 3.6-4, .5K TO 16K BY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6-8
FIGURE 3.6-5, .5K TO 16K BY 8 NVRAM FAMILY IN RCC	Release 1	Page 3.6-9
FIGURE 3.6-6, 32K TO 256K BY 8 NVRAM FAMILY IN SOJ	Release 1	Page 3.6-10
FIGURE 3.6-7, 32K TO 256K NY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6-11
FIGURE 3.6-8, 16K TO 128K BY 9 NVRAM FAMILY IN DIP	Release 1	Page 3.6-12
3.7 Static Random Access Memory (SRAM)	**Release 1**	**Page 3.7-1**
3.7.1 - JTAG Extension to Revolutionary Pinout SRAM Devices	**Release 4**	**Page 3.7-1**
FIGURE 3.7-1, JTAG ADDITION TO REVOLUTIONARY PINOUT SRAM	Release 4	Page 3.7-3
FIGURE 3.7-2, State Diagram for Pipelined-Burst SRAM	Release 7	Page 3.7-4
3.7.1 Bit Wide TTL SRAM	**Release 1**	**Page 3.7.1-1**
3.7.1.1 - .25K & 1K BY 1 TTL SRAM IN DIP	Release 1	Page 3.7.1-3
3.7.1.2 - .25K & 1K BY 1 TTL SRAM IN SCC	Release 1	Page 3.7.1-3
3.7.1.3 - 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.1-3
3.7.1.4 - 16K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-3
3.7.1.5 - 64K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-3
3.7.1.6 - 16K TO 2M BY 1 TTL SRAM IN SOJ	Release 5	Page 3.7.1-3
3.7.1.7 - 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.1-3
3.7.1.8 - 256K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-3
3.7.1.9 - 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.1-3
FIGURE 3.7.1-1, 0.25K & 1K BY 1 TTL SRAM IN DIP	Release 1	Page 3.7.1-5
FIGURE 3.7.1-2, 0.25K & 1K BY 1 TTL SRAM IN SCC	Release 1	Page 3.7.1-6
FIGURE 3.7.1-3, 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.1-7
FIGURE 3.7.1-4, 16K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-8
FIGURE 3.7.1-5, 64K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-9
FIGURE 3.7.1-6, 16K TO 2M BY 1 TTL SRAM IN SOJ AND TSOP-2	Release 5	Page 3.7.1-10
FIGURE 3.7.1-7, 256K TO 16M BY 1 TTL SRAM AND SSRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.1-11
FIGURE 3.7.1-8, 256K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-12
FIGURE 3.7.1-9, 4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.1-13
3.7.2 Bit Wide ECL SRAM	**Release 1**	**Page 3.7.2-1**
3.7.2.1 - 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.2-3
3.7.2.2 - 256K TO 16M BY 1 ECL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.2-3
3.7.2.3 - 64K AND 256K BY 1 ECL SRAM IN FLATPACK	Release 2	Page 3.7.2-3
3.7.2.4 - 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.2-3
FIGURE 3.7.2-1, 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.2-5
FIGURE 3.7.2-2, 256K TO 16M BY 1 ECL SRAM AND SSRAM FAMILY IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.2-6
FIGURE 3.7.2-3, 64K AND 256K BY 1 ECL SRAM IN FP	Release 2	Page 3.7.2-7
FIGURE 3.7.2-4, 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.2-8
3.7.3 Nibble Wide TTL SRAM	**Release 1**	**Page 3.7.3-1**
3.7.3.1 - 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC	Release 1	Page 3.7.3-3
3.7.3.2 - .25K BY 4 TTL SRAM IN DIP & RCC	Release 1	Page 3.7.3-3
3.7.3.3 - 256 BY 4 TTL SRAM WITH G IN SCC	Release 1	Page 3.7.3-3
3.7.3.4 - 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP	Release 1	Page 3.7.3-3

Section	Release #	Page #
3.7.3.5 - 4K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-3
3.7.3.6 - 4K TO 1M BY 4 TTL SRAM WITH G FAMILY IN DIP	Release 1	Page 3.7.3-3
3.7.3.7 - 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN RCC	Release 1	Page 3.7.3-3
3.7.3.8 - 16K & 64K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-3
3.7.3.9 - 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ AND TSOP-2	Release 5	Page 3.7.3-4
3.7.3.10 - 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-4
3.7.3.11 - 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-4
3.7.3.12 - 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-4
3.7.3.13 - 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ	Release 1	Page 3.7.3-4
3.7.3.14 - 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ	Release 1	Page 3.7.3-4
FIGURE 3.7.3-1, 16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN DIP	Release 1	Page 3.7.3-5
FIGURE 3.7.3-2, 16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN SCC	Release 1	Page 3.7.3-6
FIGURE 3.7.3-3, 256 BY 4 TTL SRAM IN DIP	Release 1	Page 3.7.3-7
FIGURE 3.7.3-4, 256 BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-8
FIGURE 3.7.3-5, 256 BY 4 TTL SRAM IN SCC	Release 1	Page 3.7.3-9
FIGURE 3.7.3-6, 4K TO 64K BY 4 TTL SRAM FAMILY WITHOUT G IN DIP	Release 1	Page 3.7.3-10
FIGURE 3.7.3-7, 4K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-11
FIGURE 3.7.3-8, 4K TO 256K BY 4 TTL SRAM FAMILY WITH G IN DIP	Release 1	Page 3.7.3-12
FIGURE 3.7.3-9, 16K TO 256K BY 4 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.3-13
FIGURE 3.7.3-10, 16K & 64K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-14
FIGURE 3.7.3-11, 4K TO 1M BY 4 TTL SRAM WITH AND W/O G IN SOJ AND TSOP-2	Release 1	Page 3.7.3-15
FIGURE 3.7.3-12, 64K TO 4M BY 4 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.3-16
FIGURE 3.7.3-13, 64K TO 4M BY 4 TTL SRAM FAMILY WITH SEPARATE DATA I/O IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.3-17
FIGURE 3.7.3-14, 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) FAMILY IN DIP,SOJ,AND TSOP-2	Release 4	Page 3.7.3-18
FIGURE 3.7.3-15, 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ	Release 1	Page 3.7.3-19
3.7.4 Nibble Wide ECL SRAM	**Release 1**	**Page 3.7.4-1**
3.7.4.1 - .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP	Release 1	Page 3.7.4-3
3.7.4.2 - 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP	Release 1	Page 3.7.4-3
3.7.4.3 - .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.4-3
3.7.4.4 - 16K BY 4,10K & 100K ECL SSRAM IN DIP	Release 1	Page 3.7.4-3
3.7.4.5 - 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-3
3.7.4.6 - 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-3
, 3.7.4.7 - 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
3.7.4.8 - 64K BY 4 ECL SRAM IN FP	Release 2	Page 3.7.4-4
3.7.4.9 - 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ	Release 2	Page 3.7.4-4
3.7.4.10 - 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
3.7.4.11 - 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
3.7.4.12 - 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
FIGURE 3.7.4-1, 256 BY 4, 100K ECL SRAM IN DIP, 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP	Release 1	Page 3.7.4-5
FIGURE 3.7.4-2, 256 & 1K BY 4, 100K ECL SRAM IN SFP	Release 1	Page 3.7.4-6
FIGURE 3.7.4-4, 0.25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.4-7

Section	Release #	Page #
FIGURE 3.7.4-5, 16K BY 4, 10K & 100K ECL SSRAM IN DIP	Release 1	Page 3.7.4-8
FIGURE 3.7.4-6, 64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-9
FIGURE 3.7.4-7, 64K TO 4M BY 4 ECL SRAM WITH SEPARATE I/O FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-10
FIGURE 3.7.4-8, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-11
FIGURE 3.7.4-9, 64K BY 4 ECL SRAM IN FP	Release 2	Page 3.7.4-12
FIGURE 3.7.4-10, 256K BY 4 or 512K BY 2 CONFIGURABLE ECL SRAM IN DIP AND SOJ	Release 2	Page 3.7.4-13
FIGURE 3.7.4-11, 64K TO 4M BY 4 BIT SELECTABLE ECL SRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-14
FIGURE 3.7.4-12, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-15
FIGURE 3.7.4-13, 64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-16
3.7.5 Byte Wide TTL SRAM	**Release 1**	**Page 3.7.5-1**
3.7.5.1 - 64 BY 9 TTL SRAM IN SCC	Release 1	Page 3.7.5-3
3.7.5.2 - 1K & 2K BY 8 TTL SRAM IN DIP	Release 1	Page 3.7.5-3
3.7.5.3 - 2K & 4K BY 8 TTL SRAM IN RCC	Release 1	Page 3.7.5-3
3.7.5.4 - 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,	Release 1	Page 3.7.5-3
3.7.5.5 - .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.5-3
3.7.5.6 - 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP-2,	Release 4	Page 3.7.5-3
3.7.5.7 - 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,	Release 1	Page 3.7.5-3
3.7.5.8 - 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,	Release 1	Page 3.7.5-3
3.7.5.9 - 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.5-3
3.7.5.10 - 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ	Release 1	Page 3.7.5-3
3.7.5.11 - 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC	Release 1	Page 3.7.5-3
3.7.5.12 - 32K BY 9 CACHE SRAM IN 44 SCC	Release 2	Page 3.7.5-3
3.7.5.13 - 128K BY 8 SRAM IN TSOP1	Release 2	Page 3.7.5-3
3.7.5.14 - 128K BY 8 & 9 SSRAM IN SOJ	Release 2	Page 3.7.5-3
3.7.5.15 - 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP	Release 2	Page 3.7.5-3
3.7.5.16 - 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO-N	Release 3	Page 3.7.5-3
3.7.5.17 - 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP AND SOJ	Release 3	Page 3.7.5-4
3.7.5.18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA	Release 5	Page 3.7.5-4
3.7.5.19 - 128K TO 2M BY 8/9 SSRAM IN BGA	Release 5	Page 3.7.5-4
3.7.5.20 - 32K BY 8 SRAM IN TSOP1	Release 7	Page 3.7.5-4
3.7.5.21 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 209 BGA	Release 12	Page 3.7.5-4
3.7.5.22 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 221 BGA	Release 12	Page 3.7.5-4
FIGURE 3.7.5-1, 64 BY 9 SRAM IN SCC	Release 1	Page 3.7.5-5
FIGURE 3.7.5-2, 1K & 2K BY 8 TTL SRAM IN DIP	Release 1	Page 3.7.5-6
FIGURE 3.7.5-3, 2K & 4K BY 8 TTL SRAM IN RCC	Release 1	Page 3.7.5-7
FIGURE 3.7.5-4, 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ	Release 1	Page 3.7.5-8
FIGURE 3.7.5-5, 0.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.5-9
FIGURE 3.7.5-6, 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ	Release 4	Page 3.7.5-10
FIGURE 3.7.5-7, 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5-11
FIGURE 3.7.5-8, 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5-12
FIGURE 3.7.5-9, 32K TO 2M BY 8 AND 9 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.5-13
FIGURE 3.7.5-10, 32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.5-14
FIGURE 3.7.5-11, 2K TO 32K BY 9 DPSRAM FAMILY IN SCC	Release 1	Page 3.7.5-15
FIGURE 3.7.5-12, 32K BY 9 TTL CACHE SRAM IN SCC	Release 2	Page 3.7.5-16
FIGURE 3.7.5-13, 128K BY 8 TTL SRAM IN TSOP1	Release 2c9	Page 3.7.5-17
FIGURE 3.7.5-14, 128K BY 8 & 9 TTL SSRAM IN SOJ	Release 2	Page 3.7.5-18

Section	Release #	Page #
FIGURE 3.7.5-15A, 1K AND 2K BY 9 DPSRAM IN DIP	Release 2	Page 3.7.5-19
FIGURE 3.7.5-15B, 1K AND 2K BY 9 DPSRAM TRUTH TABLE	Release 2	Page 3.7.5-20
FIGURE 3.7.5-16, 128K TO 512K BY 8 SRAM IN CDSO-N	Release 3	Page 3.7.5-21
FIGURE 3.7.5-17, 128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.5-22
FIGURE 3.7.5-18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA	Release 5	Page 3.7.5-23
FIGURE 3.7.5-19 - 128K TO 2M BY 8/9 SSRAM BGA IN BGA	Release 5	Page 3.7.5-24
FIGURE 3.7.5-20 - 128K TO 2M BY 8/9 SSRAM BGA BOUNDRY SCAN ORDER	Release 5	Page 3.7.5-25
FIGURE 3.7.5-21 - 32K BY 8 SRAM IN TSOP2	Release 7	Page 3.7.5-26
FIGURE 3.7.5-22 - 1Mb - 128Mb (x9) Sync Separate I/O SRAM in 209 BGA	Release 12	Page 3.7.5-27
FIGURE 3.7.5-23 - 1Mb - 128Mb (x9) Sync Separate I/O SRAM in 221 BGA	Release12	Page 3.7.5-28
3.7.6 Byte Wide ECL SRAM	**Release 1**	**Page 3.7.6-1**
3.7.6.1 - 32K and 128K BY 8 ECL SSRAM IN SOJ, SSOP, AND FP	Release 2	Page 3.7.6-1
FIGURE 3.7.6-1, 32K AND 256K BY 9 ECL SSRAM IN SOJ, SOP, AND FP	Release 2	Page 3.7.6-3
3.7.7 Word Wide TTL SRAM	**Release 11**	**Page 3.7.7-1**
3.7.7.1 - 4K TO 64K BY 16 TTL SRAM IN DIP	Release 1	Page 3.7.7-2
3.7.7.2 - 4K TO 256K BY 16 TTL SRAM IN SCC	Release 1	Page 3.7.7-2
3.7.7.3 - 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP	Release 1	Page 3.7.7-2
3.7.7.4 - 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC	Release 1	Page 3.7.7-2
3.7.7.5 - 16K AND 64K BY 18 SRAM IN SCC	Release 1	Page 3.7.7-2
3.7.7.6 - 64K BY 16 & 18 SRAM IN 44 SOJ	Release 3	Page 3.7.7-2
3.7.7.7 - 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES	Release 4	Page 3.7.7-2
3.7.7.8 - 64K TO 256K BY 18 SRAM & SSRAM IN TQFP	Release 5	Page 3.7.7-3
3.7.7.9 - 64K TO 1M BY 16/18 BURST SRAM IN BGA	Release 5	Page 3.7.7-3
3.7.7.10 - 64K TO 1M BY 16/18 SSRAM IN BGA	Release 5	Page 3.7.7-3
3.7.7.11 - 64K TO 256K BY 16/18 BURST SRAM IN QFP/TQFP	Release 6	Page 3.7.7-3
3.7.7.12 - 256K AND 1M BY 16/18 SRAM IN TSOP2	Release 6	Page 3.7.7-3
3.7.7.13 - 1Mb TO 128Mb Density, BY 16 OR 18 BURST SRAM IN 221 BGA	Release 11	Page 3.7.7-3
3.7.7.14 - 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 209 BGA, with Common I/O	Release 11	Page 3.7.7-3
3.7.7.15 - 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 221 BGA, with Common I/O	Release 11	Page 3.7.7-3
3.7.7.16 - 1Mb TO 128Mb Density, BY 18 SIGMA SRAM IN 209 BGA, with Separate I/O	Release 12	Page 3.7.7-4
3.7.7.17 - 1Mb TO 128Mb Density, BY 18 SIGMA SRAM IN 221 BGA, with Separate I/O	Release 12	Page 3.7.7-4
3.7.7.18 - 8Mb TO 128Mb Density, BY 18 SRAM IN 165 BGA, with Separate I/O	Release 12	Page 3.7.7-4
3.7.7.19 - 2Mb TO 256Mb Density, BY 16 or 18 Burst SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.7-4
3.7.7.20 - 2Mb TO 256Mb Density, BY 16 or 18 Network SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.7-4
3.7.7.21 - 52-Pin TSOP II Pin Assignment for Low Power SRAMs	Release 14	Page 3.7.7-4
FIGURE 3.7.7-1, 4K TO 64K BY 16 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.7-5
FIGURE 3.7.7-2, 4K TO 256K BY 16 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.7-6
FIGURE 3.7.7-3, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN DIP	Release 1	Page 3.7.7-7
FIGURE 3.7.7-4, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN RCC	Release 1	Page 3.7.7-8
FIGURE 3.7.7-5, 16K AND 64K BY 18 SRAM IN SCC	Release 1	Page 3.7.7-9
FIGURE 3.7.7-6, 64K BY 16 & 18 SRAM IN SOJ	Release 3	Page 3.7.7-10
FIGURE 3.7.7-7 A, 32K & 64K BY 16 & 18 SRAM AND SSRAM WITH LOGIC FEATURES IN SCC	Release 4	Page 3.7.7-11
FIGURE 3.7.7-7 B, WRITE CLOCK TIMING FOR SSRAM WITH BURST MODE	Release 4	Page 3.7.7-12
FIGURE 3.7.7-8, 64K TO 256K BY 18 SRAM AND SSRAM IN TQFP	Release 5	Page 3.7.7-13
FIGURE 3.7.7-9, 64K TO 1M BY 16/18 BURST SRAM BGA PADOUT	Release 5	Page 3.7.7-14

Release 14

XILINX EXHIBIT 1010
Page 704

Section	Release #	Page #
FIGURE 3.7.7-10, 64K TO 1M BY 16/18 SSRAM BGA PADOUT	Release 5	Page 3.7.7-15
FIGURE 3.7.7-11, 64K TO 1M BY 16/18 SSRAM BGA BOUNDRY SCAN ORDER	Release 5c8	Page 3.7.7-16
FIGURE 3.7.7-12, 64K TO 256K BY 16/18 BURST SRAM IN TQFP	Release 6	Page 3.7.7-17
FIGURE 3.7.7-13, 256K AND 1M BY 16/18 SRAM IN TSOP2	Release 6	Page 3.7.7-18
FIGURE 3.7.7-14, 1Mb TO 128Mb Density, BY 16 OR 18 BURST SRAM IN 221 BGA	Release 11a	Page 3.7.7-19
FIGURE 3.7.7-15, 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 209 BGA	Release 11a	Page 3.7.7-20
FIGURE 3.7.7-16, 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 221 BGA	Release 11a	Page 3.7.7-21
FIGURE 3.7.7-17, X18 SIGMA SRAM WITH SEPARATE I/O IN 209 BGA	Release 12	Page 3.7.7-22
FIGURE 3.7.7-18, X18 SIGMA SRAM WITH SEPARATE I/O IN 221 BGA	Release 12	Page 3.7.7-23
FIGURE 3.7.7-19, 8Mb - 128Mb Density in X18 SRAM WITH SEPARATE I/O IN 165 BGA	Release 12	Page 3.7.7-24
FIGURE 3.7.7-20, 2 Mb - 256 Mb Density in X16/18 BURST SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.7-25
FIGURE 3.7.7-21, 2 Mb - 256 Mb Density in X16/18 NETWORK SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.7-26
FIGURE 3.7.7-22, 52-Pin TSOP II Pin Assignment for Low Power SRAMs	Release 14	Page 3.7.7-28
3.7.8 Double Word Wide SRAM	**Release 5**	**Page 3.7.8-1**
3.7.8.1 - 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP	Release 6	Page 3.7.8-2
3.7.8.2 - 32K TO 128K BY 36 SRAM & SSRAM IN TQFP	Release 5	Page 3.7.8-2
3.7.8.3 - 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT	Release 5	Page 3.7.8-2
3.7.8.4 - 32K TO 512K BY 32/36 SSRAM BGA PADOUT	Release 5c11	Page 3.7.8-2
3.7.8.5 - 16K TO 36K BY 32 & 64 SSRAM With BURST Counter IN QFP	Release 7	Page 3.7.8-2
3.7.8.6 - 16K TO 256K BY 36 & 72 BURST SRAM IN BGA	Release 7	Page 3.7.8-2
3.7.8.7 - 1Mb TO 128Mb Density, BY 32 OR 36 BURST SRAM IN 221 BGA	Release 11	Page 3.7.8-2
3.7.8.8 - 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 209 BGA, with Common I/O	Release 11	Page 3.7.8-3
3.7.8.9 - 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 221 BGA, with Common I/O	Release 11	Page 3.7.8-3
3.7.8.10 - 1Mb TO 128Mb Density, BY 36 SIGMA SRAM IN 209 BGA, with Separate I/O	Release 12	Page 3.7.8-3
3.7.8.11 - 1Mb TO 128Mb Density, BY 36 SIGMA SRAM IN 221 BGA, with Separate I/O	Release 12	Page 3.7.8-3
3.7.8.12 - 16Mb TO 256Mb Density, BY 36 SRAM IN 165 BGA, with Separate I/O	Release 12	Page 3.7.8-3
3.7.8.13 - 8Mb TO 128Mb Density, BY 36 DDR SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.8-3
3.7.8.14 - 2Mb TO 256Mb Density, BY 32 or 36 Burst SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.8-3
3.7.8.15 - 2Mb TO 256Mb Density, BY 32 or 36 Network SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.8-4
FIGURE 3.7.8-1, 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP	Release 6c9	Page 3.7.8-5
FIGURE 3.7.8-2, 32K TO 128K BY 36 SRAM AND SSRAM IN TQFP	Release 5	Page 3.7.8-6
FIGURE 3.7.7-3 - 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT	Release 5	Page 3.7.8-7
FIGURE 3.7.7-4 - 32K TO 512K BY 32/36 SSRAM BGA PADOUT	Release 5	Page 3.7.8-8
FIGURE 3.7.7-5 - 32K TO 512K BY 32/36 SSRAM BGA BOUNDRY SCAN ORDER	Release 5	Page 3.7.8-9
FIGURE 3.7.8-6, 16K TO 36K BY 32 & 64 SSRAM With BURST Counter IN QFP	Release 7	Page 3.7.8-10
FIGURE 3.7.8-7, 16K TO 256K BY 36 & 72 BURST SSRAM IN BGA	Release 7	Page 3.7.8-11
FIGURE 3.7.8-8, 1Mb TO 128Mb Density, BY 32 OR 36 BURST SRAM IN 221 BGA	Release 11a	Page 3.7.8-12
FIGURE 3.7.8-9, 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 209 BGA	Release 11a	Page 3.7.8-13
FIGURE 3.7.8-10, 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 221 BGA	Release 11a	Page 3.7.8-14
FIGURE 3.7.8-11, X36 SIGMA SRAM WITH SEPARATE I/O IN 209 BGA	Release 12	Page 3.7.8-15
FIGURE 3.7.8-12, X36 SIGMA SRAM WITH SEPARATE I/O IN 221 BGA	Release 12	Page 3.7.8-16
FIGURE 3.7.8-13, X36 SRAM WITH SEPARATE I/O IN 165 BGA	Release 12	Page 3.7.8-17
FIGURE 3.7.8-14, X36 DDR SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.8-18
FIGURE 3.7.8-15, X32/36 BURST SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.8-19
FIGURE 3.7.8-16, X32/36 NETWORK SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.8-20

Section	Release #	Page #
3.7.9 Eight Byte Wide SRAM	**Release 11a**	**Page 3.7.9-1**
3.7.9.1 - 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 209 BGA	Release 11a	Page 3.7.9-2
3.7.9.2 - 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 221 BGA	Release 11a	Page 3.7.9-2
3.7.9.3 - 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 209 BGA	Release 11a	Page 3.7.9-2
3.7.9.4 - 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 221 BGA	Release 11a	Page 3.7.9-2
FIGURE 3.7.9-1, 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 209 BGA	Release 11a	Page 3.7.9-3
FIGURE 3.7.9-2, 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 221 BGA	Release 11a	Page 3.7.9-4
FIGURE 3.7.9-3, 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 209 BGA	Release 11a	Page 3.7.9-5
FIGURE 3.7.9-4, 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 221 BGA	Release 11a	Page 3.7.9-6
3.8 Pseudostatic Random Access Memory (PSRAM)	**Release 1**	**Page 3.8-1**
3.8.1 PSRAM, Byte Wide	**Release 1**	**Page 3.8-3**
3.8.1.1 - 2K TO 8K BY 8 PSRAM FAMILY IN DIP	Release 1	Page 3.8-3
3.8.1.2 - 2K TO 16K BY 8 PSRAM FAMILY IN RCC	Release 1	Page 3.8-3
3.8.1.3 - 32K TO 512K BY 8 PSRAM FAMILY IN SOJ	Release 1	Page 3.8-3
3.8.2 PSRAM, Word Wide	**Release 1**	**Page 3.8-3**
3.8.2.1 - 4K TO 32K BY 16 PSRAM IN DIP	Release 1	Page 3.8-3
3.8.2.2 - 4K TO 256K BY 16 PSRAM IN SCC	Release 1	Page 3.8-3
FIGURE 3.8-1, 2K TO 8K BY 8 PSRAM FAMILY IN DIP	Release 1	Page 3.8-4
FIGURE 3.8-2, 2K TO 16K BY 8 PSRAM FAMILY IN RCC	Release 1	Page 3.8-5
FIGURE 3.8-3, 32K TO 512K BY 8 PSRAM FAMILY IN SOJ	Release 1	Page 3.8-6
FIGURE 3.8-4, 4K TO 32K BY 16 PSRAM FAMILY IN DIP	Release 1	Page 3.8-7
FIGURE 3.8-5, 4K TO 256K BY 16 PSRAM FAMILY IN SCC	Release 1	Page 3.8-8
3.9 Dynamic Random Access Memory (DRAM)	**Release 1**	**Page 3.9-1**
3.9.1 Bit Wide DRAM	**Release 1**	**Page 3.9.1-1**
3.9.1.1 - 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES	Release 1	Page 3.9.1-3
3.9.1.2 - 16K TO 256K BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-3
3.9.1.3 - 16K TO 256K BY 1 DRAM IN RCC	Release 1	Page 3.9.1-3
3.9.1.4 - 64K & 256K BY 1 DRAM IN ZIP	Release 1	Page 3.9.1-3
3.9.1.5 - 1M AND 4M BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-3
3.9.1.6 - 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2	Release 4	Page 3.9.1-3
3.9.1.7 - 1M TO 16M BY 1 DRAM FAMILY IN ZIP	Release 4	Page 3.9.1-3
3.9.1.8 - 1M TO 16M BY 1 NON-MUX DRAM FAMILY IN SOJ	Release 1	Page 3.9.1-3
3.9.1.9 - 1M BY 1 DRAM IN TSOP1	Release 1	Page 3.9.1-4
3.9.1.10 - 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ	Release 1	Page 3.9.1-4
3.9.1.11 - 64M BY 1 DRAM IN SOJ OR TSOP2	Release 5	Page 3.9.1-4
3.9.1.12 - 2 X 16M BY 1 DRAM IN TSOP2	Release 4	Page 3.9.1-4
3.9.1.13 - 16M BY 1 DRAM IN USON	Release 9	Page 3.9.1-4
FIGURE 3.9.1-1, 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES 16K TO 256K BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-5
FIGURE 3.9.1-2, 16K TO 256K BY 1 DRAM IN RCC	Release 1	Page 3.9.1-6
FIGURE 3.9.1-3, 64K & 256K BY 1 DRAM IN ZIP	Release 1	Page 3.9.1-7
FIGURE 3.9.1-4, 1M TO 64M BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-8
FIGURE 3.9.1-5, 1M TO 16M BY 1 DRAM FAMILY IN SOJ and TSOP-2	Release 4	Page 3.9.1-9
FIGURE 3.9.1-6, 1M TO 16M BY 1 DRAM FAMILY IN ZIP	Release 4	Page 3.9.1-10
FIGURE 3.9.1-7, 1M TO 16M BY 1 NON-MUX DRAM FAMILY IN SOJ	Release 2	Page 3.9.1-11
FIGURE 3.9.1-8, 1M BY 1 DRAM IN TSOP1	Release 2	Page 3.9.1-12
FIGURE 3.9.1-9, 16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.1-13
FIGURE 3.9.1-10, 64M BY 1 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.1-14
FIGURE 3.9.1-11, 2 X 16M BY 1 DRAM IN TSOP2	Release 4	Page 3.9.1-15
FIGURE 3.9.1-12, 64M BY 1 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.1-16
FIGURE 3.9.1-13 16M BY 1 DRAM IN USON	Release 9	Page 3.9.1-17

Release 14

XILINX EXHIBIT 1010
Page 706

Section	Release #	Page #
3.9.2 Nibble Wide DRAM	**Release 1**	**Page 3.9.2-1**
3.9.2.1 - 16K & 64K BY 4 DRAM IN DIP	Release 1	Page 3.9.2-2
3.9.2.2 - 16K BY 4 DRAM IN DIP	Release 1	Page 3.9.2-2
3.9.2.3 - 64K BY 4 DRAM IN RCC	Release 1	Page 3.9.2-2
3.9.2.4 - 256K & 1M BY 4 DRAM FAMILY IN DIP	Release 2	Page 3.9.2-2
3.9.2.5 - 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2	Release 4	Page 3.9.2-2
3.9.2.6 - 64K TO 4M BY 4 DRAM IN ZIP	Release 2	Page 3.9.2-2
3.9.2.7 - 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2	Release 3	Page 3.9.2-2
3.9.2.8 - 256K BY 4 DRAM IN TSOP1	Release 2	Page 3.9.2-2
3.9.2.9 - 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.2-3
3.9.2.10 - 256K TO 4M BY 4 NON-MUX DRAM FAMILY IN SOJ	Release 2	Page 3.9.2-3
3.9.2.11 - 4M BY 4 DRAM WITH 1 CE AND 4 CE IN TSOP2	Release 2	Page 3.9.2-3
3.9.2.12 - 16M BY 4 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.2-3
3.9.2.13 - 1M, 2M, 4M BY 2 DRAM IN SOJ & TSOP2	Release 3r7	Page 3.9.2-3
3.9.2.14 - 16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2	Release 6	Page 3.9.2-3
3.9.2.15 - 64M BY 4 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.2-3
3.9.2.16 - 4M BY 4 DRAM IN USON	Release 9	Page 3.9.2-4
3.9.2.17 - 16M BY 4 DRAM IN USON	Release 9	Page 3.9.2-4
FIGURE 3.9.2-1, 16K & 64K BY 4 DRAM IN DIP	Release 1	Page 3.9.2-5
FIGURE 3.9.2-2, 16K & 64K BY 4 DRAM IN RCC	Release 1	Page 3.9.2-6
FIGURE 3.9.2-3, 256K & 1M BY 4 DRAM FAMILY IN DIP	Release 1	Page 3.9.2-7
FIGURE 3.9.2-4, 256K TO 4M BY 4 DRAM IN SOJ AND TSOP-2	Release 4	Page 3.9.2-8
FIGURE 3.9.2-5, 64K TO 4M BY 4 DRAM IN ZIP	Release 1	Page 3.9.2-9
FIGURE 3.9.2-6, 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2	Release 6	Page 3.9.2-10
FIGURE 3.9.2-7, 256K BY 4 DRAM IN TSOP1	Release 2	Page 3.9.2-11
FIGURE 3.9.2-8, 4M BY 4/16M BY 1 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.2-12
FIGURE 3.9.2-9, 256K TO 4M BY 4 NON-MUX DRAM IN SOJ	Release 2	Page 3.9.2-13
FIGURE 3.9.2-10, 4M BY 4 DRAM WITH 4 CE IN SOJ AND TSOP2	Release 6	Page 3.9.2-14
FIGURE 3.9.2-11, 16M BY 4 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.2-15
FIGURE 3.9.2-12, 1M, 2M, 4M BY 2 DRAM WITH 2 CE IN SOJ AND TSOP2	Release 4r7	Page 3.9.2-16
FIGURE 3.9.2-13, 16M BY 4 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.2-17
FIGURE 3.9.2-14, 16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2	Release 6r7	Page 3.9.2-18
FIGURE 3.9.2-15, 64M BY 4 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.2-19
FIGURE 3.9.2-16 4M BY 4 DRAM IN USON	Release 9	Page 3.9.2-20
FIGURE 3.9.2-17 16M BY 4 DRAM IN USON	Release 9	Page 3.9.2-21
3.9.3 Byte Wide DRAM	**Release 1**	**Page 3.9.3-1**
3.9.3.1 - 32K BY 8 DRAM IN DIP	Release 1	Page 3.9.3-3
3.9.3.2 - 32K BY 8 DRAM IN RCC	Release 1	Page 3.9.3-3
3.9.3.3 - 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP	Release 2	Page 3.9.3-3
3.9.3.4 - 512K BY 8 & BY 9 NON-MUX DRAM IN SOJ	Release 2	Page 3.9.3-3
3.9.3.5 - 2M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3-3
3.9.3.6 - 8M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3-3
3.9.3.7 - 32M BY 8 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.3-3
3.9.3.8 - 4M & 8M BY 8 DRAM IN SOP	Release 8	Page 3.9.3-4
3.9.3.9 - 2M BY 8 DRAM IN USON	Release 9	Page 3.9.3-4
3.9.3.10 - 8M BY 8 DRAM IN USON	Release 9	Page 3.9.3-4
FIGURE 3.9.3-1, 32K BY 8 DRAM IN DIP	Release 1	Page 3.9.3-5
FIGURE 3.9.3-2, 32K BY 8 DRAM IN RCC	Release 1	Page 3.9.3-6
FIGURE 3.9.3-3, 512K BY 8 & 9 DRAM IN SOJ	Release 2	Page 3.9.3-7
FIGURE 3.9.3-4, 512K BY 8 & 9 DRAM IN ZIP	Release 2	Page 3.9.3-8
FIGURE 3.9.3-5, 512K BY 8 & 9 NON-MUX DRAM IN SOJ	Release 2	Page 3.9.3-9

Release 14

XILINX EXHIBIT 1010
Page 707

Section	Release #	Page #
FIGURE 3.9.3-6, 2M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3-10
FIGURE 3.9.3-7, 8M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.3-11
FIGURE 3.9.3-8, 8M BY 8 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.3-12
FIGURE 3.9.3-9, 32M BY 8 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.3-13
FIGURE 3.9.3-10, 4M & 8M BY 8 DRAM IN SOP	Release 8	Page 3.9.3-14
FIGURE 3.9.3-11 2M BY 8 DRAM IN USON	Release 9	Page 3.9.3-15
FIGURE 3.9.3-12 8M BY 8 DRAM IN USON	Release 9	Page 3.9.3-16
3.9.4 Word Wide DRAM	**Release 1**	**Page 3.9.4-1**
3.9.4.1 - 64K BY 16 DRAM WITH 2 W IN SOJ & TSOP2	Release 1	Page 3.9.4-3
3.9.4.2 - 256K & 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ & TSOP2	Release 5	Page 3.9.4-3
3.9.4.3 - 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ	Release 4	Page 3.9.4-3
3.9.4.4 - 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP2	Release 6r7	Page 3.9.4-3
3.9.4.5 - 128K AND 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, AND ZIP	Release 6	Page 3.9.4-3
3.9.4.6 - 16M BY 16 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4-4
3.9.4.7 - 128K ANS 256K BY 32 DRAM WITH 4 $\overline{CAS}$ IN TSOP2	Release 6	Page 3.9.4-4
3.9.4.8 - 512K AND 2M BY 32 & 36 DRAM WITH 4 $\overline{CAS}$ IN TSOP2	Release 6r10	Page 3.9.4-4
3.9.4.9 - 8M BY 32 DRAM IN TSOP2 PIN ROTATION	Release 6r9	Page 3.9.4-4
3.9.4.10 - 2M BY 32 DRAM IN TSOP2	Release 7	Page 3.9.4-4
3.9.4.11 - 2M BY 32 DRAM WITH EDO IN QFP	Release 6r8	Page 3.9.4-4
3.9.4.12 - 1M BY 16 DRAM IN USON	Release 9	Page 3.9.4-4
3.9.4.13 - 4M BY 16 DRAM IN USON	Release 9	Page 3.9.4-4
FIGURE 3.9.4-1, 64K BY 16 DRAM IN SOJ	Release 1	Page 3.9.4-5
FIGURE 3.9.4-2, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN SOJ	Release 2	Page 3.9.4-6
FIGURE 3.9.4-3, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN TSOP2	Release 4	Page 3.9.4-7
FIGURE 3.9.4-4, 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ	Release 5	Page 3.9.4-8
FIGURE 3.9.4-5, 1M BY 16 & 18 DRAM WITH 2 CE IN TSOP2	Release 5	Page 3.9.4-9
FIGURE 3.9.4-6, 64K BY 16 DRAM WITH 2 W IN TSOP-2	Release 3	Page 3.9.4-10
FIGURE 3.9.4-7A, 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ	Release 4	Page 3.9.4-11
FIGURE 3.9.4-7B, 256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE	Release 4	Page 3.9.4-12
FIGURE 3.9.4-8, 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP-2	Release 6r7	Page 3.9.4-13
FIGURE 3.9.4-9, 128K AND 256K BY 16 BURST DRAM IN SOJ	Release 6	Page 3.9.4-14
FIGURE 3.9.4-10, 128K AND 256K BY 16 BURST DRAM IN TSOP2	Release 6	Page 3.9.4-15
FIGURE 3.9.4-11, 128K AND 256K BY 16 BURST DRAM IN ZIP	Release 6	Page 3.9.4-16
FIGURE 3.9.4-12, 16M BY 16 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4-17
FIGURE 3.9.4-13, 128K AND 256K BY 32 DRAM WITH 4 $\overline{CAS}$ IN SSOP	Release 8	Page 3.9.4-18
FIGURE 3.9.4-14, 512K AND 2M BY 32 & 36 DRAM IN SOJ AND TSOP2	Release 6r10	Page 3.9.4-19
FIGURE 3.9.4-15, 8M BY 32 DRAM IN TSOP2 PIN ROTATION	Release 9	Page 3.9.4-20
FIGURE 3.9.4-16, 2M BY 32 DRAM IN TSOP2	Release 7	Page 3.9.4-21
FIGURE 3.9.4-17, 256K BY 32 DRAM IN QFP	Release 8	Page 3.9.4-22
FIGURE 3.9.4-18 1M BY 16 DRAM IN USON	Release 9	Page 3.9.4-23
FIGURE 3.9.4-19 4M BY 16 DRAM IN USON	Release 9	Page 3.9.4-24
3.9.5 DRAM Optional Features	**Release 1**	**Page 3.9.5-1**
3.9.5.1 - OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM	Release 1	Page 3.9.5-3
3.9.5.2 - 1M DRAM BUILT IN TEST FUNCTION	Release 1	Page 3.9.5-3
3.9.5.3 - ON-CHIP REFRESH CONTROL FOR X8 DRAM	Release 1	Page 3.9.5-3
3.9.5.4 - G BEFORE E REFRESH	Release 1	Page 3.9.5-3
3.9.5.5 - DRAM SPECIAL TEST AND OPERATIONAL MODES	Release 1	Page 3.9.5-3
3.9.5.6 - NON-MULTIPLEXED DRAM OPERATION	Release 1	Page 3.9.5-3
3.9.5.7 - DRAM EXTENDED DATA OUT DEFINITION	Release 6	Page 3.9.5-3

Release 14

XILINX EXHIBIT 1010
Page 708

Section	Release #	Page #
3.9.5.8 - 256m DRAM TEST MODE DATA AND ADDRESS COMPRESSION	Release 7	Page 3.9.5-3
3.9.5.9 - PIPELINED NIBBLE MODE DEFINITION	Release 7	Page 3.9.5-3
FIGURE 3.9.5-1A, DRAM ON CHIP REFRESH TIMING	Release 1	Page 3.9.5-5
FIGURE 3.9.5-1B, DRAM SELF REFRESH MODE TIMING	Release 4	Page 3.9.5-5
FIGURE 3.9.5-2, DRAM BIT WRITE TIMING	Release 1	Page 3.9.5-6
DRAM SPECIAL TEST AND OPERATIONAL MODES	Release 4	Page 3.9.5-7
OPTIONAL DRAM OPERATIONAL MODES AND CYCLES	Release 3	Page 3.9.5-11
NON-ADDRESS MULTIPLEXED DRAM OPERATIONAL REQUIREMENTS	Release 3	Page 3.9.5-13
DRAM EXTENDED DATA OUT DEFINITION	Release 6	Page 3.9.5-14
256M DRAM ADDRESS AND DATA COMPRESSION DEFINITION	Release 7	Page 3.9.5-15
PIPELINED NIBBLE MODE DEFINITION	Release 7	Page 3.9.5-16
3.10 Multiport Dynamic RAM (MPDRAM)	**Release 1**	**Page 3.10-1**
3.10.1 Nibble Wide MPDRAM	**Release 1**	**Page 3.10.1-1**
3.10.1.1 - 64K BY 4 MPDRAM IN DIP, SOJ, & ZIP	Release 1	Page 3.10.1-1
3.10.1.2 - 256K BY 4 MPDRAM IN DIP, SOJ, TSOP2, & ZIP	Release 3	Page 3.10.1-1
3.10.1.3 - 256K BY 4 TPDRAM IN SOJ	Release 2	Page 3.10.1-1
FIGURE 3.10.1-1, 64K BY 4 MPDRAM IN DIP & SOJ	Release 1	Page 3.10.1-2
FIGURE 3.10.1-2, 64K BY 4 MPDRAM IN ZIP	Release 1	Page 3.10.1-3
FIGURE 3.10.1-3, 256K BY 4 MPDRAM IN DIP, SOJ, & TSOP2	Release 3	Page 3.10.1-4
FIGURE 3.10.1-4, 256K BY 4 MPDRAM IN ZIP	Release 1	Page 3.10.1-5
FIGURE 3.10.1-5, 256K BY 4 TPDRAM IN SOJ	Release 2	Page 3.10.1-6
3.10.2 Byte Wide MPDRAM	**Release 1**	**Page 3.10.2-1**
3.10.2.1 - 128K AND 256K BY 8 MPDRAM IN DIP, SOJ, & TSOP2	Release 3	Page 3.10.2-1
FIGURE 3.10.2-1, 128K AND 256K BY 8 MPDRAM IN DIP & SOJ	Release 2	Page 3.10.2-2
FIGURE 3.10.2-2, 128K BY 8 MPDRAM IN TSOP2	Release 3	Page 3.10.2-3
3.10.3 Word Wide MPDRAM	**Release 1**	**Page 3.10.3-1**
3.10.3.1 - 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS	Release 2	Page 3.10.3-1
3.10.3.2 - 128K & 256K BY 16 MPDRAM IN TSOP-2 WITH MULTIPLE CLOCKS	Release 5	Page 3.10.3-1
3.10.3.3 - 256K BY 16 SGRAM IN TSOP2	Release 6	Page 3.10.3-1
3.10.3.4 - 128K, 256K, & 512K BY 32, 2 & 4 Bank SGRAM IN QFP/TQFP	Release 6r9r10	Page 3.10.3-1
3.10.3.5 - 256K BY 32 GRAM IN TSOP-2	Release 6	Page 3.10.3-1
3.10.3.6 - 256K BY 32 SMPDRAM IN TSOP-2	Release 6	Page 3.10.3-2
3.10.3.7 - 256K BY 32 SMPDRAM IN TSOP-2	Release 7	Page 3.10.3-2
3.10.3.8 - 256K BY 32 MPDRAM IN TSOP-2	Release 7	Page 3.10.3-2
3.10.3.9 - 128K, 256K, & 512K BY 32 X 4 BANK SYNCHRONOUS DDR SGRAM IN LQFP	Release 9	Page 3.10.3-2
3.10.3.10 - 4M BY 32 DDR SGRAM (4 BANK) IN FBGA	Release11	Page 3.10.3-2
3.10.3.11- 8M BY 32 GDDR3 GRAPHICS RAM IN 144-BALL FBGA	Release 13	Page 3.10.3-2
FIGURE 3.10.3-1, 128K & 256K BY 16 MPDRAM IN SOG with 2 W & 2 CE	Release 3	Page 3.10.3-3
FIGURE 3.10.3-2, 128K & 256K BY 16 MPDRAM IN TSOP-2 with 2 W & 2 CE	Release 5	Page 3.10.3-4
FIGURE 3.10.3-3, 256K BY 16 SGRAM IN TSOP-2	Release 6	Page 3.10.3-5
FIGURE 3.10.3-4, 128K, 256K, & 512K BY 32 SGRAM, 2 & 4 BANK IN QFP/TQFP	Release 6c7r9r10	Page 3.10.3-6
FIGURE 3.10.3-5, 256K BY 32 SGRAM IN TSOP-2	Release 6	Page 3.10.3-7
FIGURE 3.10.3-6, 256K BY 32 SYNCH. MPDRAM IN QFP/TQFP	Release 6	Page 3.10.3-8
FIGURE 3.10.3-7, 256K BY 32 MPDRAM IN QFP/TQFP	Release 7	Page 3.10.3-9
FIGURE 3.10.3-8 128K, 256K, & 512K BY 32 X 4 BANK DDR SGRAM IN LQFP	Release 9r10	Page 3.10.3-10
FIGURE 3.10.3-9 4M X 32 (4 BANK) DDR SGRAM IN 144 BALL FBGA	Release 11	Page 3.10.3-11
FIGURE 3.10.3-10 8M X 32 GDDR3 Graphics RAM in 144-Ball FBGA	Release 13	Page 3.10.3-12
3.10.4 MPDRAM Optional Features	**Release 1**	**Page 3.10.4-1**
3.10.4.1 - 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-3
3.10.4.2 - 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-3

Release 14

XILINX EXHIBIT 1010
Page 709

Section	Release #	Page #
3.10.4.3 - MPDRAM BIT WRITE OPTIONAL FEATURE	Release 1	Page 3.10.4-3
3.10.4.4 - 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-3
3.10.4.5 - 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-3
3.10.4.6 - 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4-3
3.10.4.7 - 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4-3
3.10.4.8 - SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM	Release 3	Page 3.10.4-3
3.10.4.9 - PIPELINED FAST PAGE MODE FOR MPDRAM	Release 2	Page 3.10.4-4
3.10.4.10 - EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM	Release 2	Page 3.10.4-4
3.10.4.11 - SAM LENGTH DEFINITION FOR 2/4M MPDRAM	Release 5	Page 3.10.4-4
3.10.4.12 - SYNCH GRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4-4
3.10.4.13 - SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4-4
3.10.4.14 - SYNCH. GRAM OPERATIONAL FUNCTION TRUTH TABLES	Release 6	Page 3.10.4-4
3.10.4.15 - 8Mb MPDRAM FEATURE SET FUNCTION TABLE	Release 7	Page 3.10.4-4
3.10.4.16 - EXTENDED FUNCTIONSFOR SGRAM & MPDRAM	Release 6r7	Page 3.10.4-4
TABLE 3.10.4-1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-5
TABLE 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-6
FIGURE 3.10.4-1, BIT WRITE TIMING	Release 1	Page 3.10.4-7
TABLE 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4-8
FIGURE 3.10.4-2, SPLIT REGISTER WITH PROGRAMMABLE STOPS	Release 2	Page 3.10.4-9
FIGURE 3.10.4-3A, PIPELINED FAST PAGE MODE	Release 2	Page 3.10.4-10
FIGURE 3.10.4-3B, PIPELINED FAST PAGE MODE	Release 2	Page 3.10.4-11
FIGURE 3.10.4-4, MPDRAM EXTENDED DATA OUT FAST PAGE MODE	Release 4	Page 3.10.4-12
FIGURE 3.10.4-5A & 5B, SAM LENGTH DEFINITION FOR 4M MPDRAM	Release 5	Page 3.10.4-13, 14
FIGURE 3.10.4-6, SYNCH GRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4-15
FIGURE 3.10.4-7, SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE	Release 6	Page 3.10.4-16
TABLE 3.10.4-4 A,B, & C , SGRAM FUNCTION TRUTH TABLE	Release 6r7	Page 3.10.4-17⇒19
TABLE 3.10.4-5, 8Mb BURST MPDRAM FUNCTION TABLE	Release 7	Page 3.10.4-20
EXTENDED FUNCTIONS FOR SGRAM & MPDRAM	Release 7	Page 3.10.4-21
3.11 Synchronous Dynamic Random Access Memory (SDRAM)	**Release 4**	**Page 3.11-1**
3.11.1 Bit Wide SDRAM	**Release 4**	**Page 3.11.1-1**
FIGURE 3.11.1-1,	Release 4	Page 3.11.1-5
3.11.2 Nibble Wide SDRAM	**Release 4**	**Page 3.11.2-1**
3.11.2.1 - 4M BY 4 SDRAM IN TSOP2	Release 6r7r8	Page 3.11.2-1
3.11.2.2 - 16M BY 4 SDRAM IN TSOP2	Release 6	Page 3.11.2-1
3.11.2.3 - 64M BY 4 SDRAM IN TSOP2 PIN ROTATION	Release 7r9	Page 3.11.2-1
3.11.2.4 - 16M, 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.2-1
3.11.2.5 - 32M, 64M, 64M, & 256M BY 4 SDRAM IN TSOP2	Release 8r9r10r12	Page 3.11.2-1
3.11.2.6 - 16M BY 4 VIRTUAL CHANNEL SDRAM IN TSOP2	Release 9	Page 3.11.2-1
3.11.2.7 - 16M, 32M, & 64M BY 4 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.2-2
3.11.2.8 - 16M, 32M, & 64M BY 4 VIRTUAL CHANNEL DDR SDRAM IN TSOP2	Release 9r11	Page 3.11.2-2
3.11.2.9 - 16M, 32M, 64M, & 128M BY 4 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11	Page 3.11.2-2
3.11.2.10 - 16M BY 4 SDR SDRAM IN USON	Release 9	Page 3.11.2-2
3.11.2.11 - 16M, 32M, & 64M BY 4 SDR SDRAM IN TSOP2	Release 9	Page 3.11.2-2
3.11.2.12 - 16M, & 32M BY 4 SDR SDRAM IN LFBGA	Release 9	Page 3.11.2-2
3.11.2.13 - 16M, & 32M BY 4 DDR SDRAM IN LFBGA	Release 9	Page 3.11.2-3
3.11.2.14 - 16M, & 32M BY 4 SDR SDRAM IN LFBGA	Release 9	Page 3.11.2-3
3.11.2.15 - 16M, & 32M BY 4 DDR SDRAM IN LFBGA	Release 9r11	Page 3.11.2-3
3.11.2.16 - 64M, & 128M BY 4 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.2-3

Release 14

XILINX EXHIBIT 1010
Page 710

Section	Release #	Page #
3.11.2.17 - 16M, 32M, 64M, & 128M BY 4 DDR SDRAM IN LFBGA	Release 11a	Page 3.11.2-3
3.11.2.18 - 16M, 32M, 64M, & 128M BY 4 DDR SDRAM IN FBGA, with Optional Support Balls	Release 12	Page 3.11.2-3
3.11.2.19 - 64M, 128M, 256M, 512M, & 1G BY 4 DDR2 SDRAM IN TFBGA	Release 12r13	Page 3.11.2-4
3.11.2.20 - 16M, 32M, 64M, & 128M BY 4 SDRAM IN sTSOP	Release 12	Page 3.11.2-4
3.11.2.21 - 64M, 128M, 256M, 512M, & 1G BY 4 BY 2 DDR2 SDRAM IN STACKED FBGA	Release 13	Page 3.11.2-4
3.11.2.22 - 64M, 128M, 256M, 512M, & 1G BY 4 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS	Release 13	Page 3.11.2-4
FIGURE 3.11.2-1, 4M X 4 SDRAM IN TSOP2	Release 6r7	Page 3.11.2-5
FIGURE 3.11.2-2, 16M X 4 SDRAM IN TSOP2	Release 6	Page 3.11.2-6
FIGURE 3.11.2-3, 64M X 4 SDRAM IN TSOP2 PIN ROTATION	Release 7r9	Page 3.11.2-7
FIGURE 3.11.2-4, 16M, 32M, 64M, & 128M X 4 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.2-8
FIGURE 3.11.2-5 32M, 64M, & 128M X 4 SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.2-9
FIGURE 3.11.2-6 16M X 4 VC SDRAM IN TSOP2	Release 9	Page 3.11.2-10
FIGURE 3.11.2-7 16M, 32M, & 64M BY 4 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.2-11
FIGURE 3.11.2-8 16M, 32M, & 64M BY 4 VC DDR SDRAM IN TSOP2	Release 9c10r11r12	Page 3.11.2-12
FIGURE 3.11.2-9 16M, 32M, 64M & 128M BY 4 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11r12	Page 3.11.2-13
FIGURE 3.11.2-10 16M BY 4 SDRAM IN USON	Release 9	Page 3.11.2-14
FIGURE 3.11.2-11 16M, 32M, & 64M BY 4 SDR SDRAM IN TSOP2	Release 9r12	Page 3.11.2-15
FIGURE 3.11.2-12 16M & 32M BY 4 SDR SDRAM IN LFBGA	Release 9	Page 3.11.2-16
FIGURE 3.11.2-13 16M & 32M BY 4 DDR SDRAM IN LFBGA	Release 9	Page 3.11.2-17
FIGURE 3.11.2-14 16M, 32M, & 64M BY 4 SDR SDRAM IN LFBGA	Release 9c10	Page 3.11.2-18
FIGURE 3.11.2-15 16M, 32M, & 64M BY 4 DDR SDRAM IN LFBGA	Release 9c10r11	Page 3.11.2-19
FIGURE 3.11.2-16 64M, & 128M BY 4 SDR SDRAM IN FBGA	Release 11a	Page 3.11.2-20
FIGURE 3.11.2-17 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN FBGA	Release 11a	Page 3.11.2-21
FIGURE 3.11.2-18 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN 60-BALL FBGA with Optional Support Balls	Release 12	Page 3.11.2-22
FIGURE 3.11.2-19 64M, 128M, 256M, 512M, & 1G BY 4 DDR2 SDRAM IN 60-BALL TF-FBGA	Release 12r13	Page 3.11.2-23
FIGURE 3.11.2-20 16M, 32M, 64M, & 128M X 4 SDRAM IN sTSOP	Release 12	Page 3.11.2-24
FIGURE 3.11.2-21 64M, 128M, 256M, 512M, & 1G BY 4 X 2 DDR2 SDRAM IN 60-BALL Stacked FBGA	Release 13	Page 3.11.2-25
FIGURE 3.11.2-22 64M, 128M, 256M, 512M, & 1G BY 4 X 2 DDR2 SDRAM For 60-Ball Stacked FBGA Requiring Support Balls	Release 13	Page 3.11.2-26
3.11.3 BYTE WIDE SDRAM	**Release 4**	**Page 3.11.3-1**
3.11.3.1 - 2M BY 8 or 9 SDRAM IN TSOP2	Release 6r7	Page 3.11.3-1
3.11.3.2 - 8M BY 8 SDRAM IN TSOP2	Release 6	Page 3.11.3-1
3.11.3.3 - 32M BY 8 SDRAM PIN ROTATION	Release 7r9	Page 3.11.3-1
3.11.3.4 - 8M, 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.3-1
3.11.3.5 - 16M, 32M, 64M, & 128M BY 8 SDRAM IN TSOP2	Release 8r9r10r12	Page 3.11.3-1
3.11.3.6 - 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2	Release 9	Page 3.11.3-1
3.11.3.7 - 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.3-2
3.11.3.8 - 8M, 16M, 32M, & 64M BY 8 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11	Page 3.11.3-2
3.11.3.9 - 2M BY 8 SDR SDRAM IN USON	Release 9	Page 3.11.3-2
3.11.3.10 - 8M BY 8 SDR SDRAM IN USON	Release 9	Page 3.11.3-2
3.11.3.11 - 8M BY 8 VIRTUAL CHANNEL SDRAM IN TSOP2	Release 9	Page 3.11.3-2
3.11.3.12 - 8M, 16M, & 32M BY 8 VIRTUAL CHANNEL DDR SDRAM IN TSOP2	Release 9r11	Page 3.11.3-2
3.11.3.13 - 8M, & 16M BY 8 SDR SDRAM IN LFBGA	Release 9	Page 3.11.3-3
3.11.3.14 - 8M, & 16M BY 8 DDR SDRAM IN LFBGA	Release 9	Page 3.11.3-3
3.11.3.15 - 8M, & 16M BY 8 SDR SDRAM IN LFBGA	Release 9	Page 3.11.3-3
3.11.3.16 - 8M, 16M, 32M, & 64M BY 8 DDR SDRAM IN LFBGA	Release 9r11	Page 3.11.3-3

Section	Release #	Page #
3.11.3.17 - 16M, 32M, & 64M BY 8 Low Power SDR SDRAM IN FBGA	Release 11a	Page 3.11.3-3
3.11.3.18 - 32M, & 64M BY 8 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.3-3
3.11.3.19 - 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN FBGA	Release 11a	Page 3.11.3-4
3.11.3.20 - 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN 60 Ball FBGA, with Optional Support Balls	Release 12	Page 3.11.3-4
3.11.3.21 - 32M, 64M, 128M, 256M, & 512M BY 8 DDR2 SDRAM IN 60 Ball TFBGA	Release 12r13	Page 3.11.3-4
3.11.3.22 - 8M, 16M, 32M, & 64M BY 8 SDRAM IN sTSOP	Release 12	Page 3.11.3-4
3.11.3.23 - 32M, 64M, 128M, 256M, & 512M BY 8 BY 2 DDR2 SDRAM IN STACKED FBGA	Release 13	Page 3.11.3-4
3.11.3.24 - 32M, 64M, 128M, 256M, & 512M BY 8 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS	Release 13	Page 3.11.3-4
FIGURE 3.11.3-1, 2M BY 8 OR 9 SDRAM IN TSOP2	Release 6r7	Page 3.11.3-5
FIGURE 3.11.3-2, 8M BY 8 SDRAM IN TSOP2	Release 6	Page 3.11.3-6
FIGURE 3.11.3-3, 32M BY 8 SDRAM IN TSOP2 PIN ROTATION	Release 7r9	Page 3.11.3-7
FIGURE 3.11.3-4, 8M, 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.3-8
FIGURE 3.11.3-5, 16M, 32M, 64M, & 128M BY 8 SDRAM IN TSOP2	Release 8r9r10r12	Page 3.11.3-9
FIGURE 3.11.3-6 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2	Release 9	Page 3.11.3-10
FIGURE 3.11.3-7 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.3-11
FIGURE 3.11.3-8 8M, 16M, 32M, 64M & 128M BY 8 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11r12	Page 3.11.3-12
FIGURE 3.9.3-9 2M BY 8 SDRAM IN USON	Release 9	Page 3.11.3-13
FIGURE 3.11.3-10 8M BY 8 SDRAM IN USON	Release 9	Page 3.11.3-14
FIGURE 3.11.3-11 8M X 8 VC SDRAM IN TSOP2	Release 9	Page 3.11.3-15
FIGURE 3.11.3-12 8M, 16M, & 32M BY 8 VC DDR SDRAM IN TSOP2	Release 9c10r11	Page 3.11.3-16
FIGURE 3.11.3-13 8M & 16M BY 8 SDR SDRAM IN LFBGA	Release 9	Page 3.11.3-17
FIGURE 3.11.3-14 8M & 16M BY 8 DDR SDRAM IN LFBGA	Release 9	Page 3.11.3-18
FIGURE 3.11.3-15 8M, 16M, & 32M BY 8 SDR SDRAM IN LFBGA	Release 9c10	Page 3.11.3-19
FIGURE 3.11.3-16 8M, 16M, 32M & 64M BY 8 DDR SDRAM IN LFBGA	Release 9c10r11	Page 3.11.3-20
FIGURE 3.11.3-17 16M, 32M & 64M BY 8 SDR SDRAM IN FBGA	Release 11a	Page 3.11.3-21
FIGURE 3.11.3-18 32M & 64M BY 8 SDR SDRAM IN FBGA	Release 11a	Page 3.11.3-22
FIGURE 3.11.3-19 16M, 32M, 64M & 128M BY 8 DDR SDRAM IN FBGA	Release 11a	Page 3.11.3-23
FIGURE 3.11.3-20 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN 60-BALL FBGA with Optional Support Balls	Release 12	Page 3.11.3-24
FIGURE 3.11.3-21 32M, 64M, 128M, 256M, & 512M BY 8 DDR2 SDRAM IN 60-BALL TF-FBGA	Release 12r13	Page 3.11.3-25
FIGURE 3.11.3-22 8M, 16M, 32M, & 64M X 8 SDRAM IN sTSOP	Release 12	Page 3.11.3-26
FIGURE 3.11.3-23 32M, 64M, 256M, 128M, & 512M BY 8 X 2 DDR2 SDRAM IN 60-BALL Stacked FBGA	Release 13	Page 3.11.3-27
FIGURE 3.11.3-24 32M, 64M, 128M, 256M, & 512M BY 8 X 2 DDR2 SDRAM For 60-Ball Stacked FBGA Requiring Support Balls	Release 13	Page 3.11.3-28
3.11.4 WORD WIDE SDRAM	**Release 5**	**Page 3.11.4-1**
3.11.4.1 - 256K BY 16 AND 1M BY 16/18 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-1
3.11.4.2 - 2M & 4M BY 16 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-1
3.11.4.3 - 16M BY 16 SDRAM IN TSOP-2 PIN ROTATION	Release 6r9	Page 3.11.4-1
3.11.4.4 - 128K, 256K, & 512K, 2 & 4 Bank BY 32 SDRAM IN QFP/TQFP/LQFP	Release 6r7r9r10	Page 3.11.4-1
3.11.4.5 - 2M BY 32 SDRAM IN TSOP-2	Release 6r7r10	Page 3.11.4-1
3.11.4.6 - 8M BY 32 SDRAM IN TSOP-2 PIN ROTATION	Release 6r9	Page 3.11.4-2
3.11.4.7 - 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP-2	Release 7r8r10r11ar12	Page 3.11.4-2
3.11.4.8 - 4M, 8M, 16M, 32M, & 64M BY 16, DDR SDRAM IN TSOP-2	Release 8r9r10r11r12	Page 3.11.4-2
3.11.4.9 - 8M, 16M, 32M, & 64M BY 16, SDRAM IN TSOP-2	Release 8r9r10r12	Page 3.11.4-2
3.11.4.10 - 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2	Release 9	Page 3.11.4-2
3.11.4.11 - 4M, 8M, & 16M BY 16 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.4-2
3.11.4.12 - 4M, 8M, 16M, 32M, & 64M BY 16 STACKABLE DDR SDRAM IN LSOJ	Release 9r11r12	Page 3.11.4-3

Release 14

XILINX EXHIBIT 1010
Page 712

Section	Release #	Page #
3.11.4.13 - 4M BY 16 SDR SDRAM IN USON	Release 9	Page 3.11.4-3
3.11.4.14 - 4M BY 16 VIRTUAL CHANNEL SDRAM IN TSOP2	Release 9	Page 3.11.4-3
3.11.4.15 - 4M, 8M, & 16M BY 16 VIRTUAL CHANNEL DDR SDRAM IN TSOP2	Release 9r11	Page 3.11.4-3
3.11.4.16 - 4M, & 8M BY 16 SDR SDRAM IN LFBGA	Release 9r12	Page 3.11.4-3
3.11.4.17 - 4M, & 8M BY 16 DDR SDRAM IN LFBGA	Release 9	Page 3.11.4-3
3.11.4.18 - 4M, & 8M BY 16 SDR SDRAM IN LFBGA	Release 9	Page 3.11.4-4
3.11.4.19 - 4M, & 8M BY 16 DDR SDRAM IN LFBGA	Release 9r11	Page 3.11.4-4
3.11.4.20 - 4M BY 16/18 SLDRAM IN TSOP2	Release 9	Page 3.11.4-4
3.11.4.21 - 4M TO 64M BY 16/18 SLDRAM IN R-PZIP	Release 9	Page 3.11.4-4
3.11.4.22 - 128K, 256K, & 512K BY 32, 4 BANK DDR SDRAM IN LQFP	Release 9r10r11	Page 3.11.4-4
3.11.4.23 - 2M & 4M BY 32, 4 BANK, DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-4
3.11.4.24 - 8M, 16M, 32M, & 64M BY 16, Low Power SDR SDRAM IN FBGA	Release 11a	Page 3.11.4-5
3.11.4.25 - 16M, & 32M BY 16 SDR SDRAM IN FBGA	Release 11a	Page 3.11.4-5
3.11.4.26 - 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-5
3.11.4.27 - 2M & 4M BY 32 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.4-5
3.11.4.28 - 2M, 4M, 8M, & 16M BY 32, Low Power SDR SDRAM IN FBGA	Release 11ar12r13	Page 3.11.4-5
3.11.4.29 - 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA with Optional Support Balls	Release 12	Page 3.11.4-5
3.11.4.30 - 16M, 32M, 64M, 128M, & 256M BY 16 DDR2 SDRAM IN TFBGA	Release 12r13	Page 3.11.4-6
3.11.4.31 - 4M, 8M, 16M, & 32M BY 16 SDRAM IN sTSOP	Release 12	Page 3.11.4-6
3.11.4.32 - 16M, 32M, 64M, 128M, & 256M BY 16 BY 2 DDR2 SDRAM IN STACKED FBGA	Release 13	Page 3.11.4-6
3.11.4.33 - 16M, 32M, 64M, 128M, & 256M BY 16 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS	Release 13	Page 3.11.4-6
3.11.4.34 - 4M BY 32 DDR2 SDRAM IN 144-BALL LF-XBGA	Release 13	Page 3.11.4-6
3.11.4.35 - 8M BY 16 DDR SDRAM in 78-Ball BGA	Release 14	Page 3.11.4-7
3.11.4.36 - 8M,16M, & 32M BY 32 Low Power DDR SDRAM IN 90-BALL FBGA	Release 14	Page 3.11.4-7
FIGURE 3.11.4-1, 256 BY 16 AND 1M BY 16/18 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-8
FIGURE 3.11.4-2, 4M BY 16 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-9
FIGURE 3.11.4-3, 16M BY 16 SDRAM IN TSOP-2	Release 6c7r9	Page 3.11.4-10
FIGURE 3.11.4-4, 128K, 256K, & 512K BY 32 SDRAM IN QFP/TQFP	Release 6c7r9r10	Page 3.11.4-11
FIGURE 3.11.4-5, 2M BY 32 SDRAM IN TSOP-2	Release 6r7r10	Page 3.11.4-12
FIGURE 3.11.4-6, 8M BY 32 SDRAM IN TSOP-2 PIN ROTATION	Release 6c7r9	Page 3.11.4-13
FIGURE 3.11.4-7, 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP-2	Release 7r8r10r12	Page 3.11.4-14
FIGURE 3.11.4-8, 4M, 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN TSOP-2	Release 8r9r10r11r12	Page 3.11.4-15
FIGURE 3.11.4-9, 8M, 16M, 32M, & 64M BY 16 SDRAM IN TSOP-2	Release 8r9r10r12	Page 3.11.4-16
FIGURE 3.11.4-10 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2	Release 9	Page 3.11.4-17
FIGURE 3.11.4-11 4M, 8M, & 16M BY 16 SDR STACKABLE SDRAM IN LSOJ	Release 9	Page 3.11.4-18
FIGURE 3.11.4-12 4M, 8M, 16M, & 32M BY 16 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11r12	Page 3.11.4-19
FIGURE 3.11.4-13 4M BY 16 SDRAM IN USON	Release 9	Page 3.11.4-20
FIGURE 3.11.4-14 4M X 16 VC SDRAM IN TSOP2	Release 9	Page 3.11.4-21
FIGURE 3.11.4-15 4M, 8M, & 16M BY 16 VC DDR SDRAM IN TSOP2	Release 9c10r11	Page 3.11.4-22
FIGURE 3.11.4-16 4M & 16M BY 16 SDR SDRAM IN LFBGA	Release 9r12	Page 3.11.4-23
FIGURE 3.11.4-17 4M & 16M BY 16 DDR SDRAM IN LFBGA	Release 9	Page 3.11.4-24
FIGURE 3.11.4-18 4M, 8M, &16M BY 16 SDR SDRAM IN LFBGA	Release 9c10	Page 3.11.4-25
FIGURE 3.11.4-19 8M, 16M, & 32M BY 16 DDR SDRAM IN LFBGA	Release 9c10r11	Page 3.11.4-26
FIGURE 3.11.4-20 4M TO 64M BY 16 & 18 SLDRAM IN R-PZIP	Release 9	Page 3.11.4-27
FIGURE 3.10.4-21 4M BY 16/18 SLRAM IN TSOP2	Release 9	Page 3.11.4-28
FIGURE 3.11.4-22 128K, 256K, & 512K X 32 X 4 BANK DDR SDRAM IN QFP	Release 9r10r11	Page 3.11.4-29
FIGURE 3.11.4-23 2M, 4M & 8M BY 32 DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-30
FIGURE 3.11.4-24 8M, 16M, 32M & 64M BY 16 SDR SDRAM IN FBGA	Release 11ar12	Page 3.11.4-31

Release 14

XILINX EXHIBIT 1010
Page 713

Section	Release #	Page #
FIGURE 3.11.4-25 16M & 32M BY 16 SDR SDRAM IN FBGA	Release 11a	Page 3.11.4-32
FIGURE 3.11.4-26 8M, 16M, 32M & 64M BY 16 DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-33
FIGURE 3.11.4-27 2M & 4M BY 32 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.4-34
FIGURE 3.11.4-28 2M, 4M 8M, & 16M BY 32, Low Power SDR SDRAM IN LFBGA	Release 11ar12r13	Page 3.11.4-35
FIGURE 3.11.4-29 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN 60-BALL FBGA with Optional Support Balls	Release 12	Page 3.11.4-36
FIGURE 3.11.4-30 16M, 32M, 64M, 128M, & 256M BY 16 DDR2 SDRAM IN 60-BALL TFBGA	Release 12r13	Page 3.11.4-37
FIGURE 3.11.4-31 4M, 8M, 16M, & 32M X 16 SDRAM IN sTSOP	Release 12	Page 3.11.4-38
FIGURE 3.11.4-32 16M, 32M, 64M, 128M, & 256M BY 16 X 2 DDR2 SDRAM InStacked FBGA	Release 13	Page 3.11.4-39
FIGURE 3.11.4-33 16M, 32M, 64M, 128M, & 256M BY 16 X 2 DDR2 SDRAM For Stacked FBGA Packages Requiring Support Balls	Release 13	Page 3.11.4-40
FIGURE 3.11.4-34 4M x 32M DDR2 SDRAM in 144-Ball LF-XBGA	Release 13	Page 3.11.4-41
FIGURE 3.11.4-35 8M x 16 DDR SDRAM in 78-Ball TF-BGA	Release 14	Page 3.11.4-42
FIGURE 3.11.4-36 8M , 16M, & 32M x 32 Low Power DDR SDRAM in 90-Ball FBGA	Release 14	Page 3.11.4-43
3.11.5 SDRAM Architectural and Operational Features See P 3.11.5-1 for detailed Table of Contents	**Release 4-9r12**	**Page 3.11.5-1**
3.11.5.1 - General SDRAM Functions	Rel.4r9r12r13	Page 3.11.5.1-1
3.11.5.2 - DDR Specific SDRAM Functions	Release 9r12	Page 3.11.5.2-1
3.11.5.3 - ESDRAM Specific SDRAM Functions	Release 9	Page 3.11.5.3-1
3.11.5.4 - VCSDRAM Specific SDRAM Functions	Release 9	Page 3.11.5.4-1
3.11.5.5 - DDR2 Specific SDRAM Functions	Release 13	Page 3.11.5.5-1
3.11.5.6 - GDDR2 Specific SDRAM Functions	Release 13	Page 3.11.5.6-1
3.11.5.7 - GDDR3 Specific SDRAM Functions	Release 14	Page 3.11.5.7-1
3.11.6 - SDRAM Parametric Specifications	**Release 9**	**Page 3.11.6-1**
3.11.6.1 - DDR SDRAM/SGRAM I/O Voltage	Release 9	Page 3.11.6-3
3.11.6.2 - 256M SDRAM/SGRAM REFRESH SPECIFICATION	Release 9	Page 3.11.6-3
3.11.6.3-16MB & 64MB TIMING SPECIFICATIONS (LVTTL)	Release 8	Pages 3.11.6-4⇒6
3.11.6.4 - STANDARD FOR DOUBLE DATA RATE (DDR) SDRAM/SGRAM INPUT INTERFACE SPECIFICATIONS	Release 9	Pages 3.11.6-7
3.11.6.5 - DDR SDRAM Self-Refresh Exit Timing	Release 9	Pages 3.11.6-8
3.11.6.6 - AC TIMING PARAMETERS FOR DDR SDRAMs/SGRAMs	Release 9	Pages 3.11.6-9⇒19
3.20. MEMORY DEVICE COMPLETE SPECIFICATION APPENDIX	**Release 11**	**Page 3.20-1**
3.20.1 - DDR SDRAM Device Specification	Release 11	Page 3.20-1
3.20.2 - DDR2 SDRAM Device Specification	Release 11r12	Page 3.20-1
4. MULTI-CHIP MEMORY MODULES & CARDS	**Release 7r11**	**Page 4-1**
4.1. Memory Module Nomenclature and General Features	**Release 7r11r13**	**Page 4.1-1**
4.1.1 Memory Module Nomenclature	Release 1-7	Page 4.1-1
4.1.2 Serial Presence Detect General Standard	Release 1-7r9	Page 4.1.2-1
4.1.2.1 SPD Appendix A, Table of Fundamental Memory Types	Release 8r9r12	Page 4.1.2.1-1
4.1.2.2 SPD Appendix B, Table of Superset Memory Types	Release 7r9r11	Page 4.1.2.2-1
4.1.2.3 SPD Appendix C, Specific PDs for FP and EDO DRAM	Release 7	Page 4.1.2.3-1
4.1.2.4 SPD Appendix D, Specific PDs for DDR SDRAM (Rev. 1.0)	Rel.7r11r12r13	Page 4.1.2.4-1
4.1.2.5 SPD Appendix E, Specific PDs for SDR SDRAM	Release 7r8$_2$c9r11r12	Page 4.1.2.5-1
4.1.2.6 SPD Appendix F, Specific PDs for Addr. MX ROM	Release 7	Page 4.1.2.6-1
4.1.2.7 SPD Appendix G, Not yet assigned	Release 9	Page 4.1.2.7-1
4.1.2.8 SPD Appendix H, Table of ESDRAM Attributes	Release 9	Page 4.1.2.8-1
4.1.2.9 SPD Appendix V, Specific PDs for VCSDRAM	Release 9	Page 4.1.2.9-1

Release 14

XILINX EXHIBIT 1010
Page 714

Section	Release #	Page #
4.1.2.10 SPD Appendix X, Specific SPDs for DDR2 SDRAM (Rev. 1.2)	Release 13r14	Page 4.1.2.10-1
4.2. One BYTE Modules	**Release 7**	**Page 4.2-1**
4.2.1 - 22 PIN SIP/SIMM 4 bit DRAM MODULE	Release 1-7	Page 4.2-1
4.2.2 - 24 PIN SIP/SIMM 4 bit DRAM MODULE	Release 1-7	Page 4.2-1
4.2.3 - 30 PIN SIP/SIMM 8 or 9 bit DRAM MODULE	Release 4-7	Page 4.2-1
4.2.4 - 30 PIN SIP/SIMM 1, 2, 4, 5, or 8 bits DRAM MODULE FAMILY	Release 1-7	Page 4.2-1
4.2.5 - 23/25/26/28 PIN ZIP/SIMM 1 or 4 bit DRAM MODULE FAMILY	Release 1-7	Page 4.2-2
4.2.6 - 60 PIN ZIP/SIMM 4 bit SRAM MODULE	Release 1-7	Page 4.2-2
4.2.7 - 70 PIN ZIP/SIMM 9 bit SRAM MODULE	Release 1-7	Page 4.2-2
FIGURE 4.2-1, 22, 24,& 30 PIN DRAM MODULES	Release 4-7	Page 4.2-3
FIGURE 4.2-2, 30 PIN DRAM MODULE FAMILY	Release 1-7	Page 4.2-4
FIGURE 4.2-3, 23/25/26/28 PIN DRAM MODULE FAMILY	Release 1-7	Page 4.2-5
FIGURE 4.2-4, 2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY	Release 1-7	Page 4.2-6
FIGURE 4.2-5, 64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY	Release 1-7	Page 4.2-7
4.3. Two BYTE Modules and Cards	**Release 7**	**Page 4.3-1**
4.3.1 - 76 PIN ZIP/SIMM 9 or 18 bit SRAM MODULE	Release 1-7	Page 4.3-1
4.3.2 - 40 PIN SIP/SIMM 1, 2, 4, 5, 8, 9, 16, or 18 DRAM MOD FAMILY	Release 1-7	Page 4.3-1
4.3.3 - 60 PIN DRAM 16 or 18 bit CARD FAMILY	Release 2-7	Page 4.3-1
4.3.4 - 68 PIN MULTIPLE TECHNOGY MEMORY 16 bit CARD FAMILY	Release 3-7	Page 4.3-1
FIGURE 4.3-1, 2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY	Release 1-7	Page 4.3-3
FIGURE 4.3-2, 40 PIN DRAM MODULE FAMILY	Release 1-7	Page 4.3-4
FIGURE 4.3-3A, 60 PIN DRAM CARD FAMILY PIN CONNECTIONS	Release 2-7	Page 4.3-5
FIGURE 4.3-3B, 60 PIN CARD FAMILY BLOCK DIAGRAMS	Release 2-7	Page 4.3-6
FIGURE 4.3-4A, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY	Release 3-7	Page 4.3-7
FIGURE 4.3-4B, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TRUTH TABLES	Release 3-7	Page 4.3-8
4.4. Four BYTE Modules and Cards	**Release 7**	**Page 4.4-1**
4.4.1 - 64 & 72 PIN ZIP/SIMM 32 bit SRAM MODULE	Release 6-7	Page 4.4.1-1
FIGURE 4.4.1-1, 16K TO 4M BY 32, 64 & 72 PIN SRAM MODULE FAMILY	Release 6-7	Page 4.4.1-2
4.4.2 - 72 PIN SIMM 32 or 36 bit DRAM MODULE FAMILY	Release 6-7	Page 4.4.2-1
- 72 PIN SIMM 36 or 39 DRAM ECC MODULE FAMILY	Release 6-7	Page 4.4.2-1
FIGURE 4.4.2-2 A, 256K TO 256M BY 36. 72 PIN DRAM MODULE PINOUT	Release 6-7c8	Page 4.4.2-3
FIGURE 4.4.2-2 B⇒K, 72 PIN 36 BIT DRAM SIMM BLOCK DIAGRAMS	Release 6-7	Page 4.4.2-4⇒13
FIGURE 4.4.2-3 A, 256K TO 256M BY 32, 36. & 40 BIT 72 PIN DRAM MODULE	Release 6-7	Page 4.4.2-14
FIGURE 4.4.2-3 B⇒C 72 PIN 32, 36, & 40 BIT DRAM SIMM BLOCK DIAGRAMS	Release 6-7	Page 4.4.2-15⇒16
4.4.3 - 88 PIN, 32/36/39 bit DRAM CARD FAMILY	Release 6-7	Page 4.4-1
FIGURE 4.4.3-1 A, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY	Release 6-7	Page 4.4.3-3
FIGURE 4.4.3-1 B, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY CONFIGURATION TABLES	Release 6-7	Page 4.4.3-4
FIGURE 4.4.3-1 C, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-5
FIGURE 4.4.3-1 D, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-6
FIGURE 4.4.3-1 E, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-7
FIGURE 4.4.3-1 F, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-8
- 88 PIN, 40 bit DRAM CARD FAMILY	Release 4-7	Page 4.4.3-1
FIGURE 4.4.3-2 A, 256K TO 128M BY 40 DRAM CARD	Release 4-7	Page 4.4.3-9
FIGURE 4.4.3-2 B, 256K TO 128M BY 40 DRAM CARD PD TRUTH TABLE	Release 4-7	Page 4.4.3-10
FIGURE 4.4.3-2 C, 256K TO 64M BY 40 DRAM CARDUSING BY 4 DEVICES	Release 4-7	Page 4.4.3-11
FIGURE 4.4.3-2 D, 512K TO 128M BY 40 DRAM CARD USING BY 4 DEVICES	Release 4-7	Page 4.4.3-12

Release 14

XILINX EXHIBIT 1010
Page 715

Section	Release #	Page #
FIGURE 4.4.3-2 E, 512K TO 32M BY 40 DRAM CARD USING BY 8 DEVICES	Release 4-7	Page 4.4.3-13
FIGURE 4.4.3-2 F, 1M TO 64M BY 40 DRAM CARD USING BY 8 DEVICES	Release 4-7	Page 4.4.3-14
4.4.4 - 72 PIN 32 or 36 bit DRAM SO-DIMM FAMILY	Release 5-7	Page 4.4.4-1
FIGURE 4.4.4- A 32 & 36 BIT 72 PIN DRAM SO-DIMM PINOUT, PRESENCE DETECT & CONFIGURATION TABLES	Release 6-7	Page 4.4.4-1
FIGURE 4.4.4-B-D 32 & 36 BIT DRAM SO-DIMM BLOCK DIAGRAMS	Release 5-7	Page 4.4.4-2⇒5
4.4.5 - 88 PIN 32 or 36 bit DRAM SO-DIMM FAMILY	Release 5-7	Page 4.4.5-1
FIGURE 4.4.5-A, 88 PIN 32 & 36 BIT DRAM SO-DIMM PINOUT	Release 6-7	Page 4.4.5-2
FIGURE 4.4.5-B, 88 PIN 32 & 36 BIT DRAM SO-DIMM PD TRUTH TABLES	Release 6-7	Page 4.4.5-3
FIGURE 4.4.5-C⇒F, 88 PIN 32 & 36 BIT DRAM SO-DIMM BLOCK DIAGRAMS	Release 6-7	Page 4.4.5-4⇒7
4.4.6 - 112 PIN 32 bits MPDRAM SO-DIMM FAMILY	Release 5-7	Page 4.4.6-1
FIGURE 4.4.6-A, 112 PIN 32 BIT MPDRAM DIMM PINOUT	Release 6-7	Page 4.4.6-2
FIGURE 4.4.6- B, C, 112 PIN 32 BIT MPDRAM DIMM PD TRUTH TABLES AND BLOCK DIAGRAMS	Release 6-7	Page 4.4.6-3, 4
4.4.7 - 80 PIN 32 bit EEPROM SIMM FAMILY	Release 4-7c8	Page 4.4.7-1
FIGURE 4.4.7-A, 128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES	Release 4-7	Page 4.4.7-3
FIGURE 4.4.7-B, 128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM	Release 4-7	Page 4.4.7-4
4.4.8 - 100 PIN 32, 36, or 40 BIT DRAM, SDRAM, ROM DIMM FAMILY	Release 7	Page 4.4.8-1
FIGURE 4.4.8-B & C, 32, 36, or 40 bit 100 PIN MODULE PINOUT	Release 7c8	Page 4.4.8-3, 4
FIGURE 4.4.8-D, 32, 36, or 40 bit 100 PIN MODULE PIN COMPARISON	Release 7	Page 4.4.8-5
FIGURE 4.4.8-E, 32, 36, or 40 bit 100 PIN MODULE CLOCK WIRING	Release 7c8	Page 4.4.8-6
FIGURE 4.4.8-F⇒AE, 32, 36, or 40 bit 100 PIN MODULE BLOCK DIAGRAMS	Release 7c8	Page 4.4.8-7⇒32
4.5. Eight BYTE Modules and Cards	**Release 7r8r9r12**	**Page 4.5-1**
4.5.1 - 168 PIN Buffered DRAM, 64, 72, or 80 Bit DIMM FAMILY	Release 6-7	Page 4.5.1-1
FIGURE 4.5.1-A-B, 64, 72, or 80 BIT SIMM PINOUT, TOP & BOTTOM HALVES	Release 4-7r9	Page 4.5.1-2,3
FIGURE 4.5.1-C, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 6-7	Page 4.5.1-4
FIGURE 4.5.1-D, 64, 72, & 80 BIT DRAM SIMM Capacity Table	Release 4-7	Page 4.5.1-5
FIGURE 4.5.1-E-AB, 64, 72, & 80 BIT CONFIGURATION BLOCK DIAGRAMS	Release 4-c7c8	Page 4.5.1-6-29
4.5.2 - 200 PIN SDRAM, 64, 72, or 80 DIMM FAMILY	Release 5-7c8c9r11	Page 4.5.2-1
FIGURE 4.5.2-A, B, 8 -BYTE SDRAM DIMM PINOUT	Release 5-7r8r11	Page 4.5.2-3,4
FIGURE 4.5.2- C, 8-BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7	Page 4.5.2-5
FIGURE 4.5.2-D, E, 8-BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.2-6
FIGURE 4.5.2-F-M, 8-BYTE SDRAM DIMM BLOCK DIAGRAMS	Release 5-7	Page 4.5.2-7,14
4.5.3 - 168 PIN Unbuffered DRAM, 64, 72, or 80 DIMM FAMILY with SPD	Release 5-7	Page 4.5.3-1
FIGURE 4.5.3-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 5-7r9	Page 4.5.3-2,3
FIGURE 4.5.3-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.3-5
FIGURE 4.5.3-E, Pinout comparison, 168P DRAM & SDRAM	Release 5-7c8	Page 4.5.3-6
FIGURE 4.5.3- F, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7r8-1	Page 4.5.3-7
FIGURE 4.5.3-G-U, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5-7r8	Page 4.5.3-8,20
4.5.4 - 168 PIN Unbuffered SDRAM, 64, 72, or 80 DIMM FAMILY with SPD	Release 5-7c8	Page 4.5.4-1
FIGURE 4.5.4-A, B, 8 -BYTE SDRAM DIMM PINOUT	Release 5-7r9	Page 4.5.4-2,3
FIGURE 4.5.4- C, 8-BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7r8	Page 4.5.4-4
FIGURE 4.5.4-E, 8-BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7r8	Page 4.5.4-6
FIGURE 4.5.4-I-AK, 8-BYTE SDRAM DIMM BLOCK DIAGRAMS	Release 5-7r8r9	Page 4.5.4-10⇒38
4.5.5 - 144 PIN Unbuffered DRAM, 64, or 72, SO-DIMM FAMILY with SPD	Release 5-7r8	Page 4.5.5-1
FIGURE 4.5.5-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 5-7r9	Page 4.5.5-2,3

Release 14

XILINX EXHIBIT 1010
Page 716

Section	Release #	Page #
FIGURE 4.5.5-C, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.5-4
FIGURE 4.5.5-E, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7	Page 4.5.5-6
FIGURE 4.5.5-F-AB, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5-7r8	Page 4.5.5-7⇒16
4.5.6 - 144 PIN Unbuffered SDRAM, 64, or 72 SO-DIMM FAMILY with SPD	Release 5-7	Page 4.5.6-1
FIGURE 4.5.6-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 5-7r9	Page 4.5.6-2,3
FIGURE 4.5.6- C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7	Page 4.5.6-6
FIGURE 4.5.6-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.6-4
FIGURE 4.5.6-G-P, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5-7	Page 4.5.6-7⇒17
4.5.7 - 168 PIN Registered SDRAM, 64, 72 or 80 DIMM FAMILY with SPD	Release 8r11	Page 4.5.7-1
FIGURE 4.5.7-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 8r9	Page 4.5.7-2,3
FIGURE 4.5.7- C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 8	Page 4.5.7-4
FIGURE 4.5.7-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 8	Page 4.5.7-5
FIGURE 4.5.7-I-X, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 8c9r10r11	Page 4.5.7-9⇒24
4.5.8 - 144 PIN SGRAMSDRAM, 32 & 64 SO-DIMM FAMILY with SPD	Release 8r10	Page 4.5.8-1
FIGURE 4.5.8-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 8r9r10	Page 4.5.8-2,3
FIGURE 4.5.8- C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 8	Page 4.5.8-4
FIGURE 4.5.8-D-F, 8-BYTE DRAM DIMM LAYOUT CONSIDERATIONS	Release 8	Page 4.5.8-5⇒9
FIGURE 4.5.8-G-J, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 8r10	Page 4.5.8-10⇒13
4.5.9 - 144 PIN SGRAM SO-DIMM FAMILY	Release 9	Page 4.5.9-1
FIGS. 4.5.9-A & B, PIN ASSIGNMENTS	Release 9	Page 4.5.9-2,3
FIGURE 4.5.9-C, CLOCK NET ROUTING	Release 9	Page 4.5.9-6
FIGURE 4.5.9-D TO G, BLOCK DIAGRAMS	Release 9	Page 4.5.9-7⇒10
4.5.10 - 184 PIN UNBUFFERED DDR SDRAM DIMM FAMILY	Release 9	Page 4.5.10-1
FIGURES. 4.5.10-A, & B, PIN ASSIGNMENTS	Release 9r12	Page 4.5.10-2,3
FIGURES. 4.5.10-C, SUMMARY OF FEATURES AND PIN DESCRIPTION	Release 9	Page 4.5.10-4
FIGURE 4.5.10-D, SPD TABLE & INFORMATION	Release 9	Page 4.5.10-5
FIGURE 4.5.10-E, COMPARISON OF 184 PIN UNBUFFERED SDR SDRAM & DDR SDRAM DIMM--	Release 9	Page 4.5.10-6
FIGURE 4.5.10-F, KEYING METHODOLOGY	Release 9	Page 4.5.10-7
FIGURE 4.5.10-G & H, VDDID DEFINITION	Release 9	Page 4.5.10-8 & 9
FIGURES 4.5.10-I through P, CONFIGURATION BLOCK DIAGRAM--	Release 9	Page 4.5.10-10⇒17
4.5.11 - 184 PIN UNBUFFERED SDR SDRAM DIMM FAMILY	Release 10	Page 4.5.11-1
FIGURES. 4.5.11-A, & B, PIN ASSIGNMENTS	Release 10	Page 4.5.11-2,3
FIGURES. 4.5.11-C, SUMMARY OF FEATURES AND PIN DESCRIPTION	Release 10	Page 4.5.11-4
FIGURE 4.5.11-D, SPD TABLE & INFORMATION	Release 10	Page 4.5.11-5
FIGURE 4.5.11-E, COMPARISON OF 184 PIN UNBUFFERED SDR SDRAM & DDR SDRAM DIMM--	Release 10	Page 4.5.11-6
FIGURE 4.5.11-F, KEYING METHODOLOGY	Release 10	Page 4.5.11-7
FIGURE 4.5.11-G & H, VDDID DEFINITION	Release 10	Page 4.5.11-8 & 9
FIGURE 4.5.11-I & J, CLOCK LAYOUT	Release 10	Page 4.5.11-10 & 11
FIGURE 4.5.11-G & H, FET SWITCH STRUCTURE	Release 10	Page 4.5.11-12
FIGURES 4.5.11-L through U, CONFIGURATION BLOCK DIAGRAM--	Release 10	Page 4.5.11-13⇒23
4.5.12 - 184 PIN DIMM FAMILY SUPPLEMENTARY DESIGN STANDARDS	Release 10	Page 4.5.12-1, 2
FIGURES 4.5.12-A through Q, CONFIGURATION BLOCK DIAGRAM--	Release 10	Page 4.5.12-3⇒19
FIGURE 4.5.12-R & S, CLOCK LAYOUT	Release 10	Page 4.5.12-20⇒ 23
FIGURES. 4.5.12-TA, & TB, 184P DDR REGISTERED DIMM PIN ASSIGNMENTS	Release 10	Page 4.5.12-24⇒26

XILINX EXHIBIT 1010
Page 717

Section	Release #	Page #
4.5.13 - 144 & 168 PIN PROCESSOR ENHANCED MEMORY MODULE FAMILIES WITH EDO-DRAM OR SDRAM	Release 10	Page 4.5.13-1
4.5.13.1, PEMM SPECIFIC TERMS AND DEFINITIONS	Release 10	Page 4.5.13-2
4.5.13.2, PEMM MODES OF OPERATION	Release 10	Page 4.5.13-3⇒7
4.5.13.3, REPRESENTATIVE BLOCK DIAGRAMS	Release 10	Page 4.5.13-8⇒12
4.5.14 - 240 PIN UNBUFFERED AND REGISTERED DDR2 SDRAM DIMM FAMILY	Release 12	Page 4.5.14-1
FIGURES 4.5.14-A, & B, PIN ASSIGNMENTS	Release 12	Page 4.5.14-2,3
FIGURE 4.5.14-C, PIN DESCRIPTION	Release 12	Page 4.5.14-4
FIGURE 4.5.14-D, PIN SUMMARY	Release 12	Page 4.5.14-5
4.6. Sixteen BYTE Modules	Release 7	Page 4.6-1
4.6.1 - 278 PIN Buffered SDRAM, 144 Bit DIMM FAMILY	Release 7	Page 4.6.1-1
FIGURE 4.6.1-A,B,C, 144 BIT SIMM PINOUT, TOP, MIDDLE, & BOTTOM PARTS	Release 7c8	Page 4.6.1-2,3,4
FIGURE 4.6.1-D, 144 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 7	Page 4.6.1-5
FIGURE 4.6.1-E, F, 144 BIT SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.6.1-6
FIGURE 4.6.1-G, H, 144 BIT SDRAM CONFIGURATION BLOCK DIAGRAMS	Release 7	Page 4.6.1-7, 8
4.20 - MODULE SPECIFICATION APPENDIX	Release 11r12r13	Page 4.20-1
4.20.1 - Standard Template for JEDEC Module Specification Standards	Release 11	Page 4.20.1-1⇒4
4.20.2 - 168 Pin PC133 SDRAM Registered DIMM Design Specification	Release 11	Page 4.20.2-1⇒71
4.20.3 - 144 Pin PC133 SDRAM Unbuffered SO-DIMM Reference Design Specification	Release 11	Page 4.20.3-1⇒26
4.20.4 - 184 Pin PC1600/2100 DDR SDRAM Registered DIMM Design Specification	Release 11r12	Page 4.20.4-1⇒61
4.20.5 - 184 Pin PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification	Release 11r12	Page 4.20.5-1⇒41
4.20.6 - 200 Pin PC3200/PC2700 DDR SDRAM Unbuffered SO-DIMM Reference Design Spec.	Release 11r13	Page 4.20.6-1⇒28
4.20.7 - 184 Pin, PC2700/3200 DDR SDRAM Registered DIMM Reference Design Specification, Rev. 2.0	Release 12r14	Page 4.20.7-1⇒58
4.20.8 - 184 Pin, PC3200/PC2700 DDR SDRAM Unbuffered DIMM with TSOP-Based DRAMs Reference Design Specification	Release 12r13	Page 4.20.8-1⇒44
4.20.9 - 100 Pin, DDR SDRAM Unbuffered 32b DIMM Reference Design Specification, Rev 1.1	Release 13r14	Page 4.20.9-1⇒32
4.20.10 - 240-Pin PC2-3200/PC2-4300 DDR2 SDRAM Registered DIMM Reference Design Specification, Rev. 1.0	Release 14	Page 4.20.10-1⇒68
4.20.11 - 200-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev. 0.52	Release 14	Page 4.20.11-1⇒44
4.20.12 - 214-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered MicroDIMM Reference Design Specification, Rev 0.5	Release 14	Page 4.20.12-1⇒28
4.20.13 - 240-Pin PC2-3200/PC2-4300 DDR2 SDRAM Unbuffered DIMM Reference Design Specification, Rev. 1.0	Release 14	Page 4.20.13-1⇒54
5 PROGRAMMABLE LOGIC AND ASIC DEVICES	**Release 1**	**Page 5-1**
5.1 Pin Out Standards	**Release 1**	**Page 5-1**
5.1.1 PIN-OUT STANDARDS FOR PLD DIP TO SCC CONVERSION	**Release 4**	**Page 5-1**
5.1.1.1 - 20 PIN DIP to 20 TERMINAL SCC, 0.350" BY 0.350", Fig. 5-1	Release 1	Page 5-1
5.1.1.2 - 24 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5-2	Release 1	Page 5-1
5.1.1.3 - 28 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5-2	Release 1	Page 5-1
5.1.1.4 - 24 PIN FUNCTIONS IN 28 PIN DIP & 28 TERMINAL SCC, Fig. 5-9	Release 1	Page 5-1
5.1.1.5 - 20 PIN FUNCTIONS IN 28 TERMINAL SCC AND 24 PIN DIP FOR HIGH SPEED OPERATION, Fig. 5-11	Release 4	Page 5-1

Section	Release #	Page #
5.1.2 POWER PIN LOCATIONS FOR PLD and ASIC DEVICES	**Release 1**	**Page 5-1**
5.1.2.1 - POWER PIN LOCATIONS FOR ECL PLD IN DIP	Release 1	Page 5-1
5.1.2.2 - POWER PIN LOCATIONS FOR TTL PLD IN DIP and CC	Release 1	Page 5-1
5.1.2.3 - POWER PIN LOCATIONS FOR TTL PROGRAMMABLE ASIC IN DIP and CC	Release 1	Page 5-1
5.1.2.4 - POWER PIN LOCATIONS FOR PLD IN 132 PIN QFP	Release 1	Page 5-1
5.1.3 Nomenclature for FPLD	**Release 1**	**Page 5-1**
5.1.4 PLD Data Transfer Format	**Release 1**	**Page 5-1**
5.1.5 PLD Standard OUTPUT LOADS	**Release 5**	**Page 5-1**
FIGURE 5-1, 20 PIN DIP TO 20 TERMINAL CC PLD CONVERSION	Release 1	Page 5-3
FIGURE 5-2, 24 & 28 PIN DIP TO 27 TERMINAL CC CONVERSION	Release 2	Page 5-4
FIGURE 5-3, POWER PIN PLACEMENT FOR ECL PLD	Release 1	Page 5-5
FIGURE 5-4, 40 PIN DIP PLD POWER PIN PLACEMENT	Release 1	Page 5-6
FIGURE 5-5, 44 TERMINAL CC POWER PIN PLACEMENT	Release 1	Page 5-7
FIGURE 5-6, 48 & 64 PIN DIP ASIC POWER PIN PLACEMENT	Release 1	Page 5-8
FIGURE 5-7, 52, 68, & 84 TERMINAL CC ASIC POWER PIN PLACEMENT	Release 1	Page 5-9
FIGURE 5-8A, PLD STANDARD LOADS, DEFINITIONS	Release 5	Page 5-11
FIGURE 5-8B, PLD STANDARD LOAD CIRCUIT	Release 5	Page 5-12
FIGURE 5-8C, PLD OUTPUT LOAD CALCULATIONS	Release 5	Page 5-13
FIGURE 5-8D, PLD AC LOAD LINES	Release 5	Page 5-14
FIGURE 5-9, 24 PIN PLD FUNCTIONS IN 28 PIN DIP AND SCC	Release 3	Page 5-15
FIGURE 5-10, 132 PIN PQFP POWER PIN LOCATIONS	Release 3	Page 5-16
FIGURE 5-11, HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS	Release 4	Page 5-17
6 APPLICABLE OTHER DOCUMENTS	**Release 1**	**Page 6-1**
6.1 - Standard Manufacturers Identification Code., JEDEC Publication No. 106A	**Release 1**	**Page 6-1**
6.2 - Interface Standard for Low Voltage TTL-Compatible Devices (LVTTL), JEDEC Standard No. 8 and Addendum No. 1	**Release 1**	**Page 6-1**
6.3 - Package Outlines, JEDEC Publication 95	**Release 1**	**Page 6-1**
6.4 - PLD Data Transfer Format, JEDEC Standard 3-B	**Release 1**	**Page 6-1**
6.5 - Nomenclature for FPLD, EIA Standard RS-428	**Release 1**	**Page 6-1**
6.6 - DDR SDRAM Device Specification, JESD-79	**Release 11**	**Page 6-1**
Annex A - (Informative) Differences Between Release 14 and Release 13	**Release 14**	**Page A-1**

3.11.5 SDRAM & SGRAM Architectural and Operational Features

The following standards describe features or characteristics that are applicable to one or more of the SDRAM devices described in section 3.11 of Std. 21-C. This section is being reorganized in Release 9 to accommodate several new categories of devices being covered. The original Standards included in this section covered only Single Data Rate (SDR) SDRAMs (these devices were initially just referred to as SDRAM). This coverage has expanded to include Double Data Rate (DDR) SDRAMs, Enhanced SDRAMs (ESDRAM), and Virtual Channel SDRAM (VCSDRAM). The new organization of Section 3.11.5 brings together into one sub-section all standards specifically applicable to one class of device. All standards in the following section that are defined for SDRAM, are also applicable to SGRAM, (even though SGRAM is not mentioned), unless SGRAM is specifically excluded.

A complete Table of Contents of all SDRAM & SGRAM Features follows.

3.11.5.1 - General SDRAM Functions

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE FOR CKE

3.11.5.1.3 - SDRAM MODE REGISTER ARCHITECTURE

3.11.5.1.4 - POWER ON SEQUENCE (RECOMMENDED)

3.11.5.1.5 - AUTO PRECHARGE

3.11.5.1.6 - PRECHARGE ALL BANKS

3.11.5.1.7 - MODE REGISTER WRITE TIMING

3.11.5.1.8 - AUTO REFRESH

3.11.5.1.9 - WRITE LATENCY

3.11.5.1.10 - DQM LATENCY FOR READS AND WRITES

3.11.5.1.11 - PRECHARGE TIMING FOR READS

3.11.5.1.12 - COLUMN ADDRESS TO COLUMN ADDRESS DELAY

3.11.5.1.13 - CKE TIMING FOR POWER DOWN

3.11.5.1.14 - CKE TIMING FOR CLOCK SUSPEND

3.11.5.1.15 - SELF REFRESH ENTRY AND EXIT

3.11.5.1.16 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

3.11.5.1.17 - Full Page Burst Mode for SDRAM/SGRAM

3.11.5.1.18 - Deep Power Down Mode

3.11.5.2 - DDR Specific SDRAM Functions

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs/SGRAMs

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

3.11.5.2.7 - Burst Stop Command for DDR SDRAMs/SGRAMs
3.11.5.2.8 - DDR SDRAM/SGRAM Full Sequential Burst Ordering
3.11.5.2.9 - DDR SDRAM QS Coincident with Data
3.11.5.2.10 - Extended Mode Register Set for DDR SDRAM / SGRAM.
3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS
3.11.5.2.12 - Refresh Requirements
3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM
3.11.5.3 - ESDRAM Specific SDRAM Functions
3.11.5.3.1 - Read-AutoPrecharge Operation for SDR ESDRAM
3.11.5.3.2 - Read-AutoPrecharge Operation for DDR ESDRAM
3.11.5.3.3 - Cache Load Operation for SDR ESDRAM
3.11.5.3.4 - Cache Load Operation for DDR ESDRAM
3.11.5.3.5 - No Write Transfer, Mode of Operation for SDR ESDRAM
3.11.5.3.6 - No Write Transfer, Mode of Operation for DDR ESDRAM
3.11.5.4 - VCSDRAM Specific SDRAM Functions
3.11.5.4.1 - Command Table for Virtual Channel SDR SDRAM
3.11.5.4.2 - Command Table for Virtual Channel DDR SDRAM
3.11.5.4.3 - Virtual Channel SDR SDRAM Mode Register Architecture
3.11.5.4.4 - Virtual Channel DDR SDRAM Mode Register Architecture
3.11.5.5 - DDR2 Specific SDRAM Functions
3.11.5.6 - GDDR2 Specific SGRAM Functions
3.11.5.7 - GDDR3 Specific SGRAM Functions

XILINX EXHIBIT 1010
Page 721

3.11.5.1 - General SDRAM Functions

The Standards in this section are general functions that are applicable to both SDR and DDR SDRAM except where that function is specifically covered for a class of devices in one of the following sections.

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

This table defines the interface states required to execute the standard SDRAM operational functions. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE FOR CKE

This table defines the interface states required to execute the standard SDRAM operational functions with respect to the CKE input. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.1.3 - SDRAM & SGRAM MODE REGISTER ARCHITECTURE

This standard describes the architecture of the SDRAM & SGRAM internal MODE REGISTER and the codes that are allowable for use in it. This is applicable to both SDR & DDR devices.

3.11.5.1.4 through 3.11.5.1.17 — SDRAM OPERATIONAL CYCLES AND MODES

The following standards define and describe a number of operational cycles and modes of SDRAM. They are ordered roughly in the sequence in which they would be used in normal SDRAM operation.

3.11.5.1.4 - POWER ON SEQUENCE (RECOMMENDED)

This standard gives a recommended power, clock, and logic-level sequence to be used on power-up to prevent data bus contention.

3.11.5.1.5 - AUTO PRECHARGE

This standard gives the logic function used to active the AUTO-PRECHARGE function.

3.11.5.1.6 - PRECHARGE ALL BANKS

This standard gives the logic function used to activate the PRECHARGE-ALL-BANKS function.

3.11.5.1.7 - MODE REGISTER WRITE TIMING

This standard defines the logic sequence and timing required to write into the MODE REGISTER.

3.11.5.1.8 - AUTO REFRESH

This standard defines the logic state and interface sequence required to perform an AUTO REFRESH

3.11.5.1.9 - WRITE LATENCY

This standard defines WRITE LATENCY and illustrates it with a timing diagram.

3.11.5.1.10 - DQM LATENCY FOR READS AND WRITES

In this standard DQM LATENCY is defined and the relationships between the DQM signal and the interface data for READs and WRITEs is defined and shown in timing diagrams.

3.11.5.1.11 - PRECHARGE TIMING FOR READS

This standard describes the relationship between the assertion of a PRECHARGE command and data out from a READ command.

3.11.5.1.12 - COLUMN ADDRESS TO COLUMN ADDRESS DELAY

This standard defines constraints imposed on the CA to CA delay and illustrates them with a timing diagram.

3.11.5.1.13 - CKE TIMING FOR POWER DOWN

This standard describes the interface sequence required to place the SDRAM into the POWER-DOWN state using CKE.

3.11.5.1.14 - CKE TIMING FOR CLOCK SUSPEND

This standard describes the interface timing sequence when CKE is used to suspend the clock.

3.11.5.1.15 – SELF REFRESH ENTRY AND EXIT

This standard defines the logic states and timing sequence used to enter and exit the SELF–REFRESH mode.

3.11.5.1.16 – Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, this section defines the functionality that is required.

3.11.5.1.17 – Full Page Burst Mode for SDRAM/SGRAM

Full page burst mode is an optional feature for SDRAM/SGRAM. If full page burst mode is included in an SDRAM or SGRAM, this section gives the required functionality.

3.11.5.1.18 – Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, this section defines the functionality that is required.

XILINX EXHIBIT 1010
Page 723

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	Row (& Bank) active; Latch Row Address
	L	L	H	L	BA, A10	NOP[4]
	L	L	L	H	X	Auto-Refresh[5]
	L	L	L	L	Op-code	Mode Register Access[5]
ROW ACTIVE	H	X	X	X	X	NOP
	L	H	H	X	X	NOP
	L	H	L	H	BA, CA, A10	Begin Read; Latch CA; Determine AP[7]
	L	H	L	L	BA, CA, A10	Begin Write; Latch CA; Determine AP[7]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Precharge[8]
	L	L	L	X	X	ILLEGAL
READ	H	X	X	X	X	NOP (Continue Burst to End;=Row Active) [6]
	L	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)[6]
	L	H	H	L	BA	RESERVED (Term. Burst);⇒Row Active
	L	H	L	H	BA, CA, A10	Term Burst, New Read, Determine AP[3]
	L	H	L	L	BA, CA, A10	Term Burst, Start Write, Determine AP[3, 7]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Term Burst, Precharge Timing for Reads
	L	L	L	X	X	ILLEGAL
WRITE	H	X	X	X	X	NOP(Continue Burst to End;⇒Row Active)[6]
	L	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)[6]
	L	H	H	L	BA	RESERVED (Term Burst);⇒Row Active
	L	H	L	H	BA, CA, A10	Term Burst, Start Read, Determine AP[3, 7]
	L	H	L	L	BA, CA, A10	Term Burst, New Write, Determine AP[3]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Term Burst, Precharge[3]
	L	L	L	X	X	ILLEGAL
READ with AUTO Precharge	H	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)[6]
	L	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)[6]
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	ILLEGAL[2]
	L	H*	L	L	X	ILLEGAL
	L	L	H	X	BA, RA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
WRITE with AUTO Precharge	H	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)[6]
	L	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)[6]
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	ILLEGAL[2]
	L	H	L	L	X	ILLEGAL
	L	L	H	X	BA, RA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL

TABLE 3.11.5.1-1

SDRAM FUNCTION TRUTH TABLE

3.11.5.1.1 – SDRAM FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H	X	X	X	X	NOP⇒idle after tRP
	L	H	H	H	X	NOP⇒idle after tRP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	NOP[4]
	L	L	L	X	X	ILLEGAL
ROW Activating	H	X	X	X	X	NOP⇒Row Active after tRCD
	L	H	H	H	X	NOP⇒Row Active after tRCD
	L	H	H	L*	BA *	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
WRITE Recovering	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
Refreshing	H	X	X	X	X	NOP⇒idle after tRC*
	L	H	H	X	X	NOP⇒idle after tRC *
	L	H	L	X	X	ILLEGAL
	L	L	H	X	X	ILLEGAL
	L	L	L	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	X	ILLEGAL
	L	H	L	X	X	ILLEGAL
	L	L	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address Term = Terminate

CA = Column Address AP = Auto Precharge NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the ”2n–rule”, bus contention, but turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).
5. Illegal if any bank is not idle.

ILLEGAL = Device operation and/or data–integrity are not guaranteed

6. If the device is programmed to use full page burst mode, the action is NOP, continue burst.
7. The autoprecharge bit, AP, must be 0 in full page burst mode where the autoprecharge function is illegal

ILLEGAL = Device operation and/or data–integrity are not guaranteed

8. Precharge All Banks determined by state of A10

* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5.1–1

SDRAM FUNCTION TRUTH TABLE (Continued)

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE_{n-1}	CKE_n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Self-refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self-Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power-Down	H	X *	X	X	X	X	X	INVALID
	L	H *	H	X*	X*	X*	X	EXIT Power Down⇒ABI
	L	H *	L	H	H	H	X	EXIT Power Down⇒ABI
	L	H *	L	H	H*	L*	X	ILLEGAL
	L	H *	L	H*	L*	X*	X	ILLEGAL
	L	H*	L	L	X*	X*	X	ILLEGAL
	L	L	X	X*	X*	X	X	NOP(Maintain Low-Power Mode)
All Banks Idle[7]	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power-Down
	H	L	L	H	H	H	X	Enter Power-Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8]
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS
ABI = All Banks Idle
NOTES:

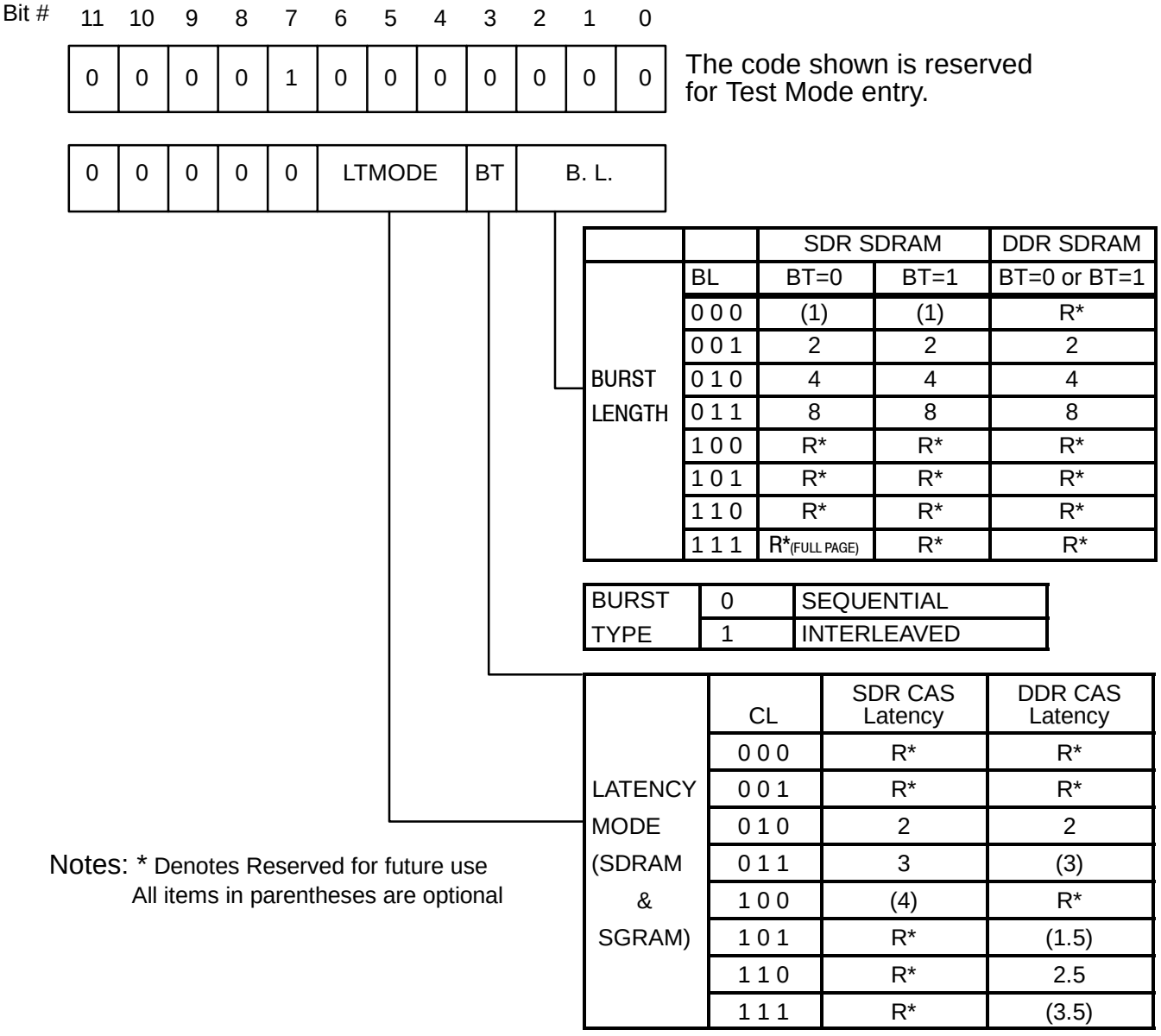
6. CKE Low-to-High transition will re-enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command.
* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5.1-2
SDRAM FUNCTION TRUTH TABLE for CKE

3.11.5.1.3 – SDRAM & SGRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM or SGRAM) chip. Its purpose is to store the mode-of-operation data. This data is written after power-on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{CAS}$ Latency (Defined separately for SDR and DDR devices), and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode-Register-Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

SDRAM Mode Register architecture:



		SDR SDRAM		DDR SDRAM
BURST LENGTH	BL	BT=0	BT=1	BT=0 or BT=1
	0 0 0	(1)	(1)	R*
	0 0 1	2	2	2
	0 1 0	4	4	4
	0 1 1	8	8	8
	1 0 0	R*	R*	R*
	1 0 1	R*	R*	R*
	1 1 0	R*	R*	R*
	1 1 1	R*(FULL PAGE)	R*	R*

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

	CL	SDR CAS Latency	DDR CAS Latency
LATENCY MODE (SDRAM & SGRAM)	0 0 0	R*	R*
	0 0 1	R*	R*
	0 1 0	2	2
	0 1 1	3	(3)
	1 0 0	(4)	R*
	1 0 1	R*	(1.5)
	1 1 0	R*	2.5
	1 1 1	R*	(3.5)

FIGURE 3.11.5.1-1
SDRAM & SGRAM MODE REGISTER ARCHITECTURE

3.11.5.1.4 - Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High-Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High-Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μS.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

3.11.5.1.5 - Auto Precharge

The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle. The following table defines the options available from AP during the column address portion of any cycle.

AP	Option
0	Do not auto precharge, leave bank active at end of burst.
1	Auto precharge bank specified by BA at end of burst.

The user must wait until the precharge is completed before issuing another command to the device. Timing for auto precharge is required to be the same as or less than the minimum requirement of external precharge.

The Autoprecharge Bit, AP, must be 0 in full page burst mode where the autoprecharge function is illegal.

The autoprecharge function is not allowed in full page burst mode since the end of the burst is indefinite. Therefore the autoprecharge bit, AP, is ignored during read or write commands if the mode register is set to full page burst mode.

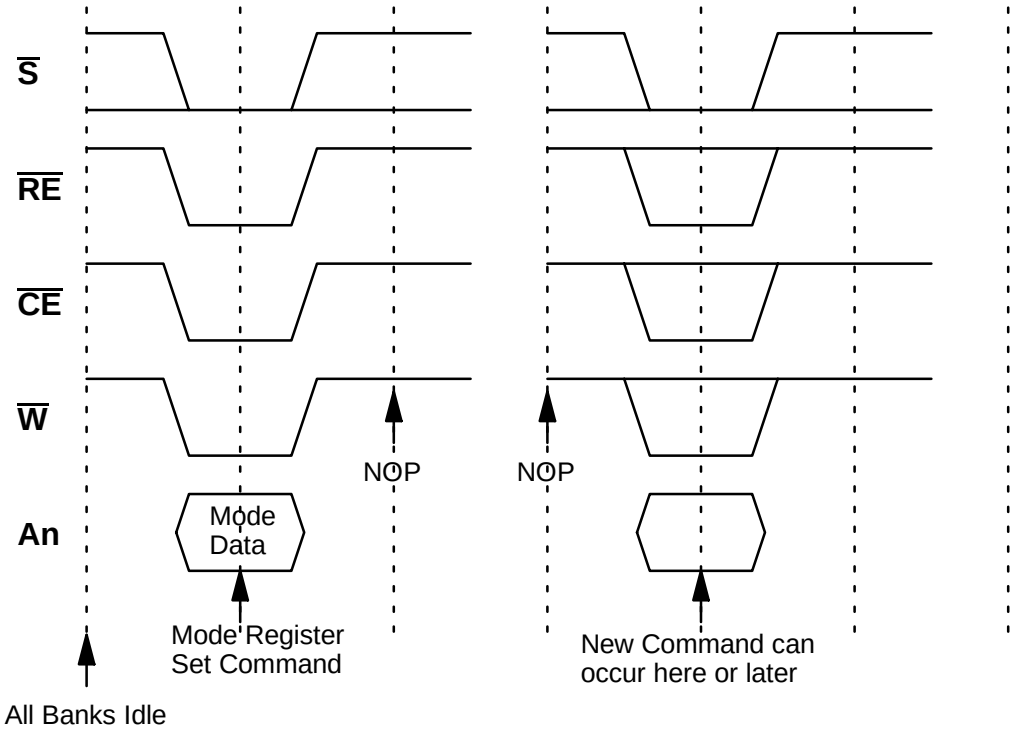
3.11.5.1.6 - Precharge All Banks

The user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks. BA is used to specify the bank to be precharge, and AP is used to indicate the precharge option. The following table defines the options available from AP during the precharge cycle.

PA	Option
0	Precharge bank specified by BA
1	Precharge All banks

3.11.5.1.7 – Mode Register Write Timing

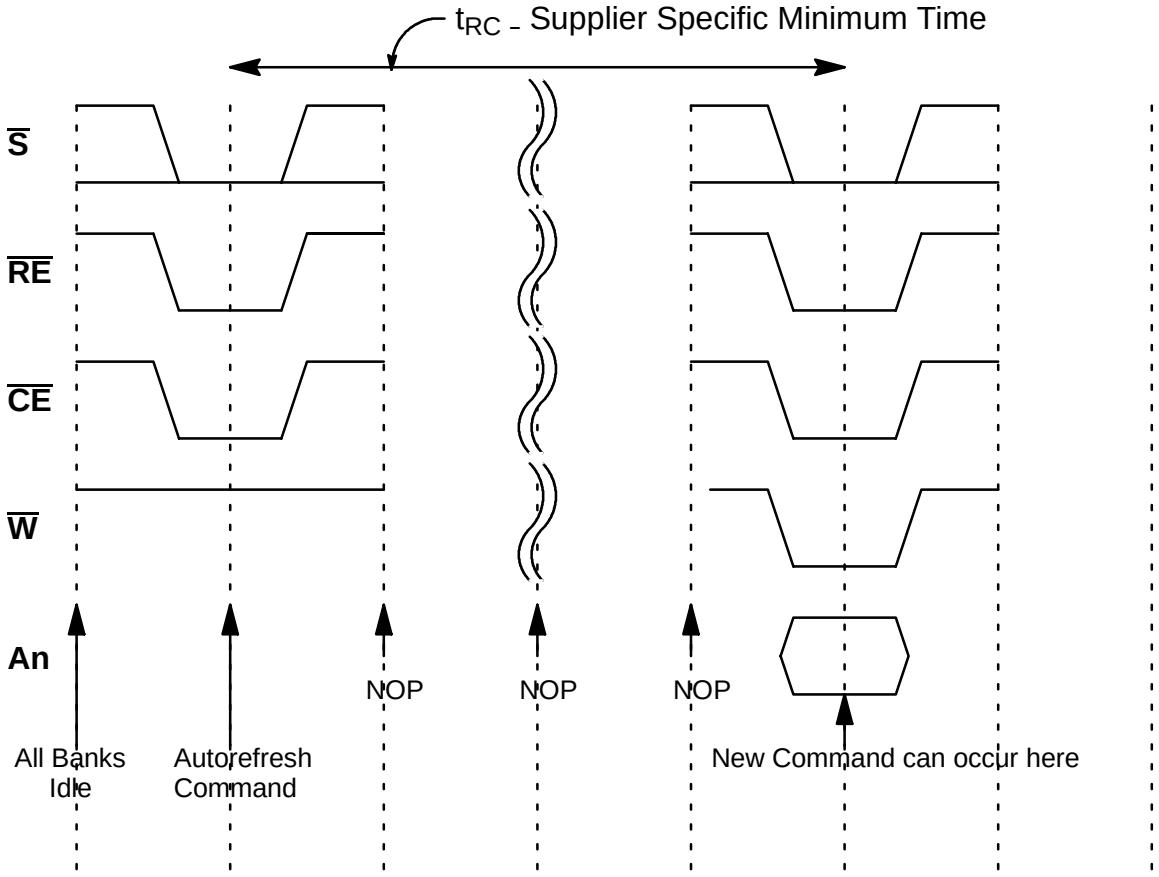
The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.1.8 - Auto Refresh

AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address being supplied by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE). Autorefresh is entered by asserting RE and CE on the same clock cycle. All banks will automatically precharge at the end of the refresh cycle. Additional commands must not be supplied to the device during the minimum refresh time specified. The following timing diagram illustrates the refresh cycle requirements.

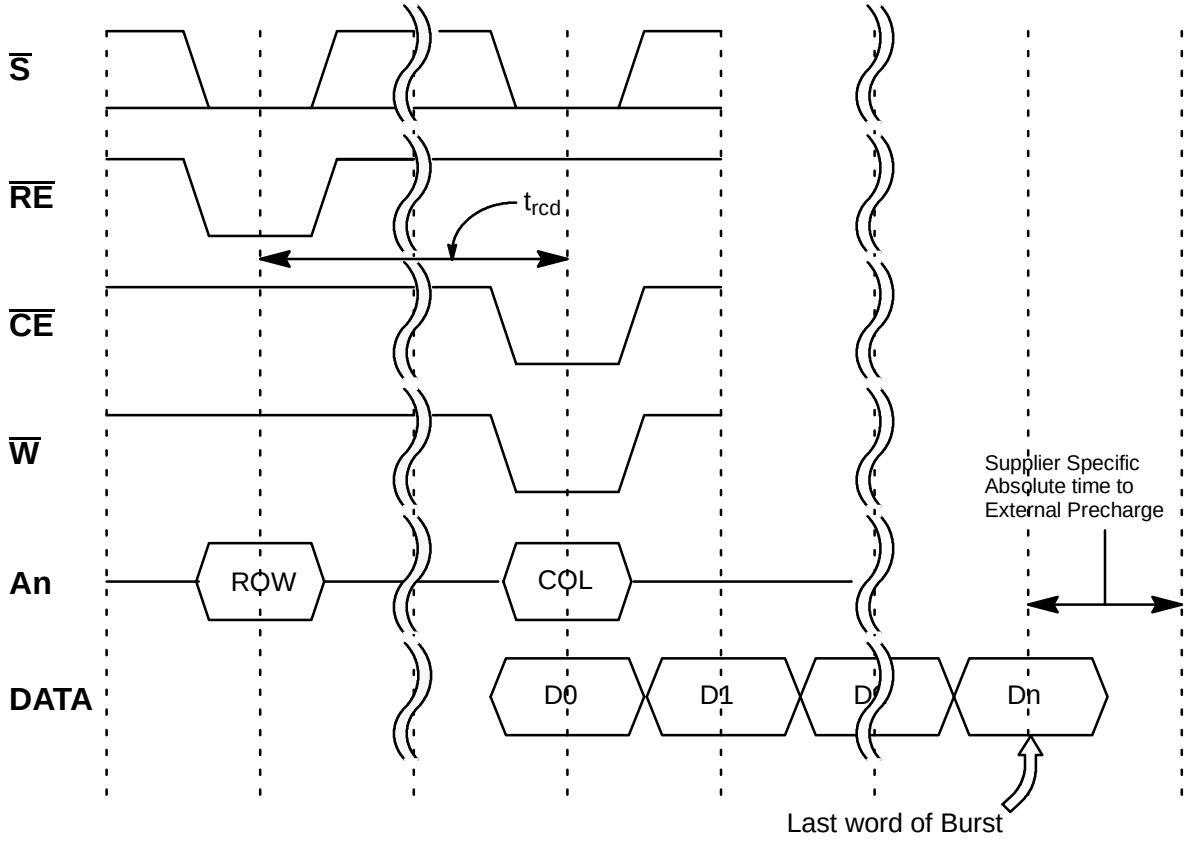


Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.9 – Write Latency

(Write Latency = 0)

Write Latency for SDR Synchronous DRAM shall be as defined as the clock cycle difference between the clock where write command and collumn address are asserted and the clock where first data to be written is asserted.

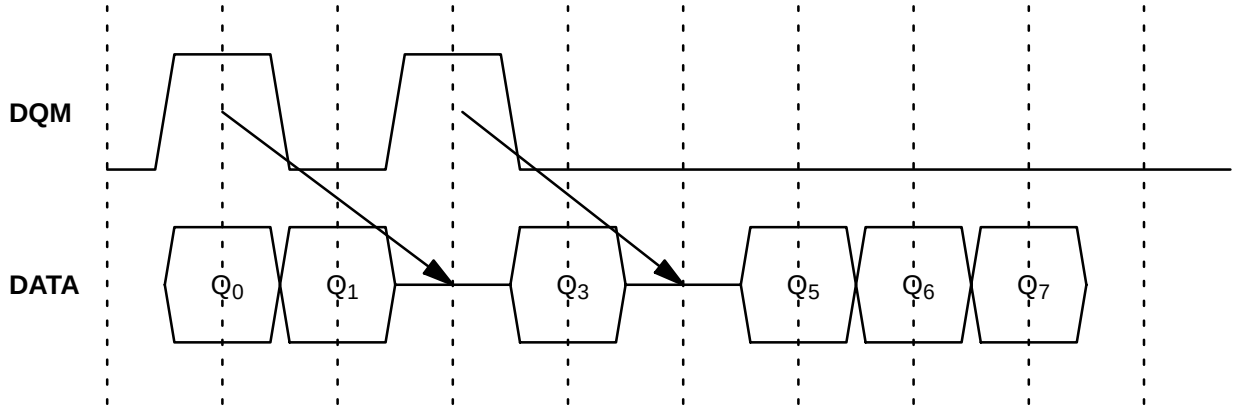


Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.1.10 – DQM Latency for Reads and Writes (DQM Write Latency = 0)

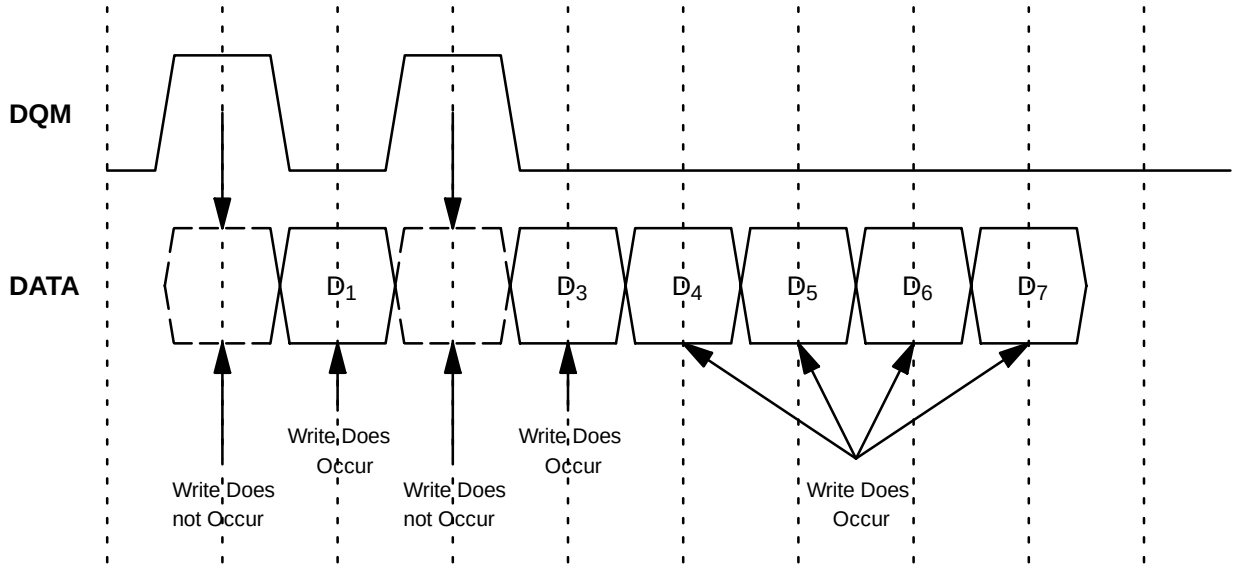
DQM is a multiple–function signal defined as the data mask for both reads and writes. During reads, DQM performs synchronous output enable. During writes, DQM performs write data masking. The requirement for high–speed operation, and the synchronous nature of SDRAM devices requires that DQM latency be different for reads than it is for writes.

For Reads, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the output bus has been forced to High–Z. The following timing diagram illustrates the standard of 2 clocks.



Note: Clock Low–to–high transitions occur at the dotted lines.

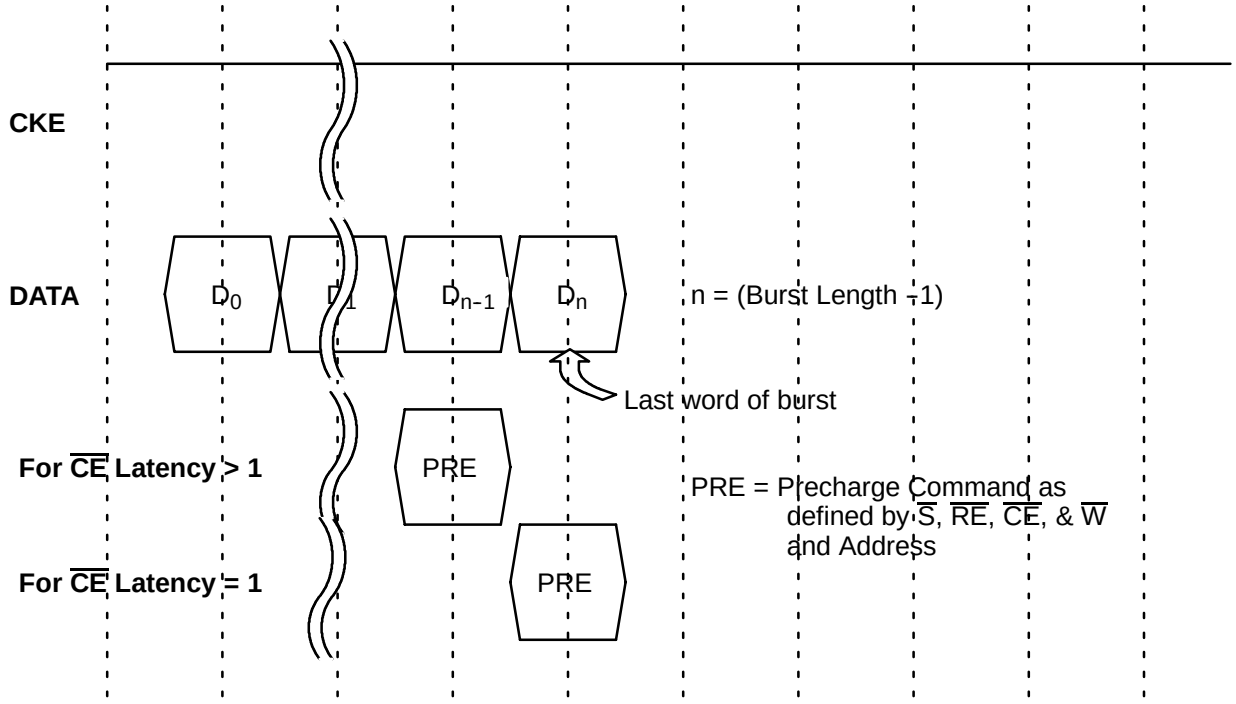
For Writes, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the write input data is inhibited. The following timing diagram illustrates the standard of 0 clocks.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.1.11 – Precharge Timing for Reads

The assertion of the precharge command has a direct relationship to the timing of data out for a read cycle. For a CE latency of 1, the minimum requirements is that the precharge command will be allowed to coincide with output of the last data from a bu;rst regardless of burst length. For a CE latency greater than 1, the minimum requirement is that the precharge command will be allowed to coincide with output of the next-to-last data from a burst, regardless of burst length, without interrupting burst data. The following timing diagrams illustrate the requirements.



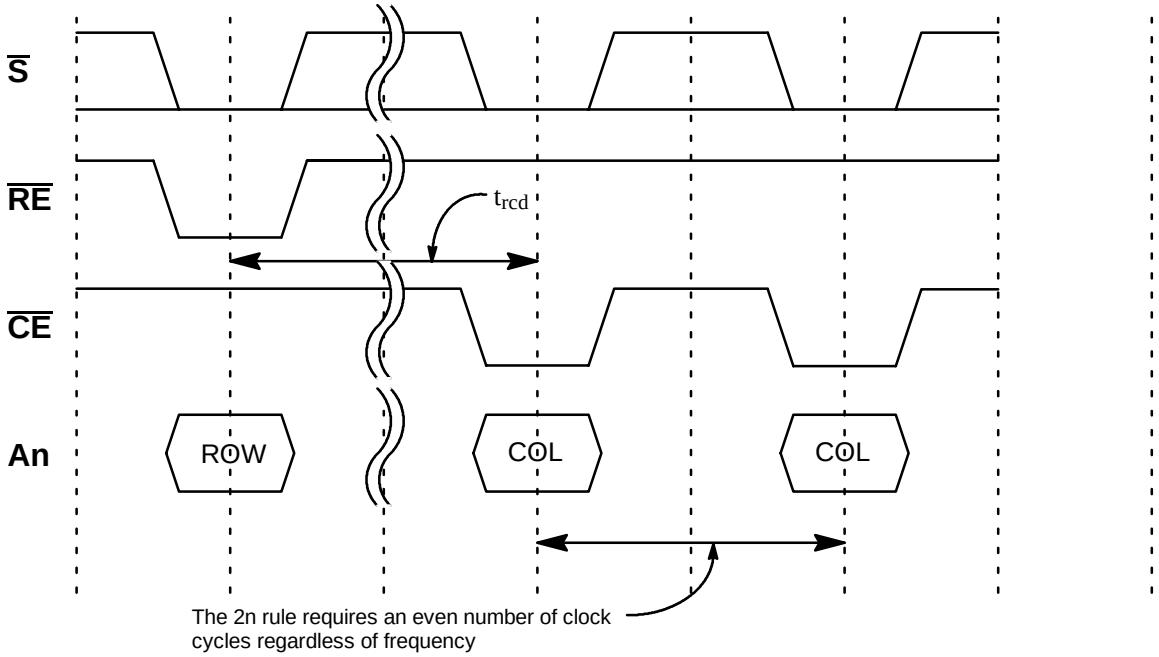
Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.12 - Column Address to Column Address Delay

The minimum column-address-to-column-address delay time, for page mode accesses, is two clock cycles, independent of operating frequency.

For interrupted bursts, column addresses must, at a minimum, follow the ”2n rule” while a read or write burst is in progress. 2n rule: after the initial read or write command, a new column address can be presented to the device every other clock cycle. That is, if the initial read-or-write command occured on an odd clock cycle, the new column addresses must presented on an odd clock cycle while the burst is in progress.

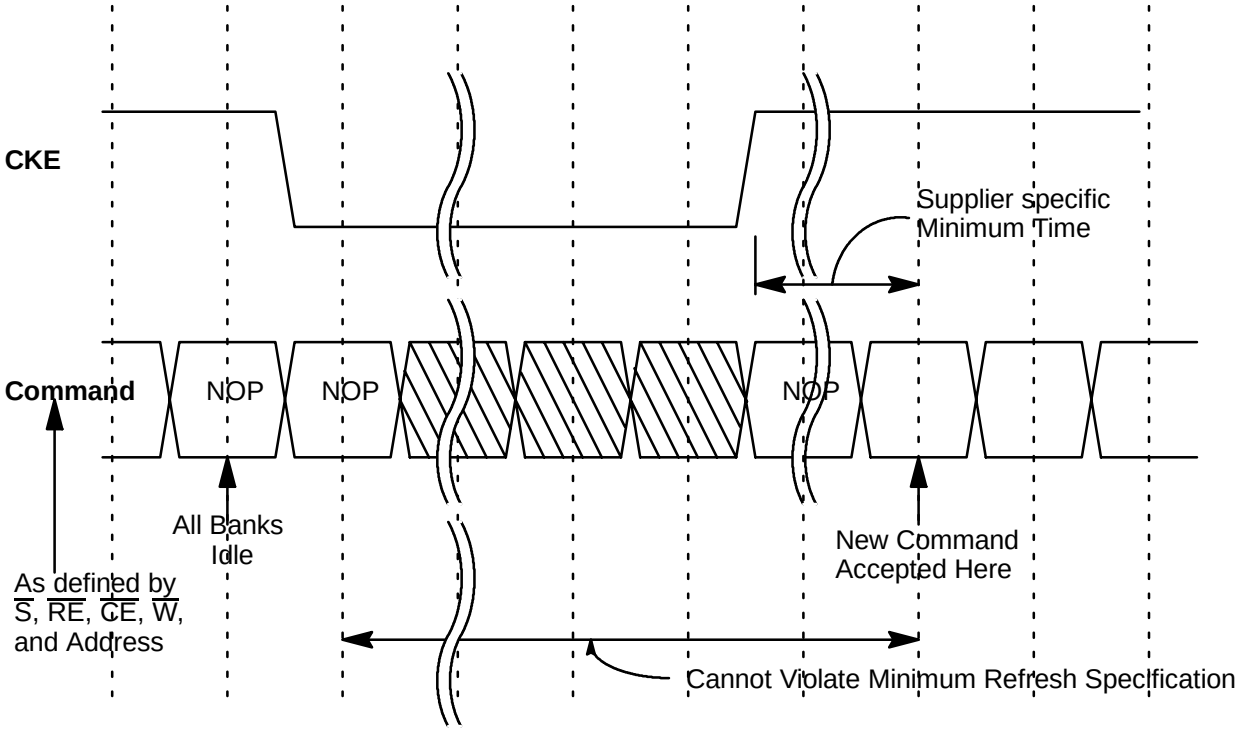
After the burst is completed, the 2n rule no longer applies, and a new column address may be presented to the device on any clock cycle. Essentially the 2n rule remains in effect for (CE Latency + burst length) clock cycles for reads and (write recovery + burst length) clock cycles for writes.



Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.13 – CKE Timing for Power Down

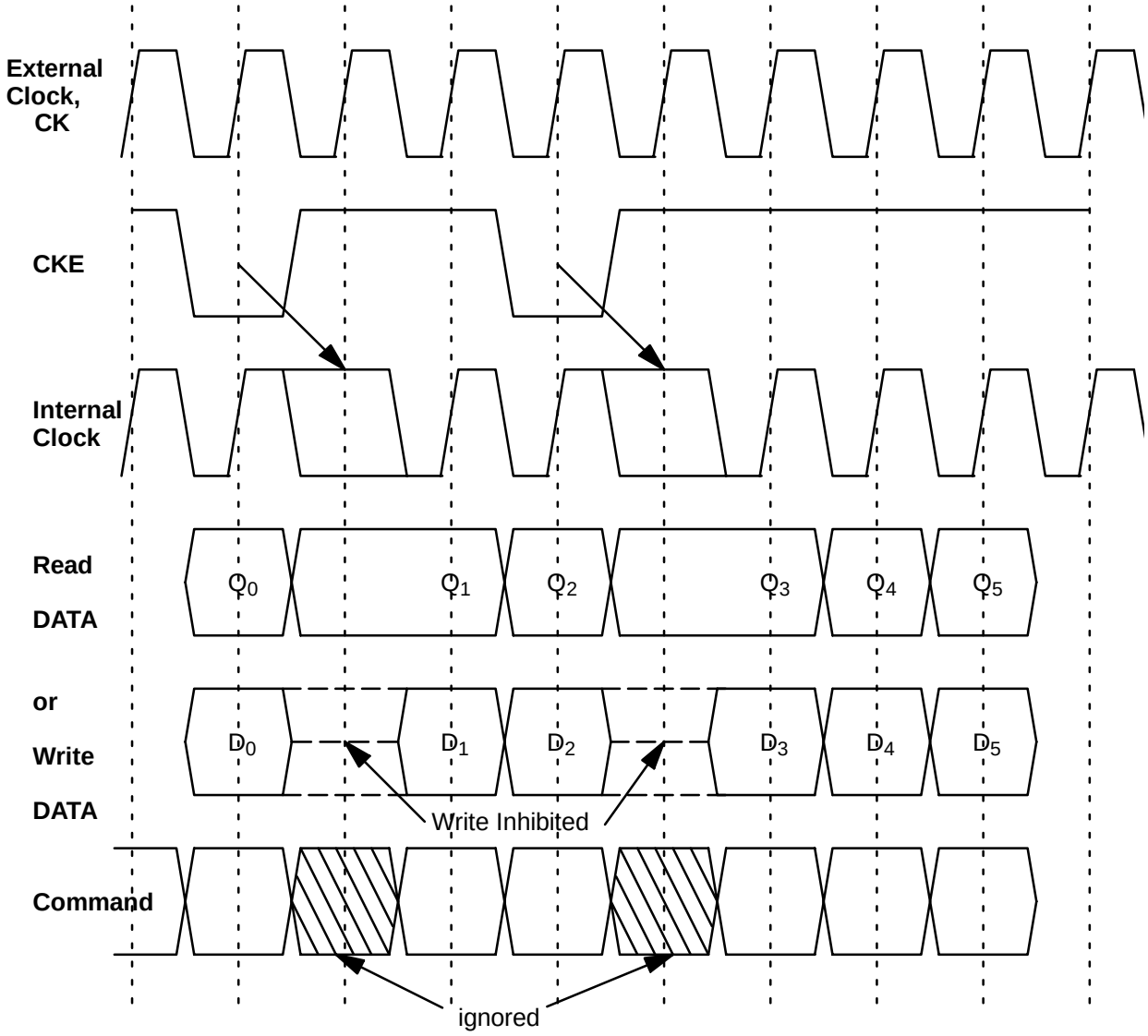
CKE is defined as the clock–enable signal and actually has the dual purpose of also being the signal that puts an SDRAM into a low power state. Using CKE to enter the low power state can only be performed while all internal banks of the device are precharged (IDLE). If all internal banks have been precharged, then CKE is used to gate the input buffers of the device. During power down the device is not refreshed. Therefore the minimum refresh specification still applies during power down. The following timing diagram illustrates power down mode.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.1.14 – CKE Timing for Clock Suspend

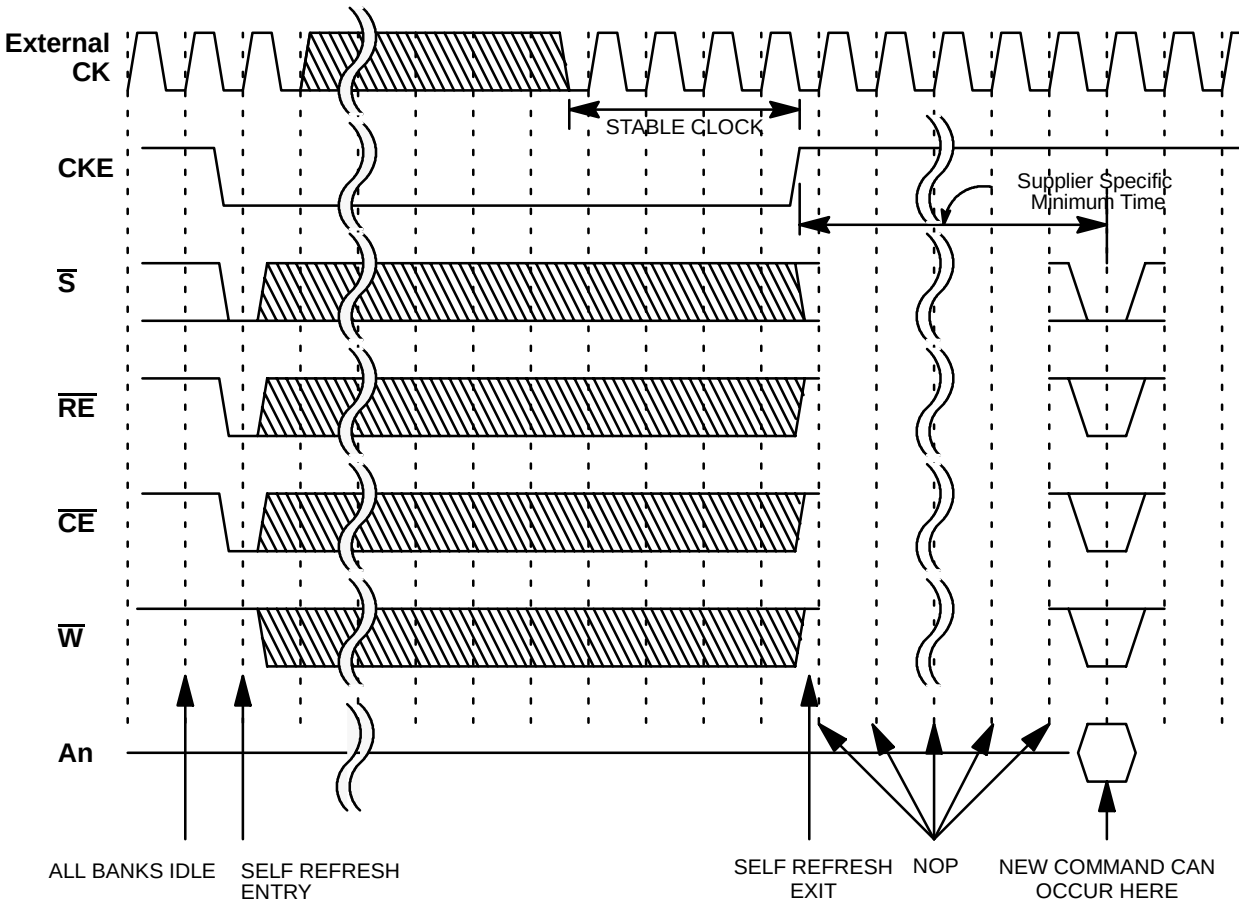
The following timing diagram is shown for CKE when 1 or more banks of the device are active. The effect on read data, write data, and command are all shown on the same diagram for reference only. The clock may be suspended for one or more clock cycles.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.1.15 – Self-Refresh Entry and Exit

In self refresh mode, the device refreshes itself without outside intervention. While the device is in self-refresh mode, CKE is the only enabled input to the device. All other inputs including the clock are disabled and any input is ignored. Self-refresh mode is entered by precharging all banks and then inserting an auto-refresh command with CKE low. Exit from self-refresh mode is accomplished by starting the clock and then asserting CKE. NOP commands must be asserted for a supplier-specified minimum period, which must include 3 clocks, to allow the device to return to the IDLE state.



3.11.5.1.16 – Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called "Burst Terminate"] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, the following functionality is required:

1. BST applies to all burst lengths, including the optional full page burst length when included.

2. BST is not a valid command during read or write with autoprecharge

3. When terminating a burst read command, the BST command must be issued n clock cycles before the clock edge at which the last desired data word is valid, where n equals the $\overline{\text{CAS}}$ latency for read operations minus 1. This is shown in Figure 3-1 with examples for $\overline{\text{CAS}}$ latency 1, 2 and 3 (higher $\overline{\text{CAS}}$ latencies follow the same pattern).

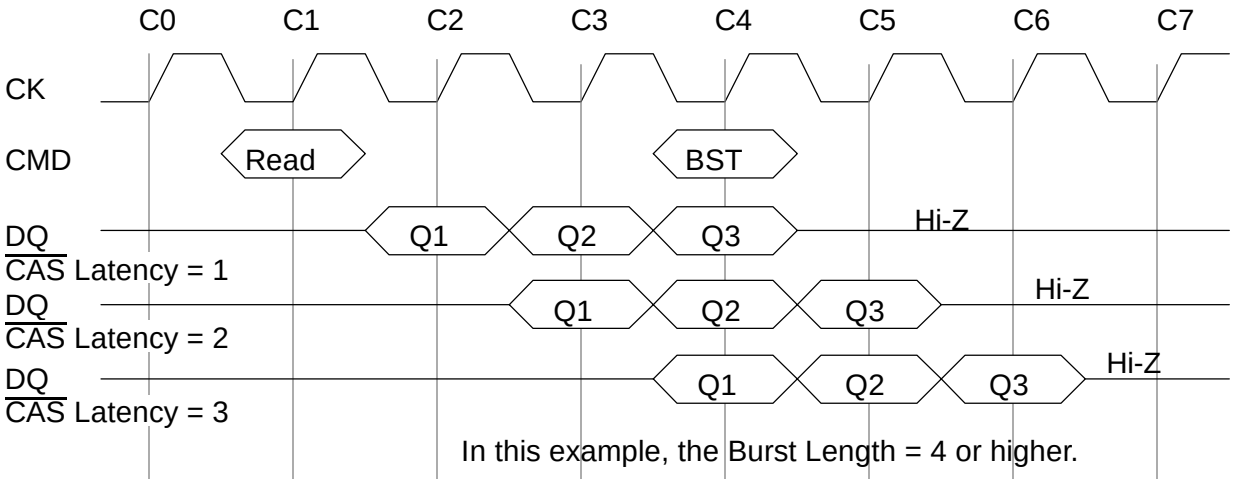


Figure -1: Terminating a Burst Read Command with BST

4. When terminating a burst write command, the BST command must be issued one clock after the clock edge which samples the last word of data that is required to be written into the memory. The DQM input(s) must be high for the clock edge that is coincident with the BST command. Input data on the DQ pins for the clock edge that is coincident with the BST command is ignored. Input data on the DQ pins for the clock edges after the BST command is also ignored unless a new write command is issued. This is shown in Figure 4-1.

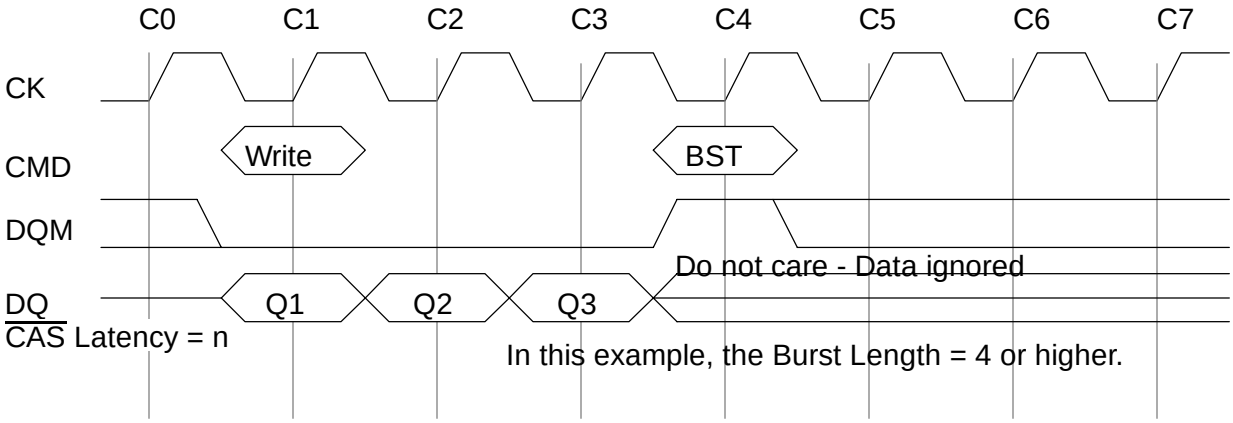


Figure –2: Terminating a Burst Write Command with BST

Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.1.17 – Full Page Burst Mode for SDRAM/SGRAM

Full page burst mode is an optional feature for SDRAM/SGRAM. If full page burst mode is included in an SDRAM or SGRAM, the following functionality is required:

1. Full page burst operations (read or write) do not self terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 or 8, full page burst mode continues until it is terminated using another command. During full page burst mode, once the highest order column address is accessed, the count "wraps around" to column address 0 and continues.

2. A full page burst sequence can be terminated by a BST (burst stop command which is also an optional feature), a PRE (Precharge Command), a PREALL (Precharge all banks command) or another full page burst read or write command.

- BST is an optional feature on SDRAMs/SGRAMs. BST will terminate the burst sequence, but will not cause the device to precharge the accessed bank (i.e., the bank remains active). Additional read or write commands can be executed while the bank is active. A subsequent PRE command is used to return the selected bank to the idle state (row precharge time must be satisfied). A subsequent PREALL command is used to return all banks to the idle state (row precharge time must be satisfied).
- PRE will terminate the burst sequence and will initiate a precharge operation which returns the selected bank to the idle state (row precharge time must be satisfied).
- PREALL will terminate the burst sequence and will initiate a precharge operation which returns all banks to the idle state (row precharge time must be satisfied)
- Read/write interrupt of the full page burst will cause the present burst sequence to terminate and initiates a new read/write full page burst sequence with a new starting address.

3. Full page burst mode with autoprecharge, AP, is not a legal command. The AP bit must be zero for full page burst read or write commands

3.11.5.1.18 – Deep Power Down Mode

Deep Power Down Mode is an operating mode that is used to achieve maximum power reduction by cutting the power of the whole memory array of the devices. Data will not be retained once the device has entered into Deep Power Down Mode. Full initialization is required when the device exits from Deep Power Down Mode.

Truth Table

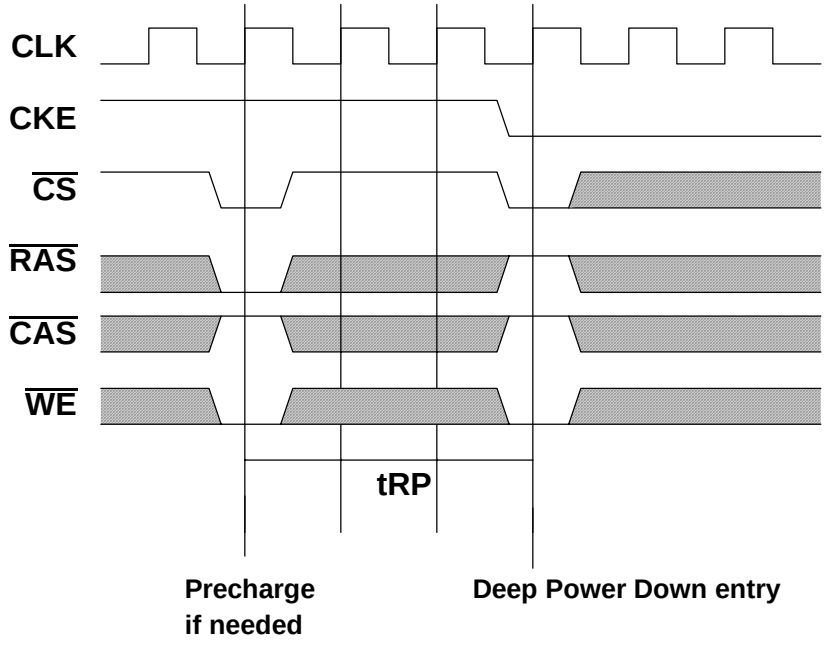
Current State	Command	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Idle	Deep Power Down Entry	H	L	L	H	H	L
Deep Power Down	Deep Power Down Exit	L	H	x	x	x	x

x: don't care

The deep power down mode is continued while CKE is kept low.

Deep Power Down Mode Entry

The deep power down mode is entered by having $\overline{CS}$ and $\overline{WE}$ held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock, while CKE is low. The following timing diagram illustrates deep power down mode entry.



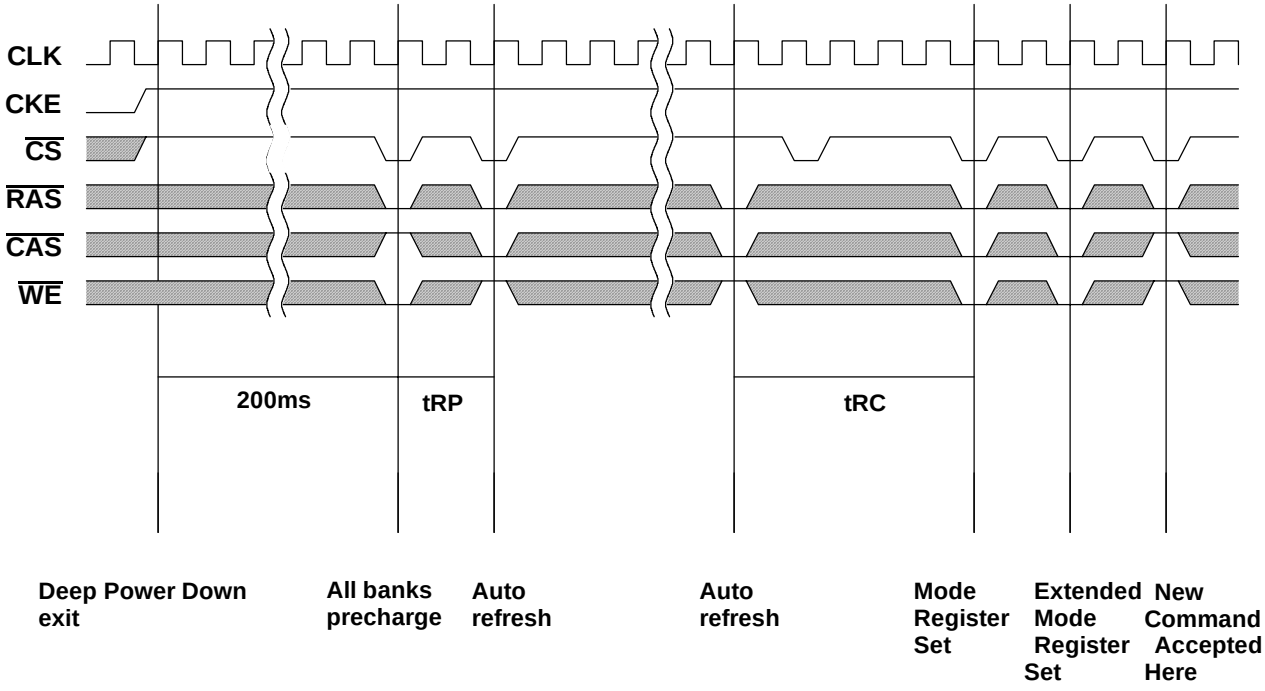
Deep Power Down Mode Exit Sequence

The deep power down mode is exited by asserting CKE high.

After the exit, the following sequence is needed to enter a new command.

1. Maintain NOP input conditions for a minimum of 200μsec.
2. Issue precharge commands for all banks of the device.
3. Issue 8 or more autorefresh commands.
4. Issue a mode register set command to initialize the mode register.
5. Issue an extended mode register set command to initialize the extended mode register.

The following timing diagram illustrates the deep power down mode exit sequence.



3.11.5.2 - DDR Specific SDRAM Functions

The Standards in this section are special functions that are applicable to DDR SDRAM except where that function specifically defines another class of device for which it is applicable.

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

To enable Doubled Data Rate and the control of that data in DDR SDRAMs, a signal to be identified by the label DQS will be added to the existing definition of the SDRAM. This section defines the timing relationships of the DQS signal.

3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

A pin will be added to the definition of DDR SDRAM devices whose polarity will be inverted to that of CK and labeled CK\ or $\overline{CK}$. That pin along with CK must be used to supply a differential clock to the DDR SDRAM devices.

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Read command may interrupt a Write burst and which input data is not written into the memory.

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Write command may interrupt a Read burst.

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

When a burst Read command is issued to a DDR SDRAM/SGRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

Precharge timing for Write operations in DRAMs requires enough time to allow “write recovery” which is the time required by a DRAM core to properly store a full “0” or “1” level before a Precharge operation. For DDR SDRAM/SGRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

3.11.5.2.7 - Burst Stop Command for DDR SDRAMs/SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is a mandatory feature for DDR SDRAMs/SGRAMs. This section describs the required functionality.

3.11.5.2.8 - DDR SDRAM/SGRAM Full Sequential Burst Ordering

This section gives, for DDR SDRAM & SGRAM, Y address ordering that is supported for sequential burst lengths (BL) of 2, 4, and 8:

3.11.5.2.9 - DDR SDRAM DQS Coincident with Data

The timing of the signal DQS relative toRead Data from the DDR SDRAM device is giving.

3.11.5.2.10 - Extended Mode Register Set for DDR SDRAM / SGRAM.

Extended mode register address space is provided by defining non-zero Bank address(s) for accesses that otherwise conform to the Mode Register Set (MRS) cycle. These Extended Mode Register Set cycles (EMRS) can be implemented as needed for function extensions to the standard.

3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS

This section defines the DLL disable/enable bit in the Extended Mode Register.

3.11.5.2.12 - Refresh Requirements

This section provides the precise definition of the refresh requirements.

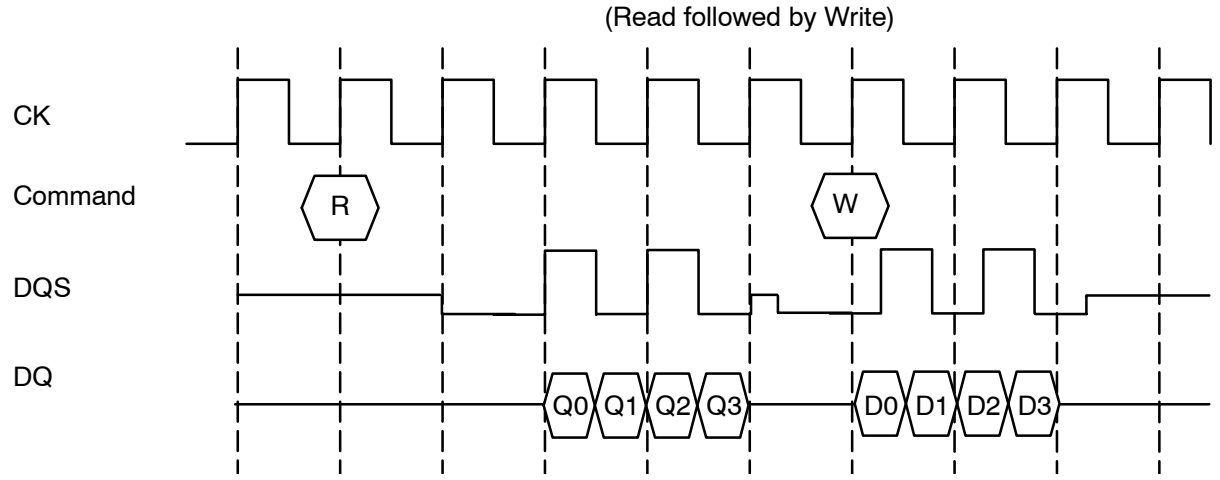
3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM

This section provides the Mode Register Set and Extemded Mode Register Set definition for Low Power DDR SDRAM.

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

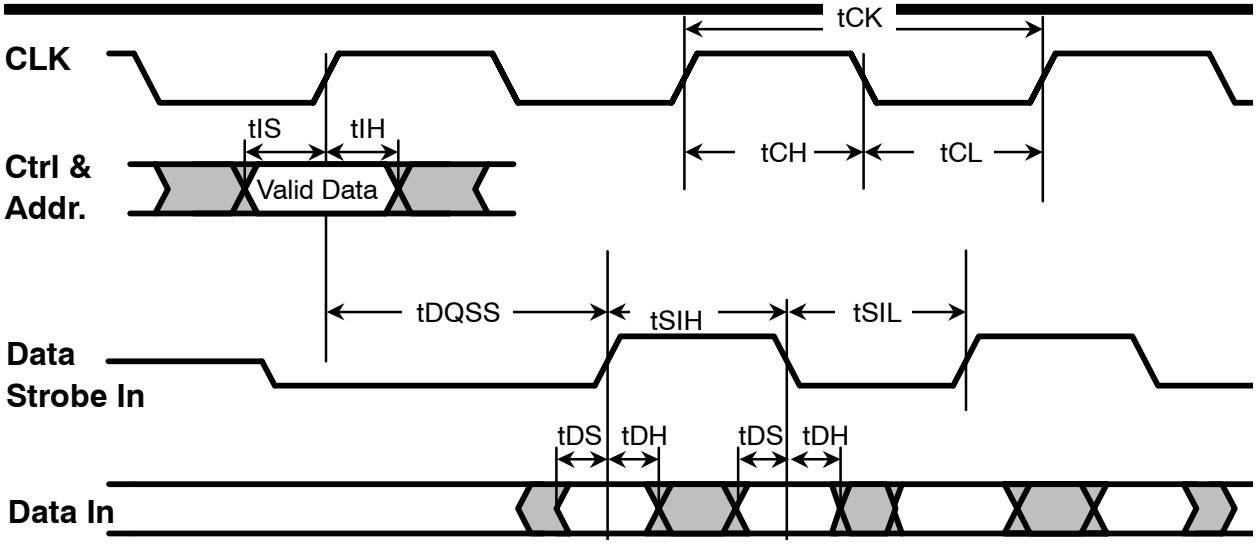
To enable Doubled Data Rate and the control of that data in DDR SDRAMs, a signal to be identified by the label DQS will be added to the existing definition of the SDRAM.

Driven by the DDR SDRAM during output of Read data, and Driven by the Memory Controller during input of Write data, the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM.



Bi-directional Data Strobe (DQS)

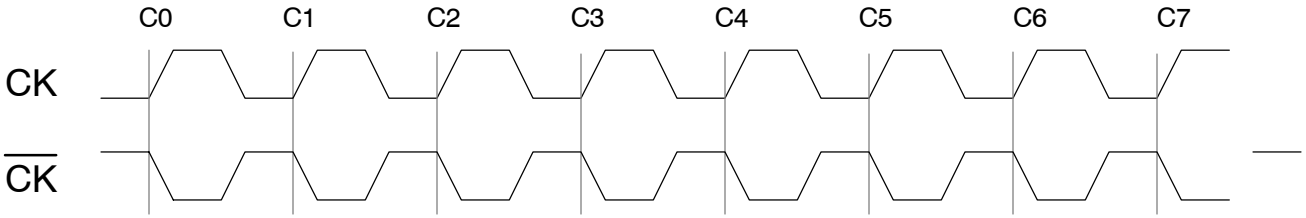
Example of BASIC WRITE TIMING (@DQS)



Bi-Directional Data Strobe (DQS)

3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

A pin will be added to the definition of DDR SDRAM devices whose polarity will be inverted to that of CK and labeled CK\ or $\overline{CK}$. That pin along with CK must be used to supply a differential clock to the DDR SDRAM devices. The slew rates, and recommended terminations will be defined in subsequent standards. The voltage levels are defined in Section 3.11.6 for which standards have been published.



Differential Clock timing relationship (for reference only)

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs & SGRAMs

The following functionality establishes how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle (refer to Figure 1) is disallowed.
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation as shown in Figures 2 and 3.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the SDRAM/SGRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the SDRAM/SGRAM.
5. It is illegal for a Read command to interrupt a Write with autoprecharge command.

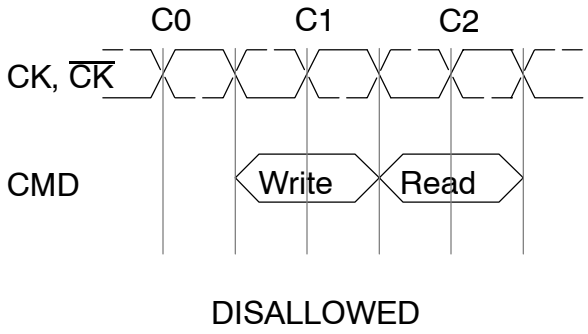
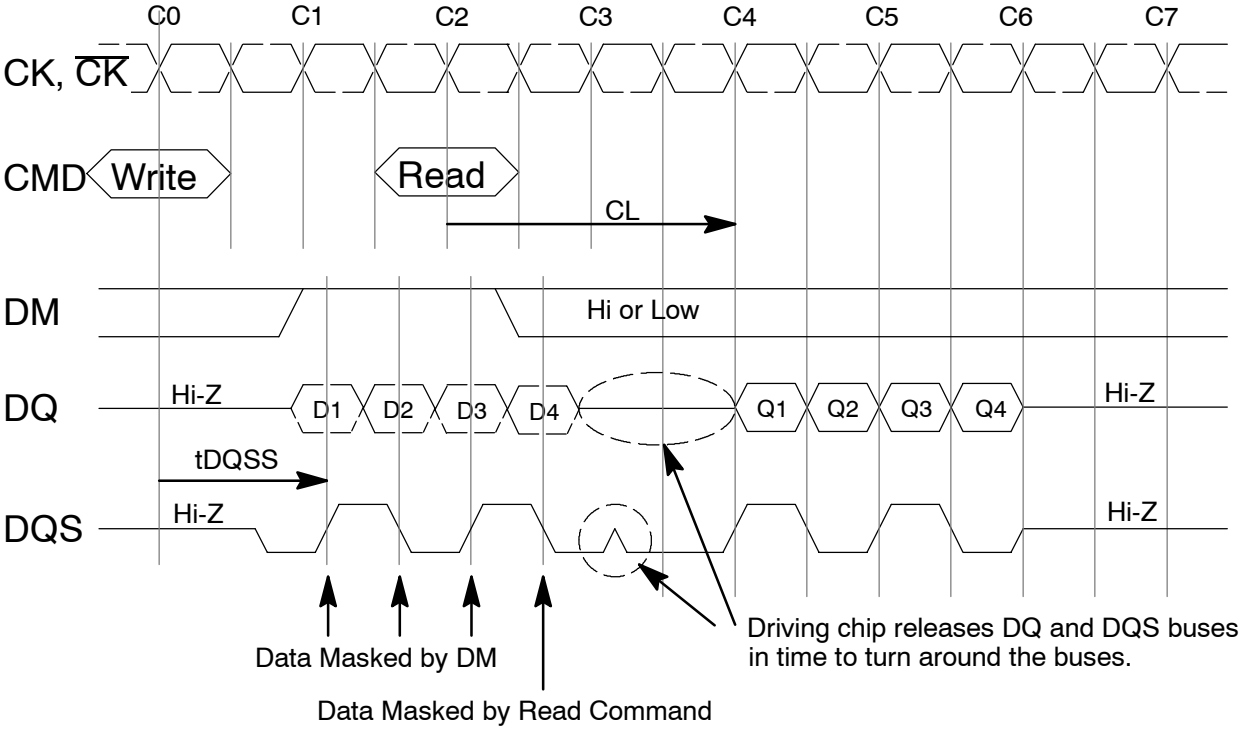


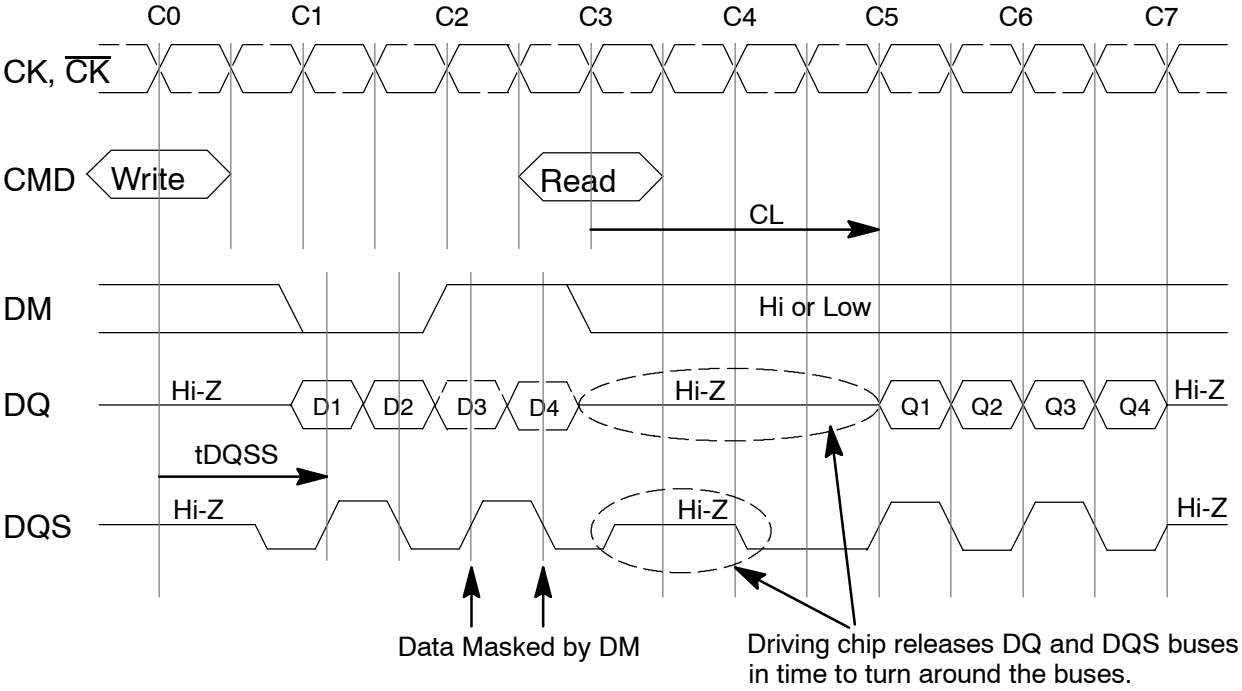
Figure 1: Read Interrupting a Write - Write to Read Delay = 1 Clock Cycle

3.11.5.2.3 (Cont) - Read Interrupting a Write Operation for DDR SDRAMs & SGRAMs



In this example, the Burst Length = 4 and the operations are not necessarily to the same bank.

Figure 2: Read Interrupting a Write - Write to Read Delay = 2 Clock Cycles



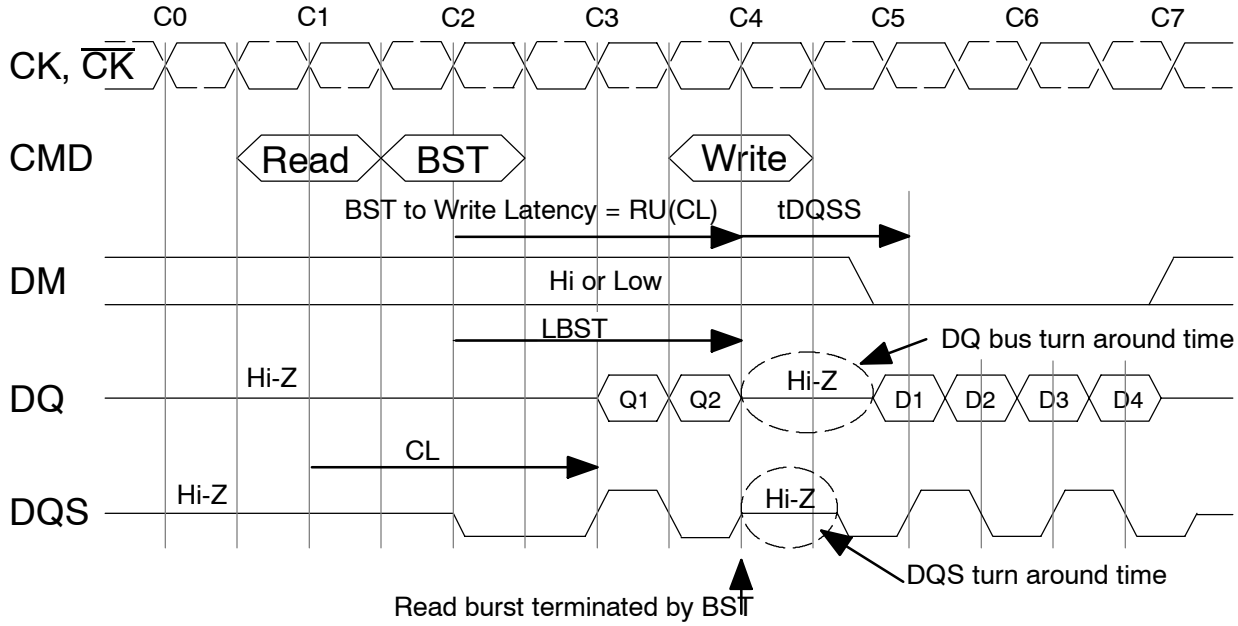
In this example, the Burst Length = 4 and the operations are not necessarily to the same bank.

Figure 3: Read Interrupting a Write - Write to Read Delay = 3 Clock Cycles

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

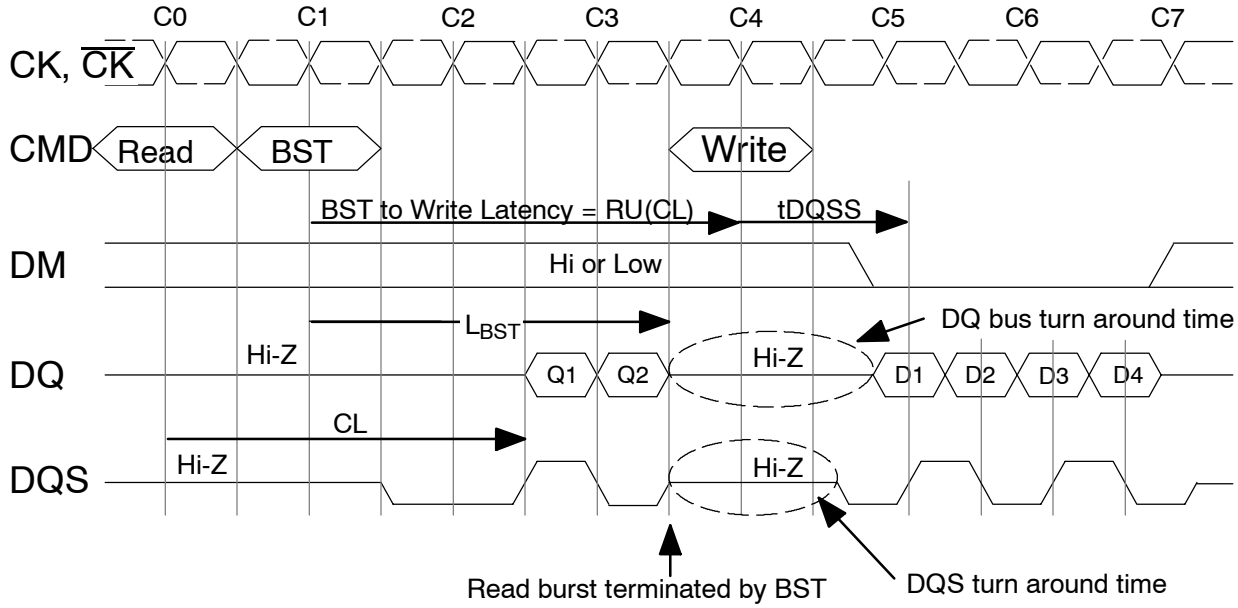
The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU(CL) [CL is the $\overline{CAS}$ Latency and RU means round up to the nearest integer]. Refer to Figures 1 and 2.
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.



In this example, the Burst Length = 4, CL=2, RU(CL) = 2 and the Read & Write operations are not necessarily to the same bank.

Figure 1: Write Interrupting a Read Burst ($\overline{CAS}$ Latency, CL, = X.0)



In this example, the Burst Length = 4, CL=2.5, RU(CL) = 3 and the Read & Write operations are not necessarily to the same bank.

Figure 2: Write Interrupting a Read Burst ($\overline{CAS}$ Latency, CL, = X.5)

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

When a burst Read command is issued to a DDR SDRAM/SGRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time). Refer to Figure 1.

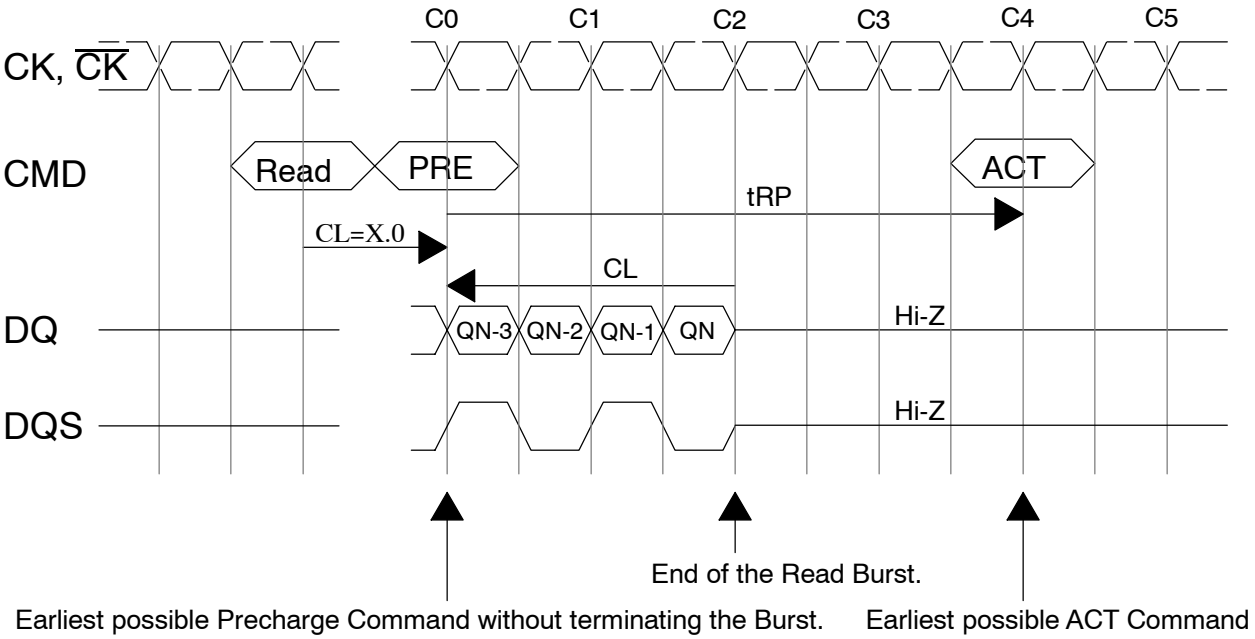
3. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{CAS}$ Latency. Once the last data word has been output, the output buffers are set to the Hi-Z state. A new Bank Activate command may be issued to the same bank after tRP. Refer to Figure 2.

4. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP where tRP begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above. Refer to Figure 3.

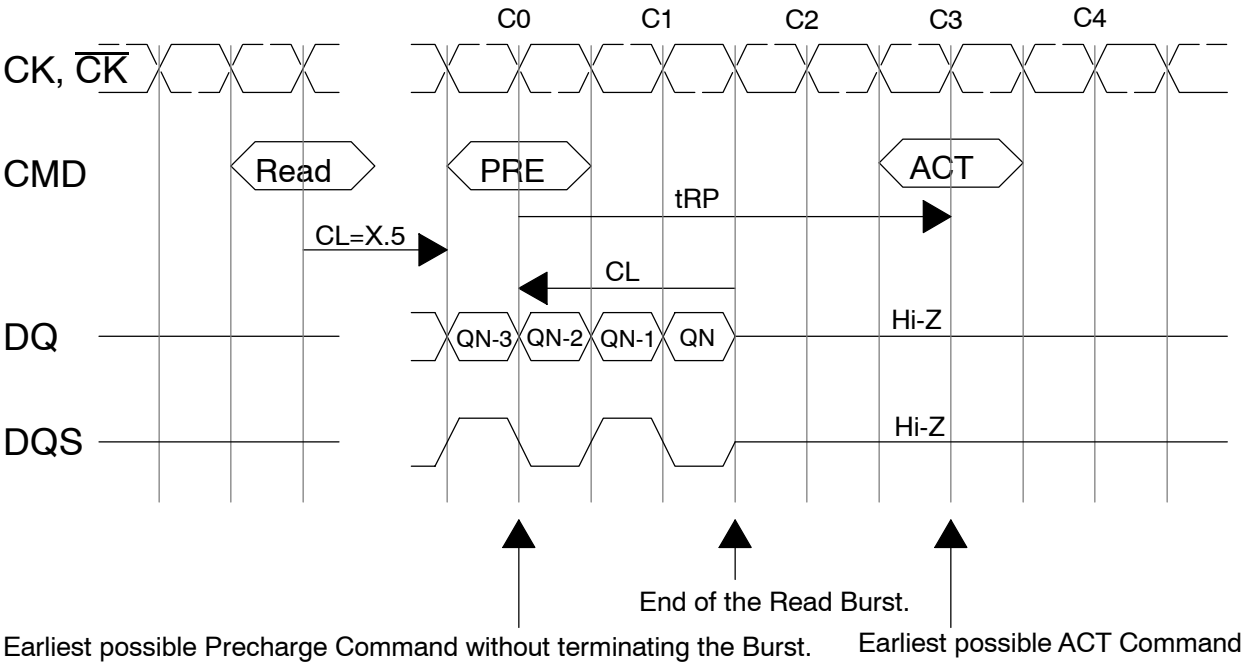
5. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a *rising* clock edge).

5. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

3.11.5.2.5 (cont) - Precharge Timing for Reads for DDR SDRAMs/SGRAMs



(A) Precharge Timing for Reads - Burst Not Interrupted - CL=X.0



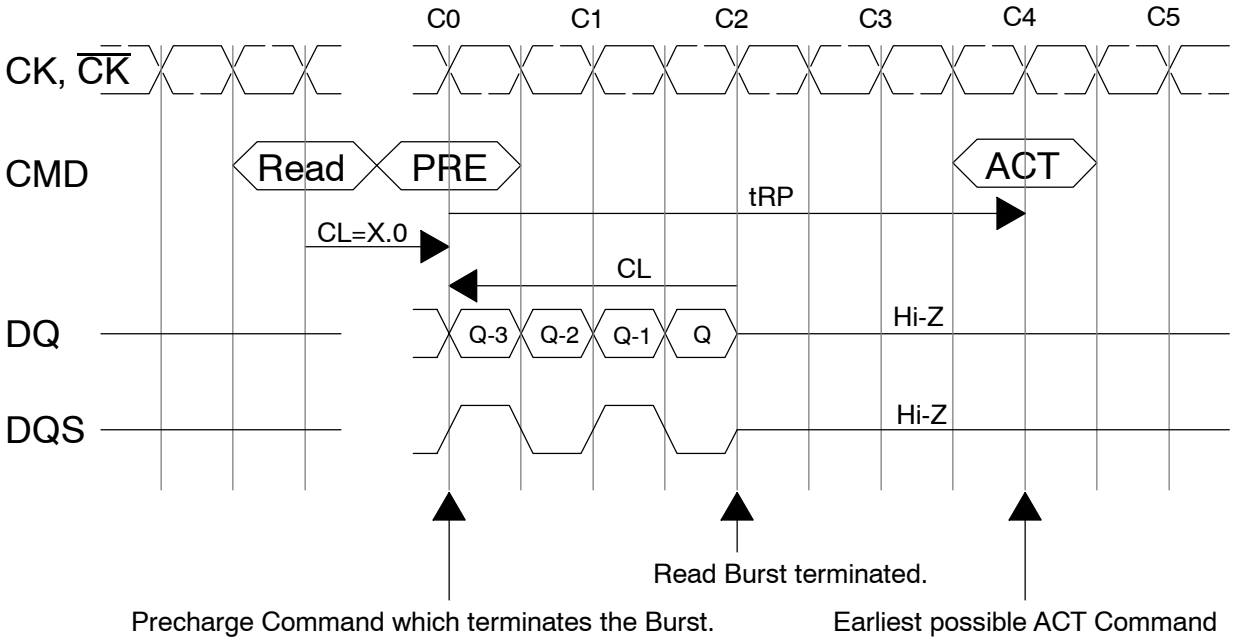
(B) Precharge Timing for Reads - Burst Not Interrupted - CL=X.5

In these examples, all operations are to the same bank.
In these examples, the Burst Length=N (N=4 or 8, if N=2, only the last 2 data words shown are output).

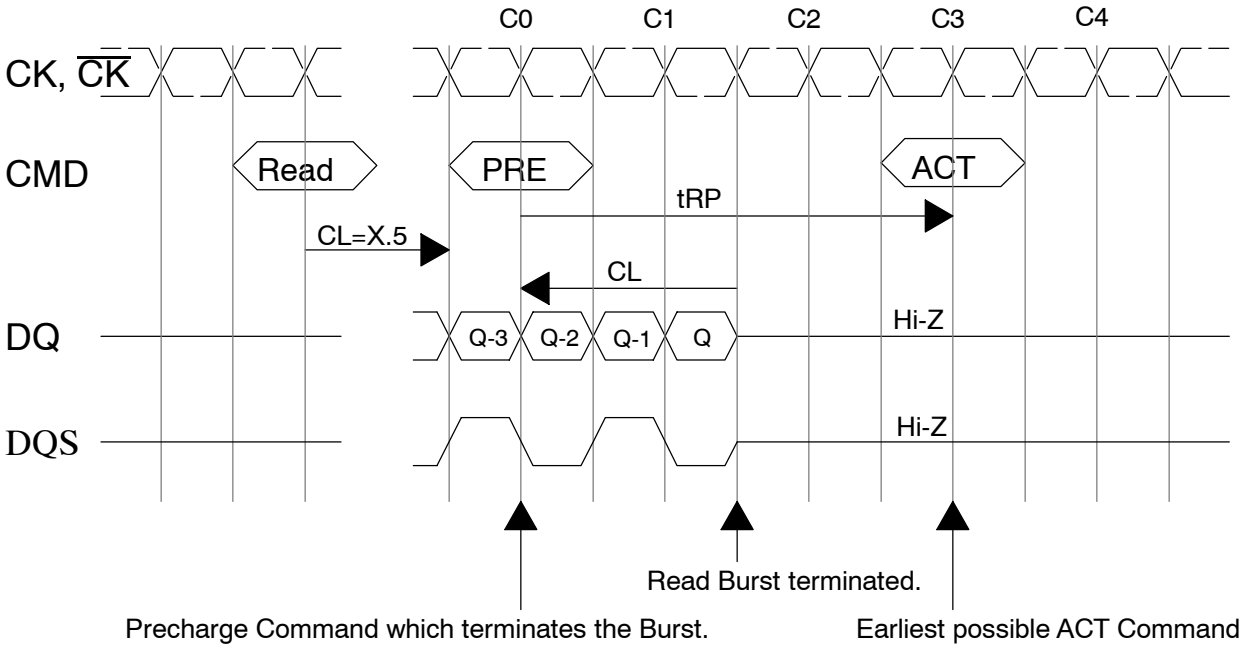
Figure 1: Precharge Timing for Reads - Burst Not Interrupted

Release 9

3.11.5.2.5 (cont) - Precharge Timing for Reads for DDR SDRAMs/SGRAMs



(A) Precharge Timing for Reads - Burst Interrupted - CL=X.0

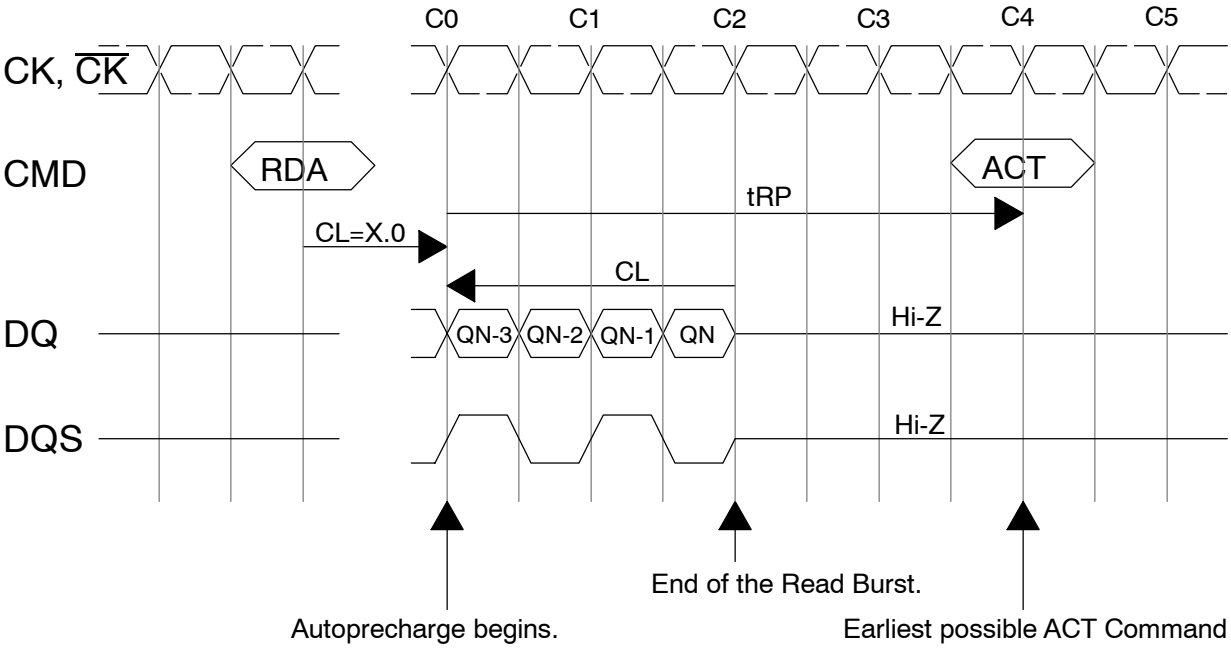


(B) Precharge Timing for Reads - Burst Interrupted - CL=X.5

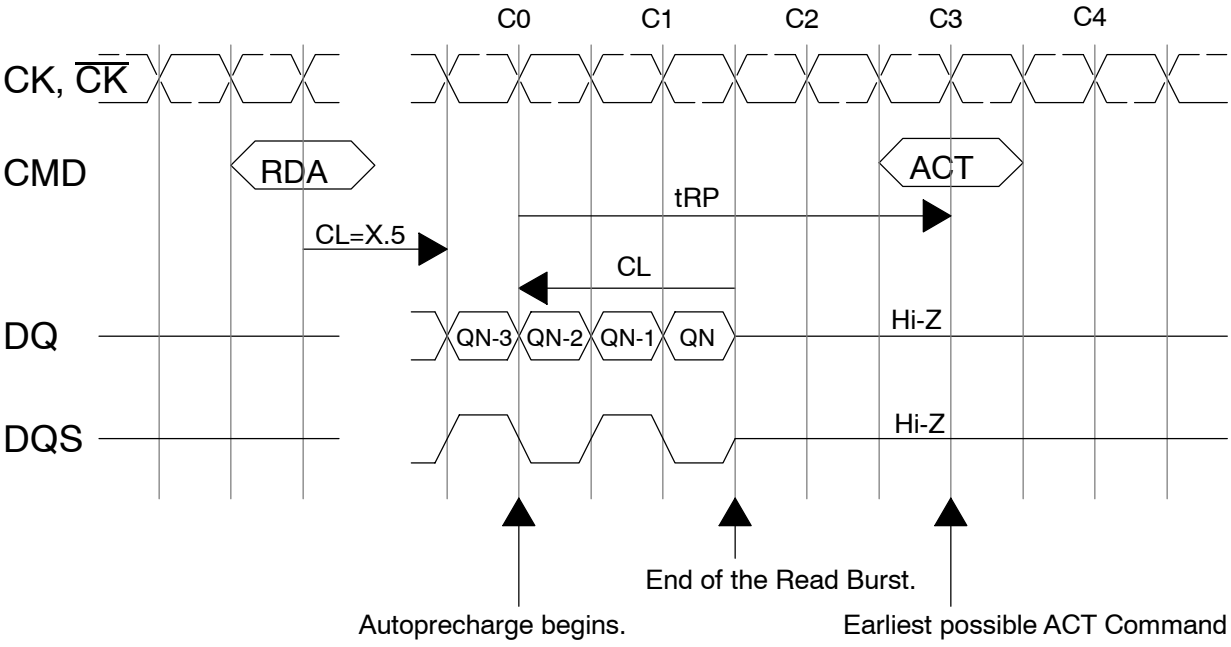
In these examples, all operations are to the same bank.
In these examples, the Burst Length=N (N=4 or 8).

Figure 2: Precharge Timing for Reads - Burst Interrupted

3.11.5.2.5 (cont) - Precharge Timing for Reads for DDR SDRAMs/SGRAMs



(A) Precharge Timing for Reads - Read with Autoprecharge - CL=X.0



(B) Precharge Timing for Reads - Read with Autoprecharge - CL=X.5

In these examples, all operations are to the same bank.

In these examples, the Burst Length=N (N=4 or 8, if N=2, only the last 2 data words shown are output).

Figure 3: Precharge Timing for Reads - Read with Autoprecharge

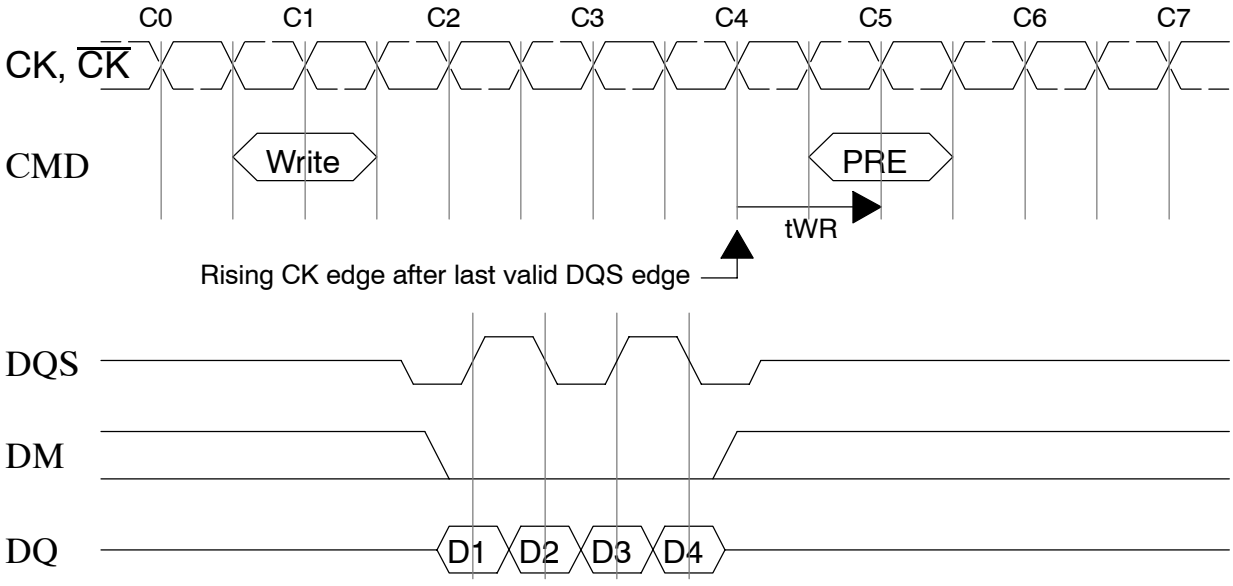
3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

Precharge timing for Write operations in DRAMs requires enough time to allow “write recovery” which is the time required by a DRAM core to properly store a full “0” or “1” level before a Precharge operation. For DDR SDRAM/SGRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the SDRAM/SGRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation, i.e., the input clock domain.

tWR starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by tWR. Refer to Figure 1.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by tWR. Refer to Figure 2.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after tWR+tRP where tWR+tRP starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above. Refer to Figure 3.
4. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where tRAS(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.



In this example, all operations are to the same bank.
In this example, the Burst Length = 4.

Figure 1: Precharge Timing for Writes - Burst Not Interrupted

3.11.5.2.6 (cont.) - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

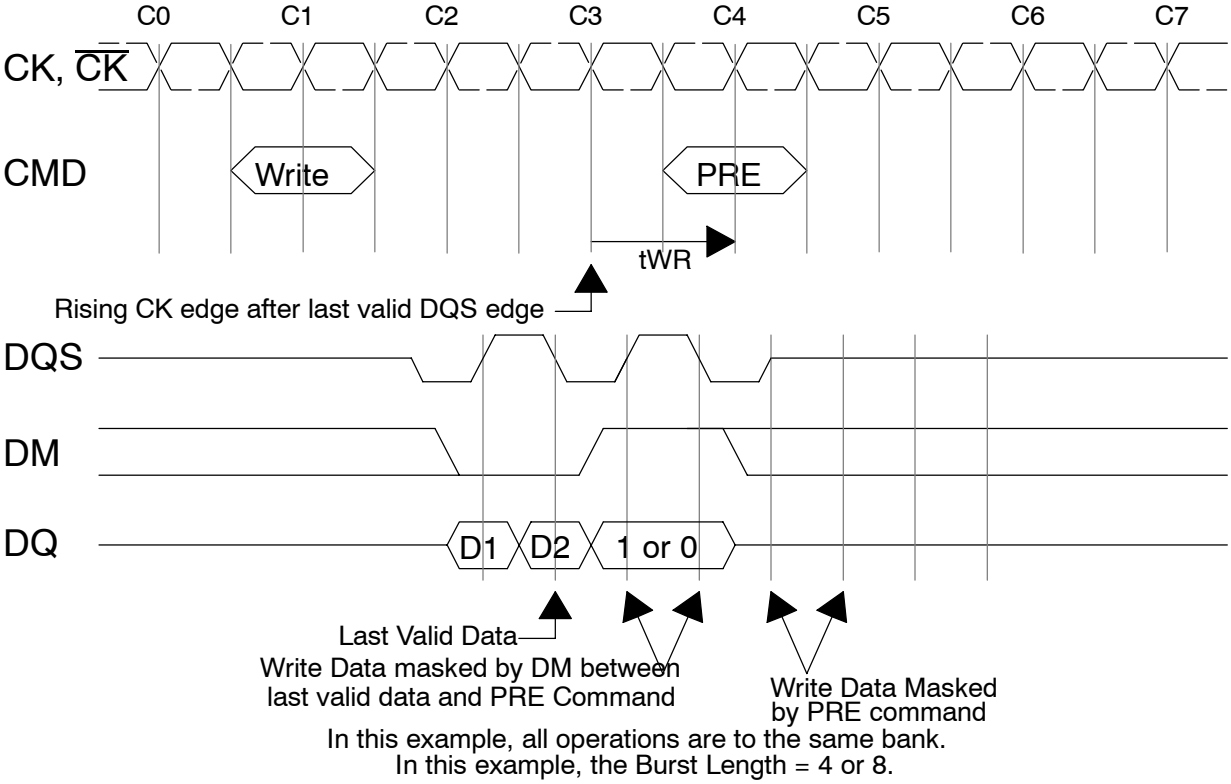


Figure 2: Precharge Timing for Writes - Burst Interrupted

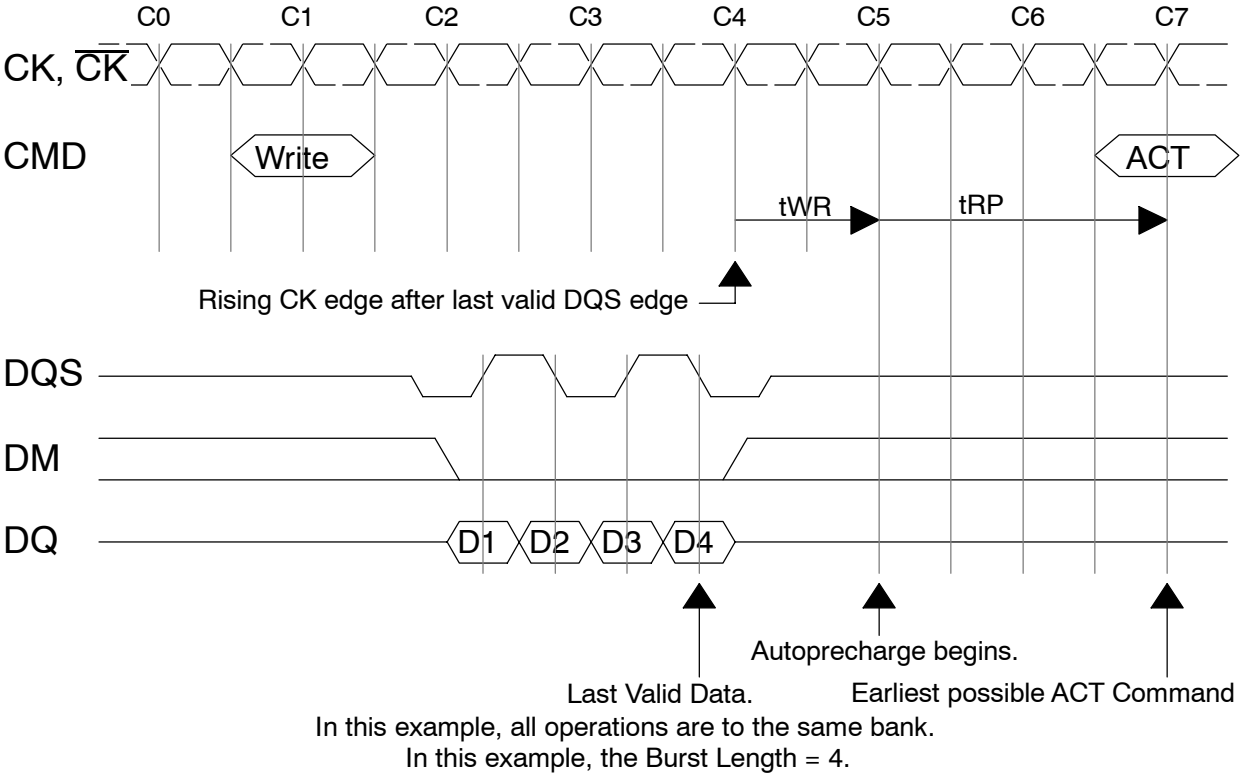
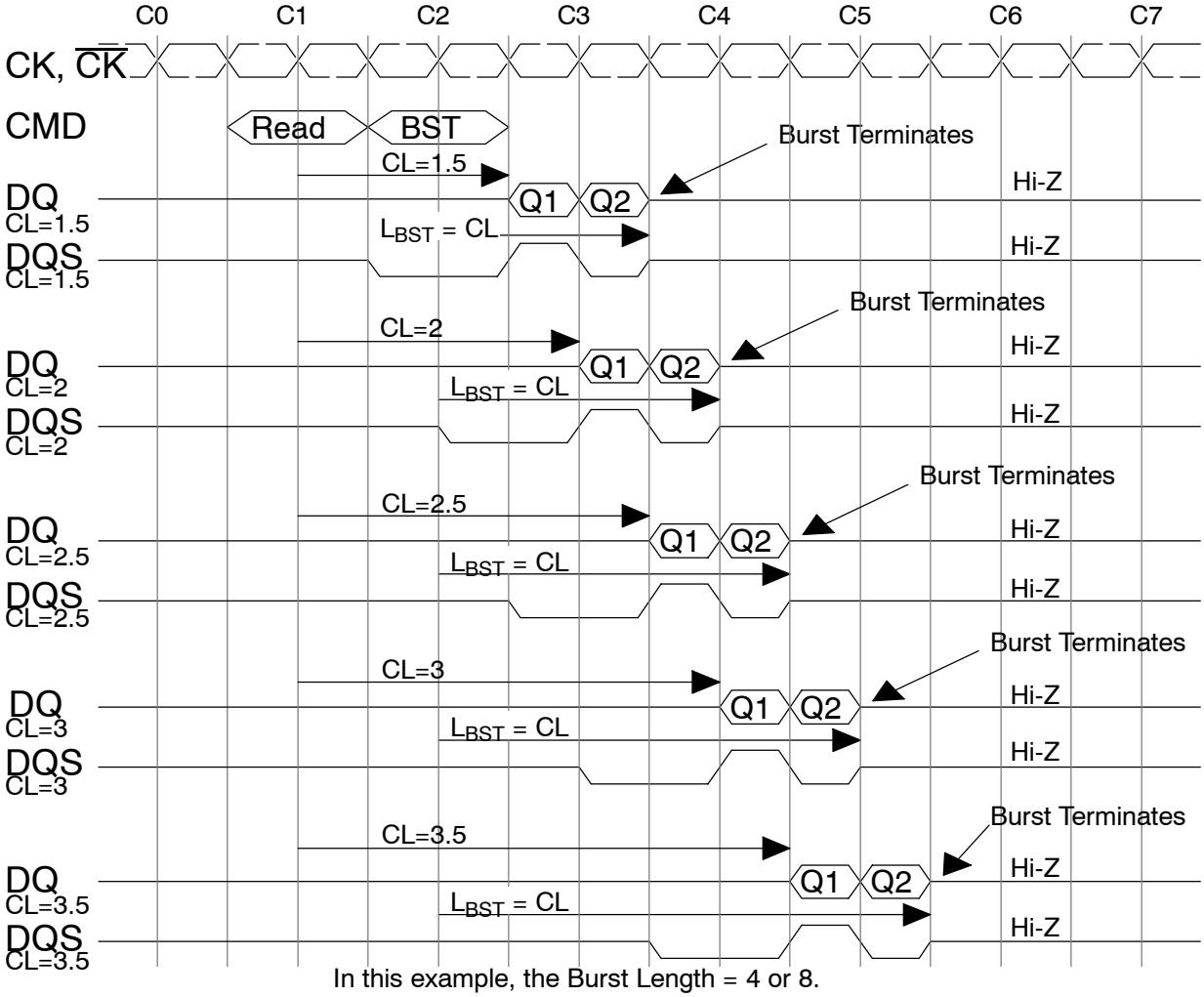


Figure 3: Precharge Timing for Writes - Write With Autoprecharge

3.11.5.2.7 - Burst Stop Command for DDR SDRAMs & SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is a mandatory feature for DDR SDRAMs/SGRAMs. The following functionality is required:

1. The BST command may only be issued on the rising edge of the input clock, CK.
2. BST is only a valid command during Read bursts.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} (“BST Latency”) clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations. This is shown in Figure 1 with examples for $\overline{CAS}$ latency (CL) of 1.5, 2, 2.5, 3 and 3.5 (only selected $\overline{CAS}$ latencies are required by the DDR SDRAM/SGRAM standards, the others are optional).
7. When the burst terminates, the DQ and DQS pins are set to a Hi-Z state.
8. The BST command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).
9. The Bank Addresses are don’t care (i.e., high or low) on the clock edge that samples a Burst Stop Command



In this example, the Burst Length = 4 or 8.

Figure 1: Terminating a DDR SDRAM/SGRAM Read Burst with BST

3.11.5.2.8 - DDR SDRAM & SGRAM Full Sequential Burst Ordering

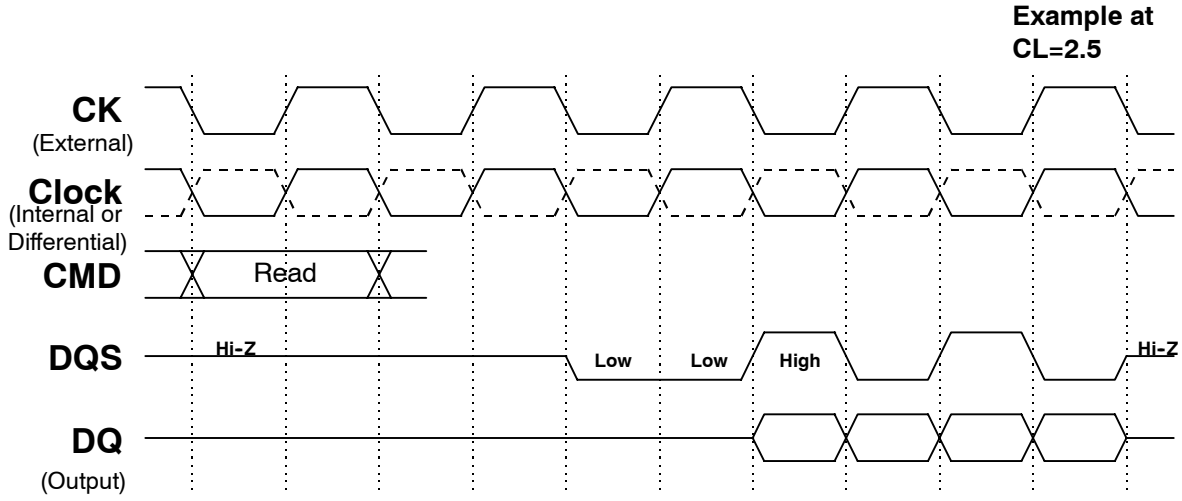
For DDR SDRAM & SGRAM, the following ordering is supported for sequential burst lengths (BL) of 2, 4, and 8:

BL = 2	BL = 4	BL = 8
0, 1	0, 1, 2, 3	0, 1, 2, 3, 4, 5, 6, 7
1, 0	1, 2, 3, 0	1, 2, 3, 4, 5, 6, 7, 0
	2, 3, 0, 1	2, 3, 4, 5, 6, 7, 0, 1
	3, 0, 1, 2	3, 4, 5, 6, 7, 0, 1, 2
		4, 5, 6, 7, 0, 1, 2, 3
		5, 6, 7, 0, 1, 2, 3, 4
		6, 7, 0, 1, 2, 3, 4, 5
		7, 0, 1, 2, 3, 4, 5, 6

The numbers in the tables are the decimal equivalents of the LSBs (1 bit for BL=2, 2 bits for BL=4, & 3 bits for BL=8) of the Y - address.

3.11.5.2.9 - DDR DQS Coincident with Data

The signal DQS shall be coincident with Read Data from the DDR SDRAM device. The timing diagram below shows the nominal relationship between data and DQS for read data at the output of the DDR SDRAM devices.



3.11.5.2.10 - Extended Mode Register Set (EMRS) for DDR SDRAM/SGRAM

- Extended mode register address space is provided by defining non-zero Bank address(s) for accesses that otherwise conform to the Mode Register Set (MRS) cycle. These Extended Mode Register Set cycles (EMRS) can be implemented as needed for function extensions to the standard.
- The EMRS is required for DDR SDRAM.
- All address bits are reserved at zero until defined and used for extended functions.
- The Extended Mode Register is independent of any MRS cycle.
- BA2 and BA1 may not be implemented on all designs. If these two Bank Address bits are not available, then there is no additional expansion beyond EMRS possible for those devices.

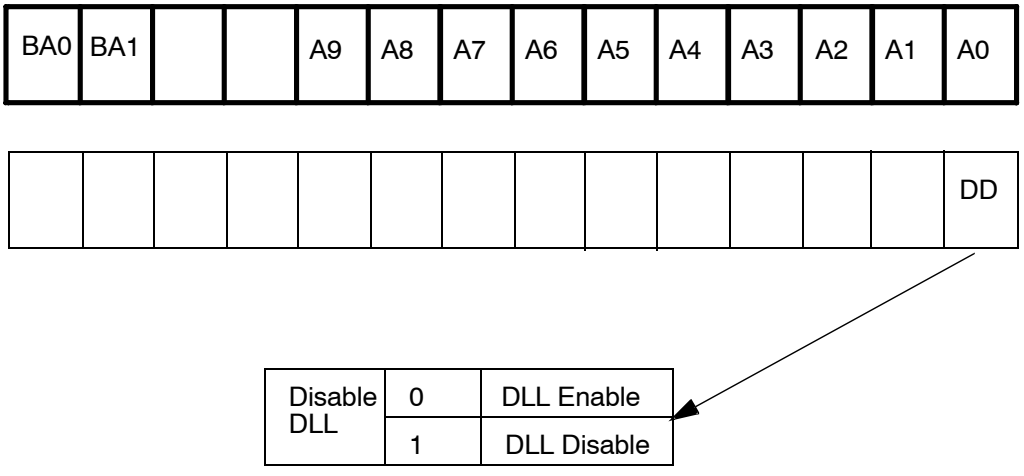
Extended Mode Register Address Space			
BA0	BA1	BA2	An - A0
0	0	0	(Existing) MRS Cycle
1	0	0	Extended Functions (EMRS)
X	1	0	Reserved For Future (EMRSn)
X	X	1	Reserved For Future

NOTE: The uses and functions defined by the address bits are or will be covered in separate Standards

3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS

The following defines the DLL disable/enable bit in the Extended Mode Register:

Extended Mode Register Definition



3.11.5.2.12 - REFRESH REQUIREMENTS

DDR SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 256 Mb DDR SDRAM has 8192 rows resulting in a tREFI of 7.8 ms.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS–BEFORE–RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of tREFI (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 * tREFI.

SELF REFRESH

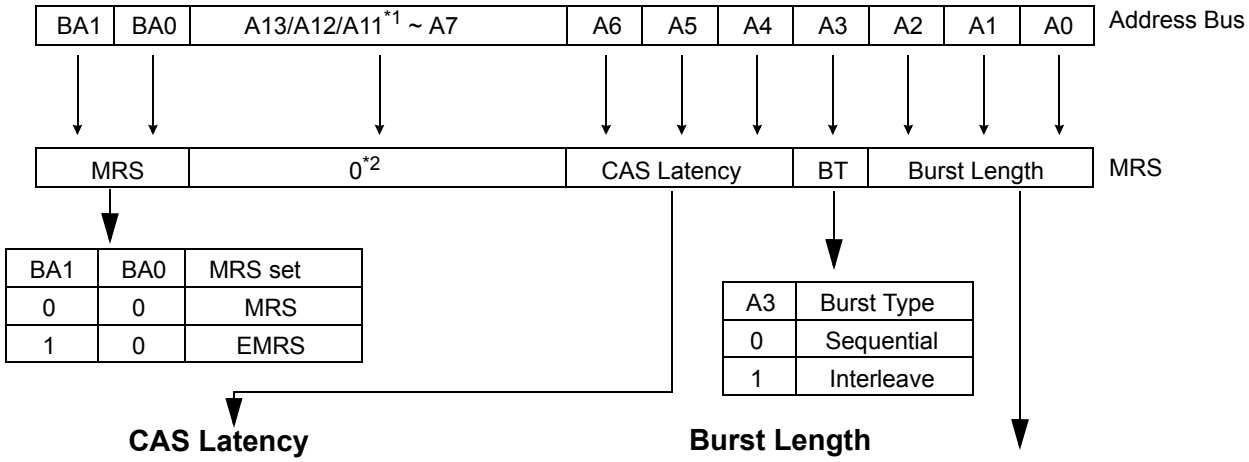
The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are ”Don’t Care” during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSC because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is not required.

3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM

Mode Register Set(MRS) for Low Power DDR SDRAM



BA1	BA0	MRS set
0	0	MRS
1	0	EMRS

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 (Optional)
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

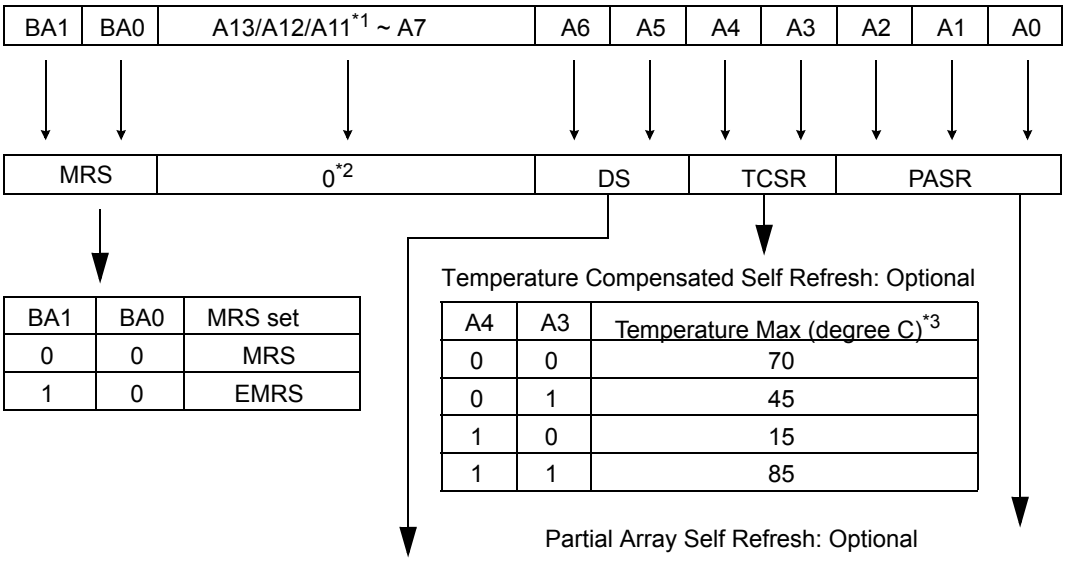
Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16 (Optional)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

* 1 : MSB depends on Low Power SDRAM density
* 2 : A logic 0 should be programmed to all unused / undefined address and bank address bits to ensure future compatibility

3.11.5.2.13 (Cont) - MRS/EMRS for Low Power DDR SDRAM

Extended Mode Register Set(EMRS) for Low Power DDR SDRAM



BA1	BA0	MRS set
0	0	MRS
1	0	EMRS

Temperature Compensated Self Refresh: Optional

A4	A3	Temperature Max (degree C)*3
0	0	70
0	1	45
1	0	15
1	1	85

Driver Strength

A6	A5	Driver Strength
0	0	Full strength driver
0	1	Weak strength driver
1	0	Reserved
1	1	Reserved

Partial Array Self Refresh: Optional

A2	A1	A0	Self Refresh Coverage
0	0	0	4 Banks (All Banks)
0	0	1	Half array (BA1 = 0)
0	1	0	Quarter array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array : Optional (BA1 = BA0 = Row Address MSB = 0)
1	1	0	1/16 array: Optional (BA1 = BA0 = Row Address 2 MSBs = 0)
1	1	1	Reserved

* 1 : MSB depends on Low Power SDRAM density
* 2 : A logic 0 should be programmed to all unused / undefined address and bank address bits to ensure future compatibility
* 3 : Temperatures specified for the TCSR feature are Case temperatures

Definitions:

Temperature Compensated Self Refresh (TCSR)
Programmable refresh rate for self refresh mode to allow the system to control power as a function of temperature

Partial Array Self Refresh (PASR)
Programmable memory array size to be refreshed during self refresh operation to reduce power. Data outside the defined area will not be retained during self refresh

3.11.5.3 – Enhanced SDRAM (ESDRAM) Specific SDRAM Functions

The Standards in this section are special functions that are applicable to Enhanced SDRAM (ESDRAM). The standards cover both SDR and DDR devices as stated on the individual Standards.

3.11.5.3.1 – Read-AutoPrecharge Operation for SDR ESDRAM

In the Enhanced SDRAM (ESDRAM), a Read-Autoprecharge command will initiate multiple functions. This standard defines those functions.

3.11.5.3.2 – Read-AutoPrecharge Operation for DDR ESDRAM

In the DDR Enhanced SDRAM (DDR ESDRAM), a Read-Autoprecharge command will initiate multiple functions. This standard defines those functions.

3.11.5.3.3 – Cache Load Operation for SDR ESDRAM

In the Enhanced SDRAM (ESDRAM), a Cache Load command will initiate multiple functions. This standard defines those functions.

3.11.5.3.4 – Cache Load Operation for DDR ESDRAM

In the DDR Enhanced SDRAM (DDR ESDRAM), a Cache Load command will initiate multiple functions. This standard defines those functions.

3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM

“No Write Transfer” mode is an optional mode of operation that allows an Enhanced SDRAM (ESDRAM) to concurrently keep a read page and a write page open per bank. This Standard defines the details of this operational mode.

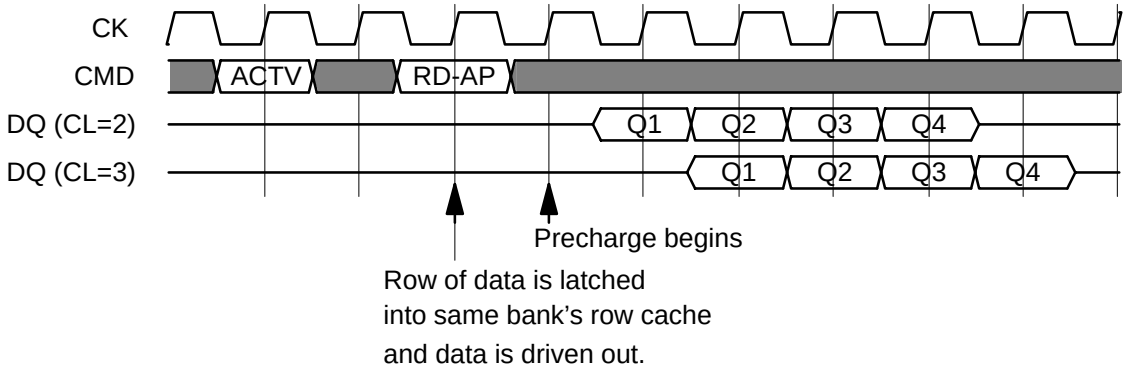
3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM

“No Write Transfer” mode is an optional mode of operation that allows a DDR Enhanced SDRAM (DDR ESDRAM) to concurrently keep a read page and a write page open per bank. This Standard defines the details of this operational mode.

XILINX EXHIBIT 1010
Page 759

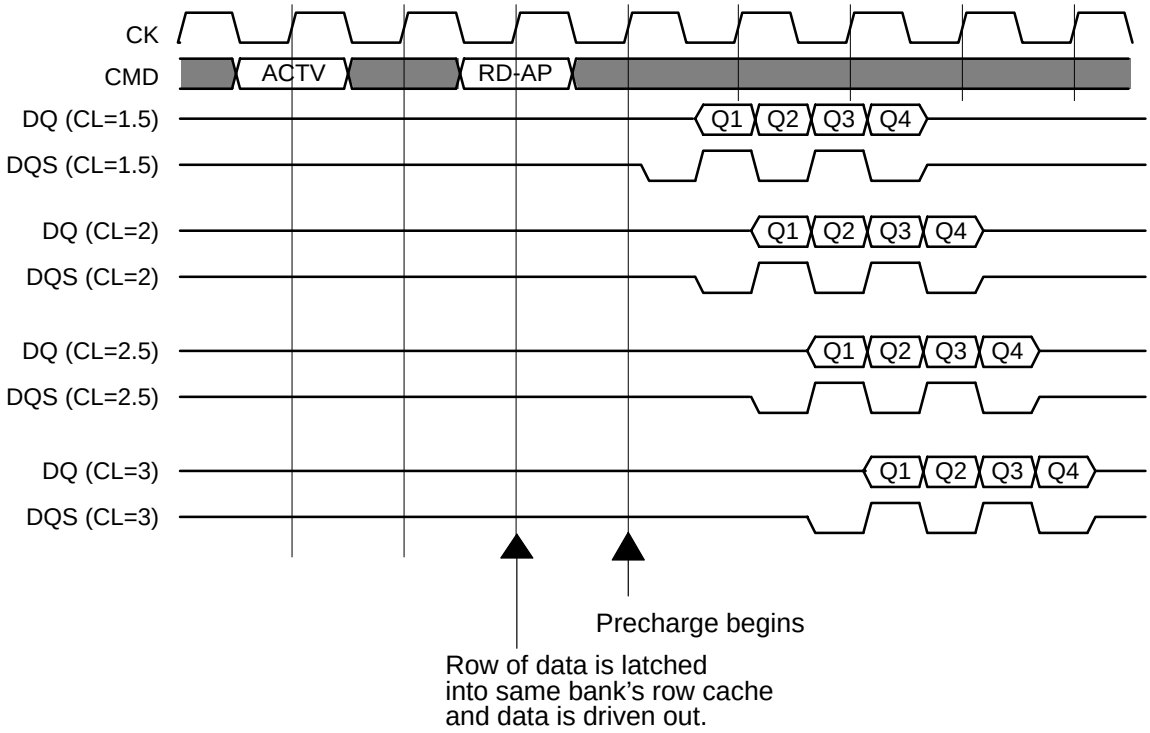
3.11.5.3.1 – Read-Auto Precharge Operation for SDR ESDRAM

The Enhanced SDRAM (ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read-Autoprecharge command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank, and begin the precharge one clock cycle following the Read Autoprecharge command independent of the burst length. In the diagram below, a 4-word burst is shown.



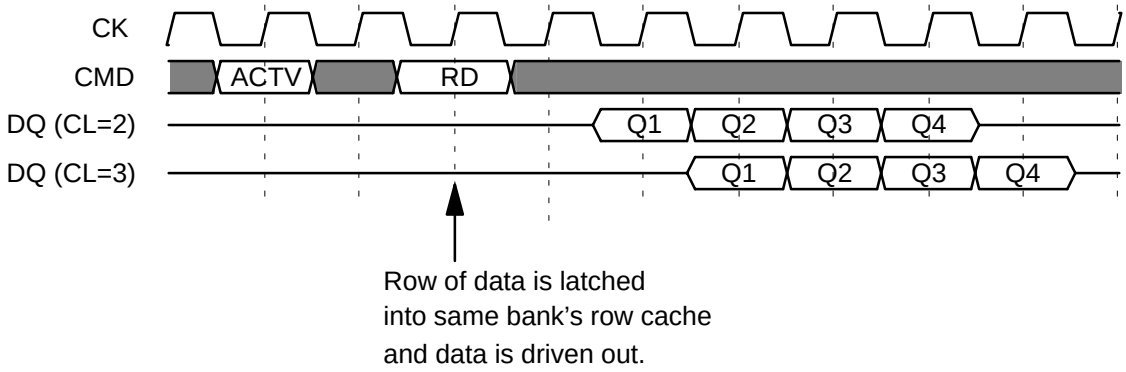
3.11.5.3.2 – Read-Auto Precharge Operation for DDR ESDRAM

The DDR Enhanced SDRAM (DDR ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read-Autoprecharge command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank, and begin the precharge one clock cycle following the Read Autoprecharge command independent of the burst length. In the diagram below, a 4-word burst is shown.



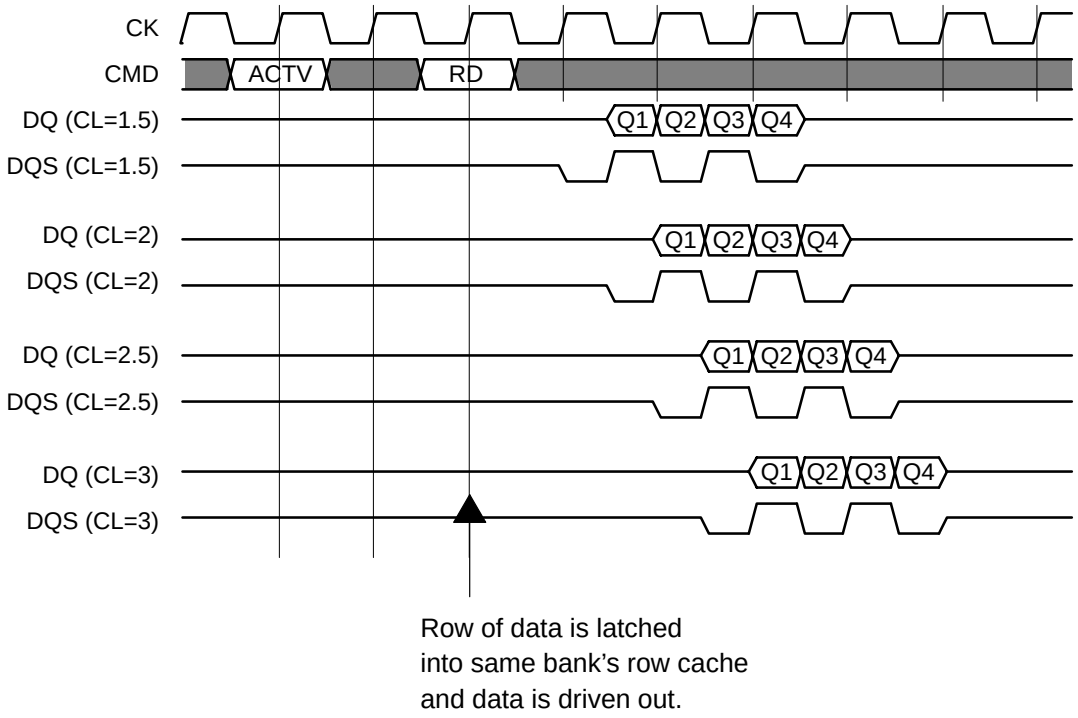
3.11.5.3.3 – Cache Load Operation for SDR ESDRAM

The Enhanced SDRAM (ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank. In the diagram below, a 4-word burst is shown.



3.11.5.3.4 – Cache Load Operation for DDR ESDRAM

The DDR ESDRAM integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read command will initiate a read (burst length defined by the Mode Register) and load the row cache with the contents of the sense amp data from the addressed row of the selected active bank. In the diagram below, a 4-word burst is shown. Although half-clock preamble is shown, it is not a requirement of this proposal.



3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM

"No Write Transfer" mode is an optional mode of operation that allows an Enhanced SDRAM (ESDRAM) to concurrently keep a read page and a write page open per bank. This mode must be entered via an MRS command to the Mode Register by setting the A9 bit to 1.

In "No Write Transfer" mode of operation, the ESDRAM will write only to the DRAM and not the cache in the case of a write page miss, i.e. the row address intended for the write data does not match the previously loaded read page row address. In the case of a write page hit, both the DRAM and the cache are written to maintain coherency. To illustrate the advantages of this mode, the timing diagram above shows same bank operations since fast alternate bank operations can be achieved with standard SDRAM. In the diagram above, a 4-word burst is shown.

		Actions Taken within the ESDRAM in No Write Transfer mode (per bank)				
Command		**Row Cache**	**DRAM**	**Row Addr reg**	**Tag**	**NewPage flag**
ACTV		-	-	Load with current address	No change	Set to 1
Read, Read-AP (NewPage = 1)		Load Cache	-	-	Load with Row Addr reg value	Set to 0
Read, Read-AP (NewPage = 0)		No change	-	-	No change	-
Read, Read-AP (Page Closed)		No change	-	-	No change	Set to 0
Write (Hit) (RowAddr = tag)		Updated	Updated	-	No change	Set to 0
Write (Miss) (RowAddr ≠ tag)		No change	Updated	-	No change	Set to 0

Internal to an ESDRAM are two registers per bank that hold row address information for comparison purposes. A Row Addr register is loaded on a bank activate command and a row address tag is loaded to track what is loaded into the row cache. Also, a one-bit NewPage flag is used only to determine whether to perform a cache load on a read command.

XILINX EXHIBIT 1010
Page 762

3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM (cont.)

The following describe the numbered events in the timing diagram below:

1. The ESDRAM is commanded to perform a Bank Activate. The ESDRAM performs a bank address decode, row address decode, and data is developed in the sense amplifiers exactly like a standard SDRAM. In addition, the ESDRAM loads the current row address into the internal Row Addr register and compares the current row address (in the case shown above, row address = x or y) with the internal tag. The compare result is subsequently used during Write cycles. The ESDRAM also sets an internal NewPage flag.

2. The ESDRAM performs a read, in this case a Read-AP in order to quickly close the read page. If the NewPage flag is set, the row cache is loaded, the current row address is loaded into an internal address tag, and the NewPage flag is subsequently reset. If the NewPage flag is reset, the row cache remains unchanged, and the tag is left unchanged.

3. If a Write or Write-AP command is issued and the current row address does not match the address tag, the ESDRAM performs a write to the DRAM and not to the row cache. The NewPage flag is then reset. If a Write or Write-AP command is issued and the current row address matches the address tag, the ESDRAM performs a write to the DRAM and the row cache. The NewPage flag is then reset.

4. The ESDRAM performs a Read. If the NewPage flag is reset, the chip does not load the cache with the sense amp contents (row y in the diagram above) and drives out the previously loaded row cache data. If the NewPage flag is set, the chip loads the cache with the sense amp contents and drives out the newly loaded row cache data.

5. This case is not shown in the timing diagram, but consider it a case that follows #2 and prior to the 2nd Activate. If a Write or Write-AP command is issued and the current row address matches the address tag, the ESDRAM performs a write to the DRAM and not to the row cache. If a Write or Write-AP command is issued and the current row address matches the Row Addr register, the ESDRAM performs a write to the DRAM and the row cache.

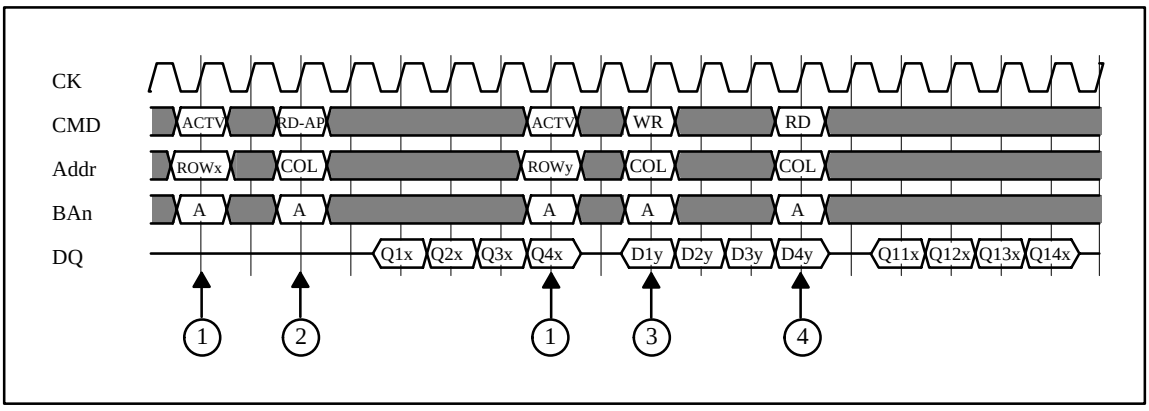


Figure 1, SDR ESDRAM “No Write Transfer” Mode of Operation

3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM

"No Write Transfer" mode is an optional mode of operation that allows a DDR Enhanced SDRAM (DDR ESDRAM) to concurrently keep a read page and a write page open per bank. This mode is entered via an EMRS command to the Mode Register by setting the A9 bit to 1.

In "No Write Transfer" mode of operation, the DDR ESDRAM will write only to the DRAM and not the cache in the case of a write page miss, i.e. the row address intended for the write data does not match the previously loaded read page row address. In the case of a write page hit, both the DRAM and the cache are written to maintain coherency. To illustrate the advantages of this mode, the timing diagram above shows same bank operations since fast alternate bank operations can be achieved with standard DDR SDRAM. In the diagram above, a 4-word burst is shown.

	Actions Taken within the DDR ESDRAM in No Write Transfer mode (per bank)				
Command	**Row Cache**	**DRAM**	**Row Addr reg**	**Tag**	**NewPage flag**
ACTV (NewPage = 0)	-	-	Load with current address	No change	Set to 1
Read, Read-AP (NewPage = 1)	Load Cache	-	-	Load with Row Addr Reg Value	Set to 0
Read, Read-AP (NewPage = 0)	No change	-	-	No change	-
Read, Read-AP (Page Closed)	No change	-	-	No change	Set to 0
Write (Hit) (RowAddr = tag)	Updated	Updated	-	No change	Set to 0
Write (Miss) (RowAddr ≠ tag)	No change	Updated	-	No change	Set to 0

Internal to the DDR ESDRAM are two registers per bank that hold row address information for comparison purposes. A Row Addr register is loaded on a bank activate command and a row address tag is loaded to track what is loaded into the row cache. Also, a one-bit NewPage flag is used only to determine whether to perform a cache load on a read command.

XILINX EXHIBIT 1010
Page 764

3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM (cont.)

The following describe the numbered events in the timing diagram below in Figure 1:

1. The DDR ESDRAM is commanded to perform a Bank Activate. The DDR ESDRAM performs a bank address decode, row address decode, and data is developed in the sense amplifiers exactly like a standard DDR SDRAM. In addition, the DDR ESDRAM loads the current row address into the internal Row Addr register and compares the current row address (in the case shown above, row address = x or y) with the internal tag. The compare result is subsequently used during Write cycles. The DDR ESDRAM also sets an internal NewPage flag.

2. The DDR ESDRAM performs a read, in this case a Read-AP in order to quickly close the read page. If the NewPage flag is set, the row cache is loaded, the current row address is loaded into an internal address tag, and the NewPage flag is subsequently reset. If the NewPage flag is reset, the row cache remains unchanged, and the tag is left unchanged.

3. If a Write or Write-AP command is issued and the current row address does not match the address tag, the DDR ESDRAM performs a write to the DRAM and not to the row cache. The NewPage flag is then reset. If a Write or Write-AP command is issued and the current row address matches the address tag, the DDR ESDRAM performs a write to the DRAM and the row cache. The NewPage flag is then reset.

4. The DDR ESDRAM performs a Read. If the NewPage flag is reset, the chip does not load the cache with the sense amp contents (row y in the diagram above) and drives out the previously loaded row cache data. If the NewPage flag is set, the chip loads the cache with the sense amp contents and drives out the newly loaded row cache data.

5. This case is not shown in the timing diagram, but consider it a case that follows #2 and prior to the 2nd Activate. If a Write or Write-AP command is issued and the current row address matches the address tag, the DDR ESDRAM performs a write to the DRAM and not to the row cache. If a Write or Write-AP command is issued and the current row address matches the Row Addr register, the DDR ESDRAM performs a write to the DRAM and the row cache.

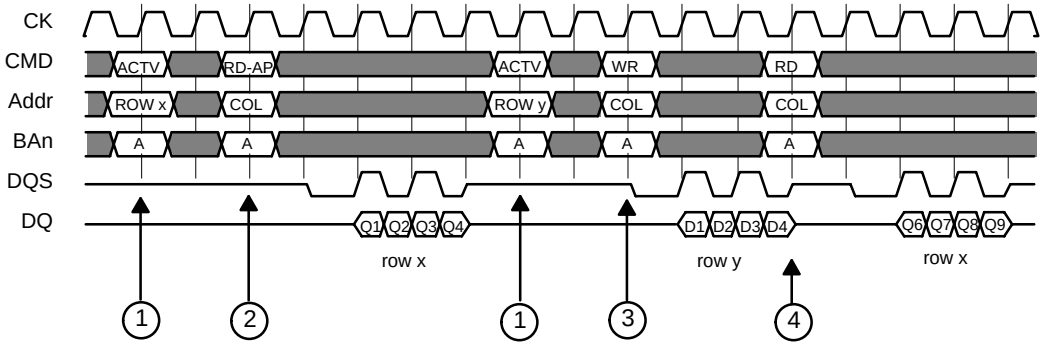


Figure 1, DDR ESDRAM "No Write Transfer" Mode of Operation

XILINX EXHIBIT 1010
Page 766

3.11.5.4 – VCSDRAM Specific SDRAM Functions

The Standards in this section are special functions that are applicable to Virtual Channel SDRAM (VCSDRAM). The standards cover both SDR and DDR devices as stated on the individual Standards.

3.11.5.4.1 – Command Table for Virtual Channel SDR SDRAM

3.11.5.4.2 – Command Table for Virtual Channel DDR SDRAM

3.11.5.4.3 – Virtual Channel SDR SDRAM Mode Register Architecture

3.11.5.4.4 – Virtual Channel DDR SDRAM Mode Register Architecture

XILINX EXHIBIT 1010
Page 767

3.11.5.4.1 – Command Table for Virtual Channel SDR SDRAM

COMMAND	SYMBOL	CKE		S	RAS	CAS	WE	BA	A12	A11	A10 /AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		n–1	n																		
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Prefetch without/with auto precharge	PFC/PFCA	H	X	L	H	H	L	BA	CHA		PS	CHA		L	L	L	X	X	X	SGA	
Pair Prefetch without/with auto precharge	PPF/PPFA	H	X	L	H	H	L	BA	CHA		PS	CHA		L	H	X	X	X	X	SGA	
Prefetch to Dummy	PFD	H	X	L	H	H	L	BA	X	X	X	X	X	L	L	H	X	X	X	SGA	
Restore without/with Auto Precharge	RST/RSTA	H	X	L	H	H	L	BA	CHA		PS	CHA		H	L	X	X	X	X	SGA	
Precharge Selected Bank	PRE	H	X	L	H	H	L	BA	X	X	L	X	X	H	H	X	X	X	X	X	X
Precharge All Banks	PALL	H	X	L	H	H	L	X	X	X	H	X	X	H	H	X	X	X	X	X	X
Channel Read	READ	H	X	L	H	L	H	X	CHA		X	CHA		CA							
Channel Write	WRIT	H	X	L	H	L	L	L	CHA		X	CHA		CA							
Dummy Channel Write without/with Auto Restore	WRD/ WRDA	H	X	L	H	L	L	H	X	X	X	X	RS	CA							
Bank Activate	ACT	H	X	L	L	H	H	BA	RA												
Prefetch Read with Auto Precharge (optional)	PFR	H	X	L	L	H	L	SGA	CHA		SGA	CHA		CA							
Self Register Operation	MRS	H	X	L	L	L	L	L	L	L	L	L	L	TM	CL			BT	BL		

REMARKS H: High Level L: Low Level X: High or Low Level (Don't Care)
PS: Auto Precharge Select (H: with auto precharge, L: without auto precharge)
RS: Auto Restore Select (H: with auto restore, L: without auro restore) BA: Bank Address
RA: Row Address CA: Column Address CHA: Channel Address SGA: Segment Addres
CL: CAS Latency BT: Burst Type BL: Burst Length TM: Test Mode Entry

NOTE: Prefetch Read with Auto Precharge Command is optional

3.11.5.4.1– Command Table for Virtual Channel SDR SDRAM

XILINX EXHIBIT 1010
Page 768

3.11.5.4.2 – Command Table for Virtual Channel DDR SDRAM

COMMAND	SYMBOL	CKE		S	RAS	CAS	WE	BA	A12	A11	A10 /AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		n–1	n																		
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Prefetch without/with auto precharge	PFC/PFCA	H	X	L	H	H	L	BA	CHA		PS	CHA		L	L	L	X	X	X	SGA	
Pair Prefetch without/with auto precharge	PPF/PPFA	H	X	L	H	H	L	BA	CHA		PS	CHA		L	H	X	X	X	X	SGA	
Prefetch to Dummy	PFD	H	X	L	H	H	L	BA	X	X	X	X	X	L	L	H	X	X	X	SGA	
Restore without/with Auto Precharge	RST/RSTA	H	X	L	H	H	L	BA	CHA		PS	CHA		H	L	X	X	X	X	SGA	
Precharge Selected Bank	PRE	H	X	L	H	H	L	BA	X	X	L	X	X	H	H	X	X	X	X	X	X
Precharge All Banks	PALL	H	X	L	H	H	L	X	X	X	H	X	X	H	H	X	X	X	X	X	X
Channel Read	READ	H	X	L	H	L	H	X	CHA		X	CHA				CA					
Channel Write	WRIT	H	X	L	H	L	L	L	CHA		X	CHA				CA					
Dummy Channel Write without/with Auto Restore	WRD/WRDA	H	X	L	H	L	L	H	X	X	X	X	RS			CA					
Bank Activate	ACT	H	X	L	L	H	H	BA	RA												
Prefetch Read with Auto Precharge (optional)	PFR	H	X	L	L	H	L	SGA	CHA		SGA	CHA				CA					
Set Register Operation	MRS	H	X	L	L	L	L	L	L	L	L	L	DR	TM	CL			BT	BL		
	EMRS	H	X	L	L	L	L	H	L	L	L	L	Reserved for future use								DD

REMARKS H: High Level L: Low Level X: High or Low Level (Don't Care)

PS: Auto Precharge Select (H: with auto precharge, L: without auto precharge)

RS: Auto Restore Select (H: with auto restore, L: without auro restore) BA: Bank Address

RA: Row Address CA: Column Address CHA: Channel Address SGA: Segment Address

CL: CAS Latency BT: Burst Type BL: Burst Length TM: Test Mode Entry

NOTE: Prefetch Read with Auto Precharge Command is optional

3.11.5.4.2–Command Table for Virtual Channel DDR SDRAM

XILINX EXHIBIT 1010

3.11.5.4.3 – Virtual Channel SDR SDRAM Mode Register Architecture

0	0	0	0	0	0	1	0	0	0	0	0	0	0

The code shown is reserved for Test Mode entry.

BA	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CL			BT	B.L.		

Mode Register Set

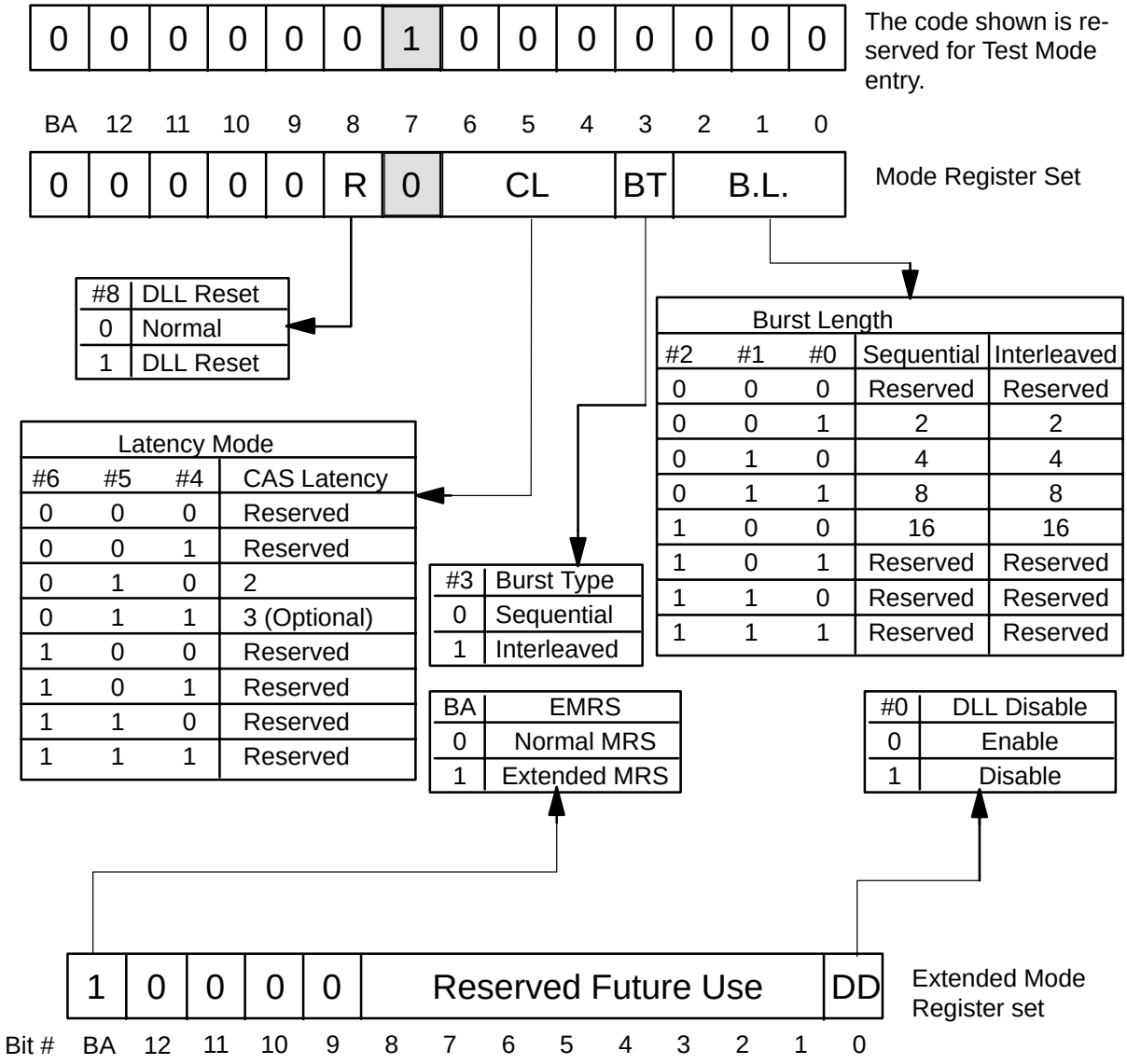
Latency Mode			
#6	#5	#4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (Optional)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

#3	Burst Type
0	Sequential
1	Interleaved

Burst Length				
#2	#1	#0	Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	16	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

XILINX EXHIBIT 1010
Page 770

3.11.5.4.4 – Virtual Channel DDR SDRAM Mode Register Architecture



3.11.5.5 – DDR2 Specific SDRAM Functions

DDR2 SDRAM EMRS2 and EMRS3

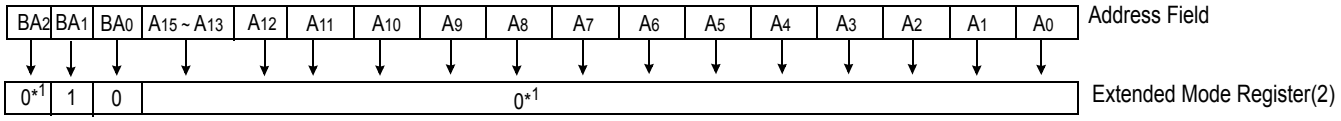
For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/Extended Mode Register Set commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

Notes:

1. Background: This is to ensure future compatibility if/when any new feature is assigned to a bit or bits in EMR(2) or EMR(3).

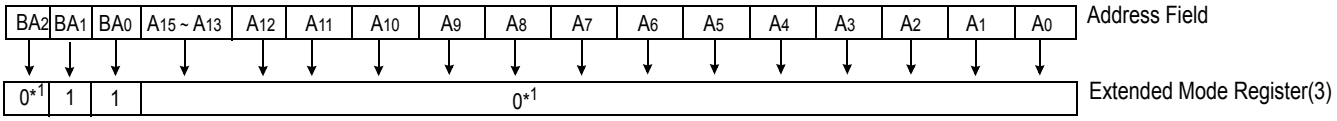
2. EMR(2) and EMR(3): At this time, there are no features defined which use bit(s) in EMR(2) or EMR(3).

EMR(2) Programming: Reserved[*1]



*1: EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMR(3) Programming: Reserved[*1]



*1: EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

3.11.5.6 — GDDR2 Specific SDRAM Functions

MRS Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	tWR			DLL	TM	CAS Latency			WL			BL

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A7	TestMode
0	Normal
1	Test

A8	DLL Reset
0	No
1	Yes

A0	BL
0	4
1	Reserved

A11	A10	A9	WR
0	0	0	Reserved
0	0	1	Reserved
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	Reserved

A6	A5	A4	CAS Latency
0	0	0	8
0	0	1	9
0	1	0	10 (optional)
0	1	1	Reserved
1	0	0	4 (optional)
1	0	1	5
1	1	0	6
1	1	1	7

A3	A2	A1	Write Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2 (optional)
0	1	1	3 (optional)
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (optional)

Notes:
1. All Devices are specified for sequential burst type operation only.

EMRS Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Vendor	System	Output Driver Ron			DLL	DQS	AL	ODT Control		ODT Option	

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A11	Vendor ID
0	Disabled
1	Enabled (optional)

A9	A8	A7	Ron
0	0	0	60
0	0	1	55
0	1	0	50
0	1	1	45
1	0	0	40
1	0	1	35
1	1	0	30
1	1	1	25

A10	System config
0	Single Rank
1	Multi Rank

A3	A2	ODT Control	
0	0	ODT OFF	ODT for DQ,DQM,DQS, /DQS, CK, /CK is off
0	1	Auto Cal	ODT for DQ,DQM,DQS, /DQS, CK, /CK is selected by resistor connected to ZQ pin
1	0	Rterm=60	ODT for DQ,DQM,DQS, /DQS, CK, /CK is nominally 60 ohm
1	1	Rterm=120	ODT for DQ,DQM,DQS, /DQS, CK, /CK is nominally 120 ohm

A1	A0	ODT Option	
0	0	OFF	ODT for CMD/ADR is off
0	1	x1	On die termination of CMD/ADD are same as DQ
1	0	x2	On die termination of CMD/ADD are 2x DQ
1	1	x4	On die termination of CMD/ADD are 4x DQ

A6	DLL
0	OFF
1	ON

A5	DQS
0	Differential
1	Single

A4	Additive Latency
0	0
1	1 (optional)

EMRS2 Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	ODT W	ODT of CKE	ODT option for CS		ODT option for CK		LP	ODT at PD	0	0

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A9	ODT W (optional)
0	Enable
1	Disable

A8	ODT of CKE (optional)
0	Off
1	Same as ADD ODT

A7	A6	ODT of CS (optional)
0	0	OFF
0	1	0.5x ADD ODT
1	0	1x ADD ODT
1	1	Reserved

A5	A4	ODT of CK (optional)
0	0	OFF
0	1	1x DQ ODT
1	0	2x DQ ODT
1	1	4x DQ ODT

A3	Low Power Mode (optional)
0	Self Refresh Mode
1	Fast wake-up Mode

A2	ODT at Power Down (optional)	
0	OFF	All pins except CK, /CK, CKE
1	ON	As defind by EMRS/EMRS2

Notes:

1. Devices must support writing to an EMRS2 register even if the only supported mode is the default mode of operation.
2. If no EMRS2 is issued memory must enter default mode for ODT and Self Refresh
3. If there is a change to EMRS, controller will need to re-issue EMRS2 command if intending to use non-default mode functionality

Default Mode is defined as:

A. ODT W mode will be enabled
B. ODT value for CS and CKE follow ADD/CMD
C. ODT value of CK follows ODT value of DQ
D. Self Refresh mode will be selected
E. ODT of all pins excluding CK,/CK,CKE at power down mode will be disabled

3.11.5.7 – GDDR3 Specific SGRAM Functions

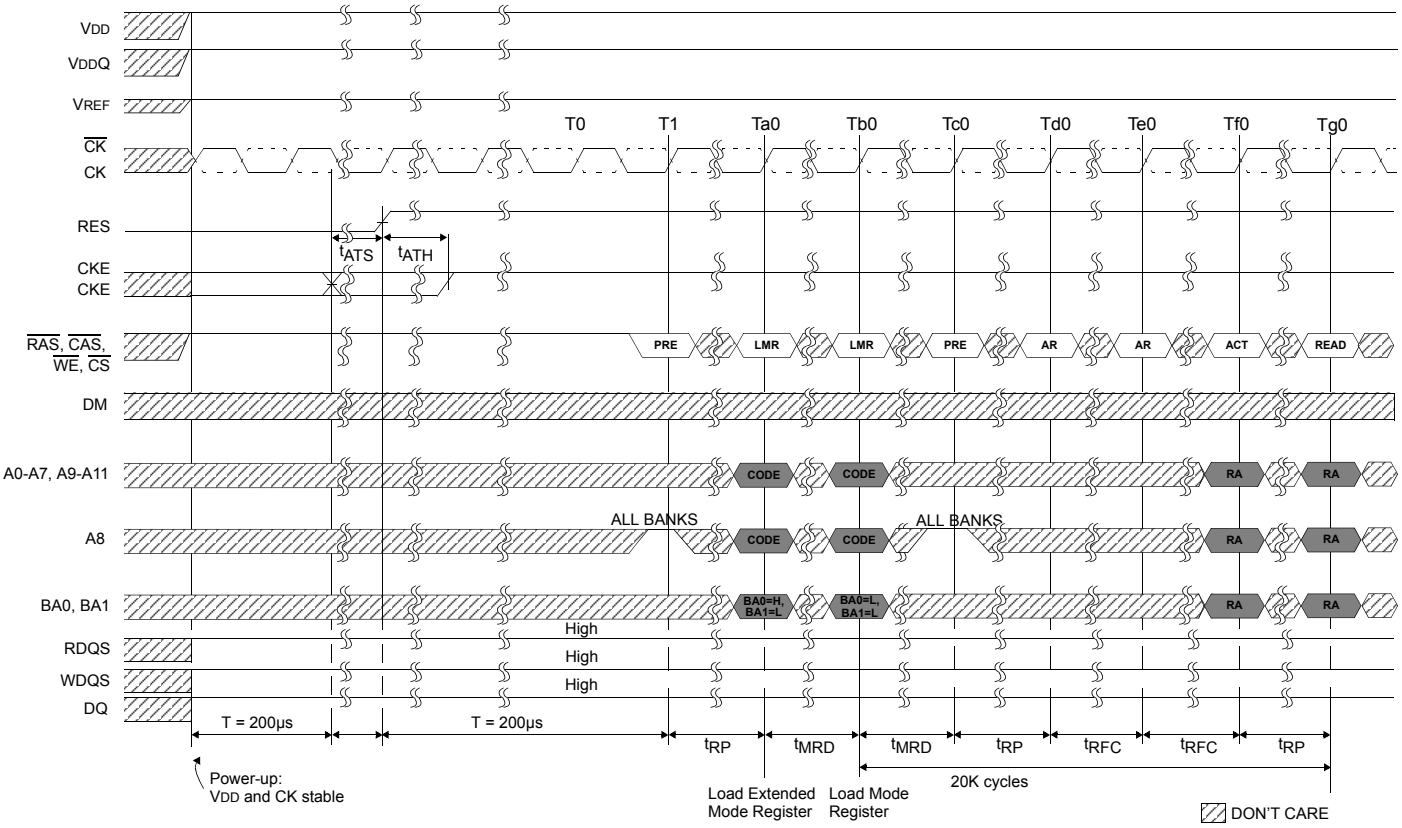
Initialization and Power Up

GDDR3 SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must be first applied to VDD and VDDQ simultaneously, and then to VREF. VREF can be applied any time after VDDQ. Once power has been applied and the clocks are stable the GDDR3 device requires 200µs before the RES pin transitions to high. Upon power-up and after the clock is stable, the on die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. On the rising edge of RES, the CKE pin is latched to determine the on die termination value for the address and control lines. If CKE is sampled at a logic LOW then the on die termination will be set to 1/2 of ZQ and, if CKE is sampled logic HIGH then the on die termination will be set to the same value as ZQ. CKE must meet tATS and tATH on the rising of RES to set the on die termination for address and control lines. Once tATH is met, set CKE to HIGH. An additional 200µs is required for the address and command on die terminations to calibrate and update.

RES must be maintained at a logic LOW-level value and CS must be maintained HIGH, during the first stage of power-up to ensure that the DQ outputs will be in a High-Z state.

After the RES pin transitions from LOW to HIGH wait until a 200µs delay is satisfied. Issue DESELECT on the command bus during this time. Issue a PRECHARGE ALL command. Next a LOAD MODE REGISTER command must be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by the LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 20k clock cycles are required between the DLL reset and any READ command to allow the DLL to lock. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be issued. Following these requirements, the GDDR3 SGRAM is ready for normal operation.


VDD
VDDQ
VREF
CK
CK
RES
CKE
CKE
RAS, CAS,
WE, CS
DM
A0-A7, A9-A11
A8
BA0, BA1
RDQS
WDQS
DQ
T0
T1
Ta0
Tb0
Tc0
Td0
Te0
Tf0
Tg0
tATS
tATH
PRE
LMR
LMR
PRE
AR
AR
ACT
READ
CODE
CODE
RA
RA
ALL BANKS
ALL BANKS
BA0=H,
BA1=L
BA0=L,
BA1=L
High
High
High
T = 200µs
T = 200µs
tRP
tMRD
tMRD
tRP
tRFC
tRFC
tRP
20K cycles
Power-up:
VDD and CK stable
Load Extended
Mode Register
Load Mode
Register
DON'T CARE

ODT Control

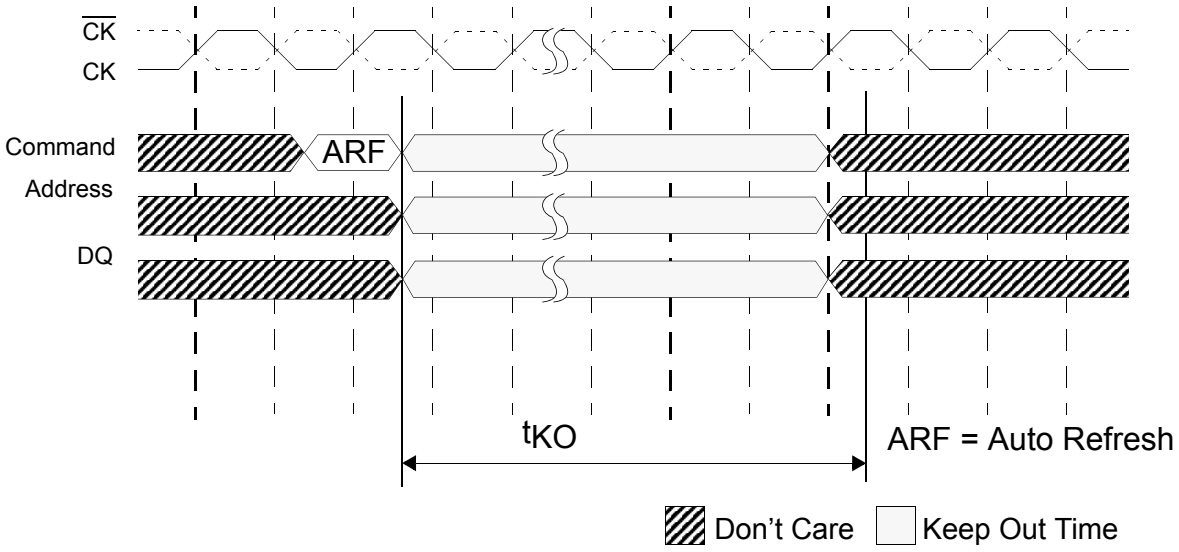
Bus snooping for READ commands excluding CS# is used to control the on die termination in the dual load configuration. The GDDR3 SGRAM will disable the DQ on die terminations when a READ command is detected regardless of the state of CS#. The on die terminations are disabled x clocks after the READ command where x equals CL - 1 and stay off for a duration of BL/2 + 2tCK. In a two-rank system, DRAM devices on both ranks snoop the bus for READ commands to devices on either rank and all DRAMs will disable the on die terminations, for the DQ pins if a READ command is detected. The on die terminations for input pins on the device such as command (except RES), address, WDQS and DM are always on for both a single-rank system and a dual-rank system unless it is turned off in the EMRS.

ODT Updating

The GDDR3 SGRAM uses a programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and $V_{SS}Q$. The value of the resistor must be six times the desired driver impedance. For example, a 240 Ω. resistor is required for an output impedance of 40 Ω. To ensure that output impedance is one-sixth the value of RQ (within 10 percent), RQ should be in the range of 210 Ω to 270 Ω (35Ω – 45 Ω output impedance).

The output impedance and on die termination is updated during every AUTO REFRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all datasheet timings and current specifications are met during an update.

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SGRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 7.8 us (70.2 us). This maximum absolute interval guarantees that the output drivers and the on die terminations of GDDR3 SGRAMs are recalibrated often enough to keep the impedance characteristics of those within the specified boundaries. During the minimum keep out time of tKO after AUTO REFRESH command, DES (i.e. /CS HIGH) should be issued on the command bus, and no activity on the address or data bus is recommended, because the signal integrity on the bus can not be guaranteed during this period.



Definition of Terminology

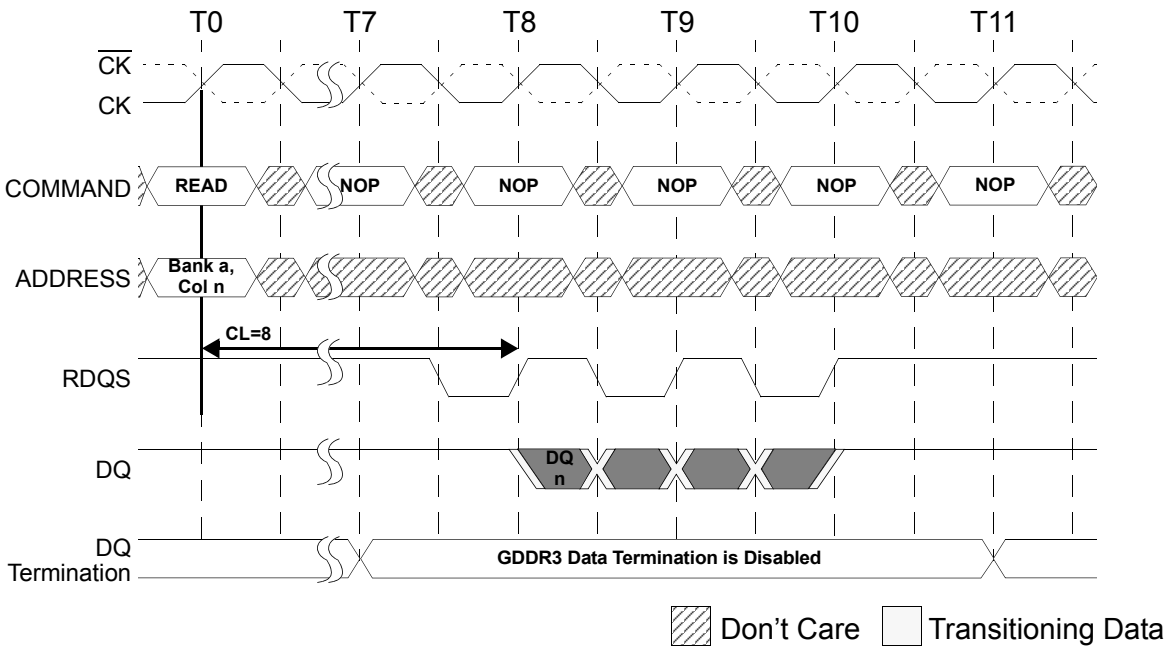
Hereafter are defined terminologies used in the GDDR3 SGRAM specification.
Although GDDR3 might be operated in ODT Disable Mode, it is not recommended and the specification describes the ODT Enable Mode only. Should a system be designed to operate the GDDR3 in ODT Disable Mode, the system should comprehend the effect of the discrepancies between this specification and its own design.

If it is stated that a bus is in one of the following state, it should be interpreted as described.
Following are three terminologies defined for ODT Enable Mode.

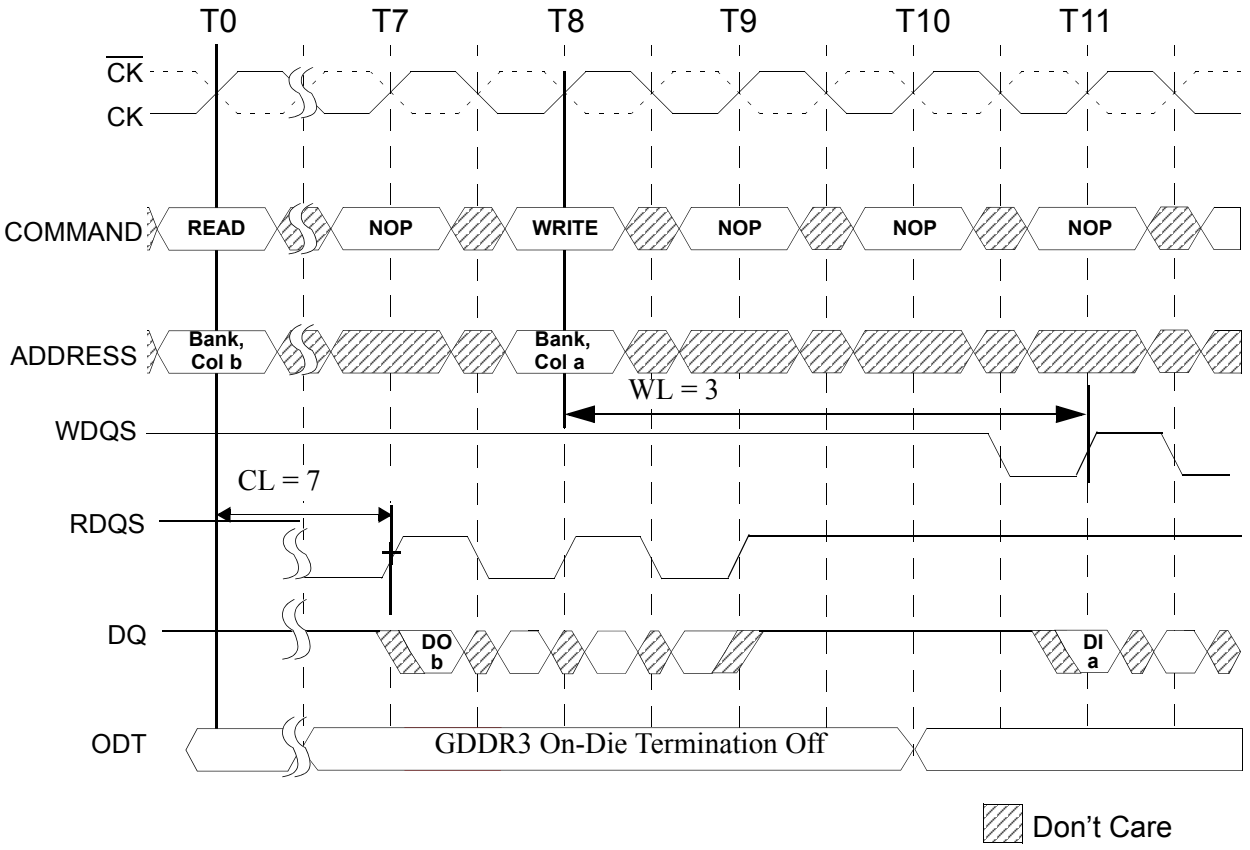
High{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.
Hi-z{terminated}: No driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.
Low{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VOL(DC).

Corresponding terminologies for ODT Disable Mode are defined below. As mentioned before, ODT Disable Mode is not an intended mode of operation. However, there exist situations where ODT Enable Mode can not be guaranteed for a short period of time, like during power up, yet is indeed an intended mode of operation

High{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active.
The voltage level of the bus would be nominally VDDQ.
Hi-z{unterminated}: No driver on the bus is driving the bus. No termination on the bus is active.
The voltage level of the bus would be undefined, because the bus would be floating.
Low{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active.
The voltage level of the bus would be nominally VSSQ.

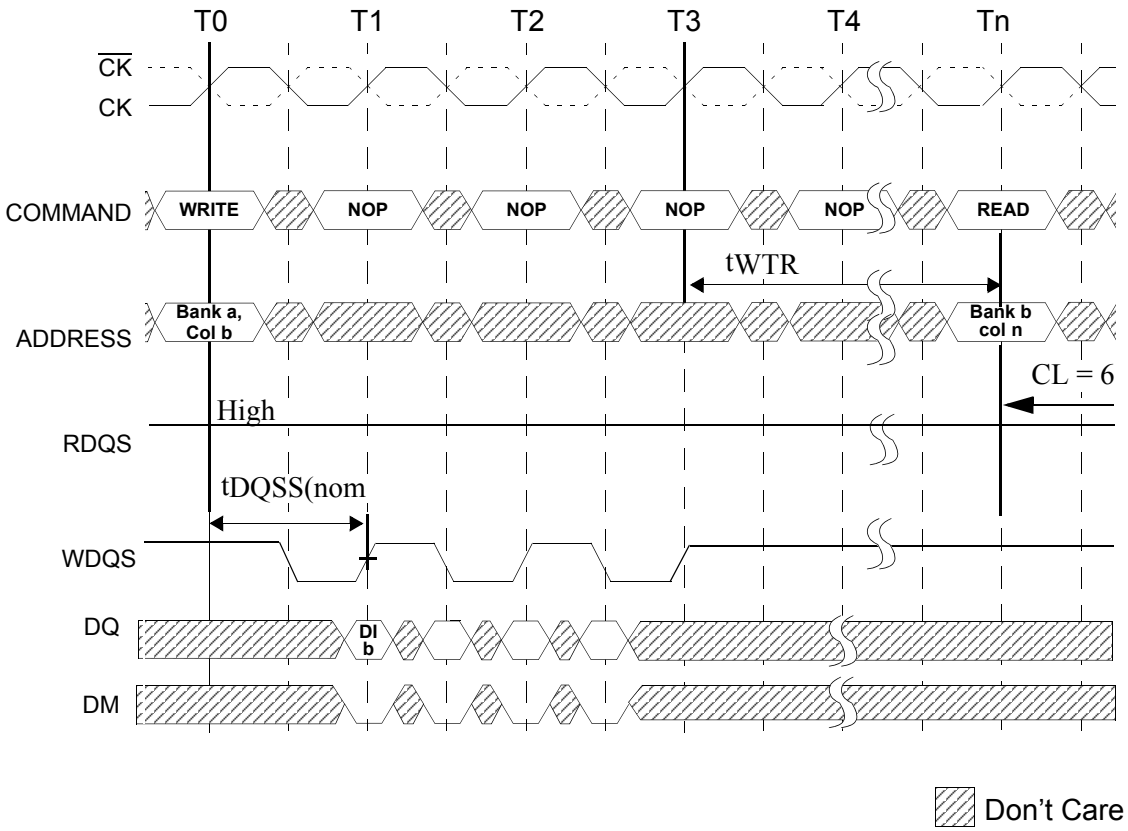

T0
T7
T8
T9
T10
T11
CK
CK
COMMAND
READ
NOP
NOP
NOP
NOP
NOP
ADDRESS
Bank a, Col n
CL=8
RDQS
DQ
DQ n
DQ Termination
GDDR3 Data Termination is Disabled
Don't Care
Transitioning Data

READ To WRITE



Notes
1. Write data can not be driven onto the DQ bus for 2 clock cycles after the READ data is off the bus.
2. The timing diagram covers a READ to a WRITE command from different banks on the same part or the same row in the same bank.

WRITE to READ Timing



1. DI b = Data In for column b
2. Three subsequent elements of Data In are applied following D1 b
3. tWTR is referenced from the first positive CK edge after the last Data In
4. The READ and WRITE commands may be to any bank.
5. WRITE Latency is set to 1.
6. RDQS level is High.

Mirror Function

The GDDR3 SGRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines, assisting in routing devices back to back. The MF ball will affect RAS#, CAS#, WE#, CS# and CKE on balls H3, F4, H9, F9 and H4 respectively and A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, BA0 and BA1 on balls K4, H2, K3, M4, K9, H11, K10, L9, K11, M9, K2, L4, G4 and G9 respectively. MF is LVCMOS input and the MF ball should be tied directly to VSS or VDD depending on the control line orientation desired.

When the MF ball is tied low the ball orientation is as follows, RAS# - H3, CAS# - F4, WE# - H9, CS# - F9, CKE - H4, A0 - K4, A1 - H2, A2 - K3, A3 - M4, A4 - K9, A5 - H11, A6 - K10, A7 - L9, A8 - K11, A9 - M9, A10 - K2, A11 - L4, BA0 - G4 and BA1- G9. The high condition on the MF ball will change the location of the control balls as follows; CS# - F4, CAS# - F9, RAS# - H10, WE# - H4, CKE - H9, A0 - K9, A1- H11, A2 - K10, A3 - M9, A4 - K4, A5 - H2, A6 - K3, A7 - L4, A8 - K2, A9 - M4, A10 - K11, A11 - L9, BA0 - G9 and BA1 - G4.

PINS	MF Logic State	
	HIGH	LOW
RAS#	H10	H3
CAS#	F9	F4
WE#	H4	H9
CS#	F4	F9
CKE	H9	H4
A0	K9	K4
A1	H11	H2
A2	K10	K3
A3	M9	M4
A4	K4	K9
A5	H2	H11
A6	K3	K10
A7	L4	L9
A8	K2	K11
A9	M4	M9
A10	K11	K2
A11	L9	L4
BA0	G9	G4
BA1	G4	G9
BA2	H3	H10

IO and ODT Drive Values

The Driver and Termination impedances are derived from the following test conditions under worst case process corners

1. Nominal 1.8V (VDD/VDDQ)
2. Power the GDDR3 device and calibrate the output drivers and termination to eliminate process variation at 25°C
3. Reduce temperature to 10°C recalibrate.
4. Reduce temperature to 0°C and take the fast corner measurement.
5. Raise temperature to 75°C and recalibrate
6. Raise temperature to 85°C and take the slow corner measurement

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN	MAX
0.1	2.144	3.366
0.2	4.268	6.516
0.3	6.373	9.454
0.4	8.449	12.185
0.5	10.505	14.715
0.6	12.542	17.051
0.7	14.540	19.400
0.8	16.509	21.828
0.9	18.449	24.219
1.0	20.341	26.580
1.1	22.203	28.913
1.2	24.017	31.222
1.3	25.783	33.508
1.4	27.480	35.813
1.5	29.119	38.213
1.6	30.671	40.551
1.7	31.387	42.900
1.8	31.648	45.176

Pull-Up Characteristic at 40ohms		
Voltage (V)	MIN	MAX
0.1	-2.377	-2.946
0.2	-4.705	-5.829
0.3	-6.984	-8.644
0.4	-9.283	-11.383
0.5	-11.524	-14.038
0.6	-13.803	-16.599
0.7	-16.015	-19.051
0.8	-18.285	-21.630
0.9	-20.302	-24.143
1.0	-22.223	-26.605
1.1	-24.066	-29.005
1.2	-25.773	-31.353
1.3	-27.344	-33.619
1.4	-28.683	-35.803
1.5	-29.731	-37.883
1.6	-30.691	-39.882
1.7	-31.544	-42.003
1.8	-32.311	-44.063

XILINX EXHIBIT 1010
Page 784

On Die termination Values

Pull-Up Characteristic at 60ohms		
Voltage (V)	MIN	MAX
0.1	-1.58	-1.96
0.2	-3.14	-3.89
0.3	-4.66	-5.76
0.4	-6.19	-7.59
0.5	-7.68	-9.36
0.6	-9.20	-11.07
0.7	-10.68	-12.70
0.8	-12.19	-14.42
0.9	-13.53	-16.10
1.0	-14.82	-17.74
1.1	-16.04	-19.34
1.2	-17.18	-20.90
1.3	-18.23	-22.41
1.4	-19.12	-23.87
1.5	-19.82	-25.26
1.6	-20.46	-26.59
1.7	-21.03	-28.00
1.8	-21.54	-29.38

Pull-Up Characteristic at 120ohms		
Voltage (V)	MIN	MAX
0.1	-0.79	-0.98
0.2	-1.57	-1.94
0.3	-2.33	-2.88
0.4	-3.09	-3.79
0.5	-3.84	-4.68
0.6	-4.60	-5.53
0.7	-5.34	-6.35
0.8	-6.09	-7.21
0.9	-6.77	-8.05
1.0	-7.41	-8.87
1.1	-8.02	-9.67
1.2	-8.59	-10.45
1.3	-9.11	-11.21
1.4	-9.56	-11.93
1.5	-9.91	-12.63
1.6	-10.23	-13.29
1.7	-10.51	-14.00
1.8	-10.77	-14.69

Pull-Up Characteristic at 240ohms		
Voltage (V)	MIN	MAX
0.1	-0.40	-0.49
0.2	-0.78	-0.97
0.3	-1.16	-1.44
0.4	-1.55	-1.90
0.5	-1.92	-2.34
0.6	-2.30	-2.77
0.7	-2.67	-3.18
0.8	-3.05	-3.60
0.9	-3.38	-4.02
1.0	-3.70	-4.43
1.1	-4.01	-4.83
1.2	-4.30	-5.23
1.3	-4.56	-5.60
1.4	-4.78	-5.97
1.5	-4.96	-6.31
1.6	-5.12	-6.65
1.7	-5.26	-7.00
1.8	-5.39	-7.34

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DDR Presentations and documents

See also Standard 21C JESD21-C

STANDARD 79:

JESD79 **JEDEC Standard 79, Double Data Rate (DDR) SDRAM Specification** (datasheet for 64 Mb SDRAM)

Documents presented at the Platform Conference, San José, CA

DDR II - The Evolution Continues by Mr. Joe Macri JC-42.3 Chairman, ATI Technologies

Configurations and Considerations for DDR Memory by Mr. Bill Gervasi Chairman, JEDEC Memory Parametrics

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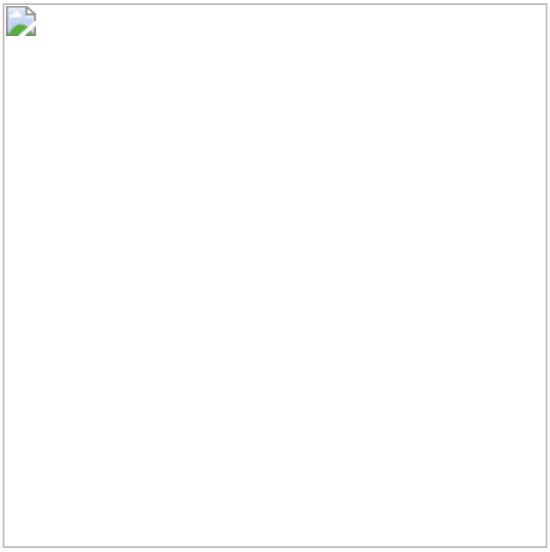


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Integrated Silicon Solution	**Symbios Logic (merged with LSI)**
Intel Corporation	**Taiwan Semiconductor**
International Rectifier	**Tanisys Technology**
Interworks Computer Products	**Technology Works, Inc.**
I/O Data Device, Inc.	**Teledyne Microelec.**
IPAC	**Teradyne Inc.**
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ITW/Camtex	**Texas Instruments**
IXYS Corp.	**Toshiba America**
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Keithly Instruments	**Trimecs Corp.**
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Lambda Advanced Analog	**Unitrode**
Lansdale Semiconductor	**UMC (USA)**
	UTMC
	Vanguard Int'l Semic.
	VIA Technologies, Inc.

Lattice Semiconductor	**Viking Components, Inc.**
LG Semicon (merged with Hyundai)	**Visiontek**
Linear Technology Corp.	**Wells-CTI**
Linfinity Microelectr.	**Western Digital Corp.**
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LSI Logic Corporation	**Winbond Electronics**
Lucent Technologies	**Wintec Industries, Inc.**
	Workstation Direct
	Xicor, Inc.
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Top

List prepared by Julie Carlson

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Return Previous Screen

Page updated: 12/19/2022 06:01:48

Exhibit L

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«Go Back

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Aeroflex UTMC	Microsemi Corporation
Agere Systems	Minco Technology Inc.
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Analog Devices Inc.	Nanya Technology Company
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Arrow Zeus Electronics	New Jersey Micro Electronic Testing Inc.
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ATI Research Silicon Valley Inc.	Nitto Denko America
Atmel Corporation	Nokia Research Center
ATP Electronics Inc.	Northrup Grumman
Avant Technology L.P.	NVIDIA Corporation
Aved Memory Products	OKI Electric Industry Company
Avnet Inc.	Olin Aegis
BAE Systems	ON Semiconductor
Broadcom Corporation	OSE USA
C-MAC Microcircuits Ltd.	Peak International
California Eastern Labs	Pericom Semiconductor
Carsem Inc.	Philips Semiconductors

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Celestica Inc.

Centon Electronics Inc.

Chartered Semiconductor Manufacturing

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Chip Supply Inc.

Cirrus Logic Inc.

Cogiscan Inc.

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Compaq Computer Corporation

Conexant Systems Inc.

Corsair Memory Inc.

Crane Interpoint Corporation

Cray Incorporated

CST (Comp.Serv.Tech)

Cypress Semiconductor

Daewon SPIC/USA

Dane-Elec Corporation

Data Device Corporation

Dataram

Delkin Devices Inc.

Dell Computer

Delphi/Delco

Denali Software

DPAC Technologies Corporation

e.PAK International Incorporated

EEMS Italia SpA

Elite Semiconductor Memory Technology

Elpida Memory Inc.

EMC Corporation

EMS Technologies Inc.

Enhanced Memory Systems

Enplas Tesco Inc.

Entegris Incorporated

Etron Technology Inc.

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Flomerics Inc.

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Foxconn International Inc.

Fujitsu Microelectronics

General Test Laboratory

Plastronics Inc.

PNY Technologies Inc.

Power Innovations Ltd.

Powerex Inc.

Qualcomm Inc.

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RF Micro Devices

Ralink Technology

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Samsung Techwin Co.

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San Max Technologies Inc.

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Sarnoff Corporation

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Semiconductor Insights

Semtech Corporation

Sensitron Semiconductor

Serverworks Corporation

Sharp Electronics

Shikatronics Inc.

Shinko Electric America

Shinon Corporation

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Silicon Graphics Inc.

Silicon Mountain Memory

Silicon Storage Technology

Siliconware USA Inc.

Simple/SiliconTech Technology

Sirenza Microdevices Inc.

Smart Modular Technology

SOISIC

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GSI Technology

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Hewlett Packard Company

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Honeywell SSEC

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Hypertec Limited

Hytek Microsystems

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IXYS Corporation

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Kentron Technologies

Kingston Technology

Kostat Incorporated

Kyocera America Inc.

Lansdale Semiconductor

LeCroy Corporation

Linear Technology Corporation

Littelfuse Inc.

LSI Logic Corporation

STMicroelectronics

Sud-Chemie Performace Packaging

Sun Microsystems Inc.

Super PC Memory

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T-RAM Inc.

Tachyon Semiconductor

Taiwan Semiconductor

Tality UK Limited

Tanisys Technology

Techtronix

Teledyne Microelectronics

Teradyne Inc.

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Top

Exhibit M

• Home »
• Join JEDEC »
• For members »
• Standards-publications »
• JEDEC Store»
• Meetings and events »
• Press and news »
• Search »
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2nd China International IC Industry Exhibition & Seminar IC China 2004
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CD from Lead Free Conference (including Tin Whiskers papers) Oct. 2003 Frankfurt,Germany.

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«Go Back

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A-Data Technology Co.	Micro Memory Bank
Actel Corporation	Micron Technology Inc.
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Advanced Micro Devices	Minco Technology Inc.
Advanced Power Technology	Mini Systems Inc.
Advanced Semiconductor Engineering	Mitsubishi
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Carsem Inc.	Renesas Technology
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Catalyst Semiconductor Inc.	Rochester Electronics
Celestica Inc.	Saifun Semiconductor
Centon Electronics Inc.	Samsung Semiconductor
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Cogiscan Inc.	Sensitron Semiconductor
Corsair Memory Inc.	Serverworks Corporation
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Cypress Semiconductor	Shinko Electric America
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Dataram	Silicon Image
Delkin Devices Inc.	Silicon Integrated Systems
Dell Computer	Silicon Laboratories
Delphi Corporation	Silicon Mountain Memory
Denali Software	Silicon Storage Technology
DPAC Technologies Corporation	Siliconware USA Inc.
e.PAK International Incorporated	Simple/SiliconTech Technology
EEMS Italia SpA	Skyworks Solutions Inc.
Elite Semiconductor Memory Technology	Smart Modular Technology
Elpida Memory Inc.	Sony Microelectronics
EMC Corporation	ST Assembly Test Services
EMS Technologies Inc.	Staktek Corporation
Endicott Interconnect Technologies	STMicroelectronics
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Fluent Incorporated	Tektronix
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Ibiden USA Corporation	Unisys Corporation
IBM Corporation	United Test & Assembly Center
IceFyre Semiconductor Inc.	Universal Networking Machines
	Ventura Technology Corp.

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Inphi Corporation	Virtium Technology Inc.
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Top

Exhibit N

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«Go Back

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Corsair Memory Inc.

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Plastronics Inc.

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PNY Technologies Inc.

Power Integrations Inc.

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Powerex Inc.

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Qualcomm

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Raza Microelectronics Inc.

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Rochester Electronics

Saifun Semiconductor

Samsung Semiconductor

Sanyo Semiconductor

Sarnoff Corporation

Satcon Electronics

Delphi Corporation

Denali Software

Diablo Technologies Inc.

EEMS Italia SpA

Elite Semiconductor Memory Technology

Elpida Memory Inc.

EMC Corporation

EMS Technologies Inc.

Endicott Interconnect Technologies

Enplas Tesco Inc.

Entegris Incorporated

Etron Technology Inc.

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Fairchild Semiconductor

FCI USA Inc.

Flomerics Inc.

Fluent Incorporated

Force 10 Networks Inc.

FormFactor Inc.

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Freescale Semiconductor

Fujitsu Microelectronics America

Gigaram Inc.

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GSI Technology

Hagiwara Sys-com Co., Ltd.

Hana Microelectronics Inc.

Hana Micron Inc.

Hewlett Packard Company

Hi/FN Inc.

Hirose Electric Co.

Honeywell

Huawei Technologies Co. Ltd.

Hynix Semiconductor America Inc.

Hypertec Limited

Hytek Microsystems Inc.

I/O Data Device Inc.

Ibiden USA Corporation

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Semtech Corporation

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Serverworks Corporation

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Silicon Motion Inc.

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Silicon Storage Technology

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Kentron Technologies

Kingmax Semiconductor Inc.

Kingston Technology
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King Tiger Technology Inc.

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LSI Logic Corporation

Lucent Technologies

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TriQuint Semiconductor

TwinMos Technologies

Tyco Electronics

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Unifosa Corporation

Unigen Corporation

Unisys Corporation

United Test & Assembly Center

Universal Network Machines

Ventura Technology Corp.

VIA Technologies Inc.

Viking Interworks
A Sanmina-SCI Company

Virtium Technology Inc.

Vishay General Semiconductor

Vishay Siliconix

Vitesse Semiconductor

VPT Inc.

Wavecrest Corporation

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Top

XILINX EXHIBIT 1010
Page 827