

JEDEC

Solid State Technology Association

JEDEC Standard No. 21-C Release 14

**CONFIGURATIONS FOR
SOLID STATE MEMORIES**

JANUARY 2005

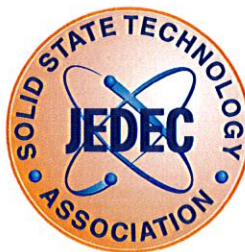
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Contents

Section	Release #	Page #
1 BACKGROUND	Release 1	Page 1 - 1
2 TERMS AND DEFINITIONS	Release 1	Page 2 - 1
2.1 Conventional Device Pin Names	Release 9r10	Page 2 - 2
2.2 Multiport DRAM Pin Names	Release 3	Page 2 - 5
2.3 Power Pin Names	Release 9	Page 2 - 6
2.4 Device Type Names	Release 9r11	Page 2 - 7
2.5 Miscellaneous Device Related Terms	Release 1	Page 2 - 9
2.6 Special Operational Cycles for MPDRAM	Release 1	Page 2 - 10
2.7 Package-Related Terms	Release 5	Page 2 - 12
2.8 Memory Card Pin Names	Release 3	Page 2 - 13
2.9 SRAM and SSRAM special Pin Names	Release 6r11	Page 2-14
2.10 SLD RAM SPECIAL PIN NAMES	Release 9	Page 2-15
3 MEMORY DEVICE STANDARDS	Release 1	Page 3 - 1
3.1 General Standards	Release 1	Page 3.1 -1
3.1.1 Bytewide	Release 1	Page 3.1 -1
3.1.1.1 - 32K TO 256K BY 8 A/A MX FAMILY IN DIP	Release 1	Page 3.1 -1
FIGURE 3.1-1, 32K TO 256K A/A MULTIPLEXED MEMORY IN DIP	Release 1	Page 3.1 -2
3.2 Read Only Memory (ROM)	Release 1	Page 3.2-1
3.2.0 ROM General Standards	Release 5	Page 3.2-2
3.2.0.1 - Mask ROM Fast Address Mode Definition	Release 5	Page 3.2-2
3.2.1 ROM, Byte Wide	Release 1	Page 3.2.1-1
3.2.1.1 - 2K TO 8K BY 8 ROM FAMILY IN DIP, TYPE A	Release 1	Page 3.2.1-1
3.2.1.2 - 4K BY 8 ROM IN DIP, Type B	Release 1	Page 3.2.1-1
3.2.1.3 - 8K TO 128K BY 8 ROM FAMILY IN DIP,	Release 1	Page 3.2.1-1
3.2.1.4 - 2K TO 32K BY 8 ROM FAMILY IN RCC	Release 1	Page 3.2.1-1
3.2.1.5 - 32K TO 512K BY 8 ROM FAMILY IN SOJ,	Release 1	Page 3.2.1-1
3.2.1.6 - 128K TO 1M BY 8 ROM IN DIP,	Release 1	Page 3.2.1-1
3.2.1.7 - 64K TO 512K BY 9 ROM IN DIP,	Release 1	Page 3.2.1-1
3.2.1.8 - 2 TO 64 X 16K BY 8 PAGE SELECT ROM IN DIP,	Release 1	Page 3.2.1-1
3.2.1.9 - 512K and 1M BY 8 ROM IN QFP,	Release 2	Page 3.2.1-1
FIGURE 3.2.1-1, 2K TO 8K BY 8 ROM IN DIP, TYPES A & B	Release 1	Page 3.2.1-2
FIGURE 3.2.1-2, 8K TO 128K BY 8 ROM IN DIP	Release 1	Page 3.2.1-3
FIGURE 3.2.1-3, 2K TO 32K BY 8 ROM IN CC	Release 1	Page 3.2.1-4
FIGURE 3.2.1-4, 32K TO 512K BY 8 ROM IN SOJ	Release 1	Page 3.2.1-5
FIGURE 3.2.1-5, 128K TO 1M BY 8 ROM IN DIP	Release 1	Page 3.2.1-6
FIGURE 3.2.1-6, 64K TO 512K BY 9 ROM IN DIP	Release 1	Page 3.2.1-7
FIGURE 3.2.1-7, 2 TO 64 X 16K BY 8 PAGE SELECT	Release 1	Page 3.2.1-8
FIGURE 3.2.1-8, 512K AND 1M BY 8 ROM IN QFP	Release 2	Page 3.2.1-9
3.2.2 ROM, Word Wide	Release 1	Page 3.2.2-1
3.2.2.1 - 32K TO 256K BY 16 ROM IN DIP	Release 1	Page 3.2.2-3
3.2.2.2 - 32K TO 256K BY 16 ROM IN SCC	Release 1	Page 3.2.2-3
3.2.2.3 - 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN DIP	Release 1	Page 3.2.2-3
3.2.2.4 - 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN RCC	Release 1	Page 3.2.2-3
3.2.2.5 - 256K and 512K BY 16 ROM IN QFP	Release 2	Page 3.2.2-3
3.2.2.6 - 512K TO 128M BY 16 ROM IN DIP AND SOP	Release 6	Page 3.2.2-3
3.2.2.7 - 512K and 1M BY 16 ROM IN SCC	Release 3	Page 3.2.2-3

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
FIGURE 3.2.2-1, 32K TO 256K BY 16 ROM IN DIP	Release 1	Page 3.2.2-5
FIGURE 3.2.2-2, 32K TO 256K BY 16 ROM IN CC	Release 1	Page 3.2.2-6
FIGURE 3.2.2-3, 16K TO 256K BY 16 AQ MX ROM IN DIP	Release 1	Page 3.2.2-7
FIGURE 3.2.2-4, 16K TO 256K BY 16 AQ MX ROM IN CC	Release 1	Page 3.2.2-8
FIGURE 3.2.2-5, 256K AND 512K BY 16 ROM IN QFP	Release 2	Page 3.2.2-9
FIGURE 3.2.2-6, 4M TO 128M BY 16 ROM IN DIP AND SOP	Release 2	Page 3.2.2-10
FIGURE 3.2.2-7, 512K & 1M BY 16 ROM IN SCC	Release 3	Page 3.2.2-11
FIGURE 3.2.2-8, 512K TO 2M BY 16 ROM IN DIP AND SOG	Release 6	Page 3.2.2-12
3.3 Programmable Read Only Memory (PROM)	Release 1	Page 3.3-1
3.3.1 PROM, Nibble Wide	Release 1	Page 3.3.1-1
3.3.1.1 - .25K & .5K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1-3
3.3.1.2 - .25K BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1-3
3.3.1.3 - 1K & 2K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1-3
3.3.1.4 - 1K & 2K BY 4 TTL PROM IN SOP	Release 1	Page 3.3.1-3
3.3.1.5 - 4K TO 8K BY 4 TTL PROM IN DIP	Release 2	Page 3.3.1-3
3.3.1.6 - .25K TO 2K BY 4 TTL PROM FAMILY IN RCC	Release 1	Page 3.3.1-3
3.3.1.7 - 4K BY 4 TTL PROM, 4K BY 4 TTL RPPROM IN SCC	Release 1	Page 3.3.1-3
3.3.1.8 - 1K TO 8K TTL BY 4 PROM FAMILY IN RCC	Release 1	Page 3.3.1-3
3.3.1.9 - 1K TO 8K TTL BY 4 PROM FAMILY IN SCC	Release 1	Page 3.3.1-3
3.3.1.10 - 1K TO 4K BY 4 DPROM FAMILIES IN DIP & SCC	Release 1	Page 3.3.1-4
3.3.1.11 - 1K TO 16K BY 4 ECL PROM FAMILY IN DIP	Release 1	Page 3.3.1-4
FIGURE 3.3.1-1, .25K TO 2K BY 4 TTL PROM IN DIP	Release 1	Page 3.3.1-5
FIGURE 3.3.1-2, 256 BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1-6
FIGURE 3.3.1-3, 1K & 2K BY 4 TTL PROM IN SOG	Release 1	Page 3.3.1-7
FIGURE 3.3.1-4, 4K AND 8K BY 4 TTL PROM IN DIP	Release 2	Page 3.3.1-8
FIGURE 3.3.1-5, .25K TO 4K BY 4 TTL PROM FAMILY IN CC	Release 1	Page 3.3.1-9
FIGURE 3.3.1-6, 1K TO 8K BY 4 TTL PROM IN RCC	Release 1	Page 3.3.1-10
FIGURE 3.3.1-7, 1K TO 8K BY 4 TTL PROM IN SCC	Release 1	Page 3.3.1-11
FIGURE 3.3.1-8, 1K TO 4K BY 4 TTL DPROM IN DIP	Release 1	Page 3.3.1-12
FIGURE 3.3.1-9, 1K TO 4K BY 4 DPROM IN CC	Release 1	Page 3.3.1-13
FIGURE 3.3.1-10, 1K TO 16K BY 4 ECL PROM IN DIP	Release 1	Page 3.3.1-14
3.3.2 PROM, Byte-wide	Release 1	Page 3.3.2-1
3.3.2.1 - 32 BY 8 TTL PROM IN DIP & SCC	Release 1	Page 3.3.2-3
3.3.2.2 - 32 BY 8 ECL PROM IN DIP & SCC	Release 1	Page 3.3.2-3
3.3.2.3 - .25K & .5K BY 8 TTL PROM IN DIP & SCC	Release 1	Page 3.3.2-3
3.3.2.4 - .25K TO 8K BY 8 TTL PROM FAMILY IN DIP	Release 1	Page 3.3.2-3
3.3.2.5 - .5K TO 4K BY 8 TTL LPROM FAMILY IN DIP	Release 1	Page 3.3.2-3
3.3.2.6 - .5K TO 4K BY 8 TTL RPPROM FAMILY IN DIP	Release 1	Page 3.3.2-3
3.3.2.7 - .5K TO 8K BY 8 TTL PROM FAMILIES IN RCC & SCC	Release 1	Page 3.3.2-3
3.3.2.8 - .5K TO 2K BY 8 TTL RPPROM FAMILY IN SCC	Release 1	Page 3.3.2-4
3.3.2.9 - 16K TO 64K BY 8 TTL PROM FAMILY IN DIP	Release 1	Page 3.3.2-4
3.3.2.10 - 512 BY 8 ECL RPPROM IN DIP & SCC	Release 2	Page 3.3.2-4
FIGURE 3.3.2-1, 32 BY 8 TTL & ECL PROM IN DIP	Release 1	Page 3.3.2-5
FIGURE 3.3.2-2, 32, 256, & 512 BY 8 TTL PROM IN CC, 32 BY 8 ECL PROM IN CC	Release 1	Page 3.3.2-6
FIGURE 3.3.2-3, 256 & 512 BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2-7
FIGURE 3.3.2-4, .25K TO 8K BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2-8
FIGURE 3.3.2-5, .5K TO 4K BY 8 TTL LPROM IN DIP	Release 1	Page 3.3.2-9
FIGURE 3.3.2-6, .5K TO 4K BY 8 TTL RPPROM IN DIP	Release 1	Page 3.3.2-10
FIGURE 3.3.2-7, .5K TO 8K BY 8 TTL PROM IN SCC	Release 1	Page 3.3.2-11
FIGURE 3.3.2-8, .5K TO 8K BY 8 TTL PROM IN RCC	Release 1	Page 3.3.2-12
FIGURE 3.3.2-9, .5K TO 2K BY 8 RPPROM IN CC	Release 1	Page 3.3.2-13

Release 14

Section	Release #	Page #
FIGURE 3.3.2-10, 16K TO 64K BY 8 TTL PROM IN DIP	Release 1	Page 3.3.2-14
FIGURE 3.3.2-11, 512 BY 8 10K & 100K ECL R PROM IN DIP AND SCC	Release 2	Page 3.3.2-15
3.3.3 PROM, Word Wide	Release 1	Page 3.3.3-1
3.3.3.1 - 32 AND 64 BY 16 PROM IN DIP AND SCC	Release 1	Page 3.3.3-3
FIGURE 3.3.3-1, 32 AND 64 BY 16 TTL PROM IN DIP	Release 1	Page 3.3.3-5
FIGURE 3.3.3-2, 32 AND 64 BY 16 TTL PROM IN CC	Release 1	Page 3.3.3-6
3.3.4 PROM Package Conversion	Release 1	Page 3.3.4-1
3.3.4.1 - PROM DIP TO SO CONVERSION, 16, 18, 20, 24 DIP	Release 1	Page 3.3.4-1
FIGURE 3.3.4-1, 1K AND 2K TTL PROM 18 DIP TO 20 SO CONVERSION	Release 1	Page 3.3.4-3
3.4 Erasable Programmable Read Only Memory (EPROM)	Release 1	Page 3.4-1
3.4.1 EPROM, Byte Wide	Release 1	Page 3.4.1-1
3.4.1.1 - 4K BY 8 EPROM IN DIP, TYPE A	Release 1	Page 3.4.1-3
3.4.1.2 - 4K AND 8K BY 8 EPROM IN DIP, ...	Release 1	Page 3.4.1-3
3.4.1.3 - 8K TO 64K BY 8 EPROM FAMILY IN DIP, ...	Release 1	Page 3.4.1-3
3.4.1.4 - 2K TO 512K BY 8 EPROM FAMILY IN RCC	Release 1	Page 3.4.1-3
3.4.1.5 - 32K TO 512K BY 8 EPROM FAMILY IN SOJ, ...	Release 1	Page 3.4.1-3
3.4.1.6 - 128K TO 1M BY 8 EPROM FAMILY IN DIP, ...	Release 1	Page 3.4.1-3
3.4.1.7 - 64K TO 512K BY 9 EPROM FAMILY IN DIP, ...	Release 1	Page 3.4.1-3
3.4.1.8 - 2 TO 64 X 16K BY 8 PAGE SELECT EPROM FAMILY IN DIP, ..	Release 1	Page 3.4.1-3
3.4.1.9 - 128K TO 512K BY 8 EPROM FAMILY IN TSOP-1, ...	Release 4	Page 3.4.1-3
FIGURE 3.4.1-1, 4K AND 8K BY 8 EPROM IN DIP, TYPES A & B	Release 1	Page 3.4.1-5
FIGURE 3.4.1-2, 8K TO 64K BY 8 EPROM IN DIP	Release 1	Page 3.4.1-6
FIGURE 3.4.1-3, 2K TO 512K BY 8 EPROM IN CC	Release 1	Page 3.4.1-7
FIGURE 3.4.1-4, 32K TO 512K BY 8 EPROM IN SOJ	Release 1	Page 3.4.1-8
FIGURE 3.4.1-5, 128K TO 1M BY 8 EPROM IN DIP	Release 1	Page 3.4.1-9
FIGURE 3.4.1-6, 64K TO 512K BY 9 EPROM IN DIP	Release 1	Page 3.4.1-10
FIGURE 3.4.1-7, 2 TO 64 X 16K BY 8 PAGE SELECT EPROM IN DIP	Release 1	Page 3.4.1-11
FIGURE 3.4.1-8, 128K TO 512K BY 8 EPROM IN TSOP-1	Release 4	Page 3.4.1-12
3.4.2 EPROM, Word Wide	Release 1	Page 3.4.2-1
3.4.2.1 - 32K TO 256K BY 16 EPROM IN DIP	Release 1	Page 3.4.2-3
3.4.2.2 - 32K TO 256K BY 16 EPROM IN SCC	Release 1	Page 3.4.2-3
3.4.2.3 - 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP	Release 1	Page 3.4.2-3
3.4.2.4 - 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC	Release 1	Page 3.4.2-3
3.4.2.5 - 512K TO 128M BY 16 EPROM or OTP IN DIP AND SOP	Release 6	Page 3.4.2-3
3.4.2.6 - 512K and 1M BY 16 EPROM IN SCC	Release 3	Page 3.4.2-3
3.4.2.7 - 64K TO 256K BY 16 EPROM IN TSOP-1	Release 4	Page 3.4.2-3
FIGURE 3.4.2-1, 32K TO 256K BY 16 EPROM IN DIP	Release 1	Page 3.4.2-5
FIGURE 3.4.2-2, 32K TO 256K BY 16 EPROM IN SCC	Release 1	Page 3.4.2-6
FIGURE 3.4.2-3, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP	Release 1	Page 3.4.2-7
FIGURE 3.4.2-4, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC	Release 1	Page 3.4.2-8
FIGURE 3.4.2-5, 4M TO 128M BY 16 EPROM OR OTP IN DIP AND SOP	Release 1	Page 3.4.2-9
FIGURE 3.4.2-6, 512K & 1M BY 16 EPROM IN CC	Release 3	Page 3.4.2-10
FIGURE 3.4.2-7, 64K BY 256K BY 16 EPROM IN TSOP-1	Release 4	Page 3.4.2-11
FIGURE 3.4.2-8, 512K TO 2M BY 16 EPROM IN DIP AND SOG	Release 6	Page 3.4.2-12
3.5 Electrically Erasable Programmable Read Only Memory (EEPROM) ..	Release 1	Page 3.5-1
3.5.1 EEPROM, Byte Wide	Release 1	Page 3.5.1-1
3.5.1.1 - .5K TO 2K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-2
3.5.1.2 - 2K & 4K BY 8 EEPROM IN RCC	Release 1	Page 3.5.1-2
3.5.1.3 - 1K TO 32K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-2
3.5.1.4 - .5K TO 32K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1-2

JEDEC Standard No. 21-C

Section	Release #	Page #
3.5.1.5 - 32K TO 256K BY 8 EEPROM FAMILY IN SOJ, ...	Release 1	Page 3.5.1-2
3.5.1.6 - 32K TO 512K BY 8 EEPROM FAMILY IN DIP, ...	Release 1	Page 3.5.1-2
3.5.1.7 - 32K TO 256K BY 8 EEPROM FAMILY IN RCC, ...	Release 1	Page 3.5.1-2
3.5.1.8 - 32K TO 256K BY 9 EEPROM FAMILY IN DIP, ...	Release 1	Page 3.5.1-2
3.5.1.9 - 128K TO 1M BY 8 EEPROM FAMILY IN SCC, ...	Release 1	Page 3.5.1-2
3.5.1.10 - 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1	Release 2	Page 3.5.1-3
3.5.1.11 - EXTENDED FEATURE SET FOR 256K BIT EEPROM	Release 2	Page 3.5.1-3
3.5.1.12 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM	Release 3	Page 3.5.1-3
3.5.1.13 - 512K BY 8 DUAL-SUPPLY EEPROM IN RCC	Release 5	Page 3.5.1-3
3.5.1.14 - 128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP1	Release 5	Page 3.5.1-3
3.5.1.15 - 256K, 512K, & 1M BY 8 DUAL-SUPPLY EEPROM IN TSOP1 ..	Release 6	Page 3.5.1-4
3.5.1.16 - 1M TO 8M BY 8 SINGLE-SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1-4
3.5.1.17 - 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2	Release 6	Page 3.5.1-4
3.5.1.18 - 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP2	Release 7	Page 3.5.1-4
3.5.1.19 - 4Mb TO 32Mb DENSITY BY 8 Dual Supply Flash EEPROM in 8 X 5 GRID Micro BGA Package	Release 9 ...	Page 3.5.1-4
3.5.1.20 - 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG ..	Release 9 ...	Page 3.5.1-4
3.5.1.21 - 2-WIRE EEPROM IN SMALL FOOTPRINT PACKAGE	Release 14 ...	Page 3.5.1-4
FIGURE 3.5.1-1, .5K TO 2K BY 8 EEPROM IN DIP	Release 1	Page 3.5.1-5
FIGURE 3.5.1-2, 2K & 4K BY 8 EEPROM IN RCC	Release 1	Page 3.5.1-6
FIGURE 3.5.1-3, 1K TO 32K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-7
FIGURE 3.5.1-4, .5K TO 32K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1-8
FIGURE 3.5.1-5, 32K TO 256K BY 8 EEPROM FAMILY IN SOJ	Release 1	Page 3.5.1-9
FIGURE 3.5.1-6, 32K TO 512K BY 8 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-10
FIGURE 3.5.1-7, 32K TO 256K BY 8 EEPROM FAMILY IN RCC	Release 1	Page 3.5.1-11
FIGURE 3.5.1-8, 32K TO 256K BY 9 EEPROM FAMILY IN DIP	Release 1	Page 3.5.1-12
FIGURE 3.5.1-9, 128K TO 1M BY 8 EEPROM FAMILY IN SCC	Release 1	Page 3.5.1-13
FIGURE 3.5.1-10, 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1	Release 2	Page 3.5.1-14
ADDENDUM 1, 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARD	Release 2	Page 3.5.1-15
FIGURE 3.5.1-11, DUAL SUPPLY EEPROM COMMAND SET	Release 3	Page 3.5.1-23
FIGURE 3.5.1-12, 512K BY 8 DUAL-SUPPLY EEPROM IN RCC	Release 5	Page 3.5.1-24
FIGURE 3.5.1-13, 128K TO 512K SINGLE-SUPPLY EEPROM FAMILY IN DIP	Release 5	Page 3.5.1-25
FIGURE 3.5.1-14, 128K TO 512K SINGLE-SUPPLY EEPROM FAMILY IN RCC	Release 5	Page 3.5.1-26
FIGURE 3.5.1-15, 128K TO 512K SINGLE-SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1-27
FIGURE 3.5.1-16, 1M BY 8 DUAL-SUPPLY EEPROM IN TSOP1	Release 5	Page 3.5.1-28
FIGURE 3.5.1-17, 1M TO 8M SINGLE-SUPPLY EEPROM FAMILY IN TSOP1	Release 5	Page 3.5.1-29
FIGURE 3.5.1-18, 256K & 512K BY 8 DUAL-SUPPLY EEPROM IN TSOP1	Release 6	Page 3.5.1-30
FIGURE 3.5.1-19 A⇒C 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2	Release 6 ..	Page 3.5.1-31⇒33
FIGURE 3.5.1-20, 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP1 ...	Release 7	Page 3.5.1-34
FIGURE 3.5.1-512K TO 4096K X 8 Dual Supply Flash EEPROM IN 8 X 5 GRID Micro BGA Package	Release 9	Page 3.5.1-35
FIGURE 3.5.1-22 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG	Release 9	Page 3.5.1-36
FIGURE 3.5.1-23 2-WIRE EEPROM, MLP 2X3 MM PINOUT	Release 14	Page 3.5.1-37
3.5.2 EEPROM, Word Wide	Release 1	Page 3.5.2-1
3.5.2.1 - 4K TO 32K BY 16 EEPROM IN DIP	Release 1	Page 3.5.2-2
3.5.2.2 - 4K TO 256K BY 16 EEPROM IN SCC	Release 1	Page 3.5.2-2
3.5.2.3 - 256K TO 128M BY 16 EEPROM IN DIP AND SOG	Release 6	Page 3.5.2-2
3.5.2.4 - 1M TO 4M BY 16 DS EEPROM IN SSOP	Release 6	Page 3.5.2-2
3.5.2.5 - 1M TO 4M DENSITY, BY 8 OR 16 EEPROM IN PSOP	Release 7	Page 3.5.2-2
3.5.2.6 - 1M TO 32M DENSITY, BY 8 OR 16 EEPROM IN TSOP1	Release 7	Page 3.5.2-2
3.5.2.7 - 4Mb TO 32Mb DENSITY BY 8 & 16 Dual Supply Flash EEPROM in 8 X 6 GRID Micro BGA Package	Release 9	Page 3.5.2-2

Release 14

Section	Release #	Page #
3.5.2.8 - 16Mb TO 64Mb DENSITY BY 8 & 16, Dual supply Flash EEPROM in 8 X 9 GRID Micro BGA Package	Release 9	Page 3.5.2-3
3.5.2.9 - 8Mb TO 128Mb Density FEEPROM/SRAM in BGA	Release 10	Page 3.5.2-3
3.5.2.10 - 4M TO 64M BY 16 FEEPROM IN TSOP1	Release 11	Page 3.5.2-3
3.5.2.11 - 2M TO 64M BY 16 FEEPROM IN FBGA	Release 11	Page 3.5.2-3
3.5.2.12 - 4M, 8M, & 16M BY 16 FEEPROM with SDRAM Interface	Release 11	Page 3.5.2-3
3.5.2.13 - 128Mb TO 4Gb Density FEEPROM, User Selectable as X8 OR X16 in SSOP	Release 11	Page 3.5.2-4
3.5.2.14 - SINGLE-SUPPLY 16Mb AND 32Mb (x16/x32) FEEPROM IN 80-PIN PQFP	Release 12	Page 3.5.2-4
3.5.2.15 - 128Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL LBGA	Release 14	Page 3.5.2-4
3.5.2.16 - 28Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL LBGA	Release 14	Page 3.5.2-4
3.5.2.17 - 16Mb TO 512Mb (x8/x16) FEEPROM IN 52-PIN TSOP II	Release 14	Page 3.5.2-4
FIGURE 3.5.2-1, 4K TO 32K BY 16 EEPROM FAMILY IN DIP	Release 1	Page 3.5.2-5
FIGURE 3.5.2-2, 4K TO 256K BY 16 EEPROM FAMILY IN SCC	Release 1	Page 3.5.2-6
FIGURE 3.5.2-3, 4M TO 128M BY 16 EEPROM FAMILY IN DIP AND SOG	Release 2	Page 3.5.2-7
FIGURE 3.5.2-4, 256K TO 2M BY 16 EEPROM FAMILY IN DIP AND SOG	Release 6	Page 3.5.2-8
FIGURE 3.5.2-5, 1M TO 4M BY 16 DS EEPROM IN SSOP	Release 6	Page 3.5.2-9
FIGURE 3.5.2-6, 1M TO 4M DENSITY BY 8 OR 16 FEEPROM IN PSOP	Release 7	Page 3.5.2-10
FIGURE 3.5.2-7, 1M TO 32M DENSITY BY 8 OR 16 FEEPROM IN PSOP	Release 7	Page 3.5.2-11
FIGURE 3.5.2-8, 512K TO 2048K X 8, 256K TO 2048K X 16, Dual Supply Flash EEPROM IN 8 X 6 GRID Micro BGA Package	Release 9	Page 3.5.2-12
FIGURE 3.5.2-9, 2048K & 8192K X 8, 1024K & 4096K X 16, Dual supply Flash EEPROM IN 8 X 9 GRID Micro BGA Package	Release 9	Page 3.5.2-13
FIGURE 3.5.2-10, FEEPROM/SRAM Mixed Technology, Multi Chip Device	Release 10/11	Page 3.5.2-14⇒19
FIGURE 3.5.2-11, 4M TO 64M BY 16 FEEPROM IN TSOP1	Release 11	Page 3.5.2-20
FIGURE 3.5.2-12, 32Mb TO 1Gb Density BY 16 FEEPROM IN BGA	Release 11	Page 3.5.2-21
FIGURE 3.5.2-13, 4M TO 16M BY 16 FEEPROM With SDRAM Interface In TSOP2	Release 11	Page 3.5.2-22
FIGURE 3.5.2-14, 4M TO 16M BY 16 FEEPROM With SDRAM Interface in FBGA	Release 11	Page 3.5.2-23
FIGURE 3.5.2-15, 128Mb TO 4Gb FEEPROM, user selectable as X8 or X16 in SSOP	Release 11	Page 3.5.2-24
FIGURE 3.5.2-16, SINGLE-SUPPLY 16Mb AND 32Mb (x16/x32) FEEPROM IN 80-PIN PQFP	Release 12	Page 3.5.2-25
FIGURE 3.5.2-17, 128Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL LBGA	Release 14	Page 3.5.2-26
FIGURE 3.5.2-18, 128Mb TO 1Gb (x8/x16) FEEPROM IN 64-BALL TFBGA	Release 14	Page 3.5.2-27
FIGURE 3.5.2-19, 16Mb TO 256Mb (x8/x16) FEEPROM IN 56-PIN TSOP II	Release 14	Page 3.5.2-28
3.5.3 EEPROM EXTENDED FEATURES	Release 1	Page 3.5.3-1
3.5.3.1 - EXTENDED FEATURE SET FOR 256Kb EEPROM	Release 1	Page 3.5.3-3
3.5.3.2 - DUAL SUPPLY EEPROM COMMAND SET	Release 7	Page 3.5.3-13
3.5.3.3 - SINGLE SUPPLY EEPROM COMMAND CODES	Release 7	Page 3.5.3-14
3.5.3.4 - EEPROM TOGGLE BIT FEATURE	Release 7	Page 3.5.3-15
3.5.3.5 - SYNCHRONOUS DRAM INTERFACE EEPROM (FLASH) IN 86-PIN TSOP-2 AND 90-BALL FBGA	Release 12	Page 3.5.3-16
3.5.3.6 - EEPROM with Two SPD Software Write Protect Methods	Release 14	Page 3.5.3-19
3.6 Non volatile Random Access Memory (NVRAM)	Release 1	Page 3.6-1
3.6.1 NVRAM, Nibble Wide	Release 1	Page 3.6-3
3.6.1.1 - .25K & 1K BY 4 NVRAM IN DIP	Release 1	Page 3.6-3
3.6.2 NVRAM, BYTE WIDE	Release 1	Page 3.6-3
3.6.2.1 - .5K, 1K BY 8 NVRAM IN DIP	Release 1	Page 3.6-3
3.6.2.2 - .5K & 1K BY 8 NVRAM IN RCC	Release 1	Page 3.6-3
3.6.2.3 - .5K TO 16K BY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6-3
3.6.2.4 - .5K TO 16K BY 8 NVRAM FAMILY IN RCC	Release 1	Page 3.6-3
3.6.2.5 - 32K TO 256K BY 8 NVRAM FAMILY IN SOJ,	Release 1	Page 3.6-3
3.6.2.6 - 32K TO 256K BY 8 NVRAM FAMILY IN DIP,	Release 1	Page 3.6-3
3.6.2.7 - 16K TO 128K BY 9 NVRAM FAMILY IN DIP,	Release 1	Page 3.6-3

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
FIGURE 3.6-1, .25K & 1K BY 4 NVRAM IN DIP	Release 1	Page 3.6-5
FIGURE 3.6-2, .5K & 1K BY 8 NVRAM IN DIP	Release 1	Page 3.6-6
FIGURE 3.6-3, .5K & 1K BY 8 NVRAM IN RCC	Release 1	Page 3.6-7
FIGURE 3.6-4, .5K TO 16K BY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6-8
FIGURE 3.6-5, .5K TO 16K BY 8 NVRAM FAMILY IN RCC	Release 1	Page 3.6-9
FIGURE 3.6-6, 32K TO 256K BY 8 NVRAM FAMILY IN SOJ	Release 1	Page 3.6-10
FIGURE 3.6-7, 32K TO 256K NY 8 NVRAM FAMILY IN DIP	Release 1	Page 3.6-11
FIGURE 3.6-8, 16K TO 128K BY 9 NVRAM FAMILY IN DIP	Release 1	Page 3.6-12
3.7 Static Random Access Memory (SRAM)	Release 1	Page 3.7-1
3.7.1 - JTAG Extension to Revolutionary Pinout SRAM Devices	Release 4	Page 3.7-1
FIGURE 3.7-1, JTAG ADDITION TO REVOLUTIONARY PINOUT SRAM	Release 4	Page 3.7-3
FIGURE 3.7-2, State Diagram for Pipelined-Burst SRAM	Release 7	Page 3.7-4
3.7.1 Bit Wide TTL SRAM	Release 1	Page 3.7.1-1
3.7.1.1 - .25K & 1K BY 1 TTL SRAM IN DIP	Release 1	Page 3.7.1-3
3.7.1.2 - .25K & 1K BY 1 TTL SRAM IN SCC	Release 1	Page 3.7.1-3
3.7.1.3 - 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.1-3
3.7.1.4 - 16K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-3
3.7.1.5 - 64K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-3
3.7.1.6 - 16K TO 2M BY 1 TTL SRAM IN SOJ	Release 5	Page 3.7.1-3
3.7.1.7 - 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.1-3
3.7.1.8 - 256K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-3
3.7.1.9 - 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.1-3
FIGURE 3.7.1-1, 0.25K & 1K BY 1 TTL SRAM IN DIP	Release 1	Page 3.7.1-5
FIGURE 3.7.1-2, 0.25K & 1K BY 1 TTL SRAM IN SCC	Release 1	Page 3.7.1-6
FIGURE 3.7.1-3, 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.1-7
FIGURE 3.7.1-4, 16K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-8
FIGURE 3.7.1-5, 64K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-9
FIGURE 3.7.1-6, 16K TO 2M BY 1 TTL SRAM IN SOJ AND TSOP-2	Release 5	Page 3.7.1-10
FIGURE 3.7.1-7, 256K TO 16M BY 1 TTL SRAM AND SSRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.1-11
FIGURE 3.7.1-8, 256K BY 1 TTL SRAM IN RCC	Release 1	Page 3.7.1-12
FIGURE 3.7.1-9, 4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ ..	Release 4	Page 3.7.1-13
3.7.2 Bit Wide ECL SRAM	Release 1	Page 3.7.2-1
3.7.2.1 - 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.2-3
3.7.2.2 - 256K TO 16M BY 1 ECL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.2-3
3.7.2.3 - 64K AND 256K BY 1 ECL SRAM IN FLATPACK	Release 2	Page 3.7.2-3
3.7.2.4 - 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.2-3
FIGURE 3.7.2-1, 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.2-5
FIGURE 3.7.2-2, 256K TO 16M BY 1 ECL SRAM AND SSRAM FAMILY IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.2-6
FIGURE 3.7.2-3, 64K AND 256K BY 1 ECL SRAM IN FP	Release 2	Page 3.7.2-7
FIGURE 3.7.2-4, 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, TSOP2, & SOJ ...	Release 4	Page 3.7.2-8
3.7.3 Nibble Wide TTL SRAM	Release 1	Page 3.7.3-1
3.7.3.1 - 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC	Release 1	Page 3.7.3-3
3.7.3.2 - .25K BY 4 TTL SRAM IN DIP & RCC	Release 1	Page 3.7.3-3
3.7.3.3 - 256 BY 4 TTL SRAM WITH G IN SCC	Release 1	Page 3.7.3-3
3.7.3.4 - 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP	Release 1	Page 3.7.3-3

Release 14

Section	Release #	Page #
3.7.3.5 - 4K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-3
3.7.3.6 - 4K TO 1M BY 4 TTL SRAM WITH G FAMILY IN DIP	Release 1	Page 3.7.3-3
3.7.3.7 - 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN RCC	Release 1	Page 3.7.3-3
3.7.3.8 - 16K & 64K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-3
3.7.3.9 - 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ AND TSOP-2	Release 5	Page 3.7.3-4
3.7.3.10 - 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-4
3.7.3.11 - 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-4
3.7.3.12 - 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-4
3.7.3.13 - 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ	Release 1	Page 3.7.3-4
3.7.3.14 - 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ	Release 1	Page 3.7.3-4
FIGURE 3.7.3-1, 16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN DIP ...	Release 1	Page 3.7.3-5
FIGURE 3.7.3-2, 16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN SCC ...	Release 1	Page 3.7.3-6
FIGURE 3.7.3-3, 256 BY 4 TTL SRAM IN DIP	Release 1	Page 3.7.3-7
FIGURE 3.7.3-4, 256 BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-8
FIGURE 3.7.3-5, 256 BY 4 TTL SRAM IN SCC	Release 1	Page 3.7.3-9
FIGURE 3.7.3-6, 4K TO 64K BY 4 TTL SRAM FAMILY WITHOUT G IN DIP	Release 1	Page 3.7.3-10
FIGURE 3.7.3-7, 4K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-11
FIGURE 3.7.3-8, 4K TO 256K BY 4 TTL SRAM FAMILY WITH G IN DIP	Release 1	Page 3.7.3-12
FIGURE 3.7.3-9, 16K TO 256K BY 4 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.3-13
FIGURE 3.7.3-10, 16K & 64K BY 4 TTL SRAM IN RCC	Release 1	Page 3.7.3-14
FIGURE 3.7.3-11, 4K TO 1M BY 4 TTL SRAM WITH AND W/O G IN SOJ AND TSOP-2	Release 1	Page 3.7.3-15
FIGURE 3.7.3-12, 64K TO 4M BY 4 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ ...	Release 4	Page 3.7.3-16
FIGURE 3.7.3-13, 64K TO 4M BY 4 TTL SRAM FAMILY WITH SEPARATE DATA I/O IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.3-17
FIGURE 3.7.3-14, 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.3-18
FIGURE 3.7.3-15, 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ	Release 1	Page 3.7.3-19
3.7.4 Nibble Wide ECL SRAM	Release 1	Page 3.7.4-1
3.7.4.1 - .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP	Release 1	Page 3.7.4-3
3.7.4.2 - 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP	Release 1	Page 3.7.4-3
3.7.4.3 - .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.4-3
3.7.4.4 - 16K BY 4, 10K & 100K ECL SSRAM IN DIP	Release 1	Page 3.7.4-3
3.7.4.5 - 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-3
3.7.4.6 - 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-3
3.7.4.7 - 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
3.7.4.8 - 64K BY 4 ECL SRAM IN FP	Release 2	Page 3.7.4-4
3.7.4.9 - 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ	Release 2	Page 3.7.4-4
3.7.4.10 - 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
3.7.4.11 - 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
3.7.4.12 - 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-4
FIGURE 3.7.4-1, 256 BY 4, 100K ECL SRAM IN DIP, 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP	Release 1	Page 3.7.4-5
FIGURE 3.7.4-2, 256 & 1K BY 4, 100K ECL SRAM IN SFP	Release 1	Page 3.7.4-6
FIGURE 3.7.4-4, 0.25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP	Release 1	Page 3.7.4-7

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
FIGURE 3.7.4-5, 16K BY 4, 10K & 100K ECL SSRAM IN DIP	Release 1	Page 3.7.4-8
FIGURE 3.7.4-6, 64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-9
FIGURE 3.7.4-7, 64K TO 4M BY 4 ECL SRAM WITH SEPARATE I/O FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-10
FIGURE 3.7.4-8, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-11
FIGURE 3.7.4-9, 64K BY 4 ECL SRAM IN FP	Release 2	Page 3.7.4-12
FIGURE 3.7.4-10, 256K BY 4 or 512K BY 2 CONFIGURABLE ECL SRAM IN DIP AND SOJ	Release 2	Page 3.7.4-13
FIGURE 3.7.4-11, 64K TO 4M BY 4 BIT SELECTABLE ECL SRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-14
FIGURE 3.7.4-12, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-15
FIGURE 3.7.4-13, 64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.4-16
3.7.5 Byte Wide TTL SRAM	Release 1	Page 3.7.5-1
3.7.5.1 - 64 BY 9 TTL SRAM IN SCC	Release 1	Page 3.7.5-3
3.7.5.2 - 1K & 2K BY 8 TTL SRAM IN DIP	Release 1	Page 3.7.5-3
3.7.5.3 - 2K & 4K BY 8 TTL SRAM IN RCC	Release 1	Page 3.7.5-3
3.7.5.4 - 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ	Release 1	Page 3.7.5-3
3.7.5.5 - .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.5-3
3.7.5.6 - 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP-2	Release 4	Page 3.7.5-3
3.7.5.7 - 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5-3
3.7.5.8 - 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5-3
3.7.5.9 - 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP-2	Release 4	Page 3.7.5-3
3.7.5.10 - 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ	Release 1	Page 3.7.5-3
3.7.5.11 - 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC	Release 1	Page 3.7.5-3
3.7.5.12 - 32K BY 9 CACHE SRAM IN 44 SCC	Release 2	Page 3.7.5-3
3.7.5.13 - 128K BY 8 SRAM IN TSOP1	Release 2	Page 3.7.5-3
3.7.5.14 - 128K BY 8 & 9 SSRAM IN SOJ	Release 2	Page 3.7.5-3
3.7.5.15 - 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP	Release 2	Page 3.7.5-3
3.7.5.16 - 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO-N	Release 3	Page 3.7.5-3
3.7.5.17 - 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP AND SOJ	Release 3	Page 3.7.5-4
3.7.5.18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA	Release 5	Page 3.7.5-4
3.7.5.19 - 128K TO 2M BY 8/9 SSRAM IN BGA	Release 5	Page 3.7.5-4
3.7.5.20 - 32K BY 8 SRAM IN TSOP1	Release 7	Page 3.7.5-4
3.7.5.21 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 209 BGA	Release 12	Page 3.7.5-4
3.7.5.22 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 221 BGA	Release 12	Page 3.7.5-4
FIGURE 3.7.5-1, 64 BY 9 SRAM IN SCC	Release 1	Page 3.7.5-5
FIGURE 3.7.5-2, 1K & 2K BY 8 TTL SRAM IN DIP	Release 1	Page 3.7.5-6
FIGURE 3.7.5-3, 2K & 4K BY 8 TTL SRAM IN RCC	Release 1	Page 3.7.5-7
FIGURE 3.7.5-4, 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ	Release 1	Page 3.7.5-8
FIGURE 3.7.5-5, 0.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.5-9
FIGURE 3.7.5-6, 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ	Release 4	Page 3.7.5-10
FIGURE 3.7.5-7, 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5-11
FIGURE 3.7.5-8, 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.5-12
FIGURE 3.7.5-9, 32K TO 2M BY 8 AND 9 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.5-13
FIGURE 3.7.5-10, 32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ	Release 4	Page 3.7.5-14
FIGURE 3.7.5-11, 2K TO 32K BY 9 DPSRAM FAMILY IN SCC	Release 1	Page 3.7.5-15
FIGURE 3.7.5-12, 32K BY 9 TTL CACHE SRAM IN SCC	Release 2	Page 3.7.5-16
FIGURE 3.7.5-13, 128K BY 8 TTL SRAM IN TSOP1	Release 2c9	Page 3.7.5-17
FIGURE 3.7.5-14, 128K BY 8 & 9 TTL SSRAM IN SOJ	Release 2	Page 3.7.5-18
	Release 14	

Section	Release #	Page #
FIGURE 3.7.5-15A, 1K AND 2K BY 9 DPSRAM IN DIP	Release 2	Page 3.7.5-19
FIGURE 3.7.5-15B, 1K AND 2K BY 9 DPSRAM TRUTH TABLE	Release 2	Page 3.7.5-20
FIGURE 3.7.5-16, 128K TO 512K BY 8 SRAM IN CDSO-N	Release 3	Page 3.7.5-21
FIGURE 3.7.5-17, 128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ	Release 4	Page 3.7.5-22
FIGURE 3.7.5-18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA	Release 5	Page 3.7.5-23
FIGURE 3.7.5-19 - 128K TO 2M BY 8/9 SSRAM BGA IN BGA	Release 5	Page 3.7.5-24
FIGURE 3.7.5-20 - 128K TO 2M BY 8/9 SSRAM BGA BOUNDARY SCAN ORDER	Release 5	Page 3.7.5-25
FIGURE 3.7.5-21 - 32K BY 8 SRAM IN TSOP2	Release 7	Page 3.7.5-26
FIGURE 3.7.5-22 - 1Mb - 128Mb (x9) Sync Separate I/O SRAM in 209 BGA	Release 12	Page 3.7.5-27
FIGURE 3.7.5-23 - 1Mb - 128Mb (x9) Sync Separate I/O SRAM in 221 BGA	Release 12	Page 3.7.5-28
3.7.6 Byte Wide ECL SRAM	Release 1	Page 3.7.6-1
3.7.6.1 - 32K and 128K BY 8 ECL SSRAM IN SOJ, SSOP, AND FP	Release 2	Page 3.7.6-1
FIGURE 3.7.6-1, 32K AND 256K BY 9 ECL SSRAM IN SOJ, SOP, AND FP	Release 2	Page 3.7.6-3
3.7.7 Word Wide TTL SRAM	Release 11	Page 3.7.7-1
3.7.7.1 - 4K TO 64K BY 16 TTL SRAM IN DIP	Release 1	Page 3.7.7-2
3.7.7.2 - 4K TO 256K BY 16 TTL SRAM IN SCC	Release 1	Page 3.7.7-2
3.7.7.3 - 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP	Release 1	Page 3.7.7-2
3.7.7.4 - 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC	Release 1	Page 3.7.7-2
3.7.7.5 - 16K AND 64K BY 18 SRAM IN SCC	Release 1	Page 3.7.7-2
3.7.7.6 - 64K BY 16 & 18 SRAM IN 44 SOJ	Release 3	Page 3.7.7-2
3.7.7.7 - 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES	Release 4	Page 3.7.7-2
3.7.7.8 - 64K TO 256K BY 18 SRAM & SSRAM IN TQFP	Release 5	Page 3.7.7-3
3.7.7.9 - 64K TO 1M BY 16/18 BURST SRAM IN BGA	Release 5	Page 3.7.7-3
3.7.7.10 - 64K TO 1M BY 16/18 SSRAM IN BGA	Release 5	Page 3.7.7-3
3.7.7.11 - 64K TO 256K BY 16/18 BURST SRAM IN QFP/TQFP	Release 6	Page 3.7.7-3
3.7.7.12 - 256K AND 1M BY 16/18 SRAM IN TSOP2	Release 6	Page 3.7.7-3
3.7.7.13 - 1Mb TO 128Mb Density, BY 16 OR 18 BURST SRAM IN 221 BGA	Release 11	Page 3.7.7-3
3.7.7.14 - 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 209 BGA, with Common I/O	Release 11	Page 3.7.7-3
3.7.7.15 - 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 221 BGA, with Common I/O	Release 11	Page 3.7.7-3
3.7.7.16 - 1Mb TO 128Mb Density, BY 18 SIGMA SRAM IN 209 BGA, with Separate I/O	Release 12	Page 3.7.7-4
3.7.7.17 - 1Mb TO 128Mb Density, BY 18 SIGMA SRAM IN 221 BGA, with Separate I/O	Release 12	Page 3.7.7-4
3.7.7.18 - 8Mb TO 128Mb Density, BY 18 SRAM IN 165 BGA, with Separate I/O	Release 12	Page 3.7.7-4
3.7.7.19 - 2Mb TO 256Mb Density, BY 16 or 18 Burst SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.7-4
3.7.7.20 - 2Mb TO 256Mb Density, BY 16 or 18 Network SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.7-4
3.7.7.21 - 52-Pin TSOP II Pin Assignment for Low Power SRAMs	Release 14	Page 3.7.7-4
FIGURE 3.7.7-1, 4K TO 64K BY 16 TTL SRAM FAMILY IN DIP	Release 1	Page 3.7.7-5
FIGURE 3.7.7-2, 4K TO 256K BY 16 TTL SRAM FAMILY IN RCC	Release 1	Page 3.7.7-6
FIGURE 3.7.7-3, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN DIP	Release 1	Page 3.7.7-7
FIGURE 3.7.7-4, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN RCC	Release 1	Page 3.7.7-8
FIGURE 3.7.7-5, 16K AND 64K BY 18 SRAM IN SCC	Release 1	Page 3.7.7-9
FIGURE 3.7.7-6, 64K BY 16 & 18 SRAM IN SOJ	Release 3	Page 3.7.7-10
FIGURE 3.7.7-7 A, 32K & 64K BY 16 & 18 SRAM AND SSRAM WITH LOGIC FEATURES IN SCC	Release 4	Page 3.7.7-11
FIGURE 3.7.7-7 B, WRITE CLOCK TIMING FOR SSRAM WITH BURST MODE	Release 4	Page 3.7.7-12
FIGURE 3.7.7-8, 64K TO 256K BY 18 SRAM AND SSRAM IN TQFP	Release 5	Page 3.7.7-13
FIGURE 3.7.7-9, 64K TO 1M BY 16/18 BURST SRAM BGA PADOUT	Release 5	Page 3.7.7-14

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
FIGURE 3.7.7-10, 64K TO 1M BY 16/18 SSRAM BGA PADOUT	Release 5	Page 3.7.7-15
FIGURE 3.7.7-11, 64K TO 1M BY 16/18 SSRAM BGA BOUNDARY SCAN ORDER	Release 5c8	Page 3.7.7-16
FIGURE 3.7.7-12, 64K TO 256K BY 16/18 BURST SRAM IN TQFP	Release 6	Page 3.7.7-17
FIGURE 3.7.7-13, 256K AND 1M BY 16/18 SRAM IN TSOP2	Release 6	Page 3.7.7-18
FIGURE 3.7.7-14, 1Mb TO 128Mb Density, BY 16 OR 18 BURST SRAM IN 221 BGA	Release 11a	Page 3.7.7-19
FIGURE 3.7.7-15, 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 209 BGA	Release 11a	Page 3.7.7-20
FIGURE 3.7.7-16, 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 221 BGA	Release 11a	Page 3.7.7-21
FIGURE 3.7.7-17, X18 SIGMA SRAM WITH SEPARATE I/O IN 209 BGA	Release 12	Page 3.7.7-22
FIGURE 3.7.7-18, X18 SIGMA SRAM WITH SEPARATE I/O IN 221 BGA	Release 12	Page 3.7.7-23
FIGURE 3.7.7-19, 8Mb - 128Mb Density in X18 SRAM WITH SEPARATE I/O IN 165 BGA	Release 12	Page 3.7.7-24
FIGURE 3.7.7-20, 2 Mb - 256 Mb Density in X16/18 BURST SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.7-25
FIGURE 3.7.7-21, 2 Mb - 256 Mb Density in X16/18 NETWORK SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.7-26
FIGURE 3.7.7-22, 52-Pin TSOP II Pin Assignment for Low Power SRAMs	Release 14	Page 3.7.7-28
3.7.8 Double Word Wide SRAM	Release 5	Page 3.7.8-1
3.7.8.1 - 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP	Release 6	Page 3.7.8-2
3.7.8.2 - 32K TO 128K BY 36 SRAM & SSRAM IN TQFP	Release 5	Page 3.7.8-2
3.7.8.3 - 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT	Release 5	Page 3.7.8-2
3.7.8.4 - 32K TO 512K BY 32/36 SSRAM BGA PADOUT	Release 5c11	Page 3.7.8-2
3.7.8.5 - 16K TO 36K BY 32 & 64 SSRAM With BURST Counter IN QFP	Release 7	Page 3.7.8-2
3.7.8.6 - 16K TO 256K BY 36 & 72 BURST SRAM IN BGA	Release 7	Page 3.7.8-2
3.7.8.7 - 1Mb TO 128Mb Density, BY 32 OR 36 BURST SRAM IN 221 BGA	Release 11	Page 3.7.8-2
3.7.8.8 - 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 209 BGA, with Common I/O	Release 11	Page 3.7.8-3
3.7.8.9 - 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 221 BGA, with Common I/O	Release 11	Page 3.7.8-3
3.7.8.10 - 1Mb TO 128Mb Density, BY 36 SIGMA SRAM IN 209 BGA, with Separate I/O	Release 12	Page 3.7.8-3
3.7.8.11 - 1Mb TO 128Mb Density, BY 36 SIGMA SRAM IN 221 BGA, with Separate I/O	Release 12	Page 3.7.8-3
3.7.8.12 - 16Mb TO 256Mb Density, BY 36 SRAM IN 165 BGA, with Separate I/O	Release 12	Page 3.7.8-3
3.7.8.13 - 8Mb TO 128Mb Density, BY 36 DDR SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.8-3
3.7.8.14 - 2Mb TO 256Mb Density, BY 32 or 36 Burst SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.8-3
3.7.8.15 - 2Mb TO 256Mb Density, BY 32 or 36 Network SRAM IN 165 BGA, with Common I/O	Release 12	Page 3.7.8-4
FIGURE 3.7.8-1, 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP	Release 6c9	Page 3.7.8-5
FIGURE 3.7.8-2, 32K TO 128K BY 36 SRAM AND SSRAM IN TQFP	Release 5	Page 3.7.8-6
FIGURE 3.7.7-3 - 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT	Release 5	Page 3.7.8-7
FIGURE 3.7.7-4 - 32K TO 512K BY 32/36 SSRAM BGA PADOUT	Release 5	Page 3.7.8-8
FIGURE 3.7.7-5 - 32K TO 512K BY 32/36 SSRAM BGA BOUNDARY SCAN ORDER	Release 5	Page 3.7.8-9
FIGURE 3.7.8-6, 16K TO 36K BY 32 & 64 SSRAM With BURST Counter IN QFP	Release 7	Page 3.7.8-10
FIGURE 3.7.8-7, 16K TO 256K BY 36 & 72 BURST SSRAM IN BGA	Release 7	Page 3.7.8-11
FIGURE 3.7.8-8, 1Mb TO 128Mb Density, BY 32 OR 36 BURST SRAM IN 221 BGA	Release 11a	Page 3.7.8-12
FIGURE 3.7.8-9, 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 209 BGA	Release 11a	Page 3.7.8-13
FIGURE 3.7.8-10, 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 221 BGA	Release 11a	Page 3.7.8-14
FIGURE 3.7.8-11, X36 SIGMA SRAM WITH SEPARATE I/O IN 209 BGA	Release 12	Page 3.7.8-15
FIGURE 3.7.8-12, X36 SIGMA SRAM WITH SEPARATE I/O IN 221 BGA	Release 12	Page 3.7.8-16
FIGURE 3.7.8-13, X36 SRAM WITH SEPARATE I/O IN 165 BGA	Release 12	Page 3.7.8-17
FIGURE 3.7.8-14, X36 DDR SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.8-18
FIGURE 3.7.8-15, X32/36 BURST SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.8-19
FIGURE 3.7.8-16, X32/36 NETWORK SRAM WITH COMMON I/O IN 165 BGA	Release 12	Page 3.7.8-20

Release 14

Section	Release #	Page #
3.7.9 Eight Byte Wide SRAM	Release 11a ..	Page 3.7.9-1
3.7.9.1 - 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 209 BGA	Release 11a ...	Page 3.7.9-2
3.7.9.2 - 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 221 BGA	Release 11a ...	Page 3.7.9-2
3.7.9.3 - 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 209 BGA	Release 11a ...	Page 3.7.9-2
3.7.9.4 - 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 221 BGA	Release 11a ...	Page 3.7.9-2
FIGURE 3.7.9-1, 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 209 BGA ..	Release 11a	Page 3.7.9-3
FIGURE 3.7.9-2, 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 221 BGA ..	Release 11a	Page 3.7.9-4
FIGURE 3.7.9-3, 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 209 BGA ..	Release 11a	Page 3.7.9-5
FIGURE 3.7.9-4, 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 221 BGA ..	Release 11a	Page 3.7.9-6
3.8 Pseudostatic Random Access Memory (PSRAM)	Release 1	Page 3.8-1
3.8.1 PSRAM, Byte Wide	Release 1	Page 3.8-3
3.8.1.1 - 2K TO 8K BY 8 PSRAM FAMILY IN DIP	Release 1	Page 3.8-3
3.8.1.2 - 2K TO 16K BY 8 PSRAM FAMILY IN RCC	Release 1	Page 3.8-3
3.8.1.3 - 32K TO 512K BY 8 PSRAM FAMILY IN SOJ	Release 1	Page 3.8-3
3.8.2 PSRAM, Word Wide	Release 1	Page 3.8-3
3.8.2.1 - 4K TO 32K BY 16 PSRAM IN DIP	Release 1	Page 3.8-3
3.8.2.2 - 4K TO 256K BY 16 PSRAM IN SCC	Release 1	Page 3.8-3
FIGURE 3.8-1, 2K TO 8K BY 8 PSRAM FAMILY IN DIP	Release 1	Page 3.8-4
FIGURE 3.8-2, 2K TO 16K BY 8 PSRAM FAMILY IN RCC	Release 1	Page 3.8-5
FIGURE 3.8-3, 32K TO 512K BY 8 PSRAM FAMILY IN SOJ	Release 1	Page 3.8-6
FIGURE 3.8-4, 4K TO 32K BY 16 PSRAM FAMILY IN DIP	Release 1	Page 3.8-7
FIGURE 3.8-5, 4K TO 256K BY 16 PSRAM FAMILY IN SCC	Release 1	Page 3.8-8
3.9 Dynamic Random Access Memory (DRAM)	Release 1	Page 3.9-1
3.9.1 Bit Wide DRAM	Release 1	Page 3.9.1-1
3.9.1.1 - 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES	Release 1	Page 3.9.1-3
3.9.1.2 - 16K TO 256K BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-3
3.9.1.3 - 16K TO 256K BY 1 DRAM IN RCC	Release 1	Page 3.9.1-3
3.9.1.4 - 64K & 256K BY 1 DRAM IN ZIP	Release 1	Page 3.9.1-3
3.9.1.5 - 1M AND 4M BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-3
3.9.1.6 - 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2	Release 4	Page 3.9.1-3
3.9.1.7 - 1M TO 16M BY 1 DRAM FAMILY IN ZIP	Release 4	Page 3.9.1-3
3.9.1.8 - 1M TO 16M BY 1 NON-MUX DRAM FAMILY IN SOJ	Release 1	Page 3.9.1-3
3.9.1.9 - 1M BY 1 DRAM IN TSOP1	Release 1	Page 3.9.1-4
3.9.1.10 - 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ	Release 1	Page 3.9.1-4
3.9.1.11 - 64M BY 1 DRAM IN SOJ OR TSOP2	Release 5	Page 3.9.1-4
3.9.1.12 - 2 X 16M BY 1 DRAM IN TSOP2	Release 4	Page 3.9.1-4
3.9.1.13 - 16M BY 1 DRAM IN USON	Release 9	Page 3.9.1-4
FIGURE 3.9.1-1, 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES 16K TO 256K BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-5
FIGURE 3.9.1-2, 16K TO 256K BY 1 DRAM IN RCC	Release 1	Page 3.9.1-6
FIGURE 3.9.1-3, 64K & 256K BY 1 DRAM IN ZIP	Release 1	Page 3.9.1-7
FIGURE 3.9.1-4, 1M TO 64M BY 1 DRAM FAMILY IN DIP	Release 1	Page 3.9.1-8
FIGURE 3.9.1-5, 1M TO 16M BY 1 DRAM FAMILY IN SOJ and TSOP-2	Release 4	Page 3.9.1-9
FIGURE 3.9.1-6, 1M TO 16M BY 1 DRAM FAMILY IN ZIP	Release 4	Page 3.9.1-10
FIGURE 3.9.1-7, 1M TO 16M BY 1 NON-MUX DRAM FAMILY IN SOJ	Release 2	Page 3.9.1-11
FIGURE 3.9.1-8, 1M BY 1 DRAM IN TSOP1	Release 2	Page 3.9.1-12
FIGURE 3.9.1-9, 16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.1-13
FIGURE 3.9.1-10, 64M BY 1 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.1-14
FIGURE 3.9.1-11, 2 X 16M BY 1 DRAM IN TSOP2	Release 4	Page 3.9.1-15
FIGURE 3.9.1-12, 64M BY 1 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.1-16
FIGURE 3.9.1-13 16M BY 1 DRAM IN USON	Release 9	Page 3.9.1-17

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
3.9.2 Nibble Wide DRAM	Release 1	Page 3.9.2-1
3.9.2.1 - 16K & 64K BY 4 DRAM IN DIP	Release 1	Page 3.9.2-2
3.9.2.2 - 16K BY 4 DRAM IN DIP	Release 1	Page 3.9.2-2
3.9.2.3 - 64K BY 4 DRAM IN RCC	Release 1	Page 3.9.2-2
3.9.2.4 - 256K & 1M BY 4 DRAM FAMILY IN DIP	Release 2	Page 3.9.2-2
3.9.2.5 - 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2	Release 4	Page 3.9.2-2
3.9.2.6 - 64K TO 4M BY 4 DRAM IN ZIP	Release 2	Page 3.9.2-2
3.9.2.7 - 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2	Release 3	Page 3.9.2-2
3.9.2.8 - 256K BY 4 DRAM IN TSOP1	Release 2	Page 3.9.2-2
3.9.2.9 - 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.2-3
3.9.2.10 - 256K TO 4M BY 4 NON-MUX DRAM FAMILY IN SOJ	Release 2	Page 3.9.2-3
3.9.2.11 - 4M BY 4 DRAM WITH 1 CE AND 4 CE IN TSOP2	Release 2	Page 3.9.2-3
3.9.2.12 - 16M BY 4 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.2-3
3.9.2.13 - 1M, 2M, 4M BY 2 DRAM IN SOJ & TSOP2	Release 3r7	Page 3.9.2-3
3.9.2.14 - 16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2	Release 6	Page 3.9.2-3
3.9.2.15 - 64M BY 4 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.2-3
3.9.2.16 - 4M BY 4 DRAM IN USON	Release 9	Page 3.9.2-4
3.9.2.17 - 16M BY 4 DRAM IN USON	Release 9	Page 3.9.2-4
FIGURE 3.9.2-1, 16K & 64K BY 4 DRAM IN DIP	Release 1	Page 3.9.2-5
FIGURE 3.9.2-2, 16K & 64K BY 4 DRAM IN RCC	Release 1	Page 3.9.2-6
FIGURE 3.9.2-3, 256K & 1M BY 4 DRAM FAMILY IN DIP	Release 1	Page 3.9.2-7
FIGURE 3.9.2-4, 256K TO 4M BY 4 DRAM IN SOJ AND TSOP-2	Release 4	Page 3.9.2-8
FIGURE 3.9.2-5, 64K TO 4M BY 4 DRAM IN ZIP	Release 1	Page 3.9.2-9
FIGURE 3.9.2-6, 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2	Release 6	Page 3.9.2-10
FIGURE 3.9.2-7, 256K BY 4 DRAM IN TSOP1	Release 2	Page 3.9.2-11
FIGURE 3.9.2-8, 4M BY 4/16M BY 1 CONFIGURABLE DRAM IN SOJ	Release 2	Page 3.9.2-12
FIGURE 3.9.2-9, 256K TO 4M BY 4 NON-MUX DRAM IN SOJ	Release 2	Page 3.9.2-13
FIGURE 3.9.2-10, 4M BY 4 DRAM WITH 4 CE IN SOJ AND TSOP2	Release 6	Page 3.9.2-14
FIGURE 3.9.2-11, 16M BY 4 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.2-15
FIGURE 3.9.2-12, 1M, 2M, 4M BY 2 DRAM WITH 2 CE IN SOJ AND TSOP2	Release 4r7	Page 3.9.2-16
FIGURE 3.9.2-13, 16M BY 4 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.2-17
FIGURE 3.9.2-14, 16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2	Release 6r7	Page 3.9.2-18
FIGURE 3.9.2-15, 64M BY 4 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.2-19
FIGURE 3.9.2-16 4M BY 4 DRAM IN USON	Release 9	Page 3.9.2-20
FIGURE 3.9.2-17 16M BY 4 DRAM IN USON	Release 9	Page 3.9.2-21
3.9.3 Byte Wide DRAM	Release 1	Page 3.9.3-1
3.9.3.1 - 32K BY 8 DRAM IN DIP	Release 1	Page 3.9.3-3
3.9.3.2 - 32K BY 8 DRAM IN RCC	Release 1	Page 3.9.3-3
3.9.3.3 - 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP	Release 2	Page 3.9.3-3
3.9.3.4 - 512K BY 8 & BY 9 NON-MUX DRAM IN SOJ	Release 2	Page 3.9.3-3
3.9.3.5 - 2M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3-3
3.9.3.6 - 8M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3-3
3.9.3.7 - 32M BY 8 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.3-3
3.9.3.8 - 4M & 8M BY 8 DRAM IN SOP	Release 8	Page 3.9.3-4
3.9.3.9 - 2M BY 8 DRAM IN USON	Release 9	Page 3.9.3-4
3.9.3.10 - 8M BY 8 DRAM IN USON	Release 9	Page 3.9.3-4
FIGURE 3.9.3-1, 32K BY 8 DRAM IN DIP	Release 1	Page 3.9.3-5
FIGURE 3.9.3-2, 32K BY 8 DRAM IN RCC	Release 1	Page 3.9.3-6
FIGURE 3.9.3-3, 512K BY 8 & 9 DRAM IN SOJ	Release 2	Page 3.9.3-7
FIGURE 3.9.3-4, 512K BY 8 & 9 DRAM IN ZIP	Release 2	Page 3.9.3-8
FIGURE 3.9.3-5, 512K BY 8 & 9 NON-MUX DRAM IN SOJ	Release 2	Page 3.9.3-9

Release 14

Section	Release #	Page #
FIGURE 3.9.3-6, 2M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 5	Page 3.9.3-10
FIGURE 3.9.3-7, 8M BY 8 & 9 DRAM IN SOJ & TSOP2	Release 4 a	Page 3.9.3-11
FIGURE 3.9.3-8, 8M BY 8 DRAM IN SOJ & TSOP2	Release 5r7	Page 3.9.3-12
FIGURE 3.9.3-9, 32M BY 8 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.3-13
FIGURE 3.9.3-10, 4M & 8M BY 8 DRAM IN SOP	Release 8	Page 3.9.3-14
FIGURE 3.9.3-11 2M BY 8 DRAM IN USON	Release 9	Page 3.9.3-15
FIGURE 3.9.3-12 8M BY 8 DRAM IN USON	Release 9	Page 3.9.3-16
3.9.4 Word Wide DRAM	Release 1	Page 3.9.4-1
3.9.4.1 - 64K BY 16 DRAM WITH 2 W IN SOJ & TSOP2	Release 1	Page 3.9.4-3
3.9.4.2 - 256K & 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ & TSOP2 ...	Release 5	Page 3.9.4-3
3.9.4.3 - 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ	Release 4	Page 3.9.4-3
3.9.4.4 - 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP2	Release 6r7	Page 3.9.4-3
3.9.4.5 - 128K AND 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, AND ZIP	Release 6	Page 3.9.4-3
3.9.4.6 - 16M BY 16 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4-4
3.9.4.7 - 128K AND 256K BY 32 DRAM WITH 4 CAS IN TSOP2	Release 6	Page 3.9.4-4
3.9.4.8 - 512K AND 2M BY 32 & 36 DRAM WITH 4 CAS IN TSOP2	Release 6r10	Page 3.9.4-4
3.9.4.9 - 8M BY 32 DRAM IN TSOP2 PIN ROTATION	Release 6r9	Page 3.9.4-4
3.9.4.10 - 2M BY 32 DRAM IN TSOP2	Release 7	Page 3.9.4-4
3.9.4.11 - 2M BY 32 DRAM WITH EDO IN QFP	Release 6r8	Page 3.9.4-4
3.9.4.12 - 1M BY 16 DRAM IN USON	Release 9	Page 3.9.4-4
3.9.4.13 - 4M BY 16 DRAM IN USON	Release 9	Page 3.9.4-4
FIGURE 3.9.4-1, 64K BY 16 DRAM IN SOJ	Release 1	Page 3.9.4-5
FIGURE 3.9.4-2, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN SOJ	Release 2	Page 3.9.4-6
FIGURE 3.9.4-3, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN TSOP2	Release 4	Page 3.9.4-7
FIGURE 3.9.4-4, 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ	Release 5	Page 3.9.4-8
FIGURE 3.9.4-5, 1M BY 16 & 18 DRAM WITH 2 CE IN TSOP2	Release 5	Page 3.9.4-9
FIGURE 3.9.4-6, 64K BY 16 DRAM WITH 2 W IN TSOP-2	Release 3	Page 3.9.4-10
FIGURE 3.9.4-7A, 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ	Release 4	Page 3.9.4-11
FIGURE 3.9.4-7B, 256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE	Release 4	Page 3.9.4-12
FIGURE 3.9.4-8, 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP-2	Release 6r7	Page 3.9.4-13
FIGURE 3.9.4-9, 128K AND 256K BY 16 BURST DRAM IN SOJ	Release 6	Page 3.9.4-14
FIGURE 3.9.4-10, 128K AND 256K BY 16 BURST DRAM IN TSOP2	Release 6	Page 3.9.4-15
FIGURE 3.9.4-11, 128K AND 256K BY 16 BURST DRAM IN ZIP	Release 6	Page 3.9.4-16
FIGURE 3.9.4-12, 16M BY 16 DRAM IN TSOP2 PIN ROTATION	Release 6	Page 3.9.4-17
FIGURE 3.9.4-13, 128K AND 256K BY 32 DRAM WITH 4 CAS IN SSOP	Release 8	Page 3.9.4-18
FIGURE 3.9.4-14, 512K AND 2M BY 32 & 36 DRAM IN SOJ AND TSOP2	Release 6r10	Page 3.9.4-19
FIGURE 3.9.4-15, 8M BY 32 DRAM IN TSOP2 PIN ROTATION	Release 9	Page 3.9.4-20
FIGURE 3.9.4-16, 2M BY 32 DRAM IN TSOP2	Release 7	Page 3.9.4-21
FIGURE 3.9.4-17, 256K BY 32 DRAM IN QFP	Release 8	Page 3.9.4-22
FIGURE 3.9.4-18 1M BY 16 DRAM IN USON	Release 9	Page 3.9.4-23
FIGURE 3.9.4-19 4M BY 16 DRAM IN USON	Release 9	Page 3.9.4-24
3.9.5 DRAM Optional Features	Release 1	Page 3.9.5-1
3.9.5.1 - OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM	Release 1	Page 3.9.5-3
3.9.5.2 - 1M DRAM BUILT IN TEST FUNCTION	Release 1	Page 3.9.5-3
3.9.5.3 - ON-CHIP REFRESH CONTROL FOR X8 DRAM	Release 1	Page 3.9.5-3
3.9.5.4 - G BEFORE E REFRESH	Release 1	Page 3.9.5-3
3.9.5.5 - DRAM SPECIAL TEST AND OPERATIONAL MODES	Release 1	Page 3.9.5-3
3.9.5.6 - NON-MULTIPLEXED DRAM OPERATION	Release 1	Page 3.9.5-3
3.9.5.7 - DRAM EXTENDED DATA OUT DEFINITION	Release 6	Page 3.9.5-3

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
3.9.5.8 - 256m DRAM TEST MODE DATA AND ADDRESS COMPRESSION	Release 7	Page 3.9.5-3
3.9.5.9 - PIPELINED NIBBLE MODE DEFINITION	Release 7	Page 3.9.5-3
FIGURE 3.9.5-1A, DRAM ON CHIP REFRESH TIMING	Release 1	Page 3.9.5-5
FIGURE 3.9.5-1B, DRAM SELF REFRESH MODE TIMING	Release 4	Page 3.9.5-5
FIGURE 3.9.5-2, DRAM BIT WRITE TIMING	Release 1	Page 3.9.5-6
DRAM SPECIAL TEST AND OPERATIONAL MODES	Release 4	Page 3.9.5-7
OPTIONAL DRAM OPERATIONAL MODES AND CYCLES	Release 3	Page 3.9.5-11
NON-ADDRESS MULTIPLEXED DRAM OPERATIONAL REQUIREMENTS ..	Release 3	Page 3.9.5-13
DRAM EXTENDED DATA OUT DEFINITION	Release 6	Page 3.9.5-14
256M DRAM ADDRESS AND DATA COMPRESSION DEFINITION	Release 7	Page 3.9.5-15
PIPELINED NIBBLE MODE DEFINITION	Release 7	Page 3.9.5-16
3.10 Multiport Dynamic RAM (MPDRAM)	Release 1	Page 3.10-1
3.10.1 Nibble Wide MPDRAM	Release 1 ...	Page 3.10.1-1
3.10.1.1 - 64K BY 4 MPDRAM IN DIP, SOJ, & ZIP	Release 1 ...	Page 3.10.1-1
3.10.1.2 - 256K BY 4 MPDRAM IN DIP, SOJ, TSOP2, & ZIP	Release 3 ...	Page 3.10.1-1
3.10.1.3 - 256K BY 4 TPD RAM IN SOJ	Release 2 ...	Page 3.10.1-1
FIGURE 3.10.1-1, 64K BY 4 MPDRAM IN DIP & SOJ	Release 1	Page 3.10.1-2
FIGURE 3.10.1-2, 64K BY 4 MPDRAM IN ZIP	Release 1	Page 3.10.1-3
FIGURE 3.10.1-3, 256K BY 4 MPDRAM IN DIP, SOJ, & TSOP2	Release 3	Page 3.10.1-4
FIGURE 3.10.1-4, 256K BY 4 MPDRAM IN ZIP	Release 1	Page 3.10.1-5
FIGURE 3.10.1-5, 256K BY 4 TPD RAM IN SOJ	Release 2	Page 3.10.1-6
3.10.2 Byte Wide MPDRAM	Release 1 ...	Page 3.10.2-1
3.10.2.1 - 128K AND 256K BY 8 MPDRAM IN DIP, SOJ, & TSOP2	Release 3 ...	Page 3.10.2-1
FIGURE 3.10.2-1, 128K AND 256K BY 8 MPDRAM IN DIP & SOJ	Release 2	Page 3.10.2-2
FIGURE 3.10.2-2, 128K BY 8 MPDRAM IN TSOP2	Release 3	Page 3.10.2-3
3.10.3 Word Wide MPDRAM	Release 1 ...	Page 3.10.3-1
3.10.3.1 - 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS	Release 2 ...	Page 3.10.3-1
3.10.3.2 - 128K & 256K BY 16 MPDRAM IN TSOP-2 WITH MULTIPLE CLOCKS	Release 5 ...	Page 3.10.3-1
3.10.3.3 - 256K BY 16 SGRAM IN TSOP2	Release 6 ...	Page 3.10.3-1
3.10.3.4 - 128K, 256K, & 512K BY 32, 2 & 4 Bank SGRAM IN QFP/TQFP	Release 6r9r10 ...	Page 3.10.3-1
3.10.3.5 - 256K BY 32 GRAM IN TSOP-2	Release 6 ...	Page 3.10.3-1
3.10.3.6 - 256K BY 32 SMPDRAM IN TSOP-2	Release 6 ...	Page 3.10.3-2
3.10.3.7 - 256K BY 32 SMPDRAM IN TSOP-2	Release 7 ...	Page 3.10.3-2
3.10.3.8 - 256K BY 32 MPDRAM IN TSOP-2	Release 7 ...	Page 3.10.3-2
3.10.3.9 - 128K, 256K, & 512K BY 32 X 4 BANK SYNCHRONOUS DDR SGRAM IN LQFP	Release 9 ...	Page 3.10.3-2
3.10.3.10 - 4M BY 32 DDR SGRAM (4 BANK) IN FBGA	Release 11 ...	Page 3.10.3-2
3.10.3.11 - 8M BY 32 GDDR3 GRAPHICS RAM IN 144-BALL FBGA	Release 13 ...	Page 3.10.3-2
FIGURE 3.10.3-1, 128K & 256K BY 16 MPDRAM IN SOG with 2 W & 2 CE	Release 3	Page 3.10.3-3
FIGURE 3.10.3-2, 128K & 256K BY 16 MPDRAM IN TSOP-2 with 2 W & 2 CE	Release 5	Page 3.10.3-4
FIGURE 3.10.3-3, 256K BY 16 SGRAM IN TSOP-2	Release 6	Page 3.10.3-5
FIGURE 3.10.3-4, 128K, 256K, & 512K BY 32 SGRAM, 2 & 4 BANK IN QFP/TQFP ..	Release 6c7r9r10 ...	Page 3.10.3-6
FIGURE 3.10.3-5, 256K BY 32 SGRAM IN TSOP-2	Release 6	Page 3.10.3-7
FIGURE 3.10.3-6, 256K BY 32 SYNCH. MPDRAM IN QFP/TQFP	Release 6	Page 3.10.3-8
FIGURE 3.10.3-7, 256K BY 32 MPDRAM IN QFP/TQFP	Release 7	Page 3.10.3-9
FIGURE 3.10.3-8 128K, 256K, & 512K BY 32 X 4 BANK DDR SGRAM IN LQFP	Release 9r10 ...	Page 3.10.3-10
FIGURE 3.10.3-9 4M X 32 (4 BANK) DDR SGRAM IN 144 BALL FBGA	Release 11 ...	Page 3.10.3-11
FIGURE 3.10.3-10 8M X 32 GDDR3 Graphics RAM in 144-Ball FBGA	Release 13 ...	Page 3.10.3-12
3.10.4 MPDRAM Optional Features	Release 1 ...	Page 3.10.4-1
3.10.4.1 - 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE ..	Release 1 ...	Page 3.10.4-3
3.10.4.2 - 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE ..	Release 1 ...	Page 3.10.4-3

Release 14

Section	Release #	Page #
3.10.4.3 - MPDRAM BIT WRITE OPTIONAL FEATURE	Release 1 ...	Page 3.10.4-3
3.10.4.4 - 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE ..	Release 1 ...	Page 3.10.4-3
3.10.4.5 - 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE ..	Release 1 ...	Page 3.10.4-3
3.10.4.6 - 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE	Release 5 ...	Page 3.10.4-3
3.10.4.7 - 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE	Release 5 ...	Page 3.10.4-3
3.10.4.8 - SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM	Release 3 ...	Page 3.10.4-3
3.10.4.9 - PIPELINED FAST PAGE MODE FOR MPDRAM	Release 2 ...	Page 3.10.4-4
3.10.4.10 - EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM ..	Release 2 ...	Page 3.10.4-4
3.10.4.11 - SAM LENGTH DEFINITION FOR 2/4M MPDRAM	Release 5 ...	Page 3.10.4-4
3.10.4.12 - SYNCH GRAM SPECIAL MODE SET PROCEDURE	Release 6 ...	Page 3.10.4-4
3.10.4.13 - SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE	Release 6 ...	Page 3.10.4-4
3.10.4.14 - SYNCH. GRAM OPERATIONAL FUNCTION TRUTH TABLES ..	Release 6 ...	Page 3.10.4-4
3.10.4.15 - 8Mb MPDRAM FEATURE SET FUNCTION TABLE	Release 7 ...	Page 3.10.4-4
3.10.4.16 - EXTENDED FUNCTIONS FOR SGRAM & MPDRAM	Release 6r7 ..	Page 3.10.4-4
TABLE 3.10.4-1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-5
TABLE 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE	Release 1	Page 3.10.4-6
FIGURE 3.10.4-1, BIT WRITE TIMING	Release 1	Page 3.10.4-7
TABLE 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE	Release 5	Page 3.10.4-8
FIGURE 3.10.4-2, SPLIT REGISTER WITH PROGRAMMABLE STOPS	Release 2	Page 3.10.4-9
FIGURE 3.10.4-3A, PIPELINED FAST PAGE MODE	Release 2	Page 3.10.4-10
FIGURE 3.10.4-3B, PIPELINED FAST PAGE MODE	Release 2	Page 3.10.4-11
FIGURE 3.10.4-4, MPDRAM EXTENDED DATA OUT FAST PAGE MODE	Release 4	Page 3.10.4-12
FIGURE 3.10.4-5A & 5B, SAM LENGTH DEFINITION FOR 4M MPDRAM ..	Release 5 ..	Page 3.10.4-13, 14
FIGURE 3.10.4-6, SYNCH GRAM SPECIAL MODE SET PROCEDURE ..	Release 6	Page 3.10.4-15
FIGURE 3.10.4-7, SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE ..	Release 6	Page 3.10.4-16
TABLE 3.10.4-4 A,B, & C, SGRAM FUNCTION TRUTH TABLE	Release 6r7 ..	Page 3.10.4-17-19
TABLE 3.10.4-5, 8Mb BURST MPDRAM FUNCTION TABLE	Release 7	Page 3.10.4-20
EXTENDED FUNCTIONS FOR SGRAM & MPDRAM	Release 7	Page 3.10.4-21
3.11 Synchronous Dynamic Random Access Memory (SDRAM)	Release 4	Page 3.11-1
3.11.1 Bit Wide SDRAM	Release 4 ...	Page 3.11.1-1
FIGURE 3.11.1-1, ...	Release 4	Page 3.11.1-5
3.11.2 Nibble Wide SDRAM	Release 4 ...	Page 3.11.2-1
3.11.2.1 - 4M BY 4 SDRAM IN TSOP2	Release 6r7r8 ..	Page 3.11.2-1
3.11.2.2 - 16M BY 4 SDRAM IN TSOP2	Release 6	Page 3.11.2-1
3.11.2.3 - 64M BY 4 SDRAM IN TSOP2 PIN ROTATION	Release 7r9 ..	Page 3.11.2-1
3.11.2.4 - 16M, 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.2-1
3.11.2.5 - 32M, 64M, 64M, & 256M BY 4 SDRAM IN TSOP2	Release 8r9r10r12	Page 3.11.2-1
3.11.2.6 - 16M BY 4 VIRTUAL CHANNEL SDRAM IN TSOP2	Release 9	Page 3.11.2-1
3.11.2.7 - 16M, 32M, & 64M BY 4 STACKABLE SDR SDRAM IN LSOJ ..	Release 9	Page 3.11.2-2
3.11.2.8 - 16M, 32M, & 64M BY 4 VIRTUAL CHANNEL DDR SDRAM IN TSOP2 ..	Release 9r11 ..	Page 3.11.2-2
3.11.2.9 - 16M, 32M, 64M, & 128M BY 4 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11 ..	Page 3.11.2-2
3.11.2.10 - 16M BY 4 SDR SDRAM IN USON	Release 9	Page 3.11.2-2
3.11.2.11 - 16M, 32M, & 64M BY 4 SDR SDRAM IN TSOP2	Release 9	Page 3.11.2-2
3.11.2.12 - 16M, & 32M BY 4 SDR SDRAM IN LFBGA	Release 9	Page 3.11.2-2
3.11.2.13 - 16M, & 32M BY 4 DDR SDRAM IN LFBGA	Release 9	Page 3.11.2-3
3.11.2.14 - 16M, & 32M BY 4 SDR SDRAM IN LFBGA	Release 9	Page 3.11.2-3
3.11.2.15 - 16M, & 32M BY 4 DDR SDRAM IN LFBGA	Release 9r11 ..	Page 3.11.2-3
3.11.2.16 - 64M, & 128M BY 4 SDR SDRAM IN LFBGA	Release 11a ..	Page 3.11.2-3

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
3.11.2.17 - 16M, 32M, 64M, & 128M BY 4 DDR SDRAM IN LFBGA	Release 11a	Page 3.11.2-3
3.11.2.18 - 16M, 32M, 64M, & 128M BY 4 DDR SDRAM IN FBGA, with Optional Support Balls	Release 12	Page 3.11.2-3
3.11.2.19 - 64M, 128M, 256M, 512M, & 1G BY 4 DDR2 SDRAM IN TFBGA	Release 12r13	Page 3.11.2-4
3.11.2.20 - 16M, 32M, 64M, & 128M BY 4 SDRAM IN sTSOP	Release 12	Page 3.11.2-4
3.11.2.21 - 64M, 128M, 256M, 512M, & 1G BY 4 BY 2 DDR2 SDRAM IN STACKED FBGA	Release 13	Page 3.11.2-4
3.11.2.22 - 64M, 128M, 256M, 512M, & 1G BY 4 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS	Release 13	Page 3.11.2-4
FIGURE 3.11.2-1, 4M X 4 SDRAM IN TSOP2	Release 6r7	Page 3.11.2-5
FIGURE 3.11.2-2, 16M X 4 SDRAM IN TSOP2	Release 6	Page 3.11.2-6
FIGURE 3.11.2-3, 64M X 4 SDRAM IN TSOP2 PIN ROTATION	Release 7r9	Page 3.11.2-7
FIGURE 3.11.2-4, 16M, 32M, 64M, & 128M X 4 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.2-8
FIGURE 3.11.2-5 32M, 64M, & 128M X 4 SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.2-9
FIGURE 3.11.2-6 16M X 4 VC SDRAM IN TSOP2	Release 9	Page 3.11.2-10
FIGURE 3.11.2-7 16M, 32M, & 64M BY 4 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.2-11
FIGURE 3.11.2-8 16M, 32M, & 64M BY 4 VC DDR SDRAM IN TSOP2	Release 9c10r11r12	Page 3.11.2-12
FIGURE 3.11.2-9 16M, 32M, 64M & 128M BY 4 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11r12	Page 3.11.2-13
FIGURE 3.11.2-10 16M BY 4 SDRAM IN USON	Release 9	Page 3.11.2-14
FIGURE 3.11.2-11 16M, 32M, & 64M BY 4 SDR SDRAM IN TSOP2	Release 9r12	Page 3.11.2-15
FIGURE 3.11.2-12 16M & 32M BY 4 SDR SDRAM IN LFBGA	Release 9	Page 3.11.2-16
FIGURE 3.11.2-13 16M & 32M BY 4 DDR SDRAM IN LFBGA	Release 9	Page 3.11.2-17
FIGURE 3.11.2-14 16M, 32M, & 64M BY 4 SDR SDRAM IN LFBGA	Release 9c10	Page 3.11.2-18
FIGURE 3.11.2-15 16M, 32M, & 64M BY 4 DDR SDRAM IN LFBGA	Release 9c10r11	Page 3.11.2-19
FIGURE 3.11.2-16 64M, & 128M BY 4 SDR SDRAM IN FBGA	Release 11a	Page 3.11.2-20
FIGURE 3.11.2-17 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN FBGA	Release 11a	Page 3.11.2-21
FIGURE 3.11.2-18 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN 60-BALL FBGA with Optional Support Balls	Release 12	Page 3.11.2-22
FIGURE 3.11.2-19 64M, 128M, 256M, 512M, & 1G BY 4 DDR2 SDRAM IN 60-BALL TF-FBGA	Release 12r13	Page 3.11.2-23
FIGURE 3.11.2-20 16M, 32M, 64M, & 128M X 4 SDRAM IN sTSOP	Release 12	Page 3.11.2-24
FIGURE 3.11.2-21 64M, 128M, 256M, 512M, & 1G BY 4 X 2 DDR2 SDRAM IN 60-BALL Stacked FBGA	Release 13	Page 3.11.2-25
FIGURE 3.11.2-22 64M, 128M, 256M, 512M, & 1G BY 4 X 2 DDR2 SDRAM For 60-Ball Stacked FBGA Requiring Support Balls	Release 13	Page 3.11.2-26
3.11.3 BYTE WIDE SDRAM	Release 4	Page 3.11.3-1
3.11.3.1 - 2M BY 8 or 9 SDRAM IN TSOP2	Release 6r7	Page 3.11.3-1
3.11.3.2 - 8M BY 8 SDRAM IN TSOP2	Release 6	Page 3.11.3-1
3.11.3.3 - 32M BY 8 SDRAM PIN ROTATION	Release 7r9	Page 3.11.3-1
3.11.3.4 - 8M, 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN TSOP2	Release 8r9r10r11r12	Page 3.11.3-1
3.11.3.5 - 16M, 32M, 64M, & 128M BY 8 SDRAM IN TSOP2	Release 8r9r10r12	Page 3.11.3-1
3.11.3.6 - 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2	Release 9	Page 3.11.3-1
3.11.3.7 - 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.3-2
3.11.3.8 - 8M, 16M, 32M, & 64M BY 8 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11	Page 3.11.3-2
3.11.3.9 - 2M BY 8 SDR SDRAM IN USON	Release 9	Page 3.11.3-2
3.11.3.10 - 8M BY 8 SDR SDRAM IN USON	Release 9	Page 3.11.3-2
3.11.3.11 - 8M BY 8 VIRTUAL CHANNEL SDRAM IN TSOP2	Release 9	Page 3.11.3-2
3.11.3.12 - 8M, 16M, & 32M BY 8 VIRTUAL CHANNEL DDR SDRAM IN TSOP2	Release 9r11	Page 3.11.3-2
3.11.3.13 - 8M, & 16M BY 8 SDR SDRAM IN LFBGA	Release 9	Page 3.11.3-3
3.11.3.14 - 8M, & 16M BY 8 DDR SDRAM IN LFBGA	Release 9	Page 3.11.3-3
3.11.3.15 - 8M, & 16M BY 8 SDR SDRAM IN LFBGA	Release 9	Page 3.11.3-3
3.11.3.16 - 8M, 16M, 32M, & 64M BY 8 DDR SDRAM IN LFBGA	Release 9r11	Page 3.11.3-3

Release 14

Section	Release #	Page #
3.11.3.17 - 16M, 32M, & 64M BY 8 Low Power SDR SDRAM IN FBGA ..	Release 11a	Page 3.11.3-3
3.11.3.18 - 32M, & 64M BY 8 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.3-3
3.11.3.19 - 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN FBGA	Release 11a	Page 3.11.3-4
3.11.3.20 - 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN 60 Ball FBGA, with Optional Support Balls	Release 12	Page 3.11.3-4
3.11.3.21 - 32M, 64M, 128M, 256M, & 512M BY 8 DDR2 SDRAM IN 60 Ball TFBGA ..	Release 12r13	Page 3.11.3-4
3.11.3.22 - 8M, 16M, 32M, & 64M BY 8 SDRAM IN sTSOP	Release 12	Page 3.11.3-4
3.11.3.23 - 32M, 64M, 128M, 256M, & 512M BY 8 BY 2 DDR2 SDRAM IN STACKED FBGA	Release 13	Page 3.11.3-4
3.11.3.24 - 32M, 64M, 128M, 256M, & 512M BY 8 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS	Release 13	Page 3.11.3-4
FIGURE 3.11.3-1, 2M BY 8 OR 9 SDRAM IN TSOP2	Release 6r7	Page 3.11.3-5
FIGURE 3.11.3-2, 8M BY 8 SDRAM IN TSOP2	Release 6	Page 3.11.3-6
FIGURE 3.11.3-3, 32M BY 8 SDRAM IN TSOP2 PIN ROTATION	Release 7r9	Page 3.11.3-7
FIGURE 3.11.3-4, 8M, 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN TSOP2 ..	Release 8r9r10r11r12	Page 3.11.3-8
FIGURE 3.11.3-5, 16M, 32M, 64M, & 128M BY 8 SDRAM IN TSOP2	Release 8r9r10r12	Page 3.11.3-9
FIGURE 3.11.3-6 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2	Release 9	Page 3.11.3-10
FIGURE 3.11.3-7 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ	Release 9	Page 3.11.3-11
FIGURE 3.11.3-8 8M, 16M, 32M, 64M & 128M BY 8 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11r12	Page 3.11.3-12
FIGURE 3.9.3-9 2M BY 8 SDRAM IN USON	Release 9	Page 3.11.3-13
FIGURE 3.11.3-10 8M BY 8 SDRAM IN USON	Release 9	Page 3.11.3-14
FIGURE 3.11.3-11 8M X 8 VC SDRAM IN TSOP2	Release 9	Page 3.11.3-15
FIGURE 3.11.3-12 8M, 16M, & 32M BY 8 VC DDR SDRAM IN TSOP2	Release 9c10r11	Page 3.11.3-16
FIGURE 3.11.3-13 8M & 16M BY 8 SDR SDRAM IN LFBGA	Release 9	Page 3.11.3-17
FIGURE 3.11.3-14 8M & 16M BY 8 DDR SDRAM IN LFBGA	Release 9	Page 3.11.3-18
FIGURE 3.11.3-15 8M, 16M, & 32M BY 8 SDR SDRAM IN LFBGA	Release 9c10	Page 3.11.3-19
FIGURE 3.11.3-16 8M, 16M, 32M & 64M BY 8 DDR SDRAM IN LFBGA	Release 9c10r11	Page 3.11.3-20
FIGURE 3.11.3-17 16M, 32M & 64M BY 8 SDR SDRAM IN FBGA	Release 11a	Page 3.11.3-21
FIGURE 3.11.3-18 32M & 64M BY 8 SDR SDRAM IN FBGA	Release 11a	Page 3.11.3-22
FIGURE 3.11.3-19 16M, 32M, 64M & 128M BY 8 DDR SDRAM IN FBGA	Release 11a	Page 3.11.3-23
FIGURE 3.11.3-20 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN 60-BALL FBGA with Optional Support Balls	Release 12	Page 3.11.3-24
FIGURE 3.11.3-21 32M, 64M, 128M, 256M, & 512M BY 8 DDR2 SDRAM IN 60-BALL TF-FBGA	Release 12r13	Page 3.11.3-25
FIGURE 3.11.3-22 8M, 16M, 32M, & 64M X 8 SDRAM IN sTSOP	Release 12	Page 3.11.3-26
FIGURE 3.11.3-23 32M, 64M, 256M, 128M, & 512M BY 8 X 2 DDR2 SDRAM IN 60-BALL Stacked FBGA	Release 13	Page 3.11.3-27
FIGURE 3.11.3-24 32M, 64M, 128M, 256M, & 512M BY 8 X 2 DDR2 SDRAM For 60-Ball Stacked FBGA Requiring Support Balls	Release 13	Page 3.11.3-28
3.11.4 WORD WIDE SDRAM	Release 5	Page 3.11.4-1
3.11.4.1 - 256K BY 16 AND 1M BY 16/18 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-1
3.11.4.2 - 2M & 4M BY 16 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-1
3.11.4.3 - 16M BY 16 SDRAM IN TSOP-2 PIN ROTATION	Release 6r9	Page 3.11.4-1
3.11.4.4 - 128K, 256K, & 512K, 2 & 4 Bank BY 32 SDRAM IN QFP/TQFP/LQFP ..	Release 6r7r9r10	Page 3.11.4-1
3.11.4.5 - 2M BY 32 SDRAM IN TSOP-2	Release 6r7r10	Page 3.11.4-1
3.11.4.6 - 8M BY 32 SDRAM IN TSOP-2 PIN ROTATION	Release 6r9	Page 3.11.4-2
3.11.4.7 - 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP-2	Release 7r8r10r11ar12	Page 3.11.4-2
3.11.4.8 - 4M, 8M, 16M, 32M, & 64M BY 16, DDR SDRAM IN TSOP-2	Release 8r9r10r11r12	Page 3.11.4-2
3.11.4.9 - 8M, 16M, 32M, & 64M BY 16, SDRAM IN TSOP-2	Release 8r9r10r12	Page 3.11.4-2
3.11.4.10 - 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2	Release 9	Page 3.11.4-2
3.11.4.11 - 4M, 8M, & 16M BY 16 STACKABLE SDR SDRAM IN LSOJ ...	Release 9	Page 3.11.4-2
3.11.4.12 - 4M, 8M, 16M, 32M, & 64M BY 16 STACKABLE DDR SDRAM IN LSOJ ..	Release 9r11r12	Page 3.11.4-3

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
3.11.4.13 - 4M BY 16 SDR SDRAM IN USON	Release 9	Page 3.11.4-3
3.11.4.14 - 4M BY 16 VIRTUAL CHANNEL SDRAM IN TSOP2	Release 9	Page 3.11.4-3
3.11.4.15 - 4M, 8M, & 16M BY 16 VIRTUAL CHANNEL DDR SDRAM IN TSOP2	Release 9r11	Page 3.11.4-3
3.11.4.16 - 4M, & 8M BY 16 SDR SDRAM IN LFBGA	Release 9r12	Page 3.11.4-3
3.11.4.17 - 4M, & 8M BY 16 DDR SDRAM IN LFBGA	Release 9	Page 3.11.4-3
3.11.4.18 - 4M, & 8M BY 16 SDR SDRAM IN LFBGA	Release 9	Page 3.11.4-4
3.11.4.19 - 4M, & 8M BY 16 DDR SDRAM IN LFBGA	Release 9r11	Page 3.11.4-4
3.11.4.20 - 4M BY 16/18 SLDRAM IN TSOP2	Release 9	Page 3.11.4-4
3.11.4.21 - 4M TO 64M BY 16/18 SLDRAM IN R-PZIP	Release 9	Page 3.11.4-4
3.11.4.22 - 128K, 256K, & 512K BY 32, 4 BANK DDR SDRAM IN LQFP	Release 9r10r11	Page 3.11.4-4
3.11.4.23 - 2M & 4M BY 32, 4 BANK, DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-4
3.11.4.24 - 8M, 16M, 32M, & 64M BY 16, Low Power SDR SDRAM IN FBGA	Release 11a	Page 3.11.4-5
3.11.4.25 - 16M, & 32M BY 16 SDR SDRAM IN FBGA	Release 11a	Page 3.11.4-5
3.11.4.26 - 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-5
3.11.4.27 - 2M & 4M BY 32 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.4-5
3.11.4.28 - 2M, 4M, 8M, & 16M BY 32, Low Power SDR SDRAM IN FBGA	Release 11a12r13	Page 3.11.4-5
3.11.4.29 - 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA with Optional Support Balls	Release 12	Page 3.11.4-5
3.11.4.30 - 16M, 32M, 64M, 128M, & 256M BY 16 DDR2 SDRAM IN TFBGA	Release 12r13	Page 3.11.4-6
3.11.4.31 - 4M, 8M, 16M, & 32M BY 16 SDRAM IN sTSOP	Release 12	Page 3.11.4-6
3.11.4.32 - 16M, 32M, 64M, 128M, & 256M BY 16 BY 2 DDR2 SDRAM IN STACKED FBGA	Release 13	Page 3.11.4-6
3.11.4.33 - 16M, 32M, 64M, 128M, & 256M BY 16 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS	Release 13	Page 3.11.4-6
3.11.4.34 - 4M BY 32 DDR2 SDRAM IN 144-BALL LF-XBGA	Release 13	Page 3.11.4-6
3.11.4.35 - 8M BY 16 DDR SDRAM in 78-Ball BGA	Release 14	Page 3.11.4-7
3.11.4.36 - 8M, 16M, & 32M BY 32 Low Power DDR SDRAM IN 90-BALL FBGA	Release 14	Page 3.11.4-7
FIGURE 3.11.4-1, 256 BY 16 AND 1M BY 16/18 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-8
FIGURE 3.11.4-2, 4M BY 16 SDRAM IN TSOP-2	Release 6r7	Page 3.11.4-9
FIGURE 3.11.4-3, 16M BY 16 SDRAM IN TSOP-2	Release 6c7r9	Page 3.11.4-10
FIGURE 3.11.4-4, 128K, 256K, & 512K BY 32 SDRAM IN QFP/TQFP	Release 6c7r9r10	Page 3.11.4-11
FIGURE 3.11.4-5, 2M BY 32 SDRAM IN TSOP-2	Release 6r7r10	Page 3.11.4-12
FIGURE 3.11.4-6, 8M BY 32 SDRAM IN TSOP-2 PIN ROTATION	Release 6c7r9	Page 3.11.4-13
FIGURE 3.11.4-7, 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP-2	Release 7r8r10r12	Page 3.11.4-14
FIGURE 3.11.4-8, 4M, 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN TSOP-2	Release 8r9r10r11r12	Page 3.11.4-15
FIGURE 3.11.4-9, 8M, 16M, 32M, & 64M BY 16 SDRAM IN TSOP-2	Release 8r9r10r12	Page 3.11.4-16
FIGURE 3.11.4-10 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2	Release 9	Page 3.11.4-17
FIGURE 3.11.4-11 4M, 8M, & 16M BY 16 SDR STACKABLE SDRAM IN LSOJ	Release 9	Page 3.11.4-18
FIGURE 3.11.4-12 4M, 8M, 16M, & 32M BY 16 STACKABLE DDR SDRAM IN LSOJ	Release 9r10r11r12	Page 3.11.4-19
FIGURE 3.11.4-13 4M BY 16 SDRAM IN USON	Release 9	Page 3.11.4-20
FIGURE 3.11.4-14 4M X 16 VC SDRAM IN TSOP2	Release 9	Page 3.11.4-21
FIGURE 3.11.4-15 4M, 8M, & 16M BY 16 VC DDR SDRAM IN TSOP2	Release 9c10r11	Page 3.11.4-22
FIGURE 3.11.4-16 4M & 16M BY 16 SDR SDRAM IN LFBGA	Release 9r12	Page 3.11.4-23
FIGURE 3.11.4-17 4M & 16M BY 16 DDR SDRAM IN LFBGA	Release 9	Page 3.11.4-24
FIGURE 3.11.4-18 4M, 8M, & 16M BY 16 SDR SDRAM IN LFBGA	Release 9c10	Page 3.11.4-25
FIGURE 3.11.4-19 8M, 16M, & 32M BY 16 DDR SDRAM IN LFBGA	Release 9c10r11	Page 3.11.4-26
FIGURE 3.11.4-20 4M TO 64M BY 16 & 18 SLDRAM IN R-PZIP	Release 9	Page 3.11.4-27
FIGURE 3.10.4-21 4M BY 16/18 SLRAM IN TSOP2	Release 9	Page 3.11.4-28
FIGURE 3.11.4-22 128K, 256K, & 512K X 32 X 4 BANK DDR SDRAM IN QFP	Release 9r10r11	Page 3.11.4-29
FIGURE 3.11.4-23 2M, 4M & 8M BY 32 DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-30
FIGURE 3.11.4-24 8M, 16M, 32M & 64M BY 16 SDR SDRAM IN FBGA	Release 11a12	Page 3.11.4-31

Release 14

Section	Release #	Page #
FIGURE 3.11.4-25 16M & 32M BY 16 SDR SDRAM IN FBGA	Release 11a	Page 3.11.4-32
FIGURE 3.11.4-26 8M, 16M, 32M & 64M BY 16 DDR SDRAM IN FBGA	Release 11a	Page 3.11.4-33
FIGURE 3.11.4-27 2M & 4M BY 32 SDR SDRAM IN LFBGA	Release 11a	Page 3.11.4-34
FIGURE 3.11.4-28 2M, 4M 8M, & 16M BY 32, Low Power SDR SDRAM IN LFBGA	Release 11a12r13	Page 3.11.4-35
FIGURE 3.11.4-29 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN 60-BALL FBGA with Optional Support Balls	Release 12	Page 3.11.4-36
FIGURE 3.11.4-30 16M, 32M, 64M, 128M, & 256M BY 16 DDR2 SDRAM IN 60-BALL TFBGA	Release 12r13	Page 3.11.4-37
FIGURE 3.11.4-31 4M, 8M, 16M, & 32M X 16 SDRAM IN sTSOP	Release 12	Page 3.11.4-38
FIGURE 3.11.4-32 16M, 32M, 64M, 128M, & 256M BY 16 X 2 DDR2 SDRAM InStacked FBGA	Release 13	Page 3.11.4-39
FIGURE 3.11.4-33 16M, 32M, 64M, 128M, & 256M BY 16 X 2 DDR2 SDRAM For Stacked FBGA Packages Requiring Support Balls	Release 13	Page 3.11.4-40
FIGURE 3.11.4-34 4M x 32M DDR2 SDRAM in 144-Ball LF-XBGA	Release 13	Page 3.11.4-41
FIGURE 3.11.4-35 8M x 16 DDR SDRAM in 78-Ball TF-BGA	Release 14	Page 3.11.4-42
FIGURE 3.11.4-36 8M, 16M, & 32M x 32 Low Power DDR SDRAM in 90-Ball FBGA ..	Release 14	Page 3.11.4-43
3.11.5 SDRAM Architectural and Operational Features		
See P 3.11.5-1 for detailed Table of Contents	Release 4-9r12	Page 3.11.5-1
3.11.5.1 - General SDRAM Functions	Rel.4r9r12r13	Page 3.11.5.1-1
3.11.5.2 - DDR Specific SDRAM Functions	Release 9r12	Page 3.11.5.2-1
3.11.5.3 - ESDRAM Specific SDRAM Functions	Release 9	Page 3.11.5.3-1
3.11.5.4 - VCSDRAM Specific SDRAM Functions	Release 9	Page 3.11.5.4-1
3.11.5.5 - DDR2 Specific SDRAM Functions	Release 13	Page 3.11.5.5-1
3.11.5.6 - GDDR2 Specific SDRAM Functions	Release 13	Page 3.11.5.6-1
3.11.5.7 - GDDR3 Specific SDRAM Functions	Release 14	Page 3.11.5.7-1
3.11.6 - SDRAM Parametric Specifications	Release 9	Page 3.11.6-1
3.11.6.1 - DDR SDRAM/SGRAM I/O Voltage	Release 9	Page 3.11.6-3
3.11.6.2 - 256M SDRAM/SGRAM REFRESH SPECIFICATION	Release 9	Page 3.11.6-3
3.11.6.3-16MB & 64MB TIMING SPECIFICATIONS (LVTTTL)	Release 8	Pages 3.11.6-4⇒6
3.11.6.4 - STANDARD FOR DOUBLE DATA RATE (DDR) SDRAM/SGRAM INPUT INTERFACE SPECIFICATIONS	Release 9	Pages 3.11.6-7
3.11.6.5 - DDR SDRAM Self-Refresh Exit Timing	Release 9	Pages 3.11.6-8
3.11.6.6 - AC TIMING PARAMETERS FOR DDR SDRAMs/SGRAMs ...	Release 9	Pages 3.11.6-9⇒19
3.20. MEMORY DEVICE COMPLETE SPECIFICATION APPENDIX	Release 11	Page 3.20-1
3.20.1 - DDR SDRAM Device Specification	Release 11	Page 3.20-1
3.20.2 - DDR2 SDRAM Device Specification	Release 11r12	Page 3.20-1
4. MULTI-CHIP MEMORY MODULES & CARDS	Release 7r11	Page 4-1
4.1. Memory Module Nomenclature and General Features	Release 7r11r13	Page 4.1-1
4.1.1 Memory Module Nomenclature	Release 1-7	Page 4.1-1
4.1.2 Serial Presence Detect General Standard	Release 1-7r9	Page 4.1.2-1
4.1.2.1 SPD Appendix A, Table of Fundamental Memory Types	Release 8r9r12	Page 4.1.2.1-1
4.1.2.2 SPD Appendix B, Table of Superset Memory Types	Release 7r9r11	Page 4.1.2.2-1
4.1.2.3 SPD Appendix C, Specific PDs for FP and EDO DRAM	Release 7	Page 4.1.2.3-1
4.1.2.4 SPD Appendix D, Specific PDs for DDR SDRAM (Rev. 1.0)	Rel.7r11r12r13	Page 4.1.2.4-1
4.1.2.5 SPD Appendix E, Specific PDs for SDR SDRAM	Release 7r8 ₂ c9r11r12	Page 4.1.2.5-1
4.1.2.6 SPD Appendix F, Specific PDs for Addr. MX ROM	Release 7	Page 4.1.2.6-1
4.1.2.7 SPD Appendix G, Not yet assigned	Release 9	Page 4.1.2.7-1
4.1.2.8 SPD Appendix H, Table of ESDRAM Attributes	Release 9	Page 4.1.2.8-1
4.1.2.9 SPD Appendix V, Specific PDs for VCSDRAM	Release 9	Page 4.1.2.9-1

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
4.1.2.10 SPD Appendix X, Specific SPDs for DDR2 SDRAM (Rev. 1.2)	Release 13r14	Page 4.1.2.10-1
4.2. One BYTE Modules	Release 7	Page 4.2-1
4.2.1 - 22 PIN SIP/SIMM 4 bit DRAM MODULE	Release 1-7	Page 4.2-1
4.2.2 - 24 PIN SIP/SIMM 4 bit DRAM MODULE	Release 1-7	Page 4.2-1
4.2.3 - 30 PIN SIP/SIMM 8 or 9 bit DRAM MODULE	Release 4-7	Page 4.2-1
4.2.4 - 30 PIN SIP/SIMM 1, 2, 4, 5, or 8 bits DRAM MODULE FAMILY	Release 1-7	Page 4.2-1
4.2.5 - 23/25/26/28 PIN ZIP/SIMM 1 or 4 bit DRAM MODULE FAMILY	Release 1-7	Page 4.2-2
4.2.6 - 60 PIN ZIP/SIMM 4 bit SRAM MODULE	Release 1-7	Page 4.2-2
4.2.7 - 70 PIN ZIP/SIMM 9 bit SRAM MODULE	Release 1-7	Page 4.2-2
FIGURE 4.2-1, 22, 24, & 30 PIN DRAM MODULES	Release 4-7	Page 4.2-3
FIGURE 4.2-2, 30 PIN DRAM MODULE FAMILY	Release 1-7	Page 4.2-4
FIGURE 4.2-3, 23/25/26/28 PIN DRAM MODULE FAMILY	Release 1-7	Page 4.2-5
FIGURE 4.2-4, 2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY	Release 1-7	Page 4.2-6
FIGURE 4.2-5, 64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY	Release 1-7	Page 4.2-7
4.3. Two BYTE Modules and Cards	Release 7	Page 4.3-1
4.3.1 - 76 PIN ZIP/SIMM 9 or 18 bit SRAM MODULE	Release 1-7	Page 4.3-1
4.3.2 - 40 PIN SIP/SIMM 1, 2, 4, 5, 8, 9, 16, or 18 DRAM MOD FAMILY	Release 1-7	Page 4.3-1
4.3.3 - 60 PIN DRAM 16 or 18 bit CARD FAMILY	Release 2-7	Page 4.3-1
4.3.4 - 68 PIN MULTIPLE TECHNOGY MEMORY 16 bit CARD FAMILY	Release 3-7	Page 4.3-1
FIGURE 4.3-1, 2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY	Release 1-7	Page 4.3-3
FIGURE 4.3-2, 40 PIN DRAM MODULE FAMILY	Release 1-7	Page 4.3-4
FIGURE 4.3-3A, 60 PIN DRAM CARD FAMILY PIN CONNECTIONS	Release 2-7	Page 4.3-5
FIGURE 4.3-3B, 60 PIN CARD FAMILY BLOCK DIAGRAMS	Release 2-7	Page 4.3-6
FIGURE 4.3-4A, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY	Release 3-7	Page 4.3-7
FIGURE 4.3-4B, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TRUTH TABLES	Release 3-7	Page 4.3-8
4.4. Four BYTE Modules and Cards	Release 7	Page 4.4-1
4.4.1 - 64 & 72 PIN ZIP/SIMM 32 bit SRAM MODULE	Release 6-7	Page 4.4.1-1
FIGURE 4.4.1-1, 16K TO 4M BY 32, 64 & 72 PIN SRAM MODULE FAMILY	Release 6-7	Page 4.4.1-2
4.4.2 - 72 PIN SIMM 32 or 36 bit DRAM MODULE FAMILY	Release 6-7	Page 4.4.2-1
- 72 PIN SIMM 36 or 39 DRAM ECC MODULE FAMILY	Release 6-7	Page 4.4.2-1
FIGURE 4.4.2-2 A, 256K TO 256M BY 36, 72 PIN DRAM MODULE PINOUT	Release 6-7c8	Page 4.4.2-3
FIGURE 4.4.2-2 B⇒K, 72 PIN 36 BIT DRAM SIMM BLOCK DIAGRAMS	Release 6-7	Page 4.4.2-4⇒13
FIGURE 4.4.2-3 A, 256K TO 256M BY 32, 36, & 40 BIT 72 PIN DRAM MODULE	Release 6-7	Page 4.4.2-14
FIGURE 4.4.2-3 B⇒C 72 PIN 32, 36, & 40 BIT DRAM SIMM BLOCK DIAGRAMS	Release 6-7	Page 4.4.2-15⇒16
4.4.3 - 88 PIN, 32/36/39 bit DRAM CARD FAMILY	Release 6-7	Page 4.4-1
FIGURE 4.4.3-1 A, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY	Release 6-7	Page 4.4.3-3
FIGURE 4.4.3-1 B, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY CONFIGURATION TABLES	Release 6-7	Page 4.4.3-4
FIGURE 4.4.3-1 C, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-5
FIGURE 4.4.3-1 D, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-6
FIGURE 4.4.3-1 E, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-7
FIGURE 4.4.3-1 F, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG.	Release 6-7	Page 4.4.3-8
- 88 PIN, 40 bit DRAM CARD FAMILY	Release 4-7	Page 4.4.3-1
FIGURE 4.4.3-2 A, 256K TO 128M BY 40 DRAM CARD	Release 4-7	Page 4.4.3-9
FIGURE 4.4.3-2 B, 256K TO 128M BY 40 DRAM CARD PD TRUTH TABLE	Release 4-7	Page 4.4.3-10
FIGURE 4.4.3-2 C, 256K TO 64M BY 40 DRAM CARD USING BY 4 DEVICES	Release 4-7	Page 4.4.3-11
FIGURE 4.4.3-2 D, 512K TO 128M BY 40 DRAM CARD USING BY 4 DEVICES	Release 4-7	Page 4.4.3-12

Release 14

Section	Release #	Page #
FIGURE 4.4.3-2 E, 512K TO 32M BY 40 DRAM CARD USING BY 8 DEVICES	Release 4-7	Page 4.4.3-13
FIGURE 4.4.3-2 F, 1M TO 64M BY 40 DRAM CARD USING BY 8 DEVICES	Release 4-7	Page 4.4.3-14
4.4.4 - 72 PIN 32 or 36 bit DRAM SO-DIMM FAMILY	Release 5-7	Page 4.4.4-1
FIGURE 4.4.4-A 32 & 36 BIT 72 PIN DRAM SO-DIMM PINOUT, PRESENCE DETECT & CONFIGURATION TABLES	Release 6-7	Page 4.4.4-1
FIGURE 4.4.4-B-D 32 & 36 BIT DRAM SO-DIMM BLOCK DIAGRAMS	Release 5-7	Page 4.4.4-2⇒5
4.4.5 - 88 PIN 32 or 36 bit DRAM SO-DIMM FAMILY	Release 5-7	Page 4.4.5-1
FIGURE 4.4.5-A, 88 PIN 32 & 36 BIT DRAM SO-DIMM PINOUT	Release 6-7	Page 4.4.5-2
FIGURE 4.4.5-B, 88 PIN 32 & 36 BIT DRAM SO-DIMM PD TRUTH TABLES	Release 6-7	Page 4.4.5-3
FIGURE 4.4.5-C⇒F, 88 PIN 32 & 36 BIT DRAM SO-DIMM BLOCK DIAGRAMS	Release 6-7	Page 4.4.5-4⇒7
4.4.6 - 112 PIN 32 bits MPDRAM SO-DIMM FAMILY	Release 5-7	Page 4.4.6-1
FIGURE 4.4.6-A, 112 PIN 32 BIT MPDRAM DIMM PINOUT	Release 6-7	Page 4.4.6-2
FIGURE 4.4.6-B, C, 112 PIN 32 BIT MPDRAM DIMM PD TRUTH TABLES AND BLOCK DIAGRAMS	Release 6-7	Page 4.4.6-3, 4
4.4.7 - 80 PIN 32 bit EEPROM SIMM FAMILY	Release 4-7c8	Page 4.4.7-1
FIGURE 4.4.7-A, 128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES	Release 4-7	Page 4.4.7-3
FIGURE 4.4.7-B, 128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM	Release 4-7	Page 4.4.7-4
4.4.8 - 100 PIN 32, 36, or 40 BIT DRAM, SDRAM, ROM DIMM FAMILY	Release 7	Page 4.4.8-1
FIGURE 4.4.8-B & C, 32, 36, or 40 bit 100 PIN MODULE PINOUT	Release 7c8	Page 4.4.8-3, 4
FIGURE 4.4.8-D, 32, 36, or 40 bit 100 PIN MODULE PIN COMPARISON	Release 7	Page 4.4.8-5
FIGURE 4.4.8-E, 32, 36, or 40 bit 100 PIN MODULE CLOCK WIRING	Release 7c8	Page 4.4.8-6
FIGURE 4.4.8-F⇒AE, 32, 36, or 40 bit 100 PIN MODULE BLOCK DIAGRAMS	Release 7c8	Page 4.4.8-7⇒32
4.5. Eight BYTE Modules and Cards	Release 7r8r9r12	Page 4.5-1
4.5.1 - 168 PIN Buffered DRAM, 64, 72, or 80 Bit DIMM FAMILY	Release 6-7	Page 4.5.1-1
FIGURE 4.5.1-A-B, 64, 72, or 80 BIT SIMM PINOUT, TOP & BOTTOM HALVES	Release 4-7r9	Page 4.5.1-2,3
FIGURE 4.5.1-C, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 6-7	Page 4.5.1-4
FIGURE 4.5.1-D, 64, 72, & 80 BIT DRAM SIMM Capacity Table	Release 4-7	Page 4.5.1-5
FIGURE 4.5.1-E-AB, 64, 72, & 80 BIT CONFIGURATION BLOCK DIAGRAMS	Release 4-c7c8	Page 4.5.1-6-29
4.5.2 - 200 PIN SDRAM, 64, 72, or 80 DIMM FAMILY	Release 5-7c8c9r11	Page 4.5.2-1
FIGURE 4.5.2-A, B, 8 -BYTE SDRAM DIMM PINOUT	Release 5-7r8r11	Page 4.5.2-3,4
FIGURE 4.5.2-C, 8-BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7	Page 4.5.2-5
FIGURE 4.5.2-D, E, 8-BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.2-6
FIGURE 4.5.2-F-M, 8-BYTE SDRAM DIMM BLOCK DIAGRAMS	Release 5-7	Page 4.5.2-7,14
4.5.3 - 168 PIN Unbuffered DRAM, 64, 72, or 80 DIMM FAMILY with SPD	Release 5-7	Page 4.5.3-1
FIGURE 4.5.3-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 5-7r9	Page 4.5.3-2,3
FIGURE 4.5.3-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.3-5
FIGURE 4.5.3-E, Pinout comparison, 168P DRAM & SDRAM	Release 5-7c8	Page 4.5.3-6
FIGURE 4.5.3-F, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7r8-1	Page 4.5.3-7
FIGURE 4.5.3-G-U, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5-7r8	Page 4.5.3-8,20
4.5.4 - 168 PIN Unbuffered SDRAM, 64, 72, or 80 DIMM FAMILY with SPD	Release 5-7c8	Page 4.5.4-1
FIGURE 4.5.4-A, B, 8 -BYTE SDRAM DIMM PINOUT	Release 5-7r9	Page 4.5.4-2,3
FIGURE 4.5.4-C, 8-BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7r8	Page 4.5.4-4
FIGURE 4.5.4-E, 8-BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7r8	Page 4.5.4-6
FIGURE 4.5.4-I-AK, 8-BYTE SDRAM DIMM BLOCK DIAGRAMS	Release 5-7r8r9	Page 4.5.4-10⇒38
4.5.5 - 144 PIN Unbuffered DRAM, 64, or 72, SO-DIMM FAMILY with SPD	Release 5-7r8	Page 4.5.5-1
FIGURE 4.5.5-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 5-7r9	Page 4.5.5-2,3

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
FIGURE 4.5.5-C, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.5-4
FIGURE 4.5.5-E, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7	Page 4.5.5-6
FIGURE 4.5.5-F-AB, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5-7r8	Page 4.5.5-7⇒16
4.5.6 - 144 PIN Unbuffered SDRAM, 64, or 72 SO-DIMM FAMILY with SPD	Release 5-7	Page 4.5.6-1
FIGURE 4.5.6-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 5-7r9	Page 4.5.6-2,3
FIGURE 4.5.6-C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 5-7	Page 4.5.6-6
FIGURE 4.5.6-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 5-7	Page 4.5.6-4
FIGURE 4.5.6-G-P, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 5-7	Page 4.5.6-7⇒17
4.5.7 - 168 PIN Registered SDRAM, 64, 72 or 80 DIMM FAMILY with SPD	Release 8r11	Page 4.5.7-1
FIGURE 4.5.7-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 8r9	Page 4.5.7-2,3
FIGURE 4.5.7-C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 8	Page 4.5.7-4
FIGURE 4.5.7-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS	Release 8	Page 4.5.7-5
FIGURE 4.5.7-I-X, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 8c9r10r11	Page 4.5.7-9⇒24
4.5.8 - 144 PIN SGRAMSDRAM, 32 & 64 SO-DIMM FAMILY with SPD	Release 8r10	Page 4.5.8-1
FIGURE 4.5.8-A, B, 8 -BYTE DRAM DIMM PINOUT	Release 8r9r10	Page 4.5.8-2,3
FIGURE 4.5.8-C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 8	Page 4.5.8-4
FIGURE 4.5.8-D-F, 8-BYTE DRAM DIMM LAYOUT CONSIDERATIONS	Release 8	Page 4.5.8-5⇒9
FIGURE 4.5.8-G-J, 8-BYTE DRAM DIMM BLOCK DIAGRAMS	Release 8r10	Page 4.5.8-10⇒13
4.5.9 - 144 PIN SGRAM SO-DIMM FAMILY	Release 9	Page 4.5.9-1
FIGS. 4.5.9-A & B, PIN ASSIGNMENTS	Release 9	Page 4.5.9-2,3
FIGURE 4.5.9-C, CLOCK NET ROUTING	Release 9	Page 4.5.9-6
FIGURE 4.5.9-D TO G, BLOCK DIAGRAMS	Release 9	Page 4.5.9-7⇒10
4.5.10 - 184 PIN UNBUFFERED DDR SDRAM DIMM FAMILY	Release 9	Page 4.5.10-1
FIGURES. 4.5.10-A, & B, PIN ASSIGNMENTS	Release 9r12	Page 4.5.10-2,3
FIGURES. 4.5.10-C, SUMMARY OF FEATURES AND PIN DESCRIPTION	Release 9	Page 4.5.10-4
FIGURE 4.5.10-D, SPD TABLE & INFORMATION	Release 9	Page 4.5.10-5
FIGURE 4.5.10-E, COMPARISON OF 184 PIN UNBUFFERED SDR SDRAM & DDR SDRAM DIMM--	Release 9	Page 4.5.10-6
FIGURE 4.5.10-F, KEYING METHODOLOGY	Release 9	Page 4.5.10-7
FIGURE 4.5.10-G & H, VDDID DEFINITION	Release 9	Page 4.5.10-8 & 9
FIGURES 4.5.10-I through P, CONFIGURATION BLOCK DIAGRAM--	Release 9	Page 4.5.10-10⇒17
4.5.11 - 184 PIN UNBUFFERED SDR SDRAM DIMM FAMILY	Release 10	Page 4.5.11-1
FIGURES. 4.5.11-A, & B, PIN ASSIGNMENTS	Release 10	Page 4.5.11-2,3
FIGURES. 4.5.11-C, SUMMARY OF FEATURES AND PIN DESCRIPTION	Release 10	Page 4.5.11-4
FIGURE 4.5.11-D, SPD TABLE & INFORMATION	Release 10	Page 4.5.11-5
FIGURE 4.5.11-E, COMPARISON OF 184 PIN UNBUFFERED SDR SDRAM & DDR SDRAM DIMM--	Release 10	Page 4.5.11-6
FIGURE 4.5.11-F, KEYING METHODOLOGY	Release 10	Page 4.5.11-7
FIGURE 4.5.11-G & H, VDDID DEFINITION	Release 10	Page 4.5.11-8 & 9
FIGURE 4.5.11-I & J, CLOCK LAYOUT	Release 10	Page 4.5.11-10 & 11
FIGURE 4.5.11-G & H, FET SWITCH STRUCTURE	Release 10	Page 4.5.11-12
FIGURES 4.5.11-L through U, CONFIGURATION BLOCK DIAGRAM--	Release 10	Page 4.5.11-13⇒23
4.5.12 - 184 PIN DIMM FAMILY SUPPLEMENTARY DESIGN STANDARDS	Release 10	Page 4.5.12-1, 2
FIGURES 4.5.12-A through Q, CONFIGURATION BLOCK DIAGRAM--	Release 10	Page 4.5.12-3⇒19
FIGURE 4.5.12-R & S, CLOCK LAYOUT	Release 10	Page 4.5.12-20⇒23
FIGURES. 4.5.12-TA, & TB, 184P DDR REGISTERED DIMM PIN ASSIGNMENTS	Release 10	Page 4.5.12-24⇒26

Release 14

Section	Release #	Page #
4.5.13 - 144 & 168 PIN PROCESSOR ENHANCED MEMORY MODULE FAMILIES WITH EDO-DRAM OR SDRAM	Release 10 ..	Page 4.5.13-1
4.5.13.1, PEMM SPECIFIC TERMS AND DEFINITIONS	Release 10 ..	Page 4.5.13-2
4.5.13.2, PEMM MODES OF OPERATION	Release 10	Page 4.5.13-3⇒7
4.5.13.3, REPRESENTATIVE BLOCK DIAGRAMS	Release 10 .	Page 4.5.13-8⇒12
4.5.14 - 240 PIN UNBUFFERED AND REGISTERED DDR2 SDRAM DIMM FAMILY	Release 12 ..	Page 4.5.14-1
FIGURES 4.5.14-A, & B, PIN ASSIGNMENTS	Release 12 .	Page 4.5.14-2,3
FIGURE 4.5.14-C, PIN DESCRIPTION	Release 12 ..	Page 4.5.14-4
FIGURE 4.5.14-D, PIN SUMMARY	Release 12 ..	Page 4.5.14-5
4.6. Sixteen BYTE Modules	Release 7	Page 4.6-1
4.6.1 - 278 PIN Buffered SDRAM, 144 Bit DIMM FAMILY	Release 7	Page 4.6.1-1
FIGURE 4.6.1-A,B,C, 144 BIT SIMM PINOUT, TOP, MIDDLE, & BOTTOM PARTS ...	Release 7c8 ..	Page 4.6.1-2,3,4
FIGURE 4.6.1-D, 144 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES	Release 7	Page 4.6.1-5
FIGURE 4.6.1-E, F, 144 BIT SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS .	Release 5-7	Page 4.6.1-6
FIGURE 4.6.1-G, H, 144 BIT SDRAM CONFIGURATION BLOCK DIAGRAMS	Release 7	Page 4.6.1-7, 8
4.20 - MODULE SPECIFICATION APPENDIX	Release 11r12r13 .	Page 4.20-1
4.20.1 - Standard Template for JEDEC Module Specification Standards	Release 11 ..	Page 4.20.1-1⇒4
4.20.2 - 168 Pin PC133 SDRAM Registered DIMM Design Specification	Release 11 .	Page 4.20.2-1⇒71
4.20.3 - 144 Pin PC133 SDRAM Unbuffered SO-DIMM Reference Design Specification	Release 11 .	Page 4.20.3-1⇒26
4.20.4 - 184 Pin PC1600/2100 DDR SDRAM Registered DIMM Design Specification ..	Release 11r12	Page 4.20.4-1⇒61
4.20.5 - 184 Pin PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification ..	Release 11r12	Page 4.20.5-1⇒41
4.20.6 - 200 Pin PC3200/PC2700 DDR SDRAM Unbuffered SO-DIMM Reference Design Spec.	Release 11r13	Page 4.20.6-1⇒28
4.20.7 - 184 Pin, PC2700/3200 DDR SDRAM Registered DIMM Reference Design Specification, Rev. 2.0	Release 12r14	Page 4.20.7-1⇒58
4.20.8 - 184 Pin, PC3200/PC2700 DDR SDRAM Unbuffered DIMM with TSOP-Based DRAMs Reference Design Specification	Release 12r13	Page 4.20.8-1⇒44
4.20.9 - 100 Pin, DDR SDRAM Unbuffered 32b DIMM Reference Design Specification, Rev 1.1	Release 13r14	Page 4.20.9-1⇒32
4.20.10 - 240-Pin PC2-3200/PC2-4300 DDR2 SDRAM Registered DIMM Reference Design Specification, Rev. 1.0	Release 14	Page 4.20.10-1⇒68
4.20.11 - 200-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev. 0.52	Release 14	Page 4.20.11-1⇒44
4.20.12 - 214-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered MicroDIMM Reference Design Specification, Rev 0.5	Release 14	Page 4.20.12-1⇒28
4.20.13 - 240-Pin PC2-3200/PC2-4300 DDR2 SDRAM Unbuffered DIMM Reference Design Specification, Rev. 1.0	Release 14	Page 4.20.13-1⇒54
5 PROGRAMMABLE LOGIC AND ASIC DEVICES	Release 1	Page 5-1
5.1 Pin Out Standards	Release 1	Page 5-1
5.1.1 PIN-OUT STANDARDS FOR PLD DIP TO SCC CONVERSION	Release 4	Page 5-1
5.1.1.1 - 20 PIN DIP to 20 TERMINAL SCC, 0.350" BY 0.350", Fig. 5-1 ..	Release 1	Page 5-1
5.1.1.2 - 24 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5-2 ..	Release 1	Page 5-1
5.1.1.3 - 28 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5-2 ..	Release 1	Page 5-1
5.1.1.4 - 24 PIN FUNCTIONS IN 28 PIN DIP & 28 TERMINAL SCC, Fig. 5-9	Release 1	Page 5-1
5.1.1.5 - 20 PIN FUNCTIONS IN 28 TERMINAL SCC AND 24 PIN DIP FOR HIGH SPEED OPERATION, Fig. 5-11	Release 4	Page 5-1

Release 14

JEDEC Standard No. 21-C

Section	Release #	Page #
5.1.2 POWER PIN LOCATIONS FOR PLD and ASIC DEVICES	Release 1	Page 5-1
5.1.2.1 - POWER PIN LOCATIONS FOR ECL PLD IN DIP	Release 1	Page 5-1
5.1.2.2 - POWER PIN LOCATIONS FOR TTL PLD IN DIP and CC	Release 1	Page 5-1
5.1.2.3 - POWER PIN LOCATIONS FOR TTL PROGRAMMABLE ASIC IN DIP and CC	Release 1	Page 5-1
5.1.2.4 - POWER PIN LOCATIONS FOR PLD IN 132 PIN QFP	Release 1	Page 5-1
5.1.3 Nomenclature for FPLD	Release 1	Page 5-1
5.1.4 PLD Data Transfer Format	Release 1	Page 5-1
5.1.5 PLD Standard OUTPUT LOADS	Release 5	Page 5-1
FIGURE 5-1, 20 PIN DIP TO 20 TERMINAL CC PLD CONVERSION	Release 1	Page 5-3
FIGURE 5-2, 24 & 28 PIN DIP TO 27 TERMINAL CC CONVERSION	Release 2	Page 5-4
FIGURE 5-3, POWER PIN PLACEMENT FOR ECL PLD	Release 1	Page 5-5
FIGURE 5-4, 40 PIN DIP PLD POWER PIN PLACEMENT	Release 1	Page 5-6
FIGURE 5-5, 44 TERMINAL CC POWER PIN PLACEMENT	Release 1	Page 5-7
FIGURE 5-6, 48 & 64 PIN DIP ASIC POWER PIN PLACEMENT	Release 1	Page 5-8
FIGURE 5-7, 52, 68, & 84 TERMINAL CC ASIC POWER PIN PLACEMENT	Release 1	Page 5-9
FIGURE 5-8A, PLD STANDARD LOADS, DEFINITIONS	Release 5	Page 5-11
FIGURE 5-8B, PLD STANDARD LOAD CIRCUIT	Release 5	Page 5-12
FIGURE 5-8C, PLD OUTPUT LOAD CALCULATIONS	Release 5	Page 5-13
FIGURE 5-8D, PLD AC LOAD LINES	Release 5	Page 5-14
FIGURE 5-9, 24 PIN PLD FUNCTIONS IN 28 PIN DIP AND SCC	Release 3	Page 5-15
FIGURE 5-10, 132 PIN PQFP POWER PIN LOCATIONS	Release 3	Page 5-16
FIGURE 5-11, HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS	Release 4	Page 5-17
6 APPLICABLE OTHER DOCUMENTS	Release 1	Page 6-1
6.1 - Standard Manufacturers Identification Code., JEDEC Publication No. 106A	Release 1	Page 6-1
6.2 - Interface Standard for Low Voltage TTL-Compatible Devices (LVTTTL), JEDEC Standard No. 8 and Addendum No. 1	Release 1	Page 6-1
6.3 - Package Outlines, JEDEC Publication 95	Release 1	Page 6-1
6.4 - PLD Data Transfer Format, JEDEC Standard 3-B	Release 1	Page 6-1
6.5 - Nomenclature for FPLD, EIA Standard RS-428	Release 1	Page 6-1
6.6 - DDR SDRAM Device Specification, JESD-79	Release 11	Page 6-1
Annex A - (Informative) Differences Between Release 14 and Release 13	Release 14	Page A-1

Release 14

3.11.5 SDRAM & SGRAM Architectural and Operational Features

The following standards describe features or characteristics that are applicable to one or more of the SDRAM devices described in section 3.11 of Std. 21-C. This section is being reorganized in Release 9 to accommodate several new categories of devices being covered. The original Standards included in this section covered only Single Data Rate (SDR) SDRAMs (these devices were initially just referred to as SDRAM). This coverage has expanded to include Double Data Rate (DDR) SDRAMs, Enhanced SDRAMs (ESDRAM), and Virtual Channel SDRAM (VCSDRAM). The new organization of Section 3.11.5 brings together into one sub-section all standards specifically applicable to one class of device. All standards in the following section that are defined for SDRAM, are also applicable to SGRAM, (even though SGRAM is not mentioned), unless SGRAM is specifically excluded.

A complete Table of Contents of all SDRAM & SGRAM Features follows.

3.11.5.1 - General SDRAM Functions

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE FOR CKE

3.11.5.1.3 - SDRAM MODE REGISTER ARCHITECTURE

3.11.5.1.4 - POWER ON SEQUENCE (RECOMMENDED)

3.11.5.1.5 - AUTO PRECHARGE

3.11.5.1.6 - PRECHARGE ALL BANKS

3.11.5.1.7 - MODE REGISTER WRITE TIMING

3.11.5.1.8 - AUTO REFRESH

3.11.5.1.9 - WRITE LATENCY

3.11.5.1.10 - DQM LATENCY FOR READS AND WRITES

3.11.5.1.11 - PRECHARGE TIMING FOR READS

3.11.5.1.12 - COLUMN ADDRESS TO COLUMN ADDRESS DELAY

3.11.5.1.13 - CKE TIMING FOR POWER DOWN

3.11.5.1.14 - CKE TIMING FOR CLOCK SUSPEND

3.11.5.1.15 - SELF REFRESH ENTRY AND EXIT

3.11.5.1.16 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

3.11.5.1.17 - Full Page Burst Mode for SDRAM/SGRAM

3.11.5.1.18 - Deep Power Down Mode

3.11.5.2 - DDR Specific SDRAM Functions

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs/SGRAMs

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

- 3.11.5.2.7 - Burst Stop Command for DDR SDRAMs/SGRAMs**
- 3.11.5.2.8 - DDR SDRAM/SGRAM Full Sequential Burst Ordering**
- 3.11.5.2.9 - DDR SDRAM QS Coincident with Data**
- 3.11.5.2.10 - Extended Mode Register Set for DDR SDRAM / SGRAM.**
- 3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS**
- 3.11.5.2.12 - Refresh Requirements**
- 3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM**

3.11.5.3 - ESDRAM Specific SDRAM Functions

- 3.11.5.3.1 - Read-AutoPrecharge Operation for SDR ESDRAM**
- 3.11.5.3.2 - Read-AutoPrecharge Operation for DDR ESDRAM**
- 3.11.5.3.3 - Cache Load Operation for SDR ESDRAM**
- 3.11.5.3.4 - Cache Load Operation for DDR ESDRAM**
- 3.11.5.3.5 - No Write Transfer, Mode of Operation for SDR ESDRAM**
- 3.11.5.3.6 - No Write Transfer, Mode of Operation for DDR ESDRAM**

3.11.5.4 - VCSDRAM Specific SDRAM Functions

- 3.11.5.4.1 - Command Table for Virtual Channel SDR SDRAM**
- 3.11.5.4.2 - Command Table for Virtual Channel DDR SDRAM**
- 3.11.5.4.3 - Virtual Channel SDR SDRAM Mode Register Architecture**
- 3.11.5.4.4 - Virtual Channel DDR SDRAM Mode Register Architecture**

3.11.5.5 - DDR2 Specific SDRAM Functions

3.11.5.6 - GDDR2 Specific SGRAM Functions

■ 3.11.5.7 - GDDR3 Specific SGRAM Functions

3.11.5.1 - General SDRAM Functions

The Standards in this section are general functions that are applicable to both SDR and DDR SDRAM except where that function is specifically covered for a class of devices in one of the following sections.

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

This table defines the interface states required to execute the standard SDRAM operational functions. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE FOR CKE

This table defines the interface states required to execute the standard SDRAM operational functions with respect to the CKE input. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.1.3 - SDRAM & SGRAM MODE REGISTER ARCHITECTURE

This standard describes the architecture of the SDRAM & SGRAM internal MODE REGISTER and the codes that are allowable for use in it. This is applicable to both SDR & DDR devices.

3.11.5.1.4 through 3.11.5.1.17 — SDRAM OPERATIONAL CYCLES AND MODES

The following standards define and describe a number of operational cycles and modes of SDRAM. They are ordered roughly in the sequence in which they would be used in normal SDRAM operation.

3.11.5.1.4 - POWER ON SEQUENCE (RECOMMENDED)

This standard gives a recommended power, clock, and logic-level sequence to be used on power-up to prevent data bus contention.

3.11.5.1.5 - AUTO PRECHARGE

This standard gives the logic function used to active the AUTO-PRECHARGE function.

3.11.5.1.6 - PRECHARGE ALL BANKS

This standard gives the logic function used to activate the PRECHARGE-ALL-BANKS function.

3.11.5.1.7 - MODE REGISTER WRITE TIMING

This standard defines the logic sequence and timing required to write into the MODE REGISTER.

3.11.5.1.8 - AUTO REFRESH

This standard defines the logic state and interface sequence required to perform an AUTO REFRESH

3.11.5.1.9 - WRITE LATENCY

This standard defines WRITE LATENCY and illustrates it with a timing diagram.

3.11.5.1.10 - DQM LATENCY FOR READS AND WRITES

In this standard DQM LATENCY is defined and the relationships between the DQM signal and the interface data for READs and WRITEs is defined and shown in timing diagrams.

3.11.5.1.11 - PRECHARGE TIMING FOR READS

This standard describes the relationship between the assertion of a PRECHARGE command and data out from a READ command.

3.11.5.1.12 - COLUMN ADDRESS TO COLUMN ADDRESS DELAY

This standard defines constraints imposed on the CA to CA delay and illustrates them with a timing diagram.

3.11.5.1.13 - CKE TIMING FOR POWER DOWN

This standard describes the interface sequence required to place the SDRAM into the POWER-DOWN state using CKE.

3.11.5.1.14 - CKE TIMING FOR CLOCK SUSPEND

This standard describes the interface timing sequence when CKE is used to suspend the clock.

3.11.5.1.15 - SELF REFRESH ENTRY AND EXIT

This standard defines the logic states and timing sequence used to enter and exit the SELF-REFRESH mode.

3.11.5.1.16 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called "Burst Terminate"] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, this section defines the functionality that is required.

3.11.5.1.17 - Full Page Burst Mode for SDRAM/SGRAM

Full page burst mode is an optional feature for SDRAM/SGRAM. If full page burst mode is included in an SDRAM or SGRAM, this section gives the required functionality.

3.11.5.1.18 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called "Burst Terminate"] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, this section defines the functionality that is required.

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H L L L L L L L	X H H H L L L L	X H H L H H L L	X H L X H L H L	X X BA BA, CA BA, RA BA, A10 X Op-code	NOP NOP ILLEGAL ² ILLEGAL ² Row (& Bank) active; Latch Row Address NOP ⁴ Auto-Refresh ⁵ Mode Register Access ⁵
ROW ACTIVE	H L L L L L L	X H H H L L L	X H L L H H L	X X H L L H L X	X X BA, CA, A10 BA, CA, A10 BA, RA BA, A10 X	NOP NOP Begin Read; Latch CA; Determine AP ⁷ Begin Write; Latch CA; Determine AP ⁷ ILLEGAL ² Precharge ⁸ ILLEGAL
READ	H L L L L L L	X H H H L L L	X H H L L H L	X H L H L H L X	X X BA BA, CA, A10 BA, CA, A10 BA, RA BA, A10 X	NOP (Continue Burst to End;⇒Row Active) ⁶ NOP(Continue Burst to End;⇒Row Active) ⁶ RESERVED (Term. Burst);⇒Row Active Term Burst, New Read, Determine AP ³ Term Burst, Start Write, Determine AP ^{3, 7} ILLEGAL ² Term Burst, Precharge Timing for Reads ILLEGAL
WRITE	H L L L L L L	X H H H L L L	X H H L L H L	X H L H L H L X	X X BA BA, CA, A10 BA, CA, A10 BA, RA BA, A10 X	NOP(Continue Burst to End;⇒Row Active) ⁶ NOP(Continue Burst to End;⇒Row Active) ⁶ RESERVED (Term Burst);⇒Row Active Term Burst, Start Read, Determine AP ^{3, 7} Term Burst, New Write, Determine AP ³ ILLEGAL ² Term Burst, Precharge ³ ILLEGAL
READ with AUTO Precharge	H L L L L L	X H H H H* L L	X H H L L H L	X H L H L X X	X X BA BA, CA, A10 X BA, RA, A10 X	NOP (Continue Burst to End;⇒Precharge) ⁶ NOP (Continue Burst to End;⇒Precharge) ⁶ ILLEGAL ² ILLEGAL ² ILLEGAL ILLEGAL ² ILLEGAL
WRITE with AUTO Precharge	H L L L L L	X H H H L L	X H H L L L	X H L H L X X	X X BA BA, CA, A10 X BA, RA, A10 X	NOP (Continue Burst to End;⇒Precharge) ⁶ NOP (Continue Burst to End;⇒Precharge) ⁶ ILLEGAL ² ILLEGAL ² ILLEGAL ILLEGAL ² ILLEGAL

TABLE 3.11.5.1-1
SDRAM FUNCTION TRUTH TABLE

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H L L L L L L	X H H H L L L	X H H L H H L	X H L X H L X	X X BA BA, CA BA, RA BA, A10 X	NOP⇒idle after tRP NOP⇒idle after tRP ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL ² NOP ⁴ ILLEGAL
ROW Activating	H L L L L L L	X H H H L L L	X H H L H H L	X H L* X H L X	X X BA * BA, CA BA, RA BA, A10 X	NOP⇒Row Active after tRCD NOP⇒Row Active after tRCD ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL ²
WRITE Recovering	H L L L L L L	X H H H L L L	X H H L H H L	X H L X H L X	X X BA BA, CA BA, RA BA, A10 X	NOP NOP ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL
Refreshing	H L L L L L L	X H H L L L L	X H L H H L L	X X X X X X X	X X X X X X X	NOP⇒idle after tRC* NOP⇒idle after tRC * ILLEGAL ILLEGAL ILLEGAL
Mode Register Accessing	H L L L L L L	X H H H L L L	X H H L H H X	X H L X X X X	X X X X X X X	NOP NOP ILLEGAL ILLEGAL ILLEGAL ILLEGAL

ABBREVIATIONS

RA = Row Address
CA = Column Address

BA = Bank Address
AP = Auto Precharge

Term = Terminate
NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
 2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
 3. Must satisfy the "2n-rule", bus contention, but turn around, and/or write recovery requirements.
 4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).
 5. Illegal if any bank is not idle.
- ILLEGAL = Device operation and/or data-integrity are not guaranteed
6. If the device is programmed to use full page burst mode, the action is NOP, continue burst.
 7. The autoprecharge bit, AP, must be 0 in full page burst mode where the autoprecharge function is illegal
 8. Precharge All Banks determined by state of A10

* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5.1-1
SDRAM FUNCTION TRUTH TABLE (Continued)

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE _{n-1}	CKE _n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	A _n	ACTION
Self- refresh ⁶	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self-Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power- Down	H	X*	X	X	X	X	X	INVALID
	L	H*	H	X*	X*	X*	X	EXIT Power Down⇒ABI
	L	H*	L	H	H	H	X	EXIT Power Down⇒ABI
	L	H*	L	H	H*	L*	X	ILLEGAL
	L	H*	L	H*	L*	X*	X	ILLEGAL
	L	H*	L	L	X*	X*	X	ILLEGAL
	L	L	X	X*	X*	X	X	NOP(Maintain Low-Power Mode)
All Banks Idle ⁷	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power-Down
	H	L	L	H	H	H	X	Enter Power-Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle ⁸
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle ⁸
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS

ABI = All Banks Idle

NOTES:

6. CKE Low-to-High transition will re-enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.

7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.

8. Must be legal command.

* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5.1-2
SDRAM FUNCTION TRUTH TABLE for CKE

3.11.5.1.3 - SDRAM & SGRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM or SGRAM) chip. Its purpose is to store the mode-of-operation data. This data is written after power-on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{\text{CAS}}$ Latency (Defined separately for SDR and DDR devices), and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode-Register-Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

SDRAM Mode Register architecture:

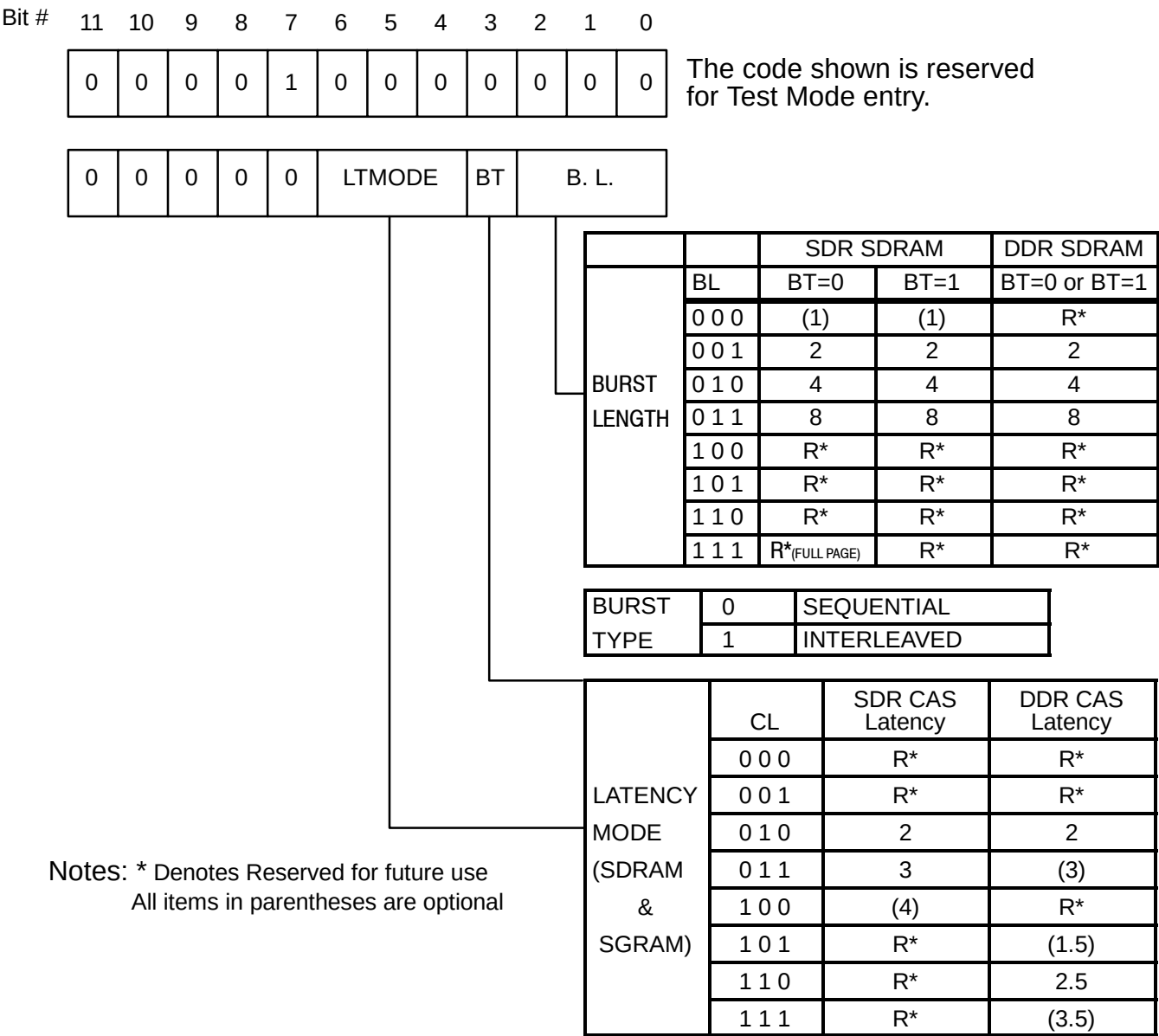


FIGURE 3.11.5.1-1
SDRAM & SGRAM MODE REGISTER ARCHITECTURE

3.11.5.1.4 - Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High-Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High-Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

3.11.5.1.5 - Auto Precharge

The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle. The following table defines the options available from AP during the column address portion of any cycle.

AP	Option
0	Do not auto precharge, leave bank active at end of burst.
1	Auto precharge bank specified by BA at end of burst.

The user must wait until the precharge is completed before issuing another command to the device. Timing for auto precharge is required to be the same as or less than the minimum requirement of external precharge.

The Autoprecharge Bit, AP, must be 0 in full page burst mode where the autoprecharge function is illegal.

The autoprecharge function is not allowed in full page burst mode since the end of the burst is indefinite. Therefore the autoprecharge bit, AP, is ignored during read or write commands if the mode register is set to full page burst mode.

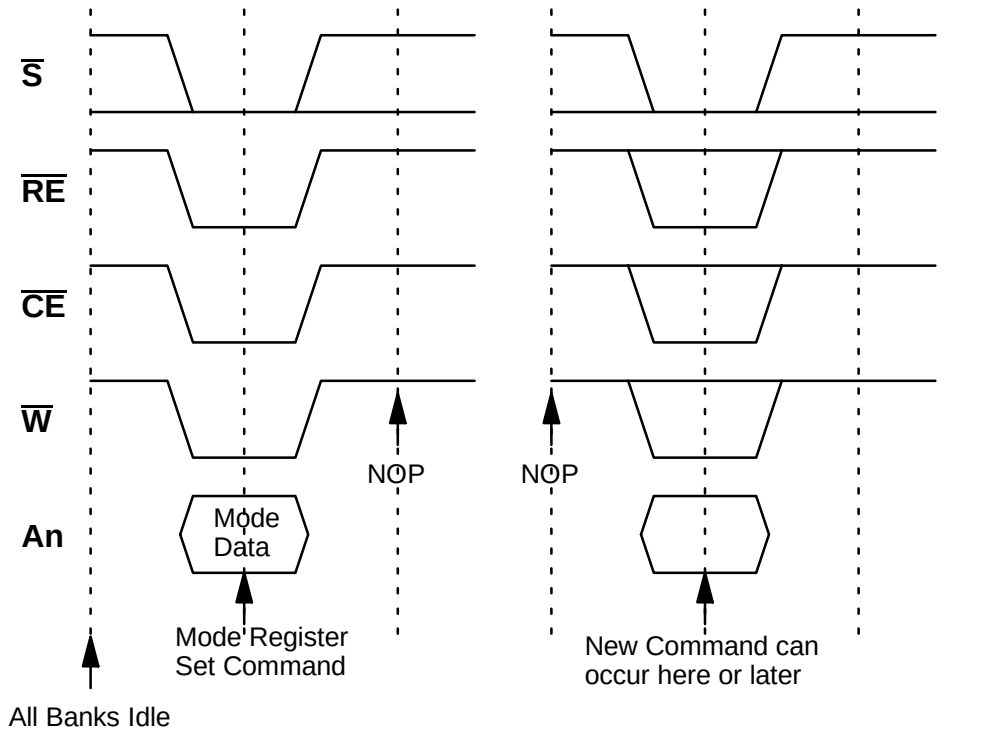
3.11.5.1.6 - Precharge All Banks

The user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks. BA is used to specify the bank to be precharge, and AP is used to indicate the precharge option. The following table defines the options available from AP during the precharge cycle.

PA	Option
0	Precharge bank specified by BA
1	Precharge All banks

3.11.5.1.7 - Mode Register Write Timing

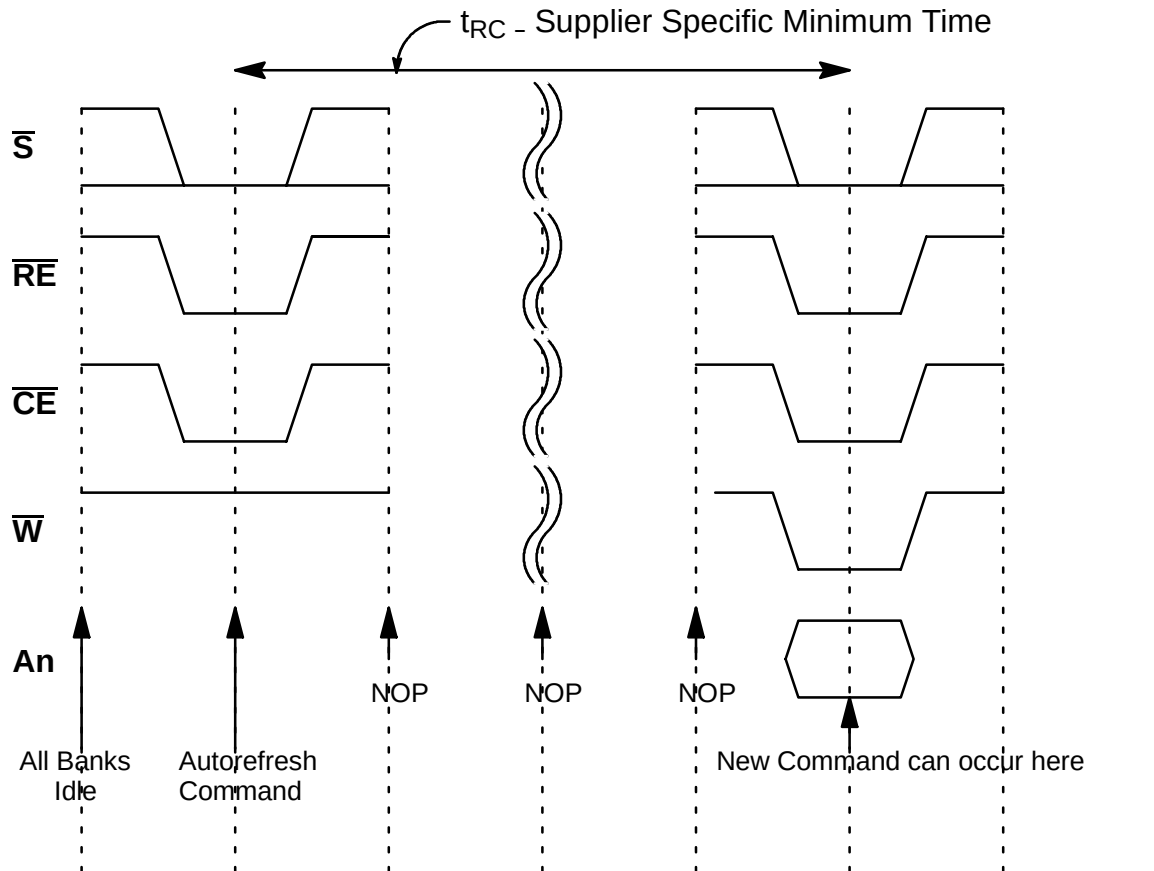
The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.



Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.8 - Auto Refresh

AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address being supplied by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE). Autorefresh is entered by asserting RE and CE on the same clock cycle. All banks will automatically precharge at the end of the refresh cycle. Additional commands must not be supplied to the device during the minimum refresh time specified. The following timing diagram illustrates the refresh cycle requirements.

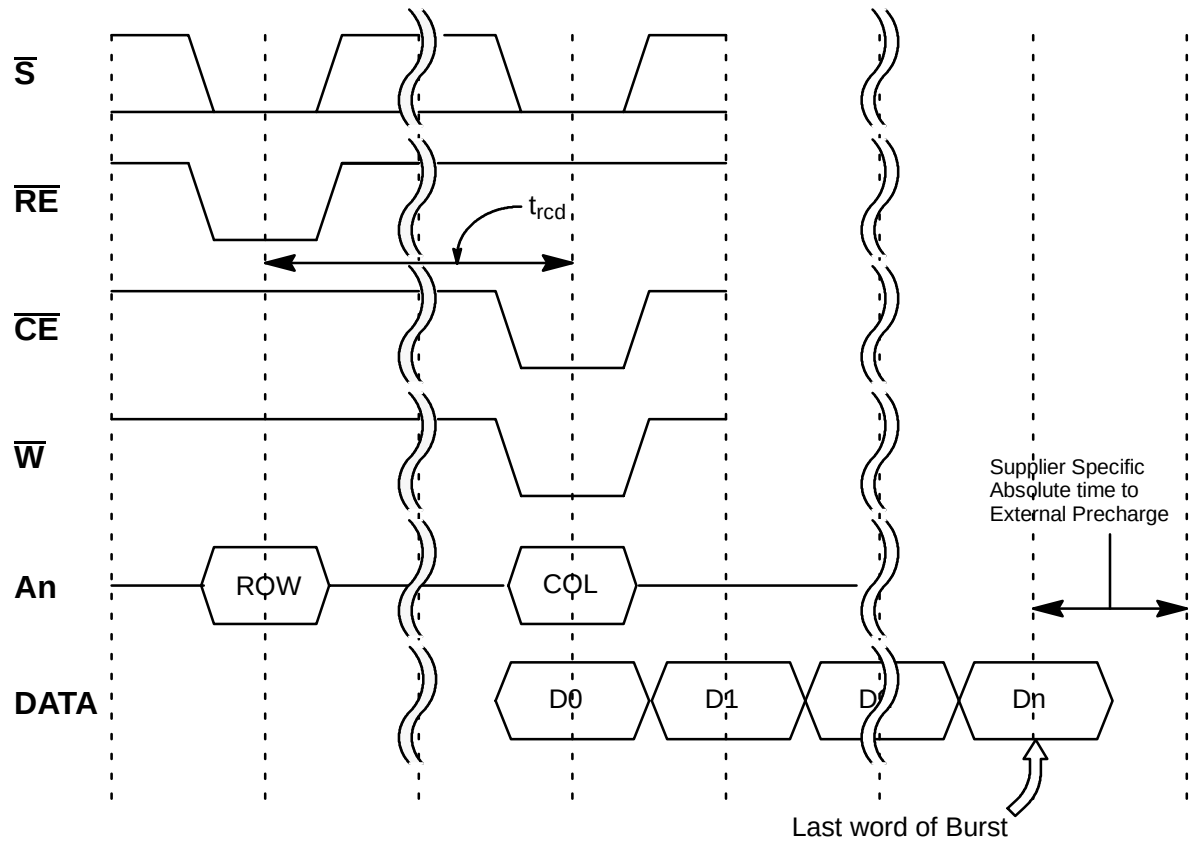


Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.9 - Write Latency

(Write Latency = 0)

Write Latency for SDR Synchronous DRAM shall be as defined as the clock cycle difference between the clock where write command and column address are asserted and the clock where first data to be written is asserted.

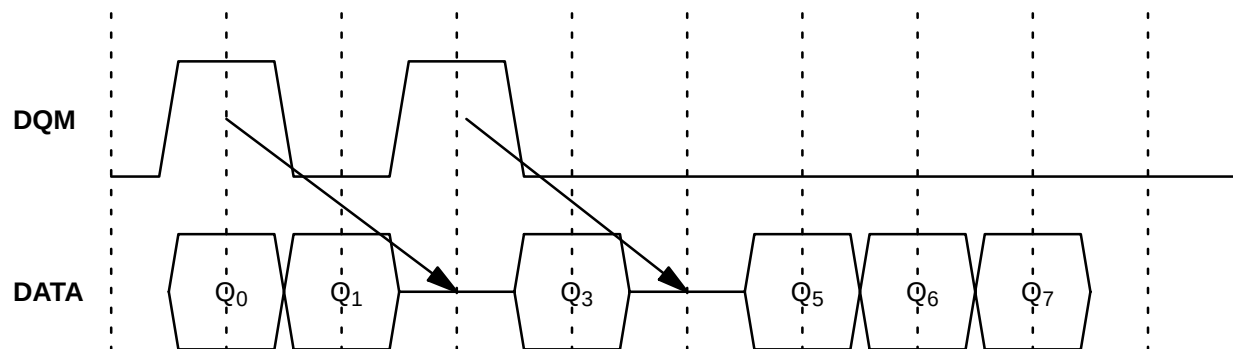


Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.10 - DQM Latency for Reads and Writes (DQM Write Latency = 0)

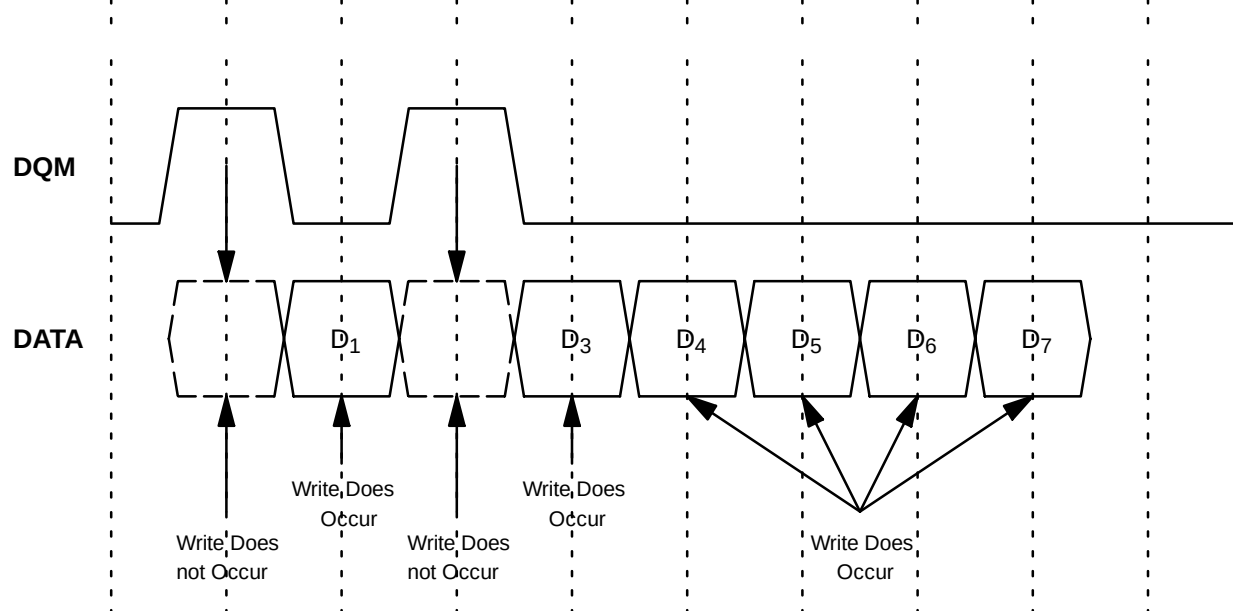
DQM is a multiple-function signal defined as the data mask for both reads and writes. During reads, DQM performs synchronous output enable. During writes, DQM performs write data masking. The requirement for high-speed operation, and the synchronous nature of SDRAM devices requires that DQM latency be different for reads than it is for writes.

For Reads, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the output bus has been forced to High-Z. The following timing diagram illustrates the standard of 2 clocks.



Note: Clock Low-to-high transitions occur at the dotted lines.

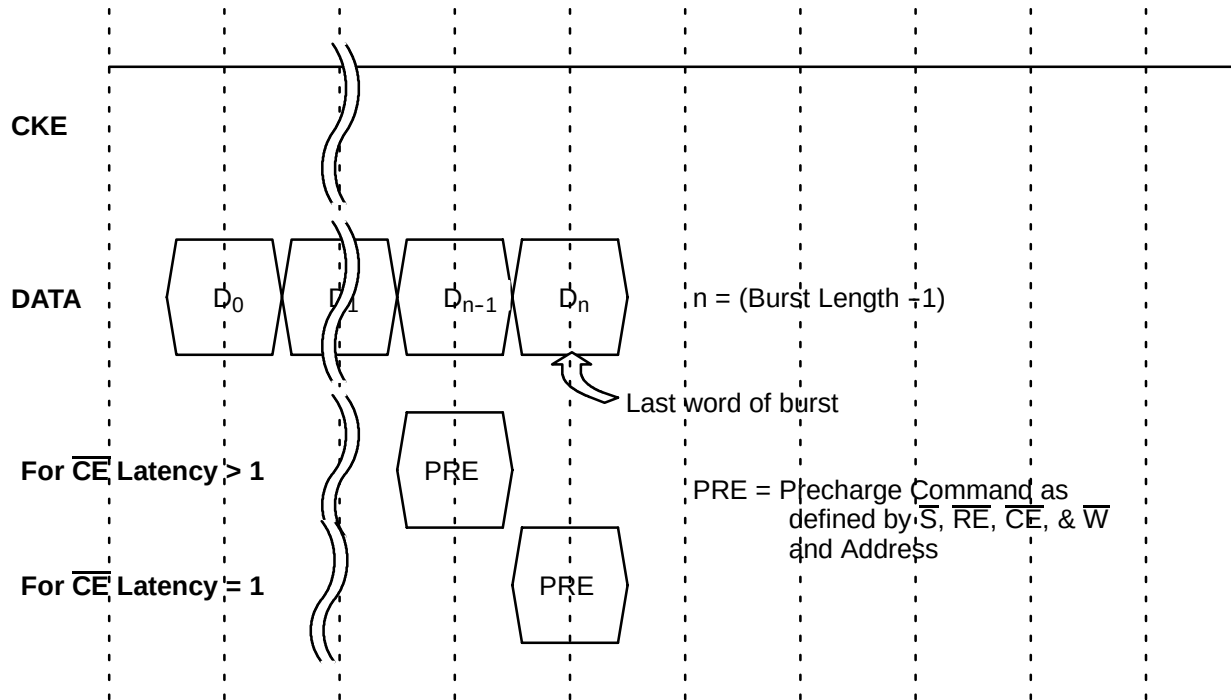
For Writes, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the write input data is inhibited. The following timing diagram illustrates the standard of 0 clocks.



Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.11 - Precharge Timing for Reads

The assertion of the precharge command has a direct relationship to the timing of data out for a read cycle. For a CE latency of 1, the minimum requirement is that the precharge command will be allowed to coincide with output of the last data from a burst regardless of burst length. For a CE latency greater than 1, the minimum requirement is that the precharge command will be allowed to coincide with output of the next-to-last data from a burst, regardless of burst length, without interrupting burst data. The following timing diagrams illustrate the requirements.



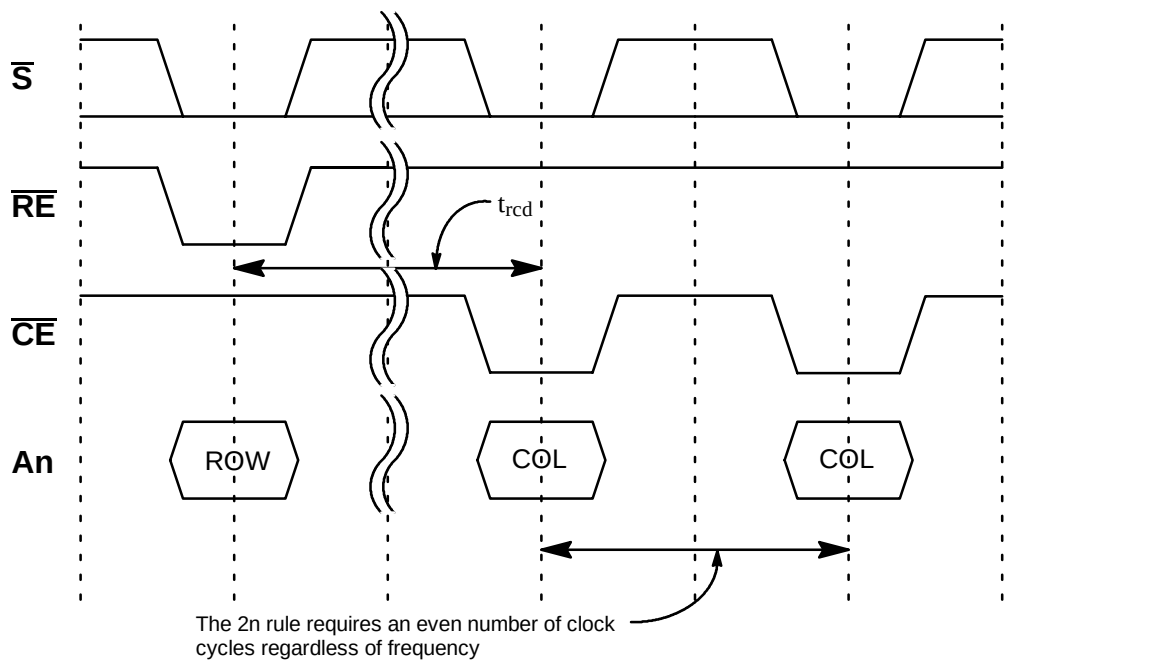
Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.12 - Column Address to Column Address Delay

The minimum column-address-to-column-address delay time, for page mode accesses, is two clock cycles, independent of operating frequency.

For interrupted bursts, column addresses must, at a minimum, follow the "2n rule" while a read or write burst is in progress. 2n rule: after the initial read or write command, a new column address can be presented to the device every other clock cycle. That is, if the initial read-or-write command occurred on an odd clock cycle, the new column addresses must be presented on an odd clock cycle while the burst is in progress.

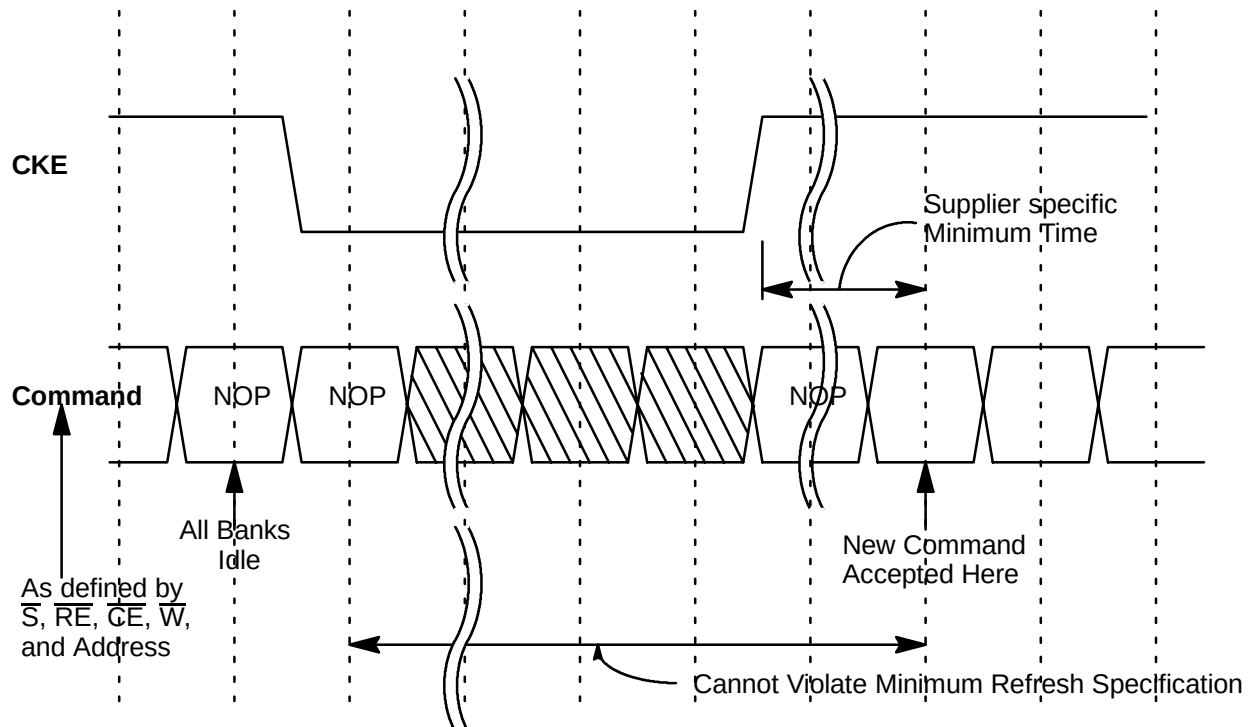
After the burst is completed, the 2n rule no longer applies, and a new column address may be presented to the device on any clock cycle. Essentially the 2n rule remains in effect for (CE Latency + burst length) clock cycles for reads and (write recovery + burst length) clock cycles for writes.



Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.13 - CKE Timing for Power Down

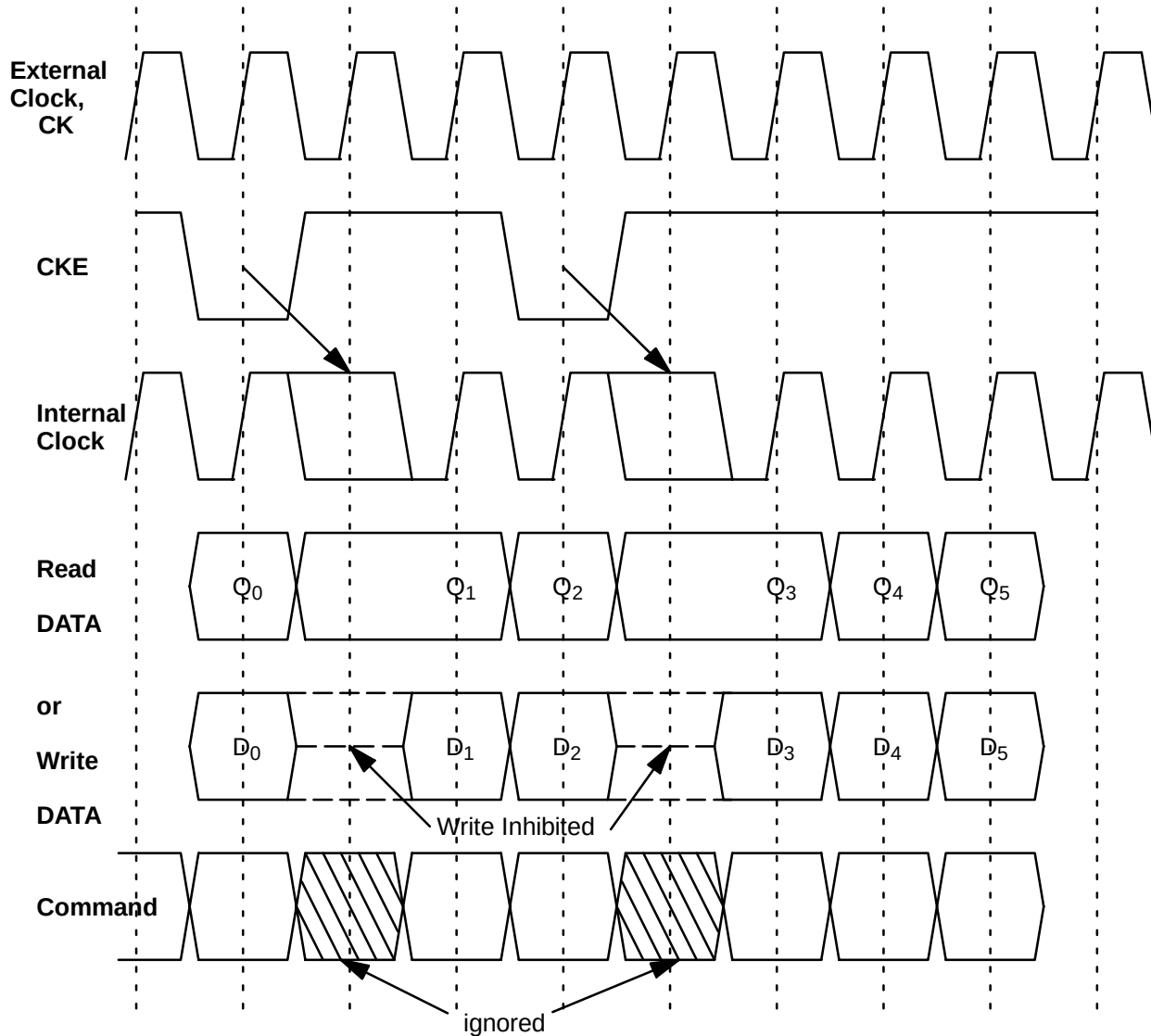
CKE is defined as the clock-enable signal and actually has the dual purpose of also being the signal that puts an SDRAM into a low power state. Using CKE to enter the low power state can only be performed while all internal banks of the device are precharged (IDLE). If all internal banks have been precharged, then CKE is used to gate the input buffers of the device. During power down the device is not refreshed. Therefore the minimum refresh specification still applies during power down. The following timing diagram illustrates power down mode.



Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.14 - CKE Timing for Clock Suspend

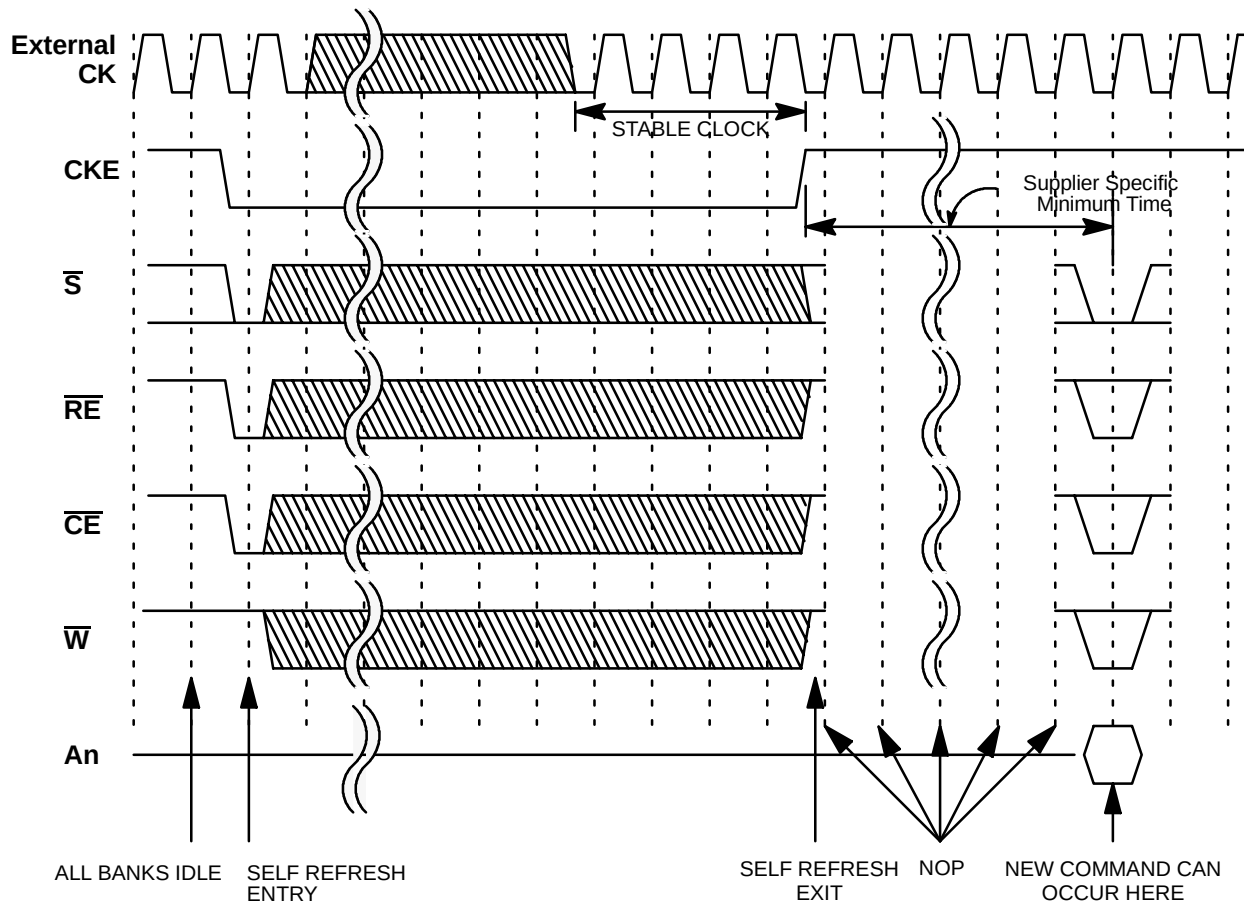
The following timing diagram is shown for CKE when 1 or more banks of the device are active. The effect on read data, write data, and command are all shown on the same diagram for reference only. The clock may be suspended for one or more clock cycles.



Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.15 - Self-Refresh Entry and Exit

In self refresh mode, the device refreshes itself without outside intervention. While the device is in self-refresh mode, CKE is the only enabled input to the device. All other inputs including the clock are disabled and any input is ignored. Self-refresh mode is entered by precharging all banks and then inserting an auto-refresh command with CKE low. Exit from self-refresh mode is accomplished by starting the clock and then asserting CKE. NOP commands must be asserted for a supplier-specified minimum period, which must include 3 clocks, to allow the device to return to the IDLE state.



3.11.5.1.16 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, the following functionality is required:

1. BST applies to all burst lengths, including the optional full page burst length when included.
2. BST is not a valid command during read or write with autoprecharge
3. When terminating a burst read command, the BST command must be issued n clock cycles before the clock edge at which the last desired data word is valid, where n equals the $\overline{\text{CAS}}$ latency for read operations minus 1. This is shown in Figure 3-1 with examples for $\overline{\text{CAS}}$ latency 1, 2 and 3 (higher $\overline{\text{CAS}}$ latencies follow the same pattern).

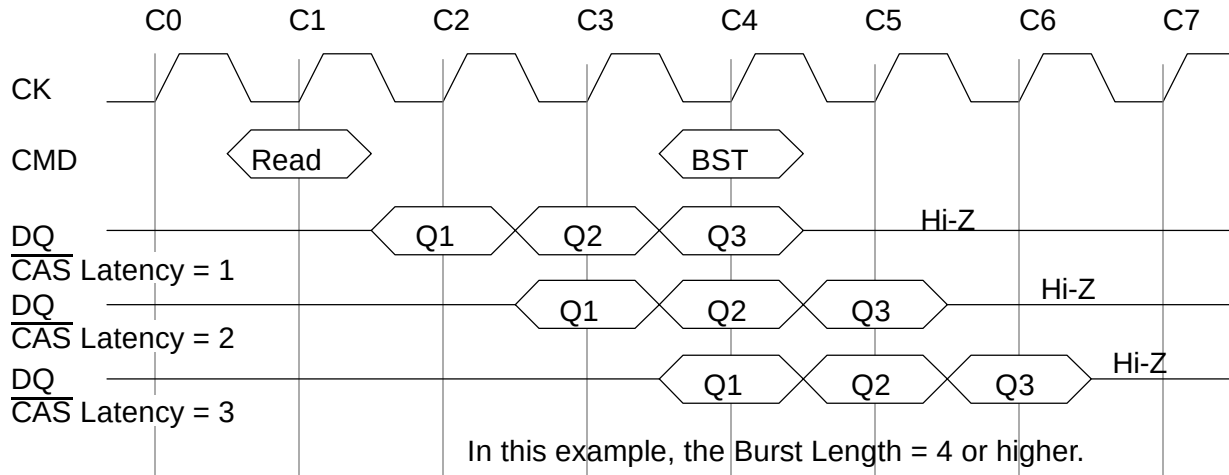


Figure -1: Terminating a Burst Read Command with BST

4. When terminating a burst write command, the BST command must be issued one clock after the clock edge which samples the last word of data that is required to be written into the memory. The DQM input(s) must be high for the clock edge that is coincident with the BST command. Input data on the DQ pins for the clock edge that is coincident with the BST command is ignored. Input data on the DQ pins for the clock edges after the BST command is also ignored unless a new write command is issued. This is shown in Figure 4-1.

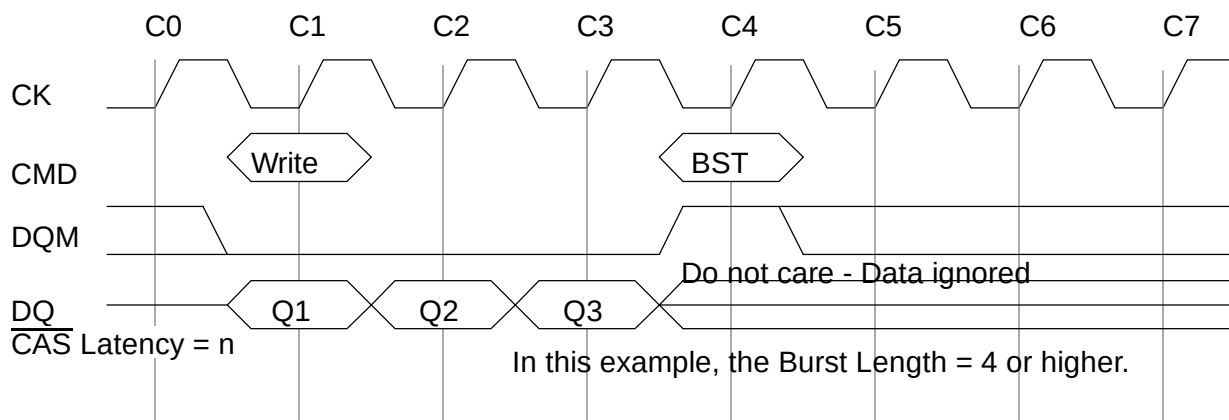


Figure -2: Terminating a Burst Write Command with BST

Note: Clock Low-to-high transitions occur at the dotted lines.

3.11.5.1.17 - Full Page Burst Mode for SDRAM/SGRAM

Full page burst mode is an optional feature for SDRAM/SGRAM. If full page burst mode is included in an SDRAM or SGRAM, the following functionality is required:

1. Full page burst operations (read or write) do not self terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 or 8, full page burst mode continues until it is terminated using another command. During full page burst mode, once the highest order column address is accessed, the count “wraps around” to column address 0 and continues.
2. A full page burst sequence can be terminated by a BST (burst stop command which is also an optional feature), a PRE (Precharge Command), a PREALL (Precharge all banks command) or another full page burst read or write command.
 - BST is an optional feature on SDRAMs/SGRAMs. BST will terminate the burst sequence, but will not cause the device to precharge the accessed bank (i.e., the bank remains active). Additional read or write commands can be executed while the bank is active. A subsequent PRE command is used to return the selected bank to the idle state (row precharge time must be satisfied). A subsequent PREALL command is used to return all banks to the idle state (row precharge time must be satisfied).
 - PRE will terminate the burst sequence and will initiate a precharge operation which returns the selected bank to the idle state (row precharge time must be satisfied).
 - PREALL will terminate the burst sequence and will initiate a precharge operation which returns all banks to the idle state (row precharge time must be satisfied)
 - Read/write interrupt of the full page burst will cause the present burst sequence to terminate and initiates a new read/write full page burst sequence with a new starting address.
3. Full page burst mode with autoprecharge, AP, is not a legal command. The AP bit must be zero for full page burst read or write commands

3.11.5.1.18 - Deep Power Down Mode

Deep Power Down Mode is an operating mode that is used to achieve maximum power reduction by cutting the power of the whole memory array of the devices. Data will not be retained once the device has entered into Deep Power Down Mode. Full initialization is required when the device exits from Deep Power Down Mode.

Truth Table

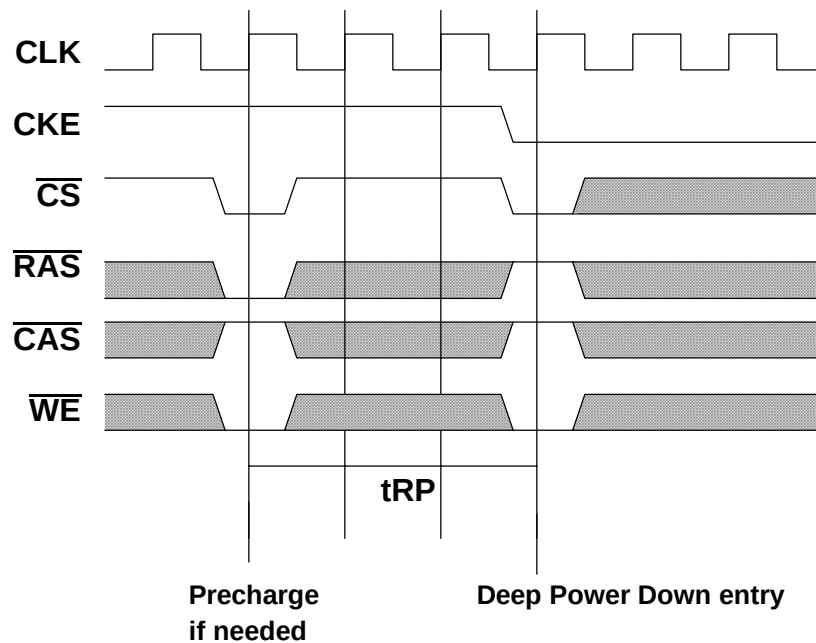
Current State	Command	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Idle	Deep Power Down Entry	H	L	L	H	H	L
Deep Power Down	Deep Power Down Exit	L	H	x	x	x	x

x: don't care

The deep power down mode is continued while CKE is kept low.

Deep Power Down Mode Entry

The deep power down mode is entered by having $\overline{CS}$ and $\overline{WE}$ held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock, while CKE is low. The following timing diagram illustrates deep power down mode entry.

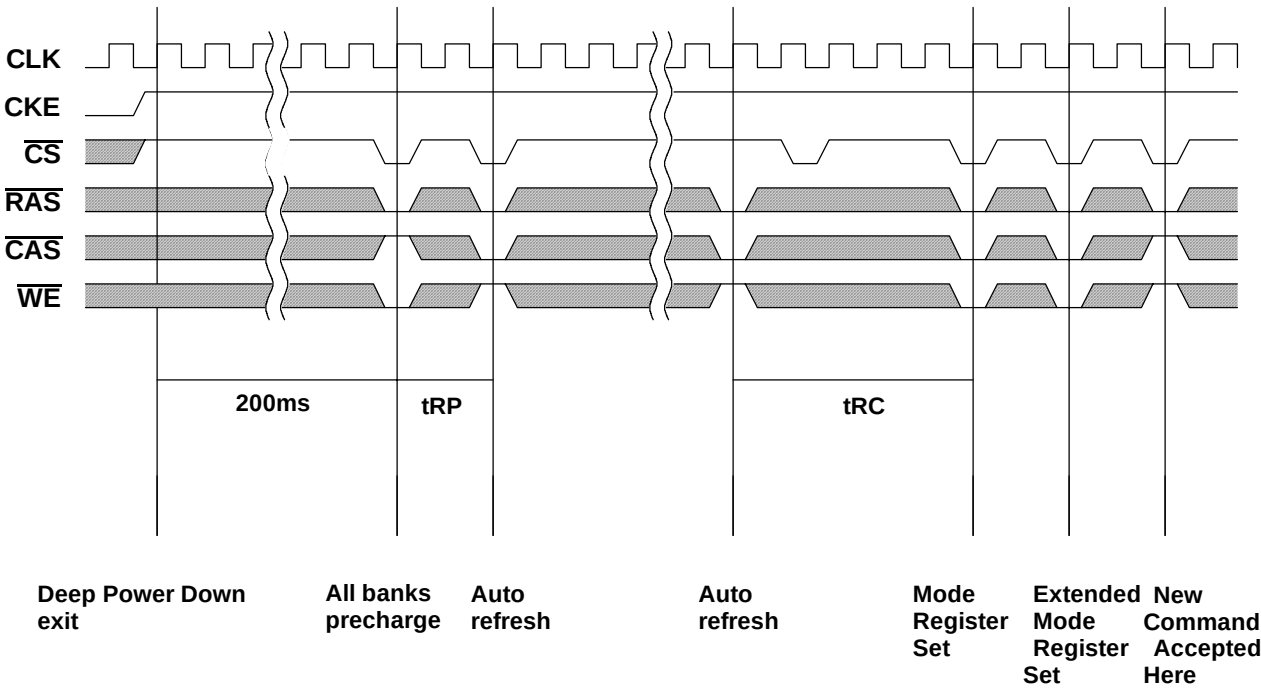


Deep Power Down Mode Exit Sequence

The deep power down mode is exited by asserting CKE high.
After the exit, the following sequence is needed to enter a new command.

- 1. Maintain NOP input conditions for a minimum of 200μsec.
- 2. Issue precharge commands for all banks of the device.
- 3. Issue 8 or more autorefresh commands.
- 4. Issue a mode register set command to initialize the mode register.
- 5. Issue an extended mode register set command to initialize the extended mode register.

The following timing diagram illustrates the deep power down mode exit sequence.



3.11.5.2 - DDR Specific SDRAM Functions

The Standards in this section are special functions that are applicable to DDR SDRAM except where that function specifically defines another class of device for which it is applicable.

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

To enable Doubled Data Rate and the control of that data in DDR SDRAMs, a signal to be identified by the label DQS will be added to the existing definition of the SDRAM. This section defines the timing relationships of the DQS signal.

3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

A pin will be added to the definition of DDR SDRAM devices whose polarity will be inverted to that of CK and labeled CK $\overline{}$ or $\overline{CK}$. That pin along with CK must be used to supply a differential clock to the DDR SDRAM devices.

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Read command may interrupt a Write burst and which input data is not written into the memory.

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Write command may interrupt a Read burst.

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

When a burst Read command is issued to a DDR SDRAM/SGRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

Precharge timing for Write operations in DRAMs requires enough time to allow "write recovery" which is the time required by a DRAM core to properly store a full "0" or "1" level before a Precharge operation. For DDR SDRAM/SGRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

3.11.5.2.7 - Burst Stop Command for DDR SDRAMs/SGRAMs

The Burst Stop [also called "Burst Terminate"] command (BST) is a mandatory feature for DDR SDRAMs/SGRAMs. This section describes the required functionality.

3.11.5.2.8 - DDR SDRAM/SGRAM Full Sequential Burst Ordering

This section gives, for DDR SDRAM & SGRAM, Y address ordering that is supported for sequential burst lengths (BL) of 2, 4, and 8:

3.11.5.2.9 - DDR SDRAM DQS Coincident with Data

The timing of the signal DQS relative to Read Data from the DDR SDRAM device is giving.

3.11.5.2.10 - Extended Mode Register Set for DDR SDRAM / SGRAM.

Extended mode register address space is provided by defining non-zero Bank address(s) for accesses that otherwise conform to the Mode Register Set (MRS) cycle. These Extended Mode Register Set cycles (EMRS) can be implemented as needed for function extensions to the standard.

3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS

This section defines the DLL disable/enable bit in the Extended Mode Register.

3.11.5.2.12 - Refresh Requirements

This section provides the precise definition of the refresh requirements.

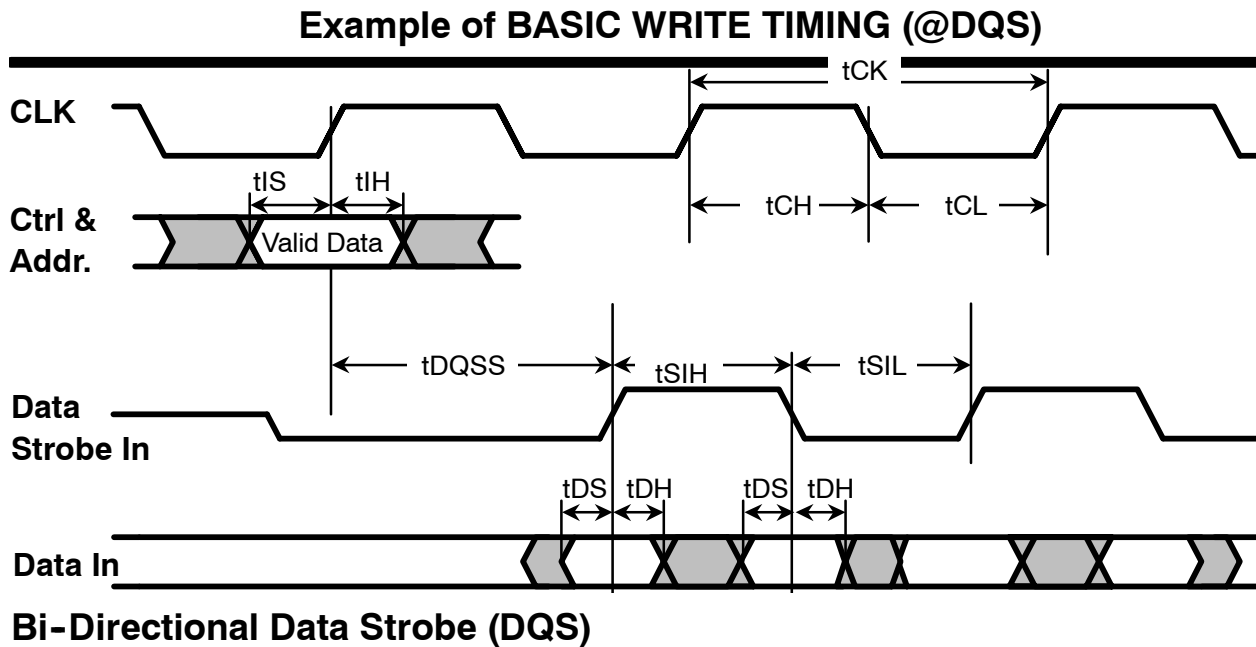
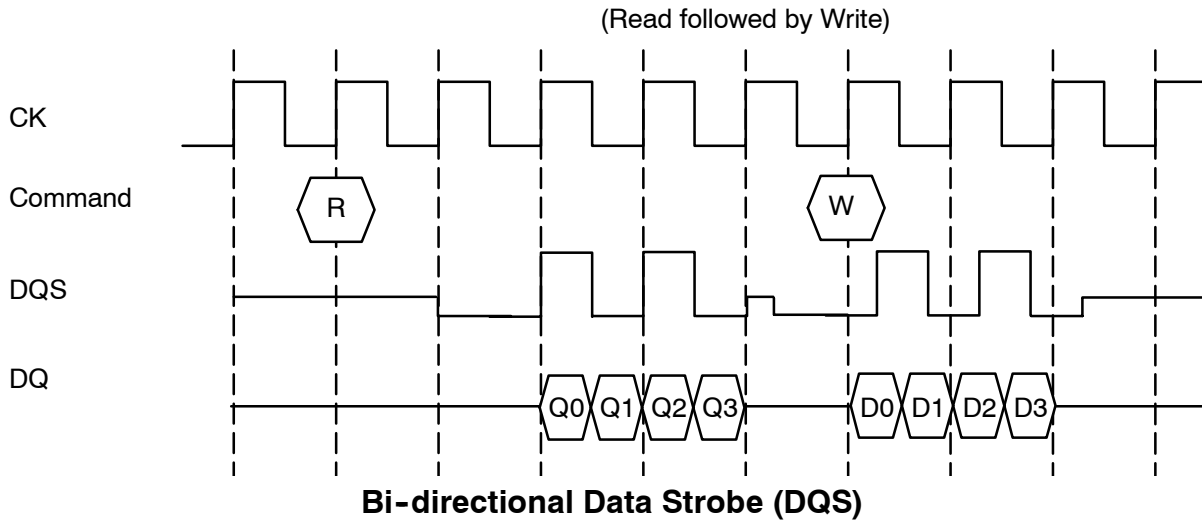
3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM

This section provides the Mode Register Set and Extended Mode Register Set definition for Low Power DDR SDRAM.

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

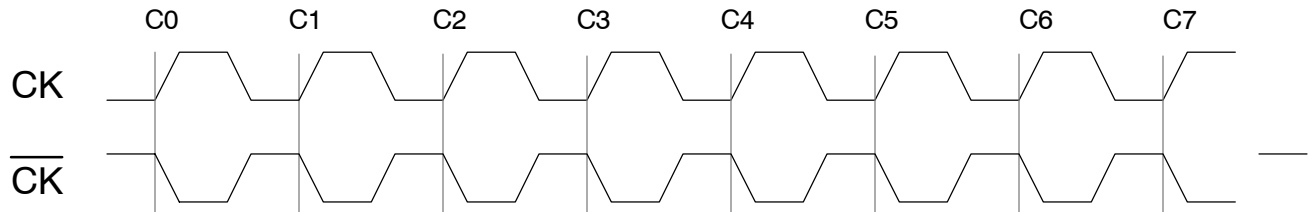
To enable Doubled Data Rate and the control of that data in DDR SDRAMs, a signal to be identified by the label DQS will be added to the existing definition of the SDRAM.

Driven by the DDR SDRAM during output of Read data, and Driven by the Memory Controller during input of Write data, the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM.



3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

A pin will be added to the definition of DDR SDRAM devices whose polarity will be inverted to that of CK and labeled CK $\bar{}$ or $\overline{CK}$. That pin along with CK must be used to supply a differential clock to the DDR SDRAM devices. The slew rates, and recommended terminations will be defined in subsequent standards. The voltage levels are defined in Section 3.11.6 for which standards have been published.



Differential Clock timing relationship (for reference only)

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs & SGRAMs

The following functionality establishes how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle (refer to Figure 1) is disallowed.
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation as shown in Figures 2 and 3.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the SDRAM/SGRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the SDRAM/SGRAM.
5. It is illegal for a Read command to interrupt a Write with autoprecharge command.

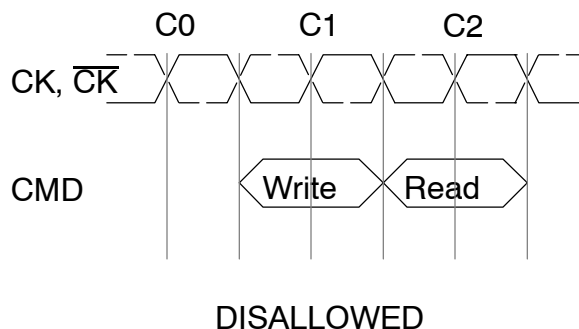
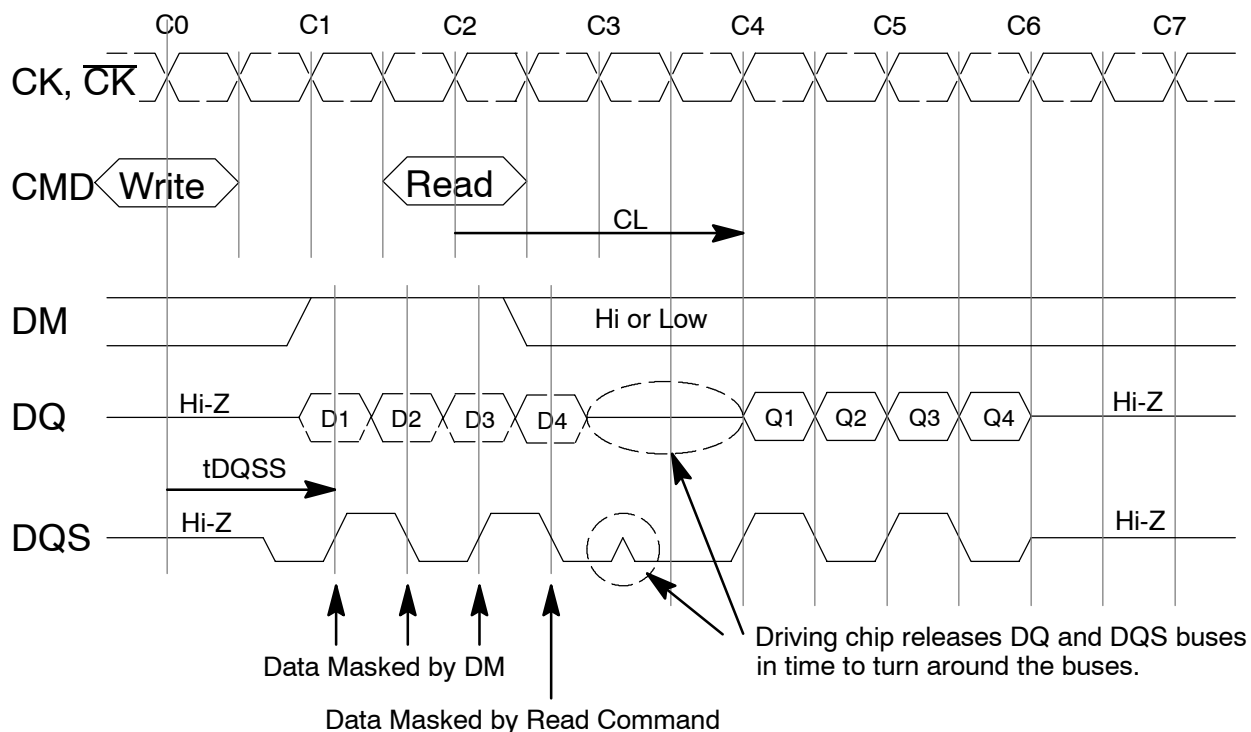


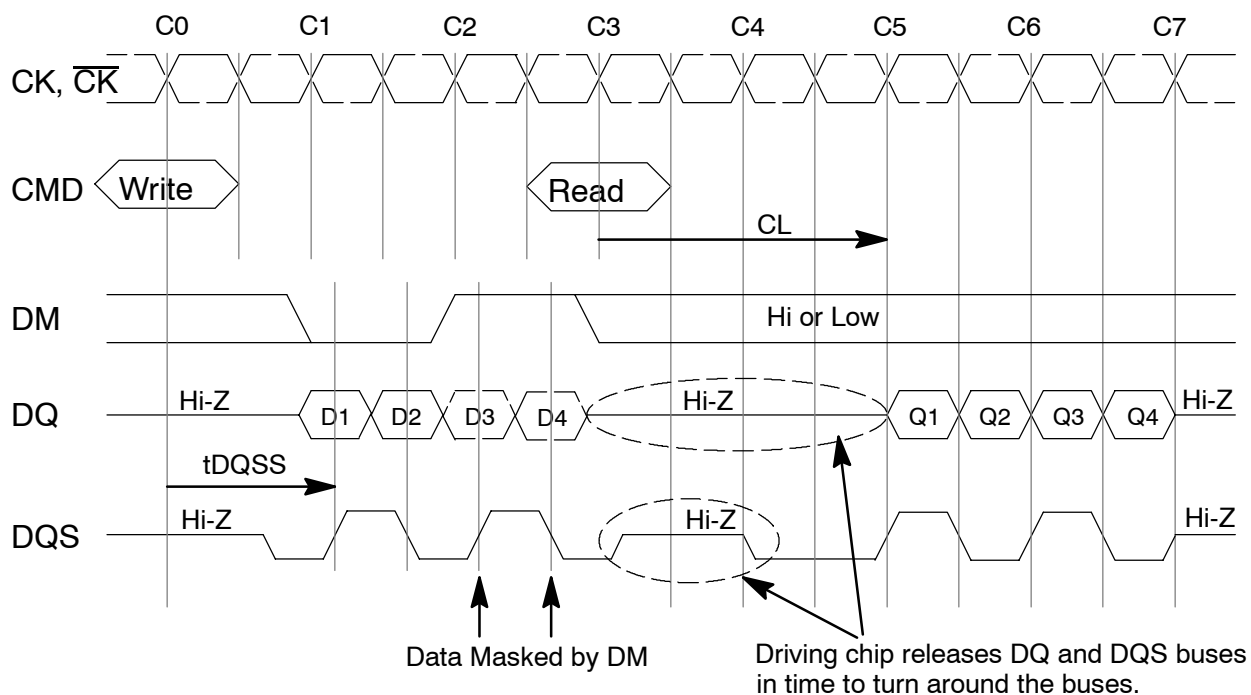
Figure 1: Read Interrupting a Write - Write to Read Delay = 1 Clock Cycle

3.11.5.2.3 (Cont) - Read Interrupting a Write Operation for DDR SDRAMs & SGRAMs



In this example, the Burst Length = 4 and the operations are not necessarily to the same bank.

Figure 2: Read Interrupting a Write - Write to Read Delay = 2 Clock Cycles



In this example, the Burst Length = 4 and the operations are not necessarily to the same bank.

Figure 3: Read Interrupting a Write - Write to Read Delay = 3 Clock Cycles

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = $RU(CL)$ [CL is the CAS Latency and RU means round up to the nearest integer]. Refer to Figures 1 and 2.
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

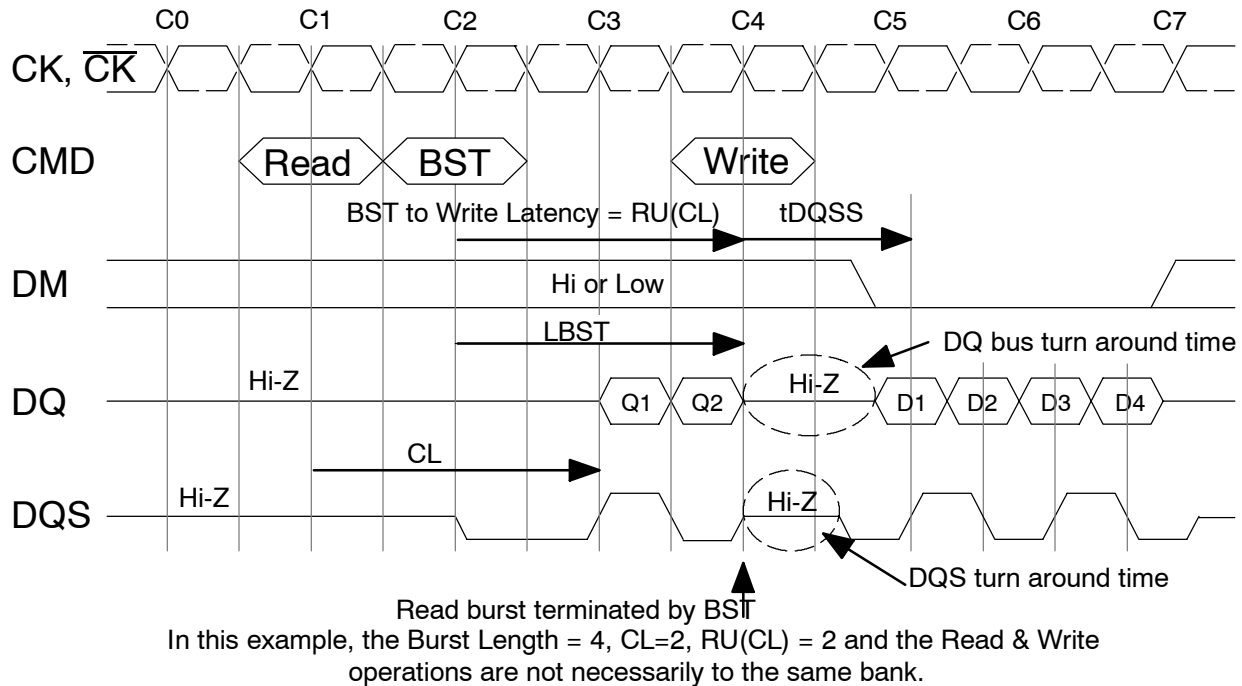


Figure 1: Write Interrupting a Read Burst ($\overline{CAS}$ Latency, CL , = X.0)

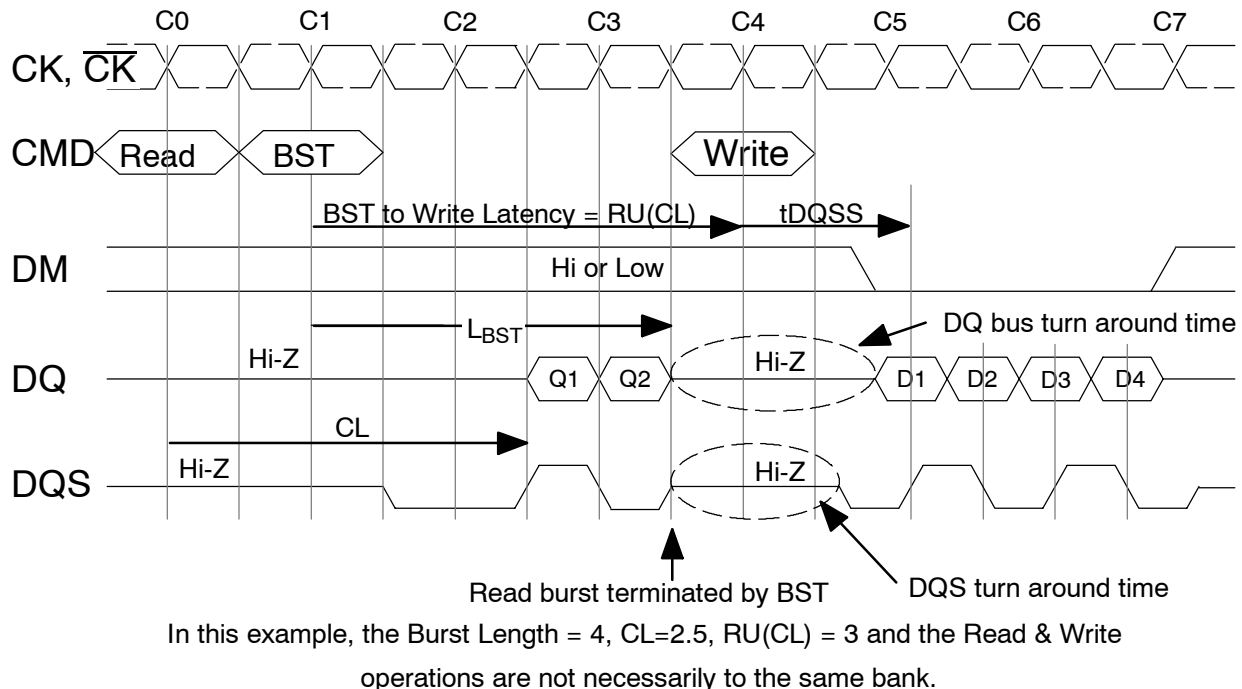


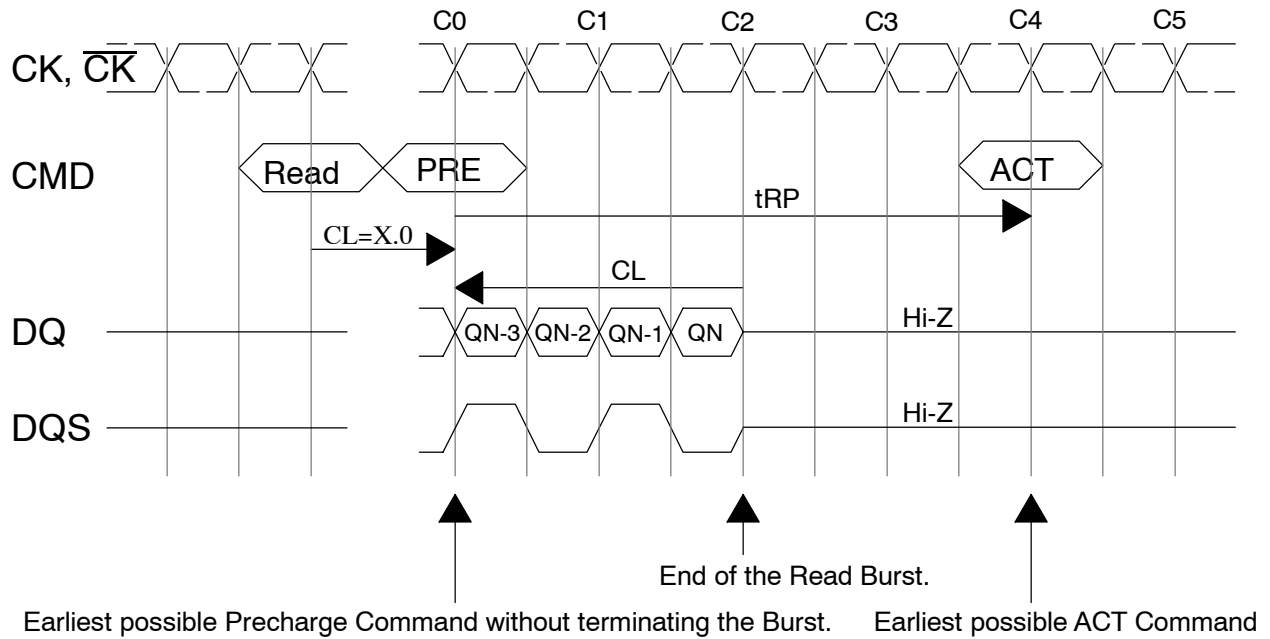
Figure 2: Write Interrupting a Read Burst ($\overline{CAS}$ Latency, CL , = X.5)

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

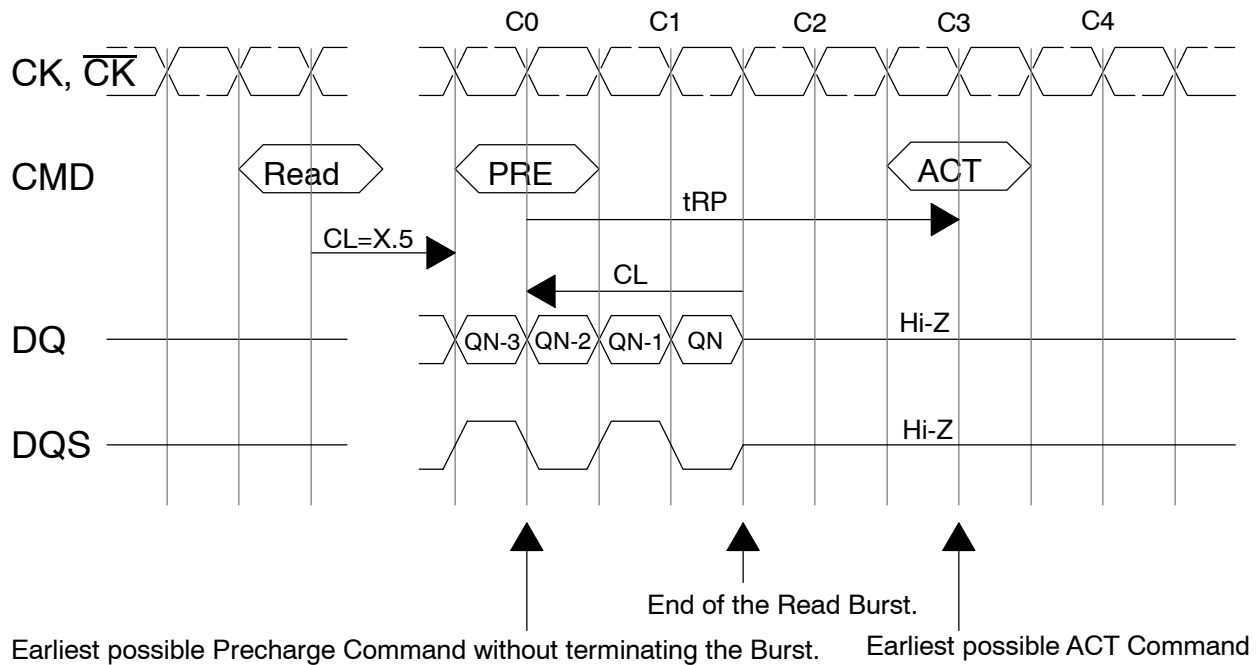
When a burst Read command is issued to a DDR SDRAM/SGRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{\text{CAS}}$ Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time). Refer to Figure 1.
3. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{\text{CAS}}$ Latency. Once the last data word has been output, the output buffers are set to the Hi-Z state. A new Bank Activate command may be issued to the same bank after tRP. Refer to Figure 2.
4. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP where tRP begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{\text{CAS}}$ Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above. Refer to Figure 3.
5. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a *rising* clock edge).
5. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

3.11.5.2.5 (cont) - Precharge Timing for Reads for DDR SDRAMs/SGRAMs



(A) Precharge Timing for Reads - Burst Not Interrupted - CL=X.0



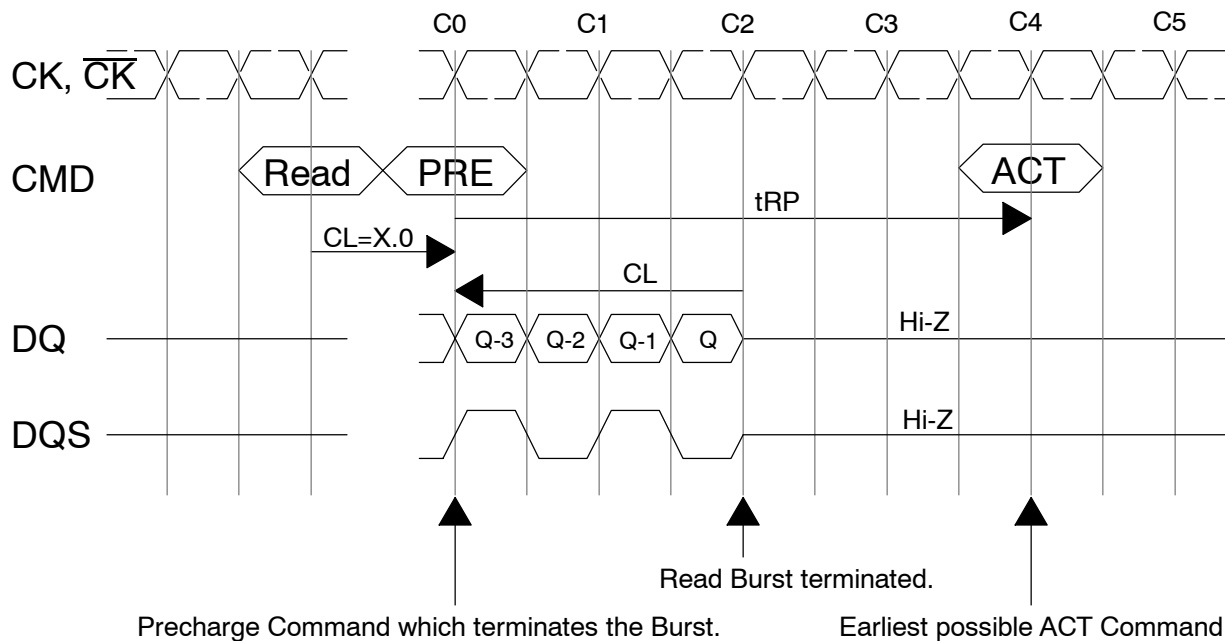
(B) Precharge Timing for Reads - Burst Not Interrupted - CL=X.5

In these examples, all operations are to the same bank.

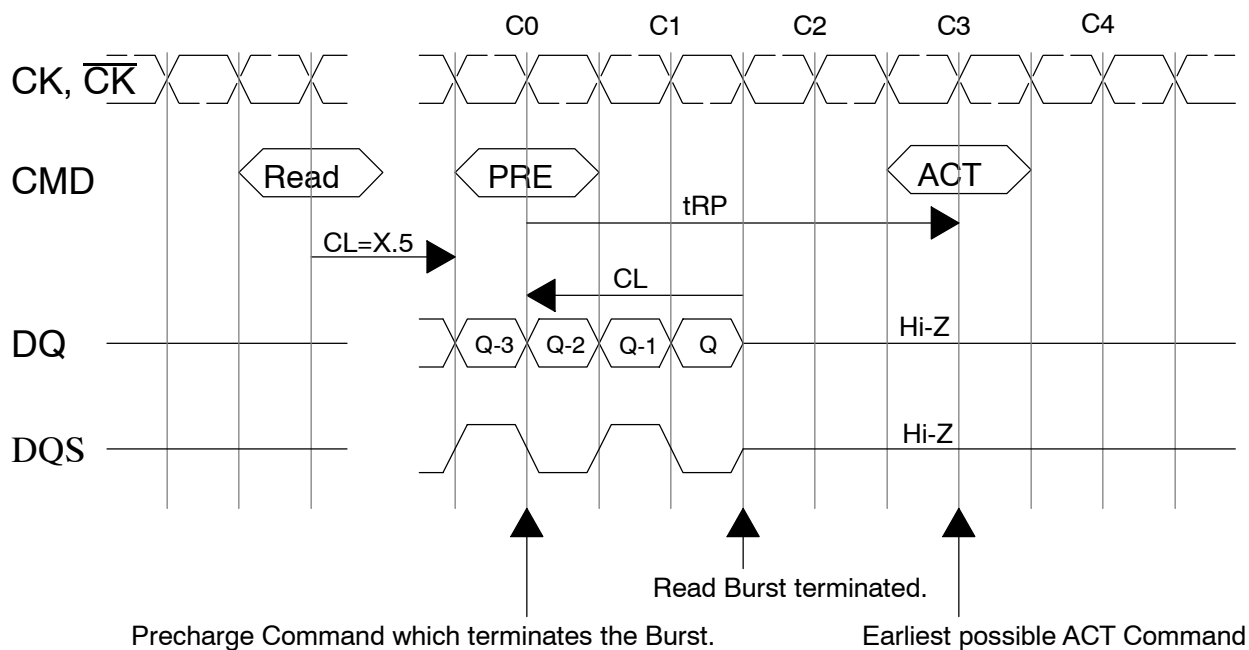
In these examples, the Burst Length=N (N=4 or 8, if N=2, only the last 2 data words shown are output).

Figure 1: Precharge Timing for Reads - Burst Not Interrupted

3.11.5.2.5 (cont) - Precharge Timing for Reads for DDR SDRAMs/SGRAMs



(A) Precharge Timing for Reads - Burst Interrupted - CL=X.0

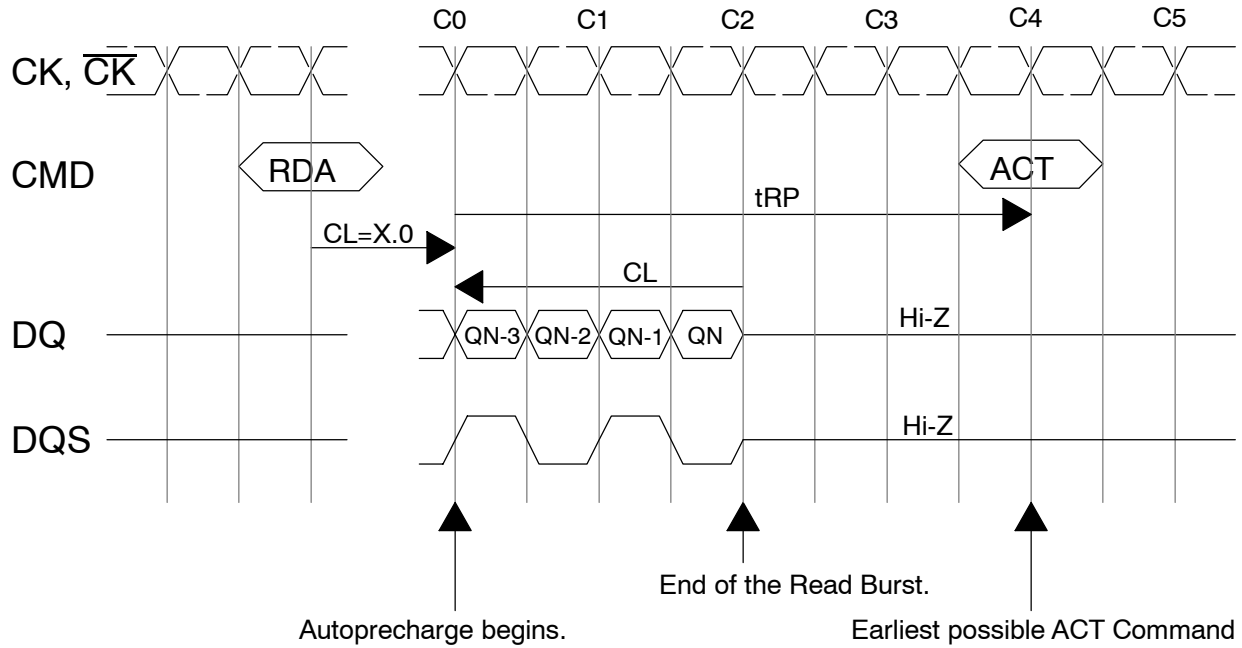


(B) Precharge Timing for Reads - Burst Interrupted - CL=X.5

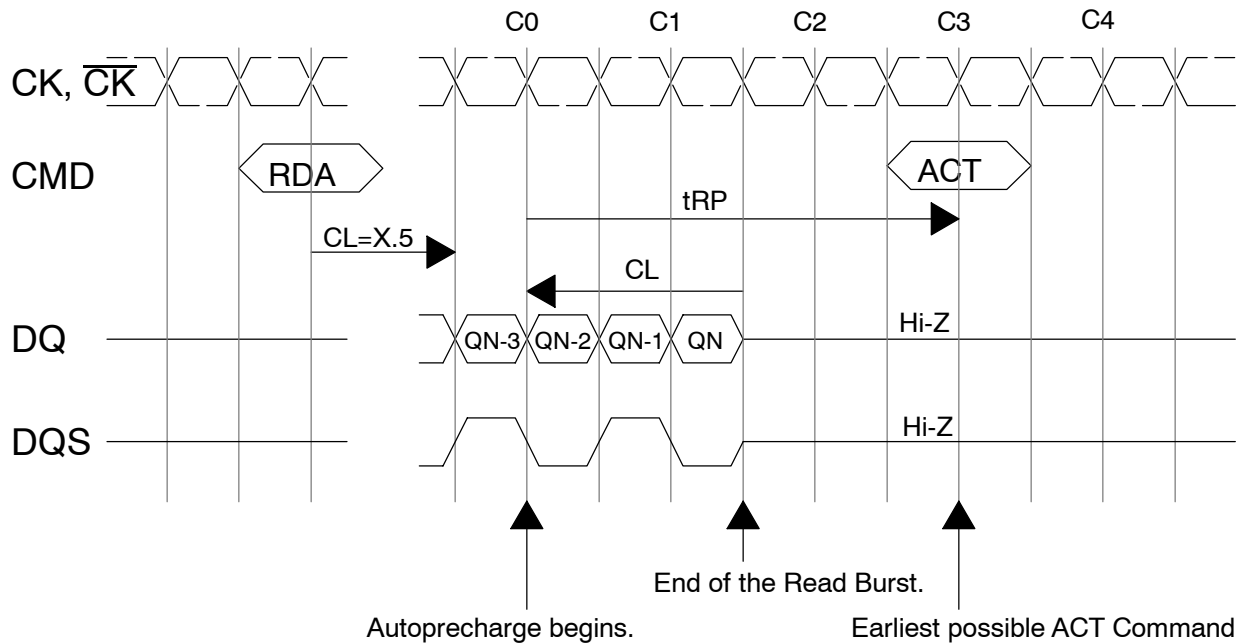
In these examples, all operations are to the same bank.
In these examples, the Burst Length=N (N=4 or 8).

Figure 2: Precharge Timing for Reads - Burst Interrupted

3.11.5.2.5 (cont) - Precharge Timing for Reads for DDR SDRAMs/SGRAMs



(A) Precharge Timing for Reads - Read with Autoprecharge - $CL=X.0$



(B) Precharge Timing for Reads - Read with Autoprecharge - $CL=X.5$

In these examples, all operations are to the same bank.

In these examples, the Burst Length= N ($N=4$ or 8 , if $N=2$, only the last 2 data words shown are output).

Figure 3: Precharge Timing for Reads - Read with Autoprecharge

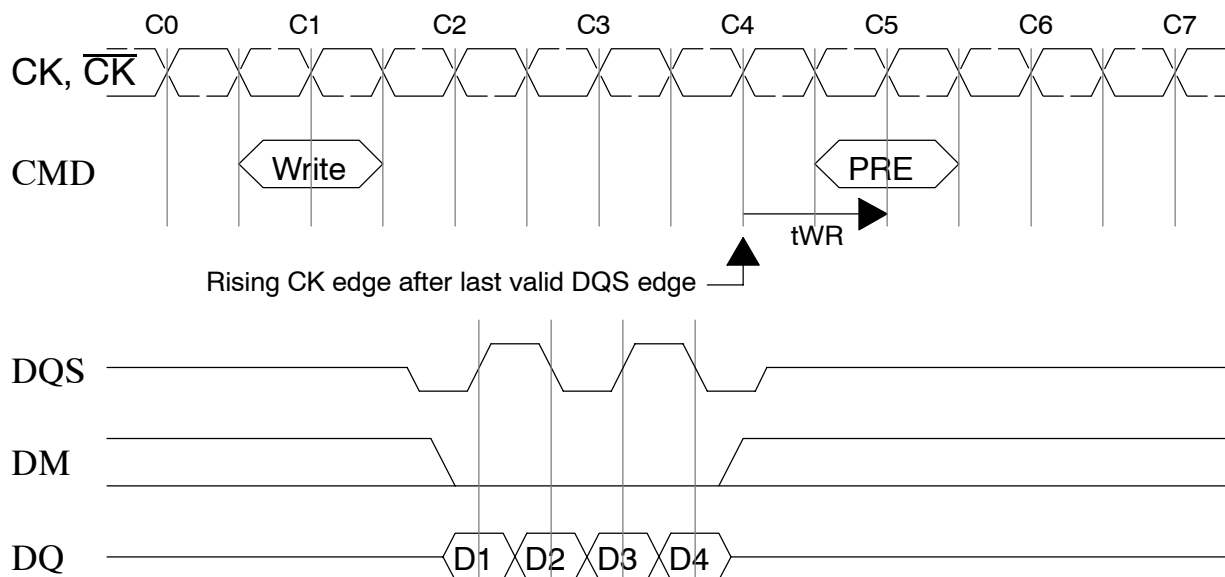
3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

Precharge timing for Write operations in DRAMs requires enough time to allow “write recovery” which is the time required by a DRAM core to properly store a full “0” or “1” level before a Precharge operation. For DDR SDRAM/SGRAM, a timing parameter, t_{WR} , is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the SDRAM/SGRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation, i.e., the input clock domain.

t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR} . Refer to Figure 1.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by t_{WR} . Refer to Figure 2.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after $t_{WR}+t_{RP}$ where $t_{WR}+t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above. Refer to Figure 3.
4. In all cases, a Precharge operation cannot be initiated unless $t_{RAS(min)}$ [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where $t_{RAS(min)}$ must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.



In this example, all operations are to the same bank.
In this example, the Burst Length = 4.

Figure 1: Precharge Timing for Writes - Burst Not Interrupted

3.11.5.2.6 (cont.) - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

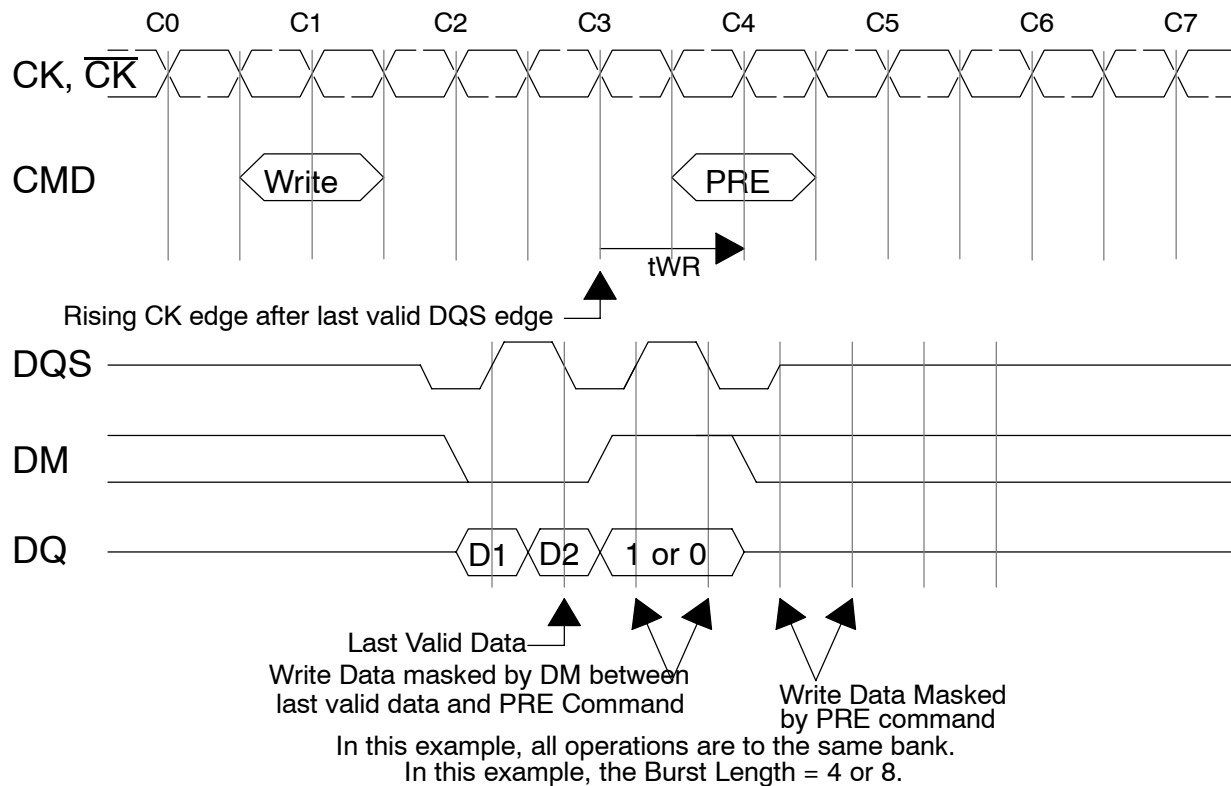


Figure 2: Precharge Timing for Writes - Burst Interrupted

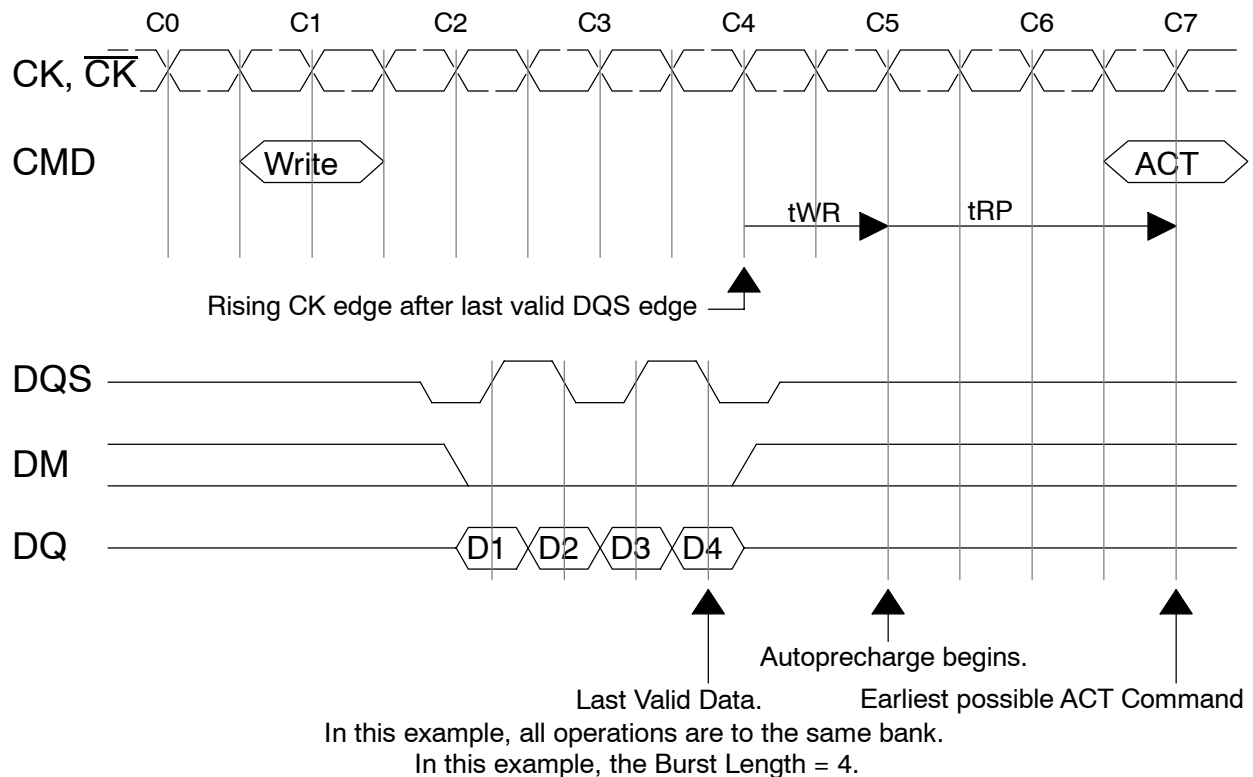


Figure 3: Precharge Timing for Writes - Write With Autoprecharge

3.11.5.2.7 - Burst Stop Command for DDR SDRAMs & SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is a mandatory feature for DDR SDRAMs/SGRAMs. The following functionality is required:

1. The BST command may only be issued on the rising edge of the input clock, CK.
2. BST is only a valid command during Read bursts.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} (“BST Latency”) clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations. This is shown in Figure 1 with examples for $\overline{CAS}$ latency (CL) of 1.5, 2, 2.5, 3 and 3.5 (only selected $\overline{CAS}$ latencies are required by the DDR SDRAM/SGRAM standards, the others are optional).
7. When the burst terminates, the DQ and DQS pins are set to a Hi-Z state.
8. The BST command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).
9. The Bank Addresses are don't care (i.e., high or low) on the clock edge that samples a Burst Stop Command

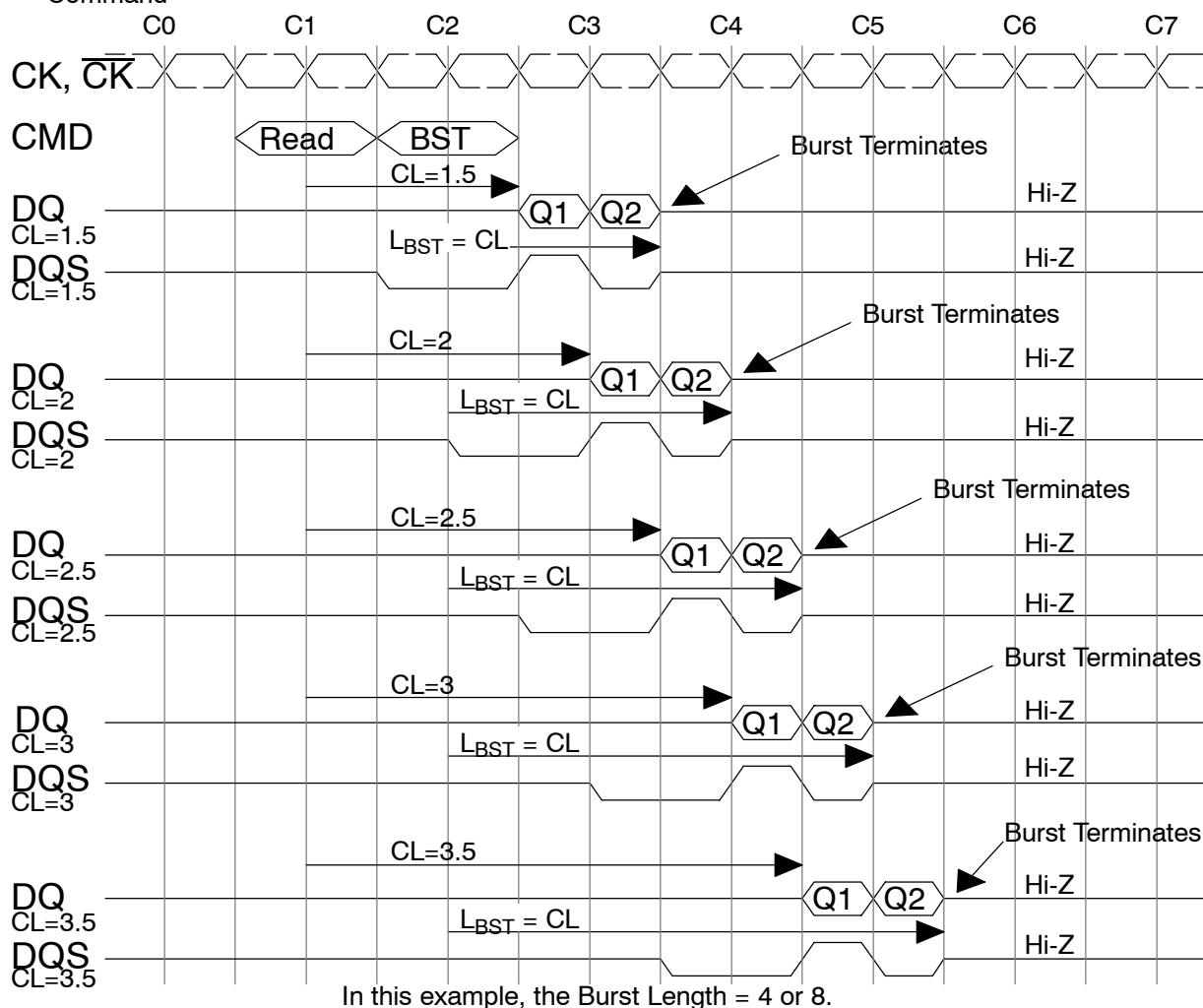


Figure 1: Terminating a DDR SDRAM/SGRAM Read Burst with BST

3.11.5.2.8 - DDR SDRAM & SGRAM Full Sequential Burst Ordering

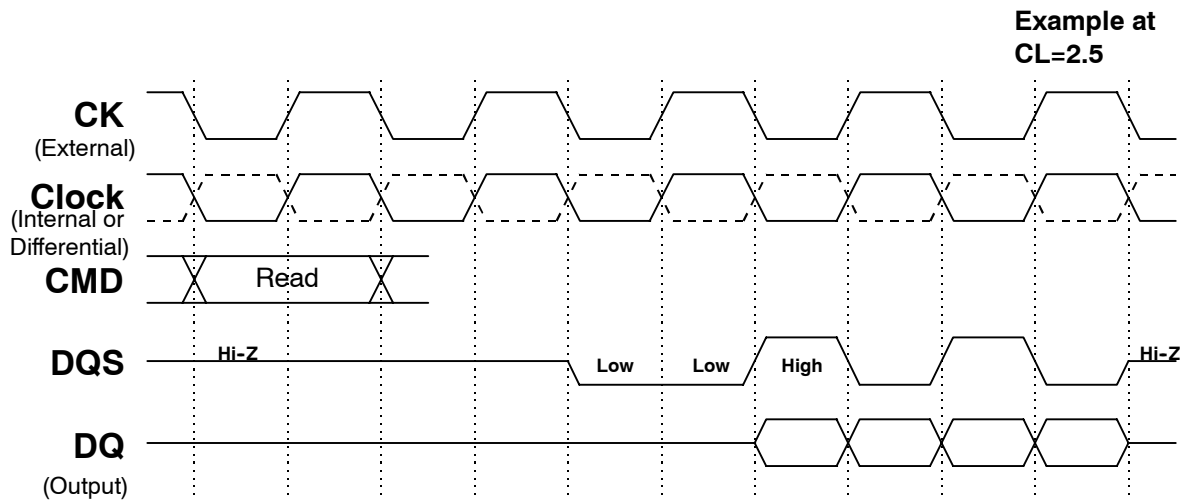
For DDR SDRAM & SGRAM, the following ordering is supported for sequential burst lengths (BL) of 2, 4, and 8:

BL = 2	BL = 4	BL = 8
0, 1	0, 1, 2, 3	0, 1, 2, 3, 4, 5, 6, 7
1, 0	1, 2, 3, 0	1, 2, 3, 4, 5, 6, 7, 0
	2, 3, 0, 1	2, 3, 4, 5, 6, 7, 0, 1
	3, 0, 1, 2	3, 4, 5, 6, 7, 0, 1, 2
		4, 5, 6, 7, 0, 1, 2, 3
		5, 6, 7, 0, 1, 2, 3, 4
		6, 7, 0, 1, 2, 3, 4, 5
		7, 0, 1, 2, 3, 4, 5, 6

The numbers in the tables are the decimal equivalents of the LSBs (1 bit for BL=2, 2 bits for BL=4, & 3 bits for BL=8) of the Y - address.

3.11.5.2.9 - DDR DQS Coincident with Data

The signal DQS shall be coincident with Read Data from the DDR SDRAM device. The timing diagram below shows the nominal relationship between data and DQS for read data at the output of the DDR SDRAM devices.



3.11.5.2.10 - Extended Mode Register Set (EMRS) for DDR SDRAM/SGRAM

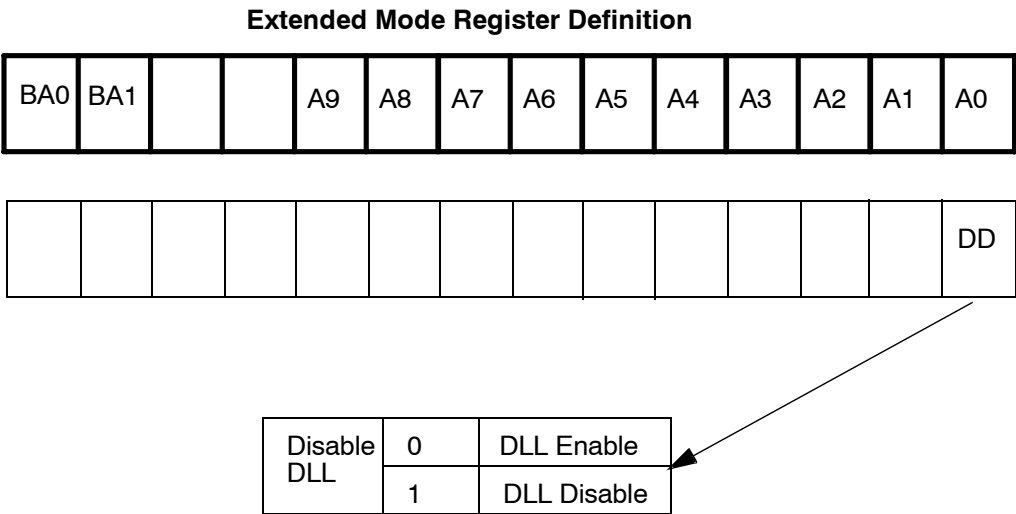
- Extended mode register address space is provided by defining non-zero Bank address(s) for accesses that otherwise conform to the Mode Register Set (MRS) cycle. These Extended Mode Register Set cycles (EMRS) can be implemented as needed for function extensions to the standard.
- The EMRS is required for DDR SDRAM.
- All address bits are reserved at zero until defined and used for extended functions.
- The Extended Mode Register is independent of any MRS cycle.
- BA2 and BA1 may not be implemented on all designs. If these two Bank Address bits are not available, then there is no additional expansion beyond EMRS possible for those devices.

Extended Mode Register Address Space			
BA0	BA1	BA2	An - A0
0	0	0	(Existing) MRS Cycle
1	0	0	Extended Functions (EMRS)
X	1	0	Reserved For Future (EMRSn)
X	X	1	Reserved For Future

NOTE: The uses and functions defined by the address bits are or will be covered in separate Standards

3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS

The following defines the DLL disable/enable bit in the Extended Mode Register:



3.11.5.2.12 - REFRESH REQUIREMENTS

DDR SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 256 Mb DDR SDRAM has 8192 rows resulting in a tREFI of 7.8 ms.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS-BEFORE-RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of tREFI (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is $8 * tREFI$.

SELF REFRESH

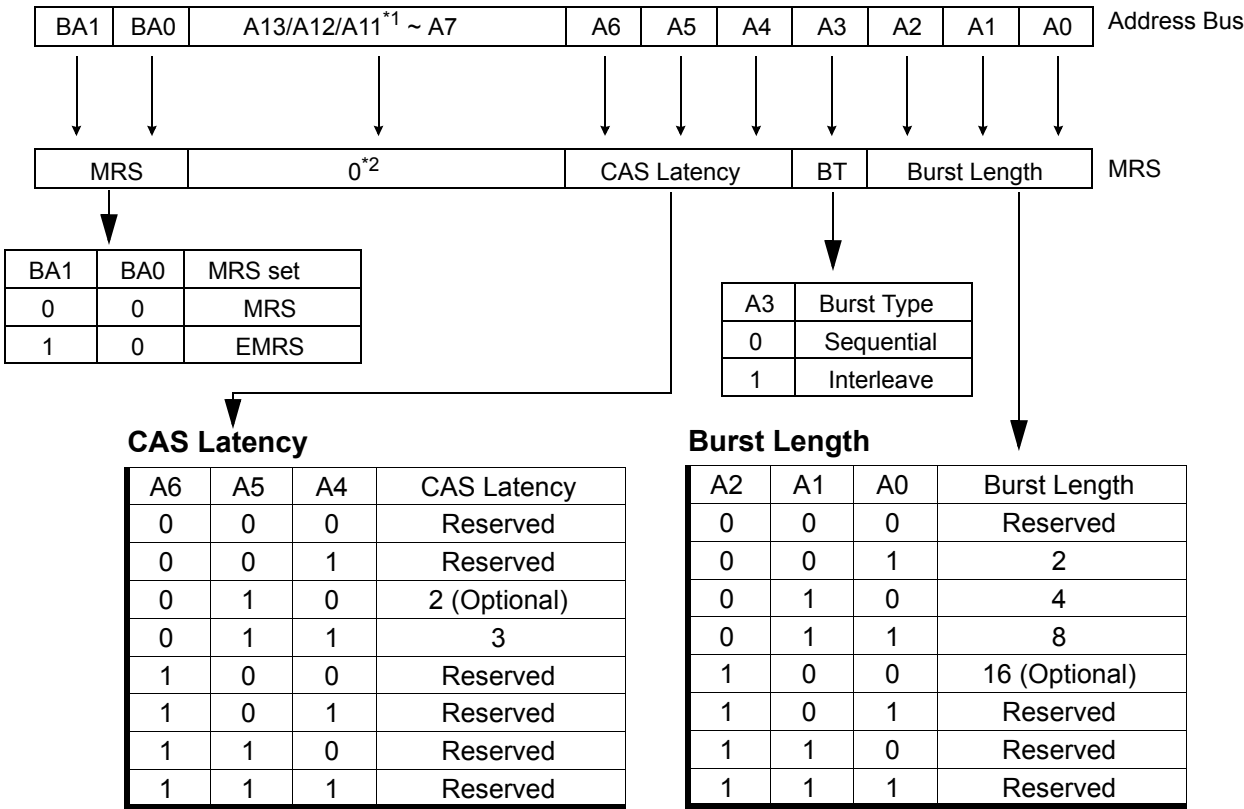
The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSC because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is not required.

3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM

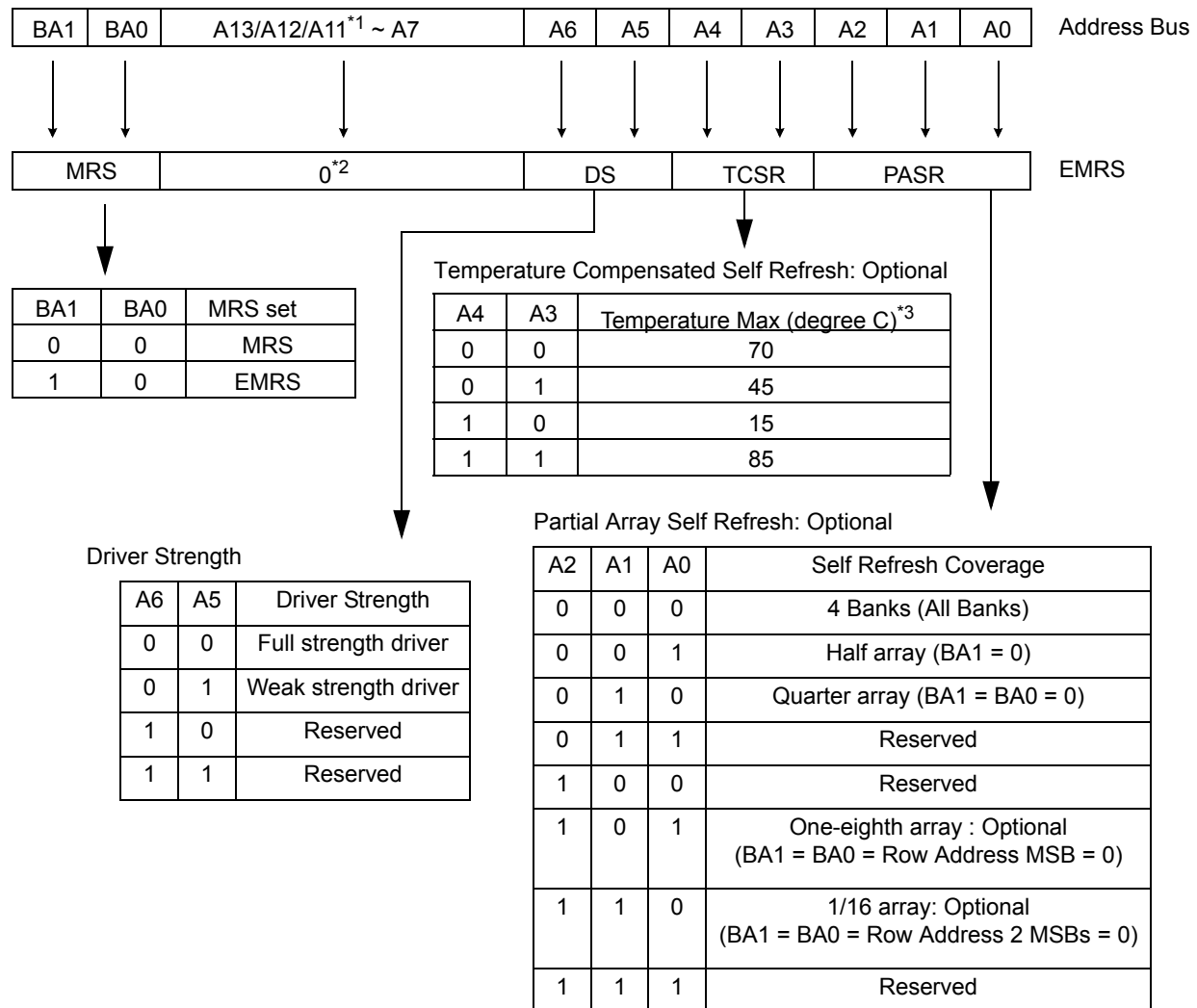
Mode Register Set(MRS) for Low Power DDR SDRAM



* 1 : MSB depends on Low Power SDRAM density
* 2 : A logic 0 should be programmed to all unused / undefined address and bank address bits to ensure future compatibility

3.11.5.2.13 (Cont) - MRS/EMRS for Low Power DDR SDRAM

Extended Mode Register Set(EMRS) for Low Power DDR SDRAM



* 1 : MSB depends on Low Power SDRAM density

* 2 : A logic 0 should be programmed to all unused / undefined address and bank address bits to ensure future compatibility

* 3 : Temperatures specified for the TCSR feature are Case temperatures

Definitions:

Temperature Compensated Self Refresh (TCSR)

Programmable refresh rate for self refresh mode to allow the system to control power as a function of temperature

Partial Array Self Refresh (PASR)

Programmable memory array size to be refreshed during self refresh operation to reduce power. Data outside the defined area will not be retained during self refresh

3.11.5.3 – Enhanced SDRAM (ESDRAM) Specific SDRAM Functions

The Standards in this section are special functions that are applicable to Enhanced SDRAM (ESDRAM). The standards cover both SDR and DDR devices as stated on the individual Standards.

3.11.5.3.1 – Read-AutoPrecharge Operation for SDR ESDRAM

In the Enhanced SDRAM (ESDRAM), a Read-Autoprecharge command will initiate multiple functions. This standard defines those functions.

3.11.5.3.2 – Read-AutoPrecharge Operation for DDR ESDRAM

In the DDR Enhanced SDRAM (DDR ESDRAM), a Read-Autoprecharge command will initiate multiple functions. This standard defines those functions.

3.11.5.3.3 – Cache Load Operation for SDR ESDRAM

In the Enhanced SDRAM (ESDRAM), a Cache Load command will initiate multiple functions. This standard defines those functions.

3.11.5.3.4 – Cache Load Operation for DDR ESDRAM

In the DDR Enhanced SDRAM (DDR ESDRAM), a Cache Load command will initiate multiple functions. This standard defines those functions.

3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM

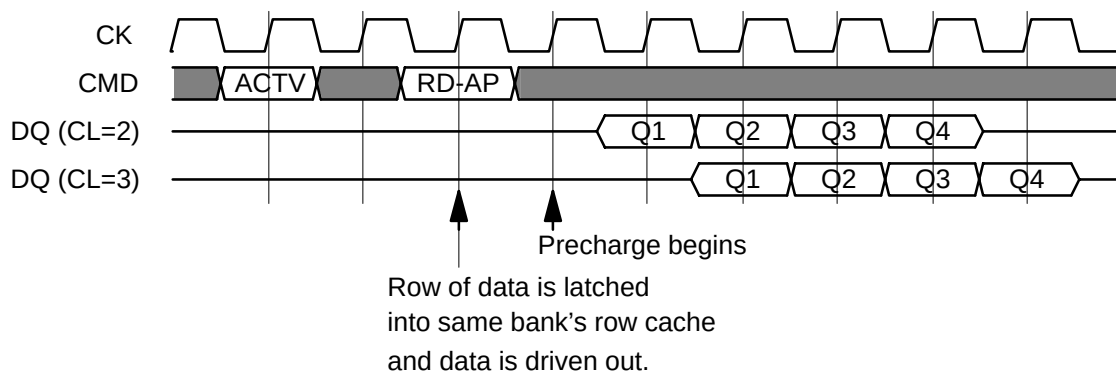
“No Write Transfer” mode is an optional mode of operation that allows an Enhanced SDRAM (ESDRAM) to concurrently keep a read page and a write page open per bank. This Standard defines the details of this operational mode.

3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM

“No Write Transfer” mode is an optional mode of operation that allows a DDR Enhanced SDRAM (DDR ESDRAM) to concurrently keep a read page and a write page open per bank. This Standard defines the details of this operational mode.

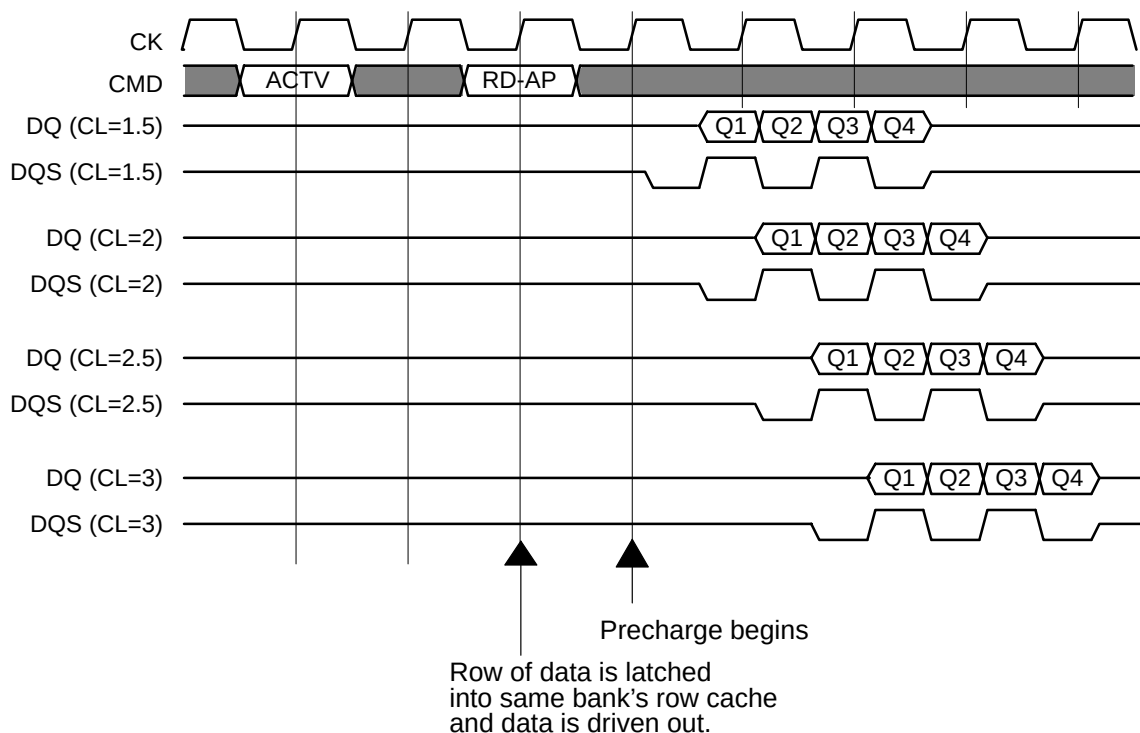
3.11.5.3.1 – Read-Auto Precharge Operation for SDR ESDRAM

The Enhanced SDRAM (ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read-Autoprecharge command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank, and begin the precharge one clock cycle following the Read Autoprecharge command independent of the burst length. In the diagram below, a 4-word burst is shown.



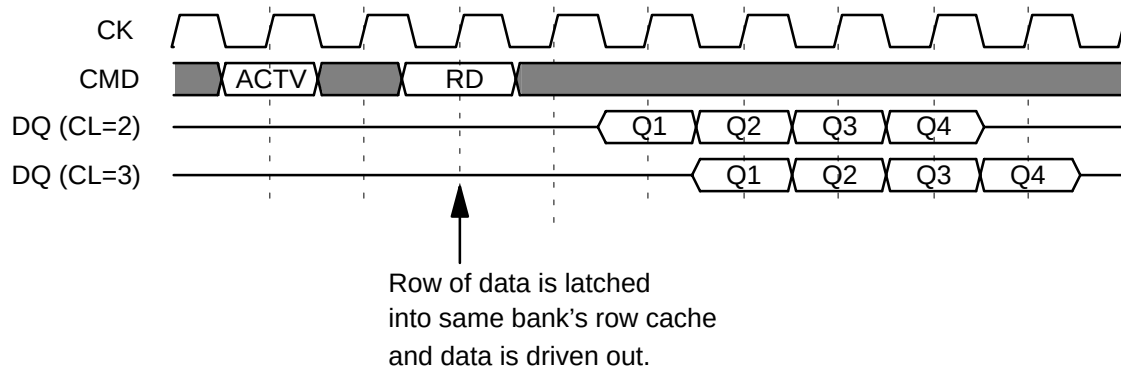
3.11.5.3.2 – Read-Auto Precharge Operation for DDR ESDRAM

The DDR Enhanced SDRAM (DDR ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read-Autoprecharge command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank, and begin the precharge one clock cycle following the Read Autoprecharge command independent of the burst length. In the diagram below, a 4-word burst is shown.



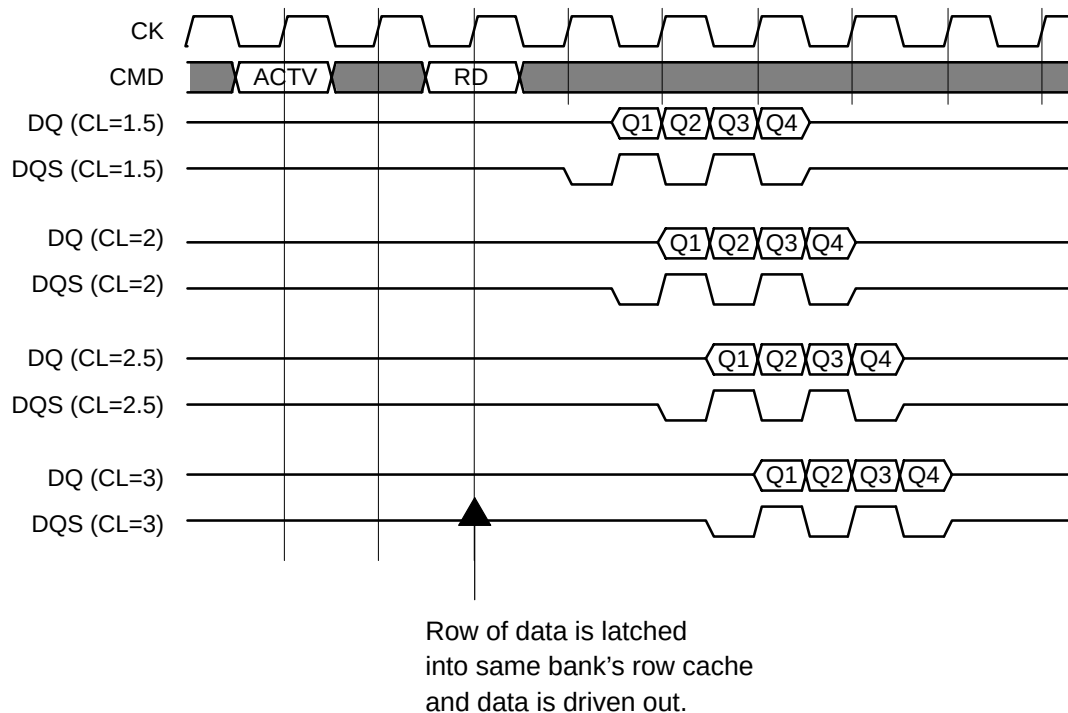
3.11.5.3.3 – Cache Load Operation for SDR ESDRAM

The Enhanced SDRAM (ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank. In the diagram below, a 4-word burst is shown.



3.11.5.3.4 – Cache Load Operation for DDR ESDRAM

The DDR ESDRAM integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read command will initiate a read (burst length defined by the Mode Register) and load the row cache with the contents of the sense amp data from the addressed row of the selected active bank. In the diagram below, a 4-word burst is shown. Although half-clock preamble is shown, it is not a requirement of this proposal.



3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM

“No Write Transfer” mode is an optional mode of operation that allows an Enhanced SDRAM (ESDRAM) to concurrently keep a read page and a write page open per bank. This mode must be entered via an MRS command to the Mode Register by setting the A9 bit to 1.

In “No Write Transfer” mode of operation, the ESDRAM will write only to the DRAM and not the cache in the case of a write page miss, i.e. the row address intended for the write data does not match the previously loaded read page row address. In the case of a write page hit, both the DRAM and the cache are written to maintain coherency. To illustrate the advantages of this mode, the timing diagram above shows same bank operations since fast alternate bank operations can be achieved with standard SDRAM. In the diagram above, a 4-word burst is shown.

Actions Taken within the ESDRAM in No Write Transfer mode (per bank)						
Command		Row Cache	DRAM	Row Addr reg	Tag	NewPage flag
ACTV		-	-	Load with current address	No change	Set to 1
Read, Read-AP (NewPage = 1)		Load Cache	-	-	Load with Row Addr reg value	Set to 0
Read, Read-AP (NewPage = 0)		No change	-	-	No change	-
Read, Read-AP (Page Closed)		No change	-	-	No change	Set to 0
Write (Hit) (RowAddr = tag)		Updated	Updated	-	No change	Set to 0
Write (Miss) (RowAddr ≠ tag)		No change	Updated	-	No change	Set to 0

Internal to an ESDRAM are two registers per bank that hold row address information for comparison purposes. A Row Addr register is loaded on a bank activate command and a row address tag is loaded to track what is loaded into the row cache. Also, a one-bit NewPage flag is used only to determine whether to perform a cache load on a read command.

3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM (cont.)

The following describe the numbered events in the timing diagram below:

1. The ESDRAM is commanded to perform a Bank Activate. The ESDRAM performs a bank address decode, row address decode, and data is developed in the sense amplifiers exactly like a standard SDRAM. In addition, the ESDRAM loads the current row address into the internal Row Addr register and compares the current row address (in the case shown above, row address = x or y) with the internal tag. The compare result is subsequently used during Write cycles. The ESDRAM also sets an internal NewPage flag.
2. The ESDRAM performs a read, in this case a Read-AP in order to quickly close the read page. If the NewPage flag is set, the row cache is loaded, the current row address is loaded into an internal address tag, and the NewPage flag is subsequently reset. If the NewPage flag is reset, the row cache remains unchanged, and the tag is left unchanged.
3. If a Write or Write-AP command is issued and the current row address does not match the address tag, the ESDRAM performs a write to the DRAM and not to the row cache. The NewPage flag is then reset. If a Write or Write-AP command is issued and the current row address matches the address tag, the ESDRAM performs a write to the DRAM and the row cache. The NewPage flag is then reset.
4. The ESDRAM performs a Read. If the NewPage flag is reset, the chip does not load the cache with the sense amp contents (row y in the diagram above) and drives out the previously loaded row cache data. If the NewPage flag is set, the chip loads the cache with the sense amp contents and drives out the newly loaded row cache data.
5. This case is not shown in the timing diagram, but consider it a case that follows #2 and prior to the 2nd Activate. If a Write or Write-AP command is issued and the current row address matches the address tag, the ESDRAM performs a write to the DRAM and not to the row cache. If a Write or Write-AP command is issued and the current row address matches the Row Addr register, the ESDRAM performs a write to the DRAM and the row cache.

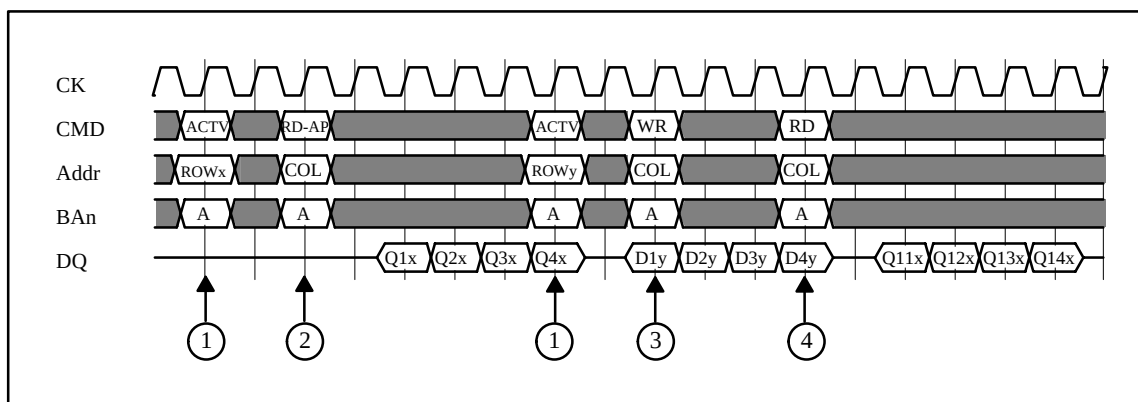


Figure 1, SDR ESDRAM “No Write Transfer” Mode of Operation

3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM

“No Write Transfer” mode is an optional mode of operation that allows a DDR Enhanced SDRAM (DDR ESDRAM) to concurrently keep a read page and a write page open per bank. This mode is entered via an EMRS command to the Mode Register by setting the A9 bit to 1.

In “No Write Transfer” mode of operation, the DDR ESDRAM will write only to the DRAM and not the cache in the case of a write page miss, i.e. the row address intended for the write data does not match the previously loaded read page row address. In the case of a write page hit, both the DRAM and the cache are written to maintain coherency. To illustrate the advantages of this mode, the timing diagram above shows same bank operations since fast alternate bank operations can be achieved with standard DDR SDRAM. In the diagram above, a 4-word burst is shown.

Actions Taken within the DDR ESDRAM in No Write Transfer mode (per bank)					
Command	Row Cache	DRAM	Row Addr reg	Tag	NewPage flag
ACTV (NewPage = 0)	-	-	Load with current address	No change	Set to 1
Read, Read-AP (NewPage = 1)	Load Cache	-	-	Load with Row Addr Reg Value	Set to 0
Read, Read-AP (NewPage = 0)	No change	-	-	No change	-
Read, Read-AP (Page Closed)	No change	-	-	No change	Set to 0
Write (Hit) (RowAddr = tag)	Updated	Updated	-	No change	Set to 0
Write (Miss) (RowAddr ≠ tag)	No change	Updated	-	No change	Set to 0

Internal to the DDR ESDRAM are two registers per bank that hold row address information for comparison purposes. A Row Addr register is loaded on a bank activate command and a row address tag is loaded to track what is loaded into the row cache. Also, a one-bit NewPage flag is used only to determine whether to perform a cache load on a read command.

3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM (cont.)

The following describe the numbered events in the timing diagram below in Figure 1:

1. The DDR ESDRAM is commanded to perform a Bank Activate. The DDR ESDRAM performs a bank address decode, row address decode, and data is developed in the sense amplifiers exactly like a standard DDR SDRAM. In addition, the DDR ESDRAM loads the current row address into the internal Row Addr register and compares the current row address (in the case shown above, row address = x or y) with the internal tag. The compare result is subsequently used during Write cycles. The DDR ESDRAM also sets an internal NewPage flag.
2. The DDR ESDRAM performs a read, in this case a Read-AP in order to quickly close the read page. If the NewPage flag is set, the row cache is loaded, the current row address is loaded into an internal address tag, and the NewPage flag is subsequently reset. If the NewPage flag is reset, the row cache remains unchanged, and the tag is left unchanged.
3. If a Write or Write-AP command is issued and the current row address does not match the address tag, the DDR ESDRAM performs a write to the DRAM and not to the row cache. The NewPage flag is then reset. If a Write or Write-AP command is issued and the current row address matches the address tag, the DDR ESDRAM performs a write to the DRAM and the row cache. The NewPage flag is then reset.
4. The DDR ESDRAM performs a Read. If the NewPage flag is reset, the chip does not load the cache with the sense amp contents (row y in the diagram above) and drives out the previously loaded row cache data. If the NewPage flag is set, the chip loads the cache with the sense amp contents and drives out the newly loaded row cache data.
5. This case is not shown in the timing diagram, but consider it a case that follows #2 and prior to the 2nd Activate. If a Write or Write-AP command is issued and the current row address matches the address tag, the DDR ESDRAM performs a write to the DRAM and not to the row cache. If a Write or Write-AP command is issued and the current row address matches the Row Addr register, the DDR ESDRAM performs a write to the DRAM and the row cache.

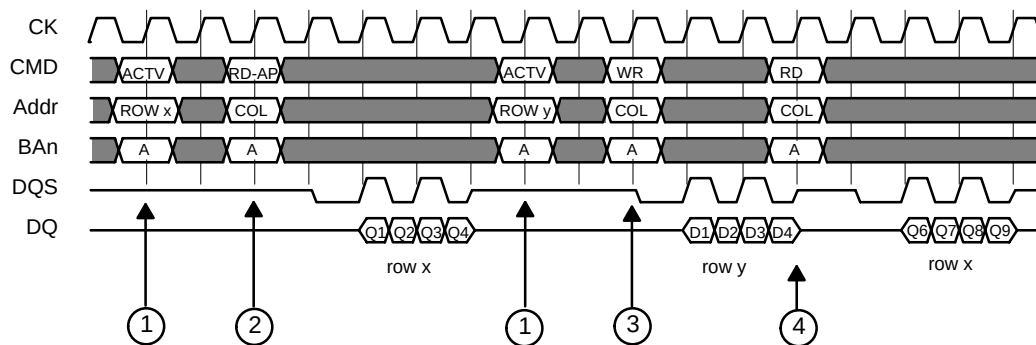


Figure 1, DDR ESDRAM “No Write Transfer” Mode of Operation

3.11.5.4 – VCSDRAM Specific SDRAM Functions

The Standards in this section are special functions that are applicable to Virtual Channel SDRAM (VCSDRAM). The standards cover both SDR and DDR devices as stated on the individual Standards.

3.11.5.4.1 – Command Table for Virtual Channel SDR SDRAM

3.11.5.4.2 – Command Table for Virtual Channel DDR SDRAM

3.11.5.4.3 – Virtual Channel SDR SDRAM Mode Register Architecture

3.11.5.4.4 – Virtual Channel DDR SDRAM Mode Register Architecture

3.11.5.4.1 – Command Table for Virtual Channel SDR SDRAM

COMMAND	SYMBOL	CKE		S	RAS	CAS	WE	BA	A12	A11	A10 /AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		n–1	n																		
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Prefetch without/with auto precharge	PFC/PFCA	H	X	L	H	H	L	BA	CHA	CHA	PS	CHA	L	L	L	L	X	X	X	SGA	SGA
Pair Prefetch without/with auto precharge	PPF/PPFA	H	X	L	H	H	L	BA	CHA	CHA	PS	CHA	L	L	L	L	X	X	X	SGA	SGA
Prefetch to Dummy	PFD	H	X	L	H	H	L	BA	X	X	X	X	X	L	L	L	X	X	X	SGA	SGA
Restore without/with Auto Precharge	RST/RSTA	H	X	L	H	H	L	BA	CHA	CHA	PS	CHA	L	H	L	X	X	X	X	SGA	SGA
Precharge Selected Bank	PRE	H	X	L	H	H	L	BA	X	X	L	X	X	H	H	X	X	X	X	X	X
Precharge All Banks	PALL	H	X	L	H	H	L	X	X	X	H	X	X	H	H	X	X	X	X	X	X
Channel Read	READ	H	X	L	H	L	H	X	CHA	CHA	X	CHA	L	L	L	L	X	X	X	CA	CA
Channel Write	WRIT	H	X	L	H	L	L	L	CHA	CHA	X	CHA	L	L	L	X	X	X	X	CA	CA
Dummy Channel Write without/with Auto Restore	WRD/ WRDA	H	X	L	H	L	L	H	X	X	X	X	R	S	L	L	L	L	L	CA	CA
Bank Activate	ACT	H	X	L	L	H	H	BA	L	L	L	L	L	L	L	L	L	L	L	L	L
Prefetch Read with Auto Precharge (optional)	PFR	H	X	L	L	H	L	SGA	CHA	CHA	SGA	CHA	L	L	L	L	L	L	L	L	L
Self Register Operation	MRS	H	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BT	BL

REMARKS

H: High Level L: Low Level X: High or Low Level (Don't Care)

PS: Auto Precharge Select (H: with auto precharge, L: without auto precharge)

RS: Auto Restore Select (H: with auto restore, L: without auto restore) BA: Bank Address

RA: Row Address CA: Column Address CHA: Channel Address SGA: Segment Address

CL: CAS Latency BT: Burst Type BL: Burst Length TM: Test Mode Entry

NOTE:

Prefetch Read with Auto Precharge Command is optional

3.11.5.4.1– Command Table for Virtual Channel SDR SDRAM

3.11.5.4.2 – Command Table for Virtual Channel DDR SDRAM

COMMAND	SYMBOL	CKE		S	RAS	CAS	WE	BA	A12	A11	A10 /AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0			
		n-1	n																					
Device Deselect	DESL	H	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
No Operation	NOP	H	X	L	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
Prefetch without/with auto precharge	PFC/PFCA	H	X	L	H	H	L	BA	CHA	PS	PS	CHA	CHA	L	L	L	X	X	X	SGA	SGA			
Pair Prefetch without/with auto precharge	PPF/PPFA	H	X	L	H	H	L	BA	CHA	CHA	PS	CHA	CHA	L	H	X	X	X	X	SGA	SGA			
Prefetch to Dummy	PFD	H	X	L	H	H	L	BA	X	X	X	X	X	L	L	H	X	X	X	SGA	SGA			
Restore without/with Auto Precharge	RST/RSTA	H	X	L	H	H	L	BA	CHA	PS	PS	CHA	CHA	H	L	X	X	X	X	SGA	SGA			
Precharge Selected Bank	PRE	H	X	L	H	H	L	BA	X	X	L	X	X	H	H	X	X	X	X	X	X			
Precharge All Banks	PALL	H	X	L	H	H	L	X	X	X	H	X	X	H	H	X	X	X	X	X	X			
Channel Read	READ	H	X	L	H	L	H	X	CHA	CHA	X	CHA	CHA	CA										
Channel Write	WRIT	H	X	L	H	L	L	L	CHA	CHA	X	CHA	CHA	CA										
Dummy Channel Write without/with Auto Restore	WRD/WRDA	H	X	L	H	L	L	H	X	X	X	X	RS	CA										
Bank Activate	ACT	H	X	L	L	H	H	BA	RA															
Prefetch Read with Auto Precharge (optional)	PFR	H	X	L	L	H	L	SGA	CHA	CHA	SGA	CHA	CHA	CA										
Set Register Operation	MRS	H	X	L	L	L	L	L	L	L	L	L	DR	TM	CL		BT	BL			DD			
	EMRS	H	X	L	L	L	L	H	L	L	L	L	Reserved for future use											

REMARKS

H: High Level L: Low Level X: High or Low Level (Don't Care)

PS: Auto Precharge Select (H: with auto precharge, L: without auto precharge)

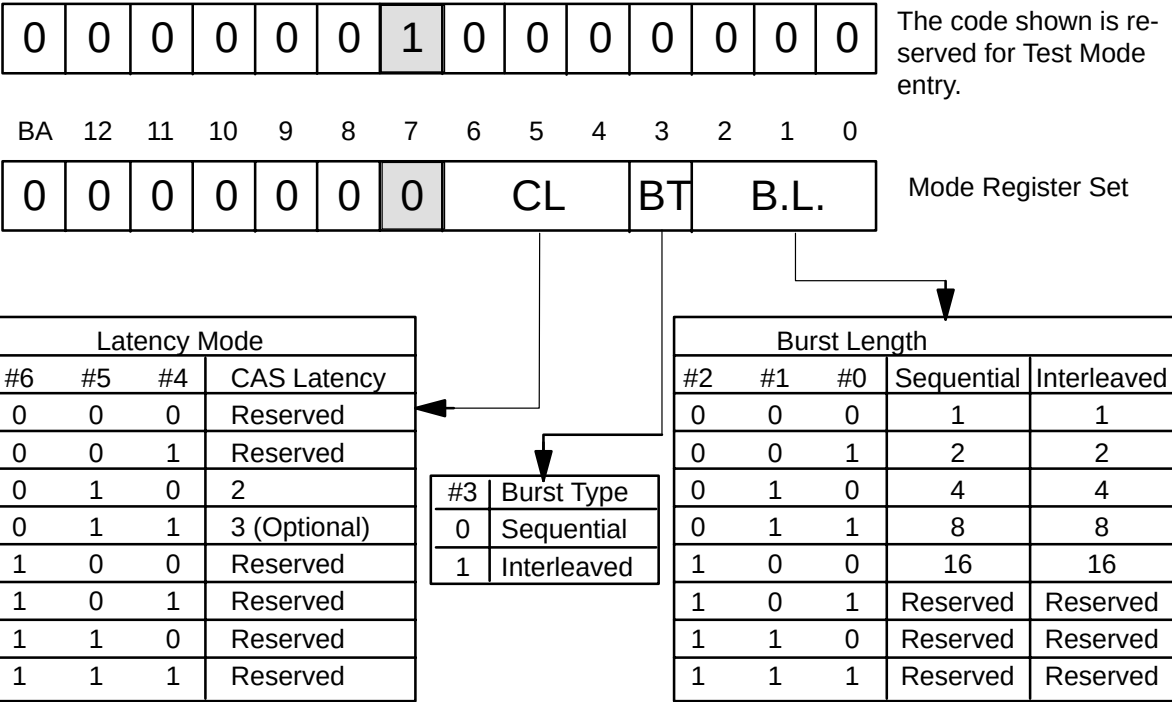
RS: Auto Restore Select (H: with auto restore, L: without auto restore) BA: Bank Address

RA: Row Address CA: Column Address CHA: Channel Address SGA: Segment Address

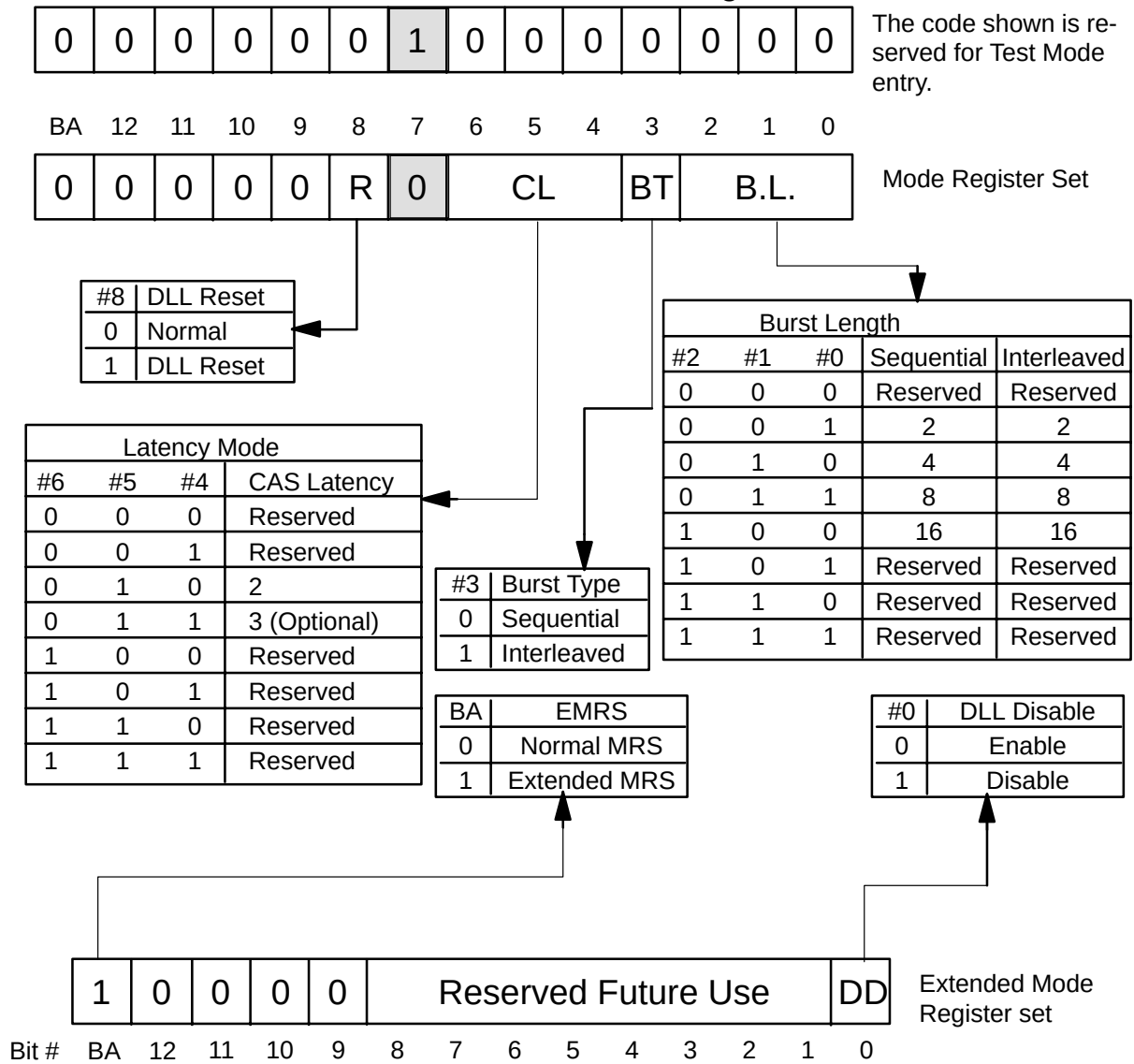
CL: CAS Latency BT: Burst Type BL: Burst Length TM: Test Mode Entry

NOTE: Prefetch Read with Auto Precharge Command is optional

3.11.5.4.3 – Virtual Channel SDR SDRAM Mode Register Architecture



3.11.5.4.4 – Virtual Channel DDR SDRAM Mode Register Architecture



3.11.5.5 – DDR2 Specific SDRAM Functions

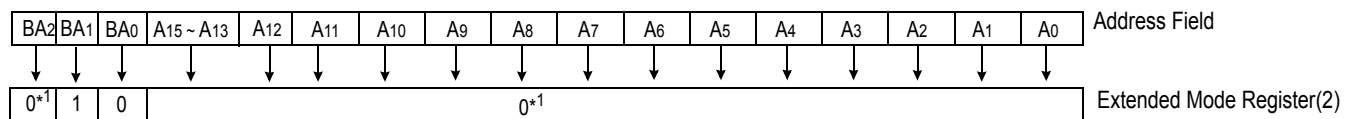
DDR2 SDRAM EMRS2 and EMRS3

For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/Extended Mode Register Set commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

Notes:

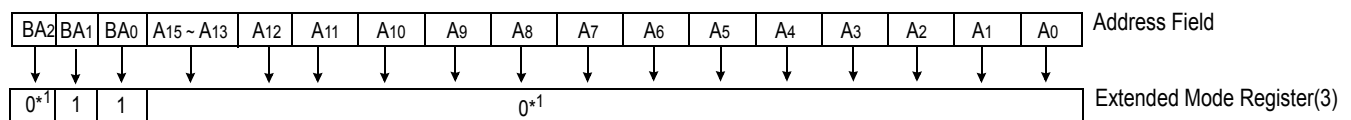
1. Background: This is to ensure future compatibility if/when any new feature is assigned to a bit or bits in EMR(2) or EMR(3).
2. EMR(2) and EMR(3): At this time, there are no features defined which use bit(s) in EMR(2) or EMR(3).

EMR(2) Programming: Reserved^{*1}



*1: EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMR(3) Programming: Reserved^{*1}



*1: EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

3.11.5.6 — GDDR2 Specific SDRAM Functions

MRS Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	tWR			DLL	TM	CAS Latency			WL			BL

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A7	TestMode
0	Normal
1	Test

A8	DLL Reset
0	No
1	Yes

A0	BL
0	4
1	Reserved

A11	A10	A9	WR
0	0	0	Reserved
0	0	1	Reserved
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	Reserved

A6	A5	A4	CAS Latency
0	0	0	8
0	0	1	9
0	1	0	10 (optional)
0	1	1	Reserved
1	0	0	4 (optional)
1	0	1	5
1	1	0	6
1	1	1	7

A3	A2	A1	Write Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2 (optional)
0	1	1	3 (optional)
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (optional)

Notes:

1. All Devices are specified for sequential burst type operation only.

EMRS Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Vendor	System	Output Driver Ron			DLL	DQS	AL	ODT Control		ODT Option	

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A11	Vendor ID
0	Disabled
1	Enabled (optional)

A9	A8	A7	Ron
0	0	0	60
0	0	1	55
0	1	0	50
0	1	1	45
1	0	0	40
1	0	1	35
1	1	0	30
1	1	1	25

A10	System config
0	Single Rank
1	Multi Rank

A3	A2	ODT Control	
0	0	ODT OFF	ODT for DQ,DQM,DQS, /DQS, CK, /CK is off
0	1	Auto Cal	ODT for DQ,DQM,DQS, /DQS, CK, /CK is selected by resistor connected to ZQ pin
1	0	Rterm=60	ODT for DQ,DQM,DQS, /DQS, CK, /CK is nominally 60 ohm
1	1	Rterm=120	ODT for DQ,DQM,DQS, /DQS, CK, /CK is nominally 120 ohm

A1	A0	ODT Option	
0	0	OFF	ODT for CMD/ADR is off
0	1	x1	On die termination of CMD/ADD are same as DQ
1	0	x2	On die termination of CMD/ADD are 2x DQ
1	1	x4	On die termination of CMD/ADD are 4x DQ

A6	DLL
0	OFF
1	ON

A5	DQS
0	Differential
1	Single

A4	Additive Latency
0	0
1	1 (optional)

EMRS2 Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	ODT W	ODT of CKE	ODT option for CS	ODT option for CK	LP	ODT at PD	0	0	0	0

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A9	ODT W (optional)
0	Enable
1	Disable

A8	ODT of CKE (optional)
0	Off
1	Same as ADD ODT

A7	A6	ODT of CS (optional)
0	0	OFF
0	1	0.5x ADD ODT
1	0	1x ADD ODT
1	1	Reserved

A5	A4	ODT of CK (optional)
0	0	OFF
0	1	1x DQ ODT
1	0	2x DQ ODT
1	1	4x DQ ODT

A3	Low Power Mode (optional)
0	Self Refresh Mode
1	Fast wake-up Mode

A2	ODT at Power Down (optional)
0	OFF All pins except CK, /CK, CKE
1	ON As defined by EMRS/EMRS2

Notes:

1. Devices must support writing to an EMRS2 register even if the only supported mode is the default mode of operation.
2. If no EMRS2 is issued memory must enter default mode for ODT and Self Refresh
3. If there is a change to EMRS, controller will need to re-issue EMRS2 command if intending to use non-default mode functionality

Default Mode is defined as:

- A. ODT W mode will be enabled
- B. ODT value for CS and CKE follow ADD/CMD
- C. ODT value of CK follows ODT value of DQ
- D. Self Refresh mode will be selected
- E. ODT of all pins excluding CK,/CK,CKE at power down mode will be disabled

3.11.5.7 – GDDR3 Specific SGRAM Functions

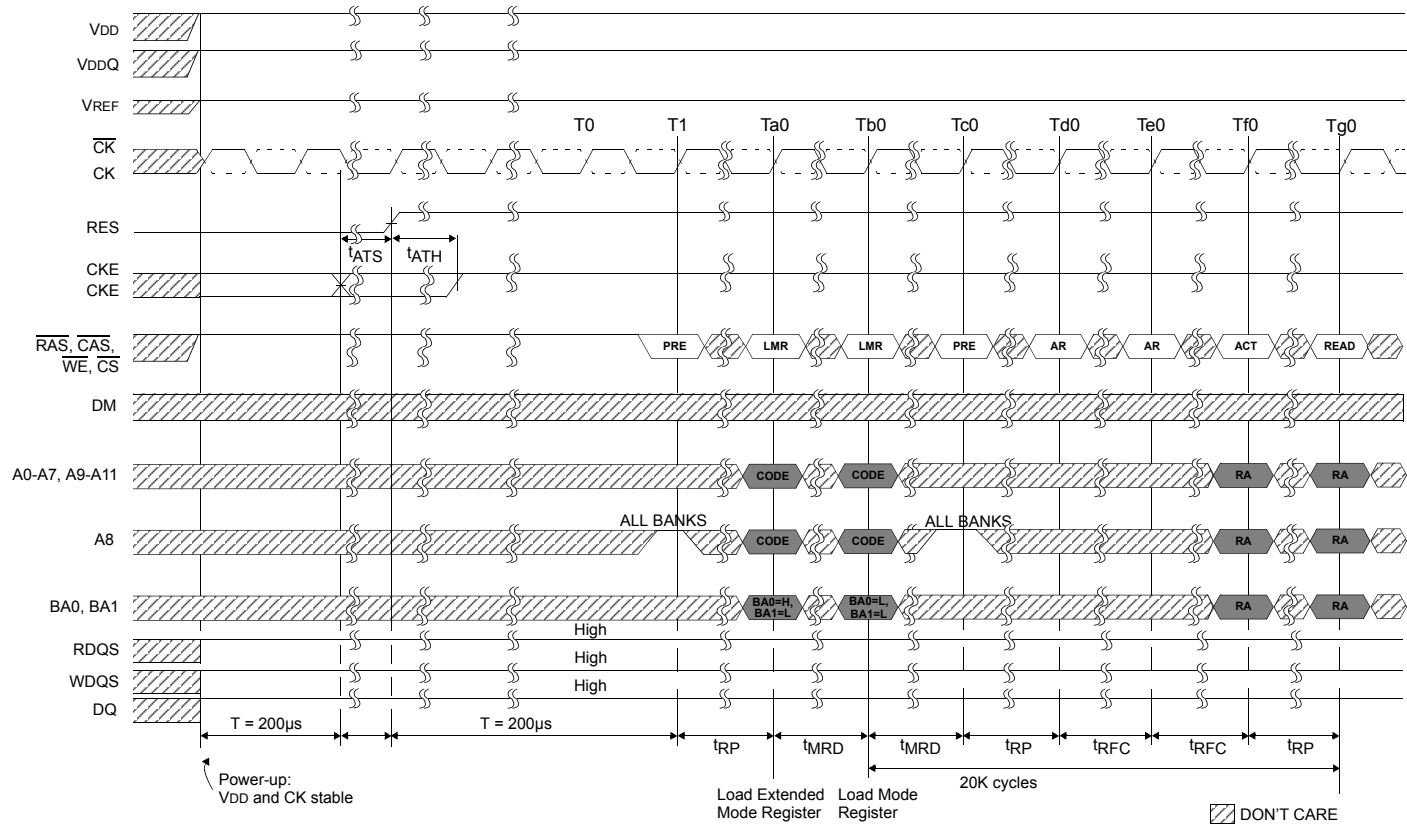
Initialization and Power Up

GDDR3 SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must be first applied to VDD and VDDQ simultaneously, and then to VREF. VREF can be applied any time after VDDQ. Once power has been applied and the clocks are stable the GDDR3 device requires 200 μ s before the RES pin transitions to high. Upon power-up and after the clock is stable, the on die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. On the rising edge of RES, the CKE pin is latched to determine the on die termination value for the address and control lines. If CKE is sampled at a logic LOW then the on die termination will be set to 1/2 of ZQ and, if CKE is sampled logic HIGH then the on die termination will be set to the same value as ZQ. CKE must meet tATS and tATH on the rising of RES to set the on die termination for address and control lines. Once tATH is met, set CKE to HIGH. An additional 200 μ s is required for the address and command on die terminations to calibrate and update.

RES must be maintained at a logic LOW-level value and CS must be maintained HIGH, during the first stage of power-up to ensure that the DQ outputs will be in a High-Z state.

After the RES pin transitions from LOW to HIGH wait until a 200 μ s delay is satisfied. Issue DESELECT on the command bus during this time. Issue a PRECHARGE ALL command. Next a LOAD MODE REGISTER command must be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by the LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 20k clock cycles are required between the DLL reset and any READ command to allow the DLL to lock. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be issued. Following these requirements, the GDDR3 SGRAM is ready for normal operation.



ODT Control

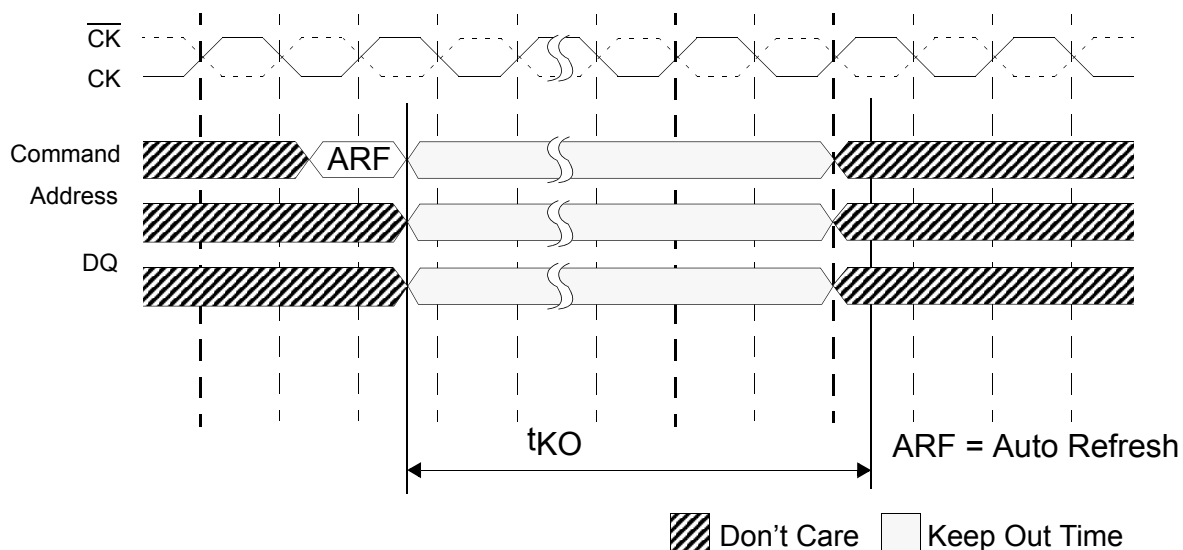
Bus snooping for READ commands excluding CS# is used to control the on die termination in the dual load configuration. The GDDR3 SGRAM will disable the DQ on die terminations when a READ command is detected regardless of the state of CS#. The on die terminations are disabled x clocks after the READ command where x equals $CL - 1$ and stay off for a duration of $BL/2 + 2tCK$. In a two-rank system, DRAM devices on both ranks snoop the bus for READ commands to devices on either rank and all DRAMs will disable the on die terminations, for the DQ pins if a READ command is detected. The on die terminations for input pins on the device such as command (except RES), address, WDQS and DM are always on for both a single-rank system and a dual-rank system unless it is turned off in the EMRS.

ODT Updating

The GDDR3 SGRAM uses a programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSSQ. The value of the resistor must be six times the desired driver impedance. For example, a 240 Ω resistor is required for an output impedance of 40 Ω . To ensure that output impedance is one-sixth the value of RQ (within 10 percent), RQ should be in the range of 210 Ω to 270 Ω (35 Ω – 45 Ω output impedance).

The output impedance and on die termination is updated during every AUTO REFRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all datasheet timings and current specifications are met during an update.

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SGRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9×7.8 us (70.2 us). This maximum absolute interval guarantees that the output drivers and the on die terminations of GDDR3 SGRAMs are recalibrated often enough to keep the impedance characteristics of those within the specified boundaries. During the minimum keep out time of t_{KO} after AUTO REFRESH command, DES (i.e. /CS HIGH) should be issued on the command bus, and no activity on the address or data bus is recommended, because the signal integrity on the bus can not be guaranteed during this period.



Definition of Terminology

Hereafter are defined terminologies used in the GDDR3 SGRAM specification.

Although GDDR3 might be operated in ODT Disable Mode, it is not recommended and the specification describes the ODT Enable Mode only. Should a system be designed to operate the GDDR3 in ODT Disable Mode, the system should comprehend the effect of the discrepancies between this specification and its own design.

If it is stated that a bus is in one of the following state, it should be interpreted as described.

Following are three terminologies defined for ODT Enable Mode.

High{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.

Hi-z{terminated}: No driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.

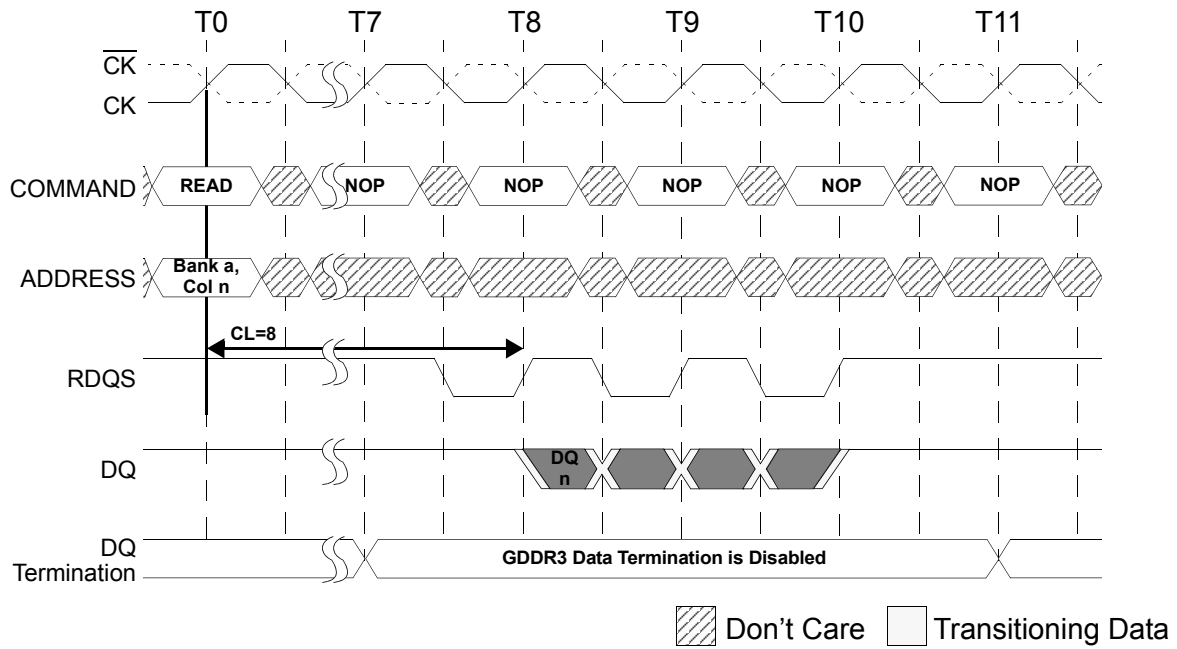
Low{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VOL(DC).

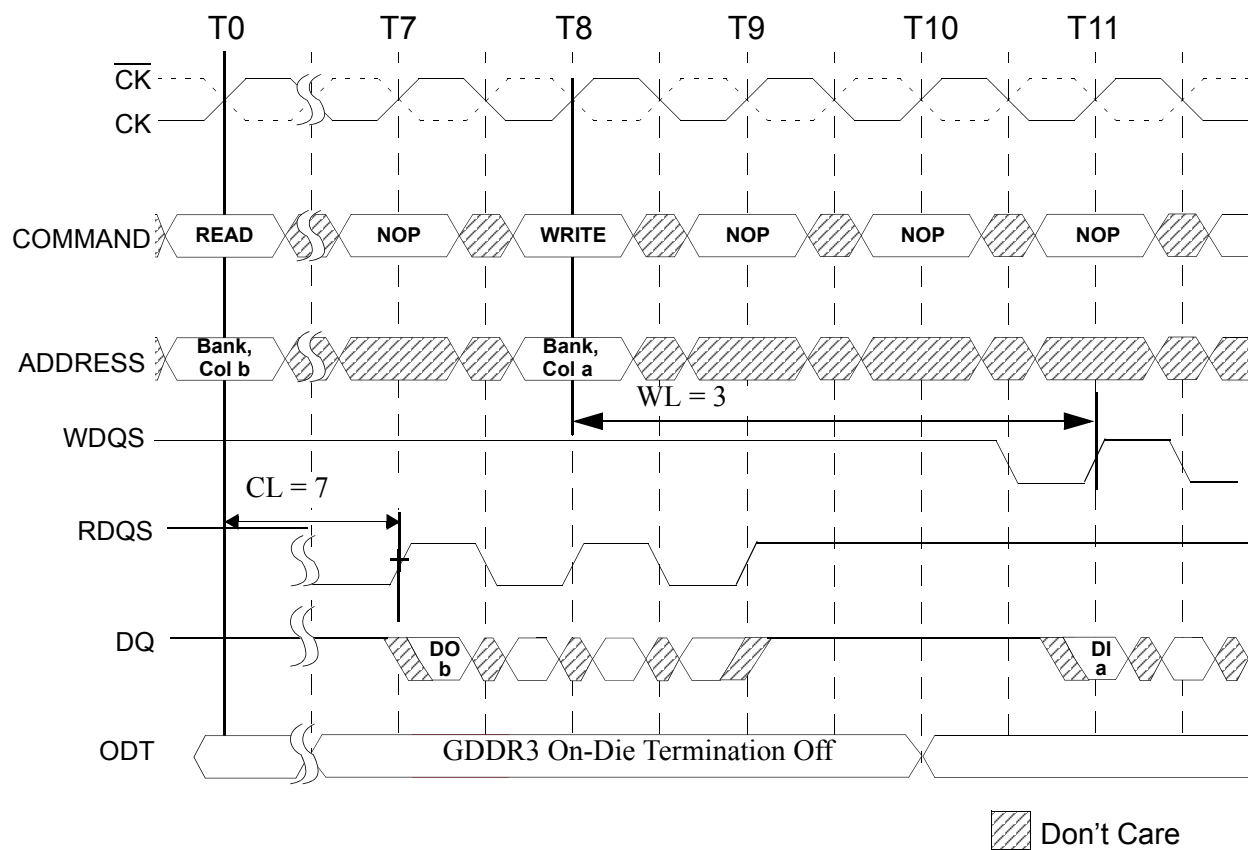
Corresponding terminologies for ODT Disable Mode are defined below. As mentioned before, ODT Disable Mode is not an intended mode of operation. However, there exist situations where ODT Enable Mode can not be guaranteed for a short period of time, like during power up, yet is indeed an intended mode of operation

High{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VDDQ.

Hi-z{unterminated}: No driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be undefined, because the bus would be floating.

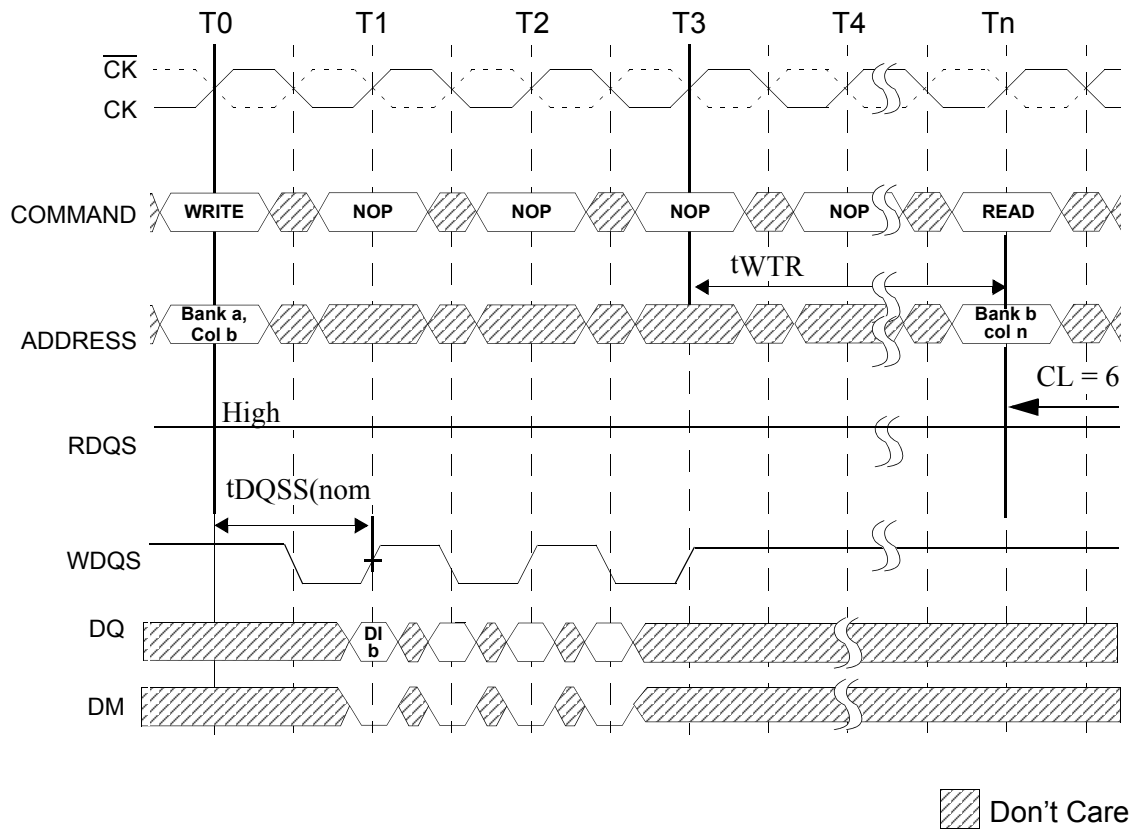
Low{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VSSQ.



READ To WRITE**Notes**

1. Write data can not be driven onto the DQ bus for 2 clock cycles after the READ data is off the bus.
2. The timing diagram covers a READ to a WRITE command from different banks on the same part or the same row in the same bank.

WRITE to READ Timing



1. DI b = Data In for column b
2. Three subsequent elements of Data In are applied following DI b
3. t_{WTR} is referenced from the first positive CK edge after the last Data In
4. The READ and WRITE commands may be to any bank.
5. WRITE Latency is set to 1.
6. RDQS level is High.

Mirror Function

The GDDR3 SGRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines, assisting in routing devices back to back. The MF ball will affect RAS#, CAS#, WE#, CS# and CKE on balls H3, F4, H9, F9 and H4 respectively and A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, BA0 and BA1 on balls K4, H2, K3, M4, K9, H11, K10, L9, K11, M9, K2, L4, G4 and G9 respectively. MF is LVCMOS input and the MF ball should be tied directly to VSS or VDD depending on the control line orientation desired.

When the MF ball is tied low the ball orientation is as follows, RAS# - H3, CAS# - F4, WE# - H9, CS# - F9, CKE - H4, A0 - K4, A1 - H2, A2 - K3, A3 - M4, A4 - K9, A5 - H11, A6 - K10, A7 - L9, A8 - K11, A9 - M9, A10 - K2, A11 - L4, BA0 - G4 and BA1 - G9. The high condition on the MF ball will change the location of the control balls as follows; CS# - F4, CAS# - F9, RAS# - H10, WE# - H4, CKE - H9, A0 - K9, A1 - H11, A2 - K10, A3 - M9, A4 - K4, A5 - H2, A6 - K3, A7 - L4, A8 - K2, A9 - M4, A10 - K11, A11 - L9, BA0 - G9 and BA1 - G4.

PINS	MF Logic State	
	HIGH	LOW
RAS#	H10	H3
CAS#	F9	F4
WE#	H4	H9
CS#	F4	F9
CKE	H9	H4
A0	K9	K4
A1	H11	H2
A2	K10	K3
A3	M9	M4
A4	K4	K9
A5	H2	H11
A6	K3	K10
A7	L4	L9
A8	K2	K11
A9	M4	M9
A10	K11	K2
A11	L9	L4
BA0	G9	G4
BA1	G4	G9
BA2	H3	H10

IO and ODT Drive Values

The Driver and Termination impedances are derived from the following test conditions under worst case process corners

1. Nominal 1.8V (VDD/VDDQ)
2. Power the GDDR3 device and calibrate the output drivers and termination to eliminate process variation at 25°C
3. Reduce temperature to 10°C recalibrate.
4. Reduce temperature to 0°C and take the fast corner measurement.
5. Raise temperature to 75°C and recalibrate
6. Raise temperature to 85°C and take the slow corner measurement

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN	MAX
0.1	2.144	3.366
0.2	4.268	6.516
0.3	6.373	9.454
0.4	8.449	12.185
0.5	10.505	14.715
0.6	12.542	17.051
0.7	14.540	19.400
0.8	16.509	21.828
0.9	18.449	24.219
1.0	20.341	26.580
1.1	22.203	28.913
1.2	24.017	31.222
1.3	25.783	33.508
1.4	27.480	35.813
1.5	29.119	38.213
1.6	30.671	40.551
1.7	31.387	42.900
1.8	31.648	45.176

Pull-Up Characteristic at 40ohms		
Voltage (V)	MIN	MAX
0.1	-2.377	-2.946
0.2	-4.705	-5.829
0.3	-6.984	-8.644
0.4	-9.283	-11.383
0.5	-11.524	-14.038
0.6	-13.803	-16.599
0.7	-16.015	-19.051
0.8	-18.285	-21.630
0.9	-20.302	-24.143
1.0	-22.223	-26.605
1.1	-24.066	-29.005
1.2	-25.773	-31.353
1.3	-27.344	-33.619
1.4	-28.683	-35.803
1.5	-29.731	-37.883
1.6	-30.691	-39.882
1.7	-31.544	-42.003
1.8	-32.311	-44.063

On Die termination Values

Pull-Up Characteristic at 60ohms		
Voltage (V)	MIN	MAX
0.1	-1.58	-1.96
0.2	-3.14	-3.89
0.3	-4.66	-5.76
0.4	-6.19	-7.59
0.5	-7.68	-9.36
0.6	-9.20	-11.07
0.7	-10.68	-12.70
0.8	-12.19	-14.42
0.9	-13.53	-16.10
1.0	-14.82	-17.74
1.1	-16.04	-19.34
1.2	-17.18	-20.90
1.3	-18.23	-22.41
1.4	-19.12	-23.87
1.5	-19.82	-25.26
1.6	-20.46	-26.59
1.7	-21.03	-28.00
1.8	-21.54	-29.38

Pull-Up Characteristic at 120ohms		
Voltage (V)	MIN	MAX
0.1	-0.79	-0.98
0.2	-1.57	-1.94
0.3	-2.33	-2.88
0.4	-3.09	-3.79
0.5	-3.84	-4.68
0.6	-4.60	-5.53
0.7	-5.34	-6.35
0.8	-6.09	-7.21
0.9	-6.77	-8.05
1.0	-7.41	-8.87
1.1	-8.02	-9.67
1.2	-8.59	-10.45
1.3	-9.11	-11.21
1.4	-9.56	-11.93
1.5	-9.91	-12.63
1.6	-10.23	-13.29
1.7	-10.51	-14.00
1.8	-10.77	-14.69

Pull-Up Characteristic at 240ohms		
Voltage (V)	MIN	MAX
0.1	-0.40	-0.49
0.2	-0.78	-0.97
0.3	-1.16	-1.44
0.4	-1.55	-1.90
0.5	-1.92	-2.34
0.6	-2.30	-2.77
0.7	-2.67	-3.18
0.8	-3.05	-3.60
0.9	-3.38	-4.02
1.0	-3.70	-4.43
1.1	-4.01	-4.83
1.2	-4.30	-5.23
1.3	-4.56	-5.60
1.4	-4.78	-5.97
1.5	-4.96	-6.31
1.6	-5.12	-6.65
1.7	-5.26	-7.00
1.8	-5.39	-7.34