

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,532,523

Case No. IPR2023-00513

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent No. 7,532,523 (the “’523 Patent”)
1002	Prosecution history of the ’523 Patent
1003	Declaration of Dr. R. Jacob Baker
1004	Curriculum Vitae of Dr. R. Jacob Baker
1005	U.S. Patent No. 7,433,992 to Bains (“Bains”)
1006	JEDEC STANDARD, Double Data Rate (DDR) 2 SDRAM Specification, JESD79-2A (“JESD79-2A”)
1007	U.S. Patent No. 7,092,299 to Kwak (“Kwak”)
1008	Samuel D., <i>DDR-II: How it Works</i> , X86-SECRET (Sept. 8, 2004), http://www.x86-secret.com/articles/ram/ddr2_667/ddr2667-6en.htm .
1009	U.S. Patent No. 6,754,132 (“Kyung”)
1010	Declaration of Julie Carlson regarding JESD79-2A
1011	First Amended Complaint, Polaris Innovations Ltd. v. Xilinx, Inc., 1:22-cv-00174-RGA (D. Del. April 28, 2022), ECF No. 14
1012	Scheduling Order, Polaris Innovations Ltd. v. Xilinx, Inc., 1:22-cv-00174-RGA (D. Del. May 31, 2022), ECF No. 20
1013	United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf
1014	Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)

Exhibit	Description
1015	JEDEC STANDARD, Configurations for Solid State Memories, JEDEC Standard No. 21-C, Release 14

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.P]	A memory chip for variably setting terminations, comprising:
[1.1]	a terminal;
[1.2]	a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;
[1.3]	a control command port for receiving a control command signal for affecting accessibility of the memory chip;
[1.4]	a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and
[1.5]	a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,
[1.6]	Wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.
Claim 2	
[2]	The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.
Claim 5	
[5.P]	A system, comprising:
[5.1]	(a) a memory controller having a terminal;

[5.2]	(b) a plurality of memory chips, at least one of the memory chips comprising:
[5.3]	a terminal;
[5.4]	a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;
[5.5]	a control command port for receiving a control command signal for affecting the accessibility of the memory chip; and
[5.6]	a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;
[5.7]	(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and
[5.8]	(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,
[5.9]	Wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.
Claim 6	
[6]	The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

Claim 9	
[9.P]	A method for operating a memory chip, comprising:
[9.1]	receiving a control command signal for affecting accessibility of the memory chip;
[9.2]	setting a resistance value for a terminal as a function of the control command signal;
[9.3]	terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and
[9.4]	receiving a termination enable signal, the presence of which is required for the terminating to occur.
Claim 10	
[10]	The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.

I. INTRODUCTION

Xilinx, Inc. (“Xilinx” or “Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1, 2, 5, 6, 9, and 10 of U.S. Patent No. 7,532,523 (the “’523 Patent”), assigned to Polaris Innovations Limited (“Polaris”).

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner Xilinx, Inc., Advanced Micro Devices, Inc. (“AMD”), and ATI Technologies ULC (“ATI”) are the real parties-in-interest. AMD is the parent of Xilinx and ATI is an indirect, wholly owned subsidiary of AMD.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Polaris asserted four patents, including the ’523 Patent, against Xilinx in *Polaris Innovations Ltd. v. Xilinx, Inc.*, CA 1:22-CV-00174-RGA (D. Del.), in a complaint filed on February 8, 2022 and served on February 22, 2022. Xilinx is concurrently filing this Petition and IPR petitions for the other three asserted patents: IPR2023-00514, IPR2023-00516, and IPR2023-00517.

C. Lead and Back-Up Counsel under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence to the address above. Petitioner consents to electronic service by email at xilinxMWETeam@mwe.com.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103

Petitioner authorizes the Office to charge Deposit Account No. 50-0417 for the petition fee set in 37 C.F.R. §42.15(a) and for any other required fees.

IV. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the '523 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR.

B. Challenge under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR of claims 1, 2, 5, 6, 9, and 10 of the '523 Patent on the grounds listed below. In support, this petition includes a declaration of Dr. R. Jacob Baker (EX1003).

Ground	Claims	Basis for Rejection
1	1, 2, 5, 6, 9, and 10	35 U.S.C. §103 over Bains
2	1, 2, 5, 6, 9, and 10	35 U.S.C. §103 over Bains in combination with JESD79-2A

V. SUMMARY OF THE '523 PATENT

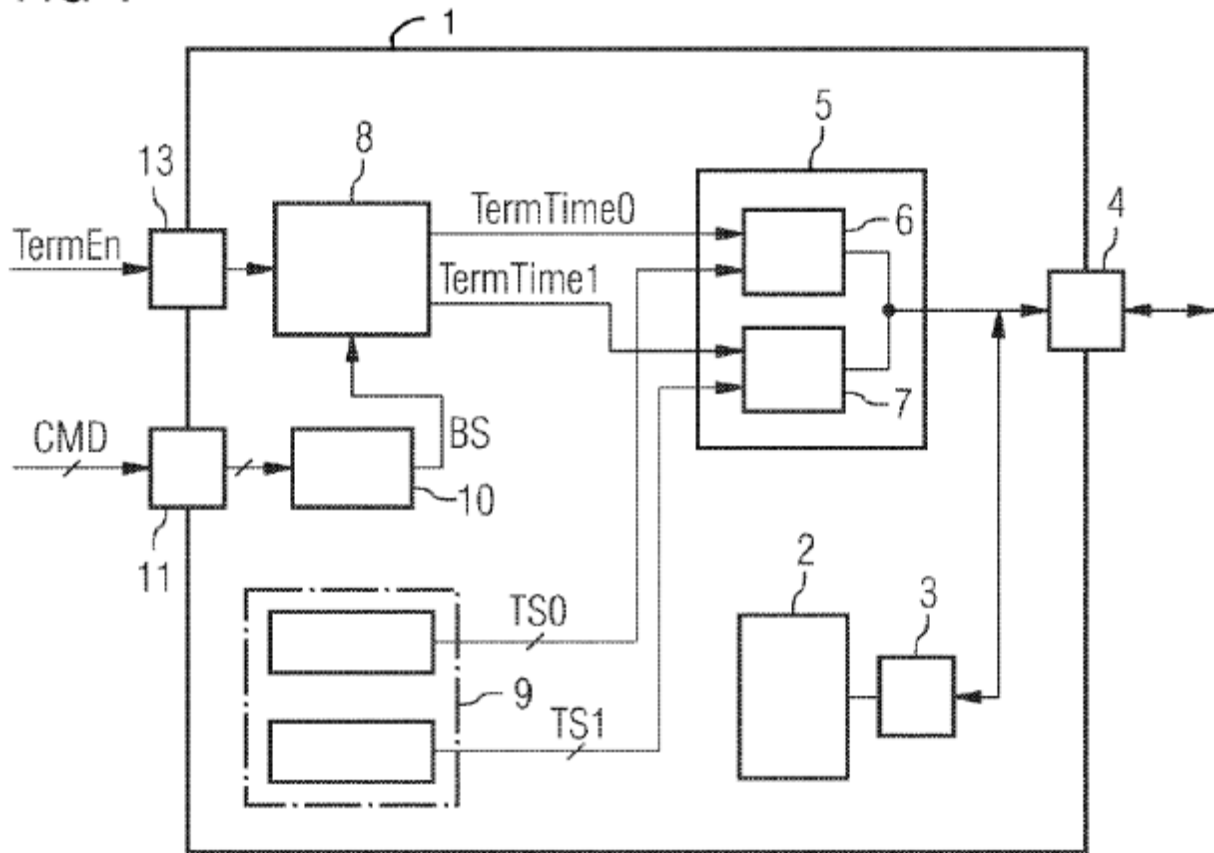
A. Brief Description

The '523 Patent relates to a system and method for terminating a memory chip with various termination resistances. EX1001 at 1:66-2:8; *see also* EX1003 at ¶¶ 50-57 (explaining memory chip termination); EX1015 at 85-88 (describing on die termination in GDDR3 SGRAM); EX1008 at 3 (identifying differences between on die termination and motherboard termination). The claimed invention is designed to be used in a memory system comprising a plurality of memory chips operated via signal lines of a memory bus by a memory controller. EX1001 at 1:23-29. The system and method for terminating a memory chip purport to

improve upon the prior art by providing suitable terminations at the terminals of the memory chips to reduce signal reflections on the signal lines, thereby allowing for higher data transmission rates. *Id.* at 1:29-36.

As shown in Fig. 1 below, the memory chip 1 includes a terminal 4 connected to a termination circuit 5 with resistors 6 and 7 for terminating the terminal 4. *Id.* at 2:40-52. The termination circuit 5 is further connected to a control unit 8 that sends two control signals, TermTime0 and TermTime1, to the termination circuit 5 for controlling which resistor is connected to the terminal 4. *Id.* at 1:52-67. More particularly, when TermTime0 is activated, the first resistor 6 is connected to the terminal 4; when TermTime1 is activated, the second resistor 7 is connected to the terminal 4; and when both signals are activated, the first and second resistors 6 and 7 may be connected to terminal 4 in parallel. *Id.* In that way, the magnitude of the termination resistance may be changed based on the received control signal.

FIG 1



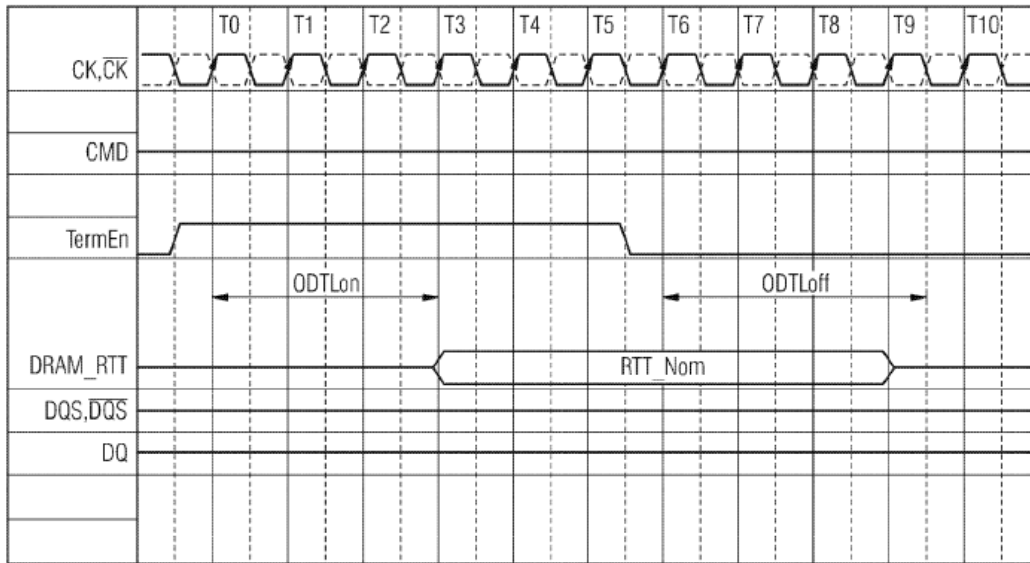
The memory chip 1 further includes a termination port 13 through which the control unit 8 receives a termination enable signal *TermEn*. *Id.* at 3:25-28. The termination enable signal controls whether termination is provided at terminal 4, such that, “via the first and the second control signal *TermTime0*, *TermTime1*, the respective terminating resistor 6, 7 is connected to the external terminal 4 only when the termination signal *TermEn* specifies that there is to be a termination.” *Id.* at 3:28-32.

The chip 1 also includes a control command port 11 for receiving a control command signal, which may be, for example, a chip select signal CS, a write enable signal WE, a row activation signal RAS, or a column activation signal CAS. *Id.* at 3:41-51. A command decoder 10 converts the control command signal into command signal BS, which determines which of the resistors 6 and 7 is connected to the terminal 4. *Id.* at 3:34-40. For a first group of control command signals, the command decoder outputs a command signal BS indicating to the control unit 8 that termination needs to be undertaken with a first resistance value when TermEn is activated. *Id.* at 5:40-58. Similarly, a second group of control command signals results in a command signal BS indicating to the control unit 8 that termination needs to be undertaken with a second resistance value. *Id.* The first group of control command signals may comprise commands that indicate a deactivation of the integrated circuit or a read access, and the second group may comprise write commands. *Id.*

The timing of the termination enable signal and the termination of the memory chip when the chip is not accessed is illustrated in Fig. 3, below. The delay ODTLon represents a predetermined termination switch-on time, or the delay in terminating the terminal 4 after the termination signal TermEn is asserted, and the delay ODTLoff is the predetermined termination switch-off time, or the delay

in disconnecting the termination resistor after the termination signal TermEn is deactivated. *Id.* at 4:30-42, Fig. 3.

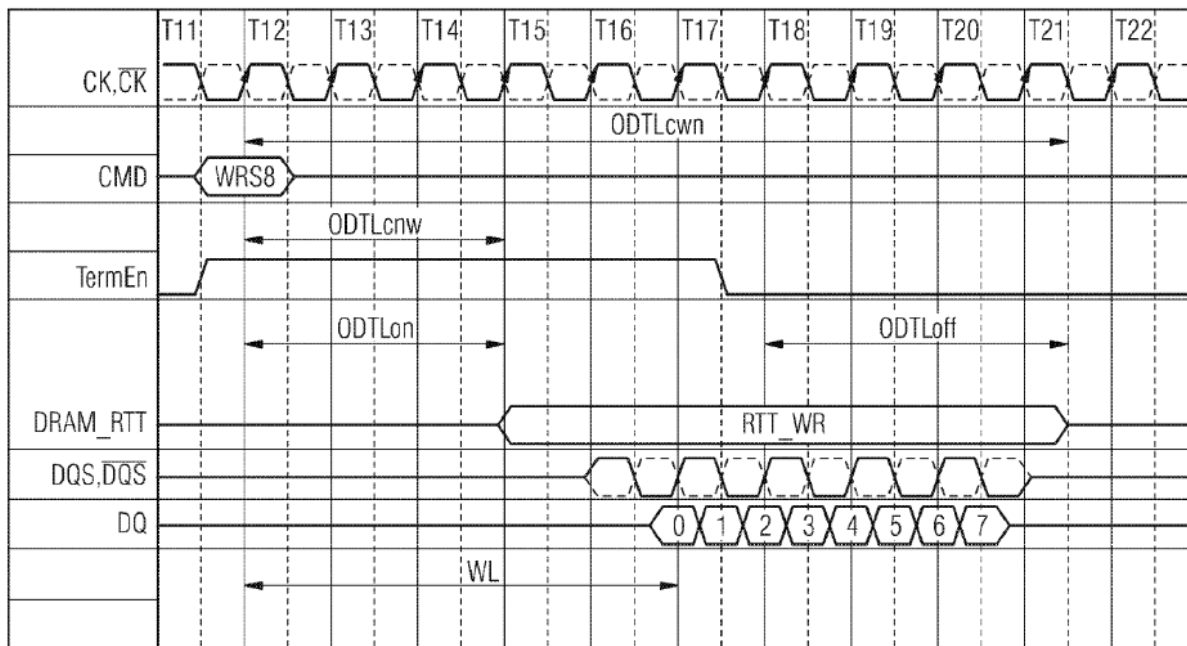
FIG 3



The timing of the control command signal, the termination enable signal, and the termination of the memory chip during a write command is illustrated in Fig. 4, below. *Id.* at 4:64-5:2, Fig. 4. As before, the delay ODTLon represents a predetermined termination switch-on time, or the delay in terminating the terminal 4 after the termination signal TermEn is asserted. *Id.* at 4:30-36. Similarly, ODTLoff is the predetermined termination switch-off time, or the delay in disconnecting the termination resistor after the termination signal TermEn is deactivated. *Id.* at 4:36-42. The termination switch-on and switch-off times ODTLon and ODTLoff may be selected to provide the terminating resistor enough time to connect or disconnect to the terminal without disrupting the data signal. *Id.*

at 4:42-50. In particular, the switch-on time ODTLon may be selected to be equal to or less than the write latency time duration WL of the data in order to ensure that the terminating resistor is connected before data transmission. *Id.* at 5:34-39.

FIG 4



The time delay between applying the control command signal (such as WRS8, above) and changing the resistance value is ODTLcnw, which may be less than or equal to the termination switch-on time ODTLon. *Id.* at 5:59-65. When the control command signal is one of the second group of control command signals, such as a write command, the control unit 8 changes the termination resistance value after a second switchover time ODTLcwn has lapsed, where ODTLcwn represents a time duration defined by the end of an access to the chip that is triggered by the control command signal, such as the end of a write access. *Id.* at

6:5-31. As shown in Fig. 4, the control unit 8 may switch the termination on or off and change the resistance value simultaneously. *Id.* at 5:66-6:4, Fig. 4; EX1003 at ¶¶ 36-43.

B. Summary of the Prosecution

On July 31, 2006, the '523 Patent was filed as Application No. 11/461,380 (the "'380 Application") entitled "Memory Chip and Method for Operating a Memory Chip." EX1002 at 200. The '380 Application claims priority to German Patent Applications DE 10 2005 035 780 and DE 10 2005 036 528, filed July 29, 2005 and August 3, 2005, respectively, and listed twenty-six claims. EX1002 at 195, 184-188. The Applicant filed a preliminary amendment on November 2, 2007 to primarily correct typographical and grammatical errors in claims 1, 5, and 11-20. EX1002 at 184-188, 145-151.

During prosecution of the '380 Application, the PTO issued one non-final office action on June 19, 2008. In the office action, the Examiner rejected claims 1-5, 10-15, and 20-24 as anticipated by U.S. Patent No. 6,762,620 to Jang and as anticipated by U.S. Patent No. 7,148,721 to Park. EX1002 at 59-66. The Examiner objected to claims 6-9, 16-19, 25, and 26 as dependent upon a rejected base claim, but noted that they would be allowable if rewritten in independent form. EX1002 at 66. In response, the Applicant canceled claims 1-5, 10-15, and 20-24 and amended claims 6, 16, and 25 by rewriting them in independent form. EX1002 at

44-50. The amended claims incorporated the limitations of the rejected base claims with an additional limitation from the allowable dependent claims relating to termination delays:

wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

EX1001 at 8:64-9:2; *see also* EX1001 at 9:42-10:4, 10:28-34; *compare* EX1002 at 44-47 *with* EX1002 at 146-150.

The Examiner allowed claims 6-9, 16-19, 25, and 26 on January 13, 2009 based on the above termination delay limitation. EX1002 at 28. However, as explained below, this limitation was already taught in the prior art. EX1003 at ¶¶ 46-48.

VI. THE BOARD SHOULD NOT DISCRETIONARILY DENY INSTITUTION

A. Section 325(d)

Advanced Bionics and §325(d) do not support discretionary denial given that the Bains reference used by Petitioner in all grounds was not considered by the Office, and no similar references were evaluated during prosecution. Denial under §325(d) is thus unwarranted. *See Thorne Rsch., Inc. v. Trs. of Dartmouth Coll.*, IPR2021-00491, Paper 18 at 8-9 (PTAB Aug. 12, 2021).

B. Fintiv (Section 314(a))

The *Fintiv* factors favor institution. This petition presents compelling evidence showing the unpatentability of the challenged claims, and thus institution should not be discretionarily denied under *Fintiv*. Although there is a case pending with Xilinx involving the '523 Patent, it remains at an early stage. Initial discovery and contentions have been served, but the parties have not briefed or argued claim construction, and any final written decision will likely be issued before trial. The current trial date is November 18, 2024 and the median time-to-trial for the Delaware court suggests trial in February 2025. EX1012 at 12; EX1013 at 14. Further, Xilinx intends to request a stay pending IPR. EX1014 (showing the Delaware court grants majority of motions to stay).

VII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) would have had a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and at least two or three years of academic or industry experience in integrated circuit input/outputs and memory systems, or comparable industry experience. EX1003 at ¶¶ 31-35. Additional training can substitute for educational or research experience, and vice versa. A POSITA would have been familiar with the JEDEC industry standards and knowledgeable about the design and operation of standardized DRAM memory systems, including memory devices, modules,

controllers, and interfaces. *Id.* A POSITA would further have been familiar with on die termination designs. *Id.*

VIII. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3)

Petitioner submits that all claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Construction of any terms is unnecessary because it is not dispositive of this case—the art teaches the limitations under any construction under the *Phillips* standard. *Cf. Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

IX. OVERVIEW OF THE PRIOR ART

A. Bains (EX1005)

U.S. Patent No. 7,433,992 (“Bains”) was filed as U.S. Application No. 10/992,953 on November 18, 2004, published on May 18, 2006 as U.S. Patent Publication No. 2006/0106951, and issued on October 7, 2008. Bains is prior art under pre-AIA §§102(a) and 102(e) because it was filed before the earliest potential foreign priority date of the ’523 Patent (July 29, 2005, hereinafter the “Priority Date”). *See* EX1001 at 1.

Bains discloses a memory system comprising a memory controller 12 and memory chips MC0 and MC1 having on die termination (ODT) circuitry 38 and 48. EX1005 at 2:33-58, 3:41-58, Fig. 2 (below). The system also includes a control

bus 20, a data bus 22, an address bus 24, and chip select buses 26 and 28 through which the memory controller and the memory chips communicate. EX1005 at 3:9-16; EX1003 at ¶¶ 61-65.

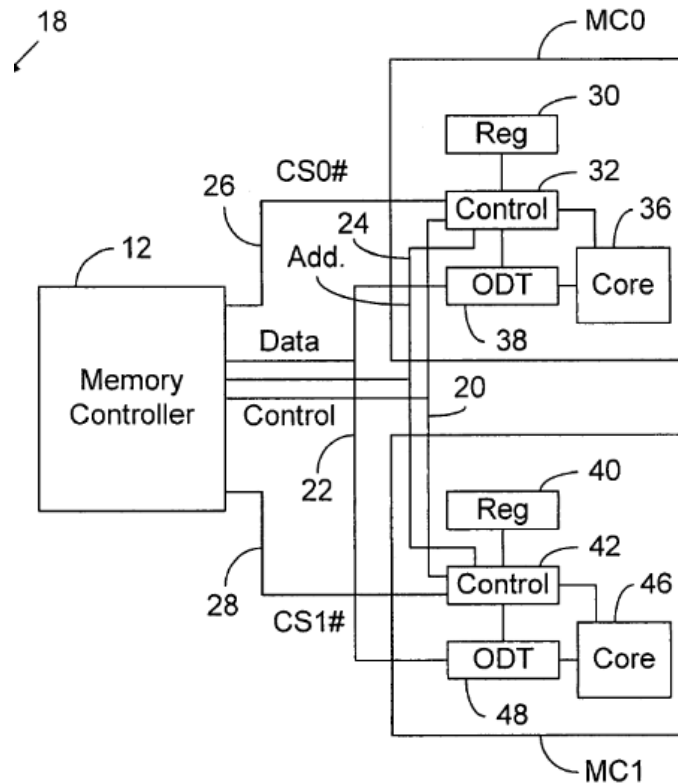


FIG. 2

EX1005 at Fig. 2.

Commands such as commands A and B may be provided from memory controller 12 to chips MC0 and MC1 through control bus 20. EX1005 at 3:17-20, 41-42. Control circuitry 32 in chip MC0 and control circuitry 42 in chip MC1

receive the commands and control the operation of ODT circuitry 38 and 48, respectively, based on the commands. EX1005 at 3:41-58. For example, chip MC0 responds to command A as a write command, while control circuitry 42 in chip MC1 responds to command A by turning on ODT 48. *Id.* Conversely, chip MC1 responds to command B as a write command, while control circuitry 32 of chip MC0 turns on ODT 38. *Id.*

An exemplary ODT circuit 38 is shown in Fig. 4, below. Control circuitry 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off.” EX1005 at 4:39-40. Additionally, the number of switches that are closed may determine the amount of resistance that is applied to the data pin. EX1005 at 4:40-42. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. While Bains discloses that the commands control whether ODT is “on” as well as the level of ODT resistance, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands. EX1005 at 6:30-37.

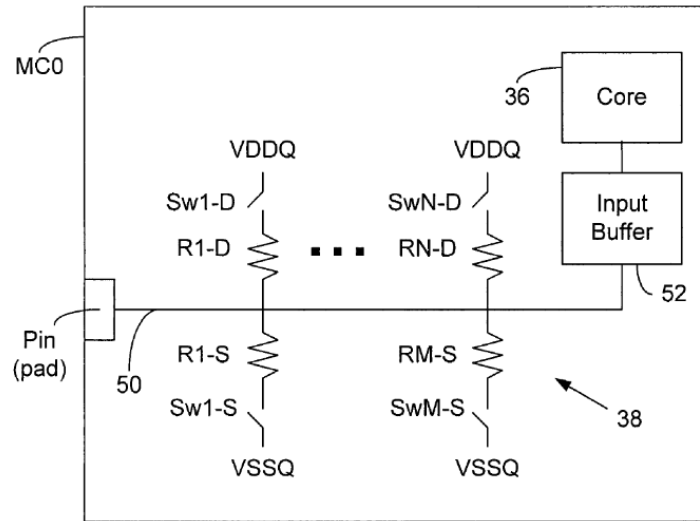


FIG. 4

EX1005 at Fig. 4.

Bains further teaches that the ODT is enabled and disabled according to predetermined delays. As illustrated in Fig. 7 below, ODT in chip MC1 is turned on after a delay of t_{AOND} after command A is asserted. EX1005 at 5:23-30. ODT in chip MC1 is turned off automatically after a fixed delay based on a burst length of 8. EX1005 at 5:40-42.

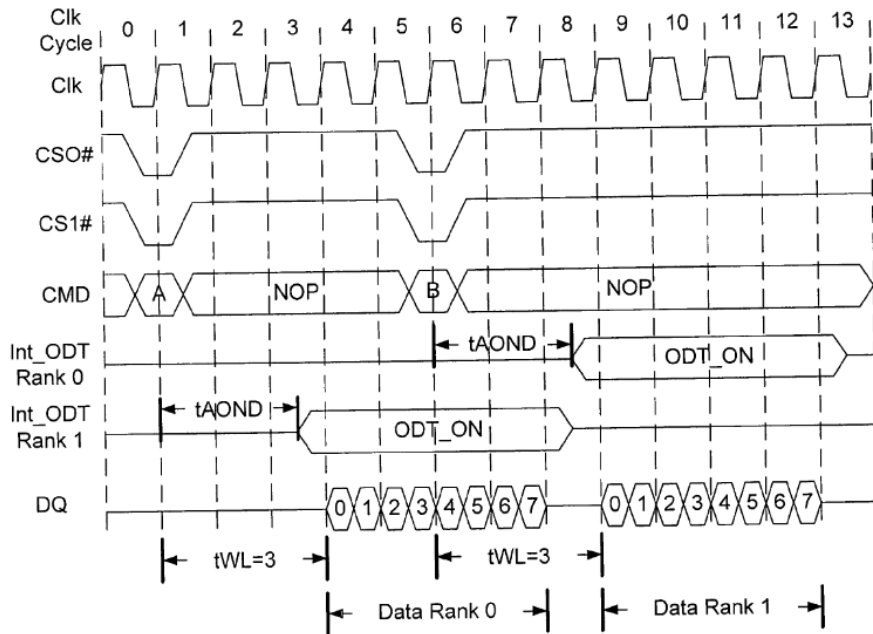


FIG. 7

EX1005 at Fig. 7.

B. JESD79-2A (EX1006)

JEDEC Double Data Rate 2 (DDR2) SDRAM Specification, JESD79-2A (“JESD79-2A”), is the Joint Electron Device Engineering Council’s (“JEDEC”) well-known memory specification for DDR2 memory. JESD79-2A qualifies as prior art under at least pre-AIA §§102(a) and 102(b) because it is a printed publication that was publicly accessible before the Priority Date and at least one year before the ’523 Patent’s United States filing date (July 31, 2006). Specifically, JESD79-2A was publicly available for download from JEDEC’s website no later than January 2004. EX1010 at ¶ 10. As support, Petitioner relies upon the Declaration of Julie D. Carlson (“the Carlson Declaration”), a full-time Consultant

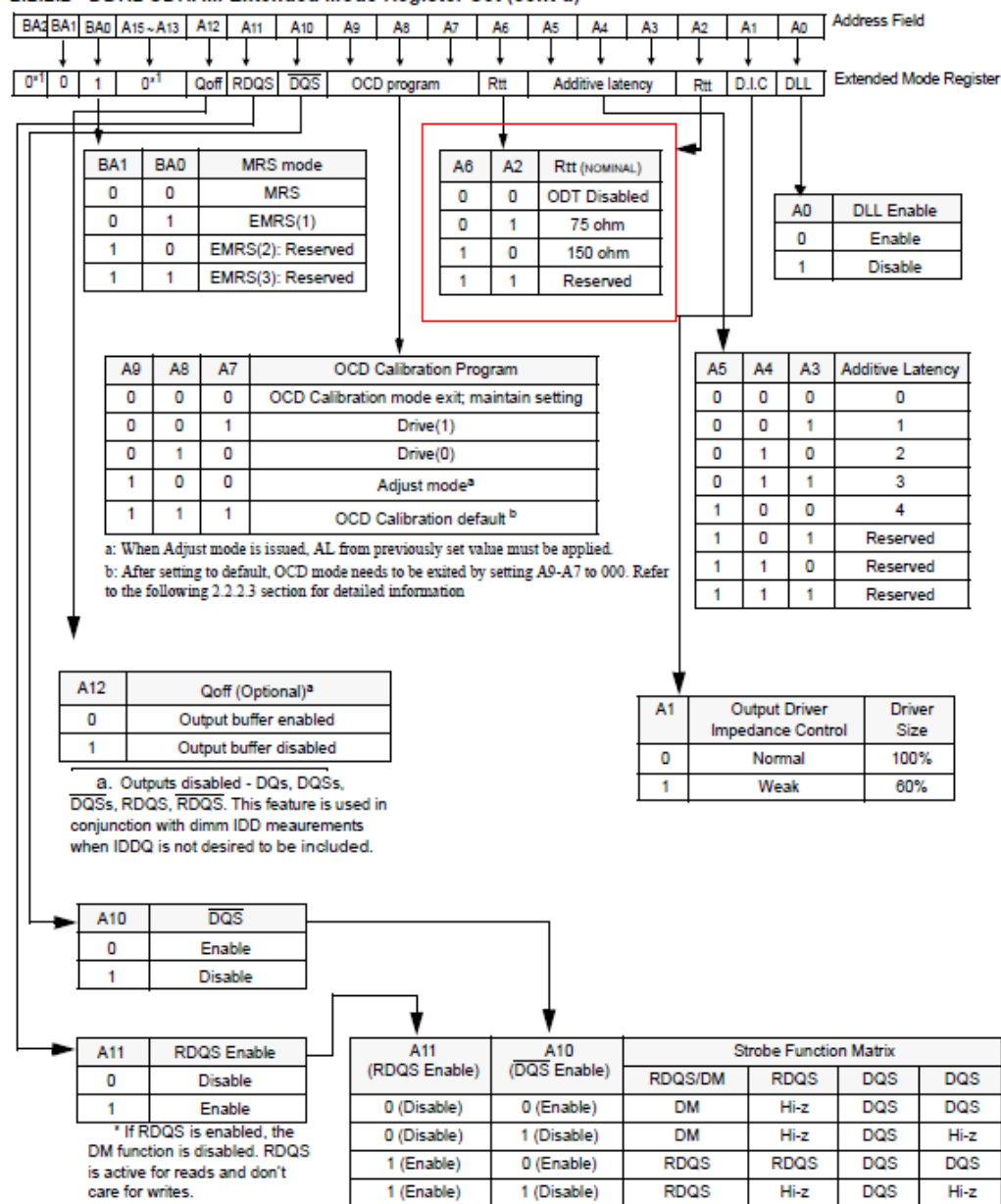
for JEDEC who is responsible for the maintenance and publication of JEDEC documents and standards. *Id.* at ¶ 3. Ms. Carlson states that JEDEC specification JESD79-2A, a copy of which is attached to her declaration as Exhibit G, was made publicly available as of the date on the cover of the specification, January 2004. *Id.* at ¶ 10. Ms. Carlson testifies that JESD79-2A would have been “made publicly available via JEDEC’s website in...January 2004,” “where [it would have been] cataloged and indexed by keyword and technological subject matter.” *Id.* at ¶¶ 14, 6. JESD79-2A was and remains a well-known memory standard published by JEDEC, a prominent memory standards setting organization. EX1003 at ¶ 66 (explaining that a POSITA would have been well-aware of JEDEC memory standards like JESD79-2A and would have been aware of how to access those standards, what they disclose, and how to design a memory device according to the standards); *see, e.g., SK hynix Inc. v. Netlist, Inc.*, IPR2017-00577, Paper 26 at 6 (PTAB July 5, 2018) (noting that JESD79 was published in June 2000); *Samsung Elecs. Am., Inc. v. Goodman*, IPR2017-02021, Paper 19 at 18-19 (PTAB Oct. 29, 2019) (JEDEC’s JESD12-C is a printed publication available in January 1997, which is listed on the face of the standard).

JESD79-2A discloses a specification for DDR2 SDRAM with ODT functionality. When the ODT signal on the ODT control pin is high, termination resistance internal to the DDR2 SDRAM is enabled and applied to the DQ

terminal. EX1006 at 14, 26.¹ The ODT feature is designed to improve signal integrity by allowing the memory controller to independently enable termination resistance for connected memory chips. EX1006 at 26. As shown in Fig. 9, below, the extended mode register set (EMRS) stores data for enabling ODT functionality and setting the ODT resistance value in bits A2 and A6. EX1006 at 21, 22. The EMRS is written by asserting low on CS, RAS, CAS, WE, high on BA0, and low on BA1. EX1006 at 21; EX1003 at ¶¶ 66-70.

¹ All page cites refer to the stamped page number of the exhibit.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)



^{*} BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

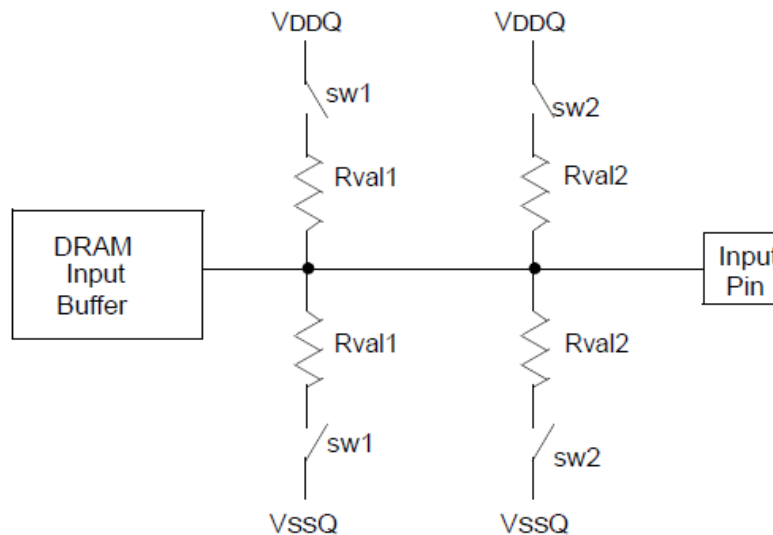
Figure 9 — EMRS(1) Programming

EX1006 at page 22, Fig. 9 (annotation added)².

² All color annotations in figures have been added unless otherwise stated.

JESD79-2A illustrates an ODT circuit in Fig. 15, below. Switches sw1 and sw2 are enabled by the ODT pin, and the selection between sw1 and sw2 is determined by bits A2 and A6 in the EMRS, as explained above. EX1006 at 27, Fig. 15. For example, if Rval1 is associated with an effective resistance of 75 ohms, and Rval2 is associated with an effective resistance of 150 ohms, then switches sw1 are selected when bit A6 is set to 0 and bit A2 is set to 1, and switches sw2 are selected when bit A6 is set to 1 and bit A2 is set to 0. When a high level is applied to the ODT pin, switches sw1 or sw2 are closed depending on the values of bits A2 and A6.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
 Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
 Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
 Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

EX1006 at 27, Fig. 15.

JESD79-2A also discloses the ODT timing for a DDR2 SDRAM in active/standby mode. As illustrated in Fig. 16 below, termination is applied after a period t_{AOND} after the ODT signal is enabled, and termination ends after a period t_{AOFD} after the ODT signal is disabled. EX1006 at 27.

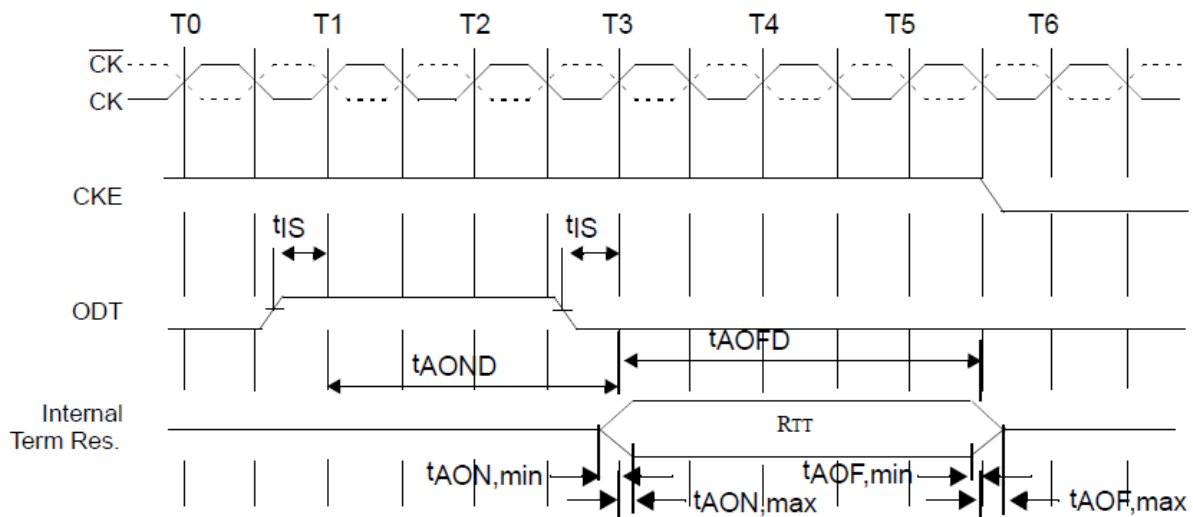


Figure 16 — ODT Timing for Active/Standby Mode

EX1006 at 27, Fig. 16.

X. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

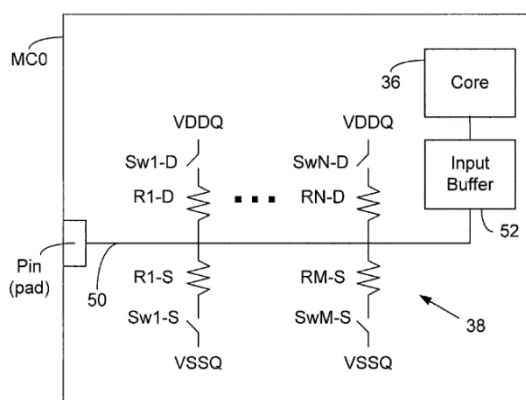
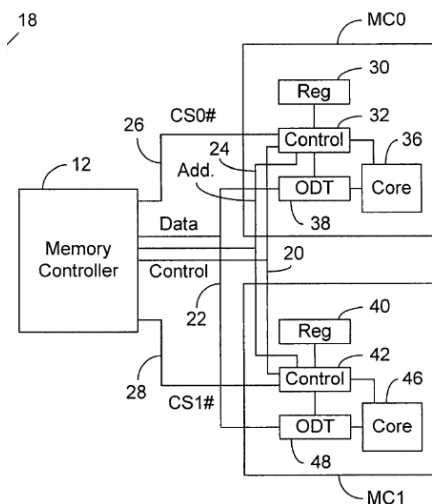
A. Ground 1: Claims 1, 2, 5, 6, 9, and 10 are obvious over Bains

1. Claim 1

a. “A memory chip for variably setting terminations, comprising:” [1.P]

To the extent the preamble is limiting, Bains teaches the limitation.

Specifically, Bains teaches a memory chip MC0 (or alternatively, MC1) with an ODT circuit 38 that may terminate a data pad with an infinite resistance³ or different finite resistances depending on the command A1 or A2 provided to the chip from the memory controller 12. EX1005 at 2:33-52, 3:41-58, 4:39-61, Figs. 2 and 4 (each figure reproduced below); *see also infra* limitation [1.2] in Section X.A.1.c.; EX1003 at ¶ 72.



³ The term “infinite resistance” refers to the high impedance state that occurs when the termination circuit is open, or deactivated.

b. “a terminal” [1.1]

Bains teaches this limitation. As shown below in Fig. 4, Bains teaches that the memory chip MC0 includes a data pin (pad), which is a terminal. EX1005 at Fig. 4 (annotated and reproduced below); EX1003 at ¶ 73; EX1001 at 2:45-48, Fig. 1.

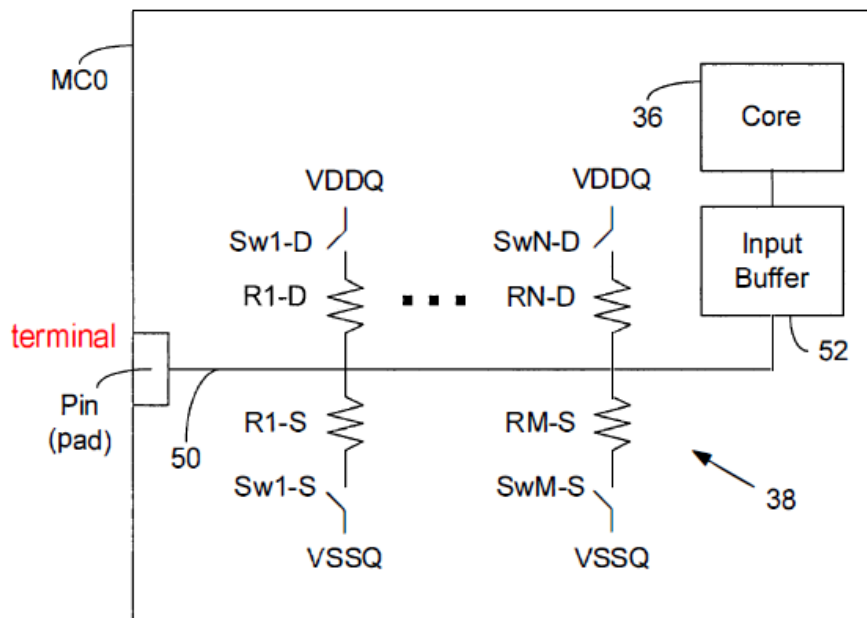


FIG. 4

c. “a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;” [1.2]

Bains also teaches this limitation. As illustrated in Figs. 2 and 4 below, Bains discloses an ODT circuit 38 coupled to the terminal. EX1005 at Figs. 2, 4 (annotated and reproduced below). Control circuitry 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S of the termination circuit 38 and thus whether

ODT is “on” or “off.” EX1005 at 4:31-40. Additionally, the number of switches that are closed determines the amount of resistance that is applied to the data pin. EX1005 at 4:40-42. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. Thus, the termination circuit 38 may apply an infinite resistance to the terminal (open circuit, ODT “off”) or any one of a variety of finite resistances depending on which switches Sw1-D...SwN-D and Sw1-S...SwM-S are activated by control circuitry 32 as a function of commands A1, A2...AN. EX1003 at ¶¶ 74-75.

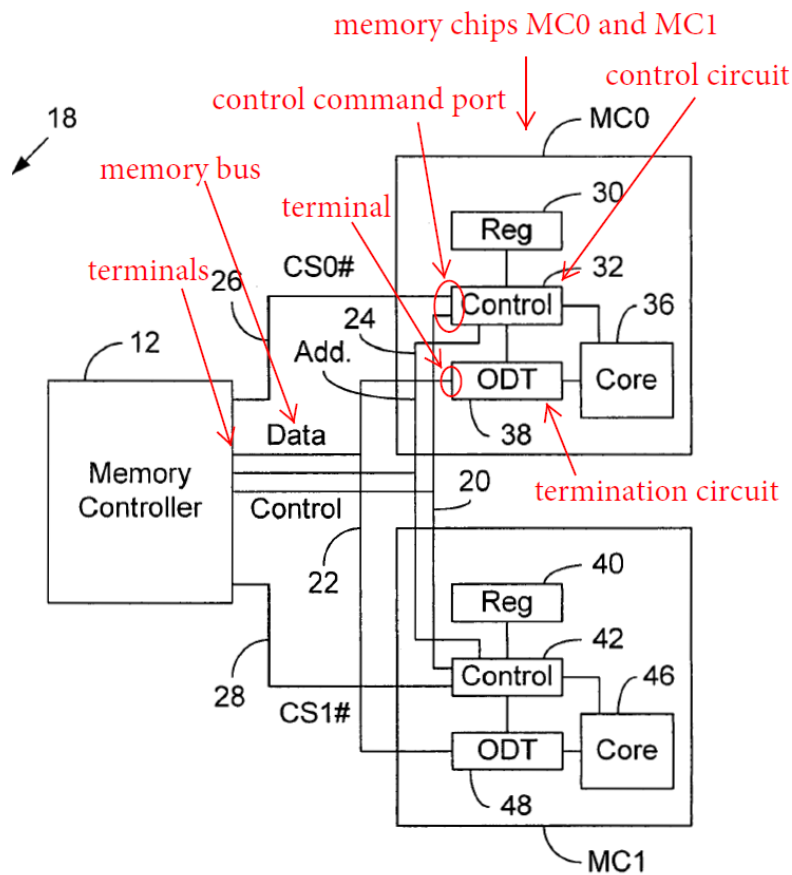


FIG. 2

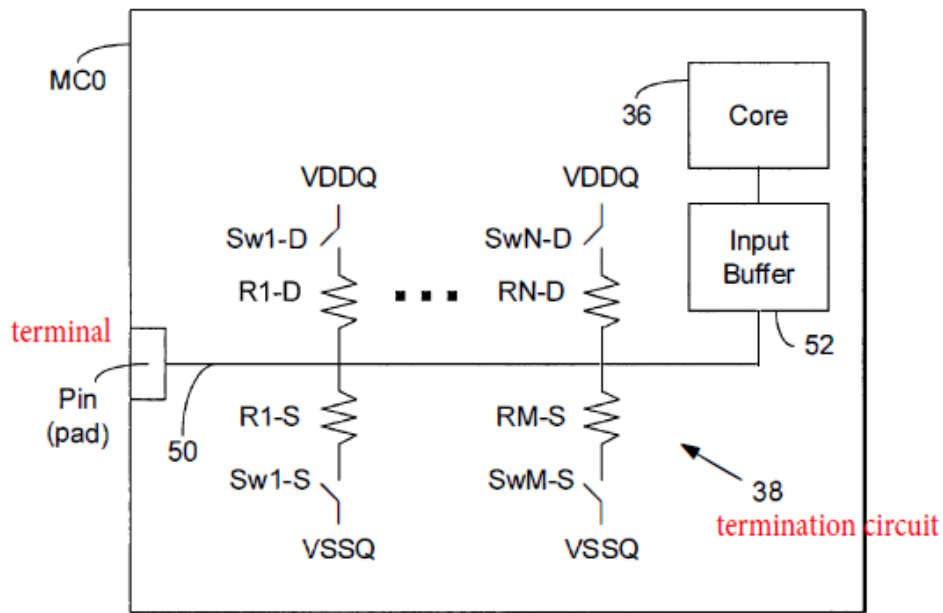


FIG. 4

d. “a control command port for receiving a control command signal for affecting accessibility of the memory chip;” [1.3]

Bains also teaches this limitation. As shown in annotated Fig. 2, below, Bains teaches that memory controller 12 is coupled to chips MC0 and MC1 through a control bus 20 and chip select buses 26 and 28 through which commands may be transmitted. EX1005 at 3:9-28, 41-42; EX1003 at ¶ 76.

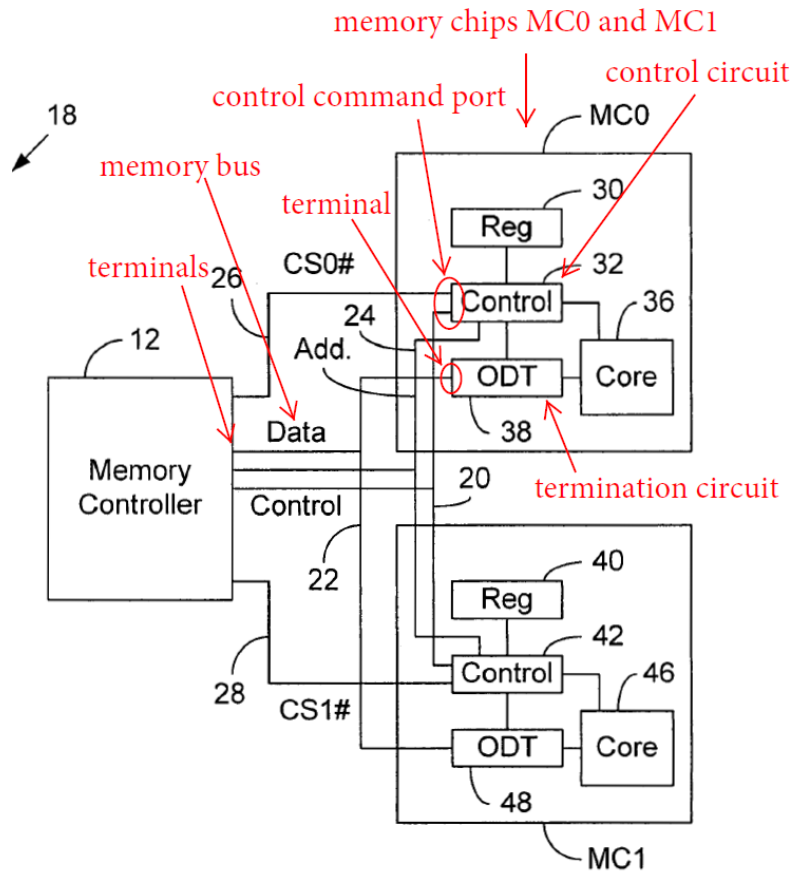


FIG. 2

EX1005 at Fig. 2 (annotated).

In order to receive commands from the memory controller 12 sent over the buses, a POSITA would understand that the control circuit 32 includes a port connected to the control bus 20 and chip select bus 26, as represented by the topmost circled portion in the above annotated Fig. 2. To the extent Patent Owner were to argue such a control command port is not expressly disclosed, it certainly would have been obvious to a POSITA that the control circuit 32 includes such a port because the control circuit is disclosed as receiving commands from controller 12, which must enter through a port. EX1005 at 3:9-28; EX1003 at ¶ 77.

Furthermore, Bains discloses that the memory controller 12 transmits commands A, B, C, or D to the memory chips via the buses. EX1005 at 3:17-28, 3:37-4:6. Bains describes that these commands may be, for example, write commands, read commands, or refresh commands, which affect accessibility of the chips MC0 and MC1. EX1005 at 3:41-65. Commands A, B, C, and D are the same type of commands as the exemplary control command signals disclosed in the '523 Patent. EX1001 at 3:41-51 (control command signals may include a chip select signal CS, a write enable signal WE, a row activation signal RAS, or a column activation signal CAS for transmitting the bit line address and for activating the bit line for reading data out and/or writing data to the memory cells). EX1003 at ¶¶ 78-80.

e. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and” [1.4]

This limitation is also taught by Bains. Control command signals such as commands A and B may be provided from memory controller 12 to chips MC0 and MC1 through the buses. EX1005 at 3:17-24, 41-42. Control circuit 32 in chip MC0 and control circuit 42 in chip MC1 receive the commands and control the operation of ODT circuitry 38 and 48, respectively, based on the commands. EX1005 at 3:41-58. For example, chip MC0 responds to command A as a write command, while control circuit 42 in chip MC1 responds to command A by

turning on ODT 48. *Id.* Conversely, chip MC1 responds to command B as a write command, while control circuit 32 of chip MC0 turns on ODT 38. *Id.*; EX1003 at ¶¶ 81-82.

As stated in Bains and shown in annotated Figs. 2 and 4, below, the control circuit 32 controls switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off.” EX1005 at 4:39-40. Bains further teaches that the number of switches that are closed by control circuit 32 determines the amount of resistance that is applied to the data pin. EX1005 at 4:40-42. Furthermore, Bains discloses that the particular command received determines what resistance value is set. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44; EX1003 at ¶ 83.

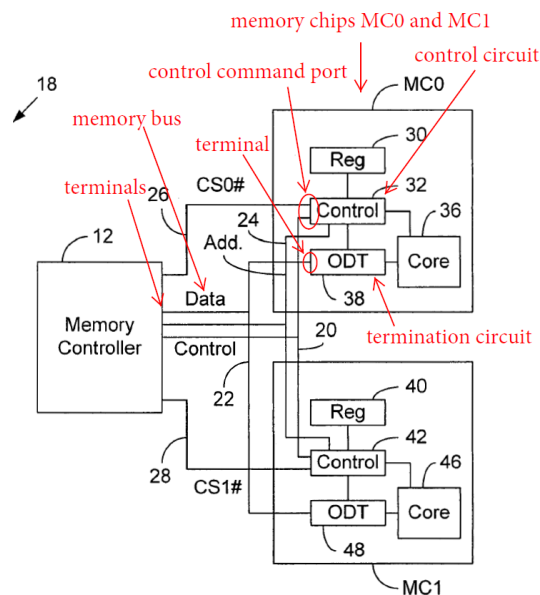


FIG. 2

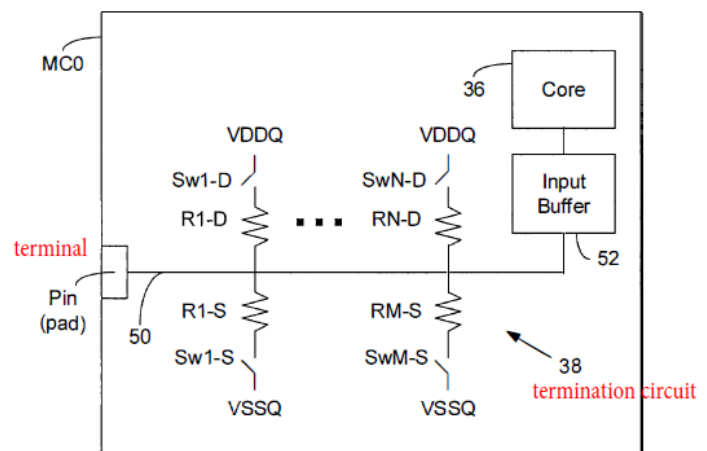


FIG. 4

f. “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,” [1.5]

Bains also teaches this limitation. As explained in the previous section with regards to limitation [1.4], Bains teaches that, in the embodiment illustrated in Fig. 2, the control command signals control whether ODT is “on” as well as the level of ODT resistance. *Supra* Section X.A.1.e. However, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands. EX1005 at 6:30-37. As admitted by the applicant in the Background section of the ’523 Patent, such ODT pins were well known in the art. EX1001 at 1:37-44 (“It has previously been provided in the case of memory chips to switch the termination on or off at a terminal of the memory chip as a function of a termination signal. That is to say, the memory controller makes a suitable termination signal available to each of the memory chips in order to support the following read, write, or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus.”); *see also* EX1003 at ¶¶ 44-45 (identifying applicant admitted prior art concepts disclosed in the ’523 Patent’s background). Indeed, Bains’ Background section also refers to the use of such ODT pins, as prescribed by the JEDEC standards for DDR2 DRAM chips. EX1005 at 1:37-45. Thus, a POSITA would have understood Bains’ disclosure at 6:30-37 to include

the use of an ODT pin for controlling whether ODT is “on” in the system taught by Bains, in addition to the use of commands, such as the disclosed A1 and A2 commands discussed above, to indicate the amount of resistance to be applied. EX1003 at ¶¶ 84-86.

Furthermore, to the extent that Patent Owner were to argue that this is not explicitly disclosed, it would have been obvious to a POSITA to provide such a configuration. As discussed above, the ’523 Patent admits, and Bains discloses, that the use of an ODT pin to switch the termination on or off was well-known. Bains also discloses the use of command signals to set the resistance value. Based on Bains’ disclosure, a POSITA would have been motivated to use an ODT pin to control whether ODT is “on” and to use commands to indicate the amount of resistance to be applied because this configuration would permit for more complex termination schemes and more customizable termination timing than a command-only control system. For example, by asserting the ODT enable signal before a command, ODT could be turned “on” before a command is asserted. In addition, by providing an ODT pin, a POSITA would also ensure compliance with JEDEC standards, which is essential for interoperability. EX1003 at ¶¶ 87-88.

g. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in

accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.” [1.6]

As discussed above, Bains teaches that the control circuit 32 controls termination circuit 38, and that termination may be turned on and off via a separate termination signal on an ODT pin. *Supra* Section X.A.1.e-f. Bains further teaches that the control circuit “performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.” As illustrated in Fig. 7 below, ODT in chip MC1 is turned on after a delay of t_{AOND} (annotated below in pink) after command A (annotated below in blue) is asserted and turned off automatically after a fixed delay based on a burst length of 8 associated with the write command (annotated below in green).⁴ EX1005 at 5:23-42. While the first and second delays in Fig. 7 are relative to command A, when the system of Bains has an ODT pin for controlling the

⁴ Fig. 7 is a timing diagram illustrating the operation of the system of Fig. 5, which includes a rank 0 of chips MC0-0 to MC0-N and a rank 1 of chips MC1-0 to MC1-N. EX1005 at 5:23-42. The operation of the systems in Figs. 2 and 5 are otherwise the same, and chips MC0 and MC1 in Fig. 2 operate the same as chips MC0-0 through MC0-N and MC1-0 through MC1-N in Fig. 5, respectively. EX1005 at 4:47-61.

enabling and disabling of termination as discussed above with respect to limitation [1.5], a POSITA would have understood or have found obvious that the first and second delays are relative to the ODT signal, rather than the command signal. Thus, a POSITA would have understood that ODT is turned on after a delay of t_{AOND} after the ODT signal is asserted, and is turned off after a delay that is based on a write burst length (such that the termination is maintained throughout the write operation). EX1003 at ¶ 89.

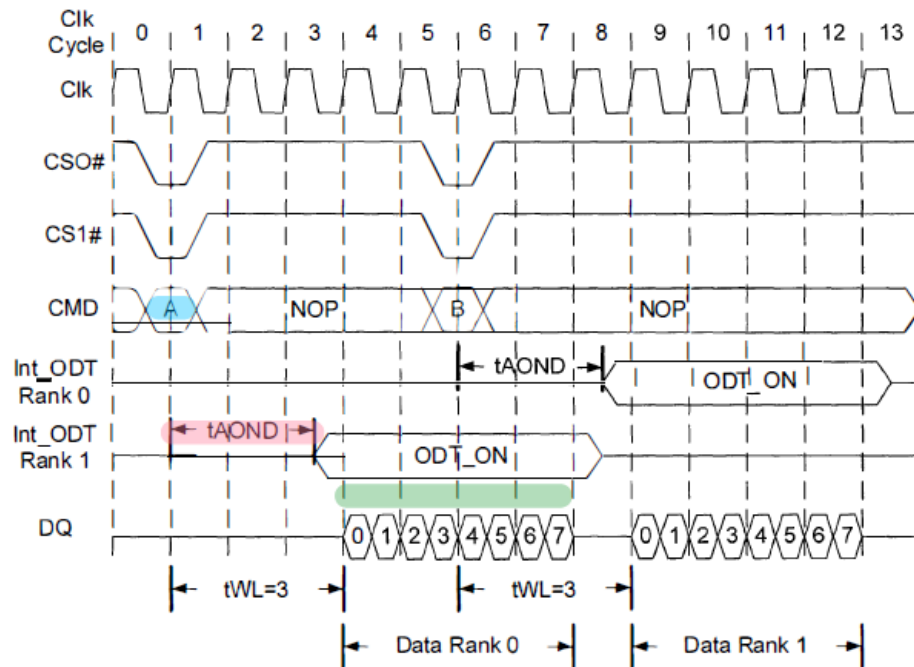


FIG. 7

EX1005 at Fig. 7.

A POSITA would have further understood or found obvious that the timing of the second delay may alternatively be defined relative to the end of the ODT signal (i.e., relative to the ODT signal turning off), rather than the burst length. In

particular, the second delay may be a fixed length of time after the ODT signal turns off. The fixed length of time may be programmed in the controller to end after the data has been written or read. This timing scheme is prevalent in the prior art—such as the JEDEC standard for DDR2 DRAM chips cited in Bains—and is well within the knowledge of a POSITA. EX1005 at 1:37-45; EX1006 at Fig. 16. EX1003 at ¶¶ 90-91.

Furthermore, because the termination actually does occur after tAOND in the timing diagram of Fig. 7, a POSITA would understand that the first time delay tAOND is sufficiently long enough for the switches Sw1-D...SwN-D and Sw1-S...SwM-S to close and set the resistance value. It also would have been obvious to a POSITA that tAOND would be long enough to set and apply the resistance value because otherwise, at least some of the data would be transmitted on the signal line without the proper termination in place, reducing the signal quality. EX1003 at ¶ 92.

2. Claim 2: “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

As explained above, Bains teaches that the control circuit 32 controls switches Sw1-D...SwN-D and Sw1-S...SwM-S in the termination circuit, where the number of switches that are closed by control circuit 32 determines the amount of

resistance that is applied to the data pin. EX1005 at 4:39-42; *supra* Section X.A.1.e. Bains further teaches that the number of switches closed by control circuit 32 is a function of the control command signal received by the control circuit 32. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. Thus, the termination circuit 38 may apply an infinite resistance to the terminal (open circuit, ODT “off”) or any one of a variety of finite resistances depending on which switches Sw1-D...SwN-D and Sw1-S...SwM-S are activated by control circuitry 32 as a function of commands A1, A2...AN. EX1003 at ¶ 93.

The first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2. EX1003 at ¶ 94.

a. Mapping to a Finite Resistance and an Infinite Resistance

The above interpretation of “second resistance value” as including an infinite resistance value is consistent with the claims and specification of the ’523 Patent. Claims 4 and 8 recite that

the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal

of the respective memory chip, and sets the resistance value to the ***second resistance value substantially simultaneously with the ending of the termination*** of the terminal of the respective memory chip.

EX1001 at 9:13-19 and 10:15-22 (emphasis added).

In particular, claims 4 and 8 state that the second resistance value is applied simultaneously with the ending of the termination. When the termination is disabled, there is an open circuit, resulting in an infinite termination resistance. Accordingly, the second resistance value in claims 4 and 8 must be an infinite resistance.⁵ Because claims 4 and 8 depend from claims 2 and 6, respectively (via another dependent claim), the scope of claims 2 and 6 must also include an infinite resistance as one potential value for the second resistance. EX1003 at ¶¶ 95-96.

Furthermore, because claims 4 and 8 require that the control circuit sets the resistance value to a first resistance value simultaneously with the switching on of the termination and to a second resistance value simultaneously with the switching

⁵ Other prior art references discussing ODT similarly recognize that a disabled termination circuit, which theoretically applies an infinite resistance, is understood as applying a high termination impedance value, rather than no termination impedance value. *See* EX1007 at 6:11-52 (During a read operation, the ODT circuit is deactivated and provides a “higher termination impedance.”).

off of the termination, the first and second time delays recited in claim 1, which govern the switching on and off of the termination, may be the same as the first and second predetermined switchover times recited in claim 2, which govern the switching of the termination from the first to the second resistance values. This is explicitly supported by the specification of the '523 Patent, which states that the “first switchover time ODTLcnw...**may be equal to** or less than the termination switch-on time ODTLon”) (emphasis added). EX1001 at 5:63-65; EX1003 at ¶ 97.⁶

In Fig. 7, below, Bains demonstrates that the resistance value is set to a first resistance value based on the received command A (blue) after a first predetermined switchover time tAOND (pink) and is then set to a second resistance value (infinite, closed circuit) after a second predetermined switchover time (green) based on a burst length of 8. EX1005 at 5:23-42; EX1003 at ¶¶ 98-99.

⁶ Indeed, Polaris also interprets claims 1 and 2 such that the time delays and the predetermined switchover times may be the same. *See* EX1011 at ¶¶ 52-53.

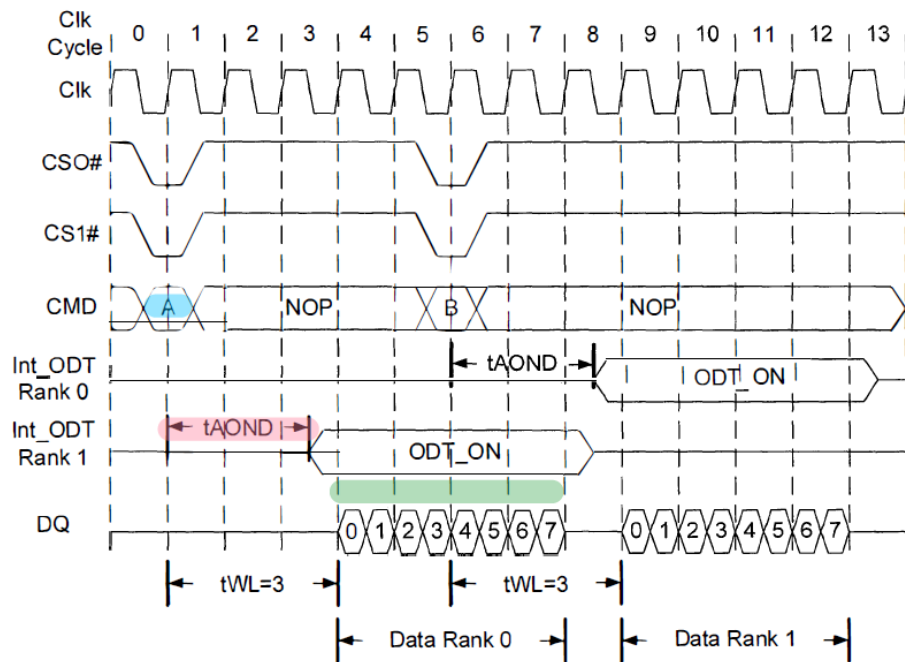


FIG. 7

b. Mapping to Finite Resistances Associated with A1 and A2 Commands

The first and second resistance values recited in claim 2 are also disclosed by the two different finite resistance values applied when a command A1 is followed by a command A2. As explained above, the number of switches closed by control circuit 32 is a function of the control command signal received by the control circuit 32. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. Thus, in the situation where commands A1 and A2 are asserted back-to-back, switches Sw1-D...SwN-D and Sw1-S...SwM-S would cause

“one level of resistance in the ODT” followed by “another level of resistance.”

EX1003 at ¶ 100.

The above scenario is illustrated in the following modified version of timing diagram Fig. 7, where commands A1 (orange) and A2 (yellow) are different commands to rank 0,⁷ each causing termination to be applied to rank 1. When command A1 is asserted, rank 1 is terminated with a first resistance value (light purple) after a first predetermined switchover time (grey). When command A2 is asserted, rank 1 is terminated with a second resistance value (dark purple) after a second predetermined switchover time (dark green). EX1005 at Fig. 7 (modified and annotated). And as noted above with respect to limitation [1.6], the first delay runs the same length of time as the first switchover time (tAOND), but is triggered by an ODT “on” signal received on an ODT pin at the same time as command A1. Similarly, the second delay would be triggered by an ODT “off” signal received on

⁷ Bains does not specify what type of commands A1 and A2 might be. A POSITA would have understood and also found obvious from Bains’ disclosure that these two commands could be any commands with which termination might be needed or desired. For example, commands A1 and A2 might be a write command and a read command, respectively. Alternatively, A2 could be a chip select signal or a no operation command. *See* EX1006 at 57, Table 10.

an ODT pin after the A2 command (timed by the controller sending the ODT off signal to end termination once the operation associated with the A2 command has been accomplished). EX1003 at ¶¶ 101-102; EX1009 at 8:42-9:32, Figs. 10A-10C.

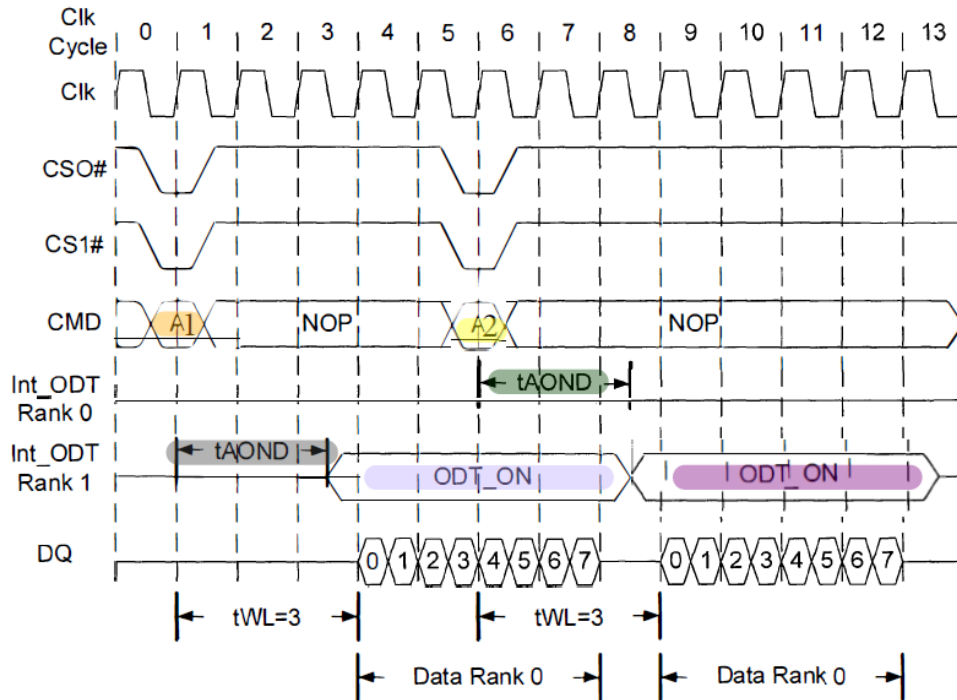


FIG. 7

3. Claim 5

a. “A system, comprising:” [5.P]

Claim 5 is similar to claim 1, but it recites additional system components, including a memory controller, a memory bus, and a plurality of memory chips, at least one chip having the features of claim 1. *Supra* Section X.A.1; EX1003 at ¶ 103.

To the extent the preamble is limiting, Bains teaches a memory system comprising a memory controller 12 and memory chips MC0 and MC1 coupled by various buses. EX1005 at 2:33-46, Fig. 2. Exemplary memory chip MC0 has an ODT circuit 38 that may terminate a data pad with an infinite resistance or different finite resistances depending on the command A1 or A2 provided to the chip from the memory controller 12. EX1005 at 2:33-52, 3:41-58, 4:39-61, Figs. 2 and 4 (each figure reproduced below); EX1003 at ¶ 104.

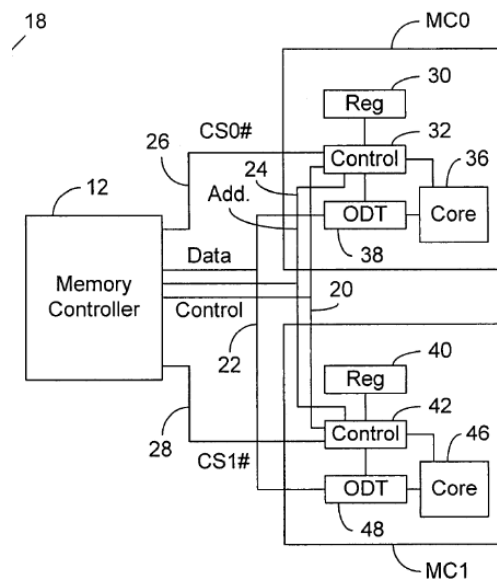


FIG. 2

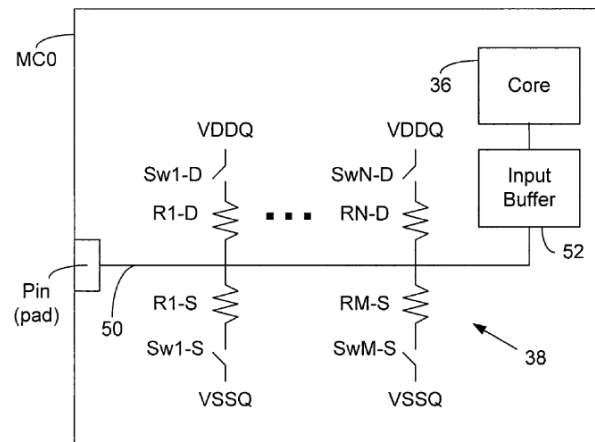


FIG. 4

b. “(a) a memory controller having a terminal;” [5.1]

Bains teaches this limitation. As shown below in annotated Fig. 2, Bains teaches a memory system comprising a memory controller 12 with terminals

connected to a control bus 20, data bus 22, address bus 24, and chip select buses 26 and 28, through which the memory controller communicates with memory chips MC0 and MC1. EX1005 at 3:9-16, Fig. 2 (annotated and reproduced below). EX1003 at ¶¶ 105-06.

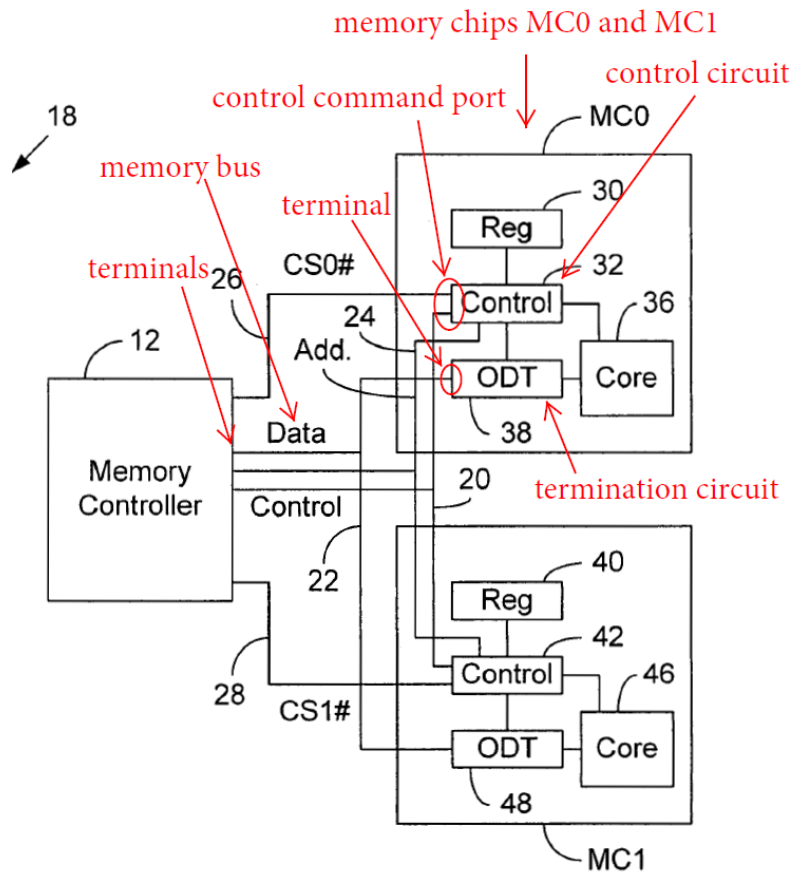


FIG. 2

c. “(b) a plurality of memory chips, at least one of the memory chips comprising:” [5.2]

Bains also teaches this limitation. As shown in annotated Fig. 2 above, the memory system comprises at least two memory chips MC0 and MC1. EX1005 at

2:33-36, Fig. 2; *see also* Figs. 5 and 6 (showing other embodiments with multi-chip/multi-bank memory modules). EX1003 at ¶ 107.

d. “a terminal” [5.3]

As explained above with respect to limitation [1.1], Bains teaches limitation [5.3]. *Supra* Section X.A.1.b; *see* EX1005 at Fig. 4; EX1001 at 2:45-48, Fig. 1; EX1003 at ¶ 108.

e. “a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;” [5.4]

As explained above with respect to limitation [1.2], Bains teaches limitation [5.4]. *Supra* Section X.A.1.c; *see* EX1005 at 4:31-44, Figs. 2, 4; EX1003 at ¶ 109.

f. “a control command port for receiving a control command signal for affecting the accessibility of the memory chip; and” [5.5]

As explained above with respect to limitation [1.3], Bains teaches limitation [5.5]. *Supra* Section X.A.1.d; *see* EX1005 at 3:9-20, 3:37-4:6, Fig. 2; EX1003 at ¶ 110.

g. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;” [5.6]

As explained above with respect to limitation [1.4], Bains teaches limitation [5.6]. *Supra* Section X.A.1.e; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs. 2, 4; EX1003 at ¶ 111.

h. “(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and” [5.7]

Bains further teaches limitation [5.7]. As shown in annotated Fig. 2, below, the system includes a memory bus 22 interconnecting the terminals of the memory chips MC0 and MC1 and the terminal of the memory controller 12. EX1005 at 3:9-16, Fig. 2; EX1003 at ¶ 112.

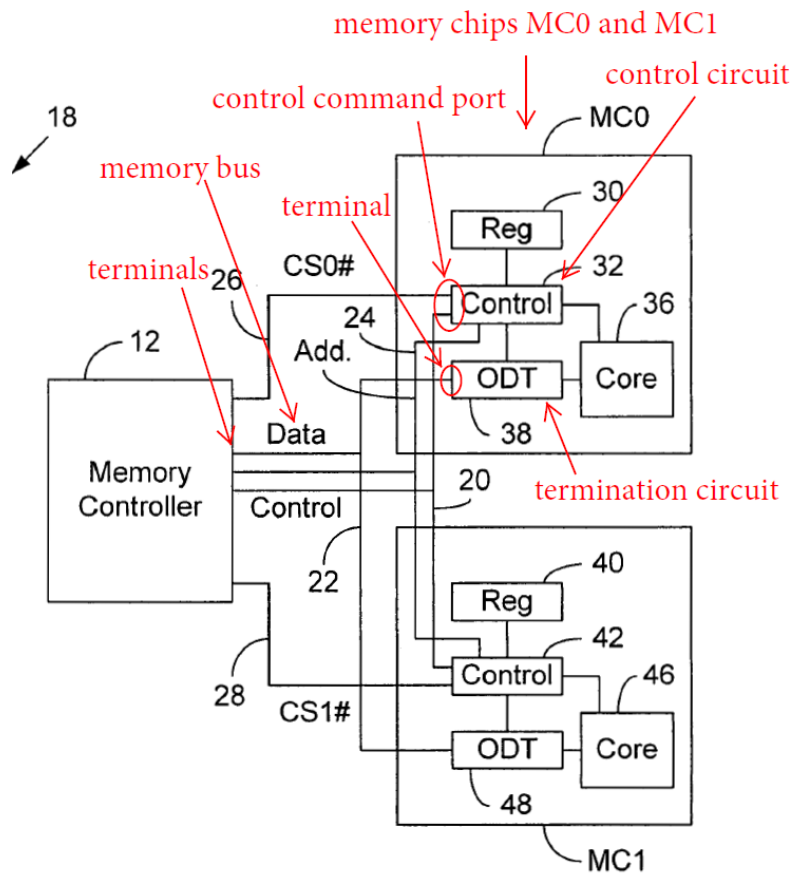


FIG. 2

i. “(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory

chip with the set resistance value in response to the termination signal,” [5.8]

As explained above with respect to limitation [1.5], Bains teaches limitation [5.8]. *Supra* Section X.A.1.f; *see* EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig. 1; EX1003 at ¶ 113.

j. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.” [5.9]

As explained above with respect to limitation [1.6], Bains teaches limitation [5.9]. *Supra* Section X.A.1.g; *see* EX1005 at 1: 37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16; EX1003 at ¶ 114.

4. Claim 6: “The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

As explained above with respect to claim 2, Bains teaches the limitations of claim 6. *Supra* Section X.A.2; *see* EX1005 at 4:39-44, 5:23-42, Fig. 7; EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1006 at Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53; EX1003 at ¶ 115.

5. Claim 9

a. “A method for operating a memory chip, comprising:” [9.P]

Claim 9 is similar to claims 1 and 5, above. In particular, claim 9 recites various method steps corresponding to functionalities recited in claims 1 and 5. To the extent that the preamble is limiting, Bains teaches the limitation. In particular, Bains teaches a system and method for operating a memory chip (e.g., MC0) having an ODT circuit 38. EX1005 at 2:33-67, Fig. 2; EX1003 at ¶ 116.

b. “receiving a control command signal for affecting accessibility of the memory chip” [9.1]

As explained above with respect to limitation [1.3], Bains teaches limitation [9.1]. *Supra* Section X.A.1.d; *see* EX1005 at 3:9-20, 3:24-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51; EX1003 at ¶ 117.

c. “setting a resistance value for a terminal as a function of the control command signal;” [9.2]

As explained above with respect to limitation [1.4], Bains teaches limitation [9.2]. *Supra* Section X.A.1.e; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs. 2, 4; EX1003 at ¶ 118.

d. “terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable

signal, the first time delay being selected such that the selected terminating resistor can be set; and” [9.3]

As an initial matter, “the termination enable signal” in limitation [9.3] lacks proper antecedent basis. However, if “the termination enable signal” is meant to refer to the later-claimed “termination enable signal,” Bains teaches this limitation. As explained above with respect to limitation [1.6], Bains teaches limitation [9.3]. *Supra* Section X.A.1.g; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16; EX1003 at ¶ 119.

e. “receiving a termination enable signal, the presence of which is required for the terminating to occur.” [9.4]

As explained in the previous section and with respect to limitation [1.5], Bains teaches a termination enable signal received via an ODT pin which turns termination on and off. *Supra* Section X.A.5.d; *supra* Section X.A.1.f; EX1005 at 6:30-37; EX1001 at 1:37-45, Fig. 1; EX1003 at ¶ 120.

6. Claim 10: “The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.”

Claim 10 is substantively the same as claim 2. In particular, claim 2 describes how the “resistance value” is set to a “first resistance value” after a “first predetermined switchover time” and is set to a “second resistance value” after a “second predetermined switchover time.” As explained above with respect to claim

2, Bains teaches the limitations of claim 10. *Supra* Section X.A.2; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53.

The “changed resistance value” in claim 10 may be met by either (a) the finite resistance (dark blue) applied as a result of a first command A (light blue), where the resistance value changes from an infinite value to a finite value after a switchover time t_{AOND} (pink) relative to command A; (b) the infinite resistance applied after a switchover time based on the burst length (green) associated with the first command A (light blue), where the resistance value changes from a finite value (dark blue) to an infinite value; or (c) the finite resistance (dark purple) applied as a result of a second command A2 (yellow) that follows a first command A1 (orange), where the resistance value changes from a first finite value (light purple) to a second finite value (dark purple) after a switchover time t_{AOND} (dark green) relative to command A2 (yellow). EX1005 at Fig. 7 (annotated and modified versions below); EX1003 at ¶ 121.

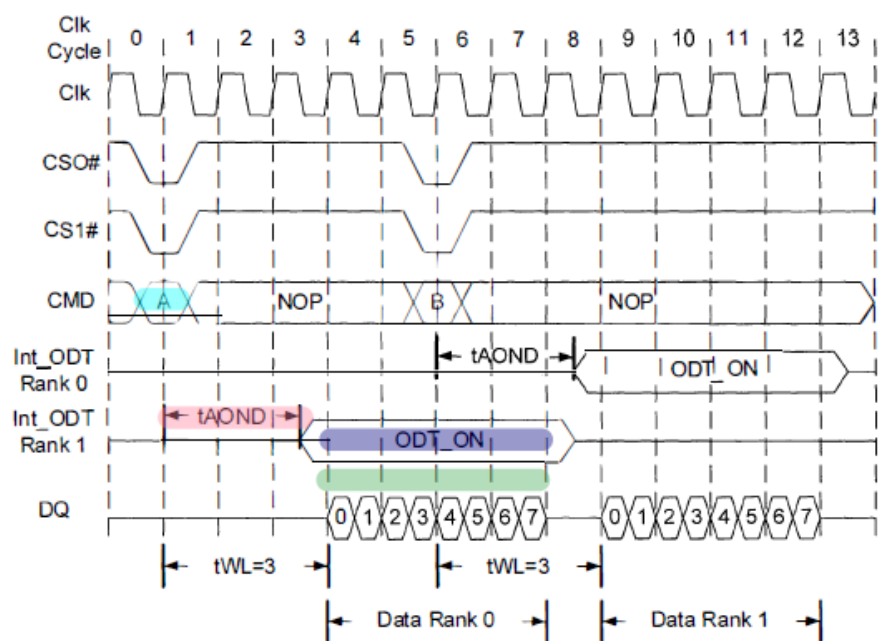


FIG. 7

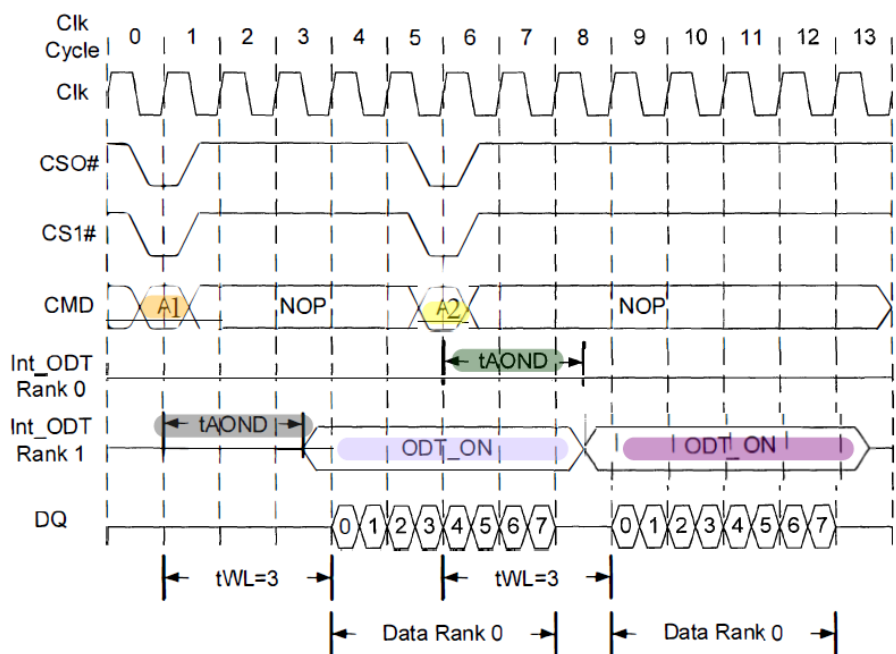


FIG. 7

B. Ground 2: Claims 1, 2, 5, 6, 9, and 10 are obvious over Bains in view of JESD79-2A

1. Motivation to Combine Bains and JESD79-2A

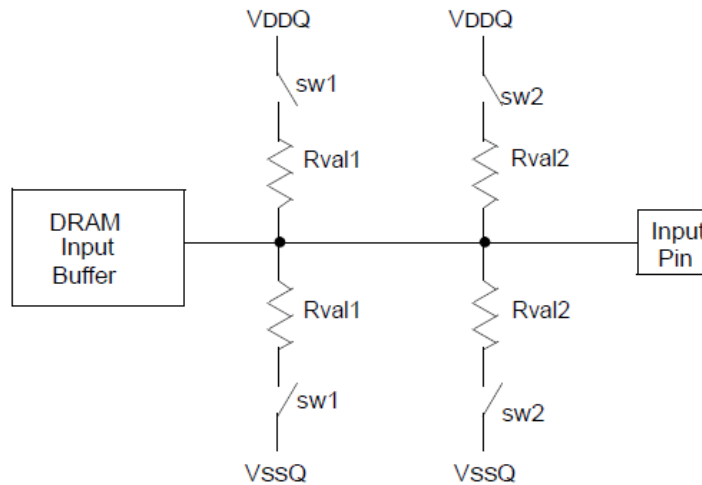
To the extent that Patent Owner argues that claims 1, 2, 5, 6, 9, and 10 of the '523 Patent are not taught by Bains alone, claims 1, 2, 5, 6, 9, and 10 are also obvious over Bains in view of JESD79-2A. As explained below, JESD79-2A teaches a DDR2 SDRAM with on die termination having an ODT pin for turning termination on and off. EX1006 at 14, 26. JESD79-2A provides further details not expressly disclosed in Bains regarding the operation of the ODT pin and associated signaling, further supporting how a POSITA would understand Bains' teaching of using both control commands and an ODT pin to accomplish ODT. EX1003 at ¶¶ 122-23.

A POSITA would have been motivated to combine Bains with JESD79-2A and would have had a reasonable expectation of success in doing so, because (a) JESD79-2A was and remains a well-known memory standard published by the preeminent memory standards setting organization, (b) Bains specifically teaches that the system may use ODT pins to control the termination, and (c) Bains refers to JEDEC's DDR2 standards with respect to the use of ODT pins. EX1005 at 1:37-45, 6:31-37. Thus, to the extent that Bains does not sufficiently describe the use of ODT pins in its system, a POSITA would have been motivated by Bains' own disclosure to implement the ODT pin design taught by JESD79-2A in the memory

system taught by Bains. This configuration may permit for more complex termination schemes and more customizable termination timing than a command-only control system. For example, by asserting the ODT enable signal before a command, ODT could be turned “on” before a command is asserted. By providing an ODT pin, a POSITA would also ensure compliance with JEDEC standards, which is essential for interoperability. Furthermore, this straightforward modification simply applies a known technique (e.g., termination control with an ODT pin) to improve a similar device (e.g., Bains’ on die termination circuit with command-based resistance control) in the same way to yield predictable results (e.g. ODT control using an ODT specific signal, and resistance level control using commands). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); EX1003 at ¶¶ 124-25.

In particular, and just like Bains, JESD79-2A teaches that the ODT pin in a DDR2 SDRAM turns termination on and off by controlling whether switches sw1 and sw2 in the termination circuit are enabled. EX1006 at 22, 27, Fig. 15. As shown below in Fig. 15, each set of switches sw1 and sw2 is connected to associated resistors Rval1 and Rval2 which cause a different level of resistance to be applied to the pin. However, only one set of switches, sw1 or sw2, are enabled at a time. EX1003 at ¶ 126.

2.2.2.4 ODT (On Die Termination) (cont'd)

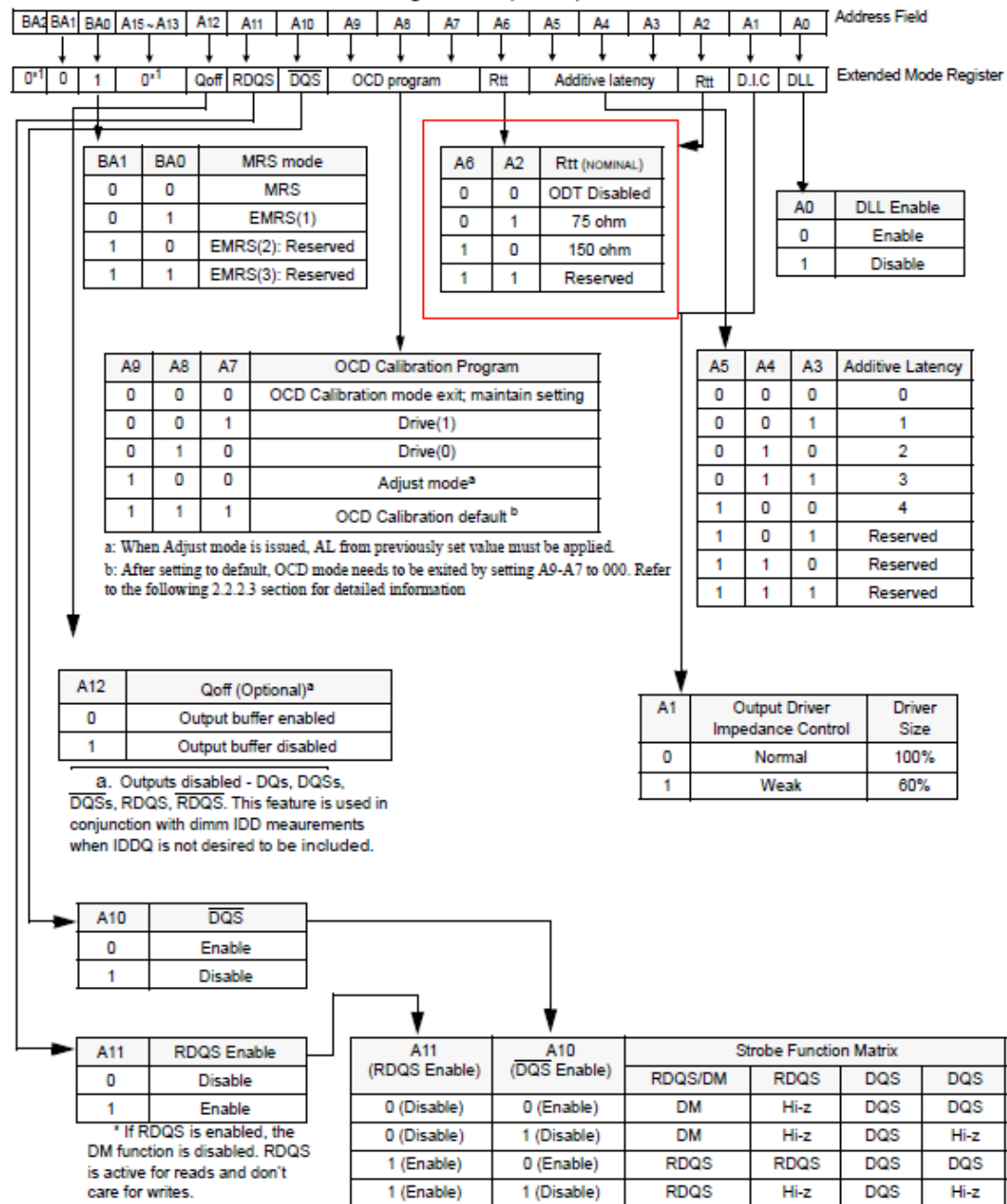


Switch sw1 or sw2 is enabled by ODT pin.
 Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
 Termination included on all DQs, DM, DQS, $\overline{DQS}$, RDQS, and $\overline{RDQS}$ pins.
 Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

The selection between sw1 or sw2—and thus, between the different resistances—is determined by bits A2 and A6 that are written in the EMRS. EX1006 at 27, Fig. 9. For example, if Rval1 is associated with an effective resistance of 75 ohms, and Rval2 is associated with an effective resistance of 150 ohms, then switches sw1 are selected when bit A6 is set to 0 and bit A2 is set to 1, and switches sw2 are selected when bit A6 is set to 1 and bit A2 is set to 0. EX1006 at 27, Fig. 9. When a high level is applied to the ODT pin, switches sw1 or sw2 are closed depending on the values of bits A2 and A6. EX1003 at ¶ 127.

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)



^{*} BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.

Figure 9 — EMRS(1) Programming

Bains teaches a nearly identical termination circuit with switches Sw1 to SwN and associated resistors R1 to RN, where the “number of switches closed may determine the amount of resistance in the termination.” EX1005 at 4:26-46,

Fig. 4. In its illustrated embodiments, instead of using the EMRS to determine which switches should be closed, Bains uses the control command signals. “For example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:26-46; EX1003 at ¶ 128.

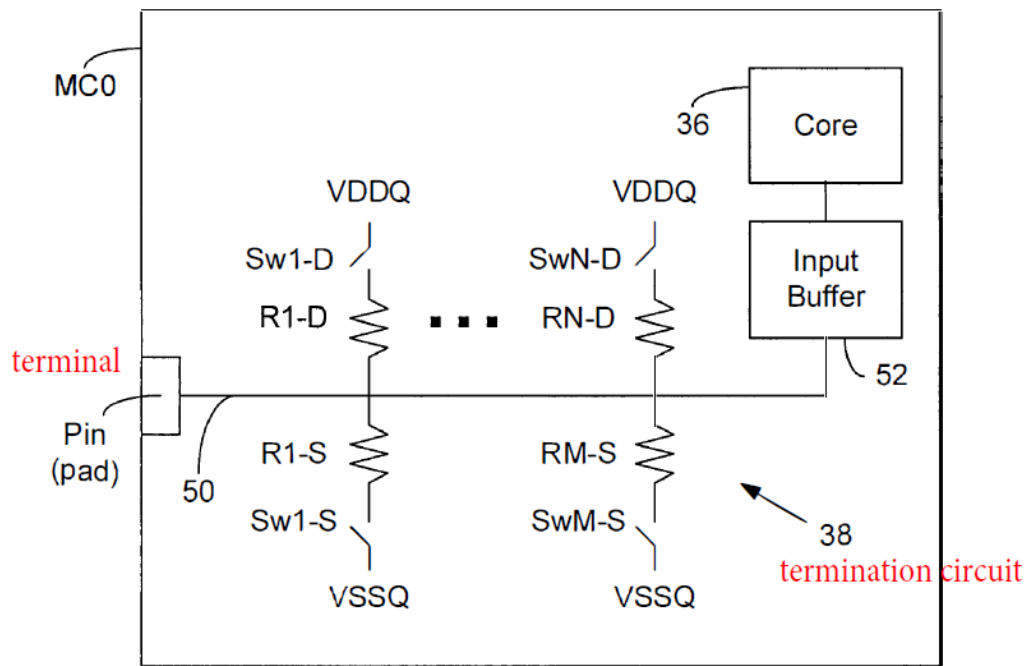


FIG. 4

However, as discussed above, Bains also discloses unillustrated embodiments that use an ODT pin. EX1005 at 6:30-37. Thus, Bains itself provides a teaching, suggestion, and motivation to modify the illustrated embodiments of Bains by adding an ODT pin, and it specifically refers to the DDR2 standard (a version of which is JESD79-2A) for an explanation of such ODT pins. *Comaper*

Corp. v. Antec, Inc., 596 F.3d 1343, 1351 (Fed. Cir. 2010) (The obviousness analysis “typically invokes the familiar teaching-suggestion-motivation (“TSM”) test, asking whether a person having ordinary skill in the art would have found some teaching, suggestion, or motivation to combine or modify the prior art references.”); *Ortho-McNeil Pharm., Inc. v. Mylan Lab’ys, Inc.*, 520 F.3d 1358, 1365 (Fed. Cir. 2008) (“As *KSR* requires, those teachings, suggestions, or motivations need not always be written references but may be found within the knowledge and creativity of ordinarily skilled artisans.”). In the combined system taught by Bains and JESD79-2A, the resistance value to be applied is a function of the control command signals as disclosed in Bains, and the ODT pin detailed in JESD79-2A is used to control when the switches are enabled to apply the selected resistance. As illustrated in Fig. 16 of JESD79-2A, below, the signal on the ODT pin determines when to apply the termination resistance.⁸ Specifically, termination is applied after a period tAOND after the ODT signal is enabled (goes high), and termination ends after a period tAOFD after the ODT signal is disabled (goes low). EX1006 at 27, Fig. 16. In the combination, the signal on the ODT pin controls

⁸ The value of the termination to be applied is determined in JESD79-2A by the setting of EMRS bits, but the proposed combination uses Bains’ improved technique of using the type of command to indicate the resistance to be applied.

when the switches are enabled according to first and second time delays t_{AOND} and t_{AOFD} , respectively, and control command signals A1, A2 through AN control which particular resistance level is applied. EX1003 at ¶ 129.

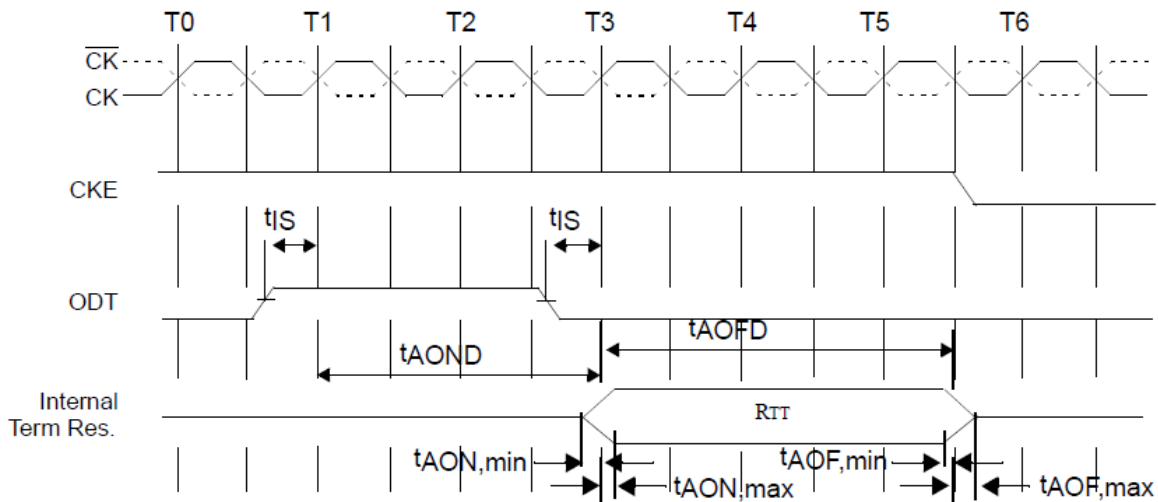


Figure 16 — ODT Timing for Active/Standby Mode

A POSITA would have had a reasonable expectation of success in combining Bains and JESD79-2A because the termination circuits taught by Bains and JESD79-2A are structurally similar, and Bains' control commands and JESD79-2A's EMRS bits serve analogous resistance setting functions. A POSITA would have understood that an ODT on/off pin could be used in a system with EMRS resistance control or control command resistance control to achieve the same end: separate control mechanisms for the timing of ODT and the value of ODT resistance. Thus, the combination involves the simple substitution of one known element (ODT on/off pin) for another (ODT on/off control using

commands) to yield predictable results. This configuration also simplifies the system taught by Bains. Using this setup, a POSITA would not need to program chips in one rank to recognize command A as a write and chips in another rank to recognize command A as a termination command. EX1005 at 3:37-4:19. Instead, an ODT signal would be used to control which chips are terminated and when. EX1003 at ¶¶ 130-31.

2. Claim 1

a. “A memory chip for variably setting terminations, comprising:” [1.P]

As explained above for Ground 1, Bains teaches the preamble of claim 1, to the extent it is limiting. *Supra* Section X.A.1.a; *see* EX1005 at 2:33-52, 3:41-58, 4:39-61, Figs. 2, 4, and 5; EX1003 at ¶ 132.

b. “a terminal;” [1.1]

As explained above for Ground 1, Bains teaches claim limitation [1.1]. *Supra* Section X.A.1.b; *see* EX1005 at Fig. 4; EX1001 at 2:45-48, Fig. 1; EX1003 at ¶ 133.

c. “a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;” [1.2]

As explained above for Ground 1, Bains teaches claim limitation [1.2]. *Supra* Section X.A.1.c; *see* EX1005 at 4:31-44, Figs. 2, 4; EX1003 at ¶ 134.

d. “a control command port for receiving a control command signal for affecting accessibility of the memory chip;” [1.3]

As explained above for Ground 1, Bains teaches claim limitation [1.3].

Supra Section X.A.1.d; *see* EX1005 at 3:9-20, 3:24-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51; EX1003 at ¶ 135.

e. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and” [1.4]

As explained above for Ground 1, Bains teaches claim limitation [1.4].

Supra Section X.A.1.e; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs. 2, 4; EX1003 at ¶ 136.

f. “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,” [1.5]

As explained above for Ground 1, Bains teaches claim limitation [1.5].

Supra Section X.A.1.f; *see* EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig.

1. To the extent that Patent Owner argues that Bains alone does not teach claim limitation [1.5], this limitation is taught by Bains in view of JESD79-2A. Bains teaches that the control command signals control whether ODT is “on” as well as the level of ODT resistance. *Supra* Section X.A.1.e. As shown in Fig. 4 below, control circuit 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off,” where the number of switches that are closed

may determine the amount of resistance that is applied to the data pin. EX1005 at 4:40-42, Fig. 4. The number of switches closed is a function of the received control command signal. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. However, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands. EX1005 at 6:30-37; EX1003 at ¶ 137.

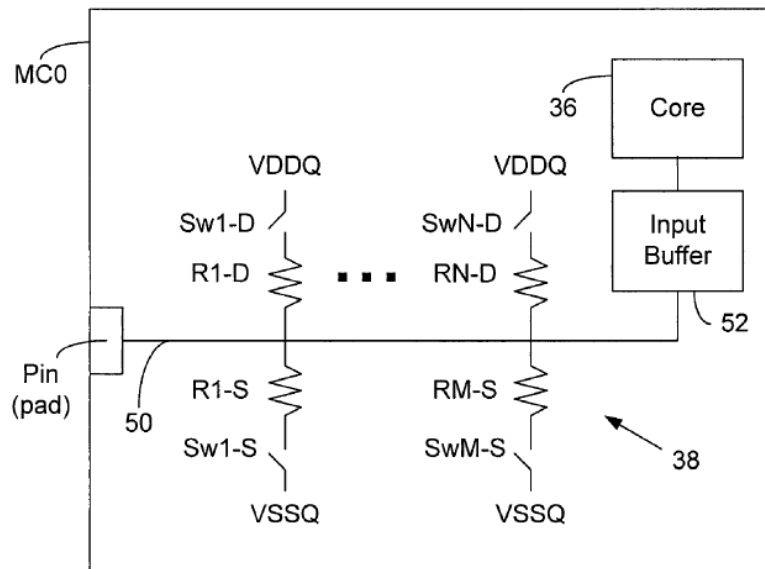


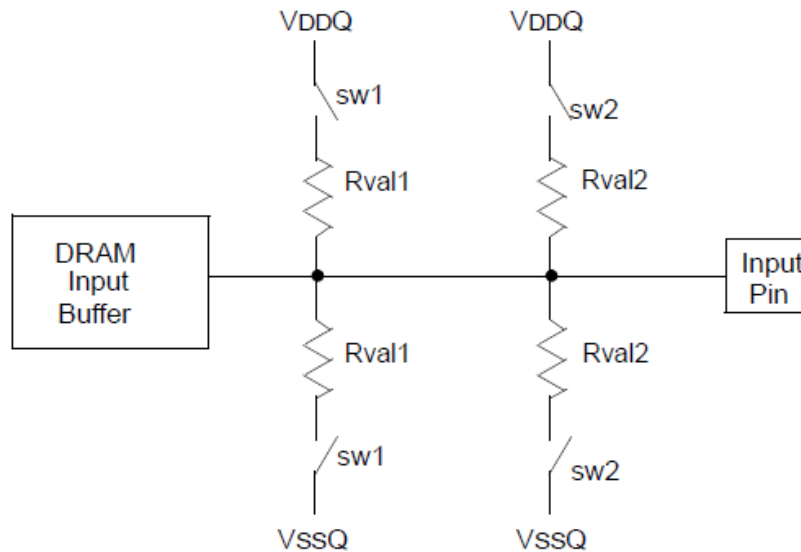
FIG. 4

JESD79-2A teaches a DDR2 SDRAM with an ODT pin for turning termination on and off. EX1006 at 22, 27. In particular, as shown in Fig. 15 below, the ODT pin determines whether switches sw1 or sw2 in the termination circuit are

enabled, where selection between sw1 or sw2 is determined by the EMRS.

EX1006 at 27, Fig. 15; EX1003 at ¶ 138.

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.

Selection between sw1 or sw2 is determined by "R_{tt} (nominal)" in EMRS

Termination included on all DQs, DM, DQS, $\overline{DQS}$, RDQS, and $\overline{RDQS}$ pins.

Target R_{tt} (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

In the combined system taught by Bains and JESD79-2A, the resistance value to be applied is a function of the control command signals as disclosed in Bains, and the ODT pin detailed in JESD79-2A is used to control when the switches are enabled to apply the selected resistance. In other words, the ODT pin controls when the switches are enabled according to first and second time delays tAOND and tAOFD, respectively (see Fig. 16, below), and control command

signals A1, A2 through AN control which resistance level is applied, as discussed in Ground 1 with respect to limitation [1.4]. EX1006 at 27; EX1003 at ¶ 139.

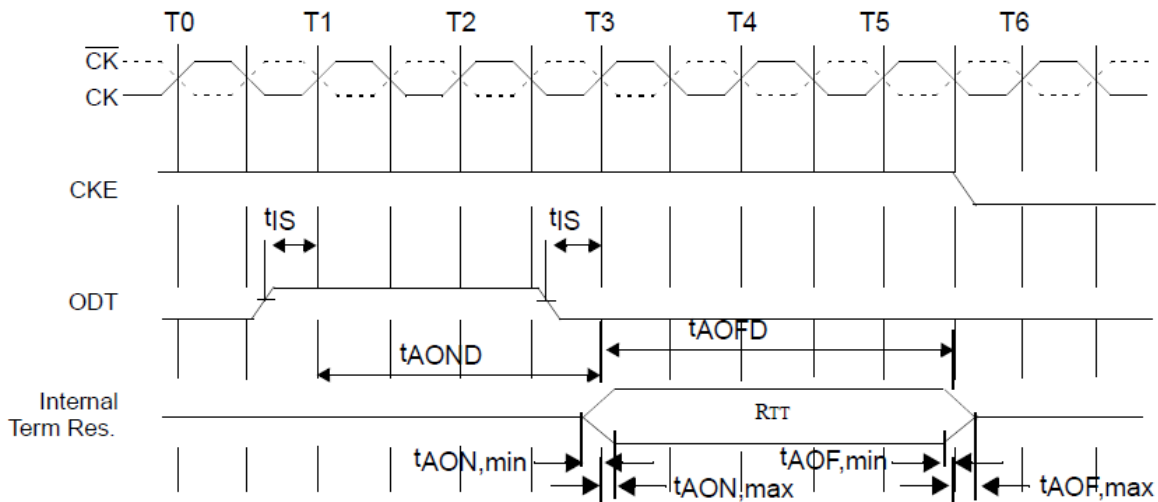


Figure 16 — ODT Timing for Active/Standby Mode

g. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.” [1.6]

As explained above with respect to limitation [1.5] in Ground 2, Bains as modified by JESD79-2A teaches claim limitation [1.6]. *Supra* Section X.B.2.f.; see EX1006 at Fig. 16. Specifically, Bains as modified by JESD79-2A teaches that the chip’s control circuit terminates the terminal as a function of the termination signal ODT (pink) after a first time delay t_{AOND} (green) that runs from when the ODT signal goes high (on), and does not terminate the terminal after a second time delay t_{AOFD} (purple) that runs from when the ODT signal goes low (off). EX1006 at

Fig. 16 (annotated below). The values of the first and second delays t_{AOND} and t_{AOFD} are further described in Table 36. EX1006 at 73; EX1003 at ¶ 140.

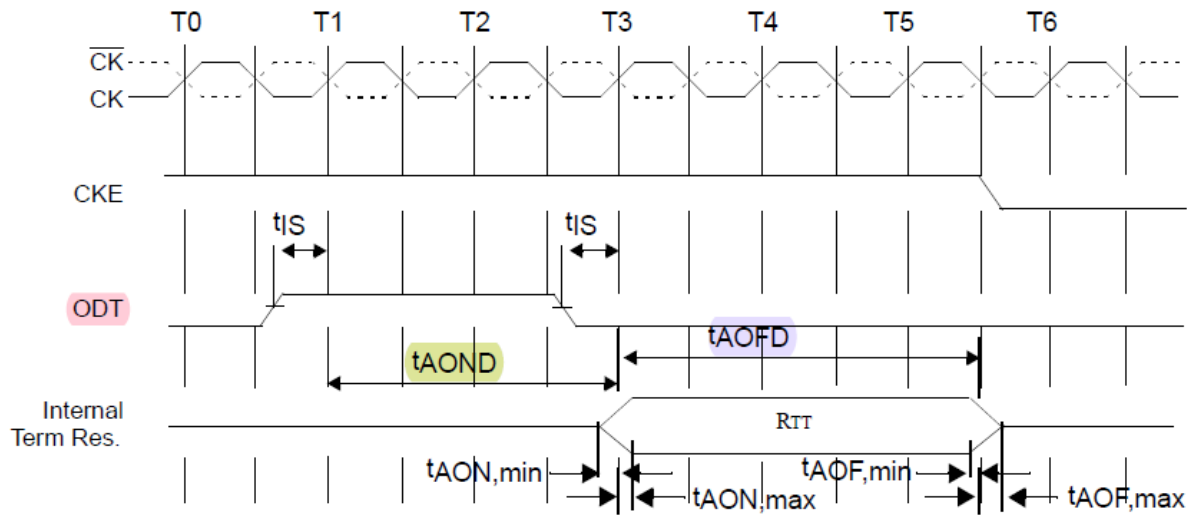


Figure 16 — ODT Timing for Active/Standby Mode

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
DQ output access time from CK/ CK	tAC	-600	+600	-500	+500	ps	
DQS output access time from CK/ CK	tDQSCK	-500	+500	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
DQ and DM input hold time	tDH	400	x	350	x	ps	6,7,8,18
DQ and DM input setup time	tDS	400	x	350	x	ps	6,7,8,18
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/CK	tHZ	x	tAC max	x	tAC max	ps	
Data-out low-impedance time from CK/CK	tLZ	tAC min	tAC max	tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13
DQ hold skew factor	tQHS	x	450	x	400	ps	12

Table 36 — Timing Parameters by Speed Grade (DDR2-400 and DDR2-533)

(Refer to notes for information related to this table at the bottom)

Parameter	Symbol	DDR2-400		DDR2-533		Units	Notes
		min	max	min	max		
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	t _{CKE}	3		3		tCK	
ODT turn-on delay	t _{AOND}	2	2	2	2	tCK	
ODT turn-on	t _{AON}	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	t _{AONPD}	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
ODT turn-off delay	t _{AOFD}	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	t _{AOF}	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17
ODT turn-off (Power-Down mode)	t _{AOFPD}	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

Furthermore, because the termination actually does occur after tAOND in the timing diagram of Fig. 16, a POSITA would understand that the first time delay tAOND is sufficiently long enough for the switches Sw1 and Sw2 to close and set the resistance value. It also would have been obvious to a POSITA that tAOND would be long enough to set and apply the resistance value because otherwise, at

least some of the data would be transmitted on the signal line without the proper termination in place, reducing the signal quality. EX1003 at ¶ 141.

3. Claim 2: “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

As explained above for Ground 1, Bains teaches the additional limitations of claim 2. *Supra* Section X.A.2; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53. In particular, Bains teaches that the first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2. EX1003 at ¶ 142.

4. Claim 5

a. “A system, comprising:” [5.P]

As explained above for Ground 1, to the extent that the preamble is limiting, Bains teaches limitation [5.P]. *Supra* Section X.A.3.a; *see* EX1005 at 2:33-52, 3:41-58, 4:39-61, Figs. 2 and 4; EX1003 at ¶ 143.

b. “(a) a memory controller having a terminal;” [5.1]

As explained above for Ground 1, Bains teaches limitation [5.1]. *Supra* Section X.A.3.b; *see* EX1005 at 3:9-16, Fig. 2; EX1003 at ¶ 144.

c. “(b) a plurality of memory chips, at least one of the memory chips comprising:” [5.2]

As explained above for Ground 1, Bains teaches limitation [5.2]. *Supra* Section X.A.3.c; *see* EX1005 at 2:33-36, Figs. 2, 5, and 6; EX1003 at ¶ 145.

d. “a terminal” [5.3]

As explained above for Ground 1, Bains teaches limitation [5.3]. *Supra* Section X.A.3.d; *see* EX1005 at Fig. 4; EX1001 at 2:45-48, Fig. 1; EX1003 at ¶ 146.

e. “a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;” [5.4]

As explained above for Ground 1, Bains teaches limitation [5.4]. *Supra* Section X.A.3.e; *see* EX1005 at 4:31-44, Figs. 2, 4; EX1003 at ¶ 147.

f. “a control command port for receiving a control command signal for affecting the accessibility of the memory chip; and” [5.5]

As explained above for Ground 1, Bains teaches limitation [5.5]. *Supra* Section X.A.3.f; *see* EX1005 at 3:9-20, 3:24-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51; EX1003 at ¶ 148.

g. “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;” [5.6]

As explained above for Ground 1, Bains teaches limitation [5.6]. *Supra* Section X.A.3.g; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs. 2, 4; EX1003 at ¶ 149.

h. “(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and” [5.7]

As explained above for Ground 1, Bains teaches limitation [5.7]. *Supra* Section X.A.3.h; *see* EX1005 at 3:9-16, Fig. 2; EX1003 at ¶ 150.

i. “(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,” [5.8]

As explained above for Ground 1, Bains teaches limitation [5.8]. *Supra* Section X.A.3.i; *see* EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-44, Fig. 1. In addition, the limitation is also taught by Bains in view of JESD79-2A, as explained with respect to limitation [1.5], above. *Supra* Section X.B.2.f; *see* EX1005 at 4:40-44, 6:30-37, Fig. 4; EX1006 at 22, 27, Figs. 15 and 16; EX1003 at ¶ 151.

j. “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in

accordance with a second time delay, the first time delay being sufficient to set the resistance value.” [5.9]

As explained above for Ground 1, Bains teaches limitation [5.9]. *Supra* Section X.A.3.j; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006 at Fig. 16; EX1003 at ¶ 152.

5. Claim 6: “The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

As explained above for Ground 1, Bains teaches the limitations of claim 6. *Supra* Section X.A.4; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53. In particular, Bains teaches that the first and second resistance values recited in claim 6 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2. EX1003 at ¶ 153.

6. Claim 9

a. “A method for operating a memory chip, comprising:” [9.P]

As explained above for Ground 1, to the extent the preamble is limiting, Bains teaches limitation [9.P]. *Supra* Section X.A.5.a; *see* EX1005 at 2:33-67, Fig. 2; EX1003 at ¶ 154.

b. “receiving a control command signal for affecting accessibility of the memory chip” [9.1]

As explained above for Ground 1, Bains teaches limitation [9.1]. *Supra* Section X.A.5.b; *see* EX1005 at 3:9-20, 3:24-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51; EX1003 at ¶ 155.

c. “setting a resistance value for a terminal as a function of the control command signal;” [9.2]

As explained above for Ground 1, Bains teaches limitation [9.2]. *Supra* Section X.A.5.c; *see* EX1005 at 3:17-20, 3:41-58, 4:39-44, Figs 2 and 4; EX1003 at ¶ 156.

d. “terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and” [9.3]

As explained above for Ground 1, Bains teaches limitation [9.3]. *Supra* Section X.A.5.d; *see* EX1005 at 1:37-45, 4:47-61, 5:23-42, Figs. 2, 5, 7; EX1006

at Fig. 16; EX1003 at ¶¶ 54-58. In addition, Bains in view of JESD79-2A teaches the limitation. This is explained with respect to limitations [1.5] and [1.6] in Ground 2. *Supra* Section X.B.2.f-g; *see* EX1005 at 4:40-44, 6:30-37, Fig. 4; EX1006 at 22, 27, 73, Figs. 15, 16; EX1003 at ¶ 157.

e. “receiving a termination enable signal, the presence of which is required for the terminating to occur.” [9.4]

As explained above for Ground 1, Bains teaches limitation [9.4]. *Supra* Section X.A.5.e; EX1005 at 6:30-37, 1:37-45; EX1001 at 1:37-45, Fig. 1. The combination of Bains and JESD79-2A also teaches wherein the termination enable signal ODT is required to enable the switches in the termination circuit and cause terminating to occur. *Supra* Section X.B.2.f; EX1005 at 4:40-44, 6:30-37, Fig. 4; EX1006 at 22, 27, Figs. 15 and 16; EX1003 at ¶ 158.

7. Claim 10: “The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.”

As explained above for Ground 1, Bains teaches claim 10. *Supra* Section X.A.6; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53; EX1003 at ¶ 159.

XI. CONCLUSION

Accordingly, Petitioner requests *inter partes* review of claims 1, 2, 5, 6, 9, and 10 pursuant to Grounds 1 and 2 set forth above.

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Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 11,320 words, which is less than the 14,000 allowed under 37 C.F.R. § 42.24(a)(1)(i).

/Brian W. Oaks/

Brian W. Oaks

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(a), the undersigned certifies that on February 6, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, cost prepaid, to the Patent Owner by serving the correspondence address of record and another address known to Petitioner as likely to effect service, as follows:

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