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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner

Case IPR2023-00513

Patent 7,532,523

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Polaris Innovations Limited (“Polaris” or “Patent Owner”) submits this Preliminary Response to Xilinx, Inc.’s (“Xilinx” or “Petitioner”) Petition for *inter partes* review (“Petition”), challenging claims 1, 2, 5, 6, 9 and 10 (the “Challenged Claims”) of U.S. Patent No. 7,532,523 (the “’523 Patent”).

Petitioner alleges that the Challenged Claims are invalid based on two different grounds. First, Petitioner argues that the Challenged Claims are obvious over U.S. Patent No. 7,433,992 (Ex. 1003, “*Bains*”). Second, Petitioner argues that the Challenged Claims are obvious over *Bains* in view of the Joint Electron Device Engineering Council Double Data Rate 2 (DDR2) SDRAM Specification, version 79-2A (Ex. 1006, “*JESD79-2A*”).

The ’523 Patent concerns providing memory chips with a settable termination resistance. Generally, a termination uses resistors to match the impedance of a transmission line. If the resistance in the termination is not properly matched to the impedance of the transmission line signal reflection can occur. Signal reflection refers to the amount of a signal wave reflected by an impedance discontinuity. Signal reflection is undesirable because it can interfere with subsequent signal transmission.

The ’523 Patent claims a specific memory chip implementation that allows for a termination using various settable resistance values. In relevant part, each

Challenged Claim requires receiving a command control signal for “affecting accessibility” of the memory chip. Further, each of the Challenged Claims requires either a control circuit configured to selectively terminate the terminal “in response to the termination signal” or “receiving a termination enable signal” that “is required for the termination to occur.”

Petitioner failed to show that the Challenged Claims are unpatentable under Grounds 1 or 2. In particular, Petitioner failed to demonstrate that any of the references disclose the aforementioned requirements of the Challenged Claims. For example, the Petition rests on the assumption that operational commands, such as write, read, and refresh are the same as accessibility commands, such as chip select, row activation, column activation, and write enable. But they are not the same thing. It is well established that patent claims cannot be considered obvious if a single element is missing from the prior art. *See, e.g., CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)). Accordingly, Petitioner failed to carry its burden of demonstrating that the references disclose all elements of the Challenged Claims, requiring dismissal of the Petition.

Additionally, Petitioner failed to show a control circuit configured to act in response to a termination signal, which is a requirement of independent claims 1 and

5. In fact, Petitioner fails to show that any of the references disclose a control circuit that receives a termination signal, let alone one that acts in response to it. Similarly, Petitioner failed to show a termination enable signal whose presence is required for termination to occur, a requirement of independent claim 9. The Board should deny institution on these bases as well.

In summary, each of Petitioner's grounds are deficient in that they fail to show that *Bains* or *Bains* in combination with *JESD79-2A* teach or suggest every limitation of the Challenged Claims. Consequently, Petitioner cannot meet its burden for obviousness, and the Board should not institute IPR.

II. THE '523 PATENT AND THE CHALLENGED CLAIMS

A. Overview of the '523 Patent

The '523 Patent concerns memory chips that have a terminal for sending/receiving high frequency signals. Ex. 1001, 1:18-20. As the '523 Patent explains, a memory bus is often used to operate a memory chip. *Id.* at 1:23-24. The memory bus often connects signals, such as command signals, clock signals, and data signals, to the memory chip. *Id.* at 1:24-27. But the transmission of high-frequency signals over the memory bus can present a problem. *Id.* at 1:29-33. Signal reflections within the memory bus can interfere with data transmission and limit data transmission rates. *Id.* Providing a suitable termination at the terminal in the memory chip prevents such signal reflections. *Id.* at 1:33-36.

At the time of the '523 Patent, the solutions for providing the termination in memory chips were sub-optimal. One such sub-optimal solution was to “switch the termination on or off at a terminal of the memory chip as a function of the termination signal.” *Id.* at 1:37-39. But as the '523 Patent explains, this solution “is not sufficient as a rule to achieve an optimal termination in every operating state, and thus, also not sufficient to improve the data transmission via the memory bus.” *Id.* at 1:44-49. In other words, simply switching the termination on or off will not prevent signal reflection at various frequencies and will thus, limit data transmission rates.

Another sub-optimal solution was to set the strength of the termination resistors based on configuration values in an initialization phase. *Id.* at 1:50-54. But this approach is both “time consuming” and not suitable for providing an optimal termination for “every case of addressing the memory chips.” *Id.* at 1:55-62. As a result, setting the strength of termination resistors based on configuration values can result in access times being “slowed down substantially.” *Id.*

The '523 Patent provided an optimal solution to setting the termination resistance. The '523 Patent recognized that it was possible to achieve the optimal resistance at every operating state by setting “the resistance value as a function of the received control command signal.” Specifically, the '523 Patent discloses a

memory chip including a termination circuit with one or more terminating resistor(s) with settable resistance values. *Id.* at Fig. 1, 2; 2:40-3:14; 3:59-4:23. The termination circuit is connected to a control unit that can receive a termination signal from a termination port and a control command signal that affects the accessibility of the memory chip (e.g., chip select signal CS, write enable signal WE, row activation signal RAS, and Column activation signal CAS) from a control command port. *Id.* 3:25-58. The control unit acts in response to the termination signal by setting the resistance value of the terminating circuit as a function of the control command signal and connects the terminating circuit to the external terminal of the memory chip. *Id.* 3:25-58; 4:51-63; 5:23-28. The claimed invention of the '523 Patent thus allows a memory chip to be terminated with an optimal resistance value set specifically for every operating state when necessary.

B. Claim Overview

Independent claims 1, 5, and 9 are directed to a novel mechanism/method for terminating a terminal with a settable resistance. Patent Owner provides claims 1, 5, and 9 in full below, with the elements relevant to the Patent Owner's Preliminary Response highlighted in **bold**:

[1.P] A memory chip for variably setting terminations, comprising:

[1.1] a terminal;

- [1.2] a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;
- [1.3] a control command port for receiving **a control command signal for affecting accessibility of the memory chip**;
- [1.4] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and
- [1.5] a termination port to receive a termination signal, wherein **the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal**,
- [1.6] wherein the control circuit, **as a function of the termination signal**, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

...

[5.P] A system, comprising:

[5.1] (a) a memory controller having a terminal;

- [5.2] (b) a plurality of memory chips, at least one of the memory chips comprising:
- [5.3] a terminal;
- [5.4] a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;
- [5.5] a control command port for receiving **a control command signal for affecting accessibility of the memory chip**; and
- [5.6] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;
- [5.7] (c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and
- [5.8] (d) a termination port to receive a termination signal, wherein **the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal**,
- [5.9] wherein the control circuit, **as a function of the termination signal**, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and

(ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

...

[9.P] A method for operating a memory chip, comprising:

[9.1] receiving **a control command signal for affecting accessibility of the memory chip;**

[9.2] setting a resistance value for a terminal as a function of the control command signal;

[9.3] terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and

[9.4] receiving **a termination enable signal, the presence of which is required for the terminating to occur.**

The arguments in this Preliminary Response pertain to independent claims 1, 5, and 9, but are equally applicable to claims 2, 6, and 10 because each depends from claim

1, 5 or 9, respectively. As such, should the Board accept Patent Owner’s arguments that trial should not be instituted on claims 1, 5, and 9, it necessarily follows that trial should not be instituted on the dependent claims.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so if trial is instituted.

IV. CLAIM CONSTRUCTION

Patent Owner submits that the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“need only be construed ‘to the extent necessary to resolve the controversy’”).

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See Office Patent Trial Practice Guide*, 77 Fed. Reg. 48,756, 48,756 (Aug. 14, 2012) (“The Board . . . may

institute a trial where the petitioner establishes that the standards for instituting the requested trial are met . . .”).

Each of Petitioner’s Grounds relies on obviousness. Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries identified below.

A. Claims cannot be found obvious if an element is missing.

If a single element of the claim is absent from the prior art, the claim is not obvious. *See CFMT*, 349 F.3d at 1342 (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, Case No. IPR2012-00001, Paper 15 at 15 (P.T.A.B. Jan. 9, 2013) (refusing to institute an IPR under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

B. A petition must address the *Graham* factors.

Obviousness is resolved on a number of factual determinations including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). Petitions for IPR “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, No. IPR2014-00358, Paper 11 at 29-30 (P.T.A.B. July 23, 2014) (citing *Graham*, 383 U.S. at 17-18). For example, the Board faulted the petitioner in *Eizo Corporation* for failing to identify the differences between the claimed subject matter and the prior art. *Id.* at 29-30. In particular, the Board found insufficient the petitioner’s “conclusory assertion” that “[t]o the extent [the first reference] may not explicitly teach” the limitation, the second reference “explicitly teaches this limitation.” *Id.* at 30. The Board explained that “such an assertion *fails* to resolve the exact differences sought to be derived from” the second reference. *Id.* (finding that petitioner had not shown a reasonable likelihood of prevailing on that ground). Other Board decisions have reached the same result. *See, e.g., Moses Lake Indus., Inc. v. Enthone, Inc.*, Case No. IPR2014-00243, Paper 6 at 18 (P.T.A.B. June 18, 2014); *Moses Lake Indus., Inc. v. Enthone, Inc.*, No. IPR2014-00246, Paper 6 at 17 (P.T.A.B. June 18, 2014); *eBay, Inc. v. Paid, Inc.*, No. CBM2014-00125, Paper 15 at 21 (P.T.A.B. Sept. 30, 2014).

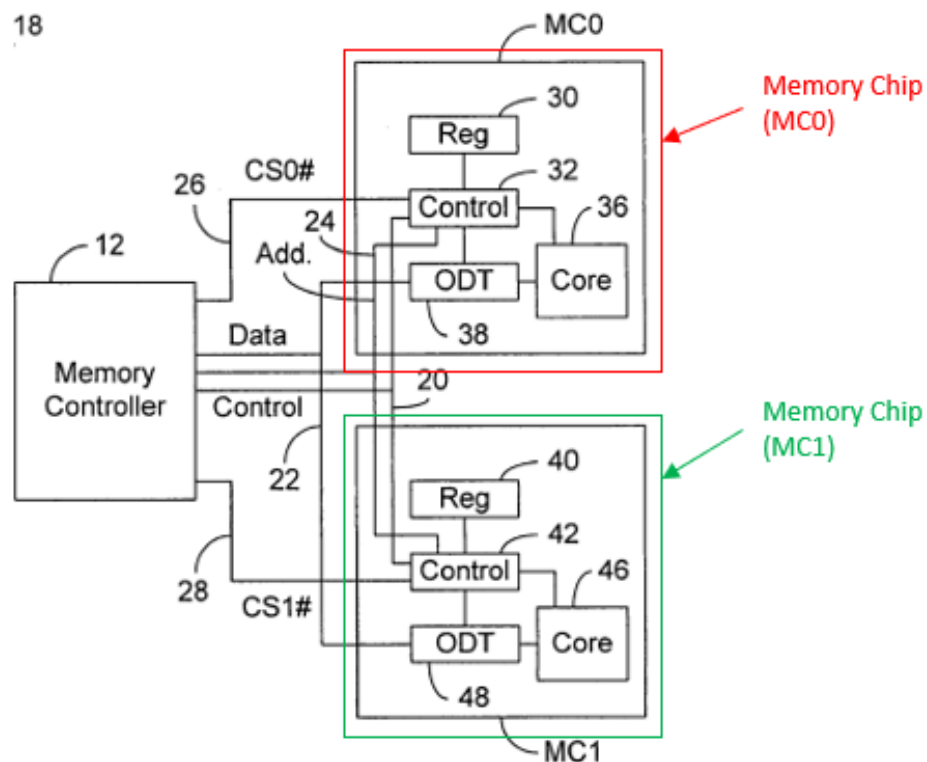
C. A petition must provide articulated reasoning with rational underpinning to combine references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has held that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, Case No. IPR2016-00197, Paper 7 at 7-11 (P.T.A.B. April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

VI. SUMMARY OF THE REFERENCES

A. Summary of *Bains*

Bains relates to a multi-rank memory system including a memory controller and at least two memory chips – MC0 and MC1 – each having its own on die termination (ODT) circuitry. *Bains* at Figs. 1, 2 (below, annotations added), 5, 6, and 10 (below, annotations added); 2:33-38; 4:62-67.



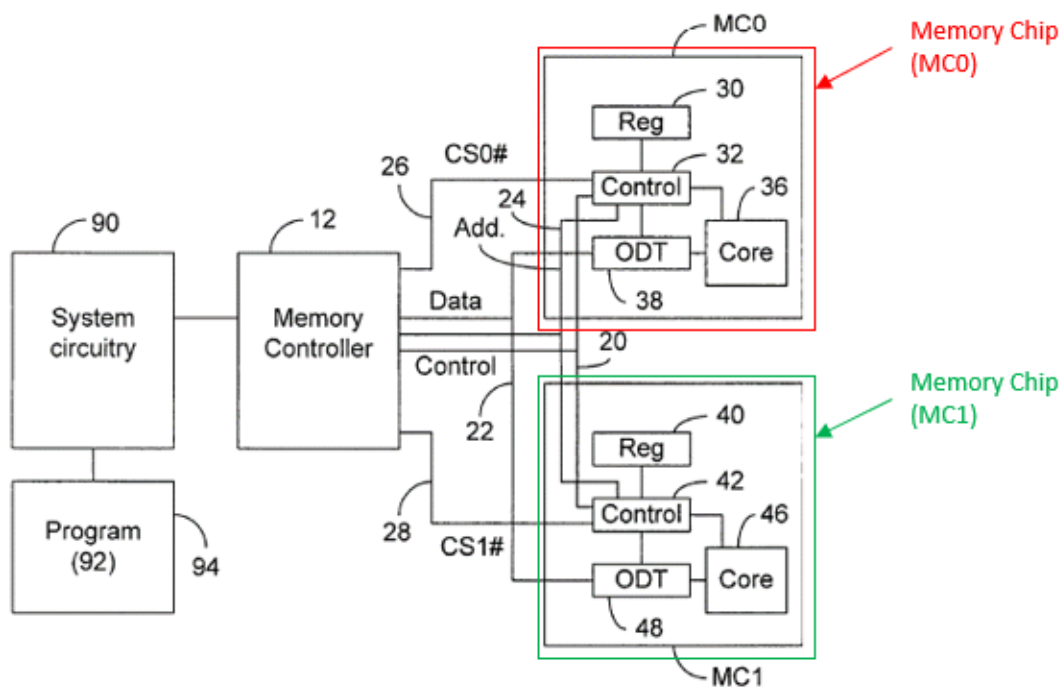


FIG. 10

The memory chips each include control circuitry connected to the ODT circuitry and configured to receive commands from the memory controller. *Id.* at Figs. 2 and 10; 3:17-28. The ODT contemplated by *Bains* includes resistive structures R1-D . . . RN-D and R1-S . . . RM-S which are controlled by switches Sw1-D . . . SwN-D and Sw1-S . . . SwM-S respectively. *Id.* at Fig. 4; 4:31-44. The control circuit connected to the ODT controls the switches and turns the ODT “on” or “off.” *Id.* at 4:31-44. The level of resistance in the ODT is controlled by the number of switches closed. *Id.*

Various commands may be provided to the memory chips through the memory controller, wherein these commands can cause the memory chips to carry

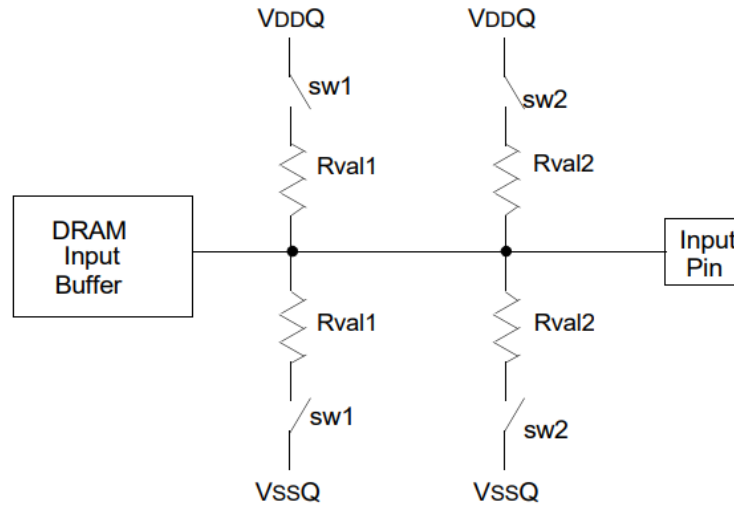
out different operations. *Id.* at 2:47-67; 3:41-52. For example, memory chip MC0 may respond to command A by performing a write operation, while memory chip MC1 may respond to the same command A by turning on an ODT. *Id.* Conversely, memory chip MC0 may respond to another command B by turning on an ODT while memory chip MC1 may respond to the same command B by performing a write operation. *Id.*

Bains contemplates using control commands to control the ODTs such that “it is not necessary to have a pin (pad) to control the ODTs.” *Id.* at 6:30-38. This results in advantageous reduction of pins as compared to other systems. *Id.* *Bains* nevertheless includes a glancing reference to the possibility of using a pin while failing to include any explanation of how a pin may be integrated into its system. *Id.*

B. Summary of JESD79-2A

Petitioner alleges that *JESD79-2A* is a DDR2 SDRAM specification published by JEDEC Solid State Technology Association. The relevant sections of *JESD79-2A* concern an on die termination (ODT) feature of DDR2 SDRAM. The ODT feature allows a DRAM to turn on/off termination resistance via the ODT control pin. *JESD79-2A* includes Figure 15, which is a “Functional Representation of ODT” (shown below):

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
 Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
 Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
 Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

JESD79-2A at 27. As shown in Figure 15, the switches sw1 and sw2 are enabled by the ODT pin such that the level of resistance in the ODT is controlled by the ODT pin and determined by the selection between sw1 or sw2. *Id.* *JESD79-2A* contemplates that the selection between sw1 or sw2 is determined by bits A2 and A6 of the Extended Mode Register Set (EMRS). *Id.* at 21-22, and 27.

VII. THE PETITION DOES NOT DEMONSTRATE THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE UNDER GROUND 1.

Petitioner relies on *Bains* to advance single-reference obviousness arguments against every claim element of claims 1, 2, 5, 6, 9, and 10. Petitioner's arguments with respect to Ground 1 fail for several reasons. First, *Bains* does not disclose a

control command port receiving a control command signal for “*affecting the accessibility*” of the memory chip. Second, with respect to independent claims 1 and 5, *Bains* does not disclose a control circuit configured to terminate the terminal “*in response to the termination signal*.” Similarly, with respect to independent claims 1 and 5, *Bains* does not disclose a control circuit that performs operations “*as a function of the termination signal*.” And, with respect to independent claim 9, *Bains* does not disclose receiving a termination enable signal whose presence “*is required for terminating to occur*.”

A. *Bains* does not disclose “receiving a control command signal for *affecting accessibility* of the memory chip.”

All independent claims of the ’523 Patent require a control command port that receives a control command signal for “affecting accessibility” of the memory chip. ’523 Patent at 8:55-56; 9:28-30; 10:24-25. The ’523 Patent provides several examples of such commands:

The control command signals CMD can assume an active or inactive state. If the memory chip 1 is a DRAM memory chip, the control command signals can be, for example, the chip select signal CS for selecting the relevant memory chip for a specific operation, the write enable signal WE for enabling a write access to the memory chip, the RAS signal (row activation signal) for transmitting the word line address and for activating the word line, as well as the CAS signal (column activation signal) for transmitting the bit line address and for

activating the bit line for reading data out and/or writing them into the memory cell field.

'523 Patent at 3:41-51. As the above example demonstrates, the '523 Patent identifies the chip select signal (CS) “for selecting the relevant memory chip,” the write enable signal (WE) “for selecting the relevant memory chip,” the row activation signal (RAS) “for activating the word line,” and the column activation signal (CAS) “for activating the bit line” as exemplary commands affecting the accessibility of the memory chip. *Id.* Each of these commands select or activate portions of the memory chip. And these commands are defined in the JEDEC standard and provide access to the memory chip. *See* Ex. 1010 at 58 (“2.1.49 – RAS, (RE) ROW ENABLE INPUT[:] A chip enable signal that, on certain dynamic RAMs, actuates only row address oriented internal circuitry.”); at 58 (“2.1.54 – S(n)(x), CHIP SELECT[:] The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption”); at 59 (“2.1.61 – WE, W, WRITE ENABLE[:] The input that, when true, causes the data present on the D or DQ pins to be written into the address cell(s) of the device”); *see Xilinx, Inc. v. Polaris Innovations Limited*, Case No. IPR2023-00516, Paper 2, Ex. 1006 at 27 (“2.1.12 – CAS, (CE), COLUMN ENABLE[:] An enable signal that on some dynamic RAMs actuates only the column oriented internal circuits and the data

input/output circuits”).¹ In other words, the commands either enable or disable access to the memory chip.

Unable to identify any actual disclosure that satisfies the claim language, Petitioner instead offers attorney argument and unsupported expert testimony. Petitioner first argues that the transmission of commands A, B, C, or D by the memory controller in *Bains* teaches “receiving a control command signal for affecting accessibility of the memory chip.” Pet. at 27. In an effort to support this claim, Petitioner makes two allegations. First, Petitioner alleges that write, read, and refresh commands affect the accessibility of MC0 and MC1. This allegation is echoed by Petitioner’s expert, Dr. Baker. EX1003 at ¶ 78. Notably, neither Petitioner nor Dr. Baker provides any explanation or evidence to support this allegation.² Instead, they cite to the same portion of *Bains* which merely identifies write, read, and refresh commands as examples of commands A, B, C, and D.

¹ The exhibits attached to Petitioner’s declarations appear to be missing at least definitions 2.1.1 – 2.1.16 of JEDEC Standard No. 21-C Release 7 (*see* pages 56-57 of Ex. 1010), which include the definition for CAS (column activation signal). Nevertheless, the definition for CAS appears in Exhibit 1006 to the Petition filed in *Xilinx, Inc. v. Polaris Innovations Limited*, Case No. IPR2023-00516, which Petitioner filed.

² Petitioner’s unsupported and conclusory argument further invites legal error because the Board cannot rely on “general conclusions” as a “replacement for documentary evidence for core factual findings in a determination of patentability.” *K/S HIMPP v. Hear-Wear Techs., LLC*, 751 F.3d 1362, 1366 (Fed. Cir. 2014).

Second, Petitioner alleges that commands A, B, C, and D “are the same type of commands as the exemplary command control signals disclosed in the ’523 patent.” Pet. at 27. Petitioner’s sole support for this allegation are paragraphs 78-80 of Dr. Baker’s declaration. As discussed above, paragraph 78 alleges without explanation that write, read, and refresh commands affect the accessibility of the memory chip. EX1003 at ¶ 78. Not only is there no explanation for this allegation, but it is also incorrect as these write, read, and refresh commands are operations performed *on* the memory chip—rather than enabling or disabling access to the memory chip.

Similarly, Paragraph 79 alleges that “a POSITA would understand commands that ‘affect accessibility of the chip’ to include conventional command signals communicated via the control, address, or chip select buses.” EX1003 at ¶ 79. Again, Dr. Baker provides no explanation for this allegation. Instead, Dr. Baker merely quotes the following portion of the ’523 Patent:

The control command signals CMD can assume an active or inactive state. If the memory chip 1 is a DRAM memory chip, the control command signals can be, for example, the chip select signal CS for selecting the relevant memory chip for a specific operation, the write enable signal WE for enabling a write access to the memory chip, the RAS signal (row activation signal) for transmitting the word line address and for activating the word line, as well as the CAS signal

(column activation signal) for transmitting the bit line address and for activating the bit line for reading data out and/or writing them into the memory cell field.

Id. While it is true that the CS, WE, RAS, and CAS signals are conventional command signals, nothing in this excerpt justifies the conclusion that *any* conventional command signal affects accessibility of the memory chip. Indeed, such a conclusion would render the phrase “affecting accessibility of the memory chip” superfluous. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 809-10 (Fed. Cir. 2021) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”).

Lastly, Paragraph 80 alleges that “Commands A, B, C, and D are the same type of commands as the exemplary control command signals disclosed in the ’523 Patent.” EX1003 at ¶ 80. Dr. Baker provides no support for this allegation. Dr. Baker simply provides the same conclusory allegation that appears in the Petition. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-16 (P.T.A.B. Aug. 24, 2022) (precedential) (rejecting expert testimony when “the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.”).

Petitioner cannot rely on unsupported, conclusory assertions to make up for the shortcomings of *Bains*. *See Cook Inc. v. Medtronic Vascular, Inc.*, IPR2018-

01570, Paper 7 at 17 (P.T.A.B. March 4, 2019) (denying institution because Petitioner’s reasoning is premised on an unsupportable assertion never mentioned in the actual reference itself); *In re Magnum Oil Tools Int’l Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements” and “must instead articulate specific reasoning, based on evidence of record . . .”). *Bains* does not disclose “a control command port for receiving a control command signal *for affecting accessibility* of the memory chip.” As such, *Bains* does not disclose limitations [1.3], [5.5], or [9.1] of the Challenged Claims. Accordingly, Petitioner cannot show a likelihood the Challenged Claims are unpatentable over *Bains* and Ground 1 fails.

B. *Bains* does not disclose “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value *in response to the termination signal*.”

Independent claims 1 and 5 require “a termination port” and “a termination signal,” in response to which the control circuit sets the resistance value. ’523 Patent at 8:60-63; 9:37-41. Petitioner alleges that the ODT pin in *Bains* constitutes a termination port. Pet. at 29. Patent Owner does not concede that the ODT pin in *Bains* constitutes a termination port. But even if the ODT pin was a termination port, *Bains* does not disclose the remaining elements of limitations [1.5] and [5.8].

As an initial matter, Petitioner bears the burden of identifying “in writing and with particularity . . . the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a)(3). Indeed, as emphasized by the Federal Circuit, “[i]t is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). Despite this, the Petition does not expressly identify a termination signal. *See TCL Commc’n Tech. Holdings Ltd. v. Dataquill Limited*, IPR2020-00746, Paper 21 at 22 (Sep. 18, 2020) (“It is Petitioner’s responsibility to cite specific evidence to support its arguments, not the Board’s”—nor Patent Owner’s—“responsibility to piece together evidence or speculate as to Petitioner’s position.”); *see also Whole Space Indus. Ltd. v. Zipshade Indus. (B.V.I.) Corp.*, IPR2015-00488 Paper 14 at 18 (July 24, 2015) (citations omitted). As a result, the Petitioner’s analysis concerning limitations [1.5] and [5.8] lacks the requisite particularity and specificity required by 35 U.S.C. § 312(a)(3) and 37 C.F.R. §§ 42.22(a)(2), and 42.104(b)(4)–(5). For this reason alone, Petitioner has not carried its burden of demonstrating a reasonable likelihood of success with respect to claims 1 or 5. Nevertheless, Dr. Baker alleges that the ODT pin, the alleged termination port, receives an ODT signal. EX. 1003 ¶ 86. Given that

the ODT signal is the only signal either Petitioner or its expert allege the ODT pin receives, seemingly Petitioner alleges that the ODT signal is the termination signal. But neither Petitioner nor its expert allege that control circuit 32, the purported control circuit, acts in response to the ODT signal. In fact, the Petition does not even use the word “response” in its discussion of limitations [1.5] and [5.8]. Similarly, Dr. Baker does not use the word response in his discussion of these limitations. EX. 1003 ¶¶ 84-88, 113.

Moreover, nothing in *Bains* suggests that the alleged control circuit acts *in response* to the termination signal. If anything, *Bains* suggests just the opposite. Indeed, Petitioner alleges that “control command signals control whether ODT is ‘on’ as well as the level of ODT resistance.” Pet. at 29. But turning the ODT on or setting the resistance level in response to a control command signal is not acting in response to a termination signal. As such, *Bains* does not disclose limitations [1.5] or [5.8] of the Challenged Claims. Accordingly, claims 1, 5, and their progeny are not unpatentable over *Bains*.

C. *Bains* does not disclose “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.”

Independent claims 1 and 5 require the control circuit to selectively perform an action “as a function of the termination signal.” ’523 Patent at 8:64-9:2; 9:42-

10:4. Petitioner ignores this requirement. Neither the Petition nor the declaration of Petitioner's expert contain any discussion or suggestion that the control circuit acts "as a function of the termination signal." Petitioner makes several assertions regarding a POSITA's understanding of *Bains* and motivation to modify *Bains*, but none of these assertions relate to the control circuit acting as a function of the termination signal.

Again, nothing in *Bains* that suggests the ODT pin transmits a signal to the alleged control circuit. *Supra* § IV.C. Even if the signal on the ODT pin constituted a termination signal, nothing in *Bains* suggests that the control circuit receives it as an input. Further, the Petition fails to make a connection between the timing diagram shown in Figure 7 and control circuit 32. *Bains* describes Figure 7 as "a timing diagram illustrating operation of the memory controller and memory chips of FIG. 5 according to some embodiments of the invention." Ex. 1005, 2:19-21. But the memory controller in *Bains* is a separate structure from the memory chips and the control circuits therein:

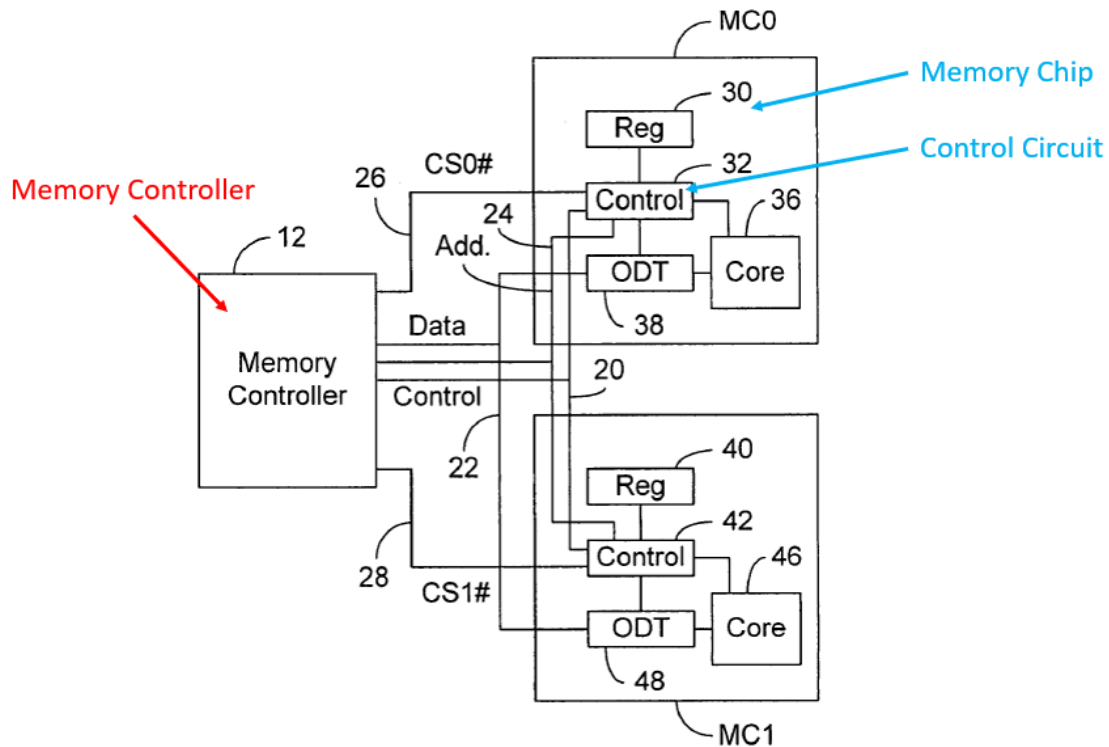


FIG. 2

Ex. 1005, Fig. 2 (annotations added). Petitioner makes no attempt to show that the alleged signals shown in Figure 7 correspond to a control circuit on a memory chip.

Put simply, *Bains* does not disclose limitations [1.6] or [5.9] of the Challenged Claims. Accordingly, claims 1, 5, and their progeny are not unpatentable over *Bains*.

D. *Bains* does not disclose “receiving a termination enable signal, the presence of which is required for the terminating to occur.”

Independent claim 9 requires receiving “a termination enable signal” whose presence “is required for the terminating to occur.” Petitioner incorrectly treats limitation [9.4] as interchangeable with limitation [1.5]. But a side-by-side comparison of limitation [1.5] and [9.4] shows the error with such an approach:

Limitation [1.5]	Limitation [9.4]
a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal	receiving a termination enable signal, the presence of which is required for the terminating to occur

'523 Patent, 8:60-63; 10:35-36. It is readily apparent that limitation [1.5] and limitation [9.4] are not interchangeable. Among other things, limitation [1.5] does not require that the presence of a signal that is required for terminating to occur.

Critically, Petitioner makes no effort to fill or explain these evidentiary gaps. The Petition does not explain what disclosures (if any) are allegedly relevant to claim limitation [9.4], and in what way. Without demonstrating where these aspects of limitation [9.4] are taught in *Bains*, the Petition's analysis is deficient. It was incumbent on Petitioner to explain how and why the "termination enable signal" limitation is met. *See* 37 C.F.R. §§ 42.104(b)(4), 42.22(a)(2); *see also InVue Sec. Prods., Inc. v. Mobile Tech., Inc.*, IPR2019-00078, Paper 7 at 15 (P.T.A.B. May 1, 2019) ("a Petition that requires the panel or the Patent Owner to [scour the Petition to discern Petitioner's evidence] lacks particularity and is tantamount to impermissibly shifting Petitioner's burden under 35 U.S.C. § 312(a)(3).").

What is more, it is unclear from Petitioner's cross-reference whether Petitioner contends that the claim language should be construed identically, or

whether Petitioner simply did not notice the difference in the claim language. In either case, Patent Owner should not be required to speculate on how this limitation is met when Petitioner fails to even address the differences in claim language between cross cited portions of its Petition. Neither should the Board. *See Microsoft Corp. v. FG SRC, LLC*, 860 F. App'x 708, 713 (Fed. Cir. 2021) (“It is not the Board’s job to cobble together assertions from different sections of a petition or citations of various exhibits in order to infer every possible permutation of a petitioner’s arguments.”); *TCL Commc’n Tech. Holdings Ltd.*, IPR2020-00746, Paper 21 at 22 (“It is Petitioner’s responsibility to cite specific evidence to support its arguments, not the Board’s”—nor Patent Owner’s—“responsibility to piece together evidence or speculate as to Petitioner’s position.”). As such, the Petition’s analysis is not only deficient, but the Petition’s web of internal cross references also “improperly shifts the burden of deciphering Petitioner’s arguments onto Patent Owner and the Board.” *Lenovo (United States) Inc. v. LiTL LLC*, No. IPR2021-00681, Paper 8 at 12 (P.T.A.B. Sept. 3, 2021) (denying institution); *see also Apple Inc. v. ContentGuard Holdings, Inc.*, No. IPR2015-00442, Paper 9 at 5–10 (P.T.A.B. July 13, 2015).

Moreover, Petitioner does not even allege that the purported termination enable signal is required for terminating to occur. Instead, Petitioner argues that “*Bains* teaches a termination enable signal received via an ODT pin which turns

termination on and off.” Pet. at 46. But, even if a signal turns termination on or off, it does not follow that the presence of the signal “is required for the terminating to occur.” Nothing in *Bains* suggests that the ODT signal must be present for the termination to be enabled.

Further, nothing in *Bains* indicates that the signal is required for termination to occur. It is entirely possible that termination could occur for reasons other than the alleged termination enable signal. As such, *Bains* does not disclose that the alleged termination enable signal is required for termination to occur. Because *Bains* does not disclose limitation [9.4] of the Challenged Claims, claim 9 and its progeny are not unpatentable over *Bains*.

E. Petitioner Has Failed to Present a Proper Obviousness Theory Regarding *Bains*.

Petitioner’s obviousness allegations are fatally flawed for multiple reasons. First, if a single element of the claim is absent from the prior art, the claims cannot be considered obvious. *See CFMT*, 349 F.3d at 1342. Here, as explained above, the Petition fails to identify disclosures from *Bains* of: 1) “a control command port for receiving a control command signal for affecting accessibility of the memory chip;” 2) “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal;” and 3) “wherein the control circuit, as a function

of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.”

Second, the Federal Circuit and the Board have held that reasons to combine or modify references must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See Kahn*, 441 F.3d at 988; *see also LG Elecs., Inc.*, Case No. IPR2016-00197, Paper 7 at 7-11. “A reason to combine the teachings is needed even in a single-reference obviousness ground.” *Ayla Pharma LLC v. Novartis AG*, No. IPR2020-00295, Paper 14, 4 (P.T.A.B. May 6, 2021) (citing *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017)). A single-reference obviousness argument must include evidence of why the features of different embodiments are interchangeable or a sufficient rationale to combine the teachings of those different embodiments. *See Stepan Co.*, 868 F.3d at 1346 & n.1 (stating that obviousness allegations based on combining “multiple embodiments from a single reference[]” require evidence that a skilled artisan would have had a rational reason to combine such embodiments and a reasonable expectation that such combinations would be successful).

Petitioner’s obviousness allegation lacks sufficient articulated reasons with rational underpinnings, especially as to the relevant features of the claims. As explained above, both the Petition and Dr. Baker’s declaration provide unsupported and conclusory statements that fail to show any disclosure of “commands signal for *affecting accessibility* of the memory chip” in *Bains*. Further, in describing its motivations to modify *Bains*, the Petition never identified in *Bains* any disclosure of a termination signal or a control circuit that sets the resistance value in response to the termination signal. In other words, without identifying such termination signal, the Petitioner has not provided any rational reasons for a POSITA to modify the disclosed system in *Bains* with ODT pins to achieve the claimed invention. *See Abiomed, Inc. v. Maquet Cardiovascular, LLC*, IPR2017-01204, Paper 9 at 8-12 (P.T.A.B. Oct. 23, 2017) (denying institution because petitioner relied on multiple embodiments disclosed in a prior art reference and did not adequately explain how those embodiments were interchangeable or why the skilled person in the art would have found it obvious to combine the teachings of those embodiments); *Hewlett Packard Enter. Co. v. Intellectual Ventures II LLC*, IPR2022-00115, Paper 9 at 15-16 (P.T.A.B. Mar. 29, 2022) (denying institution because Petitioner did not explain how or why the skilled artisan would have combined distinct embodiments or would have had an expectation of success in doing so).

The Petition equally fails to address the issue that *Bains* discourages POSITA from using ODT pins in conjunction with control commands to control the ODTs. See *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1326 (Fed. Cir. 2009) (“An inference of nonobviousness is especially strong where the prior art’s teachings undermine the very reason being proffered as to why a person of ordinary skill would have combined the known elements.”). Specifically, *Bains* states that “[b]y using a command to control the ODTs, it is not necessary to have a pin (pad) to control the ODTs.” Ex. 1005 at 6:30-37. Later, in the same paragraph, *Bains* discusses that:

“In some embodiments, the ODTs are controlled *only commands*, not pins. This results in reduction of pins compared to a system with pins used to control the ODTs. In other embodiments, the ODTs are controlled *only by pins*. In still other embodiments, the ODTs are controlled by *commands sometimes and by pins at other times*.”

Id. (emphasis added). It is apparent from these passages that *Bains* never contemplates a system wherein both the ODT pin and the commands control the ODTs on memory chips. A POSITA reading these passages would be discouraged from modifying *Bains*’s memory systems to use ODT pins in conjunction with control commands to control the ODTs on the memory chips. In other words, A POSITA would understand *Bains* as teaching away from using both a termination

port and control command signals to control the termination circuit of a memory chip. *See Arctic Cat Inc. v. Bombardier Recreational Prod. Inc.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) (“Prior art teaches away when ‘a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.’”). For this reason alone, the Petition must fail with respect to ground 1. *See In re Mouttet*, 686 F.3d 1322, 1333 (Fed. Cir. 2012) (“A reference that properly teaches away can preclude a determination that the reference renders a claim obvious.”).

In sum, Petitioner has not sufficiently shown why one of ordinary skill in the art would have modified *Bains* to account for all the features of the challenged claims. The Petition fails with respect to Ground 1 for these additional reasons.

VIII. THE PETITION DOES NOT DEMONSTRATE THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE UNDER GROUND 2.

With respect to Ground 2, Petitioner again relies on *Bains* for multiple elements of the Challenged Claims. In particular, Petitioner relies solely on *Bains* for the disclosure of limitations [1.3], [5.5], and [9.1]: “receiving a control command signal for *affecting accessibility* of the memory chip.” Thus, for the same reasons set forth in Section VII.A, the proposed combination of *Bains* and *JESD79-2A* does not disclose limitations [1.3], [5.5], and [9.1]. As such, Ground 2 necessarily fails.

Similarly, Petitioner relies solely on *Bains* for the disclosure of limitation [9.4]: “receiving a termination enable signal, the presence of which is required for the terminating to occur.” Thus, for the same reasons set forth in Section VII.D, the proposed combination of *Bains* and *JESD79-2A* does not disclose the limitations required by claim 9 and its progeny.

Further, as detailed below, Petitioner’s proposed combination of *Bains* and *JESD79-2A* does not resolve the shortcomings of the Petition with respect to the following limitations: [1.5] and [5.8]. Moreover, Petitioner failed to articulate a rational reason why a POSITA would combine *JESD79-2A*’s disclosure of ODT pins with the memory system of *Bains*. This failure is particularly significant given that *Bains* discourages simultaneous use of pins and commands to control the ODT.

A. The Combination of *Bains* and *JESD79-2A* does not disclose “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value *in response to the termination signal*.”

Petitioner contends that “[t]o the extent that Patent Owner argues that *Bains* alone does not teach limitation [1.5], this limitation is taught by *Bains* in view of *JESD79-2A*.” Pet. at 57; *see also* Pet. at 66 (discussing limitation [5.8]). Petitioner is incorrect. Neither *Bains* nor *JESD79-2A* contemplate the control circuit acting in response to the alleged termination signal.

Notably, the Petition is silent on the requirement that the control circuit be configured to selectively terminate the terminal in response to the termination signal.

The Petition simply alleges that:

Bains teaches that the control command signals control whether ODT is “on” as well as the level of ODT resistance. *Supra* Section X.A.1.e. As shown in Fig. 4 below, control circuit 32 controls the switches Sw1-D...SwN-D and Sw1-S...SwM-S and thus whether ODT is “on” or “off,” where the number of switches that are closed may determine the amount of resistance that is applied to the data pin. EX1005 at 4:40-42, Fig. 4. The number of switches closed is a function of the received control command signal. As one example, “command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42-44. However, Bains also teaches that there may be a pin for controlling the ODT in addition to the commands.

Pet. at 57-58. But this does not address the requirement that the control circuit act “in response to the termination signal.”

The Petition’s subsequent allegations do nothing to cure this deficiency.

Instead, the Petition merely alleges that the ODT pin:

is used to control when the switches are enabled to apply the selected resistance. In other words, the ODT pin controls when the switches are enabled according to first and second time delays tAOND and tAOFD, respectively (see Fig. 16, below), and control command signals A1, A2 through AN control which resistance level is applied, as discussed in Ground 1 with respect to limitation [1.4].

Pet. at 59-60. Even if this were true, it fails to address the requirement that the control circuit act “in response to the termination signal.”

As such, the proposed combination of *Bains* and *JESD79-2A* does not disclose limitations [1.5] or [5.8] of the Challenged Claims. Accordingly, claims 1, 5, and their progeny are not unpatentable over the combination of *Bains* and *JESD79-2A*.

B. Petitioner Failed to Present a Proper Obviousness Theory Regarding the Alleged Combination of *Bains* and *JESD79-2A*.

Petitioner’s obviousness allegations in this regard are fatally flawed for multiple reasons. First, if a single element of the claim is absent from the prior art, the claims cannot be considered obvious. *See CFMT*, 349 F.3d at 1342. Here, the Petition fails to identify disclosures from *Bains* and *JESD79-2A* of: 1) “a control command port for receiving a control command signal for affecting accessibility of the memory chip;” 2) “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal;” and 3) “receiving a termination enable signal, the presence of which is required for the terminating to occur.”

Second, the Federal Circuit and the Board have held that reasons to combine or modify references must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the

legal conclusion of obviousness.” *See Kahn*, 441 F.3d at 988; *see also LG Elecs., Inc.*, Case No. IPR2016-00197, Paper 7 at 7-11. Here, Petitioner’s obviousness analysis lacks articulated reasons with rational underpinnings, especially as to the relevant features of the claims. Petitioner offers only generic, boilerplate restatements of the basic tests for obviousness. *See KSR Int’l Co.*, 550 U.S. at 418 (*quoting Kahn*, 441 F.3d at 988 (Obviousness cannot be sustained by “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”)); *Ancestry.com DNA, LLC v. DNA Genotek Inc.*, IPR2016-01152, Paper 11 at 10 (P.T.A.B. Nov. 23, 2016) (“General principles on what may constitute a supporting rationale cannot substitute for specific application of those principles to facts.”). For example, Petitioner alleges that a POSITA would have been motivated to combine *Bains* and *JESD79-2A* because the *JESD79-2A* was well known, and that *Bains* includes “unillustrated” embodiments using ODT pin and refers to unspecified JEDEC standards. Pet. at 49-56. Neither the Petition, nor Dr. Baker’s declaration, provides any supports as to how a POSITA would implement the ODT pin disclosed in *JESD79-2A* with the memory system of *Bains*. Tellingly, Dr. Baker’s declaration, while acknowledging that the *JESD79-2A* and *Bains* have distinct control schemes for the resistor switches in the ODT, baldly stated that the combination of *JESD79-*

2A and *Bains* involves simple substitution or application of known technique to yield predictable results. Ex. 1003 at 75 and 80. Dr. Baker provides no explanation as to how a POSITA would substitute the ODT in *Bains*, controlled by control circuit 32 (Ex. 1005 at 4:37-39), with the ODT disclosed by JESD79-2A, which is controlled by the ODT pin. Ex. 1006 at 27, Figure 15 (“Switch sw1 or sw2 is enabled by ODT pin”). The Petitioner cannot satisfy its burden by relying on conclusory and unsupported statement that the combination is the mere application of a known technique to a known device, without explaining why a POSITA would have been motivated to seek out that particular technique to achieve the purported result. *See Commerce Bancshares, Inc. v. Intellectual Ventures II LLC*, IPR2014-00793, Paper 7 at 13- 14 (P.T.A.B. Dec. 1, 2014) (rejecting a motivation-to-combine argument where the Petition “d[id] not refer to evidence explaining how many solutions were available, what those solutions were, or specifically why a skilled artisan would have chosen the solutions disclosed in [the references] to solve the relevant problem”).

Additionally, fatal to the Petitioner’s argument is that it never addresses *Bains*’s discussion discouraging the use of ODT pins in conjunction with control commands. *See, e.g.*, Ex. 1005, 6:30-37 (“By using a command to control the ODTs, it is not necessary to have a pin (pad) to control the ODTs This results in reduction of pins compared to a system with pins used to control the ODTs. In other

embodiments, the ODTs are controlled only by pins.”). Relevant passages in *Bains* show that it never contemplates a system that uses ODT pins and commands to control an ODT. Ex. 1005, 6:30-37. *Bains*’s explicit disclosures would discourage a POSITA from modifying *Bains*’s memory systems to use ODT pins in conjunction with commands. See *Mouttet*, 686 F.3d at 1333 (“A reference that properly teaches away can preclude a determination that the reference renders a claim obvious.”); *Arctic Cat, Inc.*, 876 F.3d at 1360 (“Prior art teaches away when ‘a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.’”).

In sum, Petitioner has not shown why one of ordinary skill in the art would have combined or modified *Bains* and *JESD79-2A* to account for all the features of the challenged claims. The Petition fails with respect to Ground 2 for these additional reasons.

IX. PATENT OWNER’S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the Petition and reserves the right to rebut them later. Additionally, Patent Owner is not

limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

X. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute *inter partes* review of the '523 Patent.

Dated: June 21, 2023

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 8,467 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Dated: June 21, 2023

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on June 21, 2023, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

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