

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2023-00513
Patent 7,532,523 B2

Before JEAN R. HOMERE, BARBARA A. PARVIS, and
MINN CHUNG, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Xilinx, Inc. (“Petitioner”) filed a Petition (Paper 2 (“Pet.”)) requesting an *inter partes* review of claims 1, 2, 5, 6, 9, and 10 (“challenged claims”) of U.S. Patent No. 7,532,523 B2 (Ex. 1001, “the ’523 patent”) pursuant to 35 U.S.C. §§ 311–319, along with the supporting Declaration of Dr. R. Jacob Baker (Ex. 1003). Polaris Innovations Limited (“Patent Owner”) filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

We have authority to determine whether to institute review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4.

Upon consideration of the contentions and the evidence of record at this juncture, we conclude Petitioner establishes a reasonable likelihood of prevailing in demonstrating the unpatentability of the challenged claims of the ’523 patent. Accordingly, we grant Petitioner’s request and institute an *inter partes* review of all challenged claims of the ’523 patent and with respect to all grounds set forth in the Petition.

II. BACKGROUND

A. *Real Parties-in-Interest*

Petitioner identifies itself, Xilinx, Inc., as well as Advanced Micro Devices, Inc., and ATI Technologies ULC, as the real parties-in-interest. Pet. 1.

Patent Owner identifies itself, Polaris Innovations Limited, as the real party-in-interest. Paper 10, 2. Patent Owner also notes that it “is a wholly-owned subsidiary of Wi-LAN Inc.,” which in turn “is owned by Owlpoint IP Opportunities JVF LP and Quarterhill Inc.” *Id.*

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), the parties inform us that the '523 patent was asserted against Petitioner in the following district court case: *Polaris Innovations Ltd. v. Xilinx, Inc.*, No. 1:22-cv-00174-RGA (D. Del.). Pet. 1; Paper 10, 2. Petitioner indicates that it has also filed petitions for *inter partes* review of three other patents involved in this district court case: IPR2023-00514, IPR2023-00516, and IPR2023-00517. Pet. 1.

Patent Owner informs us that the '523 patent is also involved in *Polaris Innovations Ltd. v. Nanya Technology Corp.*, No. 2:23-cv-00044 (E.D. Tex.). Paper 10, 2–3.

C. The '523 Patent

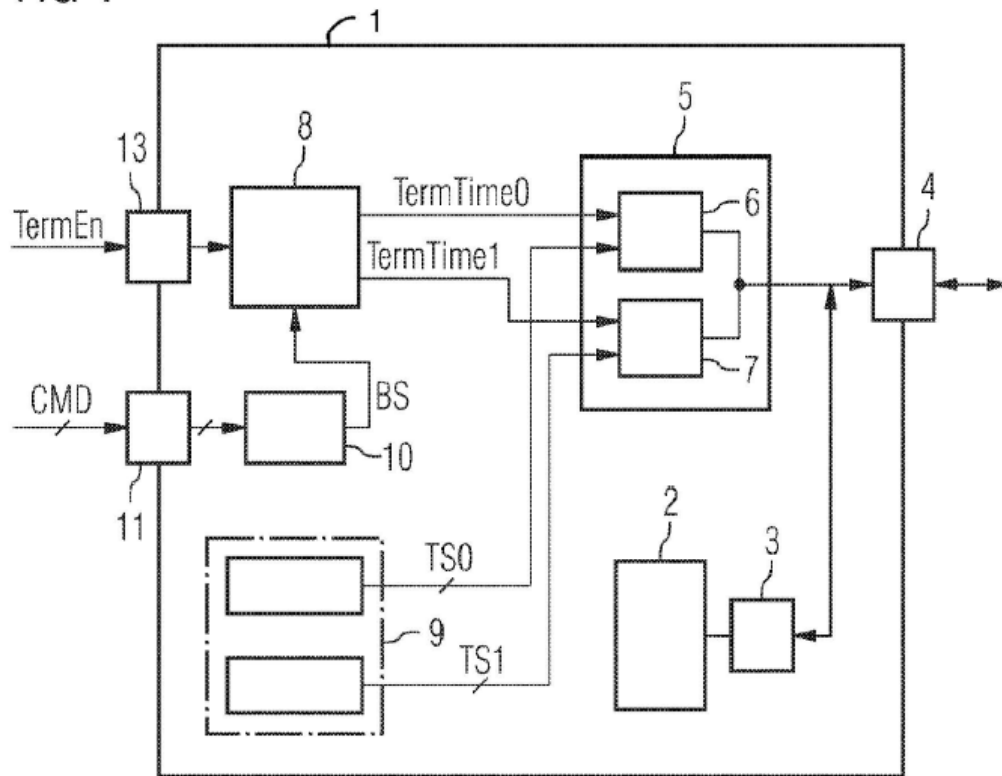
The '523 patent is titled “Memory Chip with Settable Termination Resistance Circuit.” Ex. 1001, code (54). The '523 patent “relates to a memory chip having a terminal for sending and/or receiving high-frequency signals.” *Id.* at 1:18–20.

The '523 patent observes that on a memory bus that connects memory chips to one another and a memory controller, high frequency signal transmissions may cause signal reflections “that disturb the data transmission on the memory bus and thereby limit the data transmission rates.” *Id.* at 1:27–33. Prior solutions to this problem involved “switch[ing] the termination on or off at a terminal of the memory chip as a function of a termination signal” so as to “support the following read, write or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus.” *Id.* at 1:37–44. Simply “switching the terminating resistors on and off,” however, “is not sufficient as a rule to achieve an optimal termination in every operating state” to

improve data transmission. *Id.* at 1:44–48. Accordingly, the '523 patent describes a memory chip with “a termination circuit which is connectable to the terminal in order to terminate the terminal with a settable resistance value.” *Id.* at 2:1–3.

An example of a memory chip is shown in Figure 1, reproduced below.

FIG 1



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT

Figure 1, above, shows memory chip 1 with memory cell array 2, such as a DRAM memory cell array, and with logic circuit 3 for use in writing to and reading from the array. *Id.* at 2:40–43. Logic circuit 3 is connected to external terminal 4, “via which, for example, address, clock and user data can be read in or driven out.” *Id.* at 2:45–48. Termination circuit 5 is

connected to external terminal 4 and “has a first settable terminating resistor 6 with a first resistance value, and a second settable terminating resistor 7 with a second resistance value.” *Id.* at 2:49–52. Configuration unit 9 makes configuration values available to resistor 6 and resistor 7 in order to set respective resistance values. *Id.* at 3:1–7. Accordingly, “[a] settable terminating resistor can be achieved, for example, by switchable, parallel-connected resistors.” *Id.* at 3:14–15.

In operation, control unit 8 receives a termination enable signal from termination port 13 indicating whether to provide a termination to external terminal 4. *Id.* at 3:25–28. “Which of the two terminating resistors 6, 7 is connected to the external terminal 4 is specified as a function of a command signal BS that is made available by a command decoder 10, as a function of a received control command CMD.” *Id.* at 3:34–39.

D. Illustrative Claim

Petitioner challenges claims 1, 2, 5, 6, 9, and 10 of the ’523 patent. Pet. 3. Claims 1, 5, and 9 are independent claims. Independent claim 1, reproduced below, is illustrative of the claimed subject matter.

1. [1.P] A memory chip for variably setting terminations, comprising:

- [1.1] a terminal;
- [1.2] a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;
- [1.3] a control command port for receiving a control command signal for affecting accessibility of the memory chip;
- [1.4] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and
- [1.5] a termination port to receive a termination signal, wherein the control circuit is configured to selectively

terminate the terminal with the set resistance value in response to the termination signal,
[1.6] wherein the control circuit, as a function of the termination signal, selectively performs one of:
(i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

Ex. 1001, 8:49–9:2.¹

E. Evidence

Petitioner relies on the references summarized in the table below.

Name	Reference	Exhibit
Bains	US 7,433,992 B2, issued Oct. 7, 2008	1005
JESD79–2A	JEDEC Standard, DDR2 SDRAM Specification JESD79-2A (Jan. 2004)	1006

F. Asserted Grounds

Petitioner provides a summary table with the asserted statutory grounds of unpatentability for each of the challenged claims of the '523 patent (Pet. 3), which are set forth below:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 5, 6, 9, 10	103(a) ²	Bains
1, 2, 5, 6, 9, 10	103(a)	Bains, JESD79–2A

¹ We include bracketed annotations provided by Petitioner for ease of analysis. *See* Pet. v.

² The '523 patent was filed July 31, 2006. Ex. 1001, code (22). The AIA version of 35 U.S.C. § 103 does not apply. Our analysis would not change under the AIA version of § 103.

III. ANALYSIS

A. *Principles of Law*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. *Level of Ordinary Skill in the Art*

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the time of the invention

would have had a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and at least two or three years of academic or industry experience in integrated circuit input/outputs and memory systems, or comparable industry experience.

Pet. 11 (citing Ex. 1003 ¶¶ 31–35). Petitioner also asserts “[a]dditional training can substitute for educational or research experience, and vice versa.” *Id.* At this time, “Patent Owner does not contest Petitioner’s definition of a [POSITA].” Prelim. Resp. 9.

We find that the phrase “at least” in Petitioner’s proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. With that exception,

on the current record, we preliminarily find Petitioner’s proposal is consistent with the level of skill reflected in the ’523 patent Specification and the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). We, therefore, adopt Petitioner’s proposal, with the “at least” phrase omitted.

C. Claim Construction

We construe the challenged claims by applying the standard used in federal courts, in other words, “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b),” which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2020). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips*, 415 F.3d at 1312–13.

Petitioner asserts that “[c]onstruction of any terms is unnecessary because it is not dispositive of this case—the art teaches the limitations under any construction under the *Phillips* standard.” Pet. 12. Patent Owner asserts “that the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient.” Prelim. Resp. 9.

Based on the record before us, we do not discern a need to construe explicitly any claim terms because doing so would not change the outcome of the analysis below. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”

(quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Asserted Obviousness of Claims 1, 2, 5, 6, 9, and 10

Petitioner argues that claims 1, 2, 5, 6, 9, and 10 are unpatentable under 35 U.S.C. § 103 as obvious over Bains, or, alternatively, the combination of Bains and JESD79-2A. Pet. 22–69.

1. Overview of Bains (Ex. 1005)

Bains is titled “Command Controlling Different Operations in Different Chips.” Ex. 1005, code (54). Figure 2, reproduced below, shows a block diagram of a memory controller and memory chips. *Id.* at 2:5–6.

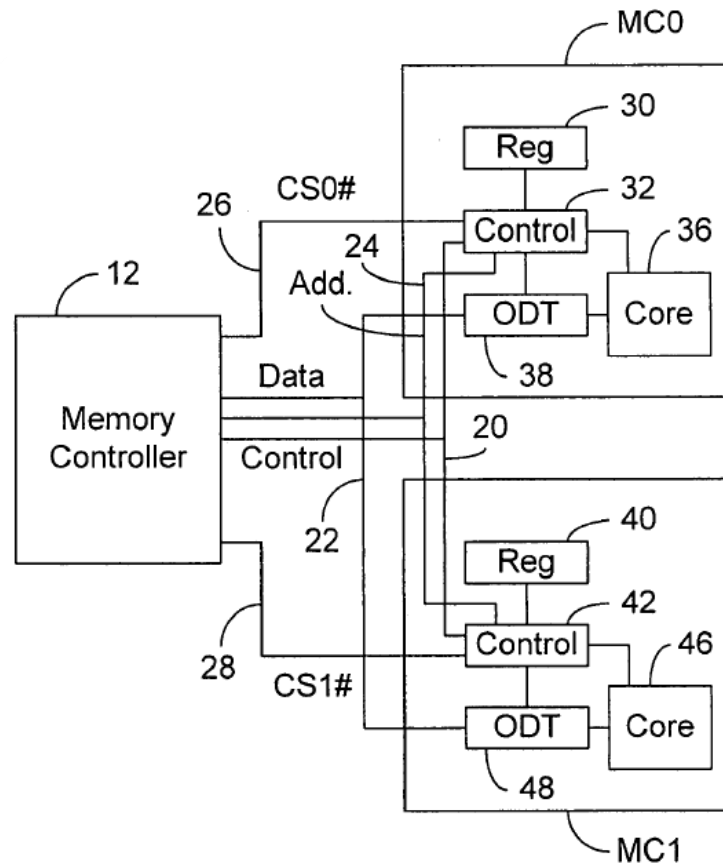


FIG. 2

Figure 2 shows memory controller 12, which is coupled to memory chip MC0 and memory chip MC1 through control bus 20, data bus 22, and address bus 24. *Id.* at 3:9–11. With respect to Figure 2, control circuitry 32 and 42 in respective chips MC0 and MC1 receive commands from memory controller 12 through control bus 20, or a combination of control bus 20 and the other buses. *Id.* at 3:17–28.

Figure 4, reproduced below, shows a block diagram of further details of a memory chip. *Id.* at 2:10–11.

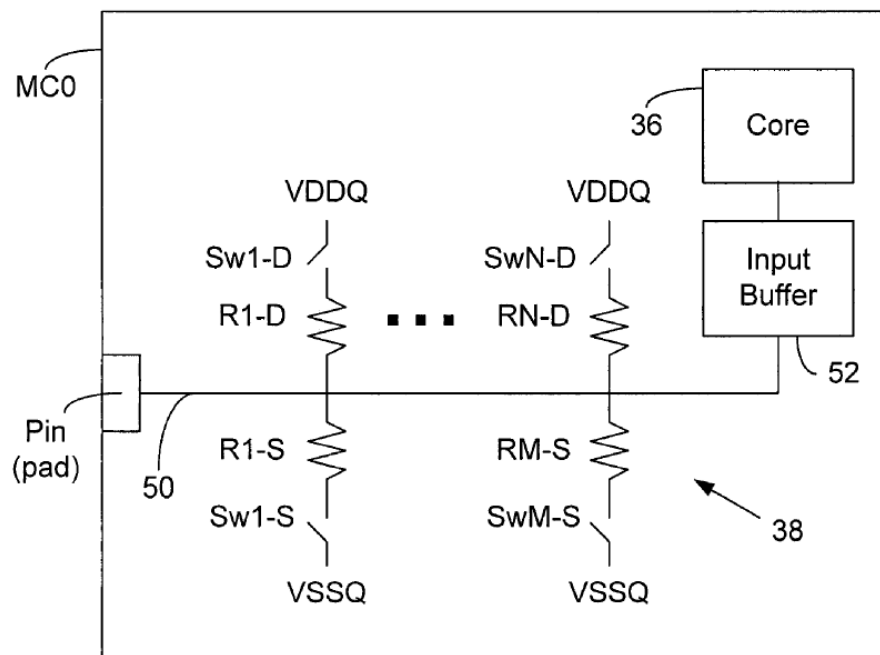


FIG. 4

Figure 4 shows an implementation of ODT 38 in chip MC0. *Id.* at 4:28. Resistive structures R1-D through RN-D are between data node 50 and switches Sw1-D through SwN-D, respectively, which in turn are coupled to supply voltage node VDDQ. *Id.* 4:31–34. Resistive structures R1-S through RM-S are between data node 50 and switches Sw1-S through SwM-S,

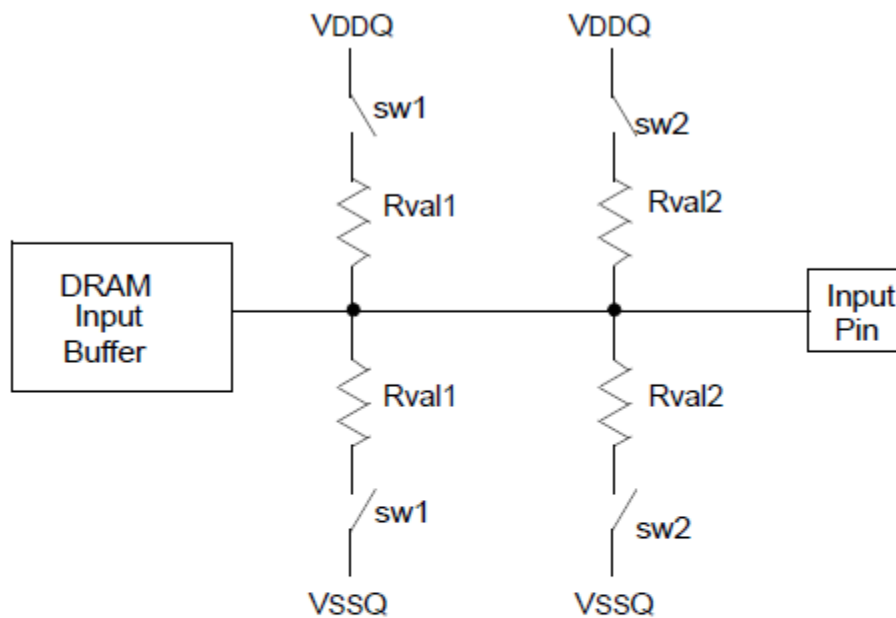
respectively, which are coupled to ground voltage node VSSQ. *Id.* at 4:34–37. “Control circuitry 32 controls the switches and hence whether ODT 38 is ‘on,’” and “[t]he number of switches closed may determine the amount of resistance in the termination.” *Id.* at 4:39–42. For example, a command A1 may cause one level of resistance in ODT 38, while another command A2 may cause another level of resistance. *Id.* at 4:42–44.

2. Overview of JESD79–2A (Ex. 1006)

JESD79-2A is a Joint Electron Device Engineering Council (JEDEC) specification for Double Data Rate 2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM). *See* Ex. 1006. In particular, JESD79-2A explains that “[t]he ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.” *Id.* at 18.³

Figure 15, reproduced below, illustrates a functional representation of an ODT circuit. *Id.* at 19.

³ We use the pagination of the original document found in the upper left or right corner.



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

As described in the text provided in Figure 15 above, "Switch sw1 and sw2 is enabled by ODT pin," and "[s]election between sw1 or sw2 is determined by" data stored in the extended mode register (EMRS). *Id.*

3. *Independent Claim 1*

a) *Rationale to Combine*

Petitioner presents reasoning to make the proposed combination of Bains and JESD79-2A in a sub-section titled "Motivation to Combine Bains and JESD79-2A." Pet. 49–56. Petitioner provides further argument in its element-by-element analysis. *See, e.g., id.* at 56–64. Relying on the testimony of Dr. Baker, Petitioner provides five reasons to combine the

teachings of Bains and JESD79-2A and also provides argument supporting that a person having ordinary skill in the art would have had a reasonable expectation of success. *Id.* at 49–56 (citing Ex. 1003 ¶¶ 122–131).

First, Petitioner argues a person having ordinary skill in the art would have been motivated and would have had a reasonable expectation of success because “JESD79-2A was and remains a well-known memory standard published by the preeminent memory standards setting organization.” *Id.* at 49 (citing Ex. 1003 ¶¶ 124–125). With respect to motivation, Petitioner, more specifically, argues a person having ordinary skill in the art would have been motivated to use the JESD79-2A standard because the resulting combination would have been in “compliance with JEDEC standards, which is essential for interoperability.” *Id.* at 50. We preliminarily find that Petitioner’s argument is consistent with the title of JEDEC79-2A, which is “JEDEC Standard No. 79-2A.” *See, e.g.*, Ex. 1006, cover, 9.

Second, Petitioner argues a person having ordinary skill in the art would have been motivated and would have had a reasonable expectation of success because “Bains specifically teaches that the system may use ODT pins to control the termination.” Pet. 49, 52–53. Patent Owner responds specifically to Petitioner’s second argument that Bains’s description is “unillustrated.” Prelim. Resp. 37. Bains describes that in “some embodiments, the ODTs are controlled only by commands, not pins,” in “other embodiments the ODTs are controlled only by pins” and in “still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times.” Ex. 1005, 6:29–31. We preliminarily find that

Bains's textual disclosure is sufficiently clear that Bains teaches that in its system, ODTs may be controlled by pins and no illustration is needed.

Third, Petitioner argues a person having ordinary skill in the art would have been motivated and would have had a reasonable expectation of success because "Bains refers to JEDEC's DDR standards with respect to the use of ODT pins." Pet. 49, 53–54 (citing Ex. 1005, 1:37–45, 6:31–37). Patent Owner responds that Bains "refers to unspecified JEDEC standards." Prelim. Resp. 37.

Consistent with Petitioner's argument, Bains describes the following:

The JEDEC Solid State Technology Association has provided standards for DDR2 (dual data rate 2 or double data rate 2) DRAM chips. In DDR2 DRAM chips, the ODTs are controlled by using discrete signals per rank. In some two rank-1 DIMM systems, two ODT pins are used on the controller and the DIMM. Two pins may also be used per DRAM chip to support stacking solutions. As used in this disclosure, the word "pin" means traditional pins or other connections to die pads.

Ex. 1005, 1:37–45. We preliminarily find Bains's disclosure is sufficiently specific with respect to JEDEC standards describing use of ODT pins.

Fourth, Petitioner argues "to the extent that Bains does not sufficiently describe the use of ODT pins in its system," JESD79-2A "provides further details not expressly disclosed in Bains regarding the operation of the ODT pin and associated signaling." Pet. 49 (citing Ex. 1003 ¶¶ 122–123). We preliminarily find JESD79-2A's disclosure provides additional details, consistent with Petitioner's argument.

Fifth, Petitioner argues that its proposed combination would have permitted "for more complex termination schemes and more customizable termination timing than a command-only control system." Pet. 50 (citing Ex. 1003 ¶¶ 124–125); *see also id.* at 30 (making similar argument with

respect to obviousness over Bains). Dr. Baker testifies “by asserting the ODT enable signal before a command, ODT could be turned ‘on’ before a command is asserted.” Ex. 1003 ¶ 125.

Patent Owner argues “Petitioner’s obviousness analysis lacks articulated reasons with rational underpinnings, especially as to the relevant features of the claims.” Prelim. Resp. 37. At this stage in the proceeding, we find that Petitioner’s argument contains sufficient specificity with respect to elements 1.5 and 1.6. Pet. 29–33, 49–60. For instance, we find that Petitioner’s fifth argument and Dr. Baker’s related testimony that the proposed combination would have permitted “for more complex termination schemes and more customizable termination” (*see, e.g.*, Pet. 50; Ex. 1003 ¶¶ 124–125) relates to customizable termination and element 1.5 requires that the control circuit “selectively terminate the terminal . . . in response to the termination signal.”

Patent Owner also argues that “[n]either the Petition, nor Dr. Baker’s declaration, provides any support as to how a POSITA would implement the ODT pin disclosed in JESD79-2A with the memory system of *Bains*.” Prelim. Resp. 37. Patent Owner argues that “JESD79-2A and Bains have distinct control schemes for the resistor switches in the ODT.” *Id.* at 37–38. Petitioner provides detailed explanations of how the teachings of Bains and JESD79-2A would have been combined. Pet. 54–56, 59–60. Petitioner also presents arguments that Bains and JESD79-2A teach similar termination circuits. Pet. 50–53, 55. Based on the preliminary record, we find that Petitioner explains sufficiently for purposes of institution how the teachings of Bains and JESD79-2A would have been combined and provides sufficient

argument and evidence preliminarily showing that the ordinary skilled artisan would have had reasonable expectation of success.

Patent Owner further argues that Petitioner fails to address “*Bains*’s discussion discouraging the use of ODT pins in conjunction with control commands.” Prelim. Resp. 38 (citing Ex. 1005, 6:30–37); *see also id.* at 32 (making a similar argument for the Petition’s ground of obviousness over *Bains* alone). We note that *Bains* describes that in “some embodiments, the ODTs are controlled only by commands, not pins” and in “other embodiments the ODTs are controlled only by pins.” Ex. 1003, 6:29–31. Importantly, however, *Bains* also describes in “still other embodiments, the ODTs are controlled by *commands sometimes and by pins at other times.*” *Id.* (emphasis added).

We preliminarily find that *Bains* does not teach away from Petitioner’s proposed combination because it describes embodiments using only commands or only pins. *See Depuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (“A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.”). *Bains* does not criticize, discredit, or otherwise discourage investigation into the claimed subject matter. Indeed, to the contrary, *Bains* also describes in “still other embodiments, the ODTs are controlled by *commands sometimes and by pins at other times.*” Ex. 1005, 6:29–31 (emphasis added).

At this stage, Petitioner’s reasons for combining *Bains* and JESD79-2A are sufficiently persuasive for institution. Petitioner’s arguments that a person having ordinary skill in the art would have had a reasonable

expectation of success also are sufficient for purposes of institution. We find that Petitioner’s reasoning is not undermined by Patent Owner’s arguments based on the preliminary record before us at this early stage in the proceeding.

b) The Preamble

Petitioner relies on Bains for teaching the preamble, which is “[a] memory chip for variably setting terminations.” Pet. 22. In particular, Petitioner relies on Bains’s teaching of “a memory chip MC0 (or alternatively, MC1) with an ODT circuit 38 that may terminate a data pad with an infinite resistance[] or different finite resistances depending on the command A1 or A2 provided to the chip from the memory controller 12.” *Id.* (citing Ex. 1005, 2:33–52, 3:41–58, 4:39–61, Figs. 2, 4; Ex. 1003 ¶ 72).⁴

We preliminarily find that Petitioner’s contentions are supported sufficiently by the cited portions of the asserted art. Patent Owner does not dispute Petitioner’s showing at this early stage. After considering the contentions and the evidence of record, we determine that Petitioner has shown sufficiently that Bains teaches the preamble for purposes of institution.

c) Element 1.1

Petitioner relies on Bains for teaching element 1.1, which is “a terminal.” Pet. 23. Petitioner argues “Bains teaches that the memory chip MC0 includes a data pin (pad), which is a terminal.” *Id.* (citing, e.g., Ex. 1005, Fig. 4; Ex. 1003 ¶ 73). Dr. Baker’s testimony includes annotated

⁴ We take no position at this stage on whether the preamble is limiting.

versions of Figure 4 of Bains (Ex. 1003 ¶¶ 73, 75), one of which is reproduced below in our discussion of element 1.2. *See* § III.D.3.d.

We preliminarily find that Petitioner’s contentions are supported sufficiently by the cited portions of the asserted art. Patent Owner does not dispute Petitioner’s showing at this early stage. After considering the contentions and the evidence of record, we determine that Petitioner has shown sufficiently that Bains teaches element 1.1 for purposes of institution.

d) Element 1.2

Petitioner relies on Bains for teaching element 1.2, which is “a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value.” Pet. 23–25. In particular, Petitioner relies on Bains’s teaching of “ODT circuit 38 coupled to the terminal.” *Id.* at 23. Petitioner argues “[c]ontrol circuitry 32 controls the switches Sw1-D . . . SwN-D and Sw1-S . . . SwM-S of the termination circuit 38” and “the number of switches that are closed determines the amount of resistance that is applied to the data pin.” *Id.* at 23–24 (citing Ex. 1005, 4:40–44; Ex. 1003 ¶¶ 74–75).

Figure 4 of Bains as annotated by Dr. Baker is reproduced below.

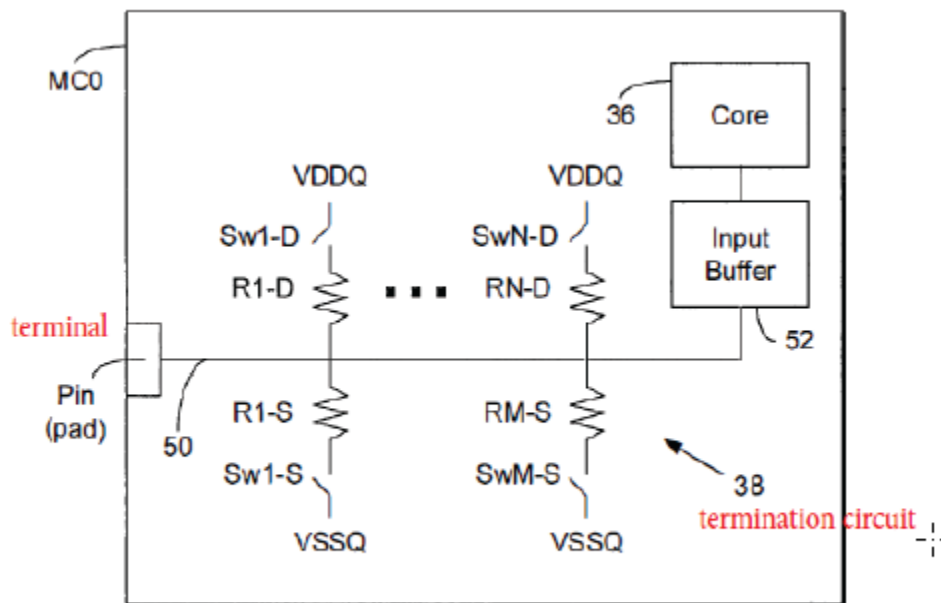


FIG. 4

Annotated figure 4 of Bains, above, shows an implementation of ODT 38 in chip MC0 and includes Dr. Baker’s red textual annotation of “terminal” next two “pin (pad)” and “termination circuit” next to “38,” which is the reference numeral of the ODT. Ex. 1005, 4:28; Ex. 1003 ¶ 75.

We preliminarily find that Petitioner’s contentions are supported sufficiently by the cited portions of the asserted art. Patent Owner does not dispute Petitioner’s showing at this early stage. After considering the contentions and the evidence of record, we determine that Petitioner has shown sufficiently that Bains teaches element 1.2 for purposes of institution.

e) Element 1.3

Petitioner relies on Bains for teaching element 1.3, which is “a control command port for receiving a control command signal for affecting accessibility of the memory chip.” Pet. 25–27. For instance, relying on the testimony of Dr. Baker, Petitioner argues “[i]n order to receive commands from the memory controller 12 sent over the buses, a POSITA would

understand that the control circuit 32 includes a port connected to the control bus 20 and chip select bus 26.” *Id.* at 26 (citing Ex. 1005, 3:9–28, Fig. 2; Ex. 1003 ¶ 77). Petitioner also argues “Bains discloses that the memory controller 12 transmits commands A, B, C, or D to the memory chips via the buses” and that “Bains describes that these commands may be, for example, write commands, read commands, or refresh commands, which affect accessibility of the chips MC0 and MC1.” *Id.* at 27 (citing Ex. 1005, 3:17–28, 3:37–4:6; Ex. 1003 ¶¶ 78–80). Regarding the understanding that a person having ordinary skill would have had, Dr. Baker testifies that Bains’s “commands may be, for example, write commands, read commands, or refresh commands, which affect accessibility of the chips MC0 and MC1.” Ex. 1003 ¶¶ 78–79.

Patent Owner argues that neither Petitioner nor Dr. Baker provides explanation or evidence to support that Bains’s write, read, and refresh commands affect the accessibility of MC0 and MC1. Prelim. Resp. 19. Patent Owner discusses the disclosure in the ’523 patent regarding commands that “either enable or disable access to the memory chip.” *Id.* at 18–19. Patent Owner argues that Bains’s “write, read, and refresh commands are operations performed on the memory chip,” which Patent Owner contrasts to the disclosure in the ’523 patent that Patent Owner argues describes “enabling or disabling access to the memory chip.” *Id.* at 20.

At this juncture, we preliminary find that element 1.3 is not limited so as to preclude commands that the chip receives and responds to, such as those described in Bains. In particular, element 1.3 recites that the memory chip comprises “a control command port *for receiving a control command signal* for affecting accessibility of the memory chip” (emphasis added). We

preliminarily find that element 1.3 is met by Bains’s disclosure of receipt of “command A” and Bains’s further disclosure that “[c]hip MC0 responds to command A as a write command, meaning that control circuitry 32 *causes certain data bits on data bus 22 to be stored in core 36 of chip MC0.*”

Ex. 1005, 3:43–45 (emphasis added). We also preliminarily find that element 1.3 is met by Bains’s disclosure of receipt of command C and that “chip MC0 responds to command C as a read command.” *Id.* at 3:61–63.

We preliminarily find that Petitioner’s contentions are supported sufficiently by the cited portions of the asserted art. We further preliminarily find that Patent Owner’s contentions do not undermine Petitioner’s showing based on the preliminary record at this juncture of the proceeding. After considering the contentions and the evidence of record at this early stage, we determine that Petitioner has shown sufficiently that Bains teaches element 1.3 for purposes of institution.

f) Element 1.4

Petitioner relies on Bains for teaching element 1.4, which is “a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal.” Pet. 27–28. Relying on the testimony of Dr. Baker, Petitioner argues the following:

[T]he control circuit 32 controls switches Sw1-D . . . SwN-D and Sw1-S . . . SwM-S and thus whether ODT is “on” or “off.” EX1005 at 4:39–40. Bains further teaches that the number of switches that are closed by control circuit 32 determines the amount of resistance that is applied to the data pin. EX1005 at 4:40–42. Furthermore, Bains discloses that the particular command received determines what resistance value is set. As one example, “command A1 may cause one level of resistance in

the ODT and a command A2 may cause another level of resistance.” EX1005 at 4:42–44; EX1003 at ¶ 83.

Pet. 28.

We preliminarily find that Petitioner’s contentions are supported sufficiently by the cited portions of the asserted art. Patent Owner does not dispute Petitioner’s showing at this early stage. After considering the contentions and the evidence of record, we determine that Petitioner has shown sufficiently that Bains teaches element 1.4 for purposes of institution.

g) Element 1.5

Petitioner relies on Bains and the combination of Bains and JESD79-2A for teaching element 1.5, which is “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal.” Pet. 29–30, 57–60. In particular, Petitioner argues Bains “teaches that there may be a pin for controlling the ODT in addition to the commands.” *Id.* at 29 (citing Ex. 1005, 1:37–45, 6:30-37). Petitioner argues that a person having ordinary skill in the art would have understood Bains’s disclosure “to include the use of an ODT pin for controlling whether ODT is ‘on.’” *Id.* at 29–30 (citing Ex. 1003 ¶¶ 84–86).

Petitioner argues in the alternative “it would have been obvious to a POSITA to provide such a configuration.” *Id.* at 30 (citing Ex. 1003 ¶¶ 87–88). Petitioner argues “the ’523 Patent admits, and Bains discloses, that the use of an ODT pin to switch the termination on or off was well-known” and that Bains discloses “the use of command signals to set the resistance value.” *Id.* (citing Ex. 1003 ¶¶ 87–88).

Petitioner also relies on “Bains in view of JESD79-2A.” *Id.* at 57. In particular, Petitioner relies on JESD79-2A for teaching using an ODT pin

“for turning termination on and off” and determining “whether switches sw1 or sw2 in the termination circuit are enabled.” *Id.* at 58–59 (citing Ex. 1006, 14, 19, Fig. 15). Petitioner argues JESD79-2A teaches that “selection between sw1 or sw2 is determined by the EMRS.” *Id.* at 59 (citing Ex. 1006, 19, Fig. 15).

Petitioner, more specifically, argues the following:

In the combined system taught by Bains and JESD79-2A, the resistance value to be applied is a function of the control command signals as disclosed in Bains, and the ODT pin detailed in JESD79-2A is used to control when the switches are enabled to apply the selected resistance. In other words, the ODT pin controls when the switches are enabled according to first and second time delays tAOND and tAOFD, respectively (see Fig. 16, below), and control command signals A1, A2 through AN control which resistance level is applied, as discussed in Ground 1 with respect to limitation [1.4]. EX1006 at [19]; EX1003 at ¶ 139.

Id. at 59–60.

Patent Owner argues that it “does not concede that the ODT pin in Bains constitutes a termination port,” but “even if the ODT pin was a termination port, Bains does not disclose” the remainder of element 1.5. Prelim. Resp. 22. Patent Owner argues Petitioner’s analysis lacks “particularity and specificity required by 35 U.S.C. § 312(a)(3) and 37 C.F.R. §§ 42.22(a)(2), and 42.104(b)(4)–(5).” Prelim. Resp. 23. Patent Owner argues that Petitioner has not shown that control circuit 32 “acts in response to the ODT signal” and “the Petition does not even use the word ‘response’ in its discussion” of element 1.5. *Id.* at 24. Patent Owner argues that JESD79-2A also does not teach “the control circuit acting in response to the alleged termination signal.” *Id.* at 34.

Petitioner relies on Bains for teaching “use of an ODT pin for controlling whether ODT is ‘on’ in the system.” Pet. 29–30 (citing Ex. 1005, 1:37–45, 6:30–37; Ex. 1003 ¶¶ 84–88); *see also id.* at 30 (arguing “Bains discloses, that the use of an ODT pin to switch the termination on or off was well-known”). We preliminarily find Petitioner’s contentions consistent with Bains’s disclosure based on the record at this early stage. For instance, Bains describes using ODT pins “on the *controller* and the DIMM.” Ex. 1005, 1:40–42 (emphasis added). Bains also discloses in some embodiments “ODTs are *controlled* only *by* pins” and in other embodiments “the ODTs are *controlled* by commands sometimes and *by pins* at other times.” Ex. 1005, 6:30–37 (emphases added).

Petitioner also relies on JESD79-2A for teaching using an ODT pin “for turning termination on and off” and determining “whether switches sw1 or sw2 in the termination circuit are enabled.” Pet. 58–59 (citing Ex. 1006, 14, 19, Fig. 15). We preliminarily find Petitioner’s contentions consistent with JESD79-2A’s disclosure based on the record at this early stage. For instance, JESD79-2A describes that “On Die Termination (ODT) is a feature that allows a DRAM *to turn on/off termination resistance*” for signals “*via the ODT control pin.*” Ex. 1006, 18 (emphases added). JESD79-2A describes “Switch sw1 or sw2 is enabled by ODT pin.” *Id.* at 19.

We preliminarily find that the Petition provides analysis with particularity and specificity sufficient for purposes of institution. That ODTs are controlled by pins and ODT pins turn on or off termination resistance is consistent with Petitioner’s argument that the combination of Bains and JESD79-2A teaches that the control circuit is configured to terminate in response to the termination signal. Contrary to Patent Owner’s argument that

the Petition does not use “response” (Prelim. Resp. 24), the analysis in the Petition begins with reciting element 1.5 including “in response to the termination signal.” Pet. 29, 57. At this early stage, we do not find the Petition deficient simply for not using the word “response” more often in its analysis for element 1.5. To the extent that Patent Owner requires the prior art to use the exact terminology as the claim language, an obviousness analysis is not an *ipsissimis verbis* test. *Cf. In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

Regarding the remainder of element 1.5, we preliminarily find that both Bains and JESD79-2A teach selectively terminating the terminal with the set resistance. For instance, Bains describes “[t]he number of switches closed may determine the amount of resistance in the termination.” Ex. 1005, 4:39–41. Bains further describes “[f]or example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.” *Id.* at 4:42–44. JESD79-2A describes that “[s]witch sw1 or sw2 is enabled by [the] ODT pin” and “[s]election between sw1 or sw2 is determined by ‘R_{tt} (nominal)’ in EMRS.” Ex. 1006, 19.

We preliminarily find that Petitioner’s contentions for element 1.5 are supported sufficiently by the cited portions of the asserted art. As discussed above (*see* § III.D.3.a), at this stage, Petitioner’s reasons for combining Bains and JESD79-2A are sufficiently persuasive for institution. We further preliminarily find that Patent Owner’s contentions do not undermine Petitioner’s showing based on the preliminary record at this juncture of the proceeding. After considering the contentions and the evidence of record at this early stage, we determine that Petitioner has shown sufficiently that the

combination of Bains and JESD79-2A teaches element 1.5 for purposes of institution.⁵

h) Element 1.6

Petitioner relies on Bains and the combination of Bains and JESD79-2A for teaching element 1.6, which is “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.” Pet. 30–33, 60–64. In particular, Petitioner relies on Bains for teaching “ODT in chip MC1 is turned on after a delay of tAOND” and after command A “is asserted and turned off automatically after a fixed delay based on a burst length of 8 associated with the write command.” *Id.* at 31 (citing Ex. 1005, 4:47–61, 5:23–42, Figs. 2, 5, 7). Petitioner argues a person having ordinary skill in the art “would have understood or found obvious that the first and second delays are relative to the ODT signal, rather than the command signal.” *Id.* at 32.

Petitioner also relies on JESD79-2A for teaching

the chip’s control circuit terminates the terminal as a function of the termination signal ODT . . . after a first time delay tAOND . . . that runs from when the ODT signal goes high (on), and does not terminate the terminal after a second time delay tAOFD . . . that runs from when the ODT signal goes low (off).

Id. at 60–61 (citing Ex. 1006, 19, 65, Fig. 16).

⁵ In light of our determination, we need not making findings as to whether Bains alone teaches element 1.5.

Patent Owner argues “the Petition fails to make a connection between the timing diagram shown in Figure 7 and control circuit 32.” Prelim. Resp. 25. In particular, Patent Owner argues “nothing in Bains suggests that the control circuit receives [the signal on the ODT pin] as an input” and “the memory controller in Bains is a separate structure from the memory chips and the control circuits.” *Id.* With respect to Petitioner’s arguments relating to JESD79-2A, at this early stage, Patent Owner relies on its arguments that the rationale to combine is deficient. *Id.* at 33–39.

Contrary to Patent Owner’s argument regarding the lack of connection in the Petition between the timing diagram in Figure 7 and the control circuit, shown in Figure 2, Petitioner explains the following:

Fig. 7 is a timing diagram illustrating the operation of the system of Fig. 5, which includes a rank 0 of chips MC0-0 to MC0-N and a rank 1 of chips MC1-0 to MC1-N. EX1005 at 5:23–42. The operation of the systems in Figs. 2 and 5 are otherwise the same, and chips MC0 and MC1 in Fig. 2 operate the same as chips MC0-0 through MC0-N and MC1-0 through MC1-N in Fig. 5, respectively. EX1005 at 4:47–61.

Pet. 31 n.4. We preliminarily find Petitioner’s explanation consistent with Bains’s teachings.

With respect to Patent Owner’s arguments that the Petition does not show that control circuit 32 receives the termination signal and the memory controller is a separate structure, Bains describes that ODTS “are *controlled*” by pins in some embodiments. Ex. 1005, 6:33–37 (emphasis added). Bains describes “commands referred to in this disclosure may be provided from memory controller 12 to chips MC0 and MC1 through various ways” and “[c]ontrol circuitry 32 in chip MC0 and control circuitry 42 *receive* the commands from controller 12.” *Id.* at 3:17–27 (emphasis added).

Furthermore, Bains describes with respect to Figure 7 that “command A is

issued” in clock cycle 0, in clock cycle 3 “the ODT in each of chips MC1-0 . . . MC1-N (rank 1) is turned on after a delay of tAOND” (*id.* at 5:26–30), and in the combined system “the ODT pin controls when the switches are enabled according to first and second time delays tAOND and tAOFD.” Pet. 59; *see also id.* at 32 (arguing that a person having ordinary skill in the art “would have understood or having found obvious that the first and second delays are relative to the ODT signal, rather than the command signal”).

We preliminarily find that Petitioner’s contentions for element 1.6 are supported sufficiently by the cited portions of the asserted art. As discussed above (*see* § III.D.3.a), at this stage, Petitioner’s reasons for combining Bains and JESD79-2A are sufficiently persuasive for institution. We further preliminarily find that Patent Owner’s contentions do not undermine Petitioner’s showing based on the preliminary record at this juncture of the proceeding. After considering the contentions and the evidence of record at this early stage, we determine that Petitioner has shown sufficiently that the combination of Bains and JESD79-2A teaches element 1.6 for purposes of institution.⁶

i) Conclusion—Claim 1

After consideration of the arguments and the evidence of record at this early stage, we determine that Petitioner has shown sufficiently, for purposes of institution, that the combination of Bains and JESD79-2A teaches all recitations in claim 1. Also, at this juncture, we are persuaded that Petitioner has articulated sufficiently persuasive reasoning, based on the evidence of record, as to why one of ordinary skill in the art would have made

⁶ In light of our determination, we need not making findings as to whether Bains alone teaches element 1.6.

Petitioner's proposed modifications. Petitioner's arguments that a person having ordinary skill in the art would have had a reasonable expectation of success also are sufficient for purposes of institution. We find that Patent Owner's arguments do not undermine Petitioner's showing at this early stage.

Accordingly, we conclude that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claim 1 is unpatentable under 35 U.S.C. § 103 as obvious over the combination of Bains and JESD79-2A.

4. *Independent Claims 5 and 9*

Independent claims 5 and 9 are similar to independent claim 1. Petitioner provides detailed contentions regarding all differences in the claims. Pet. 39–46, 64–69. For claim 5, Patent Owner relies on the same arguments it presented for claim 1.

For claim 9, Patent Owner argues “Petitioner incorrectly treats limitation [9.4] as interchangeable with limitation [1.5].” Prelim. Resp. 26. Patent Owner acknowledges “Petitioner argues that ‘Bains teaches a termination enable signal received via an ODT pin which turns termination on and off.’” *Id.* at 28–29 (citing Pet. 46). Patent Owner argues “[b]ut, even if a signal turns termination on or off, it does not follow that the presence of the signal ‘is required for the terminating to occur.’” *Id.* at 29.

At this early juncture, we find Patent Owner's attorney argument to be unsupported by the evidence of record. Argument of counsel cannot take the place of evidence lacking in the record. *Meitzner v. Mindick*, 549 F.2d 775, 782 (CCPA 1977). We preliminarily find Bains's teaching that control circuitry 32 “controls the switches and hence whether ODT 38 is ‘on’”

(Ex. 1005, 4:39–40) in connection with other teachings in Bains discussed with respect to claim 1 (*see* § III.D.3.g) to be contrary to Patent Owner’s arguments regarding claim 9. We preliminarily find that Petitioner’s contentions for claims 5 and 9 account for all differences between those claims and claim 1.⁷

After considering the arguments and the evidence of record at this early stage, we determine that Petitioner has shown sufficiently, for purposes of institution, that the combination of Bains and JESD79-2A teaches all recitations in claims 5 and 9. Also, at this juncture, we are persuaded that Petitioner has articulated sufficiently persuasive reasoning, based on the evidence of record, as to why one of ordinary skill in the art would have made Petitioner’s proposed modifications. Petitioner’s arguments that a person having ordinary skill in the art would have had a reasonable expectation of success also are sufficient for purposes of institution. We find that Patent Owner’s arguments do not undermine Petitioner’s showing at this early stage for the same reasons given with respect to claim 1.

Accordingly, we conclude that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claims 5 and 9 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Bains and JESD79-2A.

⁷ Petitioner states “[a]s an initial matter, ‘the termination enable signal’ in limitation [9.3] lacks proper antecedent basis.” Pet. 46. Petitioner further states “[h]owever, if ‘the termination enable signal’ is meant to refer to the later-claimed ‘termination enable signal.’” *Id.* We understand the later statement to be Petitioner’s interpretation of the recitation and we use that interpretation herein.

5. *Dependent Claims 2, 6, and 10*

Petitioner contends that dependent claims 2, 6, and 10 would have been obvious over the combination of Bains and JESD79-2A. Petitioner provides a detailed analysis in support of its position that the combination of Bains and JESD79-2A teaches the limitations in these dependent claims, which Patent Owner does not contest separately at this preliminary stage.

Accordingly, we conclude that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that claims 2, 6, and 10 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Bains and JESD79-2A.

IV. CONCLUSION

For the foregoing reasons, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in showing that claims 1, 2, 5, 6, 9, and 10 of the '523 patent are unpatentable. At this preliminary stage, we have not made a final determination as to the patentability of the challenged claims or any underlying factual and legal issues.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1, 2, 5, 6, 9, and 10 of the '523 patent is hereby instituted on all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision.

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