UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner

Case No.: IPR2023-00513
Patent No.: 7,532,523 B2
For: Memory Chip with Settable Termination Resistance Circuit

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DECLARATION OF TIMOTHY D. DORNEY, PH.D.

PURSUANT TO 37 C.F.R. § 1.68

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  - 2. Claim Elements 1.3, 5.5, & 9.1, “a control command port for receiving a control command signal *for affecting accessibility of the memory chip*” are not disclosed in Bains 49

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3. Claim Elements 1.5 & 5.8, "wherein the control circuit is configured to selectively terminate the terminal … *in response to the termination signal*" are not disclosed in Bains 54

4. Claim Elements 2.1 & 6.1, "wherein the control circuit is configured such that, as *a function of the received control command signal*, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time" are not disclosed in Bains 60

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1. Claim Elements 1.3, 5.5, & 9.1, "a control command port for receiving a control command signal *for affecting accessibility of the memory chip*" are not disclosed in Bains in view of JESD79-2A 70

2. Claim Elements 1.5 & 5.8, "wherein the control circuit is configured to selectively terminate the terminal … *in response to the termination signal*" are not disclosed in Bains in view of JESD79-2A 71

3. Claim Elements 2.1 & 6.1, "wherein the control circuit is configured such that, as *a function of the received control command signal*, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time" are not disclosed in Bains in view of JESD79-2A 75

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LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.P]	A memory chip for variably setting terminations, comprising:
[1.1]	a terminal;
[1.2]	a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;
[1.3]	a control command port for receiving a control command signal for affecting accessibility of the memory chip;
[1.4]	a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and
[1.5]	a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,
[1.6]	wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.
Claim 2	
[2]	The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

Claim 5	
[5.P]	A system, comprising:
[5.1]	(a) a memory controller having a terminal;
[5.2]	(b) a plurality of memory chips, at least one of the memory chips comprising:
[5.3]	a terminal;
[5.4]	a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;
[5.5]	a control command port for receiving a control command signal for affecting the accessibility of the memory chip; and
[5.6]	a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;
[5.7]	(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and
[5.8]	(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,
[5.9]	wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.
Claim 6	
[6]	The system of claim 5, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

Claim 9	
[9.P]	A method for operating a memory chip, comprising:
[9.1]	receiving a control command signal for affecting accessibility of the memory chip;
[9.2]	setting a resistance value for a terminal as a function of the control command signal;
[9.3]	terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and
[9.4]	receiving a termination enable signal, the presence of which is required for the terminating to occur.
Claim 10	
[10]	The method of claim 9, further comprising: changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and terminating the terminal with the changed resistance value.

I, Timothy D. Dorney, Ph.D., do hereby declare:

I. INTRODUCTION

1. I am making this declaration ("Declaration") at the request of Patent Owner Polaris Innovations Limited ("Polaris") in the matter of the *Inter Partes* Review No. IPR2023-00513 of U.S. Patent No. 7,532,523 ("the '523 Patent").

2. I have been asked to consider whether or not a person of ordinary skill in the art ("POSITA") would have found the invention in the '523 Patent as set forth by the original claims 1, 2, 5, 6, 9, and 10 are obvious in light of the material made available to me in this case.

3. In this declaration, I set forth my opinions concerning the general subject matter of the original claims in the '523 Patent, including the state of the art in DRAM memory design in the 2000s. My opinions are based on my knowledge, education, experience, and a review of the material provided to me in this case.

4. I understand that the PTAB has instituted an *Inter Partes* Review of claims 1, 2, 5, 6, 9, and 10 of the '523 Patent based on the arguments presented in the Petition (IPR2023-00513, Document 2) as supported by the Declaration of Dr. R. Jacob Baker (IPR2023-00513, Ex. 1003) ("the Baker Declaration"). Claims 1, 5, and 9 are independent claims.

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5. I understand that two grounds for challenging the patentability of the claims were presented. The first ground challenged claims 1, 2, 5, 6, 9, and 10 as obvious over U.S. Patent No. 7,433,992 to Bains ("Bains"). The second ground challenged claims 1, 2, 5, 6, 9, and 10 as obvious over Bains in view of JEDEC STANDARD, Double Data Rate (DDR) 2 SDRAM Specification, JESD79-2A ("JESD79-2A").

6. I reserve the right to supplement or amend this Declaration based on any additional information that becomes known that affects my opinions.

7. I am being compensated for my work in this matter at an hourly rate of $400 for consulting services. My compensation for this matter is neither determined by nor contingent on the outcome of this case.

II. PROFESSIONAL BACKGROUND

8. I earned a Bachelor of Science degree in Electrical Engineering from Texas A&M University in College Station, Texas, in 1990.

9. I earned a Master of Science degree in Electrical Engineering and Applied Physics from Case Western Reserve University in Cleveland, Ohio, in 1992.

10. I earned a Doctor of Philosophy degree in Electrical and Computer Engineering from Rice University in Houston, Texas in 2002.

11. I have extensive experience with semiconductor dynamic random access memory design and architecture. I was employed by Texas Instruments Incorporated in the Memory Products Group from 1988 to 1998. During that time, I was an engineer in the Circuits Center of Expertise, an integrated circuit design engineer, and a product development engineer.

12. The goal of the Circuits Center of Expertise was to investigate issues and provide solutions for future circuit designs that would be common across multiple devices.

13. As an integrated circuit design engineer, I worked on application specific memory designs for numerous devices including Video Random Access Memory (VRAM) and Synchronous Random Access Memory (SDRAM). As a DRAM memory designer, I was responsible for circuit design, circuit layout, and pre- and post-silicon verification. Design areas included row and row redundancy, column and column redundancy, design-for-test, I/O buffers, internal refresh, and data I/O. I performed full-chip schematic verification, design rule verification, and probe versus simulation comparison. I supported the lead frame design, ESD implementation, parasitic back annotation, laser repair, and device layout and routing.

14. I supported the identification and solution for design issues encountered by video card/graphics processor design companies. As a product

development engineer, I also used memory device testing systems to investigate memory device parameter characterization and failure mechanisms.

15. While employed at Texas Instruments Incorporated (TI), I traveled to Japan (KTI) and Singapore (TECH) to provide DRAM design support and training. I also traveled to TI-Singapore for DRAM T3/batch testing support. The training educated engineers about the new design functionality and test capabilities of forthcoming devices. Also, I was tasked with leading a team to create internal training materials on the basics of DRAM operation and to provide on-site training to TI's worldwide locations.

16. In 1998, I left Texas Instruments Incorporated to pursue my Doctor of Philosophy degree full-time. During my time at Rice University, I investigated processor design and researched the effects of modifying DRAM parameters on the processing system; I investigated efficiency improvements using wavelet-based image compression; and I investigated computed tomography and methodologies to improve imaging.

17. My thesis research involved material parameter estimation and imaging using terahertz frequency waves. The terahertz frequency band is above the microwave frequency band and below the infrared frequency band. This research, using a fiber optic coupled, terahertz time-domain spectroscopy system,

often centered on providing computer calculated graphical and synthetic image representations resulting from solutions of inverse problems.

18. Upon completion of the Ph.D. degree requirements, I was employed by Rosenthal & Osha L.L.P., to draft and prosecute patent applications. Major clients included Sun Microsystems, which was a processor and computer manufacturer, and NASA's Johnson Space Center. In 2003, I started working in patent licensing, first at Texas Instruments Incorporated and then at Personalized Media Communications, LLC, which has involved investigating patents and products from technical fields including DRAM and nonvolatile memory, analog circuits, image sensors, digital displays, processors, digital systems, video streaming, and Internet communications.

19. In 2005, I formed a company to focus on an optical delay system that would be relevant to the terahertz systems involved in my Doctor of Philosophy research. In 2009, the name of the company was changed to Uviri, LLC, as my interests expanded to basic research, development of consumer products, photography, and consulting. Many of the consumer products designs require an embedded microcontroller to support the desired operation. During my work at Uviri, LLC, I have also been involved in 2D image editing including layering and masks using Photoshop, and 3D photo-realistic rendering using Keyshot.

20. I am a member of the Institute of Electrical and Electronics Engineers (IEEE). I am a member of the IEEE honor society Eta Kappa Nu and the engineering honor society Tau Beta Pi. I passed the Texas Board of Professional Engineers and Land Surveyors: Fundamentals of Engineering exam while pursuing a Bachelor of Science degree in Electrical Engineering from Texas A&M University. In 2002, I became a registered patent agent. I am listed as an inventor on at least ten domestic or foreign patents. The subject matter of the majority of these inventions includes improvements to the performance and/or capabilities of dynamic random access memory.

21. A more complete summary of my background, qualifications, and professional experience and affiliations is set forth in my *curriculum vitae*, which is attached hereto as Appendix A, and includes a list of my patents and publications. Also included in my *curriculum vitae* is a complete list of the cases in which I have testified as an expert or have been deposed.

III. MATERIALS REVIEWED AND RELIED UPON

22. In the course of preparing this Declaration, I reviewed the following documents:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,532,523 ("Petition")
- Ex. 1001 U.S. Patent No. 7,532,523 ("the '523 Patent")
- Ex. 1002 Prosecution history of the '523 Patent ("Application")

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- Ex. 1003 Declaration of Dr. R. Jacob Baker ("the Baker Declaration")
- Ex. 1005 U.S. Patent No. 7,433,992 to Bains ("Bains")
- Ex. 1006 JEDEC STANDARD, Double Data Rate (DDR) 2 SDRAM Specification, JESD79-2A ("JESD79-2A")
- Ex. 1007 U.S. Patent No. 7,092,299 to Kwak et al. ("Kwak")
- Ex. 1009 U.S. Patent No. 6,754,132 to Kyung ("Kyung")
- Patent Owner's Preliminary Response for IPR2023-00513
- Decision Granting Institution of *Inter Partes* Review for IPR2023-00513 ("Institution Decision")
- U.S. Patent No. 6,762,620 to Jang et al. ("Jang")
- U.S. Patent No. 7,148,721 to Park ("Park")
- Micron 2Gb DDR2 SDRAM ("Micron DDR2 SDRAM") (attached as Appendix B)
- Various technical dictionaries (attached as Appendix C)

IV. LEGAL STANDARDS

23. I am not an attorney. I have been advised of the following general principles of patent law to be considered in formulating my opinions as to whether the claims of the '523 Patent would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the invention in view of the prior art.

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A. Obviousness

24. I understand that a prior art reference can render a patent claim obvious to one of ordinary skill in the art if the differences between the subject matter set forth in the patent claim and the prior art are such that the subject matter of the claim would have been obvious at the time the claimed invention was made. In analyzing obviousness, I understand that it is important to consider the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any secondary considerations.

25. I understand that when the claimed subject matter involves combining preexisting elements to yield no more than one would expect from such an arrangement, the combination is obvious. I also understand that in assessing whether a claim is obvious, one must consider whether the claimed improvement is more than the predictable use of prior art elements according to their established functions. I understand that there need not be a precise teaching in the prior art directed to the specific subject matter of a claim because one can take account of the inferences and creative steps that a person of ordinary skill in the art would employ. I further understand that a person of ordinary skill is a person of ordinary creativity, not an automaton. However, I understand that obviousness cannot be based on the hindsight combination of components selectively culled from the

prior art. I also understand that a combination is not obvious if it requires extensive additional problem-solving steps that are not taught in the references and that are not simple matters for a person of ordinary skill in the art. That is, a combination is not obvious if it requires the development of an additional complex infrastructure.

26. I understand that, when there is a reason to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. I further understand that, if this leads to the anticipated success, it is likely the product, not of innovation, but of ordinary skill and common sense, which bears on whether the claim would have been obvious.

B. Claim Construction Standard

27. It is my understanding that in determining whether a patent claim is anticipated or obvious in view of the prior art, the PTAB must construe the claim using the federal court claim construction standard that is used to construe a claim in a civil action under 35 U.S.C. § 282(b). This is the same claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) ("*Phillips*"), and its progeny.

28. The *Phillips* standard requires the claims be given their ordinary and customary meaning to a person of ordinary skill in the art at the time of the

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invention, by considering the claims, specification, and prosecution history, as well as evidence extrinsic to the patent, when construing patent claims.

29. For the purposes of this Declaration, unless otherwise stated, I have construed each claim term in accordance with the *Phillips* standard.

V. THE ’523 PATENT

30. The ’523 Patent was filed as U.S. Application No. 11/461,380 on July 31, 2006, and was issued as U.S. Patent No. 7,532,523 B2 to Braun et al. on May 12, 2009. The ’523 Patent is entitled “Memory Chip with Settable Termination Resistance Circuit.”

A. Overview of the ’523 Patent Background

31. As explained in the Background of ’523 Patent, the invention is generally concerned with “a memory chip having a terminal for sending and/or receiving high-frequency signals.” (Ex. 1001, 1:18-20.)

32. In general, there is a strong desire to send and/or receive greater amounts of data between a memory device and its controller. A “chunk” of data is transmitted at one time in what is commonly known as a “word.” Clearly, more data may be transmitted if the word size is increased; however, a larger word requires more routing, both inside the memory device and on the printed circuit board(s) that connect the memory device to a controller. Also, pin count is directly correlated to the cost of a device. Increasing the number of pins on a device to

enable more data to be transmitted at a given time using an increased word size directly affects cost.

33. Also, to send and/or receive greater amounts of data between a memory device and its controller, data may be transmitted at a higher frequency so that more words may be transmitted within a given time. Double Data Rate (DDR) memories transmit data in groups of words. For example, a burst length of four (4) transmits four (4) words of data in a sequential group. A burst length of eight (8) transmits eight (8) words of data in a sequential group. Under this approach, increasing data bandwidth involves increasing the frequency of transmission (i.e., shrinking the time any given word is available).

34. For example, the JESD79-2A specification shows a burst length of four (4) (BL=4, top), and a burst length of eight (8) (BL=8, bottom) in the following drawings (emphasis added):

2.2.4.3 Burst Read Command (cont'd)

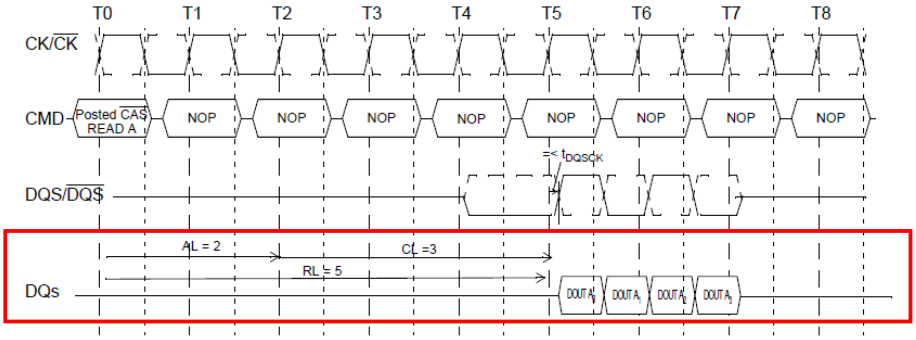

Figure 24 — Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

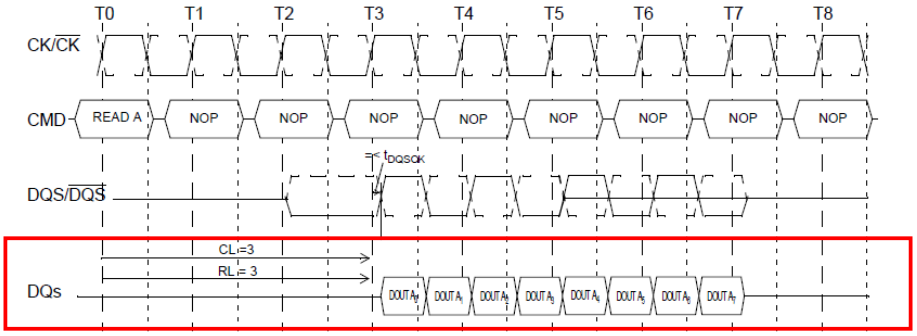

Figure 25 — Burst Read Operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

35. In practice, both the word size and transmission frequency are adjusted to optimize the data transmission bandwidth.

36. The Background of '523 Patent explains the issue that arises when the transmission frequency increases in the following paragraph:

> In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one

> another and to a memory controller. However, during transmission of high-frequency signals, signal reflections that disturb the data transmission on the memory bus and thereby limit the data transmission rates can occur at the terminals of the memory chips. It is necessary for this reason when transmitting data via the memory bus to provide suitable terminations at the terminals of the memory chips in order to reduce the signal reflections on the signal lines. (Ex. 1001, 1:23-36.)

37. The Background of ’523 Patent recognizes that signal reflections degrade the data signals, which in turn, limits the transmission frequency. The solution is using terminating resistors to reduce the disturbance to the signal lines.

38. On Die Termination (ODT) applies resistors to reduce signal reflections on the data lines in a computing system. The resistors are part of the DRAM, and the connection of the ODT resistors to the data lines is typically controlled by an ODT pin on the DRAM. As such, the host processor can control which DRAMs should apply their ODT resistors, during which operations, and to some degree, the timing of when the ODT resistors should be applied.

39. However, having a fixed terminating resistance value is not optimal in all cases; therefore, switching terminating resistors on and off, depending on the operating state, has been a prior art approach. The ’523 Patent Background explains the following:

> The disadvantage of such a control of the memory chips consists in that switching the terminating resistors on and off is not sufficient as a rule to achieve an optimal termination in every operating state, and thus, also not sufficient to improve the data transmission via the memory bus. (Ex. 1001, 1:44-49.)

40. As an improvement, the prior art allowed a fixed resistance value dependent on a configuration value communicated to a memory device. The fixed value could be changed; however, adjusting to a new fixed value before each change in operating state is time consuming, and therefore suboptimal. The '523 Patent Background explains the following:

> Setting the configuration values in the memory chips before each write and read operation is time consuming. Consequently, the initial presetting of the terminating resistor by the configuration value is also not suitable for providing terminating resistors for applying to the memory bus that are suitable for every case of addressing the memory chips of the memory system, since the access time in the memory system would thereby be slowed down substantially. (Ex. 1001, 1:55-62.)

41. The '523 Patent teaches an apparatus, system, and method to switch *between termination resistance values* without the overhead of having to send configuration values between changes in operating state. In other words, the '523

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Patent teaches, in part, that more than one resistance value is available to be selected. Simply applying or not applying a resistance value is **not** switching between termination resistance values. Having the absence of a resistance value (i.e., switching a terminating resistor "off") creates a floating node, which has no set resistance value. Advantageously, by removing the time necessary to set the termination resistance value contemporaneously for each new operating state, more time can be spent accessing data, which improves data bandwidth.

B. The Challenged Claims

42. Claims 1, 2, 5, 6, 9, and 10 of the '523 patent are reproduced below:

[1.P] A memory chip for variably setting terminations, comprising:

[1.1] a terminal;

[1.2] a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

[1.3] a control command port for receiving a control command signal for affecting accessibility of the memory chip;

[1.4] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

[1.5] a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,

[1.6] wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

[2.P] The memory chip of claim 1,

[2.1] wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

. . .

[5.P] A system, comprising:

[5.1] (a) a memory controller having a terminal;

[5.2] (b) a plurality of memory chips, at least one of the memory chips comprising:

[5.3] a terminal;

[5.4] a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;

[5.5] a control command port for receiving a control command signal for affecting accessibility of the memory chip; and

[5.6] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;

[5.7] (c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and

[5.8] (d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,

[5.9] wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

[6.P] The system of claim 5,

[6.1] wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

. . .

[9.P] A method for operating a memory chip, comprising:

[9.1] receiving a control command signal for affecting accessibility of the memory chip;

[9.2] setting a resistance value for a terminal as a function of the control command signal;

[9.3] terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and

[9.4] receiving a termination enable signal, the presence of which is required for the terminating to occur.

[10.P] The method of claim 9, further comprising:

[10.1] changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and

[10.2] terminating the terminal with the changed resistance value.

C. Prosecution History

43. Claims 1-26 were originally filed in U.S. Application No. 11/461,380 on July 31, 2006. Claims 1, 11, and 21 were independent claims. Minor amendments to clean up the language in claims 1, 5, and 11-20 were filed November 2, 2007, prior to examination. The first office action mailed June 19, 2008 objected to claims 6-9, 16-19, and 25-26. The remaining claims were rejected under 35 U.S.C. § 102(b) over U.S. Patent 6,762,620 to Jang et al. ("Jang"), and separately under 35 U.S.C. § 102(b) over U.S. Patent 7,148,721 to Park ("Park"). On September 19, 2008, Applicants amended the claims objected to by the Examiner to put them into a condition for allowance. Claims 6, 16, 17, and 25 were amended, and rejected claims cancelled. Accordingly, claims 6, 16, and 25 became independent claims. A Notice of Allowance was mailed on January 13, 2009, and the application issued on May 12, 2009 as U.S. Patent No. 7,532,523 B2.

44. In the final response to office action filed on September 19, 2008, (Ex. 1002, pg. 50/201), the response stated, "Applicants are not conceding in this

application that those claims (i.e., pre-amended and/or canceled claims) are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the Examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications." Accordingly, the failings of the June 19, 2008 office action were never discussed.

45. Jang discloses a variable impedance termination circuit applied to terminals of a device dependent on a command and an external resistance to set the variable impedance value. (Jang, Figs. 3-5.)

46. In the first office action mailed June 19, 2008, the Examiner failed to address the claim 1 requirements "for affecting accessibility of the memory chip" (Ex. 1002, pg. 60/201.)

47. Furthermore, the Examiner stated "Jang et al. show a termination port (see Fig. 4: MRS_DQi) to receive a termination signal (Fig. 4: MRS_DQi) the control circuit (Fig. 4: 300) being configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal (see Fig. 4: MRS_DQi from 200 to 300 with respect to Fig. 6-1: MRS_DQi to 300 to control the output of ICONPi and ICONNi with respect to

Fig. 7: ICONP1 ... ICONPn and ICONN1 ... ICONNn control the selection of resistors DRP1 ... DRPn and DRN1 ... DRNn)." (Ex. 1002, pg. 61/201.)

48. In Jang's Fig. 4, MRS_DQi is an internal signal, which cannot be "a termination port to receive a termination signal" for the memory chip as claimed. The Application clears teaches and claims a "port" is for receiving an externally applied "termination signal." Accordingly, the Examiner cannot use Jang to show or suggest "the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal" as claimed.

49. Park discloses a variable impedance termination circuit applied to terminals of a memory device dependent on a command and an external resistance to set the variable impedance value. (Park, Fig. 2.)

50. In the first office action mailed June 19, 2008, the Examiner failed to address the claim 1 requirements "for affecting accessibility of the memory chip" (Ex. 1002, pg. 63/201.)

51. Furthermore, the Examiner stated "Park shows a termination port (see Fig. 2: PAD1 ... PAD3) to receive a termination signal (see Fig. 2: PAD1 ... PAD3 connecting to 230 outputting a signal to 330 outputting SEL) the control circuit (Fig. 2: 340) being configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal (see Fig. 2: 340 outputting UPC and DNC to control the selection of certain

Termination resistors of 290; see Fig. 11: 64WP ... 1 WP and 64WN ... 1 WN with respect to 1 R ... 64R)." (Ex. 1002, pg. 64/201.)

52. Park's Fig. 2, block 230 is labeled as "Address & Command Buffer", and described as "the address/command buffer 230 is connected to pads PAD1-PAD3 through input transfer lines TL IN1-TL IN31 to receive address and command signals from the external (e.g., a memory controller) in pre-designed timings." (Park, 6:24-28.) Contrary to the Examiner's conclusions, PAD1-PAD3 do not show or suggest that any of these pads is a "termination port to receive a termination signal" as claimed, nor has the ability "to selectively terminate the terminal with the set resistance value in response to the termination signal" as claimed. Park is silent as to a set resistance that is selective applied in response to a termination signal, especially given that the claims require "a control command signal" is different than "a termination signal."

53. The above review of the Examiner's statements with regards to Jang and Park are not meant to be a complete and full review. The observations above particularly point out some of the failings of the June 19, 2008 office action. Other issues may also exist.

54. Nothing in the prosecution history suggests that any claim constructions were formed in discussions between the Examiner and the Applicants. Further, the Examiner failed to take a position such that a claim

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construction may be based on what the Examiner understood. The Examiner failed to provide any showing in the prior art for the requirement "for affecting accessibility of the memory chip" as claimed. The Examiner failed to consistently apply "a termination port to receive a termination signal" in the prior art. The Application clearly teaches "a termination port" is provided as a mechanism to receive "a termination signal" from external the memory device, and that the claimed "termination signal" is different than the claimed "control command signal." As such, this external signal (i.e, termination signal) causes the control circuit "to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal".

55. Both Jang and Park appear to only set a resistance based on a command control signal, which determines an internal fixed resistance, while a fixed external resistor sets an internal variable resistance. One of the key elements of the '523 Patent's invention is to prevent "[s]etting the configuration values in the memory chips before each write and read operation" (Ex. 1001, 1:55-56) because this wastes time. One aspect of the '523 Patent's invention is "a termination port to receive a termination signal" that can contemporaneously terminate the terminal in response to the termination signal. The "termination port to receive a termination signal … to selectively terminate the terminal with the set resistance value" as claimed, is a means to bypass having a enter a command "to

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selectively terminate" before each write and read operation because of the wasted time created by a command entry step.

VI. BAINS (EXHIBIT 1005)

56. Bains was filed as U.S. Application No. 10/992,953 on November 18, 2004, and was issued as U.S. Patent No. 7,433,992 B2 on October 7, 2008. Bains is entitled "Command Controlling Different Operations in Different Chips."

A. Overview of Bains' Background

57. In the Background, Bains is concerned with the prior art arrangement to apply On Die Termination (ODT) because Bains is concerned with rank 2 configurations. Bains' need for a single command to cause different operations in different chips results from the dual-rank memory system configuration the reference discloses.

58. As Bains explains, "the term rank refers to a group of memory chips that are selected together." (Ex. 1005, 1:28-29.) This is consistent with the industry meaning for the term. Fig. 2 in Bains provides an illustration of a dual-rank memory system according to its embodiments.

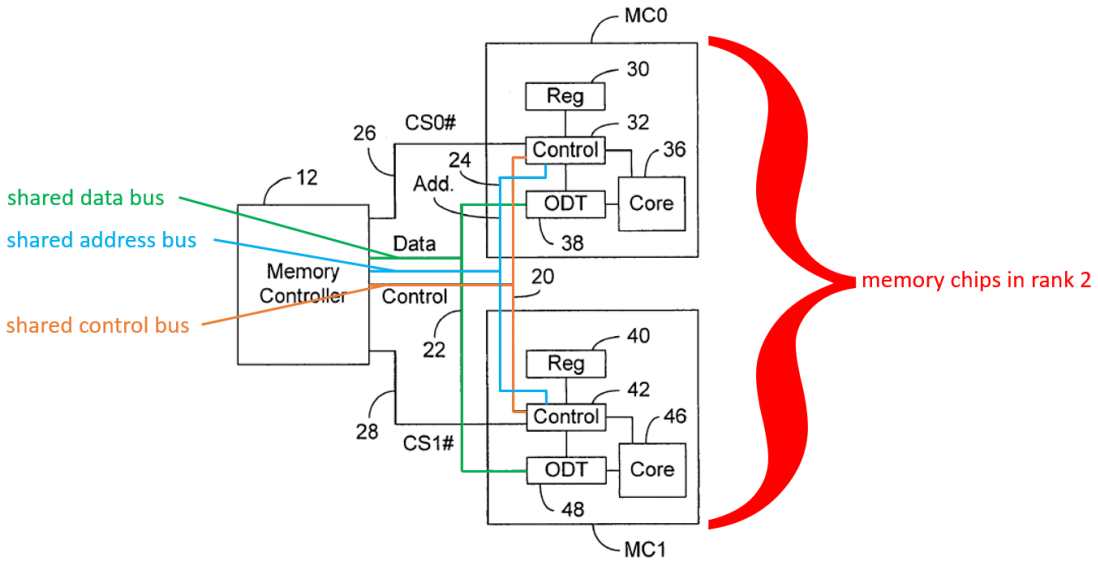

FIG. 2

(Ex. 1005, 3:9-4:6, Fig. 2, annotations added.) In the above illustration, memory chips MC0 and MC1 each comprise a rank.

59. As Bains Fig. 2 illustrates, memory chips MC0 and MC1 share common data, address, and control buses; however, MC0 and MC1 respond to different chip select signals (i.e., CS0# and CS1#). (Ex. 1005, 3:9-16.) This is a common configuration for dual-rank memory systems. As a result, of this configuration, signals sent on these common interconnects are received by both MC0 and MC1. Commands sent on control bus 20 are received by MC0 and MC1. Similarly, data sent on data bus 22 is received by MC0 and MC1. Thus, an instruction to MC0 to write the data on the data bus to memory is simultaneously received by MC1. To avoid a duplicative write operation on MC0 and MC1, Bains discloses using different command mappings and an on die termination ("ODT").

(Ex. 1005, 2:47-67; 3:37-4:6.) For example, Bains discloses command A causing MC0 to perform a write operation and MC1 to turn on an ODT. (Ex. 1005, 2:49-52.)

60. Bains discloses the following concerning the then current DDR2 DRAM chips:

> In DDR2 DRAM chips, the ODTs are controlled by using discrete signals per rank. In some two rank-1 DIMM systems, two ODT pins are used on the controller and the DIMM. Two pins may also used per DRAM chip to support stacking solutions. As used in this disclosure, the word "pin" means traditional pins or other connections to die pads. (Ex. 1005, 1:39-45.)

61. Bains goes on to note that snooping the state of WE (Write Enable) and CS (Chip Select) in proposed standards may be used to determine if ODT should be turned on; however, Bains states this is suboptimal because snooping may cause additional clock cycles. Bains states the following:

> In GDDR3 (graphics DDR3) and also DDR3/DDR2 proposals, the command bus may be shared between two ranks. *The DRAM can monitor or snoop the command bus for a write transaction. If it sees a write cycle and no CS# asserted then, it can turn its ODT on.* The write command may target the other rank. (CS# are rank or device specific). The term "2N timing" refers to a situation in

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> which it takes an extra clock cycle for sampling as compared to a 1N timing. The sampling may be of a signal, such as an address signal. Snooping may work well for 1N timings, but not for 2N timings (with an additional clock cycle before sampling) because *snooping may cause additional clock cycles in turnaround cycles* and in leadoff write cycles. (Ex. 1005, 1:46-58, emphasis added.)

62. Bottom line, Bains' invention addresses the time wasted by snooping individual signals that may use an additional clock cycle to define the memory chip's operation.

B. Bains' Disclosure

63. In Fig. 10 (similar to Fig. 2 above), Bains discloses a memory controller 12 connected to two memory chips (MC0, MC1). To communicate between the memory controller 12 and memory chips (MC0, MC1), "data, addresses, commands, and chip select signals may be on different conductors or may be shared on at least some of the same conductors." (Ex. 1005, 2:40-43.) Fig. 10 is shown below:

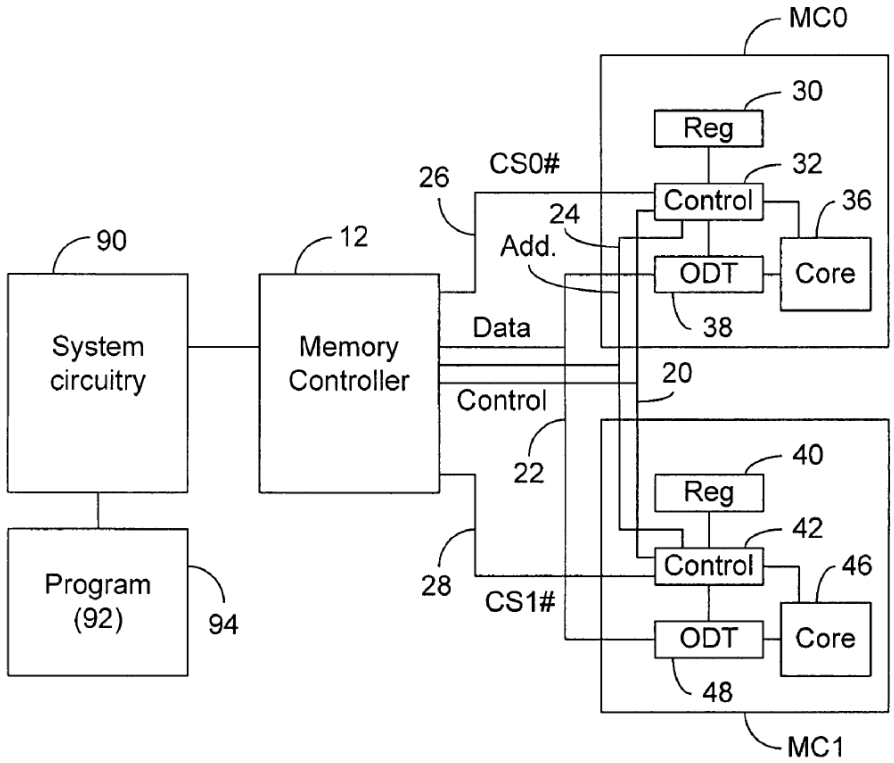

FIG. 10

64. Each memory chip contains a register (30 or 40), which determines that chip's operation to a given command. In this fashion, *each memory chip may respond differently to the same received command*. In particular, *for a command A, one memory chip may perform a write operation while the other memory chip turns on the ODT*. Bains states the following:

> Chip MC0 responds to a particular command by performing one operation and chip MC1 responds to the same command by performing another operation. For example, chip MC0 may respond to a command, for example, called command A, by performing a write operation while chip MC1 responds to command A by

> turning on an ODT. Stated another way, chip MC0 may **interpret** command A as being a write command while chip MC1 **interprets** command A as being a tum on ODT command. In some embodiments, there is a second command, for example, called command B, for which chip MC0 responds by turning on an ODT while MC1 responds by performing a write operation. (Ex. 1005, 2:47-58, emphasis added.)

65. In Fig. 3 (reproduced below) of Bains, an exemplary register is shown that represents register (30 or 40) in Fig. 10 above. The register has bits that indicate what operation should occur to a given command. For example, the "write or ODT on" bit may be in a state such that a command is *interpreted* as a write, or the "write or ODT on" bit may be in a different state such that the same command is *interpreted* as an ODT on.

66. For example, based on the register (30 or 40) settings remaining in a fixed state, command A will cause MC0 to perform a write and MC1 to turn on ODT. Command B will cause MC0 to turn on ODT and MC1 to perform a write. Fig. 3 is shown below:

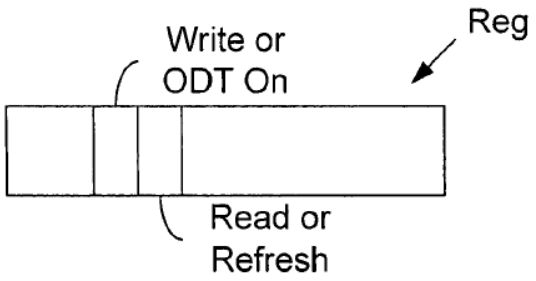

FIG. 3

67. Bains discloses this operational feature with regards to Fig. 3 by stating the following:

> FIG. 3 illustrates a register with one or more bits for "write or ODT on" and one or more bits for "read or refresh." The register of FIG. 3 may represent register 30 or 40, although registers 30 and 40 are not required to include bits for both "write or ODT on" and "read or refresh." In FIG. 3, different bits are shown to control "write or ODT on" and "read or refresh." Alternatively, the same bit(s) can control both. For example, if the operation type signal has a first value, then the chip may respond to command A as a write request and command C as a read request, and if the operation type signal as a second value, the chip responds to command B as an ODT on command and command D as a refresh request. Even other information can be encoded in the operation type signal.
>
> In examples 1 and 2, the first state could be a logical high voltage and the second state a logical low voltage, but that is not required. For example, the first state could be a

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> logical low voltage and the second state could be a logical high voltage. In other embodiments, more than two states (voltages) can be included in a register bit(s). (Ex. 1005, 4:7-25.)

68. To support the various operations based on a memory's register (30 or 40), Bains discloses a single timing diagram in Fig. 7. Clearly, as shown in the block diagrams discussed above (e.g., Fig. 10), memory chip MC0 receives chip select CS0# and memory chip MC1 receives chip select CS1#. Both memory chips (MC0 and MC1) receive the same command signals shown in Fig. 7 as CMD. At clock cycle 1, command A is sent to both memory chips (MC0 and MC1), which causes memory chip (MC0) to allow a write operation and memory chip (MC1) to turn on its ODT. At clock cycle 6, command B is sent to both memory chips (MC0 and MC1), which causes memory chip (MC0) to turn on its ODT and memory chip (MC1) to allow a write operation.

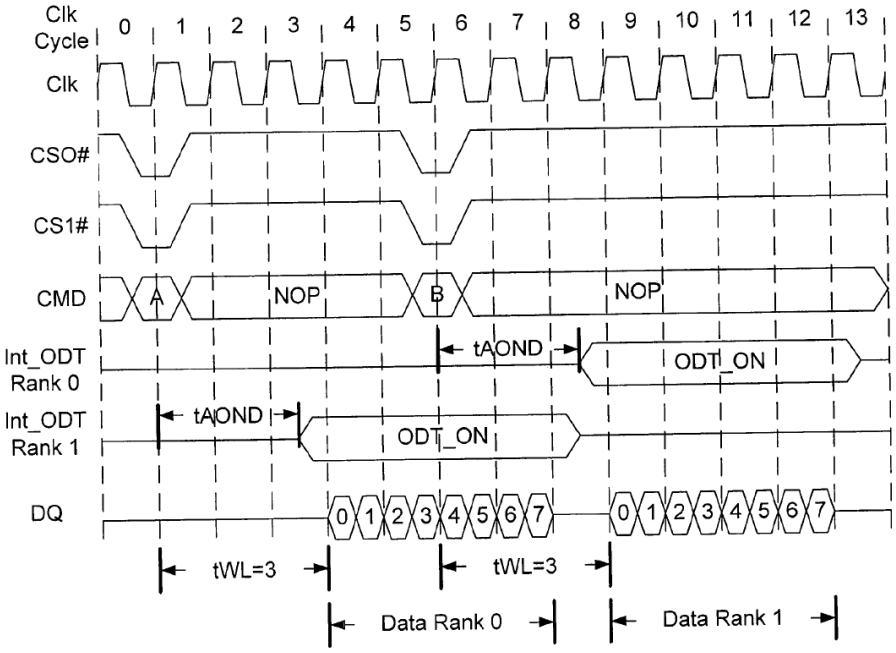

FIG. 7

69. Furthermore, Bains discloses in Fig. 4 that the ODT resistor value in the memory chip (MC0 and/or MC1) may be programmable. Fig. 4 is shown below:

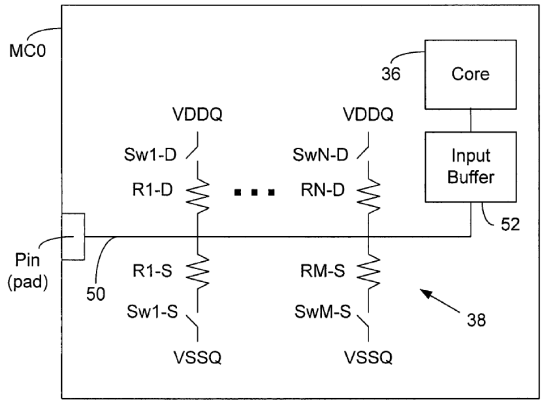

FIG. 4

70. Furthermore, Bains discloses with regards to Fig. 4 that different commands may cause a different value for the ODT resistance to be applied, as disclosed in the following:

> There are various ways in which an ODT may be constructed and this invention is not limited to any particular way. FIG. 4 illustrates an implementation of ODT 38 in chip MC0, but the invention is not limited to these details. Indeed, various other types of ODT may be used. Further, some embodiments do not include any ODT. Referring to FIG. 4, resistive structures R1-D . . . RN-D are between a data node 50 and switches Sw1-D . . . SwN-D, respectively, which in turn are coupled to a supply voltage node VDDQ. Resistive structures R1-S . . . RM-S are between data node 50 and switches Sw1-S . . . SwM-S, respectively, which in turn are coupled to a ground voltage node VSSQ. The numbers "N" and "M" may be the same or different and may have different values in different implementations. Control circuitry 32 controls the switches and hence whether ODT 38 is "on." The number of switches closed may determine the amount of resistance in the termination. *For example, a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance.* In FIG. 4, data node 50 is between a pin (pad) and an input buffer 52. Some chips do not include traditional pins, but may include pads. (Ex. 1005, 4:25-46, emphasis added.)

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71. Clearly, throughout all the exemplary embodiments in Bains, a command is used to determine whether an ODT resistance value is applied or not. This approach is in keeping with the issues stated in the Background section of Bains. To that point, Bains states, "By using commands to control ODTs, it does not matter whether a 1N or 2N timing is used. As noted, a 2N timing involves one extra clock cycle to sample a signal." (Ex. 1005, 6:38-40.)

72. As explained above with regards to Fig. 3, a bit in the register (30 or 40) is compared to the bits in the CMD to determine the operation of the memory chip (MC0 or MC1). A specific bit for ODT is not needed in the CMD as a "write or ODT on" option is provided in the register in Fig. 3, which determines how commands A and B are handled internally by the memory chips.

73. An ODT causes a termination resistance to be applied by a memory chip. Bains has arranged his command signals such that in response to a command, the memory chip either performs a write operation or applies a termination resistance. (Ex. 1005, 4:7-11; Fig. 3 (showing the same bits for write or ODT on.) Consequently, Bains provides a configuration that avoids an instruction causing duplicative write operations on MC0 and MC1.

74. However, Bains uses expansive language to allow ODT to be an input for the CMD or not. Bains states the following to expand how ODT, and the

application of a terminating resistance, may be commanded by the memory controller to a memory chip:

> By using a command to control the ODTs, it is not necessary to have a pin (pad) to control the ODTs, although there may be a pin to control the ODTs in some embodiments. In some embodiments, the ODTs are controlled only by commands, not pins. This results in reduction of pins compared to a system with pins used to control the ODTs. In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times. (Ex. 1005, 6:30-37.)

75. Beyond the disclosure at Ex. 1005, 6:30-37 (immediately above), Bains is silent as to how the ODT is applied to the exemplary embodiments, both functionally in a block diagram and as a timing waveform.

C. Limitations of the Bains' Disclosure

76. In Bains, the block diagrams in Figs. 2 and 10, the timing diagram in Fig. 7, and the specification at Ex. 1005, 2:40-46, clearly disclose that the connections between a memory controller 12 and memory chips (MC0 and MC1) are based on chip select CS, command CMD, data DQ, and address. Bains states, "Chip select signals are sometimes referred to as device select signals." (Ex. 1005, 3:15-16.) Furthermore, Bains' "FIG. 5 illustrates each chip in a rank being selected

by the same chip select signal (CS0 for the chips of rank 0 and CS1 for the chips of rank 1). The chip select signal could be provided on its own multi-drop bus as illustrated in FIG. 5 or through other ways such as a multiplexed or packetized signal." (Ex. 1005, 4:56-61.) Also, Bains discloses "[c]hip select signals CS0, CS1, CS2, and CS3 are used to select the chips in the corresponding ranks. Accordingly, chip select signals CS0 is used for all the chips of the first rank (rank 0), CS1 is used for all the chips of the second rank (rank 1) and so forth. The chip select signals in FIG. 6 could include a "#" symbol." (Ex. 1005, 5:1-6.)

77. As Bains discloses, the chip selects are solely responsible to allow an operation to occur on a memory chip, and are organized to communicate with a specific rank. Even if the chip select (CS) signals are "multiplexed or packetized," the chip select signals are separate from the command CMD bus. Bains' architecture requires the chip select signals to be separate from the command CMD bus because the chip selects determine if the command CMD bus should be evaluated or ignored.

78. Also, as shown at least in Fig. 3, Bains discloses that the ODT control is based on a command (CMD) signal that selects between a write and application of ODT. Bains expands his disclosure to allow "a pin to control the ODTs" (Ex. 1005, 6:30-31), but is silent as to how an ODT pin is connected to enable/disable a termination resistance.

79. Further, Bains discloses "a command A1 may cause one level of resistance in the ODT and a command A2 may cause another level of resistance." (Ex. 1005, 4:42-44.) However, Bains is silent as to any timing differences between the application of the two different resistances. Also, the two different resistances are the result of two different commands.

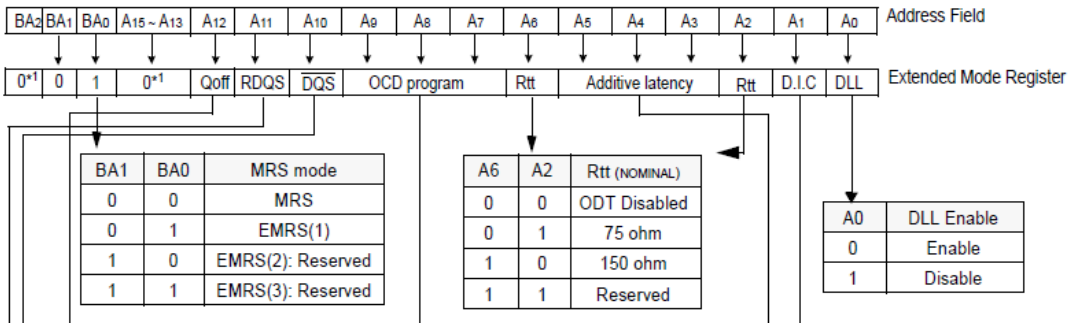
VII. JESD79-2A (EXHIBIT 1006)

80. The JESD79-2A is the JEDEC Standard that governs the required operation, features, and pinout for a DDR2 SDRAM memory device to be compliant. JESD79-2A was made available in January 2004.

A. Overview

81. The JESD79-2A discloses that an Extended Mode Register Set (EMRS) may be used to set a terminating resistance value as either 75ohms or 150ohms. Also, the terminating resistor(s) may be disabled/disconnected. Fig. 9 below shows the EMRS command to set the Rtt (nominal) value for ODT, where the EMRS command uses Bank Address (BA) and Address (A0-A15) inputs to form the command, as follows:

2.2.2.2 DDR2 SDRAM Extended Mode Register Set (cont'd)



82. The JESD79-2A discloses the terminating resistance value as selected by the EMRS register will be applied when the ODT pin is high. If the EMRS register has ODT Disabled, applying ODT high will not apply a terminating resistance value, as follows (Ex. 1006, pp. 14, 26):

ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS, RDQS, RDQS, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.

2.2.2.4 ODT (On Die Termination)

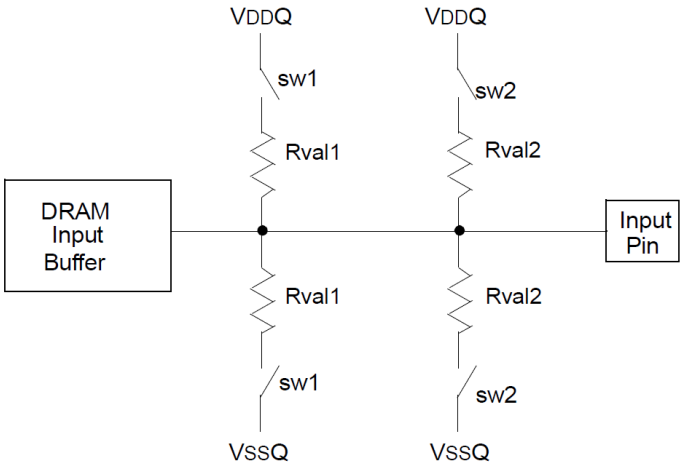
On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is supported for ACTIVE and STANDBY modes. ODT is turned off and not supported in SELF REFRESH mode.

83. The JESD79-2A discloses in Fig. 15 that either two resistors are selected to apply a 75ohm terminating resistance by using switch 1 (sw1), or a different set of two resistors are selected to apply a 150ohm terminating resistance by using switch 2 (sw2). The either switch 1 (sw1) or switch 2 (sw2) are enabled

by the ODT pin. Again, if the EMRS is set to disable ODT, having the ODT pin go high does not apply any terminating resistance. Fig. 15 is shown below (Ex. 1006, pg. 27):

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

84. The JESD79-2A discloses in Fig. 16 a timing diagram that shows when a terminating resistance value is applied relative to transitions on the ODT input, as follows (Ex. 1006, pg. 27):

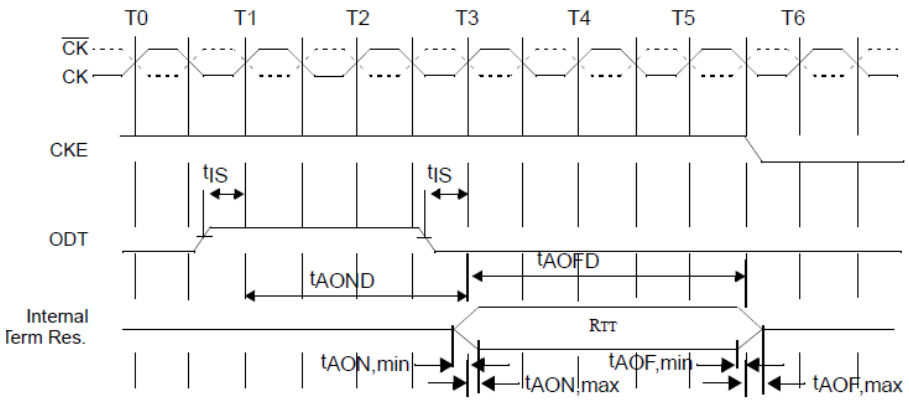


Figure 16 — ODT Timing for Active/Standby Mode

85. From the above timing diagram, clearly each DDR2 SDRAM requires a different ODT signal if one memory chip is to read or write while the other memory chip is to apply a terminating resistance.

86. Also, the terminating resistance value is applied dependent on the ODT signal, regardless of whether the memory chip has been commanded to perform a read or write operation. In other words, there is no interlock between the ODT signal and the commands for a read or write operation. The ODT signal may operate as needed to causes a terminating resistance value to be applied before, during, or after when data is transmitted or received by the memory chip.

87. Furthermore, JESD79-2A is silent as to any particular internal connectivity. JESD79-2A covers functionality, but is silent as to implementation.

B. Limitations of the Disclosure

88. Again, JESD79-2A covers functionality, but is silent as to implementation. JESD79-2A discloses that a terminating resistance value is

applied dependent on the state of the ODT signal, but the ODT signal is not interlocked to apply a terminating resistance value during a particular time for a read or write operation. JESD79-2A discloses that a terminating resistance value is either applied or the terminating resistors are disconnected from a terminal, dependent on the state of the ODT signal.

89. Also, no one command can cause a change from a first resistance value to a second resistance value. A first EMRS command can cause a first terminating resistance value to be available, and the ODT signal can determine whether to apply the first terminating resistance value or not. A second EMRS command can cause a second terminating resistance value to be available, and the ODT signal can determine whether to apply the second terminating resistance value or not. However, no one command can cause a change from a first terminating resistance value to a second terminating resistance value.

VIII. OPINIONS

90. I have formed the following opinions based principally upon (1) my experience summarized above, and (2) my review of the materials cited above in "Section III. Materials Reviewed and Relied Upon," with regards to what a POSITA would understand at the time of filing of the '523 Patent on July 31, 2006.

A. Standard for a POSITA

91. My assessment of the claim terms addressed herein assumes that they are being interpreted by a POSITA. In that regard, I have been asked to provide my opinion as to the educational level and professional experience of such a POSITA.

92. Based on the relevant time frame, my review of the ’523 Patent and its file history, and my experience in the field of the art applicable to the patent, I believe that a POSITA would have (1) a bachelor’s degree in computer engineering, electrical engineering, or an equivalent field with at least two to three years of circuit design experience, or (2) a master’s degree in computer engineering, electrical engineering, or an equivalent field with at least one year of circuit design experience at the time of filing of the ’523 Patent

93. I note that I would have met or exceeded the qualifications of a POSITA. My opinions provided herein are from the perspective of such a person.

94. From the vantage point of such a POSITA, at the time of filing of the ’523 Patent, original claims 1, 2, 5, 6, 9, and 10 of the ’523 Patent would neither have been obvious under Bains (Ground 1) nor Bains in view of JESD79-2A (Ground 2).

95. A detailed explanation of the reasoning that led to these opinions is provided below.

B. Claim Constructions

1. Port

96. The claims require "control command port" and "a termination port." In the '523 Patent, Figs. 1-2, element 11 is labeled as an "external control command ports" and element 13 is labeled "external termination port." In the '523 Patent, every instance of element 11 is described as an "external control command ports" and every instance of element 13 is described as an "external termination port." For example, the '523 Patent specification describes element 11 by stating, "Via one or more external control command ports 11, the command decoder 10 receives control command signals CMD for activating, addressing and/or driving the memory chip l." (Ex. 1001, 3:37-40.) For example, the '523 Patent specification describes element 13 by stating, "Via an external termination port 13, the control unit 8 receives a termination enable signal TermEn that indicates whether or not a termination is to be provided at the external terminal 4." (Ex. 1001, 3:25-28.)

97. Technical dictionaries from before and after the date of filing for the '523 patent demonstrate that the term port has had a longstanding meaning in memory systems. True and correct copies of the relevant portions of such dictionaries are attached to this Declaration as Appendix C. Such dictionaries provide the following definitions:

port 1. (I/O port) A connection point with associated control circuitry that allows I/O devices to be connected to the internal bus of a microprocessor.

Oxford Dictionary of Computer Science, p. 420.

Port 1. Noun. The physical interface between a device and a circuit. … .

Newton's Telecom Dictionary, 19th Edition, p. 624.

port 2. a connection where a computer can be connected to an external device … .

Barron's Dictionary of Computer and Internet Terms, p. 380.

98. Accordingly, a "port" is afforded its plain and ordinary meaning and is generally understood as "an interface allowing for external connection."

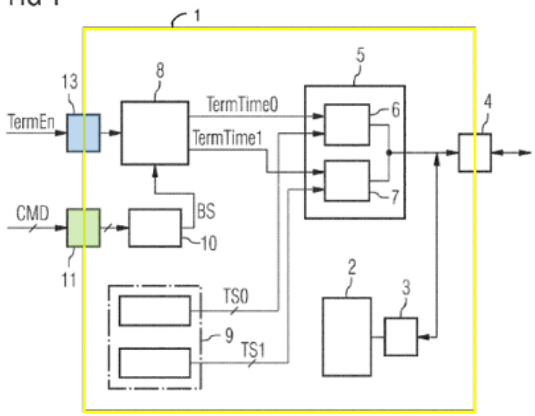
C. Claims 1, 2, 5, 6, 9, and 10 are Not Invalid under Ground 1

1. Claim Elements 1.3, 1.5, 5.5, & 5.8: "a control command port" and "a termination port" are <u>not</u> disclosed in Bains

99. Claims 1, 2, 5, and 6 require that the memory chip comprise both a "control command port" and a "termination port." (Ex. 1001, 8:55; 8:60; 9:28; 9:37.)

100. This is consistent with the embodiments disclosed in the '523 Patent. For example, the '523 Patent Figs. 1 and 2 (annotations added) expressly identify the control command and termination ports as external interfaces to the memory chip:

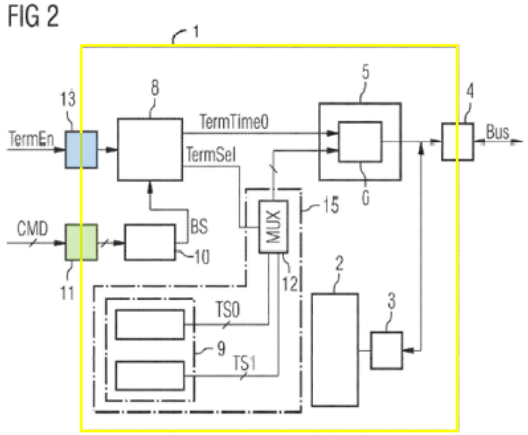
FIG 1



LEGEND:

1 - MEMORY CHIP
2 - MEMORY CELL ARRAY
3 - LOGIC CIRCUIT
4 - EXTERNAL TERMINAL
5 - TERMINATION CIRCUIT
6 - FIRST SETTABLE TERMINATING RESISTOR
7 - SECOND SETTABLE TERMINATING RESISTOR
8 - CONTROL UNIT
9 - CONFIGURATION UNIT
10 - COMMAND DECODER
11 - EXTERNAL CONTROL COMMAND PORTS
13 - EXTERNAL TERMINATION PORT

FIG 2



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10 - COMMAND DECODER
11 - EXTERNAL CONTROL COMMAND PORTS
12 - MULTIPLEXER
13 - EXTERNAL TERMINATION PORT
15 - SETTING UNIT

101. The ’523 Patent explains that these ports are separate from the control unit. (Ex. 1001, 3:25-26 (“Via an external termination port 13, the control unit 8 receives a termination enable signal TermEn.”); 3:37-40 (“Via one or more external control command ports 11, the command decoder 10 receives control command signals CMD for activating, addressing and/or driving the memory chip 1.”).)

102. Nevertheless, Petitioner incorrectly argues that *internal* components of the alleged memory chip disclosed by Bains constitute the control command and completely fails to identify a termination port in their annotations. *See, e.g.,* Petition, pp. 25-27; 29-30. Petitioner’s annotations of Bains demonstrate that the alleged control command port is an internal component of memory chip MC0 (Petition, pg. 26):

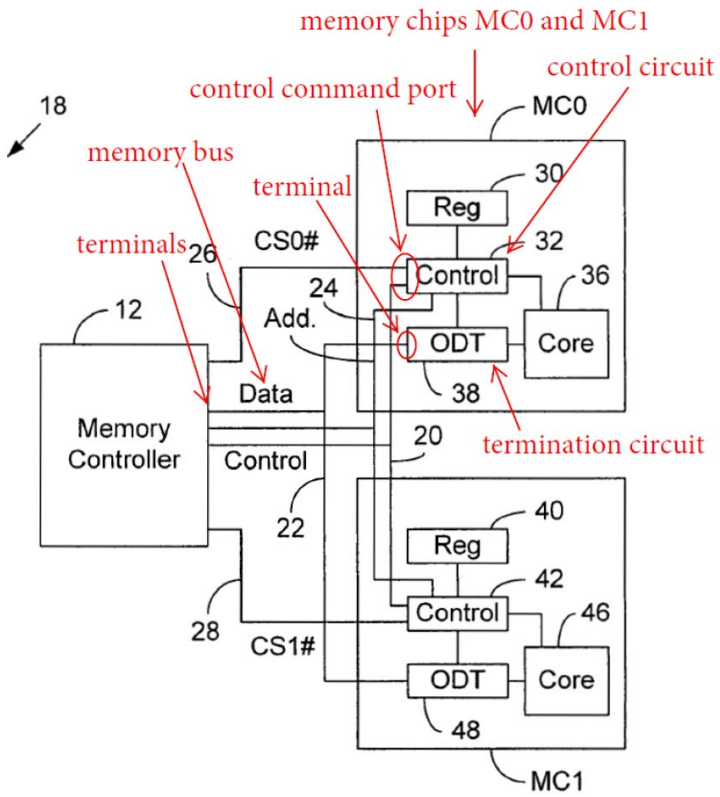

FIG. 2

103. As immediately noticed, Petitioner has labeled the claimed "control command port" as an internal node to memory chip 0 (MC0). As understood above, a "port" is "an interface allowing for external connection." The "control command port" indicated by the Petitioner encircles not only the internal signals for a control bus 20, but also the internal signal for a chip select signal (CS0#). Petitioner fails to identify "an interface allowing for external connection" for the control circuit 32. Also, glaringly missing in Petitioner's annotations is any identification of a "terminal port," which is not the separate claim element as "a terminal" identified in Fig. 2 above.

104. Petitioner contends that MC0 constitutes the claimed memory chip. (Petition, pg. 22.) Petitioner further contends that "a POSITA would understand that control circuit 32 includes a port connected to the control bus 20 and chip select bus 26." (Petition, pg. 26.) Petitioner (Petition, pg. 26.) also alleges that:

> To the extent Patent Owner were to argue such a control command port is not expressly disclosed, it certainly would have been obvious to a POSITA that the control circuit 32 includes such a port because the control circuit is disclosed as receiving commands from controller 12, which must enter through a port.

But these arguments only allege that the control command port is a component of the control circuit, they do not allege that the control command port is "an interface allowing for external connection" of the memory chip as reasonably understood by a POSITA. It is clear from claims 1 and 2 and the '523 Patent that the control circuit and the control command port are separate components (Ex. 1001, Figs. 1-2, annotated):

FIG 1

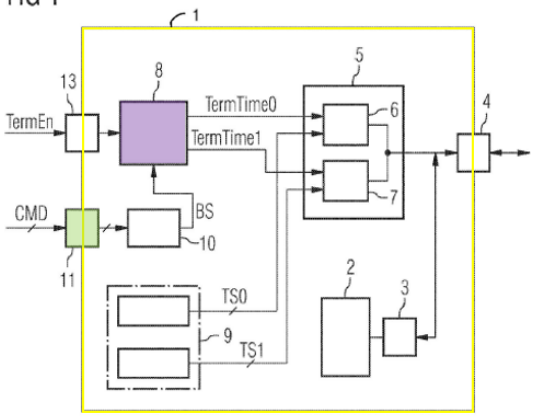

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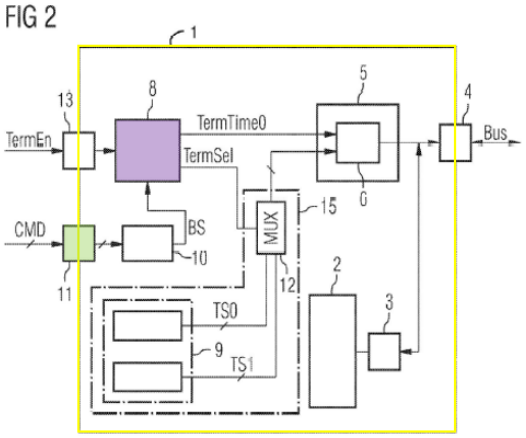
FIG 2



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11 - EXTERNAL CONTROL COMMAND PORTS
12 - MULTIPLEXER
13 - EXTERNAL TERMINATION PORT
15 - SETTING UNIT

105. Bains is silent as to a control command port. And Petitioner does not allege that it would have been obvious to modify MC0 to include a control command port. Simply put, Petitioner has not shown that Bains discloses the claimed "control command port."

106. As discussed above, Bains does not disclose separate termination and command control ports for memory chip MC0. Consequently, obviousness based on Bains necessarily requires modification of the disclosed system. But Petitioner does not allege such a modification would be obvious. Similarly, Petitioner does not offer any motivation for a POSITA to make such a modification. And given the shared bus configuration set forth in Bains, a POSITA would not have been

motivated to modify the architecture to include external termination and command control ports.

107. As detailed above, Bains does not disclose either "a control command port" or "a termination port." As such, Bains does not disclose limitations [1.3], [1.5], [5.5], or [5.8] of the Challenged Claims. Accordingly, Petitioner has not shown, and cannot show, challenged claims 1, 2, 5, and 6 are unpatentable over Bains and Ground 1 fails with respect to these claims.

2. Claim Elements 1.3, 5.5, & 9.1, "a control command port for receiving a control command signal *for affecting accessibility of the memory chip*" are <u>not</u> disclosed in Bains

108. Claim elements 1.3, 5.5, and 9.1 require "receiving a control command signal *for affecting accessibility of the memory chip*". The term control command signal encompasses a variety of signals, but not all of these signals affect accessibility of the memory chip.

109. A POSITA would understand that the claimed "control command signal" must be (1) received at "a control command port," and (2) be a signal that affects accessibility.

110. Affecting accessibility of a memory chip requires more than simply accessing the memory chip.

111. None of Bains' commands are "for affecting accessibility of the memory chip" as claimed. Bains' commands, depending on the embodiment, are provided through control bus 20, address bus 24, and the data bus 22, as follows:

> The commands referred to in this disclosure may be provided from memory controller 12 to chips MC0 and MC1 through various ways. In some embodiments, *the commands described herein are provided only through control bus 20*. In other embodiments, *the commands are provided through a combination of control bus 20 and address bus 24*. In still other embodiments, *the data bus is also used to communicate commands*. Control circuitry 32 in chip MC0 and control circuitry 42 receive the commands from controller 12, although the signal including the commands may be modified or otherwise changed between the controller 12 and controller circuitry 32 and 42. (Ex. 1005, 3:17-28, emphasis added.)

112. Bains discloses that different commands (commands A, B, C, D) may be used to read, write, turn on ODT, or refresh a memory chip, as follows:

> As an example (called example 1), an operation type signal in register 30 has a first value because, for example, a particular bit in register 30 has a first voltage state. The same operation type signal in register 40 has a second value because the corresponding bit in register 40 has a second voltage state. In example 1, there are commands called commands A and B. Chip MC0 responds to

command A as a write command, meaning that control circuitry 32 causes certain data bits on data bus 22 to be stored in core 36 of chip MC0. Chip MC1 responds to command A by turning on ODT 48. More particularly control circuitry 42 turns on ODT 48. Conversely, chip MC0 responds to command B by turning on ODT 38 and chip MC1 responds to command B as a write command. More particularly, in response to command B, control circuitry 32 turns on ODT 38 and control circuitry 42 causes data on bus 22 to be stored in core 46. In some embodiments, if the values of the operation type signals in registers 30 and 40 were reversed, then chip MC0 would respond to command A by turning on ODT 38 and to command B by performing a write operation; and chip MC1 would respond to command A by performing a write operation and to command B by performing an ODT operation.

As another example (called example 2), there are commands called commands C and D. An operation type signal in registers 30 and 40 could be set with particular values such that chip MC0 responds to command C as a read command and to a command D as a refresh command, whilst chip MC1 responds to command C as a refresh command and to command D as a read command. The values of the operation type signal can be set by the states (voltages) of one or more bits in registers 30 and 40. There

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> can be only one or more than one operation type signal in a register. In some embodiments, chips MC0 and MC1 have the features of both examples 1 and 2, whilst in other embodiments, chips MC0 and MC1 have the features of example 1, but not example 2, and in still other embodiments, chips MC0 and MC1 have the features of example 2, but not example 1. (Ex. 1005, 3:37-4:6.)

113. The ’523 Patent identifies several examples of the claimed “control command signal,” including the write enable signal. (Ex. 1001, 3:45-46 (“the write enable signal for enabling write access to the memory chip.”)).

114. A write enable signal is distinct from the alleged write command in Bains. The write enable signal is a flag that must be true in order for a write to occur. The write enable signal is not a command to write data, but rather a condition that must be present for a write to occur. In other words, the write enable signal affects access to the memory chip so that a write operation can occur.

115. Conversely, Bains’ alleged write command is an instruction that may be interpreted by each memory chip as a request to write data to the memory chip. While command A or B *may* cause access the memory chip, it does not affect such access. In other words, the signal(s) received in Bains that form command A or B do not affect accessibility because those signals do not determine a specific action within the memory chip. Only after evaluation with respect to the internal register (Bains, Fig. 3) is the action determined.

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116. Bains clearly explains that command A and B cause a memory device to either write or turn ODT on. Which action is performed cannot be determined by knowing the command. Rather, only the memory device, after evaluation with its internal register, can determine what action will occur.

117. Despite this, Petitioner incorrectly argues that commands A, B, C, and D in Bains "are the same type of commands as the exemplary control command signals disclosed in the '523 Patent." (Petition, pg. 27.) As an initial matter, commands A, B, C, and D in Bains are **not** read, write, or refresh commands, but rather commands that are resolved to a function dependent on the memory chip's internal register programming. *See, e.g.,* Ex. 1005, 2:49-55 ("For example, chip MC0 may respond to a command, for example, called command A, by performing a write operation while chip MC1 responds to command A by turning on an ODT. Stated another way, chip MC0 may interpret command A as being a write command while chip MC1 interprets command A as being a turn on ODT command"); *see also id.* at 2:55-67; 3:37-4:25. A POSITA would understand that if MC0 and MC1 respectively "interpret" command A as a write and ODT instruction, then command A is not a write or ODT instruction, but rather a command that is mapped within each respective memory chip.

118. The read, write, and refresh commands discussed in Bains are merely requests to perform an operation on a memory device, and not commands affecting

accessibility. Such commands are distinct from signals like chip select signal CS, a write enable signal WE, a row activation signal RAS, or a column activation signal CAS that are necessary for access to occur.

119. For at least the reasons provided above, Bains fails to show or suggest at least claim elements 1.3, 5.5, or 9.1.

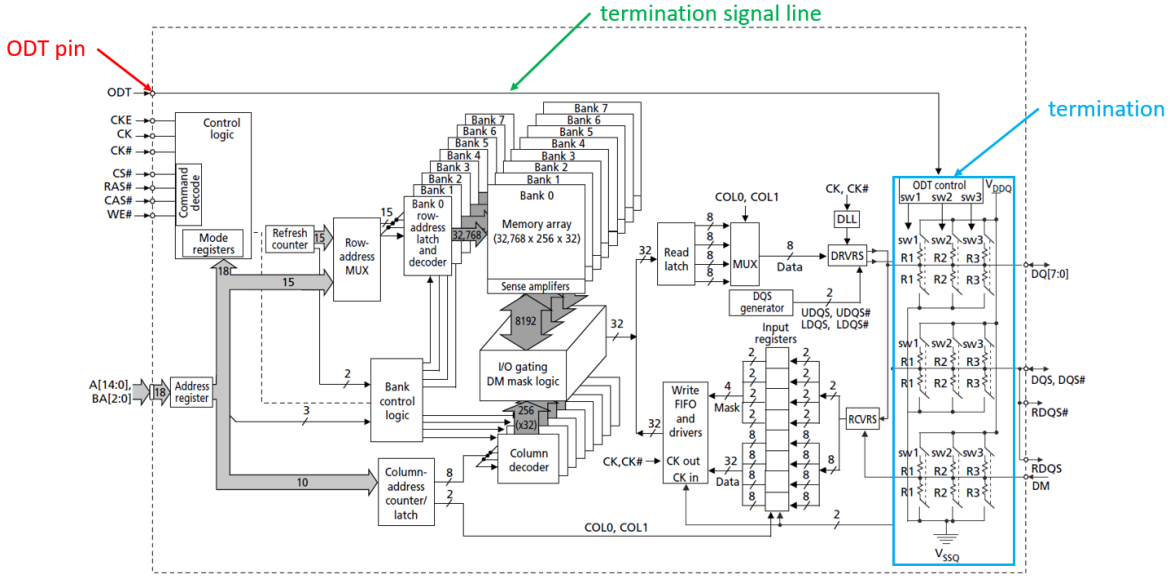
3. Claim Elements 1.5 & 5.8, "wherein the control circuit is configured to selectively terminate the terminal … *in response to the termination signal*" are <u>not</u> disclosed in Bains

120. In the Petition, the Petitioner claims Bains discloses "a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal" as claimed.

121. First, in the Petition (Petition, pg. 29), Petitioner argues that the '523 Patent, and the JEDEC standard for DDR2 DRAM chips in the Background of Bains, disclose "a termination port" as claimed in the form of an ODT pin. While ODT pins are described in the JEDEC standard for DDR2 DRAM chips, Bains does not use an ODT pin. In fact, Bains discloses a write value in a command, so that the opposite state for a write is to turn on ODT. (The JEDEC standard for DDR2 DRAM uses a single WE to indicate write or read, and has a separate ODT pin.)

122. The benefit of an ODT pin is that it allows the termination signal to be delivered directly to the termination. As contemporaneous functional block diagrams demonstrate, a POSITA would have understood that an ODT pin would deliver the termination signal directly to the termination (Appendix B, Fig. 4):

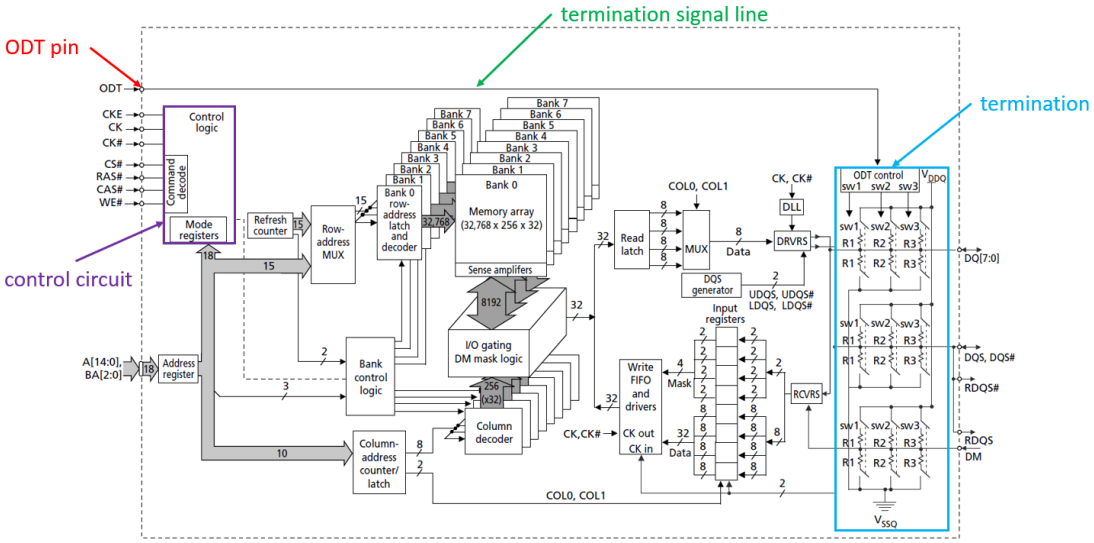
Figure 4: Functional Block Diagram – 256 Meg x 8



123. The above block diagram is an annotated figure from a true and correct copy of a 2006 Micron data sheet for Micron DDR2 SDRAM products. The data sheet is available at https://media-www.micron.com/-/media/client/global/documents/products/data-sheet/dram/ddr2/2gb_ddr2.pdf, also attached as Appendix B. This block diagram illustrates how a POSITA, at the time of the invention for the '523 patent, would understand an ODT pin would be implemented.

124. While an ODT pin may constitute a termination port, claims 1, 2, 5, and 6 require more. Specifically, claims 1, 2, 5, and 6 require that the termination port receive a termination signal and that *the control circuit* be configured to selectively terminate "in response to the termination signal." (Ex. 1001, 8:62-63; 9:40-41.) As detailed above, an ODT pin in systems around the time of the invention typically bypassed the control circuit (Appendix B, Fig. 4):

Figure 4: Functional Block Diagram – 256 Meg x 8



125. In Bains, ODT control is not a pin, but a state in a command. Bains consistently uses this approach, as described in Fig. 3 shown below:

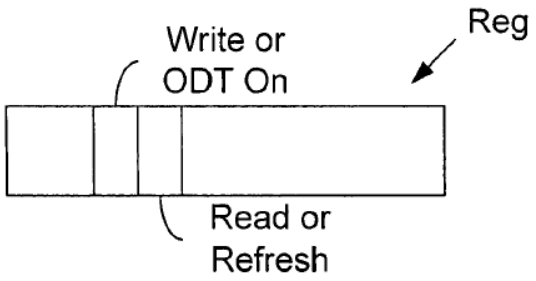


FIG. 3

126. Bains purposefully does not use an ODT pin because the stated necessity of the invention is to move away from monitoring or snooping the command bus for a write transaction. (Ex. 1005, 1:48-49.) "Snooping may work well for 1N timings, but not for 2N timings (with an additional clock cycle before sampling) because snooping may cause additional clock cycles in turnaround cycles and in leadoff write cycles." (Ex. 1005, 1:55-58.) Because the control circuit never receives the termination signal in such systems, it cannot act *in response* to the termination signal.

127. Second, Petitioner relies on the Baker Declaration to conclude "a POSITA would have understood Bains' disclosure at 6:30-37 to include the use of an ODT pin for controlling whether ODT is 'on' in the system taught by Bains, in addition to the use of commands, such as the disclosed A1 and A2 commands discussed above, to indicate the amount of resistance to be applied. EX1003 at ¶¶ 84-86." (Petition, pp. 29-30.) Bains states the following:

> By using a command to control the ODTs, it is not necessary to have a pin (pad) to control the ODTs, although there may be a pin to control the ODTs in some embodiments. In some embodiments, the ODTs are controlled only by commands, not pins. This results in reduction of pins compared to a system with pins used to control the ODTs. In other embodiments, the ODTs are controlled only by pins. In still other embodiments, the ODTs are controlled by commands sometimes and by pins at other times. (Ex. 1005, 6:30-37.)

128. Petitioner completely misses the requirements of the claim element. Claim element 1.5 requires, "a termination port to receive a termination signal, wherein **the control circuit is configured** to selectively terminate the terminal with the set resistance value **in response to the termination signal**". The question is **not** whether a POSITA would have recognized that an ODT pin might be used, or that an ODT pin would connect or disconnect the terminating resistance value. The requirement is "the control circuit is configured … in response to the termination signal." Petitioner completely fails to address this claim requirement.

129. Bains' approach through his entire specification is to have the ODT controlled by a bit within a command signal (which has no dedicated ODT pin). Then, at the end of his specification, Bains throws up a myriad of possible ways ODT might be controlled. In doing so, Bains (1) goes against his stated goal of

preventing bus snooping, and (2) fails to fully explain how an ODT pin would work.

130. It is not obvious that the control circuit, which is connected to the termination circuit and configured to set the resistance value as a function of the received control command signal, should be arranged to be responsive to an ODT pin. Bains only discloses an ODT signal to connect or disconnect the terminating resistors, and another circuit to set the terminating resistance value. As soon as Bains separates the ODT pin from a command (which has no dedicated ODT pin), the ODT pin has one of two functions: connect the terminating resistance or not. Case-in-point, in an actual implementation in Appendix B (e.g., Fig. 4), the ODT pin goes directly to the termination circuit without the claimed "control circuit," which fails the claim requirements.

131. The '523 Patent specifically claims a particular connectivity with specific circuits responsive to other specific circuits. Bains only has two circuits: one to set the resistance and one to selectively connect that resistance. Bains is completely silent as to how these circuits are arranged. Petitioner fails to explain how Bains shows or suggests the claimed connectivity and claimed response.

132. For at least the reasons provided above, Bains fails to show or suggest at least claim element 1.5.

4. Claim Elements 2.1 & 6.1, "wherein the control circuit is configured such that, as *a function of* ***the*** *received control command signal*, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time" are **not** disclosed in Bains

133. In the Petition, the Petitioner claims Bains discloses "wherein the control circuit is configured such that, *as a function of* **the** *received control command signal*, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time" as claimed.

134. Claim 2 of the '523 Patent requires "the resistance value is set to a first resistance value after a first predetermined switchover time" and the resistance value "is set to a second resistance value after a second predetermined switchover time" "as a function of **the** received control command signal." In other words, a **single** "received control command signal" causes two different resistances to be applied at two different times.

135. Petitioner first claims that "the first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination

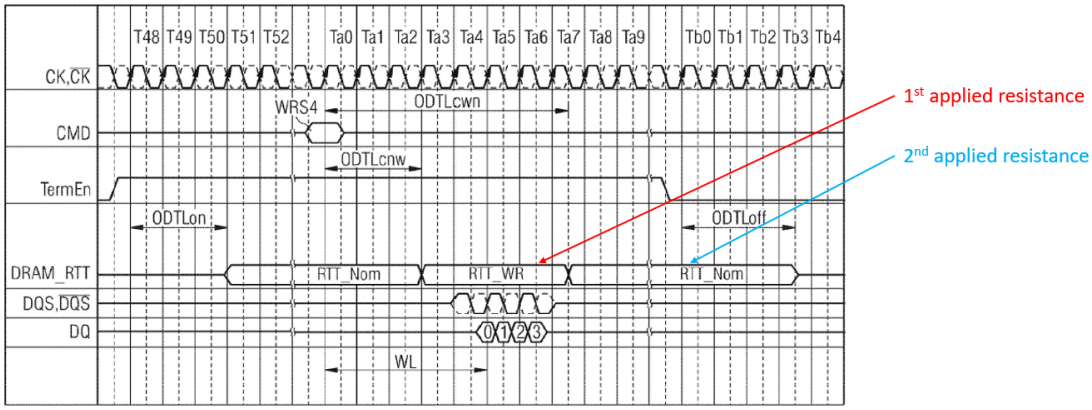
circuit is disabled." (Petition, pg. 34.) There is no dispute that Bains discloses setting a first resistance value in response to command A. In response to command A, Bains sets a resistance in the ODT for MC1 by closing some number of switches Sw1-D … SwN-D and Sw1-S … SwM-S. (Ex. 1005, 4:29-42.) Bains also discloses that the ODT in MC1 is "turned off automatically (without a separate command) after a fixed delay based on a burst length of 8." (Ex. 1005, 5:40-42.) Petitioner incorrectly contends that turning off the ODT constitutes setting a resistance value.

136. Bains explains that "[t]he number of switches closed may determine the amount of resistance in the termination." (Ex. 1005, 4:40-42.) In other words, the ODT may be set to different resistance values based on the number of switches that are closed. But a POSITA would not understand turning the ODT off to constitute setting a resistance value. Indeed, as discussed above, issues arising from switching ODT on/off as a function of a termination signal are the very issues the '523 patent seeks to address. (Ex. 1001, 1:37-39, 1:44-49.) Absent additional action, a POSITA would understand disabling the termination to be the opposite of setting a resistance value for the termination. To hold otherwise, would disregard both the claim language and purpose of the disclosed and claimed invention.

137. Petitioner's reliance on claims 4 and 8 is misplaced. The '523 Patent discloses embodiments where termination is set to a nominal value. Then, when a

control command causes "switching on of the termination of the terminal", a first resistance value is substantially simultaneously applied "with the switching on of the termination of the terminal". Then, when "the ending of the termination of the terminal" occurs, the nominal (i.e., second) resistance value is substantially simultaneously applied "with the ending of the termination of the terminal." Fig. 5 of the '523 Patent provides an illustration of this (Ex. 1001, 6:32-42, Fig. 5, annotated):

FIG 5



Further, the '523 patent discusses setting such a resistance value substantially simultaneous with the ending of the termination. *Id.* at 7:60-65. Any suggestion that the '523 patent considers turning the ODT off to constitute setting a resistance value is simply incorrect.

138. Petitioner alternatively claims that "the first and second resistance values recited in claim 2 may be met by … (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of command

A2." (Petition, pg. 34.) Because A1 and A2 are two distinct commands, they do not disclose setting the resistance to two separate values as a function of a single received control command signal, as is required by the claims. Rather Bains discloses that in response to command A1, the resistance is set to a first value and that in response to a separate command A2, the resistance is set to a second value. (Ex. 1005, 4:42-44.)

139. In fact, claim 1 distinguishes between "the set resistance value" and "not terminate the terminal." The Applicants clearly understood how to claim disconnecting a resistance. Furthermore, as shown below, the '523 Patent provides at least one embodiment showing changing from one set resistance to another set resistance based on a single control command signal. Also, as discussed in Section VIII.B.2 *supra*, the plain and ordinary meaning of the "resistance value is set" is generally understood as "a resistance having a plurality of selectable resistance values which requires at least one resistive element to be actively connected to provide a resistance." This understanding is far and away from disconnecting a resistance.

140. Petitioner has completely misunderstood the claim requirements. The commands A, A1, A2, and B are all different commands. As shown above with regards to Fig. 5, the '523 Patent teaches a single command that results in two different resistances applied at two different times. Petitioner (Petition, pg. 39),

using the Baker Declaration (Ex. 1003, ¶¶ 101-102), cites to Kyung (Ex. 1009, 8:42-9:32) as support that activating an A1 command followed by an A2 command in Bains would transition from a first terminating resistance value to a second terminating resistance value. This argument is moot as claim 2 clearly requires the two different terminating resistance values to occur as the result on a **single** "received control command signal."

141. Also, in the Petition, Petitioner attempts to convince the PTAB that a terminating resistance value that is disconnected from a terminal is a "set … resistance value." As shown above with regards to Fig. 5, the '523 Patent teaches a write resistance value (RTT_WR) and a nominal resistance value (RTT_Nom) are sequentially applied based on a single received control command. The '523 Patent never teaches that the absence (disconnection) of a terminal resistor is a "set … resistance value." A disconnected resistor (through a transistor) essentially floats the terminal, and will not have a set resistance. A transistor that is turned "off" has a resistance less than infinity (i.e., open circuit) and that varies according to manufacturing, manufacturing technology node, transistor design, etc.

142. The claims require "a termination circuit coupled to the terminal and configured to terminate the terminal according to a *settable resistance value*" and "*the resistance value is set* to a first resistance value after a first predetermined switchover time and *is set* to a second resistance value".

143. The ’523 Patent teaches the following:

> The external terminal 4 is connected to a termination circuit 5 that has a first settable terminating resistor 6 with a first resistance value, and a second settable terminating resistor 7 with a second resistance value. The termination circuit 5 is connected to a control unit 8 that makes available to the termination circuit 5 a first control signal TermTime0, and a second control signal TermTime1. Upon activation of the first control signal TermTime0, the first terminating resistor 6 is connected to the external terminal 4 such that the external terminal 4 is terminated with the first resistance value set accordingly in the first terminating resistor 6. Upon activation of the second control signal TermTime1, the second terminating resistor 7 is correspondingly connected to the first terminal such that the external terminal 4 is terminated with the second resistance value. Furthermore, given simultaneous activation of the two control signals TermTime0, TermTime1, it is also possible to generate a further resistance value for termination that results from the parallel connection of the first and second resistance values. (Ex. 1001, 2:49-67.)

144. Accordingly, the settable resistance value is based on resistor 6, resistor 7, or a combination of resistor 6 and resistor 7. Furthermore, the ’523 Patent teaches the following:

> The termination circuit can further have a number of terminating resistors in order to provide a number of various resistance values, the control circuit being fashioned in order to select at least one of the terminating resistors and apply it to the terminal. By providing the number of the terminating resistors in the memory chip, the corresponding terminating resistors can be selected relatively quickly such that there is no, or no substantial time loss in carrying out the operation in the memory system. (Ex. 1001, 7:16-24.)

145. Accordingly, the number of resistors used to create a settable resistance value may be based on "a number of terminating resistors in order to provide a number of various resistance values."

146. Also, Figs. 3-5 show when a resistance value is applied to a terminal as taught by the DRAM_RTT signal. The resistance can be set for nominal (Nom), write (WR), or disconnected, according to Figs. 3-5. Disconnecting a resistance from the terminal is not "terminat[ing] the terminal according to settable resistance value" or "the resistance value is set" as claimed because the terminal essentially floats. No **set** resistance is applied. A transistor that is turned "off" (i.e., open circuit) has a resistance less than infinity and varies according to manufacturing, manufacturing technology node, transistor design, etc. Again, disconnecting a resistance from the terminal by turning a transistor "off" is **not** coupling the

terminal to a "settable resistance value" or "the resistance value is set" because the resistance value varies widely.

147. In fact, claim 1 recognizes this fact by claiming either terminating "with the **set** resistance value" or "not terminate the terminal." Not terminating a terminal is not the same as using a set resistance value in claim 1.

148. The Petition (Petition, pg. 35 footnote) and the Baker Declaration (Ex. 1003, pg. 56 footnote) attempts to bridge this gap by citing Kwak (Ex. 1007, 6:11-52). Kwak states that deactivating the ODT "provides higher termination impedances." While accurate, Kwak does not, nor can he, state that the impedance has a set or settable resistance value as claimed.

149. Accordingly, both a "settable resistance value" and "resistance value is set to a first resistance value … and is set to a second resistance value" are afforded its plain and ordinary meaning and is generally understood as "a resistance having a plurality of selectable resistance values which requires at least one resistive element to be actively connected to provide a resistance."

150. Again, claim 1 recognizes this fact by claiming either terminating "with the **set** resistance value" or "not terminate the terminal." Not terminating a terminal is not the same as using a set resistance value in claim 1. The Applicants clearly understood how to claim disconnecting a resistance.

151. Furthermore, claim element 1.6 requires, "wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) **does not terminate the terminal** in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value." (Emphasis added.) Clearly, the Applicants understood the difference between terminating and not terminating a terminal. Claims 2 and 6 require setting a first and a second resistance value. Accordingly, claim 2 cannot stand for setting a first resistance value and not terminating a terminal.

152. For at least the reasons provided above, Bains fails to show or suggest at least claims 2 and 6.

D. Claims 1, 2, 5, 6, 9, and 10 are Not Invalid under Ground 2

153. In the Petition, the Petitioner argues "[a] POSITA would have been motivated to combine Bains with JESD79-2A and would have had a reasonable expectation of success in doing so, because (a) JESD79-2A was and remains a well-known memory standard published by the preeminent memory standards setting organization, (b) Bains specifically teaches that the system may use ODT pins to control the termination, and (c) Bains refers to JEDEC's DDR2 standards with respect to the use of ODT pins. EX1005 at 1:37-45, 6:31-37." (Petition, pg. 49)

154. While both Bains and the "JEDEC Solid State Technology Association … standards for DDR2" referenced in Bains' Background discuss On Die Termination (ODT), Bains specially calls out the failings of the JEDEC DDR2 Standard and addresses those deficiencies with his invention. Bains states the following in his Background:

> In GDDR3 (graphics DDR3) and also DDR3/DDR2 proposals, the command bus may be shared between two ranks. *The DRAM can monitor or snoop the command bus for a write transaction.* If it sees a write cycle and no CS# asserted then, it can turn its ODT on. The write command may target the other rank. (CS# are rank or device specific). The term "2N timing" refers to a situation in which it takes an extra clock cycle for sampling as compared to a 1N timing. The sampling may be of a signal, such as an address signal. *Snooping may work well for 1N timings, but not for 2N timings (with an additional clock cycle before sampling) because snooping may cause additional clock cycles in turnaround cycles and in leadoff write cycles.* (Ex. 1005, 1:46-58, emphasis added.)

155. Herein Bains' reference to the JEDEC DDR2 Standard will be referenced as JESD79-2A, which is a version of that standard.

156. The point is that while Bains and JESD79-2A have a common subject matter, a POSITA would **not** be skilled to modify Bains using JESD79-2A when

Bains specifically discloses an approach contrary to JESD79-2A. Further, a POSITA would **not** be skilled to pick-and-choose the exact feature set that results in the '523 Patent claims because **hindsight** should prevent such a combination. Otherwise, the patents issuing today should all be invalidated because they combine only known elements. On the contrary, patents are the result of an "inventive spark" that causes combinations of known elements to result in something new and useful.

1. Claim Elements 1.3, 5.5, & 9.1, "a control command port for receiving a control command signal *for affecting accessibility of the memory chip*" are not disclosed in Bains in view of JESD79-2A

157. Claim elements 1.3, 5.5, and 9.1 require "receiving a control command signal for affecting accessibility of the memory chip".

158. In the Petition, the Petitioner argues "As explained above for Ground 1, Bains teaches claim limitation [1.3]. *Supra* Section X.A.1.d; *see* EX1005 at 3:9-20, 3:24-28, 3:37-4:6, Fig. 2; EX1001 at 3:41-51; EX1003 at ¶ 135." (Petition, pg. 57.) In other words, Petitioner make no new arguments, and makes no combination of JESD79-2A with Bains to show or suggest obviousness.

159. The arguments above in Section VIII.C.2 will not be repeated here as to why Bains (without JESD79-2A) does not obviate claim element 1.3, but are incorporated in this section.

160. For at least the reasons provided above, Bains in view of JESD79-2A fails to show or suggest at least claim elements 1.3, 5.5, or 9.1.

2. Claim Elements 1.5 & 5.8, "wherein the control circuit is configured to selectively terminate the terminal … *in response to the termination signal*" are <u>not</u> disclosed in Bains in view of JESD79-2A

161. Claim element 1.5 requires, "a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal".

162. In the Petition, the Petitioner argues that if Bains is not sufficient to obviate claim element 1.5, Bains in view of JEDS79-2A would obviate claim element 1.5. (Petition, pp. 57-60.)

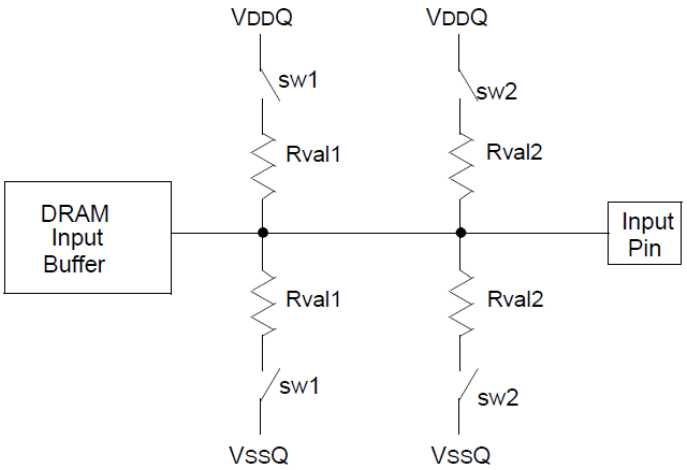
163. The arguments above in Section VIII.C.3 will not be repeated here as to why Bains does not obviate claim elements 1.5 and 5.8, but are incorporated in this section. As in Section VIII.C.3, Petitioner completely misses the requirements of the claim element. Claim elements 1.5 and 5.8 requires, "a termination port to receive a termination signal, wherein **<u>the control circuit is configured</u>** to

selectively terminate the terminal … with the set resistance value **in response to the termination signal**". The question is **not** whether a POSITA would have recognized that an ODT pin might be used, or that an ODT pin would connect or disconnect the terminating resistance value. The requirement is "the control circuit is configured … in response to the termination signal." Petitioner completely fails to address this claim requirement.

164. As in Section VIII.C.3, Bains is completely silent as to how the circuits are arranged with respect to the control circuit and the termination signal. Bains fails to show or suggest claim elements 1.5 and 5.8. JESD79-2A does not make up for what is missing in Bains.

165. JESD79-2A discloses Fig. 15 (Ex. 1006, pg. 27.), as follows:

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

166. In the notes above for Fig. 15, JESD79-2A specifically discloses that "Switch sw1 or sw2 is enabled by ODT pin" and "Selection between sw1 or sw2 is determined by 'Rtt (nominal)' in EMRS".

167. First, JESD79-2A is silent as to the circuitry and connections between the ODT pin and bits within the EMRS register.

168. Second, a POSITA would reasonably understand from the JESD79-2A Fig. 15 notes above that the ODT signal "selectively terminate the terminal"; however, the claims require "**the control circuit** is configured to selectively terminate the terminal". Also, the EMRS register (e.g., control circuit) sets the

resistance value, but JESD79-2A is silent as to *control circuit* acting "in response to the termination signal" (e.g., ODT signal) as required by the claims.

169. A POSITA would **not** understand that the EMRS register is responsive to the ODT signal. A POSITA would **not** understand that "the control circuit is configured to selectively terminate the terminal … with the set resistance value in response to the termination signal" as required by claim elements 1.5 and 5.8.

170. Third, as explained in Section VIII.C.3 above and incorporated here, the '523 Patent teaches an architecture that when Bains is mapped to the '523 Patent's architecture, does not show or suggest the claim elements 1.5 and 5.8. A POSITA might be motivated to create a similar solution, especially as instructed by JESD79-2A, which does not show or suggest the claim elements 1.5 and 5.8.

171. In summary, claim limitations 1.5 and 5.8 require that the control circuit be configured to selectively terminate the terminal in response to the termination signal. While JESD79-2A discloses an ODT pin for turning termination on and off, the termination signal is not delivered to the control circuit. Indeed, the statement in Figure 15 of JESD79-2A that "switch sw1 or sw2 is enabled by ODT pin," suggests that JESD79-2A would use the same configuration as the contemporaneous functional block diagrams discussed above.

172. For at least the reasons provided above, Bains in view of JESD79-2A fails to show or suggest at least claim elements 1.5 and 5.8.

3. Claim Elements 2.1 & 6.1, "wherein the control circuit is configured such that, as *a function of* <u>*the*</u> *received control command signal*, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time" are <u>not</u> disclosed in Bains in view of JESD79-2A

173. Claims 2 and 6 require, "wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time."

174. In the Petition, the Petitioner argues "As explained above for Ground 1, Bains teaches the additional limitations of claim 2. *Supra* Section X.A.2; *see* EX1001 at 5:63-65, 9:13-19, 10:15-22; EX1005 at 4:39-44, 5:23-42, Fig.7; EX1006 at Fig. 16; EX1007 at 6:11-52; EX1009 at 8:42-9:32, Figs. 10A-10C; EX1011 at ¶¶ 52-53. In particular, Bains teaches that the first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled, or (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of a command A2.

EX1003 at ¶ 142." (Petition, pg. 64.) In other words, Petitioner make no new arguments, and makes no combination of JESD79-2A with Bains to show or suggest obviousness.

175. JESD79-2A discloses that two possible resistance values can be programmed via the EMRS register, and the ODT signal can cause the terminating resistance value programmed in the EMRS register to be applied to a terminal or not.

176. As explained above in Section VIII.C.4, which is incorporated here, a disconnected resistor (through a transistor) essentially floats the terminal, and will not have a set resistance. A transistor that is turned "off" has a resistance less than infinity (i.e., open circuit) and varies according to manufacturing, manufacturing technology node, transistor design, etc. JESD79-2A only discloses that one resistance value can be applied "as a function of the received control command signal" as claimed. JESD79-2A does not make up for what is missing in Bains.

177. For at least the reasons provided above, Bains in view of JESD79-2A fails to show or suggest at least claim elements 2.1 and 6.1.

IX. CONCLUSIONS

178. As set forth above, it is my opinion that none of the art referenced by the Petitioner in the Petition and discussed by the Baker Declaration (Ex. 1003) invalidates any of the claims 1, 2, 5, 6, 9 and 10 of the '523 Patent.

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signed in Plano, Texas, on December 11, 2023

/s/ Timothy D. Dorney

Timothy D. Dorney, Ph.D.

Appendix A

Timothy D. Dorney, Ph.D.

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Citizenship: **U.S.A.**

EDUCATION

- **Rice University**
  Doctor of Philosophy in Electrical and Computer Engineering, January 2002
  Thesis Title: *Material Parameter Estimation and Imaging with Terahertz Time-Domain Spectroscopy*
  Thesis Advisor: Dr. Daniel Mittleman
- **Case Western Reserve University**
  Master of Science in Electrical Engineering and Applied Physics, May 1992
  Thesis Title: *Learned Adaptive Environment Control using Artificial Neural Networks and Fuzzy Logic*
  Thesis Advisor: Dr. Yoh-Han Pao
- **Texas A&M University**
  Bachelor of Science in Electrical Engineering (Cum Laude, University Honors), May 1990

REGISTRATIONS / MEMBERSHIPS

- United States Patent and Trademark Office, Patent Agent, Registration Number 51,623
- Institute of Electrical and Electronics Engineers, Member

DEPOSITIONS

- *Personalized Media Communications, LLC v. Google LLC*
  EDTX Case No. 2:19-cv-00090-JRG
- *Personalized Media Communications, LLC v. Netflix, Inc.*
  EDTX Case No. 2:19-cv-00091-JRG
  Firm: Susman Godfrey LLP
  Deposed as a Rule 30(b)(1) witness, March 2020
- *Apple Incorporated v. Personalized Media Communications, LLC*
  USPTO Inter Partes Review, IPR2016-00754 and IPR2016-00755
  Firm: Goodwin Proctor LLP
  Deposed as an Expert in support of claim amendments, February 2017
- *Personalized Media Communications, LLC v. Samsung Electronics America, Inc.*
  EDTX Case No. 2:15-cv-01754-JRG-RSP
  Firm: Susman Godfrey LLP
  Deposed as a Rule 30(b)(1) witness, November 2016

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EXPERT WITNESS

- *Xueshan Technologies, Inc. v. Renesas Electronics Corporation*
  EDTX Case No. 2:22-cv-00157-JRG-RSP
  Firm: Nelson Bumgardner Conroy PC representing Xueshan Technologies, Inc.
  Case Disposition: Settled
- *Polaris Innovations Limited v. Broadcom, Inc.*
  EDTX Case No. 2:22-cv-00347-JRG
  Firm: Nelson Bumgardner Conroy PC representing Polaris Innovations Limited
  Case Disposition: Settled

EMPLOYMENT

- **Personalized Media Communications, LLC, Sugar Land, TX 2014 - Present**
  Vice President – Intellectual Property
  Responsibilities include working on both patent licensing and patent litigation activities for approximately 100 assets originated by the same inventors. Responsible for the identification of potential patent infringement, design and execution of tests to show infringement, claim chart creation, presentation of those findings to accused infringers, and negotiation of settlement agreements. Have also been heavily involved in approximately 20 Inter Partes Reviews. Responsible for ex parte reexamination and reissue patent filings.

- **Uviri, LLC, Plano, TX 2009 - Present**
  President
  The company is involved with many different types of research projects and business activities, including the following:
  - Consulting services related to the review of patents and the enforcement of patent rights.
  - Preparation and prosecution of U.S. patent applications.
  - Research and design of a new type of fractional horsepower electric motor.
  - Basic research and development into an alternative to Fourier decomposition.
  - Product and electrical design of A-series and T-series LED lighting systems.
  - Product and electrical design of small wattage AC/DC converters.
  - Research and design of a rotating optical oscillator for use in terahertz time-domain spectroscopy systems.
  - Provide photography and photographic services.

- **Texas Instruments Incorporated, Dallas, TX 2003 - 2014**
  Patent Licensing Associate
  Responsible for the assertion and defense of patents in technical fields including DRAM and nonvolatile memory, analog circuits, image sensors, digital displays, processors, and digital systems. Identified patents of interest from a pool of over 14,000 assets. Created

claim charts to demonstrate infringement and presented those findings to accused infringers. Managed multiple teams working to identify patent infringement, to ascertain the scope of reverse engineering, and to create uniform claim charts across all teams. Worked with licensees in Japan, Asia Pacific Region, North America, and Europe. Licensing revenue generated during this employment exceeded U.S. $3 billion. Also maintained a small docket of patents submitted for ex parte reexamination with the USPTO.

- **Rosenthal & Osha L.L.P., Houston, TX** **2001 - 2003**
  Patent Agent
  Prepared over 50 utility patent applications per year by applying a broad background of experience. Technical fields for the applications included analog and digital circuits, microprocessor architecture, computer system design, and digital signal processing (DSP). Responded to both national and international Office Actions, and filed RCEs in response to Advisory Actions. Managed a five-person team focused on protecting microprocessor core IP. Mentored patent engineers and reviewed draft applications.

- **Rice University, Houston, TX** **1994 - 2001**
  Research Associate - Department of Electrical and Computer Engineering
  Applied a wide variety of DSP techniques to investigate terahertz (THz) time-domain spectroscopy signals. Solved inverse problems, improved resolution, and facilitated imaging and classification for real-time THz systems. Authored numerous journal articles and conference papers, and presented findings at numerous conferences (listed below). Other areas of investigation included wavelets, speech processing, biomedical imaging, and computer architecture.

- **Texas Instruments Incorporated, Houston, TX** **1988 - 1998**
  1997 - 1998 Circuits Center of Expertise Engineer - Memory Products Design
  Originated comparisons of internal and competitor DRAM designs through simulation, characterization, deprocessing, and internal probe. Identified and evaluated key aspects of DRAM designs by interacting with design teams, product engineering, and external resources to gather and disseminate information. Built web pages to report the analysis to a broad audience. Integrated information and made sound conclusions from which future designs could draw.

  Personal accomplishments included the following:
  - Promoted and helped implement the formation of the Circuits COE that resulted in being the only individual contributor chosen from the Houston design center.
  - Achieved an 8% speed improvement in access time through a redesign of the critical path and output buffers.
  - Identified and correlated device processing characteristics which degraded signal transmission and device performance.

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- Simulated and summarized the work on competing access versus hold time specifications which demonstrated that additional regulation circuitry was not needed.
- Texas Instruments representative during SynchLink DRAM (MOSAID) engagement.

1990 - 1997 IC Design Engineer - Application Specific DRAM Design
Demonstrated engineering breadth and depth through the design, simulation, probe, debug, and test support of various major sections on at least five DRAM devices, two of which had 95M units shipped with $525M in sales. These included row and row redundancy, column and column redundancy, design-for-test, I/O buffers, internal refresh, and data I/O. Performed full-chip schematic verification, design rule verification, and probe versus simulation comparison. Supported the lead frame design, ESD implementation, parasitic back annotation, laser repair, and layout.

Personal accomplishments included the following:

- Originated numerous patents (listed below) that focused on reduced silicon usage and improved DRAM performance.
- Traveled to Japan (KTI) and Singapore (TECH) to provide DRAM design support and training.
- Traveled to TI-Singapore for DRAM T3/batch testing support.
- Investigated and audited TI's first commercial 64 megabit Synchronous DRAM column, internal refresh, voltage regulators, and power-up circuitry.
- Selected point person by V.P. to assemble a team, create, and help instruct "DRAM Design for Non-DRAM Designers". Implemented the course both in Europe and Asia Pacific Region.
- Provided weekly training of DRAM design basics to Houston PDE/CQE engineers.
- Mentored and supervised engineers and layout support to achieve on-time schematic verification.
- Spearheaded new hire activities and on-campus recruiting which resulted in at least ten new employees.

1988 - 1990 Product Development Engineer - Video RAM Development
Programmed a PWS Colt IIIA device tester for gross functional tests and test time reduction. Drafted specification sheets. Created and updated device comparison tables. Resolved customer issues including returned device evaluation and device specification comparison.

PUBLICATIONS

Book Chapters

- "Multistatic Reflection Imaging with Terahertz Pulses," T. Dorney, W. W. Symes, and D. Mittleman, in Terahertz Sensing Technology, Vol. 1. Electronic Devices and Advanced Systems Technology, Ed. D. Woolard, W. Loerop, and M. Shur, World Scientific Publishing, Singapore (2003), pp. 327-349.

Refereed Journal Articles

- Timothy D. Dorney, William W. Symes, Daniel M. Mittleman, "Multistatic Reflection Imaging with Terahertz Pulses", *International Journal of High Speed Electronics and Systems*, Vol. 13, Issue 02, pp. 677-699, June, 2003.
- Timothy D. Dorney, Molly Rossow, William W. Symes, Daniel M. Mittleman, "Single-cycle Terahertz Electromagnetic Pulses: A New Test Bed for Physical Seismic Modeling", *Geophysics*, Vol. 68, No. 1, pp. 308-313, January, 2003.
- Timothy D. Dorney, William W. Symes, Richard G. Baraniuk, Daniel M. Mittleman, "Terahertz Multistatic Reflection Imaging", *Journal of the Optical Society of America A*, Vol. 19, Issue 7, pp. 1432-1442, 2002.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, "Enhanced Depth Resolution Using Phase-Shift Interferometry", *Optics and Photonics News*, Vol. 12, December, 2001.
- Timothy D. Dorney, Jon L. Johnson, James Van Rudd, Richard G. Baraniuk, William Symes, Daniel M. Mittleman, "Terahertz Reflection Imaging using Kirchhoff Migration", *Optics Letters*, Vol. 26, No. 19, pp. 1513-1515, October, 2001.
- Timothy D. Dorney, Richard G. Baraniuk, Daniel M. Mittleman, "Material Parameter Estimation with Terahertz Time-Domain Spectroscopy", *Journal of the Optical Society of America A*, Vol. 18, Issue 7, pp. 1562-1571, August, 2001.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, "Interferometric Imaging with Terahertz Pulses", *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 7, Issue 4, pp. 592-599, July-Sept., 2001.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, "Enhanced Depth Resolution in Terahertz Imaging using Phase-Shift Interferometry", *Applied Physics Letters*, Vol. 78, pp. 835-837, February, 2001.
- Timothy D. Dorney, "An Introduction to Fuzzy Logic Control", *Texas Instruments Technical Journal*, Vol. 10, No. 4, July/August, 1993, pp. 84-89.
- Timothy D. Dorney, "An Improved Architecture and Training Technique for Artificial Neural Networks", *Texas Instruments Technical Journal*, Vol. 10, No. 3, May/June, 1993, pp. 10-17.

Other Articles

- Jon L. Johnson, Tim Dorney, and Daniel Mittleman, "Enhanced depth resolution using phase-shift interferometry," *Optics and Photonics News, Special Issue: Optics in 2001*, 12, 21, December 2001.

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- Timothy D. Dorney, Jon Johnson, Daniel M. Mittleman, Richard G. Baraniuk, "Imaging with Terahertz Pulses", *Proceedings of SPIE - The International Society for Optical Engineering*, SPIE 4115, Applications of Digital Image Processing XXIII, December, 2000.
- J. L. Johnson, T. D. Dorney, J. V. Rudd, and D. M. Mittleman, "Terahertz Reflectometry: A Model System for the Inverse Problem," *ITW 2000 – International Terahertz Workshop*, p. 39, Sandbjerg, Denmark, December 2000.
- J. L. Johnson, T. D. Dorney, J. V. Rudd, and D. M. Mittleman, "Terahertz Reflectometry: A Model System for the Inverse Problem," *IEEE/LEOS Annual Meeting Conference Proceedings*, Vol. 1, p. 242, Rio Grande, Puerto Rico, November 2000.
- Timothy D. Dorney, Srikrishna Bhashyam, Andrew Doran, Hyeokho Choi, Patrick Flandrin, Richard G. Baraniuk, "Edge Localized Image Sharpening via Reassignment with Application to Computed Tomography", *Proceedings of SPIE - The International Society for Optical Engineering*, SPIE 4121, Mathematical Modeling, Estimation, and Imaging, October, 2000.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, "Background-free THz Imaging using Interferometric Tomography", *Ultrafast Phenomena XII*, Springer Series in Chemical Physics, Vol. 66, pp. 262-264, Springer, Charleston, SC, July 2000.
- Timothy D. Dorney, Jon Johnson, Daniel M. Mittleman, Richard G. Baraniuk, "Imaging with THz Pulses", International Conference on Image Processing 1:764-767, Vol. 1, February, 2000.
- J.L. Johnson, Timothy D. Dorney, James V Rudd, Daniel M. Mittleman, "Terahertz Reflectometry: A Model System for the Inverse Problem", Conference Proceedings - Lasers and Electro-Optics Society Annual Meeting-LEOS 1:242 Vol.1, February, 2000.
- Timothy D. Dorney, Richard G. Baraniuk, Daniel M. Mittleman, "Spectroscopic Imaging using Terahertz Time-Domain Signals", *4th IEEE Southwest Symposium on Image Analysis and Interpretation*, Austin, TX, USA, 2000. Proceedings. 4th IEEE Southwest Symposium, April 2-4, 2000.
- J. L. Johnson, T. Dorney and D. Mittleman, "Background-free THz imaging using interferometric tomography*", Conference on Lasers and Electro-Optics (CLEO 2000). Technical Digest. Postconference Edition.* TOPS Vol.39 (IEEE Cat. No.00CH37088), San Francisco, CA, USA, 2000, pp. 526-527.

Presentations

- "Terahertz Reflectometry: A Model System for the Inverse Problem", presented at the IEEE/LEOS Annual Meeting Conference, Rio Grande, Puerto Rico, November, 2000.

- "Edge localized image sharpening via reassignment with application to computed tomography", presented at the SPIE Mathematical Modeling, Estimation, and Imaging Conference, San Diego, CA, July 31, 2000.
- "Identification and Classification of Materials Using Terahertz Time-Domain Spectroscopy", presented at the Rice Quantum Institute Summer Research Colloquium, August 20, 1999.

PATENTS

- U.S. Patent Number 7,046,412, "Scanning optical delay line using a reflective element arranged to rotate", Timothy D. Dorney, May 16, 2006.
- Korean Patent Number KR100336951B1, "Method and apparatus for testing memory circuits using parallel block write operations", Timothy Dominic Dorney, Anthony Michael Balistreri, September 9, 2002.
- U.S. Patent Number 6,091,665, "Synchronous random access memory having column factor counter for both serial and interleave counting", Timothy D. Dorney, July 18, 2000.
- U.S. Patent Number 6,088,274, "Method and device for testing a semiconductor serial access memory device through a main memory", Timothy D. Dorney, Steven C. Eplett, Rishad S. Omer, John E. Riley, July 11, 2000.
- U.S. Patent Number 6,084,811, "Phased sense amplifiers", Timothy D. Dorney, July 4, 2000.
- U.S. Patent Number 5,920,573, "Method and apparatus for reducing area and pin count required in design for test of wide data path memories", Timothy D. Dorney, July 6, 1999.
- German Patent Number DE69505806T2, "Method and device for a design for testing a memory with parallel block-write operation", Timothy Dominic Dorney, Anthony Michael Balistreri, May 12, 1999.
- European Patent Number EP0757837B1, "A method and apparatus for testing a memory circuit with parallel block write operation", Timothy Dominic Dorney, Anthony Michael Balistreri, November 4, 1998.
- U.S. Patent Number 5,740,179, "Method and apparatus for a design for test, parallel block write operation", Timothy Dominic Dorney, Anthony Michael Balistreri, April 14, 1998.
- U.S. Patent Number 5,732,030, "Method and system for reduced column redundancy using a dual column select", Timothy D. Dorney, March 24, 1998.

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SKILLS & ADVANCED COURSES

Languages: C, Windows C, FORTRAN, Pascal, Assembly, BASIC, PWS tslang

Programs: TISpice, Cadence Analog Artist, Mentor Graphics Design Architect and IC Station, ADCAP, ICE, LSIM, Siganal, MATLAB, HTML, Windows, UNIX, AWK, Texas Instruments and Microchip Technology Integrated Development Environment, Interleaf, Microsoft Office, Adobe Photoshop, Nikon Capture, Imagenomic Portraiture, Alibre, KeyShot

Hardware: PC, Macintosh, DEC, HP, Apollo, Sun, PWS Colt IIIA device testers, Texas Instruments and Microchip Technology development boards

- Six Sigma Design for Manufacturability
- Advanced DSP
- Digital Image Processing
- VLSI Design and Layout
- Filter Theory
- Image Feature Extraction
- Spectral Estimation
- Computer Architecture
- Communication Theory
- Digital System Design
- Wavelets
- Random Processes
- Digital Control
- Artificial Neural Networks
- Fuzzy Logic
- Speech Processing
- Leading Effective Meetings
- Presentation Skills
- PC Board Design, Manufacture, and Test
- Laboratory Bench Testing
- Photography
- Photo editing tools

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Appendix B

DDR2 SDRAM

MT47H512M4 – 64 Meg x 4 x 8 banks
MT47H256M8 – 32 Meg x 8 x 8 banks
MT47H128M16 – 16 Meg x 16 x 8 banks

Features

- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- RoHS-compliant
- Supports JEDEC clock jitter specification

Options[1]	Marking
• Configuration	
– 512 Meg x 4 (64 Meg x 4 x 8 banks)	512M4
– 256 Meg x 8 (32 Meg x 8 x 8 banks)	256M8
– 128 Meg x 16 (16 Meg x 16 x 8 banks)	128M16
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (11.5mm x 14mm) Rev. A	HG
• FBGA package (Pb-free) – x4, x8	
– 60-ball FBGA (11.5mm x 14mm) Rev. A	HG
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (9mm x 12.5mm) Rev. C	RT
• FBGA package (Pb-free) – x4, x8	
– 60-ball FBGA (9mm x 11.5mm) Rev. C	EB
• FBGA package (Lead solder) – x16	
– 84-ball FBGA (9mm x 12.5mm) Rev. C	PK
• Timing – cycle time	
– 1.875ns @ CL = 7 (DDR2-1066)	-187E
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 2.5ns @ CL = 6 (DDR2-800)	-25
– 3.0ns @ CL = 5 (DDR2-667)	-3
• Self refresh	
– Standard	None
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +85°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C; –40°C ≤ T_A ≤ +85°C)	IT
• Revision	:A/:C

Note: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.

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Table 1: Key Timing Parameters

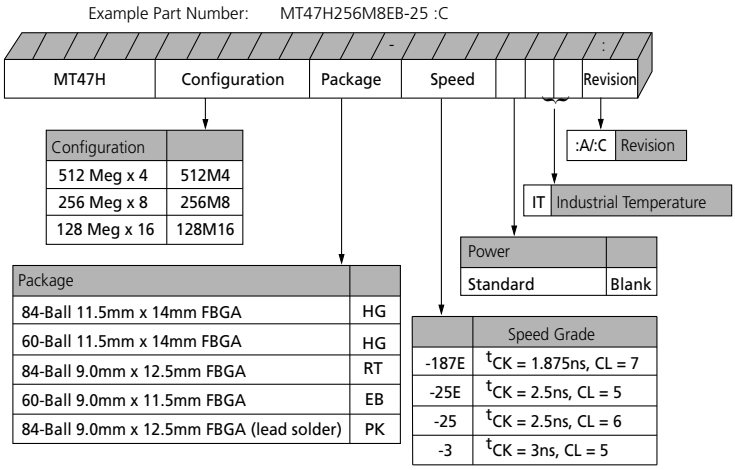
Speed Grade	Data Rate (MHz)					^{t}RC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	CL = 7	
-187E	400	533	800	800	1066	54
-25E	400	533	800	800	n/a	55
-25	400	533	667	800	n/a	55
-3	400	533	667	n/a	n/a	55

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	A[14:0] (32K)	A[14:0] (32K)	A[13:0] (16K)
Bank address	BA[2:0] (8)	BA[2:0] (8)	BA[2:0] (8)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Part Numbers

Figure 1: 2Gb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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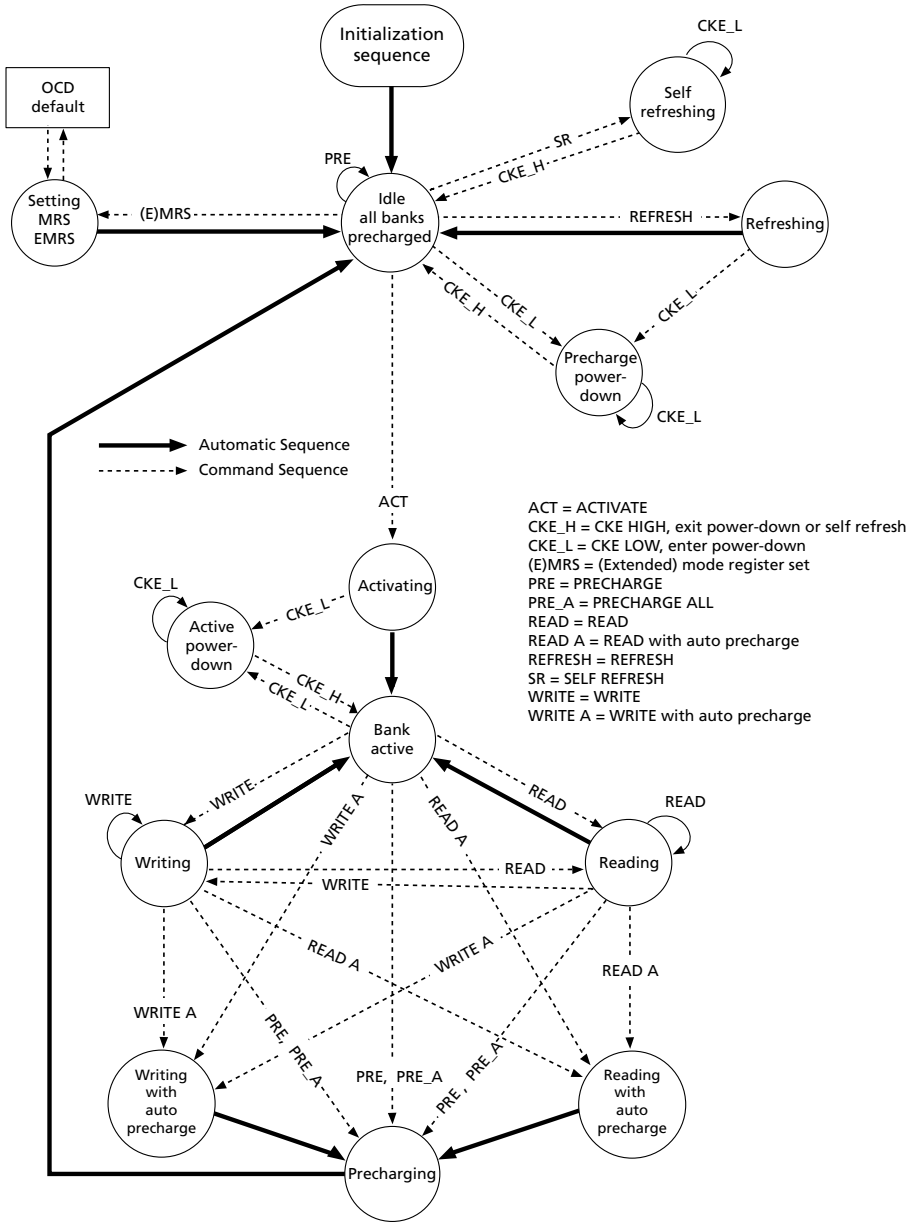
State Diagram

Figure 2: Simplified State Diagram



Note: 1. This diagram provides the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions such as multibank interaction, power down, entry/exit, etc.

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Functional Description

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single READ or WRITE operation for the DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, two-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR2 SDRAM enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than –40°C or greater than 85°C, and the case temperature cannot be less than –40°C or greater than 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, input/output impedance and I_{DD} values must be derated when T_C is < 0°C or > 85°C.

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General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor
  - Connect UDQS# to V_{DD} via 1kΩ* resistor
  - Connect UDM to V_{DD} via 1kΩ* resistor
  - Connect DQ[15:8] individually to either V_{SS} or V_{DD} via 1kΩ* resistors, or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

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Functional Block Diagrams

The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multibank DRAM.

Figure 3: Functional Block Diagram – 512 Meg x 4

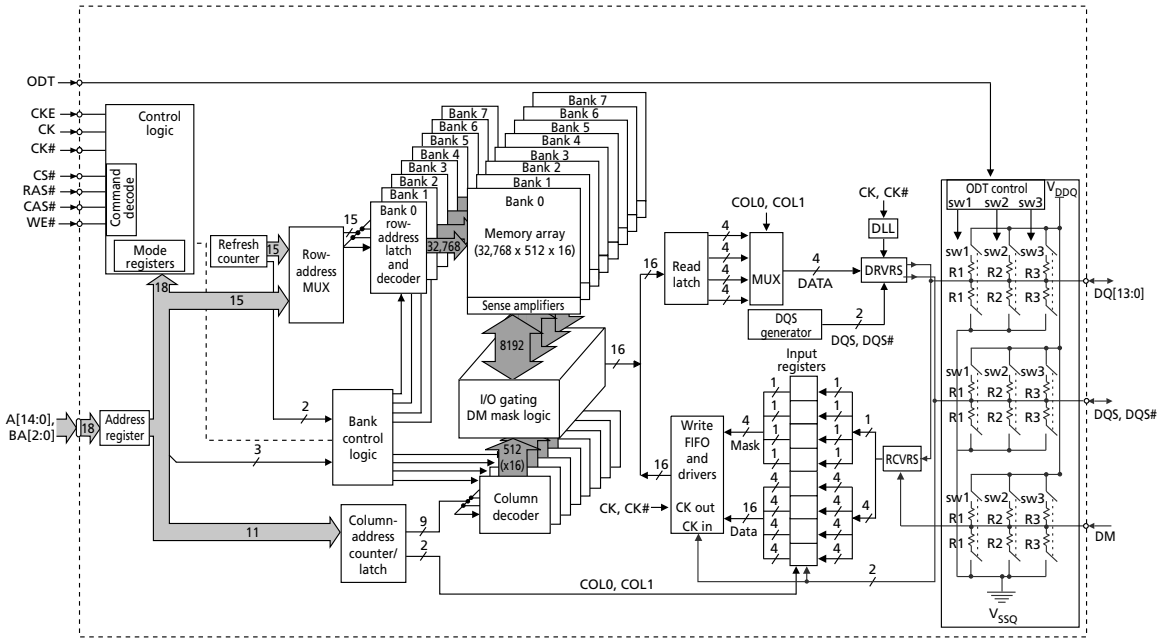

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Figure 4: Functional Block Diagram – 256 Meg x 8

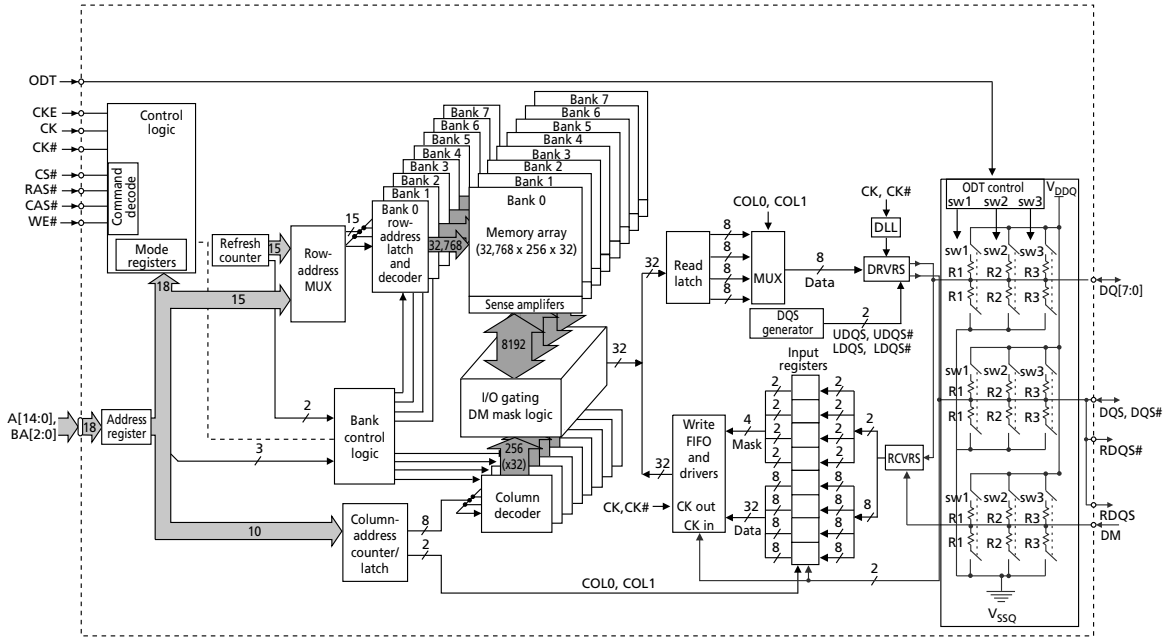

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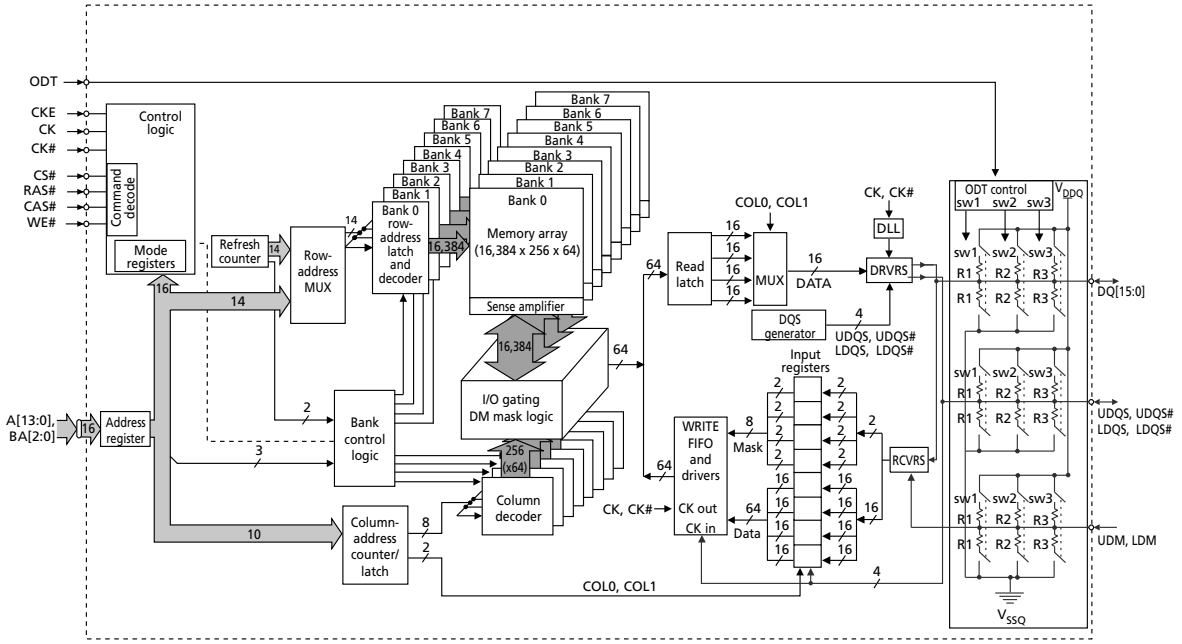
Figure 5: Functional Block Diagram – 128 Meg x 16



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Ball Assignments and Descriptions

Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)

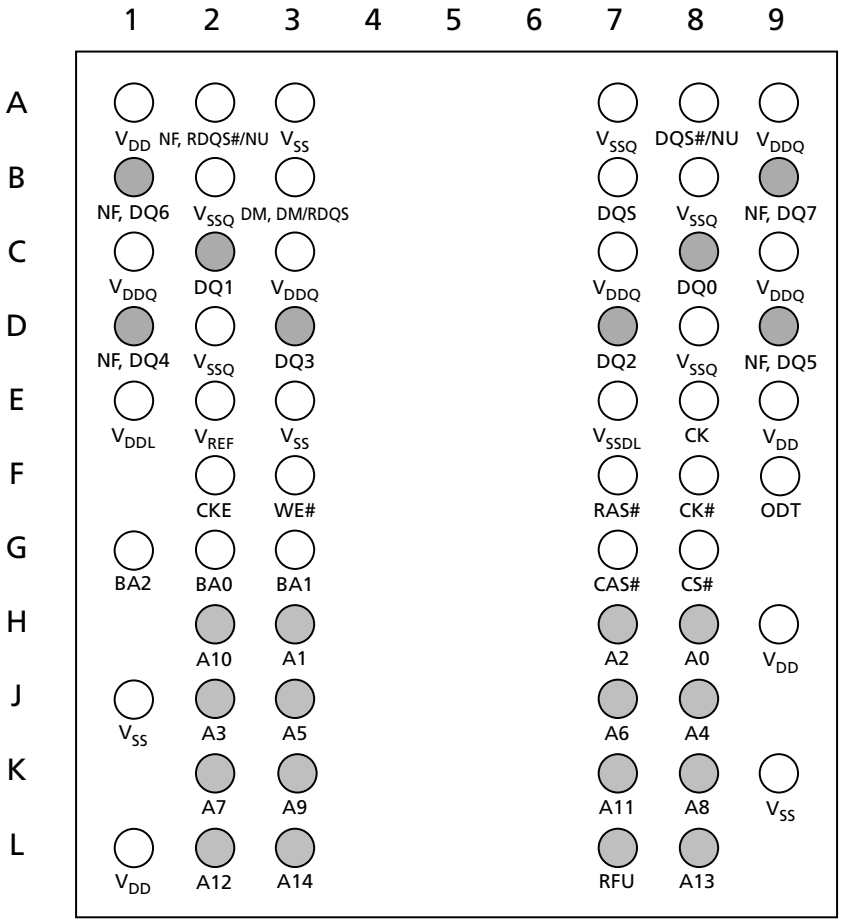

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Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)

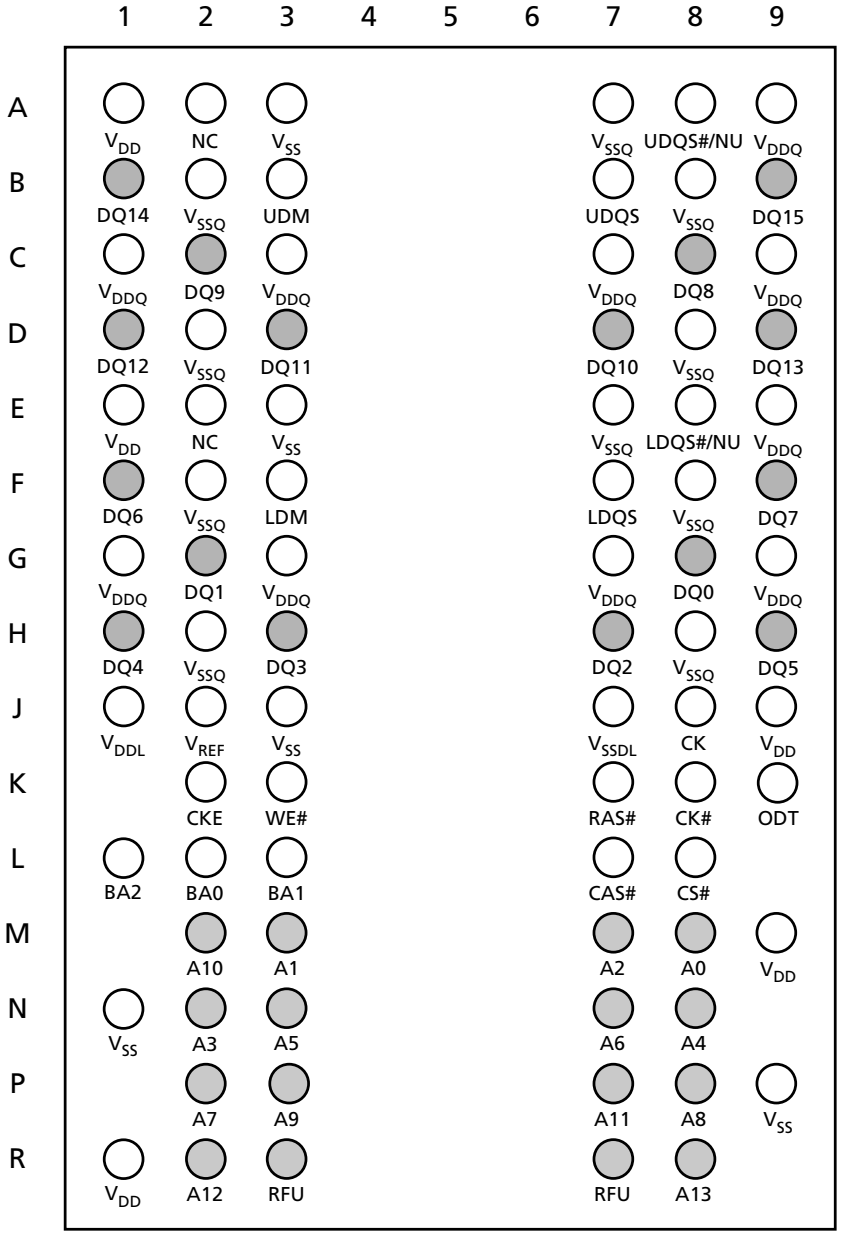

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Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions

Symbol	Type	Description
A[13:0] (x16) A[14:0] (x4, x8)	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operation (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for self refresh entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, V_{REF} must be maintained.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered high. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
LDM, UDM (DM)	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ[7:0] and UDM is DM for upper byte DQ[15:8].
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ[15:0], LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ[7:0], DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
DQ[15:0] (x16) DQ[3:0] (x4) DQ[7:0] (x8)	I/O	**Data input/output:** Bidirectional data bus for 128 Meg x 16. Bidirectional data bus for 512 Meg x 4. Bidirectional data bus for 256 Meg x 8.

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Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions (Continued)

Symbol	Type	Description
DQS, DQS#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
LDQS, LDQS#	I/O	**Data strobe for lower byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
UDQS, UDQS#	I/O	**Data strobe for upper byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
RDQS, RDQS#	Output	**Redundant data strobe:** For x8 only. RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled and differential data strobe mode is enabled.
V_{DD}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDQ}	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
V_{DDL}	Supply	**DLL power supply:** 1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage.
V_{SS}	Supply	Ground.
V_{SSDL}	Supply	**DLL ground:** Isolated on the device from V_{SS} and V_{SSQ}.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	–	**No connect:** These balls should be left unconnected.
NF	–	**No function:** Not used only on x4. These are data lines on the x8.
NU	–	**Not used:** Not used only on x16. If EMR[E10] = 0, A8 and E8 are UDQS# and LDQS#. If EMR[E10] = 1, then A8 and E8 are not used.
NU	–	**Not used:** For x4: Not used. For x8: If EMR[E10] = 0, E2 and E8 are RDQS# and DQS#; if EMR[E10] = 1, then E2 and E8 are not used.
RFU	–	**Reserved for future use:** Row address bits A14 (R3), A15 (R7) on the x16, and A15 (L7) on the x4/x8.

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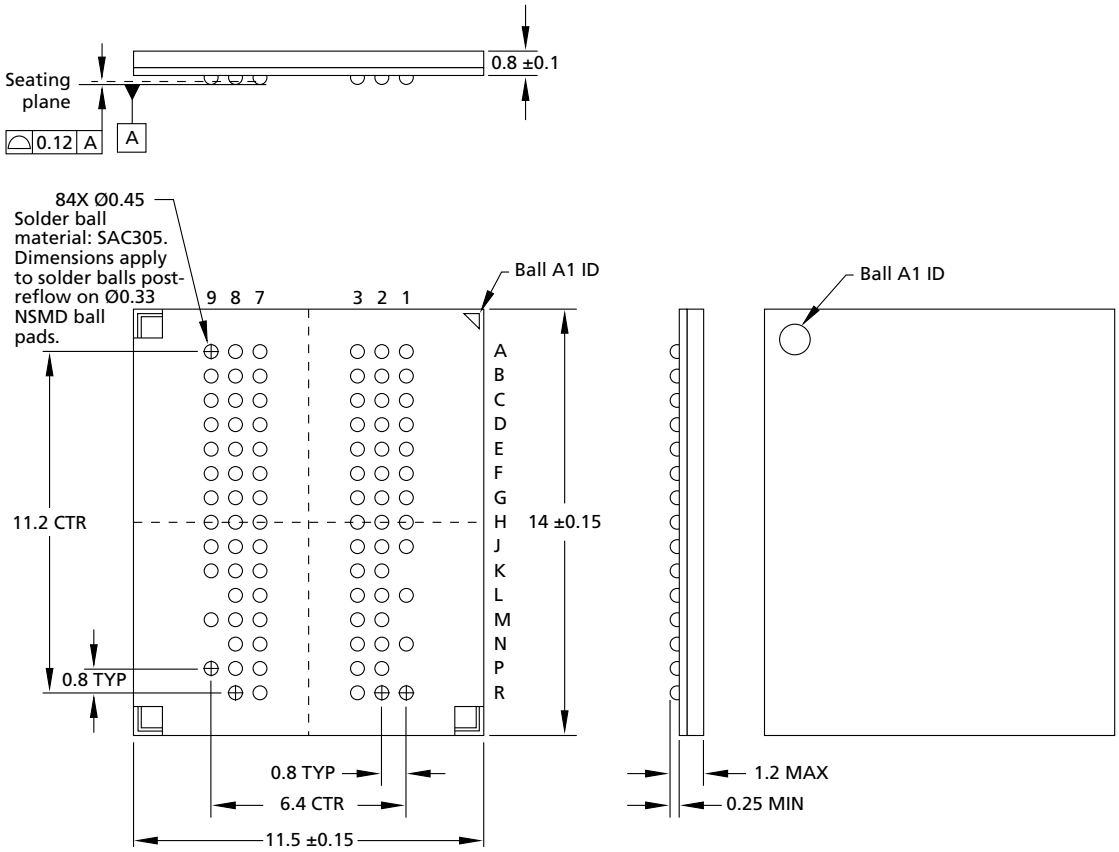
Packaging

Package Dimensions

Figure 8: 84-Ball FBGA Package (11.5mm x 14mm) – x16



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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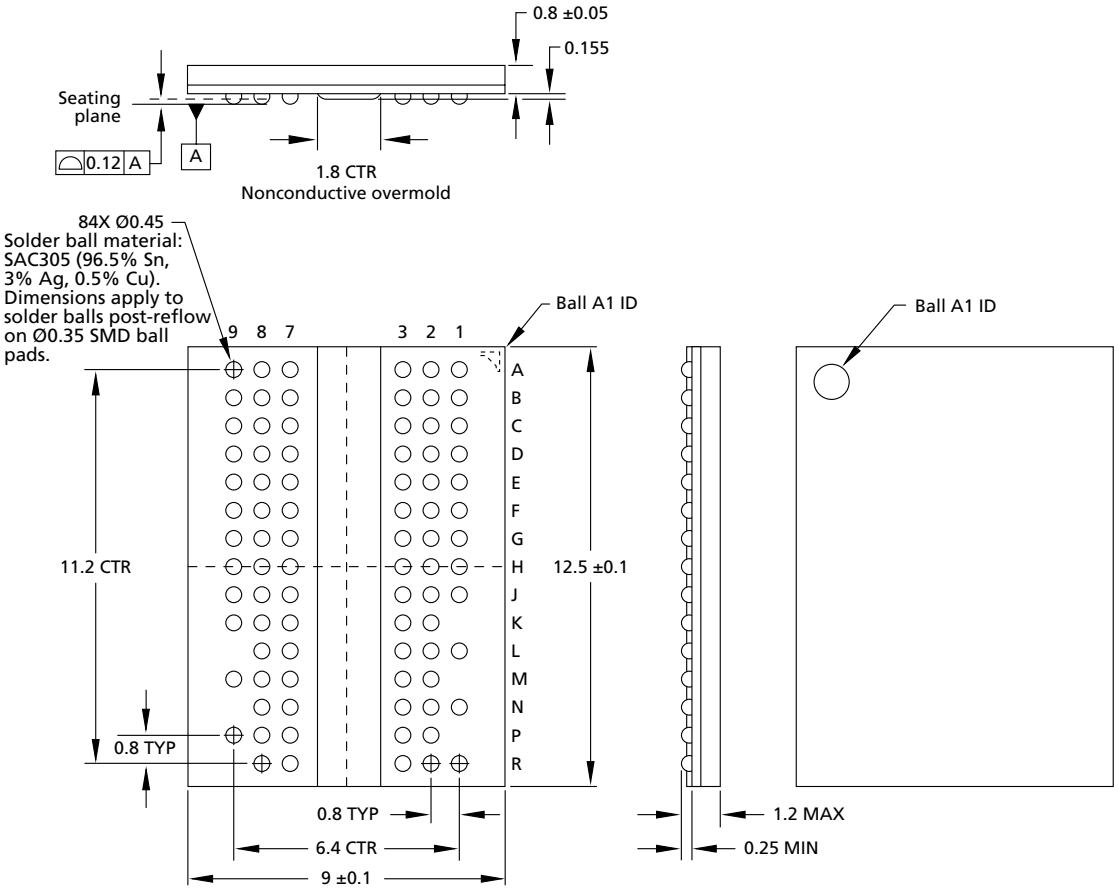
Figure 9: 84-Ball FBGA Package (9mm x 12.5mm) – x16



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) or leaded Eutectic (62% Sn, 36%Pb, 2% Ag).

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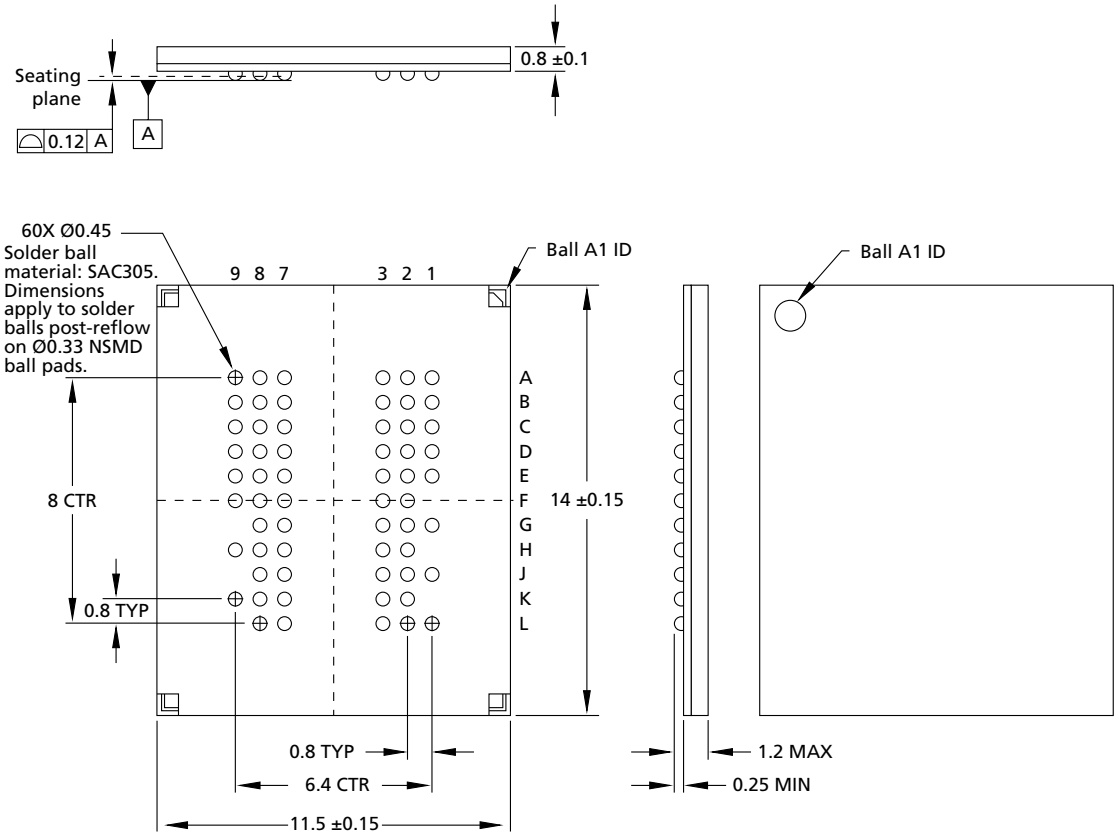
Figure 10: 60-Ball FBGA Package (11.5mm x 14mm) – x4, x8



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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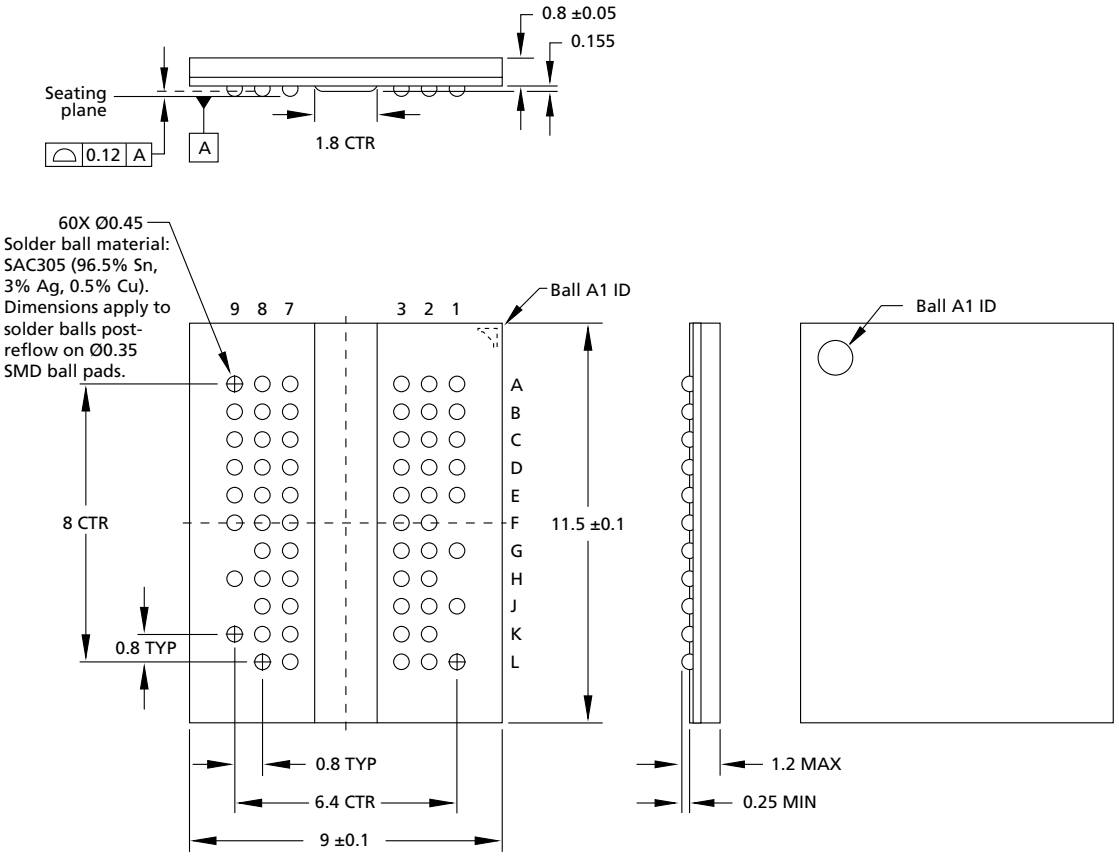
Figure 11: 60-Ball FBGA Package (9mm x 11.5mm) – x4, x8



Note: 1. All dimensions are in millimeters.

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FBGA Package Capacitance

Table 4: Input Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	C_{CK}	1.0	2.0	pF	1
Delta input capacitance: CK, CK#	C_{DCK}	–	0.25	pF	2, 3
Input capacitance: BA[2:0], A[14:0] (A[13:0] on x16), CS#, RAS#, CAS#, WE#, CKE, ODT	C_I	1.0	2.0	pF	1
Delta input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_{DI}	–	0.25	pF	2, 3
Input/output capacitance: DQ, DQS, DM, NF	C_{IO}	2.5	4.0	pF	1, 4
Delta input/output capacitance: DQ, DQS, DM, NF	C_{DIO}	–	0.5	pF	2, 3

Notes:
1. This parameter is sampled. V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C, $V_{OUT(DC)}$ = $V_{DDQ}/2$, V_{OUT} (peak-to-peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
2. The capacitance per ball group will not differ by more than this maximum amount for any given device.
3. ΔC are not pass/fail parameters; they are targets.
4. Reduce MAX limit by 0.25pF for -3/-3E speed devices.

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Electrical Specifications – Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–1.0	2.3	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.5	2.3	V	1, 2
V_{DDL} supply voltage relative to V_{SSL}	V_{DDL}	–0.5	2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V	3
Input leakage current; any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V)	I_I	–5	5	µA	
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled	I_{OZ}	–5	5	µA	
V_{REF} leakage current; V_{REF} = valid V_{REF} level	I_{VREF}	–2	2	µA	

Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times; this is not required when power is ramping down.
2. V_{REF} ≤ 0.6 x V_{DDQ}; however, V_{REF} may be ≥ V_{DDQ} provided that V_{REF} ≤ 300mV.
3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 6 (page 25), be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 7 (page 26) for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the thermal impedances listed in Table 7. For designs that are expected to last several years and require the flexibility to use several designs, consider using final target theta values, rather than existing values, to account for larger thermal impedances.

The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

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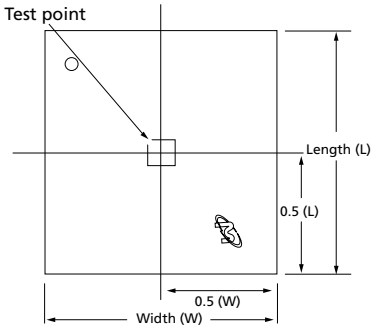
Table 6: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	–55	150	°C	1
Operating temperature – commercial	T_C	0	85	°C	2, 3
Operating temperature – industrial	T_C	–40	95	°C	2, 3, 4
	T_{AMB}	–40	85	°C	4, 5

Notes:
1. MAX storage case temperature T_{STG} is measured in the center of the package, as shown in Figure 12. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
2. MAX operating case temperature T_C is measured in the center of the package, as shown in Figure 12.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Both temperature specifications must be satisfied.
5. Operating ambient temperature surrounding the package.

Figure 12: Example Temperature Test Point Location



Lmm x Wmm FBGA

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Table 7: Thermal Impedance

Die Rev	Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
A[1]	60-ball	2-layer	48.0	34.4	29.3	21.6	1.6
		4-layer	33.7	26.7	23.8	19.7	
	84-ball	2-layer	48.0	34.4	29.3	21.6	1.6
		4-layer	33.7	26.7	23.8	19.7	
C[1]	60-ball	2-layer	63.8	46.9	40.8	29.9	4.3
		4-layer	46.9	38.1	34.4	29.2	
	84-ball	2-layer	60.0	43.5	37.9	26.0	4.1
		4-layer	43.2	34.7	31.5	25.5	

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

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Electrical Specifications – I_{DD} Parameters

I_{DD} Specifications and Conditions

Table 8: General I_{DD} Parameters

I_{DD} Parameters	-187E	-25E	-25	-3E	-3	-37E	-5E	Units
CL (I_{DD})	7	5	6	4	5	4	3	^{t}CK
^{t}RCD (I_{DD})	13.125	12.5	15	12	15	15	15	ns
^{t}RC (I_{DD})	58.125	57.5	60	57	60	60	55	ns
^{t}RRD (I_{DD}) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns
^{t}RRD (I_{DD}) - x16 (2KB)	10	10	10	10	10	10	10	ns
^{t}CK (I_{DD})	1.875	2.5	2.5	3	3	3.75	5	ns
^{t}RAS MIN (I_{DD})	45	45	45	45	45	45	40	ns
^{t}RAS MAX (I_{DD})	70,000	70,000	70,000	70,000	70,000	70,000	70,000	ns
^{t}RP (I_{DD})	13.125	12.5	15	12	15	15	15	ns
^{t}RFC (I_{DD} - 256Mb)	75	75	75	75	75	75	75	ns
^{t}RFC (I_{DD} - 512Mb)	105	105	105	105	105	105	105	ns
^{t}RFC (I_{DD} - 1Gb)	127.5	127.5	127.5	127.5	127.5	127.5	127.5	ns
^{t}RFC (I_{DD} - 2Gb)	195	195	195	195	195	195	195	ns
^{t}FAW (I_{DD}) - x4/x8 (1KB)	Defined by pattern in Table 9 (page 28)							ns
^{t}FAW (I_{DD}) - x16 (2KB)	Defined by pattern in Table 9 (page 28)							ns

I_{DD7} Conditions

The detailed timings are shown below for I_{DD7}. Changes will be required if timing parameter changes are made to the specification. Where general I_{DD} parameters in Table 8 conflict with pattern requirements of Table 9 (page 28), then Table 9 requirements take precedence.

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Table 9: I_{DD7} Timing Patterns (8-Bank Interleave READ Operation)

Speed Grade	I_{DD7} Timing Patterns
Timing patterns for 8-bank x4/x8 devices	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 A4 RA4 A5 RA5 A6 RA6 A7 RA7
-37E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D
-3	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D
-3E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D
-25	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-25E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-187E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D
Timing patterns for 8-bank x16 devices	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-3	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D
-3E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D
-25	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
-187E	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D

Notes:
1. A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at minimum ^{t}RC (I_{DD}) without violating ^{t}RRD (I_{DD}) using a BL = 4.
3. Control and address bus inputs are STABLE during DESELECTs.

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Table 10: DDR2 I_{DD} Specifications and Conditions (Die Revision A)

Notes 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-25E/-25	-3	Units
Operating one bank active-precharge current: $^tCK = {}^tCK$ (I_{DD}), $^tRC = {}^tRC$ (I_{DD}), $^tRAS = {}^tRAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x4, x8	115	100	mA
		x16	150	135	
Operating one bank active-read-precharge current: Iout = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK$ (I_{DD}), $^tRC = {}^tRC$ (I_{DD}), $^tRAS = {}^tRAS$ MIN (I_{DD}), $^tRCD = {}^tRCD$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x4, x8	165	145	mA
		x16	180	160	
Precharge power-down current: All banks idle; $^tCK = {}^tCK$ (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x4, x8, x16	12	12	mA
Precharge quiet standby current: All banks idle; $^tCK = {}^tCK$ (I_{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x4, x8	65	55	mA
		x16	75	65	
Precharge standby current: All banks idle; $^tCK = {}^tCK$ (I_{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x4, x8	70	60	mA
		x16	80	70	
Active power-down current: All banks open; $^tCK = {}^tCK$ (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast PDN exit MR[12] = 0	45	40	mA
	I_{DD3Ps}	Slow PDN exit MR[12] = 1	14	14	
Active standby current: All banks open; $^tCK = {}^tCK$ (I_{DD}), $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x4, x8	65	55	mA
		x16	85	75	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK$ (I_{DD}), $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x4, x8	180	160	mA
		x16	270	250	
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK$ (I_{DD}), $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}	x4, x8	190	170	mA
		x16	295	275	
Burst refresh current: $^tCK = {}^tCK$ (I_{DD}); refresh command at every ^tRFC (I_{DD}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}	x4, x8	300	280	mA
		x16	300	280	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}	x4, x8, x16	12	12	mA
	I_{DD6L}		8	8	

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Table 10: DDR2 I_{DD} Specifications and Conditions (Die Revision A) (Continued)

Notes 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-25E/-25	-3	Units
Operating bank interleave read current: All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = ^tRCD (I_{DD}) - 1 x ^tCK (I_{DD}); ^tCK = ^tCK (I_{DD}), ^tRC = ^tRC (I_{DD}), ^tRRD = ^tRRD (I_{DD}), ^tRCD = ^tRCD (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching (see Table 9 (page 28) for details)	I_{DD7}	x4, x8	390	340	mA
		x16	445	395	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C.
2. V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V, V_{DDL} = 1.8V ±0.1V, V_{REF} = V_{DDQ}/2.
3. I_{DD} parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. I_{DD} values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for I_{DD} conditions:

LOW	$V_{IN} \le V_{IL(AC)max}$
HIGH	$V_{IN} \ge V_{IH(AC)min}$
Stable	Inputs stable at a HIGH or LOW level
Floating	Inputs at V_{REF} = V_{DDQ}/2
Switching	Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
Switching	Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes

6. I_{DD1}, I_{DD4R}, and I_{DD7} require A12 in EMR1 to be enabled during testing.
7. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:

When T_C ≤ 0°C	I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%.
When T_C ≥ 85°C	I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5} must be derated by 2%; I_{DD2P} must be derated by 20%; I_{DD3P} slow must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2x refresh option is still enabled).

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Table 11: DDR2 I_{DD} Specifications and Conditions (Die Revision C)

Notes 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-187E	-25E/-25	-3	Units
Operating one bank active-precharge current: $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x4, x8	85	75	70	mA
		x16	100	90	85	
Operating one bank active-read-precharge current: Iout = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}), $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x4, x8	95	85	80	mA
		x16	110	105	100	
Precharge power-down current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x4, x8, x16	12	12	12	mA
Precharge quiet standby current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x4, x8	35	30	25	mA
		x16	50	45	40	
Precharge standby current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x4, x8	40	35	30	mA
		x16	55	50	45	
Active power-down current: All banks open; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast PDN exit MR[12] = 0	25	25	25	mA
	I_{DD3Ps}	Slow PDN exit MR[12] = 1	14	14	14	
Active standby current: All banks open; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x4, x8	60	50	45	mA
		x16	60	50	45	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x4, x8	160	130	110	mA
		x16	210	190	170	
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}	x4, x8	160	130	110	mA
		x16	210	190	170	

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Table 11: DDR2 I_{DD} Specifications and Conditions (Die Revision C) (Continued)

Notes 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-187E	-25E/-25	-3	Units
Burst refresh current: $^tCK = {}^tCK$ (I_{DD}); refresh command at every ^tRFC (I_{DD}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}	x4, x8	175	170	165	mA
		x16	175	170	165	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}	x4, x8, x16	12	12	12	mA
	I_{DD6L}		8	8	8	
Operating bank interleave read current: All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = ^tRCD (I_{DD}) - 1 x ^tCK (I_{DD}); $^tCK = {}^tCK$ (I_{DD}), $^tRC = {}^tRC$ (I_{DD}), $^tRRD = {}^tRRD$ (I_{DD}), $^tRCD = {}^tRCD$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching (see Table 9 (page 28) for details)	I_{DD7}	x4, x8	230	220	200	mA
		x16	290	280	250	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C.
2. V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{DDL} = +1.8V ±0.1V, $V_{REF} = V_{DDQ}/2$.
3. I_{DD} parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. I_{DD} values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for I_{DD} conditions:

LOW	$V_{IN} \le V_{IL(AC)max}$
HIGH	$V_{IN} \ge V_{IH(AC)min}$
Stable	Inputs stable at a HIGH or LOW level
Floating	Inputs at $V_{REF} = V_{DDQ}/2$
Switching	Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
Switching	Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes

6. I_{DD1}, I_{DD4R}, and I_{DD7} require A12 in EMR1 to be enabled during testing.
7. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:

When T_C ≤ 0°C	I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%.
When T_C ≥ 85°C	I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5} must be derated by 2%; I_{DD2P} must be derated by 20%; I_{DD3P} slow must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2x refresh option is still enabled).

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AC Timing Operating Specifications

Table 12: AC Operating Specifications and Conditions

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Clock	Clock cycle time CL = 7	^tCK (avg)	1.875	8.0	–	–	–	–	–	–	–	–	–	–	–	–	ns	6, 7, 8, 9
	CL = 6	^tCK (avg)	2.5	8.0	2.5	8.0	2.5	8.0	–	–	–	–	–	–	–	–		
	CL = 5	^tCK (avg)	2.5	8.0	2.5	8.0	3.0	8.0	3.0	8.0	3.0	8.0	–	–	–	–		
	CL = 4	^tCK (avg)	3.75	8.0	3.75	8.0	3.75	8.0	3.0	8.0	3.75	8.0	3.75	8.0	5.0	8.0		
	CL = 3	^tCK (avg)	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0		
	CK high-level width	^tCH (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^tCK	10
	CK low-level width	^tCL (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^tCK	
	Half clock period	^tHP	MIN = lesser of ^tCH and ^tCL MAX = n/a														ps	11
	Absolute ^tCK	^tCK (abs)	MIN = ^tCK (AVG) MIN + ^tJITper (MIN) MAX = ^tCK (AVG) MAX + ^tJITper (MAX)														ps	
	Absolute CK high-level width	^tCH (abs)	MIN = ^tCK (AVG) MIN × ^tCH (AVG) MIN + ^tJITdty (MIN) MAX = ^tCK (AVG) MAX × ^tCH (AVG) MAX + ^tJITdty (MAX)														ps	
	Absolute CK low-level width	^tCL (abs)	MIN = ^tCK (AVG) MIN × ^tCL (AVG) MIN + ^tJITdty (MIN) MAX = ^tCK (AVG) MAX × ^tCL (AVG) MAX + ^tJITdty (MAX)														ps	

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Clock Jitter	Period jitter	^tJITper	–90	90	–100	100	–100	100	–125	125	–125	125	–125	125	–125	125	ps	12
	Half period	^tJITdty	–75	75	–100	100	–100	100	–125	125	–125	125	–125	125	–150	150	ps	13
	Cycle to cycle	^tJITcc	180		200		200		250		250		250		250		ps	14
	Cumulative error, 2 cycles	$^tERR_{2per}$	–132	132	–150	150	–150	150	–175	175	–175	175	–175	175	–175	175	ps	15
	Cumulative error, 3 cycles	$^tERR_{3per}$	–157	157	–175	175	–175	175	–225	225	–225	225	–225	225	–225	225	ps	15
	Cumulative error, 4 cycles	$^tERR_{4per}$	–175	175	–200	200	–200	200	–250	250	–250	250	–250	250	–250	250	ps	15
	Cumulative error, 5 cycles	$^tERR_{5per}$	–188	188	–200	200	–200	200	–250	250	–250	250	–250	250	–250	250	ps	15, 16
	Cumulative error, 6–10 cycles	$^tERR_{6-10per}$	–250	250	–300	300	–300	300	–350	350	–350	350	–350	350	–350	350	ps	15, 16
	Cumulative error, 11–50 cycles	$^tERR_{11-50per}$	–425	425	–450	450	–450	450	–450	450	–450	450	–450	450	–450	450	ps	15
Data Strobe-Out	DQS output access time from CK/CK#	^tDQSCK	–300	300	–350	350	–350	350	–400	400	–400	400	–450	450	–500	500	ps	19
	DQS read preamble	^tRPRE	MIN = 0.9 × ^tCK MAX = 1.1 × ^tCK														^tCK	17, 18, 19
	DQS read postamble	^tRPST	MIN = 0.4 × ^tCK MAX = 0.6 × ^tCK														^tCK	17, 18, 19, 20
	CK/CK# to DQS Low-Z	$^tLZ_1$	MIN = ^tAC (MIN) MAX = ^tAC (MAX)														ps	19, 21, 22

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Data Strobe-In	DQS rising edge to CK rising edge	^tDQSS	MIN = –0.25 × ^tCK MAX = 0.25 × ^tCK														^tCK	18
	DQS input-high pulse width	^tDQSH	MIN = 0.35 × ^tCK MAX = n/a														^tCK	18
	DQS input-low pulse width	^tDQSL	MIN = 0.35 × ^tCK MAX = n/a														^tCK	18
	DQS falling to CK rising: setup time	^tDSS	MIN = 0.2 × ^tCK MAX = n/a														^tCK	18
	DQS falling from CK rising: hold time	^tDSH	MIN = 0.2 × ^tCK MAX = n/a														^tCK	18
	Write preamble setup time	^tWPRES	MIN = 0 MAX = n/a														ps	23, 24
	DQS write preamble	^tWPRE	MIN = 0.35 × ^tCK MAX = n/a														^tCK	18
	DQS write postamble	^tWPST	MIN = 0.4 × ^tCK MAX = 0.6 × ^tCK														^tCK	18, 25
	WRITE command to first DQS transition	–	MIN = WL - ^tDQSS MAX = WL + ^tDQSS														^tCK	

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

	AC Characteristics		-187E		-25E		-25		-3E		-3		-37E		-5E			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Data-Out	DQ output access time from CK/CK#	^tAC	–350	350	–400	400	–400	400	–450	450	–450	450	–500	500	–600	600	ps	19
Data-Out	DQS–DQ skew, DQS to last DQ valid, per group, per access	^tDQSQ	–	175	–	200	–	200	–	240	–	240	–	300	–	350	ps	26, 27
Data-Out	DQ hold from next DQS strobe	^tQHS	–	250	–	300	–	300	–	340	–	340	–	400	–	450	ps	28
Data-Out	DQ–DQS hold, DQS to first DQ not valid	^tQH	MIN = ^tHP - ^tQHS MAX = n/a														ps	26, 27, 28
Data-Out	CK/CK# to DQ, DQS High-Z	^tHZ	MIN = n/a MAX = ^tAC (MAX)														ps	19, 21, 29
Data-Out	CK/CK# to DQ Low-Z	$^tLZ_2$	MIN = 2 × ^tAC (MIN) MAX = ^tAC (MAX)														ps	19, 21, 22
Data-Out	Data valid output window	DVW	MIN = ^tQH - ^tDQSQ MAX = n/a														ns	26, 27
Data-In	DQ and DM input setup time to DQS	^tDSb	0	–	50	–	50	–	100	–	100	–	100	–	150	–	ps	26, 30, 31
Data-In	DQ and DM input hold time to DQS	^tDHb	75	–	125	–	125	–	175	–	175	–	225	–	275	–	ps	26, 30, 31
Data-In	DQ and DM input setup time to DQS	^tDSa	200	–	250	–	250	–	300	–	300	–	350	–	400	–	ps	26, 30, 31
Data-In	DQ and DM input hold time to DQS	^tDHa	200	–	250	–	250	–	300	–	300	–	350	–	400	–	ps	26, 30, 31
Data-In	DQ and DM input pulse width	^tDIPW	MIN = 0.35 × ^tCK MAX = n/a														^tCK	18, 32

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Command and Address	Input setup time		^{t}ISb	125	–	175	–	175	–	200	–	200	–	250	–	350	–	ps	31, 33
	Input hold time		^{t}IHb	200	–	250	–	250	–	275	–	275	–	375	–	475	–	ps	31, 33
	Input setup time		^{t}ISa	325	–	375	–	375	–	400	–	400	–	500	–	600	–	ps	31, 33
	Input hold time		^{t}IHa	325	–	375	–	375	–	400	–	400	–	500	–	600	–	ps	31, 33
	Input pulse width		^{t}IPW	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	^{t}CK	18, 32
	ACTIVATE-to-ACTIVATE delay, same bank		^{t}RC	54	–	55	–	55	–	54	–	55	–	55	–	55	–	ns	18, 34, 51
	ACTIVATE-to-READ or WRITE delay		^{t}RCD	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15	–	ns	18
	ACTIVATE-to-PRECHARGE delay		^{t}RAS	40	70K	40	70K	40	70K	40	70K	40	70K	40	70K	40	70K	ns	18, 34, 35
	PRECHARGE period		^{t}RP	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15	–	ns	18, 36
	PRE-CHARGE ALL period	<1Gb	^{t}RPA	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15	–	ns	18, 36
		≥1Gb	^{t}RPA	15	–	15	–	17.5		15		18		18.75		20		ns	18, 36
	ACTIVATE-to-ACTIVATE delay different bank	x4, x8	^{t}RRD	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	ns	18, 37
		x16	^{t}RRD	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns	18, 37
	4-bank activate period (≥1Gb)	x4, x8	^{t}FAW	35	–	35	–	35	–	37.5	–	37.5	–	37.5	–	37.5	–	ns	18, 38
		x16	^{t}FAW	45	–	45	–	45	–	50	–	50	–	50	–	50	–	ns	18, 38

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Command and Address	Internal READ-to-PRECHARGE delay	^tRTP	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	ns	18, 37, 39
Command and Address	CAS#-to-CAS# delay	^tCCD	2	–	2	–	2	–	2	–	2	–	2	–	2	–	^tCK	18
Command and Address	Write recovery time	^tWR	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns	18, 37
Command and Address	Write AP recovery + precharge time	^tDAL	$^tWR + ^tRP$	–	$^tWR + ^tRP$	–	$^tWR + ^tRP$	–	$^tWR + ^tRP$	–	$^tWR + ^tRP$	–	$^tWR + ^tRP$	–	$^tWR + ^tRP$	–	ns	40
Command and Address	Internal WRITE-to-READ delay	^tWTR	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	10	–	ns	18, 37
Command and Address	LOAD MODE cycle time	^tMRD	2	–	2	–	2	–	2	–	2	–	2	–	2	–	^tCK	18
Refresh	REFRESH-to-ACTIVATE or to -REFRESH interval – 256Mb	^tRFC	75	–	75	–	75	–	75	–	75	–	75	–	75	–	ns	18, 41
Refresh	REFRESH-to-ACTIVATE or to -REFRESH interval – 512Mb	^tRFC	105	–	105	–	105	–	105	–	105	–	105	–	105	–	ns	18, 41
Refresh	REFRESH-to-ACTIVATE or to -REFRESH interval – 1Gb	^tRFC	127.5	–	127.5	–	127.5	–	127.5	–	127.5	–	127.5	–	127.5	–	ns	18, 41
Refresh	REFRESH-to-ACTIVATE or to -REFRESH interval – 2Gb	^tRFC	195	–	195	–	195	–	195	–	195	–	195	–	195	–	ns	18, 41
Refresh	Average periodic refresh (commercial)	^tREFI	–	7.8	–	7.8	–	7.8	–	7.8	–	7.8	–	7.8	–	7.8	µs	18, 41
Refresh	Average periodic refresh (industrial)	$^tREFI_{IT}$	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	µs	18, 41
Refresh	Average periodic refresh (automotive)	$^tREFI_{AT}$	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	µs	18, 41
	CKE LOW to CK, CK# uncertainty	^tDELAY	MIN limit = $^tIS + ^tCK + ^tIH$ MAX limit = n/a														ns	42

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-187E		-25E		-25		-3E		-3		-37E		-5E			
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Self Refresh	Exit SELF REFRESH to nonREAD command		^tXSNR	MIN limit = ^tRFC (MIN) + 10 MAX limit = n/a														ns	
Self Refresh	Exit SELF REFRESH to READ command		^tXSRD	MIN limit = 200 MAX limit = n/a														^tCK	18
Self Refresh	Exit SELF REFRESH timing reference		^tISXR	MIN limit = ^tIS MAX limit = n/a														ps	33, 43
Power-Down	Exit active power-down to READ command	MR12 = 0	^tXARD	3	–	2	–	2	–	2	–	2	–	2	–	2	–	^tCK	18
Power-Down	Exit active power-down to READ command	MR12 = 1	^tXARD	10 - AL	–	8 - AL	–	8 - AL	–	7 - AL	–	7 - AL	–	6 - AL	–	6 - AL	–	^tCK	18
Power-Down	Exit precharge power-down and active power-down to any nonREAD command		^tXP	3	–	2	–	2	–	2	–	2	–	2	–	2	–	^tCK	18
Power-Down	CKE MIN HIGH/LOW time		^tCKE	MIN = 3 MAX = n/a														^tCK	18, 44

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to the entire table; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E			
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
ODT	ODT to power-down entry latency	^tANPD	4	–	3	–	3	–	3	–	3	–	3	–	3	–	^tCK	18
ODT	ODT power-down exit latency	^tAXPD	11	–	8	–	8	–	8	–	8	–	8	–	8	–	^tCK	18
ODT	ODT turn-on delay	^tAOND	2														^tCK	18
ODT	ODT turn-off delay	^tAOFD	2.5														^tCK	18, 45
ODT	ODT turn-on	^tAON	^tAC (MIN)	^tAC (MAX) + 2575	MIN = ^tAC (MIN) MAX = ^tAC (MAX) + 600				MIN = ^tAC (MIN) MAX = ^tAC (MAX) + 700				MIN = ^tAC (MIN) MAX = ^tAC (MAX) + 1000				ps	19, 46
ODT	ODT turn-off	^tAOF	MIN = ^tAC (MIN) MAX = ^tAC (MAX) + 600														ps	47, 48
ODT	ODT turn-on (power-down mode)	^tAONPD	^tAC (MIN) + 2000	2 × ^tCK + ^tAC (MAX) + 1000	MIN = ^tAC (MIN) + 2000 MAX = 2 × ^tCK + ^tAC (MAX) + 1000												ps	49
ODT	ODT turn-off (power-down mode)	^tAOFPD	MIN = ^tAC (MIN) + 2000 MAX = 2.5 × ^tCK + ^tAC (MAX) + 1000														ps	
ODT	ODT enable from MRS command	^tMOD	MIN = 12 MAX = n/a														ns	18, 50

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Notes:

1. All voltages are referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the operation of the device are warranted for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Outputs measured with equivalent load (see Figure 16 (page 51)).
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment, and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0 V/ns for signals in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$. Slew rates other than 1.0 V/ns may require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
7. Operating frequency is only allowed to change during self refresh mode (see Figure 79 (page 126)), precharge power-down mode, or system reset condition (see Reset (page 127)). SSC allows for small deviations in operating frequency, provided the SSC guidelines are satisfied.
8. The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK (AVG) MIN is the smallest clock rate allowed (except for a deviation due to allowed clock jitter). Input clock jitter is allowed provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
9. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range 8–60 kHz with an additional one percent ^{t}CK (AVG); however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN or above ^{t}CK (AVG) MAX.
10. MIN (^{t}CL, ^{t}CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; ^{t}CH (AVG) and ^{t}CL (AVG) must be met with or without clock jitter and with or without duty cycle jitter. ^{t}CH (AVG) and ^{t}CL (AVG) are the average of any 200 consecutive CK falling edges. ^{t}CH limits may be exceeded if the duty cycle jitter is small enough that the absolute half period limits (^{t}CH [ABS], ^{t}CL [ABS]) are not violated.
11. ^{t}HP (MIN) is the lesser of ^{t}CL and ^{t}CH actually applied to the device CK and CK# inputs; thus, ^{t}HP (MIN) ≥ the lesser of ^{t}CL (ABS) MIN and ^{t}CH (ABS) MIN.
12. The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less those than noted in the table (DLL locked).
13. The half-period jitter (^{t}JITdty) applies to either the high pulse of clock or the low pulse of clock; however, the two cumulatively can not exceed ^{t}JITper.
14. The cycle-to-cycle jitter (^{t}JITcc) is the amount the clock period can deviate from one cycle to the next. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than those noted in the table (DLL locked).
15. The cumulative jitter error ($^{t}ERR_{nper}$), where *n* is 2, 3, 4, 5, 6–10, or 11–50 is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
16. JEDEC specifies using $^{t}ERR_{6-10per}$ when derating clock-related output timing (see notes 19 and 48). Micron requires less derating by allowing $^{t}ERR_{5per}$ to be used.
17. This parameter is not referenced to a specific voltage level but is specified when the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).

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18. The inputs to the DRAM must be aligned to the associated clock, that is, the actual clock that latches it in. However, the input timing (in ns) references to the ^{t}CK (AVG) when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the ^{t}CK (AVG) rather than ^{t}CK: ^{t}IPW, ^{t}DIPW, ^{t}DQSS, ^{t}DQSH, ^{t}DQSL, ^{t}DSS, ^{t}DSH, ^{t}WPST, and ^{t}WPRE.
19. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}ERR_{5per}$ (MAX): ^{t}AC (MIN), ^{t}DQSCK (MIN), $^{t}LZ_{DQS}$ (MIN), $^{t}LZ_{DQ}$ (MIN), ^{t}AON (MIN); while the following parameters are required to be derated by subtracting $^{t}ERR_{5per}$ (MIN): ^{t}AC (MAX), ^{t}DQSCK (MAX), ^{t}HZ (MAX), $^{t}LZ_{DQS}$ (MAX), $^{t}LZ_{DQ}$ (MAX), ^{t}AON (MAX). The parameter ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX), is derated by subtracting ^{t}JITper (MIN). The parameter ^{t}RPST (MIN) is derated by subtracting ^{t}JITdty (MAX), while ^{t}RPST (MAX), is derated by subtracting ^{t}JITdty (MIN). Output timings that require $^{t}ERR_{5per}$ derating can be observed to have offsets relative to the clock; however, the total window will not degrade.
20. When DQS is used single-ended, the minimum limit is reduced by 100ps.
21. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
22. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
23. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
24. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
25. The intent of the "Don't Care" state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above $V_{IH[DC]min}$), then it must not transition LOW (below $V_{IH[DC]}$) prior to ^{t}DQSH (MIN).
26. Referenced to each output group: x4 = DQS with DQ[3:0]; x8 = DQS with DQ[7:0]; x16 = LDQS with DQ[7:0]; and UDQS with DQ[15:8].
27. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
28. ^{t}QH = ^{t}HP - ^{t}QHS; the worst case ^{t}QH would be the lesser of ^{t}CL (ABS) MAX or ^{t}CH (ABS) MAX times ^{t}CK (ABS) MIN - ^{t}QHS. Minimizing the amount of ^{t}CH (AVG) offset and value of ^{t}JITdty will provide a larger ^{t}QH, which in turn will provide a larger valid data out window.
29. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
30. The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew rate of 2 V/ns (1 V/ns for each signal). There are two sets of values listed: $^{t}DS_a$, $^{t}DH_a$ and $^{t}DS_b$, $^{t}DH_b$. The $^{t}DS_a$, $^{t}DH_a$ values (for reference only) are equivalent to the baseline values of $^{t}DS_b$, $^{t}DH_b$ at V_{REF} when the slew rate is 2 V/ns, differentially. The baseline values, $^{t}DS_b$, $^{t}DH_b$, are the JEDEC-defined values, referenced from the logic trip points. $^{t}DS_b$ is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while $^{t}DH_b$ is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated by adding the values from Table 31 (page 64) and Table 32 (page 65). If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended and the baseline values must be derated using

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Table 33 (page 66). Single-ended DQS data timing is referenced at DQS crossing V_{REF}. The correct timing values for a single-ended DQS strobe are listed in Table 34 (page 66)–Table 36 (page 67) on Table 34 (page 66), Table 35 (page 67), and Table 36 (page 67); listed values are already derated for slew rate variations and converted from baseline values to V_{REF} values.

31. V_{IL}/V_{IH} DDR2 overshoot/undershoot. See AC Overshoot/Undershoot Specification (page 57).
32. For each input signal—not the group collectively.
33. There are two sets of values listed for command/address: ^tIS_a, ^tIH_a and ^tIS_b, ^tIH_b. The ^tIS_a, ^tIH_a values (for reference only) are equivalent to the baseline values of ^tIS_b, ^tIH_b at V_{REF} when the slew rate is 1 V/ns. The baseline values, ^tIS_b, ^tIH_b, are the JEDEC-defined values, referenced from the logic trip points. ^tIS_b is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while ^tIH_b is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal. If the command/address slew rate is not equal to 1 V/ns, then the baseline values must be derated by adding the values from Table 29 (page 60) and Table 30 (page 61).
34. This is applicable to READ cycles only. WRITE cycles generally require additional time due to ^tWR during auto precharge.
35. READs and WRITEs with auto precharge *are* allowed to be issued before ^tRAS (MIN) is satisfied because ^tRAS lockout feature is supported in DDR2 SDRAM.
36. When a single-bank PRECHARGE command is issued, ^tRP timing applies. ^tRPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks open. For 8-bank devices (≥1Gb), ^tRPA (MIN) = ^tRP (MIN) + ^tCK (AVG) (Table 12 (page 33) lists ^tRP [MIN] + ^tCK [AVG] MIN).
37. This parameter has a two clock minimum requirement at any ^tCK.
38. The ^tFAW (MIN) parameter applies to all 8-bank DDR2 devices. No more than four bank-ACTIVATE commands may be issued in a given ^tFAW (MIN) period. ^tRRD (MIN) restriction still applies.
39. The minimum internal READ-to-PRECHARGE time. This is the time from which the last 4-bit prefetch begins to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when $^tRTP/(2 \times {}^tCK) > 1$, such as frequencies faster than 533 MHz when ^tRTP = 7.5ns. If $^tRTP/(2 \times {}^tCK) \leq 1$, then equation AL + BL/2 applies. ^tRAS (MIN) has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^tRAS (MIN) has been satisfied.
40. $^tDAL = (nWR) + (^tRP/^tCK)$. Each of these terms, if not already an integer, should be rounded up to the next integer. ^tCK refers to the application clock period; *n*WR refers to the ^tWR parameter stored in the MR9–MR11. For example, -37E at ^tCK = 3.75ns with ^tWR programmed to four clocks would have ^tDAL = 4 + (15ns/3.75ns) clocks = 4 + (4) clocks = 8 clocks.
41. The refresh period is 64ms (commercial) or 32ms (industrial and automotive). This equates to an average refresh rate of 7.8125µs (commercial) or 3.9607µs (industrial and automotive). To ensure all rows of all banks are properly refreshed, 8192 REFRESH commands must be issued every 64ms (commercial) or 32ms (industrial and automotive). The JEDEC ^tRFC MAX of 70,000ns is not required as bursting of AUTO REFRESH commands is allowed.
42. ^tDELAY is calculated from $^tIS + {}^tCK + {}^tIH$ so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition (see Reset (page 127)).
43. ^tISXR is equal to ^tIS and is used for CKE setup time during self refresh exit, as shown in Figure 69 (page 118).
44. ^tCKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $^tIS + 2 \times {}^tCK + {}^tIH$.

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45. The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47, for ^{t}AOF (MIN) and 2.5 + 0.03, or 2.53, for ^{t}AOF (MAX).
46. ODT turn-on time ^{t}AON (MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
47. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in High-Z. Both are measured from ^{t}AOFD.
48. Half-clock output parameters must be derated by the actual $^{t}ERR_{5per}$ and ^{t}JITdty when input clock jitter is present; this will result in each parameter becoming larger. The parameter ^{t}AOF (MIN) is required to be derated by subtracting both $^{t}ERR_{5per}$ (MAX) and ^{t}JITdty (MAX). The parameter ^{t}AOF (MAX) is required to be derated by subtracting both $^{t}ERR_{5per}$ (MIN) and ^{t}JITdty (MIN).
49. The -187E maximum limit is 2 × ^{t}CK + ^{t}AC (MAX) + 1000 but it will likely be 3 x ^{t}CK + ^{t}AC (MAX) + 1000 in the future.
50. Should use 8 ^{t}CK for backward compatibility.
51. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

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AC and DC Operating Conditions

Table 13: Recommended DC Operating Conditions (SSTL_18)

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1, 2
V_{DDL} supply voltage	V_{DDL}	1.7	1.8	1.9	V	2, 3
I/O supply voltage	V_{DDQ}	1.7	1.8	1.9	V	2, 3
I/O reference voltage	$V_{REF(DC)}$	0.49 × V_{DDQ}	0.50 × V_{DDQ}	0.51 × V_{DDQ}	V	4
I/O termination voltage (system)	V_{TT}	$V_{REF(DC)}$ - 40	$V_{REF(DC)}$	$V_{REF(DC)}$ + 40	mV	5

Notes:
1. V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be ≤ V_{DD}.
2. $V_{SSQ} = V_{SSL} = V_{SS}$.
3. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.
4. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of $V_{REF(DC)}$. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

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ODT DC Electrical Characteristics

Table 14: ODT DC Electrical Characteristics

All voltages are referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
R_{TT} effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1, 2
R_{TT} effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1, 2
R_{TT} effective impedance value for 50Ω setting EMR (A6, A2) = 1, 1	$R_{TT3(EFF)}$	40	50	60	Ω	1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	–6	–	6	%	3

Notes:

1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(DC)}$ to the ball being tested, and then measuring current, $I(V_{IH[AC]})$, and $I(V_{IL[AC]})$, respectively.

$$R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

2. Minimum IT and AT device values are derated by six percent less when the devices operate between –40°C and 0°C (T_C).
3. Measure voltage (VM) at tested ball with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DD}Q} - 1\right) \times 100$$

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Input Electrical Characteristics and Operating Conditions

Table 15: Input DC Logic Levels

All voltages are referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input high (logic 1) voltage	$V_{IH(DC)}$	$V_{REF(DC)}$ + 125	V_{DDQ}[1]	mV
Input low (logic 0) voltage	$V_{IL(DC)}$	–300	$V_{REF(DC)}$ - 125	mV

Note: 1. V_{DDQ} + 300mV allowed provided 1.9V is not exceeded.

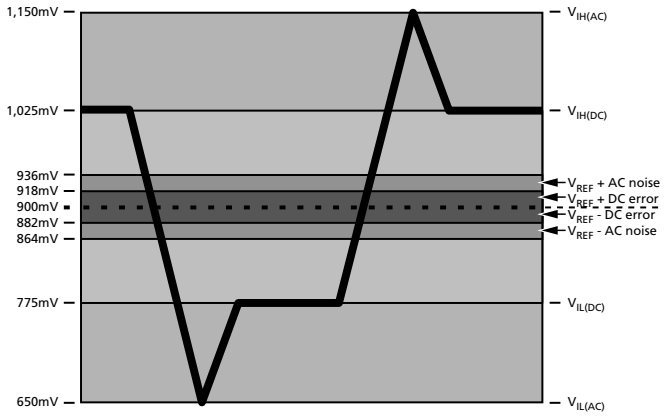
Table 16: Input AC Logic Levels

All voltages are referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input high (logic 1) voltage (-37E/-5E)	$V_{IH(AC)}$	$V_{REF(DC)}$ + 250	V_{DDQ}[1]	mV
Input high (logic 1) voltage (-187E/-25E/-25/-3E/-3)	$V_{IH(AC)}$	$V_{REF(DC)}$ + 200	V_{DDQ}[1]	mV
Input low (logic 0) voltage (-37E/-5E)	$V_{IL(AC)}$	–300	$V_{REF(DC)}$ - 250	mV
Input low (logic 0) voltage (-187E/-25E/-25/-3E/-3)	$V_{IL(AC)}$	–300	$V_{REF(DC)}$ - 200	mV

Note: 1. Refer to AC Overshoot/Undershoot Specification (page 57).

Figure 13: Single-Ended Input Signal Levels



Note: 1. Numbers in diagram reflect nominal DDR2-400/DDR2-533 values.

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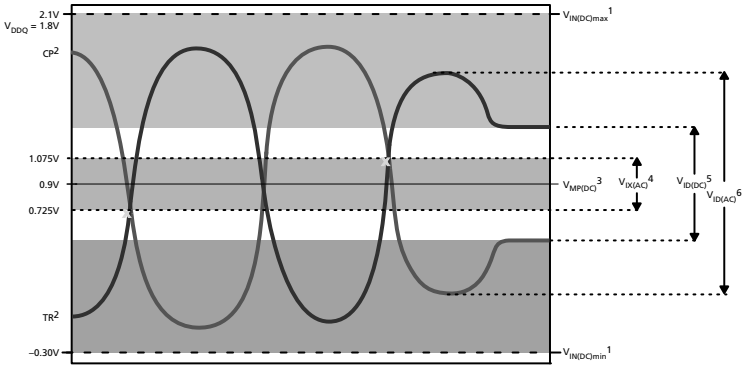
Table 17: Differential Input Logic Levels

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
DC input signal voltage	$V_{IN(DC)}$	–300	V_{DDQ}	mV	1, 6
DC differential input voltage	$V_{ID(DC)}$	250	V_{DDQ}	mV	2, 6
AC differential input voltage	$V_{ID(AC)}$	500	V_{DDQ}	mV	3, 6
AC differential cross-point voltage	$V_{IX(AC)}$	$0.50 \times V_{DDQ} - 175$	$0.50 \times V_{DDQ} + 175$	mV	4
Input midpoint voltage	$V_{MP(DC)}$	850	950	mV	5

Notes:
1. $V_{IN(DC)}$ specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
2. $V_{ID(DC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#) level. The minimum value is equal to $V_{IH(DC)} - V_{IL(DC)}$. Differential input signal levels are shown in Figure 14.
3. $V_{ID(AC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#) level. The minimum value is equal to $V_{IH(AC)} - V_{IL(AC)}$, as shown in Table 16 (page 47).
4. The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and $V_{IX(AC)}$ is expected to track variations in V_{DDQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross, as shown in Figure 14.
5. $V_{MP(DC)}$ specifies the input differential common mode voltage $(V_{TR} + V_{CP})/2$ where V_{TR} is the true input (CK, DQS) level and V_{CP} is the complementary input (CK#, DQS#). $V_{MP(DC)}$ is expected to be approximately $0.5 \times V_{DDQ}$.
6. V_{DDQ} + 300mV allowed provided 1.9V is not exceeded.

Figure 14: Differential Input Signal Levels



Notes:
1. TR and CP may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
2. TR represents the CK, DQS, RDQS, LDQS, and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS#, and UDQS# signals.
3. This provides a minimum of 850mV to a maximum of 950mV and is expected to be $V_{DDQ}/2$.
4. TR and CP must cross in this region.
5. TR and CP must meet at least $V_{ID(DC)min}$ when static and is centered around $V_{MP(DC)}$.
6. TR and CP must have a minimum 500mV peak-to-peak swing.

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7. Numbers in diagram reflect nominal values (V_{DDQ} = 1.8V).

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Output Electrical Characteristics and Operating Conditions

Table 18: Differential AC Output Parameters

Parameter	Symbol	Min	Max	Units	Notes
AC differential cross-point voltage	$V_{OX(AC)}$	0.50 × V_{DDQ} - 125	0.50 × V_{DDQ} + 125	mV	1

Note: 1. The typical value of $V_{OX(AC)}$ is expected to be about 0.5 × V_{DDQ} of the transmitting device and $V_{OX(AC)}$ is expected to track variations in V_{DDQ}. $V_{OX(AC)}$ indicates the voltage at which differential output signals must cross.

Figure 15: Differential Output Signal Levels

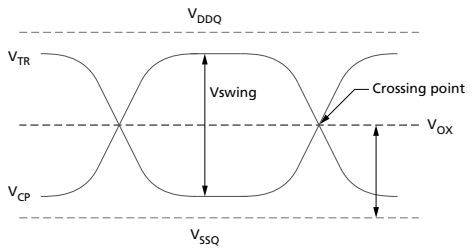

Table 19: Output DC Current Drive

Parameter	Symbol	Value	Units	Notes
Output MIN source DC current	I_{OH}	–13.4	mA	1, 2, 4
Output MIN sink DC current	I_{OL}	13.4	mA	2, 3, 4

Notes:
1. For $I_{OH(DC)}$; V_{DDQ} = 1.7V, V_{OUT} = 1,420mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV.
2. For $I_{OL(DC)}$; V_{DDQ} = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of $I_{OH(DC)}$ and $I_{OL(DC)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure $V_{IH,min}$ plus a noise margin and $V_{IL,max}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

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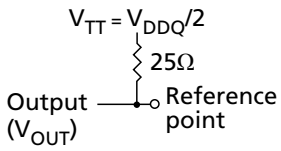
Table 20: Output Characteristics

Parameter	Min	Nom	Max	Units	Notes
Output impedance	See Output Driver Characteristics (page 52)			Ω	1, 2
Pull-up and pull-down mismatch	0	–	4	Ω	1, 2, 3
Output slew rate	1.5	–	5	V/ns	1, 4, 5, 6

Notes:
1. Absolute specifications: 0°C ≤ T_C ≤ +85°C; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V.
2. Impedance measurement conditions for output source DC current: V_{DDQ} = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - V_{DDQ})/I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. The impedance measurement condition for output sink DC current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is an absolute value between pull-up and pull-down; both are measured at the same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single-ended signals. For differential signals (DQS, DQS#), output slew rate is measured between DQS - DQS# = –500mV and DQS# - DQS = 500mV. Output slew rate is guaranteed by design but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from $V_{IL(DC)max}$ to $V_{IH(DC)min}$ is equal to or greater than the slew rate as measured from $V_{IL(AC)max}$ to $V_{IH(AC)min}$. This is guaranteed by design and characterization.
6. IT and AT devices require an additional 0.4 V/ns in the MAX limit when T_C is between –40°C and 0°C.

Figure 16: Output Slew Rate Load



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Output Driver Characteristics

Figure 17: Full Strength Pull-Down Characteristics

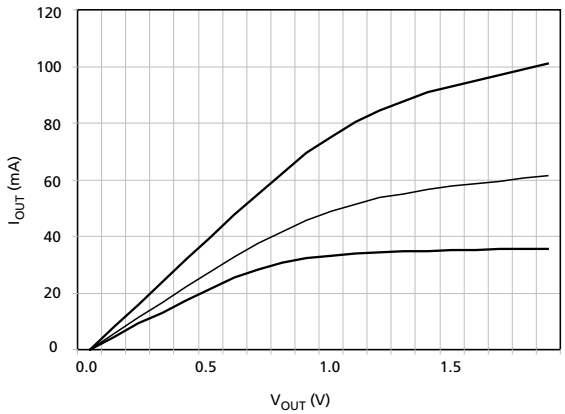

Table 21: Full Strength Pull-Down Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	4.30	5.63	7.95
0.2	8.60	11.30	15.90
0.3	12.90	16.52	23.85
0.4	16.90	22.19	31.80
0.5	20.40	27.59	39.75
0.6	23.28	32.39	47.70
0.7	25.44	36.45	55.55
0.8	26.79	40.38	62.95
0.9	27.67	44.01	69.55
1.0	28.38	47.01	75.35
1.1	28.96	49.63	80.35
1.2	29.46	51.71	84.55
1.3	29.90	53.32	87.95
1.4	30.29	54.9	90.70
1.5	30.65	56.03	93.00
1.6	30.98	57.07	95.05
1.7	31.31	58.16	97.05
1.8	31.64	59.27	99.05
1.9	31.96	60.35	101.05

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Figure 18: Full Strength Pull-Up Characteristics

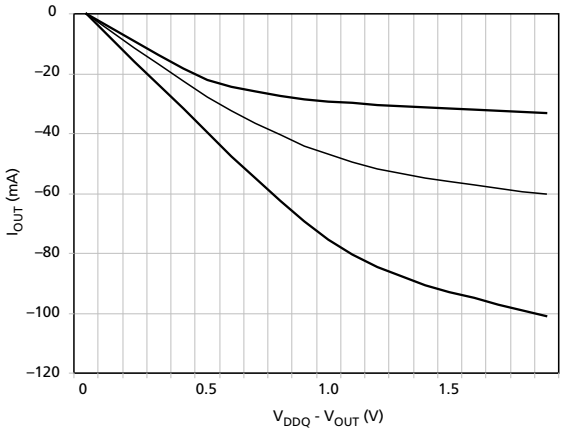

Table 22: Full Strength Pull-Up Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	–4.30	–5.63	–7.95
0.2	–8.60	–11.30	–15.90
0.3	–12.90	–16.52	–23.85
0.4	–16.90	–22.19	–31.80
0.5	–20.40	–27.59	–39.75
0.6	–23.28	–32.39	–47.70
0.7	–25.44	–36.45	–55.55
0.8	–26.79	–40.38	–62.95
0.9	–27.67	–44.01	–69.55
1.0	–28.38	–47.01	–75.35
1.1	–28.96	–49.63	–80.35
1.2	–29.46	–51.71	–84.55
1.3	–29.90	–53.32	–87.95
1.4	–30.29	–54.90	–90.70
1.5	–30.65	–56.03	–93.00
1.6	–30.98	–57.07	–95.05
1.7	–31.31	–58.16	–97.05
1.8	–31.64	–59.27	–99.05
1.9	–31.96	–60.35	–101.05

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Figure 19: Reduced Strength Pull-Down Characteristics

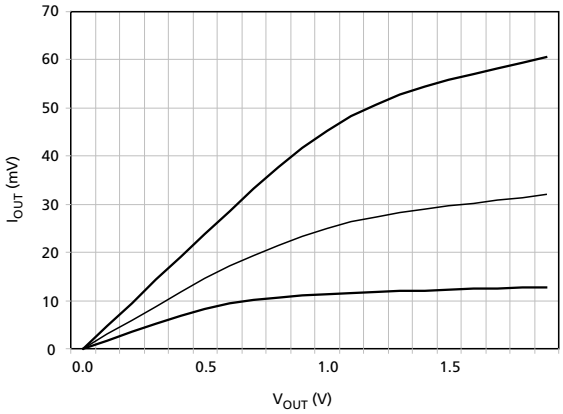

Table 23: Reduced Strength Pull-Down Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	1.72	2.98	4.77
0.2	3.44	5.99	9.54
0.3	5.16	8.75	14.31
0.4	6.76	11.76	19.08
0.5	8.16	14.62	23.85
0.6	9.31	17.17	28.62
0.7	10.18	19.32	33.33
0.8	10.72	21.40	37.77
0.9	11.07	23.32	41.73
1.0	11.35	24.92	45.21
1.1	11.58	26.30	48.21
1.2	11.78	27.41	50.73
1.3	11.96	28.26	52.77
1.4	12.12	29.10	54.42
1.5	12.26	29.70	55.80
1.6	12.39	30.25	57.03
1.7	12.52	30.82	58.23
1.8	12.66	31.41	59.43
1.9	12.78	31.98	60.63

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Figure 20: Reduced Strength Pull-Up Characteristics

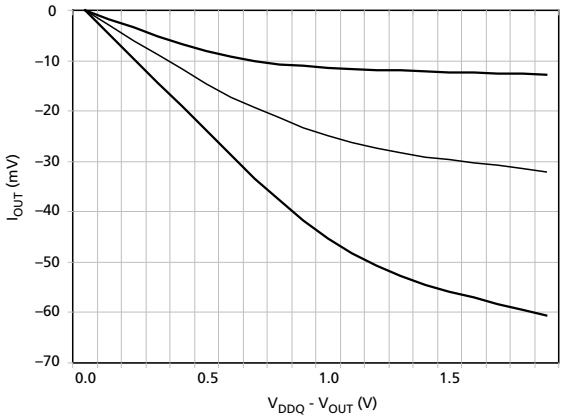

Table 24: Reduced Strength Pull-Up Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	–1.72	–2.98	–4.77
0.2	–3.44	–5.99	–9.54
0.3	–5.16	–8.75	–14.31
0.4	–6.76	–11.76	–19.08
0.5	–8.16	–14.62	–23.85
0.6	–9.31	–17.17	–28.62
0.7	–10.18	–19.32	–33.33
0.8	–10.72	–21.40	–37.77
0.9	–11.07	–23.32	–41.73
1.0	–11.35	–24.92	–45.21
1.1	–11.58	–26.30	–48.21
1.2	–11.78	–27.41	–50.73
1.3	–11.96	–28.26	–52.77
1.4	–12.12	–29.10	–54.42
1.5	–12.26	–29.69	–55.8
1.6	–12.39	–30.25	–57.03
1.7	–12.52	–30.82	–58.23
1.8	–12.66	–31.42	–59.43
1.9	–12.78	–31.98	–60.63

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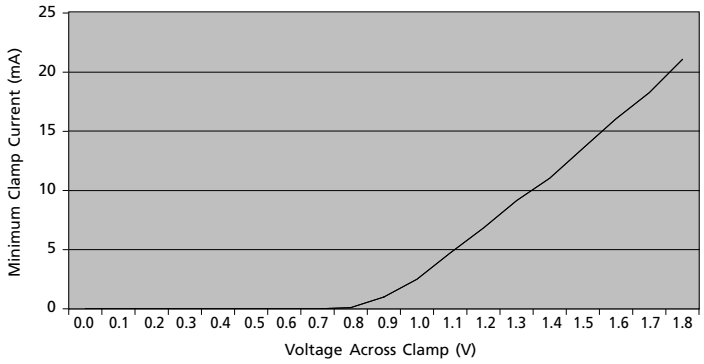
Power and Ground Clamp Characteristics

Power and ground clamps are provided on the following input-only balls: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, ODT, and CKE.

Table 25: Input Clamp Characteristics

Voltage Across Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Figure 21: Input Clamp Characteristics



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AC Overshoot/Undershoot Specification

Table 26: Address and Control Balls

Applies to address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, and ODT

Parameter	Specification				
	-187E	-25/-25E	-3/-3E	-37E	-5E
Maximum peak amplitude allowed for overshoot area (see Figure 22)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum peak amplitude allowed for undershoot area (see Figure 23)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum overshoot area above V_{DD} (see Figure 22)	0.5 Vns	0.66 Vns	0.80 Vns	1.00 Vns	1.33 Vns
Maximum undershoot area below V_{SS} (see Figure 23)	0.5 Vns	0.66 Vns	0.80 Vns	1.00 Vns	1.33 Vns

Table 27: Clock, Data, Strobe, and Mask Balls

Applies to DQ, DQS, DQS#, RDQS, RDQS#, UDQS, UDQS#, LDQS, LDQS#, DM, UDM, and LDM

Parameter	Specification				
	-187E	-25/-25E	-3/-3E	-37E	-5E
Maximum peak amplitude allowed for overshoot area (see Figure 22)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum peak amplitude allowed for undershoot area (see Figure 23)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum overshoot area above V_{DDQ} (see Figure 22)	0.19 Vns	0.23 Vns	0.23 Vns	0.28 Vns	0.38 Vns
Maximum undershoot area below V_{SSQ} (see Figure 23)	0.19 Vns	0.23 Vns	0.23 Vns	0.28 Vns	0.38 Vns

Figure 22: Overshoot

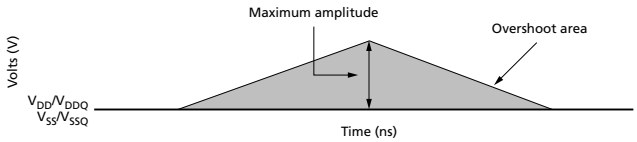

Figure 23: Undershoot

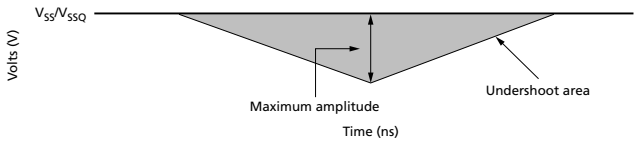

Table 28: AC Input Test Conditions

Parameter	Symbol	Min	Max	Units	Notes
Input setup timing measurement reference level address balls, bank address balls, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	V_{RS}	See Note 2			1, 2, 3, 4

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Table 28: AC Input Test Conditions (Continued)

Parameter	Symbol	Min	Max	Units	Notes
Input hold timing measurement reference level address balls, bank address balls, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	V_{RH}	See Note 5			1, 3, 4, 5
Input timing measurement reference level (single-ended) DQS for x4, x8; UDQS, LDQS for x16	$V_{REF(DC)}$	$V_{DDQ} \times 0.49$	$V_{DDQ} \times 0.51$	V	1, 3, 4, 6
Input timing measurement reference level (differential) CK, CK# for x4, x8, x16; DQS, DQS# for x4, x8; RDQS, RDQS# for x8; UDQS, UDQS#, LDQS, LDQS# for x16	V_{RD}	$V_{IX(AC)}$		V	1, 3, 7, 8, 9

Notes:
1. All voltages referenced to V_{SS}.
2. Input waveform setup timing (^tIS_b) is referenced from the input signal crossing at the $V_{IH(AC)}$ level for a rising signal and $V_{IL(AC)}$ for a falling signal applied to the device under test, as shown in Figure 32 (page 70).
3. See Input Slew Rate Derating (page 59).
4. The slew rate for single-ended inputs is measured from DC level to AC level, $V_{IL(DC)}$ to $V_{IH(AC)}$ on the rising edge and $V_{IL(AC)}$ to $V_{IH(DC)}$ on the falling edge. For signals referenced to V_{REF}, the valid intersection is where the "tangent" line intersects V_{REF}, as shown in Figure 25 (page 62), Figure 27 (page 63), Figure 29 (page 68), and Figure 31 (page 69).
5. Input waveform hold (^tIH_b) timing is referenced from the input signal crossing at the $V_{IL(DC)}$ level for a rising signal and $V_{IH(DC)}$ for a falling signal applied to the device under test, as shown in Figure 32 (page 70).
6. Input waveform setup timing (^tDS) and hold timing (^tDH) for single-ended data strobe is referenced from the crossing of DQS, UDQS, or LDQS through the Vref level applied to the device under test, as shown in Figure 34 (page 71).
7. Input waveform setup timing (^tDS) and hold timing (^tDH) when differential data strobe is enabled is referenced from the cross-point of DQS/DQS#, UDQS/UDQS#, or LDQS/LDQS#, as shown in Figure 33 (page 70).
8. Input waveform timing is referenced to the crossing point level (V_{IX}) of two input signals (V_{TR} and V_{CP}) applied to the device under test, where V_{TR} is the true input signal and V_{CP} is the complementary input signal, as shown in Figure 35 (page 71).
9. The slew rate for differentially ended inputs is measured from twice the DC level to twice the AC level: $2 \times V_{IL(DC)}$ to $2 \times V_{IH(AC)}$ on the rising edge and $2 \times V_{IL(AC)}$ to $2 \times V_{IH(DC)}$ on the falling edge. For example, the CK/CK# would be –250mV to 500mV for CK rising edge and would be 250mV to –500mV for CK falling edge.

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Input Slew Rate Derating

For all input signals, the total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) value to the Δ^{t}IS and Δ^{t}IH derating value, respectively. Example: ^{t}IS (total setup time) = ^{t}IS (base) + Δ^{t}IS.

^{t}IS, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup nominal slew rate (^{t}IS) for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$.

If the actual signal is always earlier than the nominal slew rate line between shaded "$V_{REF(DC)}$ to AC region," use the nominal slew rate for the derating value (Figure 24 (page 62)).

If the actual signal is later than the nominal slew rate line anywhere between the shaded "$V_{REF(DC)}$ to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value (see Figure 25 (page 62)).

^{t}IH, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. ^{t}IH, nominal slew rate for a falling signal, is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$.

If the actual signal is always later than the nominal slew rate line between shaded "DC to $V_{REF(DC)}$ region," use the nominal slew rate for the derating value (Figure 26 (page 63)).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to $V_{REF(DC)}$ region," the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (Figure 27 (page 63)).

Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH(AC)}/V_{IL(AC)}$.

For slew rates in between the values listed in Table 29 (page 60) and Table 30 (page 61), the derating values may obtained by linear interpolation.

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Table 29: DDR2-400/533 Setup and Hold Time Derating Values (^{t}IS and ^{t}IH)

Command/Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	
4.0	187	94	217	124	247	154	ps
3.5	179	89	209	119	239	149	ps
3.0	167	83	197	113	227	143	ps
2.5	150	75	180	105	210	135	ps
2.0	125	45	155	75	185	105	ps
1.5	83	21	113	51	143	81	ps
1.0	0	0	30	30	60	60	ps
0.9	–11	–14	19	16	49	46	ps
0.8	–25	–31	5	–1	35	29	ps
0.7	–43	–54	–13	–24	17	6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

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Table 30: DDR2-667/800/1066 Setup and Hold Time Derating Values (^{t}IS and ^{t}IH)

Command/ Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	
4.0	150	94	180	124	210	154	ps
3.5	143	89	173	119	203	149	ps
3.0	133	83	163	113	193	143	ps
2.5	120	75	150	105	180	135	ps
2.0	100	45	160	75	160	105	ps
1.5	67	21	97	51	127	81	ps
1.0	0	0	30	30	60	60	ps
0.9	–5	–14	25	16	55	46	ps
0.8	–13	–31	17	–1	47	29	ps
0.7	–22	–54	8	–24	38	6	ps
0.6	–34	–83	–4	–53	36	–23	ps
0.5	–60	–125	–30	–95	0	–65	ps
0.4	–100	–188	–70	–158	–40	–128	ps
0.3	–168	–292	–138	–262	–108	–232	ps
0.25	–200	–375	–170	–345	–140	–315	ps
0.2	–325	–500	–295	–470	–265	–440	ps
0.15	–517	–708	–487	–678	–457	–648	ps
0.1	–1000	–1125	–970	–1095	–940	–1065	ps

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Figure 24: Nominal Slew Rate for ^{t}IS

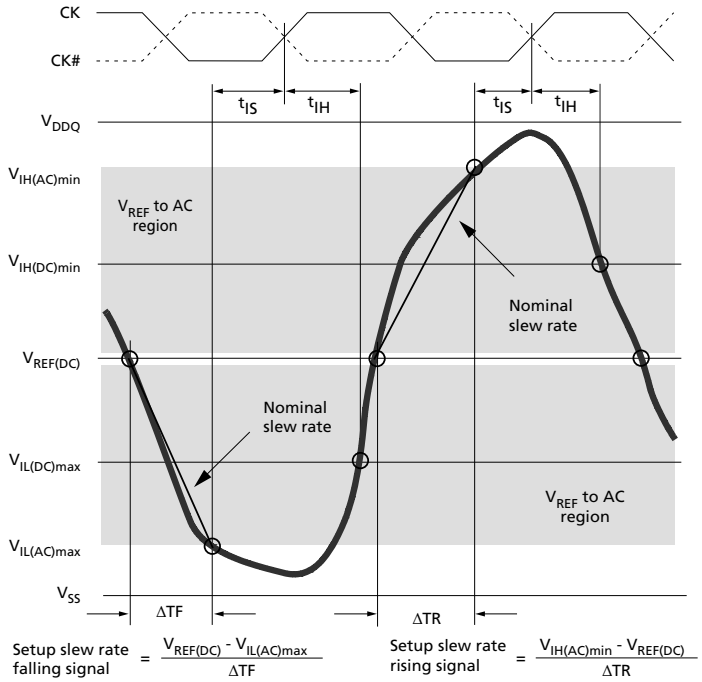

Figure 25: Tangent Line for ^{t}IS

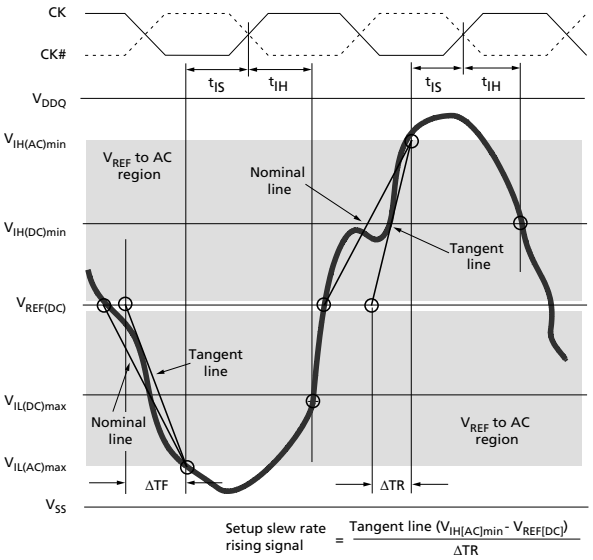

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Figure 26: Nominal Slew Rate for ^{t}IH

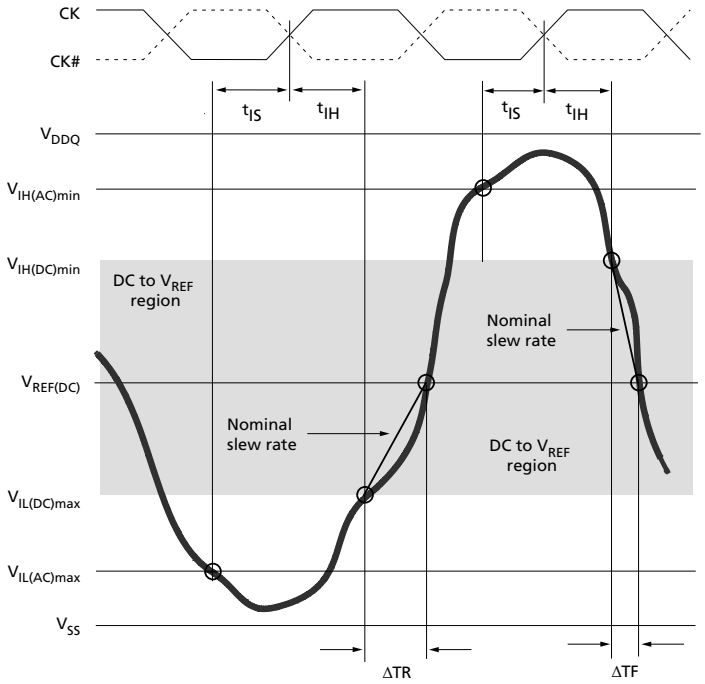
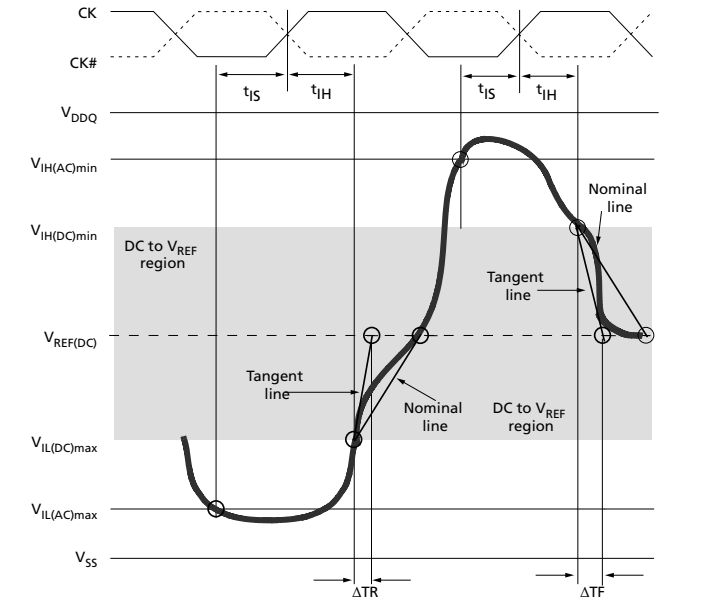


Figure 27: Tangent Line for ^{t}IH



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF[DC]} - V_{IL[DC]max})}{\Delta TR} \qquad \text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH[DC]min} - V_{REF[DC]})}{\Delta TF}$$

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Table 31: DDR2-400/533 ^{t}DS, ^{t}DH Derating Values with Differential Strobe

All units are shown in picoseconds

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH
2.0	125	45	125	45	125	45	–	–	–	–	–	–	–	–	–	–	–	–
1.5	83	21	83	21	83	21	95	33	–	–	–	–	–	–	–	–	–	–
1.0	0	0	0	0	0	0	12	12	24	24	–	–	–	–	–	–	–	–
0.9	–	–	–11	–14	–11	–14	1	–2	13	10	25	22	–	–	–	–	–	–
0.8	–	–	–	–	–25	–31	–13	–19	–1	–7	11	5	23	17	–	–	–	–
0.7	–	–	–	–	–	–	–31	–42	–19	–30	–7	–18	5	–6	17	6	–	–
0.6	–	–	–	–	–	–	–	–	–43	–59	–31	–47	–19	–35	–7	–23	5	–11
0.5	–	–	–	–	–	–	–	–	–	–	–74	–89	–62	–77	–50	–65	–38	–53
0.4	–	–	–	–	–	–	–	–	–	–	–	–	–127	–140	–115	–128	–103	–116

Notes:
1. For all input signals, the total ^{t}DS and ^{t}DH required is calculated by adding the data sheet value to the derating value listed in Table 31.
2. ^{t}DS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. ^{t}DS nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded "$V_{REF(DC)}$ to AC region," use the nominal slew rate for the derating value (see Figure 28 (page 68)). If the actual signal is later than the nominal slew rate line anywhere between the shaded "$V_{REF(DC)}$ to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value (see Figure 29 (page 68)).
3. ^{t}DH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. ^{t}DH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded "DC level to $V_{REF(DC)}$ region," use the nominal slew rate for the derating value (see Figure 30 (page 69)). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to $V_{REF(DC)}$ region," the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see Figure 31 (page 69)).
4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH(AC)}/V_{IL(AC)}$.
5. For slew rates between the values listed in this table, the derating values may be obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.
7. Single-ended DQS requires special derating. The values in Table 33 (page 66) are the DQS single-ended slew rate derating with DQS referenced at V_{REF} and DQ referenced at the logic levels $^{t}DS_b$ and $^{t}DH_b$. Converting the derated base values from DQ referenced to the AC/DC trip points to DQ referenced to V_{REF} is listed in Table 35 (page 67) and Table 36 (page 67). Table 35 provides the V_{REF}-based fully derated values for the DQ ($^{t}DS_a$ and $^{t}DH_a$) for DDR2-533. Table 36 provides the V_{REF}-based fully derated values for the DQ ($^{t}DS_a$ and $^{t}DH_a$) for DDR2-400.

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Table 32: DDR2-667/800/1066 ^{t}DS, ^{t}DH Derating Values with Differential Strobe

All units are shown in picoseconds

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72
0.9	–5	–14	–5	–14	–5	–14	7	–2	19	10	31	22	43	34	55	46	67	58
0.8	–13	–31	–13	–31	–13	–31	–1	–19	11	–7	23	5	35	17	47	29	59	41
0.7	–22	–54	–22	–54	–22	–54	–10	–42	2	–30	14	–18	26	–6	38	6	50	18
0.6	–34	–83	–34	–83	–34	–83	–22	–71	–10	–59	2	–47	14	–35	26	–23	38	–11
0.5	–60	–125	–60	–125	–60	–125	–48	–113	–36	–101	–24	–89	–12	–77	0	–65	12	–53
0.4	–100	–188	–100	–188	–100	–188	–88	–176	–76	–164	–64	–152	–52	–140	–40	–128	–28	–116

Notes:
1. For all input signals the total ^{t}DS and ^{t}DH required is calculated by adding the data sheet value to the derating value listed in Table 32.
2. ^{t}DS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. ^{t}DS nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded "$V_{REF(DC)}$ to AC region," use the nominal slew rate for the derating value (see Figure 28 (page 68)). If the actual signal is later than the nominal slew rate line anywhere between shaded "$V_{REF(DC)}$ to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value (see Figure 29 (page 68)).
3. ^{t}DH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. ^{t}DH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded "DC level to $V_{REF(DC)}$ region," use the nominal slew rate for the derating value (see Figure 30 (page 69)). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC to $V_{REF(DC)}$ region," the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see Figure 31 (page 69)).
4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH(AC)}/V_{IL(AC)}$.
5. For slew rates between the values listed in this table, the derating values may be obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.
7. Single-ended DQS requires special derating. The values in Table 33 (page 66) are the DQS single-ended slew rate derating with DQS referenced at V_{REF} and DQ referenced at the logic levels $^{t}DS_b$ and $^{t}DH_b$. Converting the derated base values from DQ referenced to the AC/DC trip points to DQ referenced to V_{REF} is listed in Table 34 (page 66). Table 34 provides the V_{REF}-based fully derated values for the DQ ($^{t}DS_a$ and $^{t}DH_a$) for

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DDR2-667. It is not advised to operate DDR2-800 and DDR2-1066 devices with single-ended DQS; however, Table 33 would be used with the base values.

Table 33: Single-Ended DQS Slew Rate Derating Values Using ^tDS_b and ^tDH_b

Reference points indicated in bold; Derating values are to be used with base ^tDS_b- and ^tDH_b-specified values

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH
2.0	130	53	130	53	130	53	130	53	130	53	145	48	155	45	165	41	175	38
1.5	97	32	97	32	97	32	97	32	97	32	112	27	122	24	132	20	142	17
1.0	30	–10	30	–10	30	–10	30	–10	30	–10	**45**	**–15**	55	–18	65	–22	75	–25
0.9	25	–24	25	–24	25	–24	25	–24	25	–24	40	–29	50	–32	60	–36	70	–39
0.8	17	–41	17	–41	17	–41	17	–41	17	–41	32	–46	42	–49	52	–53	61	–56
0.7	5	–64	5	–64	5	–64	5	–64	5	–64	20	–69	30	–72	40	–75	50	–79
0.6	–7	–93	–7	–93	–7	–93	–7	–93	–7	–93	8	–98	18	–102	28	–105	38	–108
0.5	–28	–135	–28	–135	–28	–135	–28	–135	–28	–135	–13	–140	–3	–143	7	–147	17	–150
0.4	–78	–198	–78	–198	–78	–198	–78	–198	–78	–198	–63	–203	–53	–206	–43	–210	–33	–213

Table 34: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at V_{REF}) at DDR2-667

Reference points indicated in bold

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH
2.0	330	291	330	291	330	291	330	291	330	291	345	286	355	282	365	29	375	276
1.5	330	290	330	290	330	290	330	290	330	290	345	285	355	282	365	279	375	275
1.0	330	290	330	290	330	290	330	290	330	290	**345**	**285**	355	282	365	278	375	275
0.9	347	290	347	290	347	290	347	290	347	290	362	285	372	282	382	278	392	275
0.8	367	290	367	290	367	290	367	290	367	290	382	285	392	282	402	278	412	275
0.7	391	290	391	290	391	290	391	290	391	290	406	285	416	281	426	278	436	275
0.6	426	290	426	290	426	290	426	290	426	290	441	285	451	282	461	278	471	275
0.5	472	290	472	290	472	290	472	290	472	290	487	285	497	282	507	278	517	275
0.4	522	289	522	289	522	289	522	289	522	289	537	284	547	281	557	278	567	274

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Table 35: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at V_{REF}) at DDR2-533

Reference points indicated in bold

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH
2.0	355	341	355	341	355	341	355	341	355	341	370	336	380	332	390	329	400	326
1.5	364	340	364	340	364	340	364	340	364	340	379	335	389	332	399	329	409	325
1.0	380	340	380	340	380	340	380	340	380	340	**395**	**335**	405	332	415	328	425	325
0.9	402	340	402	340	402	340	402	340	402	340	417	335	427	332	437	328	447	325
0.8	429	340	429	340	429	340	429	340	429	340	444	335	454	332	464	328	474	325
0.7	463	340	463	340	463	340	463	340	463	340	478	335	488	331	498	328	508	325
0.6	510	340	510	340	510	340	510	340	510	340	525	335	535	332	545	328	555	325
0.5	572	340	572	340	572	340	572	340	572	340	587	335	597	332	607	328	617	325
0.4	647	339	647	339	647	339	647	339	647	339	662	334	672	331	682	328	692	324

Table 36: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at V_{REF}) at DDR2-400

Reference points indicated in bold

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH	^tDS	^tDH
2.0	405	391	405	391	405	391	405	391	405	391	420	386	430	382	440	379	450	376
1.5	414	390	414	390	414	390	414	390	414	390	429	385	439	382	449	379	459	375
1.0	430	390	430	390	430	390	430	390	430	390	**445**	**385**	455	382	465	378	475	375
0.9	452	390	452	390	452	390	452	390	452	390	467	385	477	382	487	378	497	375
0.8	479	390	479	390	479	390	479	390	479	390	494	385	504	382	514	378	524	375
0.7	513	390	513	390	513	390	513	390	513	390	528	385	538	381	548	378	558	375
0.6	560	390	560	390	560	390	560	390	560	390	575	385	585	382	595	378	605	375
0.5	622	390	622	390	622	390	622	390	622	390	637	385	647	382	657	378	667	375
0.4	697	389	697	389	697	389	697	389	697	389	712	384	722	381	732	378	742	374

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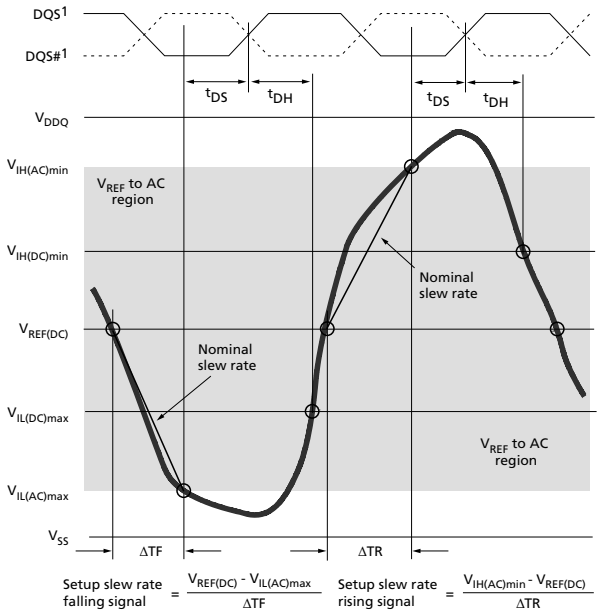
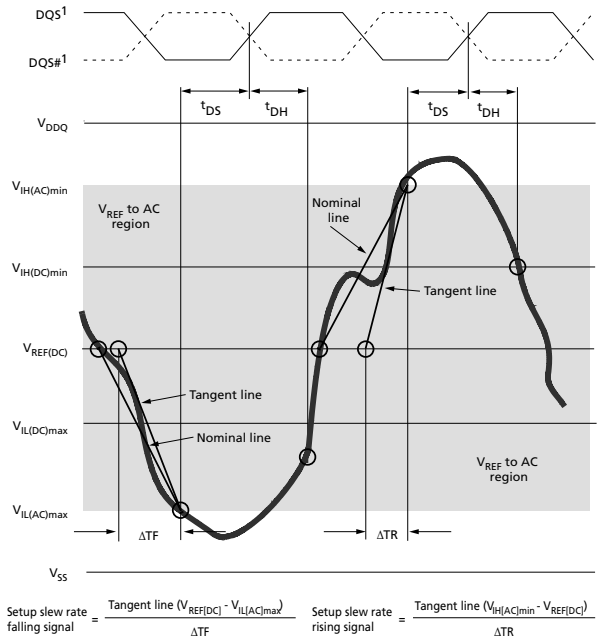
Figure 28: Nominal Slew Rate for ^{t}DS



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 29: Tangent Line for ^{t}DS



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

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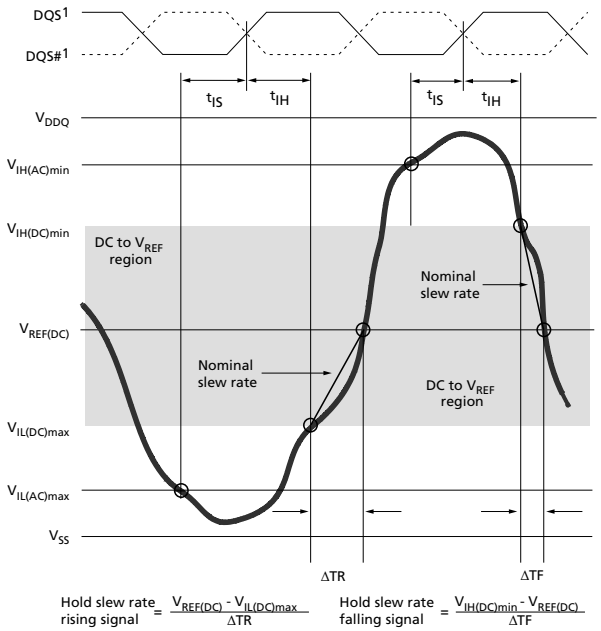
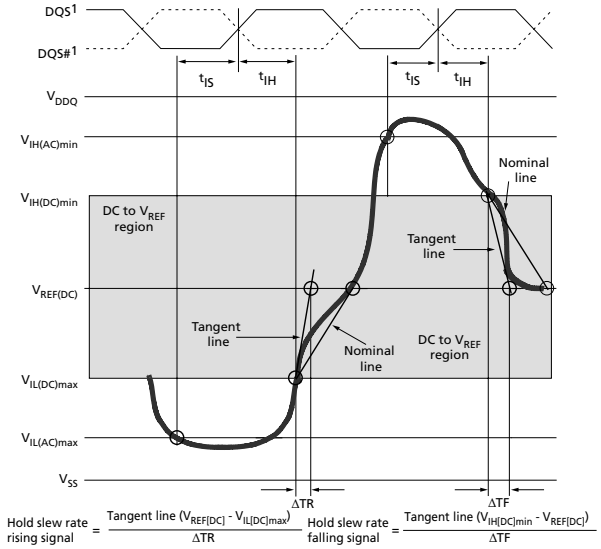
Figure 30: Nominal Slew Rate for ^{t}DH



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 31: Tangent Line for ^{t}DH



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

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Figure 32: AC Input Test Signal Waveform Command/Address Balls

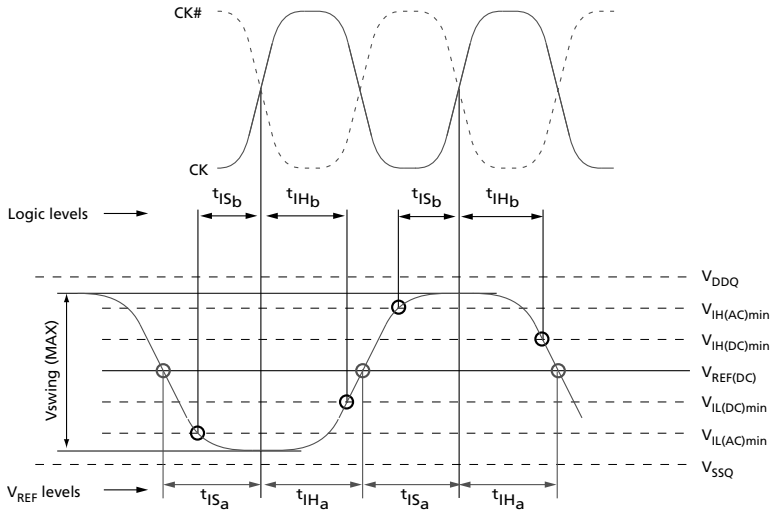

Figure 33: AC Input Test Signal Waveform for Data with DQS, DQS# (Differential)

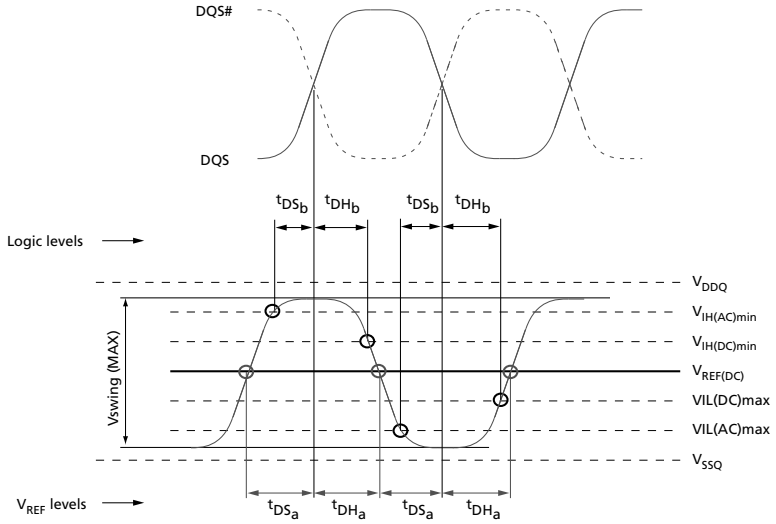

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Figure 34: AC Input Test Signal Waveform for Data with DQS (Single-Ended)

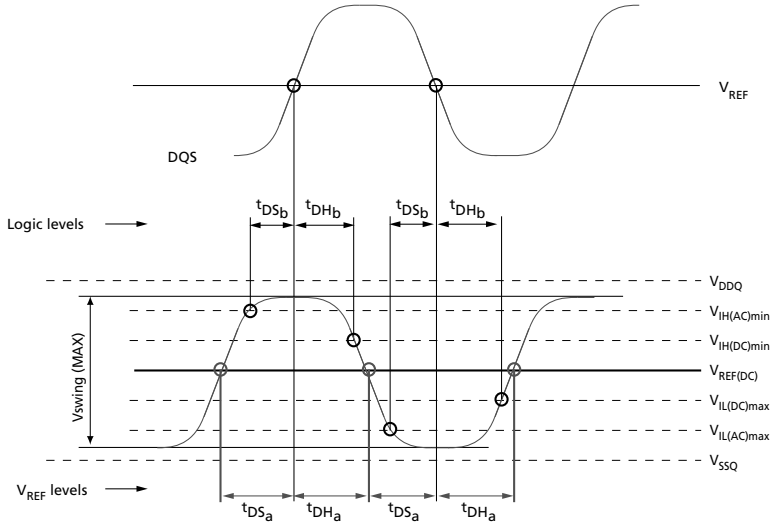
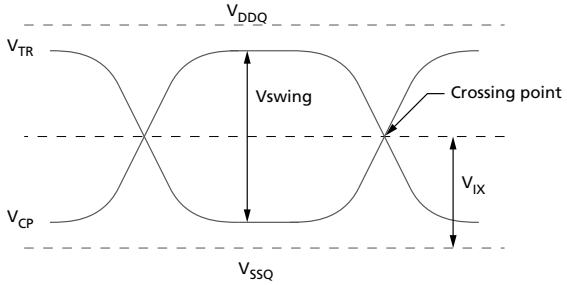


Figure 35: AC Input Test Signal Waveform (Differential)



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Commands

Truth Tables

The following tables provide a quick reference of available DDR2 SDRAM commands, including CKE power-down modes and bank-to-bank commands.

Table 37: Truth Table – DDR2 Commands

Notes: 1–3 apply to the entire table

Function	CKE Previous Cycle	CKE Current Cycle	CS#	RAS#	CAS#	WE#	BA2–BA0	*An*–A11	A10	A9–A0	Notes
LOAD MODE	H	H	L	L	L	L	BA	OP code			4, 6
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH exit	L	H	H	X	X	X	X	X	X	X	4, 7
			L	H	H	H					
Single bank PRECHARGE	H	H	L	L	H	L	BA	X	L	X	6
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank ACTIVATE	H	H	L	L	H	H	BA	Row address			4
WRITE	H	H	L	H	L	L	BA	Column address	L	Column address	4, 5, 6, 8
WRITE with auto precharge	H	H	L	H	L	L	BA	Column address	H	Column address	4, 5, 6, 8
READ	H	H	L	H	L	H	BA	Column address	L	Column address	4, 5, 6, 8
READ with auto precharge	H	H	L	H	L	H	BA	Column address	H	Column address	4, 5, 6, 8
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
Power-down entry	H	L	H	X	X	X	X	X	X	X	9
			L	H	H	H					
Power-down exit	L	H	H	X	X	X	X	X	X	X	9
			L	H	H	H					

Notes:
1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See ODT Timing (page 129) for details.
3. "X" means "H or L" (but a defined logic level) for valid I_{DD} measurements.
4. BA2 is only applicable for densities ≥1Gb.
5. An *n* is the most significant address bit for a given density and configuration. Some larger address bits may be "Don't Care" during column addressing, depending on density and configuration.

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6. Bank addresses (BA) determine which bank is to be operated upon. BA during a LOAD MODE command selects which mode register is programmed.
7. SELF REFRESH exit is asynchronous.
8. Burst reads or writes at BL = 4 cannot be terminated or interrupted. See Figure 49 (page 98) and Figure 61 (page 109) for other restrictions and details.
9. The power-down mode does not perform any REFRESH operations. The duration of power-down is limited by the refresh requirements outlined in the AC parametric section.

Table 38: Truth Table – Current State Bank *n* – Command to Bank *n*

Notes: 1–6 apply to the entire table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVATE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row active	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst)	8
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	9
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst)	8, 10
	L	L	H	L	PRECHARGE (start PRECHARGE)	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start new WRITE burst)	8
	L	L	H	L	PRECHARGE (start PRECHARGE)	9

Notes:
1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, ^{t}RP has been met, and any READ burst is complete.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated.

   Write: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.
4. The following states must not be interrupted by a command issued to the same bank. Issue DESELECT or NOP commands, or allowable commands to the other bank, on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to Table 39 (page 75).

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Precharge:	Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. After ^{t}RP is met, the bank will be in the idle state.
Read with auto precharge enabled:	Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.
Row activate:	Starts with registration of an ACTIVATE command and ends when ^{t}RCD is met. After ^{t}RCD is met, the bank will be in the row active state.
Write with auto precharge enabled:	Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command (DESELECT or NOP commands must be applied on each positive clock edge during these states):

Refresh:	Starts with registration of a REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the DDR2 SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of the LOAD MODE command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the DDR2 SDRAM will be in the all banks idle state.
Precharge all:	Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and bursts are not in progress.
8. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
9. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
10. A WRITE command may be applied after the completion of the READ burst.

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Table 39: Truth Table – Current State Bank *n* – Command to Bank *m*

Notes: 1–6 apply to the entire table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank *m*	
Row active, active, or precharge	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 9, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	

Notes:
1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table describes an alternate bank operation, except where noted (the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

Idle:	The bank has been precharged, ^{t}RP has been met, and any READ burst is complete.
Row active:	A row in the bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated with auto precharge disabled and has not yet terminated.
Write:	A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.

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READ with auto precharge enabled/ WRITE with auto precharge enabled: The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For WRITE with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (contention between read data and write data must be avoided).

The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized in Table 40 (page 76).

4. REFRESH and LOAD MODE commands may only be issued when all banks are idle.
5. Not used.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. A WRITE command may be applied after the completion of the READ burst.
9. Requires appropriate DM.
10. The number of clock cycles required to meet ^{t}WTR is either two or ^{t}WTR/^{t}CK, whichever is greater.

Table 40: Minimum Delay with Auto Precharge Enabled

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ with auto precharge	(CL - 1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2)	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK
READ with auto precharge	READ or READ with auto precharge	(BL/2)	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2) + 2	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected. DESELECT is also referred to as COMMAND INHIBIT.

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NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via bank address and address inputs. The bank address balls determine which mode register will be programmed. See Mode Register (MR) (page 78). The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the bank address inputs determines the bank, and the address inputs select the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the bank address inputs determine the bank, and the address provided on address inputs A0–A*i* (where A*i* is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the bank select inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location (see Figure 66 (page 114)).

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PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

REFRESH

REFRESH is used during normal operation of the DDR2 SDRAM and is analogous to CAS#-before-RAS# (CBR) REFRESH. All banks must be in the idle mode prior to issuing a REFRESH command. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including Vref) must be maintained at valid levels upon entry/exit *and* during SELF REFRESH operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh.

Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 36 (page 79). Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables must be programmed when the command is issued.

The MR is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVATE command. Violating either of these requirements will result in an unspecified operation.

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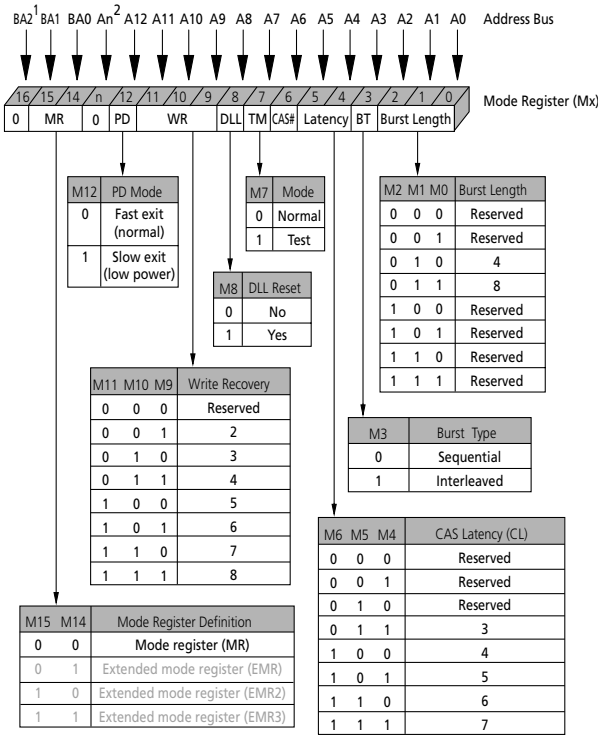
Burst Length

Burst length is defined by bits M0–M2, as shown in Figure 36. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when BL = 4 and by A3–A*i* when BL = 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

Figure 36: MR Definition



Notes:
1. M16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to "0."
2. Mode bits (M*n*) with corresponding address balls (A*n*) greater than M12 (A12) are reserved for future use and must be programmed to "0."
3. Not all listed WR and CL options are supported in any individual speed grade.

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Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 36. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 41. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleaved address ordering is supported; however, sequential address ordering is nibble-based.

Table 41: Burst Definition

Burst Length	Starting Column Address (A2, A1, A0)	Order of Accesses Within a Burst	
		Burst Type = Sequential	Burst Type = Interleaved
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Operating Mode

The normal operating mode is selected by issuing a command with bit M7 set to “0,” and all other bits set to the desired values, as shown in Figure 36 (page 79). When bit M7 is “1,” no other bits of the mode register are programmed. Programming bit M7 to “1” places the DDR2 SDRAM into a test mode that is only used by the manufacturer and should *not* be used. No operation or functionality is guaranteed if M7 bit is “1.”

DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 36. Programming bit M8 to “1” will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of “0” after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

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Write Recovery

Write recovery (WR) time is defined by bits M9–M11, as shown in Figure 36 (page 79). The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of WRITE with auto precharge is shown in Figure 65 (page 113).

WR values of 2, 3, 4, 5, 6, 7, or 8 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing ^{t}WR (in nanoseconds) by ^{t}CK (in nanoseconds) and rounding up a noninteger value to the next integer; WR (cycles) = ^{t}WR (ns) / ^{t}CK (ns). Reserved states should not be used as an unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12, as shown in Figure 36. PD mode enables the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode.

When bit M12 = 0, standard active PD mode, or "fast-exit" active PD mode, is enabled. The ^{t}XARD parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode, or "slow-exit" active PD mode, is enabled. The ^{t}XARDS parameter is used for slow-exit active PD exit timing. The DLL can be enabled but "frozen" during active PD mode because the exit-to-READ command timing is relaxed. The power difference expected between I_{DD3P} normal and I_{DD3P} low-power mode is defined in the DDR2 I_{DD} Specifications and Conditions table.

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CAS Latency (CL)

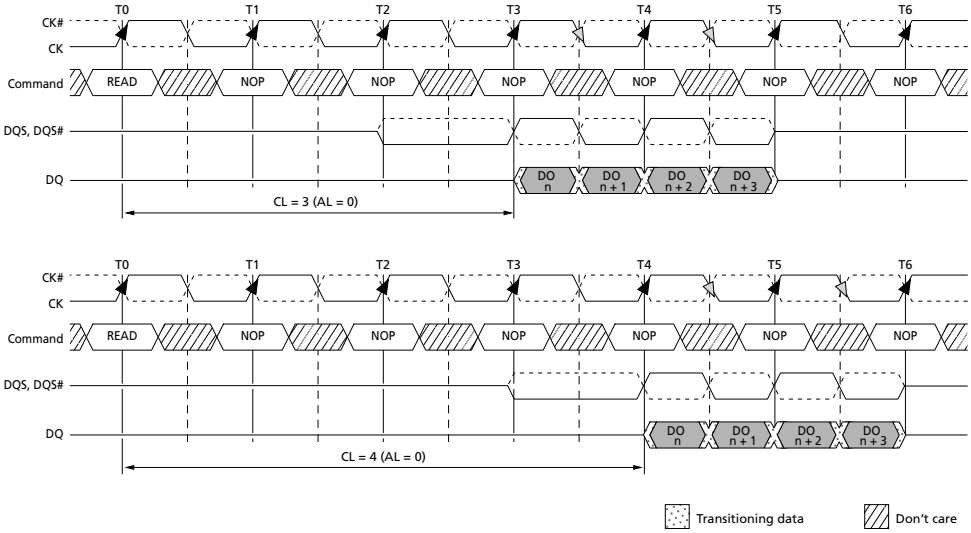
The CAS latency (CL) is defined by bits M4–M6, as shown in Figure 36 (page 79). CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, 6, or 7 clocks, depending on the speed grade option being used.

DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as an unknown operation otherwise incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD (MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks. The AL feature is described in further detail in Posted CAS Additive Latency (AL) (page 85).

Examples of CL = 3 and CL = 4 are shown in Figure 37; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CL is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

Figure 37: CL



Notes: 1. BL = 4.
2. Posted CAS# additive latency (AL) = 0.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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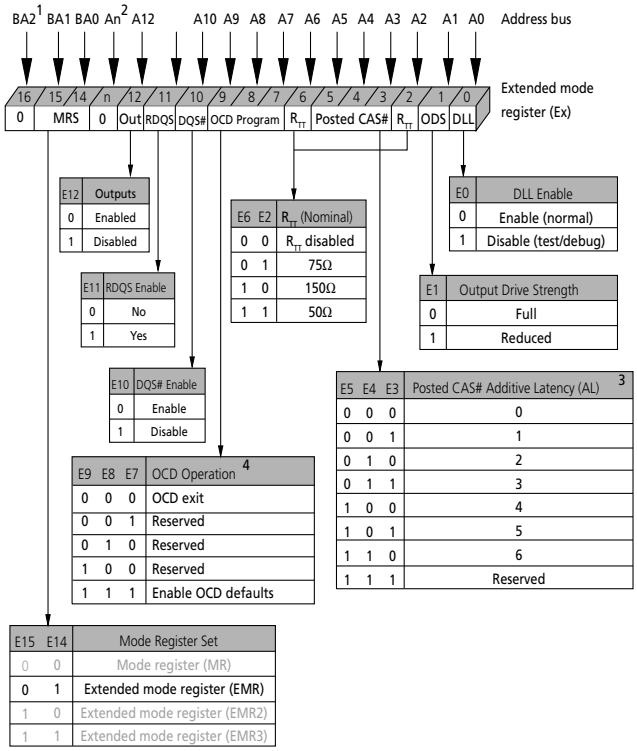
Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on-die termination (ODT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 38. The EMR is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 38: EMR Definition



Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to 0.
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to 0.
3. Not all listed AL options are supported in any individual speed grade.
4. As detailed in the Initialization section notes, during initialization of the OCD operation, all three bits must be set to 1 for the OCD default state, then set to 0 before initialization is finished.

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DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 38 (page 83). These specifications are applicable when the DLL is enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation.

Anytime the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Anytime the DLL is disabled and the device is operated below 25 MHz, any AUTO REFRESH command should be followed by a PRECHARGE ALL command.

Output Drive Strength

The output drive strength is defined by bit E1, as shown in Figure 38. The normal drive strength for all outputs is specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 45 to 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

DQS# Enable/Disable

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (E10 = 1), DQS is used in a single-ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating; however, it may be tied to ground via a 20Ω to 10kΩ resistor. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

RDQS Enable/Disable

The RDQS ball is enabled by bit E11, as shown in Figure 38. This feature is only applicable to the x8 configuration. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM.

Output Enable/Disable

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 38. When enabled (E12 = 0), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during I_{DD} characterization of read current.

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On-Die Termination (ODT)

ODT effective resistance, $R_{TT(EFF)}$, is defined by bits E2 and E6 of the EMR, as shown in Figure 38 (page 83). The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. R_{TT} effective resistance values of 50Ω, 75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signal. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off sw1, sw2, or sw3. The ODT effective resistance value is selected by enabling switch sw1, which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω ($R_{TT2\ [EFF]}$ = R2/2). Similarly, if sw2 is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω ($R_{TT2[EFF]}$ = R2/2). Switch sw3 enables R1 values of 100Ω, enabling effective resistance of 50Ω. Reserved states should not be used, as an unknown operation or incompatibility with future versions may result.

The ODT control ball is used to determine when $R_{TT(EFF)}$ is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation.

ODT must be turned off prior to entering self refresh mode. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until the EMR command is issued. This will enable the ODT feature, at which point the ODT ball will determine the $R_{TT(EFF)}$ value. Anytime the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled (see Figure 81 (page 130) for ODT timing diagrams).

Off-Chip Driver (OCD) Impedance Calibration

The OFF-CHIP DRIVER function is an optional DDR2 JEDEC feature not supported by Micron and thereby must be set to the default state. Enabling OCD beyond the default settings will alter the I/O drive characteristics and the timing and output I/O specifications will no longer be valid (see Initialization section for proper setting of OCD defaults).

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 38. Bits E3–E5 allow the user to program the DDR2 SDRAM with an AL of 0, 1, 2, 3, 4, 5, or 6 clocks. Reserved states should not be used as an unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD (MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 × ^{t}CK. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of AL and CL; RL = AL + CL. WRITE latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 × ^{t}CK. An example of RL is shown in Figure 39 (page 86). An example of a WL is shown in Figure 40 (page 86).

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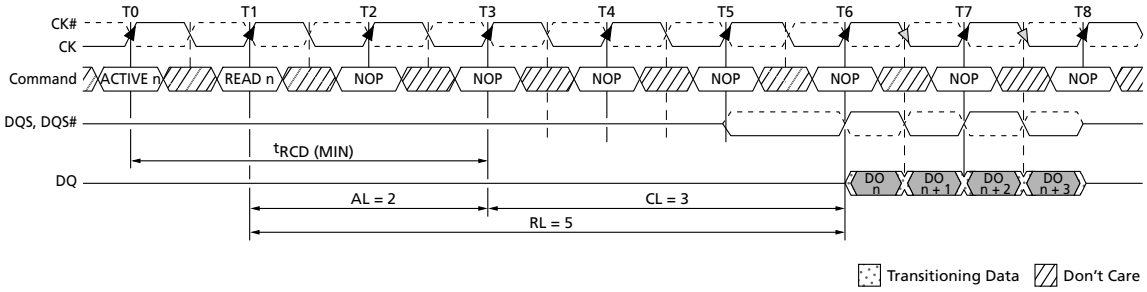
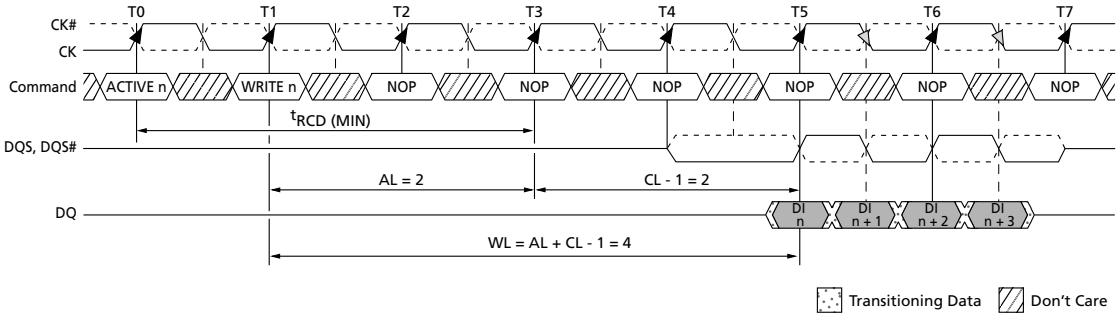
Figure 39: READ Latency



Notes: 1. BL = 4.
2. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
3. RL = AL + CL = 5.

Figure 40: WRITE Latency



Notes: 1. BL = 4.
2. CL = 3.
3. WL = AL + CL - 1 = 4.

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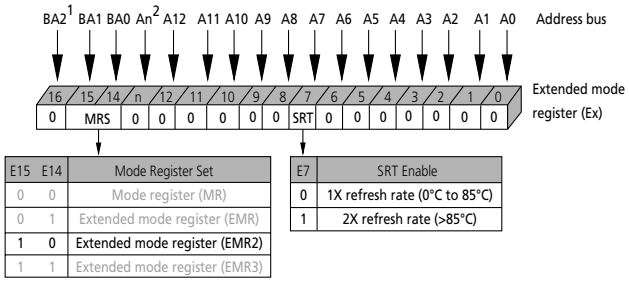
Extended Mode Register 2 (EMR2)

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, except for E7, which is used in commercial or high-temperature operations, as shown in Figure 41. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

Bit E7 (A7) must be programmed as 1 to provide a faster refresh rate on IT and AT devices if T_C exceeds 85°C.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 41: EMR2 Definition



Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to 0.
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to 0.

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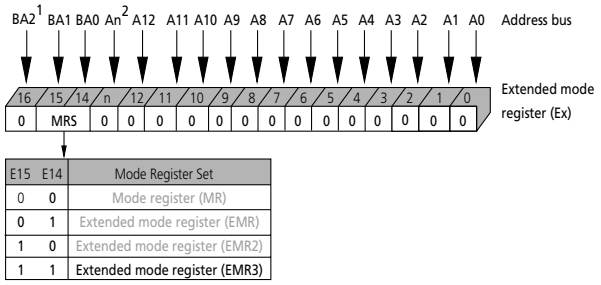
Extended Mode Register 3 (EMR3)

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved, as shown in Figure 42. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 42: EMR3 Definition



Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, is reserved for future use, and must be programmed to 0.
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to 0.

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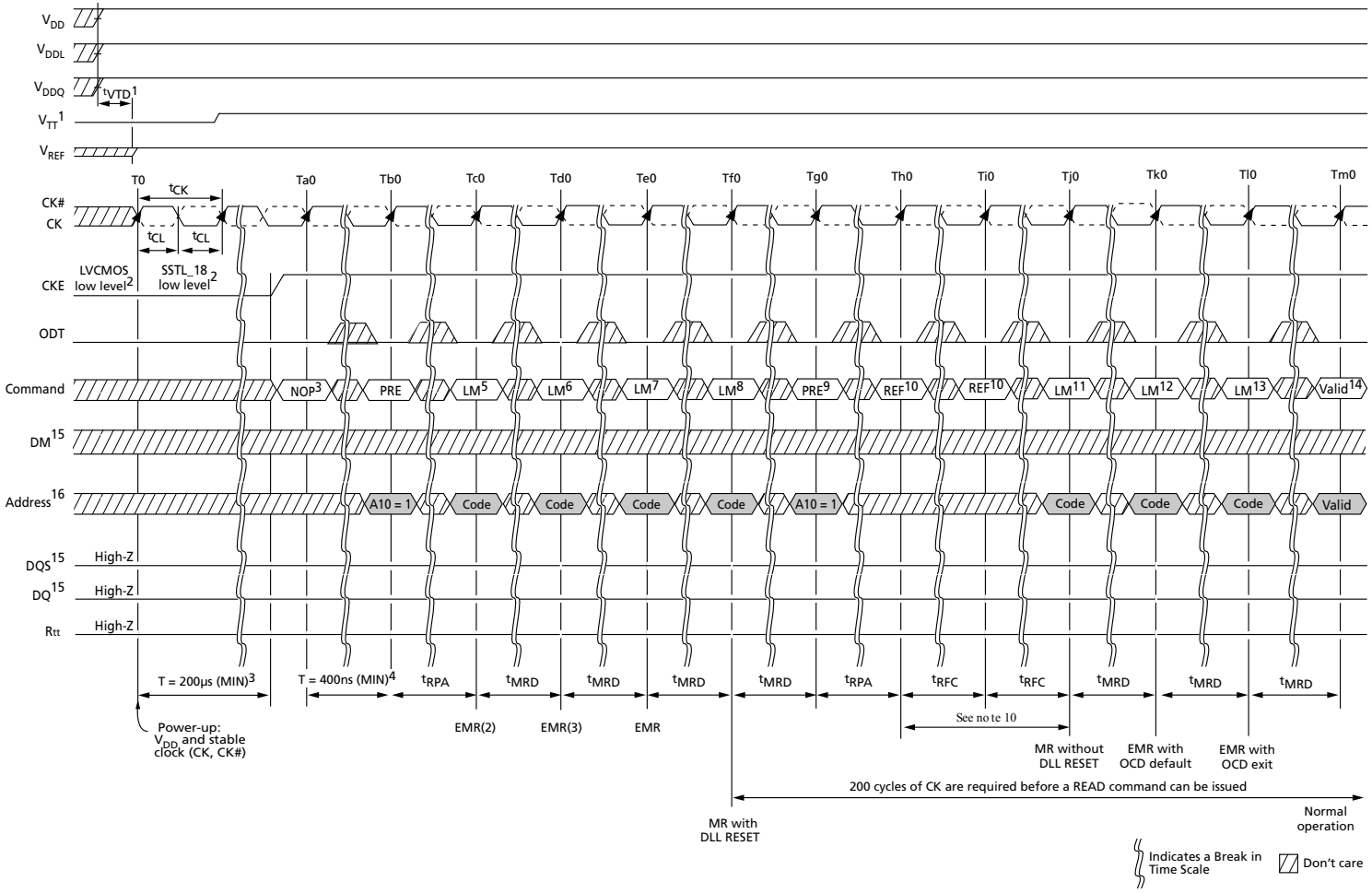
Initialization

Figure 43: DDR2 Power-Up and Initialization

DDR2 SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Figure 43 illustrates, and the notes outline, the sequence required for power-up and initialization.



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Notes:

1. Applying power; if CKE is maintained below 0.2 × V_{DDQ}, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined; I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DDR2 SDRAM device latch-up). V_{TT} is not applied directly to the device; however, ^{t}VTD should be ≥0 to avoid device latch-up. At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as V_{DD}, V_{DDL}, V_{DDQ}, V_{REF}, and V_{TT} are between their minimum and maximum values as stated in Table 13 (page 45)):

   A. Single power source: The V_{DD} voltage ramp from 300mV to $V_{DD,min}$ must take no longer than 200ms; during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3V$. Once supply voltage ramping is complete (when V_{DDQ} crosses $V_{DD,min}$), Table 13 specifications apply.

   - V_{DD}, V_{DDL}, and V_{DDQ} are driven from a single power converter output
   - V_{TT} is limited to 0.95V MAX
   - V_{REF} tracks $V_{DDQ}/2$; V_{REF} must be within ±0.3V with respect to $V_{DDQ}/2$ during supply ramp time; does not need to be satisfied when ramping power down
   - $V_{DDQ} \geq V_{REF}$ at all times

   B. Multiple power sources: $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (V_{DDQ} crosses $V_{DD,min}$). Once supply voltage ramping is complete, Table 13 specifications apply.

   - Apply V_{DD} and V_{DDL} before or at the same time as V_{DDQ}; V_{DD}/V_{DDL} voltage ramp time must be ≤ 200ms from when V_{DD} ramps from 300mV to $V_{DD,min}$
   - Apply V_{DDQ} before or at the same time as V_{TT}; the V_{DDQ} voltage ramp time from when $V_{DD,min}$ is achieved to when $V_{DDQ,min}$ is achieved must be ≤ 500ms; while V_{DD} is ramping, current can be supplied from V_{DD} through the device to V_{DDQ}
   - V_{REF} must track $V_{DDQ}/2$; V_{REF} must be within ±0.3V with respect to $V_{DDQ}/2$ during supply ramp time; $V_{DDQ} \geq V_{REF}$ must be met at all times; does not need to be satisfied when ramping power down
   - Apply V_{TT}; the V_{TT} voltage ramp time from when $V_{DDQ,min}$ is achieved to when $V_{TT,min}$ is achieved must be no greater than 500ms
2. CKE requires LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to V_{REF} being stable. After state T0, CKE is required to have SSTL_18 input levels. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
3. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
4. Wait a minimum of 400ns then issue a PRECHARGE ALL command.
5. Issue a LOAD MODE command to the EMR(2). To issue an EMR(2) command, provide LOW to BA0, and provide HIGH to BA1; set register E7 to "0" or "1" to select appropriate self refresh rate; remaining EMR(2) bits must be "0" (see Extended Mode Register 2 (EMR2) (page 87) for all EMR(2) requirements).
6. Issue a LOAD MODE command to the EMR(3). To issue an EMR(3) command, provide HIGH to BA0 and BA1; remaining EMR(3) bits must be "0." Extended Mode Register 3 (EMR3) for all EMR(3) requirements.
7. Issue a LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0; provide HIGH to BA0; bits E7, E8, and E9 can be set to "0" or "1;" Micron recommends setting them to "0;" remaining EMR bits must be "0." Extended Mode Register (EMR) (page 83) for all EMR requirements.
8. Issue a LOAD MODE command to the MR for DLL RESET. 200 cycles of clock input is required to lock the DLL. To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1 and BA0; CKE must be HIGH the entire time the DLL is resetting; remaining MR bits must be "0." Mode Register (MR) (page 78) for all MR requirements.
9. Issue PRECHARGE ALL command.

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10. Issue two or more REFRESH commands.
11. Issue a LOAD MODE command to the MR with LOW to A8 to initialize device operation (that is, to program operating parameters without resetting the DLL). To access the MR, set BA0 and BA1 LOW; remaining MR bits must be set to desired settings. Mode Register (MR) (page 78) for all MR requirements.
12. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters. To access the EMR, set BA0 HIGH and BA1 LOW (see Extended Mode Register (EMR) (page 83) for all EMR requirements.
13. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. To access the extended mode registers, EMR, set BA0 HIGH and BA1 LOW for all EMR requirements.
14. The DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at Tf0.
15. DM represents DM for the x4, x8 configurations and UDM, LDM for the x16 configuration; DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16); DQ represents DQ[3:0] for x4, DQ[7:0] for x8 and DQ[15:0] for x16.
16. A10 = PRECHARGE ALL, CODE = desired values for mode registers (bank addresses are required to be decoded).

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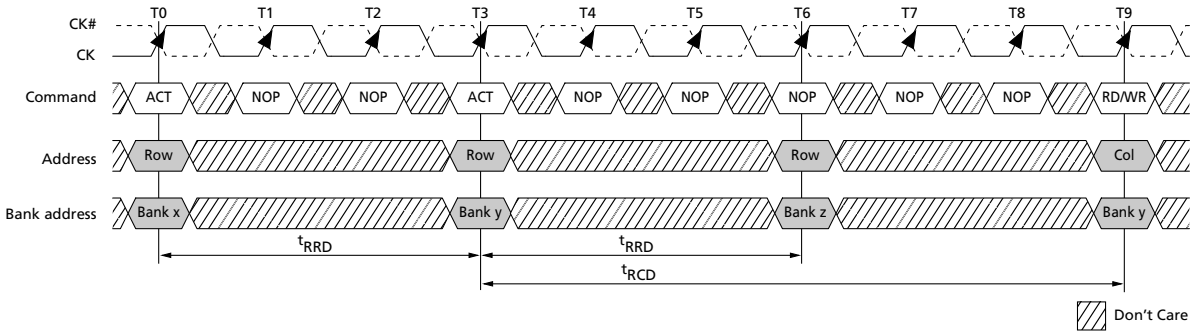
ACTIVATE

Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a ^{t}RCD (MIN) specification of 20ns with a 266 MHz clock (^{t}CK = 3.75ns) results in 5.3 clocks, rounded up to 6. This is shown in Figure 44, which covers any case where 5 < ^{t}RCD (MIN) / ^{t}CK ≤ 6. Figure 44 also shows the case for ^{t}RRD where 2 < ^{t}RRD (MIN) / ^{t}CK ≤ 3.

Figure 44: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)



A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by ^{t}RRD.

DDR2 devices with 8 banks (1Gb or larger) have an additional requirement: ^{t}FAW. This requires no more than four ACTIVATE commands may be issued in any given ^{t}FAW (MIN) period, as shown in Figure 45 (page 93).

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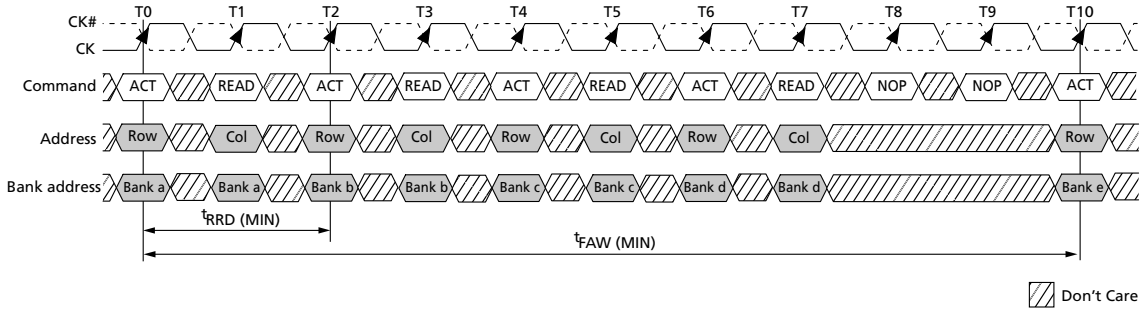
Figure 45: Multibank Activate Restriction



Note: 1. DDR2-533 (-37E, x4 or x8), ^{t}CK = 3.75ns, BL = 4, AL = 3, CL = 4, ^{t}RRD (MIN) = 7.5ns, ^{t}FAW (MIN) = 37.5ns.

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READ

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL: RL = AL + CL. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (at the next crossing of CK and CK#). Figure 46 (page 95) shows examples of RL based on different AL and CL settings.

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and the HIGH state on DQS# are known as the read preamble (^{t}RPRE). The LOW state on DQS and the HIGH state on DQS# coincident with the last data-out element are known as the read postamble (^{t}RPST).

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window are depicted in Figure 55 (page 103) and Figure 56 (page 104). A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is shown in Figure 57 (page 105).

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued *x* cycles after the first READ command, where *x* equals BL/2 cycles (see Figure 47 (page 96)).

Nonconsecutive read data is illustrated in Figure 48 (page 97). Full-speed random read accesses within a page (or pages) can be performed. DDR2 SDRAM supports the use of concurrent auto precharge timing (see Table 42 (page 100)).

DDR2 SDRAM does not allow interrupting or truncating of any READ burst using BL = 4 operations. Once the BL = 4 READ command is registered, it must be allowed to complete the entire READ burst. However, a READ (with auto precharge disabled) using BL = 8 operation may be interrupted and truncated *only* by another READ burst as long as the interruption occurs on a 4-bit boundary due to the 4*n* prefetch architecture of DDR2 SDRAM. As shown in Figure 49 (page 98), READ burst BL = 8 operations may not be interrupted or truncated with any other command except another READ command.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst is shown in Figure 50 (page 98). The ^{t}DQSS (NOM) case is shown (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in Figure 58 (page 107)).

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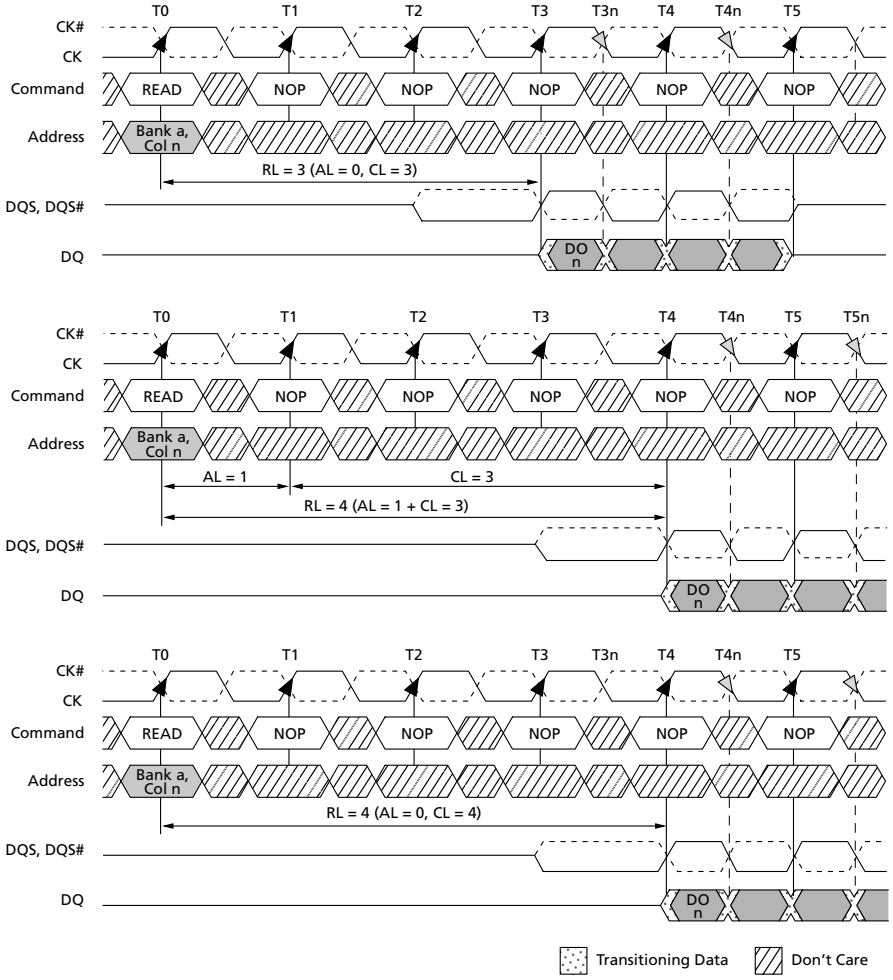
Figure 46: READ Latency



Notes:
1. DO *n* = data-out from column *n*.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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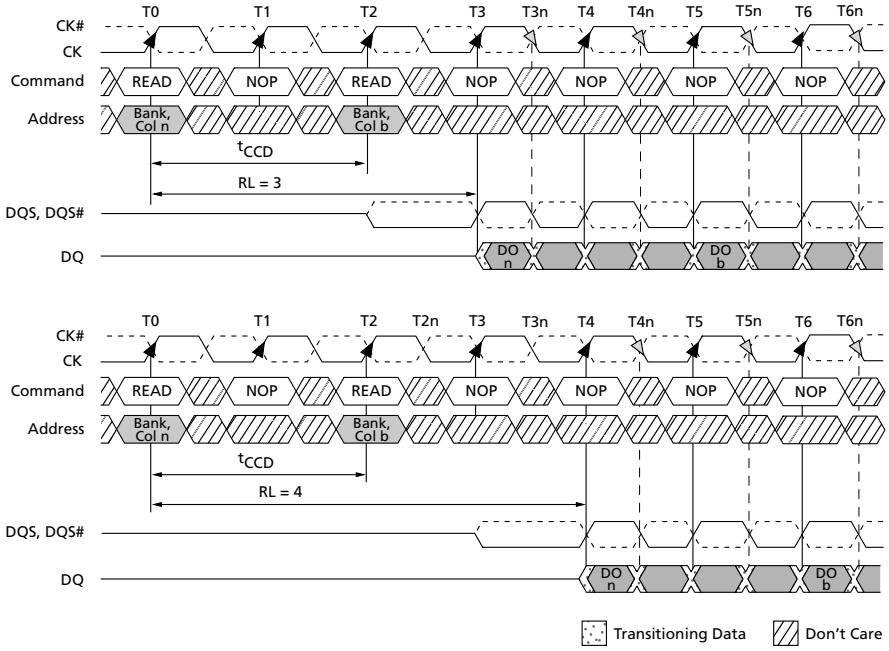
Figure 47: Consecutive READ Bursts



Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.

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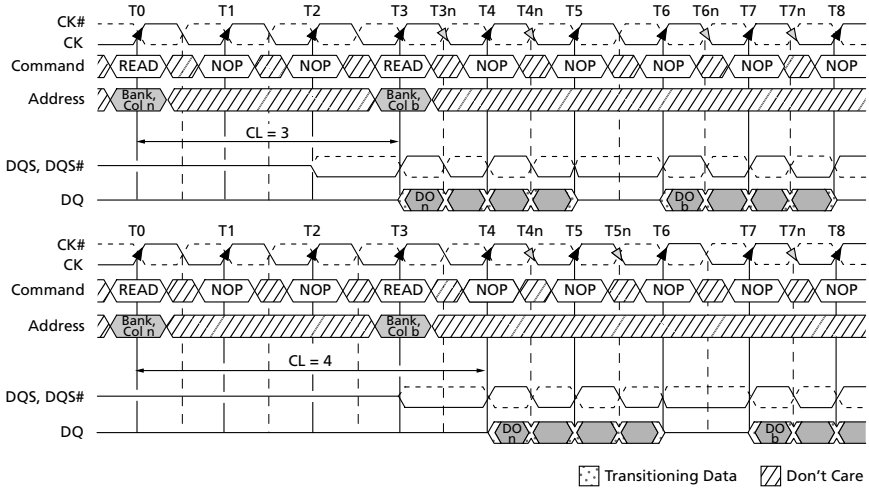
Figure 48: Nonconsecutive READ Bursts



Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

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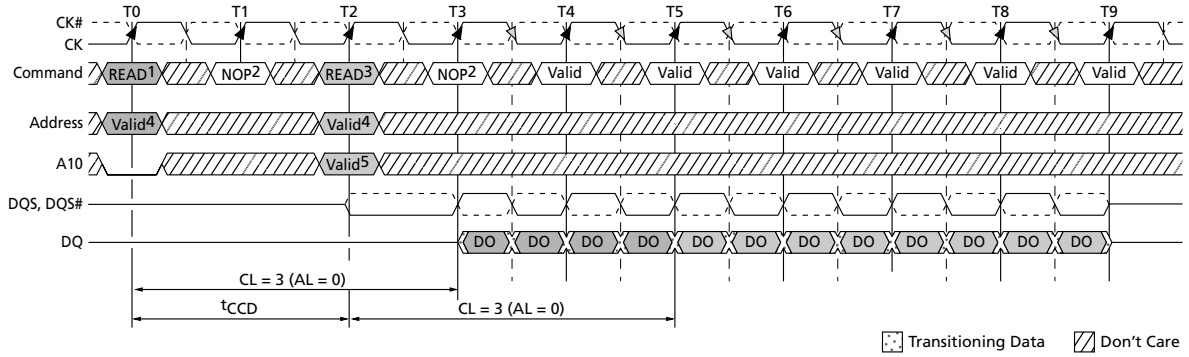
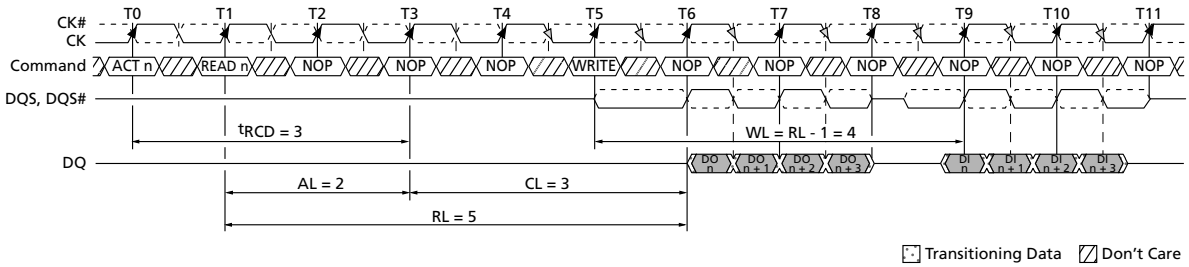
Figure 49: READ Interrupted by READ



Notes:
1. BL = 8 required; auto precharge must be disabled (A10 = LOW).
2. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for READs at T0 and T2.
3. Interrupting READ command must be issued exactly 2 × ^{t}CK from previous READ.
4. READ command can be issued to any valid bank and row address (READ command at T0 and T2 can be either same bank or different bank).
5. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting READ command.
6. Example shown uses AL = 0; CL = 3, BL = 8, shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 50: READ-to-WRITE



Notes:
1. BL = 4; CL = 3; AL = 2.
2. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

READ with Precharge

A READ burst may be followed by a PRECHARGE command to the same bank, provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank has two requirements that must be satisfied: AL + BL/2 clocks and ^{t}RTP. ^{t}RTP is the minimum time from the rising clock edge that initiates the last 4-bit prefetch of a READ command to the PRECHARGE command. For BL = 4, this is the time from the actual READ (AL after the READ command) to PRECHARGE command. For BL = 8, this is the time from AL + 2 × CK after the READ-to-PRECHARGE command. Follow-

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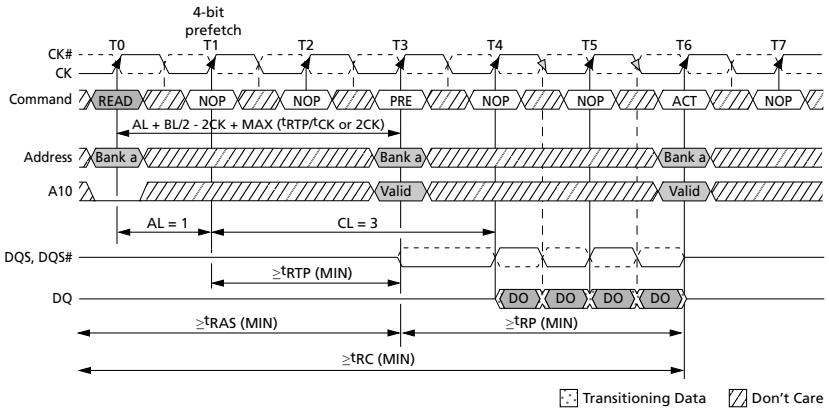
ing the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. However, part of the row precharge time is hidden during the access of the last data elements.

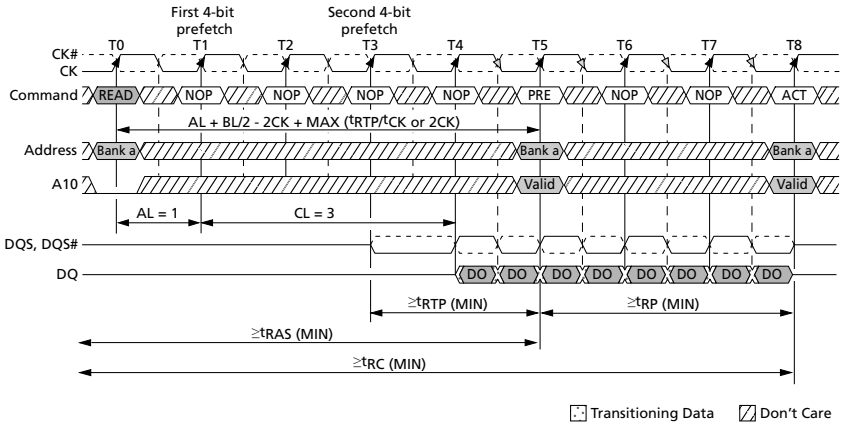
Examples of READ-to-PRECHARGE for BL = 4 are shown in Figure 51 and in Figure 52 for BL = 8. The delay from READ-to-PRECHARGE period to the same bank is AL + BL/2 - 2CK + MAX (^{t}RTP/^{t}CK or 2 × CK) where MAX means the larger of the two.

Figure 51: READ-to-PRECHARGE – BL = 4



Notes:
1. RL = 4 (AL = 1, CL = 3); BL = 4.
2. ^{t}RTP ≥ 2 clocks.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 52: READ-to-PRECHARGE – BL = 8



Notes:
1. RL = 4 (AL = 1, CL = 3); BL = 8.
2. ^{t}RTP ≥ 2 clocks.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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READ with Auto Precharge

If A10 is high when a READ command is issued, the READ with auto precharge function is engaged. The DDR2 SDRAM starts an auto precharge operation on the rising clock edge that is AL + (BL/2) cycles later than the read with auto precharge command provided ^{t}RAS (MIN) and ^{t}RTP are satisfied. If ^{t}RAS (MIN) is not satisfied at this rising clock edge, the start point of the auto precharge operation will be delayed until ^{t}RAS (MIN) is satisfied. If ^{t}RTP (MIN) is not satisfied at this rising clock edge, the start point of the auto precharge operation will be delayed until ^{t}RTP (MIN) is satisfied. When the internal precharge is pushed out by ^{t}RTP, ^{t}RP starts at the point where the internal precharge happens (not at the next rising clock edge after this event).

When BL = 4, the minimum time from READ with auto precharge to the next ACTIVATE command is AL + (^{t}RTP + ^{t}RP)/^{t}CK. When BL = 8, the minimum time from READ with auto precharge to the next ACTIVATE command is AL + 2 clocks + (^{t}RTP + ^{t}RP)/^{t}CK. The term (^{t}RTP + ^{t}RP)/^{t}CK is always rounded up to the next integer. A general purpose equation can also be used: AL + BL/2 - 2CK + (^{t}RTP + ^{t}RP)/^{t}CK. In any event, the internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

READ with auto precharge command may be applied to one bank while another bank is operational. This is referred to as concurrent auto precharge operation, as noted in Table 42. Examples of READ with precharge and READ with auto precharge with applicable timing requirements are shown in Figure 53 (page 101) and Figure 54 (page 102), respectively.

Table 42: READ Using Concurrent Auto Precharge

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
READ with auto precharge	READ or READ with auto precharge	BL/2	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2) + 2	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK

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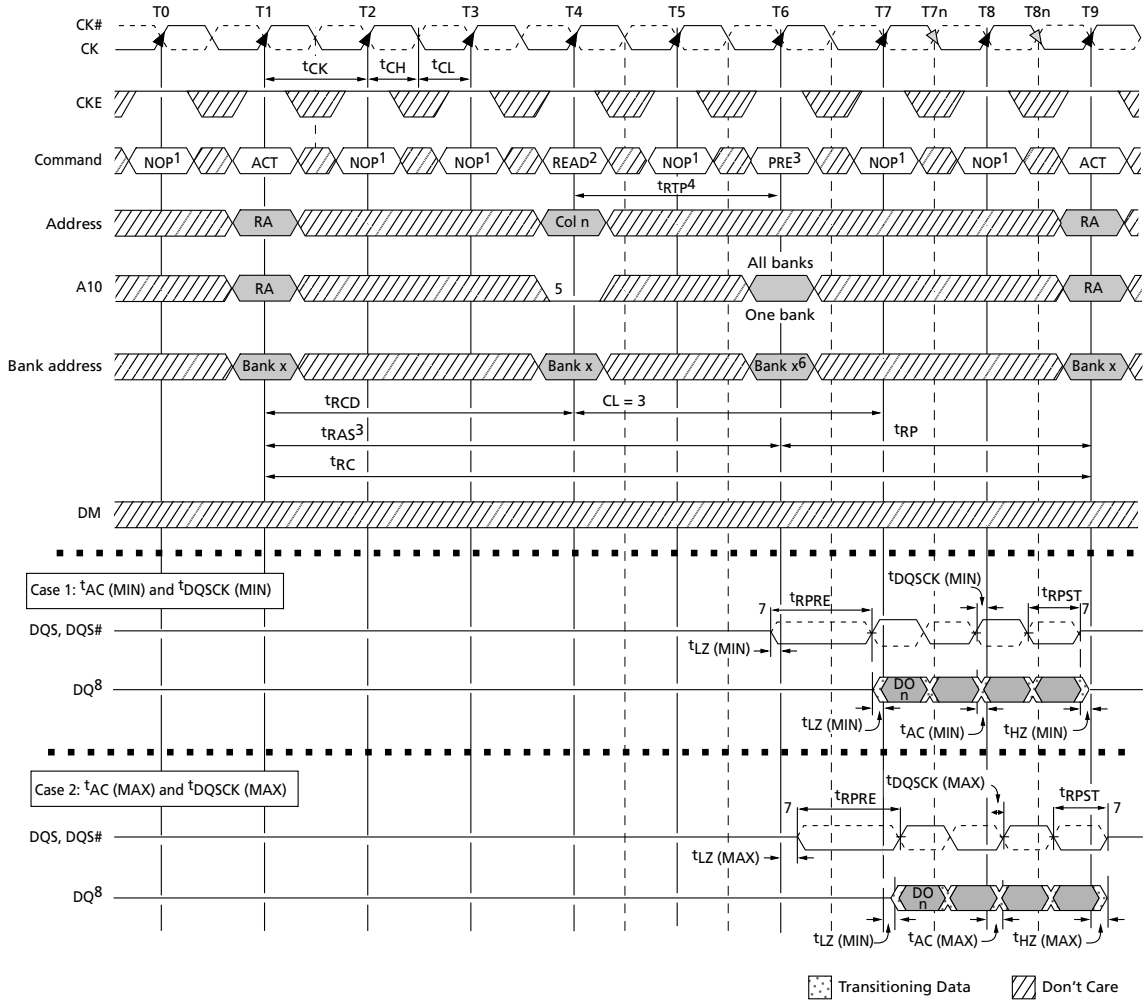
Figure 53: Bank Read – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. The PRECHARGE command can only be applied at T6 if ^{t}RAS (MIN) is met.
4. READ-to-PRECHARGE = AL + BL/2 - 2CK + MAX (^{t}RTP/^{t}CK or 2CK).
5. Disable auto precharge.
6. "Don't Care" if A10 is HIGH at T5.
7. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
8. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.

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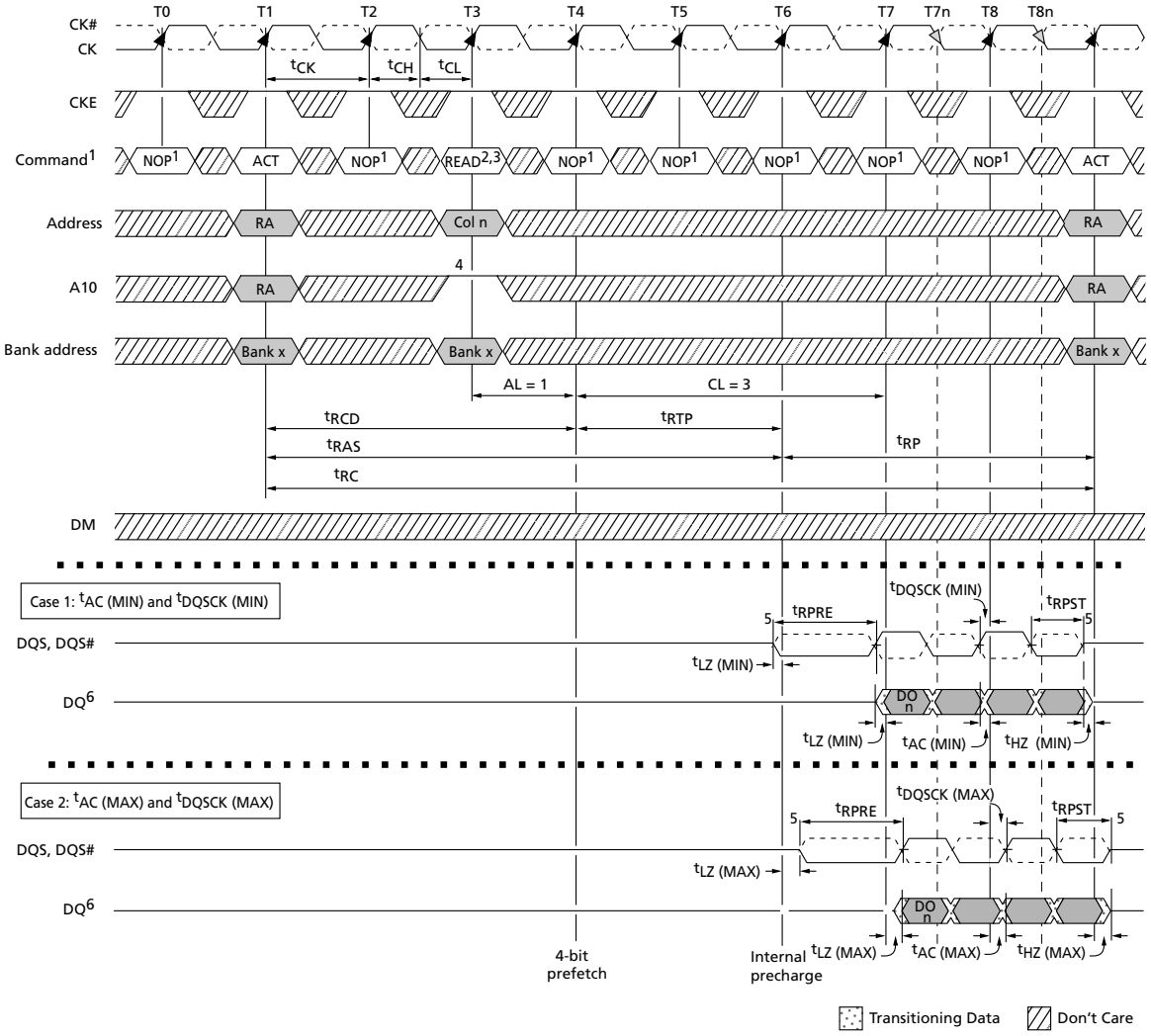
Figure 54: Bank Read – with Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4, RL = 4 (AL = 1, CL = 3) in the case shown.
3. The DDR2 SDRAM internally delays auto precharge until both ^{t}RAS (MIN) and ^{t}RTP (MIN) have been satisfied.
4. Enable auto precharge.
5. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
6. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.

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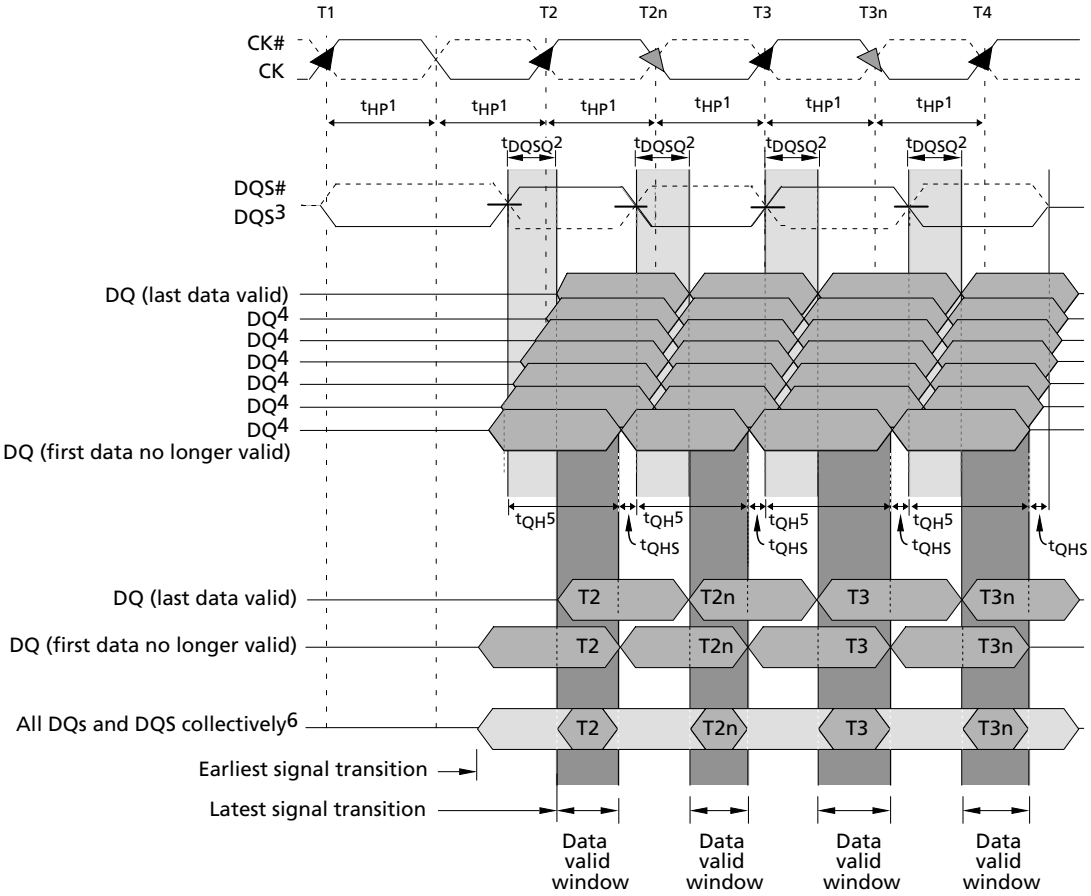
Figure 55: x4, x8 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
3. DQ transitioning after the DQS transition defines the ^{t}DQSQ window. DQS transitions at T2 and at T2n are "early DQS," at T3 are "nominal DQS," and at T3n are "late DQS."
4. DQ0, DQ1, DQ2, DQ3 for x4 or DQ[7:0] for x8.
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transition and is defined as ^{t}QH - ^{t}DQSQ.

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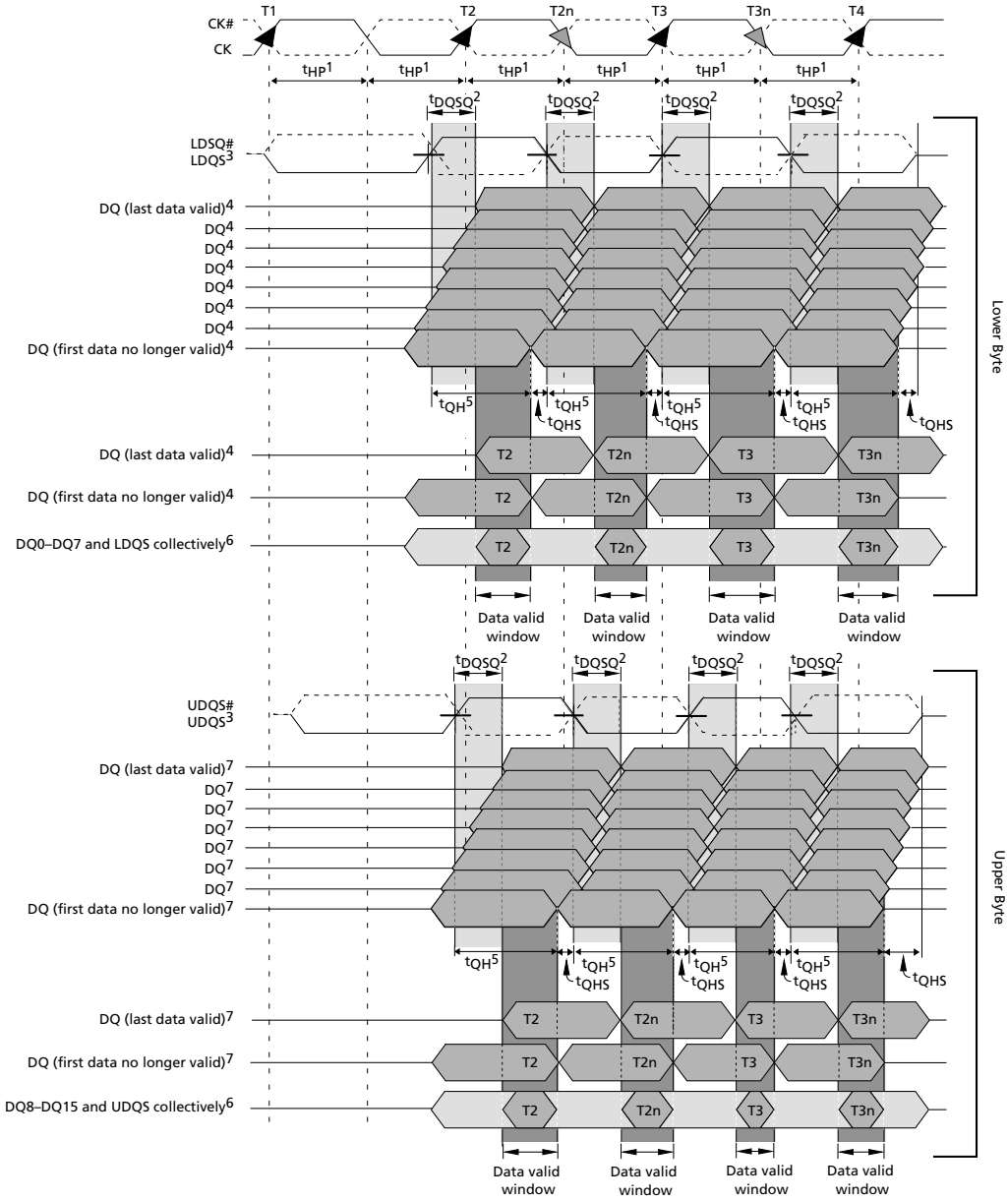
Figure 56: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
3. DQ transitioning after the DQS transitions define the ^{t}DQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.

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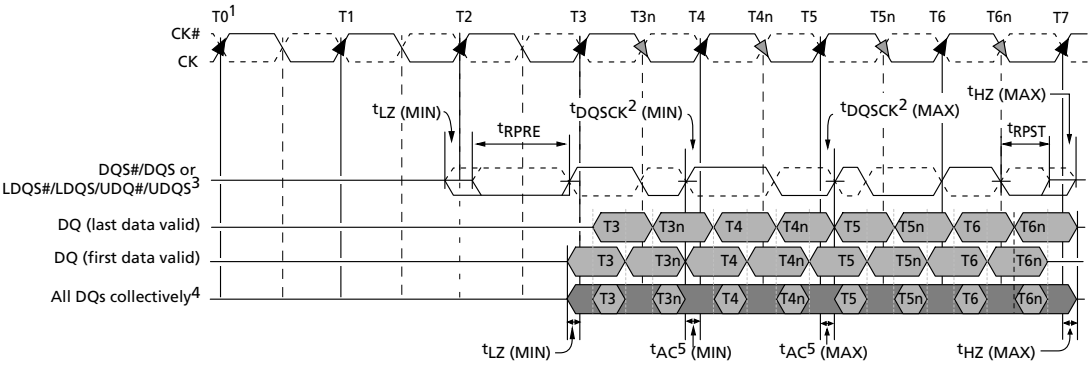
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transition and is ^{t}QH - ^{t}DQSQ.
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

Figure 57: Data Output Timing – ^{t}AC and ^{t}DQSCK



Notes:
1. READ command with CL = 3, AL = 0 issued at T0.
2. ^{t}DQSCK is the DQS output window relative to CK and is the long-term component of DQS skew.
3. DQ transitioning after DQS transitions define ^{t}DQSQ window.
4. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
5. ^{t}AC is the DQ output window relative to CK and is the "long term" component of DQ skew.
6. ^{t}LZ (MIN) and ^{t}AC (MIN) are the first valid signal transitions.
7. ^{t}HZ (MAX) and ^{t}AC (MAX) are the latest valid signal transitions.
8. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.

WRITE

WRITE bursts are initiated with a WRITE command. DDR2 SDRAM uses WL equal to RL minus one clock cycle (WL = RL - 1CK) (see READ (page 77)). The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

Note: For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is WL ± ^{t}DQSS. Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as ±^{t}DQSS. ^{t}DQSS is specified with a relatively wide range (25% of one clock cycle). All of

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the WRITE diagrams show the nominal case, and where the two extreme cases (^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 58 (page 107) shows the nominal case and the extremes of ^{t}DQSS for BL = 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals BL/2.

Figure 59 (page 108) shows concatenated bursts of BL = 4 and how full-speed random write accesses within a page or pages can be performed. An example of nonconsecutive WRITEs is shown in Figure 60 (page 108). DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 43.

DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE BL = 8 operation (with auto precharge disabled) might be interrupted and truncated *only* by another WRITE burst as long as the interruption occurs on a 4-bit boundary due to the 4*n*-prefetch architecture of DDR2 SDRAM. WRITE burst BL = 8 operations may *not* be interrupted or truncated with any command except another WRITE command, as shown in Figure 61 (page 109).

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE, ^{t}WTR should be met, as shown in Figure 62 (page 110). The number of clock cycles required to meet ^{t}WTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. ^{t}WR must be met, as shown in Figure 63 (page 111). ^{t}WR starts at the end of the data burst, regardless of the data mask condition.

Table 43: WRITE Using Concurrent Auto Precharge

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ with auto precharge	(CL - 1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2)	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK

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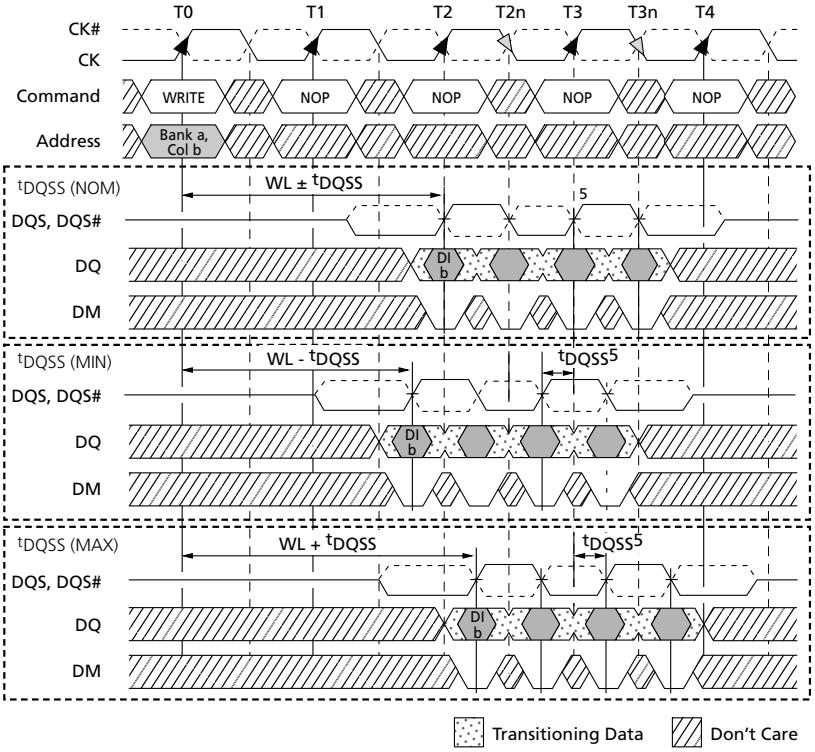
Figure 58: Write Burst



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b* = data-in for column *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

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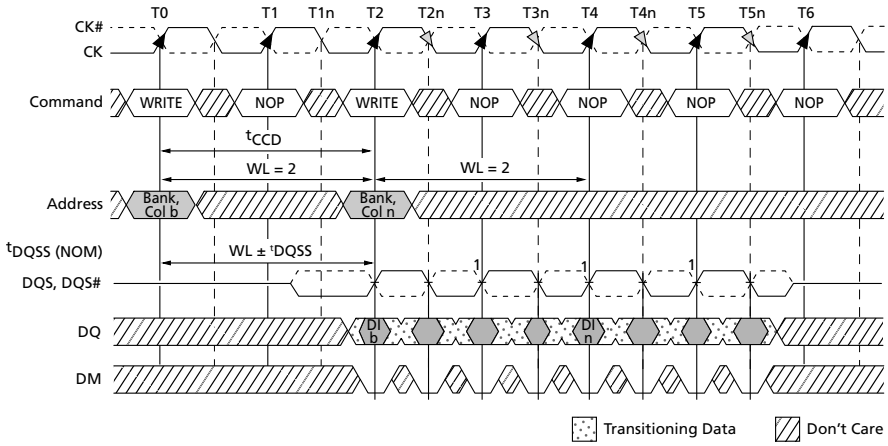
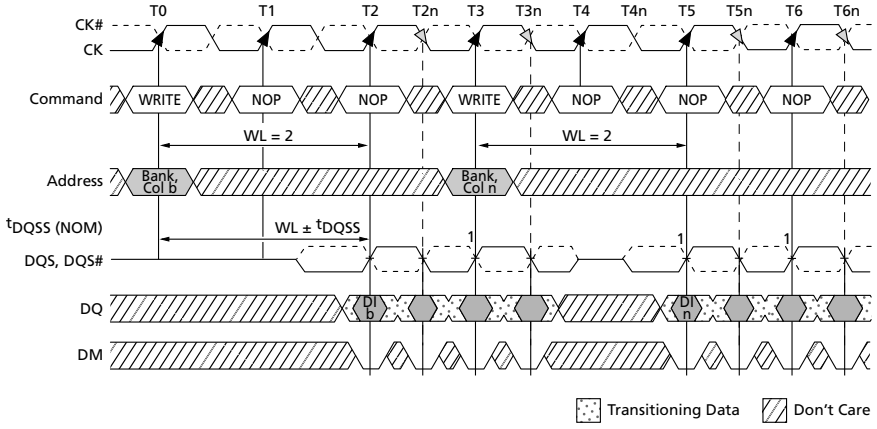
Figure 59: Consecutive WRITE-to-WRITE



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b*, etc. = data-in for column *b*, etc.
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
5. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
6. Each WRITE command may be to any bank.

Figure 60: Nonconsecutive WRITE-to-WRITE



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b* (or *n*), etc. = data-in for column *b* (or column *n*).
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
5. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
6. Each WRITE command may be to any bank.

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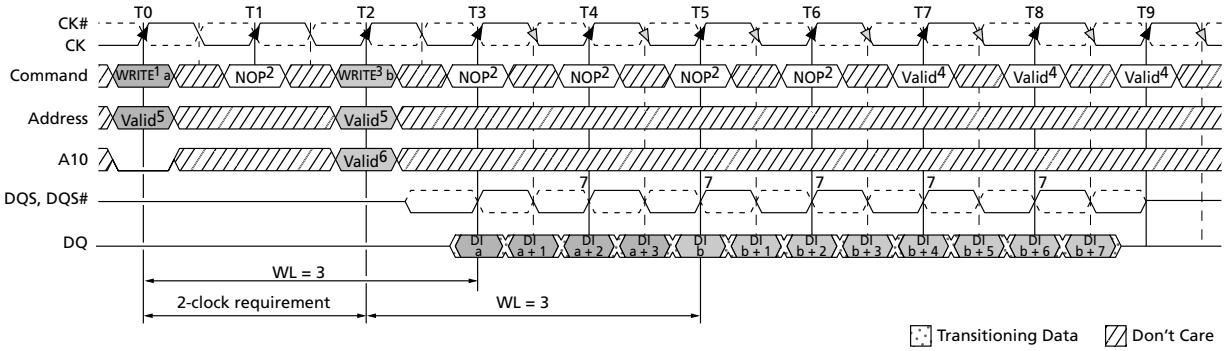
Figure 61: WRITE Interrupted by WRITE



Notes:
1. BL = 8 required and auto precharge must be disabled (A10 = LOW).
2. The NOP or COMMAND INHIBIT commands are valid. The PRECHARGE command cannot be issued to banks used for WRITEs at T0 and T2.
3. The interrupting WRITE command must be issued exactly 2 × ^{t}CK from previous WRITE.
4. The earliest WRITE-to-PRECHARGE timing for WRITE at T0 is WL + BL/2 + ^{t}WR where ^{t}WR starts with T7 and not T5 (because BL = 8 from MR and not the truncated length).
5. The WRITE command can be issued to any valid bank and row address (WRITE command at T0 and T2 can be either same bank or different bank).
6. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting WRITE command.
7. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
8. Example shown uses AL = 0; CL = 4, BL = 8.

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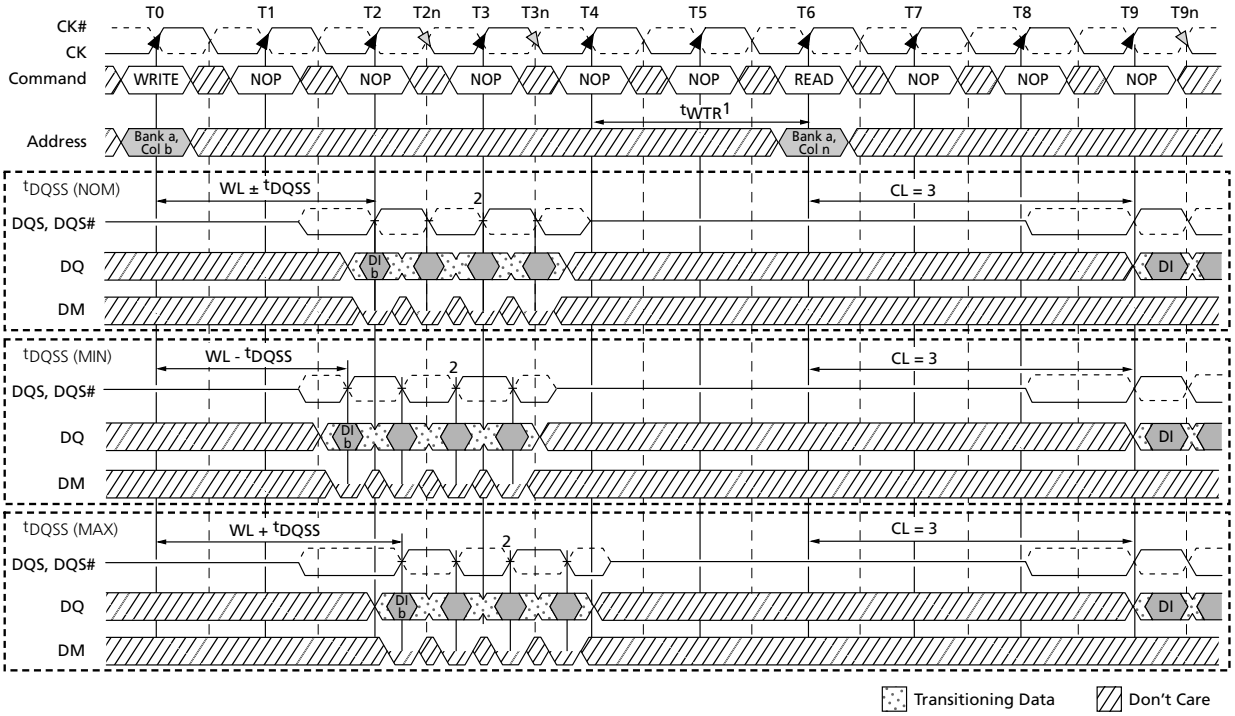
Figure 62: WRITE-to-READ



Notes:
1. tWTR is required for any READ following a WRITE to the same device, but it is not required between module ranks.
2. Subsequent rising DQS signals must align to the clock within tDQSS.
3. DI *b* = data-in for column *b*; DO *n* = data-out from column *n*.
4. BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. One subsequent element of data-in is applied in the programmed order following DI *b*.
6. tWTR is referenced from the first positive CK edge after the last data-in pair.
7. A10 is LOW with the WRITE command (auto precharge is disabled).
8. The number of clock cycles required to meet tWTR is either 2 or tWTR/tCK, whichever is greater.

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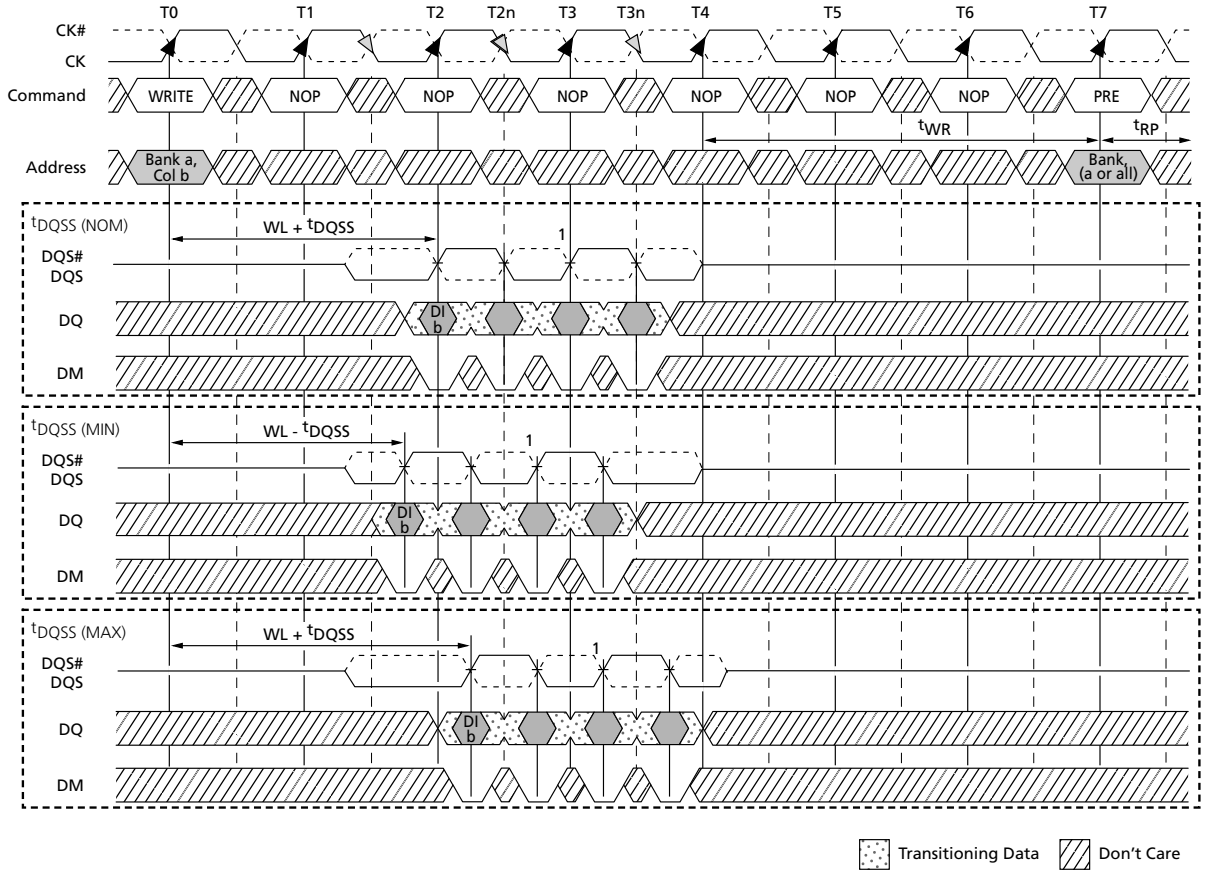
Figure 63: WRITE-to-PRECHARGE



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b* = data-in for column *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. BL = 4, CL = 3, AL = 0; thus, WL = 2.
5. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
6. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks, in which case ^{t}WR is not required and the PRECHARGE command could be applied earlier.
7. A10 is LOW with the WRITE command (auto precharge is disabled).

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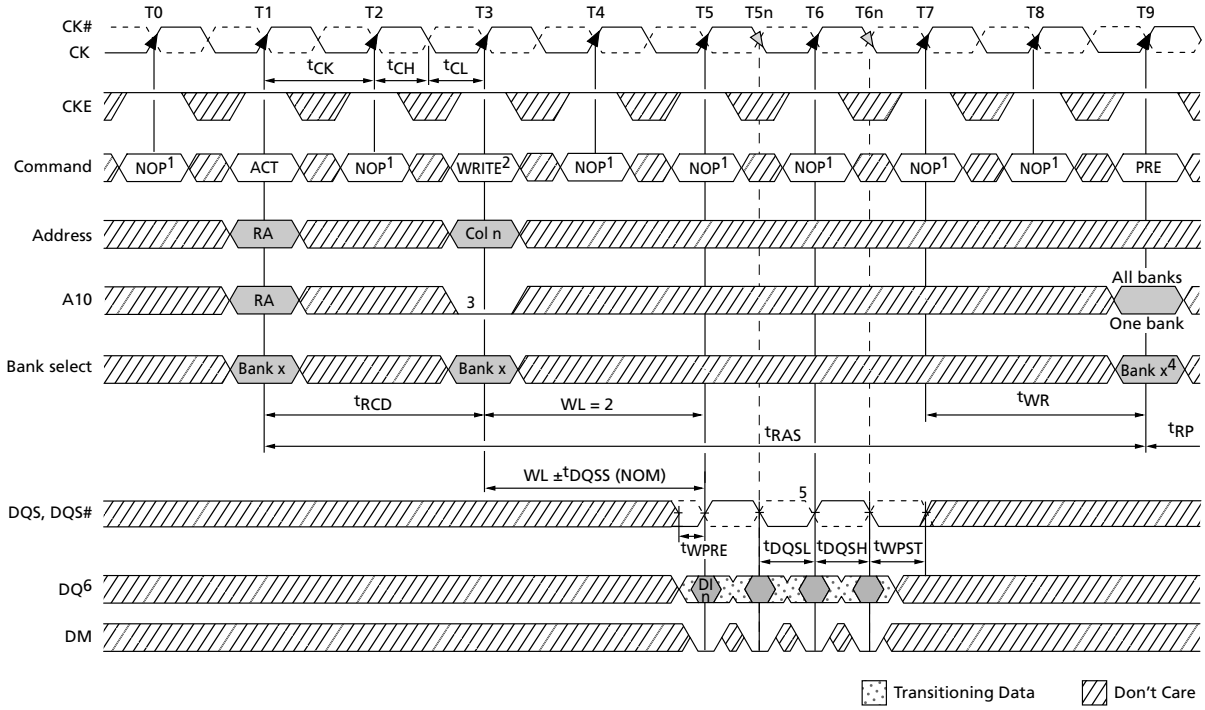
Figure 64: Bank Write – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T9.
5. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
6. DI *n* = data-in for column *n*; subsequent elements are applied in the programmed order.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.

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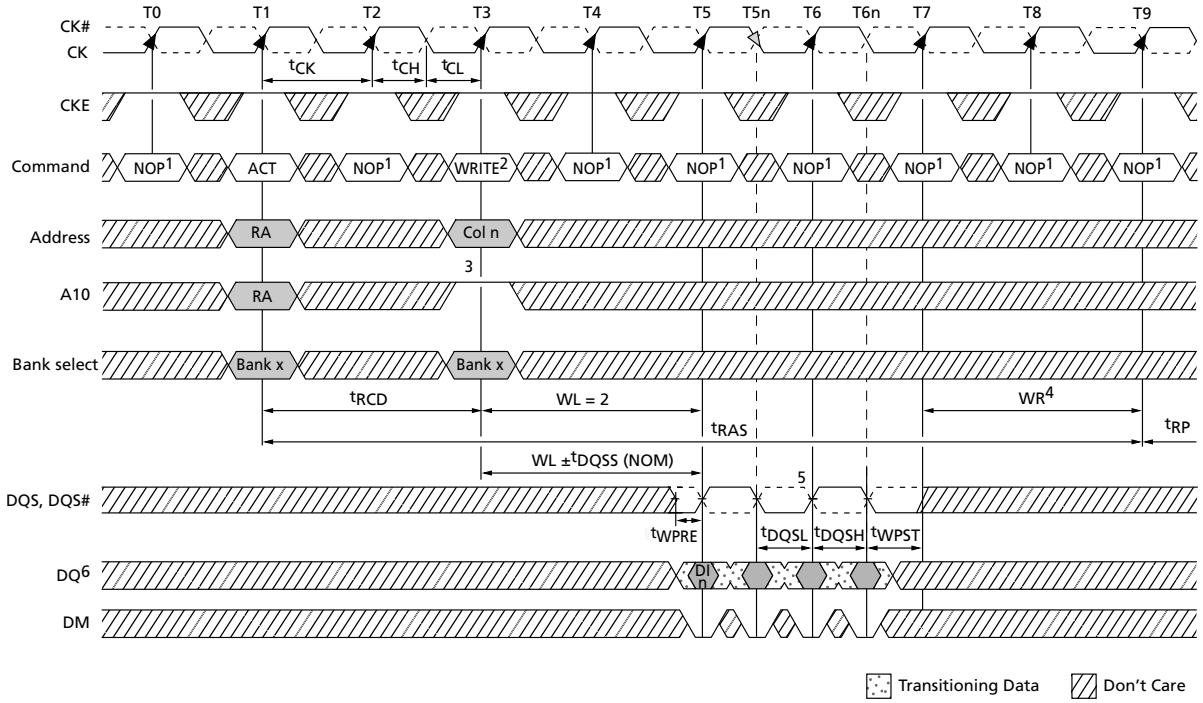
Figure 65: Bank Write – with Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. Enable auto precharge.
4. WR is programmed via MR9–MR11 and is calculated by dividing ^{t}WR (in ns) by ^{t}CK and rounding up to the next integer value.
5. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
6. DI *n* = data-in from column *n*; subsequent elements are applied in the programmed order.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.

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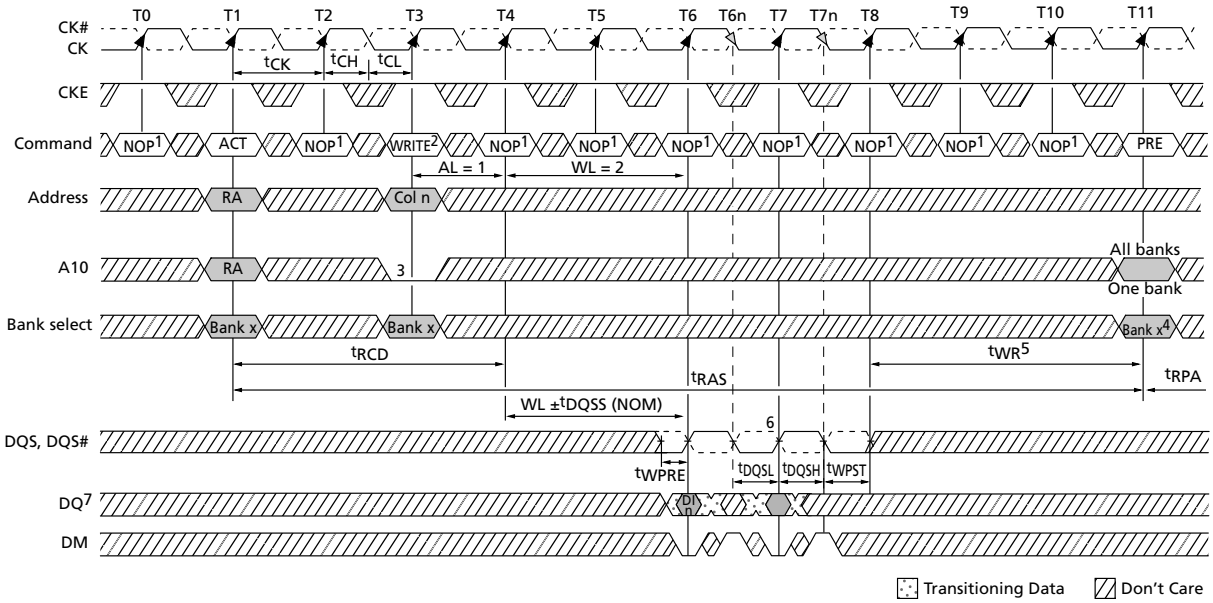
Figure 66: WRITE – DM Operation



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4, AL = 1, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T11.
5. ^{t}WR starts at the end of the data burst regardless of the data mask condition.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
7. DI *n* = data-in for column *n*; subsequent elements are applied in the programmed order.
8. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T6 or T7.
9. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T7 or T8.

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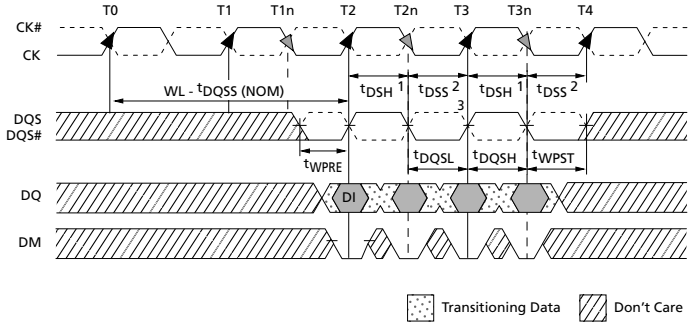
Figure 67: Data Input Timing



Notes:
1. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
2. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
3. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
4. WRITE command issued at T0.
5. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
6. WRITE command with WL = 2 (CL = 3, AL = 0) issued at T0.

PRECHARGE

Precharge can be initiated by either a manual PRECHARGE command or by an autoprecharge in conjunction with either a READ or WRITE command. Precharge will deactivate the open row in a particular bank or the open row in all banks. The PRECHARGE operation is shown in the previous READ and WRITE operation sections.

During a manual PRECHARGE command, the A10 input determines whether one or all banks are to be precharged. In the case where only one bank is to be precharged, bank address inputs determine the bank to be precharged. When all banks are to be precharged, the bank address inputs are treated as "Don't Care."

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. When a single-bank PRECHARGE command is issued, ^{t}RP timing applies. When the PRECHARGE (ALL) command is issued, ^{t}RPA timing applies, regardless of the number of banks opened.

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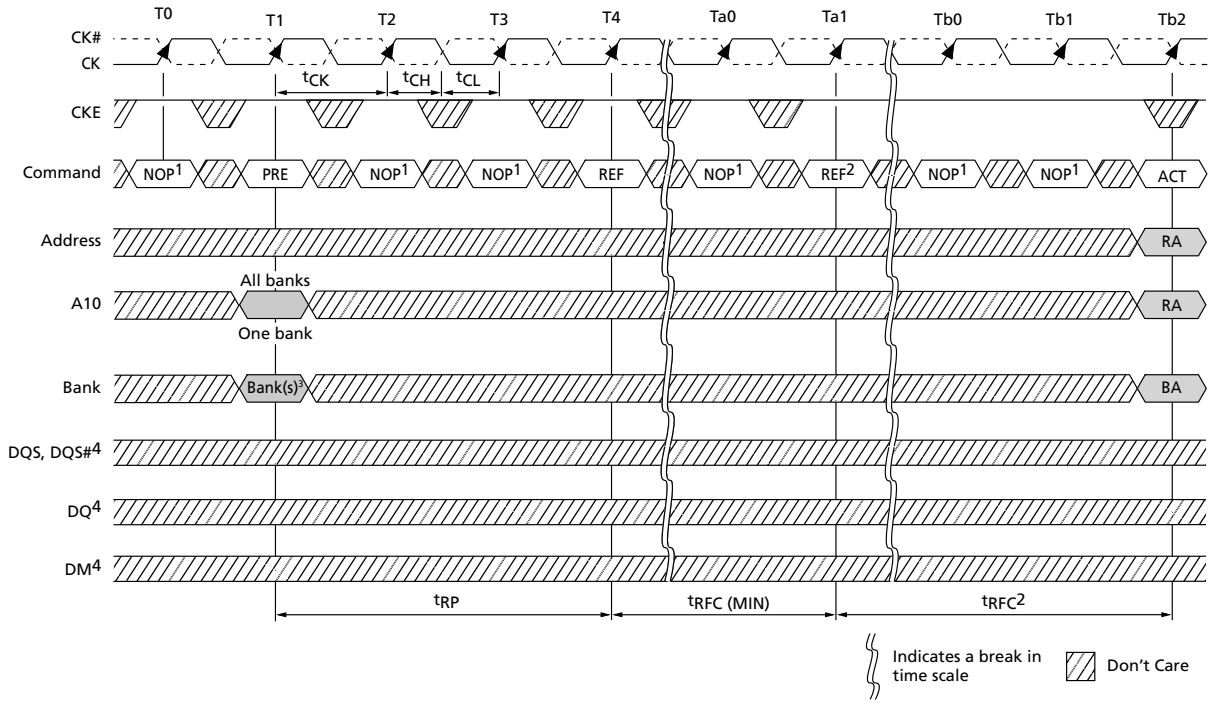
REFRESH

The commercial temperature DDR2 SDRAM requires REFRESH cycles at an average interval of 7.8125µs (MAX) and all rows in all banks must be refreshed at least once every 64ms. The refresh period begins when the REFRESH command is registered and ends ^{t}RFC (MIN) later. The average interval must be reduced to 3.9µs (MAX) when T_C exceeds 85°C.

Figure 68: Refresh Mode



Notes:
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
2. The second REFRESH is not required and is only shown as an example of two back-to-back REFRESH commands.
3. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.

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SELF REFRESH

The SELF REFRESH command is initiated when CKE is LOW. The differential clock should remain stable and meet ^{t}CKE specifications at least 1 × ^{t}CK after entering self refresh mode. The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet ^{t}CK specifications at least 1 × ^{t}CK prior to CKE going back to HIGH. Once CKE is HIGH (^{t}CKE [MIN] has been satisfied with three clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for ^{t}XSNR. A simple algorithm for meeting both refresh and DLL requirements is used to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

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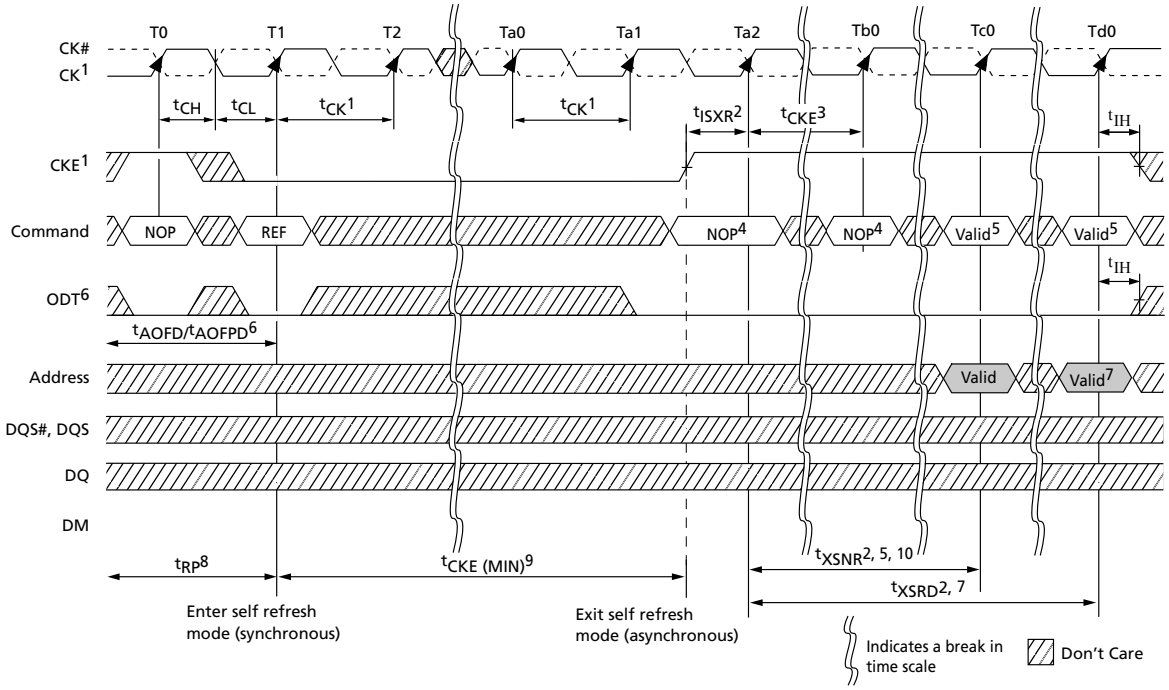
Figure 69: Self Refresh



Notes:
1. Clock must be stable and meeting ^{t}CK specifications at least 1 × ^{t}CK after entering self refresh mode and at least 1 × ^{t}CK prior to exiting self refresh mode.
2. Self refresh exit is asynchronous; however, ^{t}XSNR and ^{t}XSRD timing starts at the first rising clock edge where CKE HIGH satisfies ^{t}ISXR.
3. CKE must stay HIGH until ^{t}XSRD is met; however, if self refresh is being re-entered, CKE may go back LOW after ^{t}XSNR is satisfied.
4. NOP or DESELECT commands are required prior to exiting self refresh until state Tc0, which allows any nonREAD command.
5. ^{t}XSNR is required before any nonREAD command can be applied.
6. ODT must be disabled and R_{TT} off (^{t}AOFD and ^{t}AOFPD have been satisfied) prior to entering self refresh at state T1.
7. ^{t}XSRD (200 cycles of CK) is required before a READ command can be applied at state Td0.
8. Device must be in the all banks idle state prior to entering self refresh mode.
9. After self refresh has been entered, ^{t}CKE (MIN) must be satisfied prior to exiting self refresh.
10. Upon exiting SELF REFRESH, ODT must remain LOW until ^{t}XSRD is satisfied.

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Power-Down Mode

DDR2 SDRAM supports multiple power-down modes that allow significant power savings over normal operating modes. CKE is used to enter and exit different power-down modes. Power-down entry and exit timings are shown in Figure 70 (page 120). Detailed power-down entry conditions are shown in Figure 71 (page 122)–Figure 78 (page 125). Table 44 (page 121) is the CKE Truth Table.

DDR2 SDRAM requires CKE to be registered HIGH (active) at all times that an access is in progress—from the issuing of a READ or WRITE command until completion of the burst. Thus, a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and ^{t}WR (WRITE-to-PRECHARGE command) or ^{t}WTR (WRITE-to-READ command) are satisfied, as shown in Figure 73 (page 123) and Figure 74 (page 123) on Figure 74 (page 123). The number of clock cycles required to meet ^{t}WTR is either two or ^{t}WTR/^{t}CK, whichever is greater.

Power-down mode (see Figure 70 (page 120)) is entered when CKE is registered low coincident with an NOP or DESELECT command. CKE is not allowed to go LOW during a mode register or extended mode register command time, or while a READ or WRITE operation is in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, and CKE. For maximum power savings, the DLL is frozen during precharge power-down. Exiting active power-down requires the device to be at the same voltage and frequency as when it entered power-down. Exiting precharge power-down requires the device to be at the same voltage as when it entered power-down; however, the clock frequency is allowed to change (see Precharge Power-Down Clock Frequency Change (page 126)).

The maximum duration for either active or precharge power-down is limited by the refresh requirements of the device ^{t}RFC (MAX). The minimum duration for power-down entry and exit is limited by the ^{t}CKE (MIN) parameter. The following must be maintained while in power-down mode: CKE LOW, a stable clock signal, and stable power supply signals at the inputs of the DDR2 SDRAM. All other input signals are “Don’t Care” except ODT. Detailed ODT timing diagrams for different power-down modes are shown in Figure 83 (page 131)–Figure 88 (page 135).

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command), as shown in Figure 70 (page 120).

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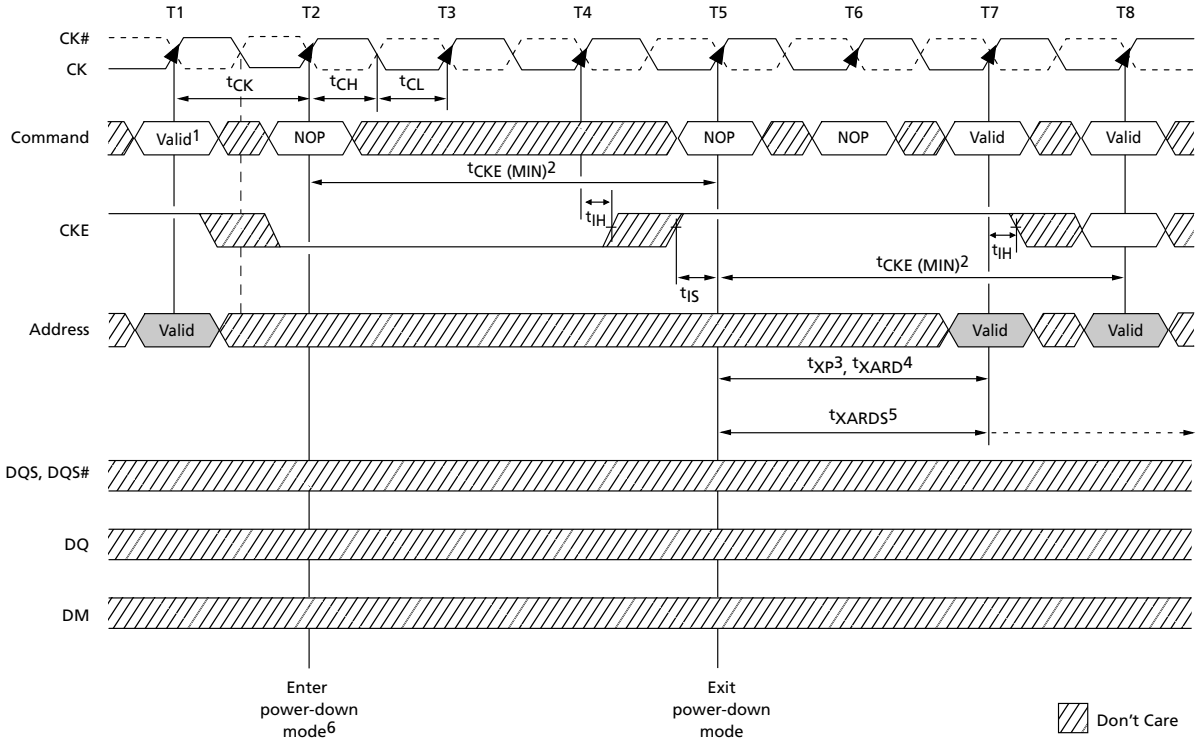
Figure 70: Power-Down



Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVATE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. ^{t}CKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 × ^{t}CK + ^{t}IH. CKE must not transition during its ^{t}IS and ^{t}IH window.
3. ^{t}XP timing is used for exit precharge power-down and active power-down to any non-READ command.
4. ^{t}XARD timing is used for exit active power-down to READ command if fast exit is selected via MR (bit 12 = 0).
5. ^{t}XARDS timing is used for exit active power-down to READ command if slow exit is selected via MR (bit 12 = 1).
6. No column accesses are allowed to be in progress at the time power-down is entered. If the DLL was not in a locked state when CKE went LOW, the DLL must be reset after exiting power-down mode for proper READ operation.

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Table 44: Truth Table – CKE

Notes 1–4 apply to the entire table

Current State	CKE		Command (*n*) CS#, RAS#, CAS#, WE#	Action (*n*)	Notes
	Previous Cycle (*n* - 1)	Current Cycle (*n*)			
Power-down	L	L	X	Maintain power-down	5, 6
	L	H	DESELECT or NOP	Power-down exit	7, 8
Self refresh	L	L	X	Maintain self refresh	6
	L	H	DESELECT or NOP	Self refresh exit	7, 9, 10
Bank(s) active	H	L	DESELECT or NOP	Active power-down entry	7, 8, 11, 12
All banks idle	H	L	DESELECT or NOP	Precharge power-down entry	7, 8, 11
	H	L	Refresh	Self refresh entry	10, 12, 13
	H	H	Shown in Table 37 (page 72)		14

Notes:
1. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n* - 1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge *n*.
3. Command (*n*) is the command registered at clock edge *n*, and action (*n*) is a result of command (*n*).
4. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh (see ODT Timing (page 129) for more details and specific restrictions).
5. Power-down modes do not perform any REFRESH operations. The duration of power-down mode is therefore limited by the refresh requirements.
6. "X" means "Don't Care" (including floating around V_{REF}) in self refresh and power-down. However, ODT must be driven high or low in power-down if the ODT function is enabled via EMR.
7. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
8. Valid commands for power-down entry and exit are NOP and DESELECT only.
9. On self refresh exit, DESELECT or NOP commands must be issued on every clock edge occurring during the ^{t}XSNR period. READ commands may be issued only after ^{t}XSRD (200 clocks) is satisfied.
10. Valid commands for self refresh exit are NOP and DESELECT only.
11. Power-down and self refresh can not be entered while READ or WRITE operations, LOAD MODE operations, or PRECHARGE operations are in progress. See SELF REFRESH (page 117) and SELF REFRESH (page 78) for a list of detailed restrictions.
12. Minimum CKE high time is ^{t}CKE = 3 × ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 × ^{t}CK. This requires a minimum of 3 clock cycles of registration.
13. Self refresh mode can only be entered from the all banks idle state.
14. Must be a legal command, as defined in Table 37 (page 72).

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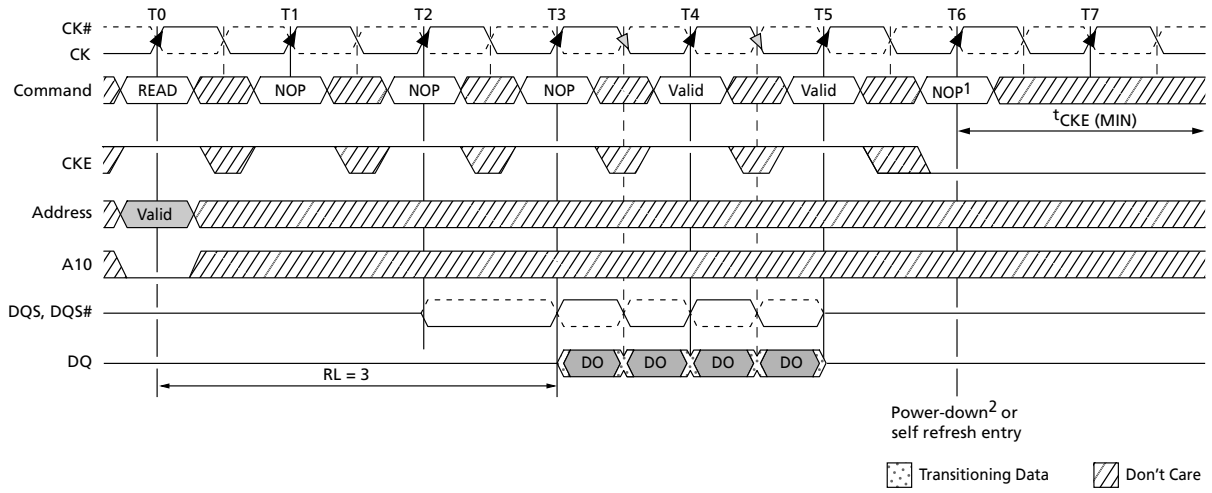
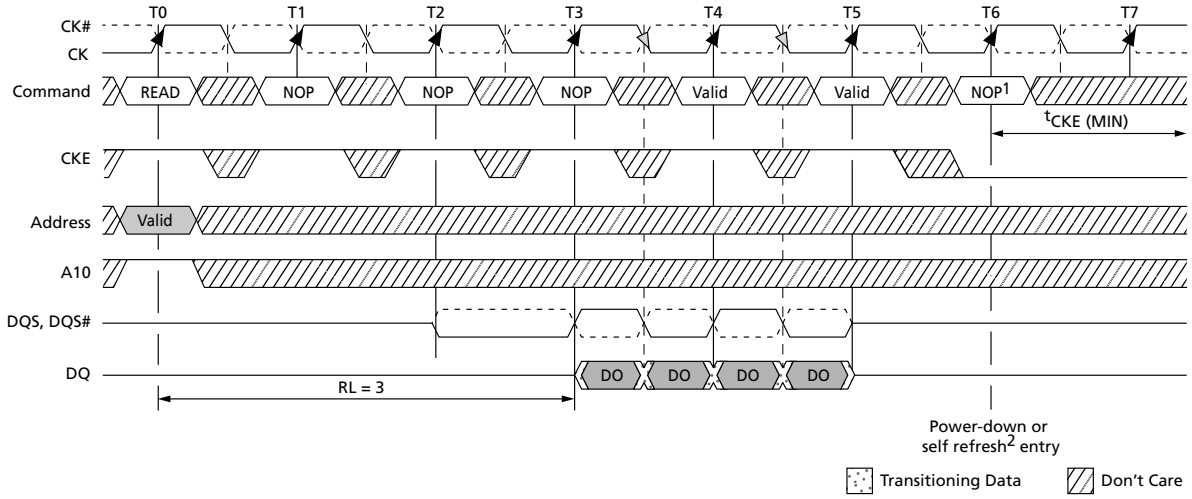
Figure 71: READ-to-Power-Down or Self Refresh Entry



Notes: 1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

Figure 72: READ with Auto Precharge-to-Power-Down or Self Refresh Entry



Notes: 1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

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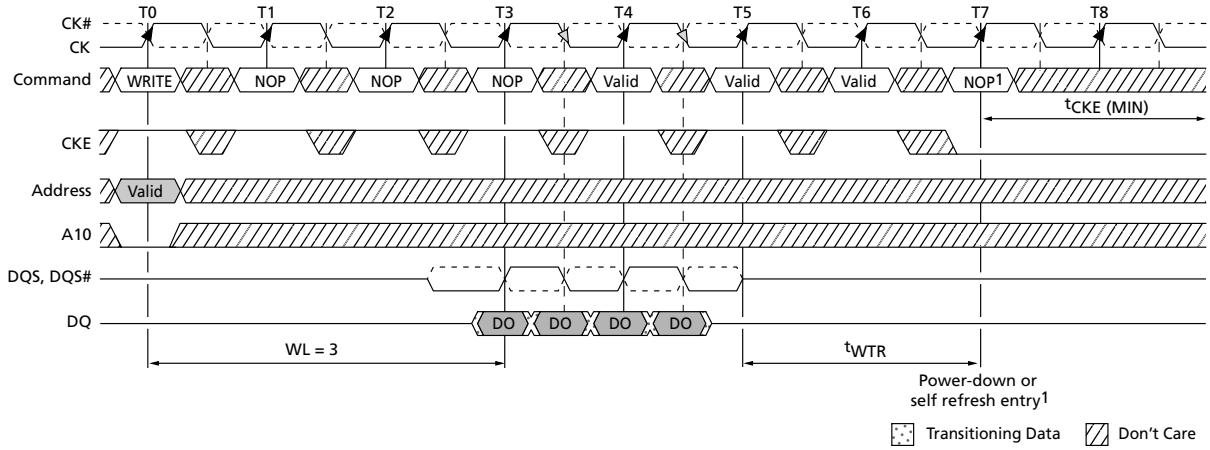
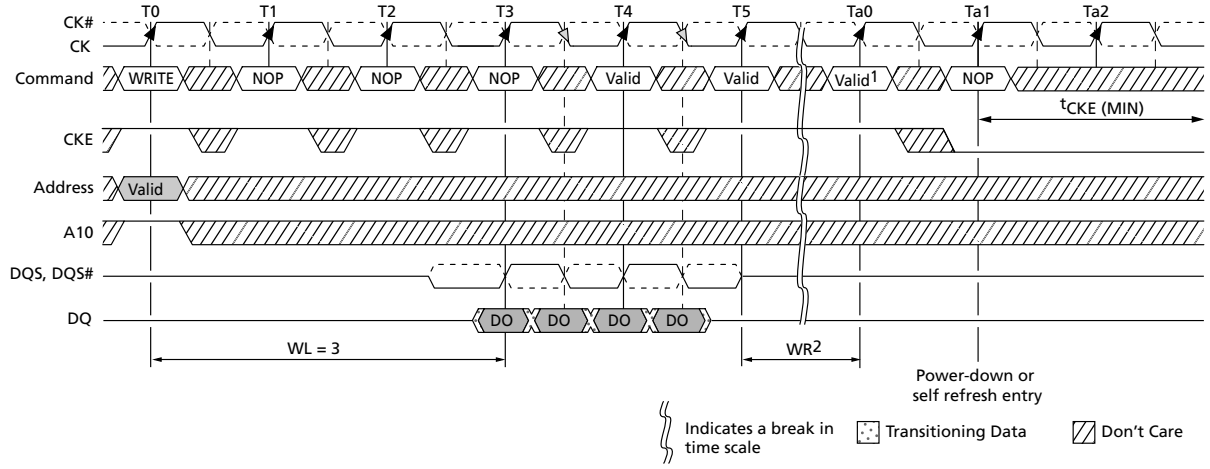
Figure 73: WRITE-to-Power-Down or Self Refresh Entry



Note: 1. Power-down or self refresh entry may occur after the WRITE burst completes.

Figure 74: WRITE with Auto Precharge-to-Power-Down or Self Refresh Entry



Notes: 1. Internal PRECHARGE occurs at Ta0 when WR has completed; power-down entry may occur 1 x ^{t}CK later at Ta1, prior to ^{t}RP being satisfied.
2. WR is programmed through MR9–MR11 and represents (^{t}WR [MIN] ns/^{t}CK) rounded up to next integer ^{t}CK.

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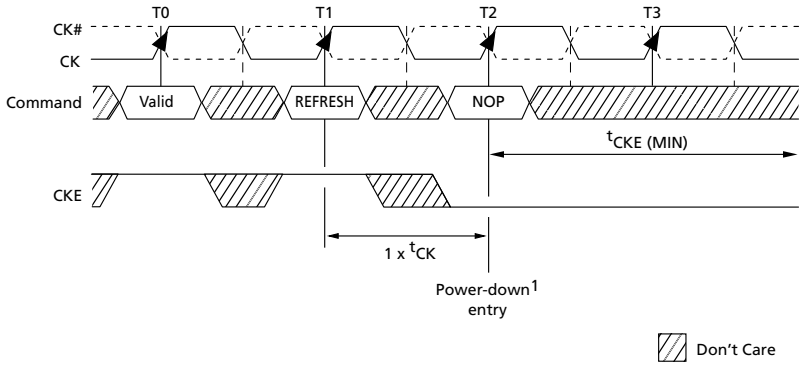
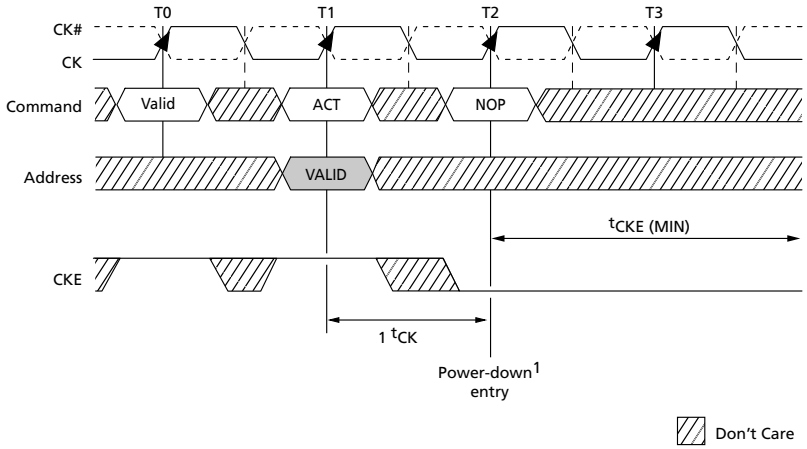
Figure 75: REFRESH Command-to-Power-Down Entry



Note: 1. The earliest precharge power-down entry may occur is at T2, which is 1 × ^{t}CK after the REFRESH command. Precharge power-down entry occurs prior to ^{t}RFC (MIN) being satisfied.

Figure 76: ACTIVATE Command-to-Power-Down Entry



Note: 1. The earliest active power-down entry may occur is at T2, which is 1 × ^{t}CK after the ACTIVATE command. Active power-down entry occurs prior to ^{t}RCD (MIN) being satisfied.

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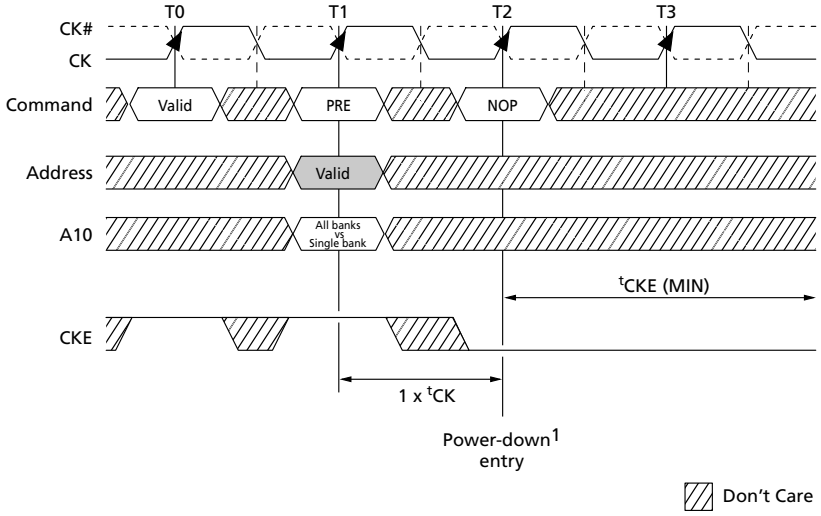
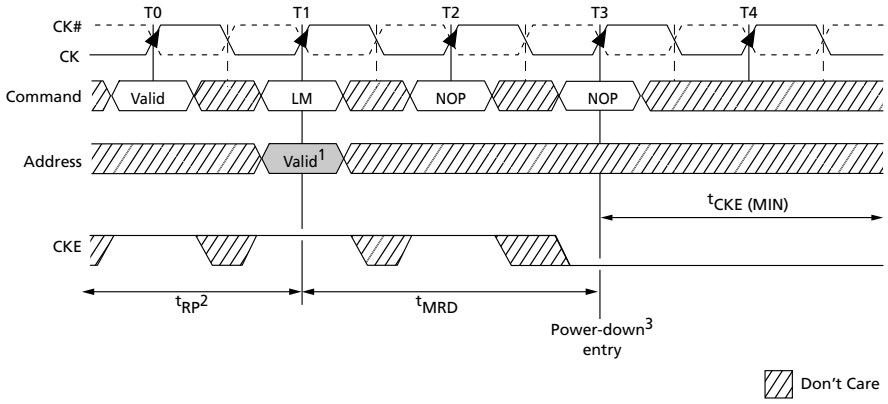
Figure 77: PRECHARGE Command-to-Power-Down Entry



Note: 1. The earliest precharge power-down entry may occur is at T2, which is 1 × ^{t}CK after the PRECHARGE command. Precharge power-down entry occurs prior to ^{t}RP (MIN) being satisfied.

Figure 78: LOAD MODE Command-to-Power-Down Entry



Notes: 1. Valid address for LM command includes MR, EMR, EMR(2), and EMR(3) registers.
2. All banks must be in the precharged state and ^{t}RP met prior to issuing LM command.
3. The earliest precharge power-down entry is at T3, which is after ^{t}MRD is satisfied.

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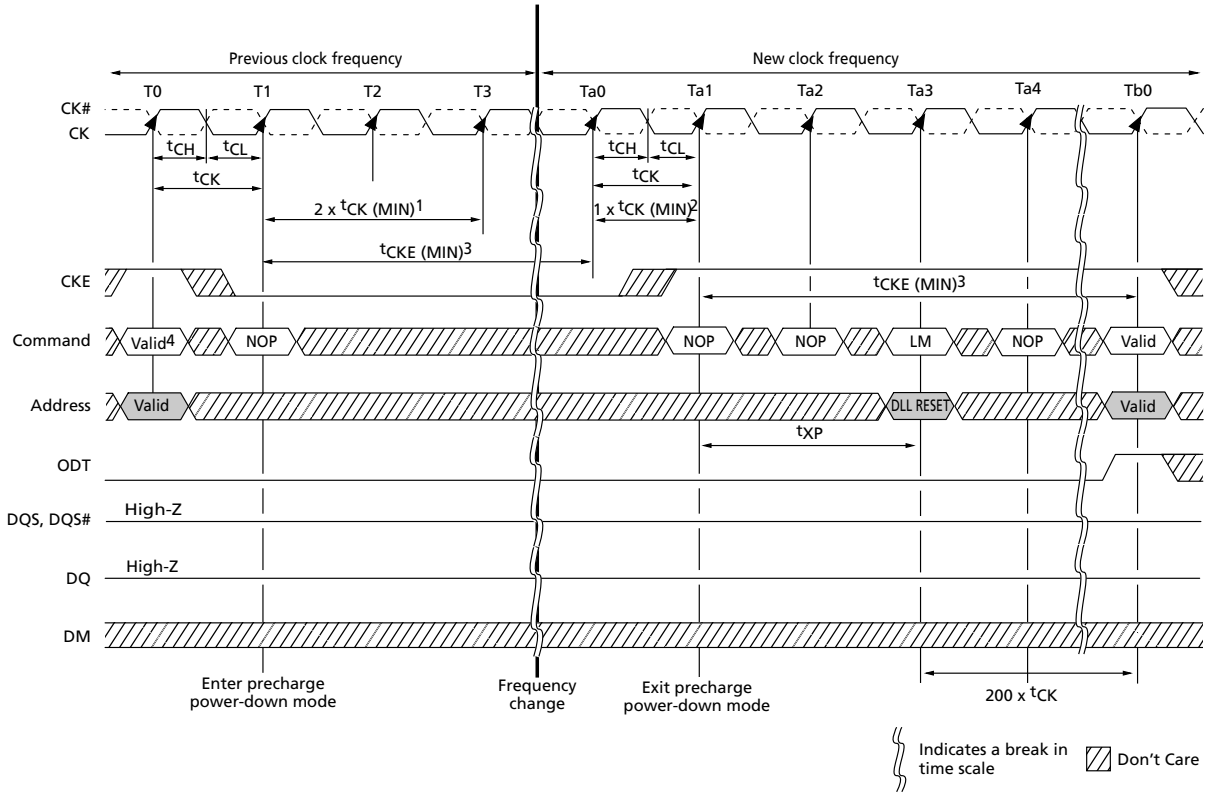
Precharge Power-Down Clock Frequency Change

When the DDR2 SDRAM is in precharge power-down mode, ODT must be turned off and CKE must be at a logic LOW level. A minimum of two differential clock cycles must pass after CKE goes LOW before clock frequency may change. The device input clock frequency is allowed to change only within minimum and maximum operating frequencies specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. When the input clock frequency is changed, new stable clocks must be provided to the device before precharge power-down may be exited, and DLL must be reset via MR after precharge power-down exit. Depending on the new clock frequency, additional LM commands might be required to adjust the CL, WR, AL, and so forth. Depending on the new clock frequency, an additional LM command might be required to appropriately set the WR MR9, MR10, MR11. During the DLL relock period of 200 cycles, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

Figure 79: Input Clock Frequency Change During Precharge Power-Down Mode



Notes:
1. A minimum of 2 × ^{t}CK is required after entering precharge power-down prior to changing clock frequencies.
2. When the new clock frequency has changed and is stable, a minimum of 1 × ^{t}CK is required prior to exiting precharge power-down.

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3. Minimum CKE high time is ^{t}CKE = 3 × ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 × ^{t}CK. This requires a minimum of three clock cycles of registration.
4. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down, which is required prior to the clock frequency change.

Reset

CKE Low Anytime

DDR2 SDRAM applications may go into a reset state anytime during normal operation. If an application enters a reset condition, CKE is used to ensure the DDR2 SDRAM device resumes normal operation after reinitializing. All data will be lost during a reset condition; however, the DDR2 SDRAM device will continue to operate properly if the following conditions outlined in this section are satisfied.

The reset condition defined here assumes all supply voltages (V_{DD}, V_{DDQ}, V_{DDL}, and V_{REF}) are stable and meet all DC specifications prior to, during, and after the RESET operation. All other input balls of the DDR2 SDRAM device are a "Don't Care" during RESET with the exception of CKE.

If CKE asynchronously drops LOW during any valid operation (including a READ or WRITE burst), the memory controller must satisfy the timing parameter ^{t}DELAY before turning off the clocks. Stable clocks must exist at the CK, CK# inputs of the DRAM before CKE is raised HIGH, at which time the normal initialization sequence must occur (see Initialization). The DDR2 SDRAM device is now ready for normal operation after the initialization sequence. Figure 80 (page 128) shows the proper sequence for a RESET operation.

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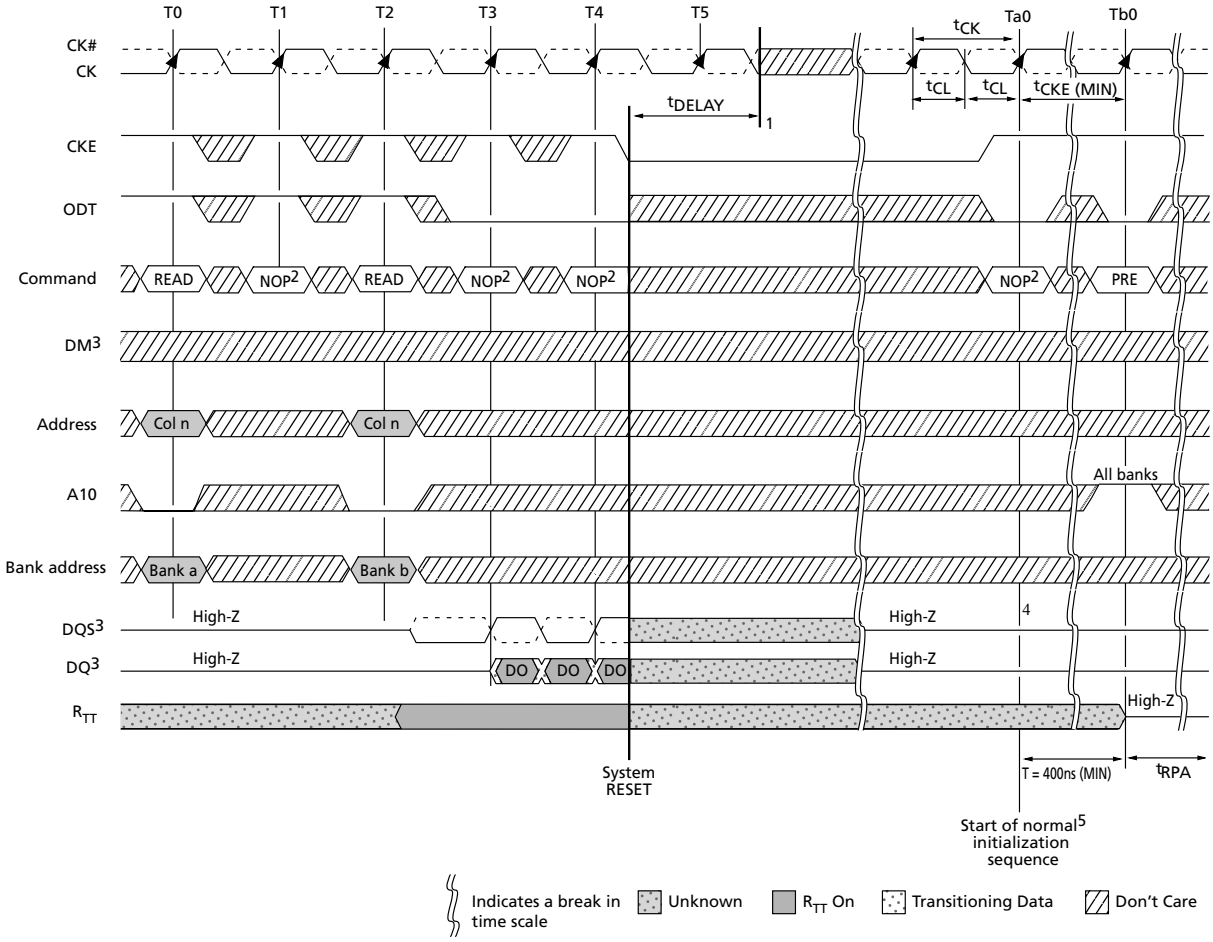
Figure 80: RESET Function



Notes:
1. V_{DD}, V_{DDL}, V_{DDQ}, V_{TT}, and V_{REF} must be valid at all times.
2. Either NOP or DESELECT command may be applied.
3. DM represents DM for x4/x8 configuration and UDM, LDM for x16 configuration. DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, and RDQS# for the appropriate configuration (x4, x8, x16).
4. In certain cases where a READ cycle is interrupted, CKE going HIGH may result in the completion of the burst.
5. Initialization timing is shown in Figure 43 (page 89).

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ODT Timing

Once a 12ns delay (^{t}MOD) has been satisfied, and after the ODT function has been enabled via the EMR LOAD MODE command, ODT can be accessed under two timing categories. ODT will operate either in synchronous mode or asynchronous mode, depending on the state of CKE. ODT can switch anytime except during self refresh mode and a few clocks after being enabled via EMR, as shown in Figure 81 (page 130).

There are two timing categories for ODT—turn-on and turn-off. During active mode (CKE HIGH) and fast-exit power-down mode (any row of any bank open, CKE LOW, MR[12 = 0]), ^{t}AOND, ^{t}AON, ^{t}AOFD, and ^{t}AOF timing parameters are applied, as shown in Figure 83 (page 131).

During slow-exit power-down mode (any row of any bank open, CKE LOW, MR[12] = 1) and precharge power-down mode (all banks/rows precharged and idle, CKE LOW), ^{t}AONPD and ^{t}AOFPD timing parameters are applied, as shown in Figure 84 (page 132).

ODT turn-off timing, prior to entering any power-down mode, is determined by the parameter ^{t}ANPD (MIN), as shown in Figure 85 (page 132). At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 85 (page 132) also shows the example where ^{t}ANPD (MIN) is **not** satisfied because ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is **not** satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing prior to entering any power-down mode is determined by the parameter ^{t}ANPD, as shown in Figure 86 (page 133). At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 86 (page 133) also shows the example where ^{t}ANPD (MIN) is **not** satisfied because ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is **not** satisfied, ^{t}AONPD timing parameters apply.

ODT turn-off timing after exiting any power-down mode is determined by the parameter ^{t}AXPD (MIN), as shown in Figure 87 (page 134). At state Ta1, the ODT LOW signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 87 (page 134) also shows the example where ^{t}AXPD (MIN) is **not** satisfied because ODT LOW occurs at state Ta0. When ^{t}AXPD (MIN) is not satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing after exiting either slow-exit power-down mode or precharge power-down mode is determined by the parameter ^{t}AXPD (MIN), as shown in Figure 88 (page 135). At state Ta1, the ODT HIGH signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 88 (page 135) also shows the example where ^{t}AXPD (MIN) is not satisfied because ODT HIGH occurs at state Ta0. When ^{t}AXPD (MIN) is not satisfied, ^{t}AONPD timing parameters apply.

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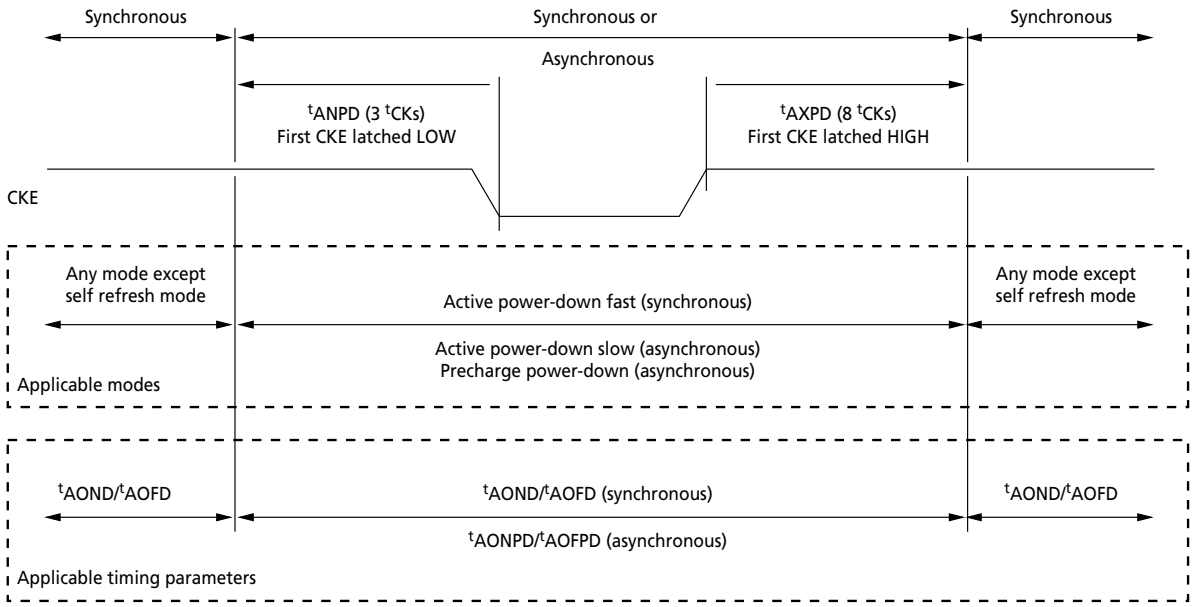
Figure 81: ODT Timing for Entering and Exiting Power-Down Mode



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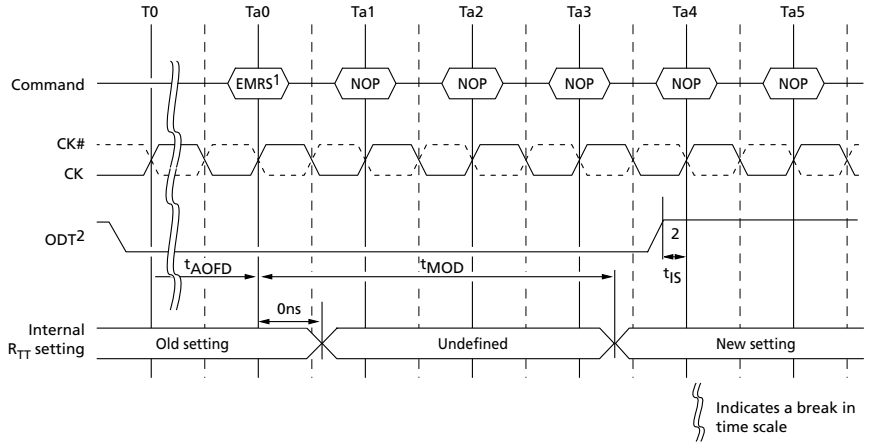
MRS Command to ODT Update Delay

During normal operation, the value of the effective termination resistance can be changed with an EMRS set command. ^{t}MOD (MAX) updates the R_{TT} setting.

Figure 82: Timing for MRS Command to ODT Update Delay



Notes: 1. The LM command is directed to the mode register, which updates the information in EMR (A6, A2), that is, R_{TT} (nominal).
2. To prevent any impedance glitch on the channel, the following conditions must be met: ^{t}AOFD must be met before issuing the LM command; ODT must remain LOW for the entire duration of the ^{t}MOD window until ^{t}MOD is met.

Figure 83: ODT Timing for Active or Fast-Exit Power-Down Mode

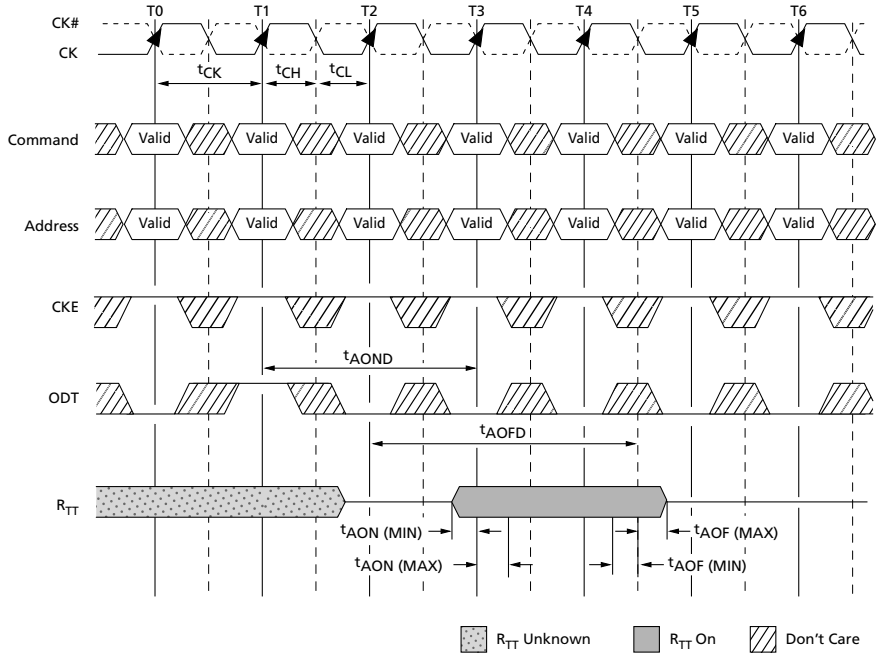


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Figure 84: ODT Timing for Slow-Exit or Precharge Power-Down Modes

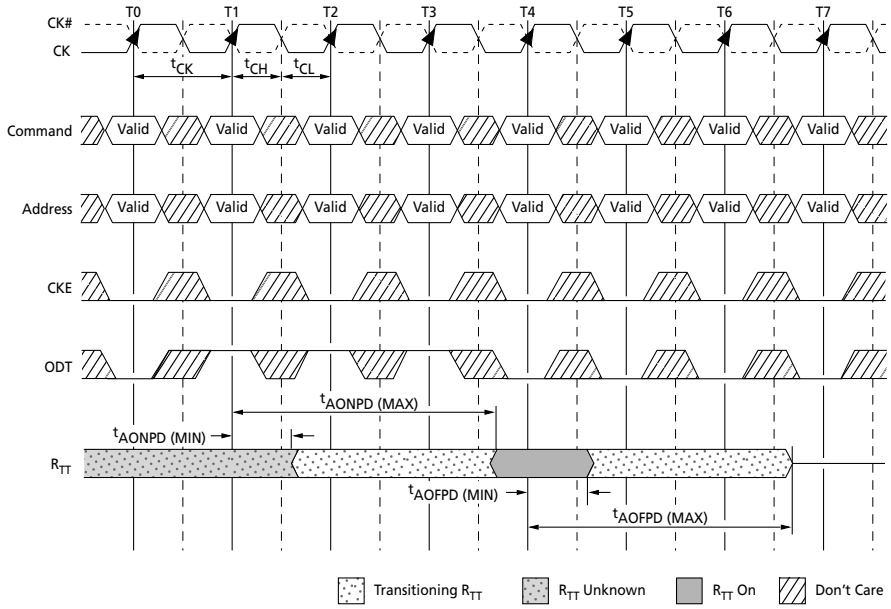

Figure 85: ODT Turn-Off Timings When Entering Power-Down Mode

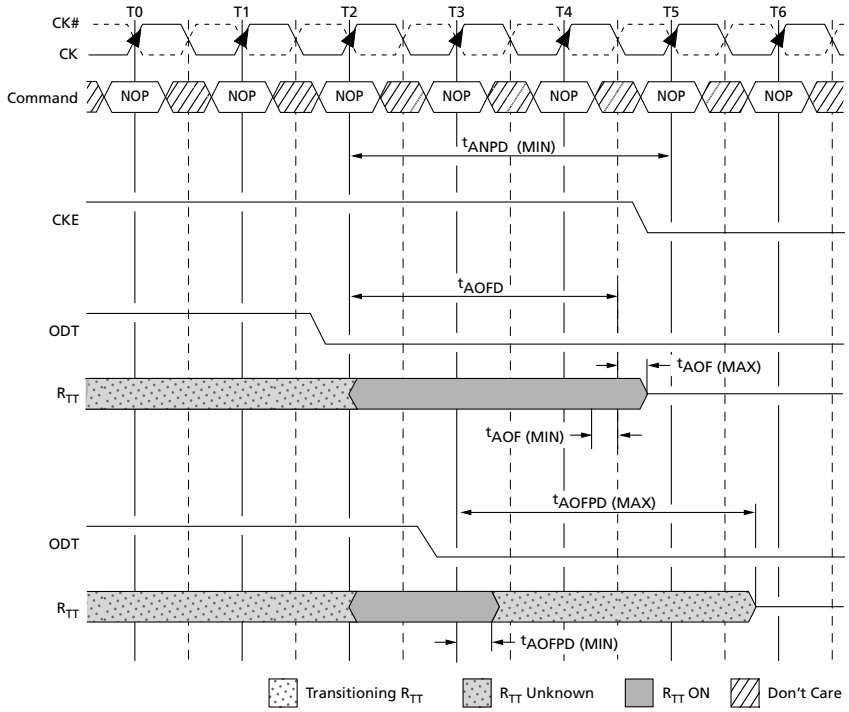

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Figure 86: ODT Turn-On Timing When Entering Power-Down Mode

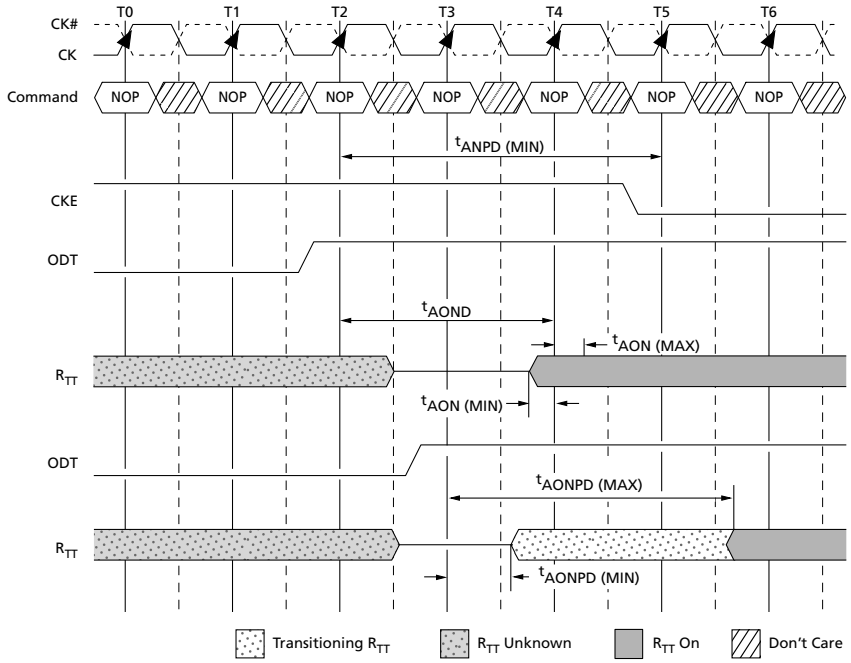

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Figure 87: ODT Turn-Off Timing When Exiting Power-Down Mode

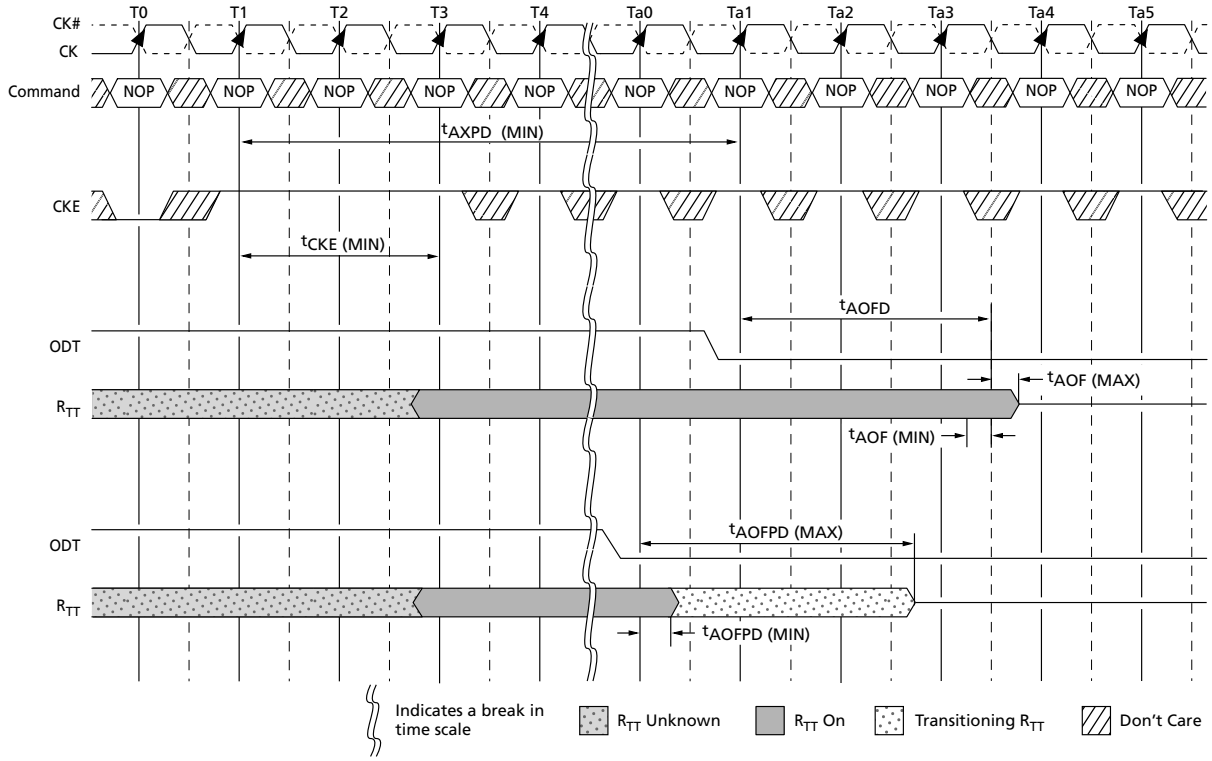

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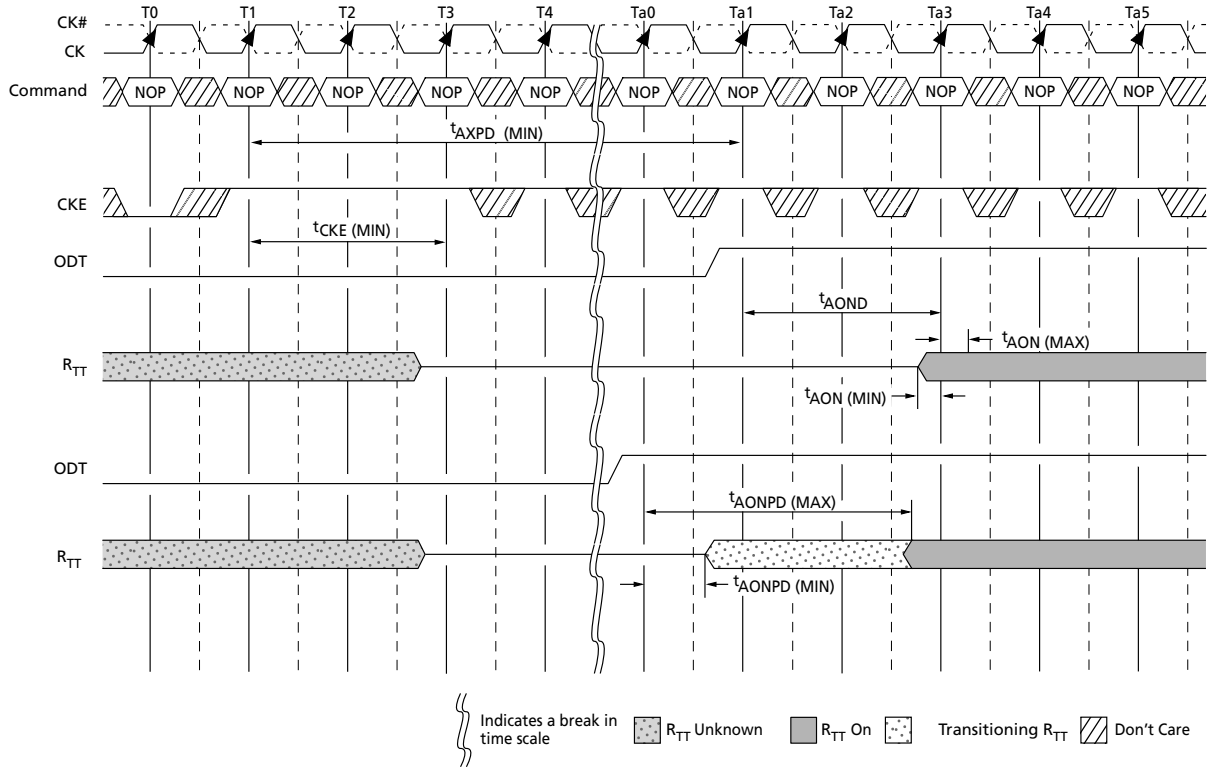
Figure 88: ODT Turn-On Timing When Exiting Power-Down Mode



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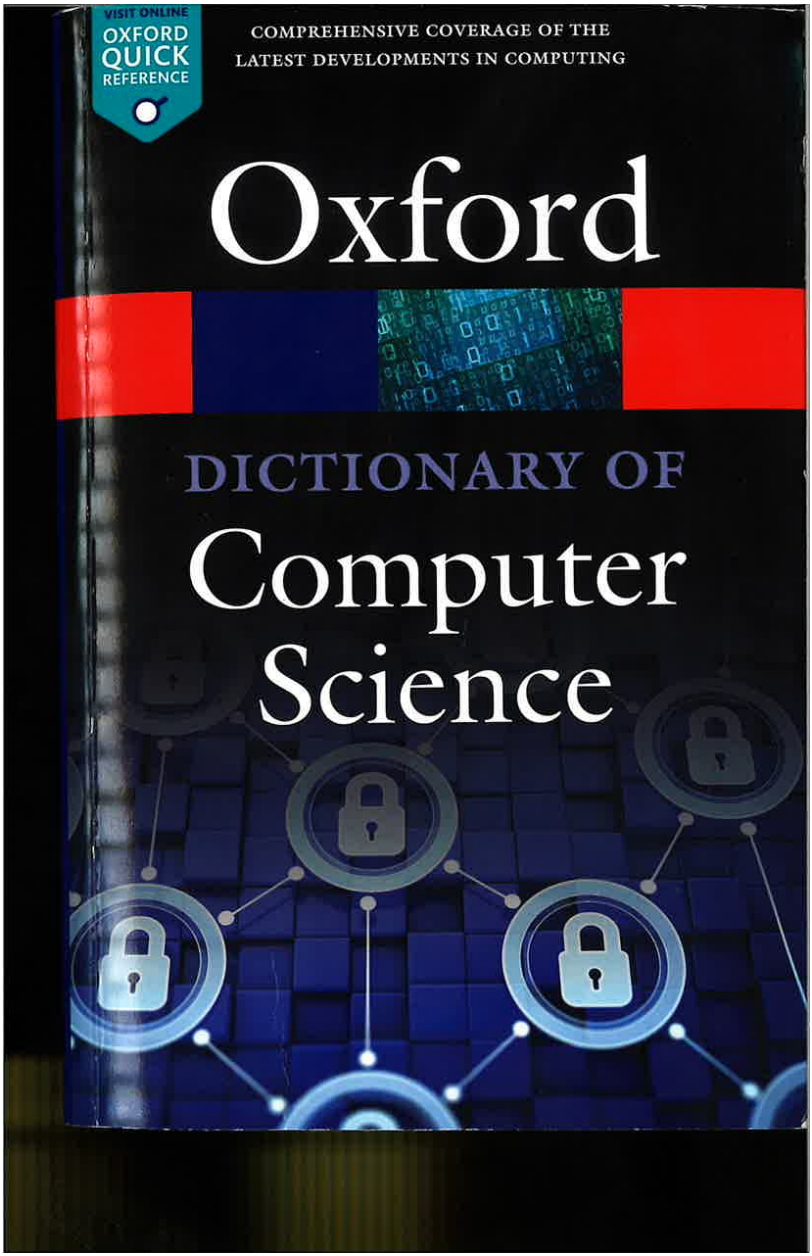
Appendix C



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the nonexhausted and previous-destination files. When there is only one file left the process stops. The repeated merging is referred to as **polyphase merging**.

PON *Abbrev. for* passive optical network.

pop *See* STACK.

PoP (point of presence) An access point to the Internet, either the geographical location or, as a technical term, the equipment that supports the Internet access hardware and software.

POP (post office protocol) A protocol that defines the communication between an email client and a utility that can accept email on behalf of a user, holding it until such time as the user wishes to recover the messages. Version 3 (**POP3**) is the standard protocol for this on the Internet. *See also* IMAP.

POP-2 A programming language developed by the University of Edinburgh (UK) for research in *artificial intelligence. POP-2 provided the facility to manipulate the linked data structures characteristic of *Lisp, but retained a more familiar procedural structure, and was thus more accessible to programmers raised in the Algol environment of the time. *POP-11 is a modern version of POP-2.

POP-11 A programming language for artificial intelligence that claims to combine *Lisp and *POP-2.

POP3 *See* POP.

P operation (down operation) *See* SEMAPHORE.

POPL (Principles of Programming Languages) Title of an annual conference organized by the *ACM at which the results of much research in programming languages are announced.

POPLOG A programming environment combining *POP-11 and *Prolog.

population *See* SAMPLING.

pop-up A web page, often containing advertisements, that appears unexpectedly when a user is browsing.

pop-up menu A *menu that appears on the display when the user changes the state of a *button or makes a selection from a *menu bar. The menu item is selected by pointing to and clicking the desired entry.

port 1. (I/O port) A connection point with associated control circuitry that allows I/O devices to be connected to the internal bus of a microprocessor. *See also* PARALLEL PORT, SERIAL PORT, COMMUNICATION PORT. **2.** A point through which data can enter or leave a *network, either on the network or the *DTE (computer) interface. **3.** To move software from one type of computer system to another, making any necessary changes en route. In a simple case little more than recompilation may be required, while in extreme cases the software might have to be entirely rewritten.

portable 1. *Another word for* machine-independent. **2.** A word applied to software that can readily be transferred to other machines, although not actually *machine-independent. **3.** A computer that can be simply carried from one place to another by one person. They cannot necessarily be used in transit. Examples include *laptop computers.

portable network graphics *See* PNG.

portal A website that seeks to act as an attractive user-friendly access point to the Internet. Portals typically provide services (email, instant messaging, games, online shopping, etc.), content (news, listings of events, etc.), facilities for online shopping, and a *search engine to search the rest of the Web.

portrait An orientation of a page in which the shorter side is at the top. *Compare* LANDSCAPE.

POS (point of sale) *See* POINT-OF-SALE SYSTEM.

poset *Short for* partially ordered set. *See* PARTIAL ORDERING.

POS expression *Short for* product of sums expression.

positional system *See* NUMBER SYSTEM.

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Actually, the two servers may well be in the form of one physical server, logically partitioned into two. So, when I access my main email account at www.TechnologyInvestor.com, using my main email address of Harry_Newton@TechnologyInvestor.com, I access a local Internet POP (Point Of Presence). I can use a dial up connection through a modem, or DSL (Digital Subscriber Line), or a cable modem network to access the Internet. Anyway is fine. In any event, I run my laptop running the TCP/IP protocol stack and POP3 software against a technologyinvestor.com server running the same software. Once I connect to my server, all of my email downloads immediately, whether I want all of it or not. This all or nothing approach is a major drawback of POP3. If I set up the POP3 options correctly on the client workstation, I can choose to leave a copy of the mail on the server. That way, I can check my email from a friend's or colleague's computer when I'm away from my office, and can still view the mail from my own computer when I get back. POP3 also helps solve the problem of accessing my email when I'm on the road, and outside the local calling areas of my ISP. Let's say I'm in Singapore and I want to check my email. I jump onto the Internet, using any local Internet Service Provider (ISP). I then instruct my email client (in my case, it's Microsoft Outlook.) to go find my technologyinvestor POP3 email server, the address of which happens to be email.technologyinvestor.com. It finds that server. The server asks me to identify myself by user name and password. Then it starts sending me my email. POP3 is particularly useful because I can pick up my email from wherever I am in the world — just so long as I can get on the Internet in some way. IMAP (Internet Message Access Protocol) is an improvement on POP3, but is not widely implemented. When you are choosing an email provider, make sure that email provider places your email on a POP3 server and that you can retrieve your email from anywhere. Some companies claim to have "POP3" servers but, for some reason (technical, security or incompetence), they don't allow you grab your mail over the Internet and download it to your machine. Some email providers insist that you be on line to read and respond to your email. When I wrote an article on the subject of POP3 servers, many readers wrote me that there are "POP3" and "POP3" servers. Thus my warning to check. See also DNS, IMAP, IP, ISP, SMTP, and TCP/IP.

Pop-Under Also called Pop-Up advertisements. You got to a web site with your browser. You close your browser. Bingo, your taskbar shows your browser has visited another "site" and it's — surprise, surprise — an advertisement for a piece of hardware, a cheap airline trip, a lottery, a casino....usually something you don't want. It's called a pop-under because it pops under your browser. It's also very annoying. Companies pay for the privilege of buying these ads. A good piece of software which gets rid of Pop-Unders is called AdsGone and is available from www.AdsGone.com.

Pop-Up A call center term. A button that displays, on demand, several items from which you can choose (by clicking on it, for example). In effect, this is a list box that you don't see until you push button. Pop-ups always have double lines on their right and bottom sides.

Pop-Up Ad A typically annoying Web-based advertising technique in which Javascript code creates a small Web browser window that suddenly "pops up" in the foreground of the visual interface. Pop-ups can contain graphics, HTML, animation, or any combination of the three. Software to prevent pop-ups is available. Our favorite is AdsGone, available from www.AdsGone.com. See Inline ads.

Pop-Up Electronic Mail An electronic mail system that runs as a terminate-and-stay-resident program (typically within DOS) and can be popped up inside any application to send or read mail. Our office, we have a TSR electronic mail program that pops up. It is called Noteworks and we really love it.

Pop-Up Program A memory-resident program that is loaded into memory but isn't visible until you press a certain key combination or until a certain event occurs, such as receiving a message. See also TSR.

POPS A cellular industry term for its customers or its potential customers. (It varies with usage.) POPS, short for "population" (well, sort of) refers to members of the population. According to Ron Schneiderman's book on Wireless, "if the coverage area of a cellular carrier include a popular base of one million people, it is said to have one million POPS. The financial community uses the number of potential users as measuring stick to value cellular carriers."

Populate The classic definition of "to populate" is to furnish with inhabitants. To populate printed circuit board, you fill it with semiconductors, capacitors and other components. To populate fields in a form, you (or your computer) fill them in.

PORPX Federal Charge, local number port.

Port 1. noun. The physical interface between a device and a circuit. The device may be a system (e.g., a mainframe, PC, or other host computer), a switch (e.g., PBX, Central Office, or ATM switch) or router, a hub or bridge, a buffer, a printer or other peripheral, or virtually any other type of device. The port and circuit may be either digital or analog, and either electrical (e.g., twisted pair or coaxial cable) or optical (e.g., optical fiber) in nature. The port and circuit connect through some sort of plug and socket arrangement. For example, your PC typically has one or more serial ports and a parallel port.

2. noun. The logical interface between a process or program and a communications or transmission facility. One or more logical ports (Lports) are associated with a single physical port. See also Logical Port

3. noun. A logical point of connection, most especially in the context of TCP (Transmission Control Protocol, which is part of the TCP/IP protocol suite developed for what we now know as the Internet. Port numbers are 16-bit values which range from 0 to 65,536. "Well-known ports" are numbered 0 to 1,023, and assigned by the IANA (Internet Assigned Numbers Authority) for the use of system (root) processes or by programs executed by "privileged users." Examples of well-known ports include 25 for SMTP (Simple Mail Transfer Protocol), 80 for HTTP (HyperText Transport Protocol), and 107 for Remote Telnet Service). In the Internet TCP/IP-based client/server environment the ports are assigned by the server in consideration of the application-level protocol being exercised at the client level. In Internet terms, it is the identifier (16-bit unsigned integer) used by Internet transport protocols to distinguish among multiple simultaneous connections to a single destination host. "Ephemeral ports" are short-lived ports assigned randomly to the source port of the sender, or client. Ephemeral port numbers usually have a value between 1,024 and 5,000. Their short life is due to the fact that the client normally stops using the randomly selected port number once the transaction or session is completed. See also HTTP, IANA, SMTP, TCP, TCP/IP, and Telnet.

4. verb. To move a process, program or subroutine from one processor, controller, or operating system to another. For example, a software developer might "port" an application software system from UNIX to Windows NT.

Port 25 Blocking ISP use "port 25 blocking" to prevent their subscribers accessing "foreign" SMTP servers, i.e. using other SMTP email servers to send our their mail. The reason? So ISPs can stop their customers spamming. The real reason? To reduce traffic on their network. See Port Services.

Port Address Translation PAT. A feature which lets you number a LAN (a local area network) with inside local addresses and filter them through one globally routable IP address. Here's an example of when you would use this. Let's say that you have subscribed at your home to a DSL line to the Internet from your local CLEC. For $80 a month you get a line and one IP address. (To get more IP addresses would cost you more money.) You would like to attach several PCs to the line — your wife's PC, your son's PC, etc. You attach a router to your "digital modem" which your DSL line is terminated on. That router has PAT. It essentially assigns IP addresses behind the DSL. You assign these separate IP addresses to each of your PCs, install cheap Ethernet hubs to joint the PCs together in a LAN and bingo you have a bunch of PCs able to access the Internet. I have exactly this configuration at my home. The device which does the Port Address Translation is a Cisco 1605R router. Companies also use PAT to use one set of IP addresses for internal traffic and a second set of addresses for external traffic. This allows a company to shield internal PCs from the outside world. None of these machines can be reached from the Internet. They can only access the Internet, surf, send email, etc. Port Address Translation is sometimes called Network Address Translation (NAT).

Port Aliasing Imagine a switch on a local area network. It switches one port to another via a common backplane. We're having trouble and we're looking to do some diagnosis. So we grab all the information flowing through the switch and mirror it (i.e. forward it, but keep it going elsewhere in the switch) to a special port, which we can hook up equipment to and then monitor and check for problems in the resulting data flow — errors in packets, etc.

Port Connection The point of entry into a public frame relay network service.

Port Density The number of ports, physical or logical, per network device.

Port Group A collection of switch interfaces through which packets can be switched. Port groupings can be distinct for different types of destination addresses: multicast, broadcast, and unicast sprays.

Port Identifier The identifier assigned by a logical node to represent the point of attachment of a link to that node.

Port Level VLAN VLAN based on source port ID. This is a multiple bridge configuration of a switch.

Port Multiplier A local area network interconnect, a concentrator providing connection to a network for multiple devices.

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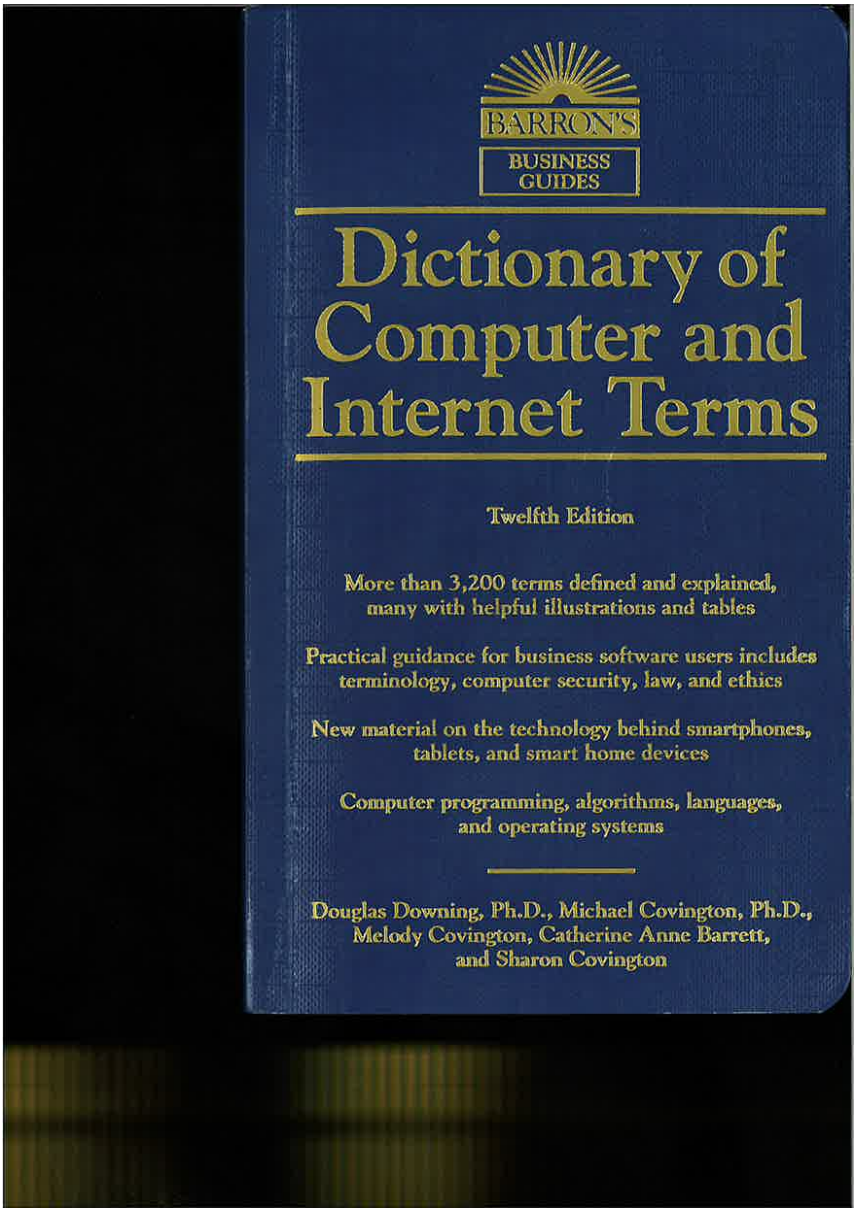

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In the United States, most of the pornography on the Internet is legal, but sexually explicit images of children are not, and images of sexual behavior may not be legal, depending on local laws. (*See* COMPUTER LAW; CIPA; OBSCENITY.) Law enforcement is hampered by the difficulty of determining the physical locations of web sites. Note, however, that because the laws prohibit *distribution* of obscene material, a link to an obscene site can itself be illegal.

There have been various efforts to keep pornography from reaching children and unwilling audiences. The Communications Decency Act of 1996 was struck down because it assumed, incorrectly, that Internet service providers can control the information sent through their computers; replacement legislation has been proposed. Schools and libraries sometimes use "filtering" software to block access to known pornographic web sites, but the filtering process is imperfect.

Pornography is associated with credit card fraud and other crimes. Several Internet pornography vendors have been caught making unauthorized charges to credit card numbers, presumably expecting the victims to be too embarrassed to complain. In some cases the numbers were stolen or made up and belonged to people who had never had any contact with the vendors.

It is naive to describe pornography as "victimless." The most obvious victims are the individuals who become addicted, and whose relationships and even marriages are damaged. The young people hired to pose for pornographic pictures are also victims of exploitation.

port

1. to adapt a program from one kind of computer to another. For example, some PC programs have been ported to the Mac.

2. a connection where a computer can be connected to an external device, such as a printer, flash drive, or digital camera. *See* PARALLEL; SCSI; SERIAL; USB.

3. a unique number used by a microprocessor to identify an input-output device.

4. a number identifying the type of connection requested by a remote computer on the Internet. *See* URL.

port replicator a DOCKING STATION for a portable computer that contains serial and parallel ports (and perhaps other ports, such as USB) which substitute for those in the computer itself.

portable

1. able to be carried around. A portable computer is larger than a laptop computer, but is still easily movable.

2. (said of programs) able to run on more than one type of computer or operating system. *Compare* INTEROPERABILITY.

Portable Document File *see* PDF.