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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner

Case IPR2023-00513

Patent 7,532,523

PATENT OWNER'S RESPONSE

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Timothy D. Dorney, Ph.D. Pursuant to 37 C.F.R. § 1.68
2002	RESERVED
2003	RESERVED
2004	RESERVED
2005	RESERVED
2006	RESERVED
2007	RESERVED
2008	RESERVED
2009	RESERVED
2010	Transcript of the Deposition of R. Jacob Baker, Ph.D., P.E.
2011	Oxford Dictionary of Computer Science, p. 420
2012	Newton's Telecom Dictionary, 19th Edition, p. 624
2013	Barron's Dictionary of Computer and Internet Terms, p. 380

Pursuant to 37 C.F.R. § 42.120, Patent Owner Polaris Innovation Limited (“Polaris” or “Patent Owner”) submits this Response to the Petition of Xilinx, Inc. (“Xilinx” or “Petitioner”) seeking inter partes review of claims 1, 2, 5, 6, 9, and 10 of U.S. Patent No. 7,532,523 (EX1001, the “’523 patent”).

I. INTRODUCTION

The ’523 patent provides a solution to minimize signal reflections in memory chips. At the time of the ’523 patent, signal reflections were known to impair data transmission rates in memory chips. To reduce the impact of such signal reflections, memory chips used terminations. But, as the ’523 patent explains, such terminations were suboptimal. In particular, there was a need to dynamically set the resistance for a termination. The ’523 patent addressed this need by using the control circuit in conjunction with the termination circuit to terminate the terminal in accordance with a settable resistance.

While the prior art in the Petition discloses terminals with settable resistance, it did not use the control circuit to terminate the terminal. Thus, Petitioner’s proposed combinations do not disclose the claimed invention. Because the prior art does not disclose all limitations of the challenged claims, Petitioner has failed to show by a preponderance of the evidence that any challenged claim is obvious.

II. THE '523 PATENT

A. Problem Presented

The '523 patent explains that memory systems normally use “a multiplicity of memory chips that are operated via a memory bus.” EX1001, 1:23-24. The memory bus typically uses signal lines to deliver a variety of signals to the memory chips, including “control command signals, clock signals, data signals and address signals.” *Id.* at 1:24-29. One shortcoming of such an arrangement is that “during transmission of high-frequency signals, signals reflections that disturb the data transmission on the memory bus” can occur. *Id.* at 1:29-31. Such signal reflections have an adverse effect on the memory system because they “limit the data transmission rates.” *Id.* at 1:31-33. The '523 patent explains that terminations within the memory chip can reduce such signal reflections. *Id.* at 1:33-36.

The '523 patent further explains that the use of such terminations in the prior art was sub-optimal. *Id.* at 1:37-49. In particular, the '523 patent describes two prior art implementations of such terminations: (1) switching “the termination on or off at a terminal of the memory chip as a function of a termination signal,” and (2) fixing the resistance of the termination “in accordance with a configuration value that is communicated ... in an initialization phase.” *Id.* at 1:37-39; 1:50-54. The “disadvantage” of the switching approach is that “switching the terminating resistors on and off is not sufficient as a rule to achieve an optimal termination in every

operating state, and thus, also not sufficient to improve the data transmission via the memory bus.” *Id.* at 1:44-49. Similarly, the disadvantage of the fixed resistance approach is that “setting the configuration values in memory before each write and read operation is time consuming,” and, as a result, “the initial presetting of the terminating resistor by the configuration value is also not suitable for providing terminating resistors for applying to the memory bus that are suitable for every case of addressing the memory chips.” *Id.* at 1:54-61. The ’523 patent recognized the limitations of such approaches and provided a solution that allowed for dynamic resistance and reduced signal reflections.

B. Challenged Claims

The claims of the ’523 patent are directed to the solution it presents. Independent claims 1, 5, and 9 are directed to a non-obvious mechanism/method for terminating a terminal with a settable resistance. Petitioner claims 1, 2, 5, 6, 9, and 10 of the ’523 patent (collectively, the “Challenged Claims”). Patent Owner provides the Challenged Claims in full below:

[1.P] A memory chip for variably setting terminations, comprising:

[1.1] a terminal;

[1.2] a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

- [1.3] a control command port for receiving a control command signal for affecting accessibility of the memory chip;
- [1.4] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and
- [1.5] a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,
- [1.6] wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.
- [2.P] The memory chip of claim 1,
- [2.1] wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

...

[5.P] A system, comprising:

[5.1] (a) a memory controller having a terminal;

[5.2] (b) a plurality of memory chips, at least one of the memory chips comprising:

[5.3] a terminal;

[5.4] a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;

[5.5] a control command port for receiving a control command signal for affecting accessibility of the memory chip; and

[5.6] a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;

[5.7] (c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and

[5.8] (d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,

[5.9] wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

[6.P] The system of claim 5,

[6.1] wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

...

[9.P] A method for operating a memory chip, comprising:

[9.1] receiving a control command signal for affecting accessibility of the memory chip;

[9.2] setting a resistance value for a terminal as a function of the control command signal;

[9.3] terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and

[9.4] receiving a termination enable signal, the presence of which is required for the terminating to occur.

[10.P] The method of claim 9, further comprising:

[10.1] changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and

[10.2] terminating the terminal with the changed resistance value.

III. CLAIM CONSTRUCTION

Claim terms subject to *inter partes* review are to be “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Petitioner has not argued for any claim elements to be construed and, for

the purposes of this Response, Patent Owner does not seek the construction of any term. Nevertheless, as detailed in this Response, Patent Owner notes that Petitioner's interpretation of the claims is not consistent with the plain and ordinary meaning of the terms therein.

IV. LEVEL OF SKILL IN THE ART

Petitioner argues that a person of ordinary skill in the art at the time of the '523 patent would have had a "Bachelor of Science degree in Electrical Engineering, Computer Science, or an equivalent field and at least two or three years of academic or industry experience in integrated circuit input/outputs and memory systems, or comparable industry experience." *See* Pet. at 11. For the purposes of this trial, Patent Owner does not dispute Petitioner's proposal for level of ordinary skill in the art.

V. SUMMARY OF THE REFERENCES

A. Bains

Bains (EX1005) is a United States Patent dated October 7, 2008, with a filing date of November 18, 2004. Bains is titled "Command Controlling Different Operations in Different Chips" and generally relates to a system "in which a command causes different operations in different chips." EX1005, 1:7-9. Bains' need for a single command to cause different operations in different chips results from the dual-rank memory system configuration the reference discloses. EX2001, ¶ 57.

As Bains explains, “the term rank refers to a group of memory chips that are selected together.” EX1005, 1:28-29. This is consistent with the industry meaning for the term. EX2001, ¶ 58. Figure 2 in Bains provides an illustration of a dual-rank memory system according to its embodiments.

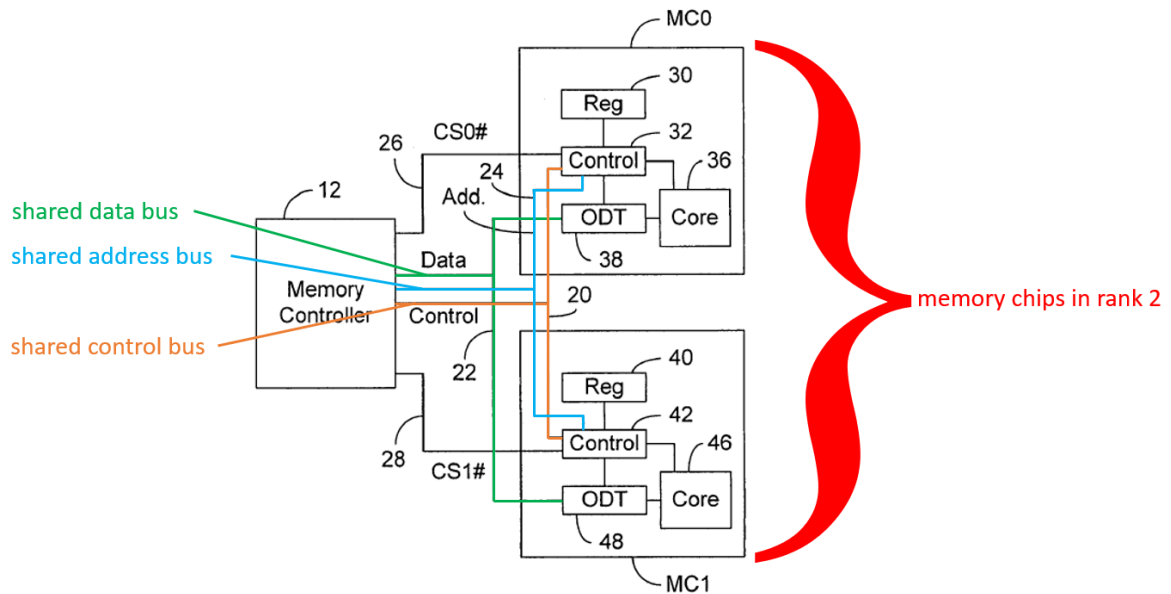


FIG. 2

EX1005, 3:9-4:6, Fig. 2 (annotations added); EX2001, ¶ 58. In the above illustration, memory chips MC0 and MC1 each comprise a rank.

As Bains Figure 2 illustrates, memory chips MC0 and MC1 share common data, address, and control buses; however, MC0 and MC1 respond to different chip select signals (i.e., CS0# and CS1#). EX1005, 3:9-16. This is a common configuration for dual-rank memory systems. EX2001, ¶ 59. As a result, of this configuration, signals sent on these common interconnects are received by both MC0

and MC1. *Id.* Commands sent on control bus 20 are received by MC0 and MC1. *Id.* Similarly, data sent on data bus 22 is received by MC0 and MC1. *Id.* Thus, an instruction to MC0 to write the data on the data bus to memory is simultaneously received by MC1. *Id.* To avoid a duplicative write operation on MC0 and MC1, Bains discloses using different command mappings and an on die termination (“ODT”). EX1005, 2:47-67; 3:37-4:6. For example, Bains discloses command A causing MC0 to perform a write operation and MC1 to turn on an ODT. EX1005, 2:49-52.

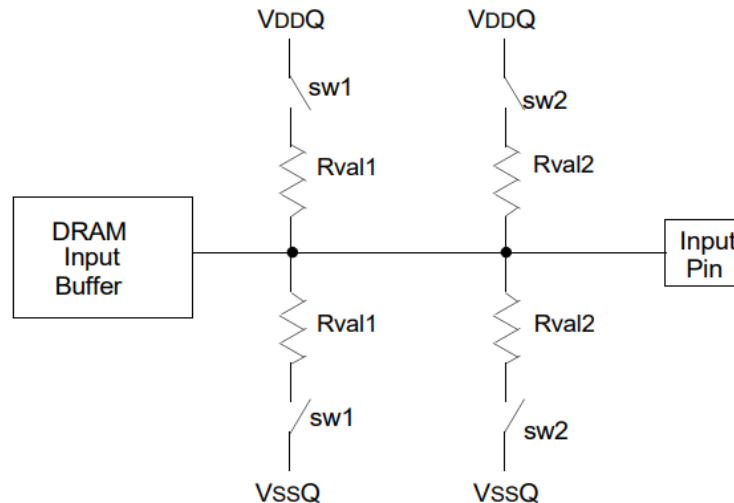
An ODT causes a termination resistance to be applied by a memory chip. EX2001, ¶ 73. Bains has arranged his command signals such that in response to a command, the memory chip either performs a write operation or applies a termination resistance. EX1005, 4:7-11; Fig. 3 (showing the same bits for write or ODT on); EX2001, ¶ 73. Consequently, Bains provides a configuration that avoids an instruction causing duplicative write operations on MC0 and MC1. EX2001, ¶ 73.

B. Summary of JESD79-2A

JESD79-2A (EX1006) is a DDR2 SDRAM specification published by JEDEC Solid State Technology Association. The relevant sections of JESD79-2A concern an on die termination (ODT) feature of DDR2 SDRAM. The ODT feature allows a

DRAM to turn on/off termination resistance via an ODT control pin. JESD79-2A includes Figure 15, which is a “Functional Representation of ODT” (shown below):

2.2.2.4 ODT (On Die Termination) (cont'd)



Switch sw1 or sw2 is enabled by ODT pin.
 Selection between sw1 or sw2 is determined by “Rtt (nominal)” in EMRS
 Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
 Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

EX1006, 27. As shown and stated in Figure 15, the switches sw1 or sw2 are enabled by an ODT pin. *Id.* The level of resistance applied when the ODT is enabled by the ODT pin, and determined by the selection between sw1 or sw2, is controlled by the Extended Mode Register Set (EMRS). *Id.* JESD79-2A contemplates that the selection between sw1 or sw2 is determined by bits A2 and A6 of the EMRS. *Id.* at 21-22, and 27.

VI. APPLICABLE LEGAL STANDARDS

Section 103 of the Patent Act provides that “[a] patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). If a single element of the claim is absent from the prior art, the claims cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“[O]bviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, Case No. IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

Further, “[o]bviousness requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination.” *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011) (citing *KSR Int’l. Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)). “Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in

the normal course of research and development to yield the claimed invention.” *Id.* If a proposed modification or enhancement of a first prior art reference through the combination of a second prior art reference would result in the first reference being rendered unsuitable for its intended purpose, then there is no suggestion or motivation to make the proposed modification or enhancement. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In addition, it is impermissible to “us[e] ‘the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the results of the claims in suit.’” *See Grain Processing Corp. v. American Maize-Prods. Co.*, 840 F.2d 902, 907 (Fed. Cir. 1988) (quoting *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1012 (Fed. Cir. 1983)).

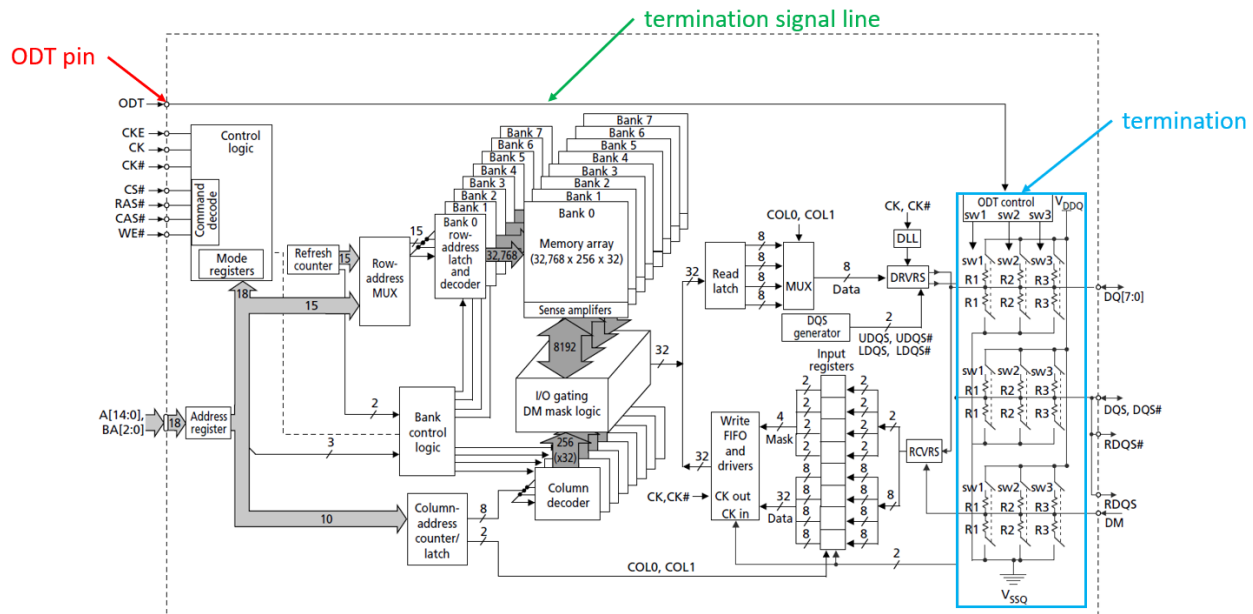
VII. THE CHALLENGED CLAIMS ARE PATENTABLE UNDER GROUND 1

A. Bains does not disclose a “control circuit” that is configured to selectively terminate “in response to the termination signal.”

Patent Owner raised this argument in its Preliminary Response. Nevertheless, the Board’s Institution Decision suggests that Patent Owner failed to effectively communicate the distinction between independent claims 1 and 5 and the asserted Grounds. To that end, Patent Owner provides the following additional detail to better explain why Bains does not disclose limitations [1.5] and [5.8].

Claims 1, 2, 5, and 6 require “a termination port to receive a termination signal.” EX1001, 8:60; 9:37. Petitioner contends that the ODT pin discussed in Bains constitutes “a termination port to receive a termination signal.” Pet. at 29-30. But neither Bains nor the Petition discuss the location of the ODT pin or (as discussed below) its relationship to any control circuit. The benefit of an ODT pin is that it allows the termination signal to be delivered directly to the termination. EX2001, ¶ 122. As contemporaneous functional block diagrams demonstrate, a POSITA would have understood that an ODT pin would deliver the termination signal directly to the termination:

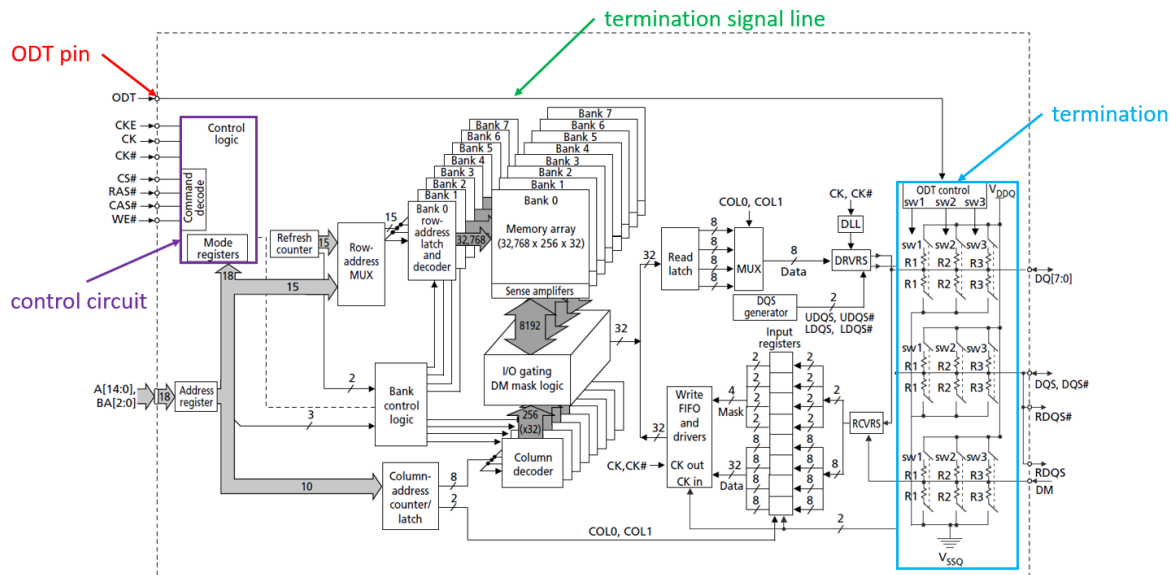
Figure 4: Functional Block Diagram – 256 Meg x 8



EX2001, Appendix B, Fig. 4 (annotations added); EX2001, ¶¶ 122-123.

While an ODT pin may constitute a termination port, claims 1, 2, 5, and 6 require more. Specifically, claims 1, 2, 5, and 6 require that the termination port receive a termination signal and that *the control circuit* be configured to selectively terminate “in response to the termination signal.” EX1001, 8:62-63; 9:40-41. As detailed above, an ODT pin in systems around the time of the invention typically bypassed the control circuit (EX2001, Appendix B, Fig. 4):

Figure 4: Functional Block Diagram – 256 Meg x 8



EX2001, Appendix B, Fig. 4 (annotations added); EX2001, ¶ 124. Because the control circuit never receives the termination signal in such systems, it cannot act *in response* to the termination signal. EX2001, ¶ 126. Merely implementing an ODT pin as disclosed in Bains, thus, fails to disclose a control circuit that is configured to selectively terminate “in response to the termination signal.”

The testimony of Petitioner's expert, Dr. Baker, confirms that he and Petitioner disregarded the challenged claims' requirement that the control circuit be configured to selectively terminate "in response to the termination signal":

Q. Dr. Baker, yes or no, does claim 1 require the control circuit in response to the termination signal be configured to selectively terminate the terminal?

A. I'm not disagreeing with your question, but you're leaving out the fact that if you take that question literally, it's saying the control circuit is providing the termination.

But I don't think it would be reasonable or accurate because -- to take that position because it's the termination circuit that has the resistors in it, it's the termination circuit that is used to terminate the signal, and it's the termination signal that -- or the control circuit that controls the termination circuit.

So I'm not arguing in part. But I mean, literally, saying the control circuit terminates the signal is -- by itself is incorrect. It does so with the termination circuit is the point I'm trying to get at.

EX2010, 34:18-35:16. During his deposition, Dr. Baker was repeatedly asked whether claim 1 requires the control circuit to selectively terminate the terminal in response to the termination signal. Despite numerous opportunities, Dr. Baker refused to admit that the literal words of claim 1 were a requirement. *See, e.g., id.* at 29:19-30:13; 30:15-31:6; 34:18-35:16; 35:18-36:5. Petitioner's and its expert's disregard of the claim language underscores the failure of their argument. Although

Bains discloses an ODT pin, there is no evidence that any disclosure from Bains alleged to satisfy the claimed “control circuit” receives the termination signal, let alone acts in response to it, as is required by the claims.

Bains does not disclose “a control circuit” that is configured to selectively terminate “in response to the termination signal.” As such, Bains does not disclose limitations [1.5] or [5.8] of the challenged claims 1, 2, 5, and 6. Accordingly, Petitioner cannot show claims 1, 2, 5, and 6 are unpatentable over Bains and Ground 1 fails with respect to these claims.

B. Bains does not disclose “receiving a control command signal for *affecting accessibility of the memory chip.*”

Patent Owner raised this argument in its Preliminary Response. Nevertheless, the Board’s Institution Decision suggests that Patent Owner failed to effectively communicate the distinction between the Challenged Claims and the asserted Grounds. To that end, Patent Owner provides the following additional explanation and detail to more clearly communicate the distinction between a general “control command signal” and a “control command signal for affecting accessibility of the memory chip.”

The Challenged Claims of the ’523 patent require a control command port that receives a control command signal for “affecting accessibility” of the memory chip. EX1001 at 8:55-56; 9:28-30; 10:24-25. The term “control command signal”

encompasses a wide variety of command signals. EX2001, ¶ 108. But not all control command signals *affect accessibility* of the memory chip. EX2001, ¶¶ 108-110. Indeed, if all control command signals affected accessibility, it would render the affect accessibility claim language superfluous. Rather, a control command signal for affecting accessibility of the memory chip is a specific type of control command signal. EX2001, ¶¶ 108-110. The '523 patent identifies several examples of such commands, including the write enable signal. EX1001, 3:45-46 (“the write enable signal for enabling write access to the memory chip.”).

A write enable signal is distinct from a write command. The write enable signal is a flag that must be true in order for a write to occur. EX2001, ¶ 114. The write enable signal is not a command to write data, but rather a condition that must be present for a write to occur. *Id.* In other words, the write enable signal affects access to the memory chip so that a write operation can occur. *Id.* Conversely, the alleged write command in Bains is an instruction that may be interpreted by the memory chip as a request write data to the memory chip. EX2001, ¶¶ 113-115. While a write command may access the memory chip, it does not *affect* such access. *Id.*

Despite this, Petitioner incorrectly argues that commands A, B, C, and D in Bains “are the same type of commands as the exemplary control command signals disclosed in the '523 Patent.” Pet. at 27. As an initial matter, commands A, B, C,

and D in Bains are not read, write, or refresh commands, but rather commands that are resolved to a function dependent on the memory chip's internal register programming. *See, e.g.*, EX1005, 2:49-55 (“For example, chip MC0 may respond to a command, for example, called command A, by performing a write operation while chip MC1 responds to command A by turning on an ODT. Stated another way, chip MC0 may interpret command A as being a write command while chip MC1 interprets command A as being a turn on ODT command”); *see also id.* at 2:55-67; 3:37-4:25. A POSITA would understand that if MC0 and MC1 respectively “interpret” command A as a write and ODT instruction, then command A is not a write or ODT instruction, but rather a command that is mapped within each respective memory chip. EX2001, ¶ 117.

But even if Bains received read, write, and refresh commands (which it does not), such commands are merely requests to perform an operation on the memory device. EX2001, ¶¶ 117-118. Read, write, and refresh commands do not affect access. *Id.* Petitioner's sole support for its “same type of commands” argument is its expert, Dr. Baker. *Id.* (citing EX1003 at ¶¶ 78-80). But Dr. Baker improperly interpreted the phrase “affecting accessibility of the memory chip”:

- Q. What is an example of a control command signal that does not affect the accessibility of the memory chip?
- A. An example would be one that comes from the memory controller that does not go to the memory chip.

...

Q. What is your position as to the meaning of affecting the accessibility of the memory chip?

A. For example, that it can read, write or do a refresh to the memory chip.

EX2010, 19:16-20:12. Dr. Baker confuses merely accessing the memory chip with *affecting accessibility* of the memory chip. Dr. Baker's analysis affords no meaning to the word "affecting." *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 809-10 (Fed. Cir. 2021) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.").

Bains does not disclose "a control command port for receiving a control command signal *for affecting accessibility* of the memory chip." As such, Bains does not disclose limitations [1.3], [5.5], or [9.1] of the Challenged Claims. Accordingly, Petitioner cannot show the Challenged Claims are unpatentable over Bains and Ground 1 fails.

C. Bains does not disclose a memory chip comprising a "control command port" and a "termination port."

Claims 1, 2, 5, and 6 require that the memory chip comprise both a "control command port" and a "termination port." EX1001, 8:55; 8:60; 9:28; 9:37. A port is generally understood to be an interface allowing for external connection. EX2001, ¶¶ 96-98. Numerous technical dictionaries explain espouse this understanding:

port 1. (I/O port) A connection point with associated control circuitry that allows I/O devices to be connected to the internal bus of a microprocessor.

EX2011 (Oxford Dictionary of Computer Science), p. 420.

Port 1. Noun. The physical interface between a device and a circuit. . . .

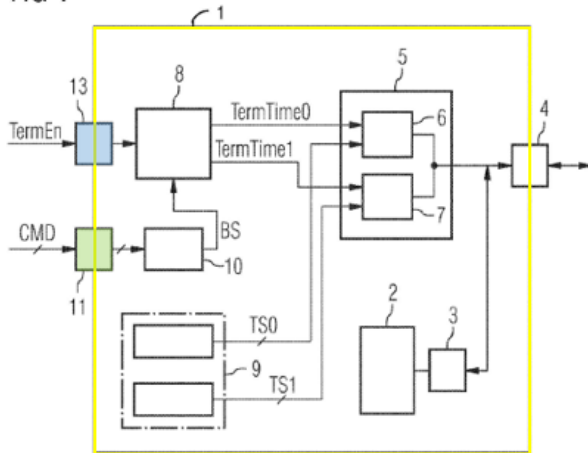
EX2012 (Newton's Telecom Dictionary, 19th Edition), p. 624.

port 2. a connection where a computer can be connected to an external device

EX2013 (Barron's Dictionary of Computer and Internet Terms), p. 380.

Thus, the claimed control command and termination ports must be external interfaces to the memory chip. This is consistent with the embodiments disclosed in the '523 patent. For example, Figures 1 and 2 expressly identify the control command and termination ports as external interfaces to the memory chip:

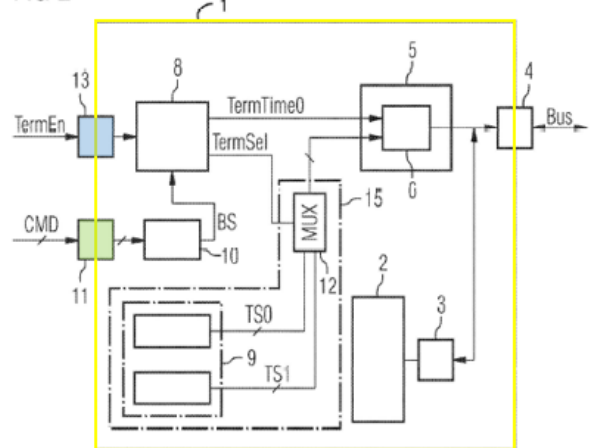
FIG 1



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT

FIG 2



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 12 - MULTIPLEXER
- 13 - EXTERNAL TERMINATION PORT
- 15 - SETTING UNIT

EX1001, Figs. 1 and 2 (annotations added). The '523 patent explains that these ports are separate from the control unit. *Id.* at 3:25-26 (“Via an external termination port 13, the control unit 8 receives a termination enable signal TermEn.”); 3:37-40 (“Via one or more external control command ports 11, the command decoder 10 receives control command signals CMD for activating, addressing and/or driving the memory chip 1.”).

Nevertheless, Petitioner incorrectly argues that *internal* components of the alleged memory chip disclosed by Bains constitute the control command and termination ports. *See, e.g.,* Pet. 25-27; 29-30. Petitioner’s annotations of Bains

demonstrate that the alleged control command port is an internal component of memory chip MC0:

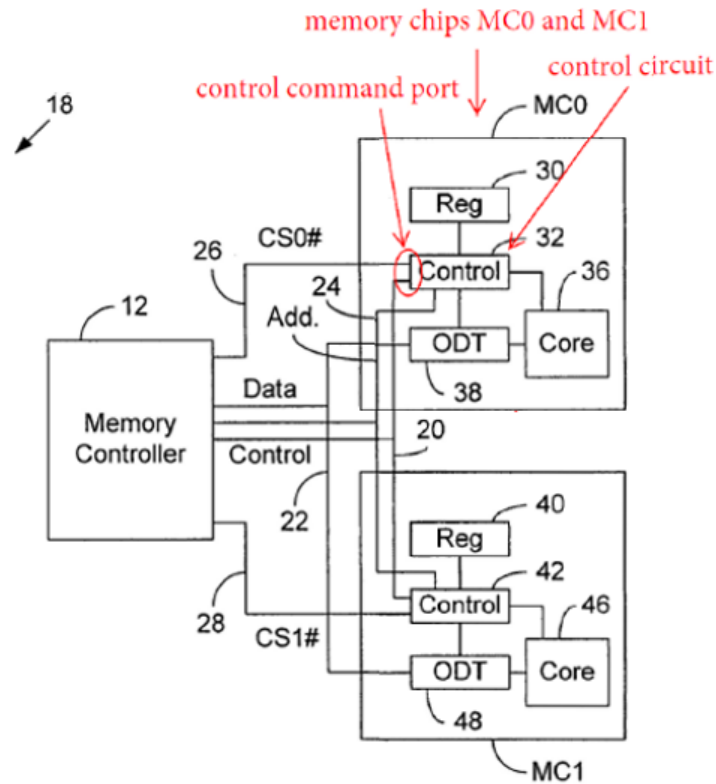


FIG. 2

Pet. at 26 (unnecessary annotations removed).

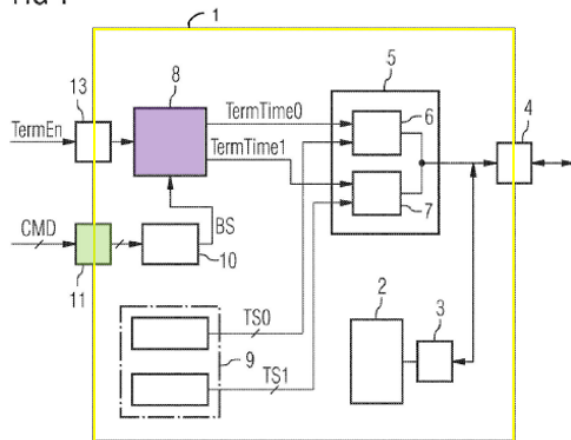
Petitioner contends that MC0 constitutes the claimed memory chip. Pet. at 22. Petitioner further contends that “a POSITA would understand that control circuit 32 includes a port connected to the control bus 20 and chip select bus 26.” Pet. at 26. Petitioner also alleges that:

To the extent Patent Owner were to argue such a control command port is not expressly disclosed, it certainly would have been obvious to a POSITA that the control circuit 32 includes such a port because the control circuit

is disclosed as receiving commands from controller 12, which must enter through a port.

Pet. at 26. But these arguments only allege that the control command port is a component of the control circuit, they do not allege that the control command port is an interface allowing for external connection of the memory chip as reasonably understood by a POSITA. Both the claims and the specification demonstrate that the control circuit and the control command port are separate components:

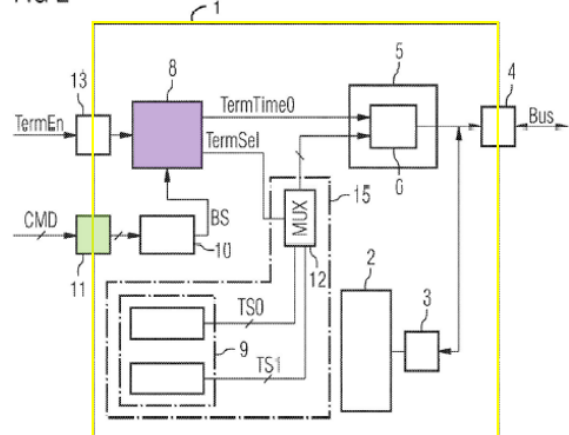
FIG 1



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 7 - SECOND SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 13 - EXTERNAL TERMINATION PORT

FIG 2



LEGEND:

- 1 - MEMORY CHIP
- 2 - MEMORY CELL ARRAY
- 3 - LOGIC CIRCUIT
- 4 - EXTERNAL TERMINAL
- 5 - TERMINATION CIRCUIT
- 6 - FIRST SETTABLE TERMINATING RESISTOR
- 8 - CONTROL UNIT
- 9 - CONFIGURATION UNIT
- 10 - COMMAND DECODER
- 11 - EXTERNAL CONTROL COMMAND PORTS
- 12 - MULTIPLEXER
- 13 - EXTERNAL TERMINATION PORT
- 15 - SETTING UNIT

EX1001, Figs. 1 and 2 (annotations added). Bains is silent as to a control command port as a component of MC0. And Petitioner does not allege that it would have been obvious to modify MC0 to include a control command port. Simply put, Petitioner has not shown that Bains discloses the claimed “control command port.”

Similarly, to the extent that Petitioner argues the ODT pin in Bains would be part of control circuit 32 (which was not alleged in the Petition), Bains would still not disclose a termination port. A POSITA would understand a termination port to require an external connection to the memory chip for receiving a termination signal. EX2001, ¶¶ 96-98. As discussed above, Bains does not disclose separate termination and command control ports for memory chip MC0. Consequently, obviousness based on Bains necessarily requires modification of the disclosed system. But Petitioner does not allege such a modification would be obvious. Similarly, Petitioner does not offer any motivation for a POSITA to make such a modification. And given the shared bus configuration set forth in Bains, a POSITA would not have been motivated to modify the architecture to include external termination and command control ports. EX2001, ¶ 106.

As detailed above, Bains does not disclose either “a control command port” or “a termination port.” As such, Bains does not disclose limitations [1.3], [1.5], [5.5], or [5.8] of the Challenged Claims. Accordingly, Petitioner has not shown, and cannot show, challenged claims 1, 2, 5, and 6 are unpatentable over Bains and Ground 1 fails with respect to these claims.

- D. Bains does not disclose a control circuit that “is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”**

Dependent claims 2 and 6 require a control circuit that is configured to set a first resistance value and a second resistance value as a function of a single received control signal:

[2.1] The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

EX1001, 9:3-8 (emphasis added); *see also id.* at 10:5-10. Bains does not disclose a received control command signal that causes the resistance value to be set to two different values. Nevertheless, Petitioner argues that Bains discloses this limitation under two distinct theories.

Petitioner first claims that “the first and second resistance values recited in claim 2 may be met by (a) the finite resistance applied as a result of a command A, A1, A2, or B, and the infinite resistance applied when the termination circuit is disabled.” Pet. at 34. There is no dispute that Bains discloses setting a first resistance value in response to command A. In response to command A, Bains sets a resistance

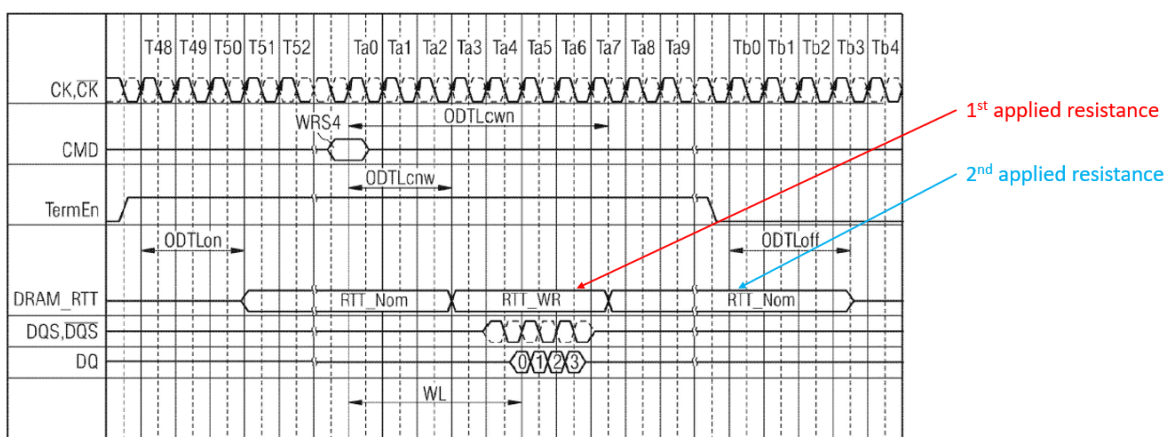
in the ODT for MC1 by closing some number of switches Sw1-D ... SwN-D and Sw1-S ... SwM-S. EX1005, 4:29-42; EX2001, ¶ 135. Bains also discloses that the ODT in MC1 is “turned off automatically (without a separate command) after a fixed delay based on a burst length of 8.” EX1005, 5:40-42. Petitioner incorrectly contends that turning off the ODT constitutes setting a resistance value.

Bains explains that “[t]he number of switches closed may determine the amount of resistance in the termination.” *Id.* at 4:40-42. In other words, the ODT may be set to different resistance values based on the number of switches that are closed. EX2001, ¶ 136. But a POSITA would not understand turning the ODT off to constitute setting a resistance value. EX2001, ¶ 136. Indeed, as discussed above, issues arising from switching ODT on/off as a function of a termination signal are the very issues the ’523 patent seeks to address. *See* Section II(A) (citing the ’523 patent, 1:37-39, 1:44-49). Absent additional action, a POSITA would understand disabling the termination to be the opposite of setting a resistance value for the termination. EX2001, ¶ 136. To hold otherwise, would disregard both the claim language and purpose of the disclosed and claimed invention.

Petitioner’s reliance on claims 4 and 8 is misplaced. The ’523 patent discloses embodiments where termination is set to a nominal value. Then, when a control command causes “switching on of the termination of the terminal”, a first resistance

value is substantially simultaneously applied “with the switching on of the termination of the terminal”. Then, when “the ending of the termination of the terminal” occurs, the nominal (i.e., second) resistance value is substantially simultaneously applied “with the ending of the termination of the terminal.” Figure 5 of the ’523 patent provides an illustration of this:

FIG 5



EX1001, Fig. 5 (annotations added); 6:32-42. Further, the ’523 patent discusses setting such a resistance value substantially simultaneous with the ending of the termination. *Id.* at 7:60-65. Any suggestion that the ’523 patent considers turning the ODT off to constitute setting a resistance value is simply incorrect.

Recognizing that disabling the termination does not constitute setting the resistance value, Petitioner alternatively claims that “the first and second resistance values recited in claim 2 may be met by ... (b) the finite resistance applied as a result of a command A1 and the finite resistance applied as a result of command A2.” Pet.

at 34. But Petitioner's alternative argument also fails because the commands A1 and A2 are separate commands. Indeed, Dr. Baker conceded that commands A1 and A2 are separate commands:

Q. As an example that Bains discloses beginning on line 42 [of column 4] that command A1 may cause one level of resistance in the ODT and that a separate command, A2, may cause another level of resistance, correct?

A. Yes.

EX2010, 39:7-11. Because A1 and A2 are two distinct commands, they do not disclose setting the resistance to two separate values as a function of a single received control command signal, as is required by the claims. Rather Bains discloses that in response to command A1, the resistance is set to a first value and that in response to a separate command A2, the resistance is set to a second value. EX1005, 4:42-44; EX2001, ¶ 138.

For the reasons discussed above, Bains does not disclose limitations [2.1] and [6.1] of the challenged claims 2 and 6. Accordingly, Petitioner has not shown, and cannot show, challenged claims 2 and 6 are unpatentable over Bains and Ground 1 fails with respect to these claims.

VIII. THE CHALLENGED CLAIMS ARE PATENTABLE UNDER GROUND 2

The deficiencies of Bains are not resolved by combining it with JESD79-2A. In Ground 2, Petitioner alleges that the combination of Bains and JESD79-2A would

render the Challenged Claims obvious. Specifically, Petitioner alleges that Bains in view of JESD79-2A discloses five limitations. The following table identifies these limitations:

Limitation	Petition
[1.5] “a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,”	Pet. pp. 57-60
[1.6] “wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.”	Pet. pp. 60-64
[5.8] “(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,”	Pet. p. 66
[9.3] “terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and”	Pet. p. 68
[9.4] “receiving a termination enable signal, the presence of which is required for the terminating to occur.”	Pet. p. 69

For all other limitations, Petitioner relies exclusively on Bains.

A. The combination of Bains and JESD79-2A does not disclose a “control circuit” that is configured to selectively terminate “in response to the termination signal.”

Petitioner incorrectly alleges that limitation [1.5] “is taught by Bains in view of JESD79-2A.” Pet. at 57. In particular, Petitioner argues that “JESD79-2A teaches a DDR2 SDRAM with an ODT pin for turning termination on and off.” *Id.* at 58. Again, Petitioner fails to appreciate the requirements of the claim language.

Limitation [1.5] requires that the control circuit be configured to selectively terminate the terminal in response to the termination signal. While JESD79-2A discloses an ODT pin for turning termination on and off, the termination signal is not delivered to the control circuit. Indeed, the statement in Figure 15 of JESD79-2A that “switch sw1 or sw2 is enabled by ODT pin,” suggests that JESD79-2A would use the same configuration as the contemporaneous functional block diagrams discussed above. EX2001, ¶¶ 122-124, 171; EX1006, 27. Consequently, there is nothing in JESD79-2A to teach or suggest that the control circuit selectively terminates the terminal *in response to* the termination signal.

Because neither Bains nor JESD79-2A disclose a control circuit that selectively terminates the terminal in response to the termination signal, their combination does not disclose all limitations of claims 1, 2, 5, and 6. As a result, Petitioner has not shown, and cannot show, that these claims are obvious in view of Bains and JESD79-2A.

B. The combination of Bains and JESD79-2A does not disclose “receiving a control command signal for *affecting accessibility* of the memory chip.”

As detailed in the table above, Petitioner does not suggest using JESD79-2A to modify Bains to disclose receiving at the control command port a control command signal for affecting accessibility of the memory chip. Consequently, for the same reasons that Ground 1 fails, Ground 2 also fails with respect to limitations [1.3], [5.5], and [9.1] and Petitioner cannot show that the Challenged Claims are invalid in view of Bains and JESD79-2A.

C. The combination of Bains and JESD79-2A does not disclose a memory chip comprising a “control command port” and a “termination port.”

As detailed in the table above, Petitioner does not suggest using JESD79-2A to modify Bains to disclose a memory chip comprising either a control command or a termination port as is required by claims 1, 2, 5, and 6. Consequently, for the same reasons that Ground 1 fails, Ground 2 also fails with respect to these claims and limitations [1.3], [1.5], [5.5], and [5.8]. Petitioner has not shown, and cannot show, that claims 1, 2, 5, or 6 are invalid in view of Bains and JESD79-2A.

- D. The combination of Bains and JESD79-2A does not disclose a control circuit that “is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”**

As detailed in the table above, Petitioner does not suggest using JESD79-2A to modify Bains to disclose the control circuit required by claims 2 and 6. Consequently, for the same reasons that Ground 1 fails, Ground 2 also fails with respect to this limitation limitations [2.1] and [6.1]. Petitioner has not shown, and cannot show, that claims 2 or 6 are invalid in view of Bains and JESD79-2A.

IX. CONCLUSION

For the reasons above, Petitioner failed to demonstrate a by a preponderance of the evidence that either Ground 1 or Ground 2 render any of the independent challenged claims obvious. Because each of the dependent claims depend from valid independent claims, Petitioner has failed to demonstrate that Grounds 1 and 2 render any of the challenged claims obvious. The Board should find in favor of Patent Owner and uphold the validity the of the challenged claims.

Dated: December 11, 2023

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 6,353 words, excluding the parts of this Patent Owner's Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Response.

Dated: December 11, 2023

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Response was served on December 11, 2023, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

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