

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

DECLARATION OF DR. R. JACOB BAKER

Case No. IPR2023-00514

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U.S. Patent and Trademark Office
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1001	U.S. Patent No. 7,145,369 (the “’369 Patent”)
1002	Prosecution history of the ’369 Patent
1003	Declaration of Dr. R. Jacob Baker
1004	Curriculum Vitae of Dr. R. Jacob Baker
1005	U.S. Patent No. 6,549,036 to Lee (“Lee”)
1006	U.S. Patent No. 6,330,194 to Thomann (“Thomann”)
1007	JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79 (“JESD79”)
1008	U.S. Patent No. 6,094,075 to Garrett (“Garrett”)
1009	Declaration of Julie Carlson and Exhibits regarding JESD79
1010	U.S. Patent No. 5,254,883 to Horowitz (“Horowitz”)
1011	U.S. Patent No. 4,665,326 to Domogalla (“Domogalla”)
1012	Excerpts of CMOS: Circuit Design, Layout, and Simulation, 2nd Edition (IEEE Press) (2005)
1013	U.S. Patent Publication No. US2003/0052369 A1 to Kajimoto (“Kajimoto”)
1014	U.S. Patent No. 6,985,037 to Veal
1015	First Amended Complaint, Polaris Innovations Limited v. Xilinx, Inc., 1:22-cv-00174-RGA, Docket No. 14 (April 28, 2022)
1016	UG585 (v1.11) Xilinx Zync-7000 All Programmable SoC Technical Reference Manual

I. Introduction

1. My name is R. Jacob Baker, Ph.D., P.E. I have prepared this Declaration in connection with Xilinx, Inc.'s Petition for *Inter Partes* Review of U.S. Patent No. 7,145,369 (the "'369 Patent") (EX1001), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the '369 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have been retained by Xilinx, Inc. ("Xilinx" or "Petitioner") as an expert in the fields of computer engineering, computer memory systems, and related technologies. I have been asked to provide my opinion regarding the state of the art of the technology described in the '369 Patent and on the patentability of the claims of this patent. I am being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in Xilinx, the '369 Patent, or the owner of the '369 Patent.

II. Background and Qualifications

4. My professional qualifications, experience, publications, and presentations, as well as a list of previous cases in which I have provided expert testimony, are outlined in my *Curriculum Vitae* (EX1004).

5. I received a Ph.D. in electrical engineering from the University of Nevada, Reno in 1993 and B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas in 1986 and 1988, respectively. I have over 35 years of industry and academic experience, and I am the named inventor on over 150 US patents, many of which are directed to memory systems and components. *See, e.g.*, U.S. Patent No. 8,516,292; U.S. Patent No. 8,395,947; U.S. Patent No. 7,877,623; U.S. Patent No. 7,421,607; U.S. Patent No. 7,237,136; U.S. Patent No. 6,704,88; U.S. Patent No. 9,697,883; U.S. Patent No. 6,026,050.

6. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). I joined UNLV in 2012 after teaching at Boise State University (BSU), where I also served as the electrical and computer engineering (ECE) department chair for three years. Prior to BSU, I worked in the department of electrical engineering at UNLV (1991-1992), and as a professor in the electrical engineering department at the University of Idaho (UI) (1993-2000).

7. While at UNLV, BLSU, and UI, I taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit, etc.), linear circuits, microelectronics, communication systems, and fiber optics. I have also advised over 100 graduate students on thesis and non-thesis research projects relating to the above topics.

8. Much of my research has focused on analog and digital integrated circuit design and fabrication. I have authored or co-authored several textbooks on the fundamentals of complementary metal oxide semiconductor (CMOS) and Dynamic Random Access Memory (DRAM) circuit design, including CMOS Circuit Design, Layout and Simulation; CMOS Mixed-Signal Circuit Design; DRAM Circuit Design: Fundamental and High-Speed Topics; and DRAM Circuit Design: A Tutorial. I have also authored or co-authored over 100 papers and presentations in the area of solid-state circuit design.

9. I am a licensed Professional Engineer with extensive industry experience in integrated circuit design and fabrication, including the design and fabrication of DRAM semiconductor integrated circuit chips. As a senior designer at Micron Technology, I designed CMOS circuits for DRAM applications and gained an understanding of the entire memory design process from fabrication to packaging. One of my projects at Micron involved the development of buffers for high-speed double-data rate (DDR) DRAM, which resulted in around 10 US patents in buffer design. I also led the development of the delay locked loop (DDL) in the 1990's to enable Micron's DRAM products to transition to the DDR memory protocol used in desktop, phone, and tablet computing systems. From 2009-2010, I served as a consultant for Sun Microsystems, where I helped design proximity connection (PxC) interfaces to DRAMs and SRAMs for transmitting

data between memory modules and memory controllers at higher speeds, and high-density 3D packaging for memory modules and controllers. I also served as a consultant for OmniVision from 2013-2015, where I designed specialty DRAM and high-speed DRAM interfaces.

10. For my contributions to memory design, I was named an IEEE Fellow in 2013. I am also a member of the honor societies Eta Kappa Nu and Tau Beta Pi. I have received a number of other honors and awards for my research contributions and teaching, including the Las Vegas (CSUN) Faculty Award (2017), Tau Beta Pi UNLV Outstanding Professor of the Year (2013-2016), UNLV ECE Department Distinguished Professor of the Year (2015), Distinguished Lecturer for the IEEE Solid-State Circuits Society (2012-2015), IEEE Circuits and Systems (CAS) Education Award (2011), Frederick Emmons Terman Award from the American Society of Engineering Education (2007), BSU President's Research and Scholarship Award (2005), IEEE Power Electronics Society's Best Paper Award (2000), and UI Department of Electrical Engineering Outstanding Researcher Award (1998-1999), among others.

11. I have significant experience providing expert witness services in the areas of electrical and computer engineering, and in the course of this work and my own research and patenting activities, I have gained experience studying and

analyzing patents and patent claims from the perspective of a person skilled in the art.

III. Documents and Materials Considered

12. In forming my opinions, in addition to my knowledge, education, training, and experience, I have considered the materials cited in this Declaration and the documents and things that I have obtained, or that have been provided to me, as listed in the Table of Exhibits.

13. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me. My consideration of materials in relation to this Declaration is ongoing and I will continue to review any new materials as it is provided. This Declaration represents only those opinions I have formed to date and I may supplement or amend this Declaration if additional information that affects my opinions becomes available.

IV. Relevant Legal Principles

14. I am not an attorney, and I offer no opinions on the law. Counsel has informed me of legal standards that apply to the issue of patent validity. I have applied these standards in arriving at my conclusions.

15. I understand that in an *inter partes* review the petitioner has the burden of proving a proposition of unpatentability by a preponderance of the evidence. I understand this standard is different from the standard that applies in a district court, where I understand a challenger bears the burden of proving invalidity by clear and convincing evidence.

16. I understand that a patent claim is invalid based on anticipation if a single prior art reference discloses all of the features of that claim in a way that enables one of ordinary skill in the art to make and use the invention. Each of the claim features may be expressly or inherently present in the prior art reference. I understand that if the prior art necessarily functions in accordance with, or includes a claim's feature, then that prior art inherently discloses that feature. I have relied on this understanding in expressing the opinions set forth below.

17. I understand that a prior art reference describes the claimed invention if it either expressly or inherently describes each and every feature set forth in the claim; *i.e.*, in determining whether a single item of prior art anticipates a patent claim, one should take into consideration not only what is expressly disclosed in that item, but also what is inherently present as a natural result of the practice of the system or method disclosed in that item.

18. I understand that to establish inherency, the evidence must make clear that the missing descriptive matter is necessarily present in the item of prior art and

that it would be so recognized by persons of ordinary skill in the art. I also understand that prior art use of the claimed patented invention that was accidental, unrecognized, or unappreciated at the time of filing can still be an invalidating anticipation.

19. I understand that although multiple prior art references may not be combined to show anticipation, additional references may be used to interpret the allegedly anticipating reference and shed light on what it would have meant to those skilled in the art at the time of the invention. These additional references must make it clear that the missing descriptive matter in the patent claim is necessarily present in the allegedly anticipating reference, and that it would be so recognized by persons of ordinary skill in the art.

20. I understand that a patent may not be valid even though the invention is not identically disclosed or described in the prior art if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art in the relevant subject matter at the time the invention was made.

21. I understand that obviousness must be tested as of the time the invention was made. I understand that the test for obviousness is what the combined teachings of the prior art references would have suggested, disclosed, or taught to one of ordinary skill in the art.

22. To determine if a claim is obvious, the following factors should be considered: (1) the level of ordinary skill in the art at the time the invention was made; (2) the scope and content of the prior art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations, including evidence of commercial success, long-felt but unsolved need, unsuccessful attempts by others, copying of the claimed invention, unexpected and superior results, acceptance and praise by others, independent invention by others, and the like.

23. For example, I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim because a court can take account of the inferences and/or creative steps that a person of ordinary skill in the art would employ.

24. I understand that the following rationales may be used to determine whether a piece of prior art can be combined with other prior art or with other information within the knowledge of one of ordinary skill in the art:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;

- Predictable use or combination of prior art elements according to their established functions;
- Use of known techniques to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- “Obvious to try” - choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; or
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. I understand that when a work is available in one field of endeavor, design incentives and/or other market forces, for example, can prompt variations of it, either in the same field or a different one. Moreover, if a person of ordinary skill can implement a predictable variation, I understand this likely bars its patentability.

26. I understand that another factor to be considered is common sense. For example, I understand that common sense teaches that familiar items may have obvious uses beyond their primary purposes, and, in many cases, a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.

27. I understand that the Supreme Court articulated additional guidance for obviousness in its *KSR* decision. My understanding is that the Supreme Court said that technical people of ordinary skill look for guidance in other solutions to problems of a similar nature, and that the obviousness inquiry must track reality, and not legal fictions. I have relied on these understandings in expressing the opinions set forth below.

28. I understand that a new use of an old product or material cannot be claimed as a new product; the apparatus or system itself is old and cannot be patented. I further understand that, in general, merely discovering and claiming a new benefit to an old process cannot render the process newly patentable.

29. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a person of ordinary skill in the art (“POSITA”). I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my

analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms unless I specify otherwise.

30. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have been asked to use a priority date of July 12, 2003.

V. Person of Ordinary Skill in the Art

31. In order to determine the characteristics of a POSITA of the '369 Patent, I have used July 12, 2003 as the relevant time frame. My understanding is that this is the alleged earliest foreign priority date of the application that resulted in the '369 Patent. For purposes of this Declaration, any reference to a priority date of the '369 Patent is intended to refer to this July 12, 2003 date.

32. In determining the characteristics of a person of ordinary skill in the art for the '369 Patent, I have considered the state of the art of integrated circuit inputs/outputs at that time, the types of problems encountered with operating output drivers for integrated circuits across variations, such as those related to semiconductor process, temperature, and voltage, and the solutions that then existed. I have also considered the then-existing technology for integrated circuit inputs/outputs and memory systems, including the sophistication of the technology involved, and the education and experience of those working in the field at that time. I have also considered my personal knowledge and experience in the field at

that time, including those I worked and interacted with regarding integrated circuit inputs/outputs and memory systems. I have also considered the knowledge, education, and experience of those in academia and industry at that time that were working, innovating, or performing research in the field of integrated circuit inputs/outputs and memory systems.

33. It is my opinion that a POSITA for the '369 Patent at the time of this filing date would have had a Bachelor's degree in Electrical Engineering, Computer Engineering, or an equivalent field, and two or three years of academic or industry experience in the field of semiconductor memory design, or a person with equivalent education, work, or other experience in this field.

34. Given this background, a POSITA would have been familiar with JEDEC industry standards and knowledgeable about the design and operation of standardized DRAM memory systems, including memory devices, modules, controllers, and interfaces. In addition, a POSITA would have been familiar with output driver designs (e.g., driver circuits, driver strength adjustment circuits, and corresponding control logic), including digital and analog circuitry.

35. Based on my background and qualifications, I am currently and was as of the priority date of the '369 Patent at least a POSITA in the subject matter of the '369 Patent.

VI. '369 Patent

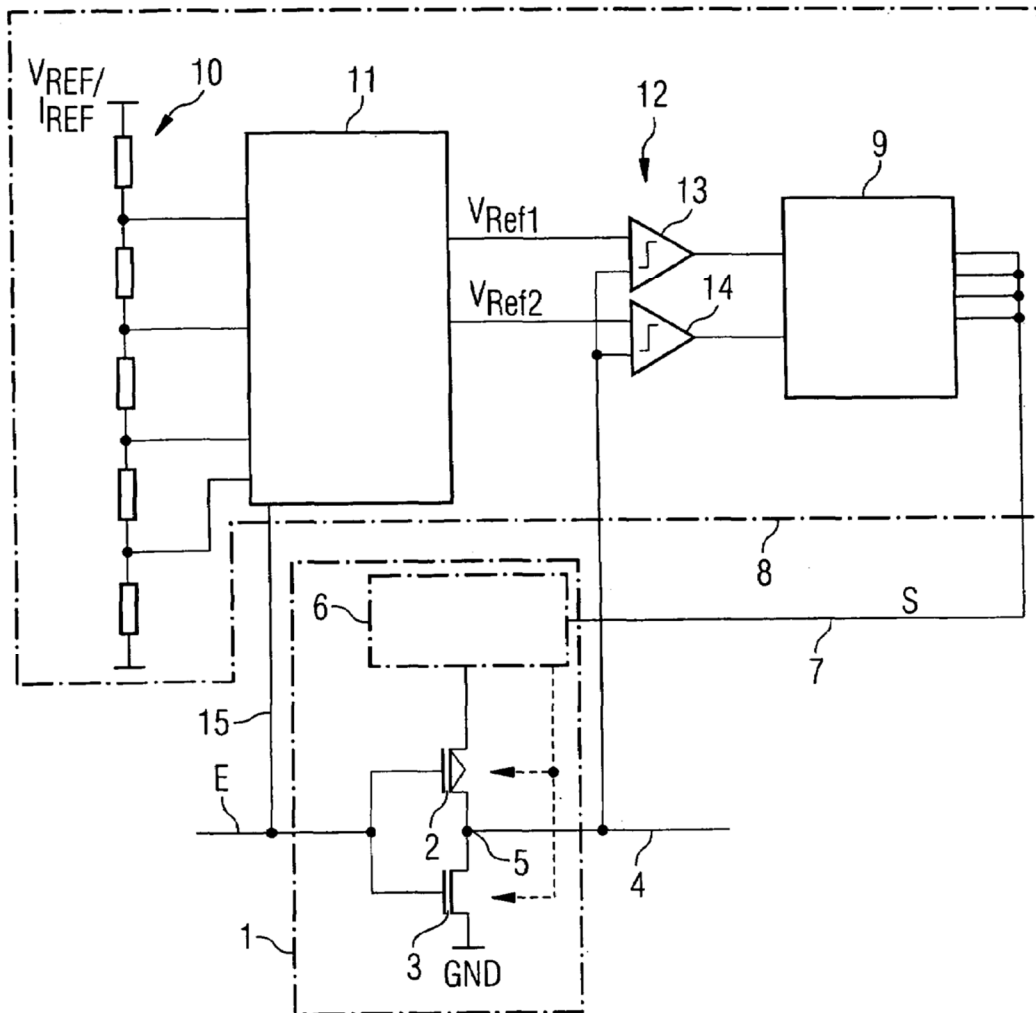
A. Overview

36. U.S. Patent No. 7,145,369 to Dickman is entitled “Output Driver for an Integrated Circuit and Method for Driving an Output Driver” and was issued on December 5, 2006.

37. The '369 Patent is directed to an output driver for an integrated circuit and a method for driving an output driver. '369 Patent (EX1001), at Title, Abstract, 1:1-2. The '369 Patent purports that it solves a problem in the prior art by reducing the power consumption of the integrated circuit. *Id.* at 1:66-2:2. This purported advancement is achieved by setting the drive strength of a driver circuit using feedback control that sets a potential or current intensity at the output of the driver circuit to a value with a desired power range of a specification-prescribed potential range or specification-prescribed current intensity range. *Id.* at 2:13-23, 7:1-3.

38. As shown in Figure 1 of the '369 Patent, reproduced below, the driver circuit 1 includes a pair of transistors (2, 3) to drive an input signal E to the output 5 and output line 4. '369 Patent (EX1001), at 4:4-11. The output line 4 is fed back to a control unit 8 to compare the potential value or voltage on the output line to reference potential(s) (at 13 and/or 14). *Id.* at 4:32-40. Based on the comparison, the control unit 8 generates a control signal S, which is provided to a setting circuit 6 that sets the driver strength based on control signal S. *Id.* at 4:18-31.

FIG 1



39. Also shown in Figure 1 of the '369 Patent is a voltage divider 10 that provides reference voltages to multiplexer 11 that correspond to a desired potential window for the output of the driver. '369 Patent (EX1001), at 5:13-24. Based on the input E , the multiplexer 11 selects two reference voltages, V_{Ref1} and V_{Ref2} , for comparison to the potential value on the output line, and an evaluation unit 9 counts based on the digital result of the comparison. *Id.* at 4:66-5:15, 5:25-30.

40. Figures 2a and 2b of the '369 Patent, reproduced below, show minimum (I_{min}), maximum (I_{max}), and nominal (nominal minimum, $I_{nom,min}$, and nominal maximum, $I_{nom,max}$) current-voltage characteristic curves for the pull-down and pull-up paths of the driver. '369 Patent (EX1001), at 3:64-67. The prescribed range, provided in a current-voltage window, spans between the minimum and maximum curves. *Id.* at 6:15-18, 6:24-26. To lower the power consumption of the driver, a lower range is defined within the permissible range. *Id.* at 6:27-37; *see, e.g., id.* at Figs. 2a, 2b. For example, a tolerance magnitude is added to the minimum current intensity curve (I_{min}), as shown by the nominal current intensity curve ($I_{nom,min}$) in each of the figures. *Id.* at 6:38-42.

FIG 2A

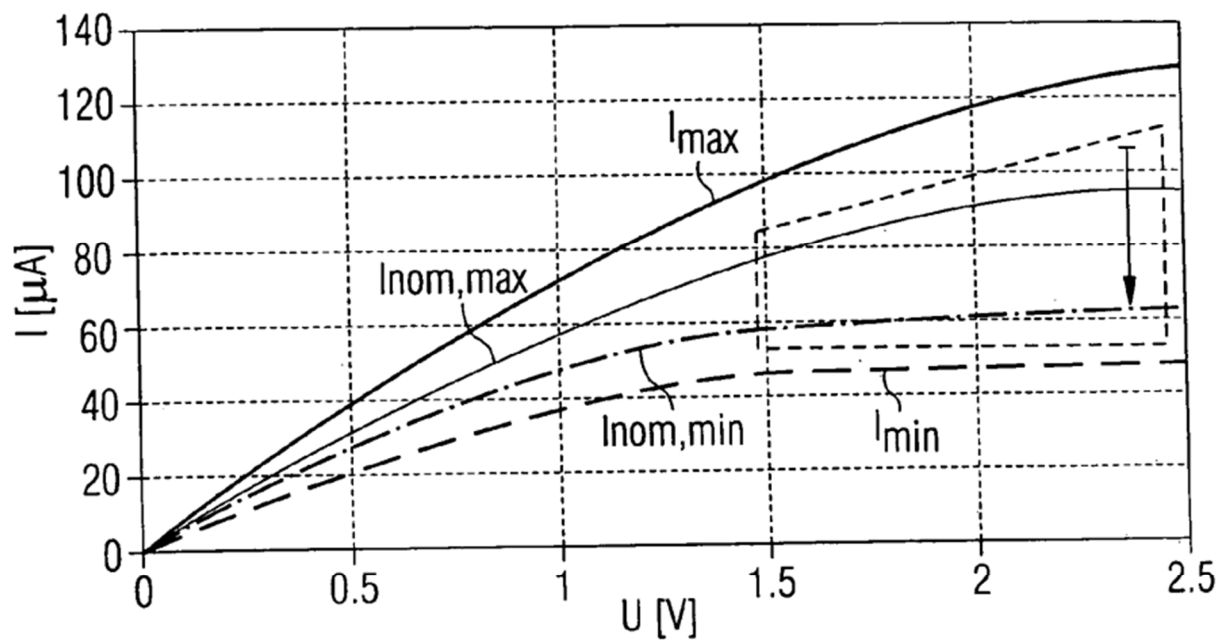
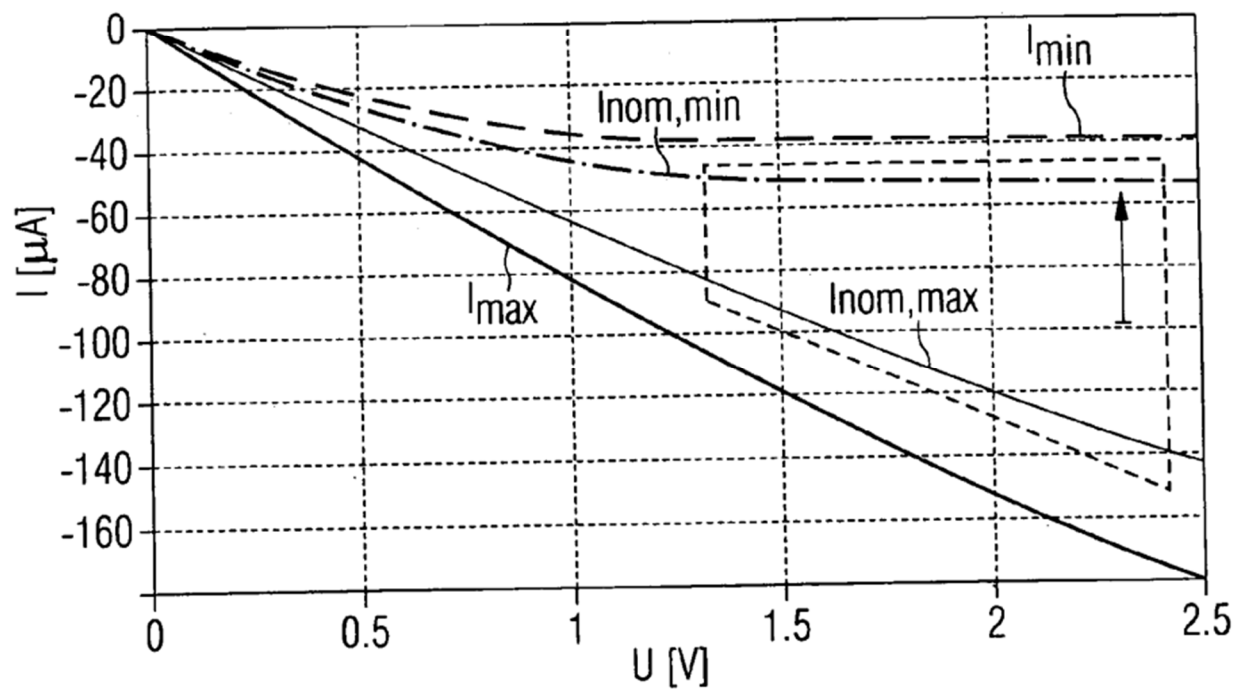


FIG 2B



B. Background / Applicant Admitted Prior Art

41. I have reviewed the '369 Patent, including the section of the Specification titled "BACKGROUND OF THE INVENTION." I understand this section of the '369 Patent to disclose technologies that were already known in the art as of the priority date of the '369 Patent. In particular, I note that many of the elements that are recited in the '369 Patent claims, or portions of those elements, are described in this section. For example:

Claim	Claim Language	Background
[1.P]	"An output driver for an integrated circuit" <i>See also</i> , claim [14.P], [18.P]	"Integrated circuits usually have output drivers for driving signals which have been generated in circuits of the integrated circuit on external lines connected to the integrated circuit." '369 Patent (EX1001), at 1:21-24.
[1.1]	"a driver circuit for driving an input signal of the output driver onto an output line" <i>See also</i> , claim [14.P], [18.1]	"In this case, the specification respectively specifies an upper and lower current-voltage characteristic curve for the activated pull-up path of the driver circuit and for the pull-down path of the driver circuit, which characteristic curve in each case defines a current intensity range within which the current intensity through the relevant path and thus through the output line must be." '369 Patent (EX1001), at 1:28-34.
[1.2]	"an output line current" and "an output line potential" <i>See also</i> , claim [14.1], [18.2]	"To define the driver behavior of the output drivers, a specification is provided which, depending on the output driver, provides an upper and a lower <u>current</u> value or an upper and

Claim	Claim Language	Background
		lower <u>potential</u> value depending on the <u>signal state (high level or low level)</u> of <u>the output signal</u> to be driven. In this case, the specification respectively specifies an upper and lower current-voltage characteristic curve for the activated pull-up path of the driver circuit and for the pull-down path of the driver circuit, which characteristic curve in each case defines a current intensity range within which <u>the current intensity through the relevant path and thus through the output line must be</u>. Depending on whether a high or low level is intended to be driven by the output driver, the specification prescribes different upper and lower current-voltage characteristic curves for the pull-up path and the pull-down path.” ’369 Patent (EX1001), at 1:24-38 (emphasis added). “Usually, the specifications for integrated circuits, in particular for SDRAM and DDR memory circuits, provide a relatively large <u>current intensity</u> range or <u>potential</u> range <u>for the output drivers</u>, so that it is simpler to achieve the specification-conforming <u>current intensity values</u> or <u>potential values</u> for process cut-off values, temperatures and voltages (PVT). The specification-conforming <u>current intensity</u> ranges or <u>voltage</u> ranges of the pull-up paths and pull-down paths may signify great differences with regard to the power consumption depending on the position of the <u>actual</u>

Claim	Claim Language	Background
		<u>potential value or current value within the specification, since more power is required in an upper <u>current intensity</u> range and/or in an <u>upper potential</u> range than if the output signal is in a lower range of the permissible predetermined <u>potential</u> window and/or <u>current intensity</u> window.”</u> ’369 Patent (EX1001), at 1:39-52 (emphasis added).
[1.2]	at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range <i>see also</i>, claim [14.2], [14.3], [18.2]	“To define the driver behavior of the output drivers, a <u>specification</u> is provided which, depending on the output driver, <u>provides an upper and a lower current value or an upper and lower potential value depending on the signal state (high level or low level) of the output signal to be driven</u>. In this case, the <u>specification respectively specifies an upper and lower current-voltage characteristic curve for the activated pull-up path of the driver circuit and for the pull-down path of the driver circuit</u>, which characteristic curve in each case <u>defines a current intensity range within which the current intensity through the relevant path and thus through the output line must be</u>. Depending on whether a high or low level is intended to be driven by the output driver, the <u>specification prescribes different upper and lower current-voltage characteristic curves for the pull-up path and the pull-down path</u>.” ’369 Patent (EX1001), at 1:24-38 (emphasis added).

Claim	Claim Language	Background
		“Usually, the specifications for integrated circuits, in particular for SDRAM and DDR memory circuits, provide <u>a relatively large current intensity range or potential range for the output drivers</u>, so that it is simpler to achieve the <u>specification-conforming current intensity values or potential values</u> for process cut-off values, temperatures and voltages (PVT). The <u>specification-conforming current intensity ranges or voltage ranges of the pull-up paths and pull-down paths</u> may signify great differences with regard to the power consumption depending on the <u>position of the actual potential value or current value within the specification</u>, since more power is required in an upper current intensity range and/or in an upper potential range <u>than if the output signal is in a lower range of the permissible predetermined potential window and/or current intensity window.</u>” ’369 Patent (EX1001), at 1:39-52 (emphasis added).

42. These same applicant admitted prior art (AAPA) concepts are also found in the prior art references that I discuss in the grounds of unpatentability below.

C. Prosecution History

43. On July 9, 2004, the ’369 Patent was filed as Application No. 10/887,949 (the “’949 Application”) entitled “Output Driver for an Integrated

Circuit and Method for Driving an Output Driver.” File History of ’369 Patent (EX1002), at 3. The ’949 Application claims priority to German Patent Application 103 31 607, filed July 12, 2003, and listed 20 claims. *Id.*

44. During prosecution of the ’949 Application, the United States PTO issued two non-final office actions. In the first action, the examiner rejected several claims of the ’949 Application as indefinite. Namely, the examiner rejected claims 1 and 14 as indefinite because it was unclear what element was the “measuring circuit,” and claim 6 as indefinite because the “control unit” included the “comparator unit” rather than the “output driver.” File History of ’369 Patent (EX1002), at 148. In addition, the examiner indicated that claims 8-13, 17, and 19-20 had allowable subject matter but rejected the remaining claims as anticipated by one of three references. *Id.* at 149-52.

45. In response, the applicant pointed to Paragraphs [0007], [0022]–[0024], and [0029] of the specification of the ’949 Application for alleged support of the “measuring circuit.” File History of ’369 Patent (EX1002), at 167-70 (response), and at 4, 5, 8-10, 11 (cited paragraphs of the ’949 Application). The applicant also amended claim 6 of the ’949 Application to recite that “the control unit” comprises “a comparator unit.” *Id.* at 164, 167. Further, the applicant argued that the cited references did not disclose a “driver circuit,” “driver,” or “control signal for setting a driver strength.” *Id.* 167-70.

46. In the second action, the examiner rejected claims 1-6 and 14-17 as anticipated by US Patent Application No. 2003/0052369 or DE10237536 to Kajimoto. File History of '369 Patent (EX1002), at 175-76. In response, the applicant amended claims 1 and 14 of the '949 Application to require feedback control "based on a measured value provided by a measuring circuit" and argued that Kajimoto discloses feed-forward control and not feedback control. *Id.* at 183, 187; *see also* Kajimoto (EX1013). In the reasons for allowance, the examiner pointed to the requirement for feedback control for claims 1 and 14, and the control and driver means for claim 18. File History of '369 Patent (EX1002), at 198.

D. Priority Date

47. As discussed above, the '949 Application claims priority to a German patent application filed on July 12, 2003. '369 Patent (EX1001) at 1. For the purposes of this Declaration, I have been told to assume that the earliest priority date of the '369 Patent is July 12, 2003.

VII. Technology Background

48. The technology of the '369 Patent relates to output driver control and ranges of current, potential/voltage, and power for operation of the output driver. An output driver typically includes driver circuitry that provides input data or information, such as a logical high or low value of a signal, to another circuit or component. The driver circuitry includes a pull-up path and a pull-down path, each

with one or more transistors to enable or disable the path in response to an input signal of the driver circuit. Output driver circuits often include some form of adjustability because they must operate in different configurations and environments. For example, the transistor(s) in each path can be designed to include multiple transistors arranged in parallel that are enabled or disabled with an adjustment signal to adjust the number of transistors driving an input to the output.

49. As of the filing date of the '369 Patent, it was well known, for example, that output drivers are subject to variations, such as those in semiconductor process, temperature, and voltage, that there were solutions for actively adjusting to such variations. For example, Lee discloses that “an active calibration scheme [to] reduce the timing uncertainty further by adjusting out the effects of process variance, voltage variation or temperature variation on output buffer drivers.” Lee (EX1005), at 1:34-38; *see also* Lee (EX1005), at 2:30-32 (“The present invention provides a simple output driver calibration circuit and calibration method which reduces timing uncertainty in high speed signaling systems”). As another example, Thomann discloses, like Lee, that “an active calibration scheme [to] reduce the timing uncertainty further by adjusting out the effects of process variance, voltage variation or temperature variation on output buffer drivers.” Thomann (EX1006), at 1:33-37; *see also* Thomann (EX1006), at 2:28-30 (“The present invention provides a simple output driver calibration circuit and calibration method which reduces timing

uncertainty in high speed signaling systems”). As a further example, it was well known that specified minimum and maximum current-voltage characteristic curves included recommended, narrower typical curves for operation, such as those disclosed by the JEDEC standard for Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM). *See* JEDEC DDR SDRAM Specification (JESD79) (EX1007), at 59-60, 64.

VIII. Claim Construction

50. I have interpreted the terms of the '369 Patent according to their plain meaning unless otherwise specified. In interpreting the terms, I have carefully considered and applied the claim construction standards referred to in Section IV above.

51. I understand that a claim term may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof. I also understand that the use of the word “means” in a claim term creates a presumption that the term is expressed as such a means or step. I further understand that such a presumption, whether or not the term is expressed as a means or step, can be rebutted. For terms that do not use the word “means,” I understand that the presumption may be rebutted by evidence indicating whether another word is used as a substitute for the word “means” and whether the term connotes sufficiently definite structure to a POSITA.

52. I understand that once it is determined that a claim term is expressed as such a means of step, the claim term is construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

53. Below, I identify four terms that recite the word “means.” In my opinion, these terms do not sufficiently connote structure to a POSITA but rather serve to claim a specified function without reciting any structure. Other claims recite several similar terms, such as “control unit,” “comparator unit,” and “evaluation unit,” but those terms do not recite the word “means” and thus I understand they are presumed not to be expressed as a means or step. If Patent Owner rebuts this presumption, it is my opinion that the corresponding structure for the claimed function is the same as the similar terms that recite the word “means,” as I discuss below.

A. “driver means”

54. Claim limitation [18.1] recites “a driver means for driving an input signal of the output driver onto an output line.” ’369 Patent (EX1001), at 8:32-33. The claimed function, as recited in claim 18, is “for driving an input signal of the output driver onto an output line.” *See id.* The specification of the ’369 Patent (’369 Specification) discloses that the corresponding structure for performing the claimed function is transistors 2 and 3 of driver circuit 3, as shown in Figure 1 of the ’369 Patent, reproduced below.

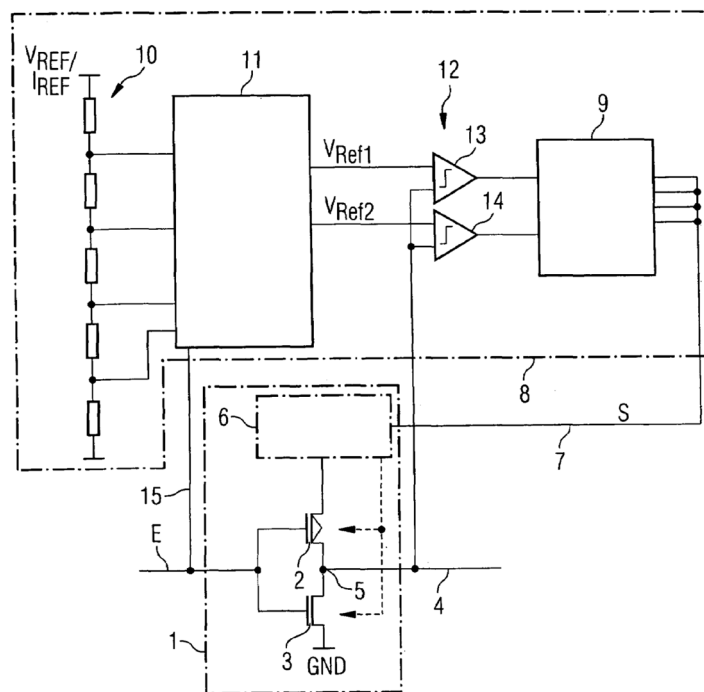
[illegible]

26

B. “comparator means”

55. Claim limitation [18.3] recites a comparator means for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value. '369 Patent (EX1001), at 8:40-43. The claimed function, as recited in claim 18, is “for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value.” *See id.* The '369 Specification discloses that the corresponding structure for performing the claimed function is one or more of comparators 13 or 14 of comparator unit 12 in Figure 1 of the '369 Patent that compare the output line current and/or potential to one or more reference current and/or potential values.

FIG 1

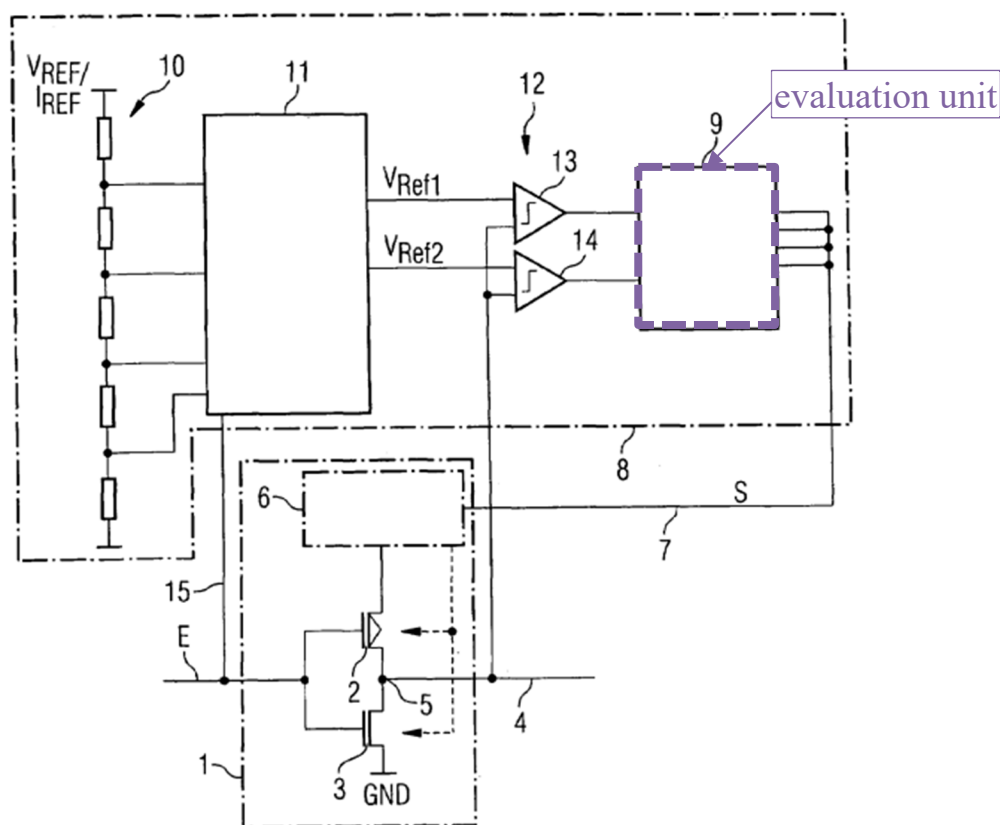


'369 Patent (EX1001), at FIG. 1, 3:19-25, 4:41-65, 5:25-6:8. Although Figure 1 shows multiple comparators (13, 14) and multiple reference values (VRef1, VRef2), the claimed function in claim 18 only requires comparing at least one output line current or potential to at least one reference current or potential value. It does not require a comparison of multiple reference values, as do other claims of the '369 Patent recite. *See* '369 Patent (EX1001), at 7:37-57 (claims 9 to 13, which recite multiple reference potentials or voltages), 8:21-30, 8:47-62 (claims 17 and 19-20, which recite multiple reference potentials or voltages). Accordingly, it is my opinion that one of the two illustrated comparators in Figure 1 can correspond to the claimed function in claim 18.

C. “evaluation means”

56. Claim limitation [18.4] recites an evaluation means for changing the control signal based upon a comparison result from the comparator means. '369 Patent (EX1001), at 8:44-46. The claimed function, as recited in claim 18, is “for changing the control signal based upon a comparison result from the comparator means.” Figure 1 and claim 7 of the '369 Patent disclose an evaluation unit (9), as annotated below, that generally provides for the claimed function.

FIG 1



Id. at FIG. 1. However, as shown in Figure 1, the evaluation unit is illustrated as a black-box. *Id.* In my opinion, this black-box by itself does not connote structure to a POSITA. The '369 Specification also describes that the black-box includes “a counter” that provides a changing control signal based on the received comparison result. *Id.* at 5:25-30, 5:42-47, 7:35-36. Thus, the '369 Specification discloses that a counter is the corresponding structure for the function claimed in claim 18.

D. “control means”

57. Claim limitation [18.2] recites a control means for providing a control signal for setting a driver strength of the driver means. '369 Patent (EX1001), at

8:34-46. The claimed function, as recited in claim 18, is “for providing a control signal for setting a driver strength of the driver means.” Claim 18 also recites that the “*control means*” is comprised of the “*comparator means*” and “*evaluation means*,” which I have discussed above in Sections VIII.B and VIII.C. Accordingly, the corresponding structure for the “control means” is the combined structure of these two means: 1) one or more comparators that compare the output line current/potential to one or more reference current/potential values; and 2) a counter that provides a changing control signal based on the comparison result.

IX. Summary of Opinions

58. In my opinion, U.S. Patent No. to Lee (Lee), either alone or in combination with U.S. Patent No. 6,330,194 to Thomann (“Thomann”), JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79 (“JESD79”), and/or U.S. Patent No. 6,094,075 to Garrett (“Garrett”), renders obvious claims 1-4, 14-16, and 18 of the ’369 Patent, as I discuss in the section below.

59. A table of the grounds is provided below for ease of reference:

	Grounds	Claims
1	Obvious over Lee	1, 2, 5-7
2	Obvious over Lee and Thomann	1, 2, 5-7
3	Obvious over Lee and JESD79	1-7, 14-16
4	Obvious over Lee, JESD79 and Garrett	1-8, 14-16, 18

A. Overview of Lee (EX1005)

60. U.S. Patent No. 6,549,036 (“Lee”) was filed as U.S. Application No. 09/583,884 on May 31, 2000 and issued and published on April 15, 2003. *See* Lee (EX1005), at 1.

61. Lee discloses an output buffer driver with drive strength calibration for driving a bus that, for example, is connected to a memory controller. Lee (EX1005), at 1, 2:11-19, 7:57-67, FIG. 5 (below).

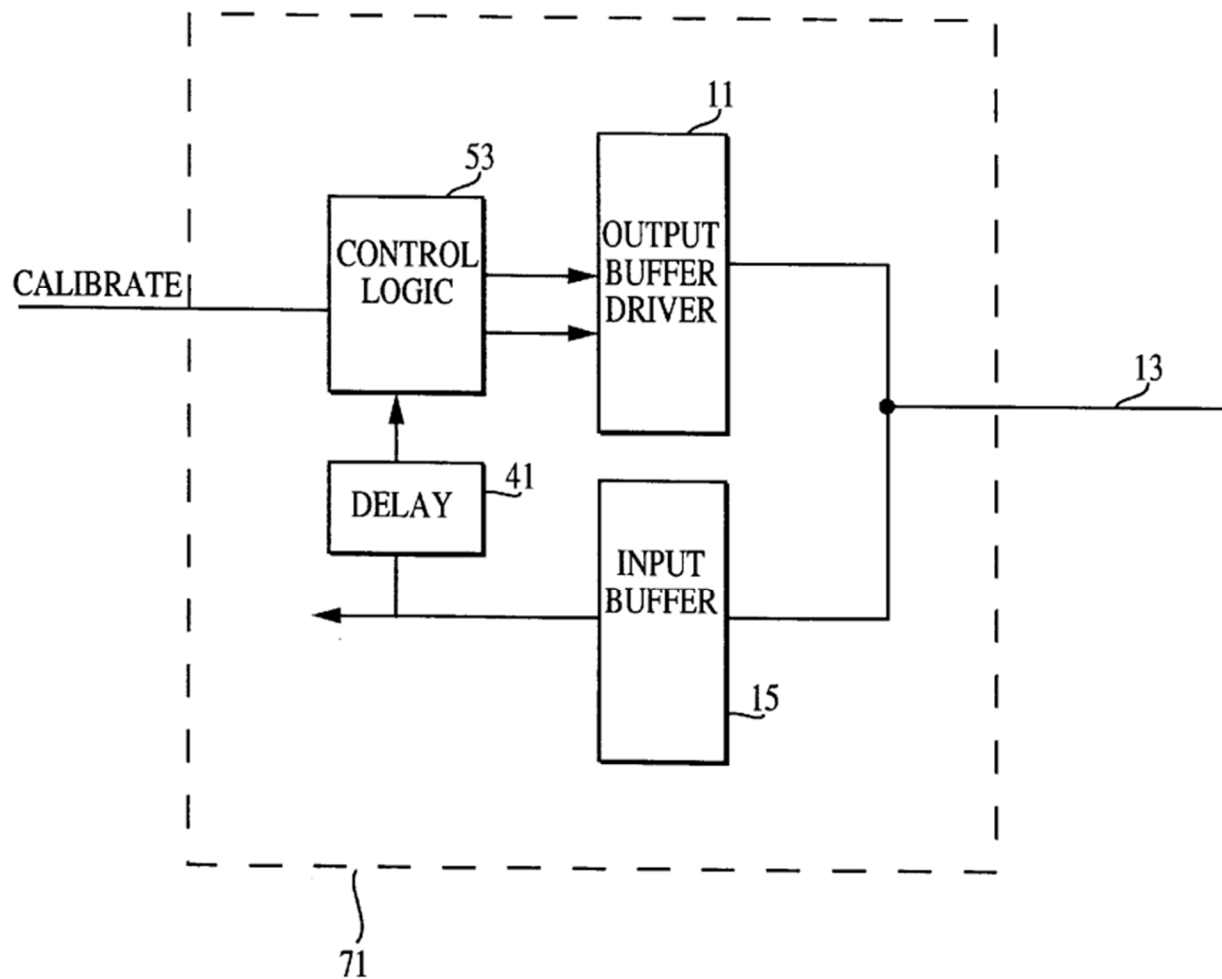


FIG. 5

62. The output voltage of the driver 11 is fed back to the input buffer 15 where it is compared to a reference voltage V_{REF} , as shown in Figures 1 and 2 below. As shown in Figures 2 and 5, the result of the comparison is used to adjust the drive strength control such that the output voltage swings across a range between a high voltage V_{OH} and low voltage V_{OL} that are symmetric about a mid-voltage V_{REF} . *Id.* at 3:7-24, 4:35-61, FIGS. 1, 2 (below).

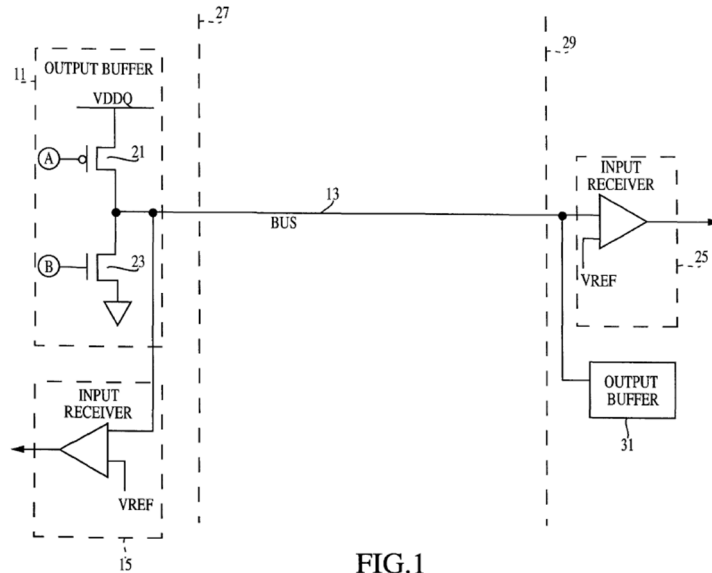


FIG. 1

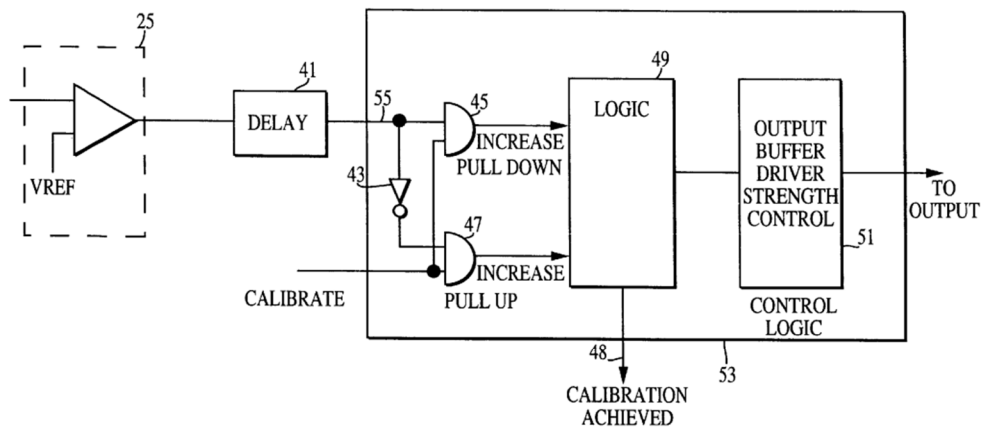


FIG. 2

63. Specifically, Lee discloses adjusting the drive strength by increasing or decreasing the strengths of the pull-up or pull-down paths of the driver, such as by adjusting the effective width of the transistors, enabling or disabling the number

of transistors arranged in parallel, or adjusting the gate fingers of the transistors. *Id.* at 4:9-5:18.

B. Overview of Thomann (EX1006)

64. U.S. Patent No. 6,330,194 (“Thomann”) was filed on June 26, 2000 and issued and published on December 11, 2001. *See* Thomann (EX1006), at 1.

65. Similar to Lee, Thomann discloses an output buffer circuit with drive strength calibration for driving a memory device. *Id.* at 1. The drive signal output on data path 18 is compared to a reference signal VREF, and the result of the comparison is used to adjust the drive strength control. *Id.* at 4:43-57, FIGS. 1 and 2 (below).

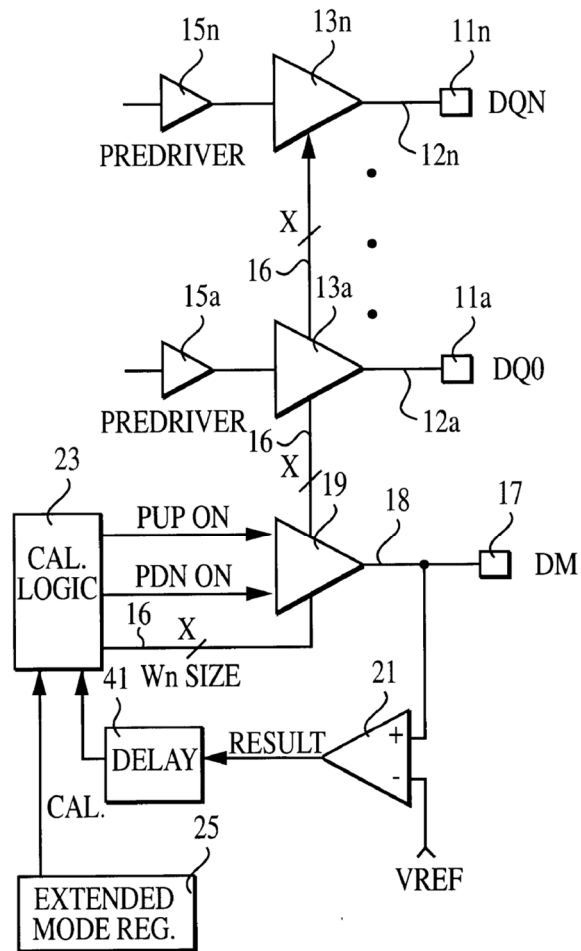


FIG. 1

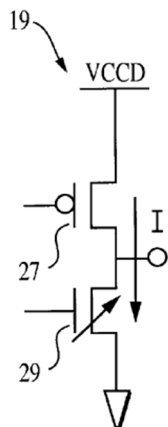


FIG. 2

66. Before calibration, Thomann discloses that the driver may provide too much drive strength, despite the output voltage VOL DRIVER falling within the prescribed minimum and maximum potentials, VOL MIN. and VOL MAX. *Id.* at 5:37-44, FIG. 3 (below).

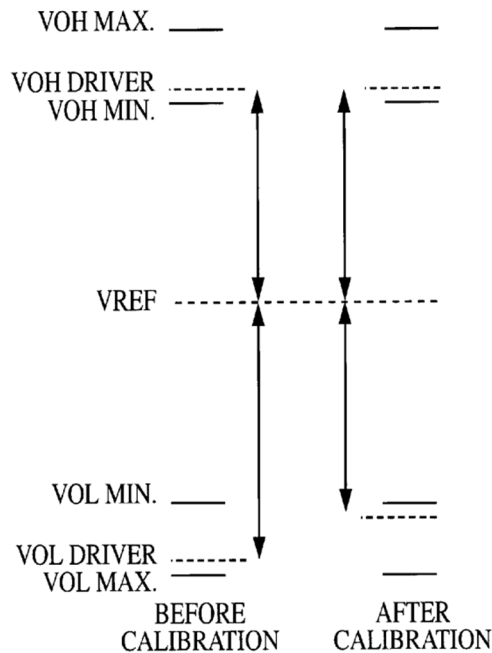


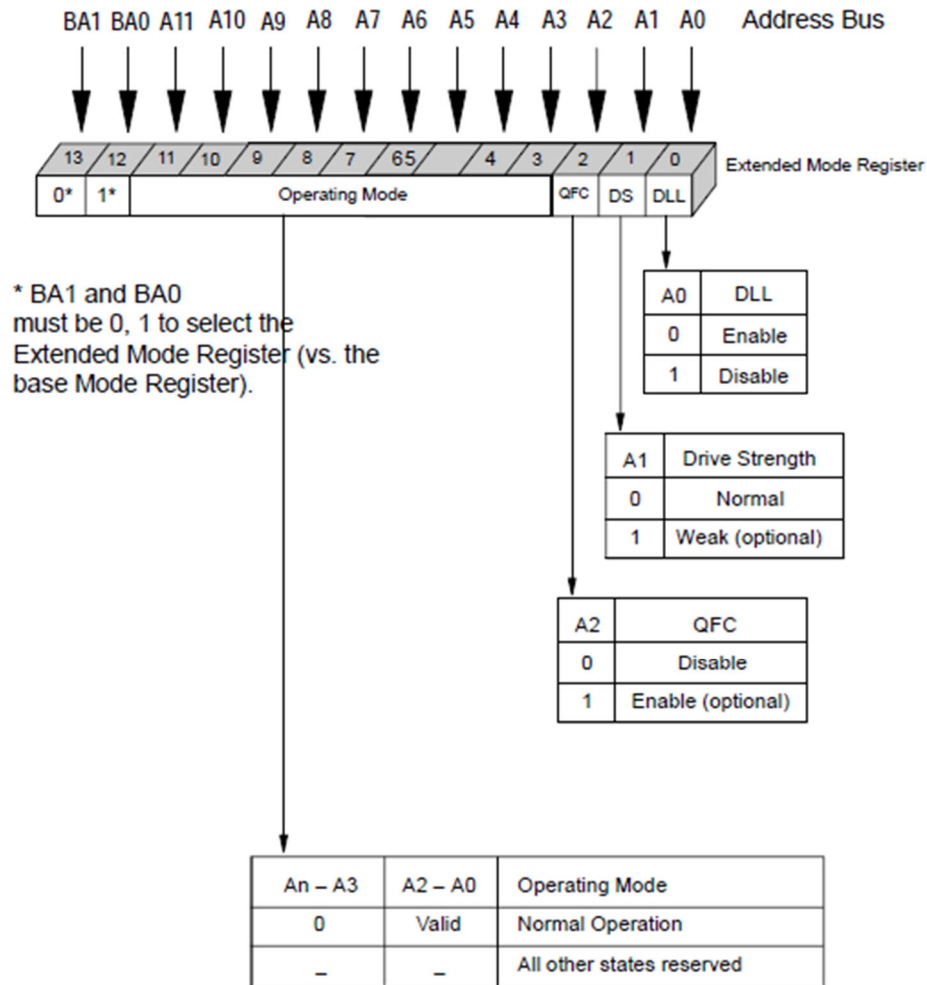
FIG. 3

67. After calibration, the driver may achieve a balanced drive strength, centered around a reference voltage, VREF. *Id.* at 6:18-31, FIG. 3. As shown in Figure 3 of Thomann above, the range or swing of the driver output voltage is lowered after calibration so that the VOL DRIVER value is closer to the VOH DRIVER and VOL MIN values. *Id.*

C. Overview of JESD79 (EX1007)

68. JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, Release 1 (“JESD79”) is a well-known standards specification for computer memory. In my view, a POSITA would have been familiar with common JEDEC memory standards, like JESD79, which were widely used in the industry. In addition to being familiar with JEDEC’s common memory standards, a POSITA would have been familiar with how to access those memory standards to design a memory device in accordance with the standards. Based on my experience in memory development, a POSITA would have visited JEDEC’s website to access and download memory standards, such as JESD79. Also, in my experience, JEDEC’s standards, like JESD79, were available to download by the public, for free or purchase, on or around the date found on the cover page of a particular standard.

69. As shown below, JESD79 discloses a specification for memory that enables a user to enter a desired drive strength setting as either “normal” or “weak.”



EX1007 (JESD79), at 16¹.

70. The “normal” or full-strength setting is defined by current-voltage characteristic curves that define the maximum values (Maximum), minimum values (Minimum), and nominal values (Typical).

¹ The citations to printed publications in this Declaration follow the stamped page numbers of the exhibit unless I state otherwise.

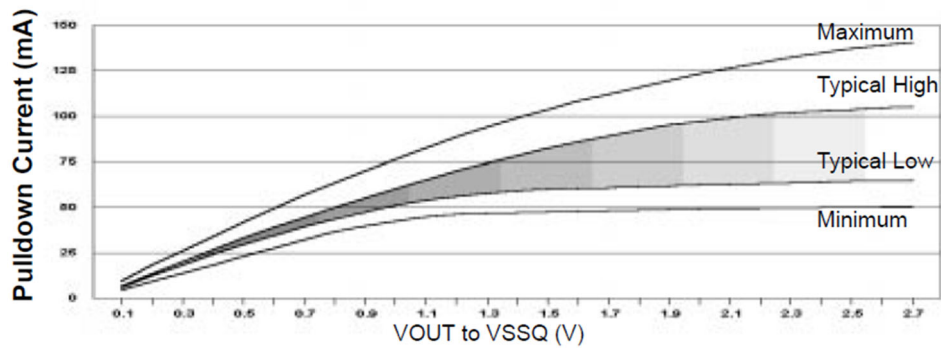
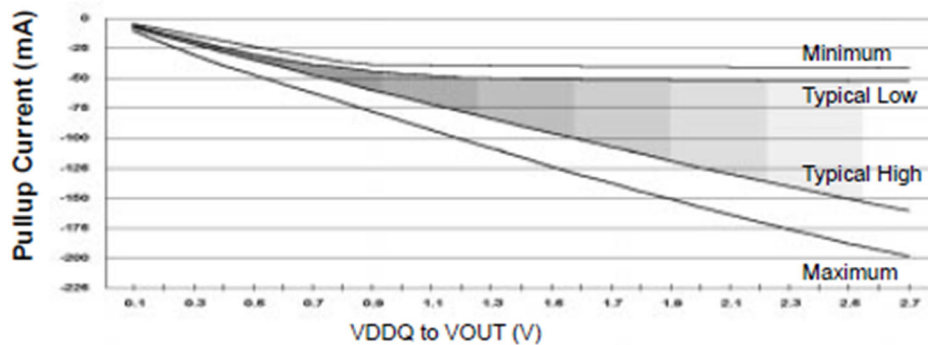


Figure a: Pulldown Characteristics



EX1007 (JESD79), at 59. Although JESD79 refers to the curves as voltage versus current (V-I) curves, a POSITA would have understood that the same curves, with the current on the vertical axis and the voltage on the horizontal axis, would also have been referred to as current versus voltage (I-V) curves. Similar to the normal strength setting, the “weak” strength setting is defined by current-voltage characteristic curves, but for lighter loads and/or point-to-point environments.

EX1007 (JESD79), at 16. For example, a POSITA would have understood that a lighter load requires less current from a driver circuit to swing the output voltage from a low state to a high state. Similarly, a POSITA would have understood that point-to-point environments for memory systems typically have a lighter load

because there are fewer memory devices connected to the output line, such as a data line of a data bus. *See id.* JESD79 also explains that the magnitude of the pullup and pulldown currents should match within a ten-percent tolerance. EX1007 (JESD79), at 59.

D. Overview of Garrett (EX1008)

71. U.S. Patent No. 6,094,075 (“Garrett”) was filed on August 27, 1998 and issued and published on July 25, 2000. *See* EX1008 (Garrett), at 1.

72. Garrett discloses an output driver with an adjustable drive current. *Id.* at 3:1-19. As shown in Figure 2 of Garrett, reproduced below, the output line, such as the line at terminals or nodes BDA and BDB, is input to an analog voltage divider (AVD) 104 that outputs an output voltage level (V_{out}) representing a weighted averaged of its input.

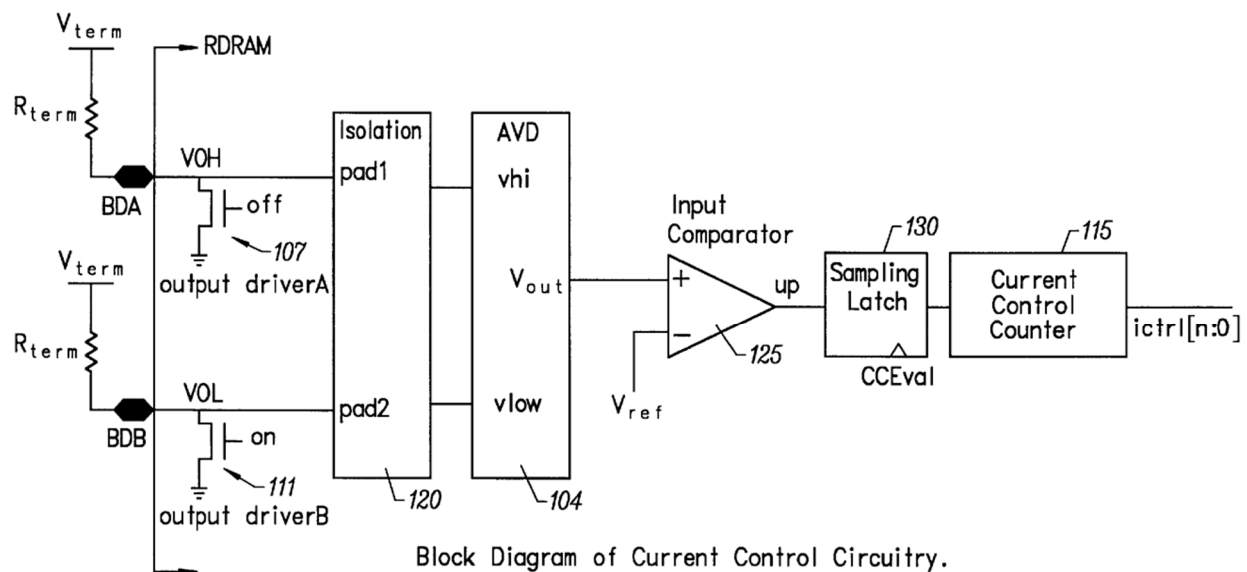


FIG. 2

73. EX1008 (Garrett), at FIGS. 2-4, 3:8-13, 5:26-6:24; *see also id.* at FIG. 11, 10:6-41. Further, an input comparator 125 compares V_{out} to a reference voltage (V_{ref}), a sampling latch 130 samples the output of the input comparator 125, and the latch 130 outputs a signal that is input to a counter 115, which outputs a control signal (e.g., $ictrl[n:0]$) to adjust the width of the output transistors. *Id.* Garrett explains that the counter may be implemented as an up-down counter or a saturating binary search counter. *Id.* at 3:38-40, 7:7-23, 8:67-9:9, 9:18-24.

X. Claims 1-8, 14-16, 18 are Unpatentable

A. Claims 1, 2, and 5-7 are Obvious Over Lee

74. In my opinion, Lee renders obvious claims 1, 2, 5-7 of the '369 Patent.

1. Claim 1

a. “An output driver for an integrated circuit, comprising:” [1.P]

75. I understand that the preamble of claim 1 is not necessarily limiting. Nevertheless, to the extent the preamble is limiting, Lee teaches the preamble of claim 1. As shown below in Figure 1 of Lee, Lee discloses a system with an output location (27), annotated in purple in the figure below, that includes an output buffer driver circuit (“*an output driver*”).

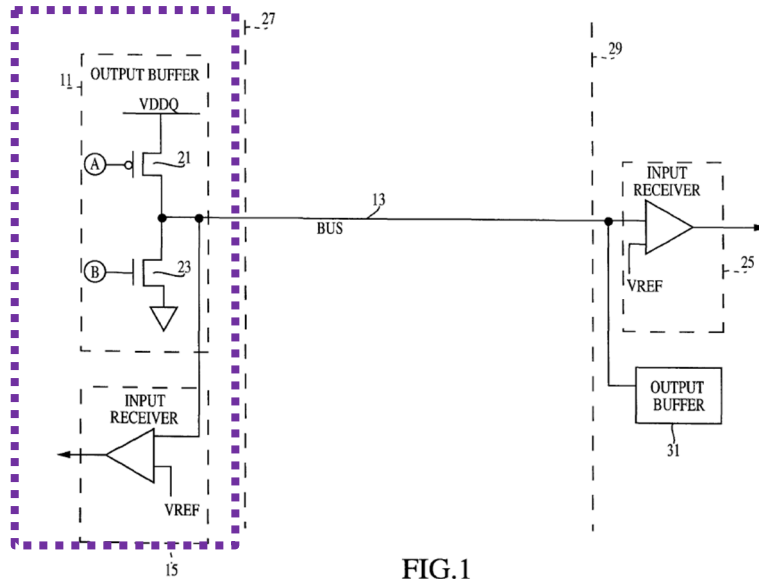


FIG. 1

Lee (EX1005), at FIG. 1, 3:13-32. Lee also illustrates an input/output buffer (71) that “includes output buffer driver 11 and an input receiver 15” (*id.* at 5:45-47), as annotated in purple in Figure 5 below.

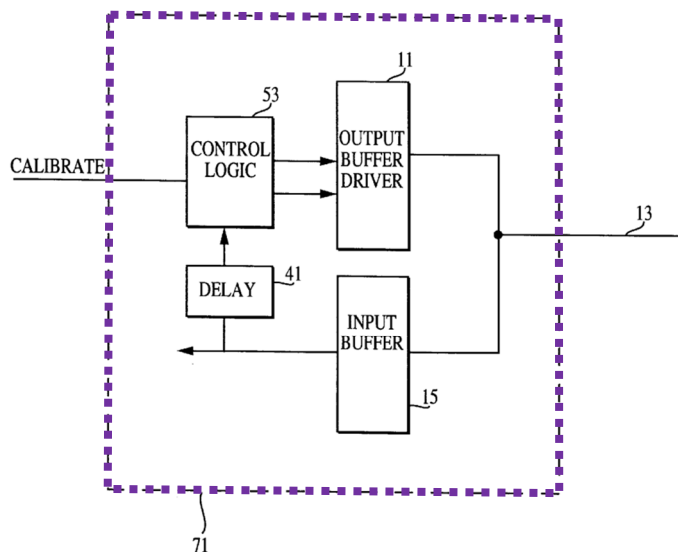


FIG. 5

Id. at FIG. 5. Lee also illustrates output drivers in Figures 4 and 6, as shown below.

Id. at FIGS. 4, 6.

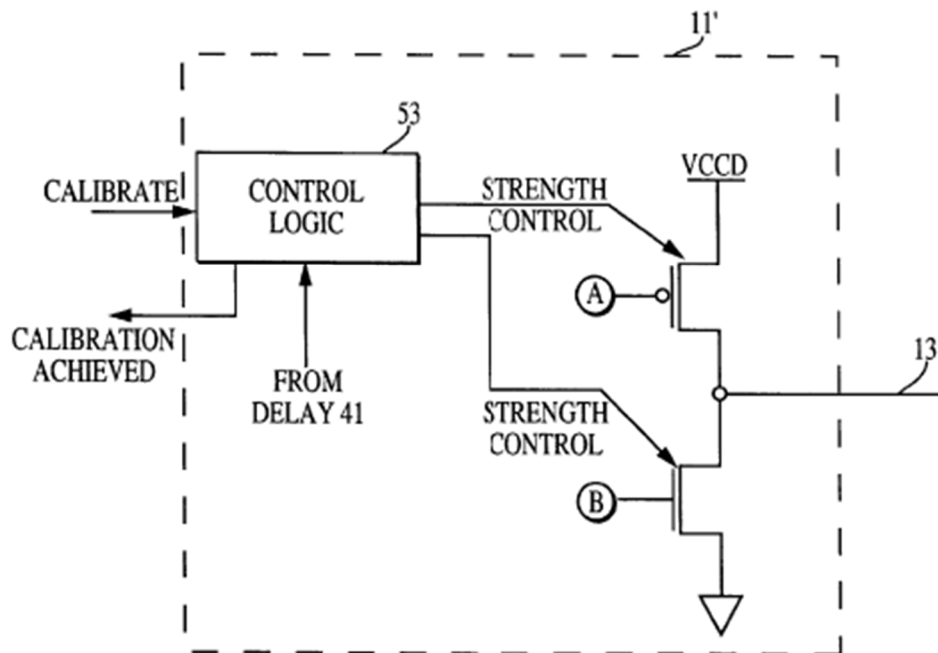


FIG. 4

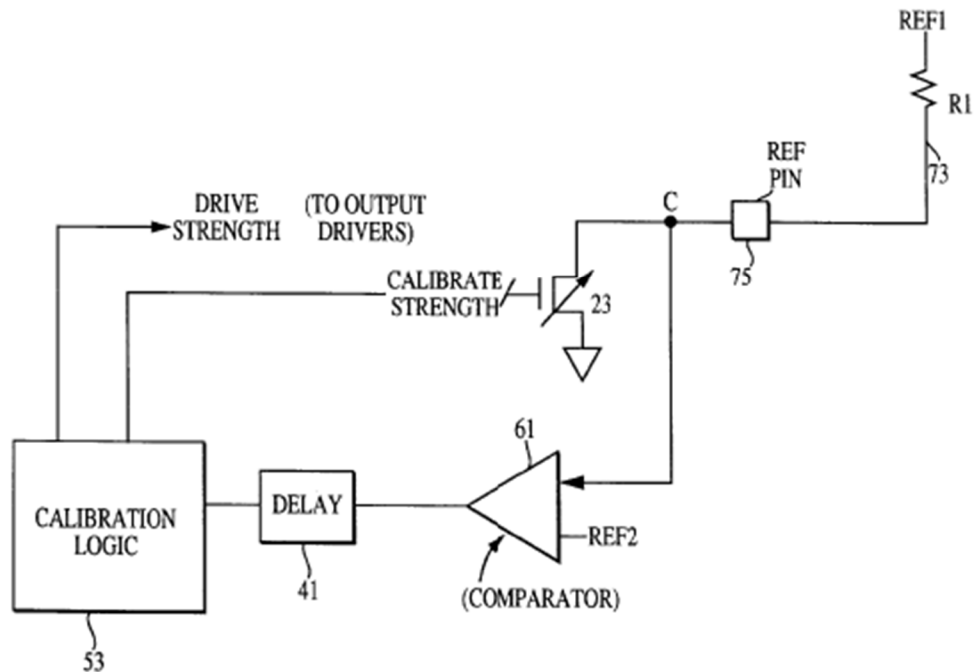


FIG. 6

76. Lee also discloses that the output driver is “*for an integrated circuit.*”

Lee explains that his “invention will find utility in any device which uses output buffer devices to apply signals to a transmission path, such as a bus.” *Id.* at 7:33-35. For example, the invention may be used in a processor based system, as shown below in Figure 7.

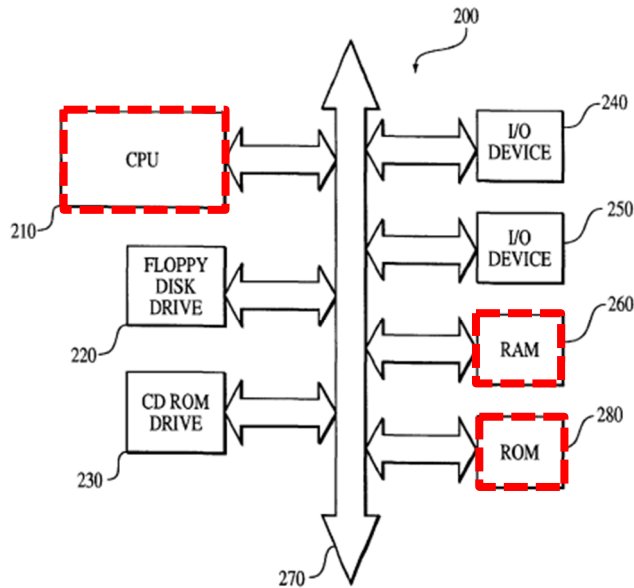


FIG.7

Id. at FIG. 7. As shown by the annotations, the processor-based system includes memory circuits, such as RAM 260 and ROM 280, and processor circuits, such as CPU 210). *Id.*; *see also id.* at 1:39-44 (disclosing memory systems). Lee explains that these circuits are “preferably constructed as integrated circuits which include a calibration circuit for calibrating the characteristics of output buffer drivers.” *Id.* at 7:57-67.

b. “a driver circuit for driving an input signal of the output driver onto an output line” [1.1]

77. Lee also teaches claim limitation [1.1]. As shown in Figures 1 and 4 of Lee below, Lee discloses “a driver circuit” that includes an output buffer driver (11 or 11”) with two transistors (21 and 23) to drive an input signal, which is

received at nodes A and B, onto a bus (13) (“for driving an input signal of the output driver onto an output line”).

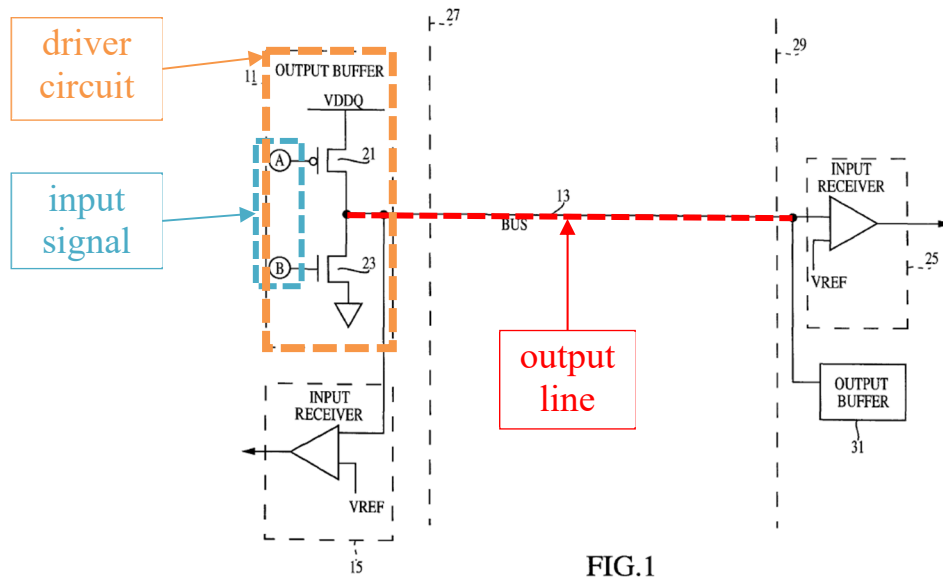


FIG. 1

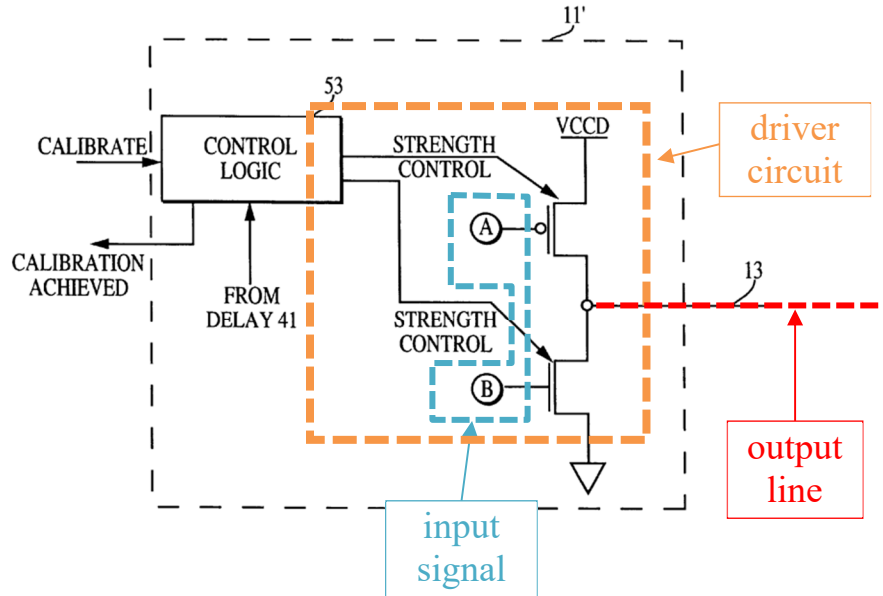


FIG. 4

Lee (EX1005), at FIGS. 1, 4. A POSITA would have recognized that Lee’s driver is a complementary circuit, such as a complementary CMOS circuit with P-channel

(PFET) and N-channel (NFET) transistors. As Lee explains, its transistor 21 is referred to as a pull-up transistor that can be implemented as a P-channel device. *Id.* at 3:33-37. Lee also explains that transistor 23 is referred to as a pull-down transistor that can be implemented as a N-channel device. *Id.* at 3:38-41.

78. During normal operation, the output buffer driver (11 or 11') switches the bus voltage to a logic high or low level in responsive to the input signal, which is individually and collectively the signal received at nodes A and B. *Id.* at 3:34-53. Indeed, it is well known that an input signal is often provided at multiple nodes of an output buffer driver. Lee explains that nodes A and B "are essentially transitioned simultaneously for the fastest switching transition." *Id.* at 3:50-51. Thus, a POSITA would have understood that nodes A and B operate together to create the fastest switching transition between a high and low voltage at the output. If "the gate of transistor [21] at node A is asserted [high] while the gate of transistor 23 at node B is asserted low," the bus voltage switches "to a high voltage or logic '1' level." *Id.* at 3:47-50. Similarly, if the gate of transistor at "node A is asserted low while [the gate of transistor 23 at] node B is asserted high for a logic '0' state." *Id.* at 3:52-53. During calibration, Lee explains that both transistors (21 and 23) of the output buffer driver (*see* 11 or 11' in FIGS. 1, 4 above) are turned on at the same time by the gate of transistor 21 at node A being asserted low while the gate of transistor 23 at node B is asserted high. *Id.* at 3:53-56. A POSITA

would have therefore understood that the signal received at nodes A and B to be “an input signal.”

79. In addition to disclosing an input signal received at two nodes (nodes A and B in FIGS. 1 and 4 of Lee, shown above), Lee discloses to a POSITA that each node is configured to receive “an input signal” to be driven to the output by output buffer driver (11 or 11’). As I explained above, Lee discloses an input signal for a driver, such as one implemented as a complementary CMOS circuit, in which the logic level at node A is the opposite or inverse of the logic level at node B. *See, e.g., id.* at 3:47-53. The output state is logic low (‘0’) when node A is asserted low and node B is asserted high, and the output state is logic high (‘1’) when node A is asserted high and node B is asserted low.

80. Further, it would have been obvious for a POSITA to implement Lee’s output buffer driver (11 or 11’) in a system such that nodes A and B are coupled to one “input signal” for normal operation to enable either the pull-up transistor (23) or the pull-down transistor (21) and control logic for calibration to enable both the pull-up and pull-down transistors. Lee explains that during “calibration of the output buffer driver 11, node A is asserted low while node B is asserted high, so both transistors 21 and 23 are turned on at the same time.” *Id.* at 3:53-56. Output buffer drivers were commonly implemented using a pull-up transistor, such as a PFET that turns on when the voltage at its gate is asserted low,

and a pull-down transistor, such as an NFET that turns on when the voltage at its gate is asserted high. For example, Lee discloses that the output buffer can include control logic and can be implemented with a P-channel pull-up transistor and an N-channel pull-down transistor.

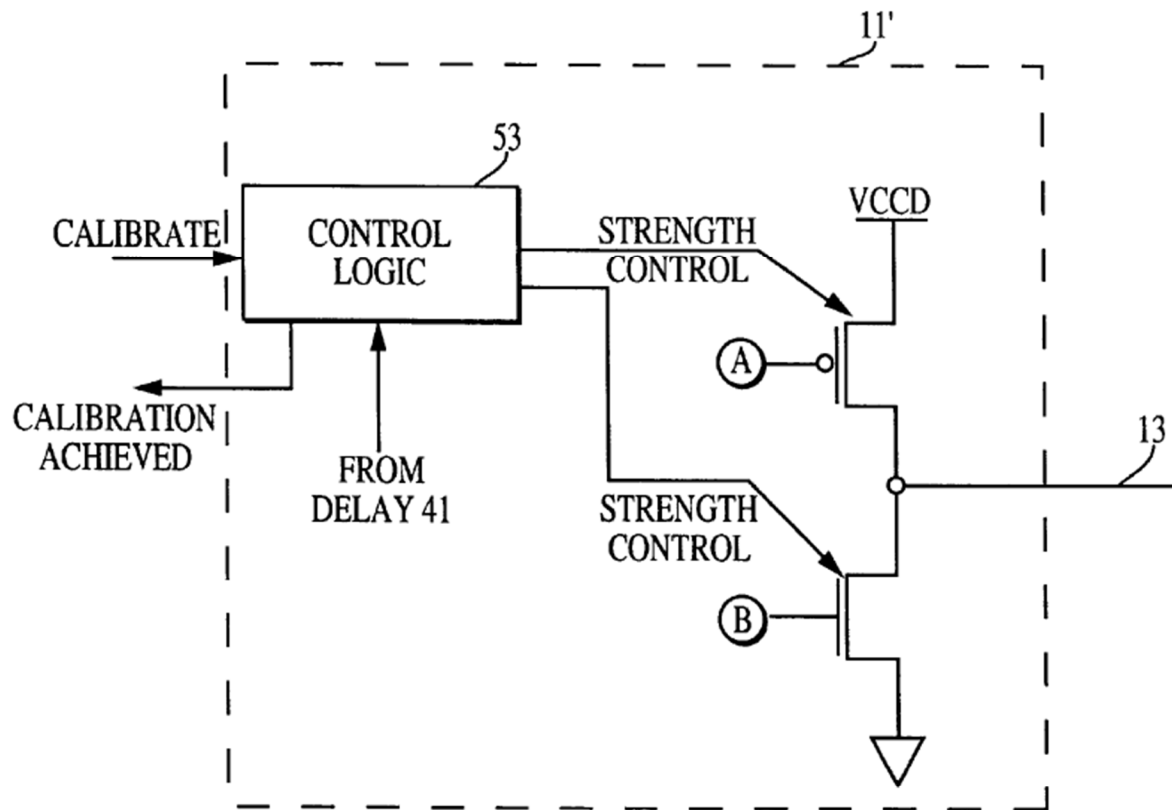


FIG. 4

EX1005 (Lee), FIG. 4. As another example, Thomann discloses that the output buffer includes a P-channel pull-up transistor and an N-channel pull-down transistor:

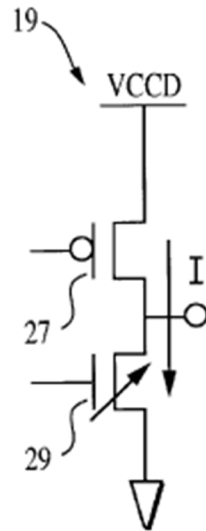


FIG. 2

EX1006 (Thomann), at FIG. 2. Thomann explains that the transistors “may be turned on in sequence or at the same time. *See id.* at 4:35-42. During calibration, Thomann discloses that both transistors are turned on the same time.

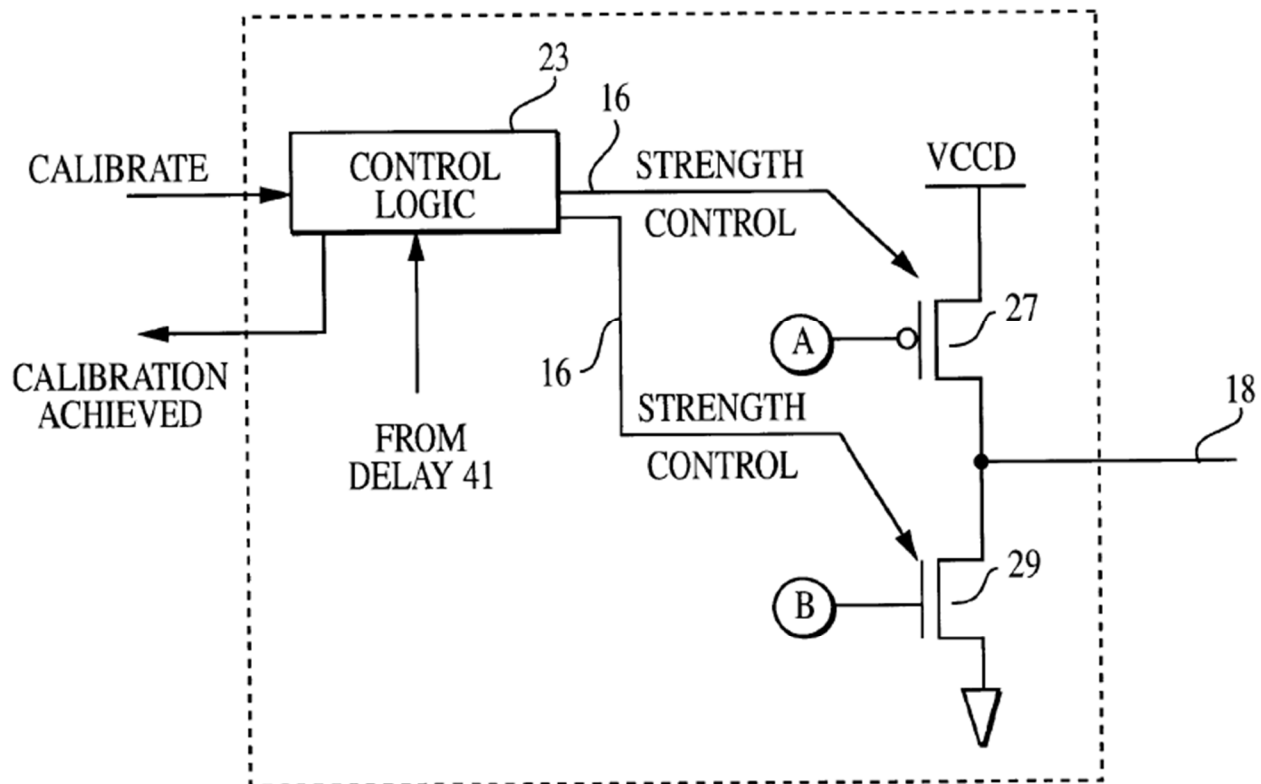


FIG. 5

EX1006 (Thomann), at FIG. 5, 6:7-16 (“Once calibration is completed ... it is no longer necessary for the buffer 19 to be connected to the mask data path 18, and it is therefore disconnected by the calibration logic circuit 23, which turns off both the pull up and pull down transistors 27 and 29 with appropriate signals to the A and B inputs of the transistors, as shown in FIG. 5. Now the data mask path 18 can be used the way it is normally used in a memory device for a data masking operation.”). As another example, Lee discloses an output buffer circuit 11 with a pull-down transistor 23 or pull-up transistor 21 to drive an output.

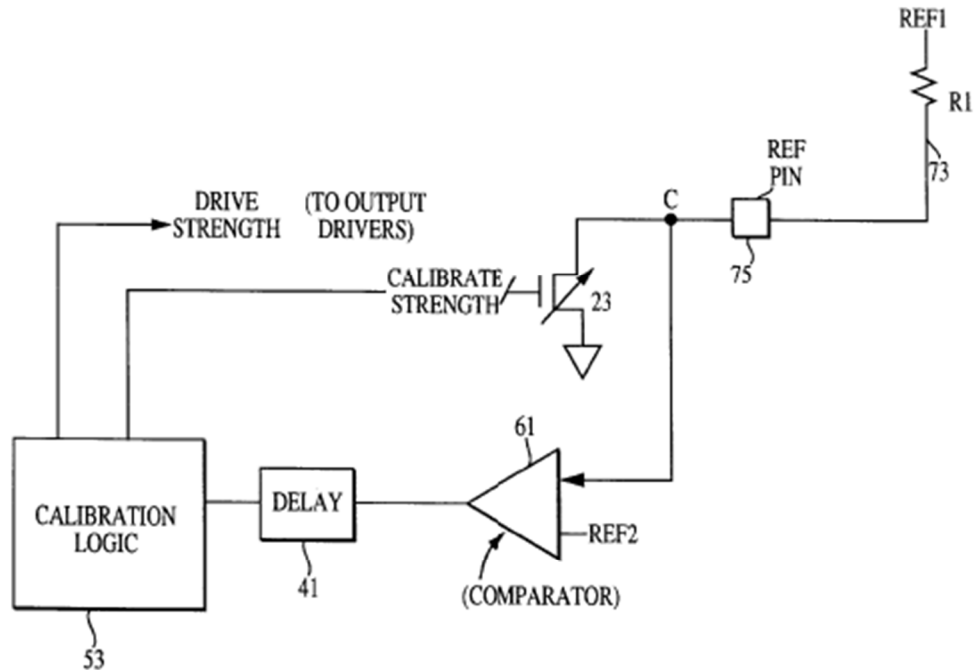


FIG. 6

Lee (EX1005), at FIG. 6, 6:11-53.

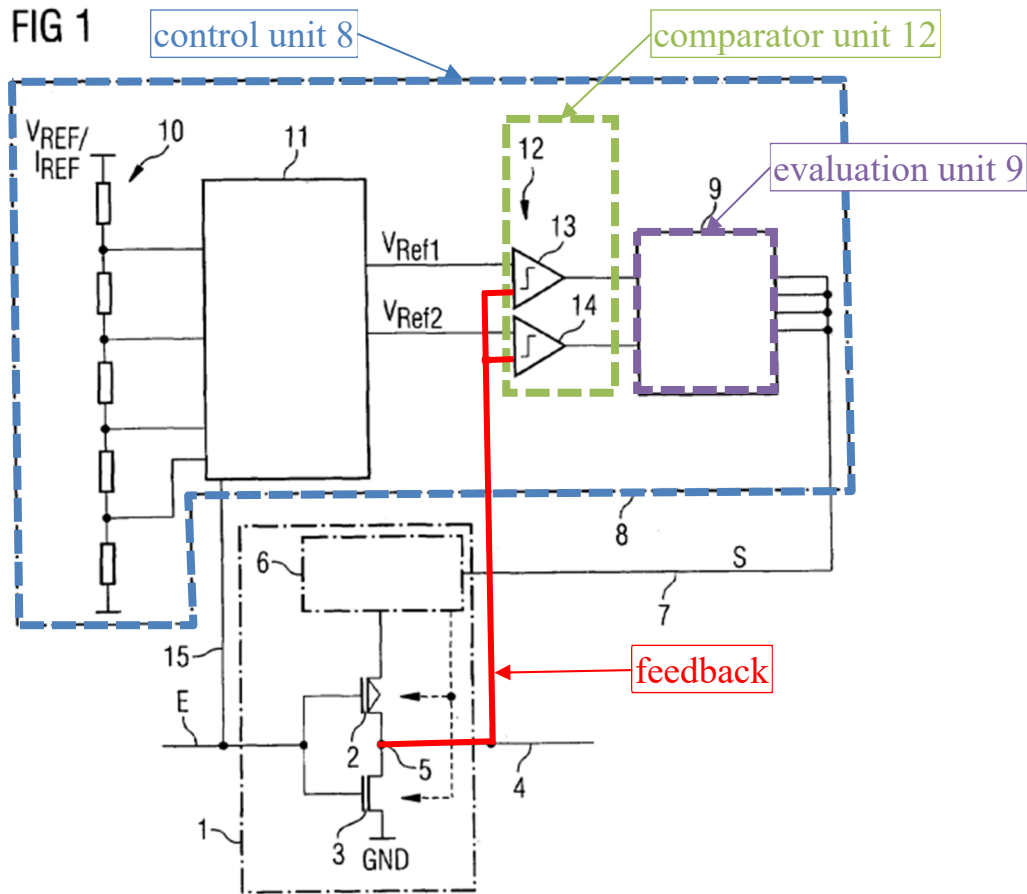
c. “a measuring circuit for measuring at least one of an output line current and an output line potential; and” [1.2]

81. As I explain below, Lee teaches claim limitation [1.3]. This claim limitation recites “an output line potential.” To a POSITA, a “potential” is synonymous with a “voltage,” which is the difference in potential between two points, such as between a specific point and a reference point like ground, which has a potential at or near zero. More specifically, an electric potential is conventionally an amount of work to move a unit of charge from a reference point, such as ground, to a specific point in an electric field. Consistent with this common

understanding, the '369 Patent indicates that an example of “a low supply potential” is a “ground potential GND.” '369 Patent (EX1001), at 3:19-25, 4:15-17.

82. While the '369 Patent provides an example of a “*measuring circuit*” for measuring a “*current*” at the output line (*see, id.* at 5:65-6:3), it is unclear from the disclosure of the '369 Patent what “*measuring circuit*” is for measuring a “*potential*” at the output line before comparing the measured output line potential to a reference potential. As I explain in more detail below, Lee teaches claim limitation [1.3] because it contains a similar structure as disclosed in the '369 Patent between the output line and circuitry for comparing the output line potential.

83. As shown in Figure 1 of the '369 below, a wire annotated in red connects the output of the driver circuit 1 and the input of a comparator unit 12, which is annotated in green:



'369 Patent (EX1001), at FIG. 1. The specification of the '369 Patent ("369 Specification") explains that the control unit 8, as annotated in blue in the figure above, includes a comparator unit, annotated in green, for comparing the previously measured potential value to a reference. *Id.* at 3:19-25, 4:32-36. The comparator unit 12 is connected to an evaluation unit 9, annotated in purple in the figure above, that outputs the control signal 'S' to a setting circuit 6 to set the driver strength. *Id.* at 4:49-56.

84. Consistent with the '369 Specification, claim 1 of the '369 Patent recites an "output driver" that comprises the "measuring circuit" and a separate

“control unit” that “includes a feedback control . . . based on a measured value provided by the measuring circuit.” *Id.* at 6:57-7:3. In addition, claim 6 of the ’369 Patent recites that the “control unit” comprises “a comparator unit for comparing . . . the measured output line potential . . . [to] a reference potential value.” *Id.* at 7:26-30. Further, claim 7 of the ’369 Patent recites that the “control unit” comprises “an evaluation unit connected to the comparator unit . . . [for changing] the control signal based upon a result from the comparator unit.” *Id.* at 7:31-34. In summary, the “measuring circuit” measures the output line potential and provides the measurement as feedback to the “control unit,” including a “comparator unit,” to compare the measured output line potential to a reference and an “evaluation unit” for changing the control signal based on the result of the comparison. *Id.* at 6:57-7:34.

85. Similar to Figure 1 of the ’369 Patent in which there is a feedback path (shown in red above) from the output of the driver circuit to the comparator unit, Lee discloses a wire that feeds back the output voltage of output buffer 11 to a comparator (e.g., a differential amplifier in input receiver 15).

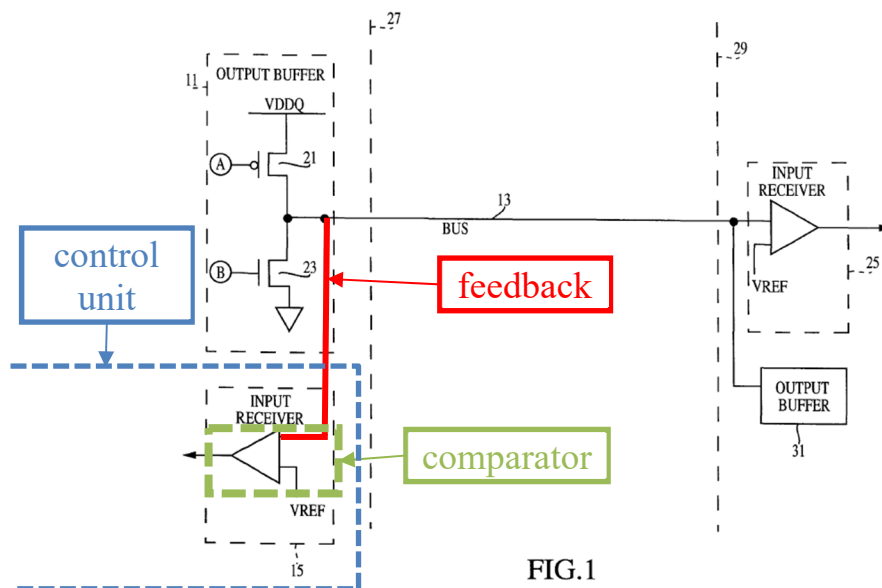
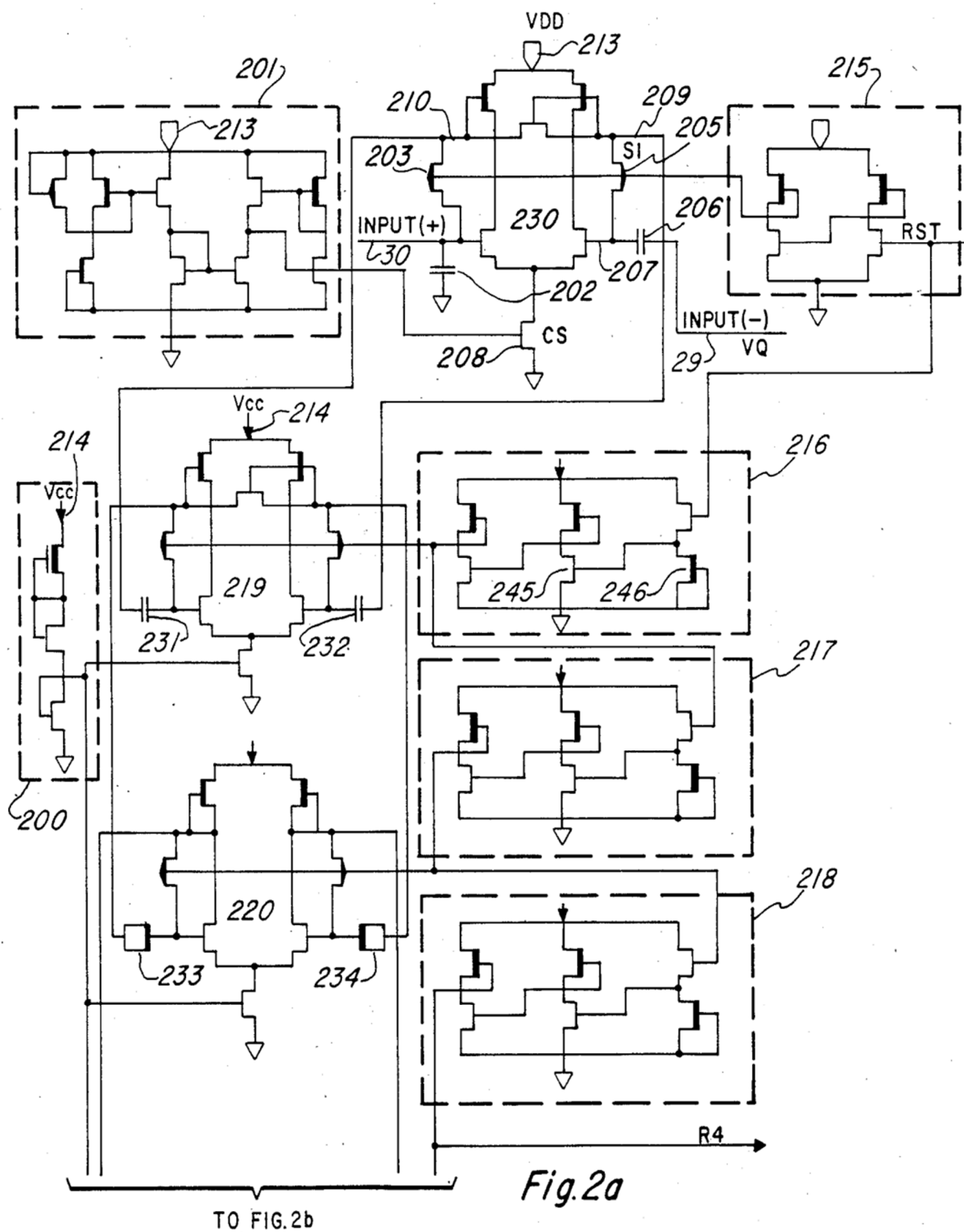


FIG.1

Lee (EX1005), at FIG. 1 (reproduced and annotated above), FIG. 5 (illustrating input buffer 15), FIGS. 3, 6 (illustrating comparator 61). And, similar to the comparator unit 12 disclosed in the '369 Specification, which compares the feedback output value to a reference, Lee discloses an input receiver 15 for comparing the feedback output value to a reference value. For example, Lee discloses that the input receiver 15 is implemented as “a common source differential amplifier” or alternatively “a higher accuracy comparator 61” to compare the bus voltage at the output to a voltage reference VREF. Lee (EX1005), at 3:43-46, 5:28-31. The result of the comparison is a “‘1’ or ‘0’ logic state ... depending on whether the bus voltage is higher or lower than VREF.” *Id.* at 4:46-49; *see also id.* at FIGS. 1-3, 5-6. Accordingly, Lee teaches a “*measuring circuit*” that is similar to the one described in the '369 Specification. Both the '369

Specification and Lee disclose that the output of the driver is fed back via a wire, annotated in red above, to a comparator unit that compares the driver output to a reference voltage, as shown in green above. *See* '369 Patent (EX1001), at FIG. 1; Lee (EX1005), at FIG. 1.

86. Further, Lee also teaches a “measuring *circuit*” for measuring the output-line potential that is part of its input receiver, which is part of the “*control unit*” identified below. *See infra* Section X.A.1.d (claim limitation [1.3]). Lee discloses that the input receiver is “typically implemented as a common source differential amplifier.” Lee (EX1005), at 3:43-46. A POSITA would have understood that a common source differential amplifier compares two inputs by measuring them relative to a common source voltage. For example, U.S. Patent No. 4,665,326 to Domogalla (EX1011) discloses circuitry for a comparator implemented as a common source differential amplifier as shown below.



EX1011 at FIG. 2a, 5:45-6:51. Domogalla's comparator includes a preamplifier section with four stages (stages 230, 219, 220 in FIG. 2a above and stage 221 as shown in FIG. 2b) and a power amplifier (as shown in FIG. 2b). *Id.*, at FIGS. 2a-2b, 5:45-50. For stage 230, the two inputs to the circuitry are provided on lines 29 and 30 as "INPUT(-)" and "INPUT(+)," and the output of stage 230 is provided on lines 209 and 210. *Id.* at 5:54-57. As shown in Figure 2a of Domogalla above, the two inputs on lines 29 and 30 are provided to the control terminals of two n-channel transistors. *Id.* at FIG. 2a. The comparator also includes a common source transistor 208, labeled "CS," that connects the source of the two transistors to a common ground supply. *Id.*

87. Accordingly, a POSITA would have understood that in a comparator implemented as a common source differential amplifier, as in Lee and Domogalla, the common ground supply enables the circuitry to measure the two inputs in a relative manner with more accuracy. For example, a POSITA would have recognized that such an amplifier would improve the accuracy of the differential amplifier by rejecting the voltage common to both inputs. *See, e.g.,* Domogalla (EX1011), at 5:53-57.

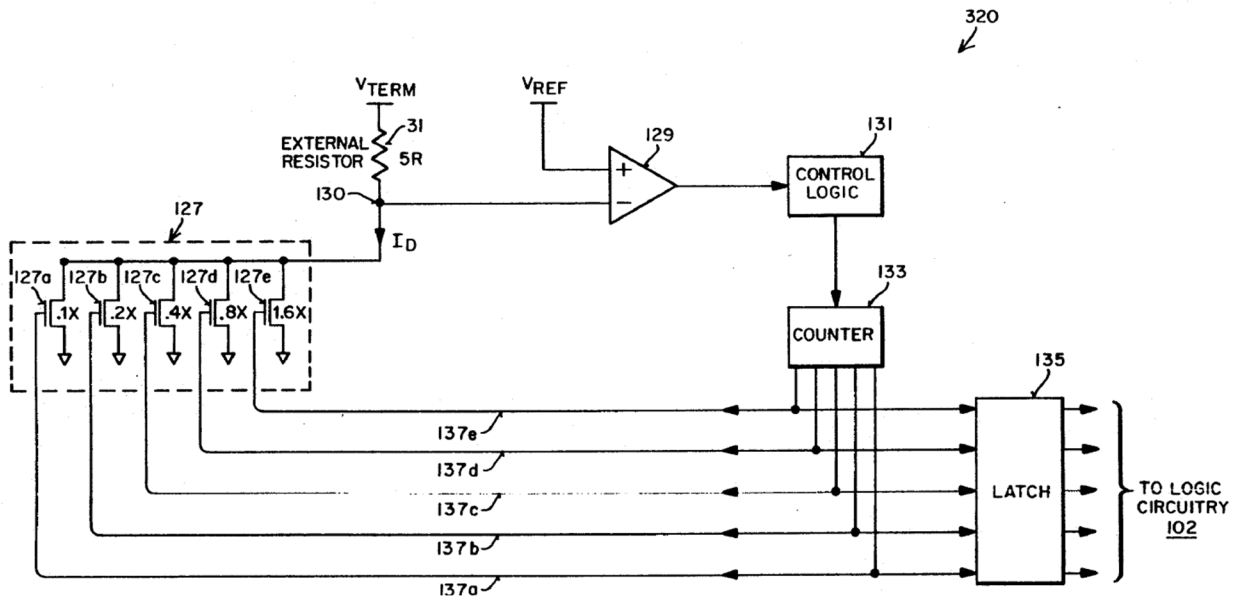
88. Thus, a POSITA would have understood that Lee's common source differential amplifier measures the voltages at its inputs, including the output

voltage, relative to a common source and amplifies the difference between the voltages while rejecting the common source voltage between the two inputs. *Id.*

89. In addition to teaching calibration by comparing the output voltage or output potential to a reference voltage or reference potential, Lee teaches that calibration may also be performed by comparing the drive current on the bus 13 to a reference drive current value. Lee (EX1005), at 7:22-26. As Lee explains, “[a]lthough the calibration circuit and method of the invention have been described and illustrated with reference to a comparison of bus voltage in a reference voltage VREF, calibration may also be obtained by comparing the drive current on the bus 13 with a reference drive current.” *Id.* It would have been obvious to a POSITA that to be able to compare a drive current with a reference current, the drive current output by the driver must be measured by a measuring circuit, as I explain below.

90. For example, U.S. Patent No. 5,254,883 to Horowitz (“Horowitz”) discloses a comparator, as illustrated in Figure 6 below, that receives one input from a voltage reference VREF and another input from a node (130).

FIG 6

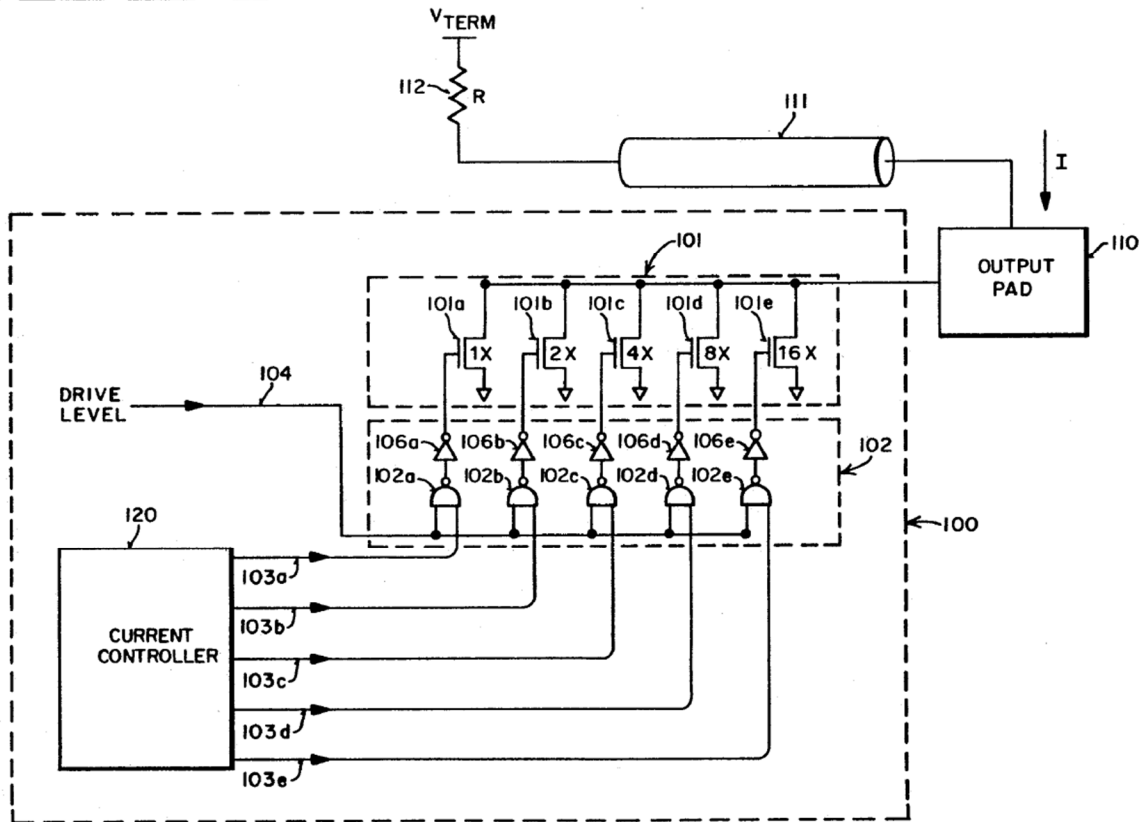


Horowitz (EX1010), at FIG. 6, 10:8-11:18. A current I_D flows from a voltage supply (V_{TERM}) through an external resistor (31) and a transistor array (127).

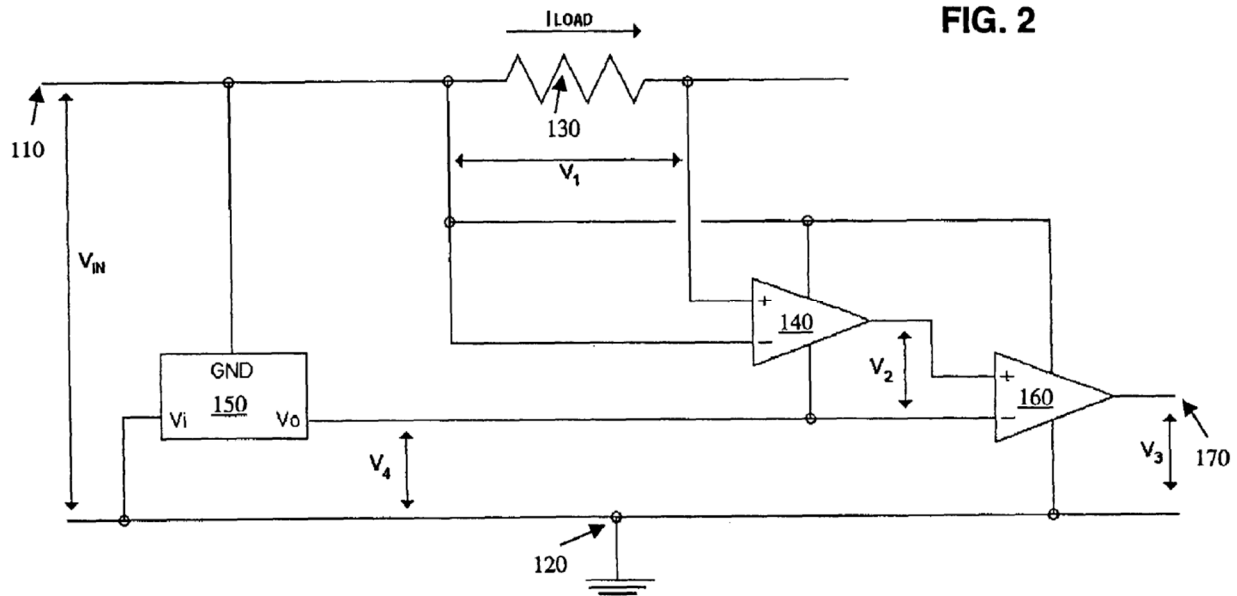
Horowitz explains that external resistor 31 “is used to set the value of the desired current of transmission line 111” (which is shown below in Figure 4 of Horowitz.

Id. at 10:32-33, FIG. 4 (below). Accordingly, a POSITA would have understood that the output line current (e.g., current of transmission line 111) in Horowitz is measured by converting that current to a voltage based on the resistance of the external resistor (31) and the resistance of the transistor array (127). A POSITA would also have understood that the reference voltage V_{REF} corresponds to a reference drive current because it is compared to a voltage corresponding to a measured drive current.

FIG 4



91. As another example, U.S. Patent No. 6,985,037 to Veal ("Veal") discloses a differential amplifier 140 that receives two inputs connected to the two terminals of a resistor 130.



Veal (EX1014), FIG. 2, 3:24-30. As shown in the figure above, a load current (I_{LOAD}) flows through the resistor (130) to provide a voltage drop across the resistor of V_1 . *Id.* at Abstract. Differential amplifier 140 therefore amplifies the voltage difference at its input (V_1) by a gain (A_1) to provide an output at another voltage (V_2). *See id.* at 3:64-4:1. Accordingly, a POSITA would have understood that the resistor 130 is used to measure the output current (I_{LOAD}) and that measurement is amplified by amplifier 140. *See id.*

92. As another example, Circuit Design, Layout, and Simulation, 2nd Edition (IEEE Press) (2005) discloses an operational amplifier that receives a voltage reference (V_{REF}) at an input (vp) and a measured feedback voltage at another input (vm).

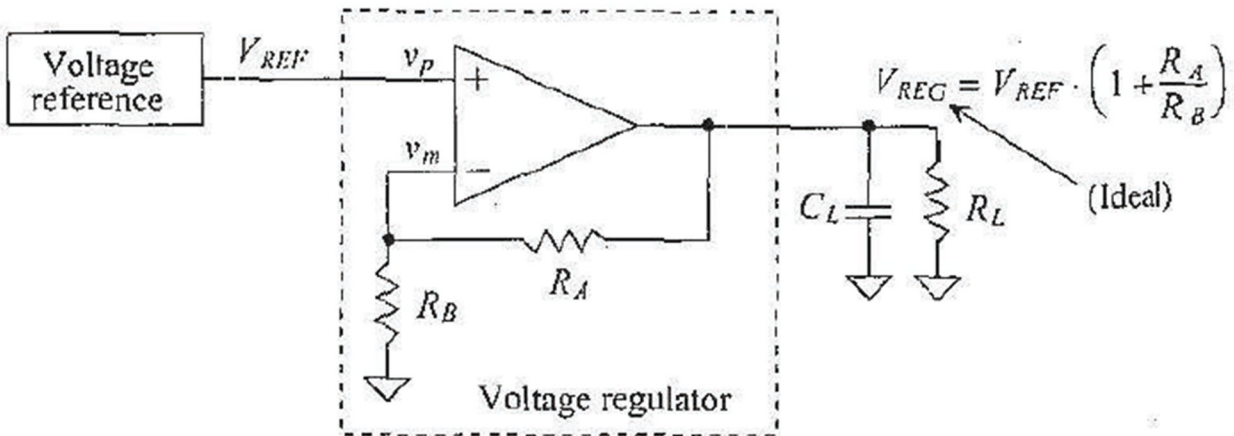


Figure 24.54 Schematic of a voltage regulator.

EX1012 at 813 (FIG. 24.54). The measured feedback voltage corresponds to the voltage at a node between two resistances, R_A and R_B , in which current flows through the resistances and ratio of the resistances sets the expected regulated voltage at the output. *See id.* at 812-13; *see also id.* at 814-17, FIG. 24.56 (illustrating schematic of circuit on page 815). Accordingly, a POSITA would have understood that the resistors R_A and R_B are used to measure the feedback current as a voltage (v_m) that is input to be compared to a voltage reference. *See id.*

93. Thus, Lee also teaches “a measuring circuit for measuring . . . an output line current.”

d. “a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a

desired power range of a specification-prescribed potential range and a specification-prescribed current range,” [1.3]

94. Lee teaches claim limitation [1.3], as I discuss below. In Figure 5 of Lee, he shows a calibration control logic circuit 53 that is connected via delay 41 to an input receiver/buffer 15:

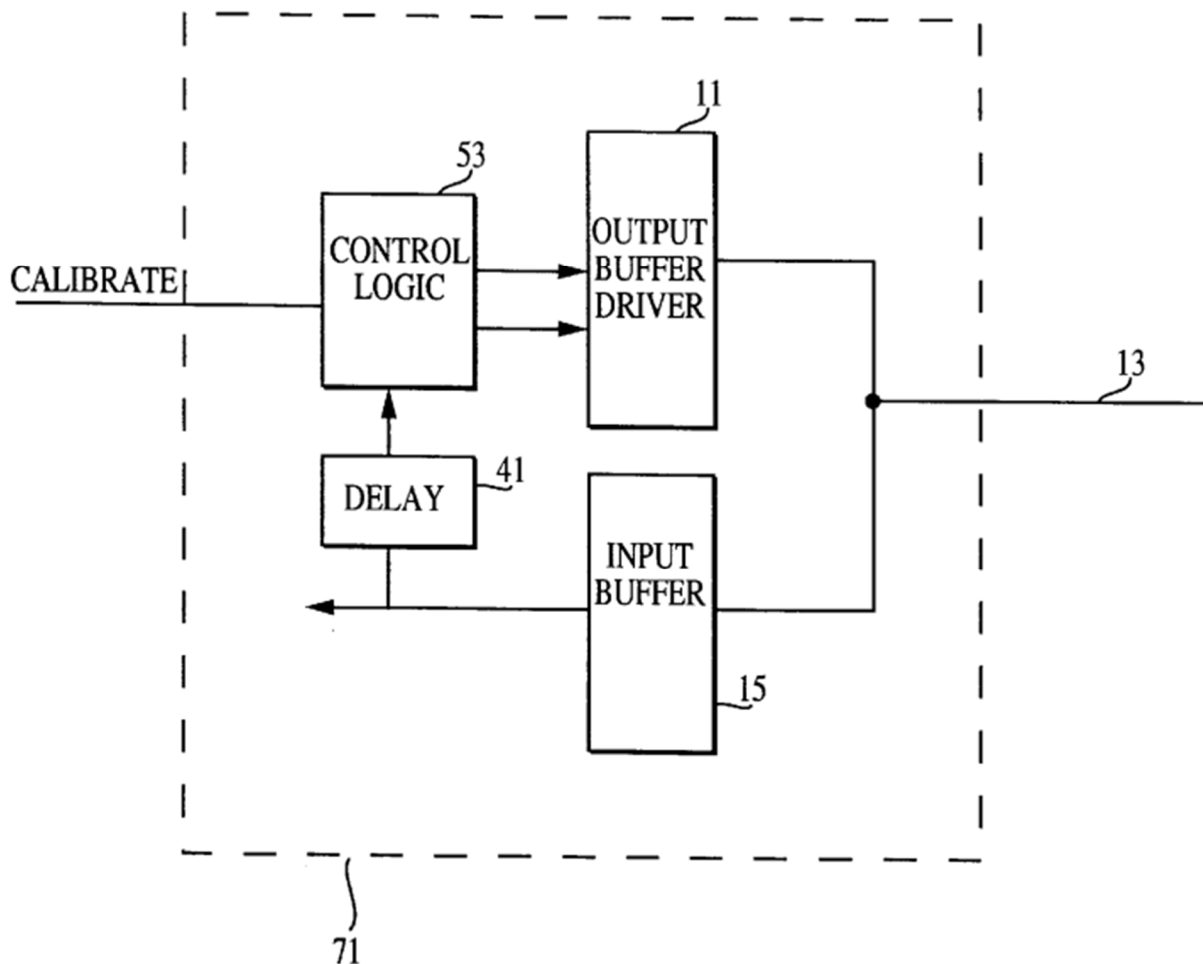
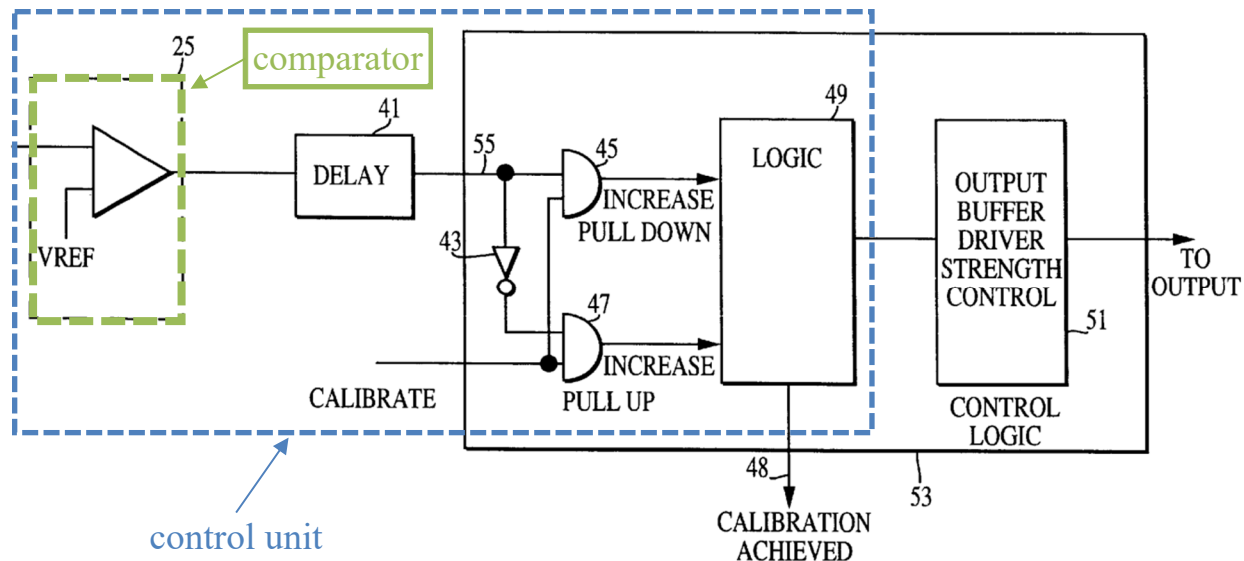


FIG. 5

Lee (EX1005) at FIG. 5.

95. Lee illustrates the circuitry of the input receiver/buffer 15 and control logic 53 in more detail in Figure 2, shown below.



Lee (EX1005), at FIG. 2. Although Figure 2 of Lee illustrates control logic 53 sampling an input receiver 25, Lee explains that the logic of Figure 2 can sample the output of the input receiver 25 (as shown) or input receiver 15, which is located along with the output buffer driver (11), as shown in Figures 1 and 5 of Lee. *See id.* at 4:31-34, FIGS. 1, 2, 5. Further, although Figure 2 of Lee illustrates control logic 53 for increasing the pull down or pull up drive strength, Lee also teaches that the control logic can decrease the pull down or pull up drive strength by, for example, adjusting the number of parallel pull-down or parallel pull-up transistors. *See, e.g.*, Lee (EX1005), at 2:39-44, 4:6-30, 4:62-5:18. Lee also teaches different algorithms, such as a binary search algorithm:

For example, a binary search algorithm can be used to seek the best output buffer driver setting by first using coarse driver strength adjustments by logic 49 until the input receiver 25 (or 15) changes state and thereafter having logic 49 make finer adjustments in the opposite direction until receiver 25 (or 15) changes state again. This back and forth adjustment using finer strength adjustment stages can continue until a predetermined end point is reached.

Id. at 5:19-27. As Lee explains, such an algorithm enables adjustments in both directions, increasing and decreasing the drive strength setting, to achieve the best output buffer driver setting. *Id.*

96. As illustrated in Figure 2, Lee teaches that the input receiver/buffer includes a comparator, as annotated in green above, and that the logic circuit 49 provides a signal for appropriate strength adjustments to an output buffer driver strength control circuit 51. *Id.* at FIG. 2, 4:58-61; *see also supra* Section X.A.3 (claim 5) (addressing the circuit 51 which is a “*setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit*”).

97. The comparator illustrated in Lee compares the output voltage to a voltage reference (VREF) and generates a resulting signal with “either a ‘1’ or ‘0’ logic state . . . depending on whether the bus voltage is higher or lower than VREF.” Lee (EX1005), at 4:46-48. The resulting signal is input to circuitry that provides a request to logic circuit 49 to change the drive strength. *Id.* at 4:46-55; *see also Id.* at FIG. 2 (delay 41, inverter 43, and AND-gates 45 and 47).

Specifically, the logic circuit 49 outputs “an appropriate strength adjustment command” based on its inputs that adjusts the output driver strength of the pull-down transistor or the pull-up transistor. EX1005 at 4:49-61. Thus, Lee teaches “*a control unit for providing a control signal for setting a driver strength of the driver circuit.*”

98. Lee also teaches setting the driver strength “*to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range,*” as I explain below.

99. Although the ’369 Patent generically references “specifications for integrated circuits . . . for SDRAM and DDR memory” (EX1001 at 1:39-40), it is unclear what “specification-prescribed” means in the terms “a specification-prescribed potential range” and “a specification-prescribed current range.” The ’369 Patent does not identify any particular specification available at the time, it does not provide a definition or example of a range that is prescribed by a specification, and it does not specify what ranges are included in, or excluded from, the meaning of a “*specification-prescribed*” range. Also, the ’369 Patent does not expressly define or otherwise explain how a “*power range*” is “*desired*” or by whom it is “*desired*.” Looking at the ’369 Specification, the word “*desired*” only appears once to describe a prescribed “potential value range.” *Id.* at 5:8-13.

To the extent there is a sufficient disclosure in the '369 Patent for a “*specification-prescribed*” range and a “*desired*” power range, Lee discloses those ranges as I explain below.

100. Regarding a “*specification-prescribed potential range*,” Lee teaches that the output range in normal operation is between VDDQ and ground. As shown below, transistor 21 of the output buffer 11 is connected to a voltage supply VDDQ and transistor 23 of the output buffer is connected to a ground supply.

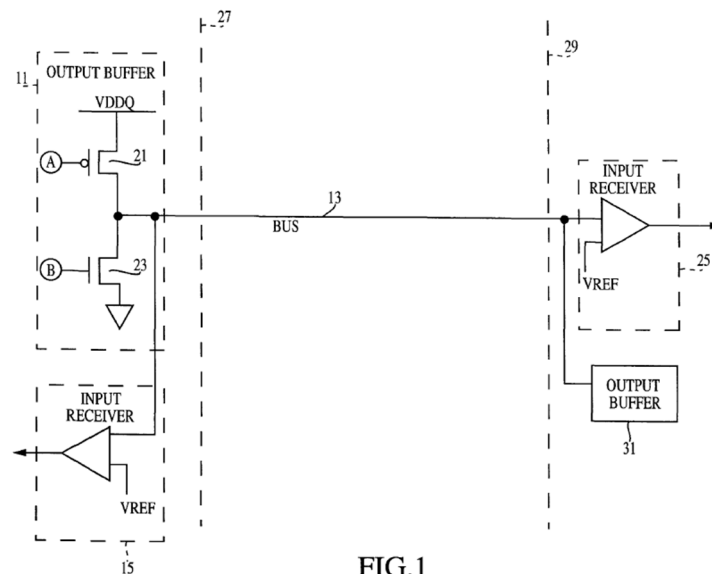


FIG.1

Lee (EX1005), at FIG. 1, 3:33-41, 10:6-12 (claim 32 of Lee) (“wherein said driving circuit has said pull-up device coupled to a first voltage potential V1 and said pull-down device coupled to a second voltage potential V2, and said reference voltage is established at a voltage in between V1 and V2.”), 12:37-46 (claims 70-72 of Lee). Accordingly, a POSITA would have understood that the range of the output-line voltage during normal operation is between VDDQ and a ground

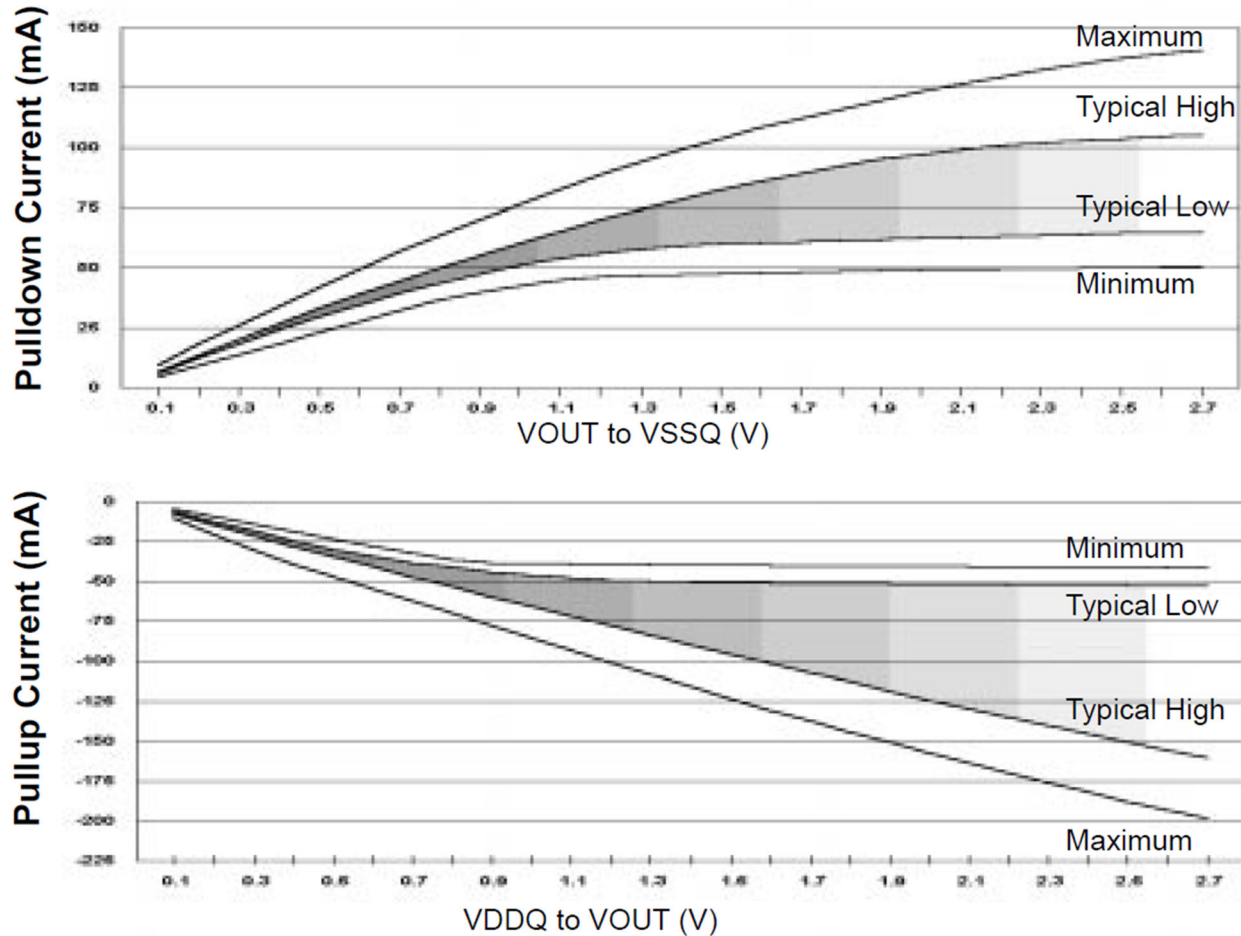
potential. Further, the range between VDDQ and ground is expressly prescribed by Lee's specification, which is part of the Lee's patent which pre-dates the priority date of the '369 Patent (*see supra* Section VI.D (Priority Date)), and thus teaches a "*specification-prescribed*" potential range to the extent the term is sufficiently disclosed by the '369 Patent.

101. Lee also teaches "*a specification-prescribed current range.*" Lee discloses that current-versus-voltage curves for output buffer drivers are specified with minimum limits and maximum limits for the voltage and current levels.

"Some of the benefits obtained by calibrated output buffer drivers can be achieved by closing [sic] specifying the driver characteristics for all transistors in an output buffer driver and all output buffer drivers in a system. Techniques such as specifying minimum and maximum output currents, specifying the current versus voltage curves with minimum and maximum limits, and by providing limits on the minimum and maximum slew rates have been used."

Lee (EX1005), at 1:26-33 (added emphasis). A POSITA would have understood and found it obvious from this disclosure in Lee that for a given voltage on one axis of the current-versus-voltage curve, the corresponding current on the other axis of the curve must be in a range between minimum and maximum limits. For example, as shown below in the exemplary curves from JEDEC's DDR JESD79 specification, which are similar to the curves disclosed by the '369 Patent, as the voltage increases (as labeled on the horizontal axis), the magnitude of the pulldown

and pullup currents (as labeled on the vertical axis in milliamps) also generally increases.



JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79 (EX1007), at 59; *see* '369 Patent (EX1001), at FIGS 2a-2b. This relationship is also shown below in the data points across voltages and currents:

Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Id. at 60. As I explained above, Lee teaches a voltage range during normal operation between VDDQ and ground. A POSITA would have understood and found it obvious that when the output is at each of these two voltages there is a corresponding current range between the minimum and maximum limits that are individually and collectively “a specification-prescribed current range.” For example, for a VDDQ to ground voltage of 2.5 volts, the pull-up current would

range between 50.2 and 137.3 milliamps and the pull-down current would range between -41.0 and -187.6 milliamps, according to JESD79 (see table reproduced above). *Id.* at 59-60.

102. Lee also teaches a “*desired power range*,” to the extent it is sufficiently described by the ’369 Specification, that is the product of the prescribed potential and current ranges. As explained above, Lee teaches “*a specification-prescribed current range*” and “*a specification-prescribed potential range*” between the minimum and maximum currents associated with VDDQ and ground. Lee also teaches an ensured potential range because its calibration scheme ensures that the output voltage of the driver swings across a range, between a high voltage (VOH) and a low voltage (VOL). *See* Lee (EX1005), at 3:6-24, 4:35-61, FIG. 2, FIG. 3 (below). In addition, Lee’s invention “ensures that the calibration scheme adjusts the VOH and VOL levels to be symmetric about a midpoint voltage, VREF.” *See id.* at 3:6-9. In calibration, both transistors in Lee’s output buffer are turned on and the output voltage of the bus is compared to VREF, as shown in Figure 3 below.

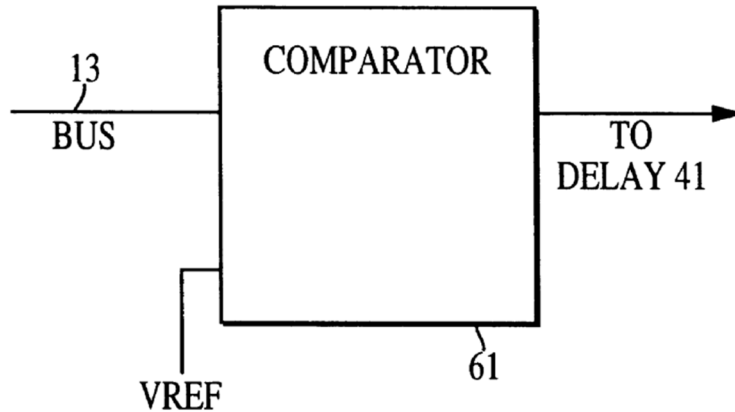


FIG. 3

Id. at FIG. 3. Accordingly, a POSITA would have understood that the VOH and VOL levels, adjusted via calibration to be symmetric about VREF or VDDQ/2, would be used during normal operation to represent the high or low logic states of the output line. *See id.* at 3:47-53; *see also id.* at 3:6-9 (VOH and VOL symmetric about VREF), 1:61-63 (same), 3:56-58 (VREF is equivalent to VDDQ/2). A POSITA would have also understood that the VOH level for Lee’s output buffer driver is no higher than VDDQ because the pull-up transistor 21 is supplied VDDQ and that the VOL level is no lower than a ground potential because the pull-down transistor 23 is supplied the ground potential. *Id.* at 3:33-41, FIG. 1.

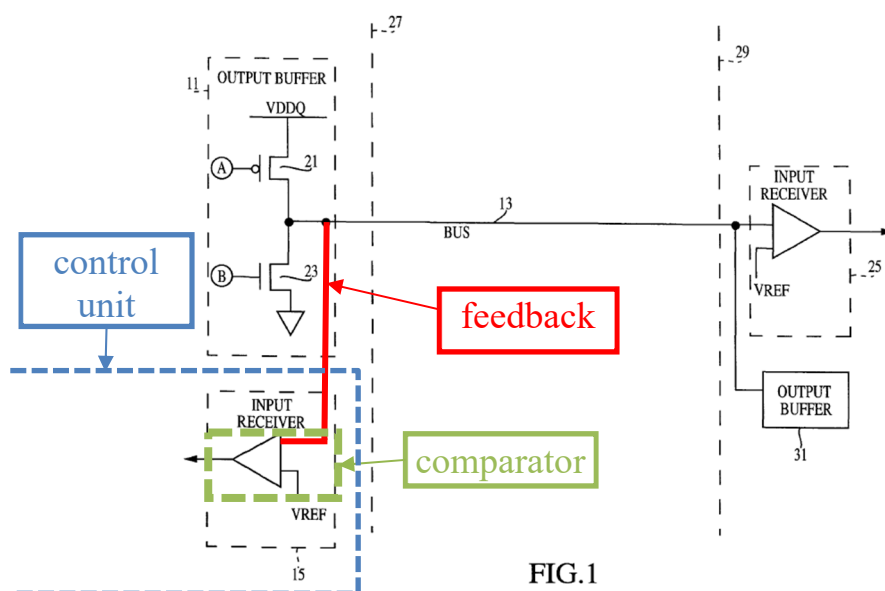
103. Further, a POSITA would have understood that the specified potential and current ranges in Lee define an intended “*power range*” for the output buffer

driver. A POSITA would have been familiar with Ohm's law, which defines current through a resistor as equivalent to a voltage across a resistor divided by the resistance of the resistor (i.e., $I = V / R$). A POSITA would also have been familiar with how to represent power as the product of voltage and current (i.e., $P = I \times V$). A POSITA would have recognized that the definition of current or voltage, consistent with Ohm's law, can be substituted to represent power as the product of voltage and a voltage across a resistor divided by the resistance of the resistor (i.e., $P = (V / R) \times V$), which is equivalent to the potential squared divided by resistance (i.e., $P = V^2 / R$), or as the product of current and a current multiplied by resistance (i.e., $P = I \times (I \times R) = I^2 \times R$). Accordingly, it would have been obvious to a POSITA that Lee teaches a "*desired power range*" that is between V_{OH} and V_{OL} (which is between V_{DDQ} and ground) and the corresponding minimum and maximum current range(s) for each or both of the voltages. See Lee (EX1005), at 1:26-33, FIG. 1. Thus, Lee teaches drive strength adjustment "*to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*"

e. “wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.” [1.4]

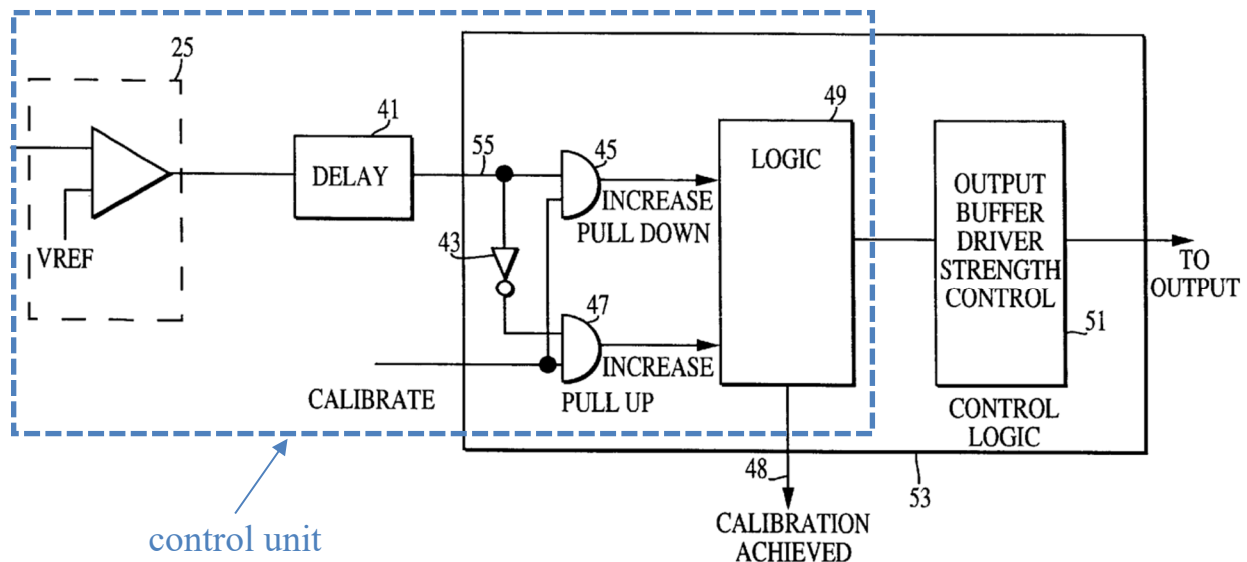
104. As I discussed above for claim limitation [1.2], to the extent a “*measuring circuit for measuring*” an “*output line potential*” is supported by the ’369 Specification, the limitation is taught by Lee. *See supra* Section X.A.1.c. Similarly, to the extent the ’369 Specification supports “*a measured value provided by the measuring circuit,*” as recited in claim limitation [1.4], Lee teaches claim limitation [1.4].

105. As shown in Figure 1 below, Lee discloses that the output of the driver is fed back (“*a measured value provided by the measuring circuit*”) to a comparator via a wire to compare the output potential or current to a reference.



Lee (EX1005) at FIG. 1 (annotations added); *see also id.* at FIG. 5 (input buffer 15), FIGS. 3, 6 (comparator 61), 7:26-32 (providing a “reference current from an external circuit which is compared to the drive current of the transistor whose strength is to be adjusted”). As I explained above for claim limitation [1.2], this disclosure in Lee is similar to the wire disclosed in the ’369 Patent that feeds back the output to a comparator unit. *See supra* Section X.A.1.c.

106. The result of the comparison in Lee is provided to additional circuitry, including “a control unit,” that is used to determine the output buffer driver strength control (in output buffer driver strength control 51):



Lee (EX1005), at FIG. 2, 4:36-61; *see also id.* at FIGS. 4-6. Specifically, the result of the comparison in Lee is provided to delay circuit 41 and the output of the delay circuit 41 is provided via line 55 and inverter 43 to AND gates 45 and 47. *Id.* at

FIG. 2, 5:46-58. The two AND gates (45 and 47) enable driver strength adjustments, such as increasing the pull-down or pull-up drive strength, when the CALIBRATE signal is asserted to indicate the start of calibration. *Id.* at FIG. 2, 5:39-41, 5:49-55. Thus, Lee teaches a control unit that includes a feedback control, in the feedback path from the comparison circuit, to affect the setting of the driver strength (via output buffer driver strength control 51) based on a measured value provided by the measuring circuit that is input to the comparison circuit (e.g., input receiver 15). *See id.*

2. Claim 2: “The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude.”

107. As I explained above for claim limitation [1.3], Lee teaches a desired power range during normal operation with a prescribed voltage range between VDDQ and ground and a desired voltage range between VOH and VOL within the prescribed range. *See supra* Section X.A.1.d. A POSITA would have understood that Lee’s desired power range is determined, in part, by the ground potential (“a *specification-prescribed lower potential limit value*”) that is lower in potential than VDDQ. Lee (EX1005), at FIGS. 1-2. For example, claims 32-34 of Lee recite two

voltage potentials, V1 and V2, in which the pull-up device is coupled to V1, a positive voltage potential, and the pull-down device is coupled to V2, ground:

“32. A method as in claim 1, wherein said driving circuit has said pull-up device coupled to a first voltage potential V1 and said pull-down device coupled to a second voltage potential V2, and said reference voltage is established at a voltage in between V1 and V2.

33. A method as in claim 32, wherein V1 is a positive voltage potential and V2 is ground.

34. A method as in claim 33, wherein said reference voltage is established as a voltage of substantially $V1/2$.”

Id. at 10:6-13.

108. Lee also teaches adjusting the low voltage level, VOL, via drive strength settings during calibration such that the high voltage level, VOH, and VOL are symmetric about a reference voltage, VREF. *See* EX1005 (Lee), at 3:47-53, 10:6-13 (claims 32-24, reproduced above).

109. Accordingly, a POSITA would have understood that the power range intended by Lee’s specification is also determined by VOL (“*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*”), which is adjusted relative to the ground potential to achieve symmetry with VOH about VREF. EX1005 (Lee), at 3:47-53, 10:6-13 (claims 32-34), FIGS. 1-2.

110. Alternatively, Lee teaches this limitation under Patent Owner’s interpretation of the claim. I understand that Patent Owner alleges that VREF (a reference voltage for inputs and outputs) is an example of “*a specification-*

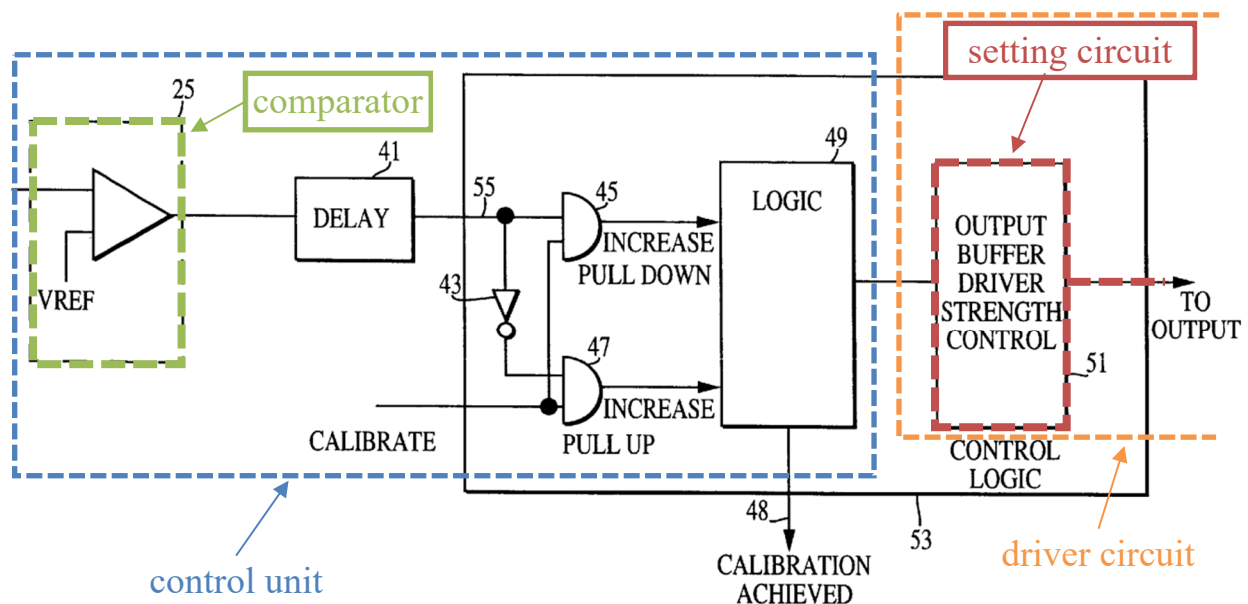
prescribed lower potential limit value” and VRN (the voltage of an impedance calibration output), adjusted relative to VREF, is “*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*”:

37. On information and belief, the desired power range of the output driver of the 369 Patent Infringing Products is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value, for example, VREF, and a specification prescribed lower potential limit value adjusted with the tolerance magnitude, for example, VRN adjusted relative to VREF.

EX1015 at ¶37; *see* EX1016 at 309. Under Patent Owner’s interpretation of claim 2, a POSITA would have understood that the power range intended by Lee’s specification during calibration is also determined by VREF, which is a reference voltage for inputs and outputs in Lee, (“*a specification-prescribed lower potential limit value,*” as alleged by Patent Owner) and by the output to the bus 13 in Lee that is adjusted relative to VREF. Lee (EX1005), at 3:8-10, 4:62-5:11, FIGS. 1, 2; *see supra* Section X.A.1.d. In particular, Lee’s output voltage that is output to the bus is compared to VREF to adjust the drive strength settings that, when applied, adjust the output voltage relative to VREF. *Id.* Thus, under Patent Owner’s interpretation that the voltage VRN is “*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*” because it is adjusted relative to VREF, Lee’s output voltage that is output to the bus also satisfies the same limitation because it is also adjusted relative to Lee’s VREF. *Id.*

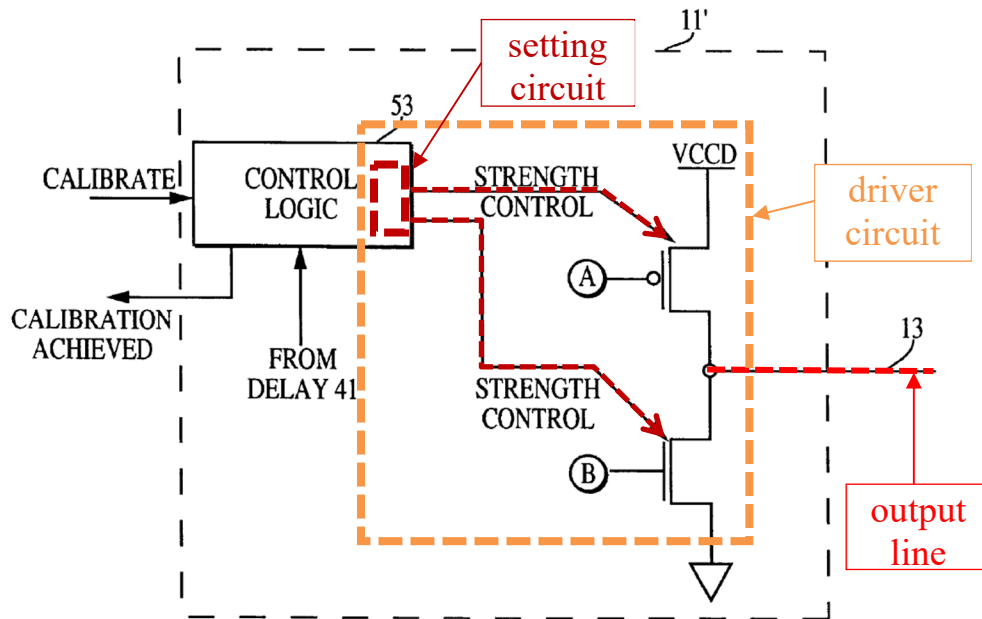
3. Claim 5: “The output driver of claim 1, wherein the driver circuit further comprises a setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit.”

111. As I explain below, Lee teaches claim 5. As shown in the figures below, Lee discloses a driver circuit that includes an output buffer driver strength control circuit 51 (“a setting circuit”) of control logic 53. The output buffer driver strength control circuit 51 receives an appropriate strength adjustment command from logic circuit 49 (“for receiving the control signal from the control unit”) and adjusts the output driver strength by providing an output from control logic 53.



Lee (EX1005), at FIG. 2, 4:58-61. As shown below in Figure 4 of Lee, the control logic 53 includes both the logic unit 49 (in the “control unit”) and the output buffer driver strength control circuit 51 (the “setting circuit”). In particular, the output

buffer driver strength control circuit 51 (“*setting circuit*”) in control logic 53 outputs a “STRENGTH CONTROL” signal for the pull-up and pull-down transistors of the driver circuit (“*for setting the driver strength of the driver circuit*”):



Id. at FIG. 4, 5:42-67; *see also id.* at FIG. 6, 6:54-63.

112. Lee also discloses that the output buffer driver, such as output buffer driver 11' in Figure 4 shown below and/or input/output buffer 71 in Figure 5 shown below, can include the control logic 53, delay 41, and/or input buffer 15:

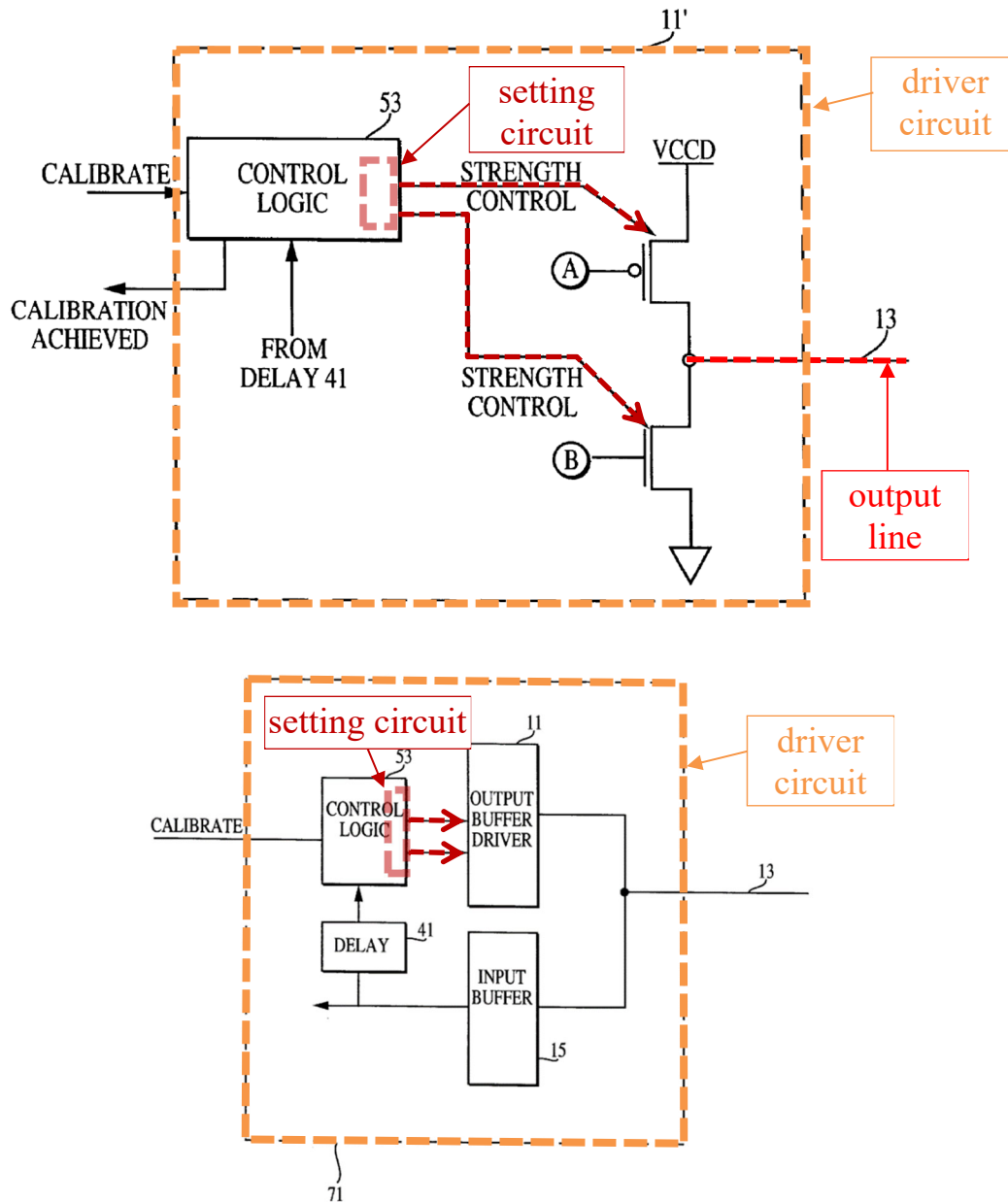
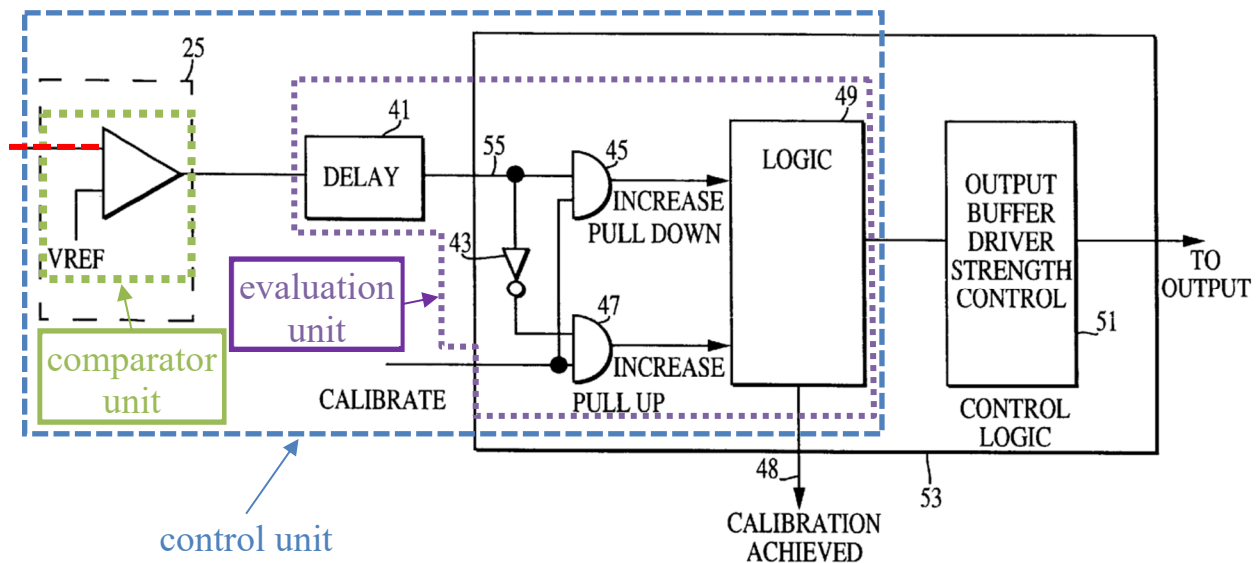


FIG. 5

Id. at FIGS. 4, 5, 5:42-47. Thus, Lee teaches “the driver circuit further comprises a setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit.”

4. Claim 6 (“The output driver of claim 1, wherein the control unit further comprises a comparator unit for comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value”) and claim 7 (“The output driver of claim 6, wherein the control unit further comprises an evaluation unit connected to the comparator unit, the evaluation unit configured to change the control signal based upon a result from the comparator unit”).

113. As I explain below, Lee teaches claims 6 and 7. As shown in the figure below, Lee discloses control logic and circuitry (the “control unit”), annotated in blue.



Lee (EX1005), at FIG. 2, 4:31-34, FIG. 1; *see also* Lee (EX1005), at 5:29-34, FIGS. 3, 6. The control unit includes a “comparator unit,” annotated in green, connected to an “evaluation unit,” annotated in purple. *Id.*

114. Lee explains that the comparator unit is implemented as “a common source differential amplifier” or “higher accuracy comparator” that compares the

measured output line potential (annotated in red in the figure above) with a reference potential (VREF) (“for comparing ... the measured output line potential ... with ... a reference potential value”). *Id.* at 3:41-46, 3:58-63, 4:46-49, 5:29-34; see also *id.* at FIG. 2 (above), 4:31-34, FIGS. 1, 3, 6. Lee also teaches that the comparator unit can compare the measured output line current with a reference current value (“for comparing ... the measured output line current ... with ... a reference current value”). *Id.* at 7:22-32.

115. Lee also explains that the output of the comparator is connected to the evaluation unit, which includes a delay 41, logic circuitry 45 and 47, and logic 49. Lee teaches that delay 41 ensures a precise comparison, that AND-gates 45 and 47 apply signals to logic 49 to instruct driver strength adjustments, such as increasing the pull-down or pull-up drive strength, when the CALIBRATE signal is logic high, and that logic 49 sends an appropriate strength adjustment command to output buffer driver strength control circuit 51. *Id.* at FIG. 2, 4:31-5:5, 4:17-30 (providing examples of drive strength adjustment techniques), 5:39-58. Accordingly, Lee also teaches that its evaluation unit changes the strength adjustment command based on the comparator output (“change the control signal based upon a result from the comparator unit”).

B. Claims 1, 2, and 5-7 are Obvious Over Lee and Thomann

116. In my opinion, Lee in combination with Thomann also renders obvious claims 1, 2, 5-7 of the '369 Patent.

1. Combination of Lee and Thomann

117. Ground 2 combines Lee with Thomann. As explained below, Thomann teaches how to calibrate an output buffer driver, such as the one disclosed in Lee, to achieve a symmetric midpoint voltage, V_{REF} .

118. As I explain below, a POSITA would have been motivated to combine Lee with Thomann and had a reasonable expectation of success in doing so. Both references relate to calibration of an output buffer driver. *See, e.g.*, Lee (EX1005), at Title (“Simple Output Buffer Drive Strength Calibration”); Thomann (EX1006), at Title (“High Speed I/P Calibration Using An Input Path and Simplified Logic”); *see also* EX1005 at Abstract; EX1006 at Abstract. Both references also share common inventorship. In particular, Terry R. Lee is the sole inventor of Lee and is the second-listed inventor of Thomann. *See* EX1005 at 1; EX1006 at 1. Further, both Lee and Thomann were originally assigned to the same entity—Micron Technology, Inc. *See id.* Moreover, Lee and Thomann both disclose the same field of invention. EX1005 at 1:6-8; EX1006 at 1:5-7. More specifically, Lee discloses an output buffer driver that feeds back the driver output to a comparison circuit to adjust the drive strength of the driver. Lee (EX1005), at FIG. 1, 3:13-32, 4:31-61;

see supra Section IX.A (Overview of Lee (EX1005)). Similar to Lee, Thomann discloses an output buffer driver that feeds back the output to a comparison circuit to adjust the drive strength. Thomann (EX1006), at FIG. 1, 4:19-24, 4:47-57; *see supra* Section IX.B (Overview of Thomann (EX1006)).

119. Lee recognizes that calibration adjusts the VOH and VOL levels at the output to be symmetric about a mid-point voltage, VREF (EX1005 at 3:7-9), and that different algorithms may be used for drive strength adjustment (EX1005 at 5:6-28), but it does not describe the specific range of VOH and VOL levels or how the output driver voltage swings between the VOH and VOL levels changes with calibration. However, Thomann does provide these details, showing the ranges of VOH and VOL levels and the voltage swing of the driver between the VOH and VOL levels, both before and after calibration. *See, e.g.*, EX1006 at 5:37-65, 6:17-31, FIGS. 1, 3.

120. In the example shown in Figure 3 below, Thomann shows that the range of the logic output high voltage (VOH) level spans between a minimum (VOH MIN) and a maximum (VOH MAX) and that the range of the logic output low voltage (VOL) level spans between a minimum (VOL MIN) and a maximum (VOL MAX).

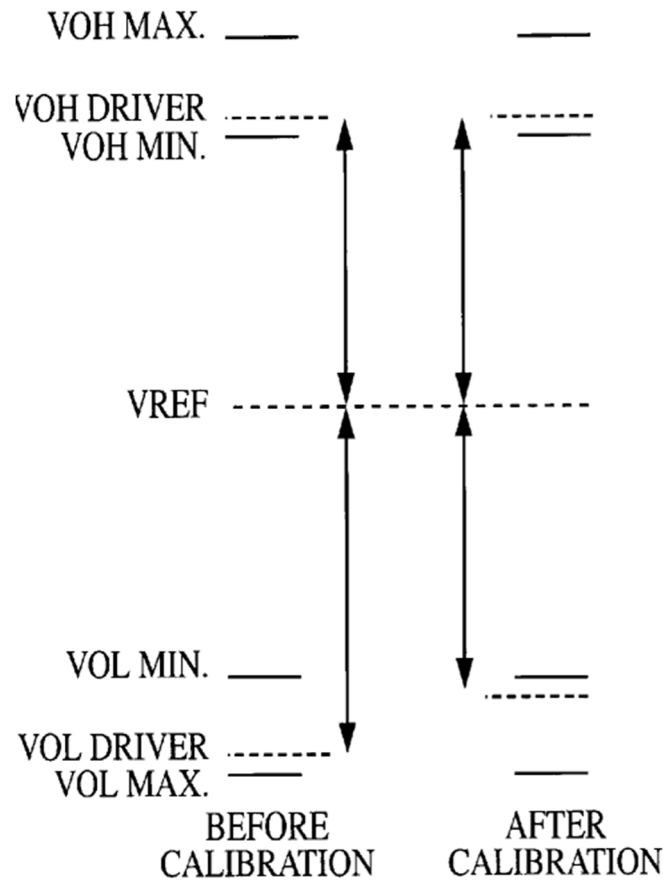
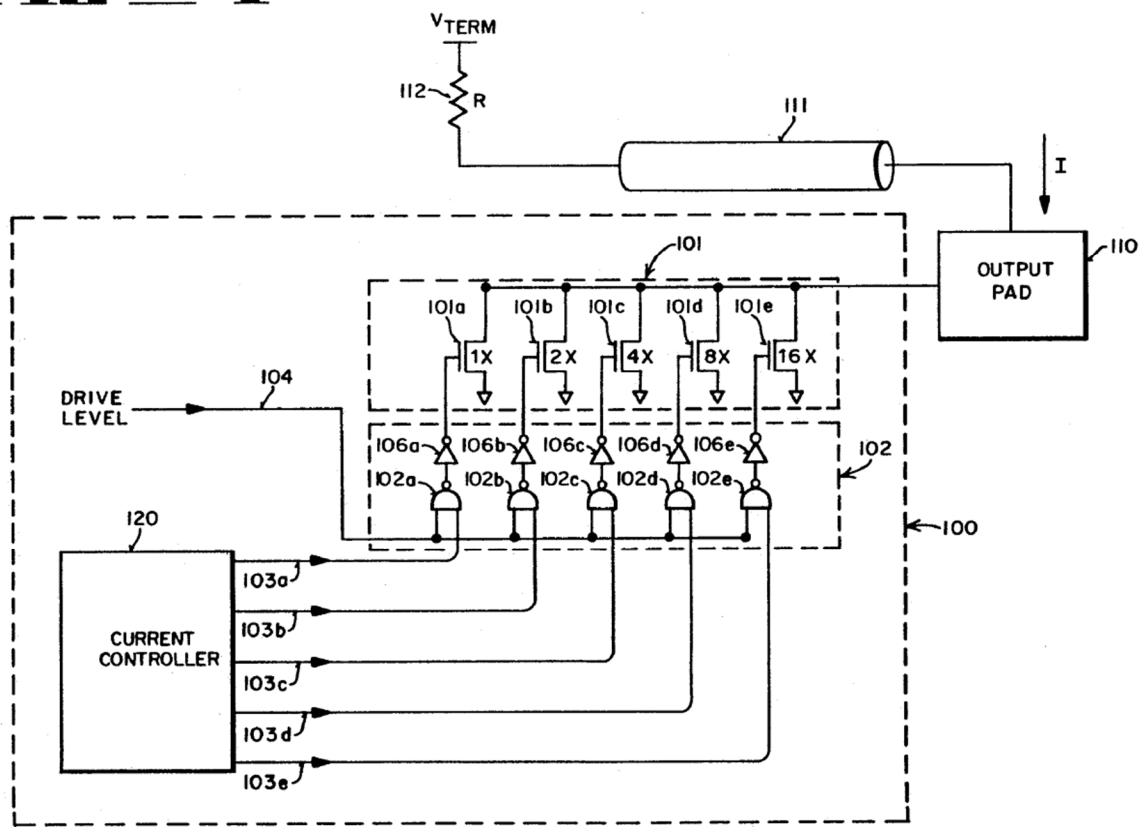


FIG. 3

EX1006 at FIG. 3, 5:39-44. As shown to the left above, the voltage swing of the driver output before calibration is unbalanced and the mid-point voltage deviates from the reference voltage V_{REF} because the VOL DRIVER level is further from V_{REF} than the VOH DRIVER level. *Id.* By contrast, as shown to the right, the voltage swing of the driver output after calibration of the drive strength setting is balanced with a mid-point voltage V_{REF} because the VOL DRIVER level and the VOH DRIVER level are symmetric about V_{REF} . *Id.* at FIG. 3, 5:58-65. To achieve the balanced voltage swing of the driver output, Thomann explains that

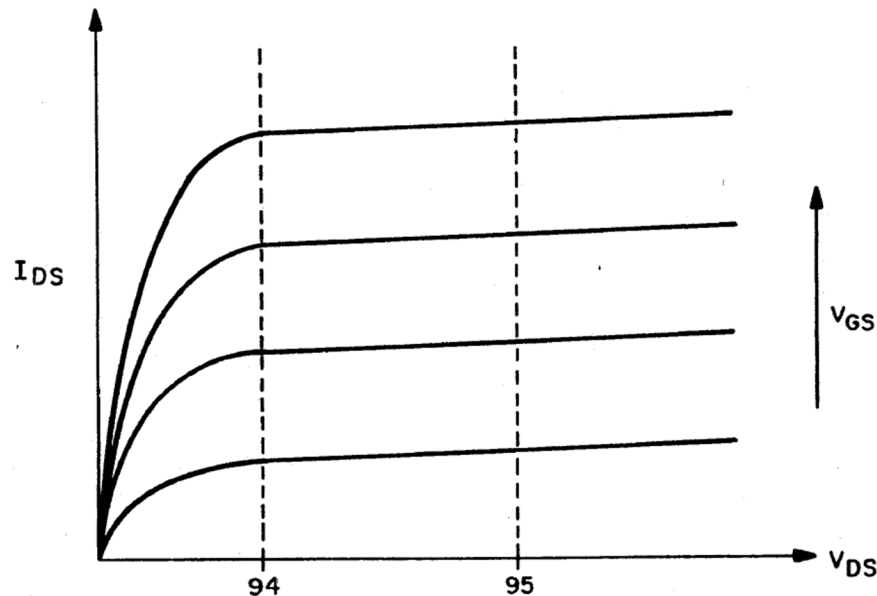
one of the transistors of the driver is first set to a drive strength, such as a minimum drive strength or a maximum drive strength. *Id.* at 6:23-31. Then similar to Lee, the drive strength is incrementally adjusted from the first setting, such as being increased from the minimum setting or decreased from the maximum setting. *Id.* at 6:23-31; *see also id.* at 4:3-5:19. Indeed, it was well-known that setting a minimum drive strength in which the voltage is above a minimum level, such as VOH MIN/VOL MIN as disclosed in Thomann, minimizes the power dissipated during voltage swings. *See* Horowitz (EX1010), at 8:13-32, FIGS. 4-5; EX1006, 6:23-31. For example, Horowitz discloses a driver with an NMOS transistor array, as shown below.

FIG 4



Horowitz (EX1010), at FIG. 4. Figure 5 of Horowitz discloses the relationship of the drain current (I_{DS}) with respect to the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) for an NMOS transistor.

FIG 5



Id. at FIG. 5. Horowitz explains that “[a]s long as the drain-source voltage is kept above a minimum level (for example, shown by line 94 [in Figure 5]), the drain current is consistent and essentially independent of the V_{DS} voltages.” *Id.* at 8:17-21. However, Horowitz recognizes a well-known behavior of transistors—“the larger the voltage level, the higher the power dissipation when the transistor is in the on state.” *Id.* at 8:23-25. Due to this disadvantage, a balance must be struck between the voltage level for operation of the transistor and minimizing power dissipation. *See id.* at 8:25-28. For example, Horowitz defines “a range ... by lines 94 and 96 as shown in FIG. 5 [above that] maintains the V_{DS} above a minimum

level (to allow current to be independent of V_{DS}) while minimizing V_{DS} (to minimize power dissipated during voltage swings).” *Id.* at 8:28-32.

121. Thus, a POSITA would have been motivated to implement Lee’s calibration logic with the teachings of Thomann’s calibration routine to set an initial drive strength and adjust the voltage swing using drive strength adjustments to achieve a balanced driver. This straightforward modification of Lee’s calibration logic in view of Thomann and the knowledge of a POSITA simply uses a known technique (e.g., Thomann’s calibration technique to setting the initial drive strength and performing adjustments) to improve a similar device (e.g., Lee’s output buffer driver with calibration) in the same way (e.g., adjusting the drive strength of the driver to obtain a reduced voltage swing balanced around a midpoint at a reference voltage V_{REF}). Additionally, the modification simply applies a known technique (e.g., Thomann’s calibration by setting an initial drive strength and performing adjustments) to a known device (e.g., Lee’s output buffer driver with calibration) that is ready for improvement to yield predictable results (e.g., a balanced driver with a reduced voltage swing having a midpoint at a reference voltage V_{REF}).

2. Claim 1

a. “An output driver for an integrated circuit, comprising:” [1.P]

122. I understand that the preamble of claim 1 is not necessarily limiting. Nevertheless, to the extent the preamble is limiting, Lee teaches claim limitation

[1.P] as I explained above for Ground 1. *See supra* Section X.A.1.a; Lee (EX1005), at FIG. 1, 3:13-32, 5:45-47, FIGS 4-6, 7:33-35, 1:39-44, 7:57-67.

b. “a driver circuit for driving an input signal of the output driver onto an output line” [1.1]

123. As I explained above for Ground 1, Lee also teaches claim limitation [1.1]. *See supra* Section X.A.1.b; *see also* Lee (EX1005), at FIGS. 1, 4; 3:33-56, FIG. 6, 6:11-53; *see also* Thomann (EX1006), at FIG. 2, 4:35-42, FIG. 5, 6:7-16.

c. “a measuring circuit for measuring at least one of an output line current and an output line potential; and” [1.2]

124. As I explained above for Ground 1, Lee also teaches claim limitation [1.2] to the extent the limitation is supported by the '369 Specification. *See supra* Section X.A.1.c; *see also* Lee (EX1005), at FIGS. 1-3, 5-6, 3:43-46, 5:28-31, 4:46-49, 7:22-26.

d. “a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range,” [1.3]

125. As I explained above for Ground 1, Lee also teaches claim limitation [1.3] to the extent the limitation is supported by the '369 Specification. *See supra* Section X.A.1.d; *see also* Lee (EX1005), at FIGS. 1-3, 5, 1:26-33, 1:61-63, 2:39-44, 3:6-24, 3:33-41, 3:47-53, 3:56-58, 4:6-61, 4:62-5:27, 10:6-12.

126. Further, in the combination of Lee and Thomann, Lee's comparator, delay, and calibration logic (“*a control unit*”), as modified by Thomann's teachings

of its calibration routine, provides a control signal for driver strength settings to provide the output line potential “*in a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*” As explained for claim limitation [1.3] in Ground 1, a POSITA would have understood that power is equivalent to potential or voltage multiplied by current. *See supra* Section X.A.1.d (discussing Ohm’s law and the relationship between power, voltage, current, and resistance).

127. Thomann specifies “*a specification-prescribed potential range*” for each of the VOH DRIVER output voltage level and the VOL DRIVER output level. As prescribed in the figure below from Thomann, the VOH DRIVER output voltage level is between VOH MAX and VOH MIN and the VOL DRIVER output voltage level is between VOL MAX and VOL MIN.

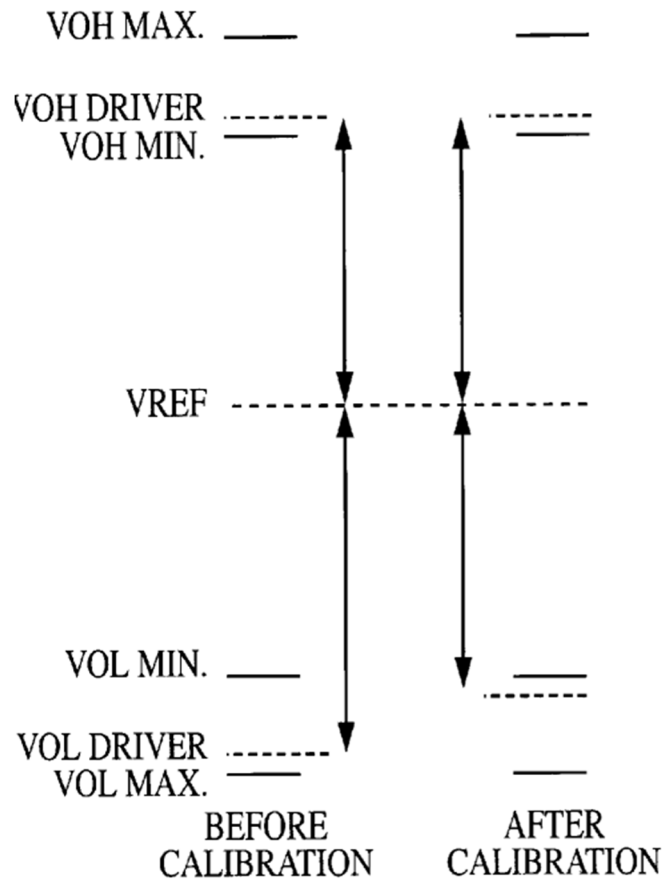


FIG. 3

Thomann (EX1006), at FIG. 3, 5:62-65, 6:23-26. Thomann explains that it desires for “the VOH and VOL levels to be symmetric about a midpoint voltage,” VREF. EX1006 at 3:33-36. Accordingly, a POSITA would have understood that the corresponding desired power range in Thomann corresponds to calibrated VOH and VOL levels symmetric about VREF and within the voltage ranges between VOH MAX and VOH MIN and between VOL MAX and VOL MIN.

128. Thomann also teaches and discloses “*a specification-prescribed current range.*” Like Lee, Thomann explains that specifications for output drivers

prescribe current versus voltage curves with minimum and maximum limits. Lee (EX1005), at 1:29-33; Thomann (EX1006), at 1:29-33; *see, e.g.*, JESD79 (EX1007), at 59-60 (illustrating examples of curves and providing data points). A POSITA would have understood that each of the VOH and VOL ranges, individually and collectively, have corresponding current ranges (between minimum and maximum current limits) that are individually and collectively “*a specification-prescribed current range.*” For example, for a VDDQ to ground voltage of 2.5 volts, the pull-up current would range between 50.2 and 137.3 milliamps and the pull-down current would range between -41.0 and -187.6 milliamps, according to JESD79 (see table reproduced above). JESD79 (EX1007), at 59-60. The pull-up and pull-down currents are individually a current range, and collectively, the current range is between -41.0 and -187.6 milliamps (for the pullup current) and between 50.2 and 137.3 milliamps (for the pulldown current). *See id.*

129. Further, a POSITA would have understood that Thomann desires the power range to be the product of the prescribed voltage and current ranges and thus Thomann teaches the drive strength adjustment “*to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*” As explained for claim limitation [1.3] in Ground 1, a POSITA would have

understood that power is equivalent to potential or voltage multiplied by current. *See supra* Section X.A.1.d (discussing Ohm’s law and the relationship between power, voltage, current, and resistance). In the combination of Lee and Thomann, the “desired power range” corresponds to the product of the voltage range(s), between VOL MAX and VOL MIN and between VOH MAX and VOH MIN, and the current range(s), corresponding minimum and maximum currents for each of the four voltages (VOL MAX, VOL MIN, VOH MAX, and VOH MIN).

e. “wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.” [1.4]

130. As I explained above for Ground 1, Lee also teaches claim limitation [1.4] to the extent the limitation is supported by the ’369 Specification. *See supra* Section X.A.1.e; *see also* Lee (EX1005), at FIGS. 1-3, 5-6, 4:36-61, 5:39-41, 5:46-58, 7:26-32.

3. Claim 2: “The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude.”

131. Claim 2 is obvious over Lee and Thomann. In the combination, Lee is modified by Thomann’s teachings of its calibration routine and the combination teaches “*the desired power range is determined by . . . a specification-prescribed*

lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude.” See supra Section X.B.1

(Combination of Lee and Thomann). As I explained above, a POSITA would have understood that the desired power range corresponds to a desired potential range because power is equivalent to potential multiplied by current. *See supra* Sections X.A.1.d, X.B.2.d (claim limitation [1.3]). Thomann specifies a VOH DRIVER output voltage range between VOH MAX and VOH MIN, a VOL DRIVER output voltage range between VOL MAX and VOL MIN, and teaches that the VOH and VOL levels should be symmetric about VREF. *See supra* Section X.B.2.d. As shown by the annotations to Figure 3 of Thomann below, the desired power range is determined by VOH MIN and VOL MIN (in purple), which are individually and collectively, “*a specification-prescribed lower potential limit value*” as they are lower in magnitude from the mid-point voltage VREF than VOH MAX and VOL MAX (in red).

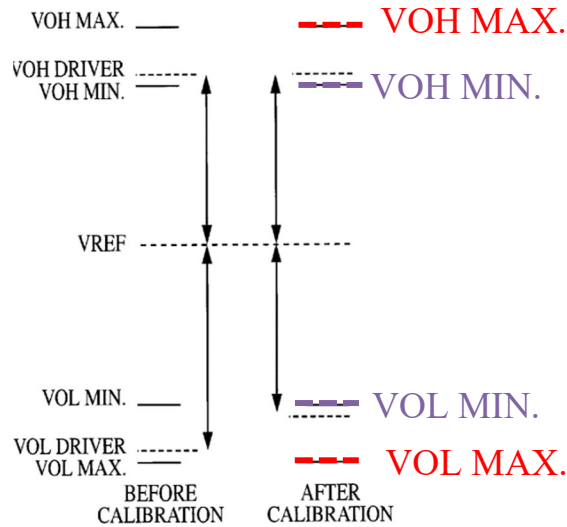


FIG. 3

Thomann (EX1006) at FIG. 3, 3:33-38, 6:23-31.

132. The combination of Lee and Thomann also teach “a *specification-prescribed lower potential limit value adjusted with the tolerance magnitude*.” The ’369 Patent does not define a particular amount of the “*tolerance magnitude*” or specify whether the “*tolerance magnitude*” must be a fixed value or whether the adjustment with the “*tolerance magnitude*” is limited to, for example, adding the tolerance magnitude to the specification-prescribed lower potential limit value. See ’369 Patent (EX1001), at 6:38-42.

133. To the extent the claim limitation is sufficiently described by the ’369 Specification, Lee and Thomann also teach that the desired power range is also determined by VOH DRIVER and VOL DRIVER, which are individually and collectively, “a *specification-prescribed lower potential limit value adjusted with*

the tolerance magnitude” as VOH DRIVER is equivalent to VOH MIN (“a specification-prescribed lower potential limit value”) increased by a tolerance magnitude (in blue) and VOL DRIVER is equivalent to VOL MIN (“a specification-prescribed lower potential limit value”) decreased by the same tolerance magnitude (in blue), as shown by the annotations to Figure 3 of Thomann below.

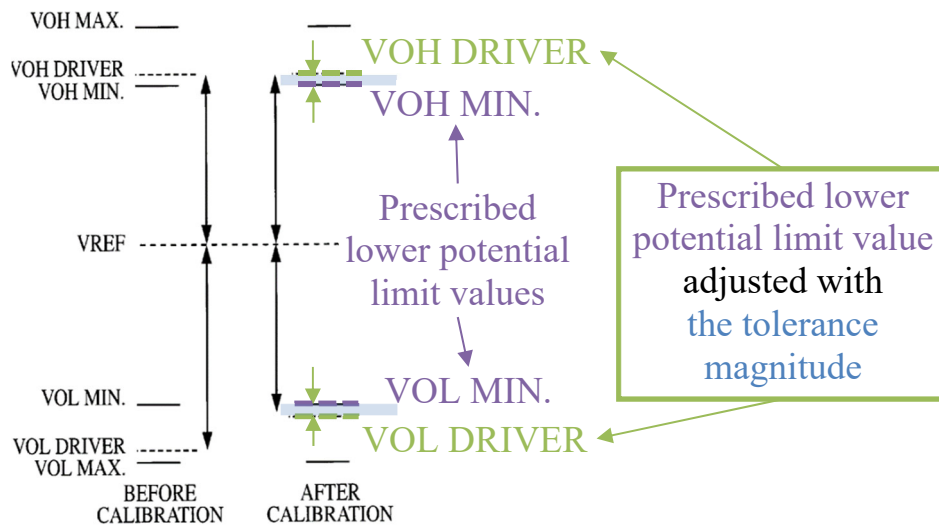


FIG. 3

Thomann (EX1006), at FIG. 3. Thomann discloses that the VOH and VOL levels of the driver should be symmetric about V_{REF} . *Id.* at 3:33-38, 6:23-31. A POSITA would have understood that the corresponding voltage range values, including the minimum values ($VOH\ MIN.$ and $VOL\ MIN.$) and maximum values ($VOH\ MAX.$ and $VOL\ MAX.$), are symmetric about V_{REF} as well. *See id.* Accordingly, a POSITA would have also understood that the tolerance magnitude between VOH

DRIVER AND VOH MIN. and between VOL DRIVER and VOL MIN. are the same magnitude. *See id.* at 5:58-65, FIG. 3.

134. Although Thomann teaches that calibration adjusts the drive strengths of the pull-up or pull-down transistors, Thomann also teaches that, in a preferred embodiment, the drive strength of only one of the pull-up/pull-down transistors is adjusted. *See id.* at 6:18-23. For example, as shown below in Figure 3, the VOL DRIVER can be calibrated by setting the pull-down transistors to a “minimum strength value ... which can be adjusted up incrementally until it achieves a balanced driver with the pull-up transistor[s].” *Id.*, 6:23-26.

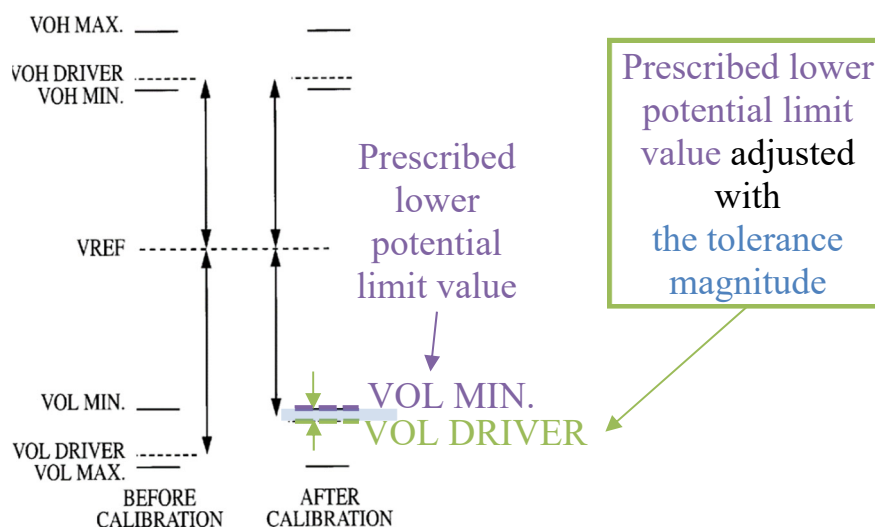


FIG. 3

Id. at FIG. 3.

135. Thomann also explains that the VOH DRIVER can be calibrated by setting the pull-down transistors to a “maximum drive strength” and then

“adjust[ing] the strength down until there is a balanced drive of the pull down transistor with the pull up transistor.” *Id.*, 6:26-31. This is shown below by the annotations to Figure 3 of Thomann.

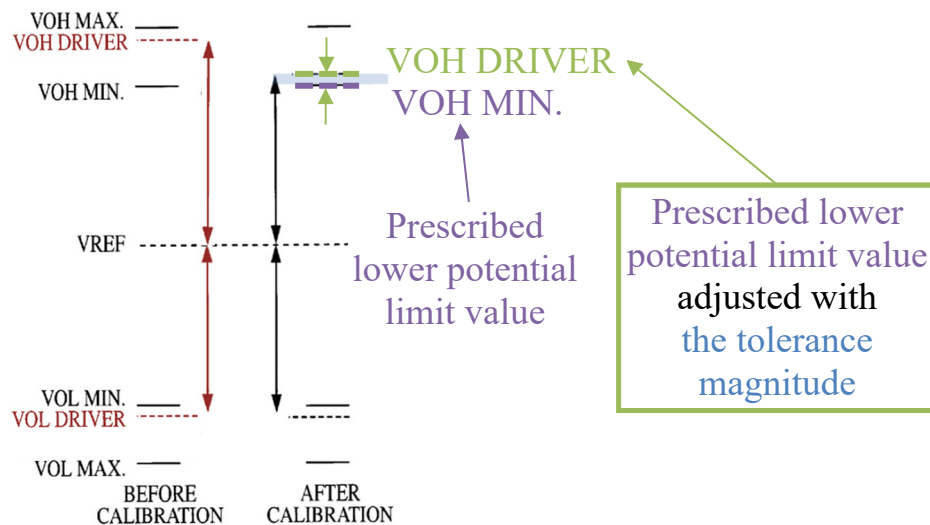


FIG. 3

Id. at FIG. 3; *see also id.*, 5:64-6:6, 6:26-31. Before calibration, VOH DRIVER is further from the mid-point voltage (VREF) than VOL DRIVER, as shown by the annotations in red. *See id.* And after calibration, VOH DRIVER is reduced to just above VOH MIN, adjusted with a tolerance magnitude (annotated in blue in the figure above), to achieve a balanced drive about the mid-point voltage (VREF). *See id.*

136. Thus, Thomann teaches that, in the combination, the output potential after calibration is in the desired power range determined by the current-voltage curves of the output driver transistors and the potential ranges for VOH and VOL,

which include VOH MIN and VOL MIN (“a *specification-prescribed lower potential limit value*”) and the output driver voltages VOH DRIVER and VOL DRIVER (“a *specification-prescribed lower potential limit value adjusted with the tolerance magnitude*”).

4. Claim 5: “The output driver of claim 1, wherein the driver circuit further comprises a setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit.”

137. Claim 5 depends from claim 1, whose limitations are discussed above in this ground. *See supra* Section X.B.2. Further, for the reasons explained above for Ground 1, Lee teaches the additional limitations of claim 5. *See supra* Section X.A.3; *see also* Lee (EX1005), at FIG. 2, 4:58-61, FIGS. 4-5, 5:42-67, FIG. 6, 6:54-63.

5. Claim 6 (“The output driver of claim 1, wherein the control unit further comprises a comparator unit for comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value”) and claim 7 (“The output driver of claim 6, wherein the control unit further comprises an evaluation unit connected to the comparator unit, the evaluation unit configured to change the control signal based upon a result from the comparator unit”).

138. Claims 6 and 7 each depends from claim 1, whose limitations are discussed above in this ground. *See supra* Section X.B.2. Further, for the reasons explained above for Ground 1, Lee teaches the additional limitations of claims 6

and 7. *See supra* Section X.A.4; *see also* Lee (EX1005), at FIGS. 1-3, 6, 3:41-46, 3:58-63, 4:17-5:5, 5:29-34, 5:39-58, 7:22-32.

C. Claims 1-7 and 14-16 are obvious over Lee and JESD79

139. In my opinion, Lee in combination JESD79 renders obvious claims 1-7 and 14-16 of the '369 Patent.

1. Combination of Lee and JESD79

140. Ground 3 combines Lee with JESD79. As explained below, JESD79 is a memory specification that discloses prescribed potential and current ranges for pulldown and pullup paths of an output driver.

141. As I explain below, a POSITA would have been motivated to combine Lee with JESD79 and had a reasonable expectation of success in doing so. Both Lee and JESD79 relate to drive strengths of pull-up and pull-down devices for an output driver. For example, Lee is entitled “Simple Output Buffer Driver Strength Calibration” and discloses an “output buffer driver calibration circuit and method” in which the output buffer driver has “[p]ull-up and pull-down devices.” Lee (EX1005) at 1. And, JESD79 is a memory specification that specifies data driver output pulldown and pullup characteristic curves and data points. JESD79 (EX1007) at 59-60. In addition, Lee discloses an output buffer driver with drive strength adjustment. Lee (EX1005), at FIG. 1, 3:13-32, 4:31-61; *see supra* Section IX.A (Overview of Lee (EX1005)). Lee expressly contemplates using its driver in

memory circuits, including Dynamic Random Access Memory (DRAM), specifically. Lee (EX1005), at 2:11-20, 7:38-47. Consistent with Lee contemplating use of its driver in memory circuits, JESD79 is a memory specification for DRAM, specifically Double Data Rate (DDR) Synchronous DRAM (SDRAM). JESD79 (EX1007), at 1, 4-5; *see supra* Section IX.C (Overview of JESD79 (EX1007)).

142. Lee recognizes that output drivers have specified current versus voltage (I-V) curves with minimum and maximum limits and that the output buffer currents are well matched when the mid-voltage is at VREF (*see* EX1005 at 1:30-34), but it does not disclose examples of the I-V curves or specific currents for a well-matched driver. However, JESD79 does provide these details, providing I-V curves for the output driver, including minimum, maximum, typical low, and typical high curves for the pull-up and pull-down transistor(s) of the output driver. JESD79 (EX1007), at 59-60. JESD79 also discloses a weak drive-strength setting for lighter loads and/or point-to-point environments. JESD79 (EX1007), at 16.

143. In the figure shown below, JESD79 shows that for a normal drive strength the range of the pulldown I-V curve spans between maximum and minimum curves and it is recommended the range of the typical high and typical low curves fall within the lower portion between the maximum and minimum curves.

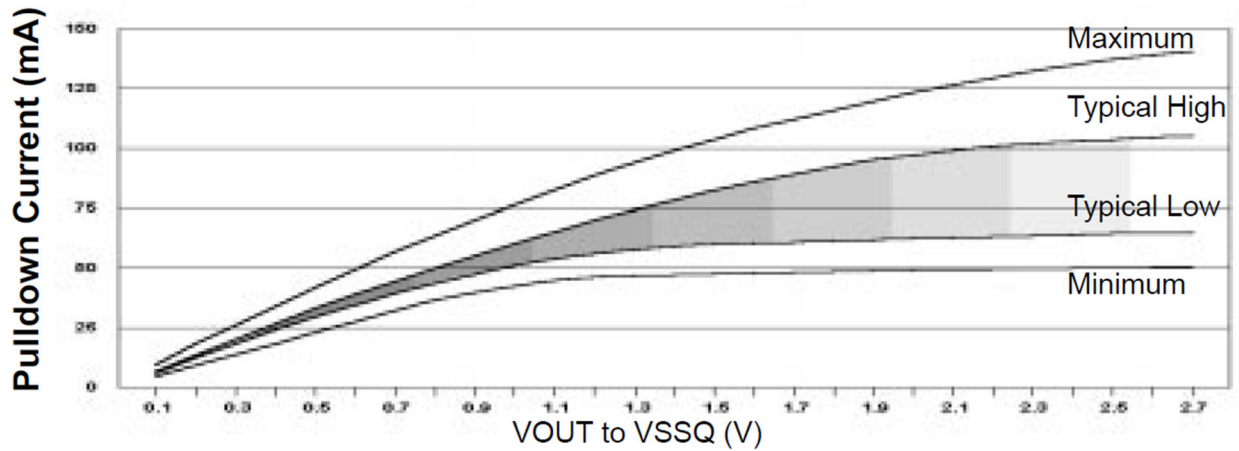


Figure a: Pulldown Characteristics

JESD79 (EX1007), at 59-60. For example, at a voltage of 2.5 volts, the current ranges between a minimum of 50.2 milliamps and a maximum of 137.3 milliamps, within which the desired typical current ranges between 64.6 and 103.8 milliamps.

Id.

144. Similarly, the range of the pullup I-V curve spans between maximum and minimum curves and is recommended to be in the range of the typical high and typical low curves.

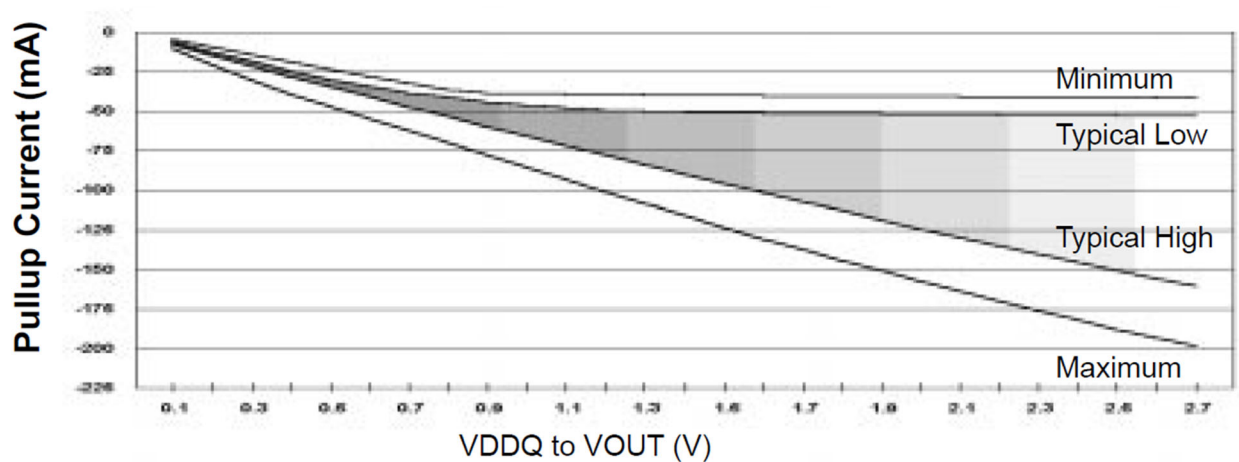


Figure b: Pull Up Characteristics

JESD79 (EX1007), at 59-60. For example, at a voltage of 2.5 volts, the current ranges from a minimum magnitude of 41.0 milliamps and a maximum magnitude of 187.6 milliamps, within which the desired typical current ranges between a magnitude of 52.5 and 150.5 milliamps. *Id.* JESD79 also teaches there are similar I-V curves for the weak drive strength setting, which represents a strength setting for lighter loads and/or point-to-point environments. *Id.* at 16.

145. The curves specified by JESD79 also disclose an output voltage of the driver relative to VDDQ, a power supply potential for a DQ memory pin, and VSSQ, a ground potential for a DQ memory pin. *Id.* at 11, 58. In the combination, a POSITA would have understood that VDDQ is a power supply for Lee's output driver and VSSQ is a ground potential, as shown in the figure below.

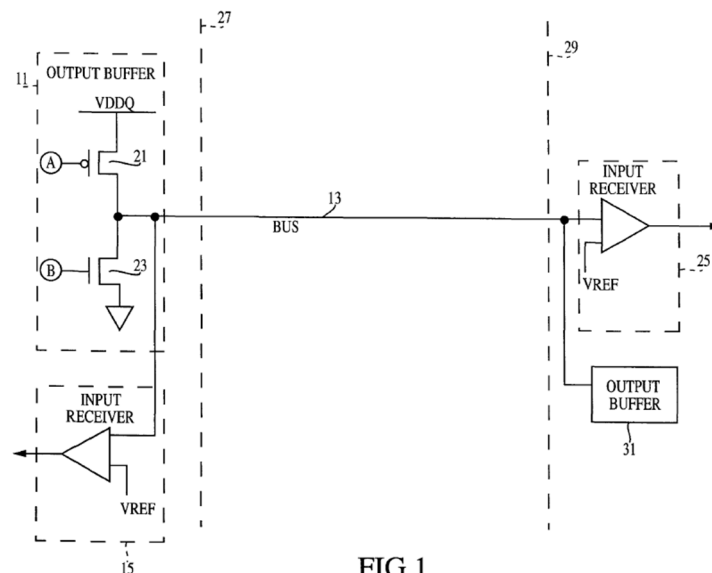


FIG.1

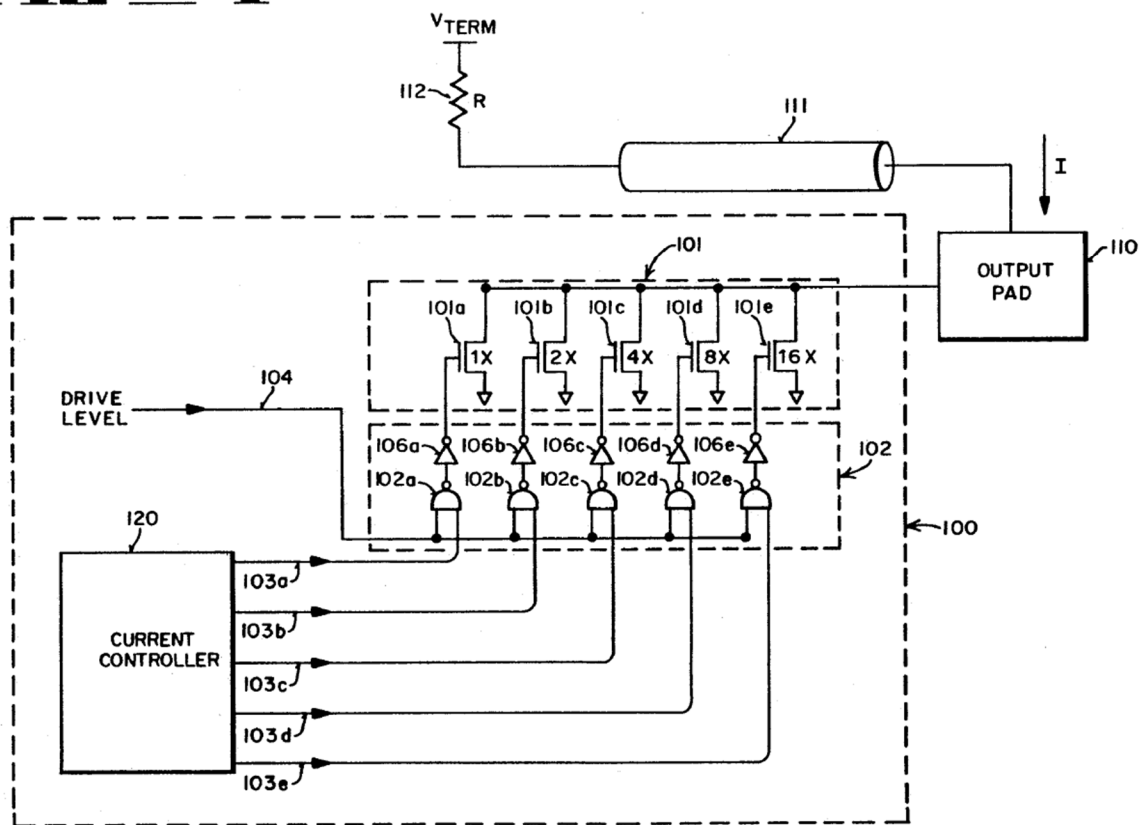
Lee (EX1005), at FIG. 1.

146. Thus, a POSITA would have been motivated to implement Lee's feedback control logic in accordance with the teachings of JESD79 that specify the I-V curves for the pullup and pulldown transistors of Lee's buffer output driver for memory. This straightforward modification of Lee's control logic in view of the voltages and currents prescribed in JESD79 and the knowledge of a POSITA simply uses a known technique (e.g., setting the drive strength consistent with the I-V curves in JESD79) to improve a similar device (e.g., Lee's output buffer driver with feedback control logic) in the same way (e.g., setting the feedback control logic to adjust the drive strength consistent with the I-V curves in JESD79). Additionally, the modification simply applies a known technique (e.g., setting the drive strength consistent with the I-V curves in JESD79) to a known device (e.g., an output buffer driver with calibration) that is ready for improvement to yield predictable results (e.g., a driver with drive strength settings such that the driver operates in a desired lower, typical range for the specified I-V curves). *Id.* Indeed, Lee contemplates that his active calibration scheme can further improve upon fixed driver strengths settings based on specified curves, "by adjusting out the effects of process variance, voltage variation or temperature variation on output buffer drivers." Lee (EX1005), at 1:34-38.

147. Further, it was well-known that a driver can be adjusted by, for example, adjusting the number of transistors enabled or disabled or adjusting the

effective width of the transistors, to operate above a minimum voltage level, which minimizes power dissipation during voltage swings while allowing the current through the transistors of the driver to be largely independent of voltage. For example, Horowitz discloses a driver with an NMOS transistor array, as shown below.

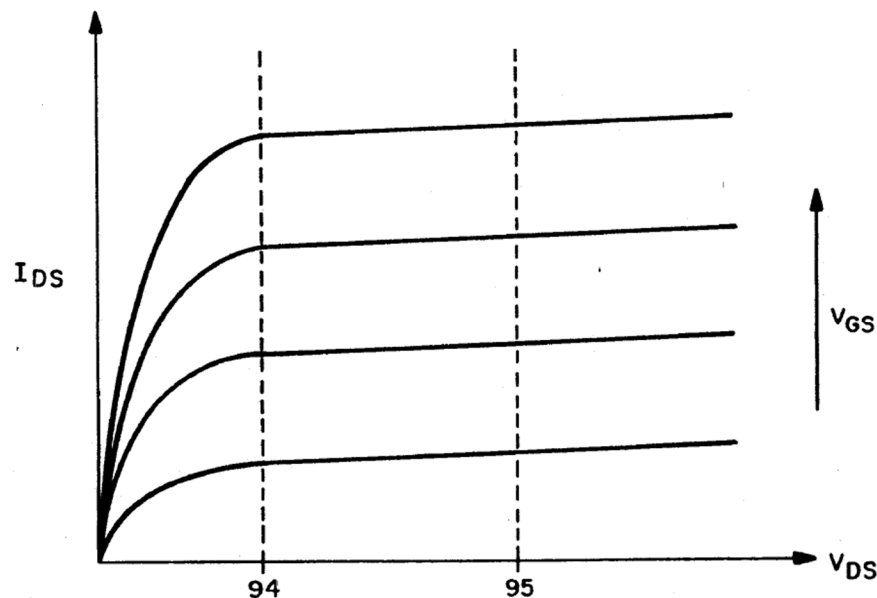
FIG 4



Horowitz (EX1010), at FIG. 4, 7:28-8:32. Horowitz discloses that transistors in the driver are enabled or disabled to adjust the drive strength. *See id.* Figure 5 of Horowitz discloses the relationship of the drain current (I_{DS}) with respect to the

drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) for an NMOS transistor.

FIG 5



Id. at FIG. 5. Horowitz explains that “[a]s long as the drain-source voltage is kept above a minimum level (for example, shown by line 94 [in Figure 5]), the drain current is consistent and essentially independent of the VDS voltages.” *Id.* at 8:17-21. However, Horowitz recognizes a well-known behavior of transistors—“the larger the voltage level, the higher the power dissipation when the transistor is in the on state.” *Id.* at 8:23-25. Due to this disadvantage, a balance must be struck between the voltage level for operation of the transistor and minimizing power dissipation. *See id.* at 8:25-28. For example, Horowitz defines “a range ... by lines

94 and 96 as shown in FIG. 5 [above that] maintains the V_{DS} above a minimum level (to allow current to be independent of V_{DS}) while minimizing V_{DS} (to minimize power dissipated during voltage swings).” *Id.* at 8:28-32. Accordingly, a POSITA would have recognized from Horowitz that the drive strength is adjusted to match the current-versus-voltage curve such that the voltage across the path of the driver (V_{DS}) is maintained at a minimum level that allows current to be largely independent of V_{DS} while minimizing V_{DS} to minimize power dissipated during voltage swings. *See id.* at FIGS. 4-5, 7:28-8:32.

148. Moreover, a POSITA would have been motivated to implement Lee in accordance with well-known memory standards like JESD79. Using such standards ensures interoperability between memory circuitry, proper operation of a memory device, and compliance between the components in memory systems, such as between a processor and the memory devices. *See, e.g.*, Lee (EX1005), at FIG. 7. Accordingly, a POSITA implementing Lee’s teachings for memory, as Lee contemplates, would have looked to JESD79, a well-known memory standard to ensure interoperability, proper operation, and compliance between components in the system. *Id.*

2. Claim 1

a. “An output driver for an integrated circuit, comprising:” [1.P]

149. I understand that the preamble of claim 1 is not necessarily limiting. Nevertheless, to the extent the preamble is limiting, Lee teaches claim limitation [1.P] as I explained above for Ground 1. *See supra* Section X.A.1.a; Lee (EX1005), at FIG. 1, 3:13-32, 5:45-47, FIGS 4-6, 7:33-35, 1:39-44, 7:57-67.

b. “a driver circuit for driving an input signal of the output driver onto an output line” [1.1]

150. As I explained above for Ground 1, Lee also teaches claim limitation [1.1]. *See supra* Section X.A.1.b; *see also* Lee (EX1005), at FIGS. 1, 4; 3:33-56, FIG. 6, 6:11-53. In addition, JESD79 discloses input voltage levels, output currents, and data driver output characteristic curves and data points. *See* JESD79 (EX1007), at 58-60. *See also* JESD79 (EX1007) at 16 (disclosing output drive strength options).

c. “a measuring circuit for measuring at least one of an output line current and an output line potential; and” [1.2]

151. As I explained above for Ground 1, Lee also teaches claim limitation [1.2] to the extent the limitation is supported by the '369 Specification. *See supra* Section X.A.1.c; *see also* Lee (EX1005), at FIGS. 1-3, 5-6, 3:43-46, 5:28-31, 4:46-49, 7:22-26.

d. “a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one

of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range,” [1.3]

152. As I explained above for Ground 1, Lee also teaches claim limitation [1.3] to the extent the limitation is supported by the '369 Specification. *See supra* Section X.A.1.d; *see also* Lee (EX1005), at FIGS. 1-3, 5, 1:26-33, 1:61-63, 2:39-44, 3:6-24, 3:33-41, 3:47-53, 3:56-58, 4:6-61, 4:62-5:27, 10:6-12. In addition, JESD79 discloses output drive strength options including a normal drive strength option and a weak drive strength option. *See* JESD79 (EX1007), at 16.

153. To the extent claim limitation [1.3] requires a prescribed potential range and prescribed current range that is in a memory standard specification, JESD79 discloses “*a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*” In the combination, Lee’s calibration logic (including “a control unit”), as modified by JESD79’s teachings of setting a drive strength consistent with the desired, lower typical I-V curves, provides a control signal for driver strength settings to provide the output line potential “*in a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*”

154. JESD79 specifies “*a specification-prescribed current range*” between the “Maximum” and “Minimum” current to voltage (I-V) curves. As annotated in red in the figures below, the current spans across a range prescribed by JESD79.

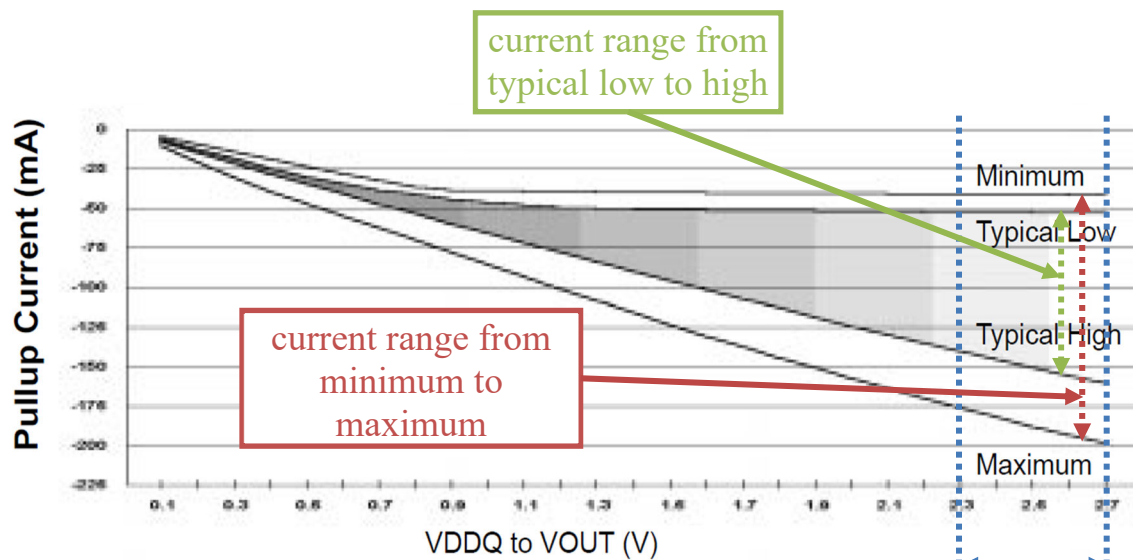


Figure b: Pull Up Characteristics

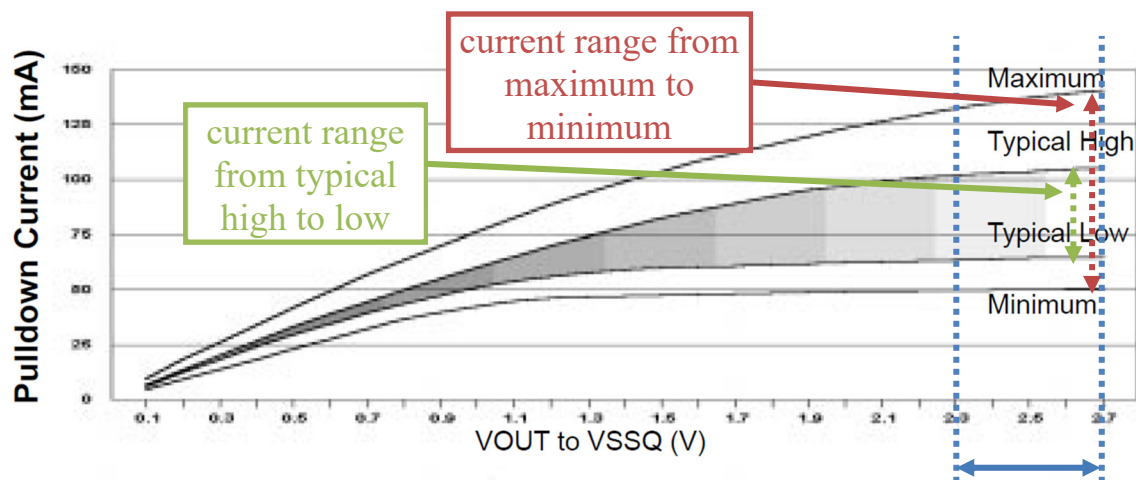


Figure a: Pulldown Characteristics

JESD79 (EX1007), at 59-60. For example, at a voltage of 2.5 volts, the pull-up current ranges from a minimum magnitude of 41.0 milliamps and a maximum magnitude of 187.6 milliamps and the pull-down current ranges from a minimum of 50.2 milliamps and a maximum of 137.3 milliamps. *Id.*

155. Further, the I-V curves in JESD79 also specify “a specification-prescribed potential range” between a minimum input/output (I/O) supply voltage, VDDQ, of 2.3 volts and a maximum I/O supply voltage of 2.7 volts, as annotated in blue in the figures above and in the table below. *Id.* at 11, 58. A POSITA would have understood that the driver output in the combination would swing during normal operation between the prescribed range for VDDQ and a ground potential (e.g., VSSQ). *Id.* Indeed, Lee discloses an output buffer driver (11 or 11’) in which the pull-up path is coupled to a supply voltage, such as VDDQ, and the pull-down path is coupled to a ground supply. *See* Lee (EX1005), at FIGS. 1, 4, 6.

156. A POSITA would also have understood that, during calibration, the driver output in the combination would vary between 49 percent and 51 percent of VDDQ, as specified by JESD79 for the I/O reference voltage VREF:

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6

EX1007 at 58; *see also* EX1005 at FIG. 1. As Lee explains, the calibration circuitry has an accuracy within which the drive strengths of the pull-up and pull-down transistors are matched. *See* EX1005, 5:8-11, 5:29-32. A POSITA would have understood that the accuracy of Lee’s calibration circuitry includes the

accuracy of the reference voltage V_{REF} , as specified by JESD79. *See* EX1007 at 58.

157. Further, a POSITA would have understood that the specified current range(s) and potential range(s) by the JESD79 collectively specify a “*desired power range*” because power is equivalent to current multiplied voltage. *See supra* Section X.A.1.d (discussing Ohm’s law and the relationship between power, voltage, current, and resistance). As shown in the figures below, JESD79 recommends that the typical curves, “Typical Low” and “Typical High,” lie within the purple shaded region, which is within the region formed by the “Minimum” and “Maximum” curves.

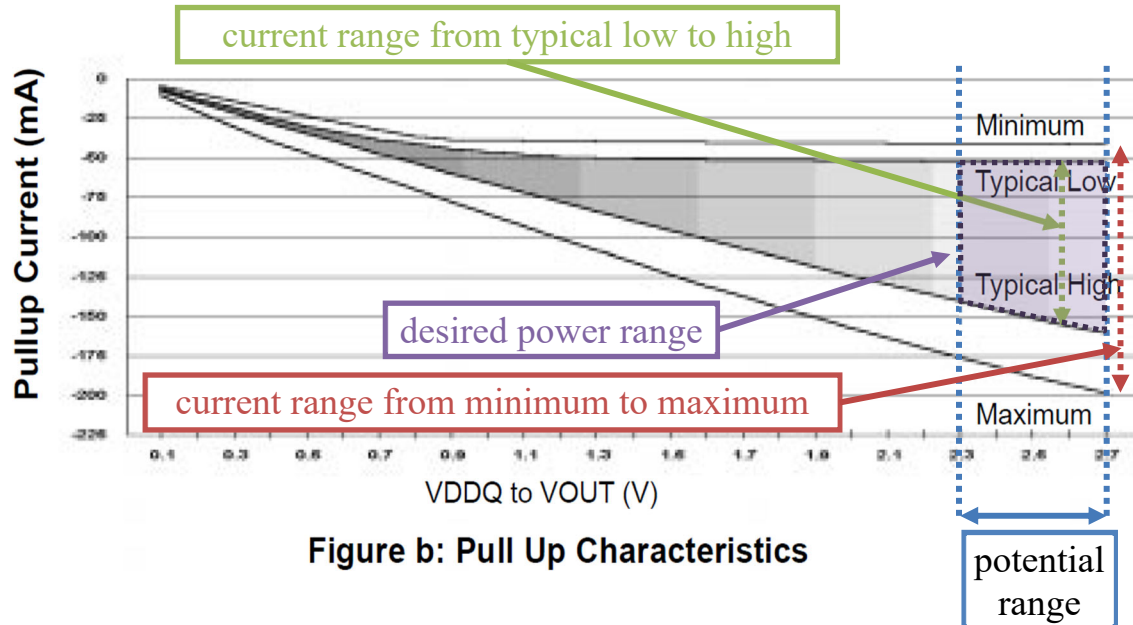
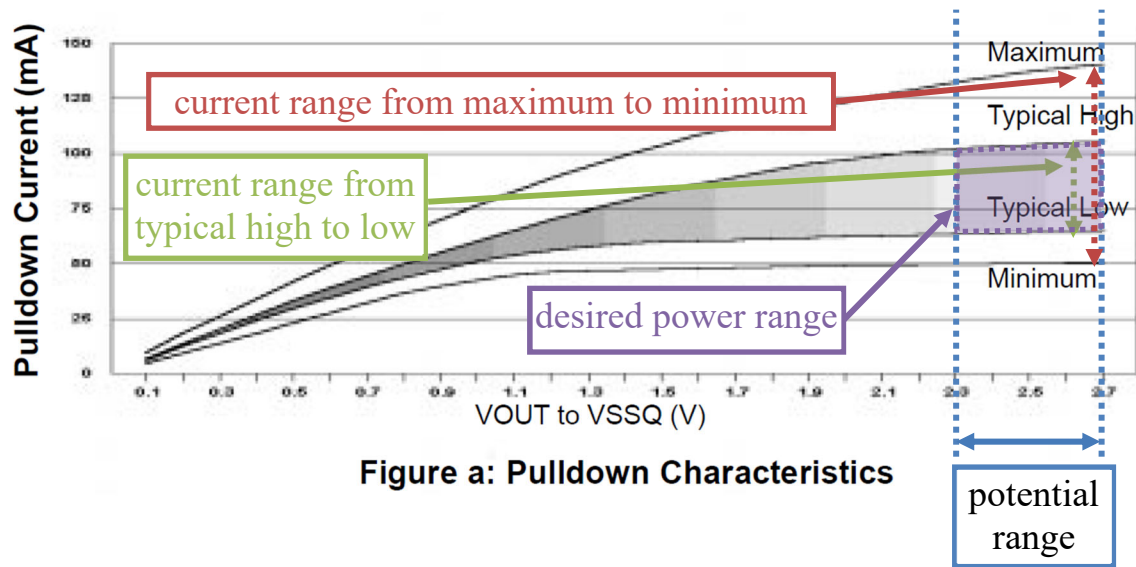


Figure b: Pull Up Characteristics



JESD79 (EX1007), at 59-60. A POSITA would thus have understood that in the combination, the desired power range (annotated in purple above) corresponds to the typical current range and the specified potential range. In particular, the typical current range is shown above in green between the “Typical Low” and “Typical High” curves, which are within the “Minimum” and “Maximum” curves. *Id.* And, the prescribed voltage range is between 2.3 and 2.7 volts, as shown in blue. *Id.* at 58-60.

e. “wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.” [1.4]

158. As I explained above for Ground 1, Lee also teaches claim limitation [1.4] to the extent the limitation is supported by the ’369 Specification. *See supra* Section X.A.1.e; *see also* Lee (EX1005), at FIGS. 1-3, 5-6, 4:36-61, 5:39-41, 5:46-58, 7:26-32.

3. Claim 2: “The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude.”

159. As explained above for Ground 1, Lee teaches claim 2 under Patent Owner’s interpretation. *See supra* Section X.A.2.

160. To the extent claim 2 is narrower than Patent Owner’s interpretation that VREF is “*a specification-prescribed lower potential limit value*,” claim 2 would still have been obvious over Lee and JESD79. In the combination, Lee is modified by JESD79’s teachings regarding prescribed current and voltage range(s) such that “*the desired power range is determined by . . . a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, [and] a specification-prescribed lower potential limit value . . .*.” As explained above, a POSITA would have understood that the desired power range can correspond to a potential range and/or a current range because power is equivalent to potential multiplied by current. *See supra* Sections X.A.1.d (Ground 1 for claim limitation [1.3]), X.B.2.d (Ground 2 for claim limitation [1.3]).

161. JESD79 species a desired potential range, such as a range for voltage VDDQ and a range for voltage VREF, as shown below.

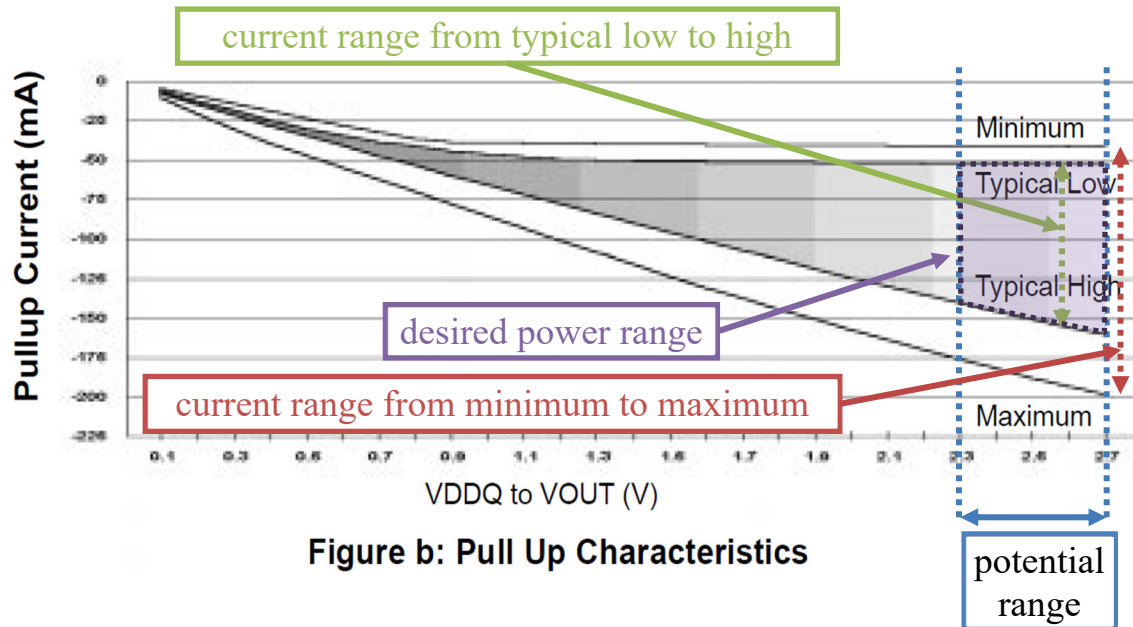
ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{DDQ} = +2.5\text{ V} \pm 0.2\text{ V}$, $V_{dd} = +3.3\text{ V} \pm 0.3\text{ V}$ or $+2.5\text{ V} \pm 0.2\text{ V}$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	$0.49 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	V	6

JESD79 (EX1007), at 58; *see supra* Section X.C.2.d (claim limitation [1.3]); *see also* Lee (EX1005), at FIG. 1. JESD79 prescribes “*lower potential limit value*” of 2.3 volts for VDDQ and 0.49 percent of 2.3 volts or 1.15 volts for VREF. *Id.*

162. JESD79 also specifies a desired current range, such as between the “Typical High” and “Typical Low” I-V curves, which are within the “Maximum” and “Minimum” I-V curves, as shown below.



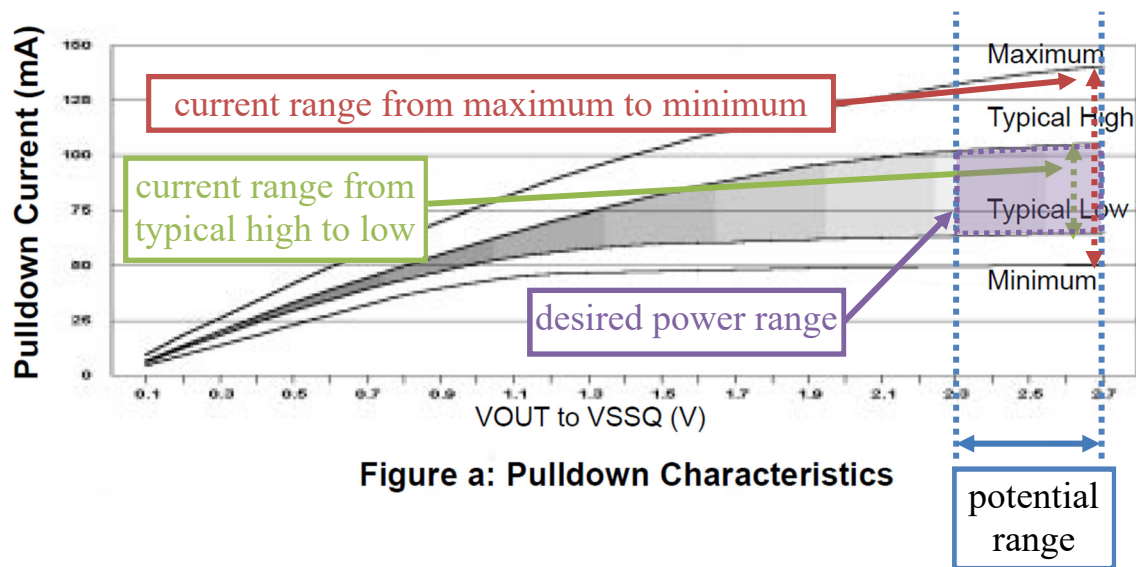


Figure a: Pulldown Characteristics

JESD79 (EX1007), at 58-60; *see supra* Section X.C.2.d (claim limitation [1.3]). As shown by the red annotations in the figures above, the “Minimum” curve at the end of the current range(s) (e.g., corresponding to the potential range in blue) corresponds to the “*specification-prescribed lower current limit value*” as the minimum curve has a lower magnitude than the maximum curve. *Id.* Further, as shown by the green annotations in the figures above, the “Typical Low” curve at the end of the narrower and lower current range(s) (e.g., corresponding to the potential range in blue) corresponds to the “*specification-prescribed lower current limit value adjusted with a tolerance magnitude*” as the typical low curve is adjusted relative to the minimum curve by a tolerance magnitude. *Id.*

163. For example, at 2.3 volts, the pull-down current range is between 49.9 and 132.4 milliamps with a desired typical range between 63.8 and 101.9

milliamps and the magnitude for the pull-up current range is between 40.8 and 176 milliamps with a desired typical range between 52.2 and 139.9 milliamps:

Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

JESD79 (EX1007), at 60. Accordingly, JESD79 prescribes for a voltage of 2.3 volts a “*specification-prescribed lower current limit value*” of -40.8 milliamps for the pull-up current and 49.9 milliamps for the pulldown current (as shown by the lower end of the current range in red in the figures above). *See id.* at 58-60.

JESD79 also prescribes for a voltage of 2.3 volts a “*specification-prescribed lower current limit value adjusted with a tolerance magnitude*” of -52.2 milliamps and 63.8 milliamps (shown by typical low curve in green in the figures above). A POSITA would have recognized that the adjusted tolerance magnitude is calculated by taking the difference between the “Minimum” and “Typical Low” values. For example, the difference between -52.2 milliamps and -40.8 milliamps is 11.4 milliamps, which is the adjusted tolerance magnitude for the pull-up current, and the difference between 63.8 and 49.9 milliamps is 13.8 milliamps for the pull-down current. *See id.* A POSITA would have recognized these values to be a value “*adjusted with a tolerance magnitude.*” *See id.* Further, JESD79 teaches that the ratio of typical pullup to pulldown current should be within a tolerance of 10 percent. JESD79 (EX1007), at 59. Accordingly, a POSITA would have been motivated to adjust the pull-up and pull-down current limits such that they were within a tolerance of 10 percent of each other, in addition to being within the “Typical High” and “Typical Low” curves.

164. Accordingly, in the combination, JESD79 teaches a desired power range determined by “*a specification-prescribed lower current limit value,*” “*a specification-prescribed lower current limit value adjusted with a tolerance magnitude,*” and “*a specification-prescribed lower potential limit value.*”

4. Claim 3: “The output driver of claim 1, wherein the driver circuit includes a pull-up path defined by a first maximum and

minimum current/potential (I/V) characteristic curve and a pull-down path defined by a second maximum and minimum I/V characteristic curve and wherein the desired power range is determined depending on respectively activated pull-up path and pull-down path of the driver circuit.”

165. As I explained above for claim limitation [1.1], Lee discloses a driver circuit with “a pull-up path” (via transistor 21) and “a pull-down path” (via transistor 23).

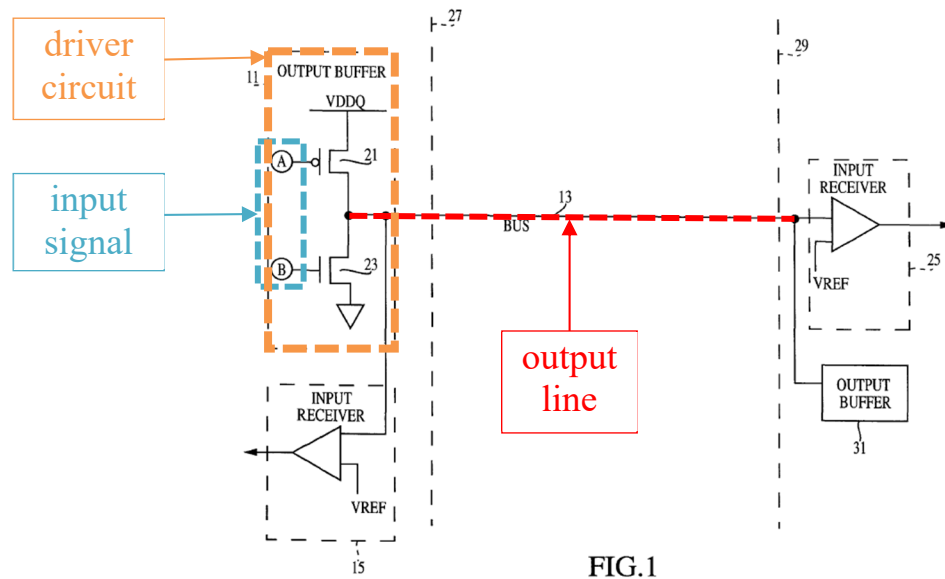


FIG.1

Lee (EX1005), at FIG. 1 (above), FIG. 4; *see supra* Section X.A.1.b. When the input is low, the driver activates the pull-up path to provide current to pull the bus (13) toward VDDQ and when the input is high, the driver activates the pull-down path to provide current to pull the bus toward ground. Lee (EX1005), at 3:33-53, FIG. 1 (above), FIG. 4.

166. As shown in JESD79's figures below, Lee in view of JESD79 teaches that the pull-up and pull-down paths each have a maximum and a minimum characteristic current-potential (I-V) curve.

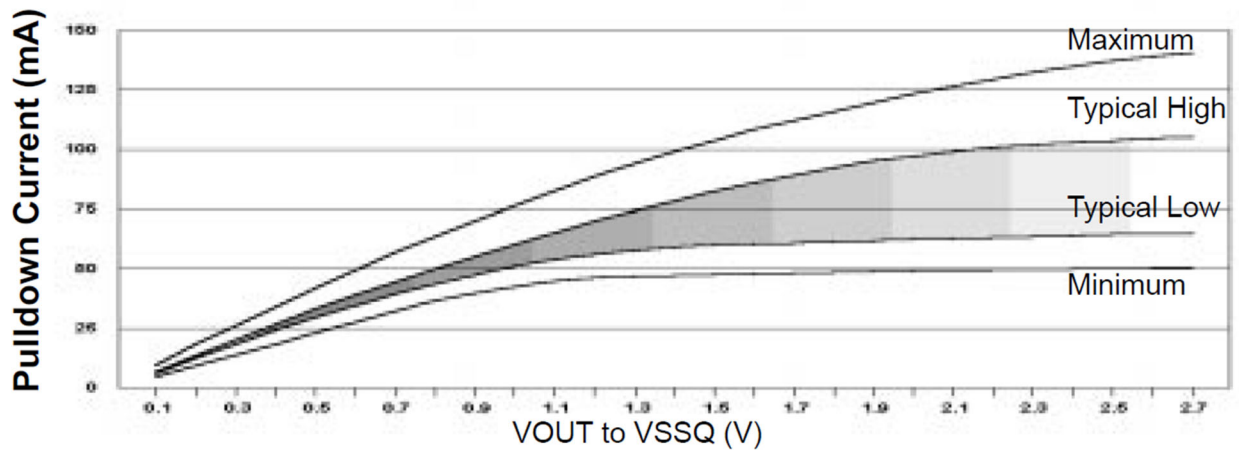


Figure a: Pulldown Characteristics

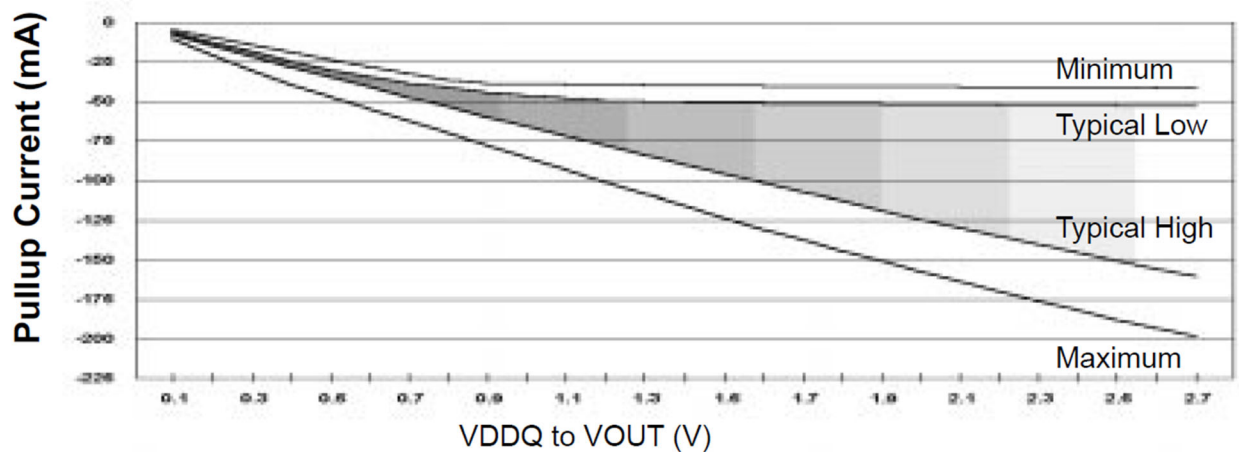
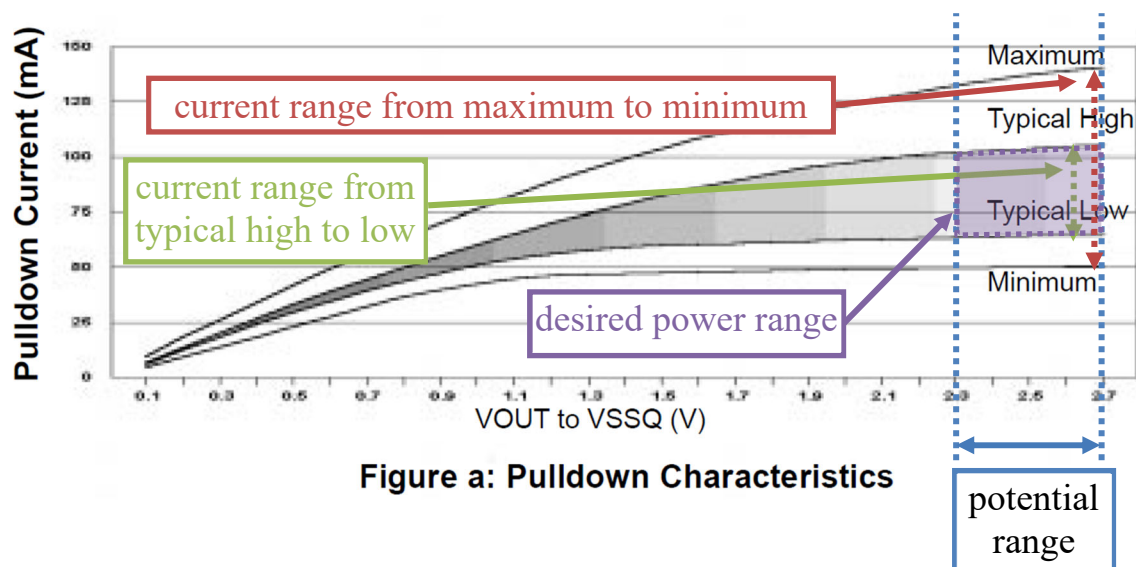
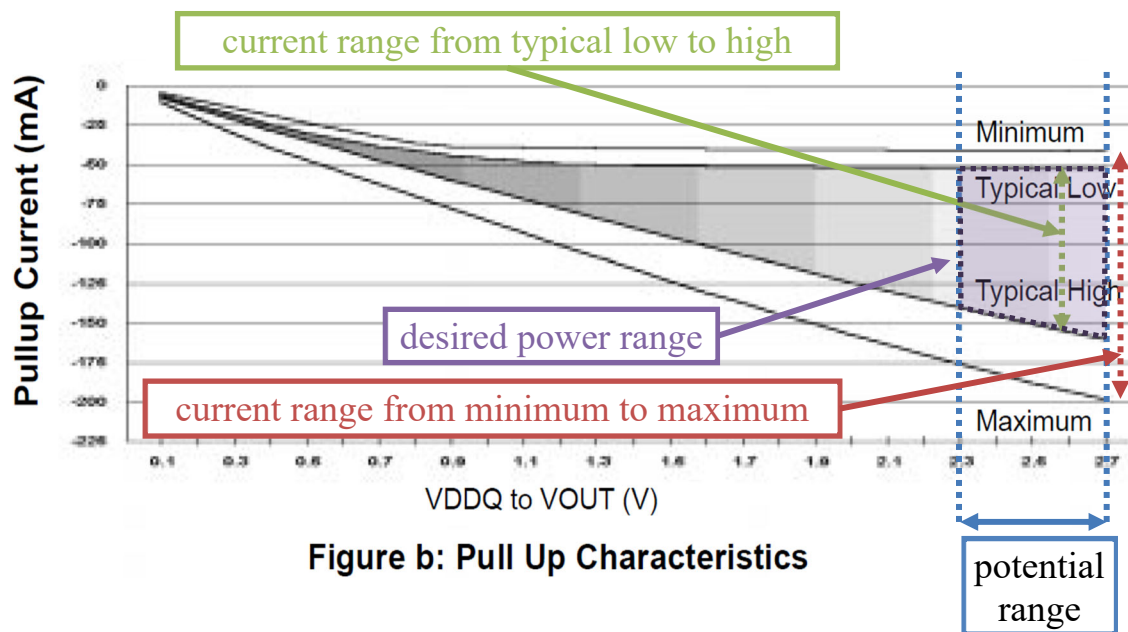


Figure b: Pull Up Characteristics

JESD79 (EX1007), at 59-60.

167. Further, as I explained above for claim limitation [1.3], the “*desired power range*” corresponds to these I/V curves and is determined based on the

activation of the pull-up or pull-down path. *See supra* Section X.C.2.d; *see, e.g.*, JESD79 (EX1007), at 59.



JESD79 (EX1007), at 59-60; *see supra* Section X.C.2.d. Thus, Lee in view of JESD79 teaches claim 3.

5. Claim 4: “The output driver of claim 1, wherein the desired power range corresponds to a lower portion of the specification-

prescribed potential range and a lower portion of the specification-prescribed current range.”

168. Lee in view of JESD79 also teaches claim 4. As shown in the figures below, the combination teaches a “*desired power range*” for the pull-up and pull-down paths.

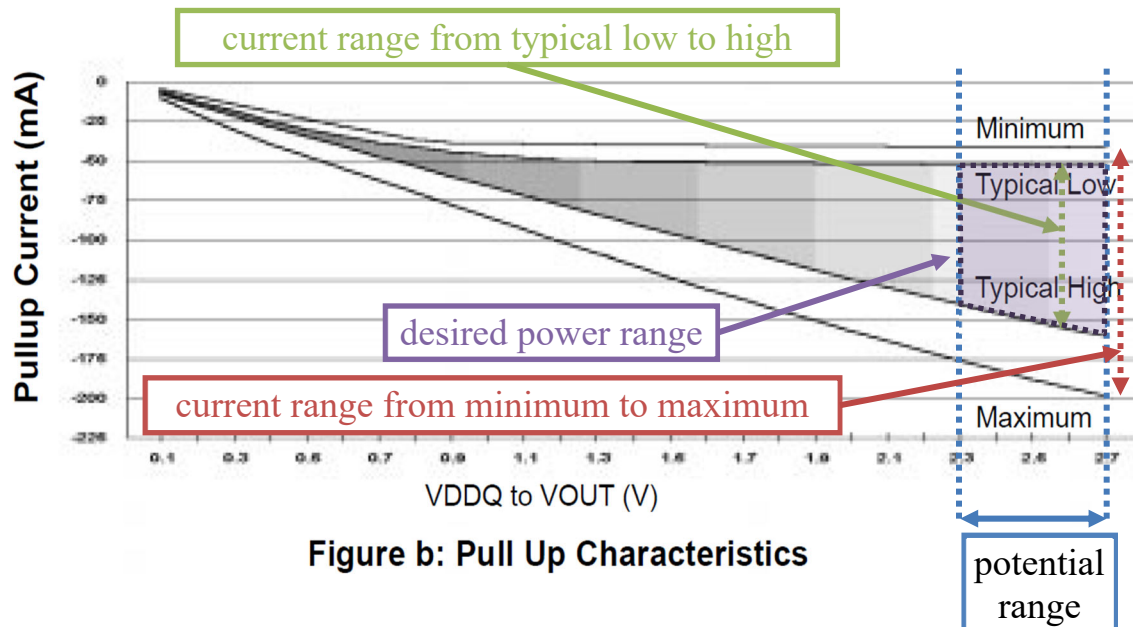


Figure b: Pull Up Characteristics

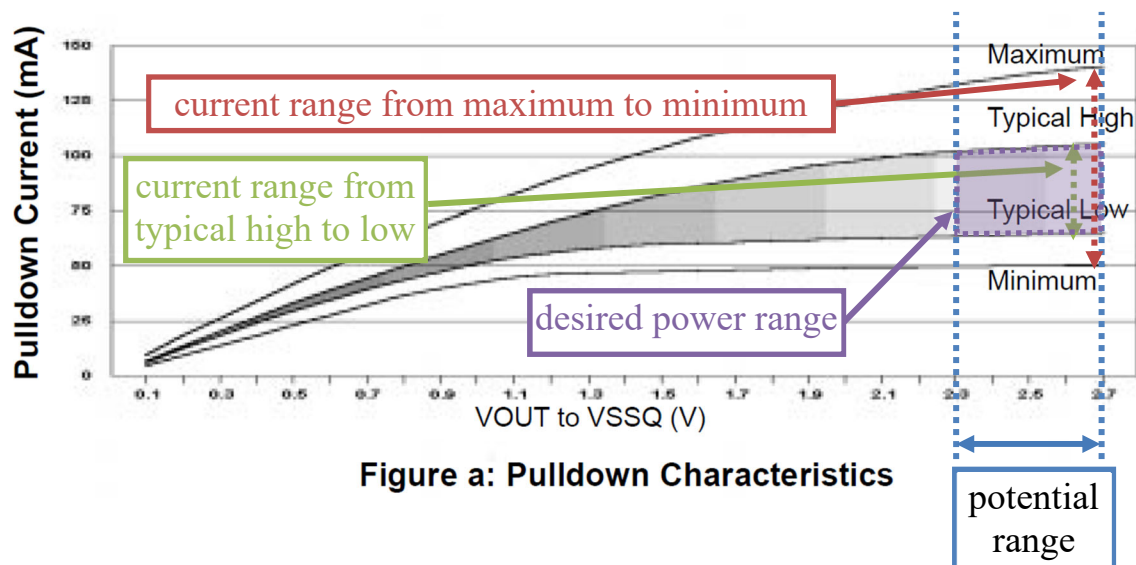


Figure a: Pulldown Characteristics

JESD79 (EX1007), at 59-60; *see supra* Section X.C.2.d. As shown, the desired power range corresponds to a typical current range, which is the vertical range annotated in green, that is between the “Typical High” and “Typical Low” current curves. *Id.* The typical current range is lower than the “Maximum” current curves and is narrower than, and in a lower portion of, the specification-prescribed current range, which is the vertical range annotated in red. *Id.* Accordingly, a POSITA would have understood that the “*desired power range*” corresponds to “*a lower portion of the specification-prescribed current range*” because the typical current range is lower than the maximum curve and because the typical current range (in green above) is narrower and in a lower portion of the specification-prescribed current range (annotated vertical range in red).

169. Further, JESD79 discloses that for a semiconductor process technology with slow NMOS and slow PMOS transistors, the voltage VDDQ is at 2.3V, and for a process technology with typical NMOS and PMOS transistors, the voltage VDDQ is around 2.5 volts. JESD79 (EX1007), at 60. Indeed, a POSITA would have recognized that a range of operation between the voltages for slow and typical semiconductor process technologies would support minimizing the voltage and power of the driver during operation in which the output voltage swings between logical low (e.g., around 0 volts) and logical high (e.g., around VDDQ). *See, e.g.,* Horowitz (EX1010), at 8:13-32, FIG. 5 (defining a range above a

minimum level that minimizes voltage and power); *see also supra* Section X.C.1 (discussing teachings of Horowitz). A POSITA would have understood that the “desired power range” corresponds to “a lower portion of the specification-prescribed potential range” because it corresponds more specifically to a voltage between 2.3 and 2.5 volts, which is lower than the maximum voltage of 2.7 volts for VDDQ and is narrower and in a lower portion of the specification-prescribed range (annotated horizontal range above in blue), between 2.3 and 2.7 volts. JESD79 (EX1007), at 58-60.

6. Claim 5: “The output driver of claim 1, wherein the driver circuit further comprises a setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit.”

170. Claim 5 depends from claim 1, whose limitations are discussed above in this ground. *See supra* Section X.C.2. Further, for the reasons explained above for Ground 1, Lee teaches the additional limitations of claim 5. *See supra* Section X.A.3; *see also* Lee (EX1005), at FIG. 2, 4:58-61, FIGS. 4-5, 5:42-67, FIG. 6, 6:54-63.

7. Claim 6 (“The output driver of claim 1, wherein the control unit further comprises a comparator unit for comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value”) and claim 7 (“The output driver of claim 6, wherein the control unit further comprises an evaluation unit connected to the comparator unit, the evaluation

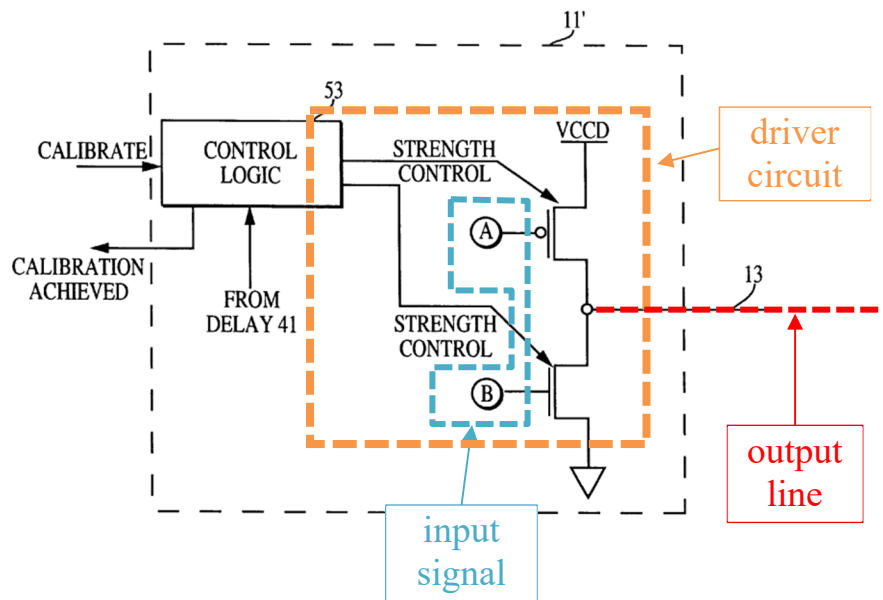
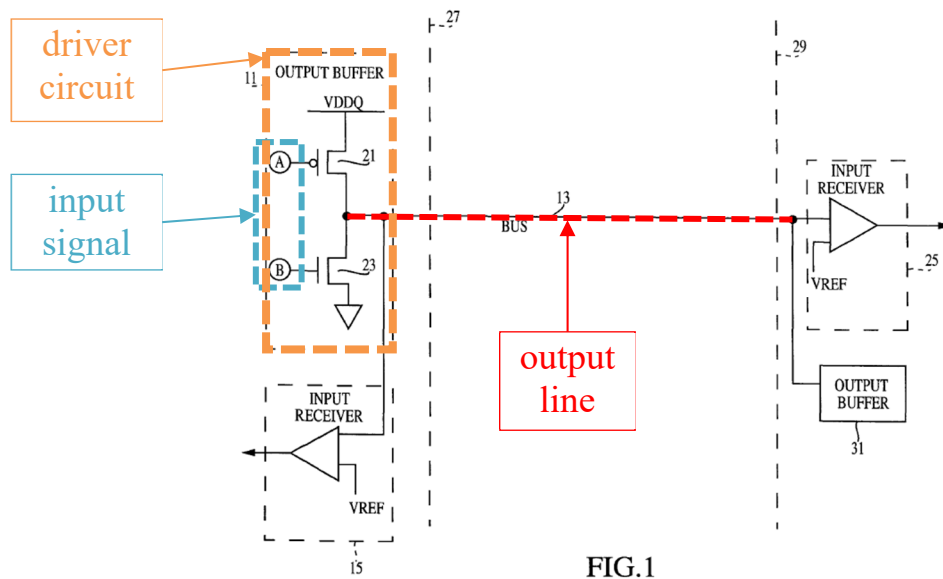
unit configured to change the control signal based upon a result from the comparator unit”).

171. Claims 6 and 7 each depends from claim 1, whose limitations are discussed above in this ground. *See supra* Section X.C.2. Further, for the reasons explained above for Ground 1, Lee teaches the additional limitations of claims 6 and 7. *See supra* Section X.A.4; *see also* Lee (EX1005), at FIGS. 1-3, 6, 3:41-46, 3:58-63, 4:17-5:5, 5:29-34, 5:39-58, 7:22-32.

8. Claim 14

a. “A method for driving an output driver for an integrated circuit having a driver circuit driving an input signal onto an output line, comprising:” [14.P]

172. I understand that the preamble of claim 14 is not necessarily limiting. Nevertheless, to the extent the preamble is limiting, Lee teaches this limitation for the reasons provided above for claim limitations [1.P] and [1.1]. *See supra* Sections X.C.2.a-X.C.2.b (Ground 3 for claim limitations [1.P] and [1.1]) and X.A.1.a-X.A.1.b (Ground 1 for claim limitations [1.P] and [1.1]). As shown in the figure below, Lee discloses driving an output driver (annotated in purple below) for an integrated circuit, such as memory or processors, with a driver circuit (annotated in orange below) that drives an input signal (annotated in blue) onto an output line (annotated in red).



Lee (EX1005), at FIGS. 1, 4 (both shown above), FIGS. 5, 7 (both shown below);
see also Lee (EX1005), at 1:39-44, 3:13-32, 7:57-67, FIG. 6.

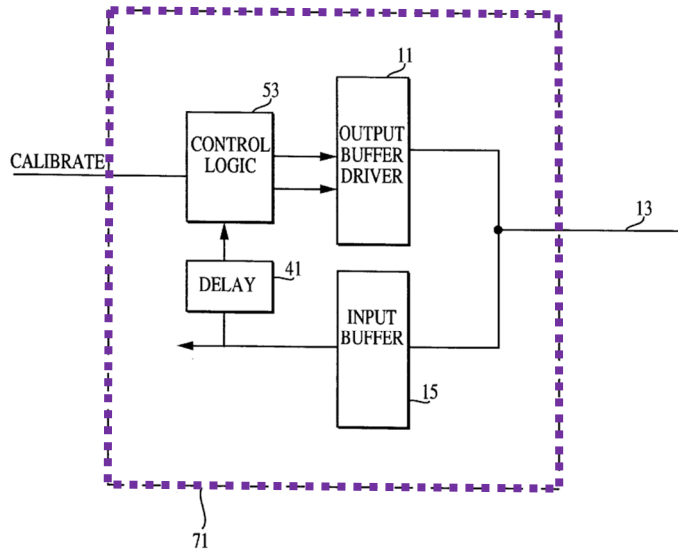


FIG. 5

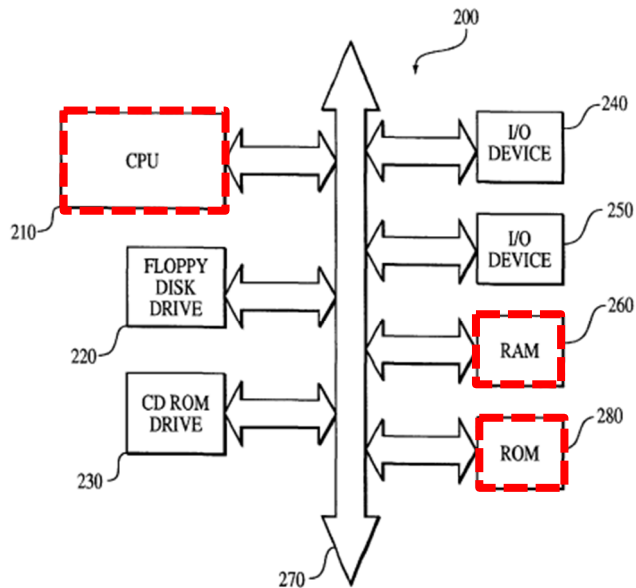


FIG. 7

b. “measuring at least one of an output line current and an output line potential; and” [14.1]

173. As I explained above for claim limitation [1.2], Lee teaches “a measuring circuit for measuring at least one of an output line current and an output

line potential” to the extent it is supported by the ’369 Specification, and thus also teaches this limitation. *See supra* Sections X.A.1.c, X.C.2.c; Lee (EX1005), at FIG. 1, 3:43-46, 4:46-49, 5:28-31, 7:22-26.

c. “controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range, respectively,” [14.2]

174. As I explained above for claim limitation [1.3], Lee in view of JESD79 teaches “*a control unit ... for setting a driver strength ... to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range*” and thus also teaches this limitation. *See supra* Section X.C.2.d; *see, e.g.*, Lee (EX1005) at 1:26-33, 1:61-63, 3:6-9, 3:47-53, 4:6-34, 4:46-5:27, FIGS. 1, 2; JESD79 (EX1007), at 11, 59-60; *see also supra* Section X.A.1.d (Ground 1 for claim limitation [1.3]). In particular, the driver strength of the driver circuit disclosed by Lee is controlled in the combination to set the current in a specification-prescribed current range (e.g., between the “Minimum” and “Maximum” currents shown below in red), and to set the potential in a specification-prescribed potential range (e.g., between 2.3 and 2.7 volts as shown below in blue). *See id.*

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{DDQ} = +2.5\text{ V} \pm 0.2\text{ V}$, $V_{dd} = +3.3\text{ V} \pm 0.3\text{ V}$ or $+2.5\text{ V} \pm 0.2\text{ V}$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	$0.49 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	V	6

JESD79 (EX1007), at 58.

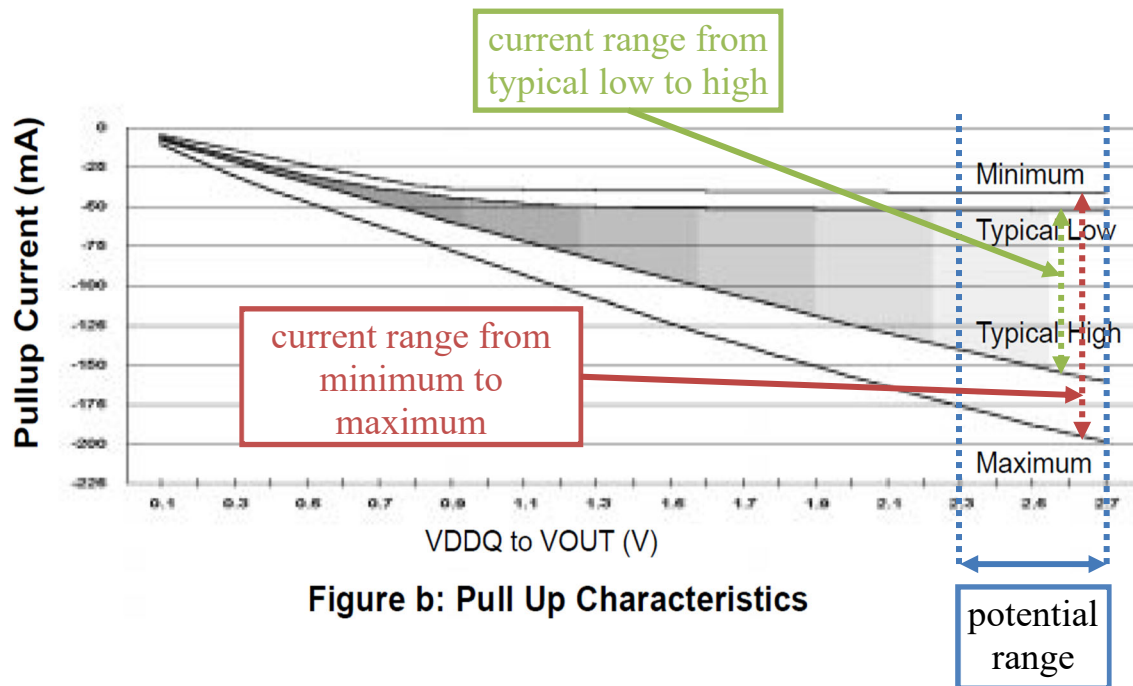
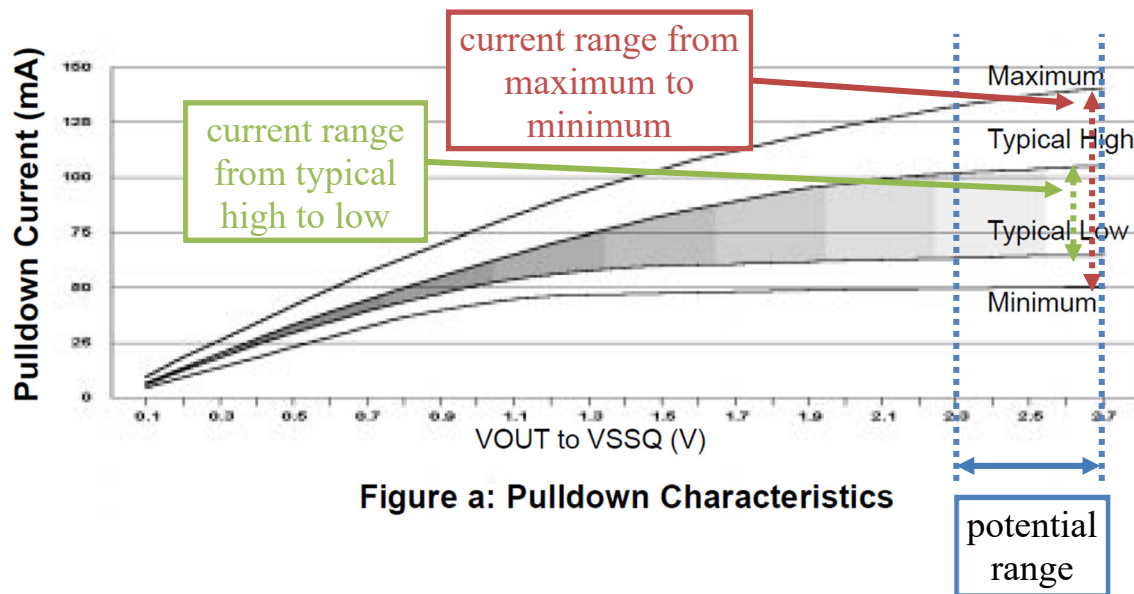


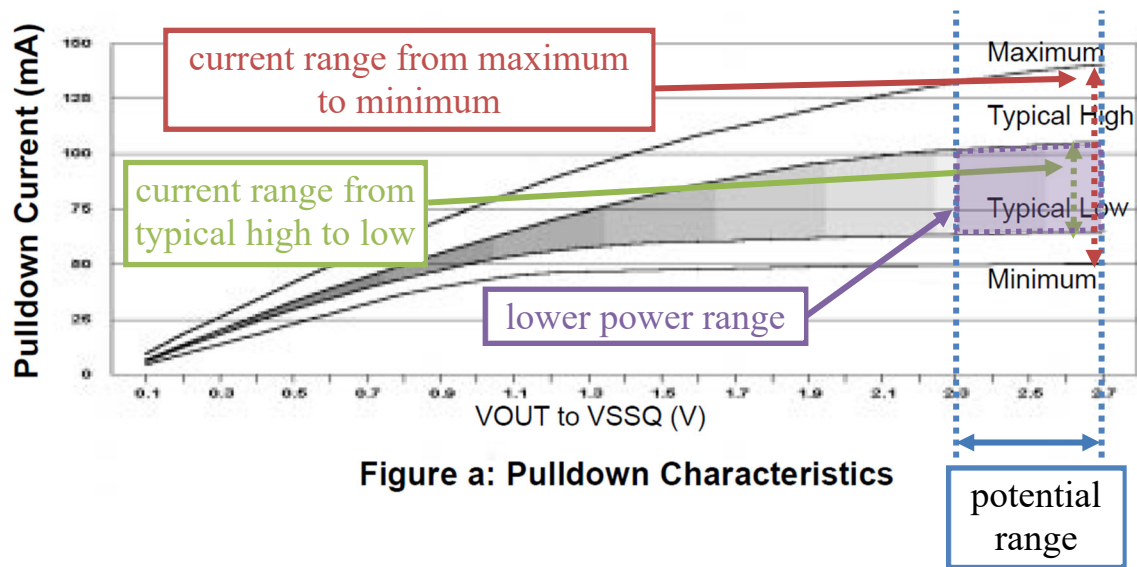
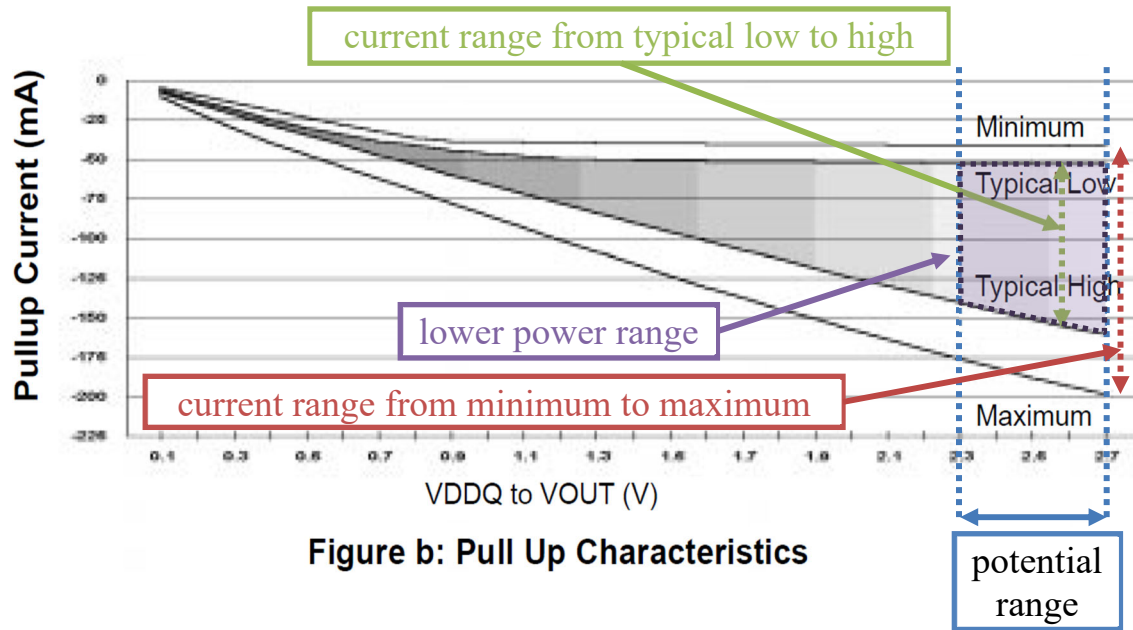
Figure b: Pull Up Characteristics



JESD79 (EX1007), at 59-60.

d. “wherein the driver strength is set such that the potential and the current intensity lie in a lower power range of the specification-prescribed current range and the specification-prescribed potential range, and” [14.3]

175. As I explained above for claim 4, Lee in view of JESD79 teaches a “desired power range [that] corresponds to a lower portion of the specification-prescribed potential range and a lower portion of the specification-prescribed current range” See *supra* Sections X.C.5 (claim 4), X.C.2.d (claim limitation [1.3]). For the reasons provided in claim limitation [1.3] and claim 4, the combination teaches this limitation, including “a lower power range” that corresponds to the “lower portion” of the prescribed potential and current ranges.



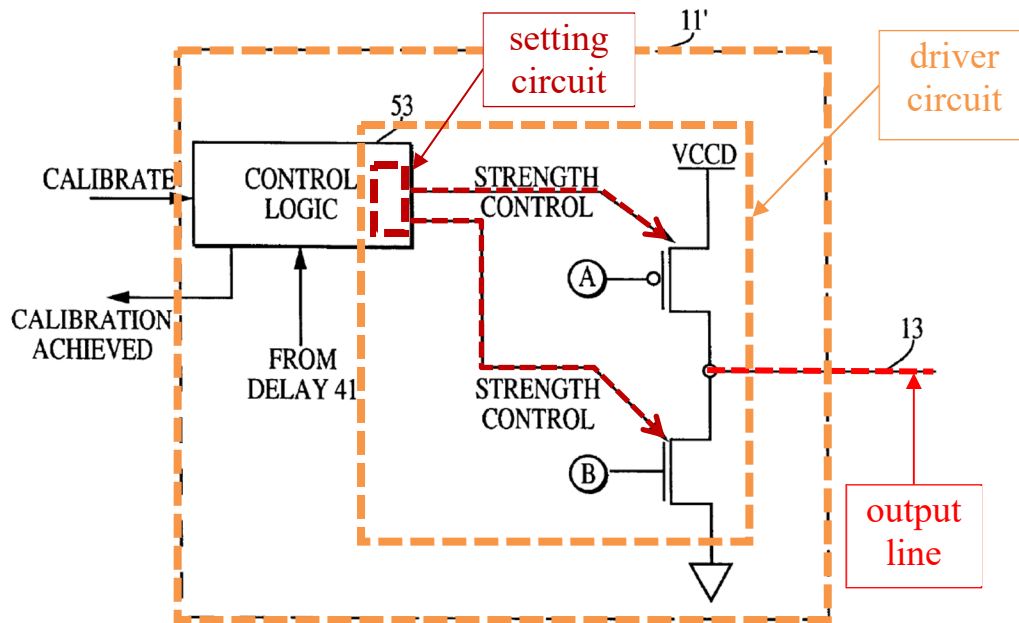
JESD79 (EX1007), at 58-60; *see supra* Sections X.C.5 (claim 4), X.C.2.d (claim limitation [1.3]).

e. “wherein the driver strength is feedback-controlled based on a measured value provided by a measuring circuit.” [14.4]

176. As I explained for claim limitation [1.4], Lee teaches “*a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit*” to the extent the limitation is supported by the ’369 Specification. Therefore, Lee in view of JESD79 teaches this limitation for the same reasons. *See supra* Sections X.A.1.e (Ground 1 for claim limitation [1.4]), X.C.2.e (Ground 2 for claim limitation [1.4]); *see, e.g.*, Lee (EX1005), at 4:36-61, 5:39-58, 7:26-32, FIGS. 1, 2, 4-6.

9. Claim 15: “The method of claim 14, wherein the driver strength of the driver circuit is controlled in a manner selected from continuously, periodically and in accordance with a setting signal.”

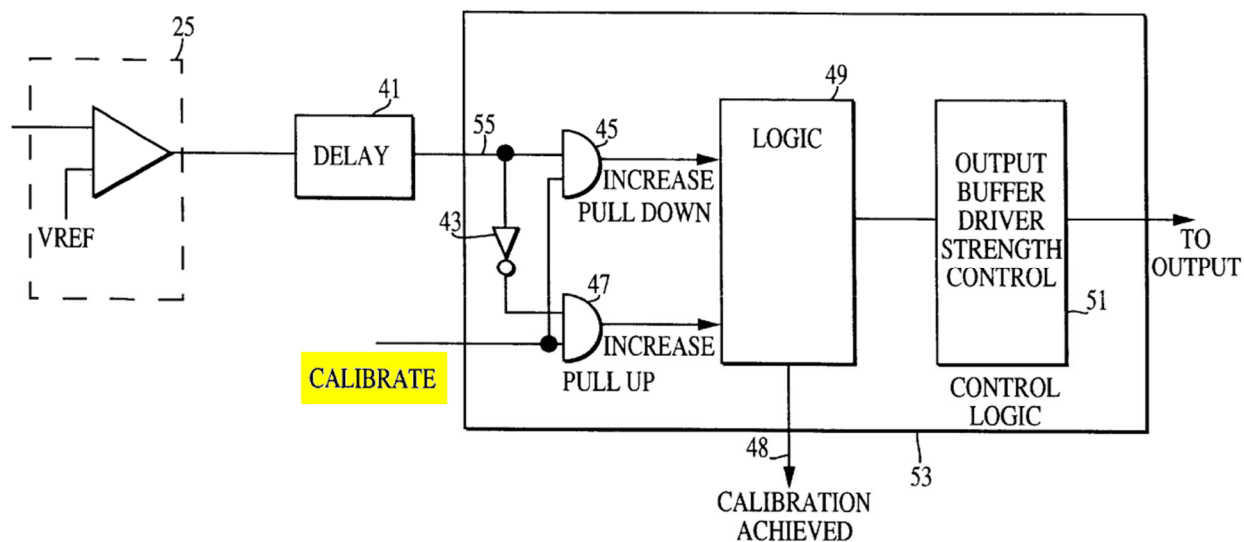
177. As I explained above for claim 5, Lee teaches a “*setting circuit . . . for setting the driver strength of the driver circuit.*” *See supra* Sections X.A.3 (Ground 1 for claim 5); X.C.6 (Ground 3 for claim 5). Specifically, Lee’s output buffer driver strength control circuit 51 (“*setting circuit*”) outputs a strength control signal (“STRENGTH CONTROL”) to the driver. *See id.*



Lee (EX1005), at FIG. 4, 5:42-47; *see also* Lee (EX1005), at FIGS. 5-6, 6:54-63.

The output of the setting circuit (labeled above in red) is “a setting signal,” and thus Lee discloses controlling the driver strength of the driver circuit “in accordance with a setting signal.” *See id.*

178. In addition, Lee teaches that the driver strength of the driver circuit is controlled in accordance with a CALIBRATE signal, which is an additional “setting signal.” Lee (EX1005), at 4:39-41, 5:49-53. As shown in the figure below, the CALIBRATE signal is input to AND-gates 45 and 47 of control logic 53:



Id. at FIG. 2. If the CALIBRATE signal is de-asserted, the outputs of the gates are logic low, and if the CALIBRATE signal is asserted, the outputs of the gates can be logic low or high based on the comparator output via delay 41 and inverter 43.

Id. at 4:36-61, 5:48-54.

179. Further, a POSITA would have understood that Lee’s CALIBRATE signal would have been periodically asserted “after an appropriate delay,” as Lee teaches, to repeat the calibration process. *Id.* at 4:66-67. Thus, the driver strength is also controlled “*periodically*.” *See, e.g., id.* Accordingly, Lee teaches and discloses this limitation alone or in combination with JESD79.

10. Claim 16: “The method of claim 14, further comprising: comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value; and

changing a control signal for setting the driver strength supplied to the driver circuit based upon a result from the comparison.”

180. As I explained above for claim 6, Lee teaches “a comparator unit” “for comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value.” See *supra* Sections X.A.4 (Ground 1 for claims 6 and 7), X.C.7 (Ground 3 for claims 6 and 7). Further, as I explained above for claim 7, Lee teaches “an evaluation unit” “*configured to change the control signal based upon a result from the comparator unit.*” *Id.* In addition, as I explained above for claim limitation [1.3], Lee teaches “*a control unit for providing a control signal for setting a driver strength of the driver circuit.*” See *supra* Section X.A.1.d (Ground 1 for claim limitation [1.3]), X.C.2.d (Ground 3 for claim limitation [1.3]). For the same reasons, Lee in combination with JESD79 teaches claim 16. See, e.g., Lee (EX1005), FIGS. 2-3, 6, 3:41-46, 3:58-63, 4:17-30, 4:31-5:5, 5:28-34, 7:22-32.

D. Claims 1-8, 14-16, and 18 are Obvious over Lee, JESD79, and Garrett

181. In my opinion, the combination of Lee, JESD79, and Garrett renders obvious claims 1-8, 14-16, and 18 of the '369 Patent.

1. Combination of Lee, JESD79, and Garrett

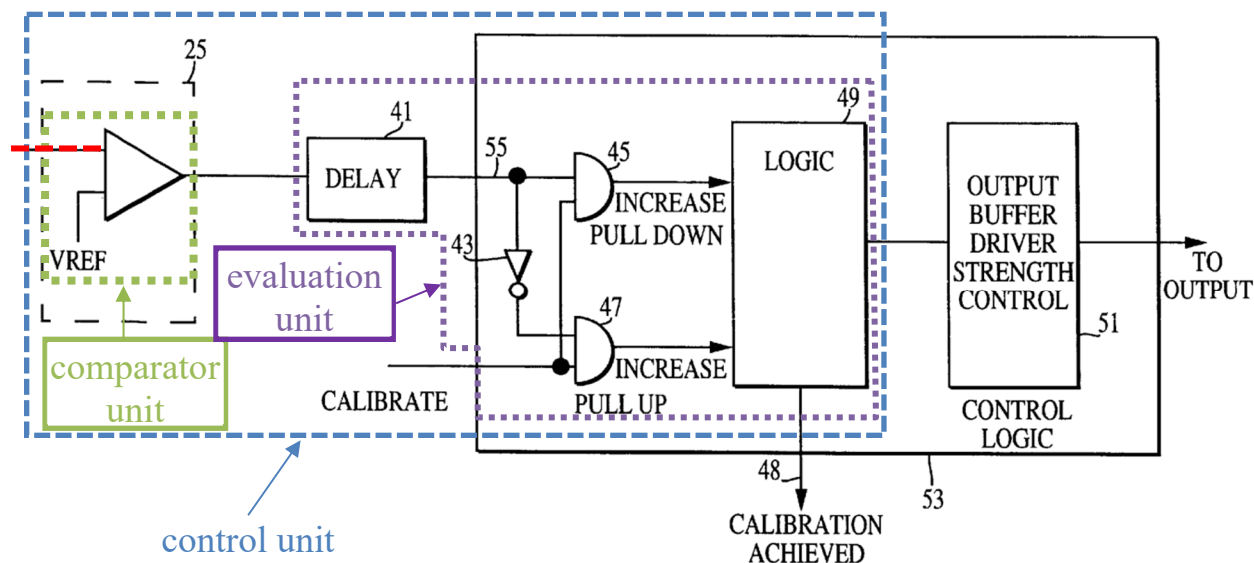
182. Ground 4 combines Ground 3 (Lee and JESD79) with Garrett. As I explain below, Garrett teaches logic for evaluating a comparison to a reference

voltage by using a counter, and it would have been obvious to implement each of the pull-down and pull-up functionality in Lee's logic circuit 49 using the counter of Garrett.

183. As I explain, a POSITA would have been motivated to combine Lee and JESD79 with Garrett and had a reasonable expectation of success in doing so. Lee and Garrett both relate to drive current strength adjustment for a driver that uses feedback control with a comparator. For example, Figure 1 of Lee shows "a simplified schematic diagram of an output buffer driver 11 driving a bus system 13 which can utilize the calibration circuit and method of [Lee's] invention." Lee (EX1005), at 3:13-15, FIG. 1; *see also* Lee (EX1005), at 3:16-32, 4:31-61; *see supra* Section IX.A (Overview of Lee (EX1005)). Similarly, Garrett discloses an "output driver circuit and current control technique to facilitate high-speed buses" such as those "used to interface with high-speed dynamic RAMs (DRAMs)." Garrett (EX1008), at Abstract; *see also* Garrett (EX1008), at FIGS. 2, 11, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 10:6-41; *see supra* Section IX.D (Overview of Garrett (EX1008)). Further, Lee, JESD79, and Garrett each relate to DRAM memory. Lee (EX1005), at 1:39-47, 2:11-20, 2:30-34, 7:38-47; JESD79 (EX1007), at 1, 4-5; Garrett (EX1008), at 1, Abstract, 2:59-62, FIG. 2.

184. As shown in the figure below, Lee discloses a control unit (annotated in blue) with a comparator unit (annotated in green) that is connected to an

evaluation unit (annotated in purple), in which the sampled output from the comparator unit is delayed and then input to AND-gates 45 and 47 that provide instructions to logic 49 for driver strength adjustments for the pull-up and pull-down paths.



Lee (EX1005), at 4:67-5:5, 4:17-34, 5:29-58, FIGS. 1, 2 (shown above), 3, 6. As explained in Ground 3 above, JESD79 provides I-V curves for calibration of an output driver like Lee's. JESD79 (EX1007) at 58-60; *see supra* Section X.C.1 (Combination of Lee and JESD79).

185. Although Lee describes algorithms for its logic block 49, it does not disclose a structure for performing the algorithms. *See* Lee (EX1005), at 4:62-5:27. However, Garrett does disclose structure used to implement algorithms for driver strength feedback control, including a counter. Garrett (EX1008), at FIGS. 2, 11, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 10:6-41.

186. Similar to Lee's sampled comparator output, Garrett discloses a sampled comparator output from sampling latch 130, as shown below.

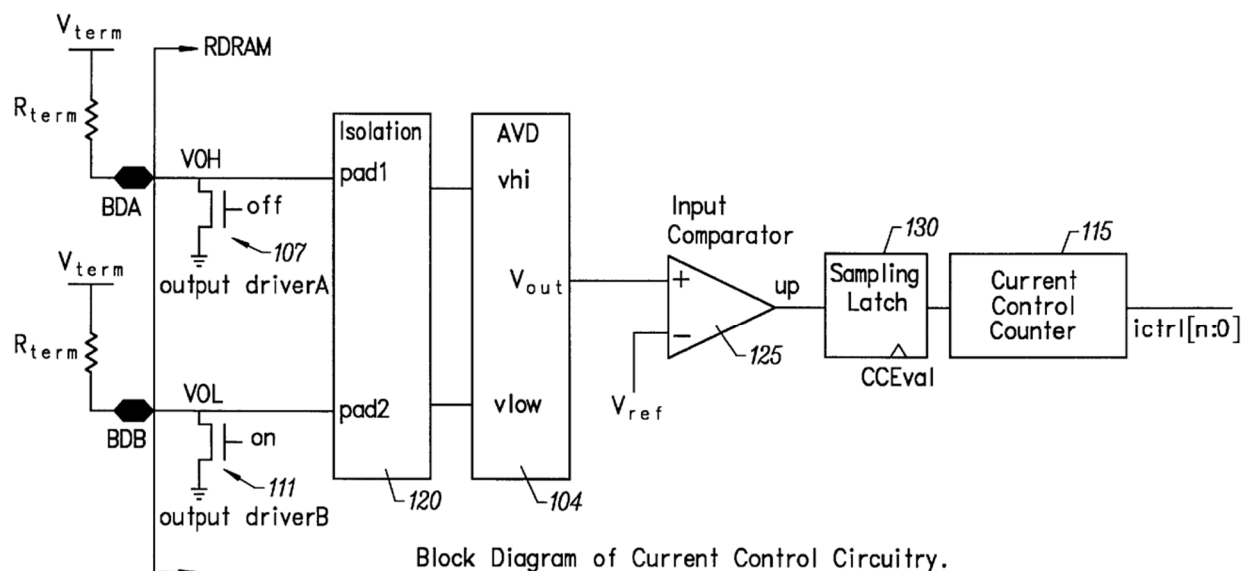


FIG. 2

Garrett (EX1008), at FIGS. 2, 10, 11, 3:14-29, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 9:29-10:5, 10:6-41; *see supra* Section IX.D (Overview of Garrett (EX1008)). Garrett discloses that the output of sampling latch (130) is input to a counter (115), which may be implemented as an up-down counter or a saturating binary search counter, to provide a control signal (ictrl[n:0]) for setting the drive strength. *Id.*

187. Thus, a POSITA would have been motivated to implement Lee's calibration logic 49 with counters to implement the algorithms disclosed in Lee for the pull-up and pull-down paths. Lee (EX1005), at 4:62-5:27, FIG. 2. Specifically, Lee discloses iteratively adjusting the drive strength by increasing or decreasing

the strengths of the pull-up or pull-down transistors, by for example, adjusting effective width of transistors (*id.* at 4:9-10), adjusting the number of parallel transistors enabled or disabled (*id.* at 4:11-20), or adjusting the gate fingers of the transistors (*id.* at 4:20-24). *See also id.* at 4:43-61 (providing an example of increasing drive strength of the weaker transistor), 4:62-5:18 (repeating calibration using newly set driver strength settings until calibration is achieved), FIG. 2. Lee also discloses that a binary search algorithm with coarse and fine adjustments can be used to perform calibration. Lee (EX1005), at 5:20-27 (disclosing a binary search algorithm), 9:63-10:5 (claims 30-31) (coarse and fine adjustment), 12:28-36 (claims 68-69) (course and fine adjustment). Similarly, Garrett teaches using a counter for simple up and down adjustments for drive strengths and more complex binary search algorithms. Garrett (EX1008), at 3:38-40, 7:7-23, 8:67-9:9, 9:18-24.

188. This is simple implementation of Lee's calibration logic in view of Garrett and the knowledge of a POSITA simply combines prior art elements (e.g., Lee's output buffer driver with feedback to adjust the drive strength in accordance with JESD79's I-V curves based on a sampled comparison with a reference and Garrett's counters coupled to a sampled comparison with a reference) according to known methods (e.g., implementing logic to adjust the drive strength settings for the pull-up and pull-down paths using counters) to yield predictable results (e.g., a logic block with counters to perform the algorithms disclosed in Lee for the pull-up

and pull-down paths). Additionally, the implementation applies a known technique (e.g., Garrett’s implementation of logic for drive strength adjustment with counters) to a known device (e.g., Lee’s logic block in combination with JESD79) that is ready for improvement to yield predictable results (e.g., structure for Lee’s logic block that includes counters to perform the algorithms disclosed by Lee for the pull-up and pull-down paths). *Id.*

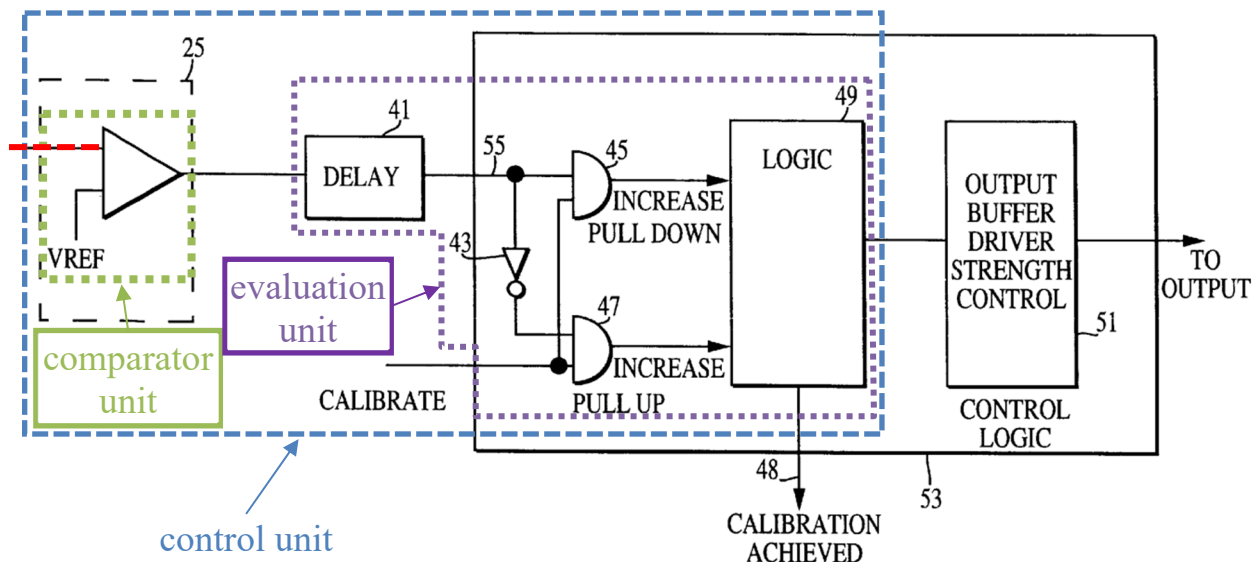
2. Claims 1-7 and 14-16

189. As explained above for Ground 3, Lee and JESD79 teach the limitations of claims 1-7 and 14-16 to the extent each is limiting and supported by the ’369 Specification. *See supra* Sections X.C.2-X.C.10 (Ground 3 for claims 1-7 and 14-16), X.A.1-X.A.4 (Ground 1 for claims 1-2 and 5-7).

190. If any terms in claims 1-7 and 14-16 (e.g., “control unit” in claim 1, “comparator unit” in claim 6, “evaluation unit” in claim 7) are to be construed as means-plus-function limitations, the combination of Lee, JESD79, and Garrett teaches the corresponding structures and claimed functions for these terms, as discussed below for claim 18. *See supra* Sections VIII.B (construction of “comparator means”), VIII.C (construction of “evaluation means”), and VIII.D (construction of “control means”), X.D.4.d (claim limitation [18.3] reciting a “comparator means”), X.D.4.e (claim limitation [18.4] reciting an “evaluation means”), X.D.4.c (claim limitation [18.2] reciting a “control means”).

3. Claim 8: “The output driver of claim 7, wherein the evaluation unit comprises a counter.”

191. Lee and JESD79 in view of Garrett teaches claim 8. As discussed above with respect to claim 7, Lee discloses an evaluation unit (annotated in the figure below in purple) in which the sampled output from the comparator is delayed, input to AND-gates 45 and 47 that provide instructions to logic 49 for driver strength adjustments.



EX1005 (Lee), at 4:67-5:5, 4:17-34, 5:29-58, FIGS. 1, 2 (shown above), 3, 6; *see supra* Sections X.A.4 (Ground 1 for claim 7) and X.C.7 (Ground 3 for claim 7).

192. In combination with Garrett, a POSITA would have been motivated to implement Lee’s logic 49 using a counter, as disclosed in Garrett. *See supra* Section X.D.1 (Combination of Lee, JESD79, and Garrett). Specifically, Garrett

discloses a counter 115 coupled to a sampled comparator output from sampling latch 130, as shown below.

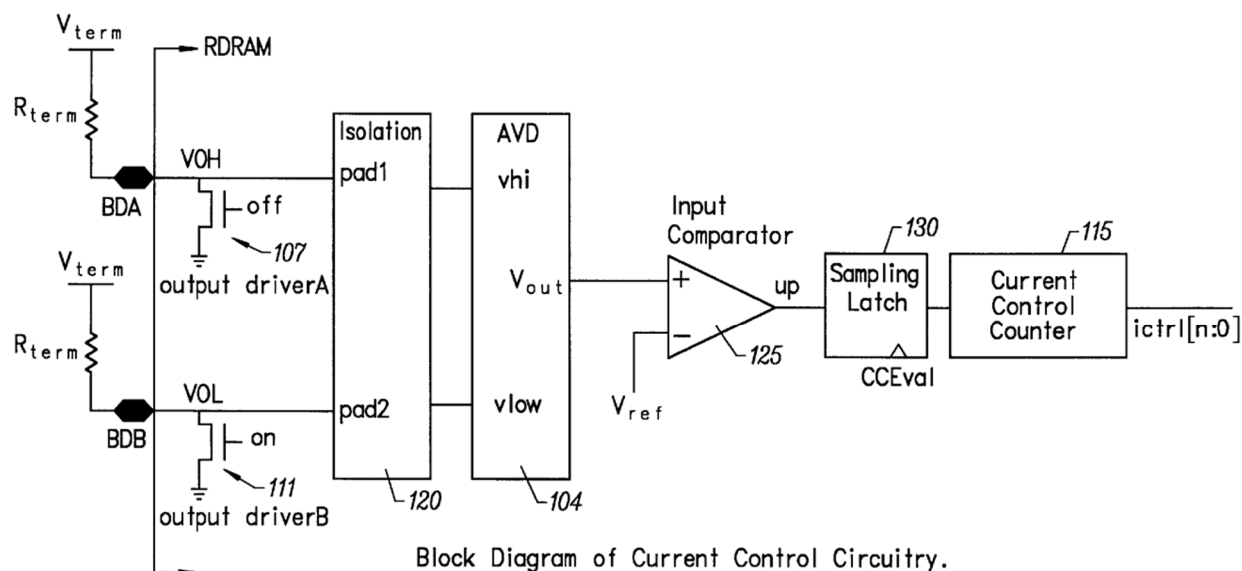


FIG. 2

Garrett (EX1008), at FIGS. 2, 11, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 10:6-41; *see supra* Section IX.D (Overview of Garrett (EX1008)). Garrett discloses that the counter may be implemented as an up-down counter or a saturating binary search counter. *Id.* A POSITA would have understood that the counter in Garrett would have been used to implement the calibration algorithm in Lee for each of the pull-up and pull-down paths, in which the algorithm can be a simple iterative increase or decrease in drive strength (similar to simple up-down control) or a more complex binary search algorithm. Lee (EX1005), at 4:9-24, 4:43-5:18, 5:20-27. Accordingly, Lee's logic 49 (in the "*evaluation unit*") would

have been implemented in the combination with Garrett with “*a counter.*” Thus, the combination teaches claim 8.

4. Claim 18

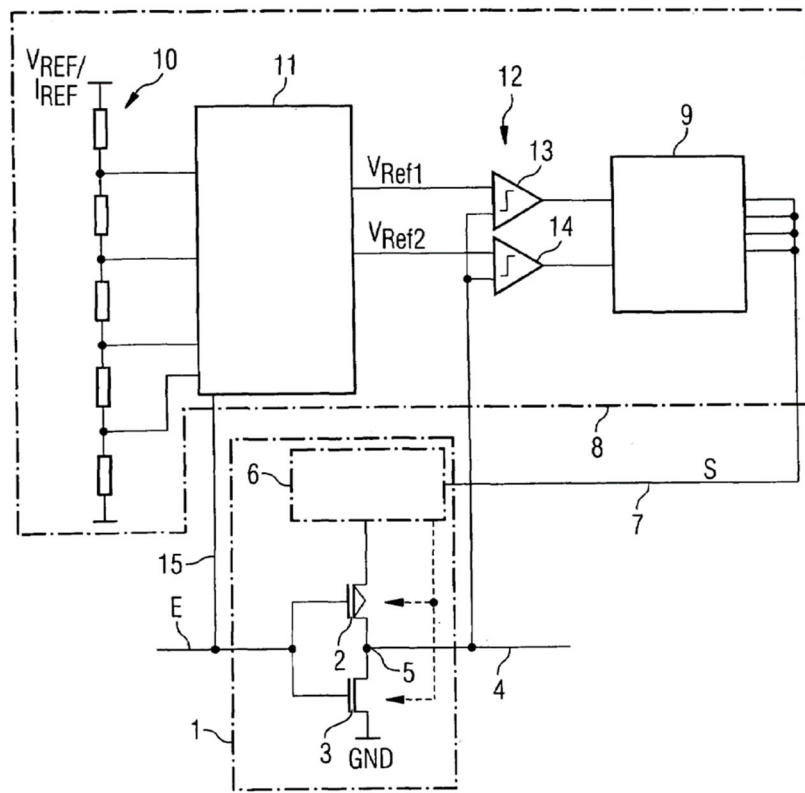
a. “An output driver for an integrated circuit, comprising:” [18.P]

193. I understand that the preamble of claim 18 is not necessarily limiting. Nevertheless, to the extent the preamble is limiting, the combination in Ground 4 discloses this limitation for the reasons provided above in Ground 3 for claim limitation [1.P]. *See supra* Section X.C.2.a (“An output driver for an integrated circuit, comprising:” [1.P]).

b. “a driver means for driving an input signal of the output driver onto an output line; and” [18.1]

194. As I discussed above, “*a driver means*” should be construed as transistors 2 and 3 in Figure 1 of the ’369 Patent that correspond to the claimed function of “*driving an input signal of the output driver onto an output line.*” *See supra* Section VIII.A (“driver means”); EX1001 at FIG. 1 (below).

FIG 1



195. As I discussed for claim limitations [1.1] and [14.P], which each recite the same claimed function of driving an input signal of the output driver onto an output line, Lee teaches two transistors (21 and 23) to drive an input signal onto a bus (13) and thus the combination teaches both the claimed function and corresponding structure. *See supra* Sections X.A.1.b (Ground 1 for claim limitation [1.1]), X.C.2.b (Ground 3 for claim limitation [1.1]), X.C.8.a (Ground 3 for claim limitation [14.P]), X.D.2 (Ground 4 for claim 1 and 14); *see, e.g.*, Lee (EX1005), at FIGS. 1, 4 (both below).

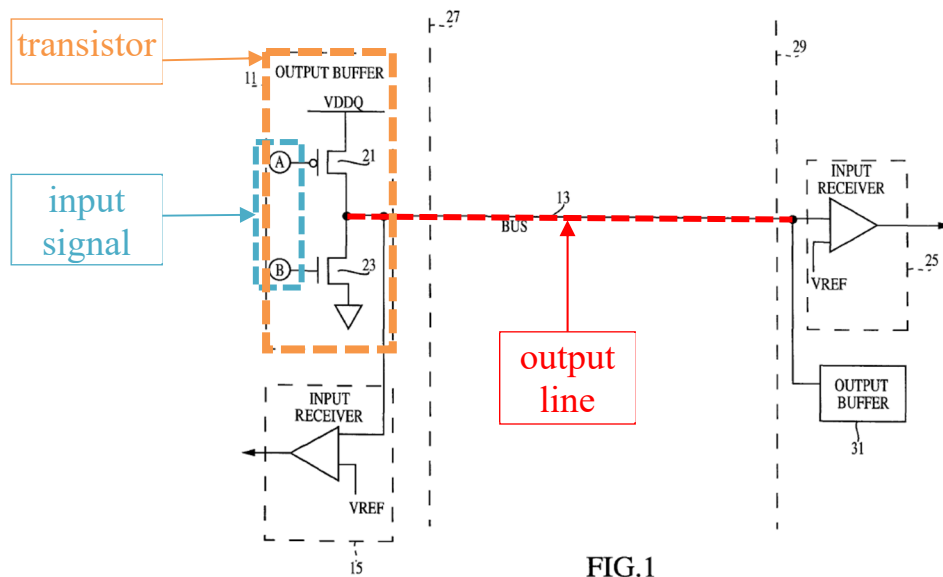


FIG. 1

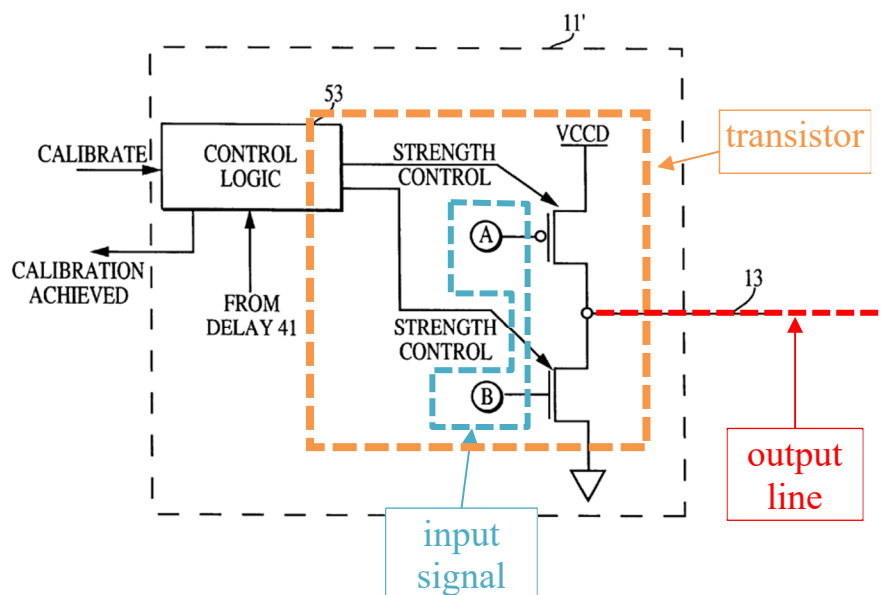


FIG. 4

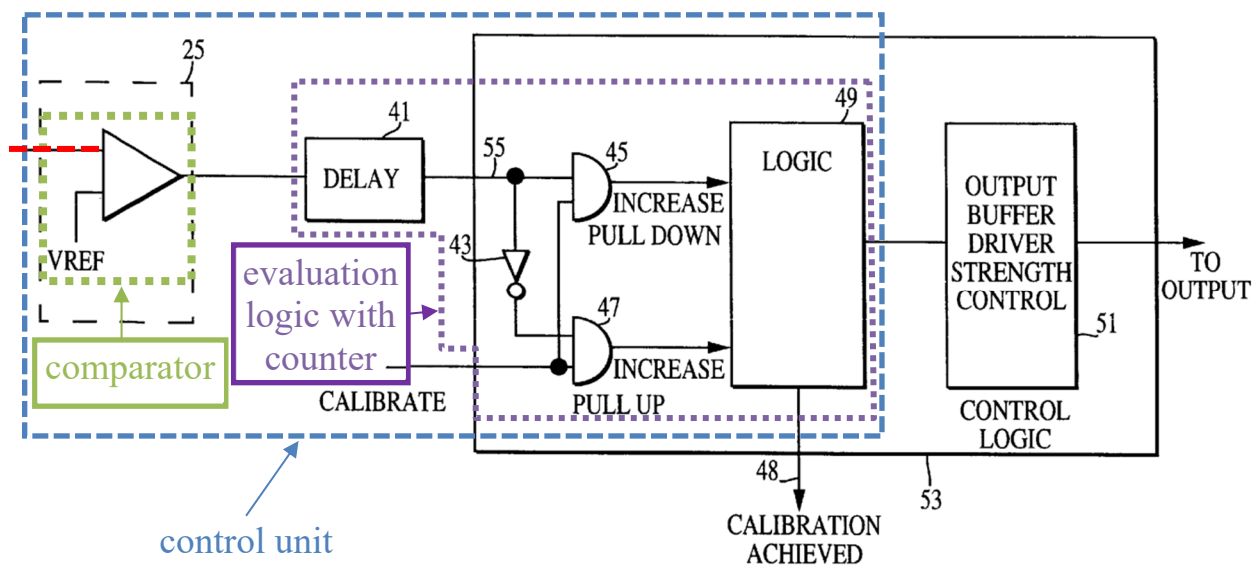
Thus, the combination of Lee, JESD79, and Garrett teaches claim limitation [18.1].

c. “a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range of a specification-prescribed

**potential range and a specification-prescribed current range,
the control means comprising:” [18.2]**

196. As I discussed above, “*a control means*” should be construed as comprised of the combined structure of the “*comparator means*” (a comparator) and “*evaluation means*” (a counter), which are discussed below for claim limitations [18.3] and [18.4]. *See supra* Section VIII.D (“control means”); *see also infra* Sections X.D.4.d-X.D.4.e (Ground 4 for claim limitations [18.3] and [18.4]).

197. As I discussed above for claim limitation [1.3] and claim 8, the combination of Lee, JESD79, and Garrett teach a “*control unit*,” with a comparator and a counter, for nearly the same claimed function (“*for providing a control signal for setting a driver strength of the driver*”) to provide a similar intended result (“... *a desired power range* ...”). *See supra* Sections X.A.1.d (Ground 1 for claim limitation [1.3]), X.C.2.d (Ground 3 for claim limitation [1.3]), X.D.2 (Ground 4 for claim 1), and X.D.3 (Ground 4 for counter of claim 8); *see, e.g.*, Lee (EX1005), at FIG. 2 (below). For this same reasons, the combination also teaches the “*control unit*” of claim 1 if it is construed as a means-plus-function limitation. *See supra* Section X.D.2 (Ground 4 for claim 1).



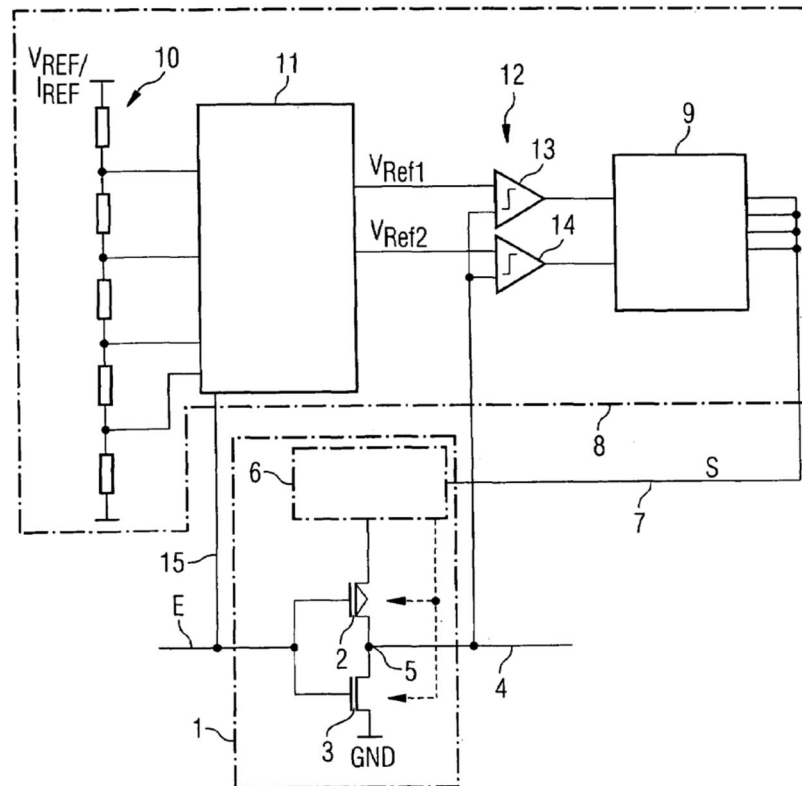
198. Further, the same intended result (“... *a lower power range* ...”) is very similar to that in claim limitation [14.3] (“... *a lower power range* ...”), which is taught by Lee in view of JESD79, both alone and in combination with Garrett. *See supra* Sections X.C.8.d (Ground 3 for claim limitation [14.3]), X.D.2 (Ground 4 for claim 14). Thus, the combination teaches both the claimed function and corresponding structure of claim limitation [18.2].

d. “a comparator means for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value; and” [18.3]

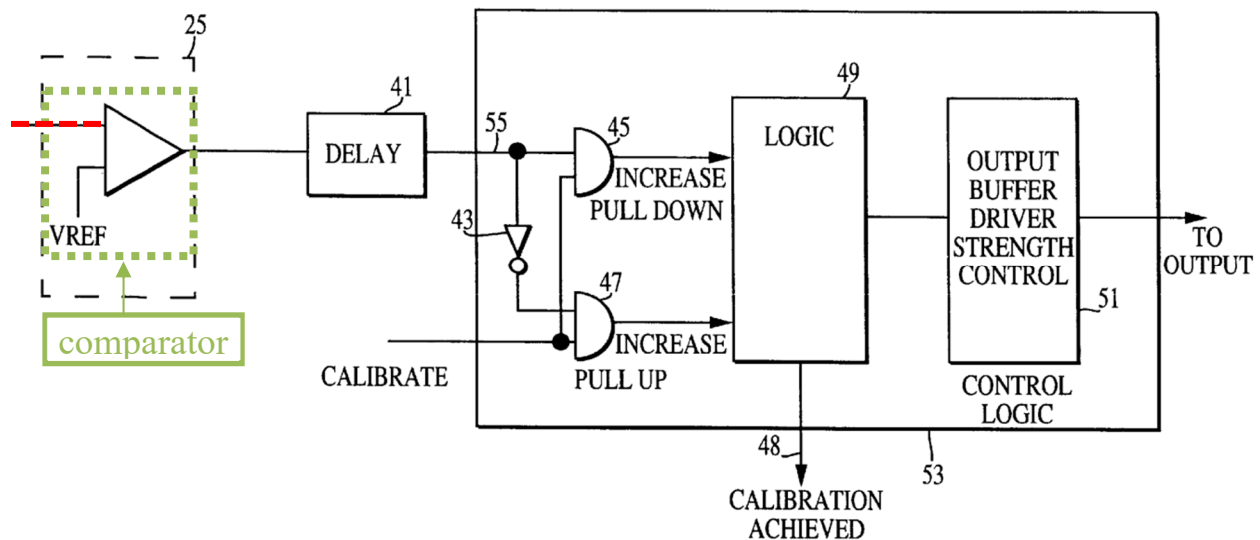
199. As I discussed above, “*a comparator means*” should be construed as one or more comparators (e.g., one or more of comparators 13 or 14 in Figure 1 of the ’369 Patent) that corresponds to the claimed function of “*comparing at least one of the output line current and the output line potential respectively with at*

least one of a reference current value and a reference potential value.” See *supra* Section VIII.B (“comparator means”); ’369 Patent (EX1001), at FIG. 1 (below).

FIG 1



200. As I discussed above for claim 6, which recites a “*comparator unit*” and the same claimed function, Lee teaches a comparator that compares the measured output line potential to a reference potential value and/or the measured output line current to a reference current value. See *supra* Section X.A.4 (Ground 1 for claim 6), X.C.7 (Ground 3 for claim 6), X.D.2 (Ground 4 for claim 6). Thus, alone, in combination with JESD79, and in combination with JESD79 and Garrett, Lee teaches both the claimed function and corresponding structure of claim limitation [18.3]. See *id.*; see, e.g., EX1005 at FIG. 2 (below).



201. For these reasons, the combination of Lee, JESD79, and Garrett also teaches the “*comparator unit*” of claim 6 if it is construed as a means-plus-function limitation. *See supra* Section X.D.2 (Ground 4 for claim 6).

e. “an evaluation means for changing the control signal based upon a comparison result from the comparator means.” [18.4]

202. As I discussed above, “*an evaluation means*” should be construed as a counter that corresponds to the claimed function of “*changing the control signal based upon a comparison result from the comparator means.*” *See supra* Section VIII.C (“evaluation means”); ’369 Patent (EX1001), at 5:25-30, 5:42-47, 7:35-36.

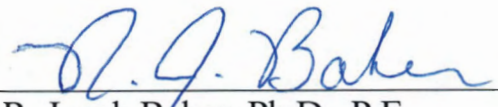
203. As I discussed above for claim 7, which recites the same claimed function, Lee teaches an “*evaluation unit*” that includes Lee’s calibration logic 49. *See supra* Section X.A.4 (Ground 1 for claim 7), X.C.7 (Ground 3 for claim 7), X.D.2 (Ground 4 for claim 7); *see, e.g.*, Lee (EX1005), at FIG. 2. Further, as I

discussed above for claim 8, which recites “*a counter*” in the “*evaluation unit*,” a POSITA would have understood that the counter disclosed in Garrett would have been used in implementing Lee’s calibration logic 49 for each of the pull-up and pull-down paths. *See supra* Section X.D.3 (Ground 4 for claim 8); *see, e.g.*, Garrett (EX1008), at FIG. 2. Thus, the combination of Lee, JESD79, and Garrett teaches the claimed function and the corresponding structure of claim limitation [18.4].

204. For these reasons, the combination of Lee, JESD79, and Garrett also teaches the “*evaluation unit*” of claim 7 if it is construed as a means-plus-function limitation. *See supra* Section X.D.2 (Ground 4 for claim 7).

I, R. Jacob Baker, Ph.D., P.E., declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Dated: February 3, 2023



R. Jacob Baker, Ph.D., P.E.