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Double Data Rate (DDR) SDRAM Specification

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Double Data Rate (DDR) SDRAM Specification

(The material contained in this standard was formulated under the cognizance of the JC-42.3 Subcommittee on RAM Memories and approved by the JEDEC Board of Directors. The text in this standard is from the following BoD Ballots: JCB-99-70, JCB-99-84, JCB-00-08, JCB-00-10 JCB-00-11, JCB-00-12, JCB-00-13, and JCB-00-23.)

1 Purpose

To define the minimum set of requirements for JEDEC-compliant 64M x4/x8/x16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

2 Scope

This comprehensive standard defines all required aspects of 64M x4/x8/x16 DDR SDRAMs, including features, functionality, AC and DC parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

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DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M x4 (4 M x4 x4 banks), 8 M x8 (2 M x8 x4 banks), 4 M x16 (1 M x16 x4 banks)

FEATURES

- Double–data–rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge–aligned with data for READs; center–aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 15.6 μs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ = +2.5 V ±0.2 V
- VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V

GENERAL DESCRIPTION

The 64 Mb DDR SDRAM is a high–speed CMOS, dynamic random–access memory containing 67,108,864 bits. It is internally configured as a quad–bank DRAM.

The 64 Mb DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM effectively consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half–clock–cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge–aligned with data for READs and center–aligned with data for WRITEs.

The 64 Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW will be referred to as the postive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self–timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power–saving, power–down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices will have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC 64 M x4/x8/x16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

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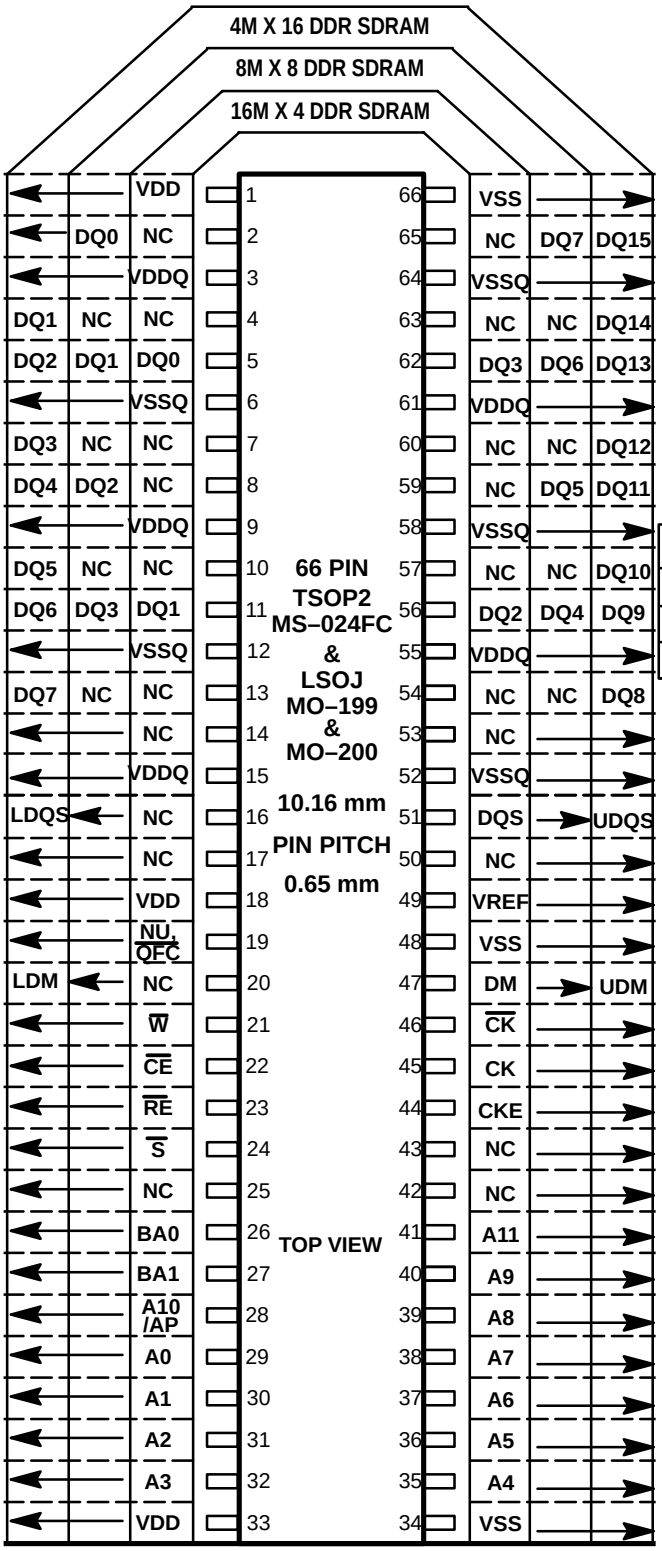


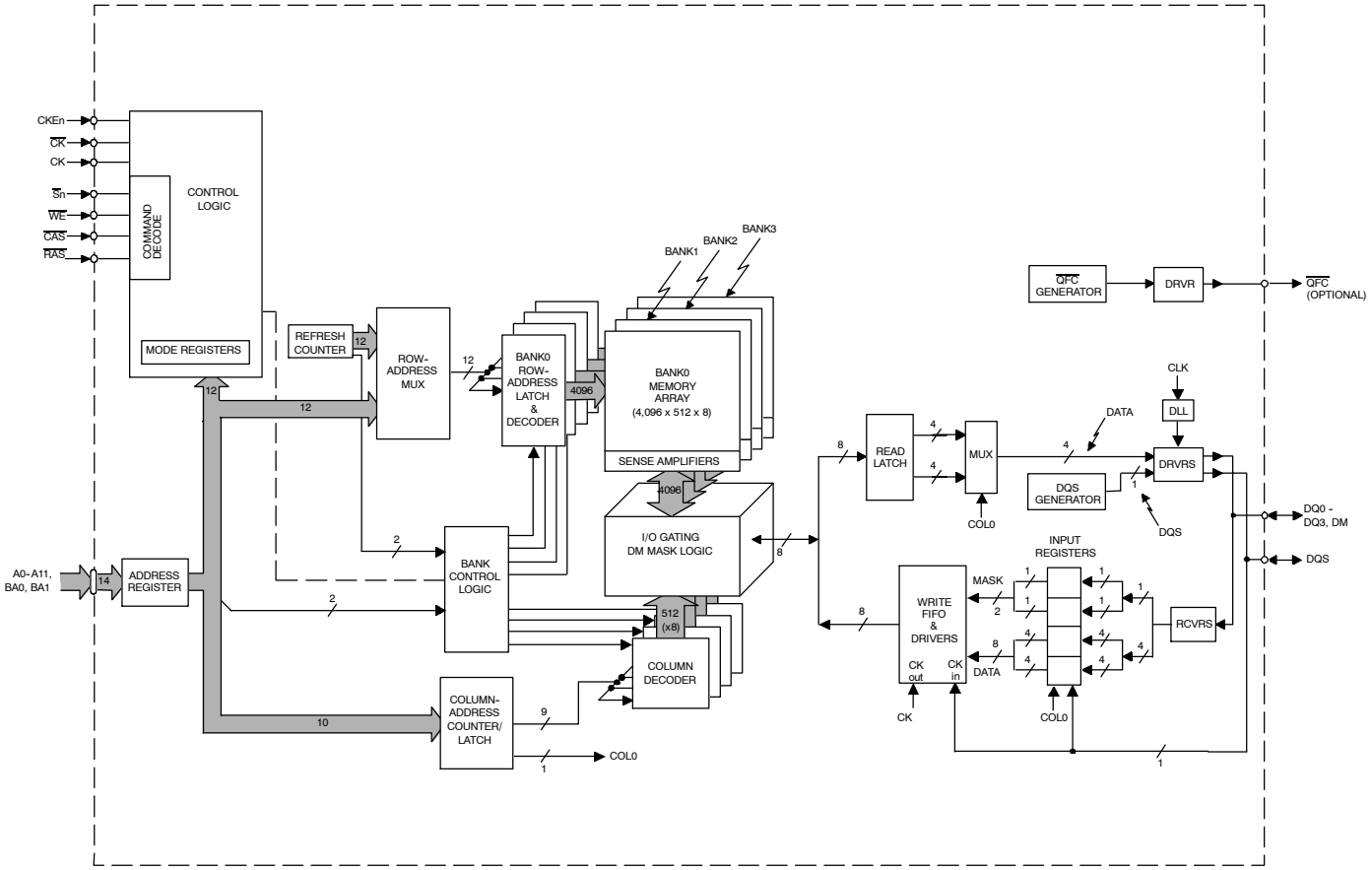
ADDRESS ASSIGNMENT TABLE

	DENSITY	BANKS	ROW ADDR.	COL ADDR	BANK ADDR
16M X 4	64 Mb	4	A0⇒A11	A0⇒A9	BA0, BA1
8M X 8	64 Mb	4	A0⇒A11	A0⇒A8	BA0, BA1
4M X 16	64 Mb	4	A0⇒A11	A0⇒A7	BA0, BA1

64 M DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ

Release 1

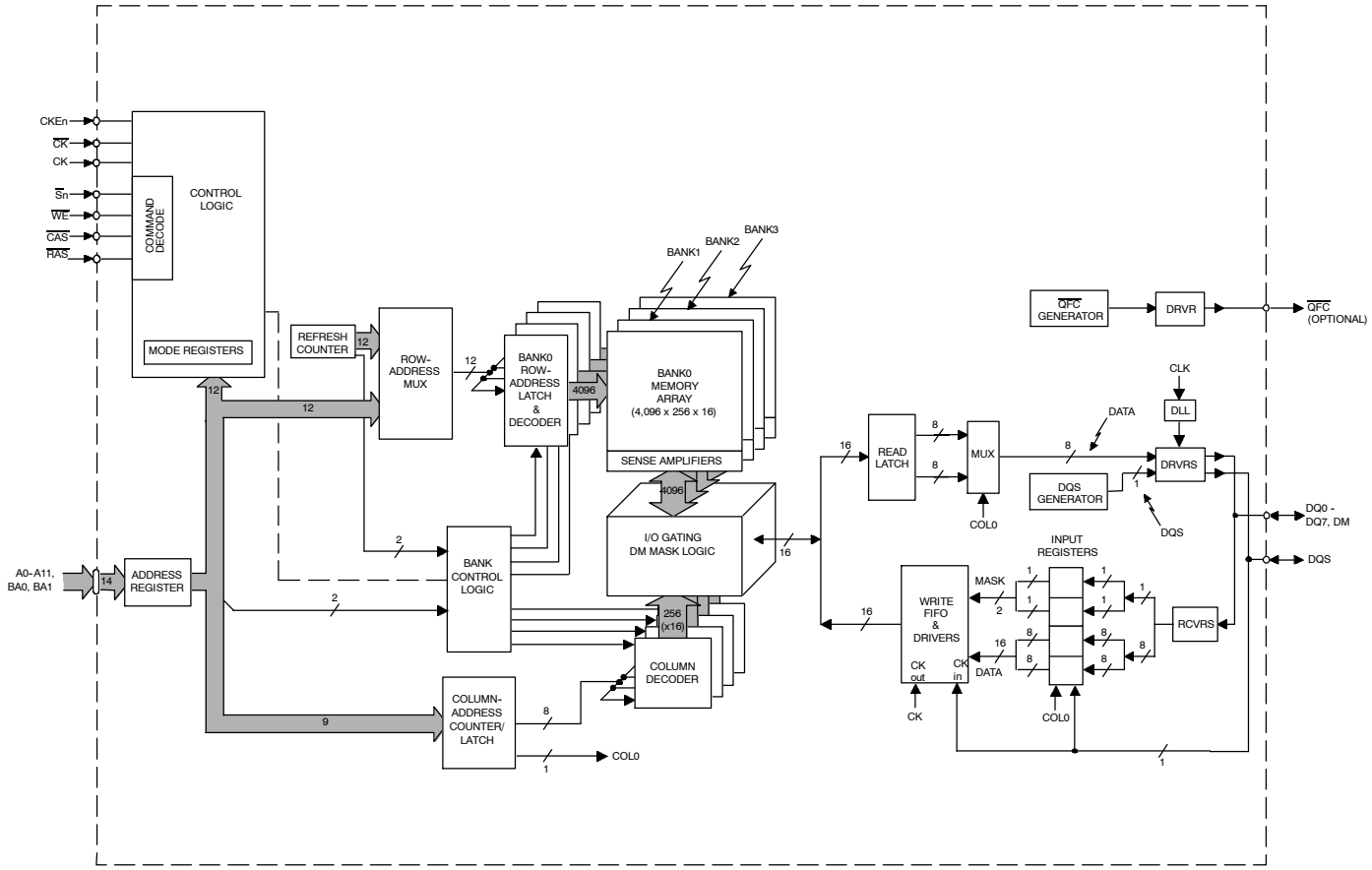
FUNCTIONAL BLOCK DIAGRAM – x4 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

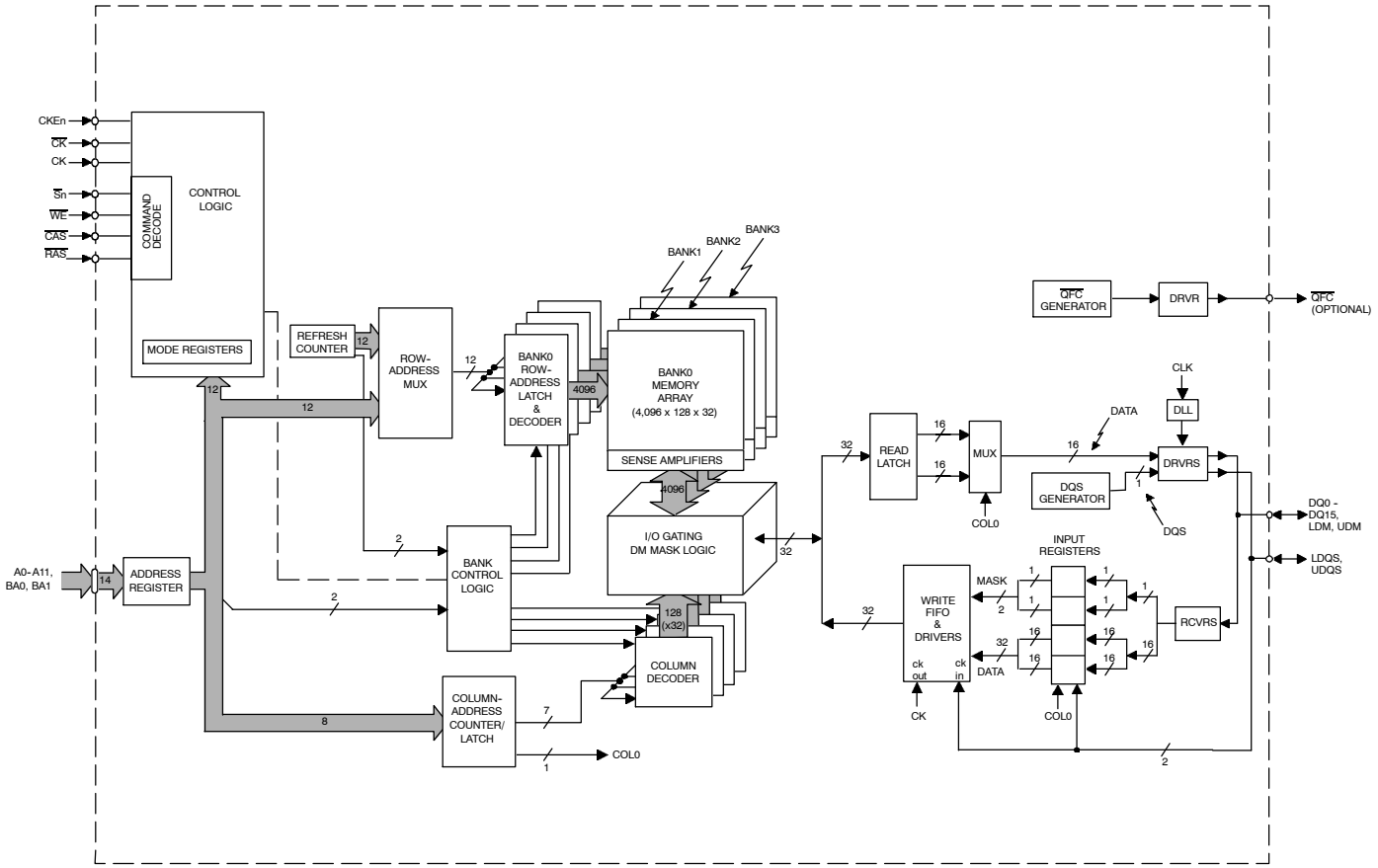
FUNCTIONAL BLOCK DIAGRAM – x8 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

FUNCTIONAL BLOCK DIAGRAM – x16 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: LDM and UDM are unidirectional signals (input only) but are internally loaded to match the load of the bidirectional DQ and DQS signals.

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE(n)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER–DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER–DOWN (row ACTIVE in any bank). CKE is synchronous for POWER–DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER–DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied. The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{S}$(n)	Input	Chip Select: All commands are masked when $\overline{S}$ is registered high. $\overline{S}$ provides for external bank selection on systems with multiple banks. $\overline{S}$ is considered part of the command code. The standard pinout includes one $\overline{S}$ pin. Optional pinouts include $\overline{S}$0 and $\overline{S}$1 on different pins, to facilitate device stacking.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{S}$) define the command being entered.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0–DQ7; UDM corresponds to the data on DQ8–DQ15.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.–
A0–A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op–code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Input/Output: Data bus
DQS	I/O	Data Strobe: Output with read data, input with write data. Edge–aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0–DQ7; UDQS corresponds to the data on DQ8–DQ15.
$\overline{QFC}$	Output	FET Control: Optional. Output during every Read and Write access. Can be used to control isolation switches on modules. Open drain output.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V ±0.2 V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V ±0.3 V or +2.5 V ±0.2 V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

FUNCTIONAL DESCRIPTION

The 64 Mb DDR SDRAM is a high–speed CMOS, dynamic random–access memory containing 67,108,864 bits. The 64 Mb DDR SDRAM is internally configured as a quad–bank DRAM.

The 64 Mb DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double–data–rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch–up, which may cause permanent damage to the device. Vref can be applied any time after VDDQ, but is expected to be nominally coincident with Vtt. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power–up is required to guarantee that the DQ and DQS outputs will be in the High–Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 µs delay prior to applying an executable command.

Once the 200 µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the ”all banks idle” state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 1. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self–clearing).

Mode Register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 specify the operating mode.

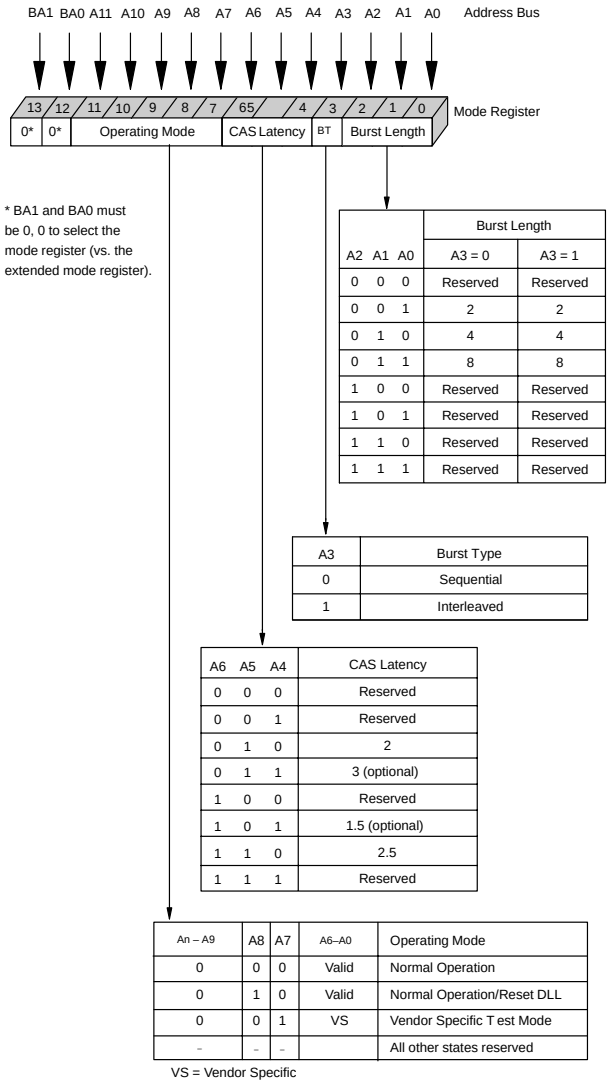
The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–Ai when the burst length is set to two, by A2–Ai when the burst length is set to four and by A3–Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.



A2	A1	A0	Burst Length A3 = 0	Burst Length A3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

A3	Burst Type
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (optional)
1	0	0	Reserved
1	0	1	1.5 (optional)
1	1	0	2.5
1	1	1	Reserved

An – A9	A8	A7	A6–A0	Operating Mode
0	0	0	Valid	Normal Operation
0	1	0	Valid	Normal Operation/Reset DLL
0	0	1	VS	Vendor Specific T est Mode
–	–	–		All other states reserved

Figure 1
MODE REGISTER DEFINITION

Table 1

BURST DEFINITION

Burst Length	Starting Coumn Adress:			Order of Accesses Within a Burst Type = Sequential	Order of Accesses Within a Burst Type = Interleaved
2			A0		
			0	0–1	0–1
			1	1–0	1–0
4		A1	A0		
		0	0	0–1–2–3	0–1–2–3
		0	1	1–2–3–0	1–0–3–2
		1	0	2–3–0–1	2–3–0–1
		1	1	3–0–1–2	3–2–1–0
8	A2	A1	A0		
	0	0	0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0	0	1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0	1	0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0	1	1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1	0	0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1	0	1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1	1	0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1	1	1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0

Note:
1. For a burst length of two, A1–Ai selects the two–data–element block; A0 selects the first access within the block.
2. For a burst length of four, A2–Ai selects the four–data–element block; A0–A1 selects the first access within the block.
3. For a burst length of eight, A3–Ai selects the eight–data–element block; A0–A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A11 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is inititated by issuing a Mode Register Set command with bits A7 and A9–A11 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7–A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Table 2
CAS LATENCY AND FREQUENCY

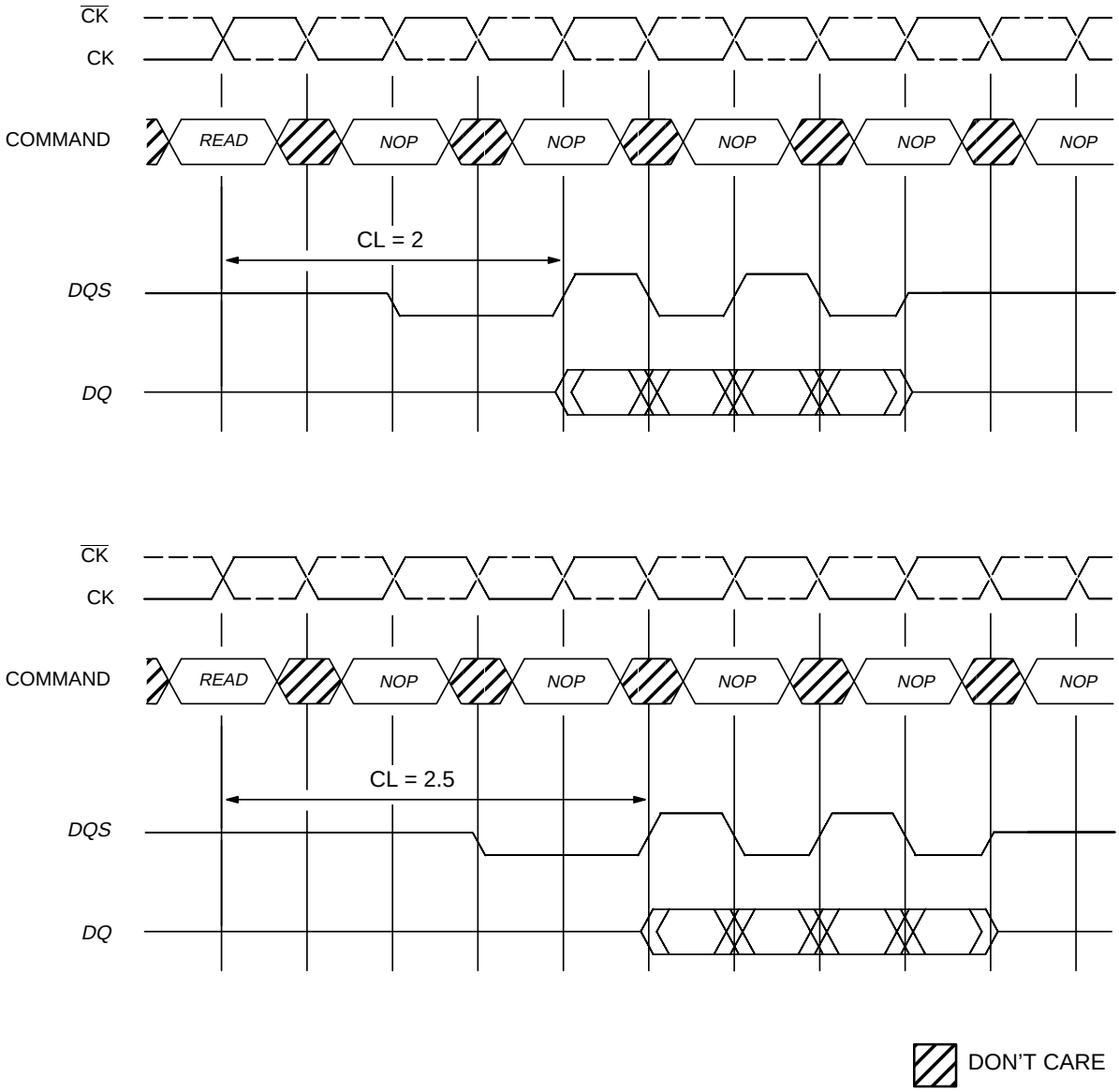
	MAXIMUM OPERATING FREQUENCY (MHz)*		
	DDR–266A	DDR–266B	DDR–200
CL2	133	100	100
CL2.5	143	133	125

* Values are nominal (i.e., may have been rounded off; exact tCK should be used).

Terminology Definitions. The following are definitions of the terms DDR–200 & DDR–266 as used in this specification

DDR–200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The corresponding nominal data rate is 200 MHz.

DDR–266n: Speed grades for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is 266 MHz. Devices designated as DDR–266B will operate with CAS Latency = 2.5 clock periods at a 133 MHz clock frequency. Devices designated as DDR–266A will operate with CAS Latency = 2 clock periods at a 133 MHz clock frequency.



Burst Length = 4 in the cases shown
Shown with nominal tDQSCK, and tDQSQ

Figure 2
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional), and $\overline{\text{QFC}}$ output enable/disable (optional). These functions are controlled via the bits shown in Figure 3. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power–up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point–to–point environments. I–V curves for the normal drive strength are included in this document; the curves for the weak drive strength will be included in a future revision.

$\overline{\text{QFC}}$ Enable/Disable

The $\overline{\text{QFC}}$ signal might be provided by certain vendors to control FET switches used to isolate module loads from the system memory bus at times when the given module is not being accessed.

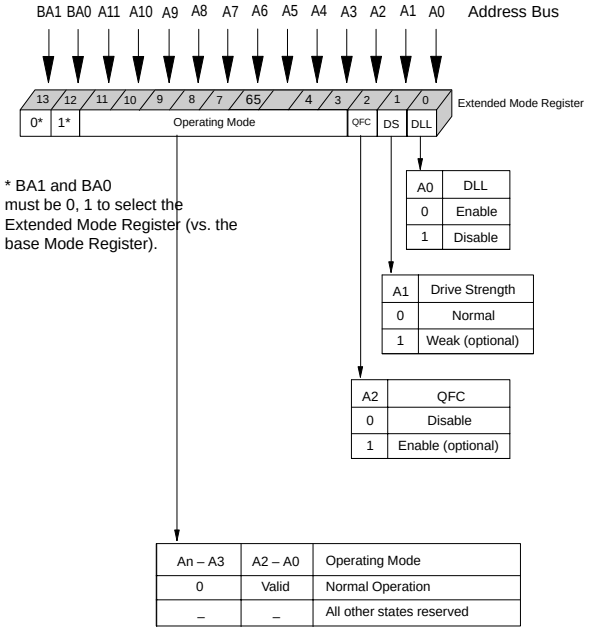


Figure 3
EXTENDED MODE REGISTER DEFINITION

COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a _ Commands

(Notes: 1)

NAME (Function)	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7
MODE REGISTER SET	L	L	L	L	Op–Code	2

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0–BA1 are reserved; A0–A11 provide the op–code to be written to the selected Mode Register.
3. BA0–BA1 provide bank address and A0–A11 provide row address.
4. BA0–BA1 provide bank address; A0–Ai provide column address (where i = 7 for x16, 8 for x8 and 9 for x4); A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are ”Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are ”Don’t Care” except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.

TRUTH TABLE 1b _ DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

NOTE: 1. Used to mask write data, provided coincident with the corresponding data.

DESELECT

The DESELECT function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an DDR SDRAM which is selected ($\overline{S}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A11. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as ”Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual–bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to /CAS–BEFORE–/RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an AUTO REFRESH command. The 64 Mb DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of 15.6 µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 * 15.6 µs (140.4 µs).

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are ”Don’t Care” during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be ”opened.” This is accomplished via the ACTIVE command (Figure 4), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been ”closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row–access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

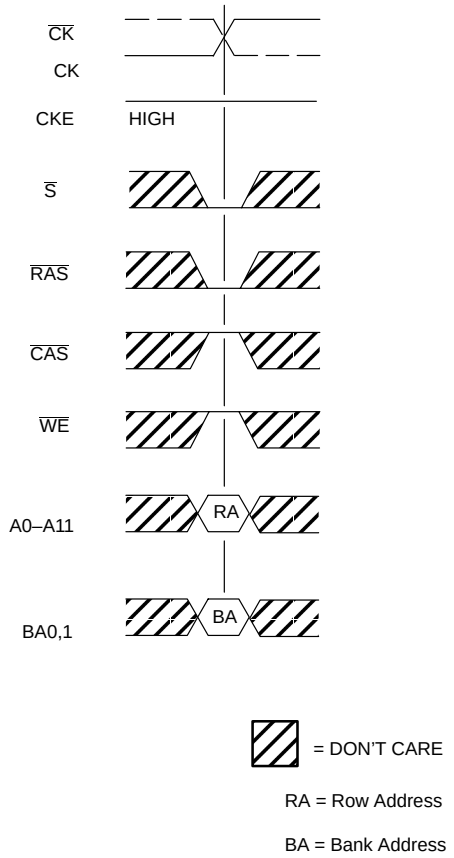


Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

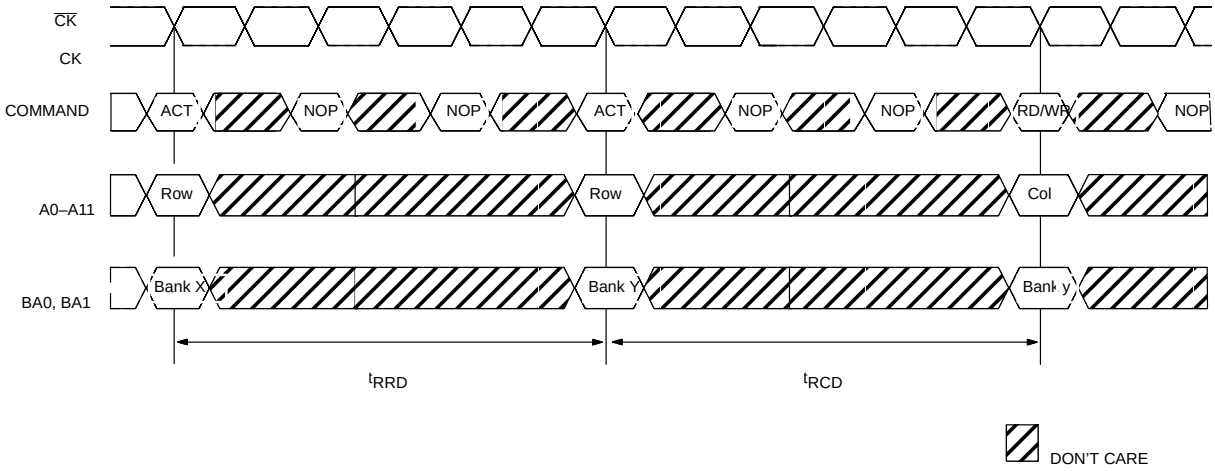


Figure 5
tRCD and tRRD Definition

Reads

READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data–out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data–out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 7 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data–out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High–Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 8. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 9. Full–speed random read accesses within a page (or pages) can be performed as shown in Figure 10.

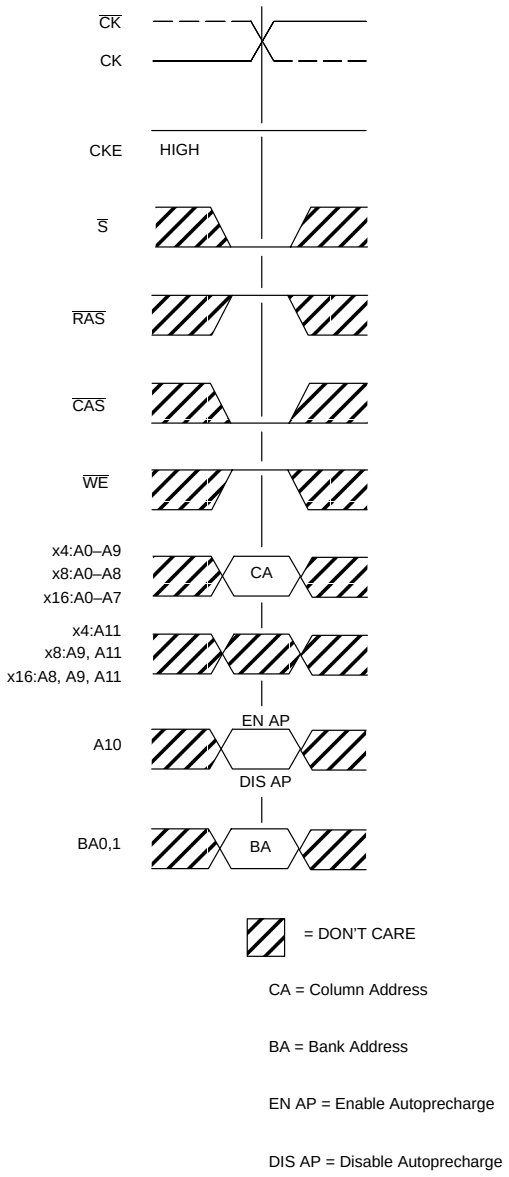
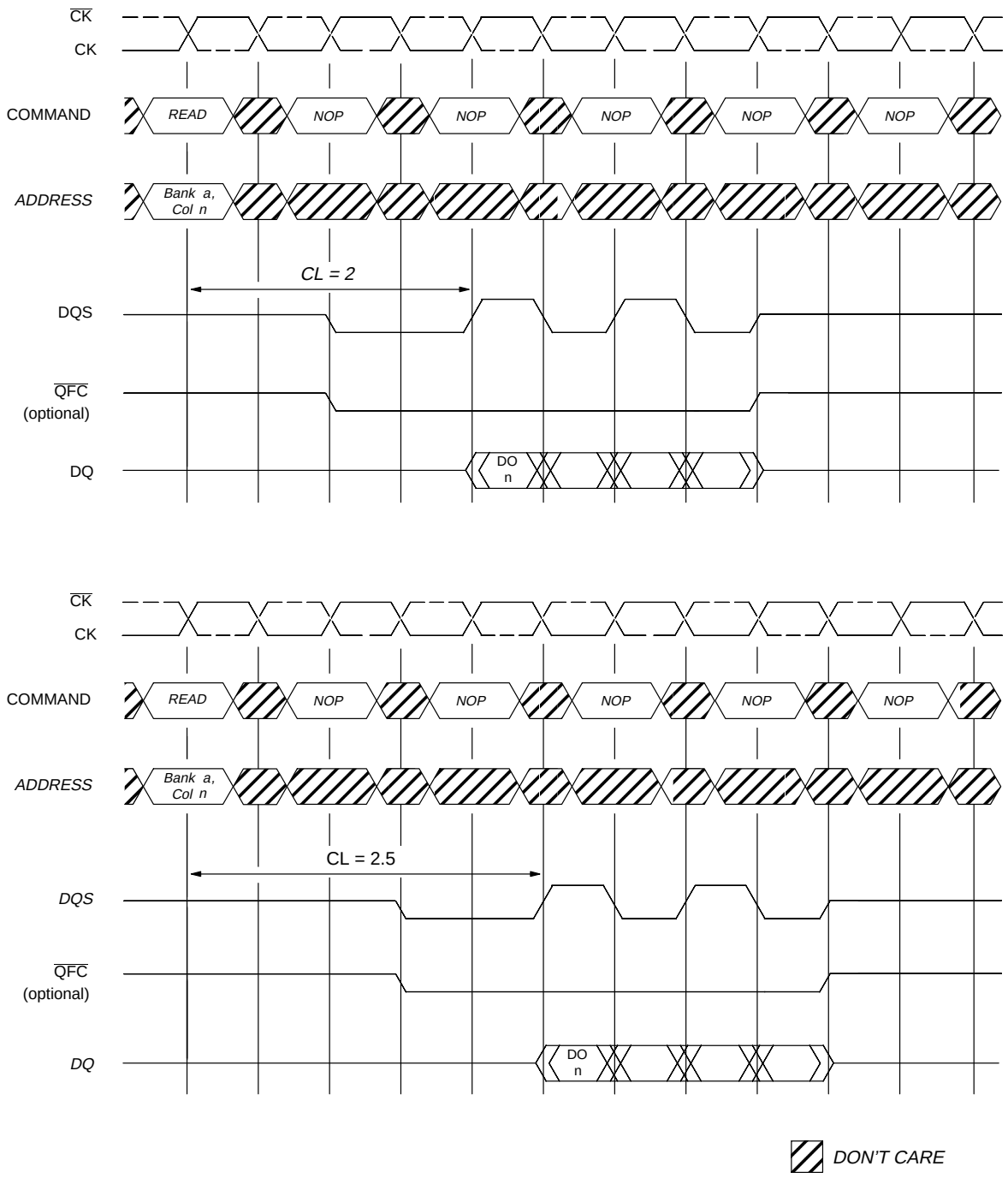
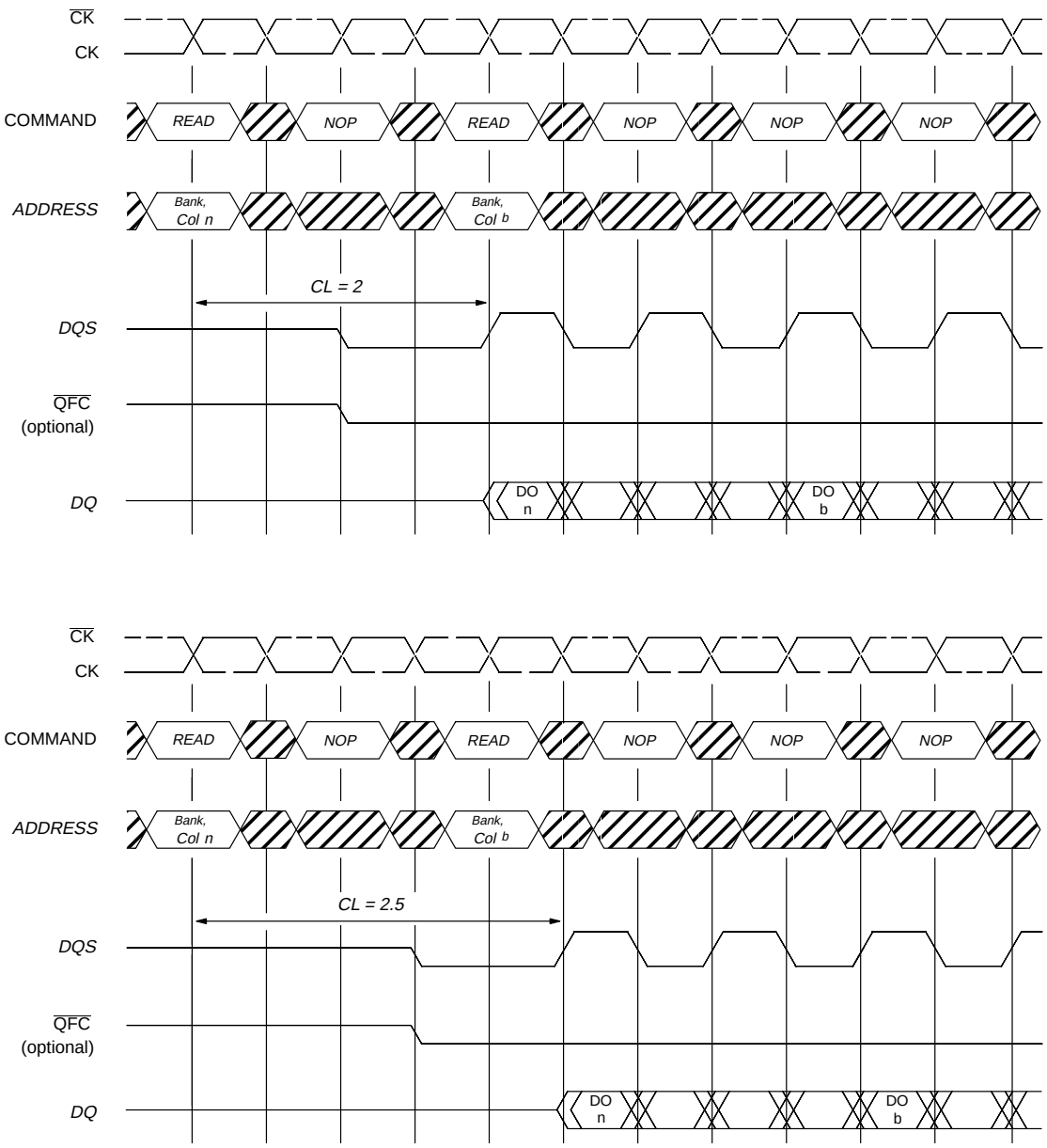


Figure 6
READ COMMAND



DO n = Data Out from column n
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

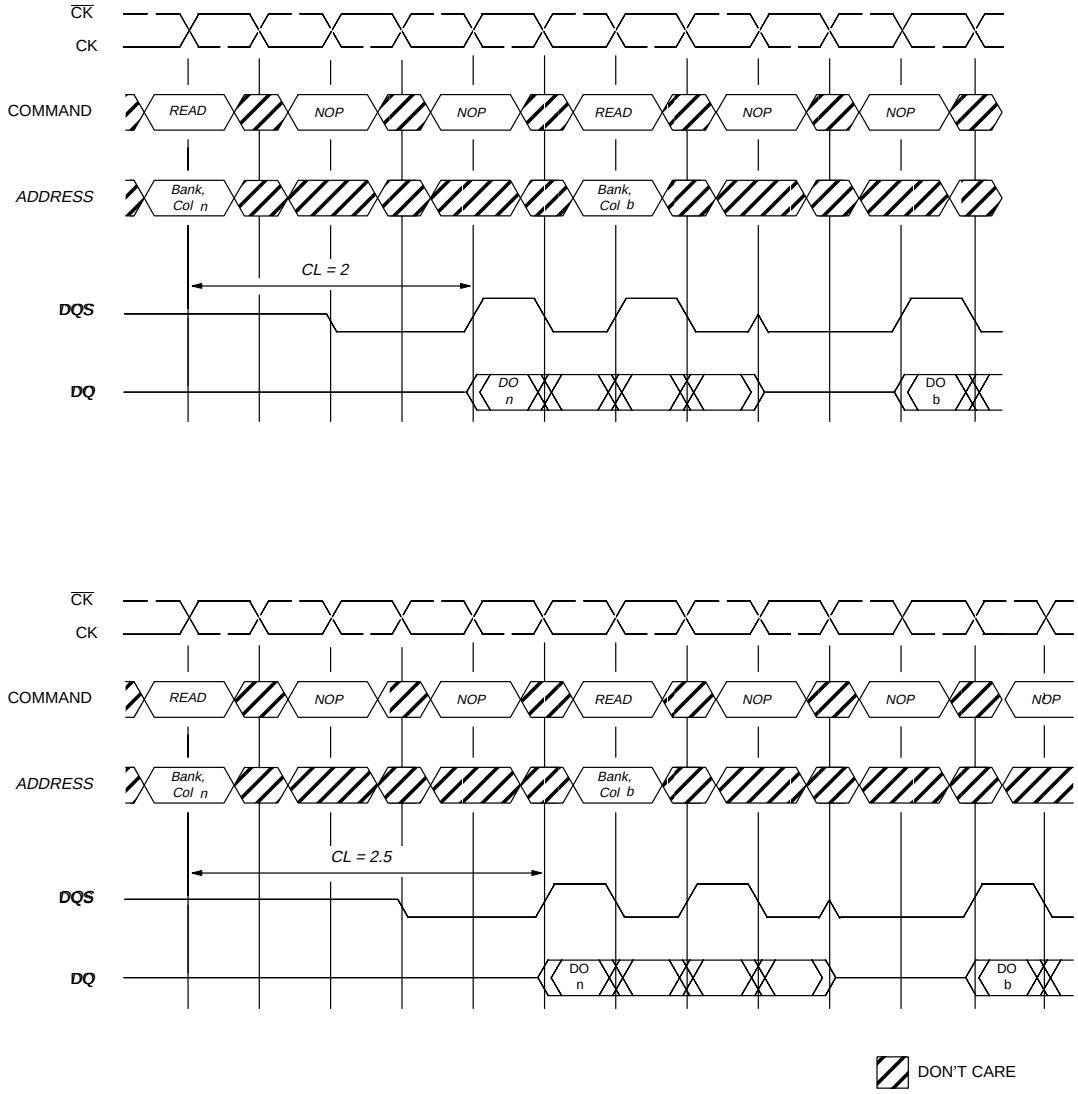
Figure 7
READ BURST – REQUIRED CAS LATENCIES



DON'T CARE

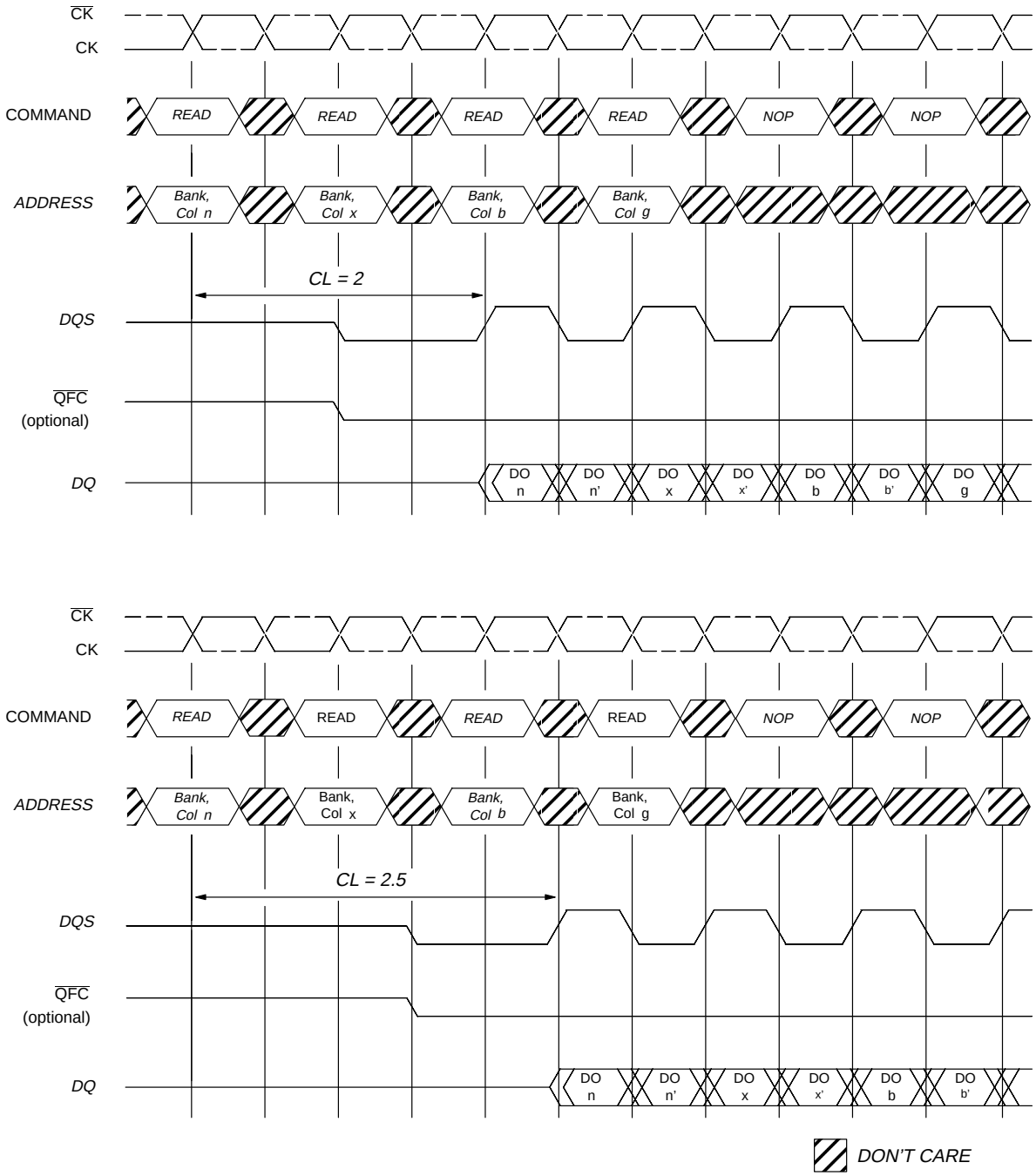
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b
Shown with nominal tDQSCK, and tDQSQ
Read commands shown must be to the same device

Figure 8
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)
Shown with nominal tDQSCK, and tDQSQ

Figure 9
NONCONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n, etc. = Data Out from column n, etc.
n' , etc. = the next Data Out following DO n, etc. according to the programmed burst order
Burst Length = 2, 4 or 8 in cases shown
Reads are to active rows in any banks
Shown with nominal tDQSCK, and tDQSQ

Figure 10
RANDOM READ ACCESSES – REQUIRED CAS LATENCIES

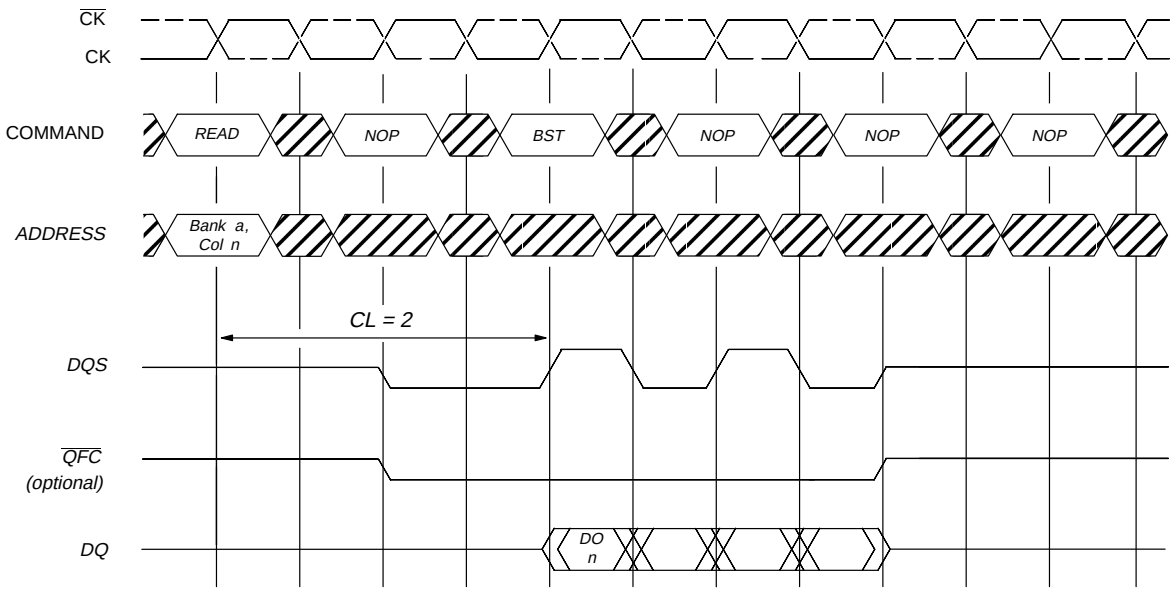
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs.

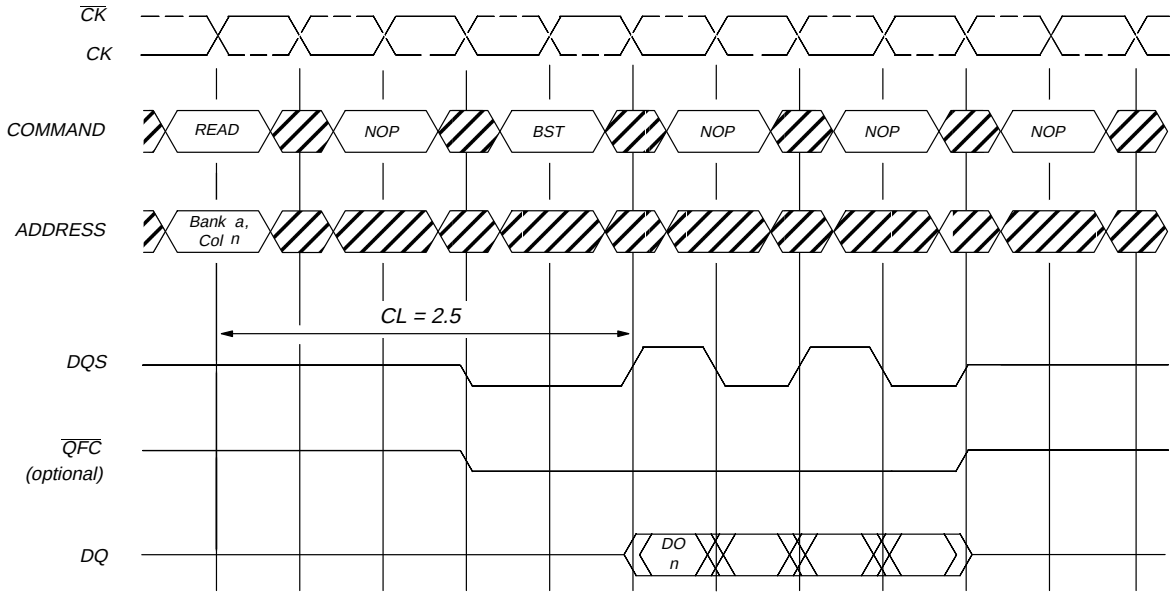
Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued.

If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITEs).

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 13 for READ latencies of 2, and 2.5. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

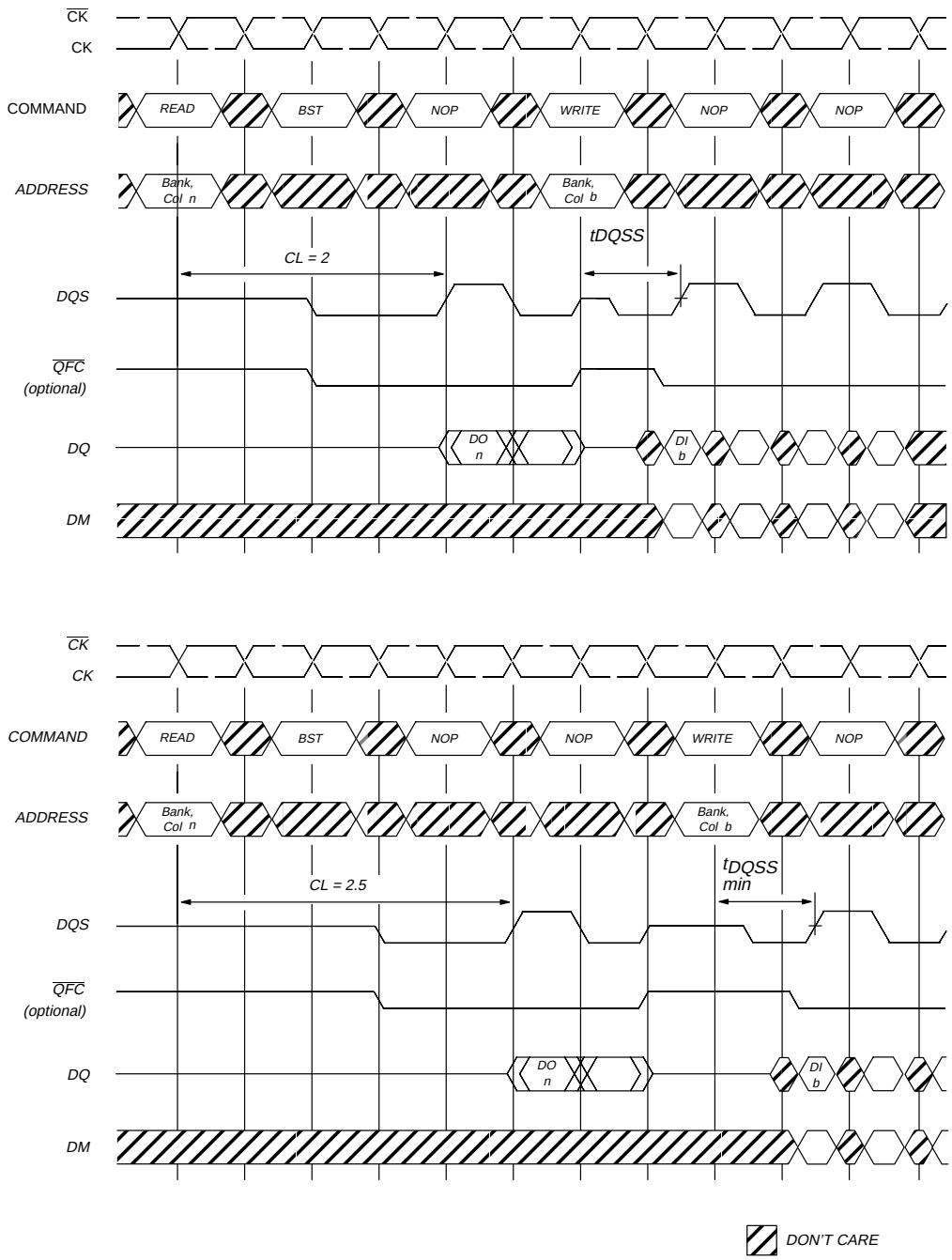
In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.





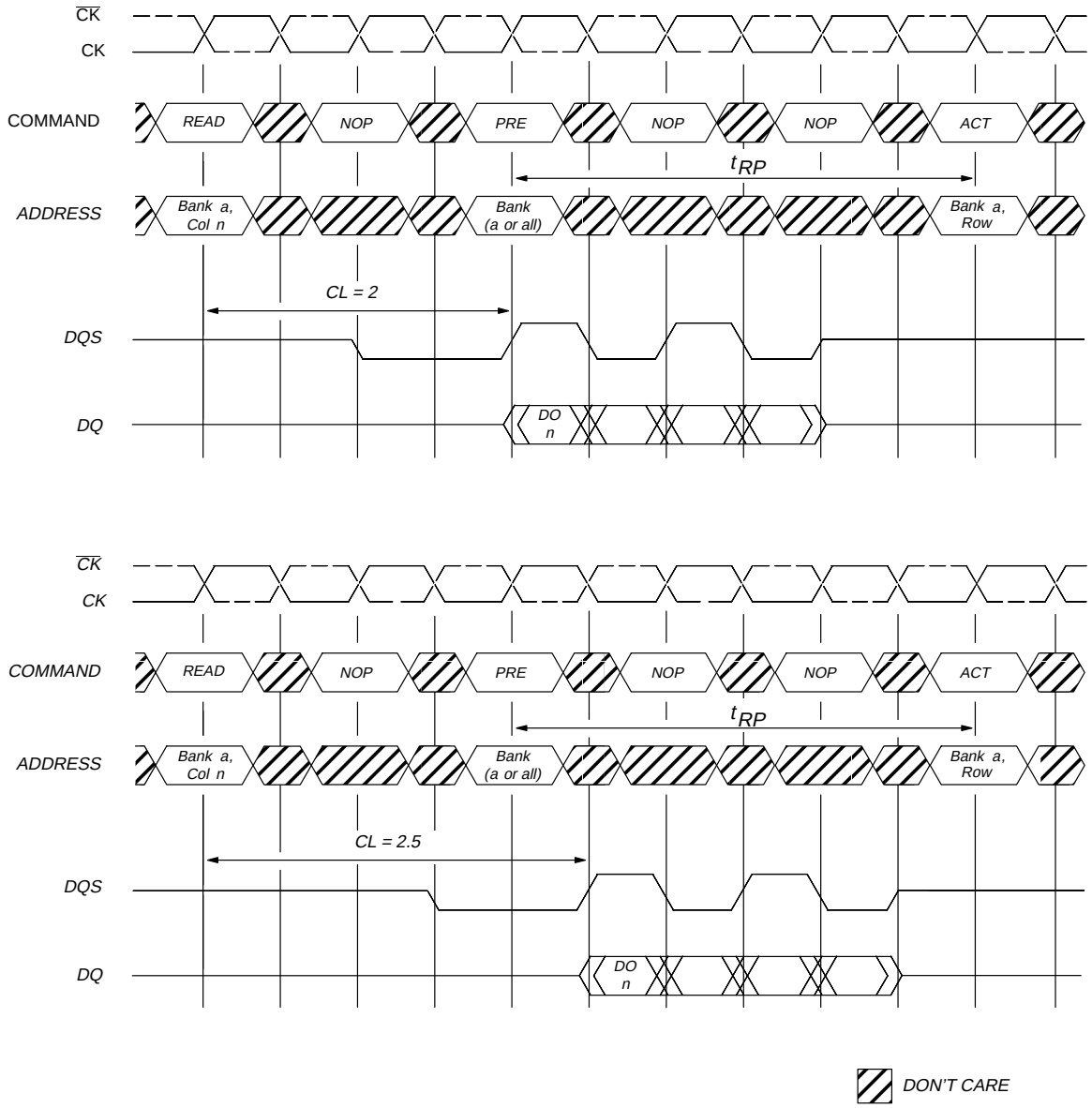
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 11
TERMINATING A READ BURST – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
1 subsequent element of Data Out appears in the programmed order following DO n
Data In elements are applied following DI b in the programmed order
Shown with nominal tDQSCK, and tDQSQ

Figure 12
READ TO WRITE – REQUIRED CAS LATENCIES



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 13
READ TO PRECHARGE – REQUIRED CAS LATENCIES

Writes

WRITE bursts are initiated with a WRITE command, as shown in Figure 14.

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data–in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data–in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle), so most of the WRITE diagrams that follow are drawn for the two extreme cases (i.e., tDQSS MIN and tDQSS MAX). Figures 15 and 16 show the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High–Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figures 17 and 18 show concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 19. Full–speed random write accesses within a page or pages can be performed as shown in Figures 20 and 21.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figures 22 and 23.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 24–27. Note that only the data–in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data–in must be masked with DM, as shown in Figures 24–27.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, tWR should be met as shown in Figures 28 and 29.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 30–33.

Note that only the data–in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data–in should be masked with DM, as shown in Figures 30–33. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

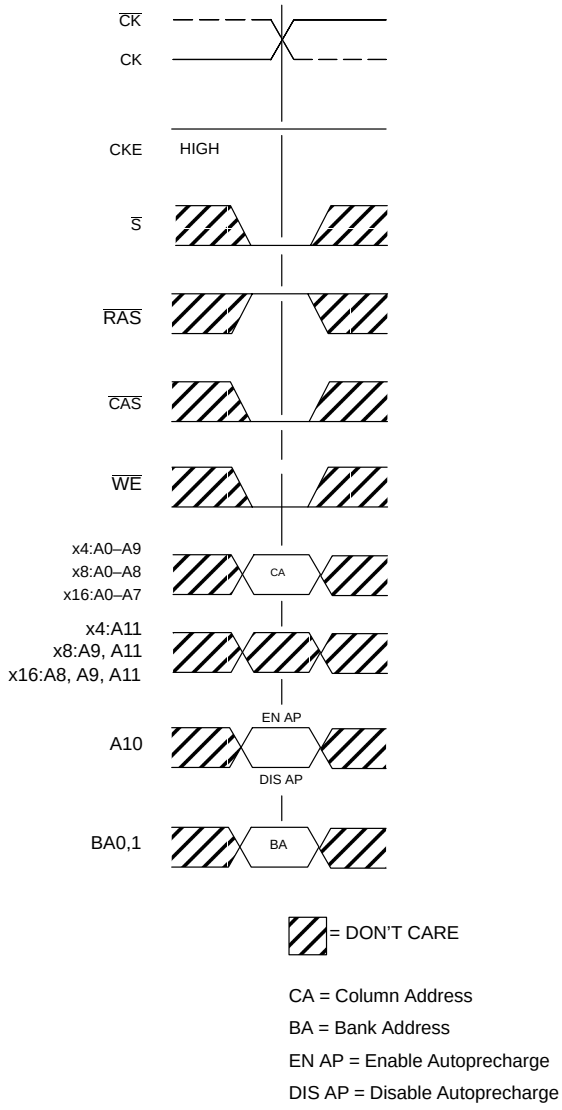
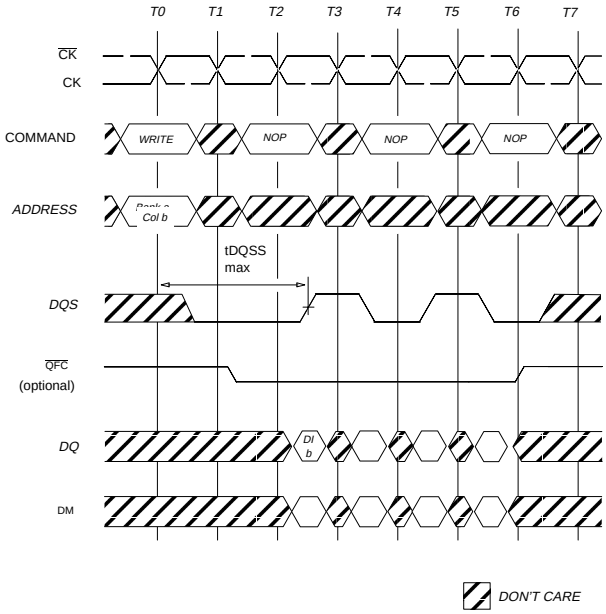
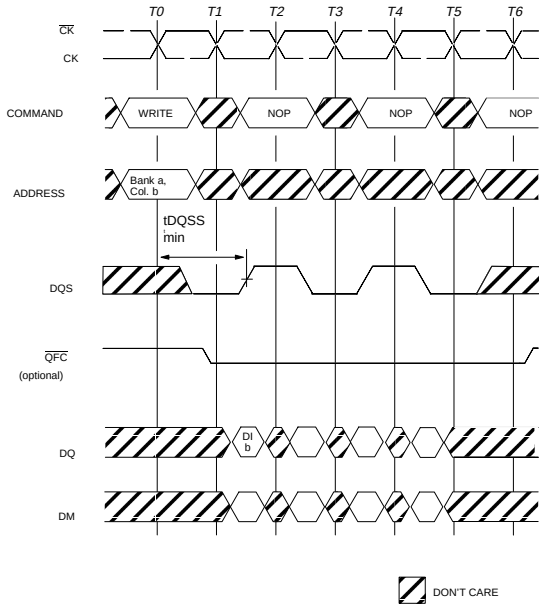


Figure 14
WRITE COMMAND



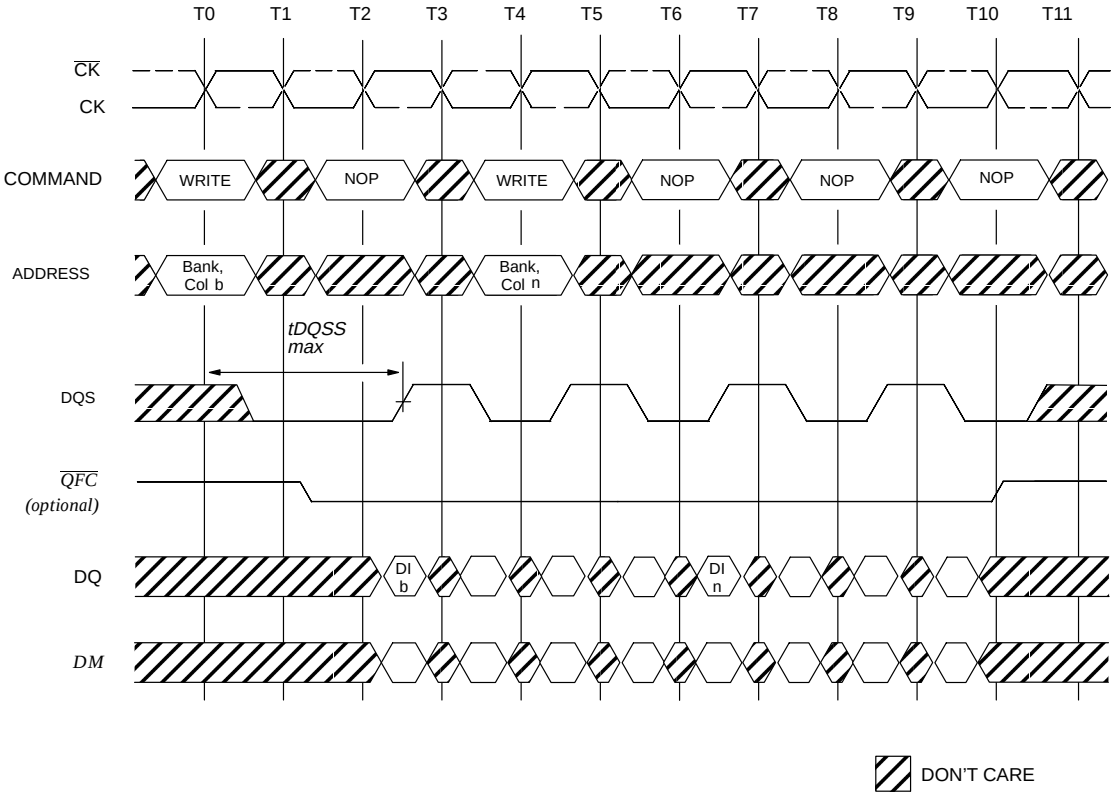
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI
A non–interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 15
WRITE TO WRITE – MAX DQSS



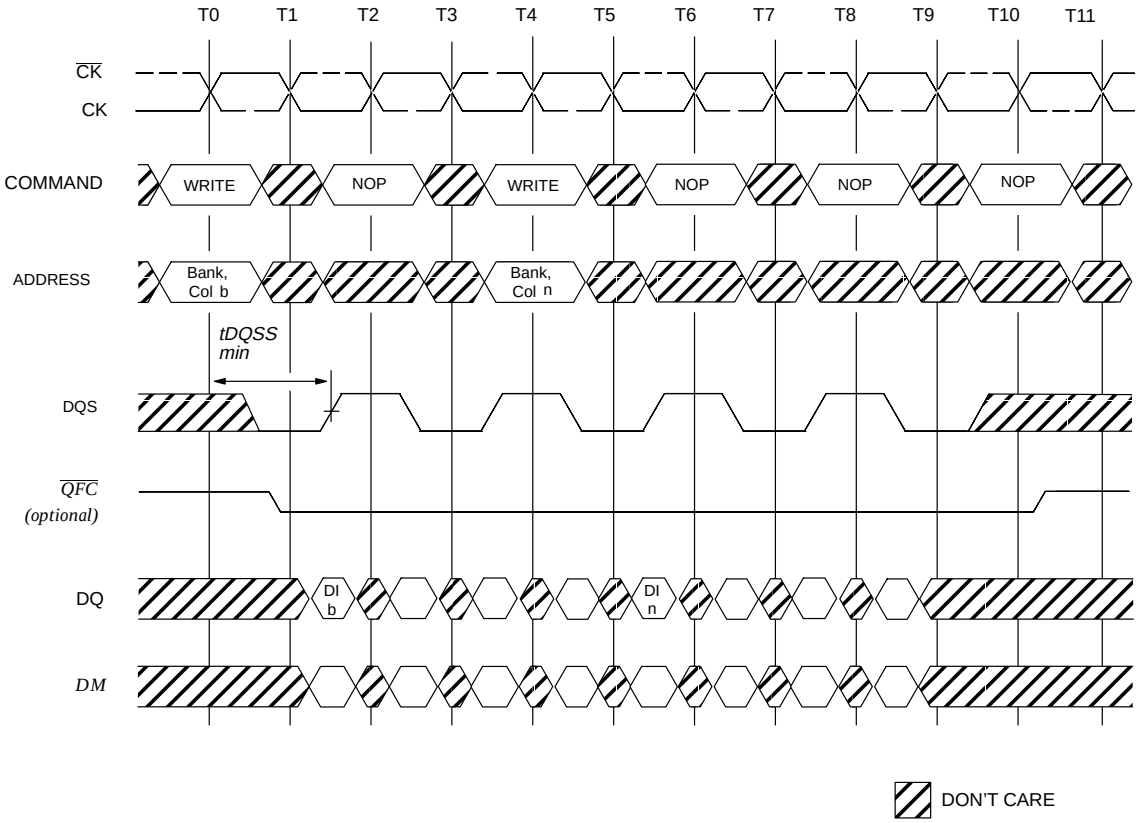
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non–interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 16
WRITE TO WRITE – MIN DQSS



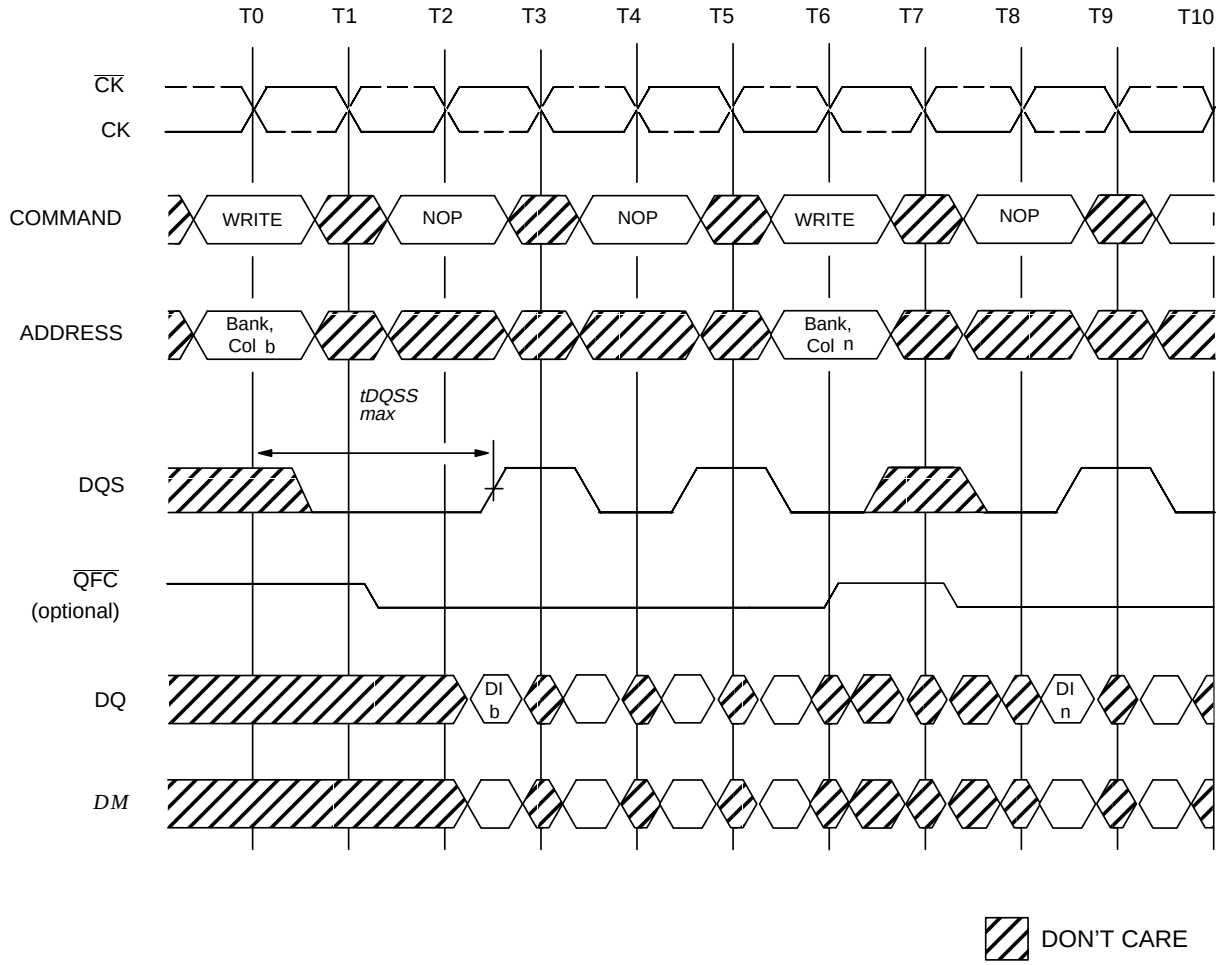
DI b, etc = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)
For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 17
WRITE TO WRITE – MAX DQSS



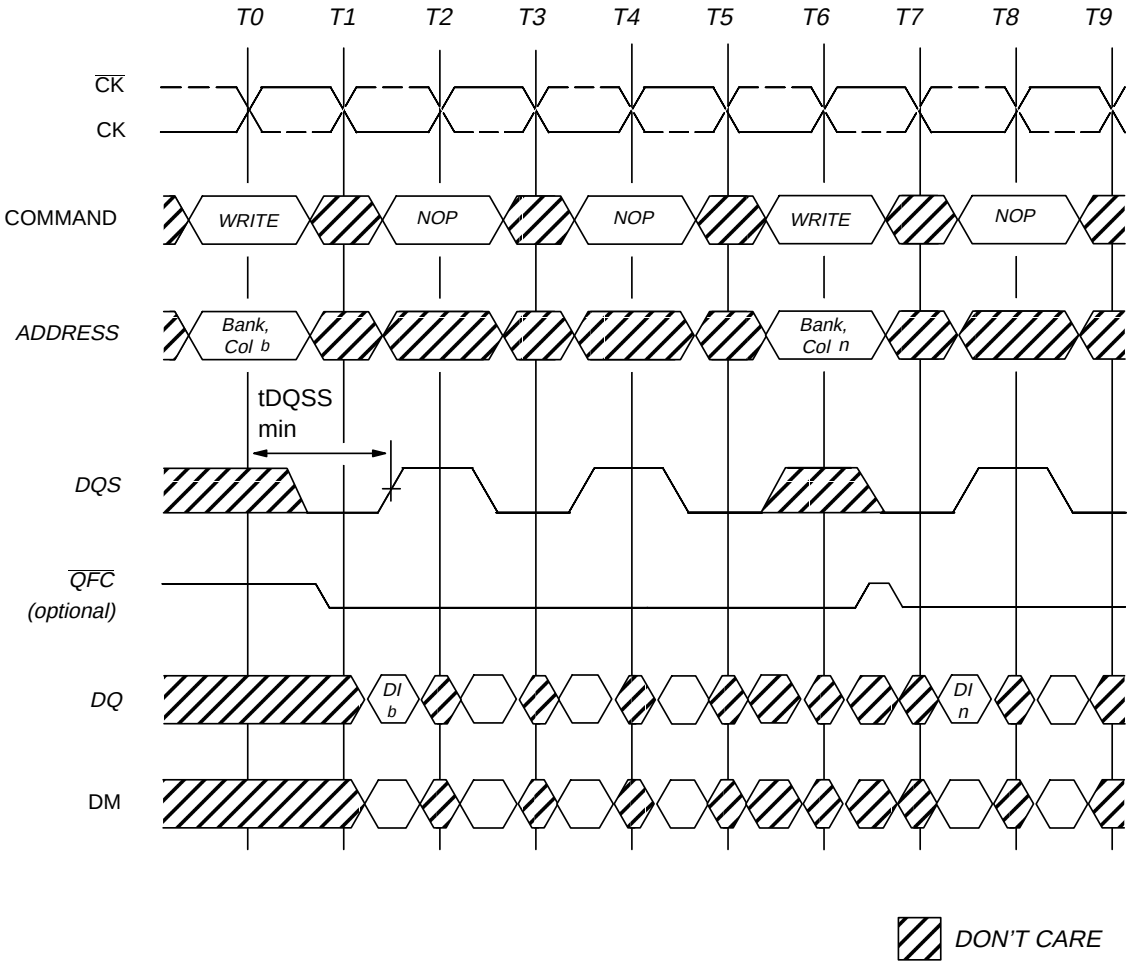
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device
For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 18
WRITE TO WRITE – MIN DQSS,



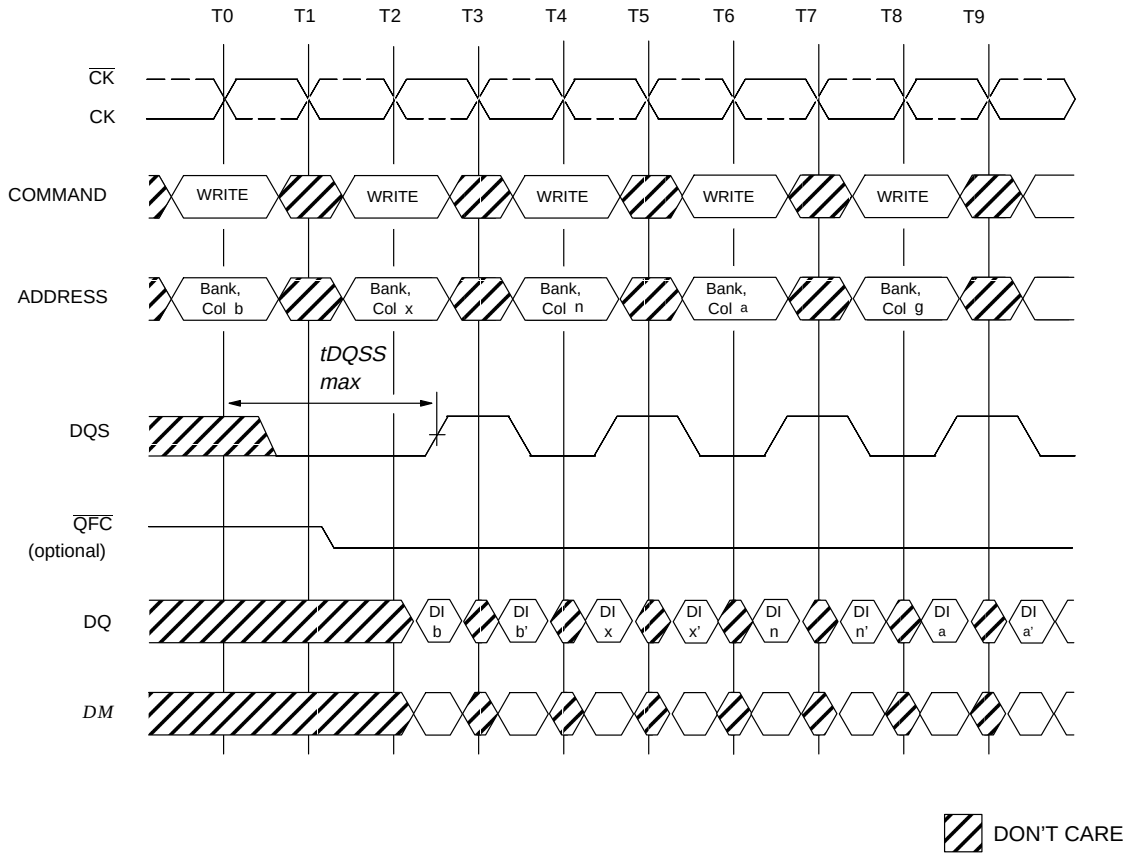
DI b, etc. = Data In for column b, etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
Each Write command may be to any bank and may be to the same or different devices

Figure 19 a
WRITE TO WRITE – MAX DQSS, NONCONSECUTIVE



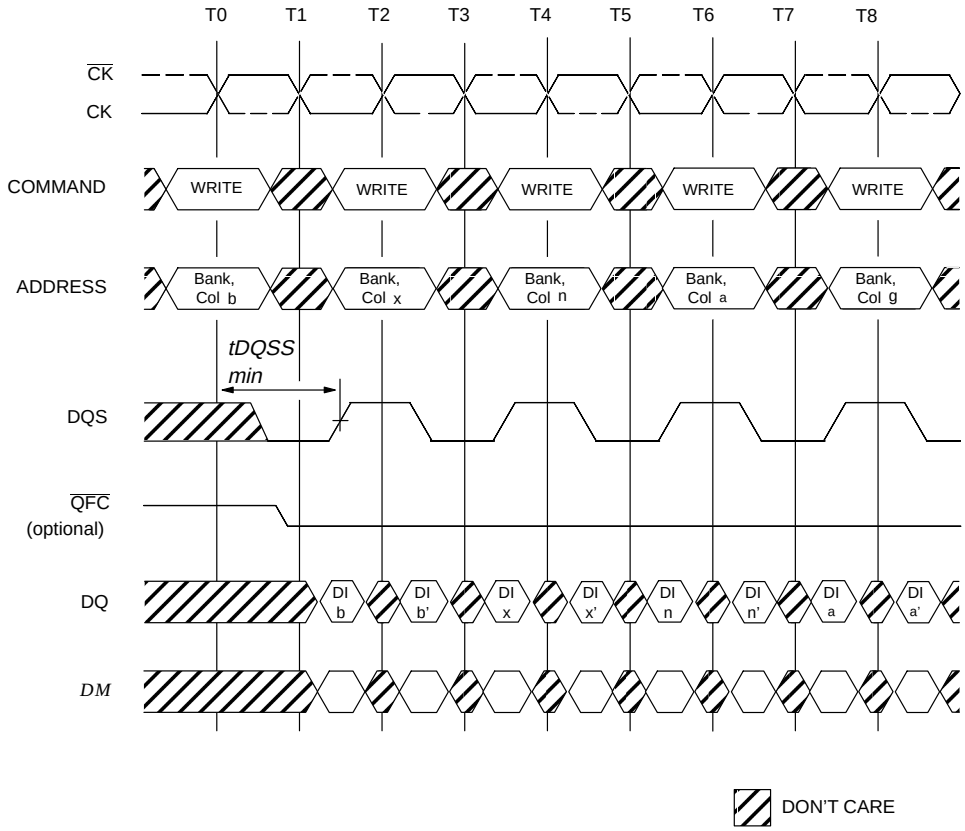
DI b, etc. = Data In for column b. etc.
3 subsequent elements of Data In are applied in the programmed order following DI b
3 subsequent elements of Data In are applied in the programmed order following DI n
A noninterrupted burst of 4 is shown
Each Write command may be to any bank, and may be to the same or different devices
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 19 b
WRITE TO WRITE – MIN DQSS, NONCONSECUTIVE



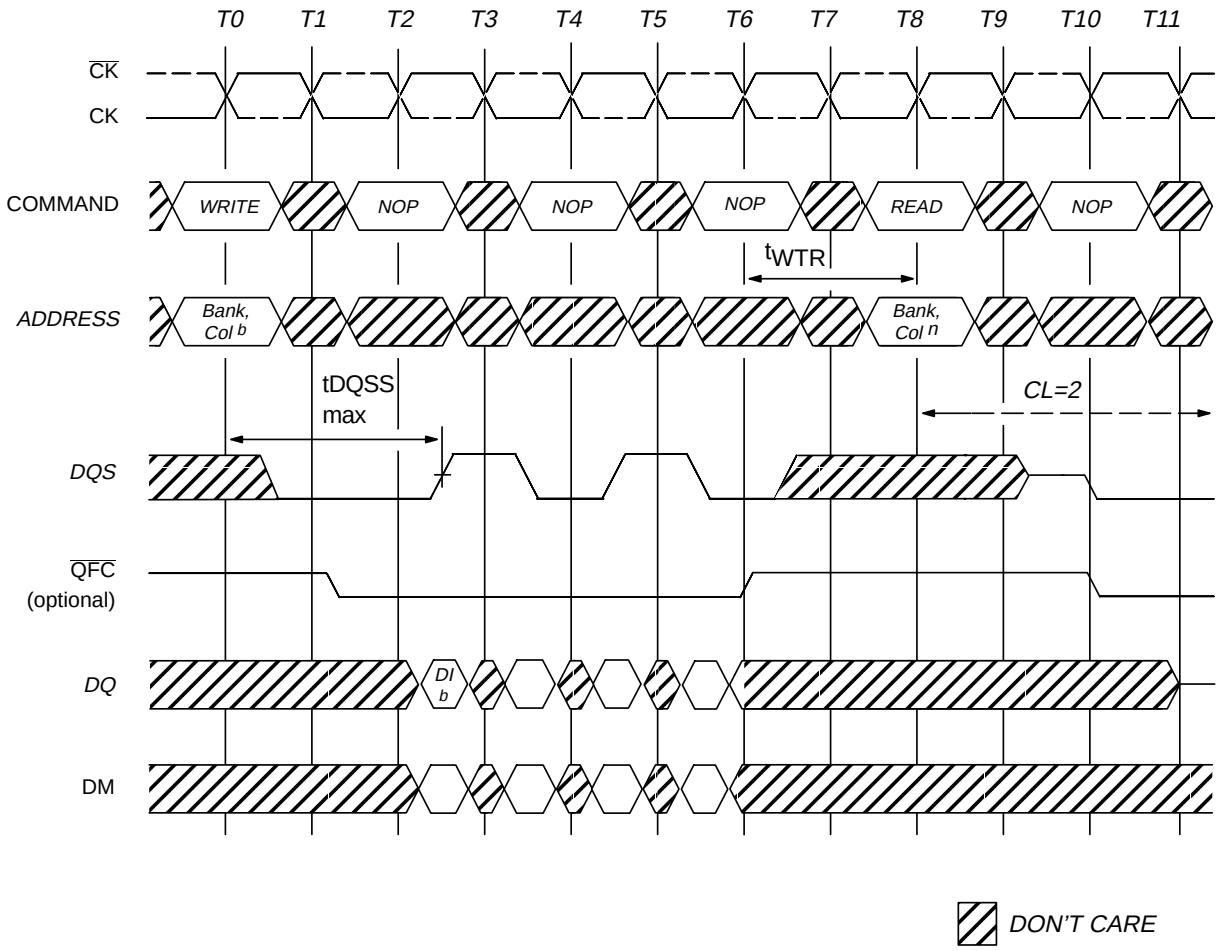
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order
Programmed Burst Length = 2, 4 or 8 in cases shown
For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)
For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 20
RANDOM WRITE CYCLES – MAX DQSS



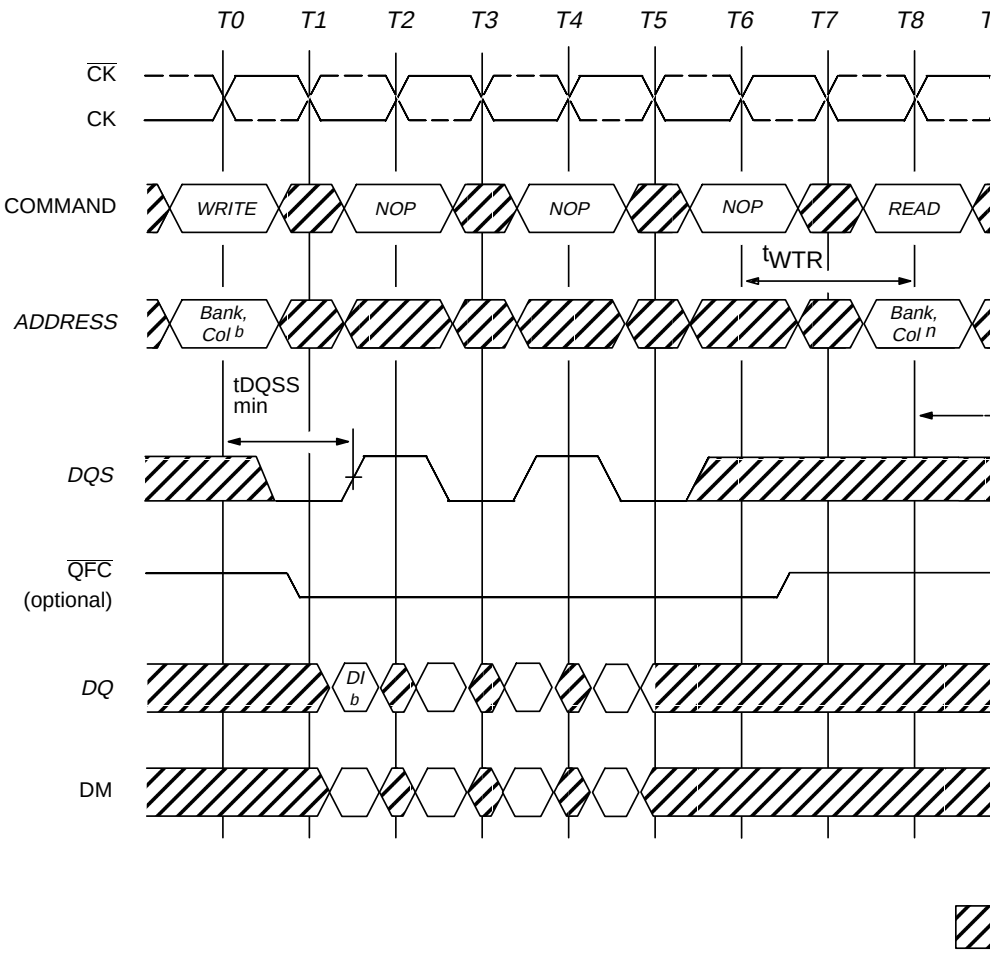
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b , etc., according to the programmed burst order
Programmed Burst Length = 2, 4 or 8 in cases shown
For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device
For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 21
RANDOM WRITE CYCLES – MIN DQSS



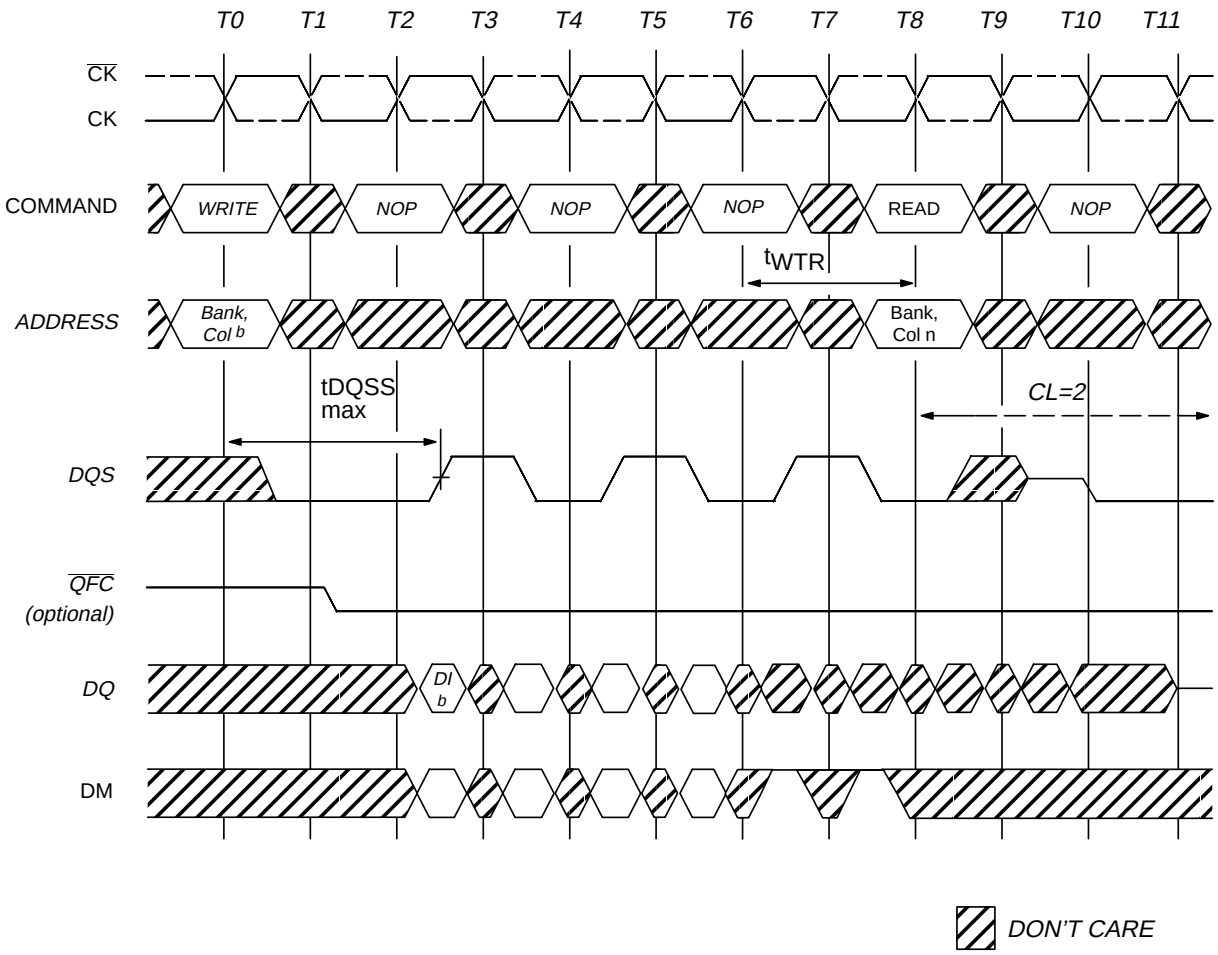
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non–interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands may be to any bank, and may be to the same or different devices
In the case where the READ and WRITE commands are to different devices, tWTR need not be met, and the READ command can be applied earlier
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)

Figure 22
WRITE TO READ – MAX DQSS, NONINTERRUPTING



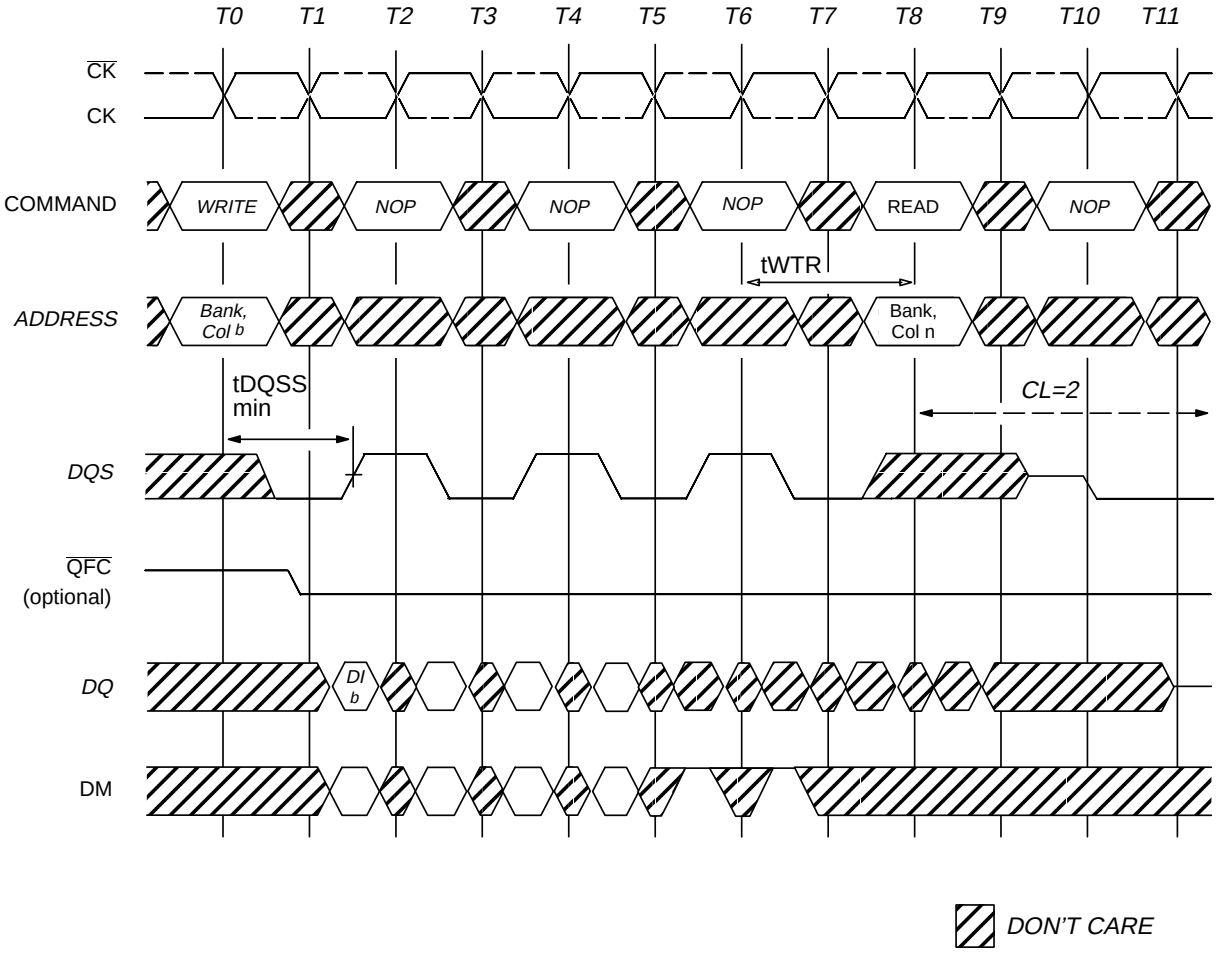
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following D
A non–interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands may be to any bank, and may be to the same o
In the case where the READ and WRITE commands are to different devices, tWTR
and the READ command can be applied earlier
tWTR = 2 tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be p
at the maximum operating frequency of the device

Figure 23
WRITE TO READ – MIN DQSS, NON–INTERRUPTING



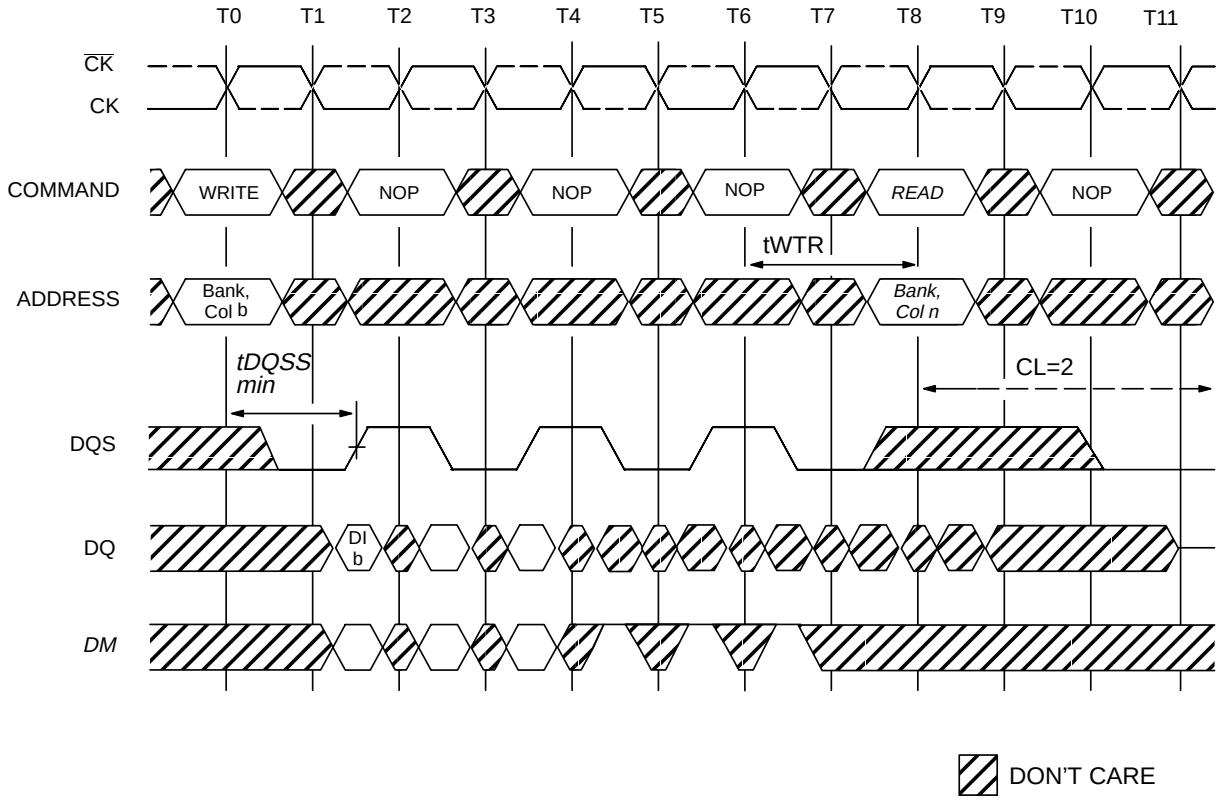
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank

Figure 24
WRITE TO READ – MAX DQSS, INTERRUPTING



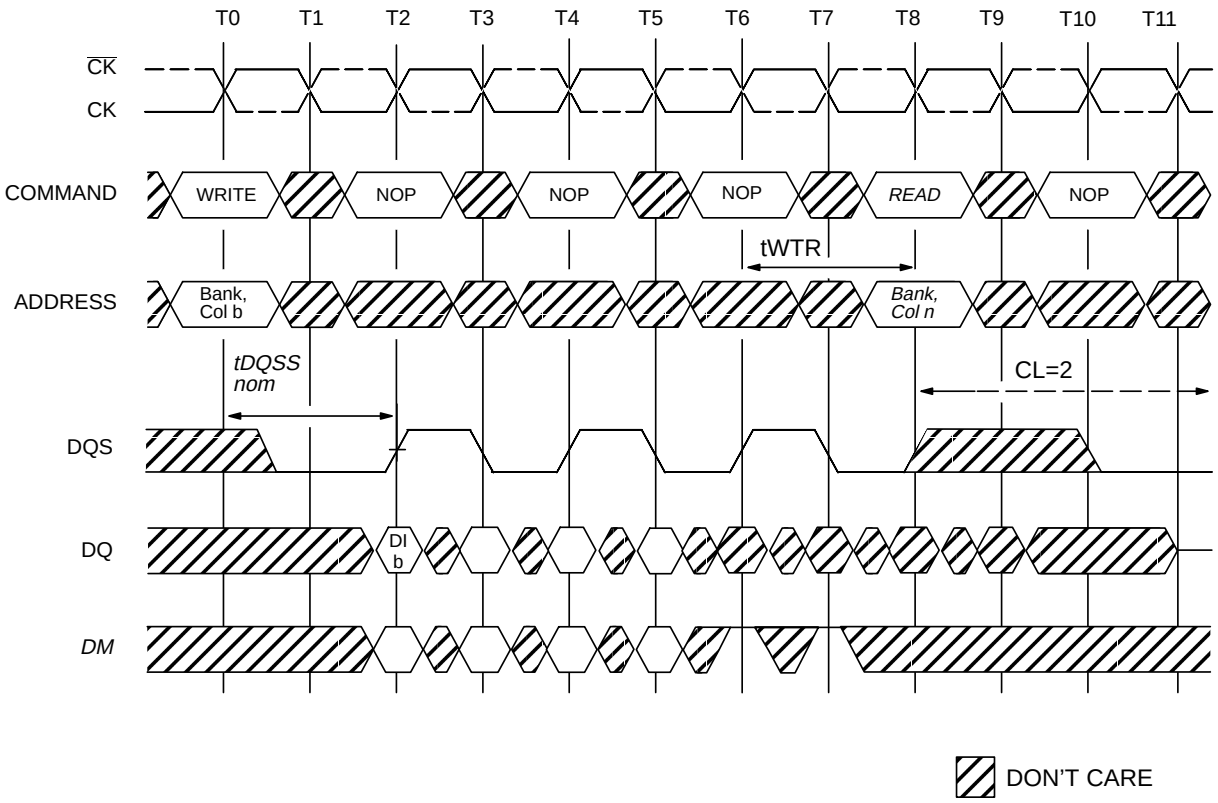
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last desired Data In pair
tWTR = 2 tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device, but not necessarily to the same bank
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 25
WRITE TO READ – MIN DQSS, INTERRUPTING



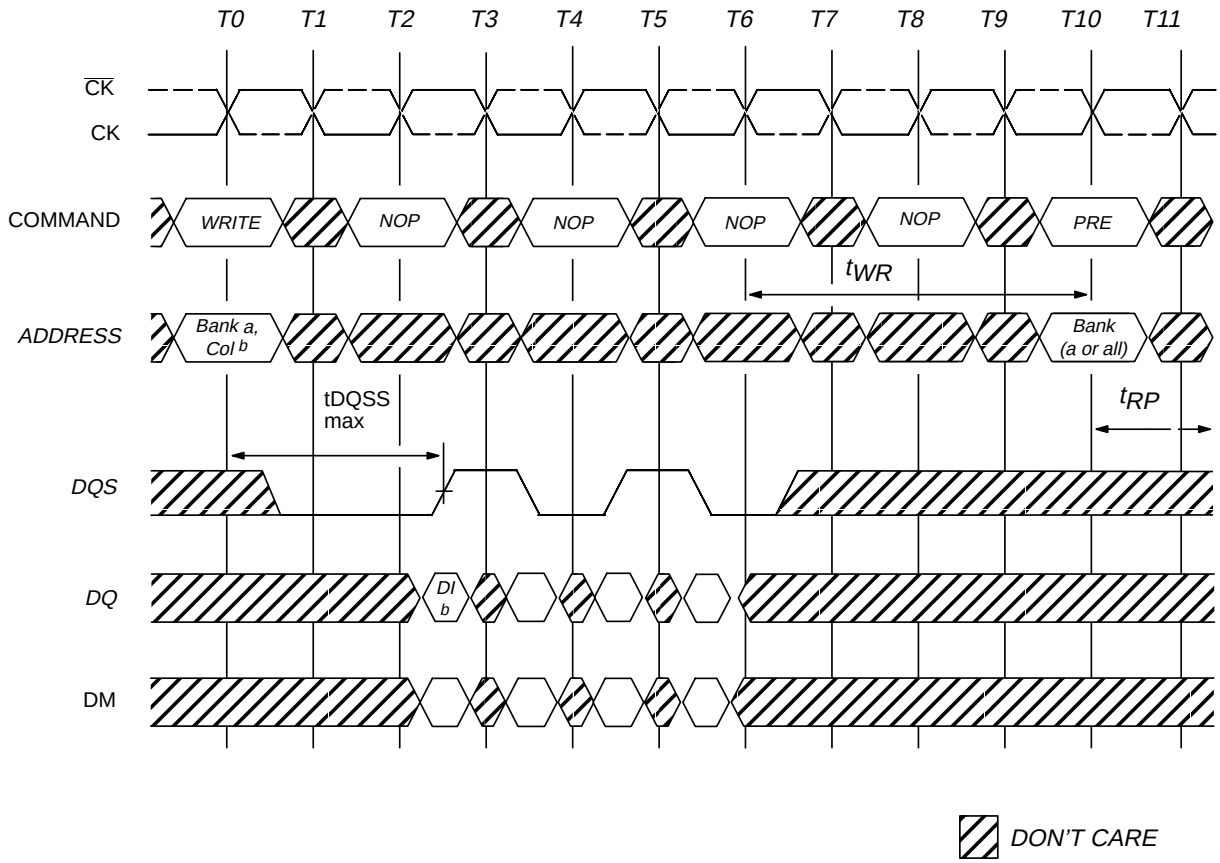
DI b = Data In for column b
An interrupted burst of 8 is shown, 3 data elements are written
2 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last desired Data In pair (not the last desired data in element)
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 26
WRITE TO READ – MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



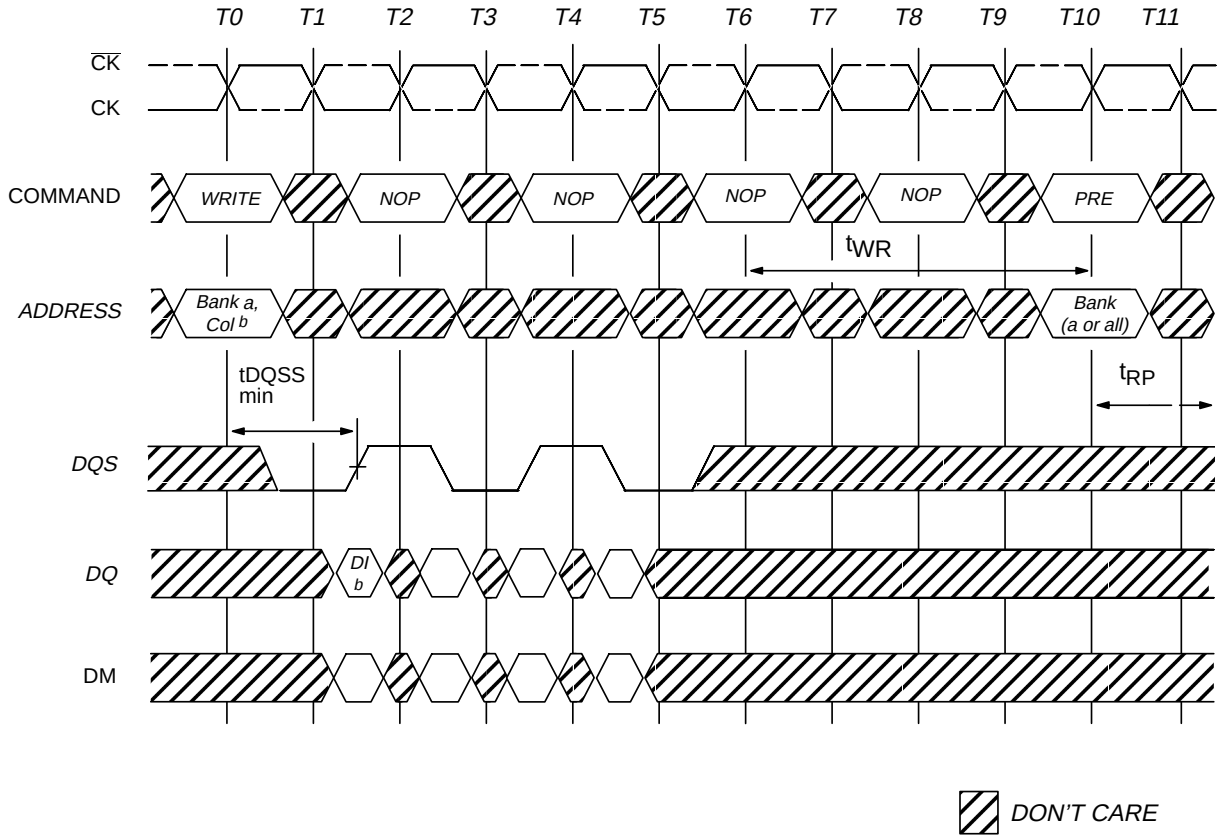
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
3 subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last desired Data In pair
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)
The READ command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are not necessarily to the same bank

Figure 27
WRITE TO READ – NOMINAL DQSS, INTERRUPTING



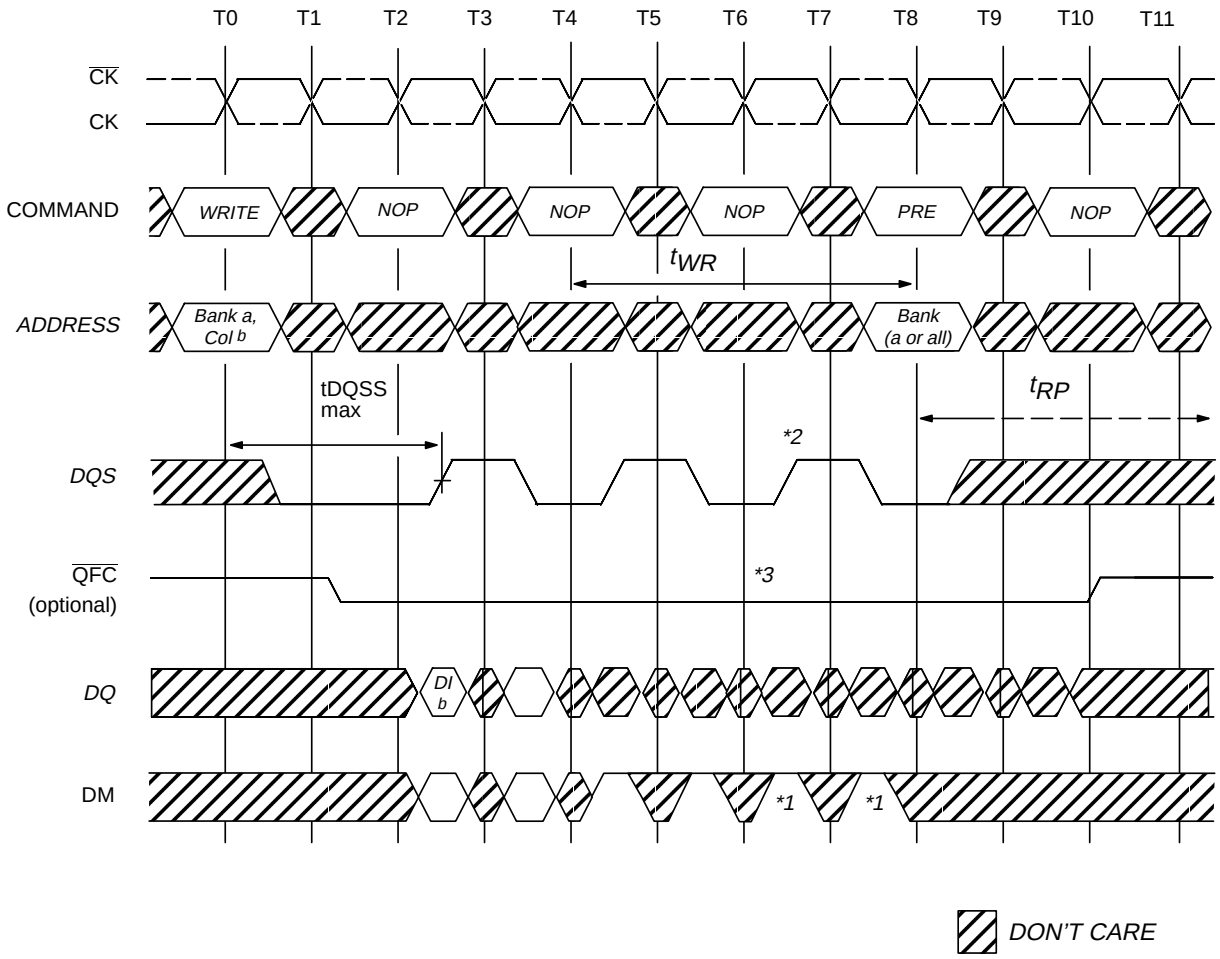
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A noninterrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 28
WRITE TO PRECHARGE – MAX DQSS, NON–INTERRUPTING



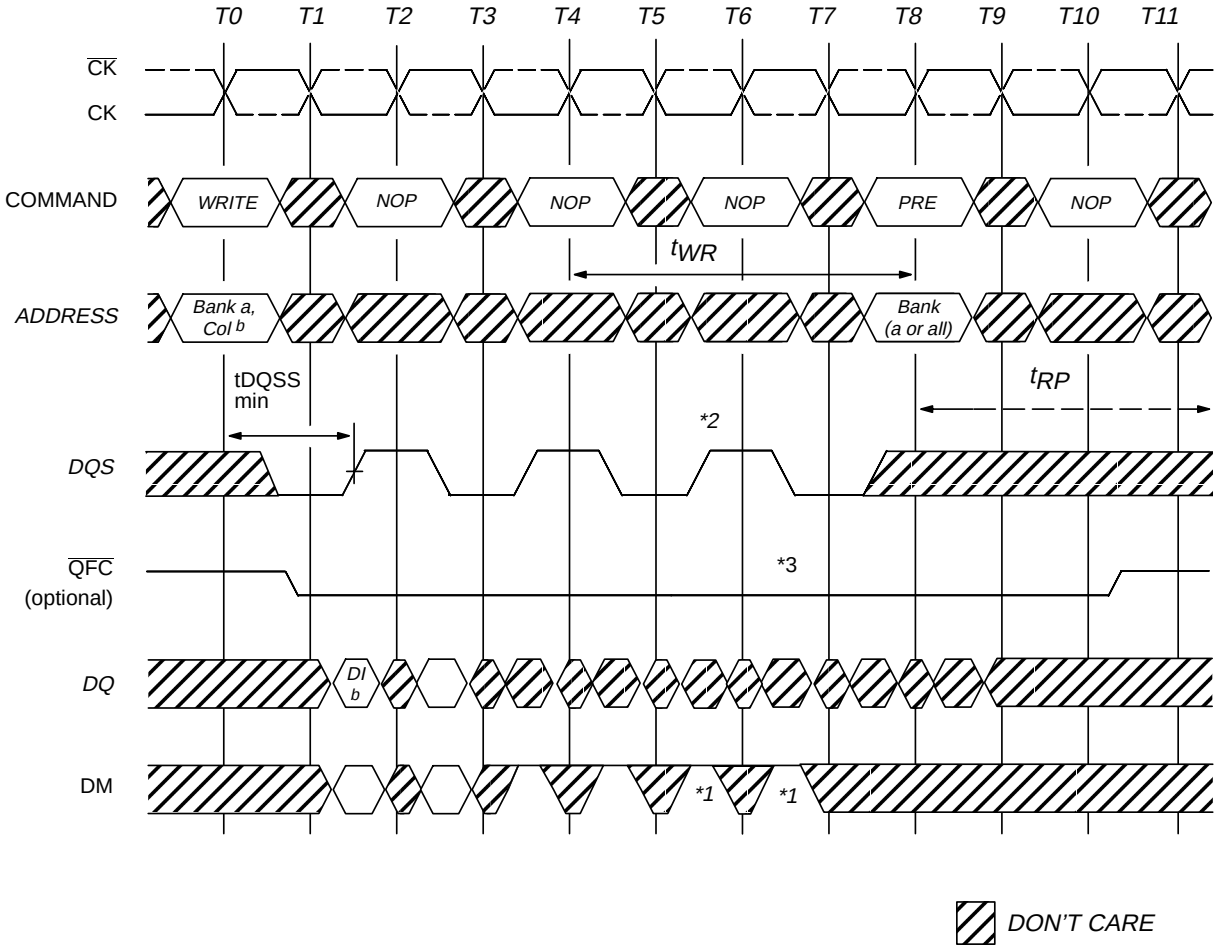
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A noninterrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 29
WRITE TO PRECHARGE – MIN DQSS, NON–INTERRUPTING



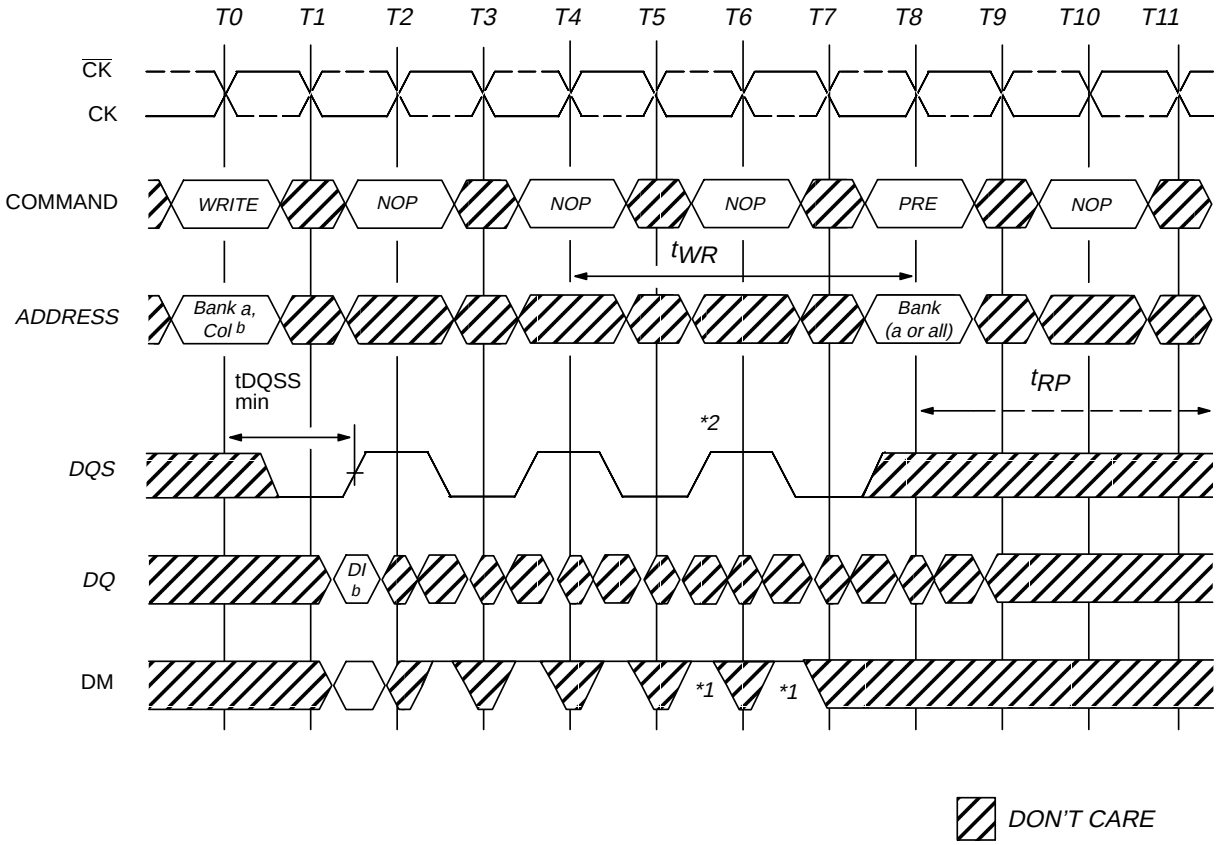
DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
**1 = can be don't care for programmed burst length of 4*
**2 = for programmed burst length of 4, DQS becomes don't care at this point*
**3 = for programmed burst length of 4, $\overline{QFC}$ becomes High–Z at this point*

Figure 30
WRITE TO PRECHARGE – MAX DQSS, INTERRUPTING



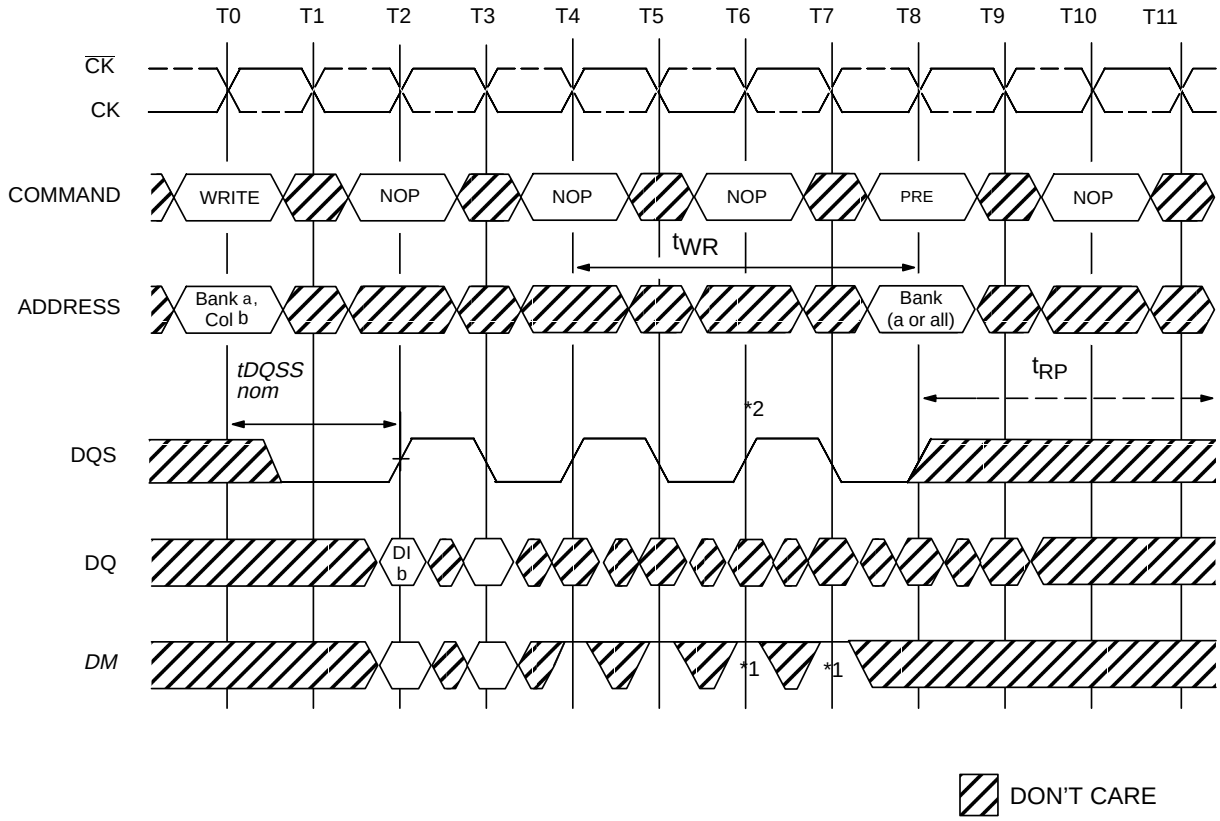
DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
**1 = can be don't care for programmed burst length of 4*
**2 = for programmed burst length of 4, DQS becomes don't care at this point*
**3 = for programmed burst length of 4, $\overline{QFC}$ becomes High–Z at this point*
Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 31
WRITE TO PRECHARGE – MIN DQSS, INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
**1 = can be don't care for programmed burst length of 4*
**2 = for programmed burst length of 4, DQS becomes don't care at this point*

Figure 32
WRITE TO PRECHARGE – MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWR is referenced from the first positive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point

Figure 33
WRITE TO PRECHARGE – NOMINAL DQSS, INTERRUPTING

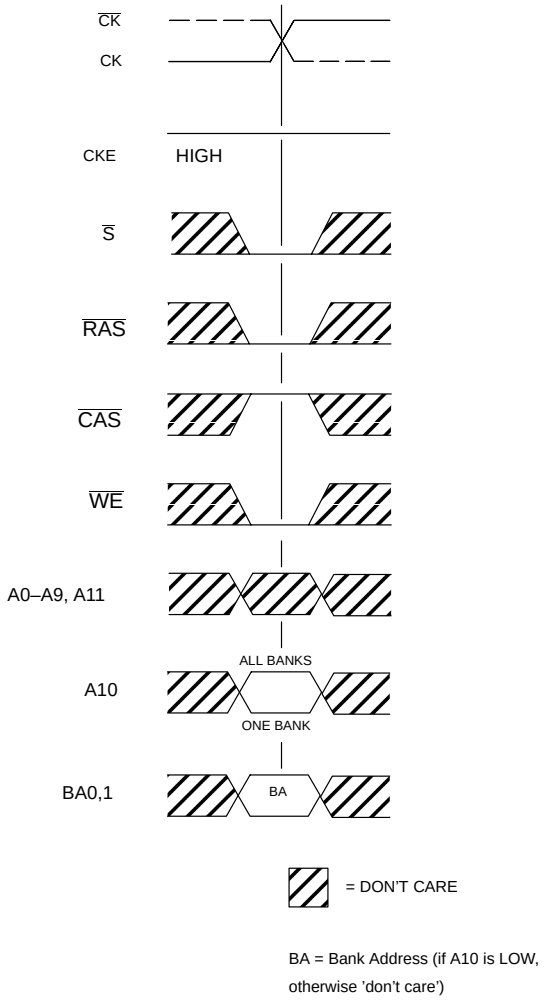


Figure 34
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as ”Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER–DOWN

Power–down is entered when CKE is registered low (no accesses can be in progress). If power–down occurs when all banks are idle, this mode is referred to as precharge power–down; if power–down occurs when there is a row active in any bank, this mode is referred to as active power–down. Entering power–down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power–down. In that case, the DLL must be enabled after exiting power–down, and 200 clock cycles must occur before a READ command can be issued. However, power–down duration is limited by the refresh requirements of the device, so in most applications, the self–refresh mode is preferred over the DLL–disabled power–down mode.

In power–down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are ”Don’t Care”.

The power–down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

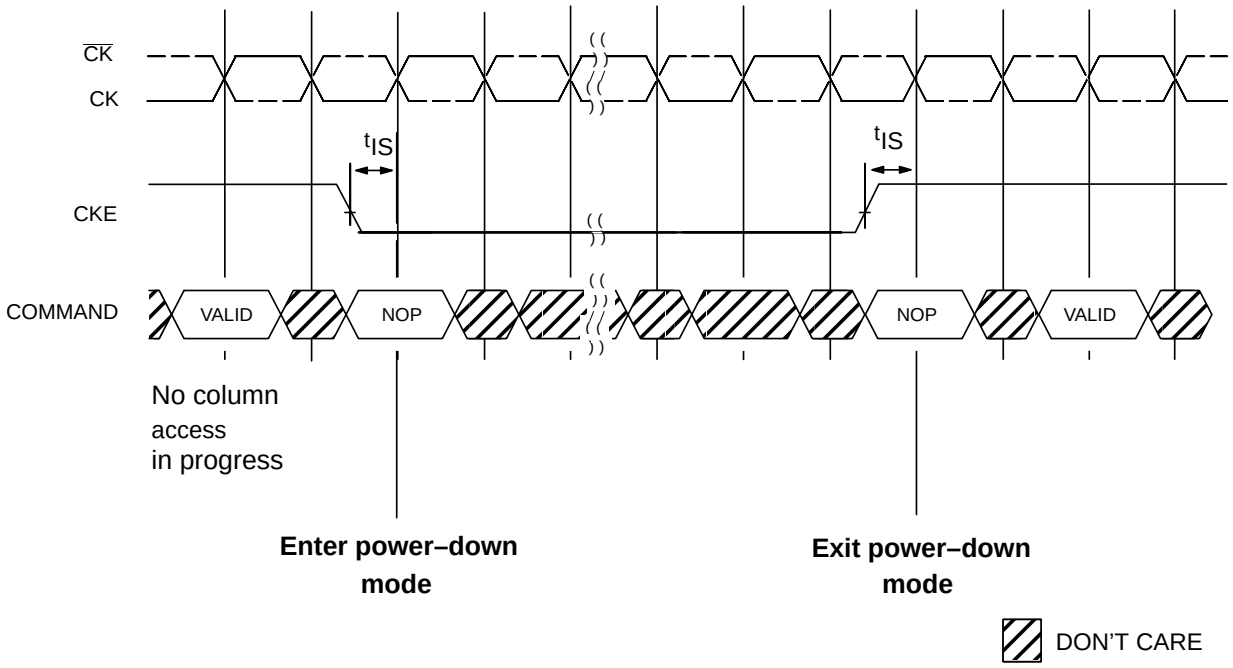


Figure 35
POWER–DOWN

(Notes: 1–4)

TRUTH TABLE 2 – CKE

CKEn–1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power–Down	X	Maintain Power–Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power–Down	DESELECT or NOP	Exit Power–Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power–Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power–Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn–1 was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.

4. All states and sequences not shown are illegal or reserved.

5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3 – Current State Bank n – Command to Bank n

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION(NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table is bank–specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

   Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the ”row active” state.

   Read w/Auto–Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE eabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

   Write w/Auto–Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the ”all banks idle” state.

   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMTC is met, the DDR SDRAM will be in the ”all banks idle” state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank–specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank–specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank–specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.

TRUTH TABLE 4 – Current State Bank n – Command to Bank m

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto–Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	L	H	L	PRECHARGE	
Write (Auto–Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto–Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto–Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst) 3a,	7
	L	H	L	L	WRITE (select column and start new WRITE burst) 3a,	7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

NOTE: (continued)

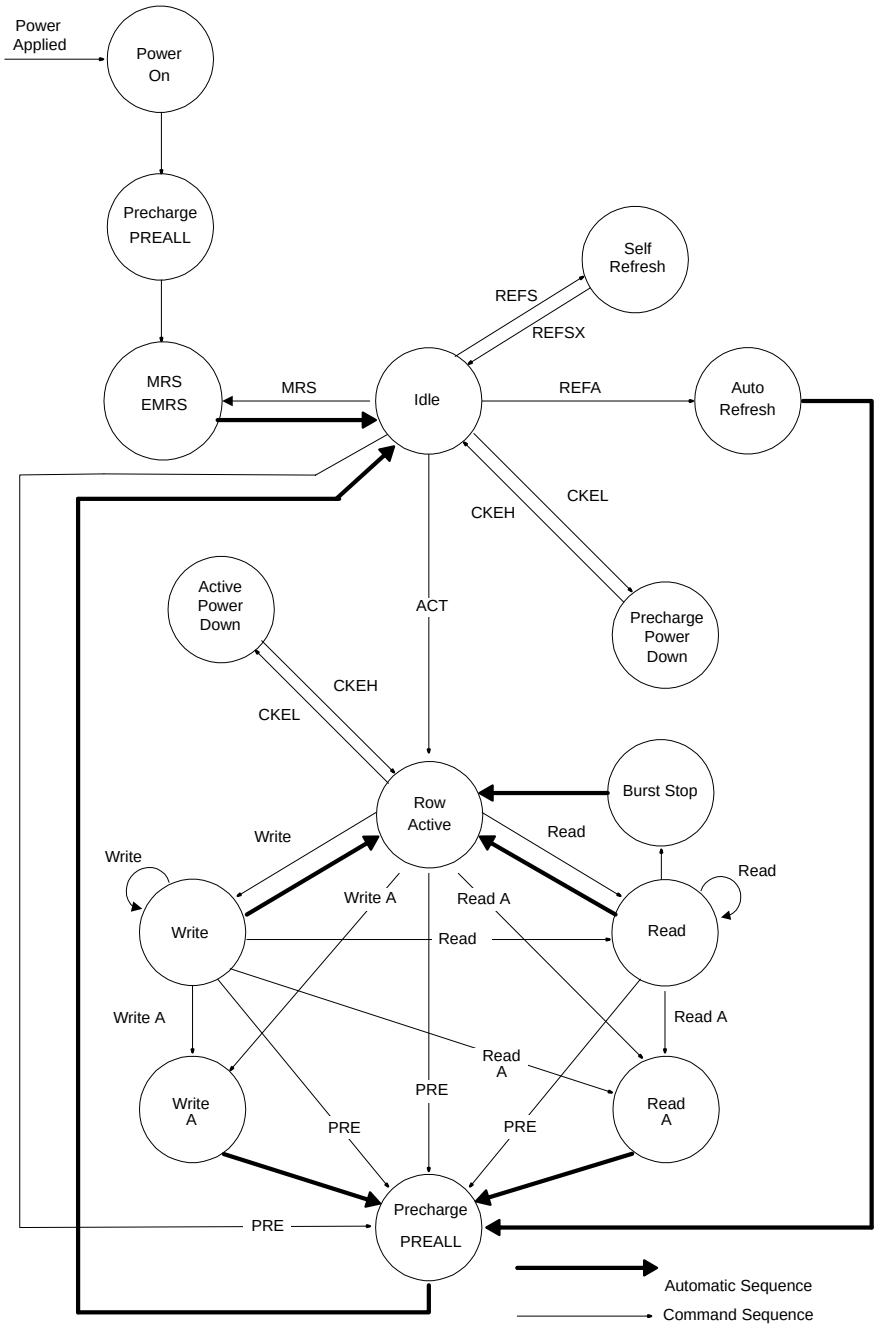
3. Current state definitions:

Idle:	The bank has been precharged, and tRP has been met.
Row Active:	A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
Read with Auto Precharge Enabled:	See following text
Write with Auto Precharge Enabled:	See following text

3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHAGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output.

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vdd Supply (For devices with nominal Vdd of 3.3 V)
Relative to Vss –1 V to +4.6 V
Voltage on Vdd Supply (For devices with nominal Vdd of 2.5 V)
Relative to Vss –1 V to +3.6 V
Voltage on VddQ Supply
Relative to Vss –1 V to +3.6 V
Voltage on Inputs
Relative to Vss –1 V to +3.6 V
Voltage on I/O Pins
Relative to Vss –0.5 V to VddQ+0.5 V

Operating Temperature, TA (ambient)	0 °C to +70 °C
Storage Temperature (plastic)	–55 °C to +150 °C
Power Dissipation	1 W
Short Circuit Output Current	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance:CK, $\overline{CK}$	Ci1	2.5	3.5	pF	13
Input Capacitance: All other input–only pins	Ci2	2.5	3.5	pF	13
Input/Output Capacitance: DQ, DQS, DM	Cio	4.0	5.0	pF	13
Delta Input/Output Capacitance: DQ, DQS, DM	Cdio	–	0.5	pF	13
Output Capacitance: ($\overline{QFC}$)	Co	TBD	TBD	pF	13

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.18	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	–0.3	VREF–0.18	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN(DC)	–0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	8
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	II	–2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	–5	5	µA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	 IOH IOL	 –15.2 15.2		 mA mA	

1) The full variation in driver pulldown current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of Figure a.
2) It is recommended that the ”typical” IBIS pulldown V–I curve lie within the shaded region of the V–I curve of Figure a.

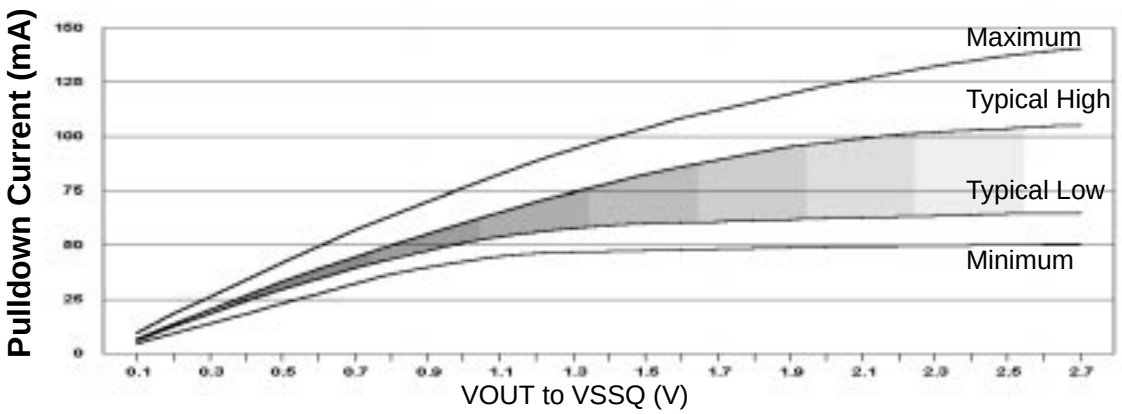


Figure a: Pulldown Characteristics

3) The full variation in driver pullup current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of Figure b.
4) It is recommended that the ”typical” IBIS pullup V–I curve lie within the shaded region of the V–I curve of Figure b.

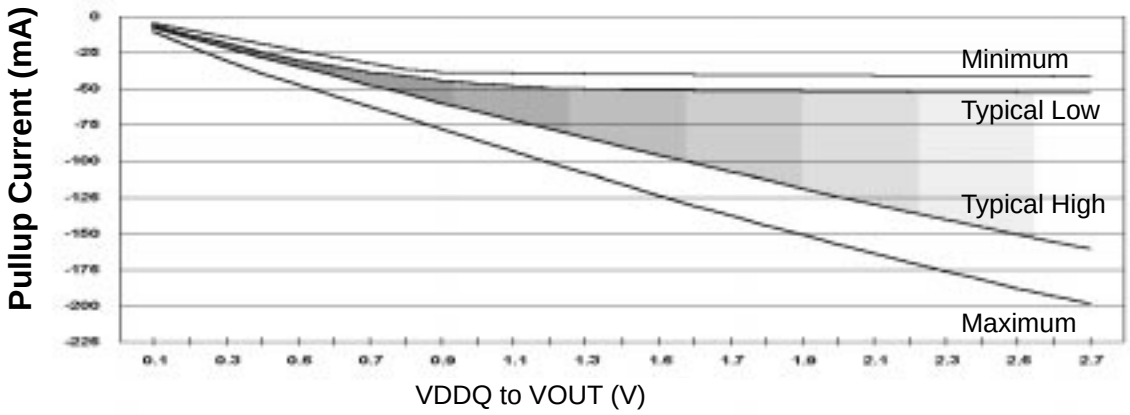


Figure b: Pull Up Characteristics

5) The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.
6) The full variation in the ratio of the ”typical” IBIS pullup to ”typical” IBIS pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.
7) These characteristics obey the SSTL_2 class II standard.
8) This specification is intended for DDR SDRAM only.

DATA DRIVER OUTPUT CHARACTERISTIC CURVES

	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.9	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	–155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	–160.1	–41.2	–198.2

Evaluation conditions:

Typical 25 ^{o} C ($T_{Ambient}$), VDDQ=2.5 V, typical process

Minimum 70° C ($T_{Ambient}$), VDDQ=2.3 V, slow–slow process

Maximum 0° C ($T_{Ambient}$), VDDQ=2.7 V, fast–fast process

DATA DRIVER OUTPUT CHARACTERISTIC V–I DATA POINTS

AC OPERATING CONDITIONS

(Notes: 1–5, 14, 16) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(ac)	VREF + 0.35		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(ac)		VREF –.35	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(ac)	0.7	VDDQ + 0.6	V	8
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(ac)	0.5*VDDQ–0.2	0.5*VDDQ+0.2	V	9

IDD SPECIFICATIONS AND CONDITIONS

(Notes: 1–5, 12, 14) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

		MAX		
PARAMETER/CONDITION	SYMBOL		UNITS	NOTES
OPERATING CURRENT: One Bank; Active–Precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cyle; address and control inputs changing once per clock cycle	IDD0	V/DS*	mA	
OPERATING CURRENT: One Bank; Active–Read–Precharge; Burst = 2; tRC = tRC MIN; CL = 2.5; tCK = tCK MIN; Iout = 0 mA; Address and control inputs changing once per clock cycle	IDD1	V/DS*	mA	
PRECHARGE POWER–DOWN STANDBY CURRENT: All banks idle; power–down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD2P	V/DS*	mA	
IDLE STANDBY CURRENT: $\overline{S}$ ≥ Vih (MIN); All banks idle; CKE ≥ Vih (MIN); tCK = tCK MIN; Address and other control inputs changing once per clock cycle	IDD2N	V/DS*	mA	
ACTIVE POWER–DOWN STANDBY CURRENT: One bank active; power–down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD3P	V/DS*	mA	
ACTIVE STANDBY CURRENT: $\overline{S}$ ≥ Vih (MIN); CKE ≥ Vih (MIN); One bank; Active–Precharge; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	V/DS*	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = tCK MIN; Iout = 0 mA	IDD4R	V/DS*	mA	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle	IDD4W	V/DS*	mA	
AUTO REFRESH CURRENT: tRC = tRFC (MIN)	IDD5	V/DS*	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2 V	IDD6	V/DS*	mA	11

V/DS* = Vendor/Device Specific

ELECTRICAL CHARACTERISTICS AND AC TIMING for DDR–266/DDR–200 – Absolute Specifications

(Notes: 1–5, 14–17) (0°C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		DDR–266A		DDR–266B		DDR–200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ output access time from CK/$\overline{CK}$	tAC	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	
CK high–level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low–level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)		min(tCL, tCH)		min(tCL, tCH)		ns	29
Clock cycle time CL = 2.5	tCK	7	15	7.5	15	8	15	ns	
CL = 2	tCK	7.5	15	10	15	10	15	ns	
DQ and DM input hold time	tDH	0.5		0.5		0.6		ns	
DQ and DM input setup time	tDS	0.5		0.5		0.6		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.5		ns	27
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		2		ns	27
Data–out high–impedance time from CK/$\overline{CK}$	tHZ	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	18
Data–out low–impedance time from CK/$\overline{CK}$	tLZ	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	18
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5		+0.5		+0.6	ns	
DQS–DQ Skew (for DQS and all DQ signals)	tDQSQA		+0.5		+0.5		+0.6	ns	
DQ/DQS output hold time from DQS	tQH	tHP–0.75		tHP–0.75		tHP–1.0		ns.	30
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	15		15		16		ns	
Write preamble setup time	tWPRES	0		0		0		ns	22
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.40	0.60	tCK	19
Write preamble	tWPRE	0.25		0.25		0.25		tCK	
Address and Control input hold time (fast slew rate)	tIH	0.9		0.9		1.2		ns	24,26,27
Address and Control input setup time (fast slew rate)	tIS	0.9		0.9		1.2		ns	25,26,27
Address and Control input hold time (slow slew rate)	tIH	1.0		1.0		1.2		ns	25,26,27
Address and Control input setup time (slow slew rate)	tIS	1.0		1.0		1.2		ns	25,26,27
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
$\overline{QFC}$ preamble during reads	tQPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
$\overline{QFC}$ postamble during reads	tQPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
$\overline{QFC}$ output access time from CK/$\overline{CK}$, for writes	tQCK		4		4		4	ns	
$\overline{QFC}$ output hold time for writes	tQOH	1.25	2.0	1.25	2.0	1.25	2.0	ns	
ACTIVE to PRECHARGE command	tRAS	45	120,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	65		65		70		ns	
Auto Refresh to Active/Auto Refresh command period	tRFC	75		75		80		ns	
ACTIVE to READ or WRITE delay	tRCD	20		20		20		ns	
PRECHARGE command period	tRP	20		20		20		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	15		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	35		35		35		ns	
Internal Write to Read Command Delay	tWTR	1		1		1		tCK	
Exit self refresh to non–READ command	tXSNR	75		75		80		ns	
Exit self refresh to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval	tREFI		15.6		15.6		15.6	µs	23

ELECTRICAL CHARACTERISTICS AND AC TIMING for DDR–266 – Applicable Specifications Expressed in Clock Cycles

(Notes: 1–5, 14–17) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		tCK = 7.5 ns			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQ output access time from CK/$\overline{CK}$	tAC	–0.75	+0.75	ns	
DQS output access time from CK/$\overline{CK}$	tDQSCK	–0.75	+0.75	ns	
CK high–level width	tCH	3.4	4.1	ns	
CK low–level width	tCL	3.4	4.1	ns	
CK half period	tHP	min(tCL, tCH)		ns	29
DQ and DM input hold time	tDH	0.5		ns	
DQ and DM input setup time	tDS	0.5		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		ns	27
DQ and DM input pulse width (for each input)	tDIPW	1.75		ns	27
Data–out high–impedance time from CK/$\overline{CK}$	tHZ	–0.75	+0.75	ns	18
Data–out low–impedance time from CK/$\overline{CK}$	tLZ	–0.75	+0.75	ns	18
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5	ns	
DQS–DQ Skew (for DQS and all DQ signals)	tDQSQA		+0.5	ns	
DQ/DQS output hold time	tQH	tHP–0.75		ns	30
Write command to first DQS latching transition	tDQSS	5.6	9.4	ns	
DQS input high pulse width	tDQSH	2.63		ns	
DQS input low pulse width	tDQSL	2.63		ns	
DQS falling edge to CK setup time	tDSS	1.5		ns	
DQS falling edge hold time from CK	tDSH	1.5		ns	
MODE REGISTER SET command cycle time	tMRD	2		tCK	
Write preamble setup time	tWPRES	0		ns	22
Write postamble	tWPST	3	4.5	ns	19
Write preamble	tWPRE	0.25			
Address and Control input hold time (fast slew rate)	tIH	0.9		ns	24,26,27
Address and Control input setup time (fast slew rate)	tIS	0.9		ns	24,26,27
Address and Control input hold time (slow slew rate)	tIH	1.0		ns	25,26,27
Address and Control input setup time (slow slew rate)	tIS	1.0		ns	25,26,27
Read preamble	tRPRE	6.75	8.25	ns	
Read postamble	tRPST	3	4.5	ns	
$\overline{QFC}$ preamble during reads	tQPRE	6.75	8.25	ns	
$\overline{QFC}$ postamble during reads	tQPST	3	4.5	ns	
$\overline{QFC}$ output access time from CK/$\overline{CK}$, for writes	tQCK		4	ns	
$\overline{QFC}$ output hold time for writes	tQOH	1.25	2.0	ns	
ACTIVE to PRECHARGE command	tRAS	6	16000	tCK	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	9		tCK	
Auto Refresh to Active/Auto Refresh command period	tRFC	10		tCK	
ACTIVE to READ or WRITE delay	tRCD	3		tCK	
PRECHARGE command period	tRP	3		tCK	
ACTIVE bank A to ACTIVE bank B command	tRRD	2		tCK	
Write recovery time	tWR	2		tCK	
Auto Precharge write recovery + precharge time	tDAL	5		tCK	
Internal Write to Read Command Delay	tWTR	1		tCK	
Exit self refresh to non–READ command	tXSNR	10		tCK	
Exit self refresh to READ command	tXSRD	200		tCK	
Average Periodic Refresh Interval	tREFI	15.6		µs	23

NOTES

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 36 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

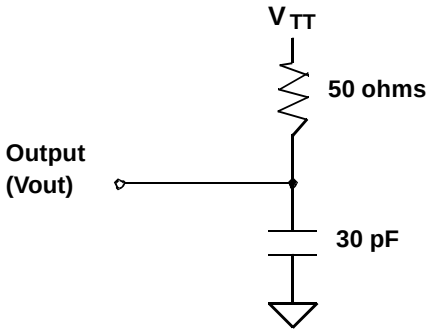
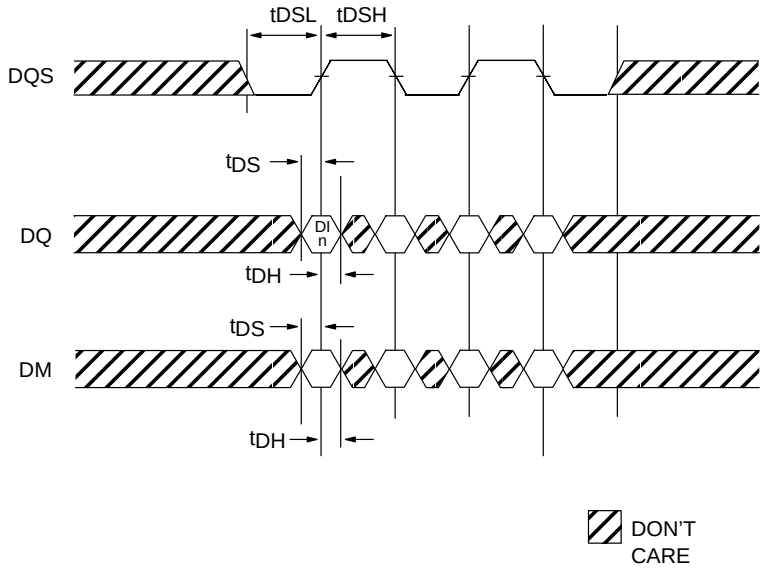


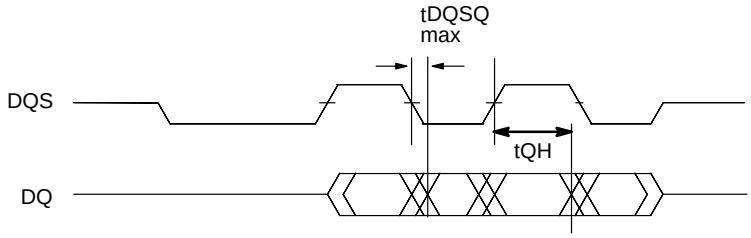
Figure 36: Timing Reference Load

4. ac timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/$\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak–to–peak noise on VREF may not exceed +/–2% of the dc value.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
8. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
9. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
11. Enables on–chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. This parameter is sampled. VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V , f = 100 MHz, tA = 25 °C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2 V. DM inputs are grouped with I/O pins – reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
15. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$, is VREF.
16. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.2VDDQ is recognized as LOW.
17. The output timing reference voltage level is VTT.
18. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
22. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High–Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
23. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
24. For command/address input slew rate ≥1.0 V/ns
25. For command/address input slew rate ≥0.5 V/ns and <1.0 V/ns
26. For CK & $\overline{CK}$ slew rate ≥1.0 V/ns
27. These parameters guarantee device timing, but they are not necessarily tested on each device.
28. Slew Rate is measured between VOH(ac) and VOL(ac).
29. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
30. tQH = tHPmin – X where:
    tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
    X consists of tDQSQmax, the pulse width distortion of on–chip clock circuits, data pin to pin skew and output pattern effects, and p–channel to n–channel variation of the output drivers.



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n

Figure 37 – DATA INPUT (WRITE) TIMING

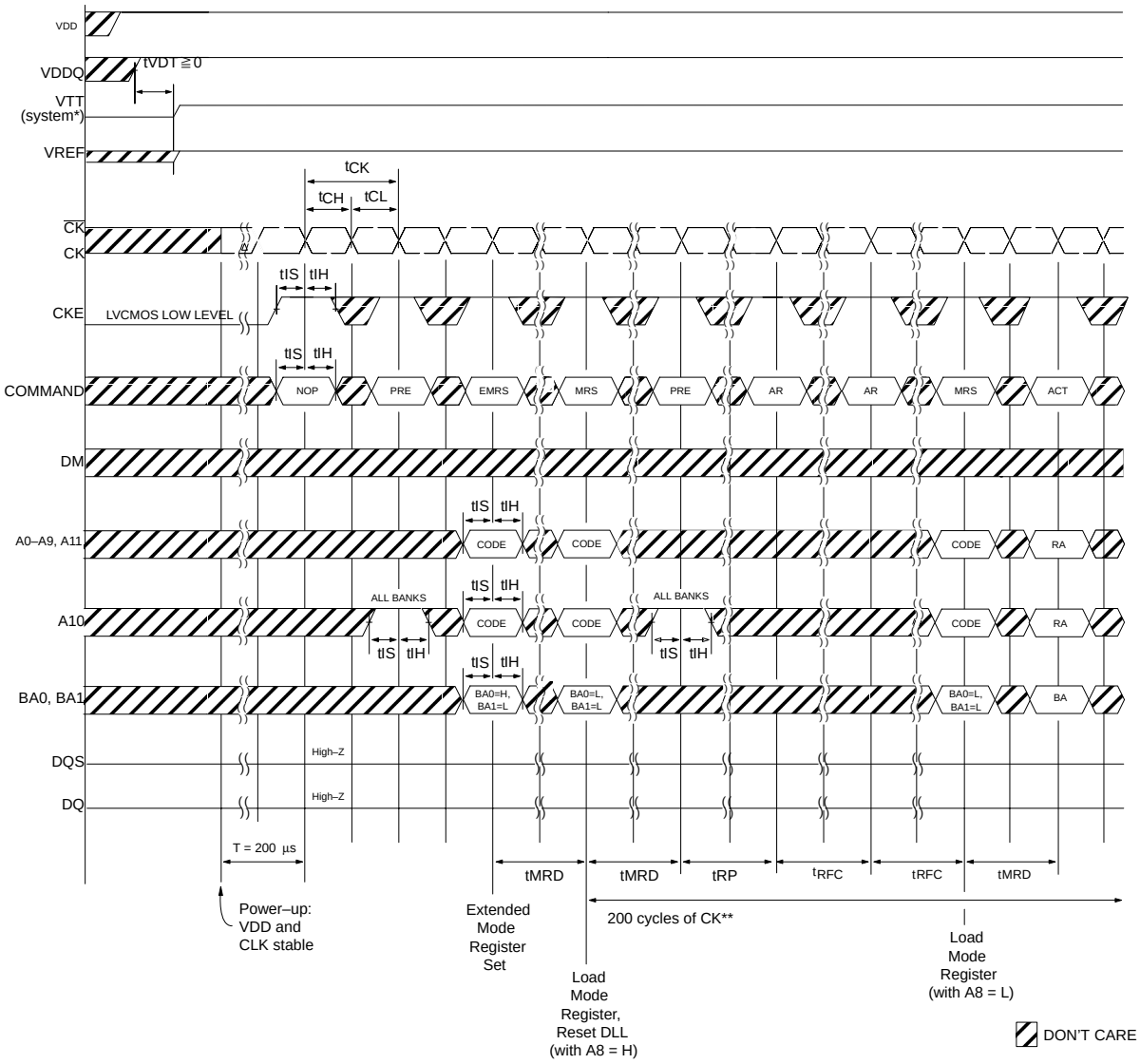


Burst of 4 is shown.

tDQSQ and tQH are only shown once, and are shown referenced to different edges of DQS, only for clarity of illustration. tDQSQ and tQH both apply to each of the four relevant edges of DQS.

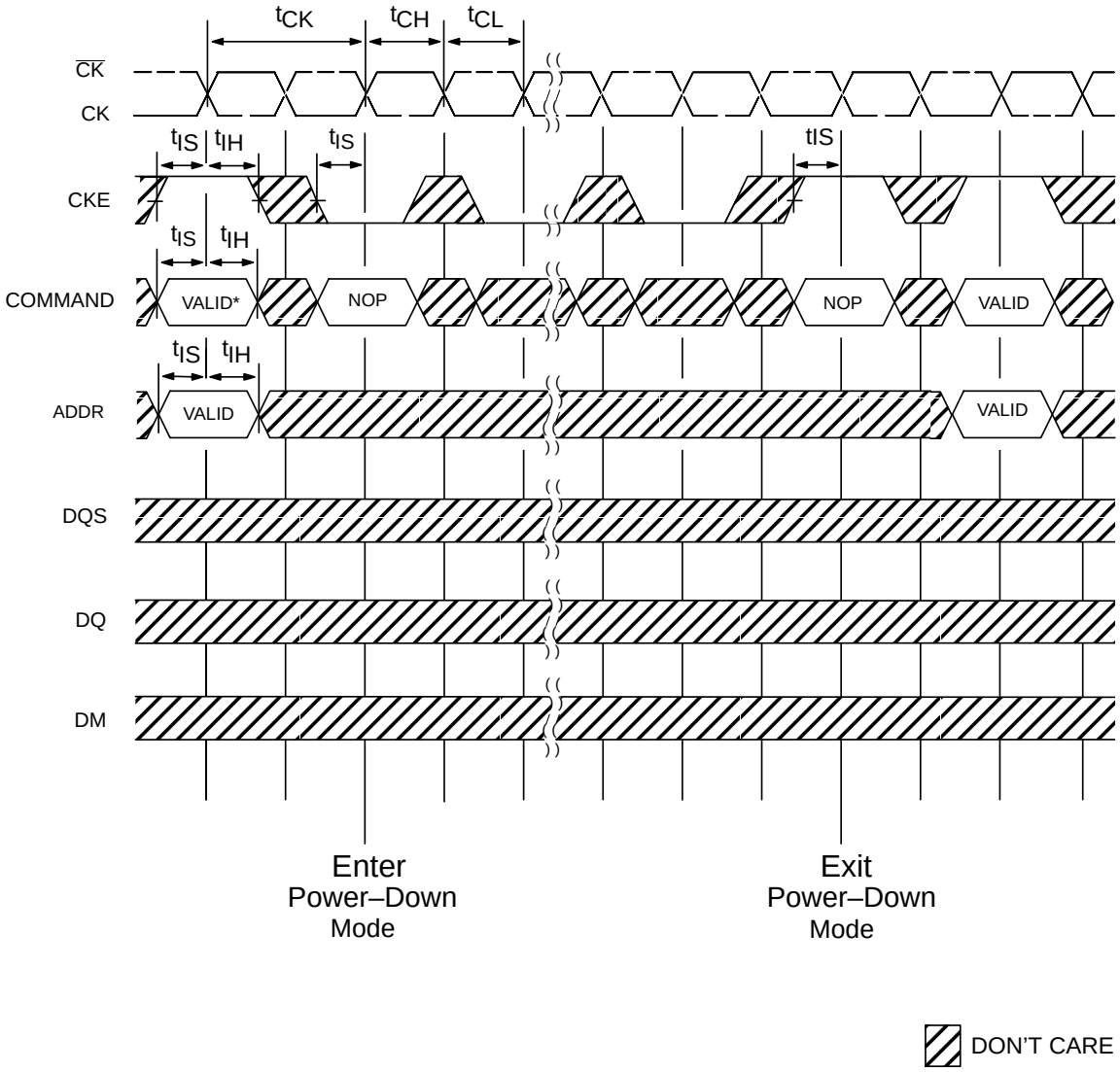
tQHmin = tHPmin – X where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
X consists of tDQSQmax, the pulse width distortion of on–chip clock circuits, data pin to pin skew and output pattern effects, and p–channel to n–channel variation of the output drivers.

Figure 38 – DATA OUTPUT (READ) TIMING



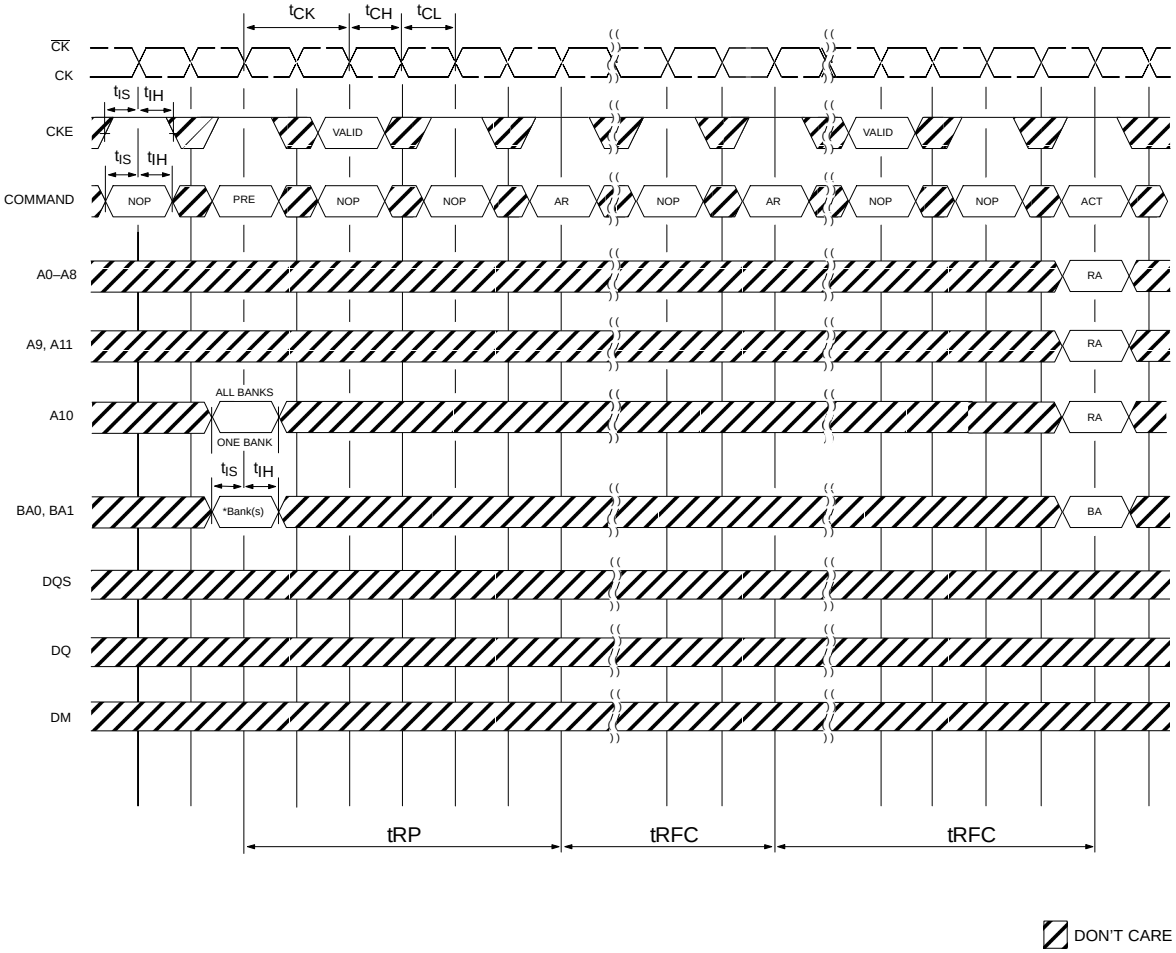
* = VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch–up.
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied
The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

Figure 39 – INITIALIZE AND MODE REGISTER SETS



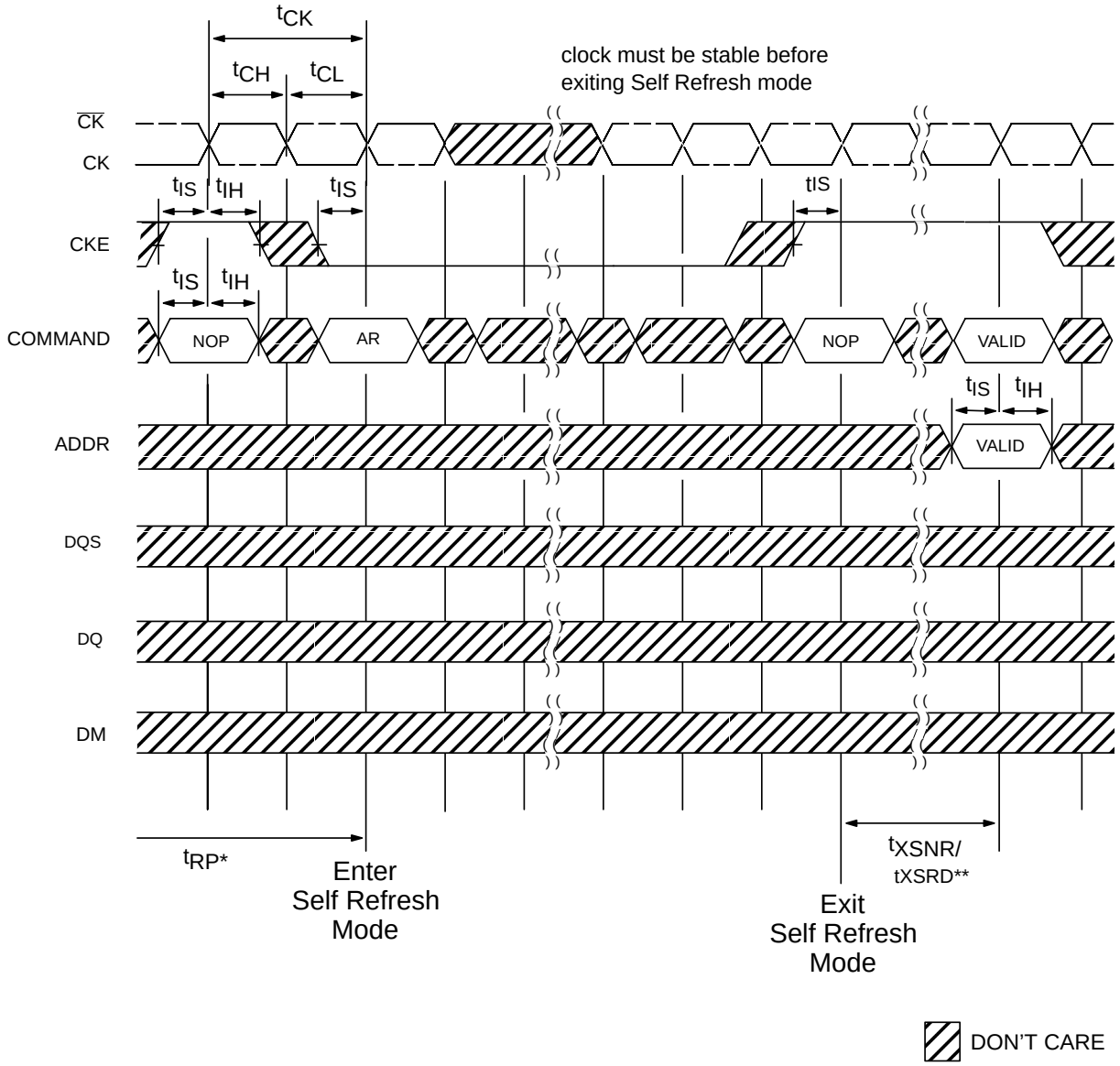
No column accesses are allowed to be in progress at the time Power–Down is entered
* = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power–Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power–Down mode shown is Active Power Down.

Figure 40 – POWER–DOWN MODE



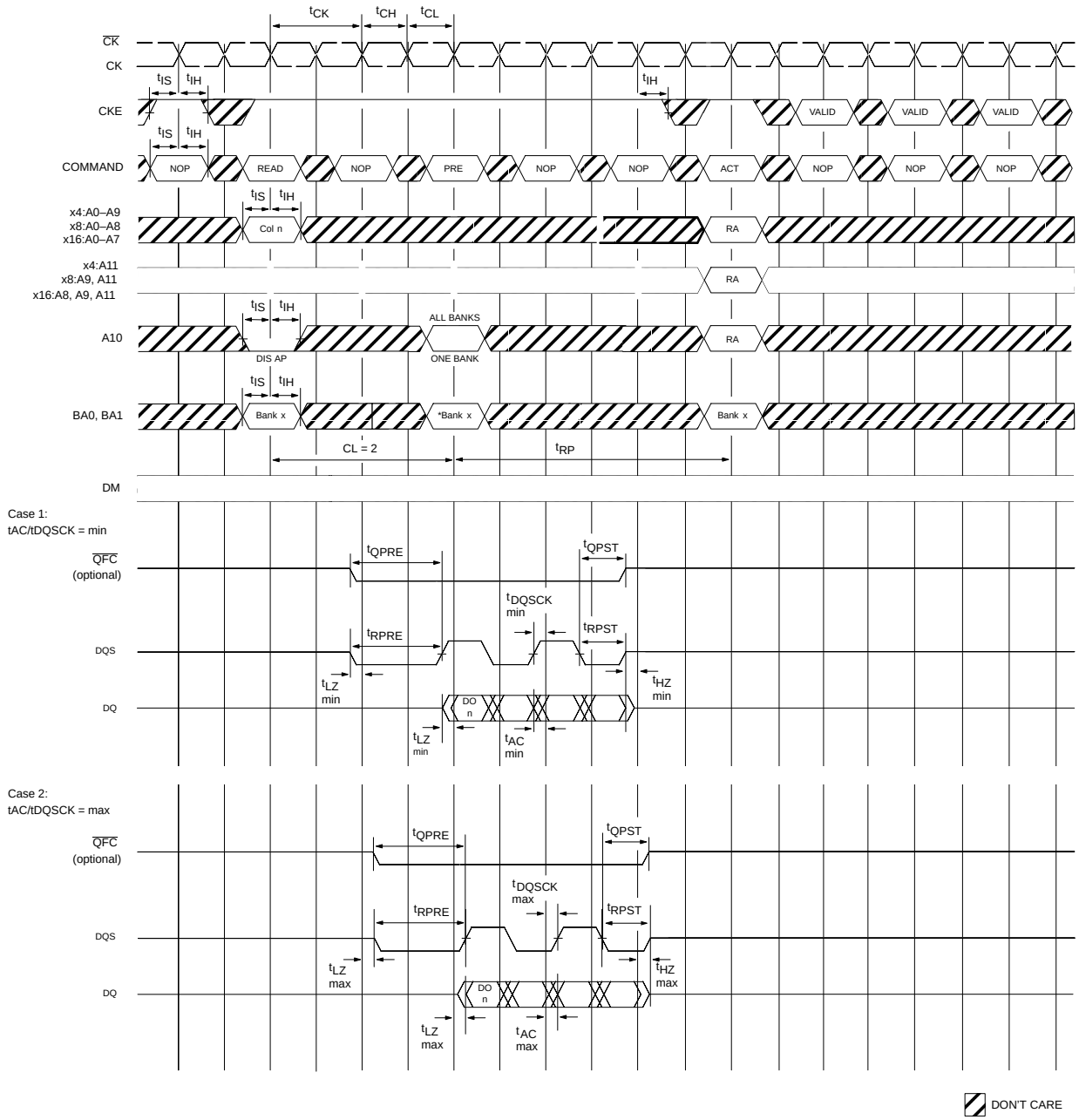
* = ”Don’t Care”, if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
DM, DQ and DQS signals are all ”Don’t Care”/High–Z for operations shown

Figure 41 – AUTO REFRESH MODE



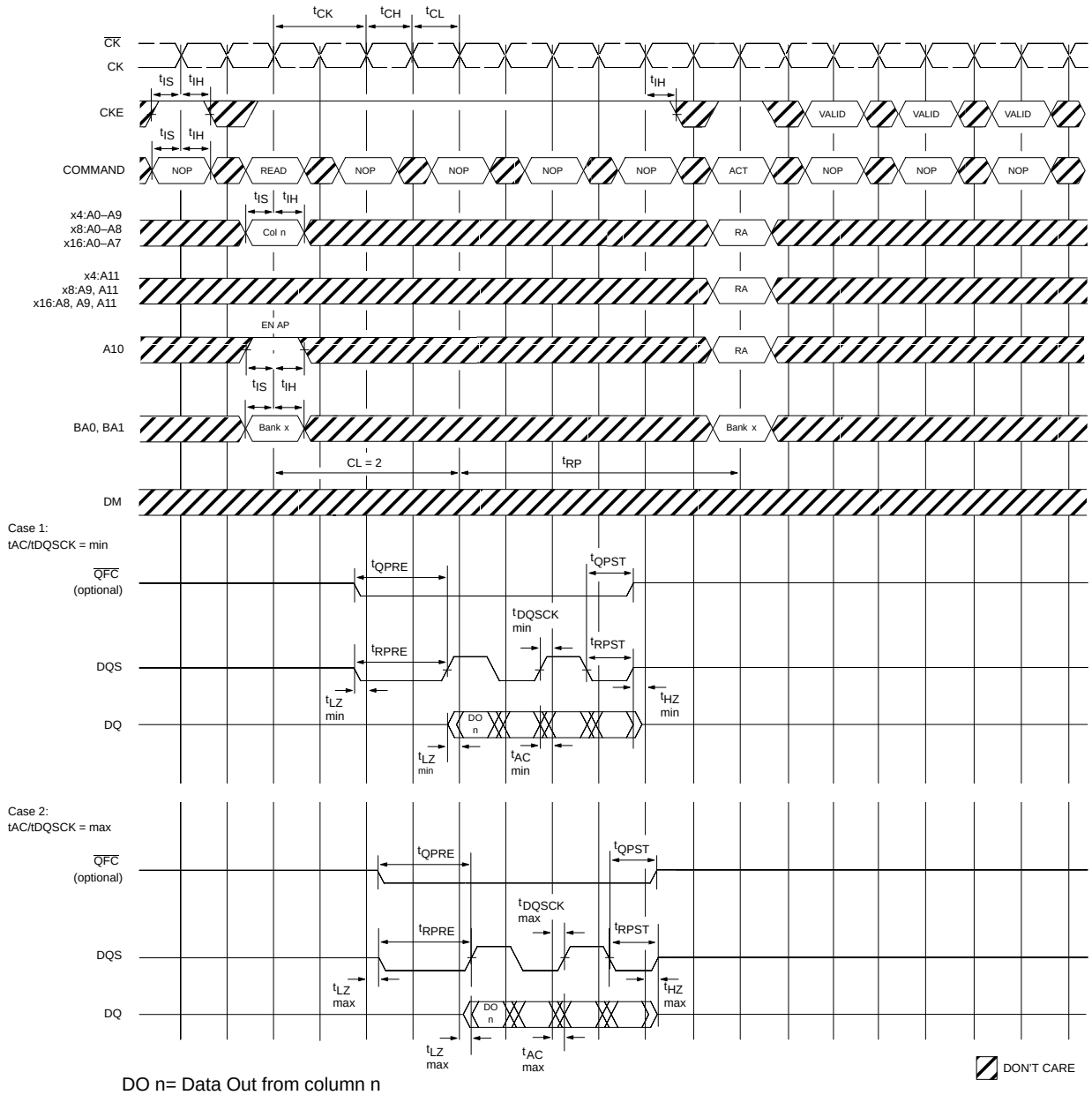
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non–READ command can be applied, and tXSRD (200 cycles of CK) are required before a READ command can be applied.

Figure 42 – SELF REFRESH MODE



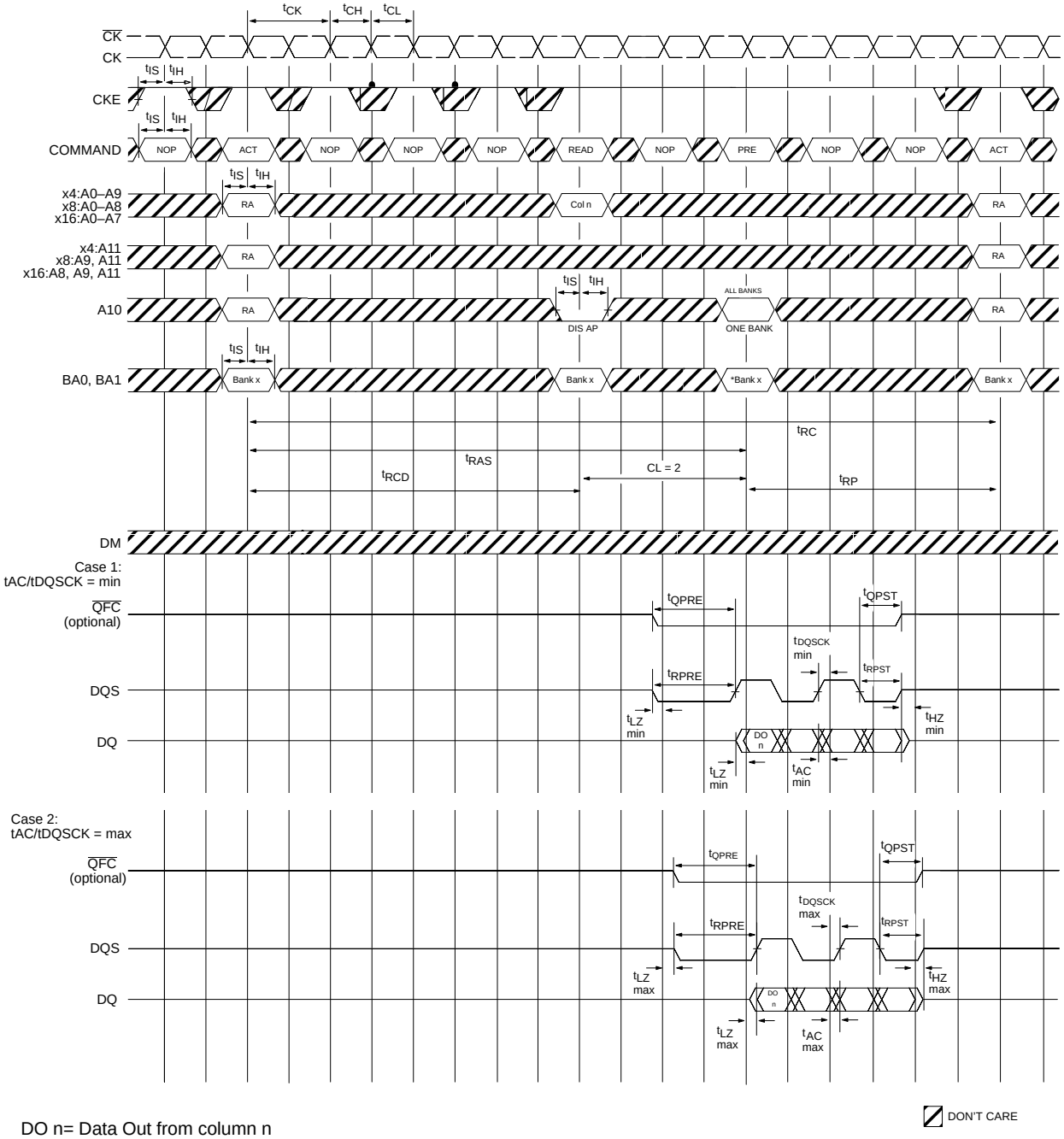
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 43 – READ _ WITHOUT AUTO PRECHARGE



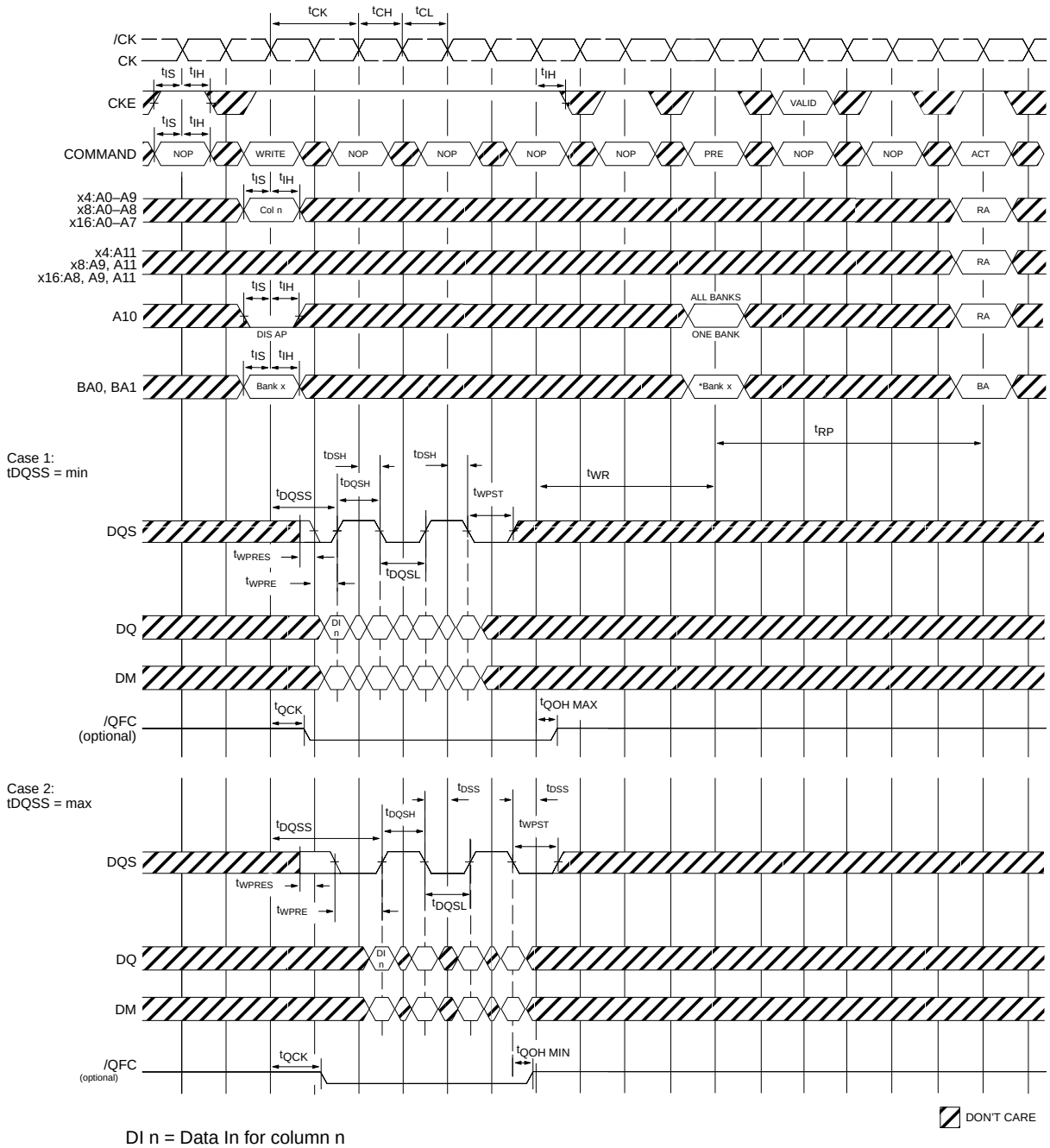
DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP = Enable Autoprecharge
ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 44 – READ _ WITH AUTO PRECHARGE



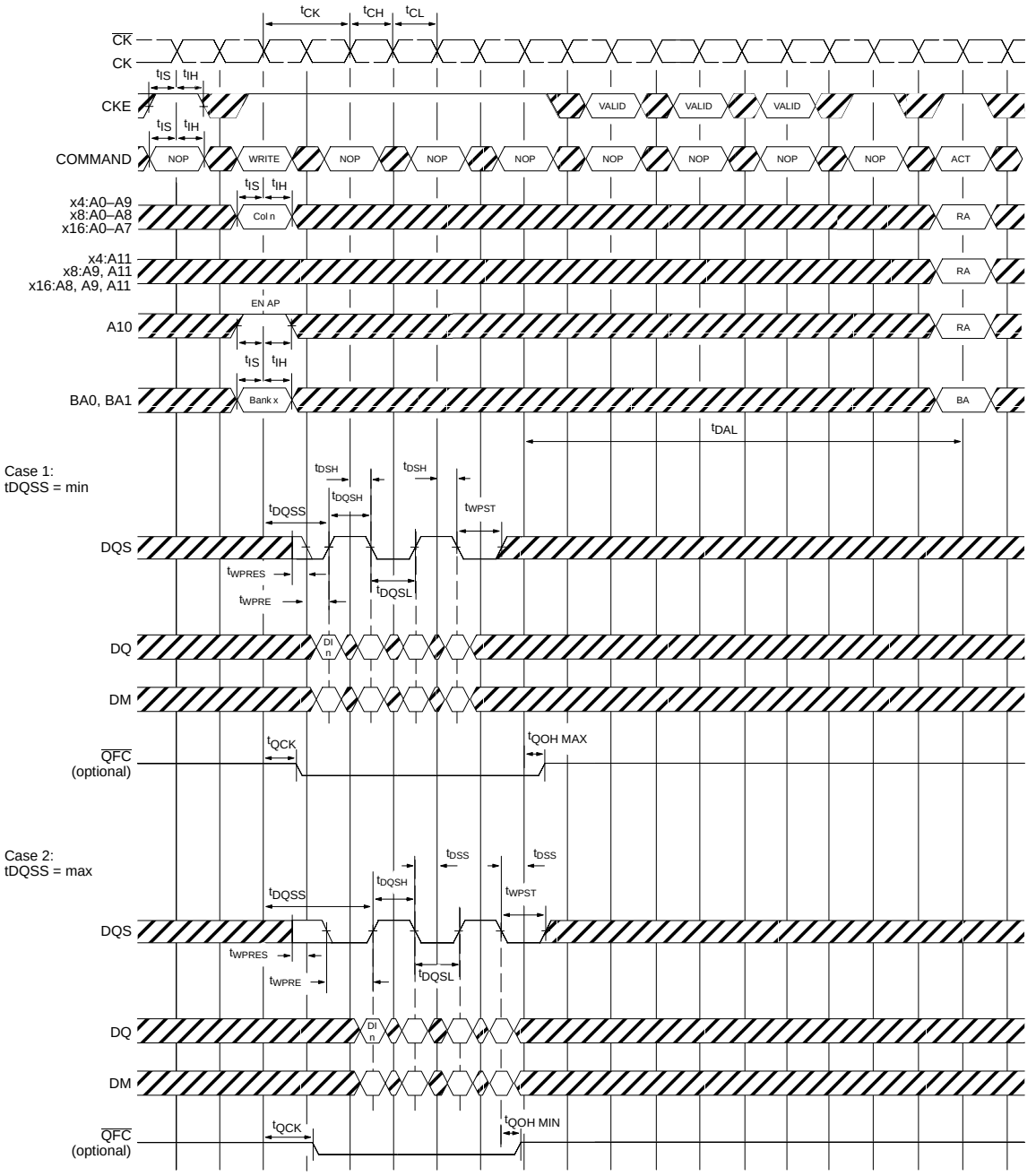
DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Figure 45 – BANK READ ACCESS



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 46 – WRITE – WITHOUT AUTO PRECHARGE



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n

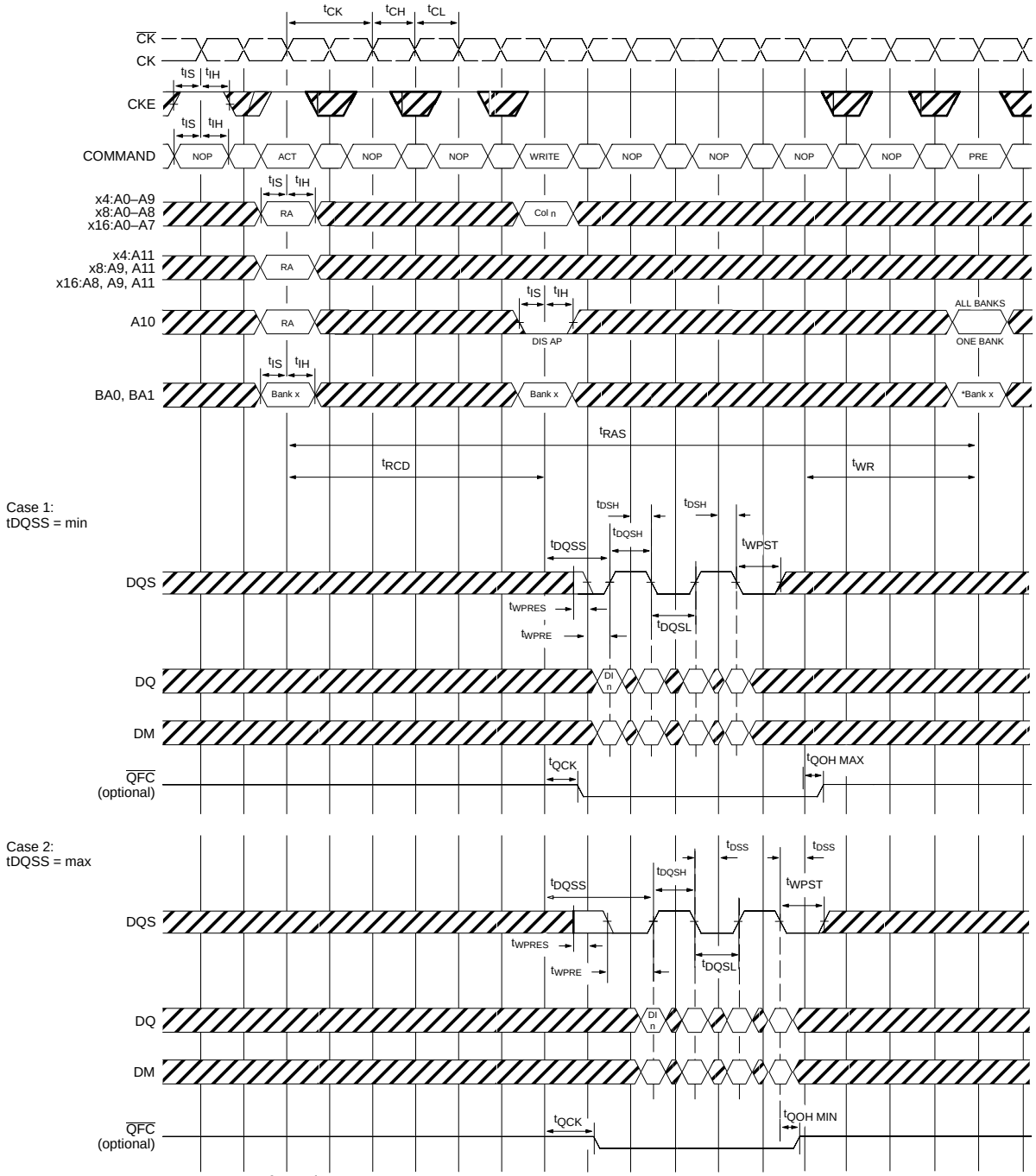
EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

DON'T CARE

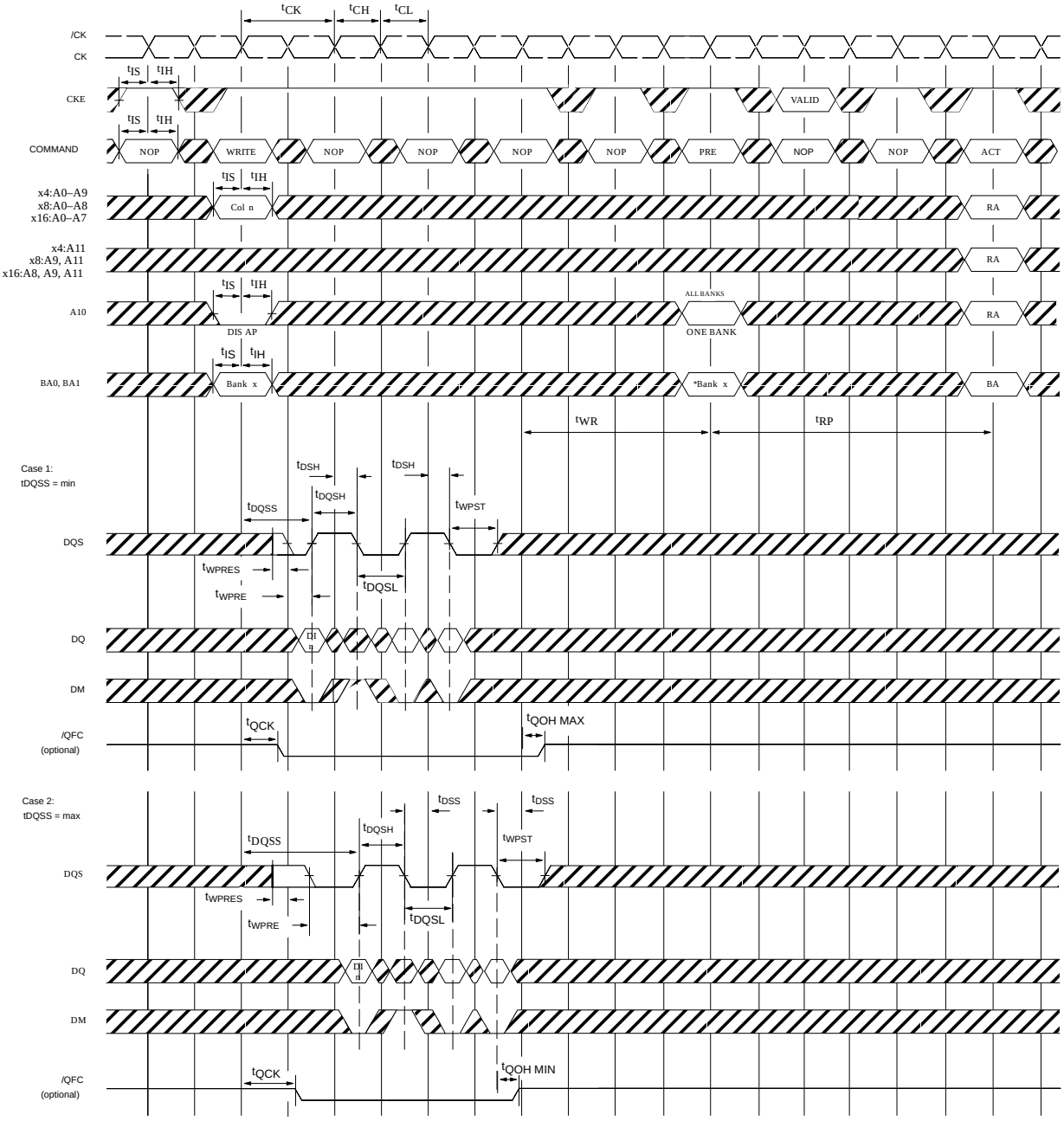
Figure 47 – WRITE – WITH AUTO PRECHARGE



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = ”Don’t Care”, if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

DON’T CARE

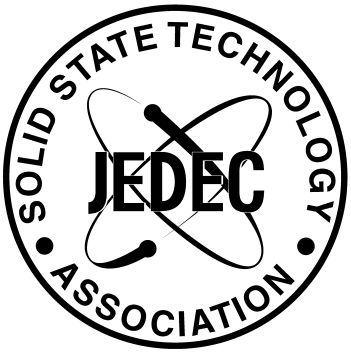
Figure 48 – BANK WRITE ACCESS



DON'T CARE

DI n= Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n (the second element of the four is masked)
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 49 – WRITE _ DM OPERATION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