

I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. During this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. After relocating to Maine in 2005, I transitioned to working as a full-time Consultant for JEDEC. Since June 2005, I have continued to work as a Consultant for JEDEC, where my responsibilities include the maintenance and publication of JEDEC documents and standards. I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members. During my tenure at JEDEC, JEDEC has not changed the system it uses to maintain JEDEC documents.

4. As a Consultant, I maintain all documents approved for publishing and have access to all documents at JEDEC. I receive JEDEC documents in draft form and prepare them for publishing. I also edit and help draft JEDEC's manuals of operation and procedure.

5. For over 60 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing over 350 member companies, and includes key technical individuals from most device, assembly, system, and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

6. Prior to 2000, JEDEC standards were typically available for purchase from JEDEC or approved reseller IHS. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (<https://www.jedec.org>), where they are cataloged and indexed by keyword and technological subject matter. Most of the standards are free to download, but larger volumes are available for purchase through JEDEC's website and approved reseller IHS.

7. By 2000, the JEDEC website was publicly available and commonly used by manufacturers, companies in the microelectronics industry, and other

interested parties to access and obtain standards information pertaining to that industry. Anyone can register online at JEDEC.org to access free standards and other JEDEC publications. Registration and most published standards are free and selected standards are only available to non-members for a fee. Between approximately 2000 and 2010, a registered user was required to log in before viewing JEDEC's free download area, which featured a list of standards and documents available for download. Around 2010, the website was re-designed so that a log-in was no longer required to visit the free download area and view a list of available standards and documents—instead, login information was only required to view and download a standard or other JEDEC document.

8. To confirm my statements above regarding access to JEDEC documents via JEDEC's website, I have visited the Internet Archive to look at captures of the "FREE Download Area" login and registration pages of JEDEC's website, which occurred on June 15, 2000 and September 1, 2000, respectively: <<http://web.archive.org/web/20000615041617/http://www.jedec.org/DOWNLOAD/default.cfm>> and <http://web.archive.org/web/20000901000313/http://www.jedec.org/DOWNLOAD/copyright_agreement.htm>. Printouts of these captures are attached as Exhibits A and B and are consistent with my personal recollection of the JEDEC website. I have also visited the Internet Archive to look at the first capture after the re-design

of JEDEC's website, which occurred on February 24, 2010:

<http://web.archive.org/web/20100224045304/http://www.jedec.org/standards-documents/results/field_doc_type%3A%22JESD%22?order=field_doc_full_number_value&sort=asc>. A printout of this capture is attached as Exhibit C and is consistent with my personal recollection of the JEDEC website.

9. This declaration concerns the following standards published by JEDEC:

(1) JEDEC STANDARD, Configurations for Solid State Memories, JEDEC Standard No. 21-C, Release 7 (January 1997) (hereinafter, "JESD21-C Release 7");

(2) JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, Release 1 (June 2000) (hereinafter, "JESD79 Release 1");

(3) JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, Release 2 (May 2002) (hereinafter, "JESD79 Release 2");

(4) JEDEC STANDARD, DDR2 SDRAM Specification, JESD79-2A (January 2004) (hereinafter, "JESD79-2A"); and

(5) JEDEC STANDARD, Configurations for Solid State Memories, JEDEC Standard No. 21-C, Release 14 (January 2005) (hereinafter, "JESD21-C Release 14") (collectively, "the JEDEC Standards"). I have reviewed the above JEDEC standards. The copies of the JEDEC Standards attached to this declaration as Exhibits D-H are identical to the copies of the JEDEC Standards in JEDEC's files.

10. The following statements on the public availability of the JEDEC Standards as of their respective publish dates are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and published. For the JESD21-C Release 7, JESD79 Release 1, JESD79 Release 2, JESD79-2A, and JESD21-C Release 14 standards, the dates on the covers (and thus the dates the standards were published and/or posted to JEDEC's website) are January 1997, June 2000, May 2002, January 2004, and January 2005, respectively.

11. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication and seeks final review and approval to publish from the JEDEC legal department.

12. Before 2000, once legal approval was received, the JEDEC publications department made the approved document available to the JEDEC membership and members of the public through JEDEC and, for most documents except larger volumes and subscription services, through an approved reseller IHS. For larger volumes, such as JESD21-C, the date on the cover of the Standard indicates the date that it was sent to those with a subscription to the annual updating

service for the volume, in which subscribers would receive the new and/or updated replacement pages of the various modules of the Standard as they were released and insertion instructions for the new and/or updated replacement pages. In addition, copies of the entire volume, as well as any other finalized standard, would have been available for purchase from JEDEC by anyone in the public. The release indicated at the bottom of a given page of larger volumes indicates the release in which that page would have received by subscribers and would have been available for purchase by anyone in the public.

13. Since 2000, once legal approval is received, the JEDEC publications department uploads the approved documents to the JEDEC website with a brief description. When a standard is published on JEDEC's website, it becomes available in the "Standards & Documents" section, where standards are listed by title, document number, and publish date. An email announcement is then sent to the sponsoring committee and any approved resellers.

14. Based on my personal knowledge of JEDEC's policies, the JESD21-C Release 7 Standard was made publicly available in January 1997, consistent with the date notation on the first page of the Standard, through a subscription and availability for purchase by any member of the public, and the JESD79 Release 1, JESD79 Release 2, JESD79-2A, and JESD21-C Release 14 standards were made publicly available via JEDEC's website in June 2000, May 2002, January 2004, and

January 2005, respectively, consistent with the date on the cover page of each respective Standard.

15. Based on my personal knowledge of JEDEC's policies, the JESD21-C Releases 1 through 6 were also publicly available at least by January 1997, when JESD21-C Release 7 was made publicly available, through a subscription and availability for purchase by any member of the public of JESD21-C as an entire volume. Similarly, the JESD21-C Releases 1 through 13 were also publicly available at least by January 2005, when JESD21-C Release 14 was made publicly available, through a subscription and availability for purchase by any member of the public of JESD21-C as an entire volume.

16. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's typical practice was not followed. I have no reason to believe that the JESD21-C Release 7 Standard was not published and made accessible to JEDEC membership and any member of the public in January 1997. I also have no reason to believe that the JESD21-C Release 14 Standard was not published and made accessible to JEDEC membership and any member of the public in January 2005. I also have no reason to believe that the JESD79 Release 1, JESD79 Release 2, and JESD79-2A standards were not

made publicly available via JEDEC's website in June 2000, May 2002, and January 2004, respectively. I also have no reason to believe that the JESD21-C Releases 1 through 6 were not published and made accessible to any member of the public by a subscription or purchase of JESD21-C at least by January 1997, when the JESD-21C Release 7 Standard was made publicly available. I also have no reason to believe that the JESD21-C Releases 1 through 13 were not published and made accessible to any member of the public by a subscription or purchase of JESD21-C at least by January 2005, when the JESD-21C Release 14 Standard was made publicly available.

17. To further confirm my statements above regarding the JESD79 DDR Standard, I visited the Internet Archive to look at the first capture of the JEDEC website after June 2000, which occurred on August 17, 2000:

<<http://web.archive.org/web/20000817100341/http://www.jedec.org/Default.htm>>.

A printout of this capture is attached as Exhibit I and is consistent with my personal recollection of the JEDEC website. As shown in Exhibit I, the JESD79 Release 1 "DDR" Standard was featured on the JEDEC homepage, which included a link to the following page captured on August 17, 2000, which allowed anyone to download the JESD79 DDR Standard for "DDR" memory:

<<http://web.archive.org/web/20000817100514/http://www.jedec.org/DOWNLOAD/pub21/HotDDR/Default.cfm>>. A printout of this capture is attached as Exhibit J

and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on August 17, 2000, the JESD79 Release 1 DDR Standard was described on the JEDEC website as the “JEDEC Standard 79, Double Data Rate (DDR) SDRAM Specification (datasheet for 64Mb SDRAM)” and was available for download by the public by that date, consistent with my statements above.

18. Exhibit K is a printout of https://web.archive.org/web/20000711020535/http://www.jedec.org/service_members/New_Members/memberco.htm, which is a capture on July 11, 2000 of JEDEC’s list of member companies as of that date. Exhibit L is a printout of https://web.archive.org/web/20020605015448/http://www.jedec.org/service_members/New_Members/memberco.htm, which is a capture on June 5, 2002 of JEDEC’s list of member companies as of that date. Exhibit M is a printout of https://web.archive.org/web/20040202081543/http://jedec.org:80/service_members/New_Members/memberco.cfm, which is a capture on February 2, 2004 of JEDEC’s list of member companies as of that date. Exhibit N is a printout of https://web.archive.org/web/20051024132448/http://www.jedec.org:80/service_members/New_Members/memberco.cfm, which is a capture on October 24, 2005 of JEDEC’s list of member companies as of that date. Exhibits K, L, M, and N are consistent with my personal recollection of JEDEC’s membership. The member

companies listed in Exhibit K would have had access to JESD79 Release 1 by no later than July 11, 2000. The member companies listed in Exhibit L would have had access to JESD79 Release 2 by no later than June 5, 2002. The member companies listed in Exhibit M would have had access to JESD79-2A by no later than February 2, 2004. Lastly, the members listed in Exhibit N would have had access to JESD21-C Release 14 no later than October 24, 2005.

I, Julie Carlson, do hereby declare and state that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 1/27/2023



Julie D. Carlson

Exhibit A



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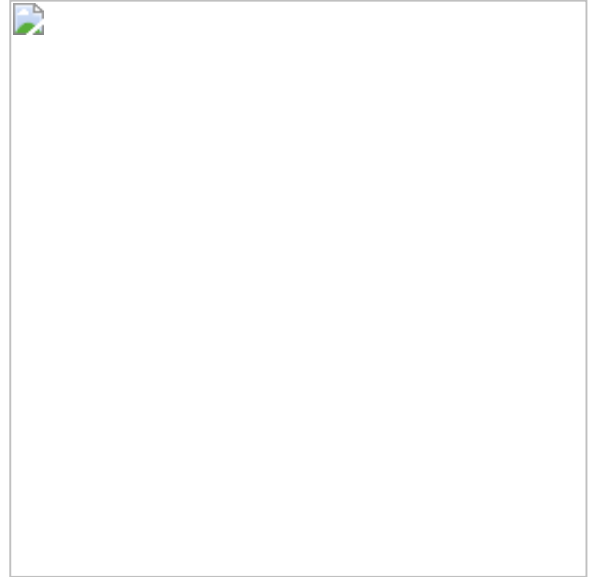
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Exhibit C



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LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS:	JESD1	Apr 1982

This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages.

Committee(s): [JC-41](#)

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<u>Title</u>	<u>Document #</u> ▲	<u>Date</u>
<u>LOW FREQUENCY POWER TRANSISTORS:</u> Status: Reaffirmed September 1981, October 2002	JESD10	Jan 1976

This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

Committee(s): [JC-25](#)

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<u>TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:</u>	JESD100B.01	Dec 2002
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A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, microcontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

Committee(s): [JC-10](#)

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<u>CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS:</u>	JESD11	Dec 1984
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This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

Committee(s): [JC-40.2](#)

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<u>SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET):</u>	JESD12	Jun 1985
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The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

Committee(s): [JC-44](#)

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ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS:	JESD12-1B	Aug 1993
The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.		
Committee(s): JC-44		
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ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET:	JESD12-2	Feb 1986
The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs.		
Committee(s): JC-44		
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ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD:	JESD12-3	Jun 1986
This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits.		
Committee(s): JC-44		
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ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS:	JESD12-4	Apr 1987
This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation.		
Committee(s): JC-44		
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<u>ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:</u>	JESD12-5	Aug 1988
This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility. Committee(s): <u>JC-44</u> <u>Download JESD12-5</u> Free download. <u>Registration</u> or <u>login</u> required.		
<u>ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:</u>	JESD12-6	Mar 1991
This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation. Committee(s): <u>JC-44</u> <u>Download JESD12-6</u> Free download. <u>Registration</u> or <u>login</u> required.		
<u>STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES:</u>	JESD13-B	May 1980
This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices. Committee(s): <u>JC-40.2</u> <u>Download JESD13-B</u> Free download. <u>Registration</u> or <u>login</u> required.		
<u>SEMICONDUCTOR POWER CONTROL MODULES:</u> Status: Reaffirmed June 1992, April 1999, April 2002	JESD14	Nov 1986
Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both. Committee(s): <u>JC-22.2</u> <u>Download JESD14</u> Free download. <u>Registration</u> or <u>login</u> required.		

<u>Title</u>	<u>Document #</u> ▲	<u>Date</u>
<u>THERMAL MODELING OVERVIEW</u>	JESD15	Oct 2008

This document and the associated series of documents are intended to promote the continued development of modeling methods, while providing a coherent framework for their use by defining a common vocabulary to discuss modeling, creating requirements for what information should be included in a thermal modeling report, and specifying modeling procedures, where appropriate, and validation methods. This document provides an overview of the methodology necessary for performing meaningful thermal simulations for packages containing semiconductor devices. The actual methodology components are contained in separate detailed documents.

Committee(s): [JC-15.1](#), [JC-15](#)

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<u>COMPACT THERMAL MODEL OVERVIEW</u>	JESD15-1	Oct 2008
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This document should be used in conjunction with the master document, JESD15, and JESD15-2, and subsidiary documents as they become available. This document is intended to function as an overview to support the effective use of Compact Thermal Model (CTM) methodologies as specified in the companion methods documents. At present, there are two such documents; JESD15-3, and JESD15-4.

Committee(s): [JC-15.1](#), [JC-15](#)

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<u>TWO-RESISTOR COMPACT THERMAL MODEL GUIDELINE</u>	JESD15-3	Jul 2008
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This document specifies the definition and construction of a two-resistor compact thermal model (CTM) from the JEDEC junction-to-case and junction-to-board thermal metrics. The guidance provided in this document only applies to thermal metrics defined in JEDEC standards JESD51-8 and JESD51-12. The scope of this document is limited to single-die packages that can be effectively represented by a single junction temperature.

Committee(s): [JC-15](#)

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<u>DELPHI COMPACT THERMAL MODEL GUIDELINE</u>	JESD15-4	Oct 2008
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This guideline specifies the definition and lists acceptable approaches for constructing a compact thermal model (CTM) based on the DELPHI methodology. The purpose of this document is twofold. First, it aims to provide clear guidance to those seeking to create DELPHI compact models of packages. Second, it aims to provide users with an understanding of the methodology by which they are created and validated, and the issues associated with their use.

Committee(s): [JC-15](#)

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[ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION \(PPM\)](#); Status: Reaffirmed September 2008 JESD16-A

Apr
1995

This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combining groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met. Not all sections of EIA-554 are appropriate for use by device manufacturers therefore JEDEC wishes to continue using JESD16A. In December 2008 the formulating committee approved to remove EIA-554 (July 1996, Reaffirmed September 2002) from the JEDEC website. To obtain a copy of EIA-554 please contact GEIA at <http://www.geia.org/>

Committee(s): [JC-13](#)

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[LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999](#) Status: Rescinded February 1999 JESD17

Aug
1988

Committee(s): [JC-40.2](#)

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[STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC](#); JESD18-A

Jan
1993

The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices.

Committee(s): [JC-40.2](#)

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Exhibit E

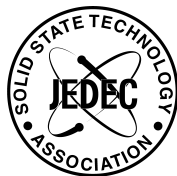
JEDEC STANDARD

Double Data Rate (DDR) SDRAM Specification

JESD79

JUNE 2000

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Double Data Rate (DDR) SDRAM Specification

(The material contained in this standard was formulated under the cognizance of the JC-42.3 Subcommittee on RAM Memories and approved by the JEDEC Board of Directors. The text in this standard is from the following BoD Ballots: JCB-99-70, JCB-99-84, JCB-00-08, JCB-00-10, JCB-00-11, JCB-00-12, JCB-00-13, and JCB-00-23.)

1 Purpose

To define the minimum set of requirements for JEDEC-compliant 64M x4/x8/x16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

2 Scope

This comprehensive standard defines all required aspects of 64M x4/x8/x16 DDR SDRAMs, including features, functionality, AC and DC parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M x4 (4 M x4 x4 banks), 8 M x8 (2 M x8 x4 banks), 4 M x16 (1 M x16 x4 banks)

FEATURES

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 15.6 μs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ = +2.5 V ± 0.2 V
- VDD = +3.3 V ± 0.3 V or +2.5 V ± 0.2 V

GENERAL DESCRIPTION

The 64 Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM.

The 64 Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n pre-fetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The 64 Mb DDR SDRAM operates from a differential clock (CK and $\overline{\text{CK}}$; the crossing of CK going HIGH and

$\overline{\text{CK}}$ going LOW will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices will have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

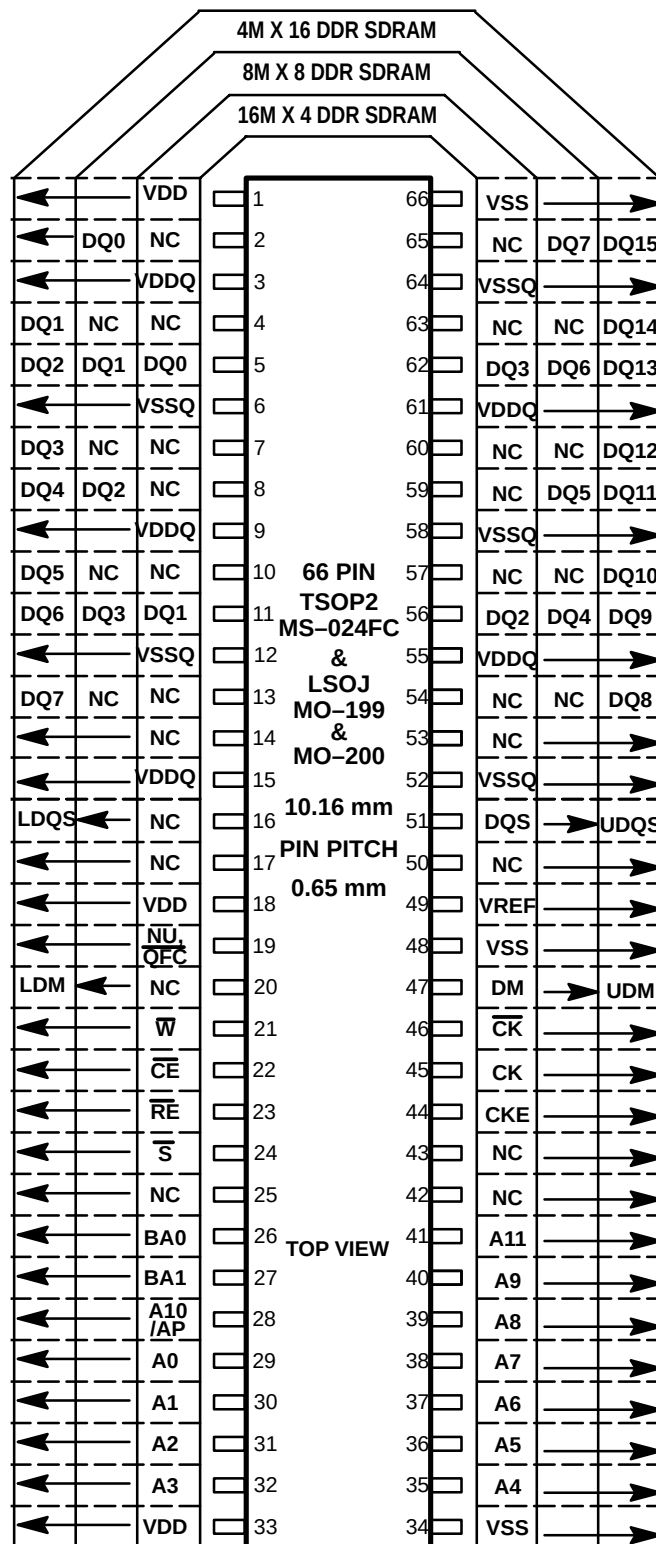
This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC 64 M x4/x8/x16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

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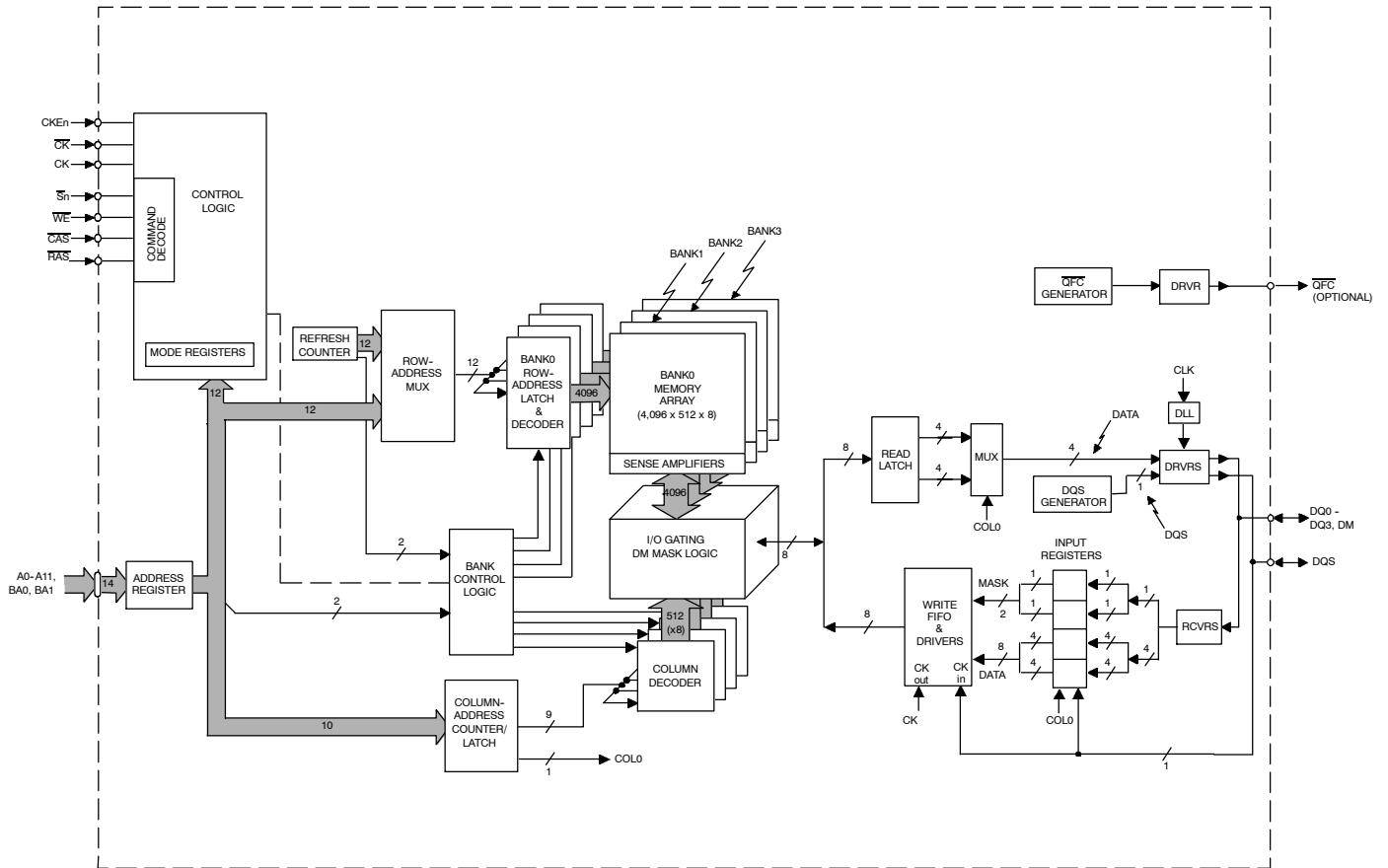


ADDRESS ASSIGNMENT TABLE

	DENSITY	BANKS	ROW ADDR.	COL ADDR.	BANK ADDR
16M X 4	64 Mb	4	A0⇒A11	A0⇒A9	BA0, BA1
8M X 8	64 Mb	4	A0⇒A11	A0⇒A8	BA0, BA1
4M X 16	64 Mb	4	A0⇒A11	A0⇒A7	BA0, BA1

64 M DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ

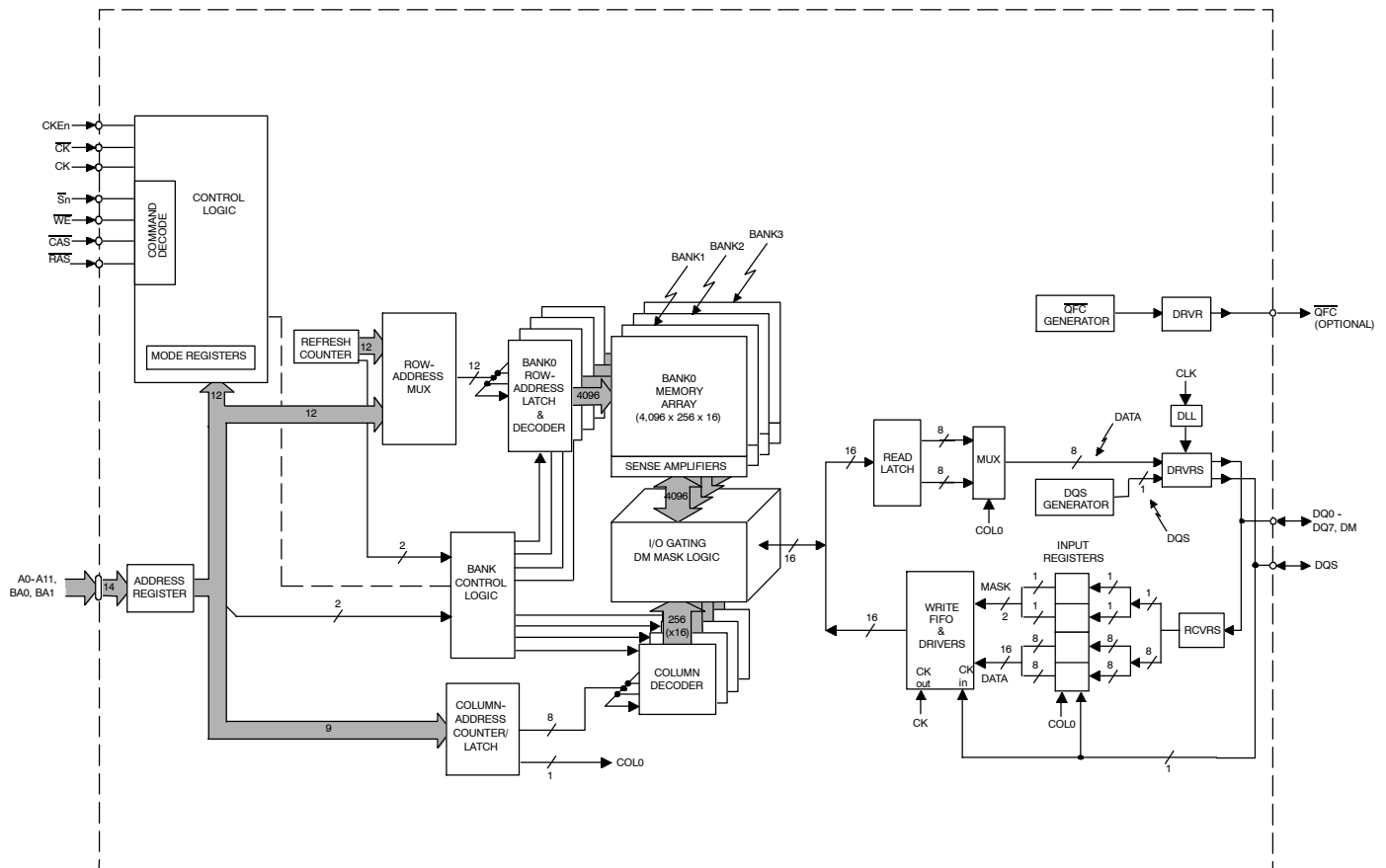
FUNCTIONAL BLOCK DIAGRAM - x4 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

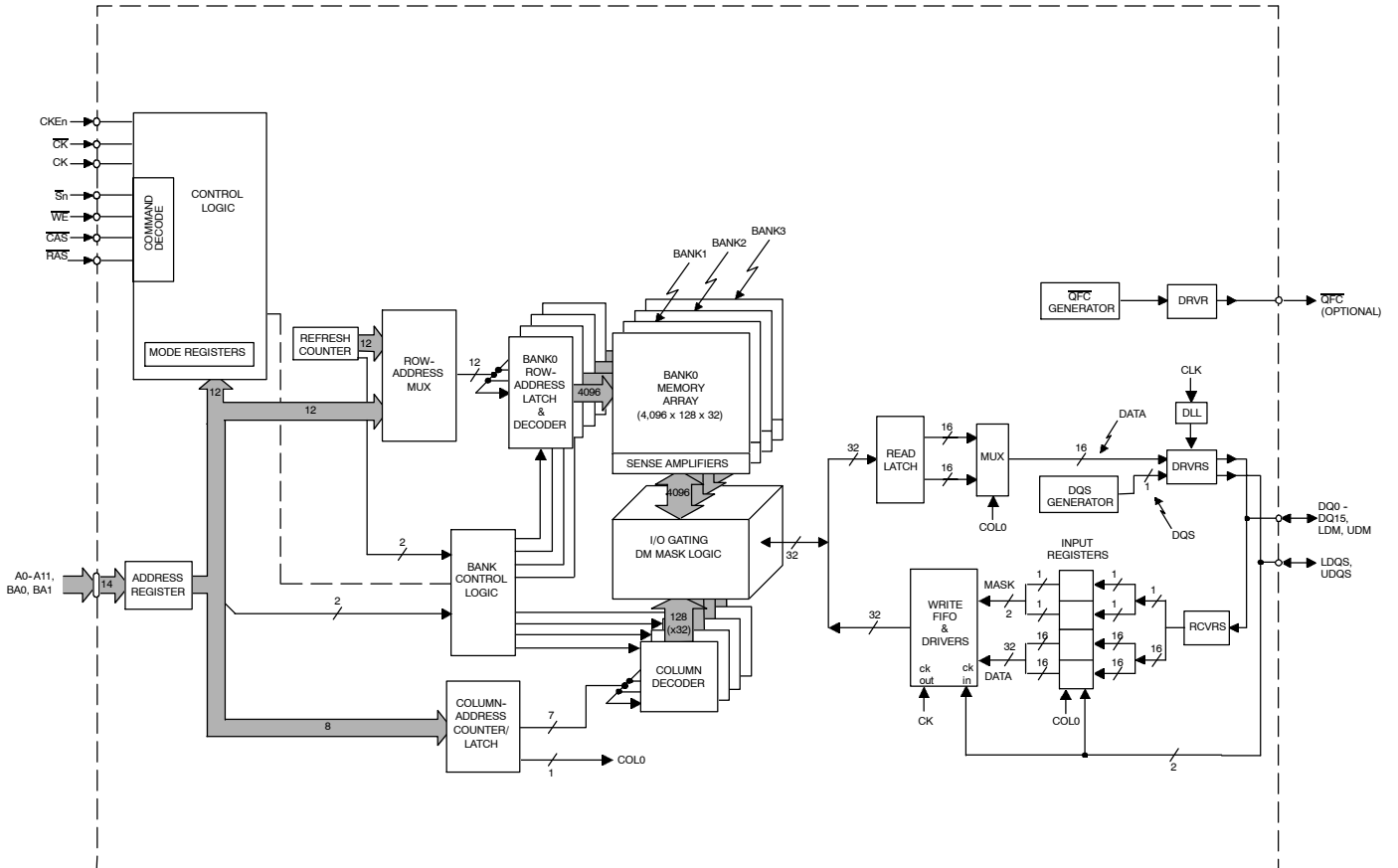
FUNCTIONAL BLOCK DIAGRAM - x8 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

FUNCTIONAL BLOCK DIAGRAM - x16 CONFIGURATION



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: LDM and UDM are unidirectional signals (input only) but are internally loaded to match the load of the bidirectional DQ and DQS signals.

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE(n)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied. The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{S}$ (n)	Input	Chip Select: All commands are masked when $\overline{S}$ is registered high. $\overline{S}$ provides for external bank selection on systems with multiple banks. $\overline{S}$ is considered part of the command code. The standard pinout includes one $\overline{S}$ pin. Optional pinouts include $\overline{S}$ 0 and $\overline{S}$ 1 on different pins, to facilitate device stacking.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{S}$) define the command being entered.
DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0–DQ7; UDM corresponds to the data on DQ8–DQ15.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.–
A0–A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	I/O	Input/Output: Data bus
DQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0–DQ7; UDQS corresponds to the data on DQ8–DQ15.
$\overline{QFC}$	Output	FET Control: Optional. Output during every Read and Write access. Can be used to control isolation switches on modules. Open drain output.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V $\pm$ 0.2 V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V $\pm$ 0.3 V or +2.5 V $\pm$ 0.2 V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

FUNCTIONAL DESCRIPTION

The 64 Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. The 64 Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 64 Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. Vref can be applied any time after VDDQ, but is expected to be nominally coincident with Vtt. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μ s delay prior to applying an executable command.

Once the 200 μ s delay has been satisfied, a DE-SELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the "all banks idle" state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 1. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–Ai when the burst length is set to two, by A2–Ai when the burst length is set to four and by A3–Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

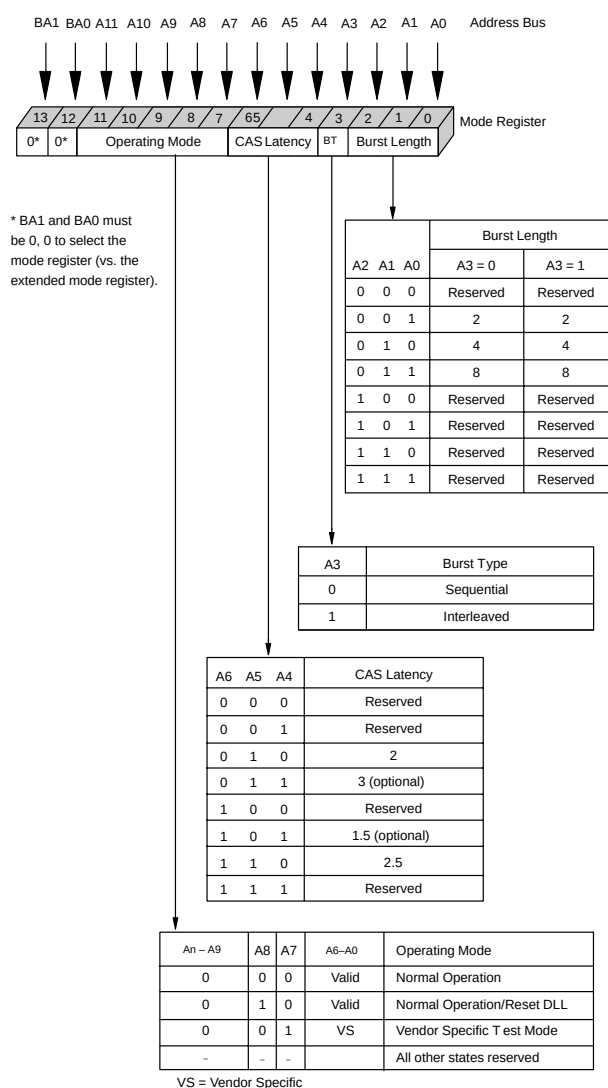


Figure 1

MODE REGISTER DEFINITION

Table 1

BURST DEFINITION

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0–1	0–1
	1	1–0	1–0
4	A1 A0		
	0 0	0–1–2–3	0–1–2–3
	0 1	1–2–3–0	1–0–3–2
	1 0	2–3–0–1	2–3–0–1
	1 1	3–0–1–2	3–2–1–0
8	A2 A1 A0		
	0 0 0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0 0 1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0 1 0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0 1 1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1 0 0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1 0 1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1 1 0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1 1 1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0

- Note:
1. For a burst length of two, A1–Ai selects the two–data–element block; A0 selects the first access within the block.
 2. For a burst length of four, A2–Ai selects the four–data–element block; A0–A1 selects the first access within the block.
 3. For a burst length of eight, A3–Ai selects the eight–data–element block; A0–A2 selects the first access within the block.
 4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n , and the latency is m clocks, the data will be available nominally coincident with clock edge $n + m$. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A11 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9–A11 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7–A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Table 2

CAS LATENCY AND FREQUENCY

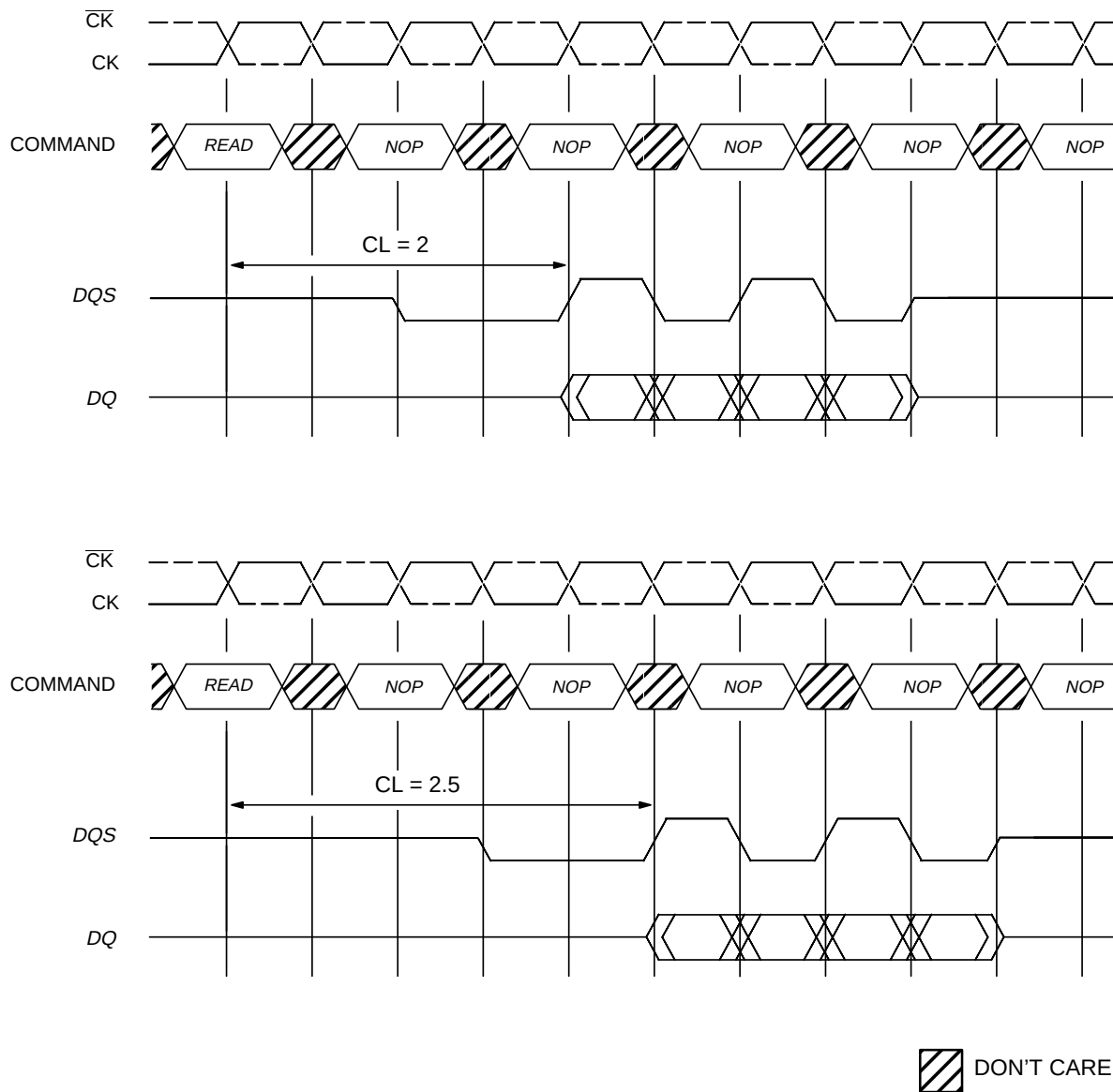
	MAXIMUM OPERATING FREQUENCY (MHz)*		
	DDR–266A	DDR–266B	DDR–200
CL2	133	100	100
CL2.5	143	133	125

* Values are nominal (i.e., may have been rounded off; exact tCK should be used).

Terminology Definitions. The following are definitions of the terms DDR–200 & DDR–266 as used in this specification

DDR–200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The corresponding nominal data rate is 200 MHz.

DDR–266n: Speed grades for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is 266 MHz. Devices designated as DDR–266B will operate with CAS Latency = 2.5 clock periods at a 133 MHz clock frequency. Devices designated as DDR–266A will operate with CAS Latency = 2 clock periods at a 133 MHz clock frequency.



Burst Length = 4 in the cases shown
Shown with nominal t_{DQSCK} , and t_{DQSQ}

Figure 2
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional), and $\overline{QFC}$ output enable/disable (optional). These functions are controlled via the bits shown in Figure 3. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point-to-point environments. I-V curves for the normal drive strength are included in this document; the curves for the weak drive strength will be included in a future revision.

$\overline{QFC}$ Enable/Disable

The $\overline{QFC}$ signal might be provided by certain vendors to control FET switches used to isolate module loads from the system memory bus at times when the given module is not being accessed.

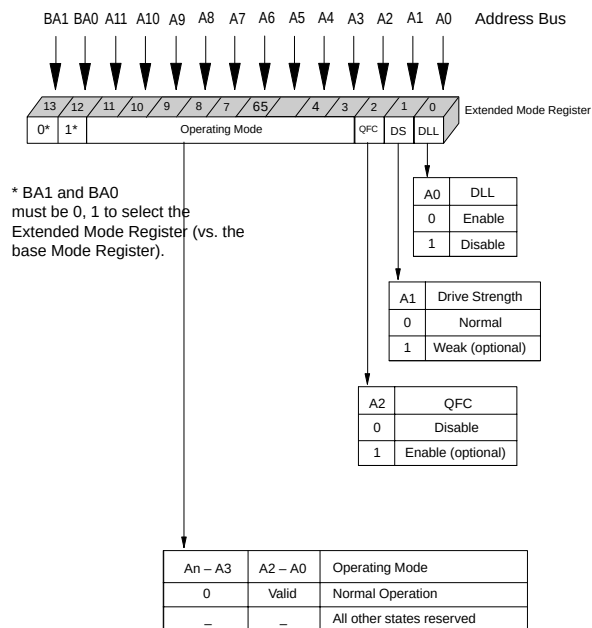


Figure 3
EXTENDED MODE REGISTER
DEFINITION

COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a _ Commands

(Notes: 1)

NAME (Function)	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7
MODE REGISTER SET	L	L	L	L	Op-Code	2

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.

2. BA0–BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0–BA1 are reserved; A0–A11 provide the op-code to be written to the selected Mode Register.
3. BA0–BA1 provide bank address and A0–A11 provide row address.
4. BA0–BA1 provide bank address; A0–Ai provide column address (where i = 7 for x16, 8 for x8 and 9 for x4); A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. Deselect and NOP are functionally interchangeable.

TRUTH TABLE 1b _ DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

NOTE: 1. Used to mask write data, provided coincident with the corresponding data.

DESELECT

The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an DDR SDRAM which is selected ($\overline{S}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A11. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 64 Mb DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of 15.6 μ s (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is $9 * 15.6 \mu$ s (140.4 μ s).

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command (Figure 4), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (pre-charged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

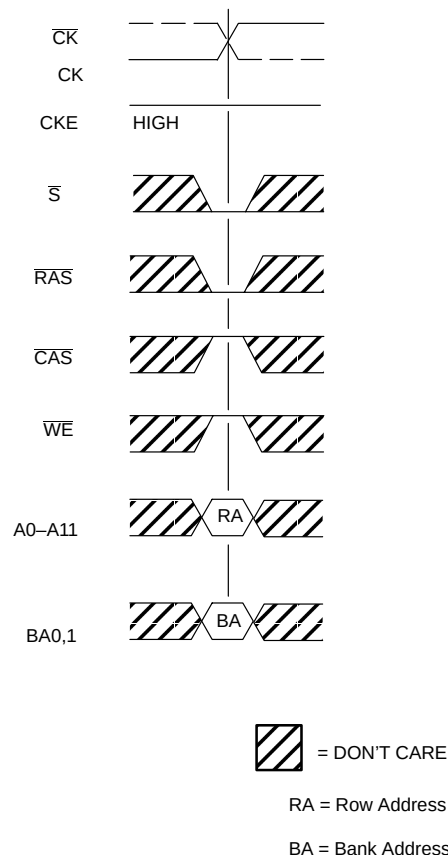


Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

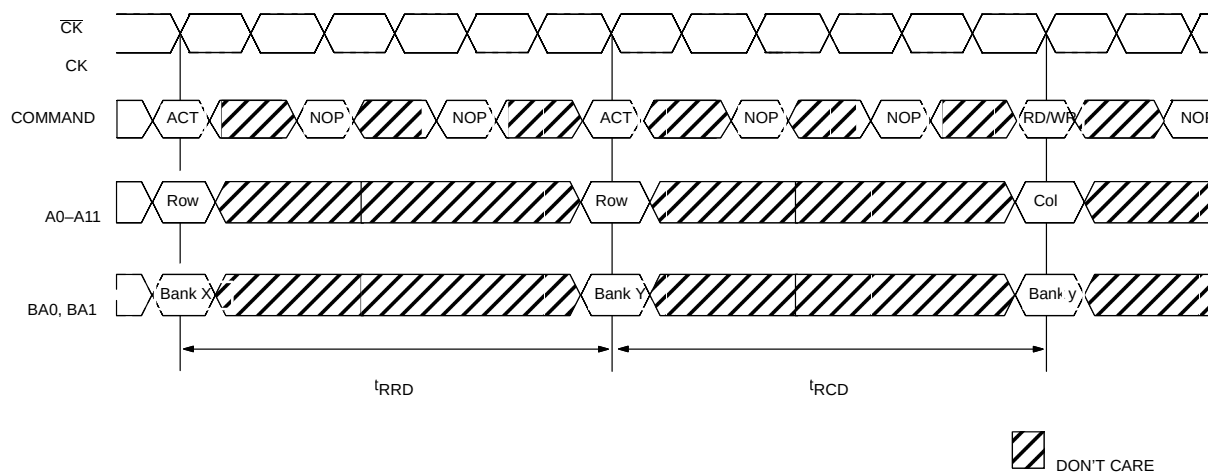


Figure 5
tRCD and tRRD Definition

Reads

READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 7 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the $2n$ prefetch architecture). This is shown in Figure 8. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 9. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 10.

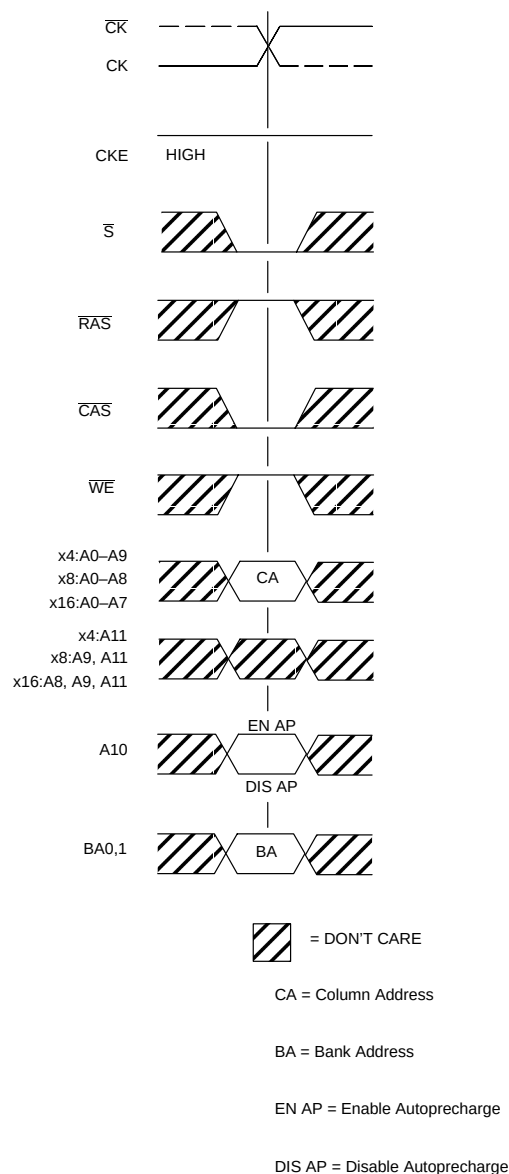
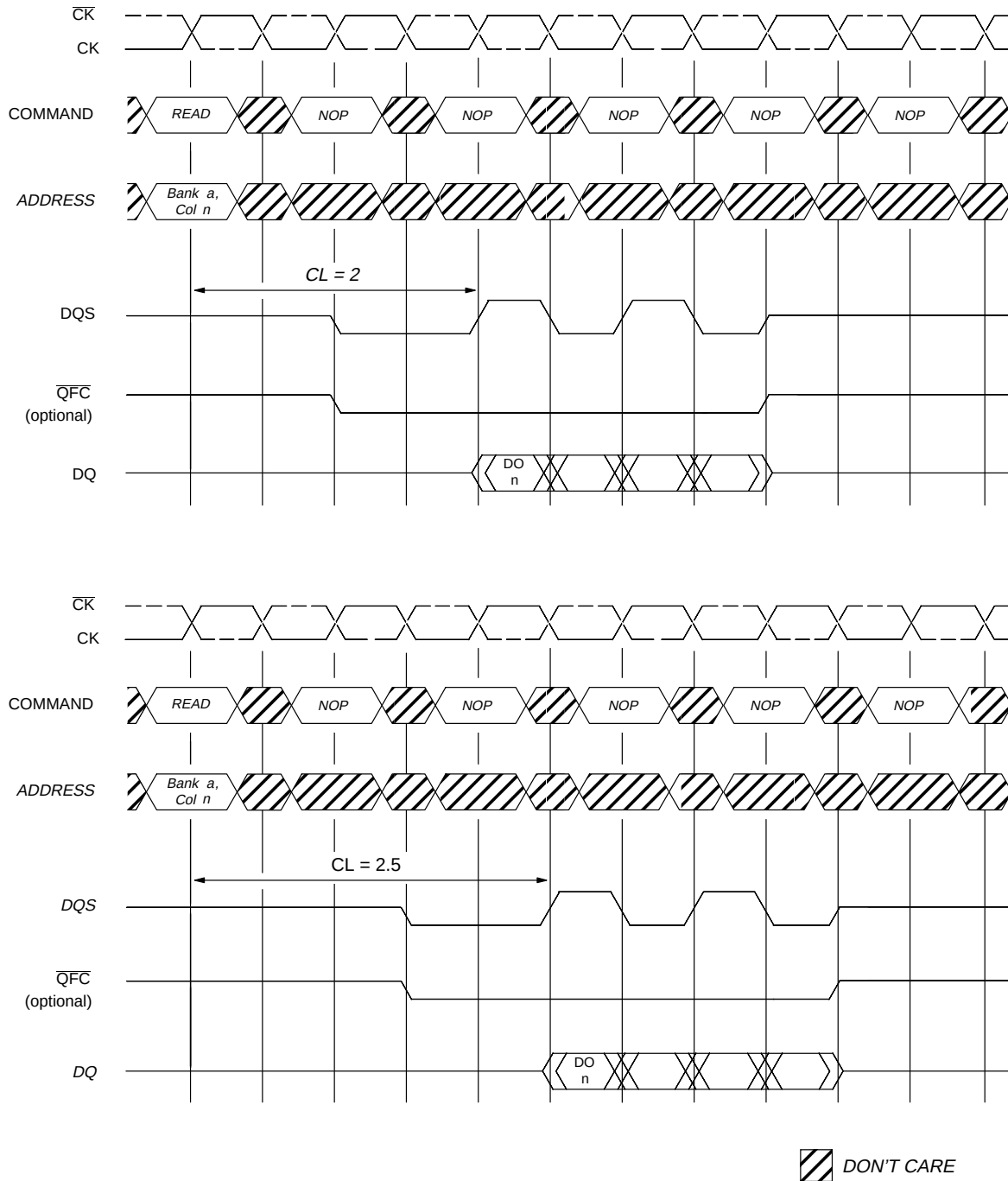
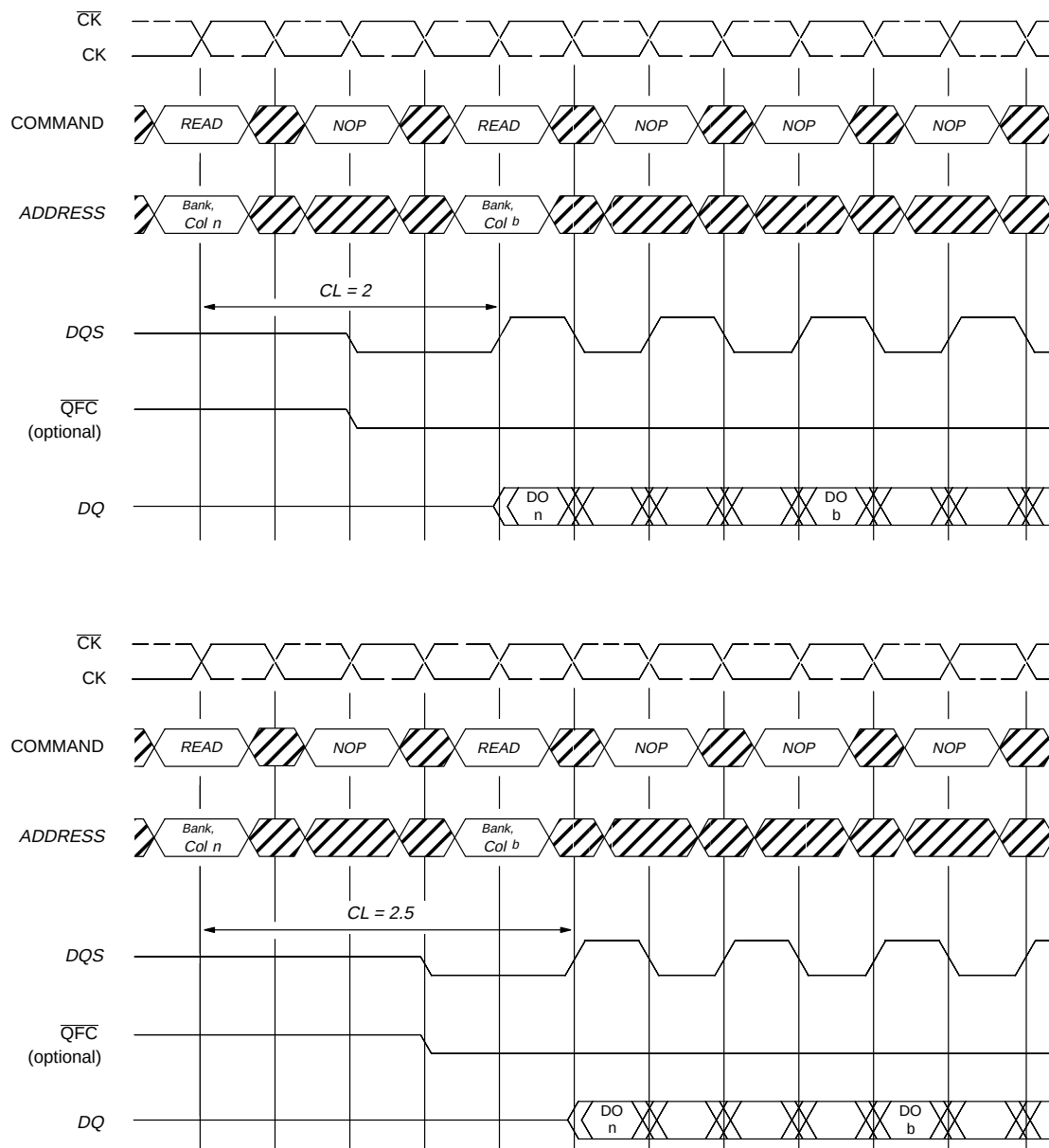


Figure 6
READ COMMAND



DO n = Data Out from column n
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 7
READ BURST – REQUIRED CAS LATENCIES



 DON'T CARE

DO n (or b) = Data Out from column n (or column b)

Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

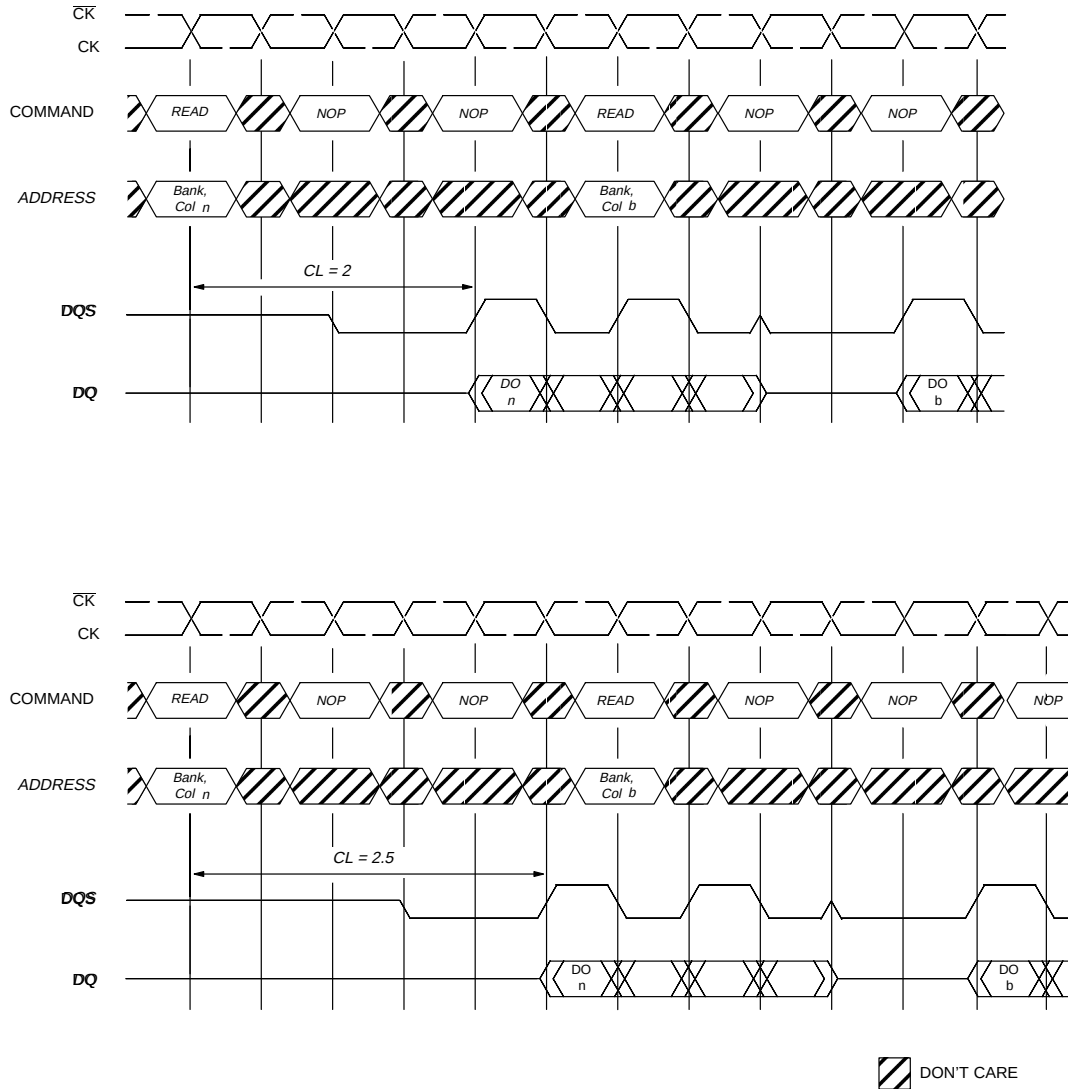
3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

Shown with nominal t_{DQSCK} , and t_{DQSQ}

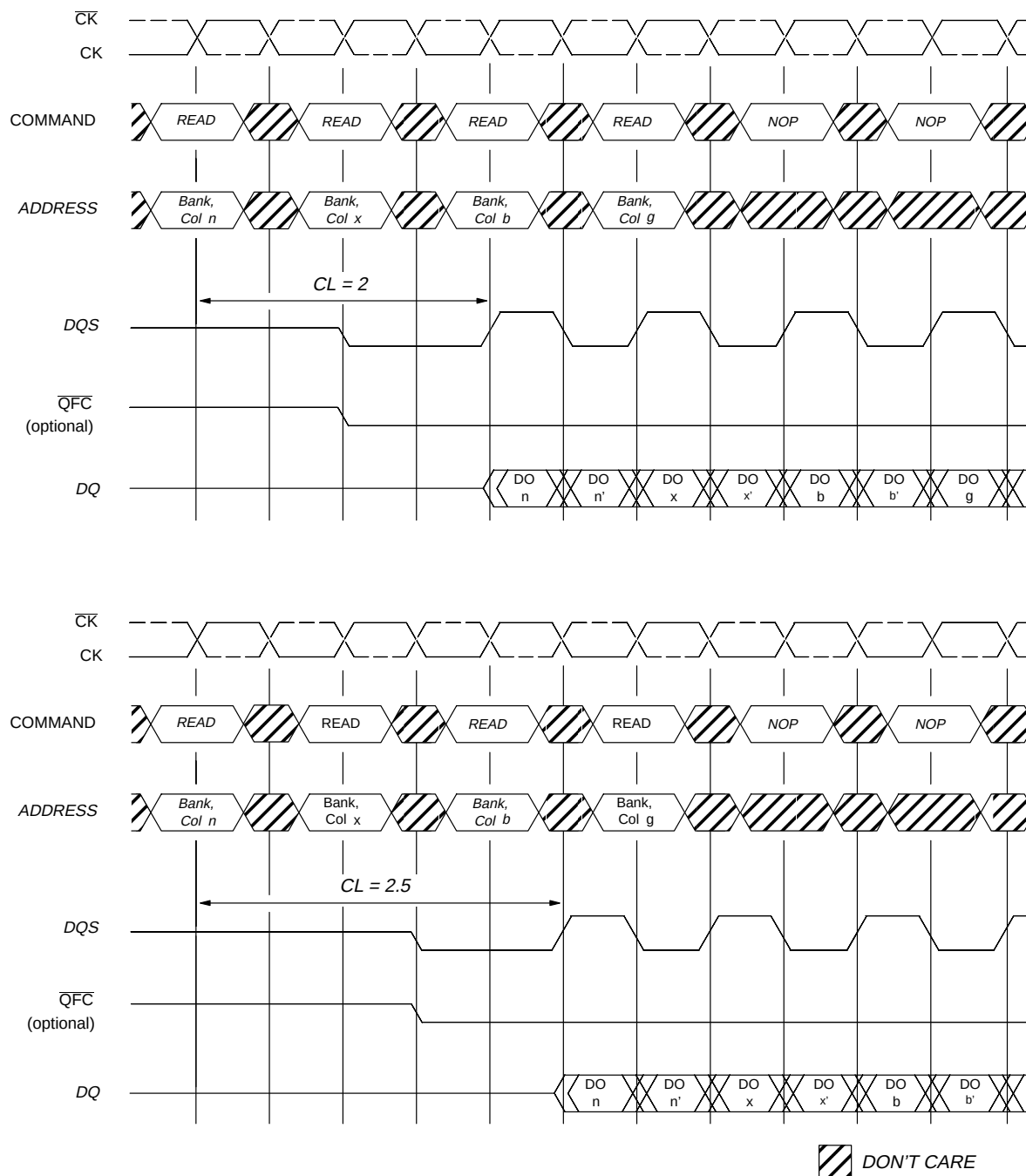
Read commands shown must be to the same device

Figure 8
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
 Burst Length = 4
 3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)
 Shown with nominal tDQSK, and tDQSQ

Figure 9
NONCONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n, etc. = Data Out from column n, etc.
 n', etc. = the next Data Out following DO n, etc. according to the programmed burst order
 Burst Length = 2, 4 or 8 in cases shown
 Reads are to active rows in any banks
 Shown with nominal tDQSCK, and tDQSQ

Figure 10
RANDOM READ ACCESSES – REQUIRED CAS LATENCIES

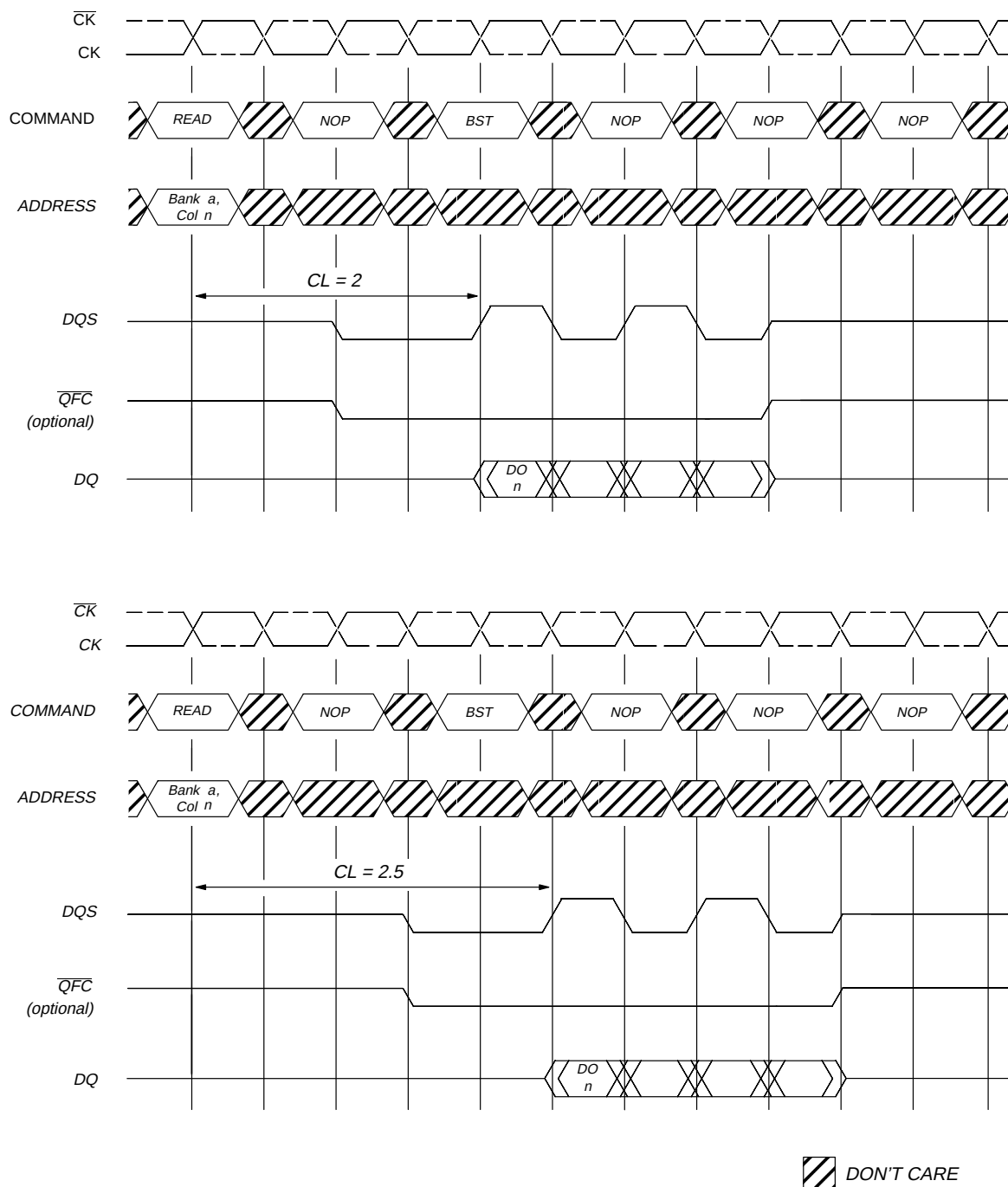
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 11. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs.

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued.

If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 12. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITES).

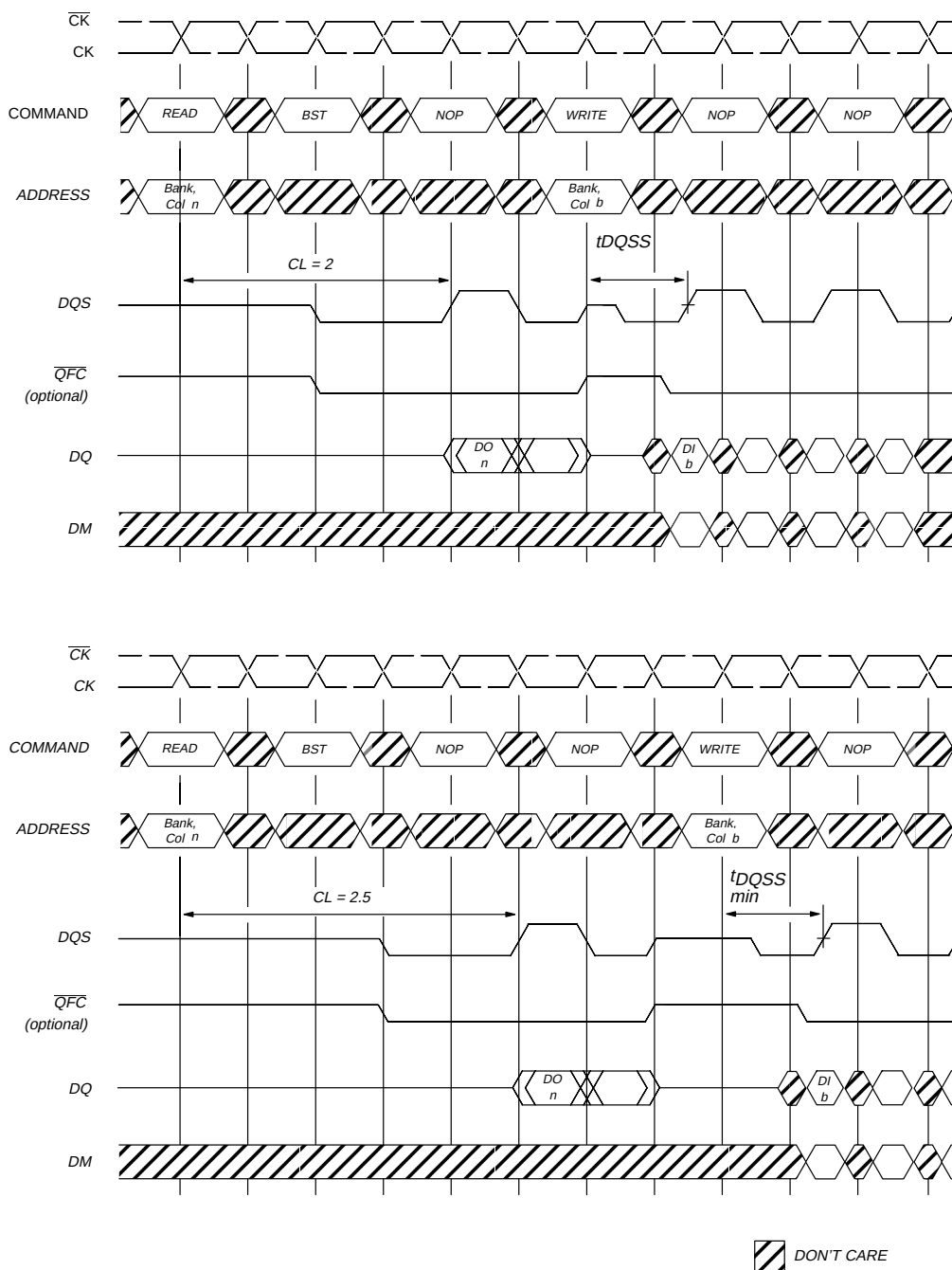
A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the $2n$ prefetch architecture). This is shown in Figure 13 for READ latencies of 2, and 2.5. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.



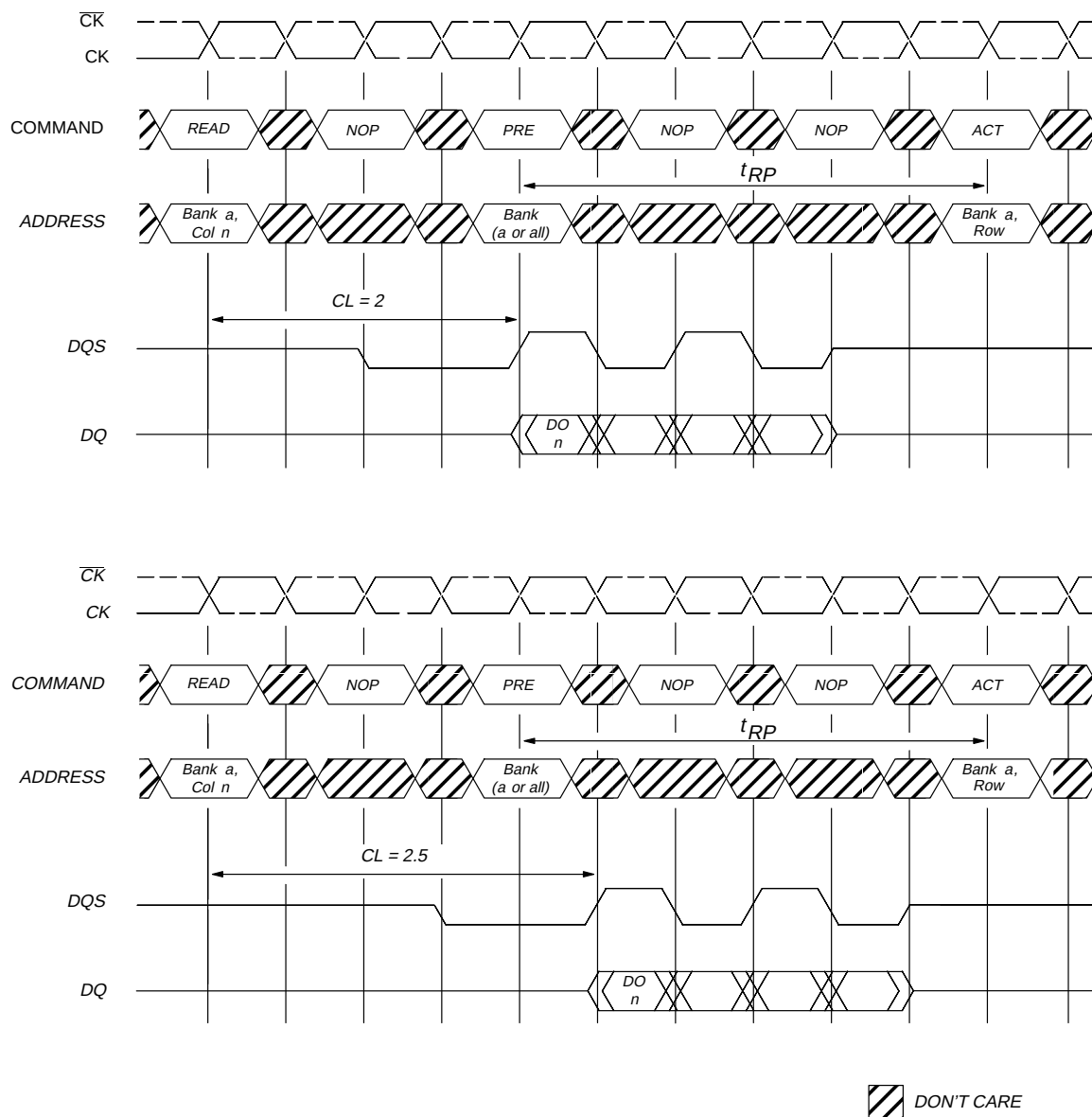
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal tDQSCK, and tDQSQ

Figure 11
TERMINATING A READ BURST – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
 Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
 1 subsequent element of Data Out appears in the programmed order following DO n
 Data In elements are applied following DI b in the programmed order
 Shown with nominal tDQSC, and tDQSQ

Figure 12
READ TO WRITE – REQUIRED CAS LATENCIES



DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Shown with nominal t_{DQSCK}, and t_{DQSQ}

Figure 13
READ TO PRECHARGE – REQUIRED CAS LATENCIES

Writes

WRITE bursts are initiated with a WRITE command, as shown in Figure 14.

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle), so most of the WRITE diagrams that follow are drawn for the two extreme cases (i.e., t_{DQSS} MIN and t_{DQSS} MAX). Figures 15 and 16 show the two extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the $2n$ prefetch architecture). Figures 17 and 18 show concatenated bursts of 4. An example of nonconsecutive WRITES is shown in Figure 19. Full-speed random write accesses within a page or pages can be performed as shown in Figures 20 and 21.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, t_{WTR} should be met as shown in Figures 22 and 23.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 24–27. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the in-

ternal array, and any subsequent data-in must be masked with DM, as shown in Figures 24–27.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, t_{WR} should be met as shown in Figures 28 and 29.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 30–33.

Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figures 30–33. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

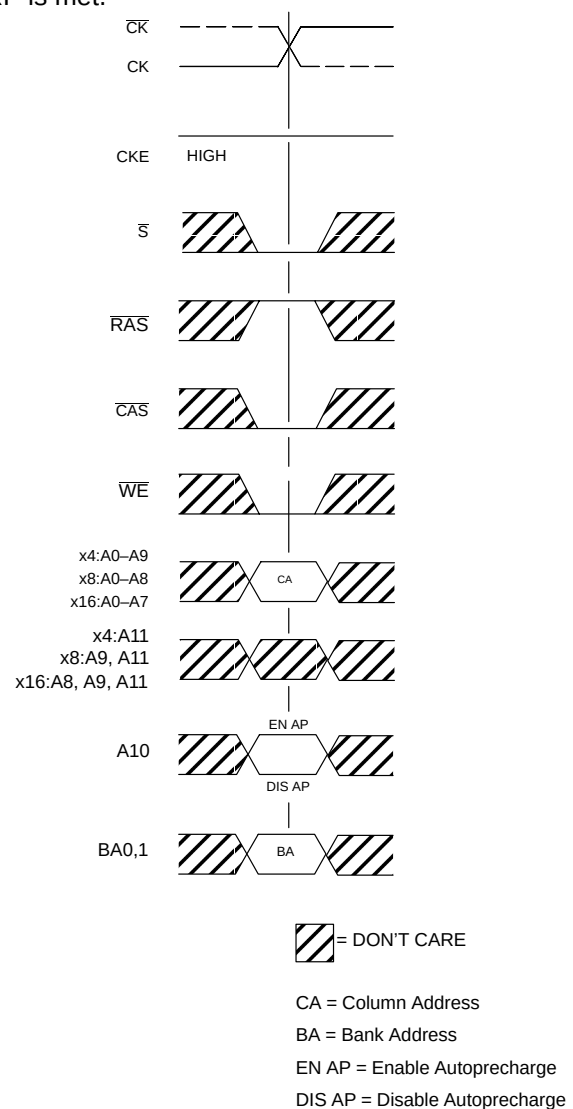
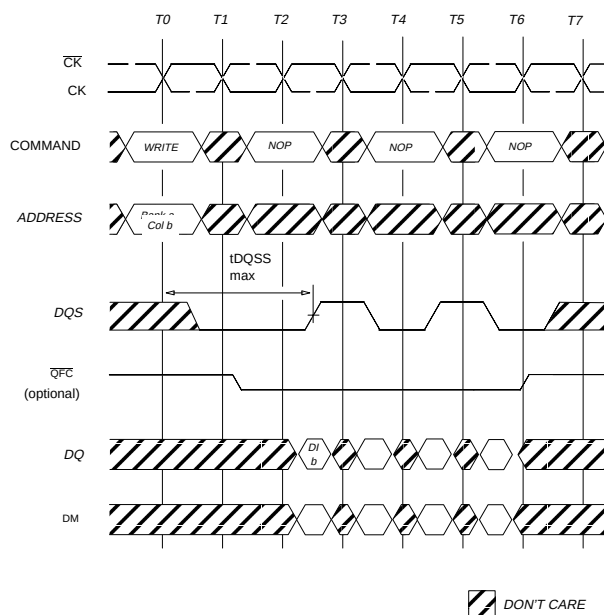
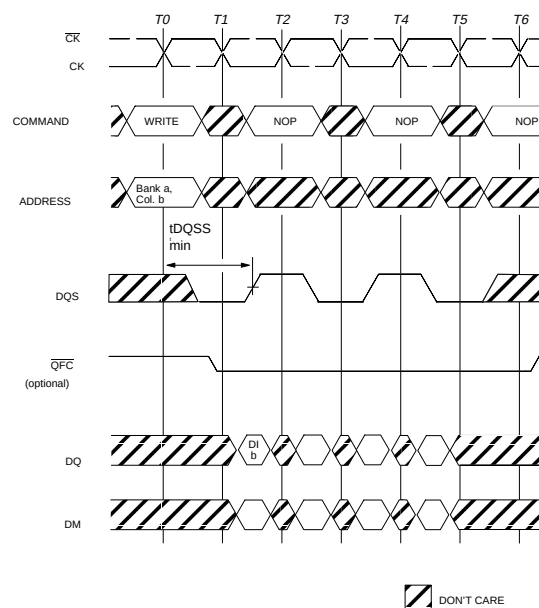


Figure 14
WRITE COMMAND



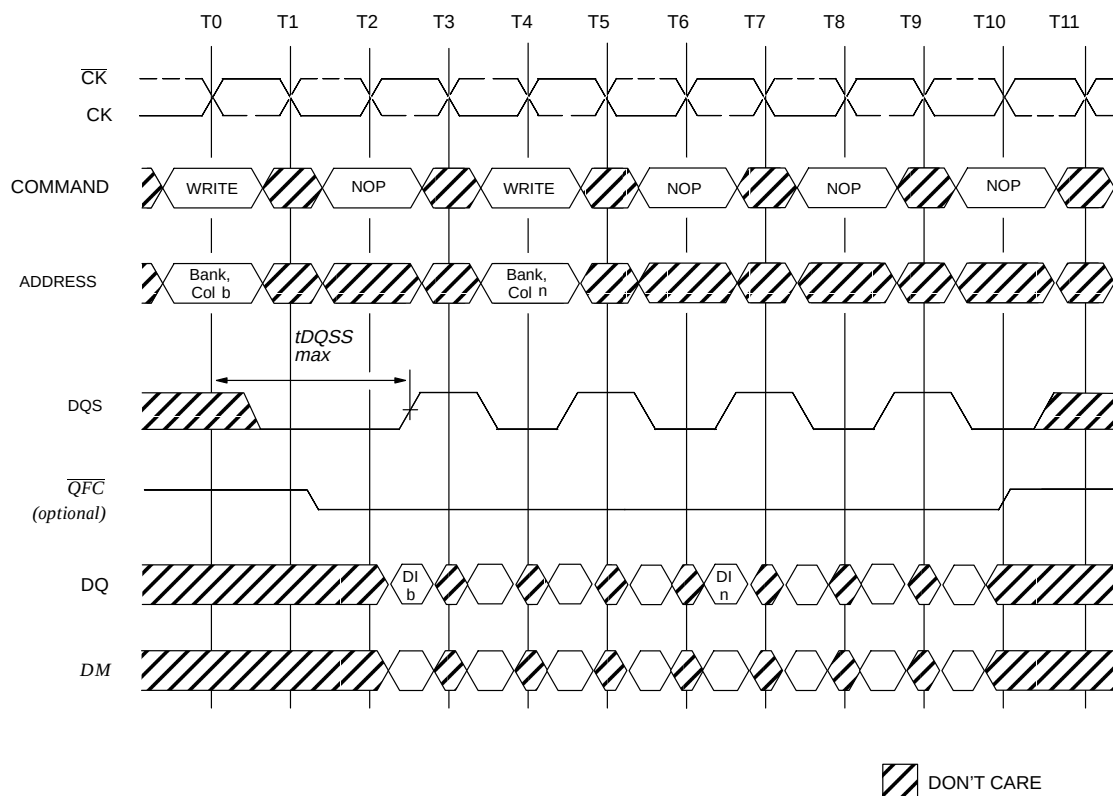
DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 15
WRITE TO WRITE – MAX DQSS



DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
Depending on external components, QFC operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 16
WRITE TO WRITE – MIN DQSS



DI b, etc = Data In for column b, etc.

3 subsequent elements of Data In are applied in the programmed order following DI b

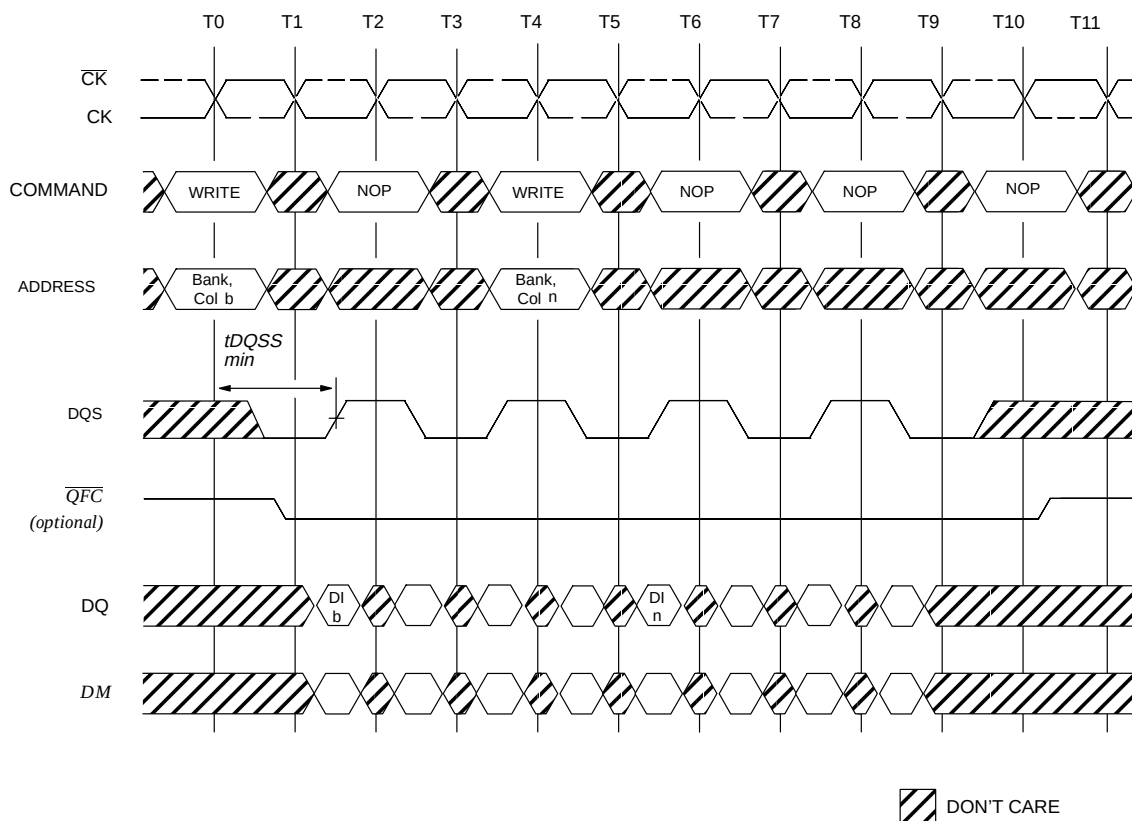
3 subsequent elements of Data In are applied in the programmed order following DI n

A noninterrupted burst of 4 is shown

For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)

For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 17
WRITE TO WRITE – MAX DQSS



DI b, etc. = Data In for column b, etc.

3 subsequent elements of Data In are applied in the programmed order following DI b

3 subsequent elements of Data In are applied in the programmed order following DI n

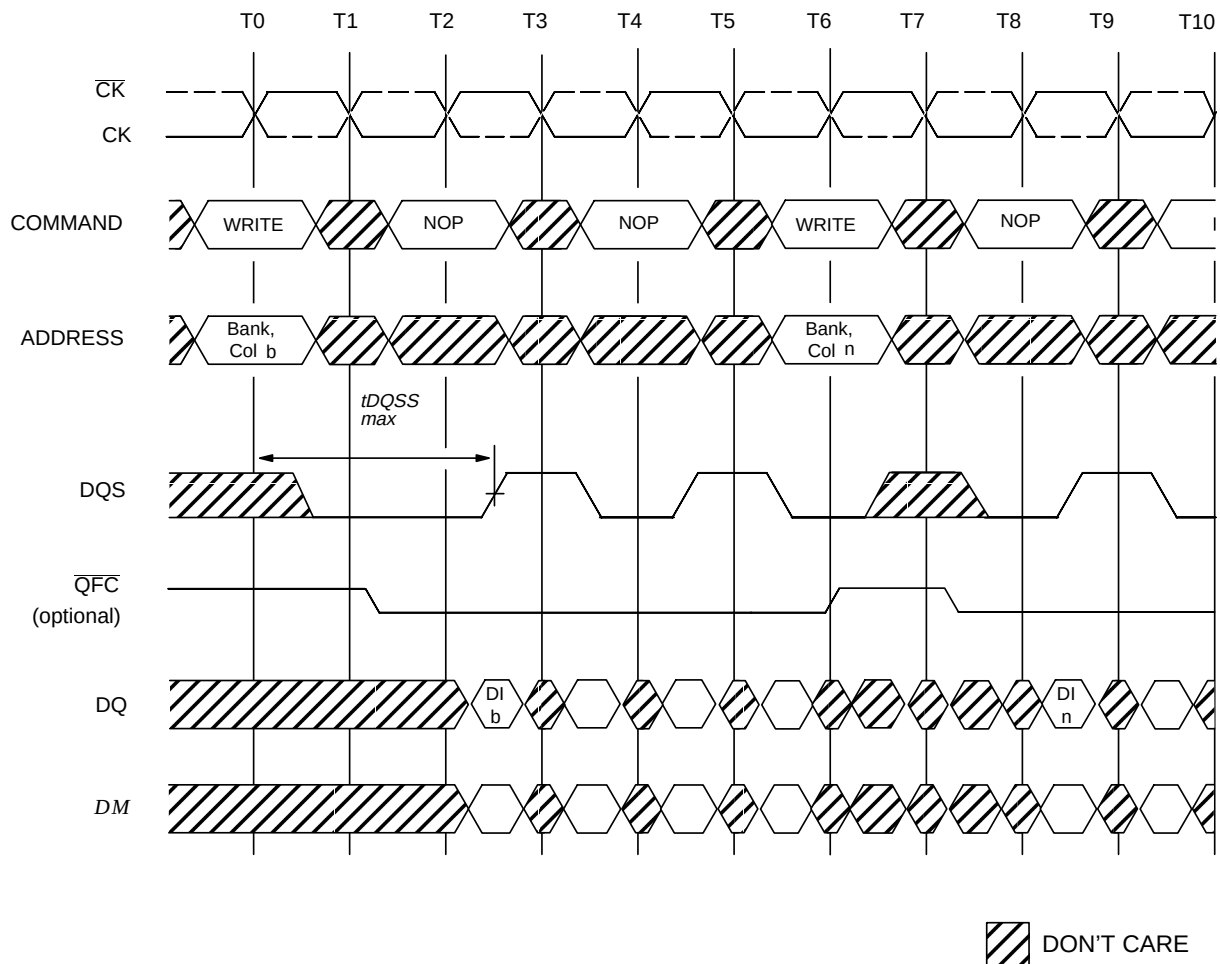
A noninterrupted burst of 4 is shown

For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)

Depending on external components, $\overline{QFC}$ operation with min t_{DQSS} might not be possible at the maximum operating frequency of the device

For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 18
WRITE TO WRITE – MIN DQSS,



DI b, etc. = Data In for column b, etc.

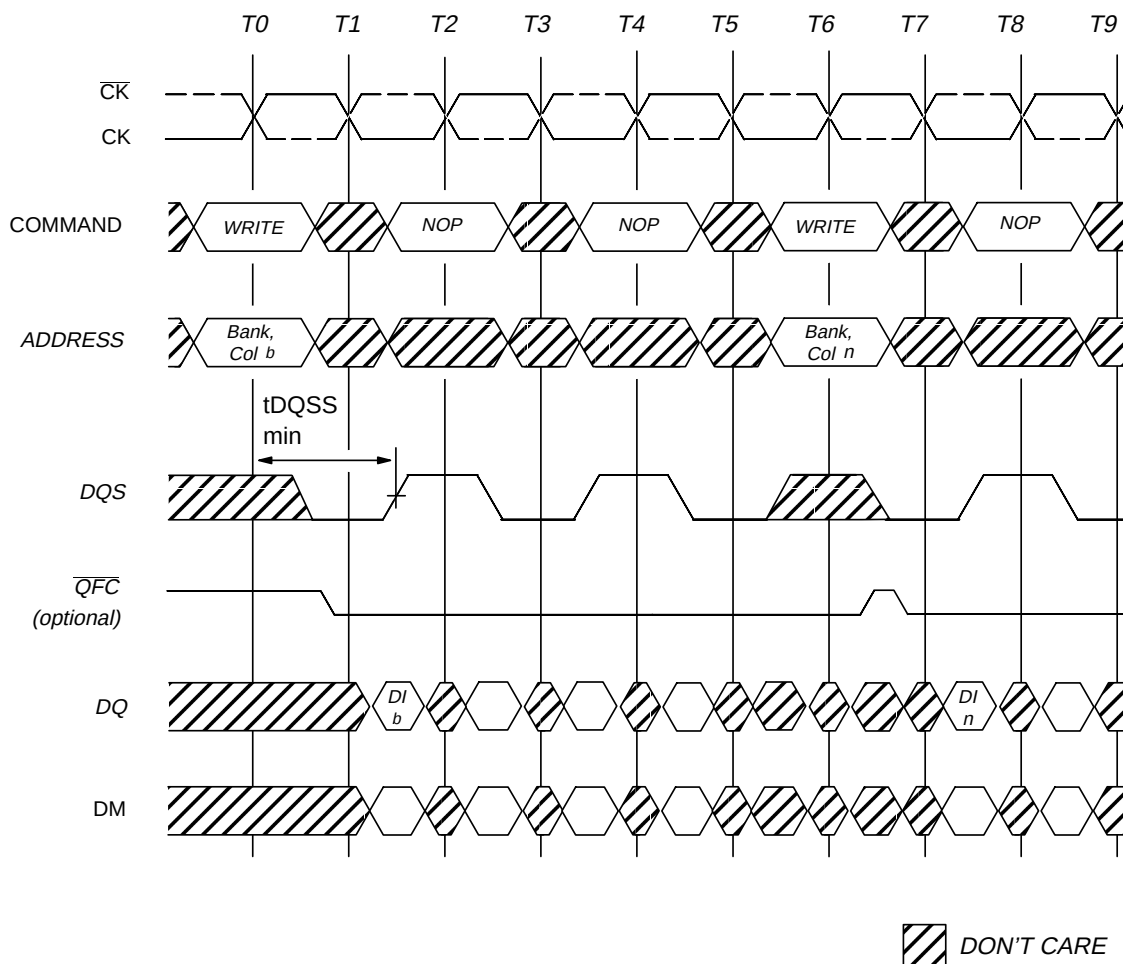
3 subsequent elements of Data In are applied in the programmed order following DI b

3 subsequent elements of Data In are applied in the programmed order following DI n

A noninterrupted burst of 4 is shown

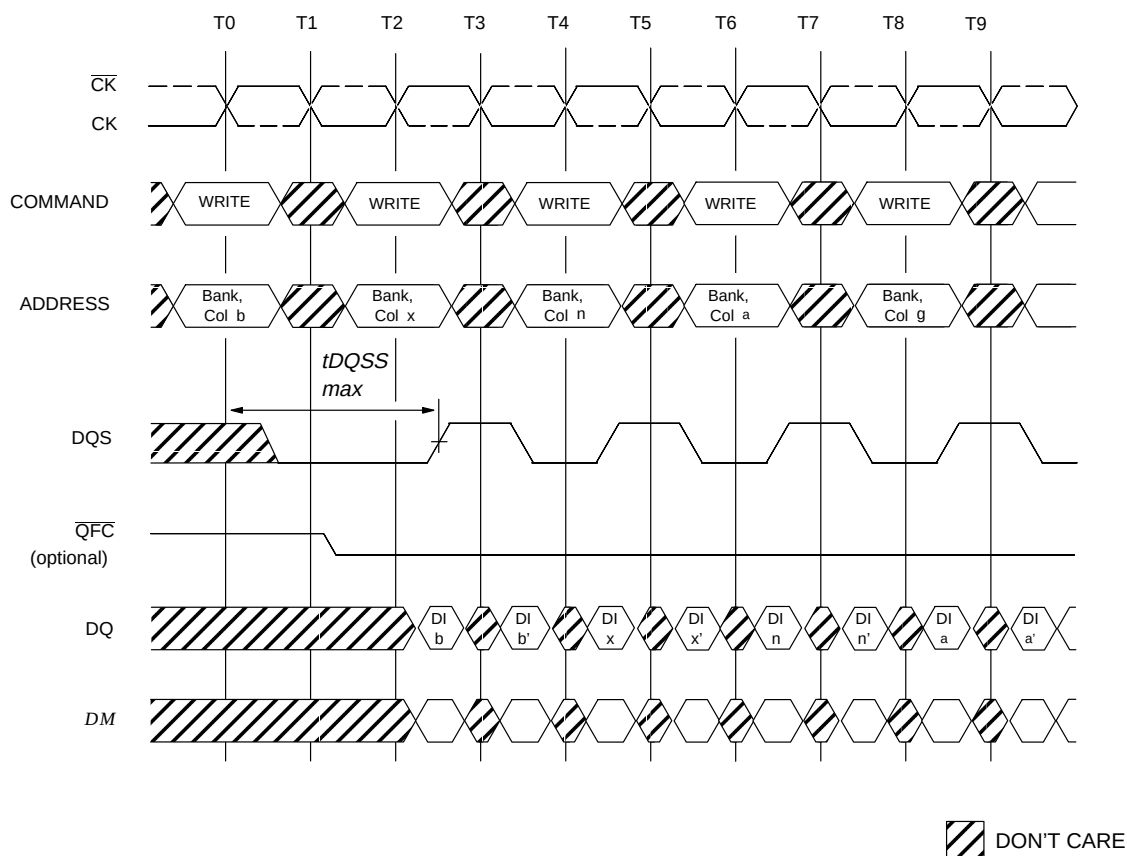
Each Write command may be to any bank and may be to the same or different devices

Figure 19 a
WRITE TO WRITE – MAX DQSS, NONCONSECUTIVE



*DI b, etc. = Data In for column b. etc.
 3 subsequent elements of Data In are applied in the programmed order following DI b
 3 subsequent elements of Data In are applied in the programmed order following DI n
 A noninterrupted burst of 4 is shown
 Each Write command may be to any bank, and may be to the same or different devices
 Depending on external components, $\overline{QFC}$ operation with min t_{DQSS} might not be possible
 at the maximum operating frequency of the device*

Figure 19 b
WRITE TO WRITE – MIN DQSS, NONCONSECUTIVE



DI b, etc. = Data In for column b, etc.

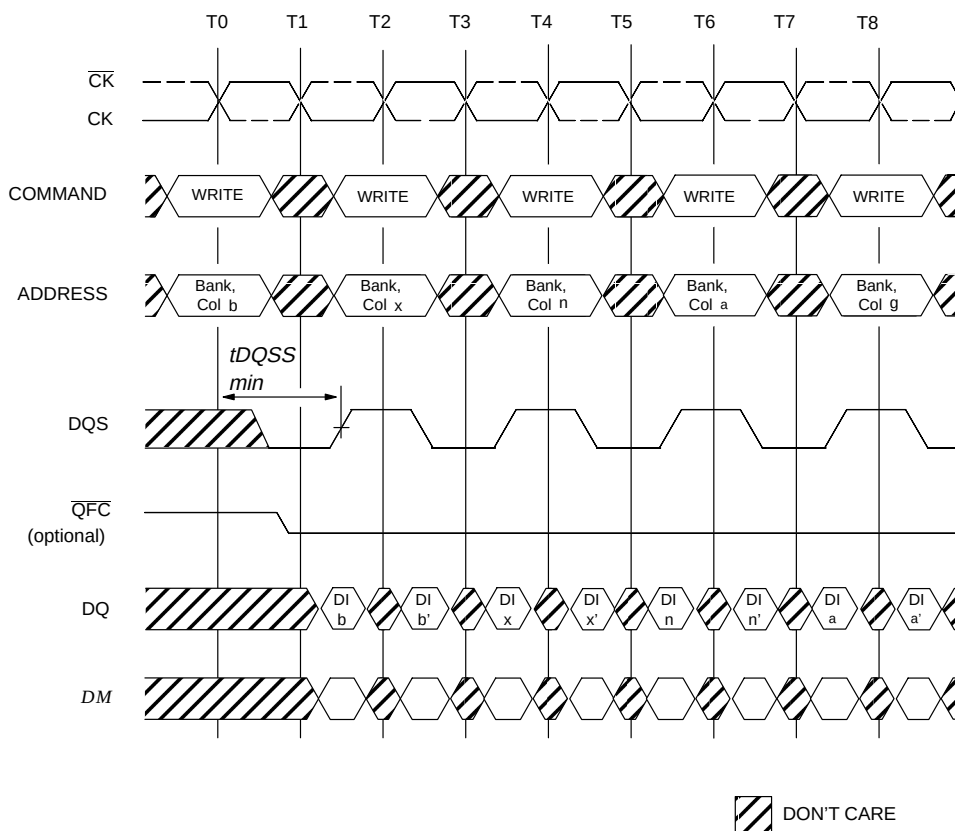
b', etc. = the next Data In following DI b, etc. according to the programmed burst order

Programmed Burst Length = 2, 4 or 8 in cases shown

For system configurations using QFC: the Write commands shown must be to the same device (but can be to any bank within the device)

For system configurations not using QFC: each Write command may be to any bank and may be to the same or different devices

Figure 20
RANDOM WRITE CYCLES – MAX DQSS



DI b, etc. = Data In for column b, etc.

b', etc. = the next Data In following DI b, etc., according to the programmed burst order

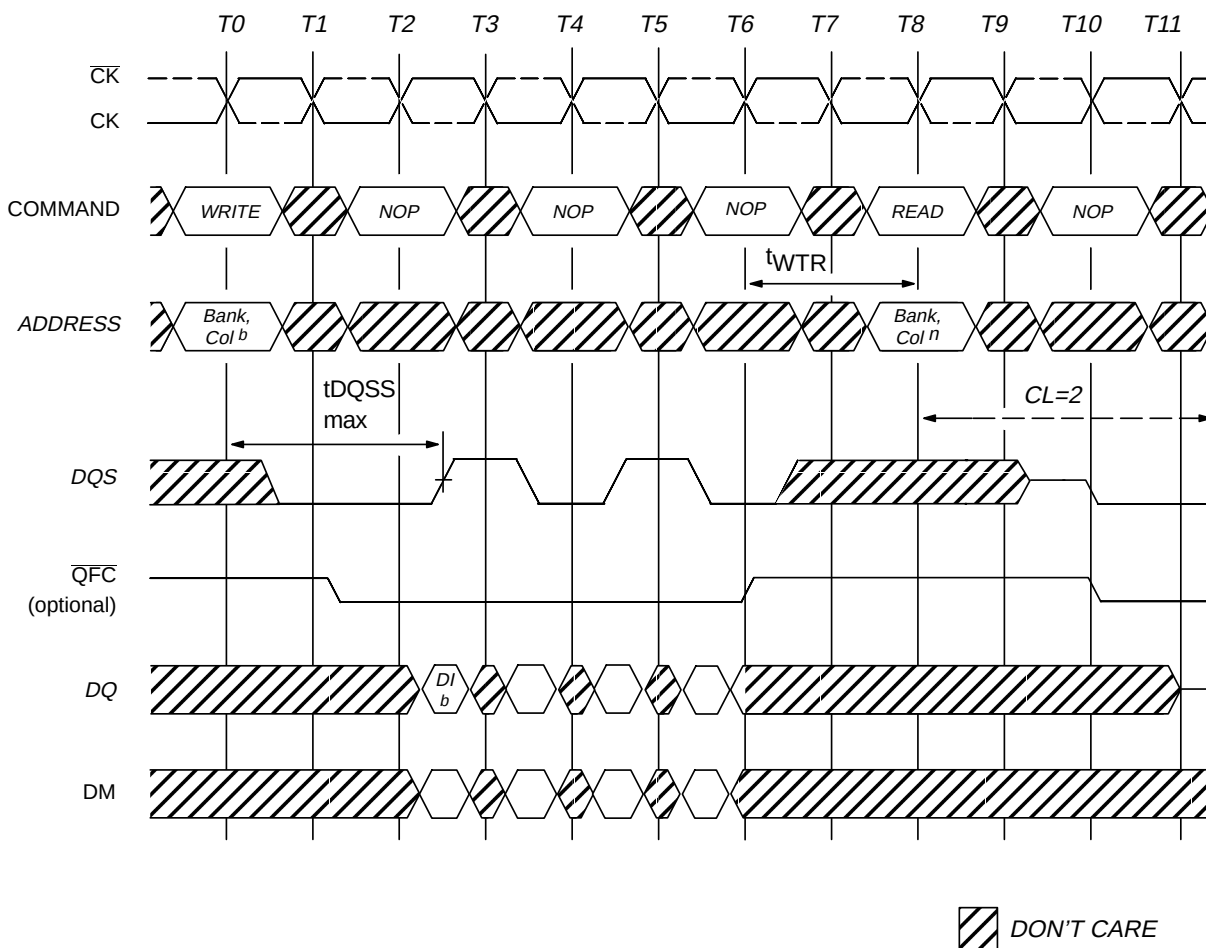
Programmed Burst Length = 2, 4 or 8 in cases shown

For system configurations using $\overline{QFC}$: the Write commands shown must be to the same device (but can be to any bank within the device)

Depending on external components, $\overline{QFC}$ operation with min t_{DQSS} might not be possible at the maximum operating frequency of the device

For system configurations not using $\overline{QFC}$: each Write command may be to any bank and may be to the same or different devices

Figure 21
RANDOM WRITE CYCLES – MIN DQSS



DI_b = Data In for column b

3 subsequent elements of Data In are applied in the programmed order following DI_b

A non-interrupted burst of 4 is shown

t_{WTR} is referenced from the first positive CK edge after the last Data In pair

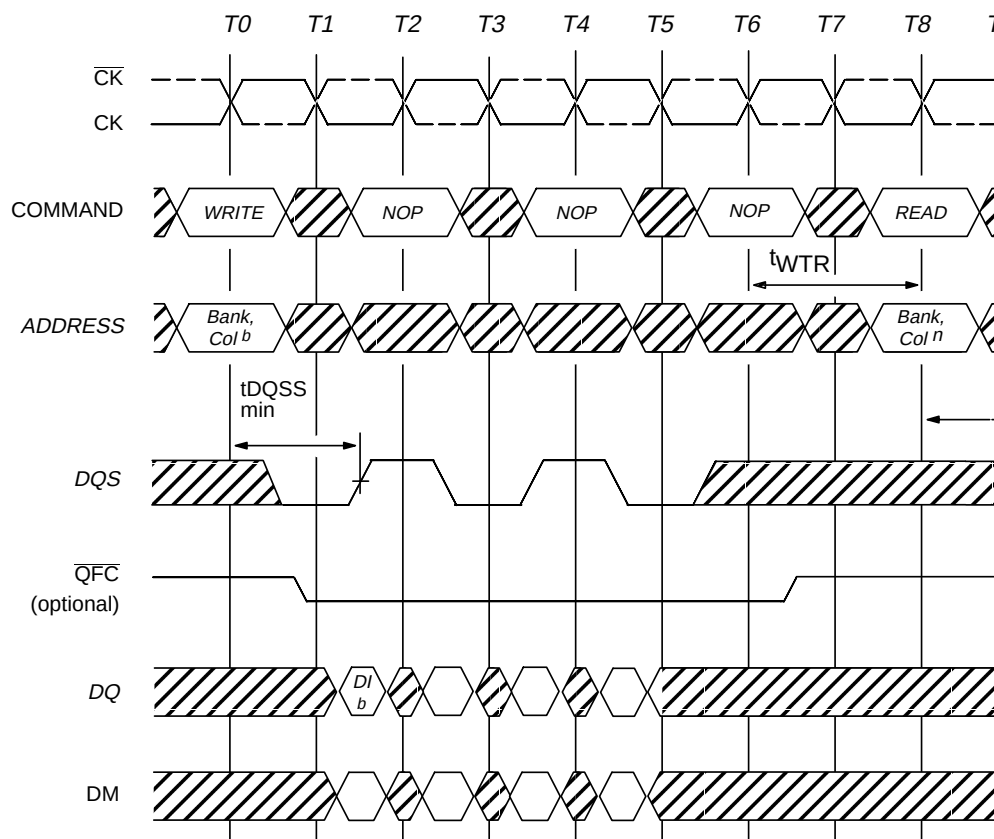
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands may be to any bank, and may be to the same or different devices

In the case where the READ and WRITE commands are to different devices, t_{WTR} need not be met, and the READ command can be applied earlier

$t_{WTR} = 2t_{CK}$ for optional $CL = 1.5$ (otherwise $t_{WTR} = 1 t_{CK}$)

Figure 22
WRITE TO READ – MAX DQSS, NONINTERRUPTING



DI b = Data In for column b

3 subsequent elements of Data In are applied in the programmed order following D.
A non-interrupted burst of 4 is shown

tWTR is referenced from the first positive CK edge after the last Data In pair

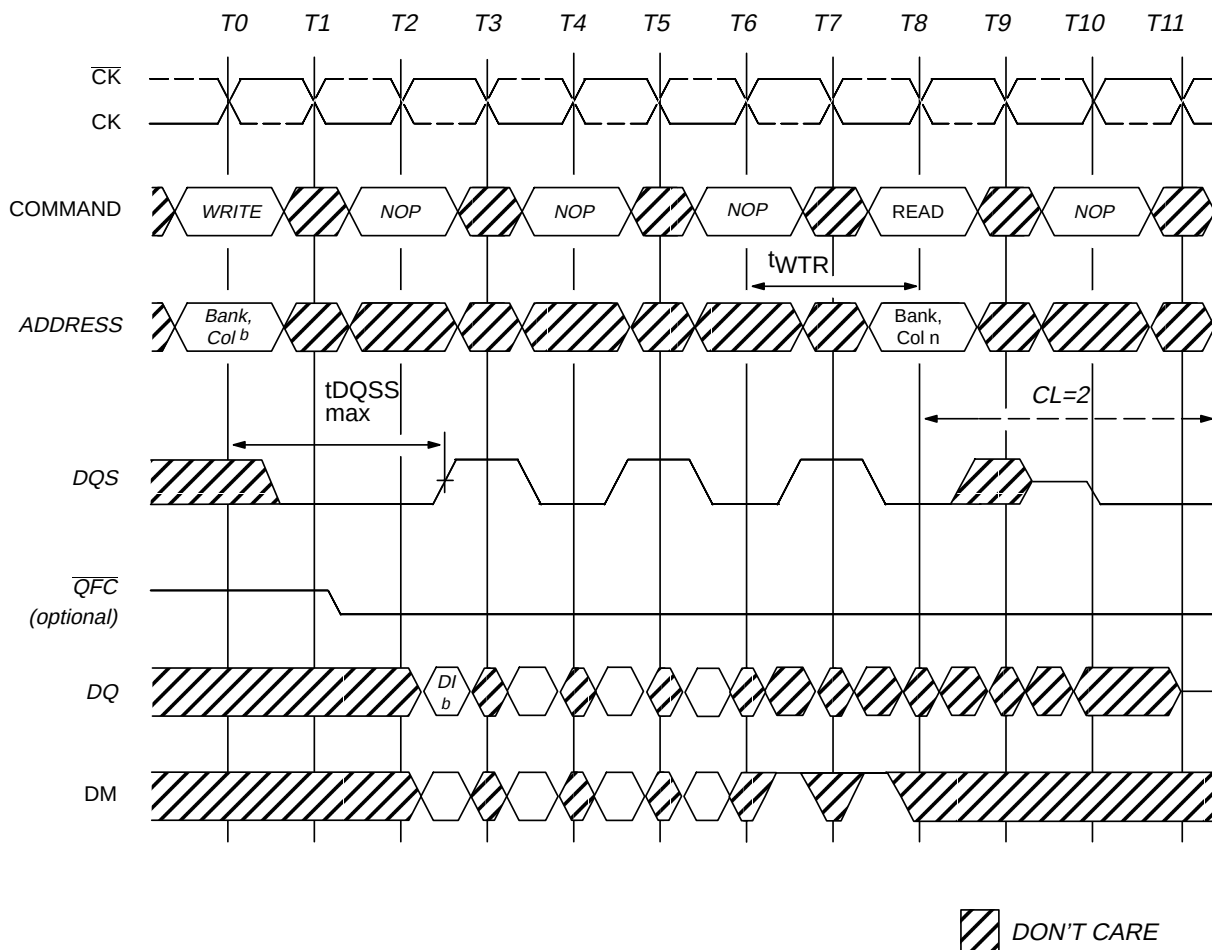
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands may be to any bank, and may be to the same or
In the case where the READ and WRITE commands are to different devices, tWTR
and the READ command can be applied earlier

tWTR = 2 tCK for optional CL = 1.5 (otherwise tWTR = 1 tCK)

Depending on external components, QFC operation with min tDQSS might not be p
at the maximum operating frequency of the device

Figure 23
WRITE TO READ – MIN DQSS, NON-INTERRUPTING



DI_b = Data In for column b

An interrupted burst of 8 is shown, 4 data elements are written

3 subsequent elements of Data In are applied in the programmed order following DI_b

t_{WTR} is referenced from the first positive CK edge after the last Data In pair

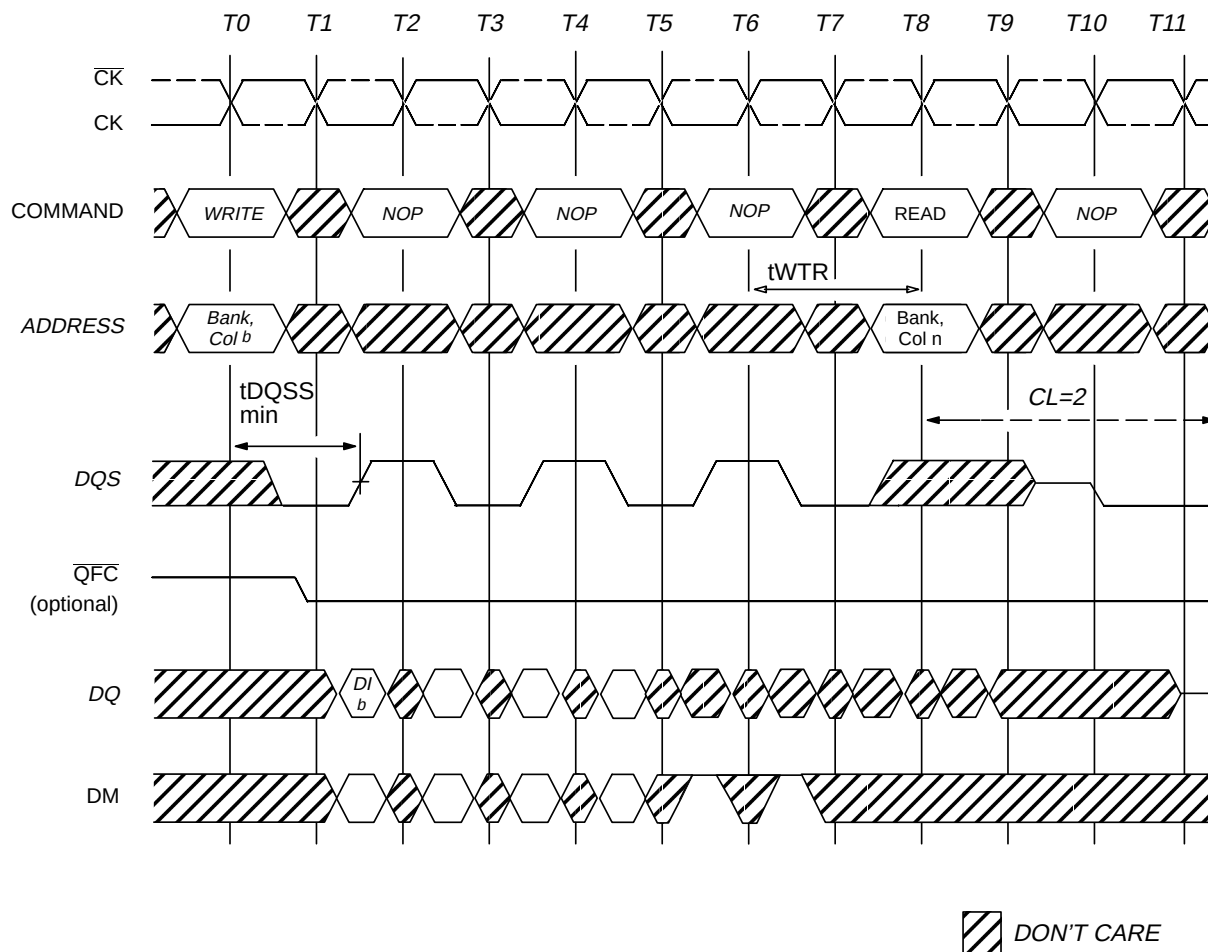
$t_{WTR} = 2t_{CK}$ for optional $CL = 1.5$ (otherwise $t_{WTR} = 1t_{CK}$)

The READ command masks the last two data elements in the burst

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same device but not necessarily to the same bank

Figure 24
WRITE TO READ – MAX DQSS, INTERRUPTING



DI b = Data In for column b

An interrupted burst of 8 is shown, 4 data elements are written

3 subsequent elements of Data In are applied in the programmed order following DI b

t_{WTR} is referenced from the first positive CK edge after the last desired Data In pair

$t_{WTR} = 2 t_{CK}$ for optional $CL = 1.5$ (otherwise $t_{WTR} = 1 t_{CK}$)

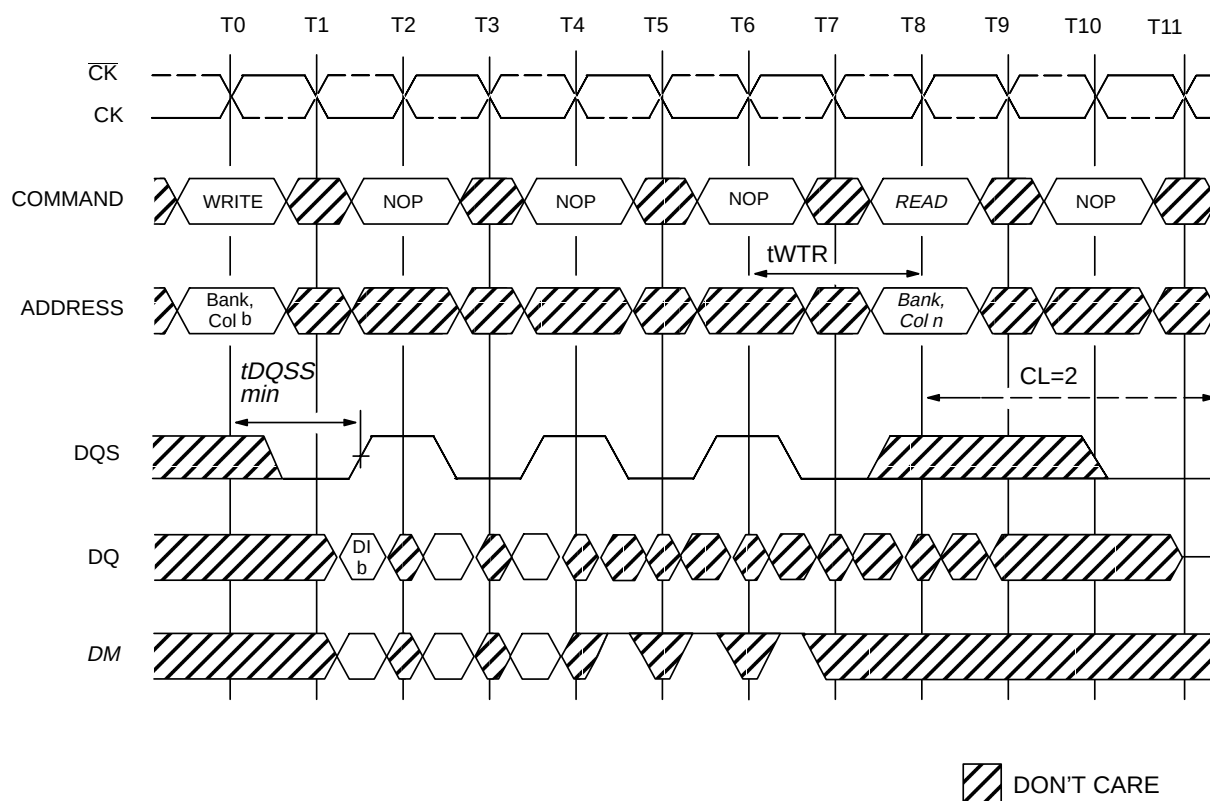
The READ command masks the last two data elements in the burst

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same device, but not necessarily to the same bank

Depending on external components, QFC operation with min t_{DQSS} might not be possible at the maximum operating frequency of the device

Figure 25
WRITE TO READ - MIN DQSS, INTERRUPTING



DI b = Data In for column b

An interrupted burst of 8 is shown, 3 data elements are written

2 subsequent elements of Data In are applied in the programmed order following DI b

t_{WTR} is referenced from the first positive CK edge after the last desired Data In pair (not the last desired data in element)

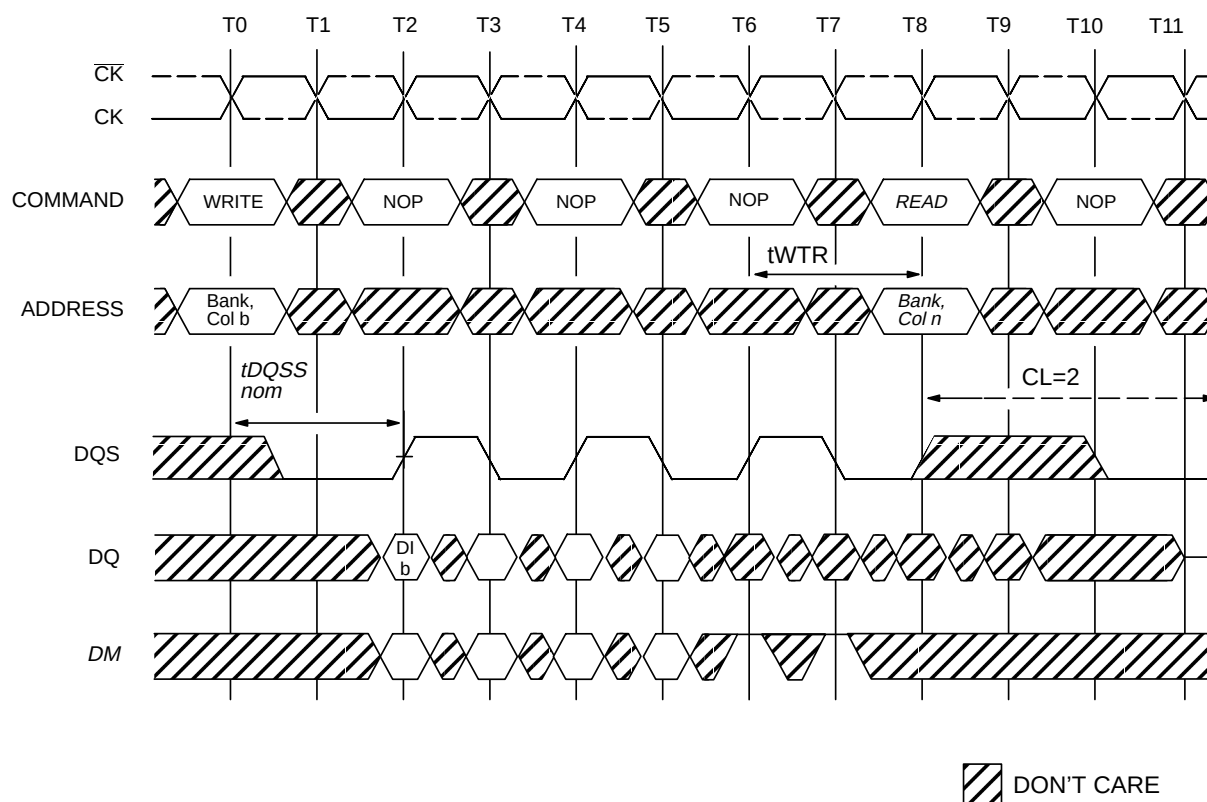
$t_{WTR} = 2t_{CK}$ for optional CL = 1.5 (otherwise $t_{WTR} = 1t_{CK}$)

The READ command masks the last two data elements in the burst

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are not necessarily to the same bank

Figure 26
WRITE TO READ – MIN DQSS, ODD NUMBER OF DATA, INTERRUPTING



DI b = Data In for column b

An interrupted burst of 8 is shown, 4 data elements are written

3 subsequent elements of Data In are applied in the programmed order following DI b

t_{WTR} is referenced from the first positive CK edge after the last desired Data In pair

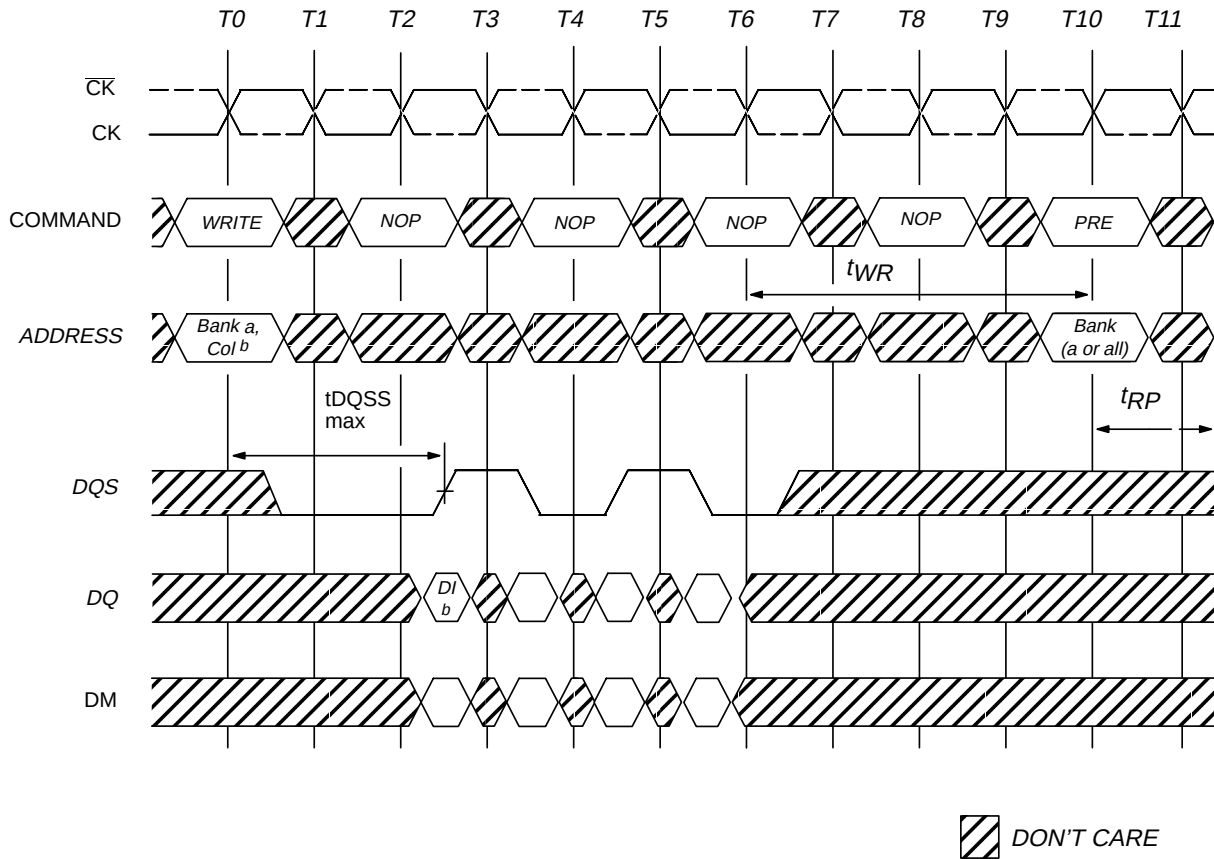
$t_{WTR} = 2t_{CK}$ for optional $CL = 1.5$ (otherwise $t_{WTR} = 1t_{CK}$)

The READ command masks the last two data elements in the burst

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are not necessarily to the same bank

Figure 27
WRITE TO READ – NOMINAL DQSS, INTERRUPTING



DI b = Data In for column b

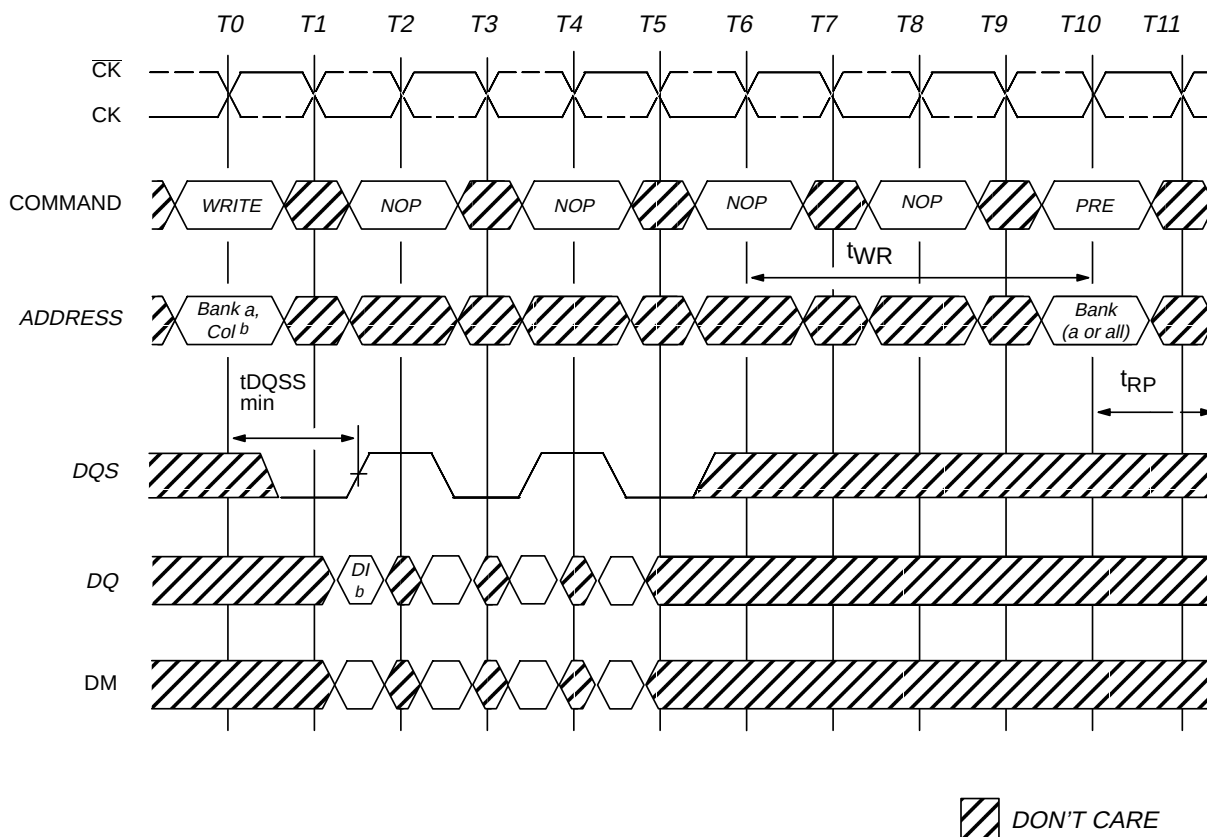
3 subsequent elements of Data In are applied in the programmed order following DI b

A noninterrupted burst of 4 is shown

t_{WR} is referenced from the first positive CK edge after the last Data In pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 28
WRITE TO PRECHARGE – MAX DQSS, NON-INTERRUPTING



DI b = Data In for column b

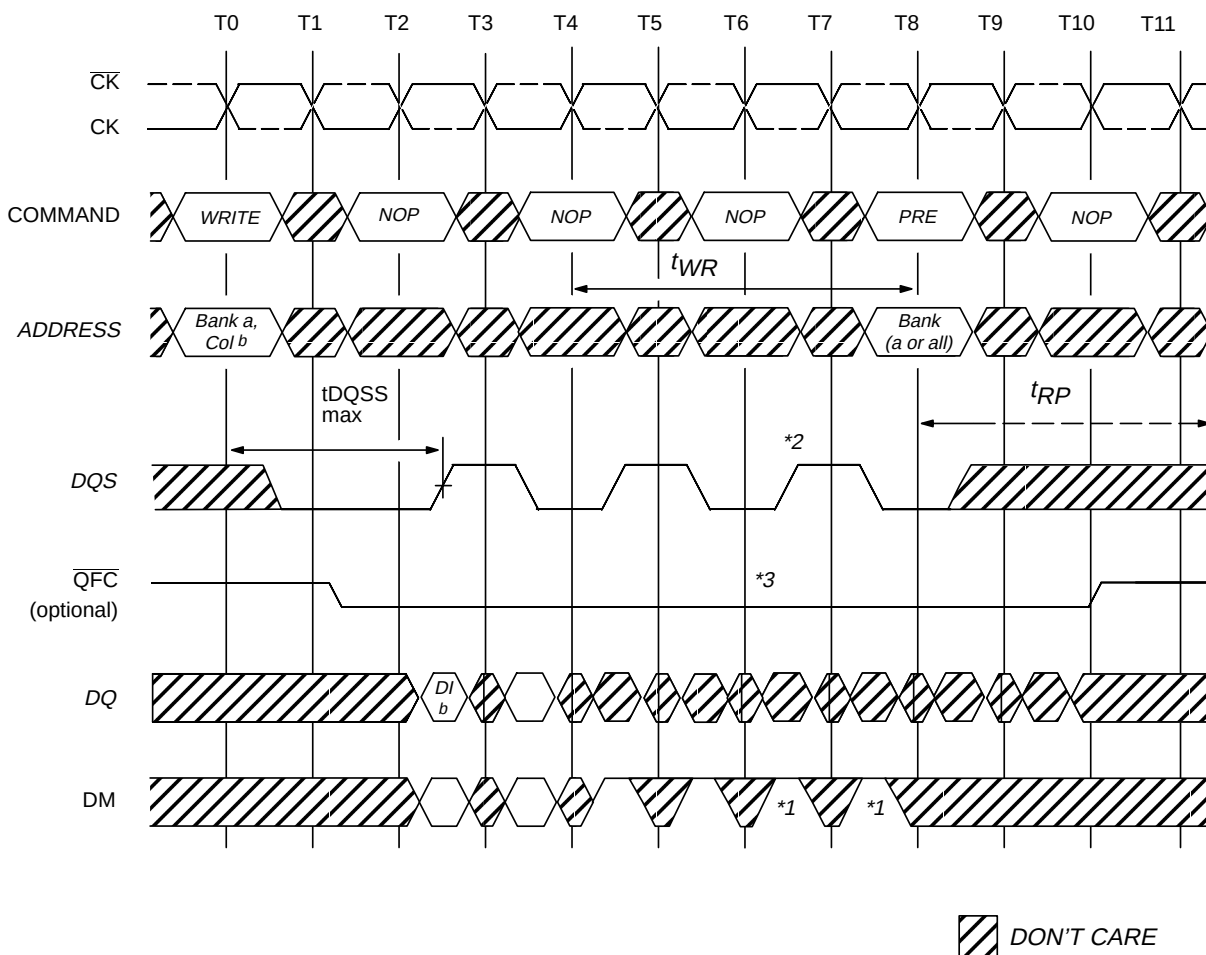
3 subsequent elements of Data In are applied in the programmed order following DI b

A noninterrupted burst of 4 is shown

tWR is referenced from the first positive CK edge after the last Data In pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure 29
WRITE TO PRECHARGE – MIN DQSS, NON-INTERRUPTING



DI b = Data In for column b

An interrupted burst of 4 or 8 is shown, 2 data elements are written

1 subsequent element of Data In is applied in the programmed order following DI b

tWR is referenced from the first positive CK edge after the last desired Data In pair

The PRECHARGE command masks the last two data elements in the burst

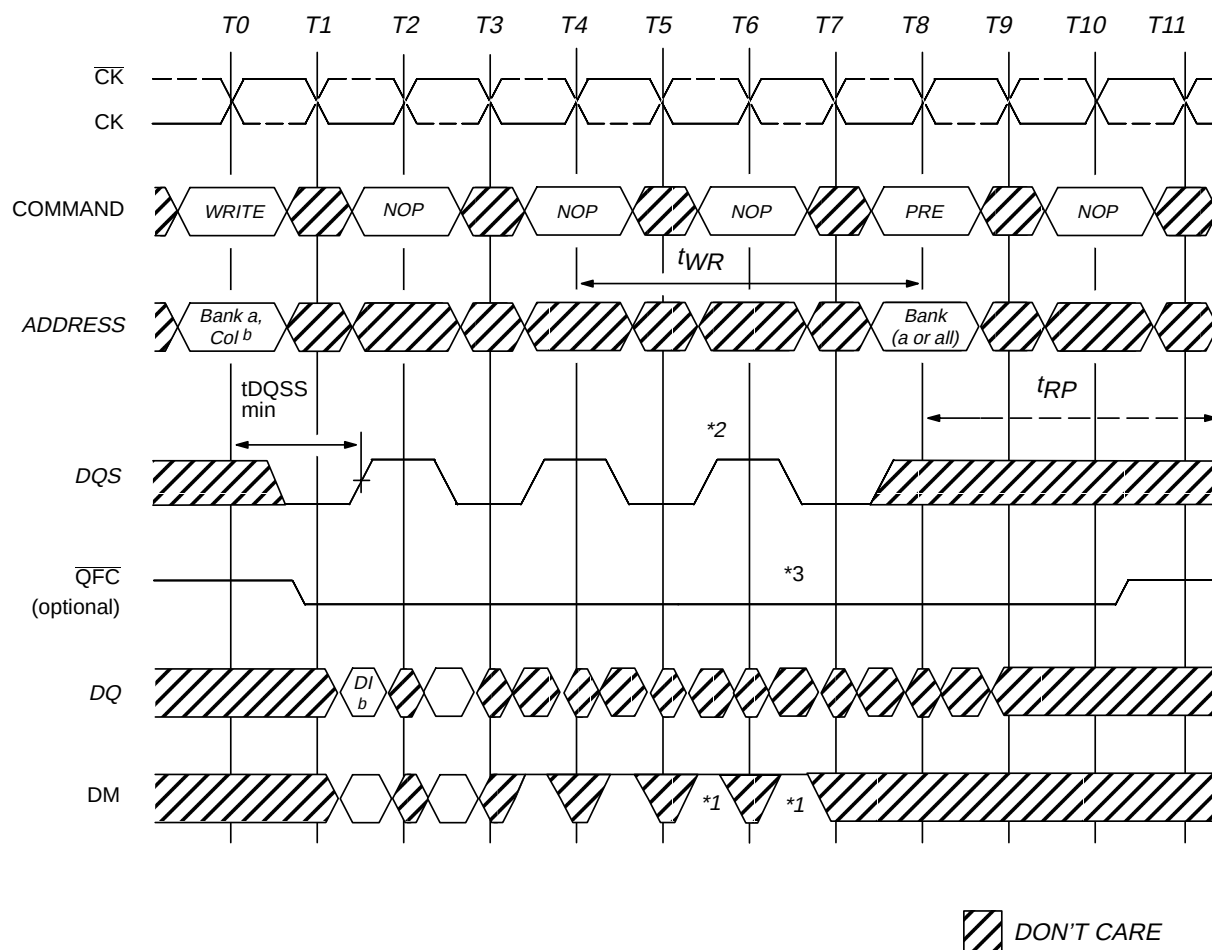
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

**1 = can be don't care for programmed burst length of 4*

**2 = for programmed burst length of 4, DQS becomes don't care at this point*

**3 = for programmed burst length of 4, QFC becomes High-Z at this point*

Figure 30
WRITE TO PRECHARGE – MAX DQSS, INTERRUPTING



DI b = Data In for column b

An interrupted burst of 4 or 8 is shown, 2 data elements are written

1 subsequent element of Data In is applied in the programmed order following DI b

t_{WR} is referenced from the first positive CK edge after the last desired Data In pair

The PRECHARGE command masks the last two data elements in the burst

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

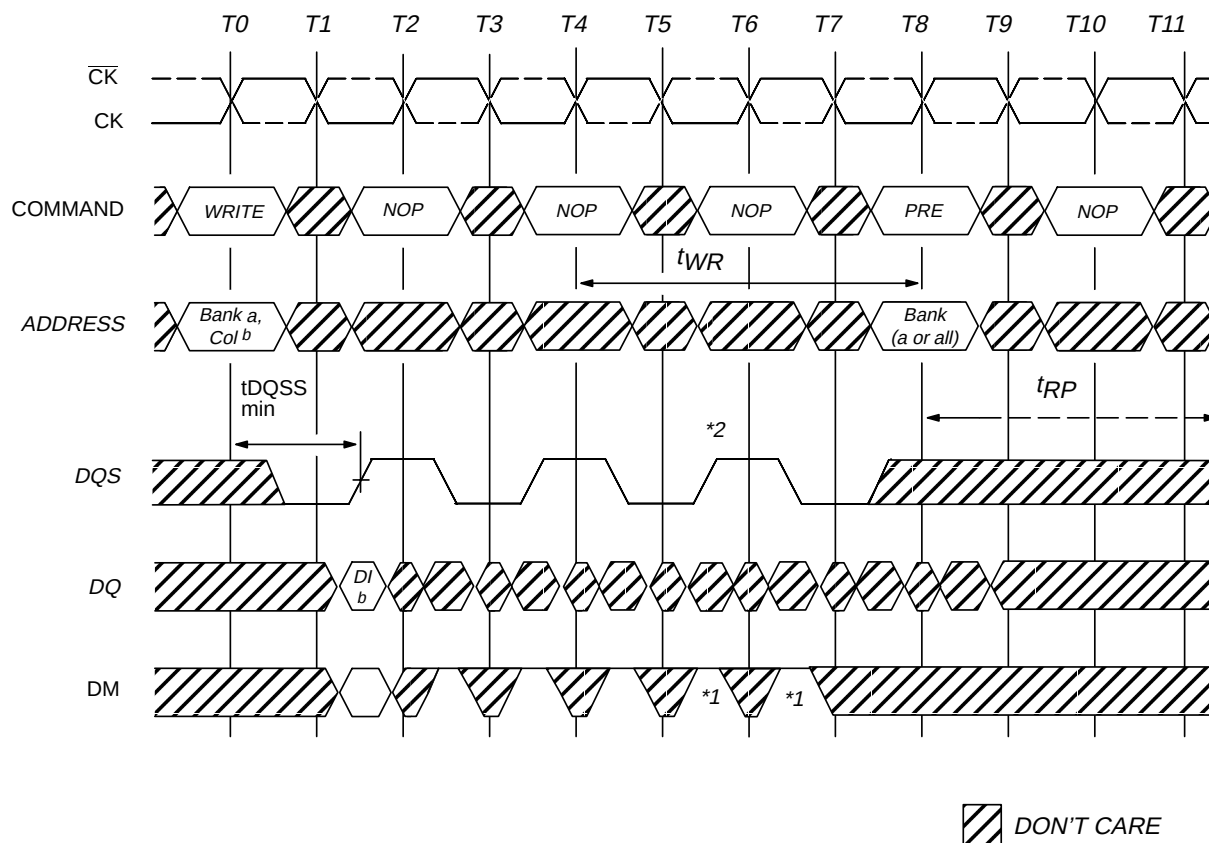
**1 = can be don't care for programmed burst length of 4*

**2 = for programmed burst length of 4, DQS becomes don't care at this point*

**3 = for programmed burst length of 4, $\overline{QFC}$ becomes High-Z at this point*

Depending on external components, $\overline{QFC}$ operation with min tDQSS might not be possible at the maximum operating frequency of the device

Figure 31
WRITE TO PRECHARGE – MIN DQSS, INTERRUPTING



DI b = Data In for column b

An interrupted burst of 4 or 8 is shown, 1 data element is written

tWR is referenced from the first positive CK edge after the last desired Data In pair

The PRECHARGE command masks the last two data elements in the burst

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

**1 = can be don't care for programmed burst length of 4*

**2 = for programmed burst length of 4, DQS becomes don't care at this point*

Figure 32
WRITE TO PRECHARGE – MIN DQSS, ODD NUMBER OF DATA,
INTERRUPTING

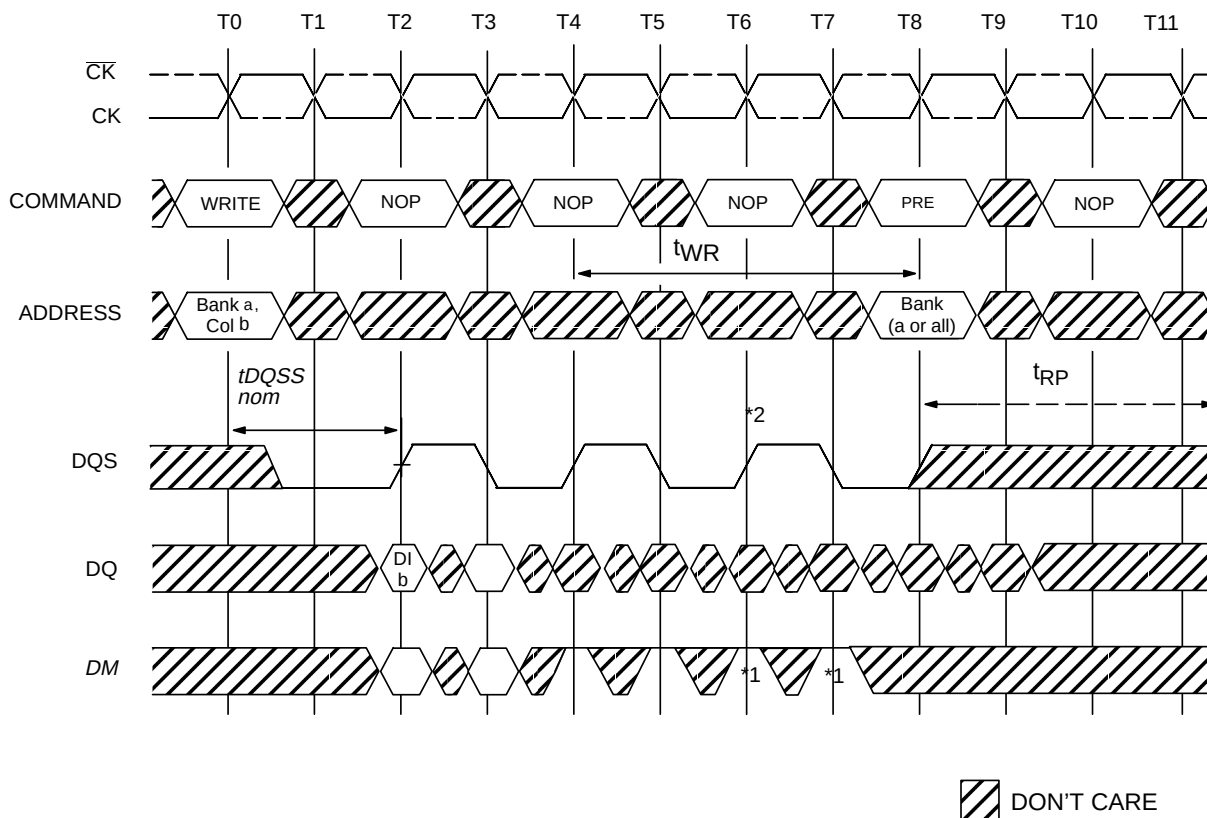


Figure 33
WRITE TO PRECHARGE – NOMINAL DQSS, INTERRUPTING

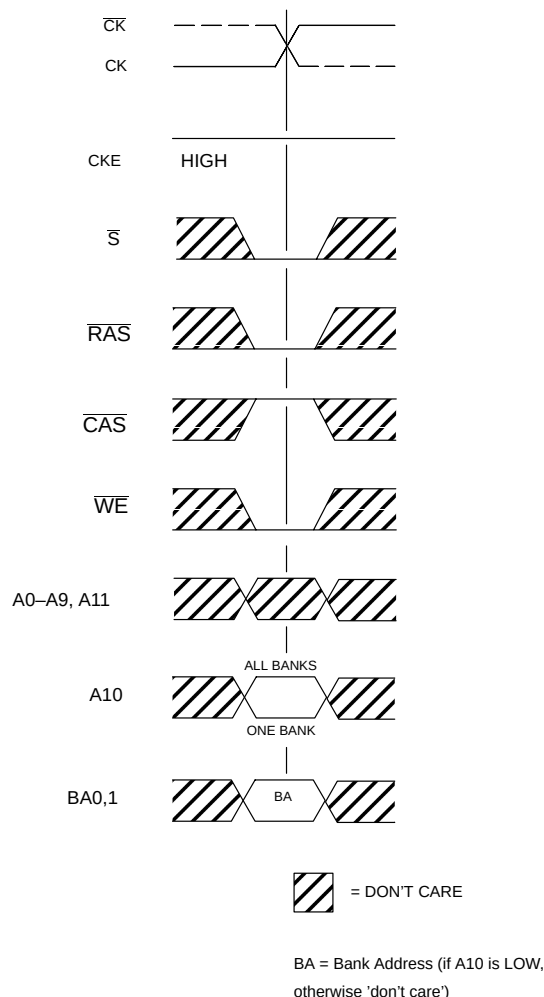


Figure 34
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down is entered when CKE is registered low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL-disabled power-down mode.

In power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care".

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

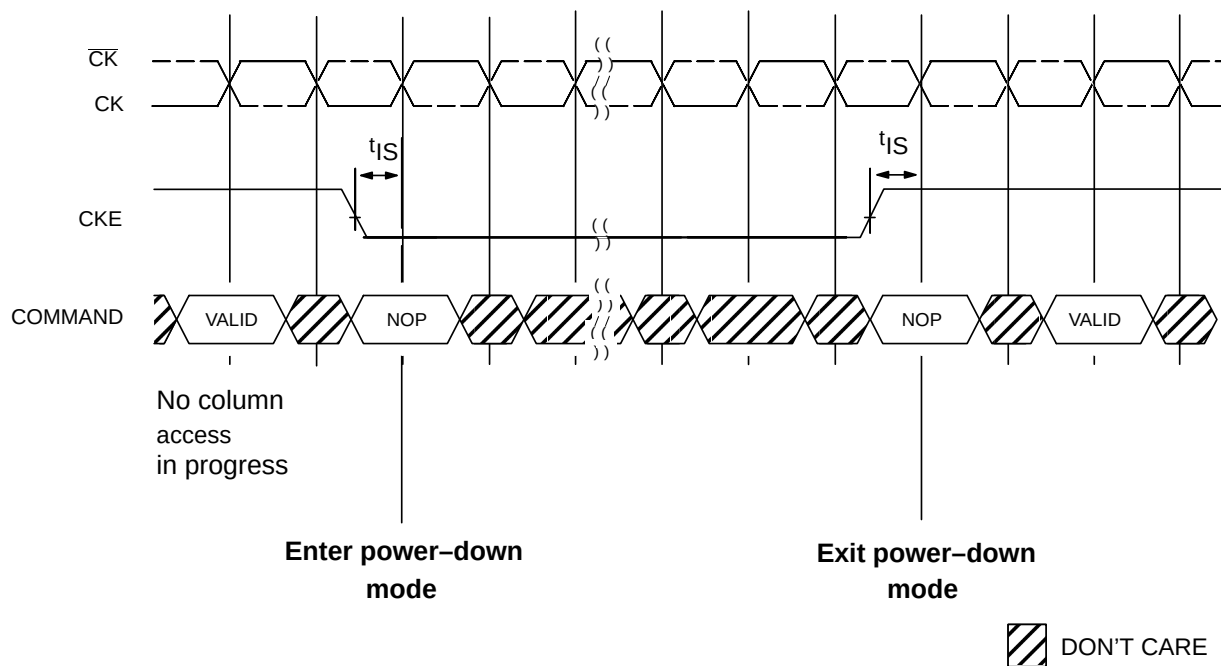


Figure 35
POWER-DOWN

(Notes: 1–4)

TRUTH TABLE 2 – CKE

CKEn–1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power–Down	X	Maintain Power–Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power–Down	DESELECT or NOP	Exit Power–Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power–Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power–Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

- NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn–1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. Deselect or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3 – Current State Bank n – Command to Bank n

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION(NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

- This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
- This table is bank–specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
- Current state definitions:
 - Idle: The bank has been precharged, and tRP has been met.
 - Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
 - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
 - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
- The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
 - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
 - Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the "row active" state.
 - Read w/Auto–Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
 - Write w/Auto–Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
 - Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the "all banks idle" state.
 - Accessing Mode
 - Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMTC is met, the DDR SDRAM will be in the "all banks idle" state.
 - Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for pre-charging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.

TRUTH TABLE 4 – Current State Bank n – Command to Bank m

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto– Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	L	H	L	PRECHARGE	
Write (Auto– Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto– Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto– Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst) 3a,	7
	L	H	L	L	WRITE (select column and start new WRITE burst) 3a,	7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

NOTE: (continued)

3. Current state definitions:

- Idle: The bank has been precharged, and tRP has been met.
- Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
- Read: A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
- Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.

Read with Auto

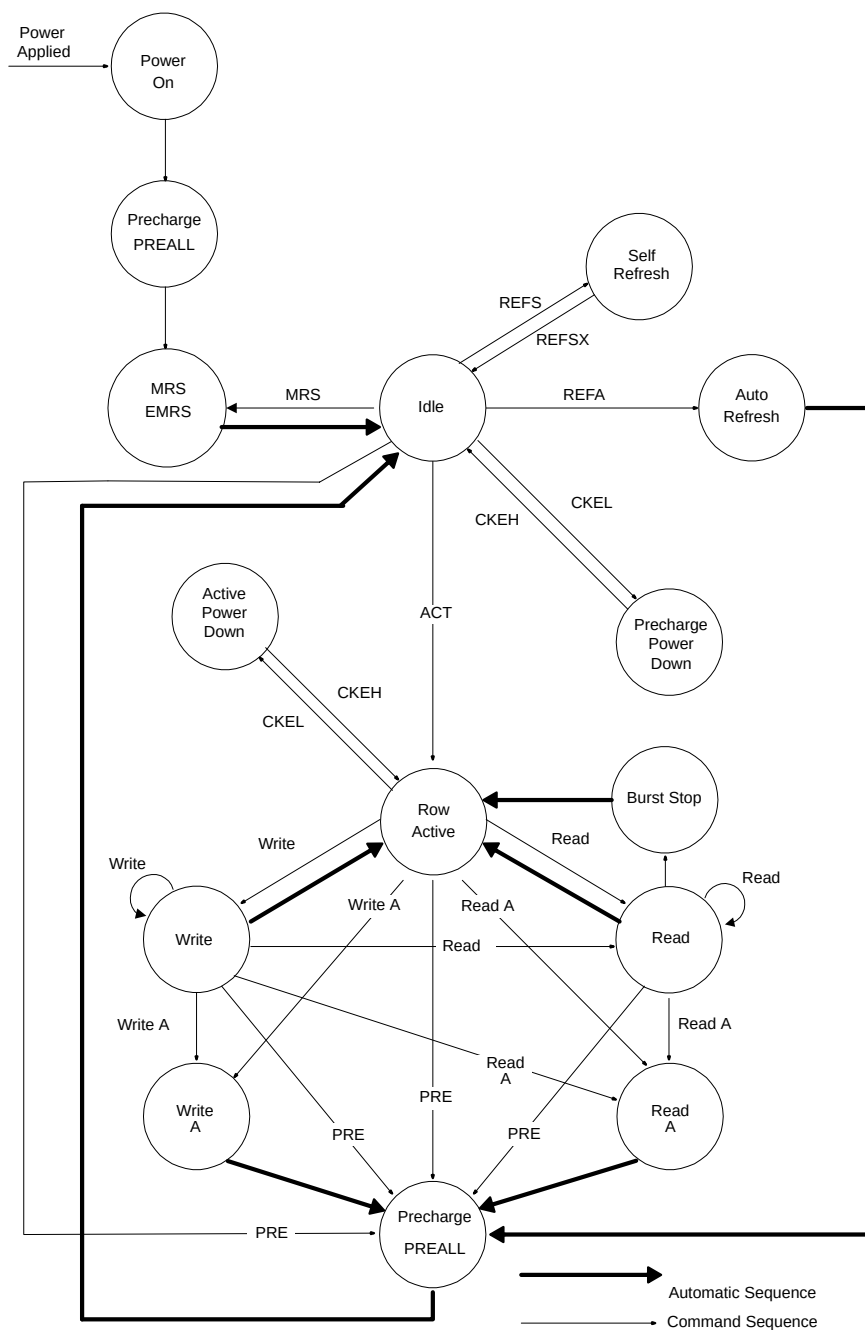
Precharge Enabled: See following text

Write with Auto

Precharge Enabled: See following text

- 3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).
- 4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
- 5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
- 6. All states and sequences not shown are illegal or reserved.
- 7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
- 8. Requires appropriate DM masking.
- 9. A WRITE command may be applied after the completion of data output.

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vdd Supply (For devices with nominal Vdd of 3.3 V)
Relative to Vss –1 V to +4.6 V
Voltage on Vdd Supply (For devices with nominal Vdd of 2.5 V)
Relative to Vss –1 V to +3.6 V
Voltage on VddQ Supply
Relative to Vss –1 V to +3.6 V
Voltage on Inputs
Relative to Vss –1 V to +3.6 V
Voltage on I/O Pins
Relative to Vss –0.5 V to VddQ+0.5 V

Operating Temperature, TA (ambient) 0 °C to +70 °C
Storage Temperature (plastic) –55 °C to +150 °C
Power Dissipation 1 W
Short Circuit Output Current 50 mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CK, $\overline{\text{CK}}$	Ci1	2.5	3.5	pF	13
Input Capacitance: All other input-only pins	Ci2	2.5	3.5	pF	13
Input/Output Capacitance: DQ, DQS, DM	Cio	4.0	5.0	pF	13
Delta Input/Output Capacitance: DQ, DQS, DM	Cdio	–	0.5	pF	13
Output Capacitance: ($\overline{\text{QFC}}$)	Co	TBD	TBD	pF	13

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.18	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	–0.3	VREF–0.18	V	
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	VIN(DC)	–0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	8
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	II	–2	2	μA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	–5	5	μA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	IOH IOL	–15.2 15.2		mA mA	

- 1) The full variation in driver pulldown current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figure a.
- 2) It is recommended that the "typical" IBIS pulldown V-I curve lie within the shaded region of the V-I curve of Figure a.

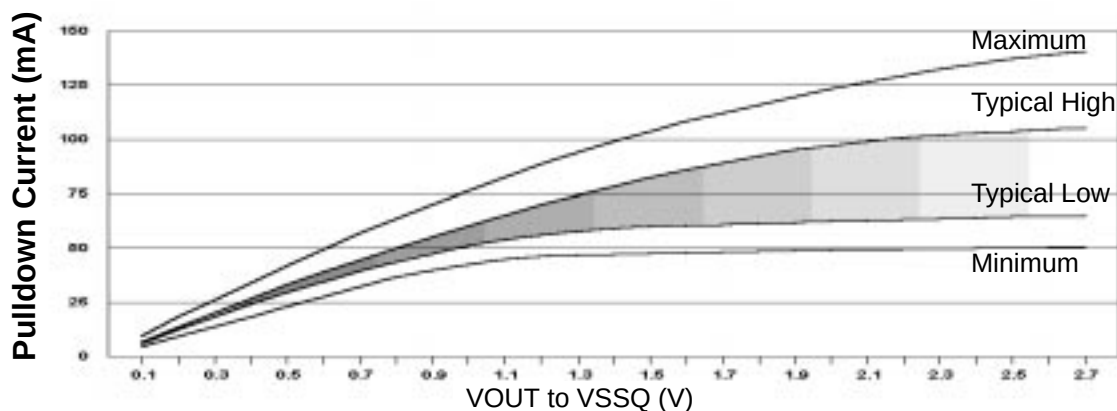


Figure a: Pulldown Characteristics

- 3) The full variation in driver pullup current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figure b.
- 4) It is recommended that the "typical" IBIS pullup V-I curve lie within the shaded region of the V-I curve of Figure b.

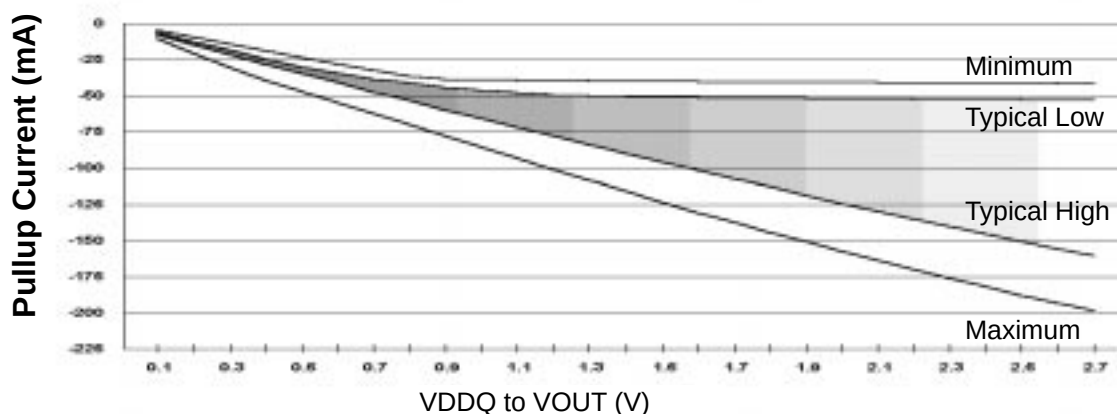


Figure b: Pull Up Characteristics

- 5) The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.
- 6) The full variation in the ratio of the "typical" IBIS pullup to "typical" IBIS pulldown current should be $\pm 10\%$, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.
- 7) These characteristics obey the SSTL_2 class II standard.
- 8) This specification is intended for DDR SDRAM only.

DATA DRIVER OUTPUT CHARACTERISTIC CURVES

Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Evaluation conditions:

Typical 25 ° C (T_{Ambient}), VDDQ=2.5 V, typical process
Minimum 70 ° C (T_{Ambient}), VDDQ=2.3 V, slow-slow process
Maximum 0 ° C (T_{Ambient}), VDDQ=2.7 V, fast-fast process

DATA DRIVER OUTPUT CHARACTERISTIC V-I DATA POINTS

AC OPERATING CONDITIONS(Notes: 1–5, 14, 16) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{DDQ} = +2.5\text{ V} \pm 0.2\text{ V}$, $V_{DD} = +3.3\text{ V} \pm 0.3\text{ V}$ or $+2.5\text{ V} \pm 0.2\text{ V}$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH}(ac)$	$V_{REF} + 0.35$		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	$V_{IL}(ac)$		$V_{REF} - .35$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID}(ac)$	0.7	$V_{DDQ} + 0.6$	V	8
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX}(ac)$	$0.5 \cdot V_{DDQ} - 0.2$	$0.5 \cdot V_{DDQ} + 0.2$	V	9

IDD SPECIFICATIONS AND CONDITIONS(Notes: 1–5, 12, 14) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{DDQ} = +2.5\text{ V} \pm 0.2\text{ V}$, $V_{DD} = +3.3\text{ V} \pm 0.3\text{ V}$ or $+2.5\text{ V} \pm 0.2\text{ V}$)

		MAX		
PARAMETER/CONDITION	SYMBOL		UNITS	NOTES
OPERATING CURRENT: One Bank; Active–Precharge; $t_{RC} = t_{RC\text{ MIN}}$; $t_{CK} = t_{CK\text{ MIN}}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0	V/DS*	mA	
OPERATING CURRENT: One Bank; Active–Read–Precharge; Burst = 2; $t_{RC} = t_{RC\text{ MIN}}$; $CL = 2.5$; $t_{CK} = t_{CK\text{ MIN}}$; $I_{out} = 0\text{ mA}$; Address and control inputs changing once per clock cycle	IDD1	V/DS*	mA	
PRECHARGE POWER–DOWN STANDBY CURRENT: All banks idle; power–down mode; $CKE \leq V_{IL}(\text{MAX})$; $t_{CK} = t_{CK\text{ MIN}}$	IDD2P	V/DS*	mA	
IDLE STANDBY CURRENT: $\overline{S} \geq V_{IH}(\text{MIN})$; All banks idle; $CKE \geq V_{IH}(\text{MIN})$; $t_{CK} = t_{CK\text{ MIN}}$; Address and other control inputs changing once per clock cycle	IDD2N	V/DS*	mA	
ACTIVE POWER–DOWN STANDBY CURRENT: One bank active; power–down mode; $CKE \leq V_{IL}(\text{MAX})$; $t_{CK} = t_{CK\text{ MIN}}$	IDD3P	V/DS*	mA	
ACTIVE STANDBY CURRENT: $\overline{S} \geq V_{IH}(\text{MIN})$; $CKE \geq V_{IH}(\text{MIN})$; One bank; Active–Precharge; $t_{RC} = t_{RAS\text{ MAX}}$; $t_{CK} = t_{CK\text{ MIN}}$; DQ, DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	V/DS*	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $CL = 2.5$; $t_{CK} = t_{CK\text{ MIN}}$; $I_{out} = 0\text{ mA}$	IDD4R	V/DS*	mA	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $CL = 2.5$; $t_{CK} = t_{CK\text{ MIN}}$; DQ, DM and DQS inputs changing twice per clock cycle	IDD4W	V/DS*	mA	
AUTO REFRESH CURRENT: $t_{RC} = t_{RFC}(\text{MIN})$	IDD5	V/DS*	mA	
SELF REFRESH CURRENT: $CKE \leq 0.2\text{ V}$	IDD6	V/DS*	mA	11

V/DS* = Vendor/Device Specific

ELECTRICAL CHARACTERISTICS AND AC TIMING for DDR-266/DDR-200 –

Absolute Specifications

(Notes: 1–5, 14–17) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{DDQ} = +2.5\text{ V} \pm 0.2\text{ V}$, $V_{DD} = +3.3\text{ V} \pm 0.3\text{ V}$ or $+2.5\text{ V} \pm 0.2\text{ V}$)

AC CHARACTERISTICS		DDR-266A		DDR-266B		DDR-200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ output access time from CK/CK	tAC	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	
DQS output access time from CK/CK	tDQSK	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)		min(tCL, tCH)		min(tCL, tCH)		ns	29
Clock cycle time CL = 2.5 CL = 2	tCK	7	15	7.5	15	8	15	ns	
	tCK	7.5	15	10	15	10	15	ns	
DQ and DM input hold time	tDH	0.5		0.5		0.6		ns	
DQ and DM input setup time	tDS	0.5		0.5		0.6		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.5		ns	27
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		2		ns	27
Data-out high-impedance time from CK/CK	tHZ	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	18
Data-out low-impedance time from CK/CK	tLZ	–0.75	+0.75	–0.75	+0.75	–0.8	+0.8	ns	18
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5		+0.5		+0.6	ns	
DQS–DQ Skew (for DQS and all DQ signals)	tDQSQA		+0.5		+0.5		+0.6	ns	
DQ/DQS output hold time from DQS	tQH	tHP–0.75		tHP–0.75		tHP–1.0		ns.	30
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	15		15		16		ns	
Write preamble setup time	tWPRES	0		0		0		ns	22
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.40	0.60	tCK	19
Write preamble	tWPRE	0.25		0.25		0.25		tCK	
Address and Control input hold time (fast slew rate)	tIH	0.9		0.9		1.2		ns	24,26,27
Address and Control input setup time (fast slew rate)	tIS	0.9		0.9		1.2		ns	25,26,27
Address and Control input hold time (slow slew rate)	tIH	1.0		1.0		1.2		ns	25,26,27
Address and Control input setup time (slow slew rate)	tIS	1.0		1.0		1.2		ns	25,26,27
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
QFC preamble during reads	tQPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
QFC postamble during reads	tQPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
QFC output access time from CK/CK, for writes	tQCK		4		4		4	ns	
QFC output hold time for writes	tQOH	1.25	2.0	1.25	2.0	1.25	2.0	ns	
ACTIVE to PRECHARGE command	tRAS	45	120,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	65		65		70		ns	
Auto Refresh to Active/Auto Refresh command period	tRFC	75		75		80		ns	
ACTIVE to READ or WRITE delay	tRCD	20		20		20		ns	
PRECHARGE command period	tRP	20		20		20		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	15		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	35		35		35		ns	
Internal Write to Read Command Delay	tWTR	1		1		1		tCK	
Exit self refresh to non-READ command	tXSNR	75		75		80		ns	
Exit self refresh to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval	tREFI		15.6		15.6		15.6	μs	23

ELECTRICAL CHARACTERISTICS AND AC TIMING for DDR-266 –**Applicable Specifications Expressed in Clock Cycles**

(Notes: 1–5, 14–17) (0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		tCK = 7.5 ns		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX		
DQ output access time from CK/ $\overline{\text{CK}}$	tAC	–0.75	+0.75	ns	
DQS output access time from CK/ $\overline{\text{CK}}$	tDQSCK	–0.75	+0.75	ns	
CK high-level width	tCH	3.4	4.1	ns	
CK low-level width	tCL	3.4	4.1	ns	
CK half period	tHP	min(tCL, tCH)		ns	29
DQ and DM input hold time	tDH	0.5		ns	
DQ and DM input setup time	tDS	0.5		ns	
Control & Address input pulse width (for each input)	tIPW	2.2		ns	27
DQ and DM input pulse width (for each input)	tDIPW	1.75		ns	27
Data-out high-impedance time from CK/ $\overline{\text{CK}}$	tHZ	–0.75	+0.75	ns	18
Data-out low-impedance time from CK/ $\overline{\text{CK}}$	tLZ	–0.75	+0.75	ns	18
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.5	ns	
DQS–DQ Skew (for DQS and all DQ signals)	tDQSQA		+0.5	ns	
DQ/DQS output hold time	tQH	tHP–0.75		ns	30
Write command to first DQS latching transition	tDQSS	5.6	9.4	ns	
DQS input high pulse width	tDQSH	2.63		ns	
DQS input low pulse width	tDQSL	2.63		ns	
DQS falling edge to CK setup time	tDSS	1.5		ns	
DQS falling edge hold time from CK	tDSH	1.5		ns	
MODE REGISTER SET command cycle time	tMRD	2		tCK	
Write preamble setup time	tWPRES	0		ns	22
Write postamble	tWPST	3	4.5	ns	19
Write preamble	tWPRE	0.25			
Address and Control input hold time (fast slew rate)	tIH	0.9		ns	24,26,27
Address and Control input setup time (fast slew rate)	tIS	0.9		ns	24,26,27
Address and Control input hold time (slow slew rate)	tIH	1.0		ns	25,26,27
Address and Control input setup time (slow slew rate)	tIS	1.0		ns	25,26,27
Read preamble	tRPRE	6.75	8.25	ns	
Read postamble	tRPST	3	4.5	ns	
$\overline{\text{QFC}}$ preamble during reads	tQPRE	6.75	8.25	ns	
$\overline{\text{QFC}}$ postamble during reads	tQPST	3	4.5	ns	
$\overline{\text{QFC}}$ output access time from CK/ $\overline{\text{CK}}$, for writes	tQCK		4	ns	
$\overline{\text{QFC}}$ output hold time for writes	tQOH	1.25	2.0	ns	
ACTIVE to PRECHARGE command	tRAS	6	16000	tCK	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	9		tCK	
Auto Refresh to Active/Auto Refresh command period	tRFC	10		tCK	
ACTIVE to READ or WRITE delay	tRCD	3		tCK	
PRECHARGE command period	tRP	3		tCK	
ACTIVE bank A to ACTIVE bank B command	tRRD	2		tCK	
Write recovery time	tWR	2		tCK	
Auto Precharge write recovery + precharge time	tDAL	5		tCK	
Internal Write to Read Command Delay	tWTR	1		tCK	
Exit self refresh to non-READ command	tXSNR	10		tCK	
Exit self refresh to READ command	tXSRD	200		tCK	
Average Periodic Refresh Interval	tREFI	15.6		μs	23

NOTES

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 36 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

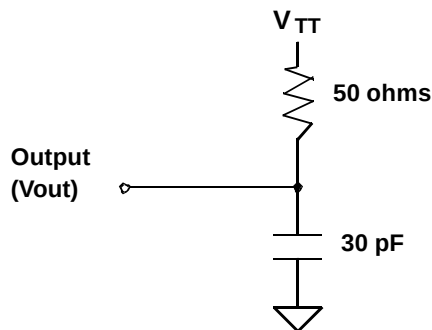
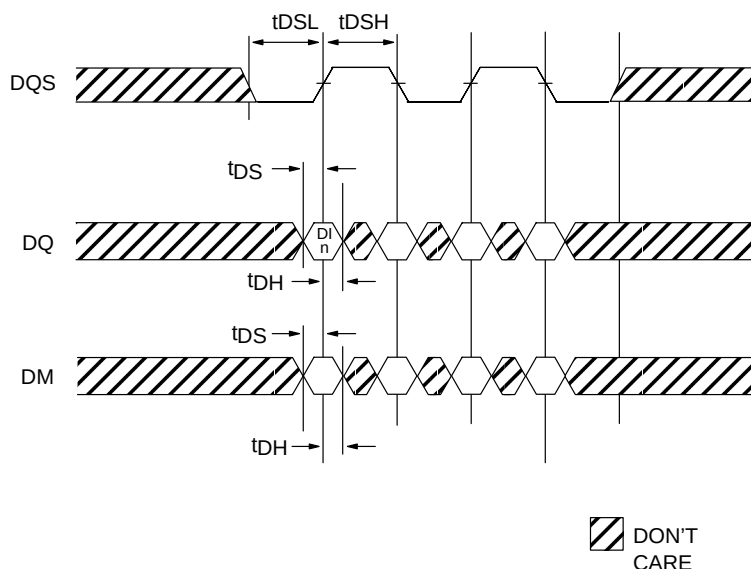


Figure 36: Timing Reference Load

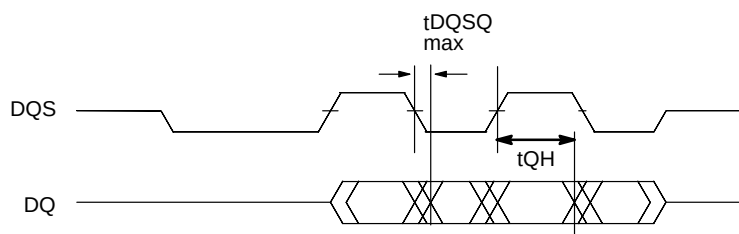
4. ac timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/ $\overline{CK}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. VREF is expected to be equal to $0.5 \cdot V_{DDQ}$ of the transmitting device, and to track variations in the dc level of the same. Peak-to-peak noise on VREF may not exceed $\pm 2\%$ of the dc value.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
8. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
9. The value of VIX is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the dc level of the same.

11. Enables on-chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized.
13. This parameter is sampled. $V_{DDQ} = +2.5 \text{ V} \pm 0.2 \text{ V}$, $V_{DD} = +3.3 \text{ V} \pm 0.3 \text{ V}$ or $+2.5 \text{ V} \pm 0.2 \text{ V}$, $f = 100 \text{ MHz}$, $t_A = 25^\circ\text{C}$, $V_{out}(dc) = V_{DDQ}/2$, $V_{out}(\text{peak to peak}) = 0.2 \text{ V}$. DM inputs are grouped with I/O pins – reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
15. The CK/ $\overline{CK}$ input reference level (for timing referenced to CK/ $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/ $\overline{CK}$, is VREF.
16. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, $C_{KE} \leq 0.2 V_{DDQ}$ is recognized as LOW.
17. The output timing reference voltage level is VTT.
18. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turn-around) will degrade accordingly.
22. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
23. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
24. For command/address input slew rate $\geq 1.0 \text{ V/ns}$
25. For command/address input slew rate $\geq 0.5 \text{ V/ns}$ and $< 1.0 \text{ V/ns}$
26. For CK & $\overline{CK}$ slew rate $\geq 1.0 \text{ V/ns}$
27. These parameters guarantee device timing, but they are not necessarily tested on each device.
28. Slew Rate is measured between VOH(ac) and VOL(ac).
29. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
30. tQH = tHPmin – X where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
X consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n

Figure 37 – DATA INPUT (WRITE) TIMING



Burst of 4 is shown.

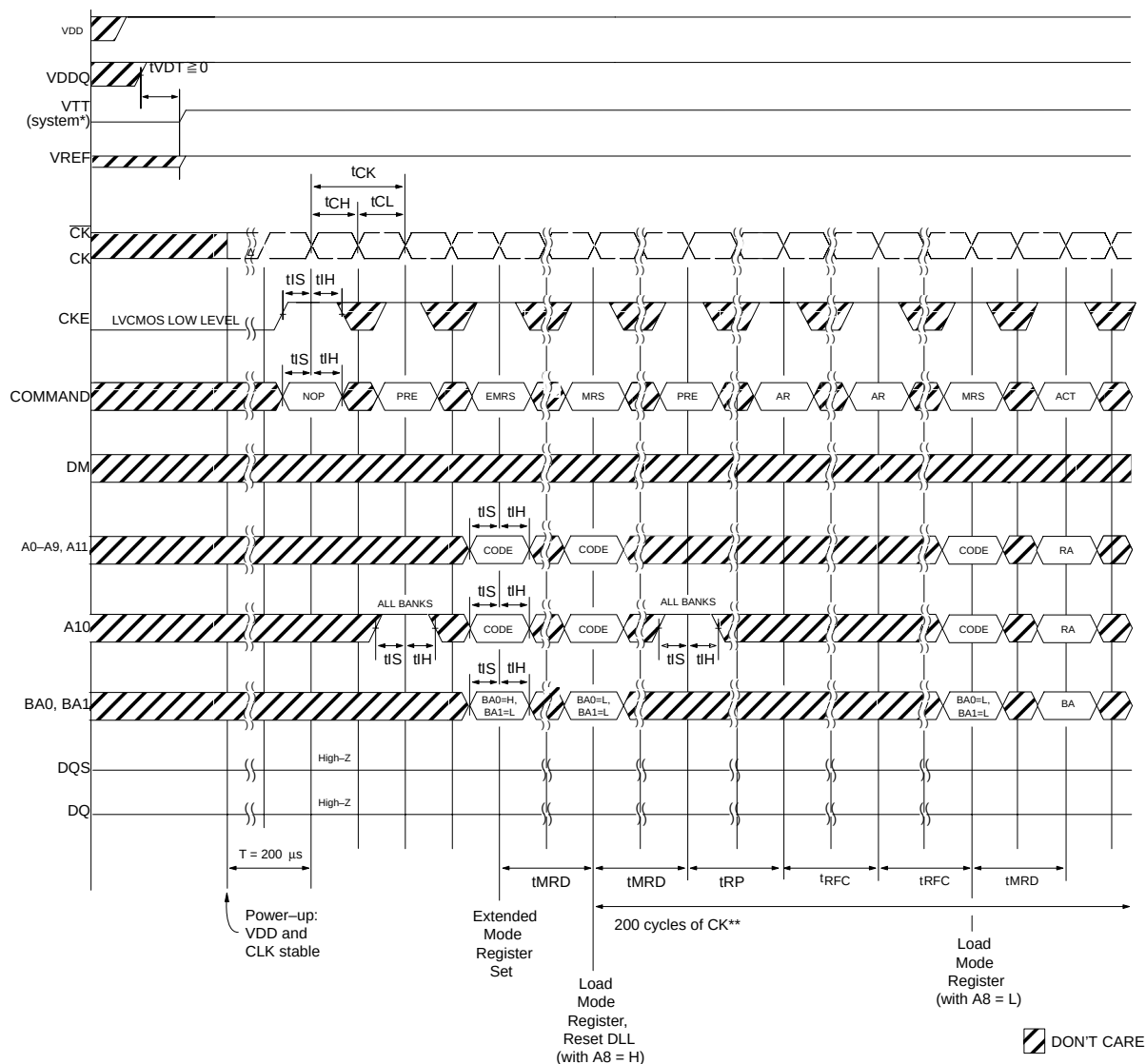
tDQSQ and tQH are only shown once, and are shown referenced to different edges of DQS, only for clarity of illustration. tDQSQ and tQH both apply to each of the four relevant edges of DQS.

tQHmin = tHPmin – X where:

tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).

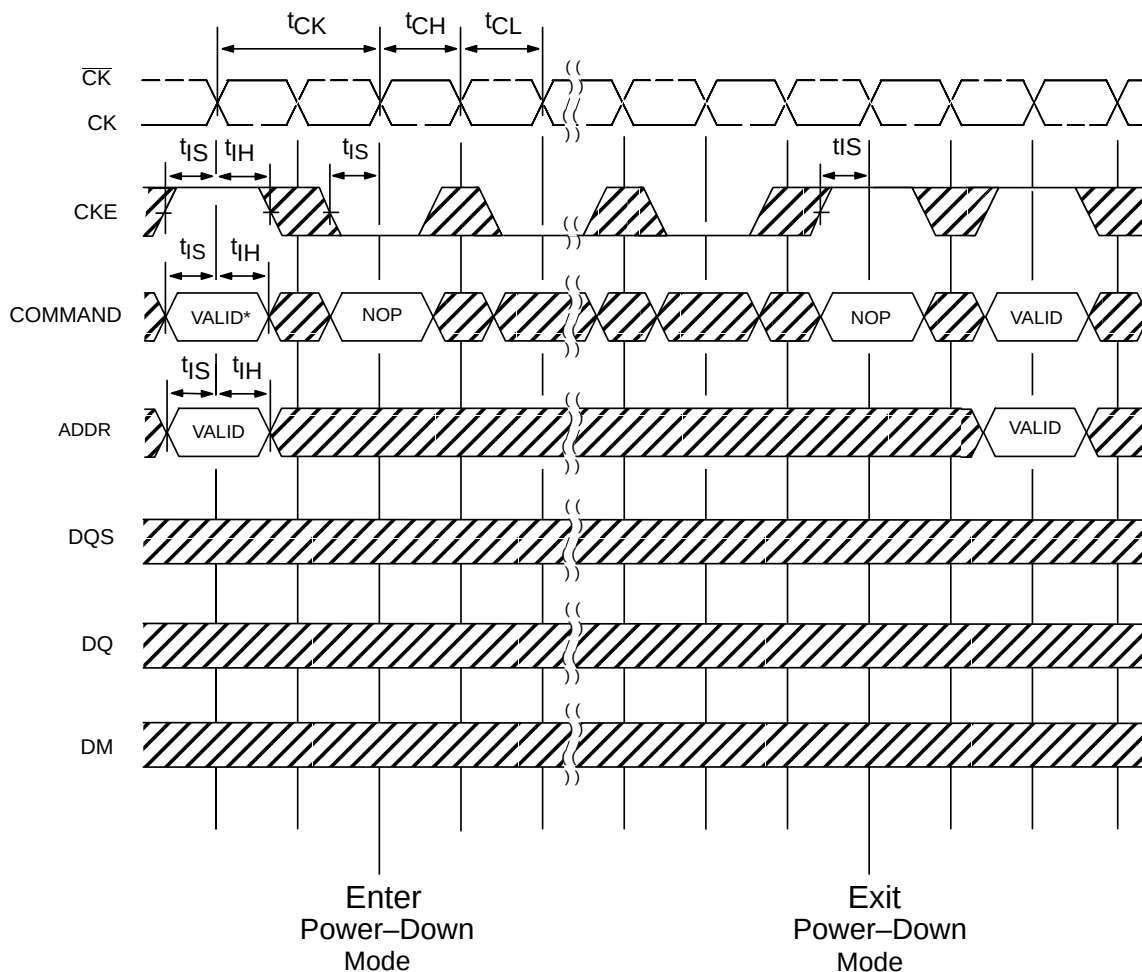
X consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

Figure 38 – DATA OUTPUT (READ) TIMING



* = VTT is not applied directly to the device, however tVDT must be greater than or equal to zero to avoid device latch-up.
 ** = tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied
 The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

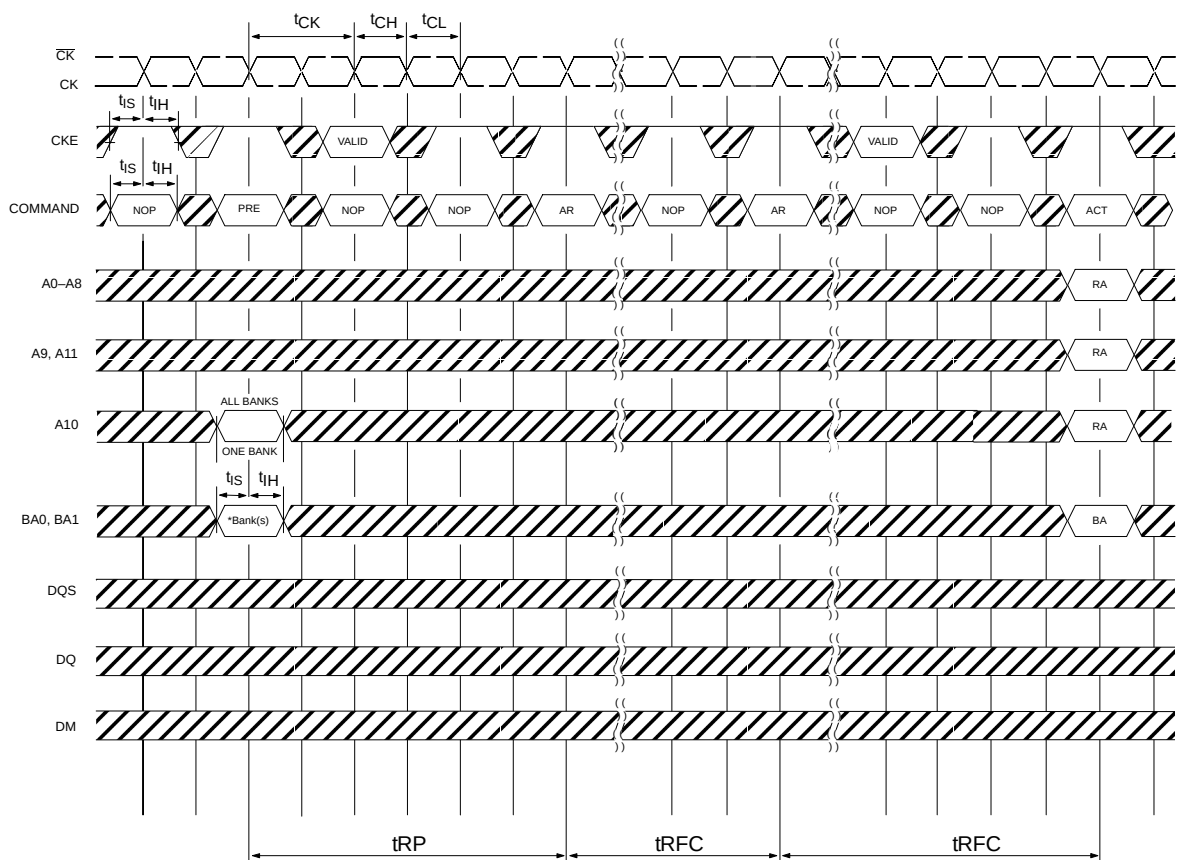
Figure 39 – INITIALIZE AND MODE REGISTER SETS



 DON'T CARE

No column accesses are allowed to be in progress at the time Power-Down is entered
 * = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down.

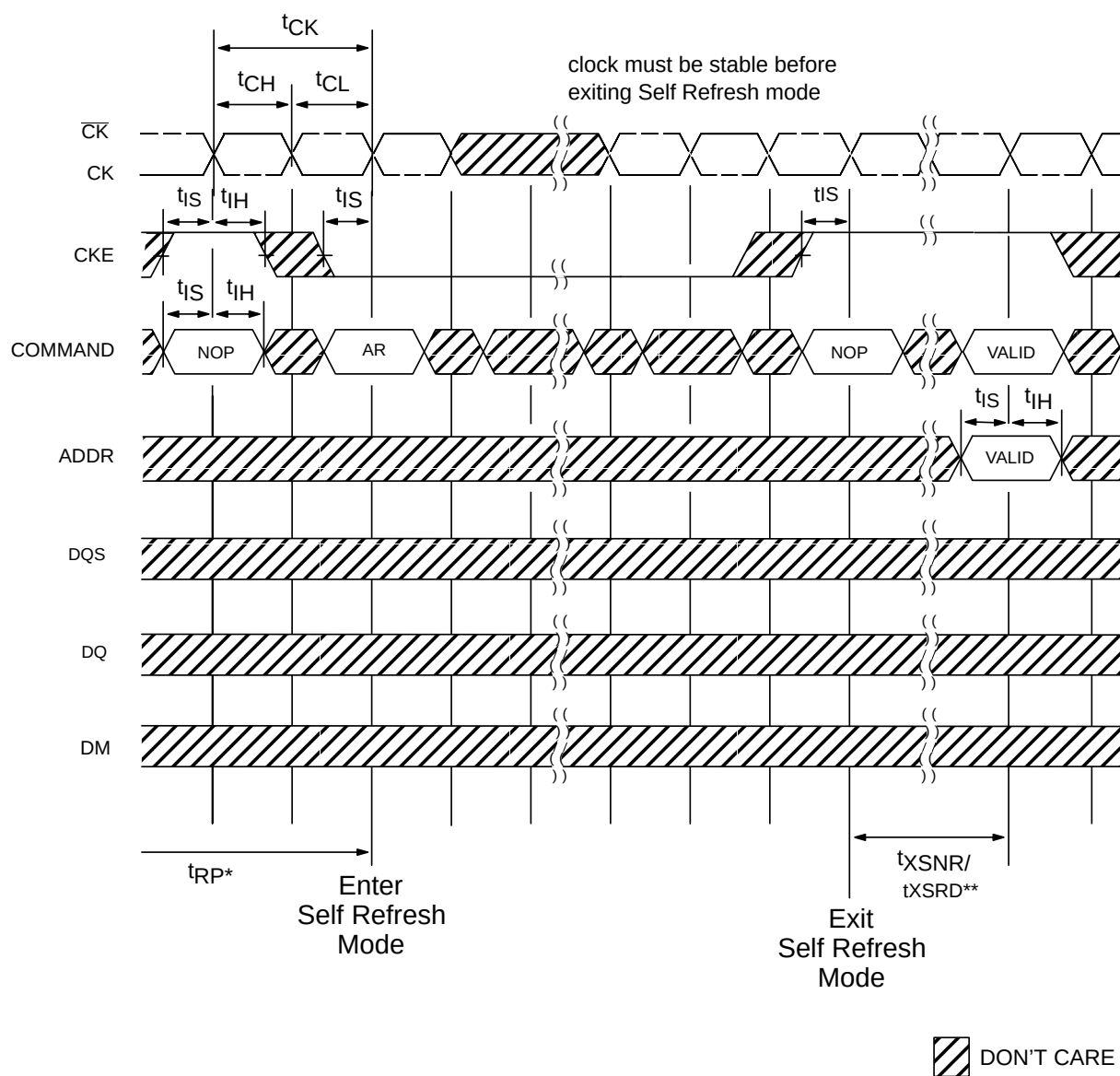
Figure 40 – POWER-DOWN MODE



DON'T CARE

* = "Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
 PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
 NOP commands are shown for ease of illustration; other valid commands may be possible at these times
 DM, DQ and DQS signals are all "Don't Care"/High-Z for operations shown

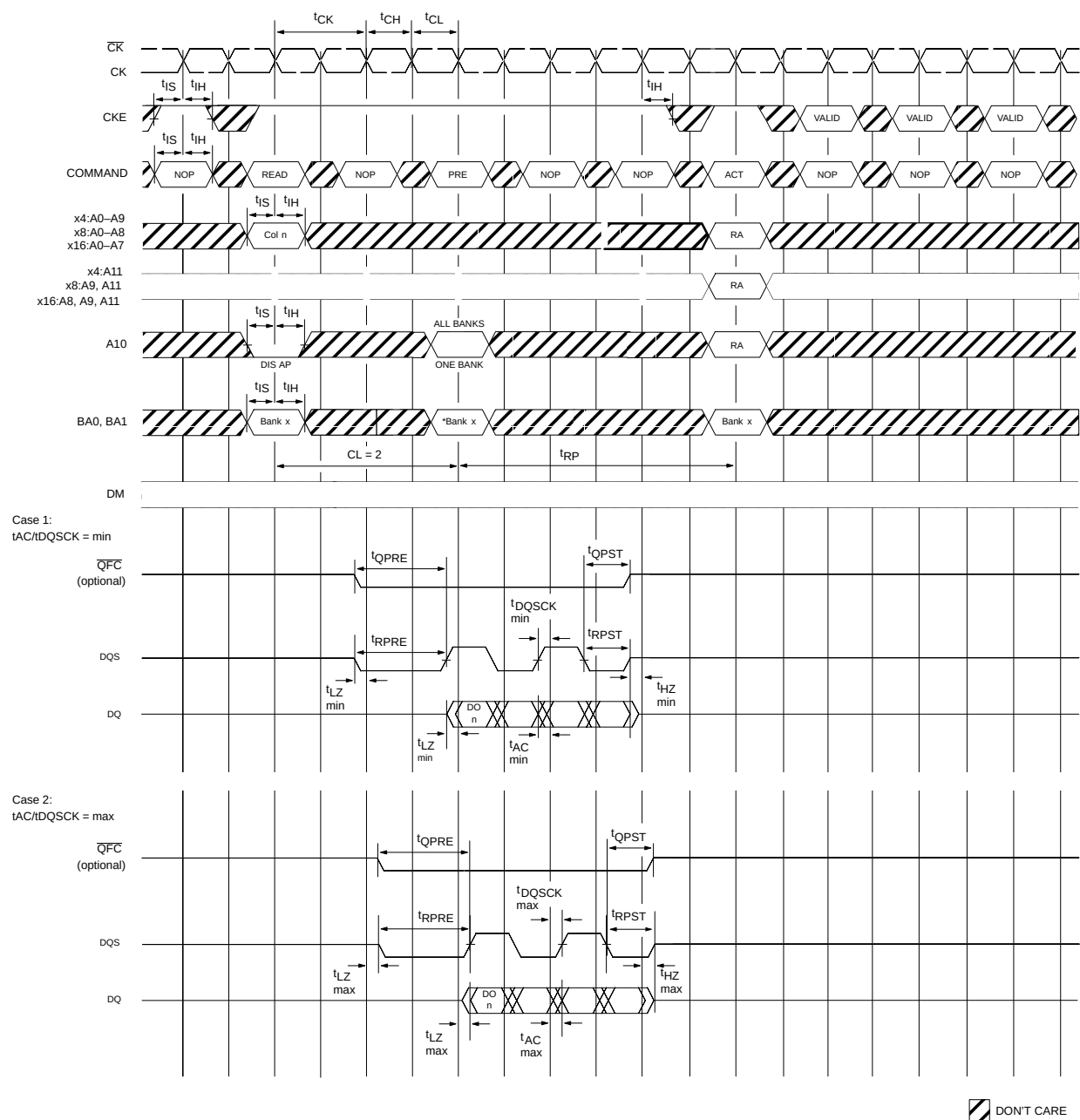
Figure 41 – AUTO REFRESH MODE



* = Device must be in the "All banks idle" state prior to entering Self Refresh mode

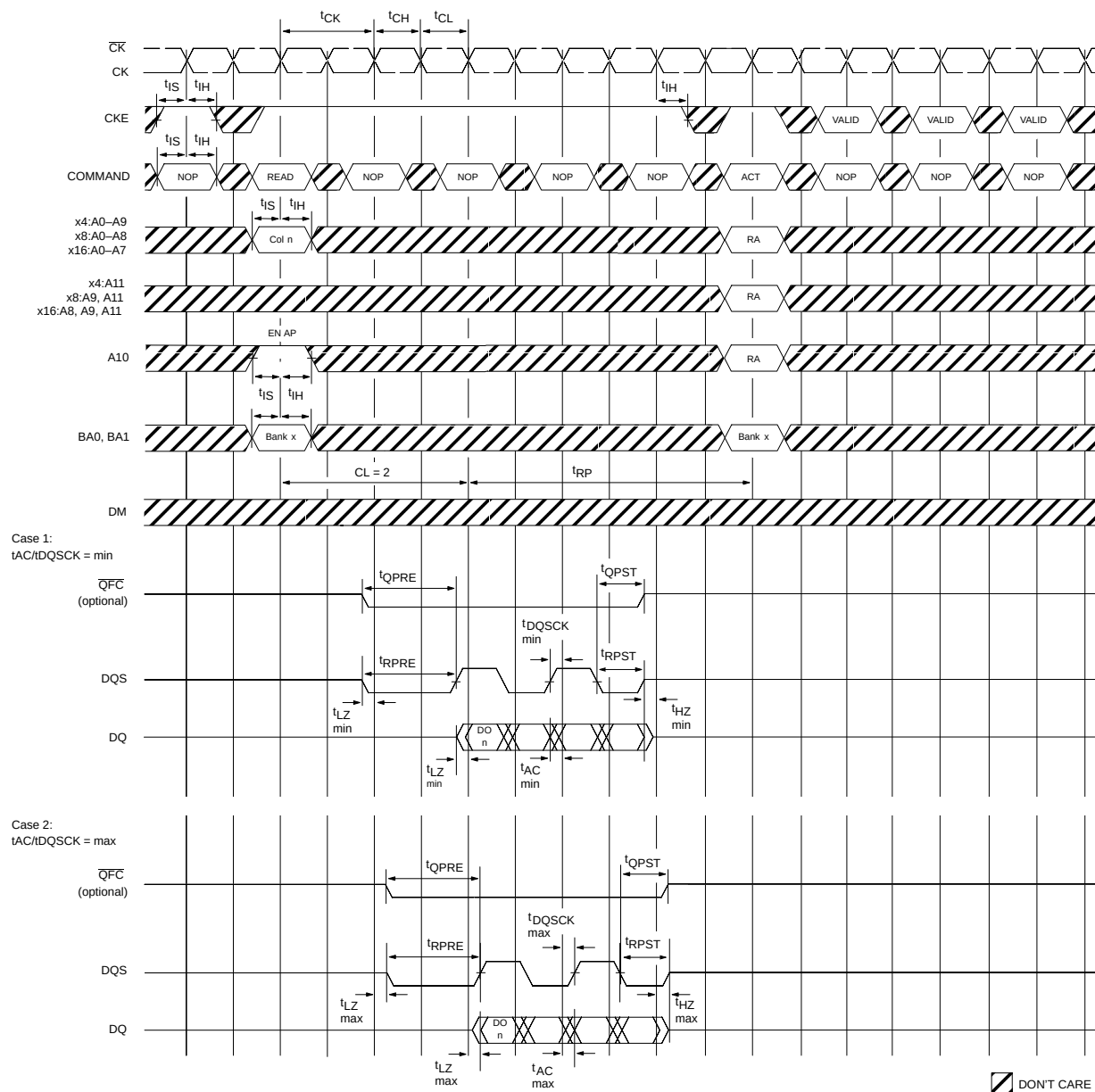
** = t_{XSNR} is required before any non-READ command can be applied, and t_{XSRD} (200 cycles of CK) are required before a READ command can be applied.

Figure 42 – SELF REFRESH MODE



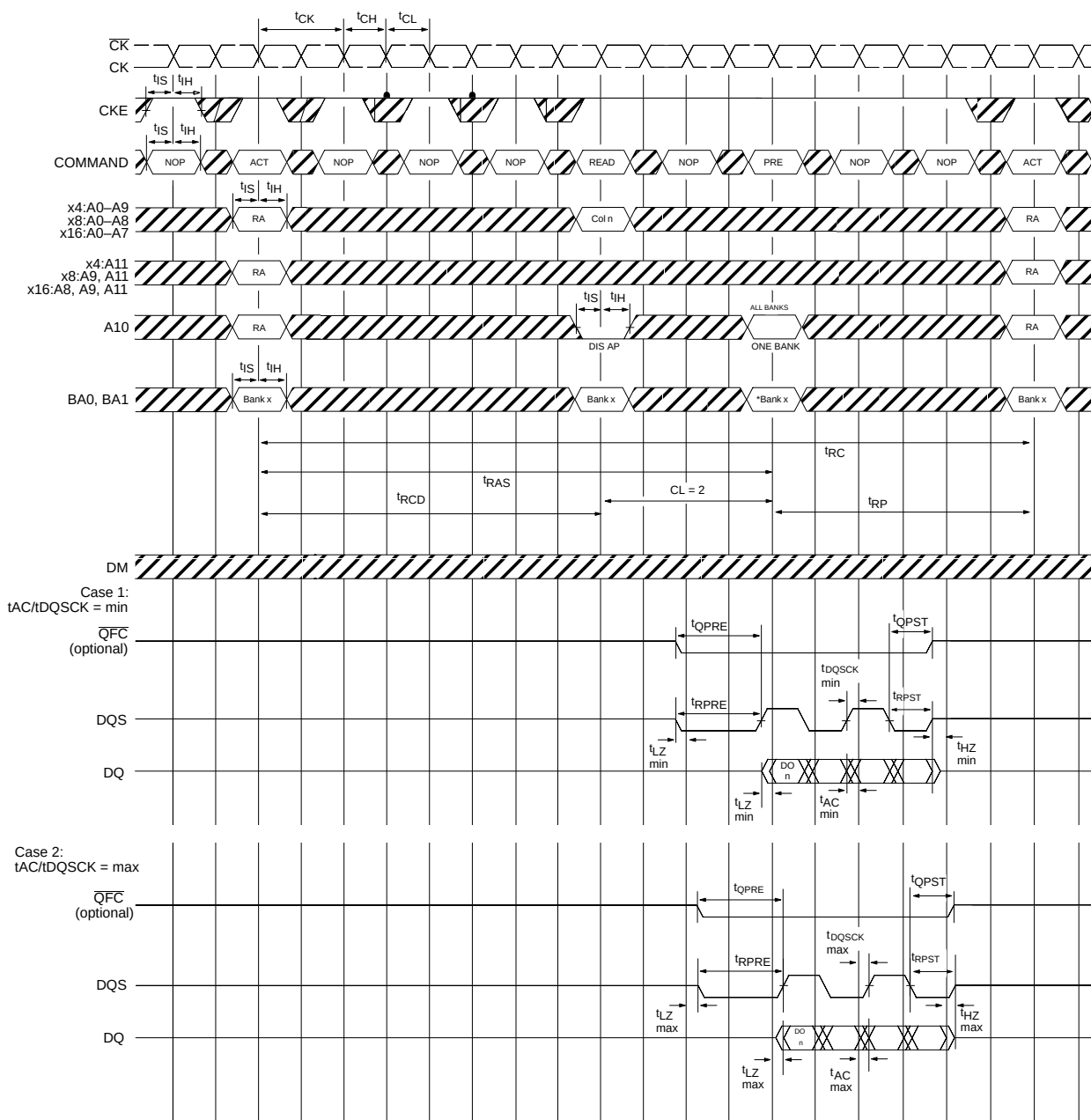
DO n = Data Out from column n
 Burst Length = 4 in the case shown
 3 subsequent elements of Data Out are provided in the programmed order following DO n
 DIS AP = Disable Autoprecharge
 * = "Don't Care", if A10 is HIGH at this point
 PRE = PRECHARGE, ACT = ACTIVE, BA = Bank Address
 NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 43 – READ _ WITHOUT AUTO PRECHARGE



DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP = Enable Autoprecharge
ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 44 – READ _ WITH AUTO PRECHARGE



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

* = "Don't Care", if A10 is HIGH at this point

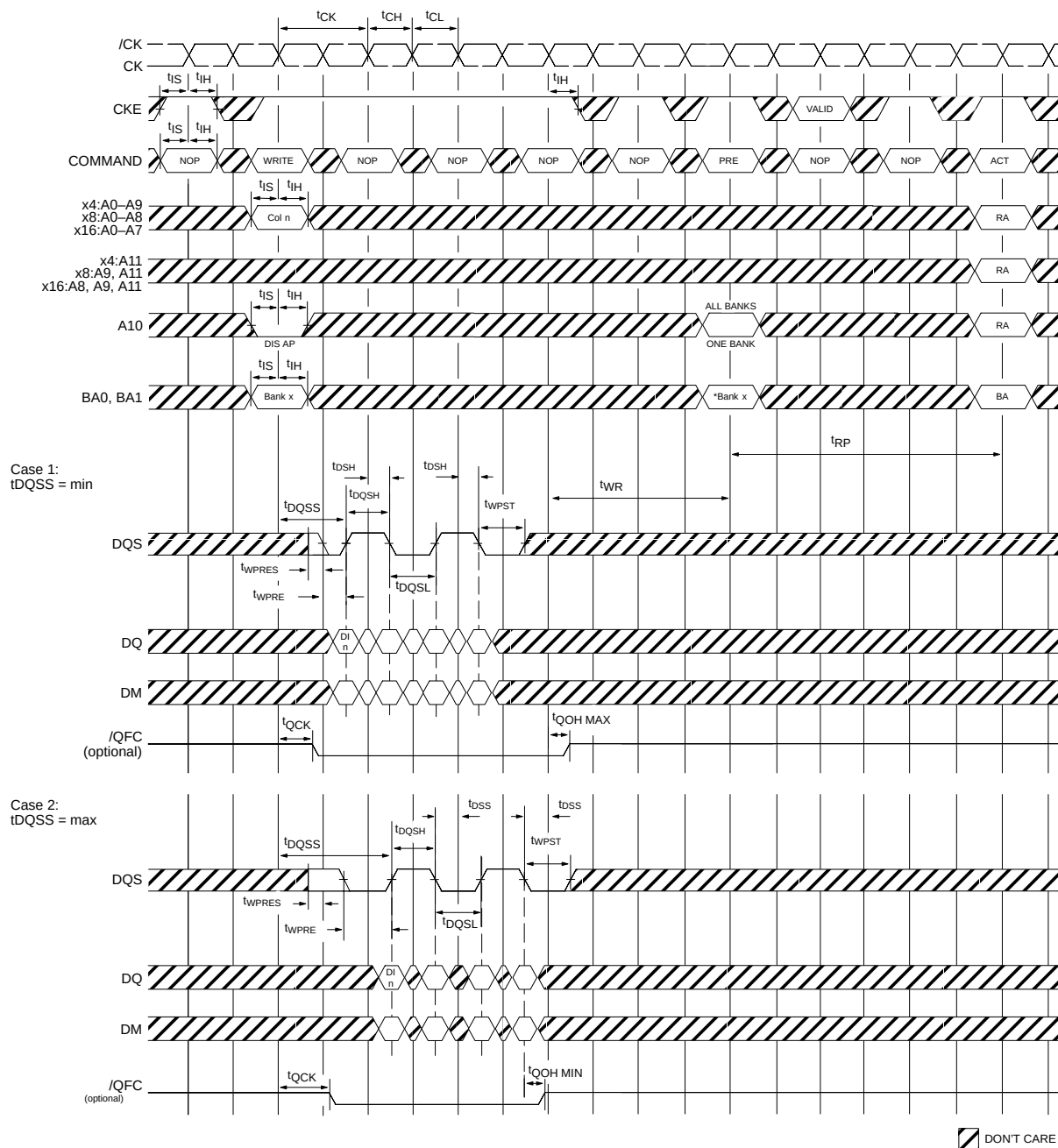
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Note that $t_{RCD} > t_{RCD\ MIN}$ so that the same timing applies if Autoprecharge is enabled (in which case t_{RAS} would be limiting)

□ DON'T CARE

Figure 45 – BANK READ ACCESS



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n

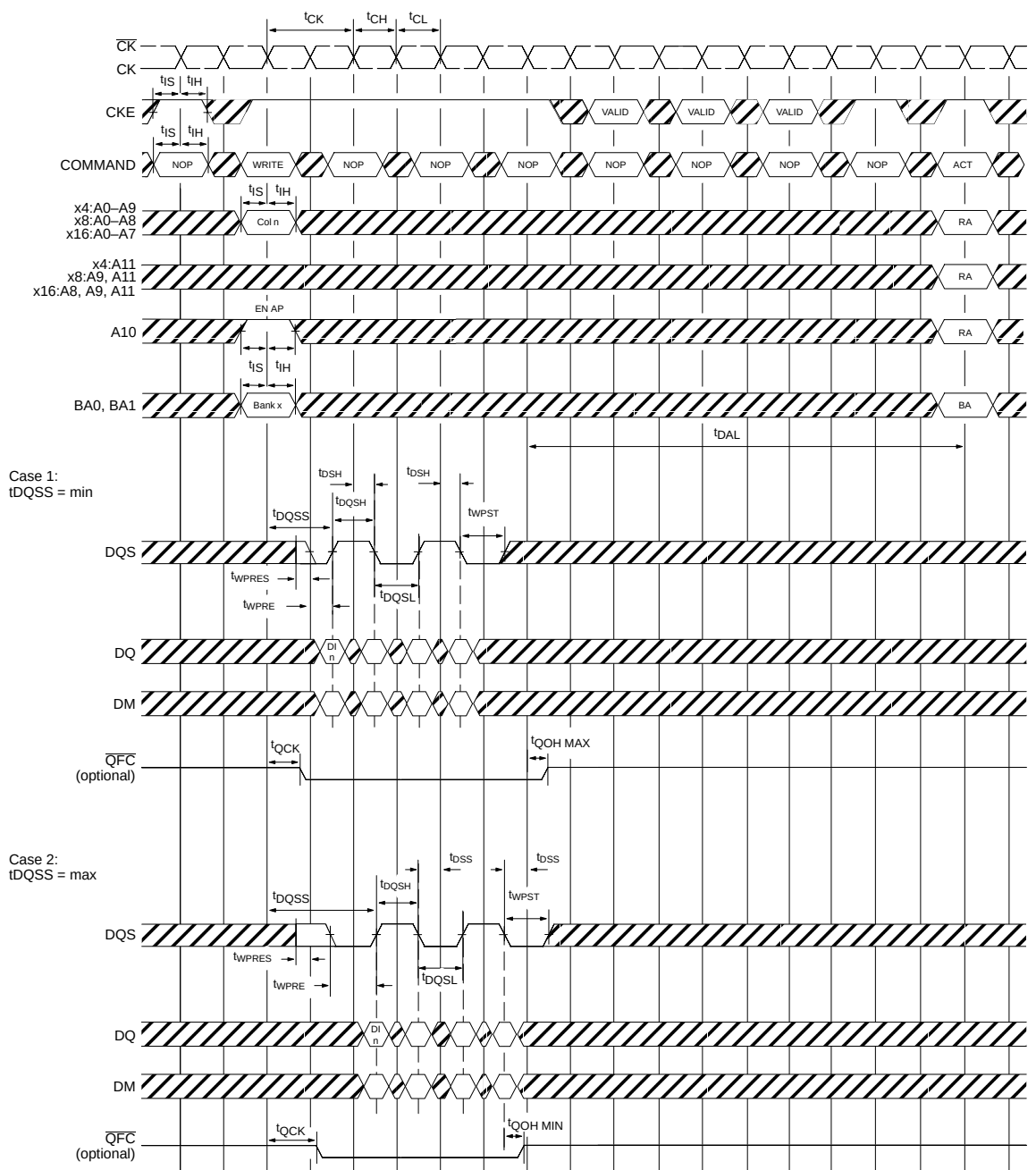
DIS AP = Disable Autoprecharge

* = "Don't Care", if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 46 – WRITE – WITHOUT AUTO PRECHARGE



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI

EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

□ DON'T CARE

Figure 47 – WRITE – WITH AUTO PRECHARGE

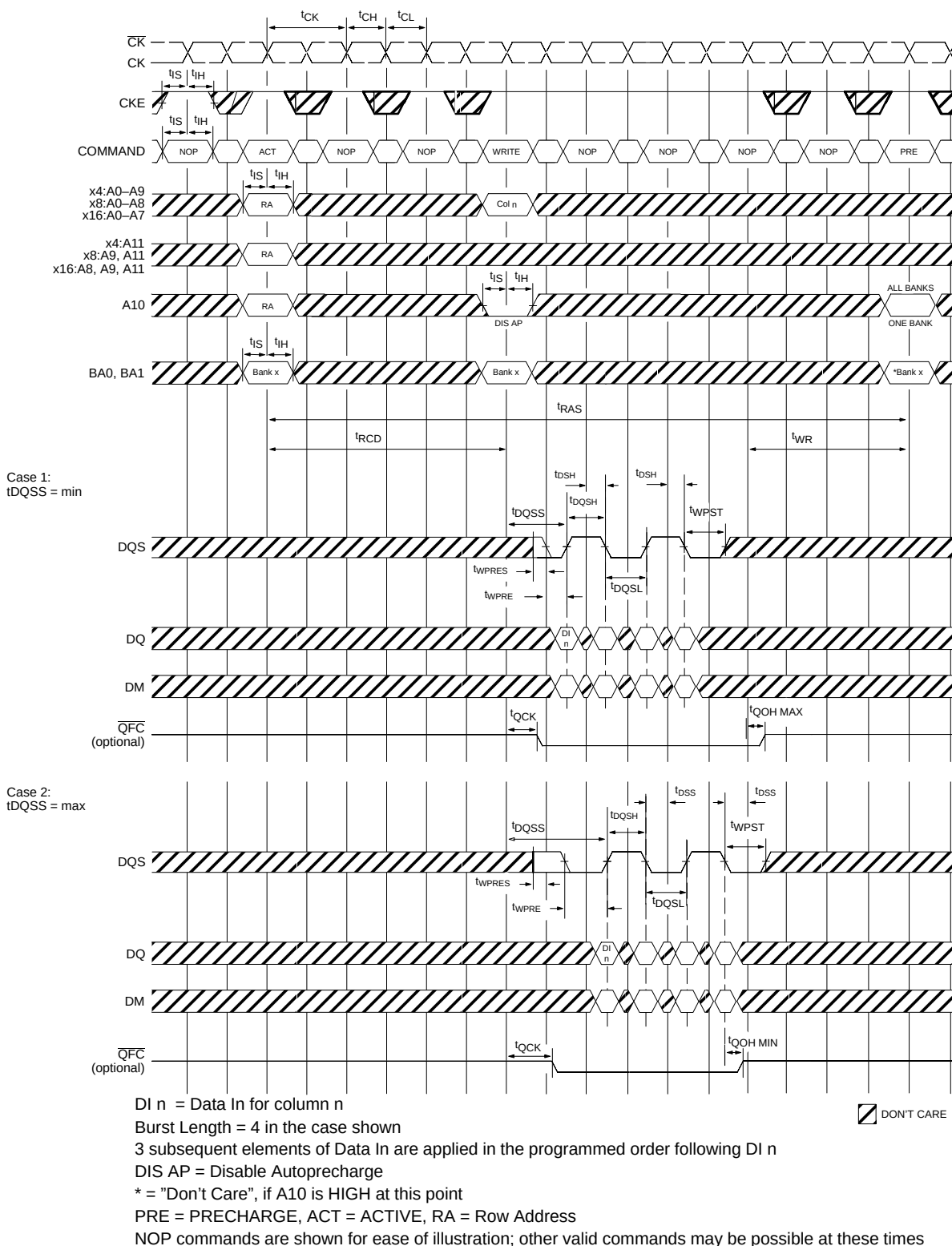
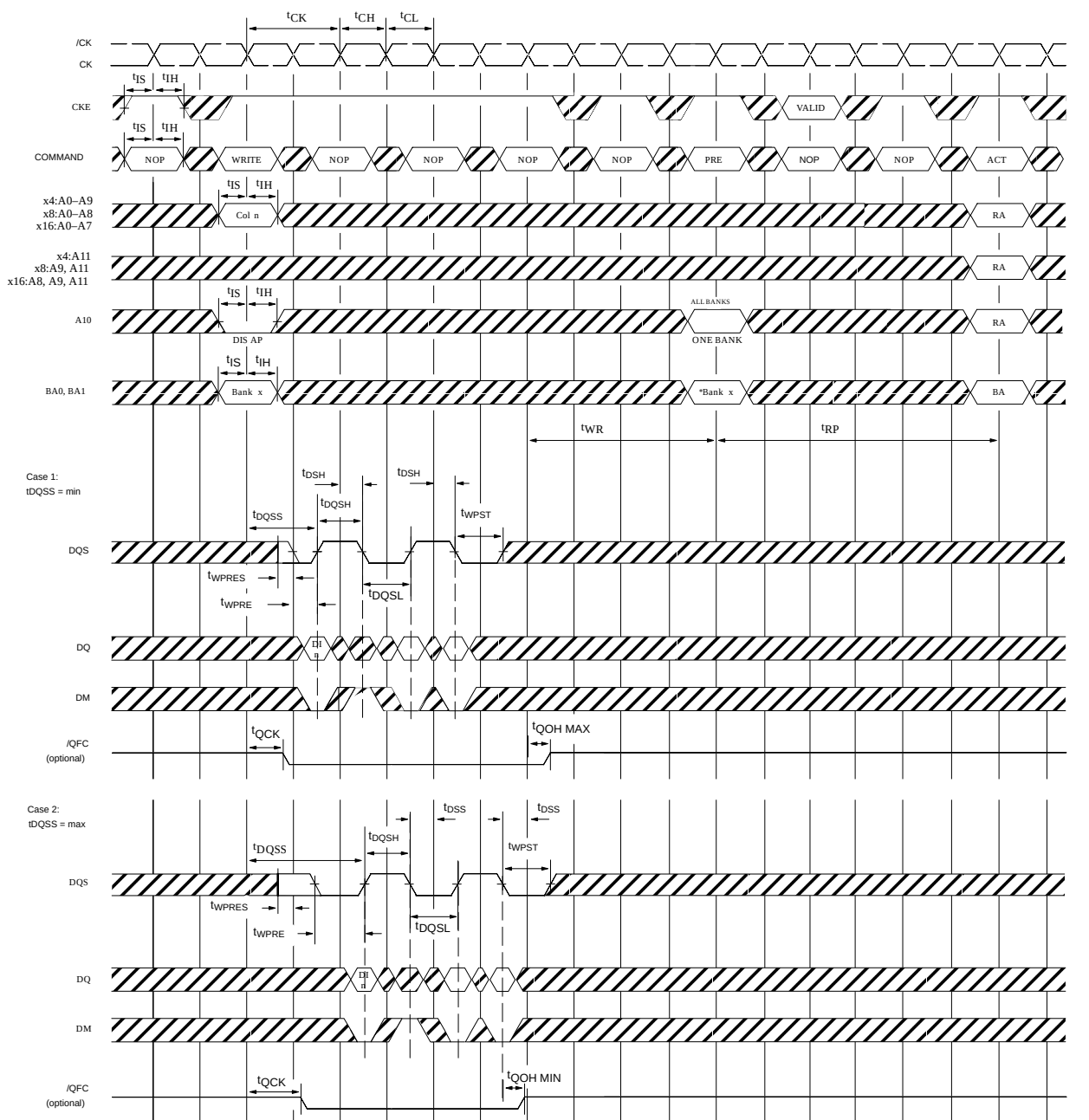


Figure 48 – BANK WRITE ACCESS



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n (the second element of the four is masked)

DIS AP = Disable Autoprecharge

* = "Don't Care", if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

▨ DON'T CARE

Figure 49 – WRITE _ DM OPERATION

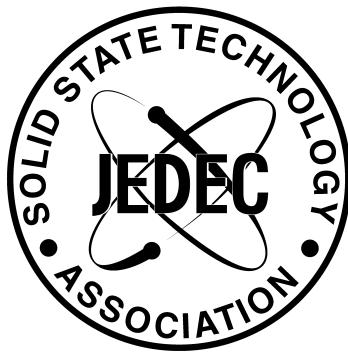


Exhibit F

JEDEC STANDARD

Double Data Rate (DDR) SDRAM Specification

JESD79

(Release 2)

MAY 2002

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

(From JEDEC Board Ballot JCB-99-70, and modified by numerous other Board Ballots, formulated under the cognizance of Committee JC-42.3 on DRAM Parametrics.)

Standard No. 79 Revision Log.

Release 1, June 2000

Release 2, May 2002

Scope

This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M X4 (4 M X4 X4 banks), 8 M X8 (2 M X8 X4 banks), 4 M X16 (1 M X16 X4 banks)
 32 M X4 (8 M X4 X4 banks), 16 M X8 (4 M X8 X4 banks), 8 M X16 (2 M X16 X4 banks)
 64 M X4 (16 M X4 X4 banks), 32 M X8 (8 M X8 X4 banks), 16 M X16 (4 M X16 X4 banks)
 128 M X4 (32 M X4 X4 banks), 64 M X8 (16 M X8 X4 banks), 32 M X16 (8 M X16 X4 banks)
 256 M X4 (64 M X4 X4 banks), 128 M X8 (32 M X8 X4 banks), 64 M X16 (16 M X16 X4 banks)

FEATURES

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ = +2.5 V ± 0.2 V
- VDD = +3.3 V ± 0.3 V or +2.5 V ± 0.2 V

GENERAL DESCRIPTION

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64 Mb has 67,108,864 bits
 128 Mb has 134,217,728 bits
 256 Mb has 268,435,456 bits
 512 Mb has 536,870,912 bits
 1 Gb has 1,073,741,824 bits

The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller

during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The DDR SDRAM operates from a differential clock (CK and $\overline{\text{CK}}$; the crossing of CK going HIGH and $\overline{\text{CK}}$ going LOW will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices may have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC X4/X8/X16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

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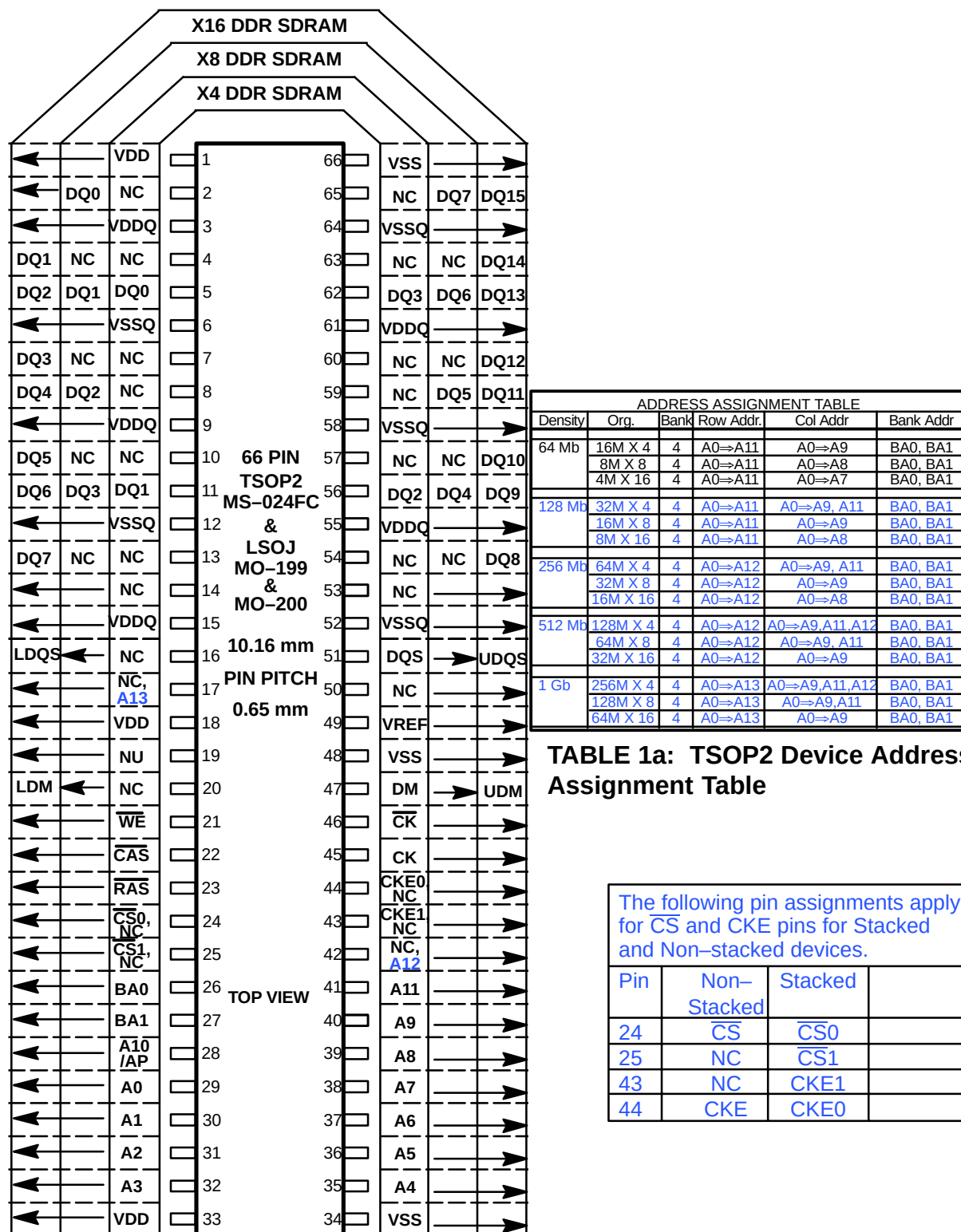
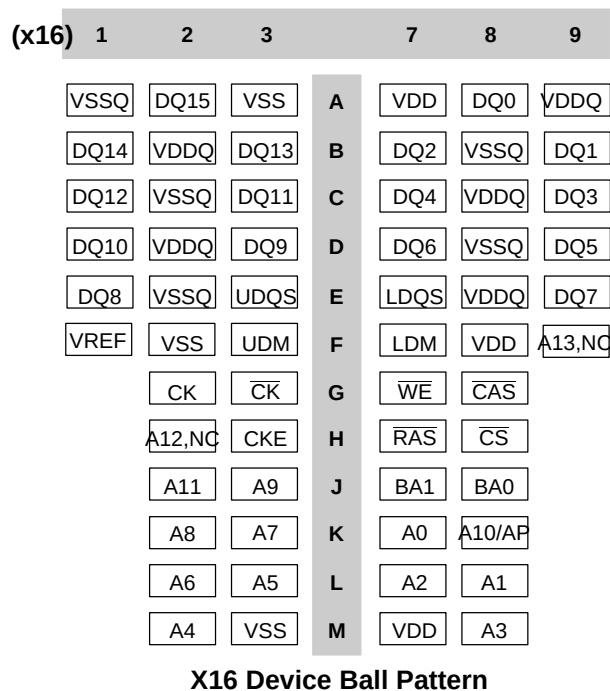
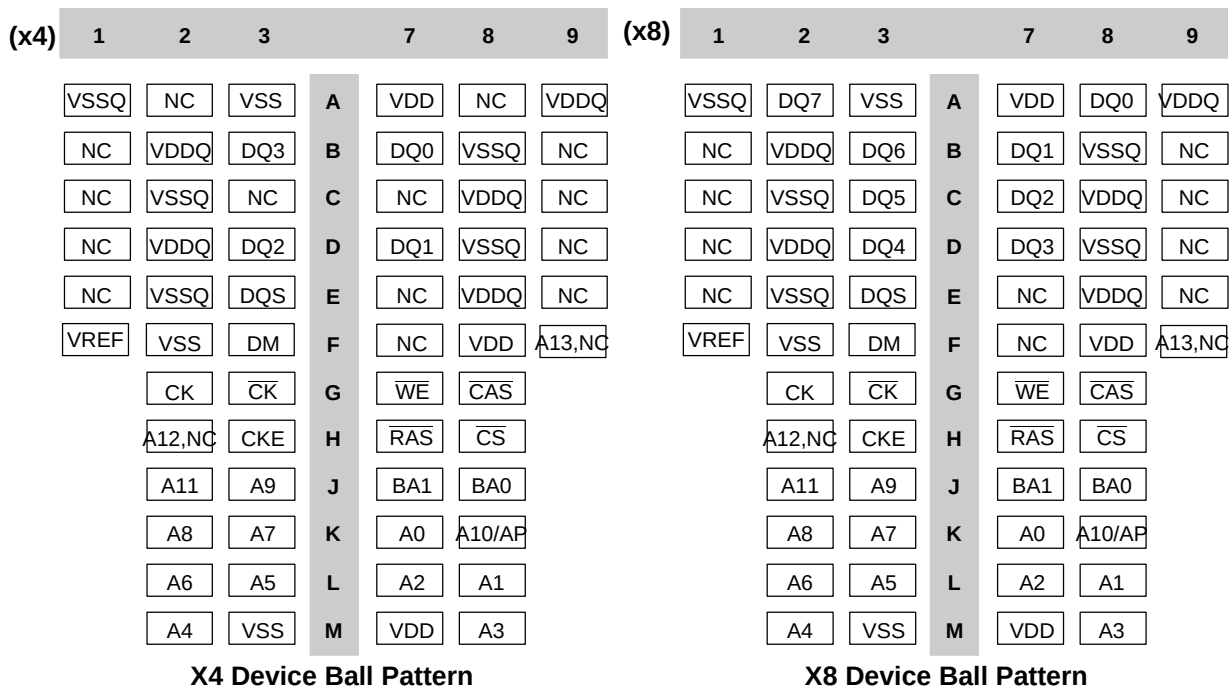


TABLE 1a: TSOP2 Device Address Assignment Table

The following pin assignments apply for $\overline{CS}$ and CKE pins for Stacked and Non-stacked devices.

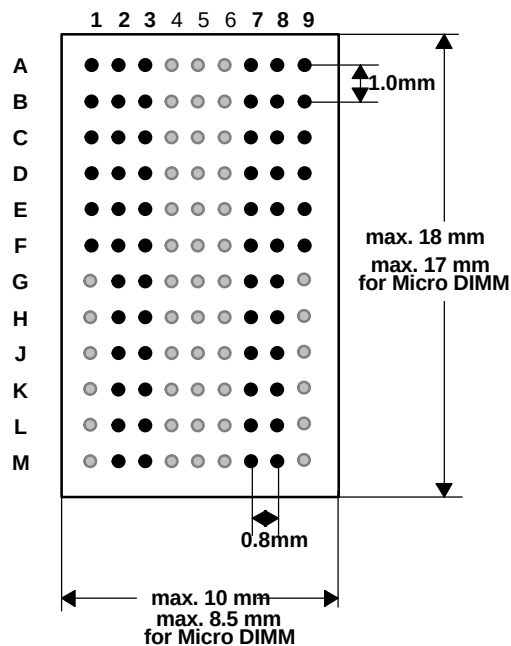
Pin	Non-Stacked	Stacked
24	$\overline{CS}$	$\overline{CS0}$
25	NC	$\overline{CS1}$
43	NC	CKE1
44	CKE	CKE0

Figure 1
64 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN TSOP2 & LSOJ



● : Ball Existing [For Reference Only]
○ : Depopulated Ball

Top View(See the balls through the Package)

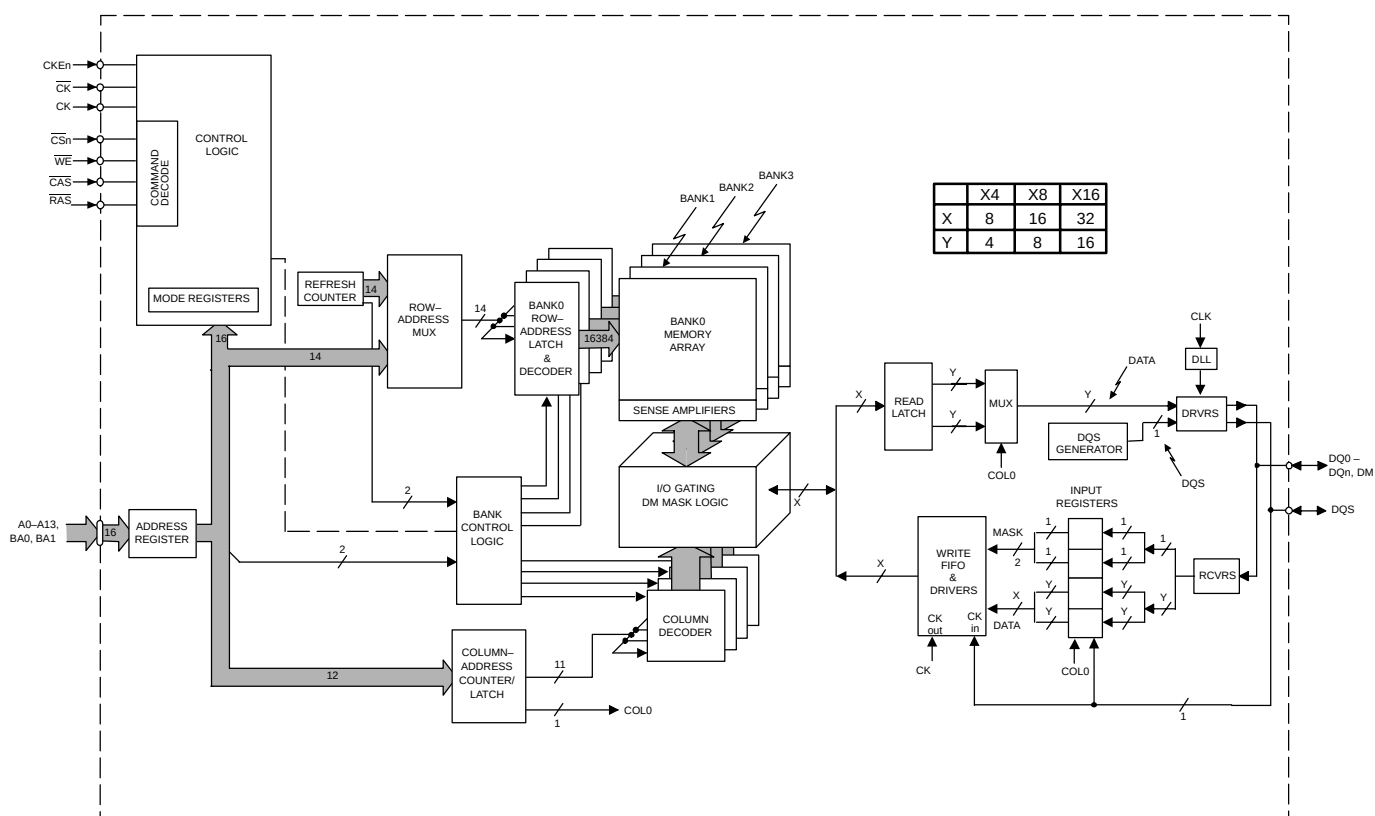


**BGA Package Ball Pattern,
Top View**

Figure 2
128 Mb Through 1Gb DDR SDRAM (X4, X8, & X16) IN BGA

Item	128Mb	256Mb	512Mb	1Gb	Note
Number of banks	4	4	4	4	
Bank Address Pins	BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1	
Autoprecharge Pins	A10/AP	A10/AP	A10/AP	A10/AP	
Row Addresses	A0-A11	A0-A12	A0-A12	A0-A13	
Column Addresses x4	A0-A9,A11	A0-A9,A11	A0-A9,A11,A12	A0-A9,A11,A12	
x8	A0-A9	A0-A9	A0-A9,A11	A0-A9,A11	
x16	A0-A8	A0-A8	A0-A9	A0-A9	
H2 pin function	NC	A12	A12	A12	
F13 pin function	NC	NC	NC	A13	
JC11 MO #	MO-233A	MO-233A	MO-233A	MO-233A	
JC11 Variation #	AA	AA	AA	AA	
JC11 Package Name	DSBGA	DSBGA	DSBGA	DSBGA	
Pin Pitch	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	0.8 mm x 1.0 mm	

TABLE 1b: BGA Device Address Assignment and Package Table



Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

FIGURE 3: FUNCTIONAL BLOCK DIAGRAM OF DDR SDRAM

TABLE 2: PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE (CKE0) (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{\text{CK}}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied. The standard pinout includes one CKE pin. Optional pinouts include CKE0 and CKE1 on different pins, to facilitate device stacking.
$\overline{\text{CS}}$ (CS0) (CS1)	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered high. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code. The standard pinout includes one $\overline{\text{CS}}$ pin. Optional pinouts include CS0 and CS1 on different pins, to facilitate device stacking.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM (LDM) (UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the X16, LDM corresponds to the data on DQ0–DQ7; UDM corresponds to the data on DQ8–DQ15. <i>DM may be driven high, low, or floating during READs.</i>
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0–A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS). <i>A12 is used on device densities of 256Mb and above; A13 is used on device densities of 1Gb.</i>
DQ	I/O	Data Bus: Input/Output.
DQS (LDQS) (UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0–DQ7; UDQS corresponds to the data on DQ8–DQ15.
NC	—	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: +2.5 V $\pm$ 0.2 V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply: One of +3.3 V $\pm$ 0.3 V or +2.5 V $\pm$ 0.2 V (device specific).
VSS	Supply	Ground.
VREF	Input	SSTL_2 reference voltage.

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64Mb has 67,108,864 bits

128Mb has 134,217,728 bits

256Mb has 268,435,456 bits

512Mb has 536,870,912 bits

1Gb has 1,073,741,824 bits

The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. DQ, DQS, & DM may be floated when no data is being transferred.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A13 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. **No power sequencing is specified during power up and power down given the following criteria:**

- VDD and VDDQ are driven from a single power converter output, AND
- VTT is limited to 1.35 V, AND
- VREF tracks VDDQ/2

OR, the following relationships must be followed:

- VDDQ is driven after or with VDD such that $VDDQ < VDD + 0.3 \text{ V}$ AND
- VTT is driven after or with VDDQ such that

$VTT < VDDQ + 0.3 \text{ V}$, AND

- VREF is driven after or with VDDQ such that $VREF < VDDQ + 0.3 \text{ V}$.

At least one of these two conditions must be met.

Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μs delay prior to applying an executable command.

Once the 200 μs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the "all banks idle" state.

Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 4. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A13 or (A12 on 256Mb/512Mb, A13 on 1Gb see figure 4) specify the operating mode.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Table 3
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0–1	0–1
	1	1–0	1–0
4	A1 A0		
	0 0	0–1–2–3	0–1–2–3
	0 1	1–2–3–0	1–0–3–2
	1 0	2–3–0–1	2–3–0–1
	1 1	3–0–1–2	3–2–1–0
8	A2 A1 A0		
	0 0 0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0 0 1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0 1 0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0 1 1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1 0 0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1 0 1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1 1 0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1 1 1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0

Notes:

- For a burst length of two, A1–Ai selects the two–data–element block; A0 selects the first access within the block.
- For a burst length of four, A2–Ai selects the four–data–element block; A0–A1 selects the first access within the block.
- For a burst length of eight, A3–Ai selects the eight–data–element block; A0–A2 selects the first access within the block.
- Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–Ai when the burst length is set to two, by A2–Ai when the burst length is set to four and by A3–Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

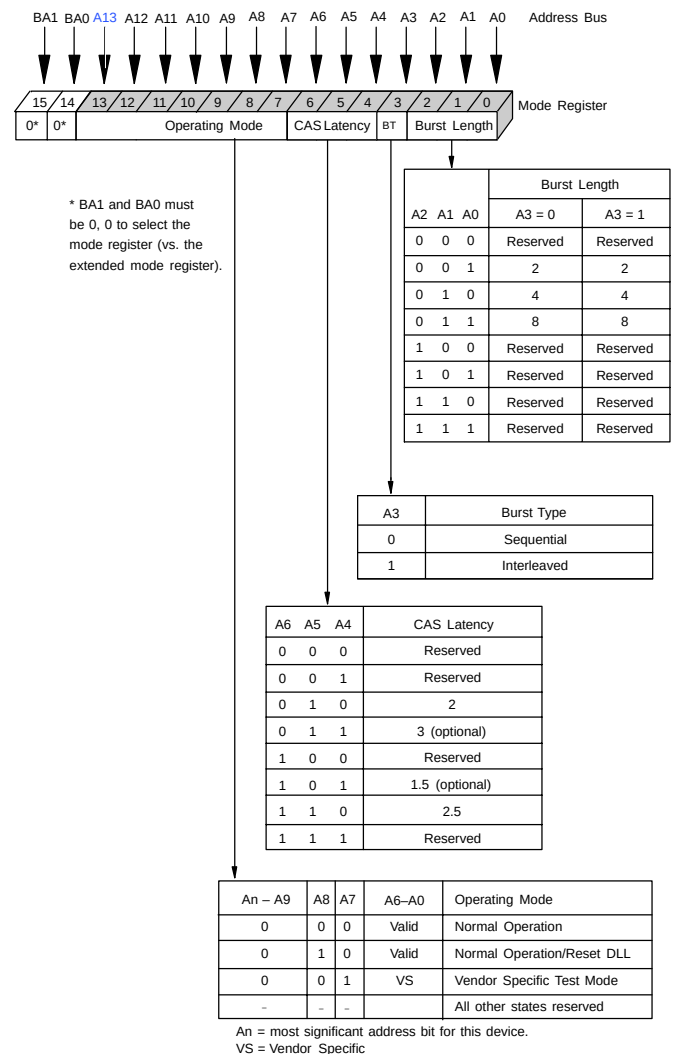


Figure 4
Mode Register Definition

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 3.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors).

If a READ command is registered at clock edge n , and the latency is m clocks, the data will be available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation, or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7–A13 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9–A13 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7–A13 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

DDR266: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency). The corresponding nominal data rate is *266 MHz.

DDR333: A Speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 167 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 167 MHz clock frequency). The corresponding nominal data rate is *333 MHz.

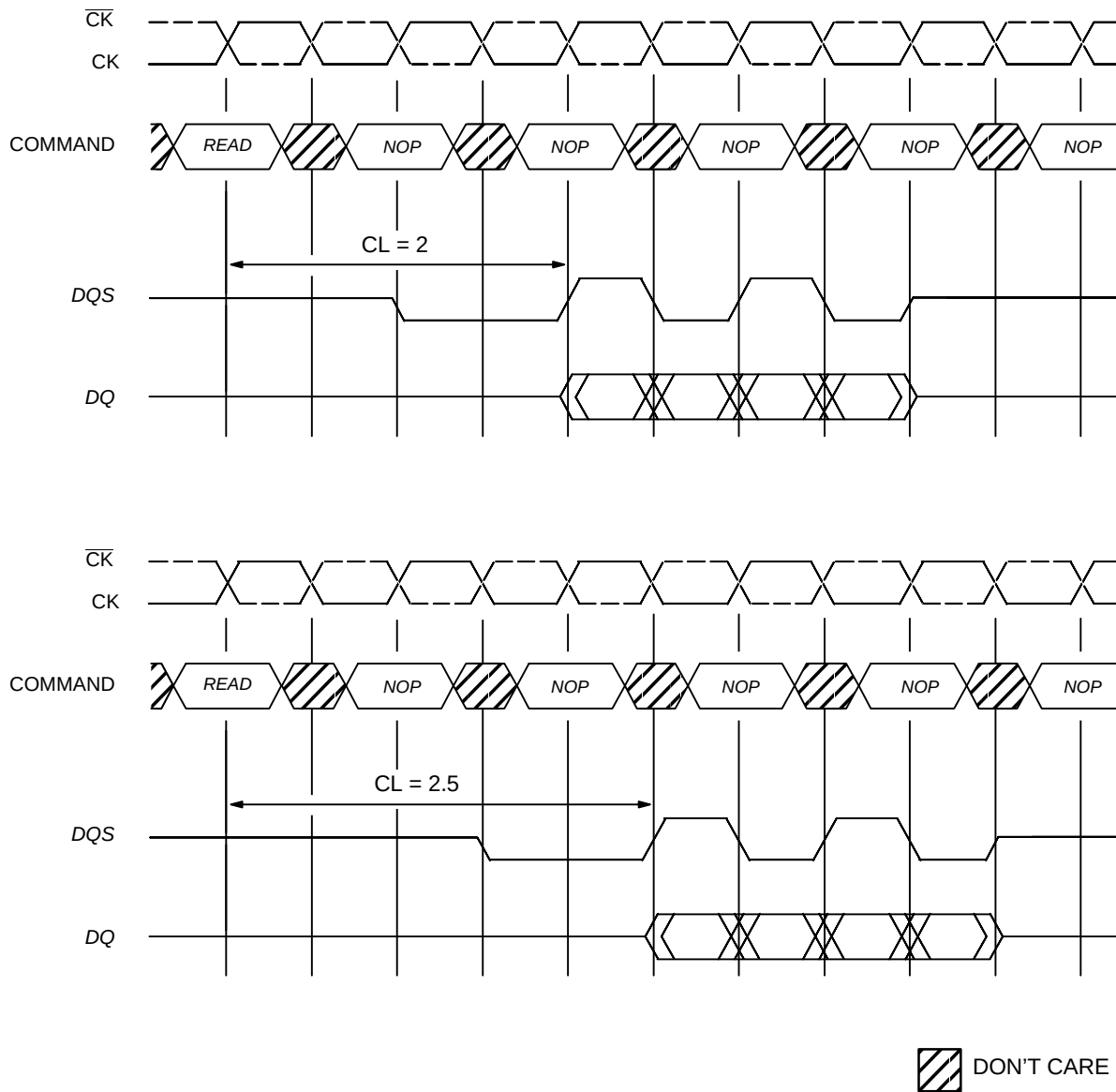
In addition to the above DDRxxx specification, a letter modifier may be applied to indicate special timing characteristics for these devices in various market applications. For example, DDR266A and DDR266B classifications define distinct sorts for operation as a function of CAS latency. These differences between sorts are described in Table 10, "AC Timing Variations".

* In this context, the term MHz is used loosely. A more technically precise definition is "million transfers per second per data pin"

Terminology Definitions.

The following are definitions of the terms DDR200, DDR266, & DDR333, as used in this specification.

DDR200: A speed grade for DDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz (meaning that although the devices operate over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency). The corresponding nominal data rate is *200 MHz.



Burst Length = 4 in the cases shown
Shown with nominal t_{DQSCK}

Figure 5
REQUIRED CAS LATENCIES

EXTENDED MODE REGISTER

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output drive strength selection (optional). These functions are controlled via the bits shown in Figure 6. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Some vendors might also support a weak driver strength option, intended for lighter load and/or point-to-point environments. I-V curves for the normal drive strength and weak drive strength are included in this document.

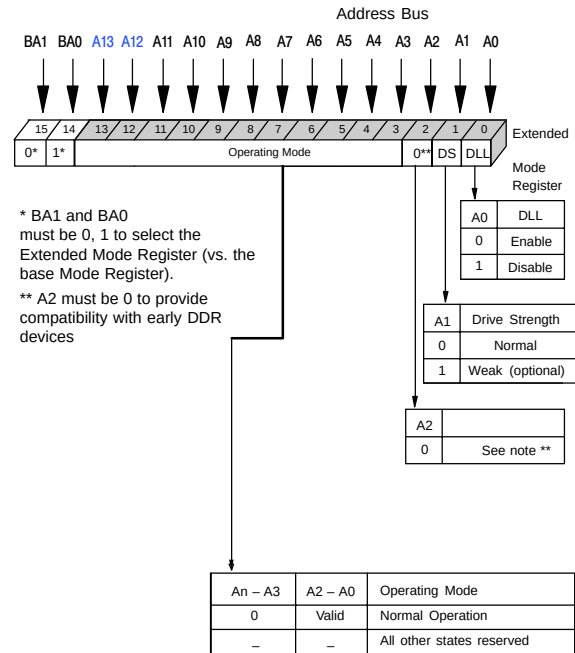


Figure 6
EXTENDED MODE REGISTER
DEFINITION

COMMANDS

Truth Table 1a provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1a – Commands

(Notes: 1)

NAME (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7
MODE REGISTER SET	L	L	L	L	Op-Code	2

TRUTH TABLE 1b – DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTE: 1. CKE is HIGH for all commands shown except SELF REFRESH.

- BA0–BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0–BA1 are reserved; A0–A13 provide the op-code to be written to the selected Mode Register.
- BA0–BA1 provide bank address and A0–A13 provide row address.
- BA0–BA1 provide bank address; A0–Ai provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
- A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
- This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
- Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
- Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
- DESELECT and NOP are functionally interchangeable.
- Used to mask write data, provided coincident with the corresponding data.

TRUTH TABLE 2 – CKE

(Notes: 1–4)

CKEn–1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power–Down	X	Maintain Power–Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power–Down	DESELECT or NOP	Exit Power–Down	
L	H	Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power–Down Entry	
H	L	Bank(s) Active	DESELECT or NOP	Active Power–Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

- NOTE: 1. CKEn is the logic state of CKE at clock edge n; CKEn–1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. Deselect or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

TRUTH TABLE 3 – Current State Bank n – Command to Bank n

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto–Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

- This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
- This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
- Current state definitions:
 - Idle: The bank has been precharged, and tRP has been met.
 - Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
 - Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
 - Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
- The following states must not be interrupted by a command issued to the same bank. Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
 - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
 - Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the "row active" state.
 - Read w/Auto–Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
 - Write w/Auto–Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE (continued):

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
 - Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the "all banks idle" state.
 - Accessing Mode
 - Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM will be in the "all banks idle" state.
 - Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,

TRUTH TABLE 4 – Current State Bank n – Command to Bank m

(Notes: 1–6; notes appear below and on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto– Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto– Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto– Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto– Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	3a, 7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn–1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

NOTE: (continued)

3. Current state definitions:

- Idle: The bank has been precharged, and tRP has been met.
- Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
- Read: A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
- Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.

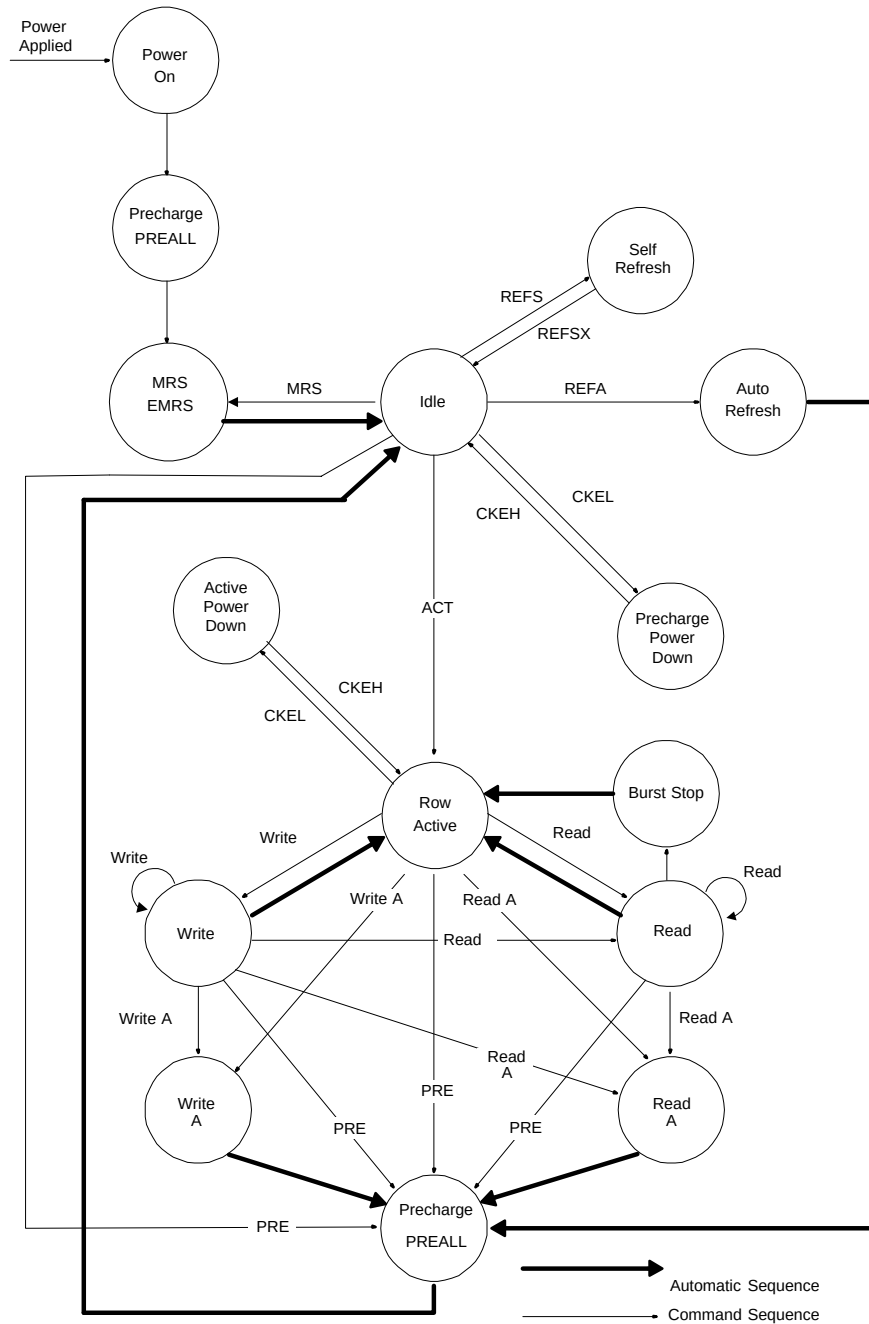
Read with Auto

Precharge Enabled: See following text

Write with Auto

Precharge Enabled: See following text

- 3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).
- 4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
- 5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
- 6. All states and sequences not shown are illegal or reserved.
- 7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
- 8. Requires appropriate DM masking.
- 9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command..



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

Figure 7
SIMPLIFIED STATE DIAGRAM

DESELECT

The Deselect function ($\overline{CS} = \text{High}$) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to a DDR SDRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A13. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A13 selects the row. This row remains active (or open) for accesses until a precharge (or READ or WRITE with AUTOPRECHARGE) is issued to that bank. A PRECHARGE (or READ or WRITE with AUTOPRECHARGE) command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai, shown in Table 4, selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

Density	Column Address			Row Address
	X16	X8	X4	
64 Mb	A0→A7	A0→A8	A0→A9	A0→A11
128 Mb	A0→A8	A0→A9	A0→A9,A11	A0→A11
256 Mb	A0→A8	A0→A9	A0→A9,A11	A0→A12
512 Mb	A0→A9	A0→A9,A11	A0→A9,A11,A12	A0→A12
1 Gb	A0→A9	A0→A9,A11	A0→A9,A11,A12	A0→A13

Table 4**ROW–COLUMN ORGANIZATION BY DENSITY**

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual Read or Write command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

REFRESH REQUIREMENTS

DDR SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing. For example, a 256 Mb DDR SDRAM has 8192 rows resulting in a tREFI of 7.8 μ s. To avoid excessive interruptions to the memory controller, higher density DDR SDRAMs maintain the 7.8 μ s average refresh time and perform multiple internal refresh bursts. In these cases, the refresh recovery times, tRFC and tXSNR, are extended to accommodate these internal operations.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS-BEFORE-RAS (CBR) refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average periodic interval of tREFI (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is $8 * tREFI$.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNRC because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command (Figure 8), which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (pre-charged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

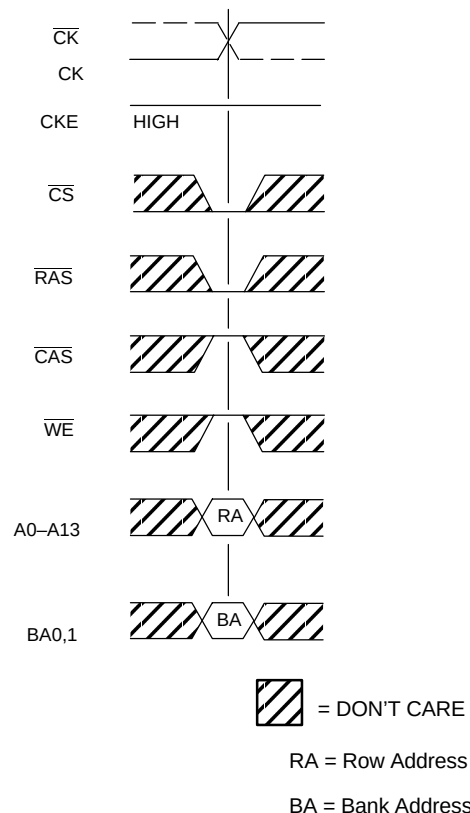


Figure 8
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

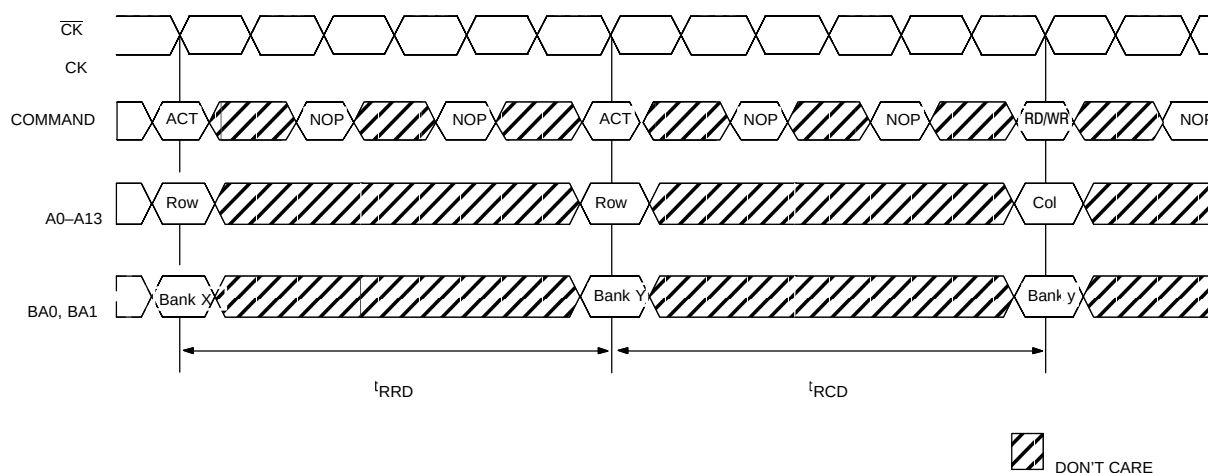


Figure 9
tRCD and tRRD Definition

Reads

READ bursts are initiated with a READ command, as shown in Figure 10.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row that is accessed will start precharge at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and $\overline{CK}$). Figure 11 shows general timing for each required (CL=2 and CL=2.5) CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 12. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive READ data is shown for illustration in Figure 13. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 14.

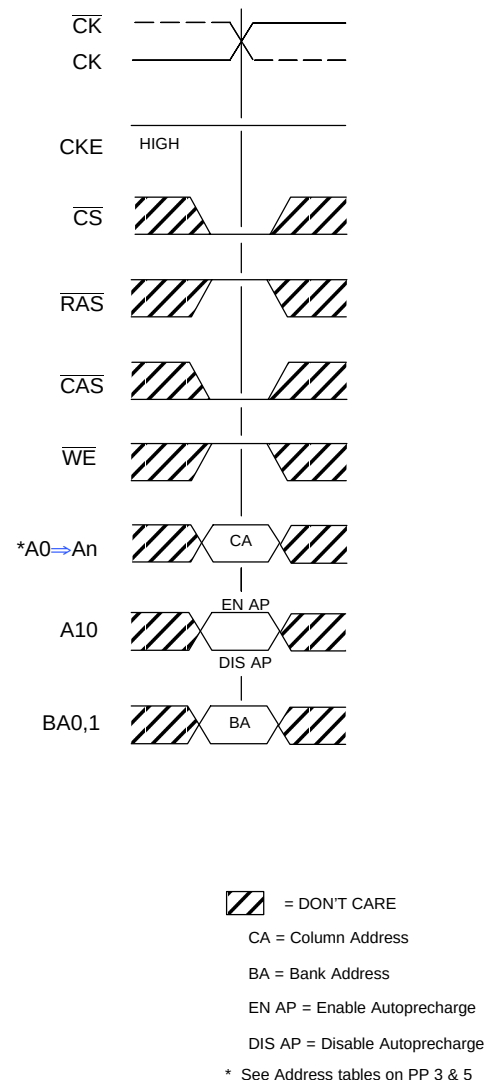


Figure 10
READ COMMAND

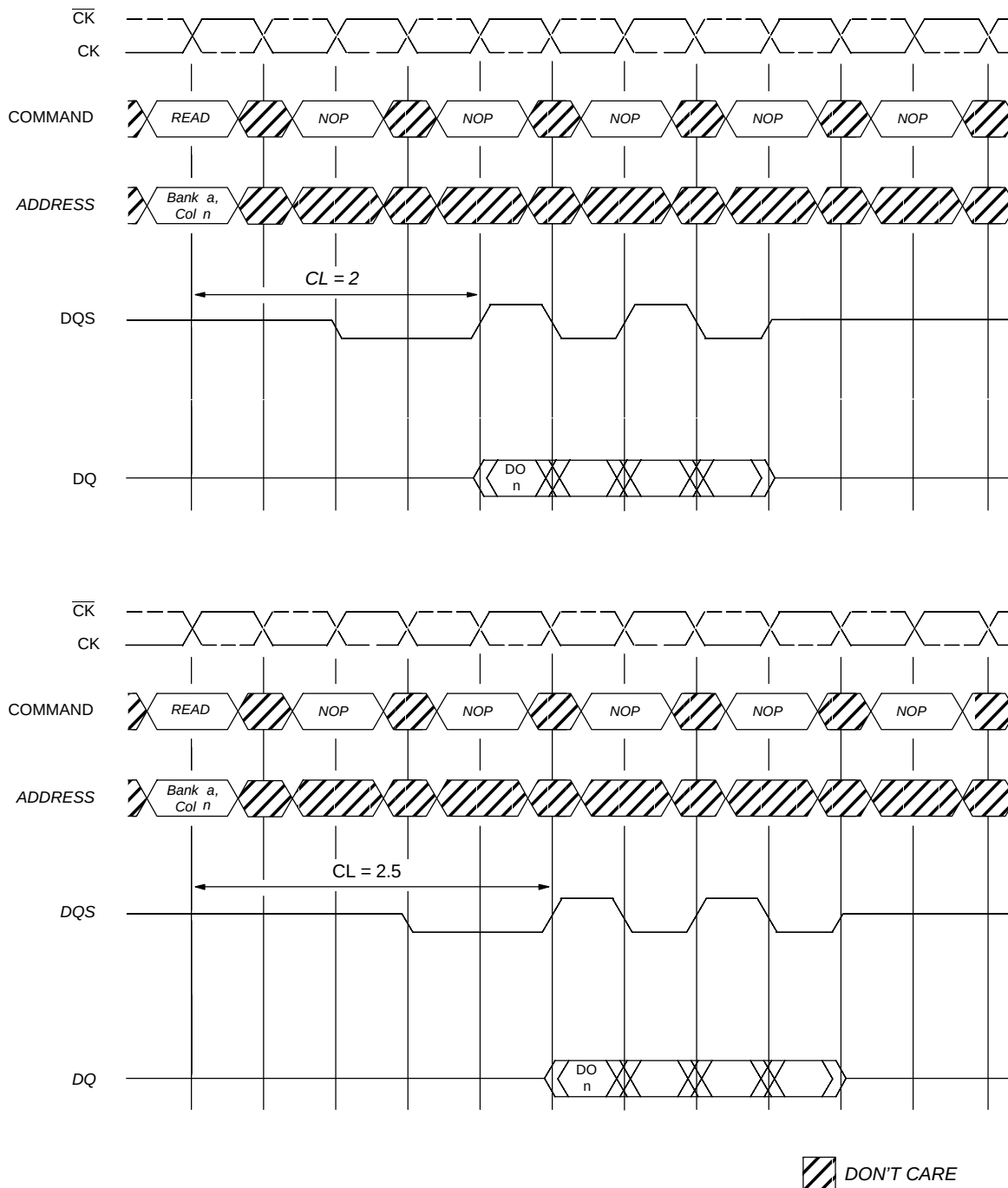
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 15. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs.

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued.

If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 16. The tDQSS MIN case is shown; the tDQSS MAX case has a longer bus idle time (tDQSS MIN and tDQSS MAX are defined in the section on WRITES).

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in Figure 17 for READ latencies of 2 and 2.5. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

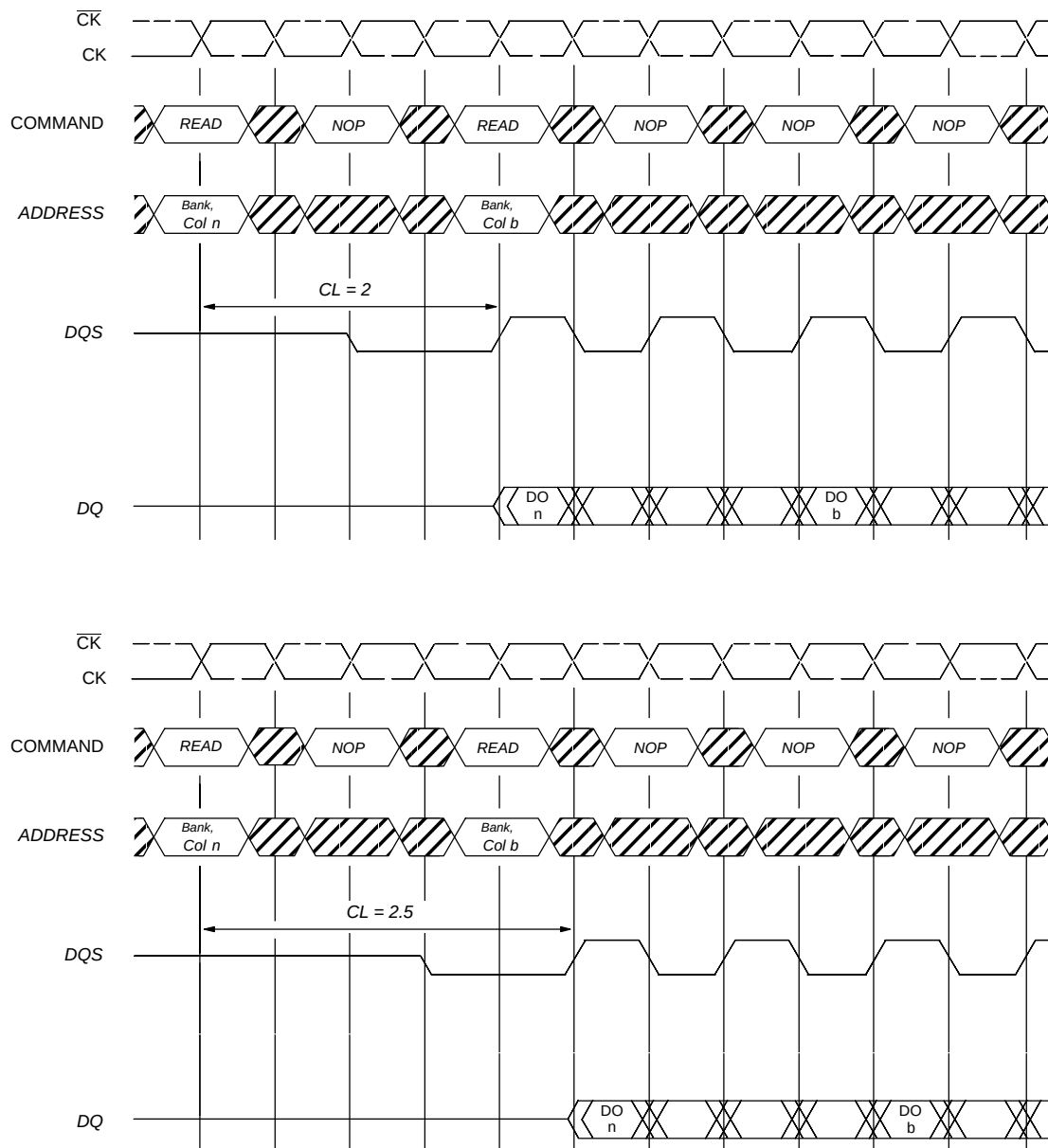


DO n = Data Out from column n

Burst Length = 4

3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 11
READ BURST – REQUIRED CAS LATENCIES



 **DON'T CARE**

DO n (or b) = Data Out from column n (or column b)

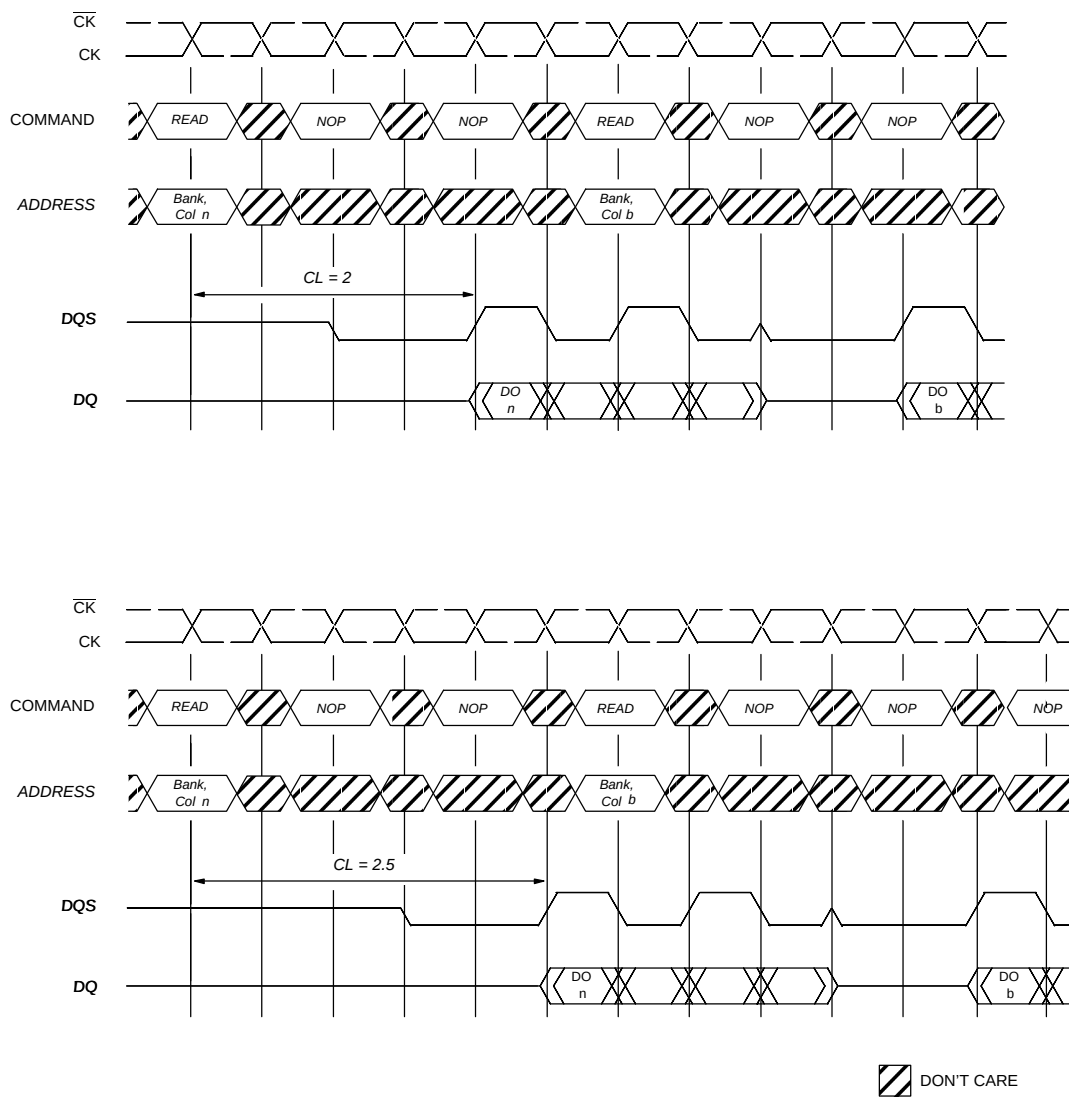
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b

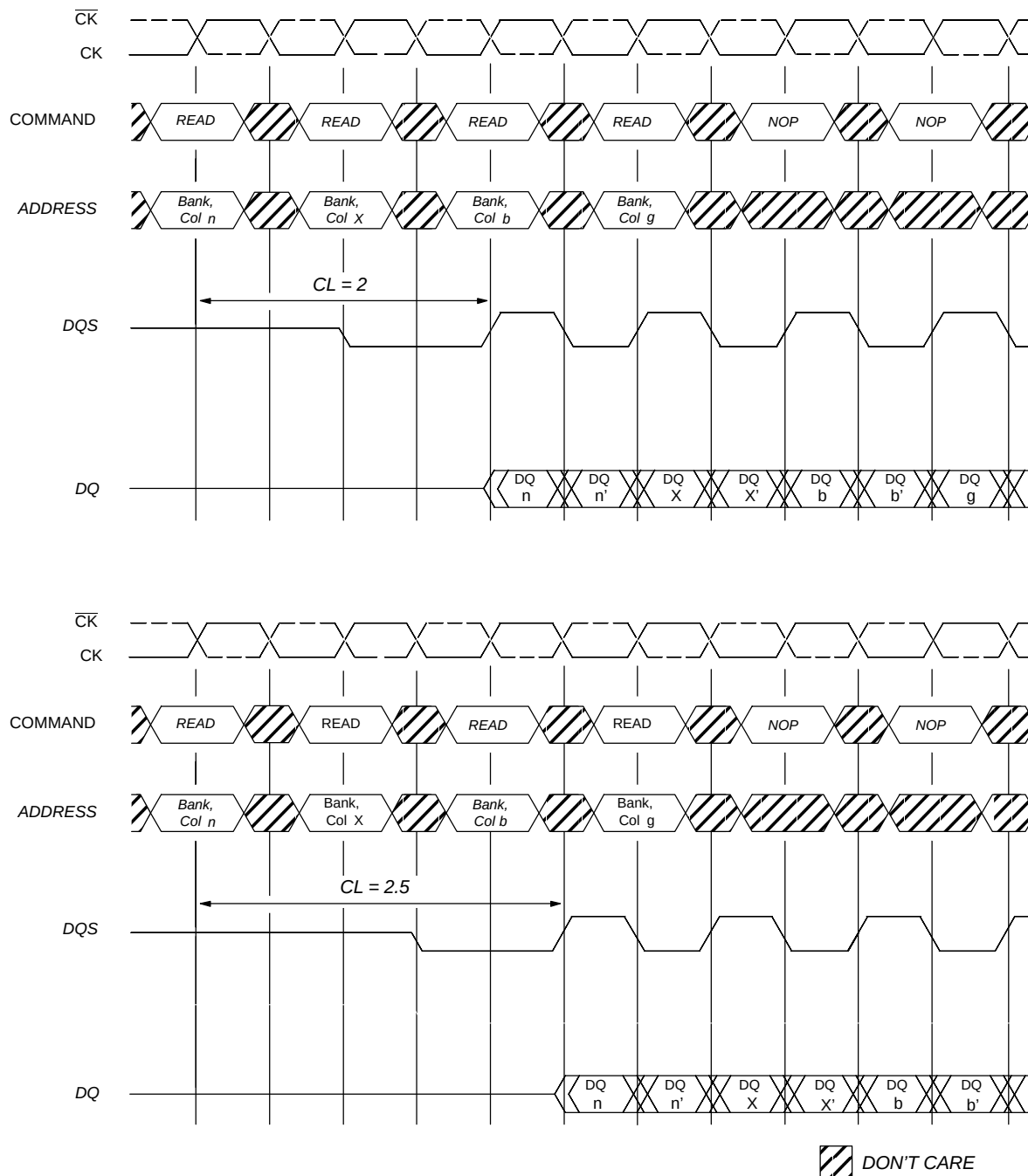
Read commands shown must be to the same device

Figure 12
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



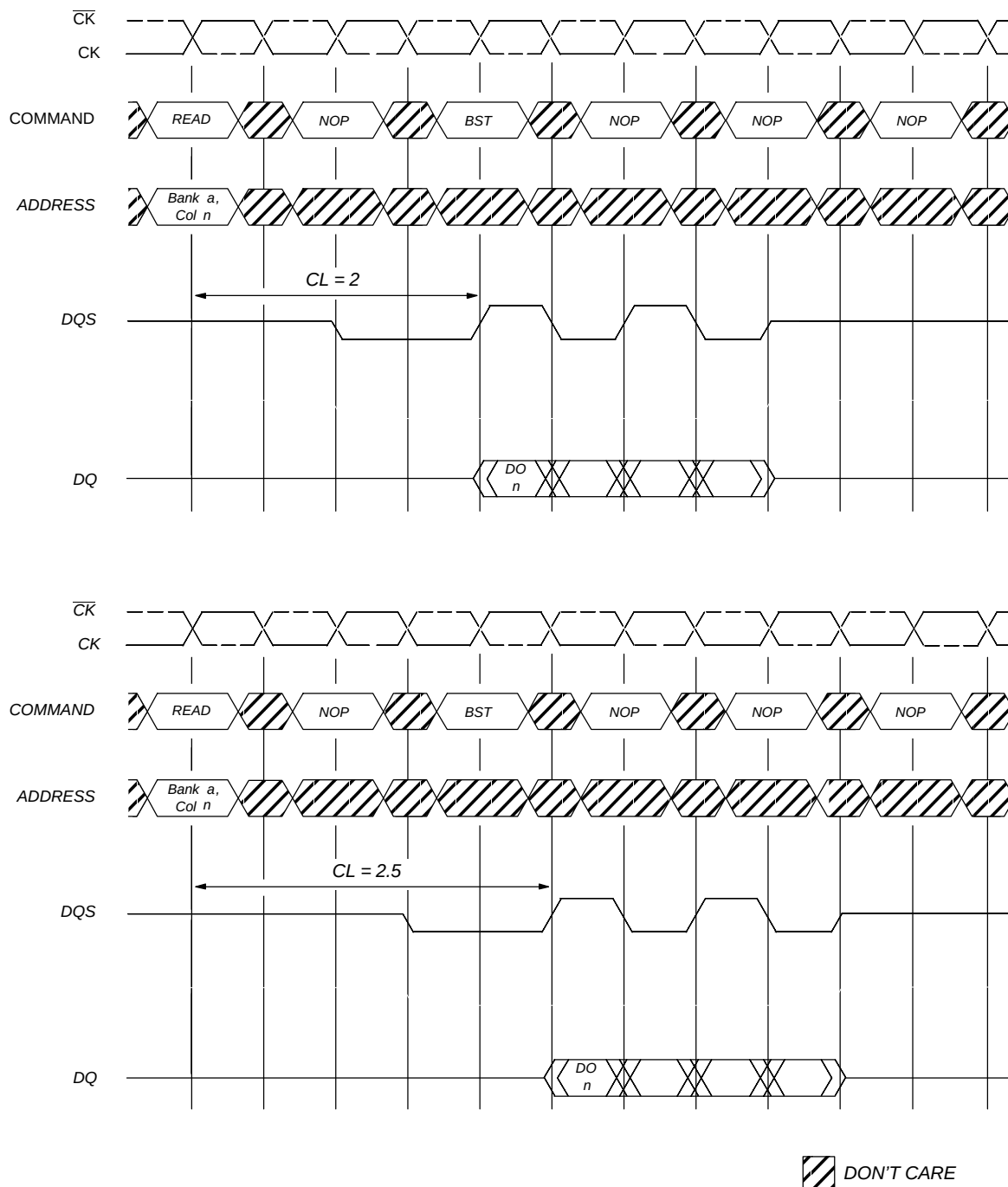
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Figure 13
NONCONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



DO n, etc. = Data Out from column n, etc.
 n', etc. = the next Data Out following DO n, etc. according to the programmed burst order
 Burst Length = 2, 4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted,
 Reads are to active rows in any banks

Figure 14
RANDOM READ ACCESSES – REQUIRED CAS LATENCIES

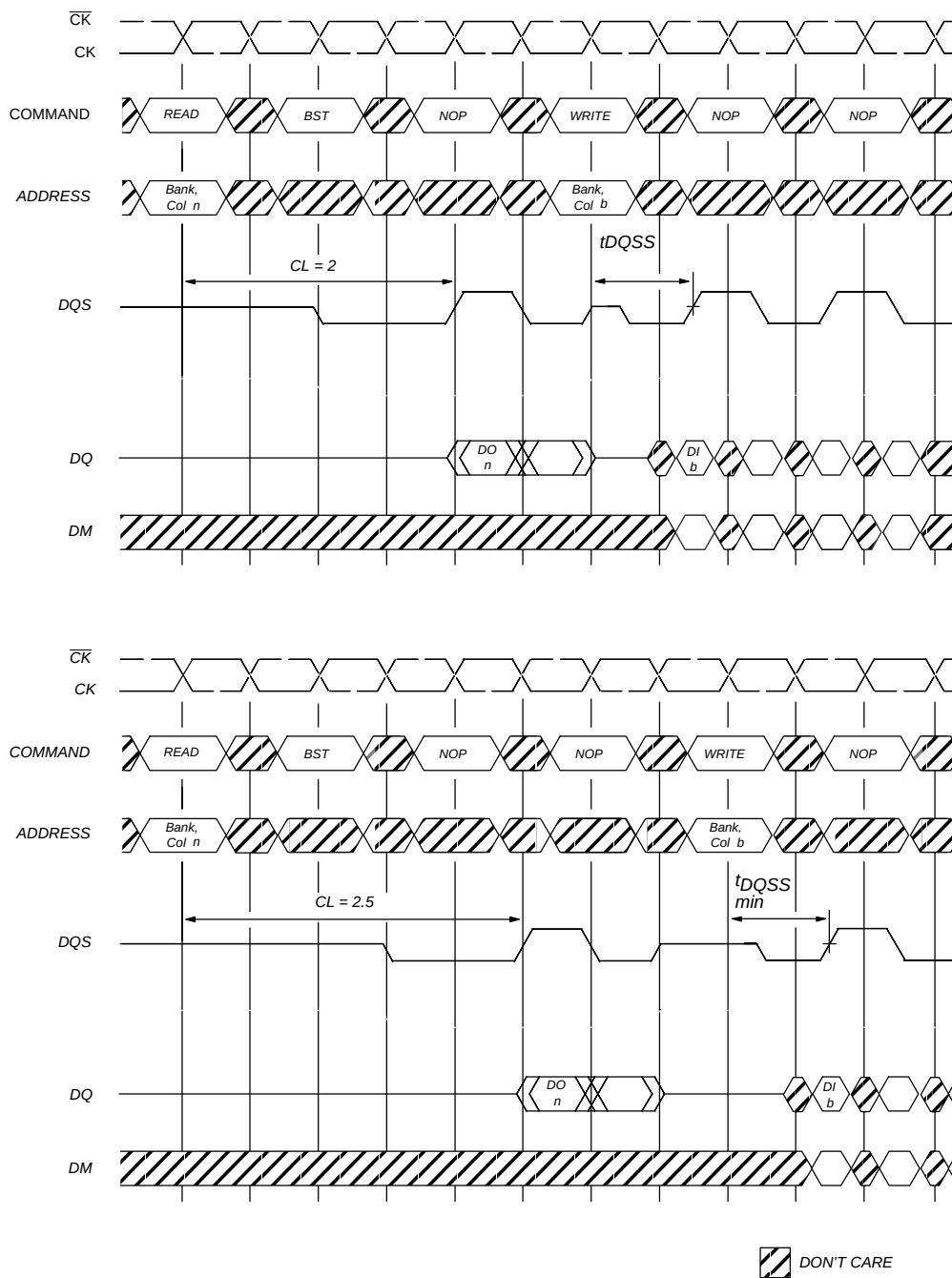


DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

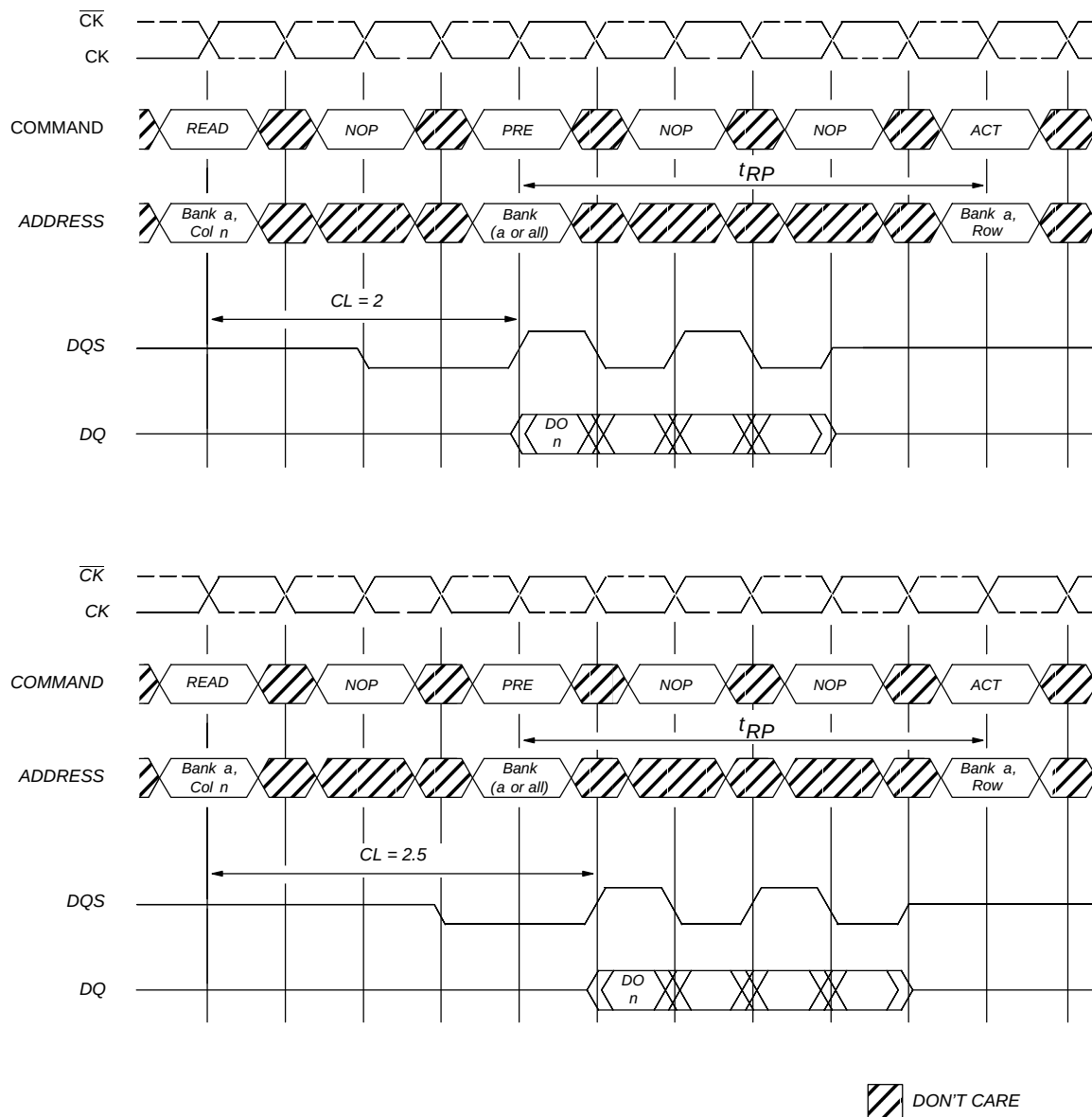
3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 15
TERMINATING A READ BURST – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
 Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
 1 subsequent element of Data Out appears in the programmed order following DO n
 Data In elements are applied following DI b in the programmed order

Figure 16
READ TO WRITE – REQUIRED CAS LATENCIES



DO_n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

3 subsequent elements of Data Out appear in the programmed order following DO_n

Precharge may be applied at $(BL/2)$ tCK after the READ command.

Note that Precharge may not be issued before t_{RAS} ns after the ACTIVE command for applicable banks.

The Active command may be applied if t_{RC} has been met.

Figure 17
READ TO PRECHARGE – REQUIRED CAS LATENCIES

Writes

WRITE bursts are initiated with a WRITE command, as shown in Figure 18.

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle). Figures 19 and 20 show the two extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Figure 22 shows concatenated bursts of 4. An example of nonconsecutive WRITES is shown in Figure 23. Full-speed random write accesses within a page or pages can be performed as shown in Figure 24.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, t_{WTR} should be met as shown in Figure 25

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figures 26. and 27. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in Figures 26 and 27.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, t_{WR} should be met as shown in Figure 28.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figures 29 and 30.

Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figures 29 and 30. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

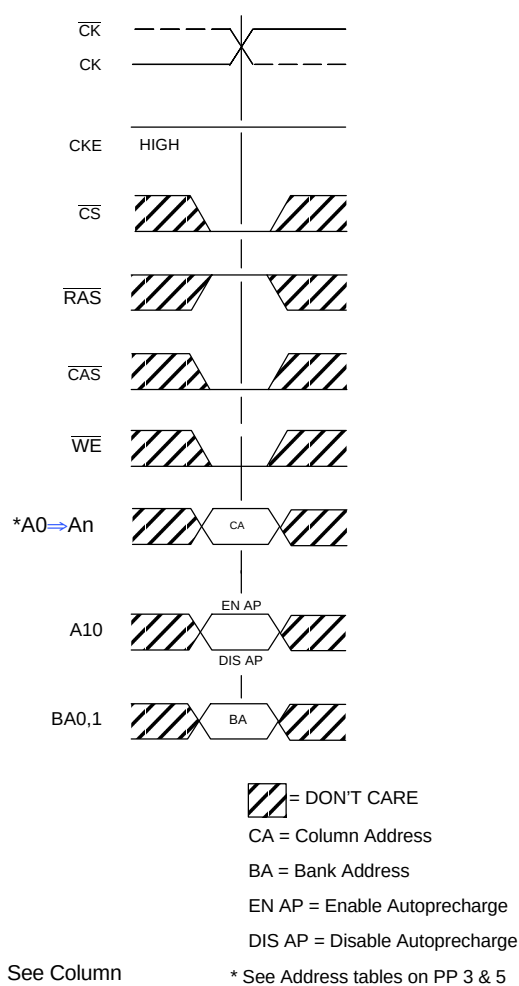
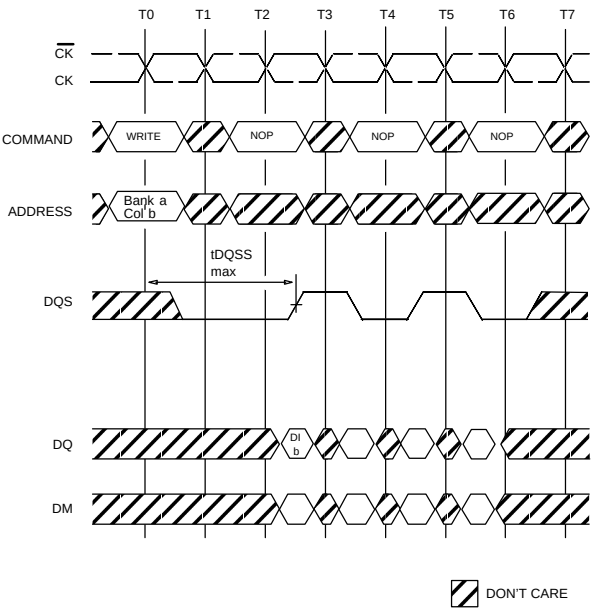
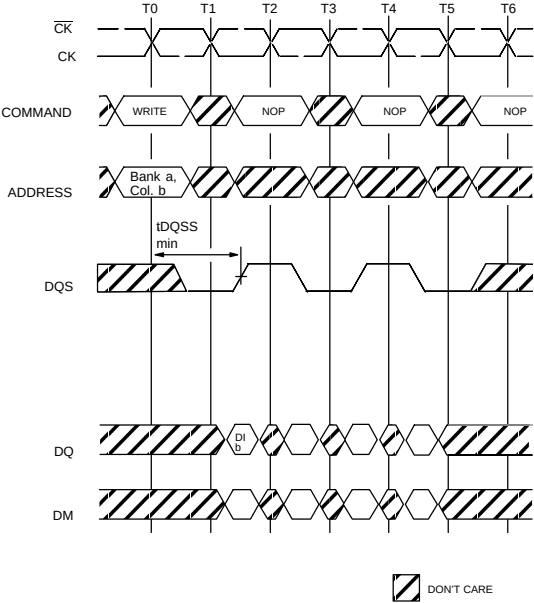


Figure 18
WRITE COMMAND



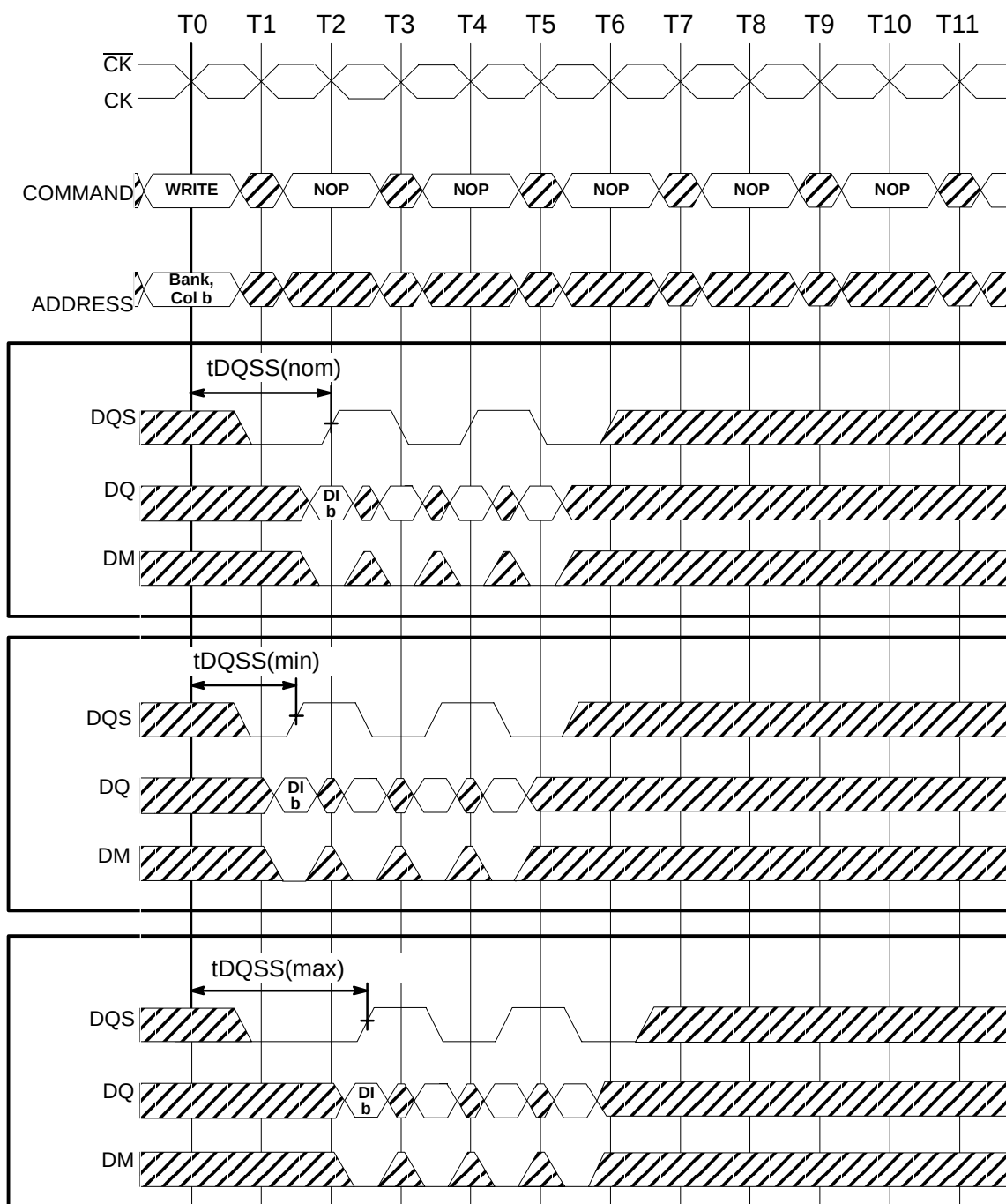
DI b = Data in for column b
3 subsequent elements of Data IN are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Figure 19
WRITE – MAX DQSS



DI b = Data In for column b
3 subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Figure 20
WRITE – MIN DQSS



DI b = Data In for column b

Three elements of data are applied in the programmed order following DI

A noninterrupted burst of 4 is shown

A10 is low with the WRITE command (autoprecharge is disabled)

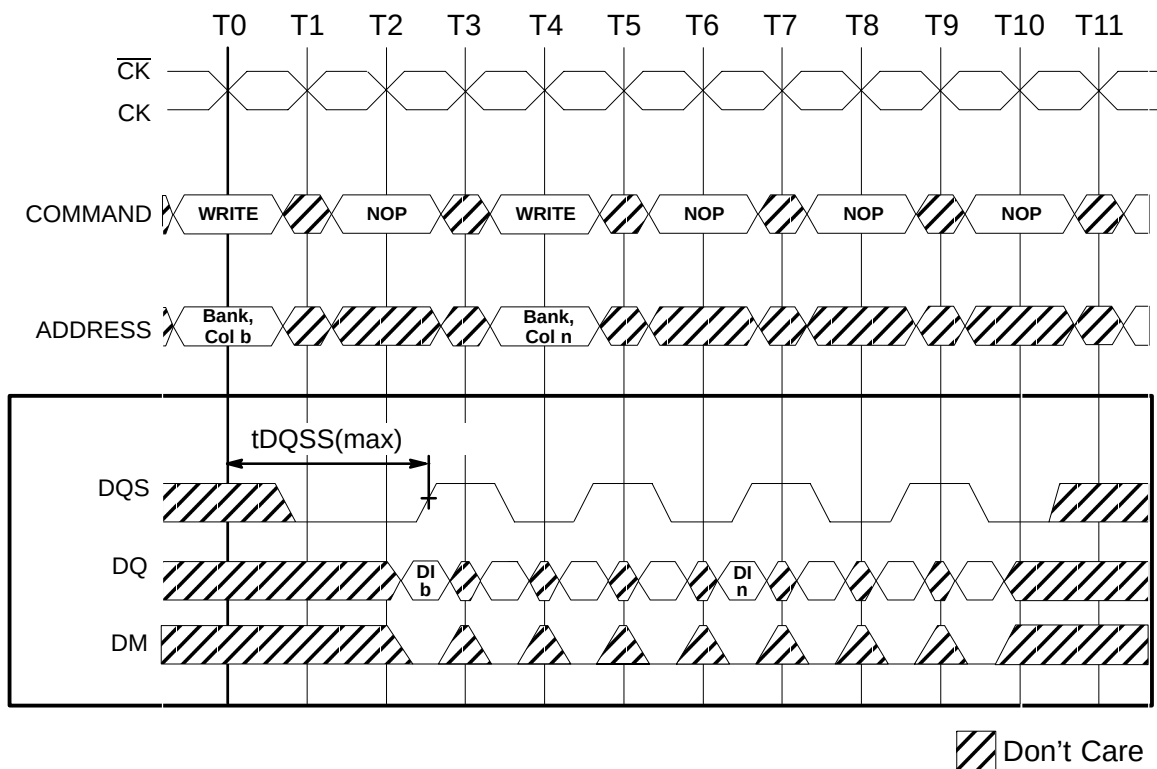
Example is for a x4 or x8 device where only one Data Mask and one

Data Strobe are used. For a X16, UDM and LDM would be required, as

well as UDQS and LDQS.

Don't Care

Figure 21
WRITE BURST – Nom., Min., and Max t_{DQSS}



DI b, etc. = Data In for column b, etc.

Three subsequent elements of Data In are applied in the programmed order following DI b

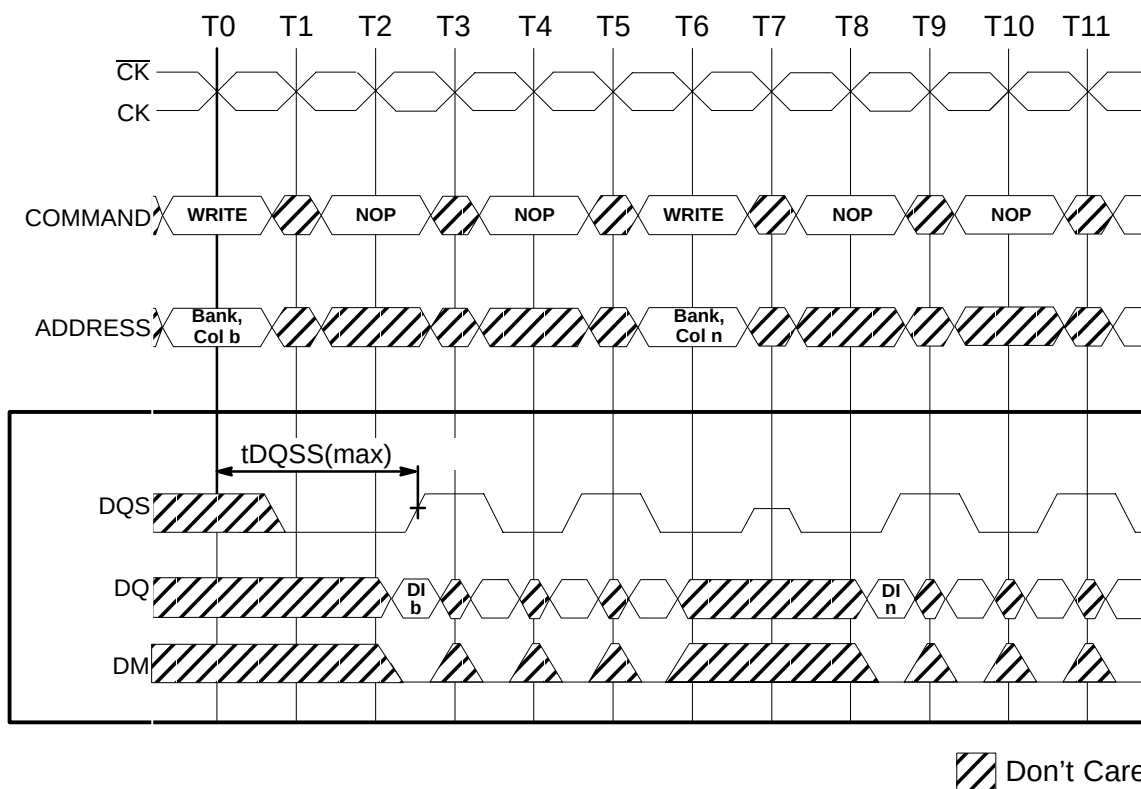
Three subsequent elements of Data In are applied in the programmed order following DI n

Noninterrupted bursts of 4 are shown

Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.

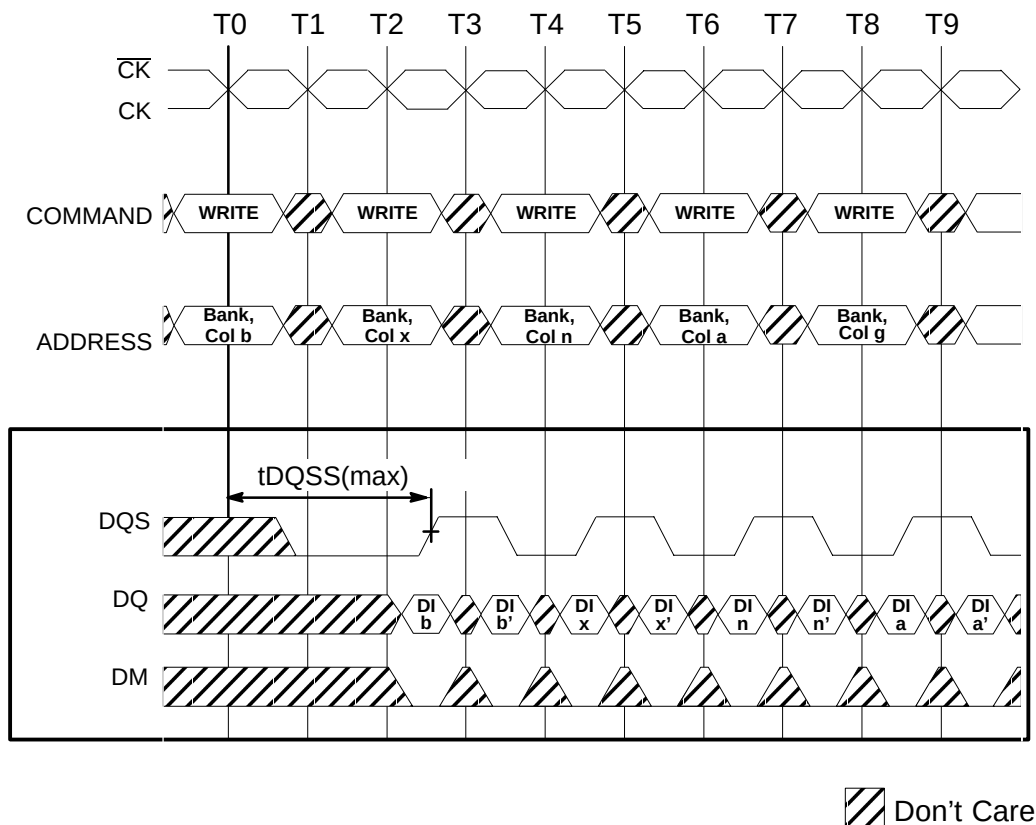
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 22
WRITE TO WRITE – Max tDQSS



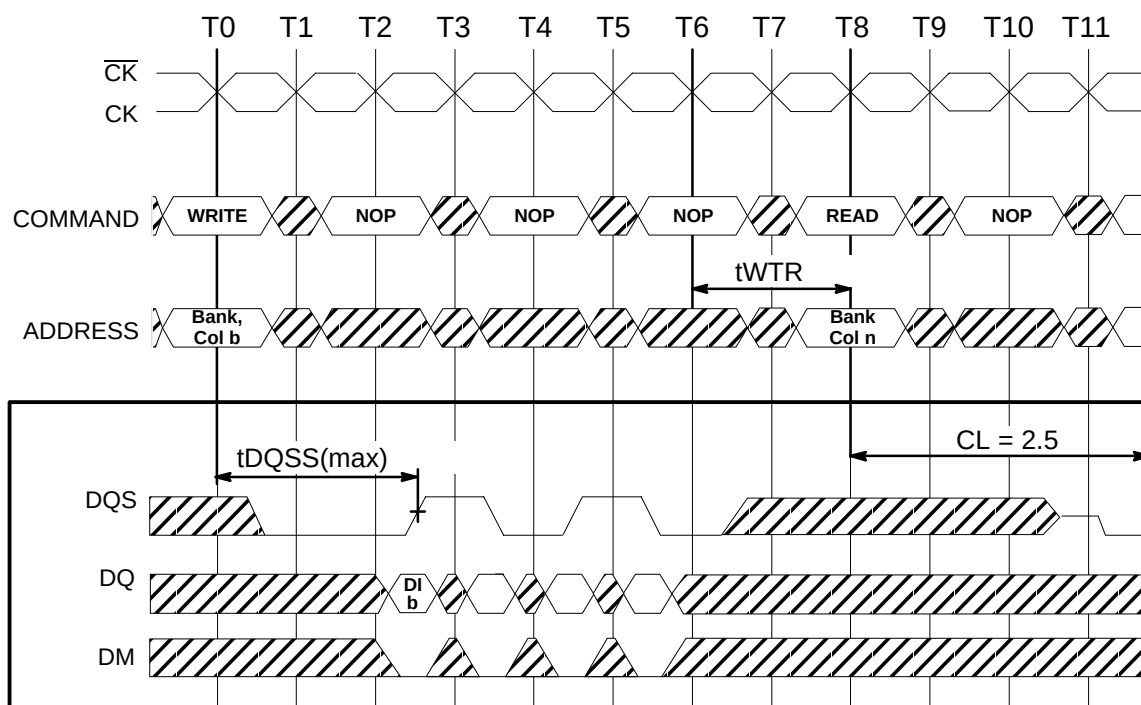
DI b, etc. :: Data In for column b, etc.
 Three subsequent elements of Data In are applied in the programmed order following DI b
 Three subsequent elements of Data In are applied in the programmed order following DI n
 Noninterrupted bursts of 4 are shown
 Each WRITE command may be to any bank and may be to the same or different devices
 Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
 For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 23
WRITE TO WRITE – Max tDQSS, NON CONSECUTIVE



DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order.
Programmed Burst Length = 2, 4, or 8 in cases shown.
If burst of 4 or 8, the burst would be truncated.
Each WRITE command may be to any bank and may be to the same or different devices.
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 24
RANDOM WRITE CYCLES – Max tDQSS



Don't Care

DI b = Data In for column b

Three subsequent elements of Data In are applied in the programmed order following DI b

A non-interrupted burst of 4 is shown

tWTR is referenced from the first positive CK edge after the last Data In pair

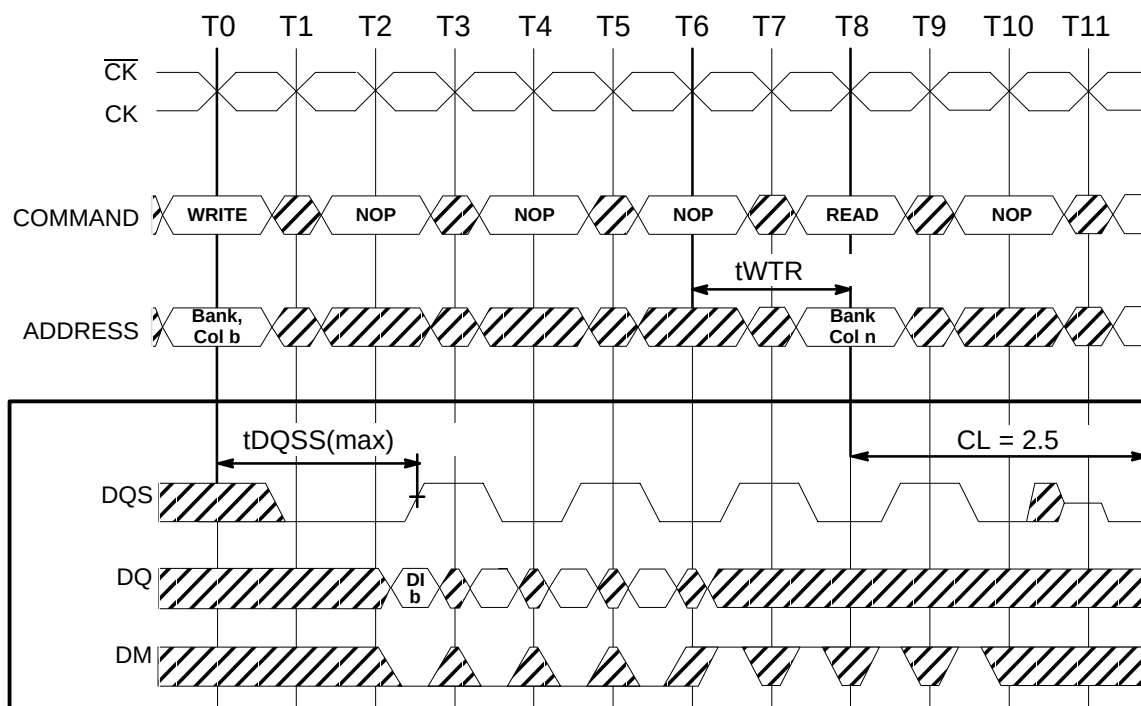
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same device but not necessarily to the same bank

Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 25
WRITE TO READ – Max tDQSS, NON-INTERRUPTING



 Don't Care

DI b = Data In for column b

An interrupted burst of 8 is shown, 4 data elements are written

Three subsequent elements of Data In are applied in the programmed order following DI b

tWTR is referenced from the first positive CK edge after the last Data In pair

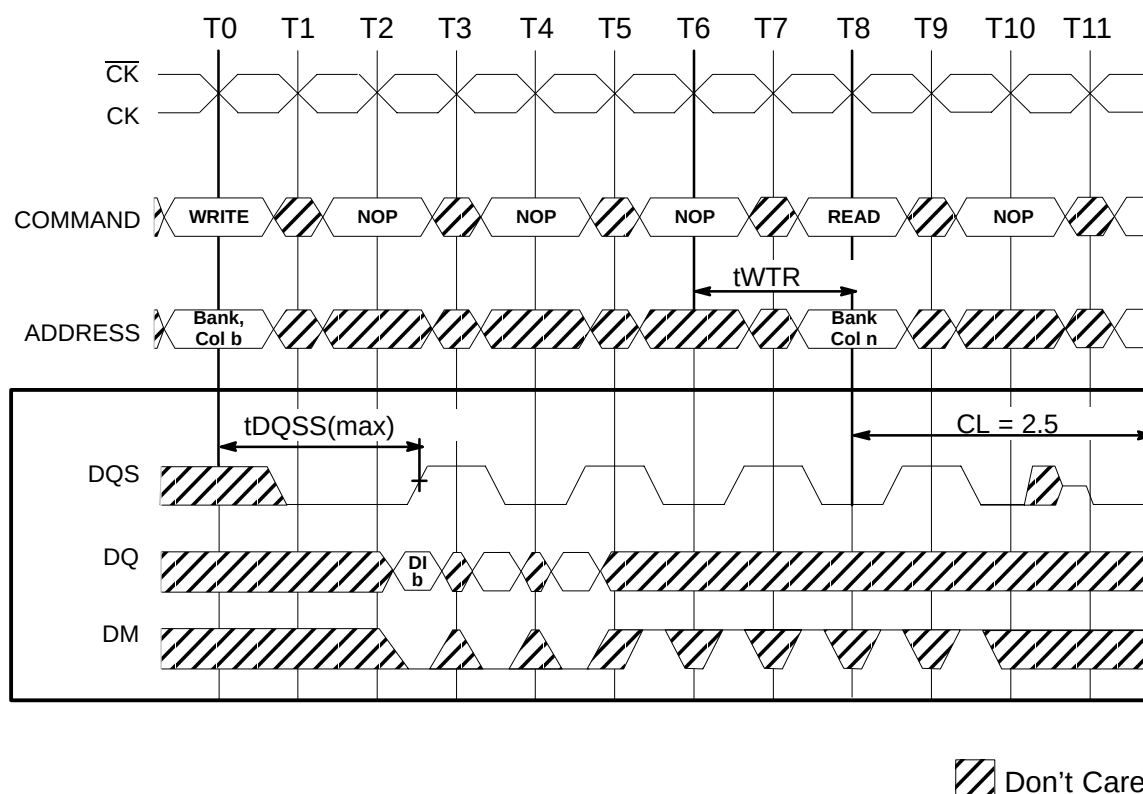
tWTR = 2tCK for optional CL = 1.5 (otherwise tWTR = 1tCK)

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same device but not necessarily to the same bank

Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 26
WRITE TO READ – Max tDQSS, INTERRUPTING



DI b = Data In for column b

An interrupted burst of 8 is shown, 3 data elements are written

Two subsequent elements of Data In are applied in the programmed order following DI b
 t_{WTR} is referenced from the first positive CK edge after the last Data In pair (not the last desired Data In element)

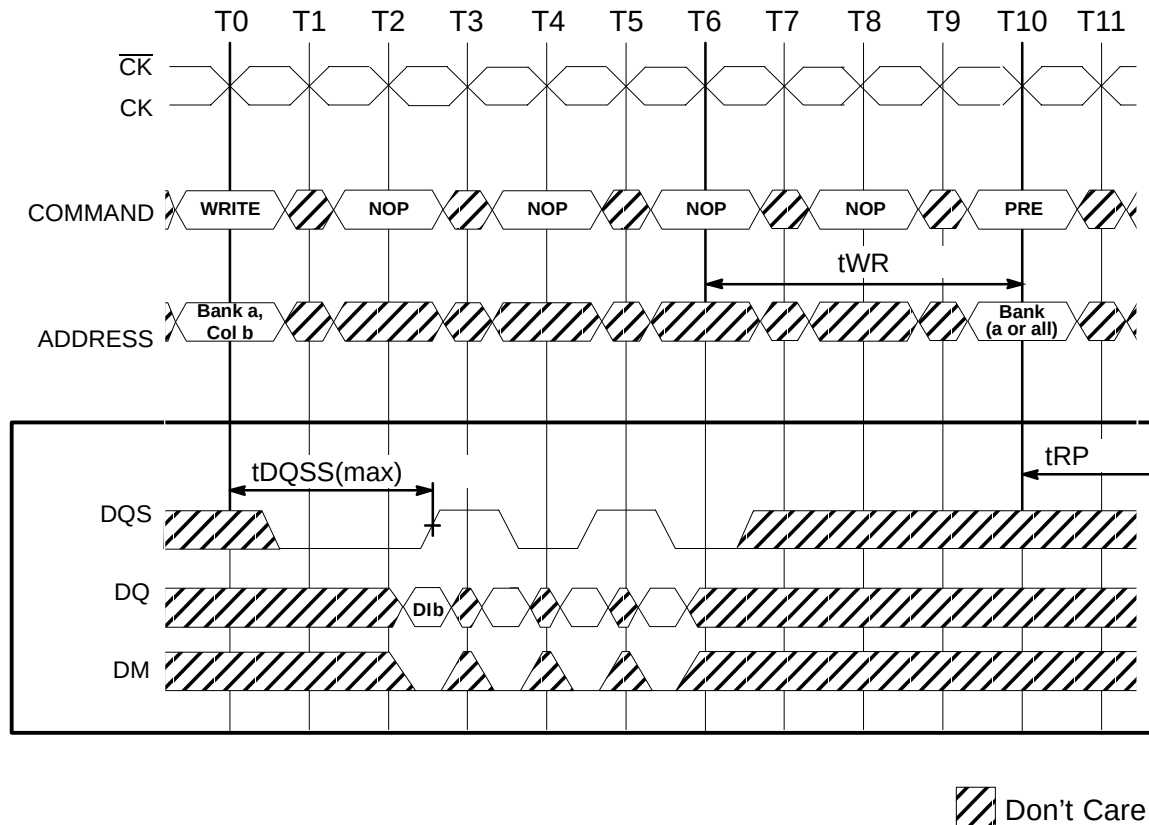
$t_{WTR} = 2t_{CK}$ for optional CL = 1.5 (otherwise $t_{WTR} = 1t_{CK}$)

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Example is for x4 or x8 devices where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

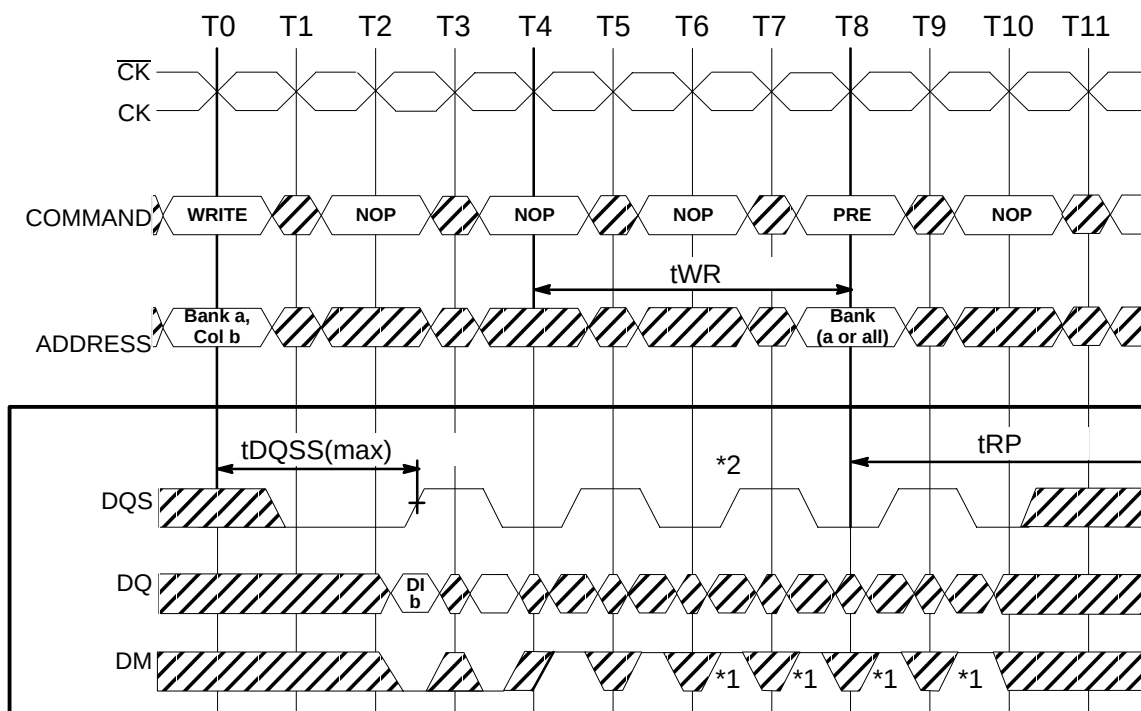
The READ and WRITE commands are to the same device but not necessarily to the same bank.

Figure 27
WRITE TO READ – Max t_{DQSS} , ODD NUMBER OF DATA, INTERRUPTING



DI b = Data In for column b
 Three subsequent elements of Data In are applied in the programmed order following DI b
 A non-interrupted burst of 4 is shown
 tWR is referenced from the first positive CK edge after the last Data In pair
 A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
 Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used.
 For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 28
WRITE TO PRECHARGE – Max tDQSS, NON-INTERRUPTING



DI b = Data In for column b

Don't Care

An interrupted burst of 4 or 8 is shown, 2 data elements are written

tWR is referenced from the first positive CK edge after the last desired Data In pair

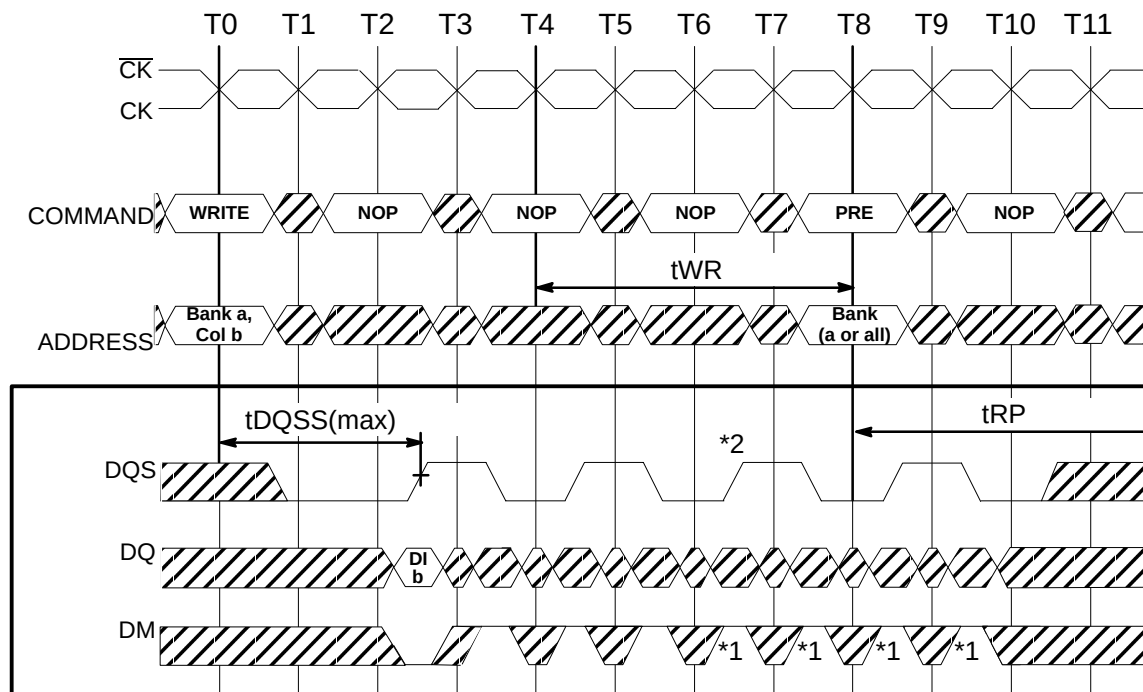
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

*1 = can be don't care for programmed burst length of 4

*2 = for programmed burst length of 4, DQS becomes don't care at this point

Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 29
WRITE TO PRECHARGE – Max tDQSS, INTERRUPTING



DI b = Data In for column b

 Don't Care

An interrupted burst of 4 or 8 is shown, 1 data element is written

tWR is referenced from the first positive CK edge after the last desired Data In pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

*1 = can be don't care for programmed burst length of 4

*2 = for programmed burst length of 4, DQS becomes don't care at this point

Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 30
WRITE TO PRECHARGE – Max tDQSS,
ODD NUMBER OF DATA, INTERRUPTING

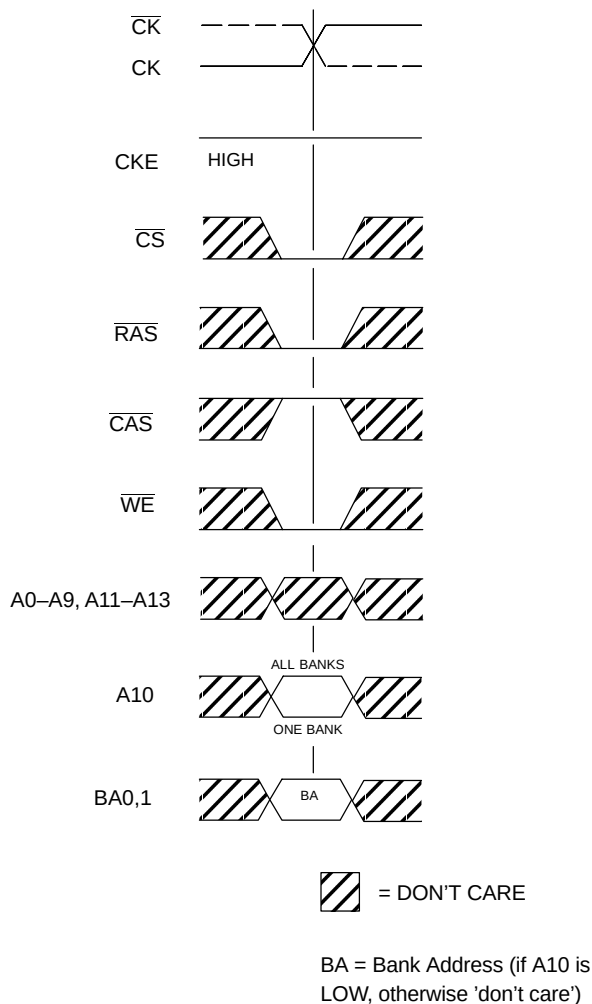


Figure 31
PRECHARGE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down is entered when CKE is registered low (no accesses can be in progress and Table 2 criteria must be met). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL-disabled power-down mode.

In power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care".

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

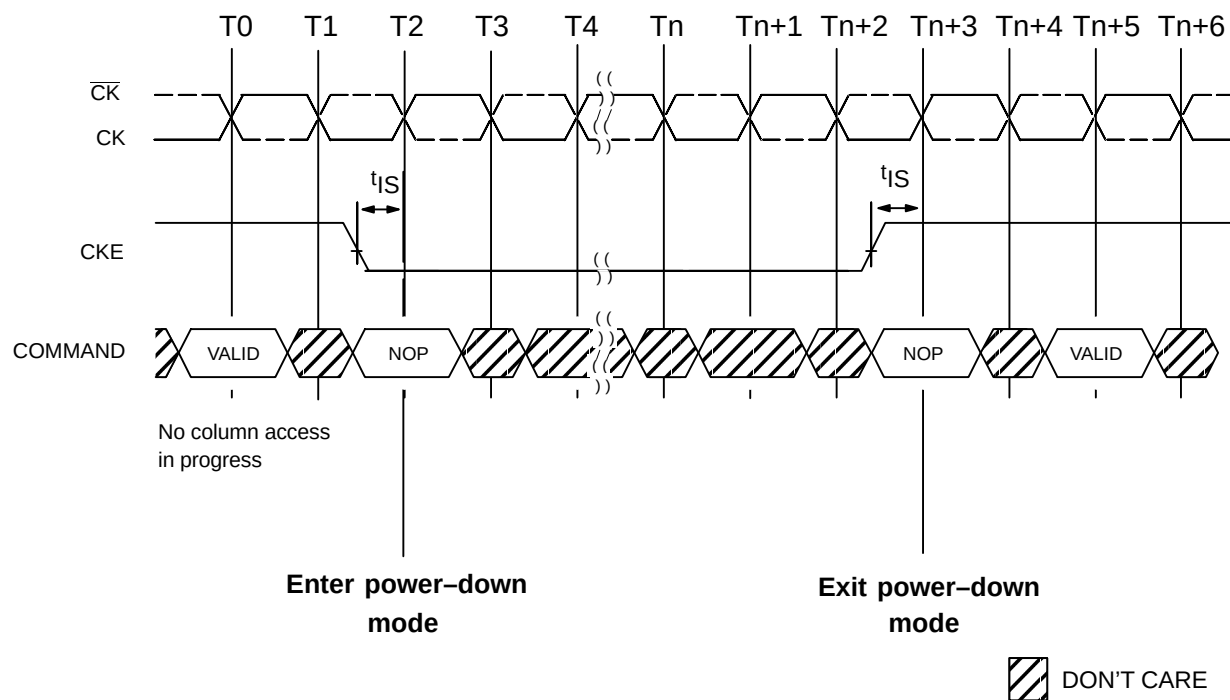


Figure 32
POWER-DOWN

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vdd Supply (For devices with nominal Vdd of 3.3 V)
Relative to Vss: -1 V to +4.6 V
Voltage on Vdd Supply (For devices with nominal Vdd of 2.5 V)
Relative to Vss: -1 V to +3.6 V
Voltage on VddQ Supply Relative to Vss: -1 V to +3.6 V
Voltage on Inputs Relative to Vss: -1 V to +3.6 V
Voltage on I/O Pins Relative to Vss: -0.5 V to VddQ+0.5 V

Operating Temperature, TA (ambient) 0 °C to +70 °C
Storage Temperature (plastic) -55 °C to +150 °C
Power Dissipation 1 W
Short Circuit Output Current 50 mA
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: CAPACITANCE

PARAMETER	PACKAGE	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CK, $\overline{\text{CK}}$	TSOP	Ci1	2.0	3.0	pF	a,d
	BGA		1.5	2.5		a,d
Delta Input Capacitance: CK, $\overline{\text{CK}}$	TSOP	Cdi1	—	0.25	pF	a,d
	BGA		—	0.25		a,d
Input Capacitance: All other input-only pins	TSOP	Ci2	2	3	pF	a,d
	BGA		1.5	2.5		a,d
Delta Input Capacitance: All other input-only pins	TSOP	Cdi2	—	0.5	pF	a,d
	BGA		—	0.5		a,d
Input/Output Capacitance: DQ, DQS, DM	TSOP	Cio	4.0	5.0	pF	a,b,c,d
	BGA		3.5	4.5		a,b,c,d
Delta Input/Output Capacitance: DQ, DQS, DM	TSOP	Cdio	—	0.5	pF	a,b,c,d
	BGA		—	0.5		a,b,c,d

- a) These values are guaranteed by design and are tested on a sample basis only.
b) Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
c) Unused pins are tied to ground.
d) This parameter is sampled. VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V, f = 100 MHz, tA = 25 °C, Vout(dc) = VDDQ/2, Vout(peak to peak) = 0.2 V. DM inputs are grouped with I/O pins – reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
e) The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25 V to 1.0 V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

TABLE 6: ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–6, These characteristics are for DDR SDRAM only and obey SSTL 2 class II standard.)
(0 °C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	7
I/O Termination Voltage (system)	VTT	VREF-0.04	VREF+0.04	V	8
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.15	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF-0.15	V	
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	VIN(DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	9
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	—	e
INPUT LEAKAGE CURRENT, Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	IL	-2	2	μA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	5	μA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	IOH IOL	-16.2 16.2		mA mA	

TABLE 7: AC OPERATING CONDITIONS

(Notes: 1–6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(ac)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(ac)		VREF – 0.31	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	VID(ac)	0.7	VDDQ + 0.6	V	9
Input Crossing Point Voltage, CK and $\overline{\text{CK}}$ inputs	VIX(ac)	0.5*VDDQ–0.2	0.5*VDDQ+0.2	V	10

TABLE 8: IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

This table is provided for the users of this Standard so that suppliers use a common format for parameter definitions of their individual IDD specifications. Values will be specific to each supplier.

Conditions	Symbol	Typ	Max
Operating current for one bank active-precharge; $t_{RC} = t_{RC}(\text{min})$; $t_{CK} = 10$ ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; $\overline{\text{CS}} = \text{high}$ between valid commands.	IDD0	-	-
Operating current for one bank operation; one bank open, BL = 4, reads - Refer to the following page for detailed test conditions: $\overline{\text{CS}} = \text{high}$ between valid commands.	IDD1	-	-
Precharge power-down standby current; all banks idle; power-down mode; $\text{CKE} \leq V_{IL}(\text{max})$; $t_{CK} = 10$ ns for DDR200, 7.5 ns for DDR266A, DDR266B, 6 ns for DDR333; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2P	-	-
Precharge floating standby current; $\overline{\text{CS}} \geq V_{IH}(\text{min})$; all banks idle; $\text{CKE} \geq V_{IH}(\text{min})$; $t_{CK} = 10$ ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2F	-	-
Precharge quiet standby current; $\overline{\text{CS}} \geq V_{IH}(\text{min})$; all banks idle; $\text{CKE} \geq V_{IH}(\text{min})$; $t_{CK} = 10$ ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; address and other control inputs stable at $\geq V_{IH}(\text{min})$ or $\leq V_{IL}(\text{max})$; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2Q	-	-
Active power-down standby current ; one bank active; power-down mode; $\text{CKE} \leq V_{IL}(\text{max})$; $t_{CK} = 10$ ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD3P	-	-
Active standby current; $\overline{\text{CS}} \geq V_{IH}(\text{min})$; $\text{CKE} \geq V_{IH}(\text{min})$; one bank active; $t_{RC} = t_{RAS}(\text{max})$; $t_{CK} = 10$ ns for DDR200, 7.5 ns for DDR266, 6 ns for DDR333; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	-	-
Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; CL = 2 at $t_{CK} = 10$ ns for DDR200, CL = 2 at $t_{CK} = 7.5$ ns for DDR266A, CL = 2.5 at $t_{CK} = 7.5$ ns for DDR266B, 6 ns for DDR333; 50% of data changing on every transfer; $I_{OUT} = 0$ mA	IDD4R	-	-
Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; CL = 2 at $t_{CK} = 10$ ns for DDR200, CL = 2 at $t_{CK} = 7.5$ ns for DDR266A, CL = 2.5 at $t_{CK} = 7.5$ ns for DDR266B, 6 ns for DDR333; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	IDD4W	-	-
Auto refresh current; $t_{RC} = t_{RFC}(\text{min})$ which is $8 * t_{CK}$ for DDR200 at $t_{CK} = 10$ ns, $10 * t_{CK}$ for DDR266 at $t_{CK} = 7.5$ ns; $12 * t_{CK}$ for DDR333 at $t_{CK} = 6$ ns;	IDD5	-	-
Self refresh current; $\text{CKE} \leq 0.2$ V; external clock on; $t_{CK} = 10$ ns for DDR200, $t_{CK} = 7.5$ ns for DDR266, 6 ns for DDR333	IDD6	-	-
Operating current for four bank operation; four bank interleaving with BL = 4 - Refer to the following page for detailed test condition	IDD7	-	-
Typical case : $V_{DD} = 2.5$ V, $T = 25$ °C Worst case : $V_{DD} = 2.7$ V, $T = 10$ °C Self refresh: normal/low power respectively Measured values for all items will be averaged from repeated cycles with the above description			

Detailed test conditions for DDR SDRAM IDD1 and IDD7

Typical Case: $V_{DD} = 2.5\text{ V}$, $T = 25^\circ\text{ C}$, Worst Case: $V_{DD} = 2.7\text{ V}$, $T = 10^\circ\text{ C}$

Legend: A = Active, R = Read, RA = Read with Autoprecharge, P = Precharge, N = DESELECT

IDD1 : Operating current: One bank operation

Only one bank is accessed with $t_{RC}(\min)$, Burst Mode, Address and Control inputs change logic state once per Deselect cycle. $I_{OUT} = 0\text{ mA}$

Timing patterns

- DDR200 (100 MHz, CL = 2): $t_{CK} = 10\text{ ns}$, BL = 4, $t_{RCD} = 2 * t_{CK}$, **$t_{RC} = 7 * t_{CK}$** , $t_{RAS} = 5 * t_{CK}$
Setup: A0 N R0 N N P0 N
Read: A0 N R0 N N P0 N - repeat the same timing with random address changing
50% of data changing at every transfer
- DDR266B (133 MHz, CL = 2.5): $t_{CK} = 7.5\text{ ns}$, BL = 4, $t_{RCD} = 3 * t_{CK}$, $t_{RC} = 9 * t_{CK}$, **$t_{RAS} = 6 * t_{CK}$**
- DDR266A (133 MHz, CL = 2): $t_{CK} = 7.5\text{ ns}$, BL = 4, $t_{RCD} = 3 * t_{CK}$, $t_{RC} = 9 * t_{CK}$, **$t_{RAS} = 6 * t_{CK}$**
Setup: A0 N N R0 N N P0 N N
Read: A0 N N R0 N N P0 N N - repeat the same timing with random address changing
50% of data changing at every transfer
- DDR333B (167 MHz, CL = 2.5): $t_{CK} = 6\text{ ns}$, BL = 4, $t_{RCD} = 3 * t_{CK}$, $t_{RC} = 10 * t_{CK}$, $t_{RAS} = 7 * t_{CK}$
Setup: A0 N N R0 N N N P0 N N
Read: A0 N N R0 N N N P0 N N - repeat the same timing with random address changing
50% of data changing at every transfer

IDD7 : Operating current: Four bank operation

Four banks are being interleaved with $t_{RC}(\min)$, Burst Mode, Address and Control inputs on Deselect edge are not changing. $I_{OUT} = 0\text{ mA}$

Timing patterns

- DDR200 (100 MHz, CL = 2): $t_{CK} = 10\text{ ns}$, BL = 4, $t_{RRD} = 2 * t_{CK}$, $t_{RCD} = 3 * t_{CK}$, $t_{RAS} = 5 * t_{CK}$
Setup: A0 N A1 RA0 A2 RA1 A3 RA2
Read: A0 RA3 A1 RA0 A2 RA1 A3 RA2 - repeat the same timing with random address changing
50% of data changing at every transfer
- DDR266B (133 MHz, CL = 2.5): $t_{CK} = 7.5\text{ ns}$, BL = 4, $t_{RRD} = 2 * t_{CK}$, $t_{RCD} = 3 * t_{CK}$, $t_{RAS} = 6 * t_{CK}$
- DDR266A (133 MHz, CL = 2): $t_{CK} = 7.5\text{ ns}$, BL = 4, $t_{RRD} = 2 * t_{CK}$, $t_{RCD} = 3 * t_{CK}$, $t_{RAS} = 6 * t_{CK}$
Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer
- DDR333B (167 MHz, CL = 2.5): $t_{CK} = 6\text{ ns}$, BL = 4, $t_{RRD} = 2 * t_{CK}$, $t_{RCD} = 3 * t_{CK}$, $t_{RAS} = 7 * t_{CK}$
Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing 50% of data changing at every transfer

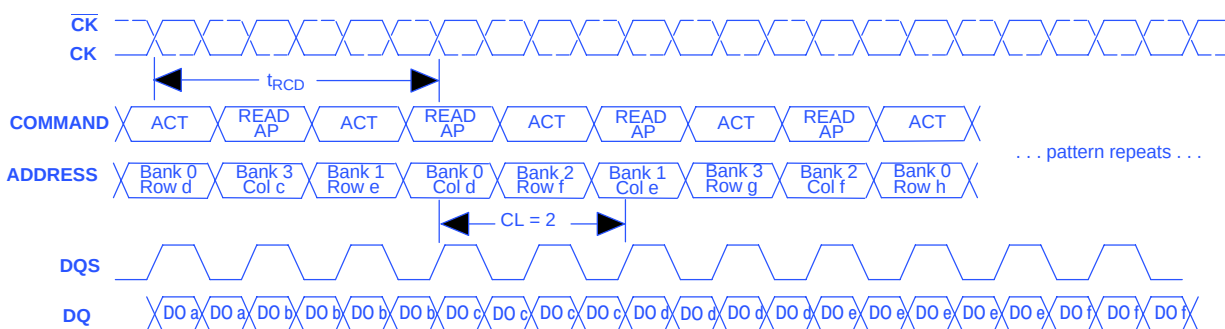


FIGURE 33: Timing waveform for IDD7 measurement at 100 MHz Ck operation

TABLE 9: ELECTRICAL CHARACTERISTICS AND AC TIMING

All specification parameters are guaranteed by the supplier, but it is not implied that this table represents a test specification.

Absolute Specifications (Notes: 1–6, 13, 14) (0°C ≤ TA ≤ 70 °C; VDDQ = +2.5 V ±0.2 V, VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

AC CHARACTERISTICS		DDR333		DDR266		DDR200		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX		
DQ output access time from CK/CK	tAC	–0.70	+0.70	–0.75	+0.75	–0.8	+0.8	ns	
DQS output access time from CK/CK	tDQSCK	–0.60	+0.60	–0.75	+0.75	–0.8	+0.8	ns	
CK high–level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low–level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	24, 25
Clock cycle time CL = 2.5 CL = 2	tCK	6	12	7.5	12	10	12	ns	30
	tCK	7.5	12	7.5	12	10	12	ns	30
DQ and DM input hold time	tDH	0.45		0.5		0.6		ns	j, k
DQ and DM input setup time	tDS	0.45		0.5		0.6		ns	j, k
Control & Address input pulse width (for each input)	tIPW	2.2		2.2		2.5		ns	22
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		2		ns	22
DQ & DQS high–impedance time from CK/CK	tHZ		+0.70		+0.75		+0.8	ns	15
DQ & DQS low–impedance time from CK/CK	tLZ	–0.70	+0.70	–0.75	+0.75	–0.8	+0.8	ns	15
DQS–DQ Skew (for DQS and associated DQ signals)	tDQSQ		+0.45		+0.5		+0.6	ns	26
	tDQSQ		+0.4		+0.5		+0.6	ns	26
DQ/DQS output hold time from DQS	tQH	tHP–tQHS		tHP–tQHS		tHP–tQHS		ns.	25
Data Hold Skew Factor (for DQS and associated DQ Signals)	tQHS		+0.55		+0.75		+1.0	ns	25
	tQHS		+0.5		+0.75		+1.0	ns	25
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		0.2		tCK	
MODE REGISTER SET command cycle time	tMRD	2		2		2		tCK	
Write preamble setup time	tWPRES	0		0		0		ns	17
Write postamble	tWPST	0.40	0.60	0.4	0.6	0.40	0.60	tCK	16
Write preamble	tWPRE	0.25		0.25		0.25		tCK	
Address and Control input hold time (fast slew rate)	tIH	0.75		0.9		1.1		ns	i, 19, 21–23
Address and Control input setup time (fast slew rate)	tIS	0.75		0.9		1.1		ns	i, 19, 21–23
Address and Control input hold time (slow slew rate)	tIH	0.80		1.0		1.1		ns	i, 20–23
Address and Control input setup time (slow slew rate)	tIS	0.80		1.0		1.1		ns	i, 20–23
Read preamble CL=2.5 CL = 2.0 CL = 1.5	tRPRE	0.9 0.9 N/A	1.1 1.1 N/A	0.9 0.9 N/A	1.1 1.1 N/A	0.9 0.9 –	1.1 1.1 1.1	tCK tCK tCK	28 28 28
	tRPRE		N/A		N/A		1.5	ns	28
	tRPRE	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE to PRECHARGE command	tRAS	42	70,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	60		65		70		ns	
Auto Refresh to Active/Auto Refresh command period 64Mb, 512Mb 1Gb	tRFC	72		75		80		ns	
	tRFC	120		120		120		ns	
ACTIVE to READ or WRITE delay	tRCD	18		20		20		ns	
PRECHARGE command period	tRP	18		20		20		ns	
Active to Autoprecharge Delay	tRAP	tRCD or tRASmin		tRCD or tRASmin		tRCD or tRASmin		ns	
ACTIVE bank A to ACTIVE bank B command	tRRD	12		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Auto Precharge write recovery + precharge time	tDAL	—		—		—		tCK	27
Internal Write to Read Command Delay CL=2.5 CL=2.0 CL=1.5	tWTR	1 1 N/A		1 1 N/A		1 1 2		tCK tCK tCK	
	tWTR	75		75		80		ns	29
	tWTR	126		127.5		130		ns	
Exit self refresh to non–READ command 64Mb to 512 Mb 1Gb	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval 64Mb, 128Mb 256Mb, 1Gb	tREFI		15.6		15.6		15.6	μs	18
	tREFI		7.8		7.8		7.8	μs	18

TABLE 10: AC TIMING VARIATIONS FOR DDR333, DDR266, & DDR200

This table defines several parameters that differ from those given in Table 9 to establish A & B variants of the primary speed sort specifications for DDR200, DDR266, & DDR333.

	DDR333B		DDR266A		DDR266B		DDR200		DDR200B		Units
Parameter	min	max	min	max	min	max	min	max	min	max	ns
tAC	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
tDQSCK	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	-0.8	0.8	ns
tCK CL = 2.5	6	12	7.5	12	7.5	12	10	12	10	12	ns
tCK CL = 2.0	7.5	12	7.5	12	10	12	10	12	10	12	ns
tRRD	12		15		15		15		20		ns
tWR	15		15		15		15		20		ns

Component Notes

- All voltages referenced to Vss.
- Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
- Figure 34 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

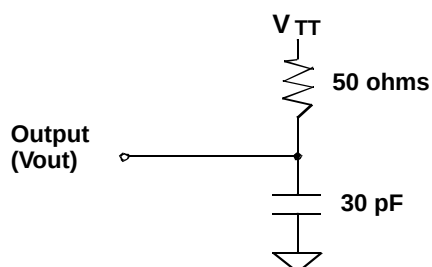


Figure 34: Timing Reference Load

- AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/ $\overline{\text{CK}}$), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
- The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
- Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, $\text{CKE} \leq 0.2\text{VDDQ}$ is recognized as LOW.
- VREF is expected to be equal to $0.5 \cdot \text{VDDQ}$ of the transmitting device, and to track variations in the dc level of the same. Peak-to-peak noise on VREF may not exceed $\pm 2\%$ of the dc value.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF.
- VID is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.
- The value of VIX is expected to equal $0.5 \cdot \text{VDDQ}$ of the transmitting device and must track variations in the dc level of the same.
- Enables on-chip refresh and address counters.
- IDD specifications are tested after the device is properly initialized.
- The CK/ $\overline{\text{CK}}$ input reference level (for timing referenced to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross; the input reference level for signals other than CK/ $\overline{\text{CK}}$, is VREF.
- The output timing reference voltage level is VTT.
- tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
- The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turn-around) will degrade accordingly.

17. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
18. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
19. For command/address input slew rate ≥ 1.0 V/ns
20. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
21. For CK & $\overline{\text{CK}}$ slew rate ≥ 1.0 V/ns
22. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
23. Slew Rate is measured between VOH(ac) and VOL(ac).
24. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
25. tQH = tHP – tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
26. **tDQSQ**
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
27. **tDAL = (tWR/tCK) + (tRP/tCK)**
For each of the terms above, if not already an integer, round to the next highest integer.
Example: For DDR266B at CL=2.5 and tCK=7.5 ns
tDAL = ((15 ns / 7.5 ns) + (20 ns / 7.5 ns)) clocks
= ((2) + (3)) clocks
= 5 clocks
28. Optional CAS Latency, 1.5, is only defined for DDR200 speed grade
29. In all circumstances, tXSNR can be satisfied using
tXSNR = tRFCmin + 1*tCK
30. The only time that the clock frequency is allowed to change is during self-refresh mode.

SYSTEM CHARACTERISTICS for DDR SDRAMS

The following specification parameters are required in systems using DDR333, DDR266 & DDR200 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

Table 11: Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR333		DDR266		DDR200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	0.5	4.0	V/ns	a, m

Table 12: Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	Δt_{IS}	Δt_{IH}	UNITS	NOTES
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 13: Input/Output Setup & Hold Time Derating for Slew Rate

I/O Input Slew Rate	Δt_{DS}	Δt_{DH}	UNITS	NOTES
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 14: Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	Δt_{DS}	Δt_{DH}	UNITS	NOTES
± 0.0 ns/V	0	0	ps	j
± 0.25 ns/V	+50	+50	ps	j
± 0.5 ns/V	+100	+100	ps	j

Table 15: Output Slew Rate Characteristics (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 – 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown Slew Rate	1.2 – 2.5	1.0	4.5	b,c,d,f,g,h

Table 16: Output Slew Rate Characteristics (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	NOTES
Pullup Slew Rate	1.2 – 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown Slew Rate	1.2 – 2.5	0.7	5.0	b,c,d,f,g,h

Table 17: Output Slew Rate Matching Ratio Characteristics

Slew Rate Characteristic	DDR266A		DDR266B		DDR200		
PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Output Slew Rate Matching Ratio (Pullup to Pulldown)	—	—	—	—	0.71	1.4	e,m

Table 18: AC Overshoot/Undershoot Specification for Address and Control Pins
This specification is intended for devices with no clamp protection and is guaranteed by design

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot (See Figure 35):	TBD	1.5 V
Maximum peak amplitude allowed for undershoot (See Figure 35):	TBD	1.5 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 35):	TBD	4.5 V–ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 35):	TBD	4.5 V–ns

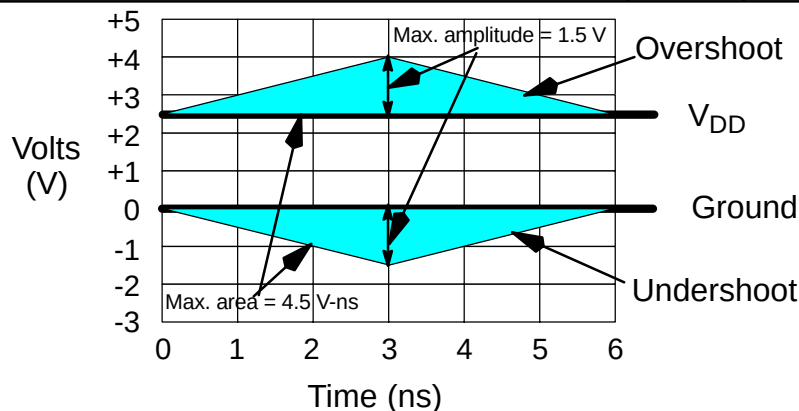


Figure 35: Address and Control AC Overshoot and Undershoot Definition

TABLE 19: Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

Parameter	Specification	
	DDR333	DDR200/266
Maximum peak amplitude allowed for overshoot (See Figure 36):	TBD	1.2 V
Maximum peak amplitude allowed for undershoot (See Figure 36):	TBD	1.2 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 36):	TBD	2.4 V–ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 36):	TBD	2.4 V–ns

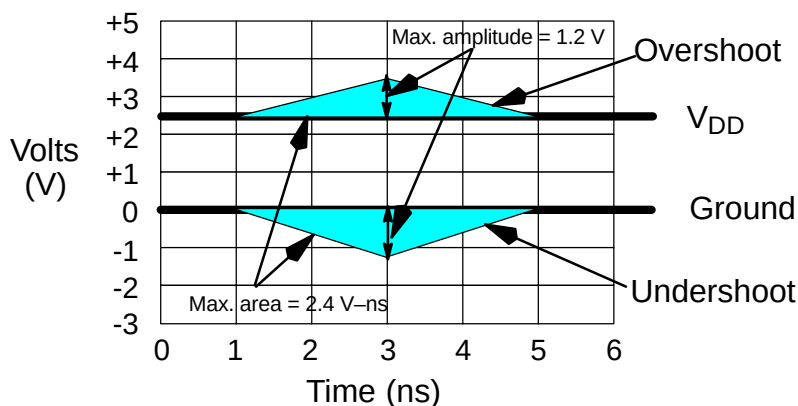


Figure 36: DQ/DM/DQS AC Overshoot and Undershoot Definition

TABLE 20. Clamp V-I Characteristics for Address, Control and Data Pins

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0.1
0.8	0.1	0.6
0.9	1.0	1.8
1.0	2.5	3.4
1.1	4.7	5.6
1.2	6.8	7.6
1.3	9.1	10.0
1.4	11.0	13.0
1.5	13.5	15.4
1.6	16.0	18.0
1.7	18.2	21.6
1.8	21.0	25.0
1.9	23.3	28.0
2.0	26.0	31.0
2.1	28.2	34.4
2.2	31.0	38.0
2.3	33.0	42.0
2.4	35.0	46.0
2.5	37.0	50.0

Power & Ground Clamp V-I Characteristics

System Notes:

- a. Pullup slew rate is characterized under the test conditions as shown in Figure 37.

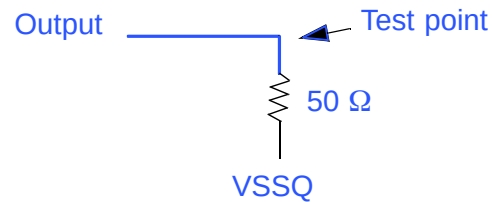


Figure 37: Pullup slew rate test load

- b. Pulldown slew rate is measured under the test conditions shown in Figure 38.

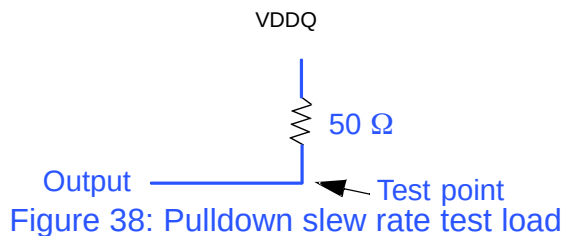


Figure 38: Pulldown slew rate test load

- c. Pullup slew rate is measured between $(VDDQ/2 - 320 \text{ mV} \pm 250 \text{ mV})$
Pulldown slew rate is measured between $(VDDQ/2 + 320 \text{ mV} \pm 250 \text{ mV})$
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew rate, DQ0 is switching
For minimum slew rate, all DQ bits are switching worst case pattern
For maximum slew rate, only one DQ is switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

- d. Evaluation conditions
Typical: 25 °C (T Ambient), VDDQ = 2.5 V, typical process
Minimum: 70 °C (T Ambient), VDDQ = 2.3 V, slow-slow process
Maximum: 0 °C (T Ambient), VDDQ = 2.7 V, fast-fast process
- e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.
- f. Verified under typical conditions for qualification purposes.
- g. TSOP11 package devices only.
- h. Only intended for operation up to 266 Mbps per pin.
- i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table 12. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
- j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 13 & 14. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as:
 $\{1/(\text{Slew Rate1})\} - \{1/(\text{slew Rate2})\}$
For example: If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise,fall rate is -0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

- k. Table 13 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC–AC slew rate and the DC–DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions.
- m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

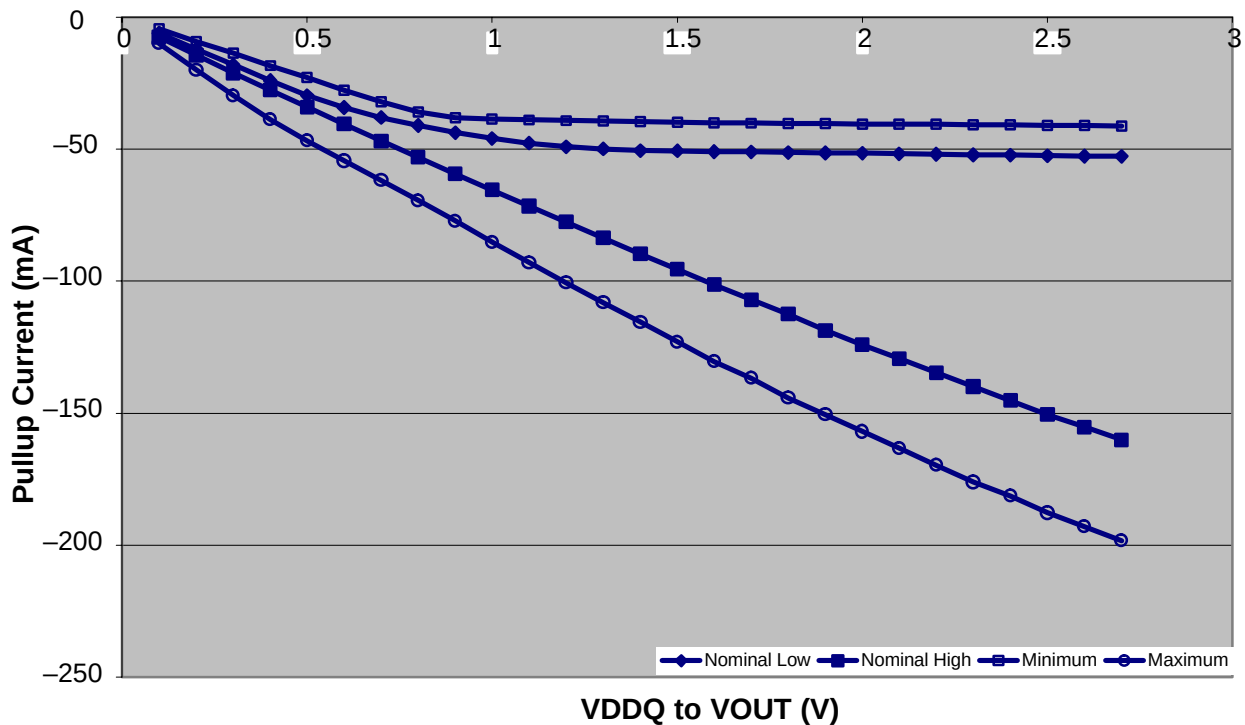


Figure 39a: Pullup characteristics for Full Strength Output Driver

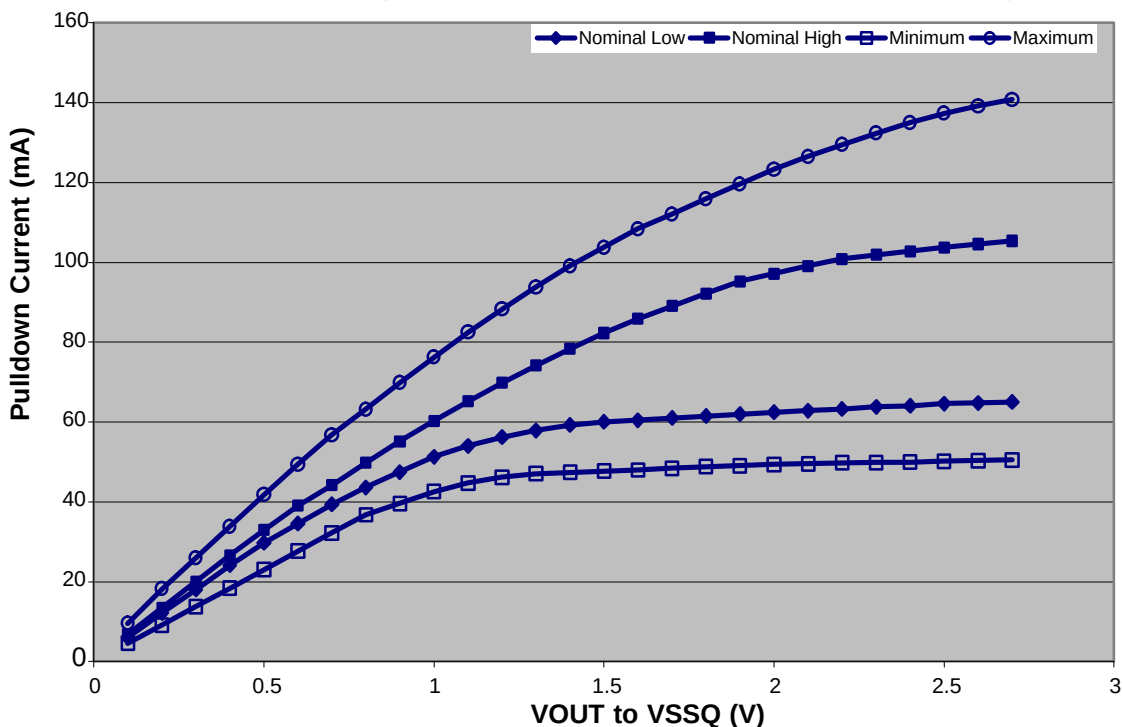


Figure 39b: Pulldown characteristics for Full Strength Output Driver

FIGURE 39: FULL STRENGTH OUTPUT DRIVER CHARACTERISTIC CURVES

TABLE 21: Full Strength Driver Characteristics

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	160.1	-41.2	-198.2

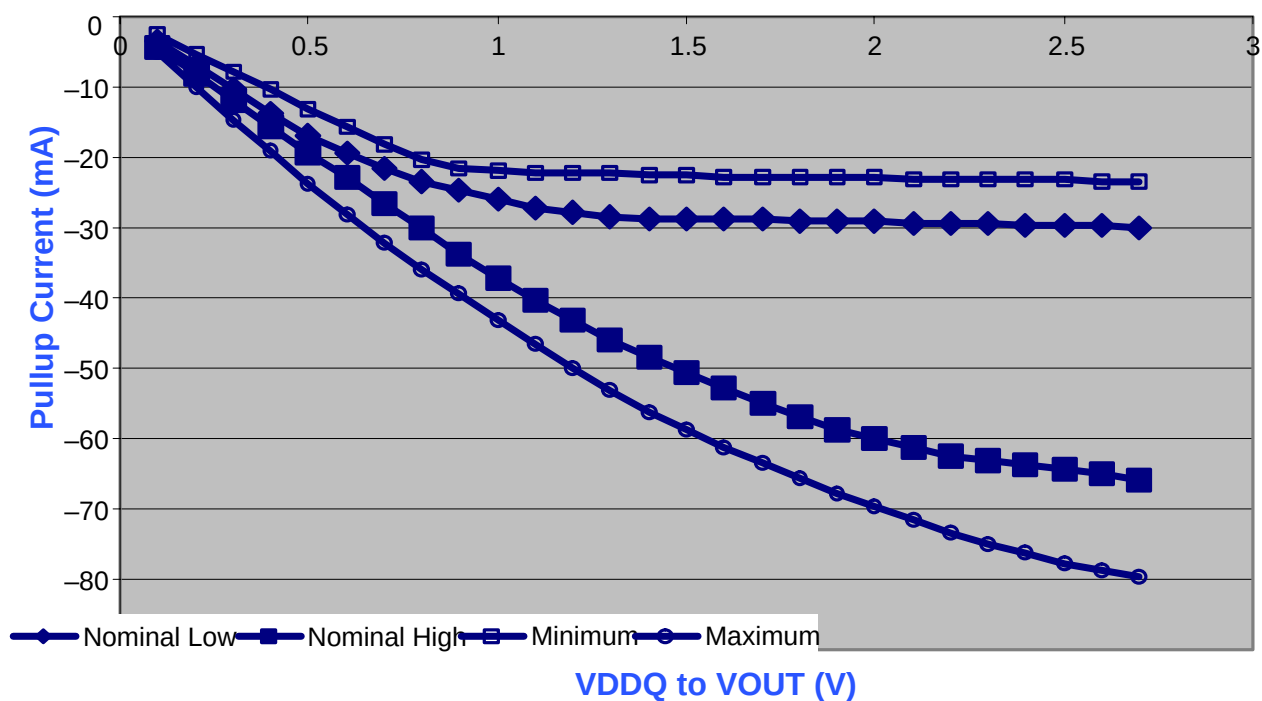


Figure 40a: Pullup Characteristics for Weak Output Driver

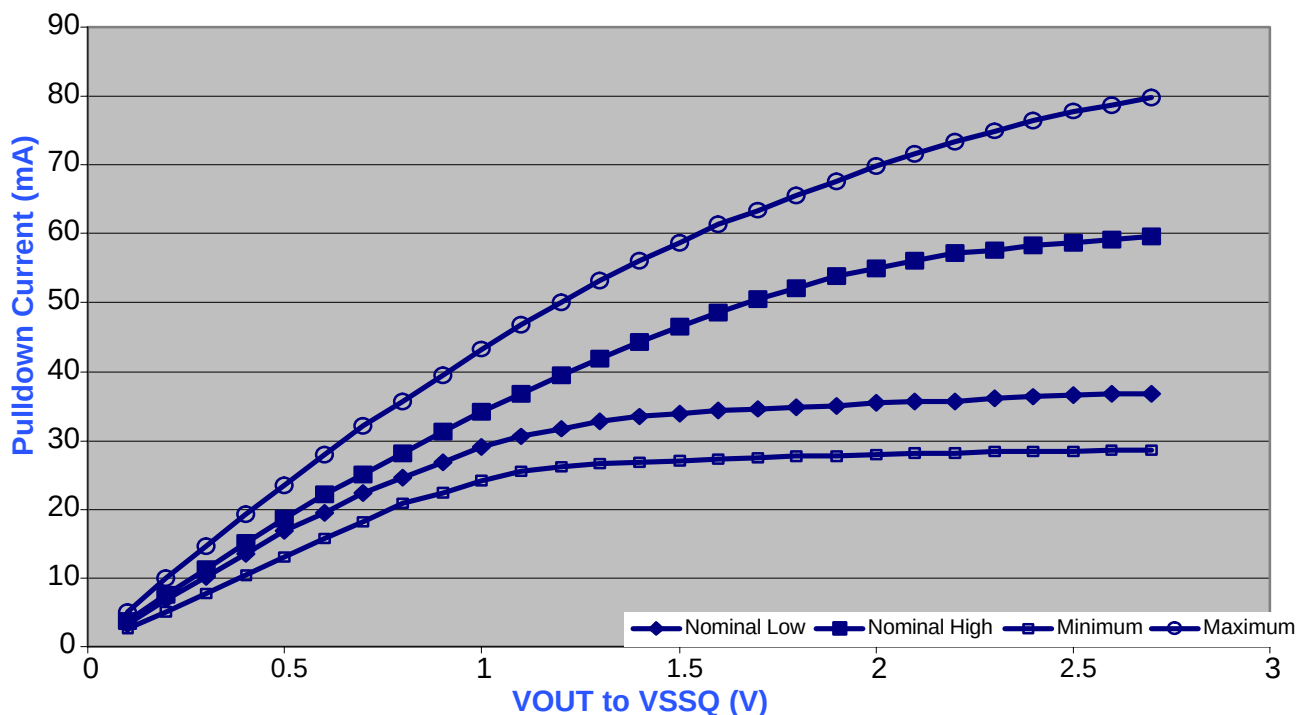


Figure 40b: Pulldown Characteristics for Weak Output Driver

FIGURE 40: WEAK OUTPUT DRIVER CHARACTERISTIC CURVES

TABLE 22: Weak Driver Characteristics

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5	-3.5	-4.3	-2.6	-5
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13	23.6	-16.9	-19.3	-13	-23.6
0.6	19.6	22.1	15.7	28	-19.4	-22.9	-15.7	-28
0.7	22.3	25	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1	29	34.1	24.1	43.2	-26	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34	46.6	27	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2	35.4	55	28	69.8	-29.2	-60	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

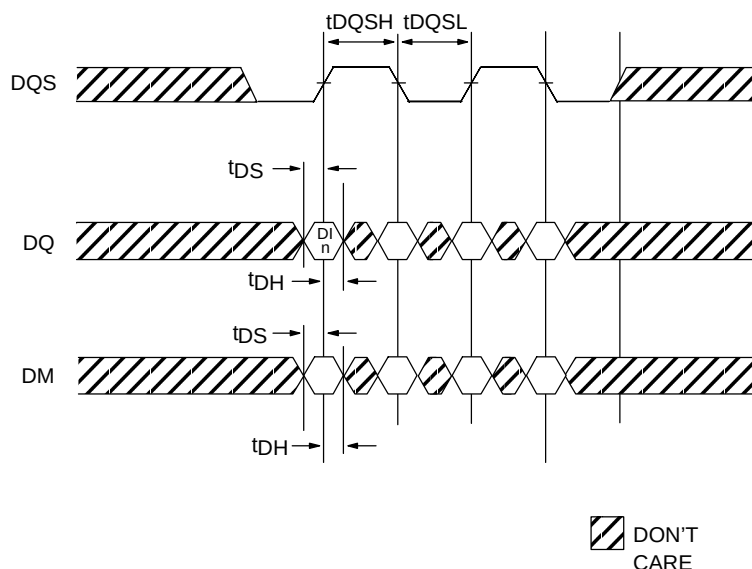
DDR SDRAM Output Driver V-I Characteristics

DDR SDRAM output driver characteristics are defined for full and half strength operation as selected by the EMRS bit A1. Figures 39 and 40 show the driver characteristics graphically, and tables 21 and 22 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

Typical	25 °C (T ambient),	VDDQ = 2.5 V,	typical process
Minimum	70 °C (T ambient),	VDDQ = 2.3 V,	slow-slow process
Maximum	0 °C (T ambient),	VDDQ = 2.7 V,	fast-fast process

Output Driver Characteristic Curves Notes:

- 1) The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V-I curve of Figures 39 and 40.
- 2) It is recommended that the "typical" IBIS V-I curve lie within the inner bounding lines of the V-I curves of Figures 39 and 40.
- 3) The full variation in the ratio of the "typical" IBIS pullup to "typical" IBIS pulldown current should be unity $\pm$ 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.



DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n

Figure 41 – DATA INPUT (WRITE) TIMING

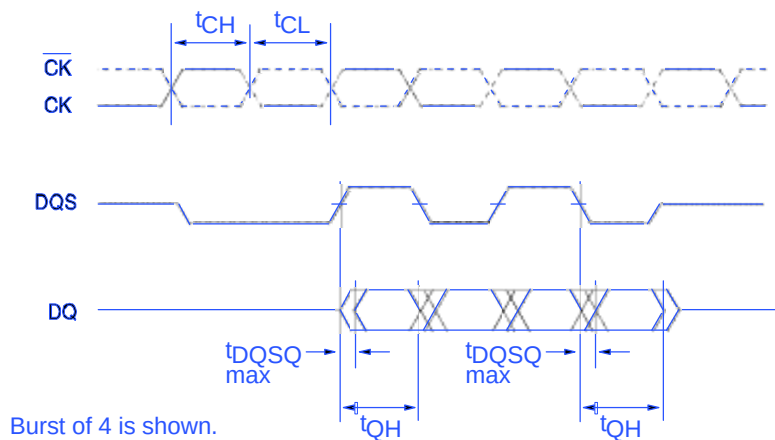
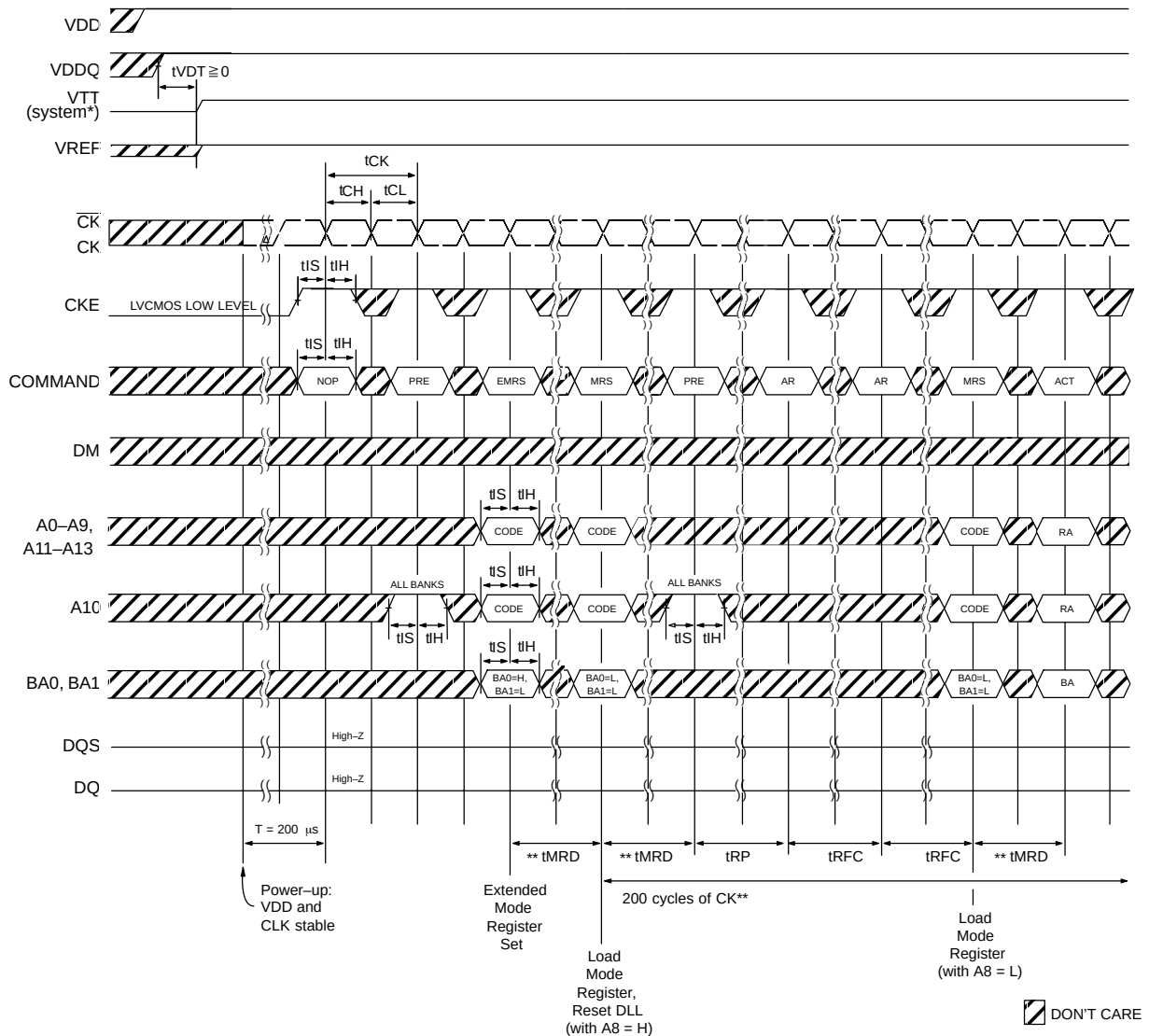
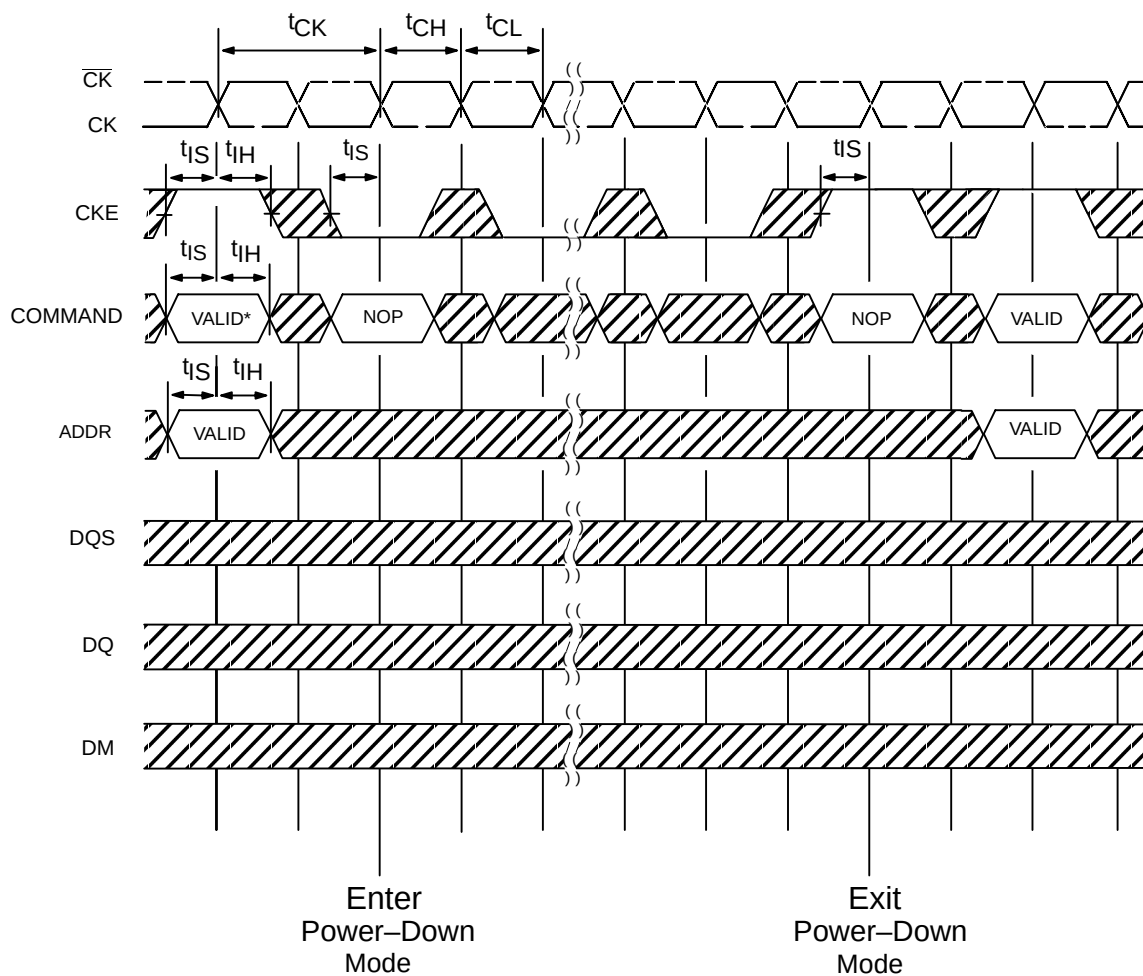


Figure 42 – DATA OUTPUT (READ) TIMING



* = VTT is not applied directly to the device, however t_{VDT} must be greater than or equal to zero to avoid device latch-up.
 ** = tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied
 The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

Figure 43 – INITIALIZE AND MODE REGISTER SETS

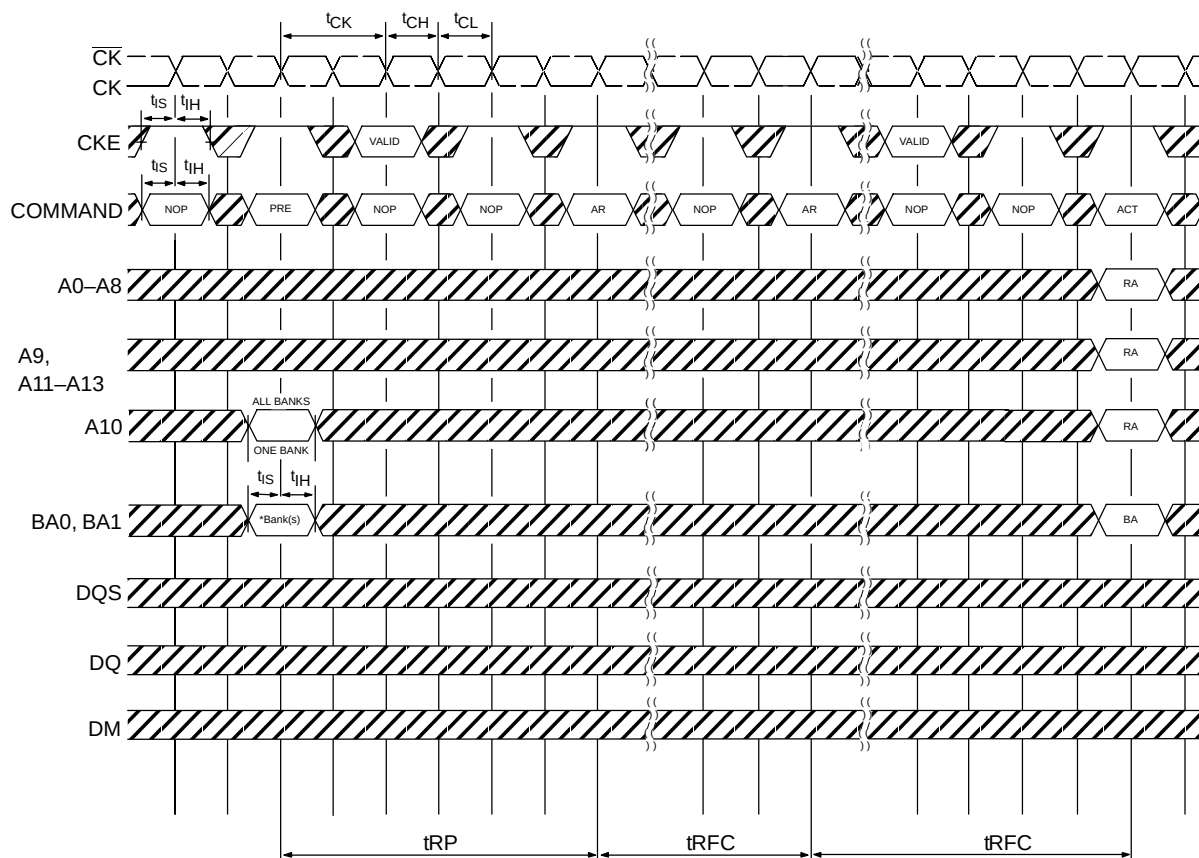


 DON'T CARE

No column accesses are allowed to be in progress at the time Power-Down is entered

* = If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down.

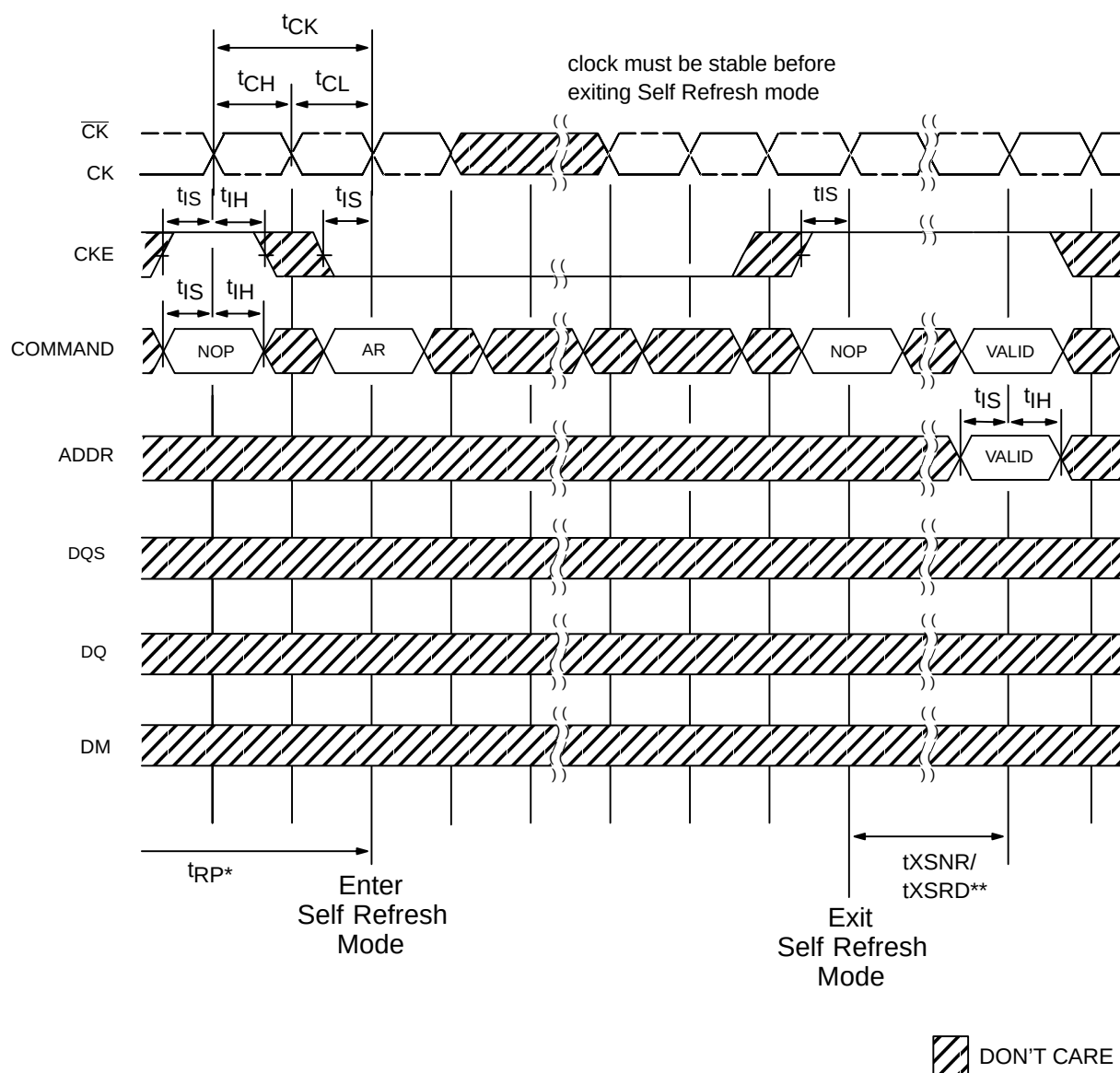
Figure 44 – POWER-DOWN MODE



DON'T CARE

* = "Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
 PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
 NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC.
 DM, DQ and DQS signals are all "Don't Care"/High-Z for operations shown

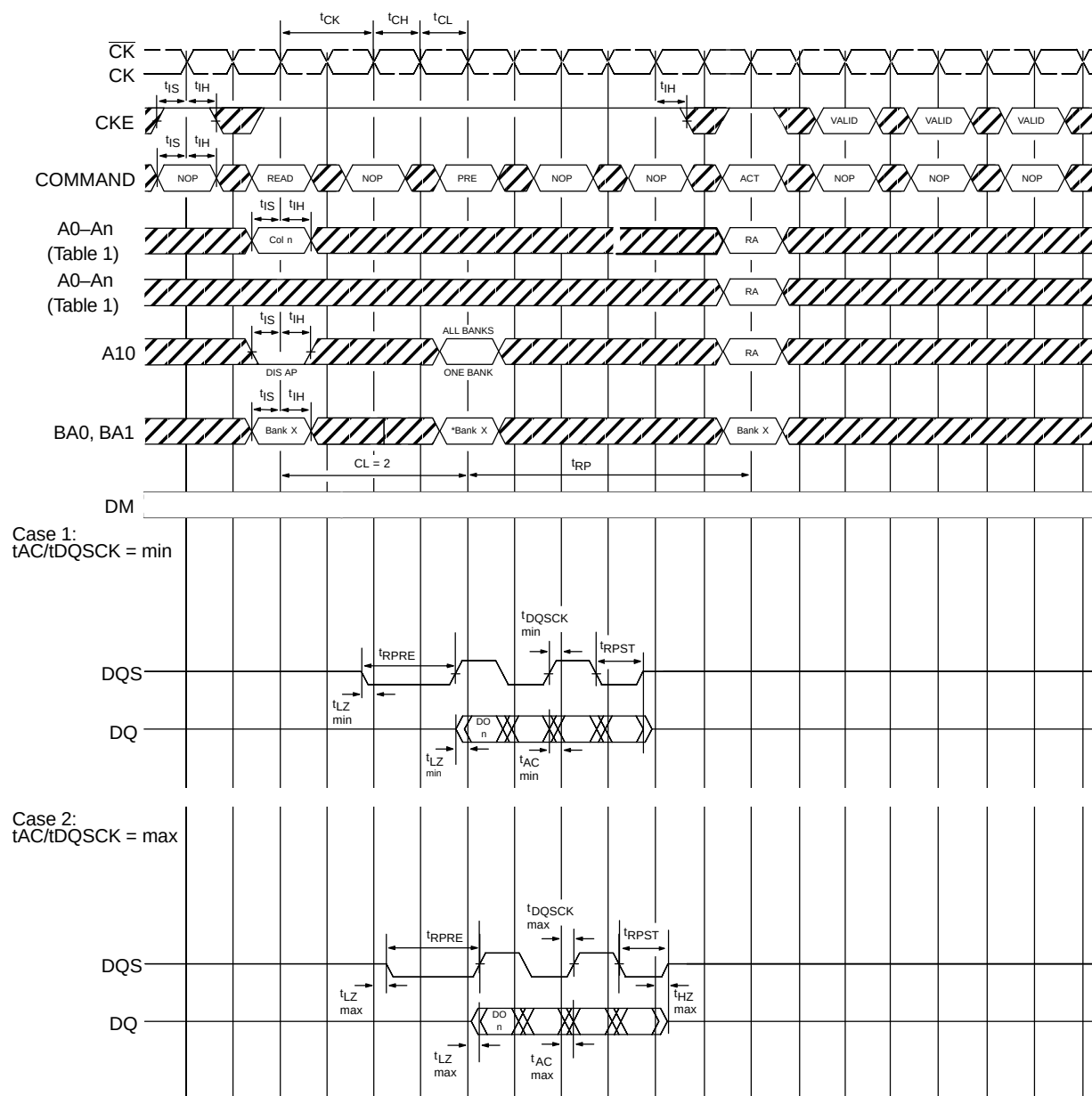
Figure 45 – AUTO REFRESH MODE



* = Device must be in the "All banks idle" state prior to entering Self Refresh mode

** = t_{XSNR} is required before any non-READ command can be applied, and t_{XSRD} is required before a READ command can be applied.

Figure 46 – SELF REFRESH MODE



DON'T CARE

DO n = Data Out from column n
 Burst Length = 4 in the case shown
 3 subsequent elements of Data Out are provided in the programmed order following DO n
 DIS AP = Disable Autoprecharge
 * = "Don't Care", if A10 is HIGH at this point
 PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
 NOP commands are shown for ease of illustration; other commands may be valid at these times
 Precharge may not be issued before t_{RAS} ns after the ACTIVE command for applicable banks.

Figure 47 – READ – WITHOUT AUTO PRECHARGE

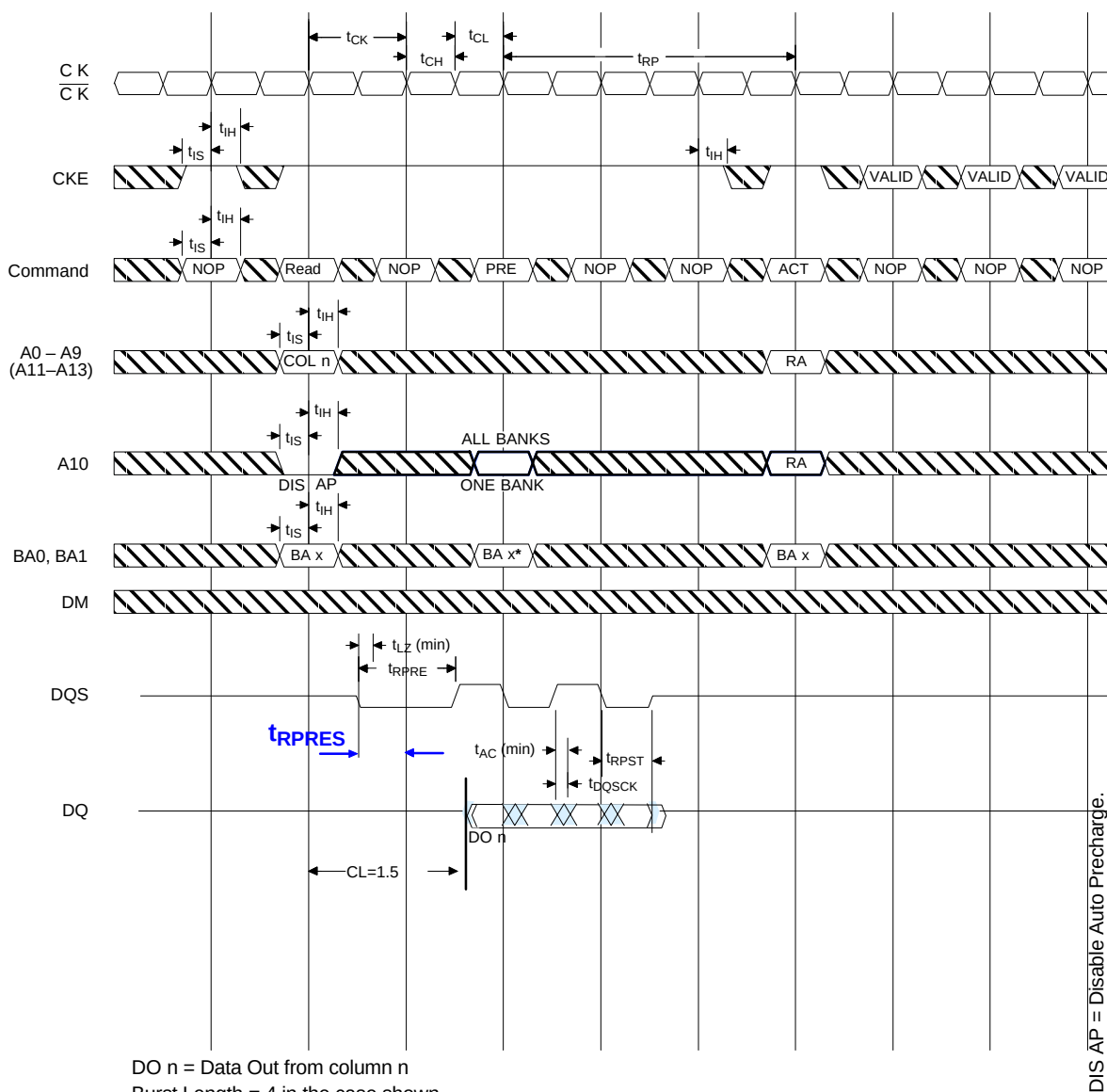


Figure 48 – READ WITHOUT AUTOPRECHARGE (CL=1.5, BL=4)

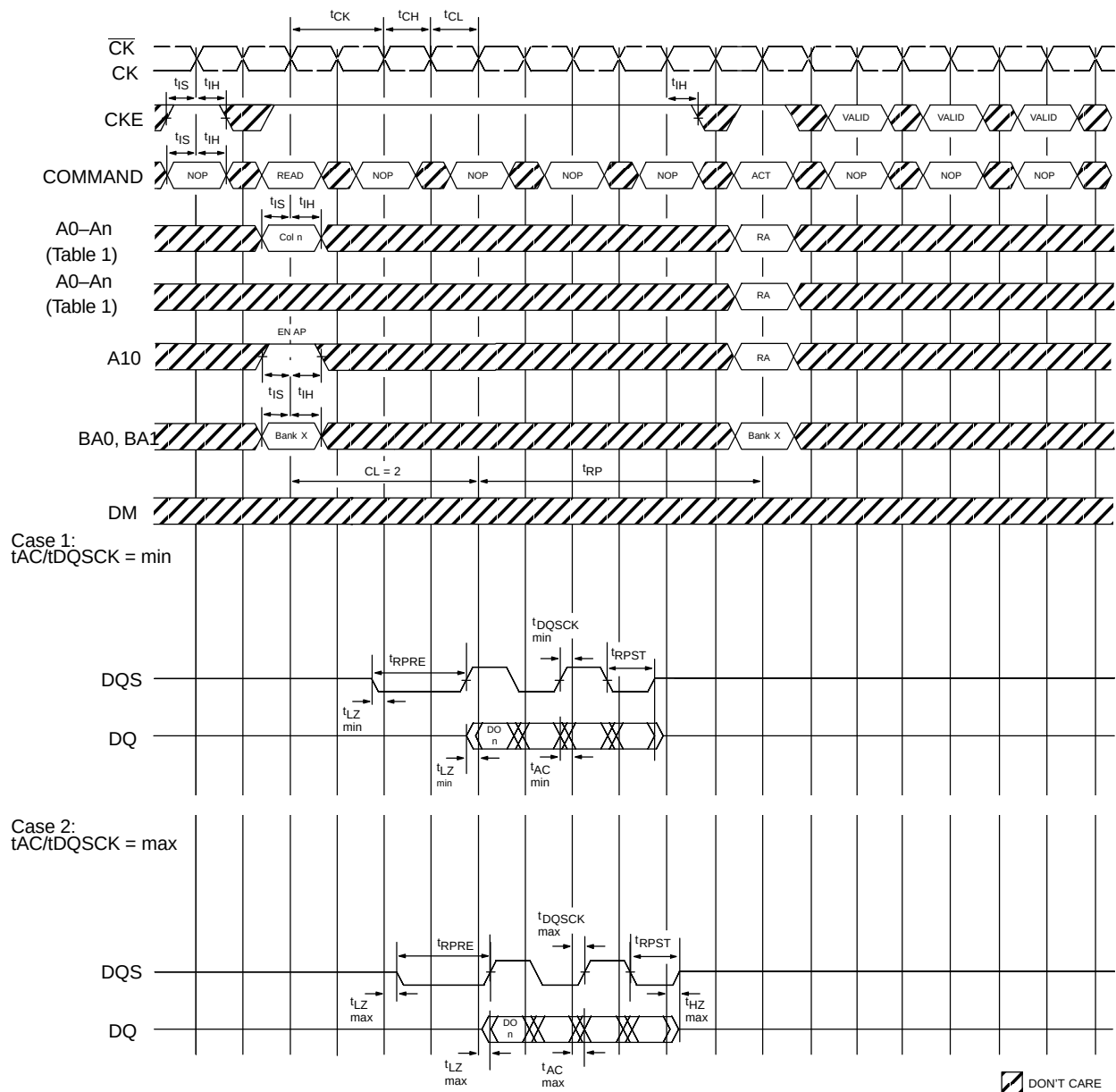
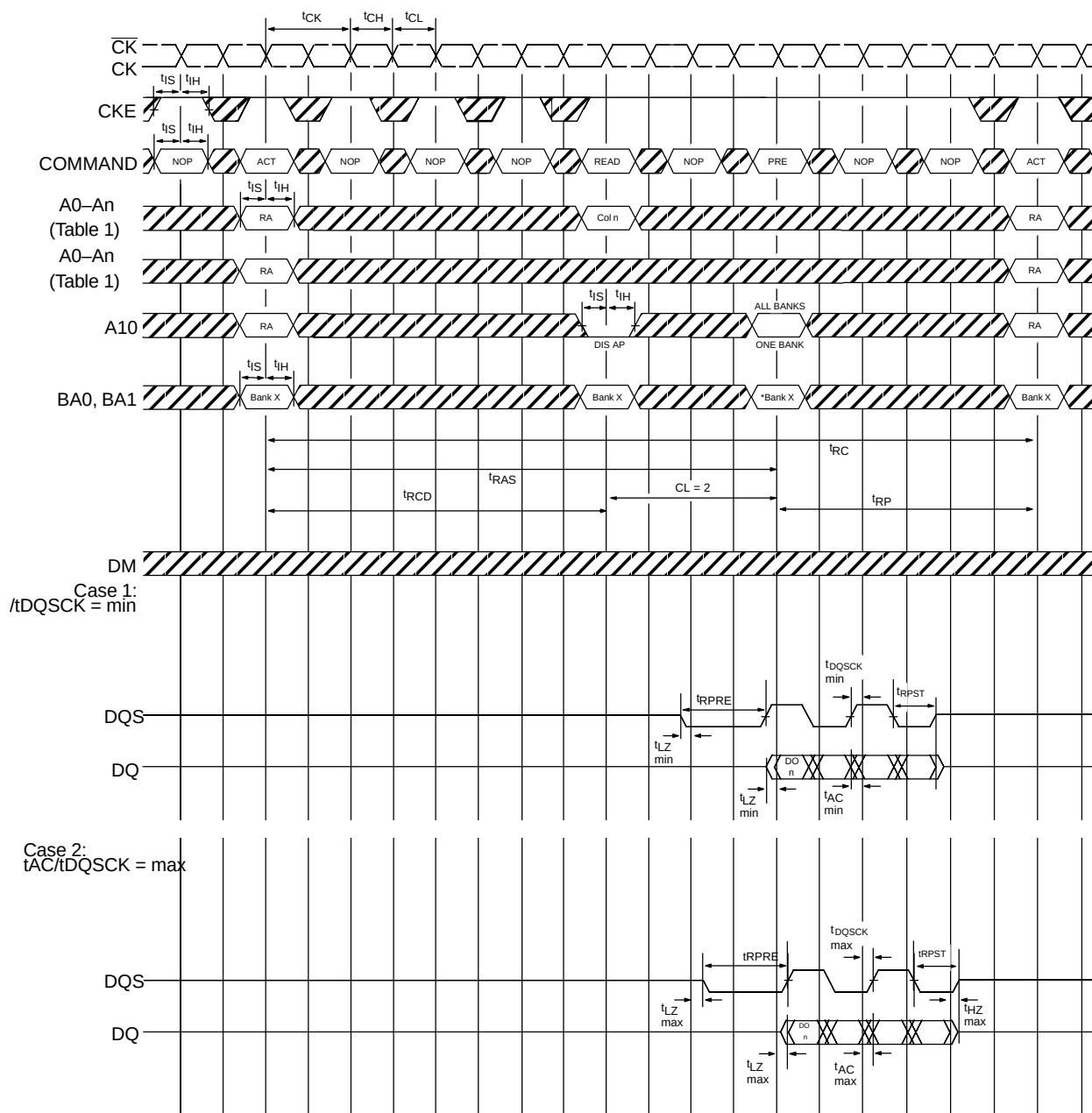


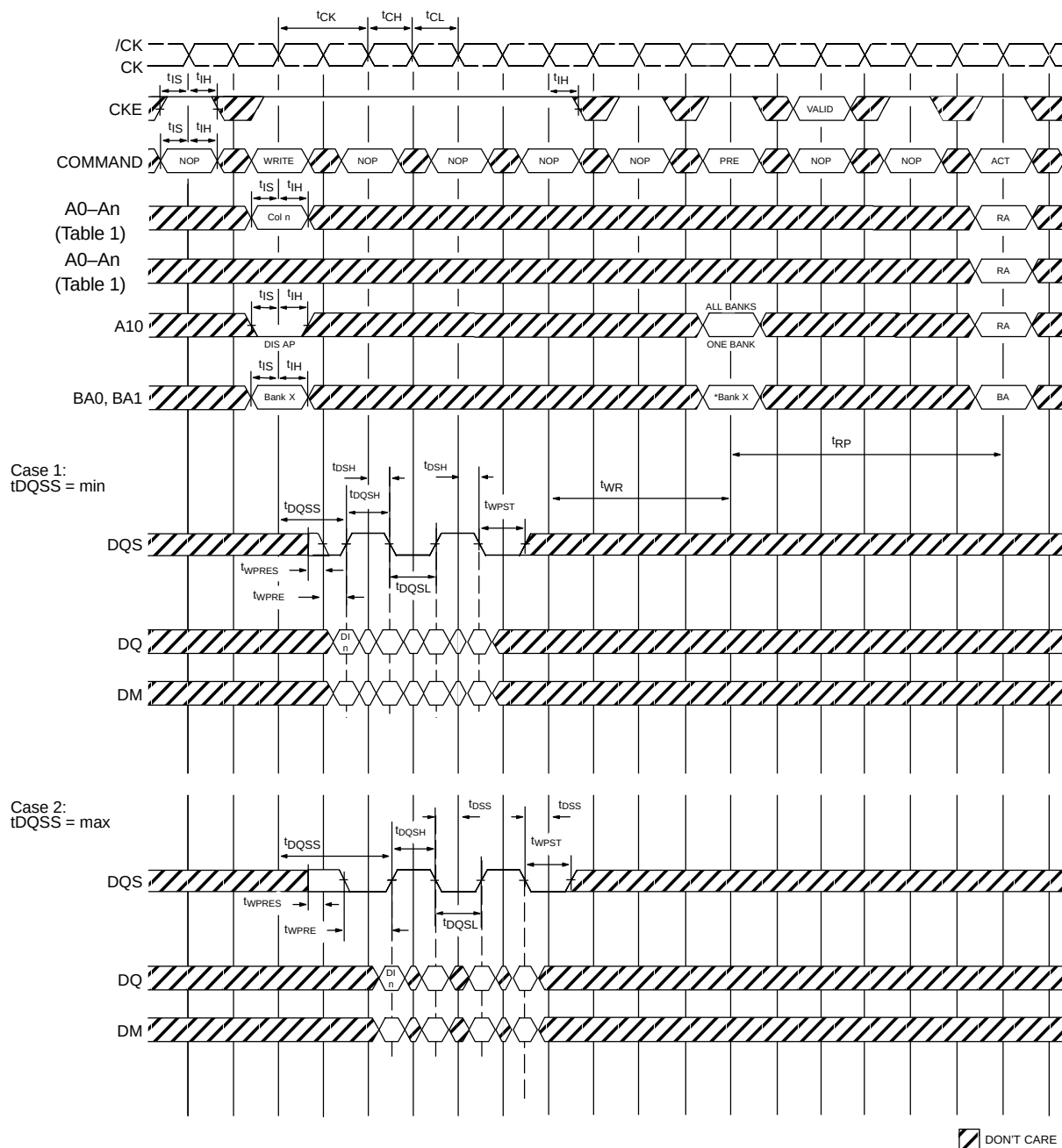
Figure 49 – READ – WITH AUTO PRECHARGE



DO n= Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that $t_{RCD} > t_{RCD\ MIN}$ so that the same timing applies if Autoprecharge is enabled (in which case t_{RAS} would be limiting)



Figure 50 – BANK READ ACCESS



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n

DIS AP = Disable Autoprecharge

* = "Don't Care", if A10 is HIGH at this point

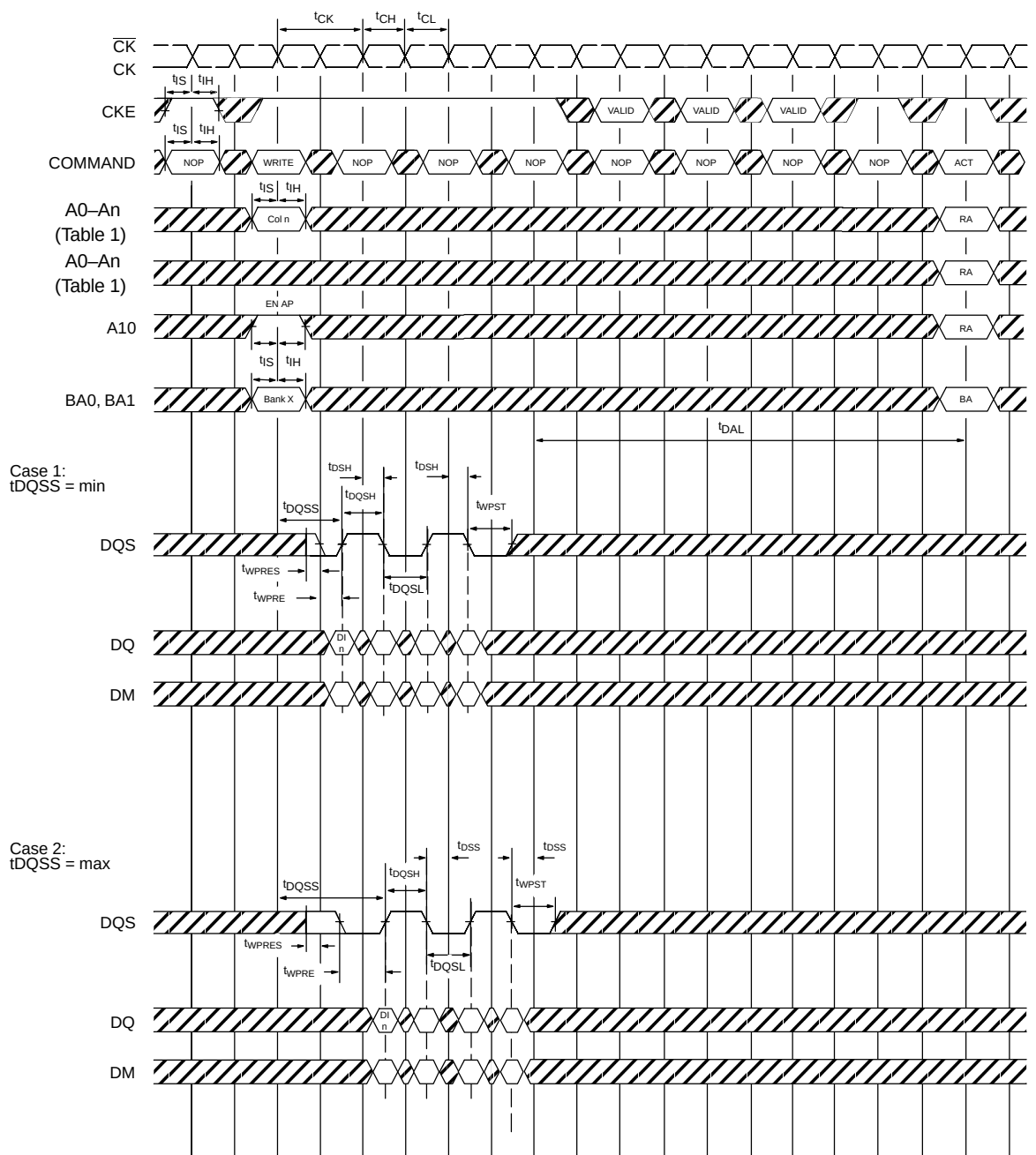
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Although t_{DQSS} is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the $\pm 25\%$ window of the corresponding positive clock edge.

Precharge may not be issued before t_{RAS} ns after the ACTIVE command for applicable banks.

Figure 51 – WRITE – WITHOUT AUTO PRECHARGE



Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI
EN_AD = Enable Autocharge ☐

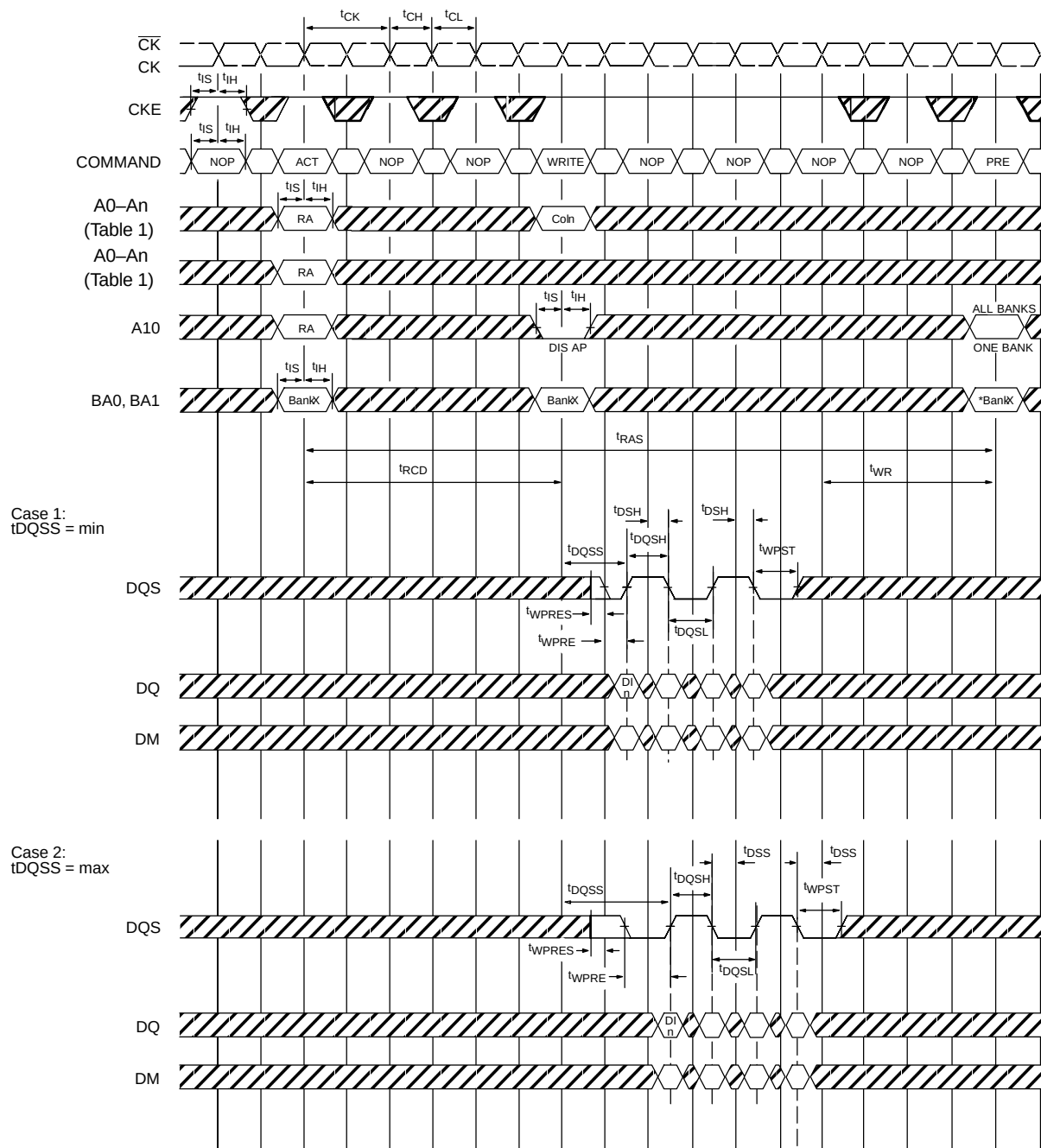
EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the $\pm 25\%$ window of the corresponding positive clock edge.

Figure 52 – WRITE – WITH AUTO PRECHARGE



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n

DIS AP = Disable Autoprecharge

* = "Don't Care", if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address

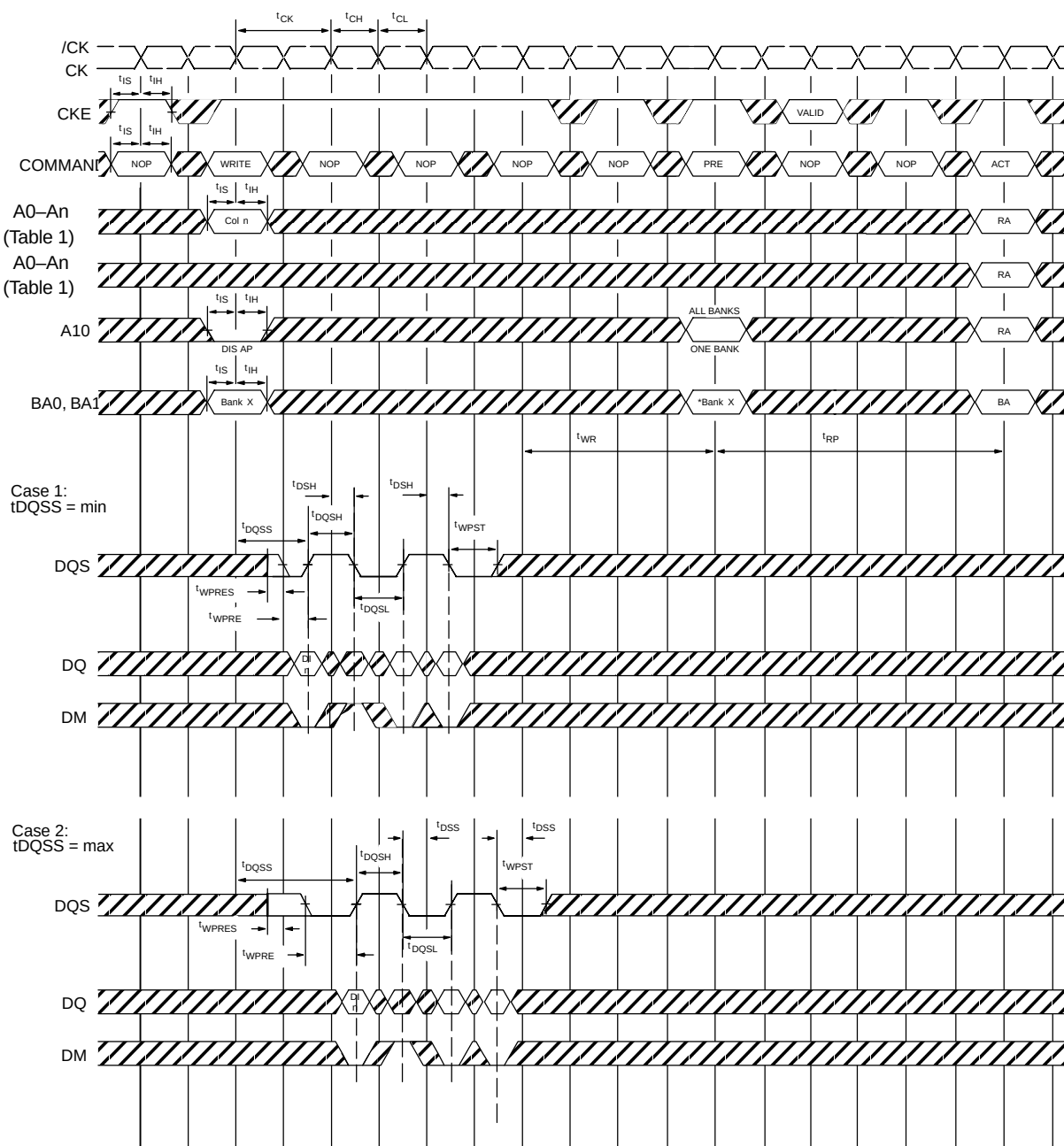
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Although t_{DQSS} is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the $\pm 25\%$ window of the corresponding positive clock edge.

Precharge may not be issued before t_{RAS} ns after the ACTIVE command for applicable banks.

DON'T CARE

Figure 53 – BANK WRITE ACCESS



DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n (the second element of the four is masked)

DIS AP = Disable Autoprecharge

* = "Don't Care", if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the $\pm 25\%$ window of the corresponding positive clock edge.

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.



Figure 54 – WRITE – DM OPERATION



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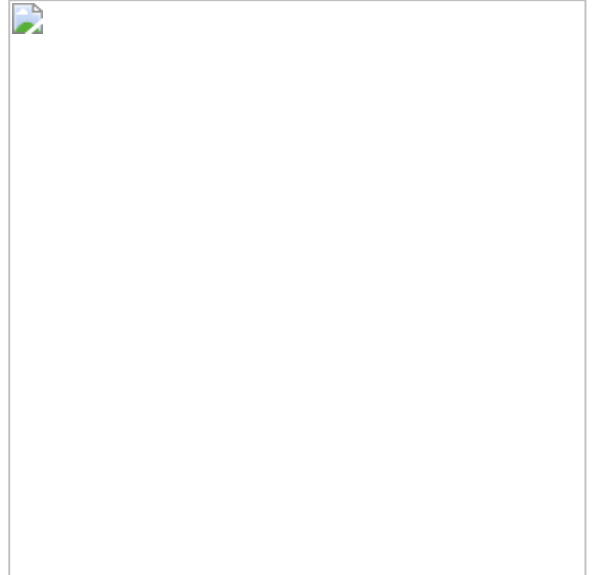


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Cirrus Logic, Inc.	Optek Technology, Inc.
Cisco Systems, Inc.	Panasonic Semiconductor Development Company
C-MAC Microcircuits Ltd.	Panda Project, Inc.
Compaq Computer Corp.	Peak International
Compensated Devices	Peregrine Semiconductor Corporation
Conexant Systems, Inc.	Pericom Semiconductor
Crane Interpoint Corp.	

Credence Systems Corporation	Philips Semiconductors
CST (Comp.Serv.Tech)	Plastronics, Inc.
Cypress Semiconductor	PNY Technologies, Inc.
Daewon USA	PolarFab
Dallas Semiconductor	Power Innovations, Ltd.
Data Device Corp.	Powerex, Inc.
Data General Corp.	Protek Devices
Data I/O Corporation	Qualcomm Inc.
DATARAM	Qualified Parts Lab
Delkin Devices, Inc.	Quality Semic. Inc. (merged with IDT)
Delphi/Delco	Quantum Effect Design
Delta Design, Inc.	R.H. Murphy Co. Inc.
Denali Software	Polyswitch/Tyco
Dense-Pac Microsystems	Real 3D
Digital Equipment Corp.	REMEC
e.PAK International, Incorporated	ROHM Co. LTD, LSI Packaging Division
ELANTEC, Inc.	RF Micro Devices
Electronic Design, Inc. (merged with White Electronic)	Rochester Electronics
Elmos Semiconductor AG	RTP Company
EMC Corporation	RVSI
EMS Technologies, Inc.	Samsung Semiconductor
Enhanced Memory Systems	Sanyo Semiconductor
Enplas/Tesco, Inc.	Schlumberger Tech.
Entegris, incorporated	Schott Glasswerke
Ericsson Telecom	Seiko-Epson/S-mos Systems
Etron Technology, Inc.	Semicoa Semicond.

Evans & Sutherland	Semiconductor Insights
Fairchild Semiconductor	Semitronics, Inc.
Flip Chip Technologies	Semtech Corporation
Flomerics, Inc.	Sensitron Semiconductor
Fluent Incorporated	Serverworks Corporation
Fluoroware, Inc.	Sharp Electronics
Ford Motor Company	Shikatronics, Inc.
Foxconn International	Shinko Electric America
Fujitsu Microelectronics	Shinon Corp.
Galvantech, Inc.	Siemens (See Infineon)
Genesis Semic. Inc.	Signetics KP
General Semiconductor	Silicon Graphics, Inc.
General Test Laboratory	Silicon Magic Corp.
Genesis Semiconductor	Silicon Storage Tech.
Giga Semiconductor/GSI	Siliconix Inc.
GOLDENRAM	Siliconware USA, Inc.
Hagiwara Sys-Com	Simple Technology
Hana Technologies, Inc.	Simtek Corp.
Harris Corp.	Sipex Corp.
Hewlett Packard Co.	SMART Modular Tech.
Hi/FN, Inc.	Solitron Devices, Inc.
High Connection Density, Inc.	Sony Corporation
Hitachi Semiconductor	Southland Micro Systems
Hirose Electric	ST Assembly Test Serv.
Honeywell SSEC	STAKTEK Corporation
Hytek Microsystems	Stellex Microwave System (formerly

Hyundai Electronics	Watkins Johnson)
Hughes Aircraft Co.	STMicroelectronics
IBIDEN USA Corp.	Sud-Chemie
IBM Corporation	Performace Packaging
Infineon (formerly Siemens)	Sun Microsystems, Inc.
Integrated Circuit Systems	Super PC Memory
Integrated Device Tech.	Switchcore AB
Integrated Silicon Solution	Symbios Logic (merged with LSI)
Intel Corporation	Taiwan Semiconductor
International Rectifier	Tanisys Technology
Interworks Computer Products	Technology Works, Inc.
I/O Data Device, Inc.	Teledyne Microelec.
IPAC	Teradyne Inc.
ITT Defense & Electronic	Tessera
ITW/Camtex	Texas Instruments
IXYS Corp.	Toshiba America
JAE Electronics, Inc.	Transmeta Corp.
Keithly Instruments	Trimecs Corp.
Kentron Technologies	TriQuint Semiconductor
KeyTek Instrument Corp.	TRW Space & Electron.
Kingston Technology	Tundra Semiconductor
Kostat, Incorporated	Unigen Corp.
Kyocera America, Inc.	United Desiccants
Lambda Advanced Analog	Unitrode
Lansdale Semiconductor	UMC (USA)
	UTMC
	Vanguard Int'l Semic.
	VIA Technologies, Inc.

Lattice Semiconductor	Viking Components, Inc.
LG Semicon (merged with Hyundai)	Visiontek
	Wells-CTI
Linear Technology Corp.	Western Digital Corp.
Linfinity Microelectr.	White Electronic Designs
LNP Eng. Plastics, Inc.	Wichmann Work AG
Lockheed Martin	Winbond Electronics
LSI Logic Corporation	Wintec Industries, Inc.
Lucent Technologies	Workstation Direct
	Xicor, Inc.
	Xilinx, Inc.
	Yamaichi Electronics USA

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List prepared by Julie Carlson

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Exhibit L

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Actel Corporation	Macronix Int'l Co. Ltd.
Adaptec Inc.	Manufacturing Technology Inc.
Adtec Corporation	Mardec Industrial
Advanced Memory International	Matrox Graphics Inc.
Advanced Micro Devices	Melco Inc.
Advanced Power Technology	Memory Strategies International
Advanced Semiconductor Engineering	Micro Memory Bank
Advantest Corporation	Micron Technology Inc.
Aeroflex Labs Inc.	Micropac Industries
Aeroflex UPMC	Microsemi Corporation
Agere Systems	Minco Technology Inc.
Agilent Technologies	Mini Systems Inc.
ALi Corporation	Mitsubishi Electric and Electronics USA
Allegro MicroSystems	Molex Inc.
Alpha Industries	Mosaic Systems
Altera Corporation	Mosaid Technologies Inc.
Airoha Technology Corporation	Mosel Vitelic Corporation
Amkor Technology	Motorola Inc.
Anadigics Inc.	NanoAmp Solutions Incorporated
Analog Devices Inc.	Nanya Technology Company
Ansoft	National Semiconductor
Apple Computer Inc.	NEC Electronics
Applied Microcircuit Corporation	Netlist Incorporated
Arrow Zeus Electronics	New Jersey Micro Electronic Testing Inc.
ASAT Inc.	NewLogic Technologies AG
ATI Research Silicon Valley Inc.	Nitto Denko America
Atmel Corporation	Nokia Research Center
ATP Electronics Inc.	Northrup Grumman
Avant Technology L.P.	NVIDIA Corporation
Aved Memory Products	OKI Electric Industry Company
Avnet Inc.	Olin Aegis
BAE Systems	ON Semiconductor
Broadcom Corporation	OSE USA
C-MAC Microcircuits Ltd.	Peak International
California Eastern Labs	Pericom Semiconductor
Carsem Inc.	Philips Semiconductors

Caspian Networks Inc.	Plastronics Inc.
Celestica Inc.	PNY Technologies Inc.
Centon Electronics Inc.	Power Innovations Ltd.
Chartered Semiconductor Manufacturing	Powerex Inc.
ChipPac Inc.	Qualcomm Inc.
Chip Supply Inc.	Qualified Parts Lab
Cirrus Logic Inc.	REMEC
Cogiscan Inc.	R.F. Magic
Comax Technology	RF Micro Devices
Compaq Computer Corporation	Ralink Technology
Conexant Systems Inc.	Ricoh Company Limited
Corsair Memory Inc.	Rochester Electronics
Crane Interpoint Corporation	RTP Company
Cray Incorporated	Samsung Semiconductor
CST (Comp.Serv.Tech)	Samsung Techwin Co.
Cypress Semiconductor	SanDisk Corporation
Daewon SPIC/USA	San Max Technologies Inc.
Dane-Elec Corporation	Sanyo Semiconductor
Data Device Corporation	Sarnoff Corporation
Dataram	Semicoa Semiconductor
Delkin Devices Inc.	Semiconductor Insights
Dell Computer	Semtech Corporation
Delphi/Delco	Sensitron Semiconductor
Denali Software	Serverworks Corporation
DPAC Technologies Corporation	Sharp Electronics
e.PAK International Incorporated	Shikatronics Inc.
EEMS Italia SpA	Shinko Electric America
Elite Semiconductor Memory Technology	Shinon Corporation
Elpida Memory Inc.	Silicon Integrated Systems
EMC Corporation	Silicon Graphics Inc.
EMS Technologies Inc.	Silicon Mountain Memory
Enhanced Memory Systems	Silicon Storage Technology
Enplas Tesco Inc.	Siliconware USA Inc.
Entegris Incorporated	Simple/SiliconTech Technology
Etron Technology Inc.	Sirenza Microdevices Inc.
Fairchild Semiconductor	Smart Modular Technology
FCI USA Inc.	SOISIC
Flomerics Inc.	Sony Corporation
Fluent Incorporated	Southland Micro Systems
Foxconn International Inc.	Spirea AB
Fujitsu Microelectronics	ST Assembly Test Services
General Test Laboratory	Staktek Corporation

Global Communication Devices	STMicroelectronics
GSI Technology	Sud-Chemie Performace Packaging
Hagiwara Systems	Sun Microsystems Inc.
Hana Microelectronics Inc.	Super PC Memory
Hana Micron Inc.	Switchcore Inc.
Helic S.A.	T-RAM Inc.
Hewlett Packard Company	Tachyon Semiconductor
Hi/FN Inc.	Taiwan Semiconductor
High Connection Density Inc.	Tality UK Limited
Hitachi Semiconductor	Tanisys Technology
Honeywell SSEC	Techtronix
Huawei Technologies Co. Ltd.	Teledyne Microelectronics
Hynix Semiconductor America Inc.	Teradyne Inc.
Hypertec Limited	Texas Instruments
Hytek Microsystems	Thermo KeyTek
I/O Data Device Inc.	Toshiba America
Ibiden USA Corporation	Transmeta Corporation
IBM Corporation	TriQuint Semiconductor
Infineon Technologies	TRW Inc.
InProComm Inc.	Tundra Semiconductor
Integrated Circuit Systems	Twinmos Technologies
Integrated Device Technology	Tyco Electronics
Integrated Measurement Systems	Ubicom
Integrated Silicon Solution	Unigen Corporation
Intel Corporation	United Plastics Group Inc.
Interactive Silicon Inc.	United Test & Assembly Center
International Rectifier Company	United Test Center Inc.
Intersil Corporation	Vanguard International Semiconductor
Interworks A Sanmina Company	Ventura Technology Corp.
Irvine Sensors Corporation	VIA Technologies Inc.
ITW/Camtex	Virtium Technology Inc.
IXYS Corporation	Vishay Siliconix
JAE Electronics Inc.	Visteon Corporation
Kentron Technologies	White Electronic Designs
Kingston Technology	Winbond Electronics
Kostat Incorporated	Wintec Industries Inc.
Kyocera America Inc.	Xilinx Inc.
Lansdale Semiconductor	Yamaichi Electronics
LeCroy Corporation	
Linear Technology Corporation	
Littelfuse Inc.	
LSI Logic Corporation	

Lucent Technologies

M/A-Com Inc.

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Exhibit M



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[Micron rolls out GDDR3 SDRAM for graphics applications](#)

Proposed by: Youri Peplinkhuizen

Micron Technology Inc. Wednesday said it has delivered what it claimed are the industry's first samples of the next-generation GDDR3 SDRAM for graphics applications.

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5 th International Lead-Free Conference (JEDEC-IPC)
March 17-19, 2004 San Jose
Marriott San Jose, CA.



2nd China International IC Industry Exhibition & Seminar
IC China 2004
Date: September 1~3.2004
Venue: Shanghai Everbright Convention & Exhibition Centre, Shanghai



CD from Lead Free Conference (including Tin Whiskers papers)
Oct. 2003 Frankfurt, Germany.

A Sanmina-SCI	Mathios Associates
A-Data Technology Co.	Micro Memory Bank
Actel Corporation	Micron Technology Inc.
Adtec Corporation	Micropac Industries
Advanced Memory International	Microsemi Corporation
Advanced Micro Devices	Minco Technology Inc.
Advanced Power Technology	Mini Systems Inc.
Advanced Semiconductor Engineering	Mitsubishi
Advantest Corporation	Molex Inc.
Aeluros	Mosel Vitelic Corporation
Aeroflex	Motorola Inc.
Agere Systems	Nanya Technology Semiconductor
Agilent Technologies	National Semiconductor
	NEC Electronics



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Allegro MicroSystems	New Jersey Micro Electronic Testing Inc.
Alliance Semiconductor	NewLogic Technologies AG
Altera Corporation	Nimbus Wireless Inc.
Amkor Technology	Nokia
Anadigics Inc.	Northrup Grumman
Analog Devices Inc.	NVIDIA Corporation
Apacer Technology	OKI Electric Industry Company
Apple Computer Inc.	Olin Aegis
ArrayComm Inc.	ON Semiconductor
Arrow Zeus Electronics	OSE USA
Artisan Components	Peak International
ASAT Inc.	Pericom Semiconductor
ATI Research Silicon Valley Inc.	Philips Semiconductors
Atmel Corporation	Plastronics Inc.
ATP Electronics Inc.	PMC/Sierra
Austin Semiconductor	PNY Technologies Inc.
Avant Technology L.P.	Power Integrations Inc.
Aved Memory Products	Powerex Inc.
Avnet Inc.	Pulse Engineering
BAE Systems	QP Semiconductor
Bourns Ltd.	Qualcomm
Broadcom Corporation	REMEC

Buffalo Inc.	RF Micro Devices
C-MAC Microcircuits Ltd.	Ramaxel Technology Ltd.
California Eastern Labs	Raza Foundries
Carsem Inc.	Renesas Technology
Caspian Networks Inc.	Ricoh Company Limited
Catalyst Semiconductor Inc.	Rochester Electronics
Celestica Inc.	Saifun Semiconductor
Centon Electronics Inc.	Samsung Semiconductor
Chartered Semiconductor Manufacturing	SanDisk Corporation
ChipPac Inc.	San Max Technologies Inc.
Chip Supply Inc.	Sanyo Semiconductor
Cirrus Logic Inc.	Sarnoff Corporation
Cisco Systems Inc.	Semicoa Semiconductor
CMC Electronics Cincinnati	Semtech Corporation
Cogiscan Inc.	Sensitron Semiconductor
Corsair Memory Inc.	Serverworks Corporation
Crane Interpoint Corporation	Shanghai Hua Hong NEC Electronics
Cray Incorporated	Sharp Microelectronics
CST (Comp.Serv.Tech)	Shikatronics Inc.
Cypress Semiconductor	Shinko Electric America
Daewon USA	

Dane-Elec Corporation	Silego Technology
Data Device Corporation	Silicon Graphics Inc.
Dataram	Silicon Image
Delkin Devices Inc.	Silicon Integrated Systems
Dell Computer	Silicon Laboratories
Delphi Corporation	Silicon Mountain Memory
Denali Software	Silicon Storage Technology
DPAC Technologies Corporation	Siliconware USA Inc.
e.PAK International Incorporated	Simple/SiliconTech Technology
EEMS Italia SpA	Skyworks Solutions Inc.
Elite Semiconductor Memory Technology	Smart Modular Technology
Elpida Memory Inc.	Sony Microelectronics
EMC Corporation	ST Assembly Test Services
EMS Technologies Inc.	Staktek Corporation
Endicott Interconnect Technologies	STMicroelectronics
Enplas Tesco Inc.	Sud-Chemie Performace Packaging
Entegris Incorporated	Summit Computer Systems Inc.
Etron Technology Inc.	Sun Microsystems Inc.
Exar Corporation	Swissbit Germany AG
Fairchild Semiconductor	T-RAM Inc.
FCI USA Inc.	

Flomerics Inc.	Taiwan Semiconductor
Fluent Incorporated	Tektronix
FormFactor Inc.	Teledyne Microelectronics
Foxconn International Inc.	Teradyne Inc.
Fujitsu Microelectronics America	Texas Instruments
General Test Laboratory	Tezzaron Semiconductor
Globespan Virata Inc.	Thermo KeyTek
GSI Technology	Theta Microelectronics
Hagiwara Systems	Toshiba America
Hana Microelectronics Inc.	Transmeta Corporation
Hewlett Packard Company	TriQuint Semiconductor
Hi/FN Inc.	TwinMos Technologies
Honeywell SSEC	Tyco Electronics
Huawei Technologies Co. Ltd.	U.S. Army
Hynix Semiconductor America Inc.	Ubicom
Hytek Microsystems Inc.	Ultratera Corporation
I/O Data Device Inc.	Unigen Corporation
Ibiden USA Corporation	Unisys Corporation
IBM Corporation	United Test & Assembly Center
IceFyre Semiconductor Inc.	Universal Networking Machines
	Ventura Technology Corp.

Infineon Technologies	VIA Technologies Inc.
Inphi Corporation	Virtium Technology Inc.
Integrated Circuit Systems	Vishay General Semiconductor
Integrated Device Technology	Vishay Siliconix
Integrated Silicon Solution Inc.	Wells-CTI
Intel Corporation	White Electronic Designs
International Rectifier Company	White Mountain Labs
Intersil Corporation	Winbond Electronics
ITW/ECPS	Wintec Industries Inc.
IXYS Corporation	Xilinx Inc.
JAE Electronics Inc.	Yamaichi Electronics
Jazz Semiconductor	
Kentron Technologies	
Kingmax Semiconductor Inc.	
Kingston Technology Company Inc.	
King Tiger Technology Inc.	
Kostat Incorporated	
Lansdale Semiconductor Inc.	
LeCroy Corporation	
Legacy Electronics Inc.	

Linear Technology Corporation	
Littelfuse Inc.	
LSI Logic Corporation	
Lucent Technologies	
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Mentor Graphics Corporation
Micro Memory Bank
Microchip Technology
Micron Technology Inc.
Micropac Industries
Microsemi Corporation
Minco Technology Labs Inc.
Mini Systems Inc.
Mitsubishi
Molex Inc.
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 Brain Power USA
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[Buffalo Inc.](#)
 C-MAC Microcircuits Ltd.
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[Carsem Inc.](#)
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[Catalyst Semiconductor Inc.](#)
[Celestica Inc.](#)
[Centon Electronics Inc.](#)
 Century Micro Inc.
 Chartered Semiconductor Manufacturing
[Chip Supply In.](#)
[Cirrus Logic Inc.](#)
 Cisco Systems Inc.
 CMC Electronics Cincinnati
 CompuTaiwan Information Corp. Ltd.
[Corsair Memory Inc.](#)
 COS Memory AG
 Crane Interpoint Corporation
[Cray Inc.](#)
 Credence
[CST \(Comp.Serv.Tech\)](#)
[Cypress Semiconductor](#)
 D.E. Shaw Research & Development
 Daewon USA
 Dane-Elec Corporation
 Data Device Corporation
 Dataram
[Dell Inc.](#)

[National Semiconductor](#)
[NEC Electronics America Inc.](#)
[Netlist Inc.](#)
 Nexus Technology Inc.
 Nokia
 Northrup Grumman
[NVIDIA Corporation](#)
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[OKI Electric Industry Company](#)
 Olin Aegis
 ON Semiconductor
[Oneida Research Services Inc.](#)
[Pacific Fore Technologies Ltd.](#)
[PDP Systems Inc.](#)
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 Pericom Semiconductor
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[Hana Micron Inc.](#)
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Hirose Electric Co.
Honeywell
Huawei Technologies Co. Ltd.
Hynix Semiconductor America Inc.
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Silicon Image
Silicon Motion Inc.
[Silicon Mountain Memory](#)
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[Siliconware USA Inc.](#)
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[Teledyne Microelectronics](#)
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Tezzaron Semiconductor
[Thermo Electron](#)
Toshiba America
Total Parts Plus

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Intersil Corporation
ITW/ECPS
IXYS Corporation
JAE Electronics Inc.
Jazz Semiconductor
Jiang Su Changjiang Elec. Tech. Co. Ltd.
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Kingmax Semiconductor Inc.
Kingston Technology
Company Inc.
King Tiger Technology Inc.
Kostat Incorporated
Kreton Corporation
Lansdale Semiconductor Inc.
Lattice Semiconductor
LeCroy Corporation
Legacy Electronics Inc.
Legend Australasia
Lenovo International
Linear Technology Corporation
Littlefuse Inc.
Lord Corporation
Lotes Co. Ltd.
LSI Logic Corporation
Lucent Technologies

Transcend
TriQuint Semiconductor
TwinMos Technologies
Tyco Electronics
U.S. Army
Unifosa Corporation
Unigen Corporation
Unisys Corporation
United Test & Assembly Center
Universal Network Machines
Ventura Technology Corp.
VIA Technologies Inc.
Viking Interworks
A Sanmina-SCI Company
Virtium Technology Inc.
Vishay General Semiconductor
Vishay Siliconix
Vitesse Semiconductor
VPT Inc.
Wavecrest Corporation
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White Mountain Labs
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Xilinx Inc.
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