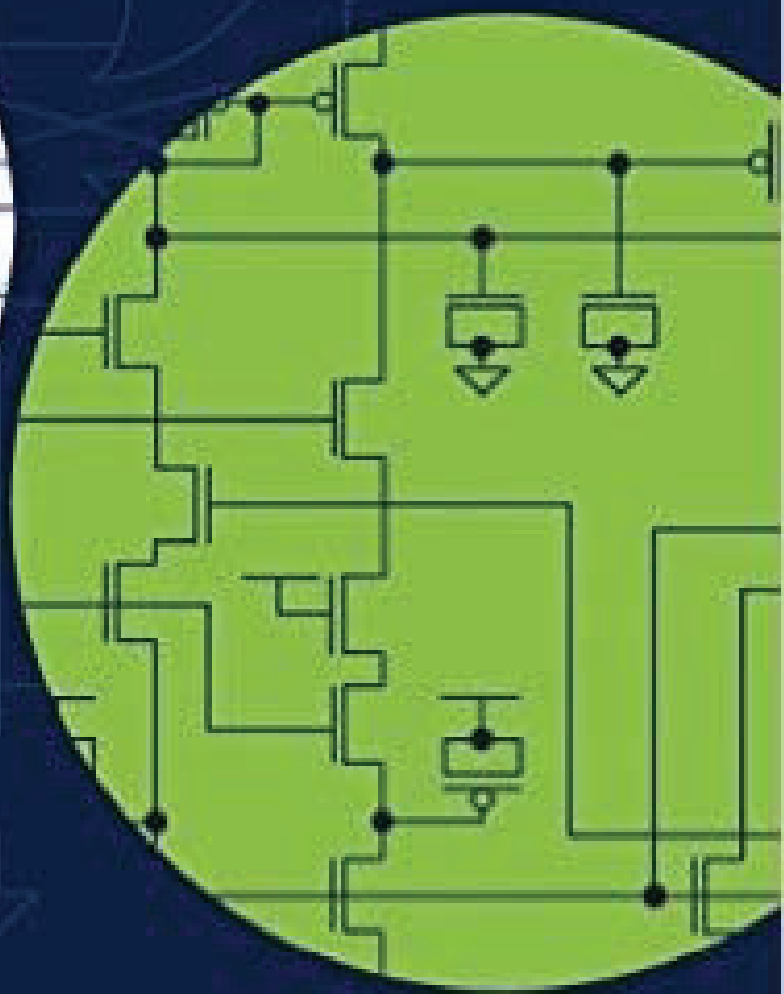
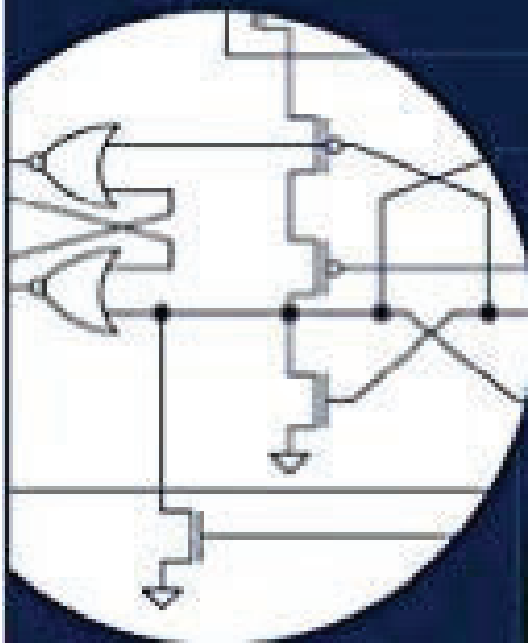


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Preface

For the last 25 years, CMOS (complementary metal oxide semiconductor) technology has been the dominant technology for fabricating integrated circuits (ICs or chips). For the next 25 years, CMOS will, no doubt, continue to be the dominant integrated circuit technology. Why? CMOS technology is reliable, manufacturable, low power, low cost, and, perhaps most importantly, scalable. The fact that silicon integrated circuit technology is scalable was observed and described in 1965 by Intel founder Gordon Moore. His observations are now referred to as *Moore's law* and state that the number of transistors on a chip will double every 18 months. While originally not specific to CMOS, Moore's law has been fulfilled over the years by scaling down the feature size in CMOS technology (it's getting cut in half every 18 months). Whereas the gate lengths of early CMOS transistors were in the micrometer range (long-channel devices) the feature sizes of current CMOS devices are in the nanometer range (short-channel devices).

To encompass both the long- and short-channel CMOS technologies in this book, I take a two-path approach to custom CMOS integrated circuit design. Design techniques are developed for both and then compared. This comparison gives readers deep insight into the circuit design process.

As an academic text, the book is filled with practical design examples, discussions, and problems. The assumed background of the reader is a knowledge of linear circuits, microelectronics, and digital logic design. The solutions to the end-of-chapter problems (for self-study) and the netlists used when simulating the circuits are found at <http://cmosedu.com>. Those interested in gaining an in-depth knowledge of CMOS analog and digital design will be greatly aided by downloading, modifying, and simulating the netlists of the book's circuits.

Several courses can be taught using this book including VLSI or physical IC design (chapters 1–7 and 10–15), analog IC design (chapters 8–9 and 20–24), memory circuit design (16–19), and advanced analog IC design (25–29). A graduate course in mixed-signal design following the advanced analog IC design course can be taught using the second volume of this book entitled *CMOS Mixed-Signal Circuit Design*.

In this edition, LASICAD software is used once again to introduce circuit layout and WinSPICE is used for the circuit simulations. The material covering the LASICAD tool can be skipped if other layout software packages are used. I like using LASICAD in a first course on IC design because it takes very little class time to learn. Further, other SPICE programs can be used to simulate the circuit netlists with little or no modifications. Both the LASICAD software and the WinSPICE circuit simulator run under Windows and can be downloaded at <http://cmosedu.com>.

How will this book be useful to the student, researcher, or practicing engineer?

I've put a great deal of effort into making this book useful to an eclectic audience. For the student, the book is filled with hundreds of examples, problems, and practical discussions (according to one of my students there can never be too many examples in a textbook). The layout discussions build a knowledge foundation important for troubleshooting and precision or high-speed design. Layout expertise is gained in a step-by-step fashion by including circuit design details, process steps, and simulation concerns (parasitics). Covering layout in a single chapter and decoupling the discussions from design and simulation was avoided. The digital design chapters emphasize real-world process parameters (e.g., I_{off} , I_{on} , t_{ox} , V_{DD}). The analog chapters provide coherent discussions about selecting device sizes and design considerations. Likewise "cookbook" design procedures for selecting the widths/lengths of MOSFETs and design using long-channel equations in a short-channel process are not present. The focus is on preparing the student to "hit the ground running" when they become a custom CMOS IC designer or product engineer.

For the researcher, topics in circuit design such as noise considerations and sensing using delta-sigma modulation (DSM) have been added to this edition. I've also tried to anticipate future design paradigms. For example, the addition of DSM has been applied to CMOS image sensors, Flash memory, and memory using thin oxides (direct tunneling). Sensing using DSM was included because it makes use of the fact that as CMOS clock speeds are going up, the gain and matching of transistors is deteriorating. Further, I've tried to anticipate noise-limited design issues such as, "Why can't I improve the signal-to-noise ratio in my imaging chip?" or "Why is integrating thermal or flicker noise harmful?"

For the working engineer, I've tried to provide design and layout examples that will be immediately useful in products. At the risk of stating the obvious, matching, power, speed, process shifts, power supply voltage variations, and temperature behavior are extremely important in practical design. I've focused the discussions and examples found in this book on these topics. Phase-locked loops, charge pumps, low-voltage references, single and fully-differential op-amp designs, continuous-time and clocked comparators, memory circuits, etc., are covered in detail with numerous examples. To ensure the most practical computer validation of the designs, the simulations for the nanometer designs (a 50 nm process) use the BSIM4 SPICE models.

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R. Jacob (Jake) Baker

- 23.7 Show why n^+ directly in the p-substrate cannot be used as a diode in a CMOS process.
- 23.8 Generate a diode model that produces a forward voltage drop of 700 mV when driven with 1 μ A and has a change with temperature, dV_f/dT , near room temperature, of -2 mV/C. Use simulations to verify your model meets the requirements.
- 23.9 Generate a SPICE model for the Schottky diode seen in Fig. 23.21. Assume that the series resistance of the diode is 1 k Ω .
- 23.10 Estimate, using hand calculations, the minimum allowable V_{DD} for the reference of Ex. 23.4. What are the PMOS and NMOS gate-source and drain-source voltages when the reference current is 1 μ A? Note that the parameters in Table 9.1 have nothing to do with the operating conditions in this question. Verify your answers using SPICE.
- 23.11 Show that K forward-biased diodes in parallel behave like a single diode with a scale current of $K \cdot I_s$, as assumed in Eq. (23.30).
- 23.12 Suggest a reference design that would output a voltage of $n \cdot V_T$.
- 23.13 Determine whether the performance of the BGR of Fig. 23.32 can be enhanced by using the topology of Fig. 23.33. Use simulations to verify your answer.

Chapter 24

Operational Amplifiers I

The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design. A block diagram of the two-stage op-amp with output buffer is shown in Fig. 24.1. The first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as a common source stage, and finally by an output buffer. If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. If the op-amp is used to drive a resistive load or a large capacitive load (or a combination of both), the output buffer is used.

Design of the op-amp consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp A_{OL} (open-loop gain), CMR (common-mode range on the input), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio), output voltage range, current sourcing/sinking capability, and power dissipation.

We'll start this chapter off with a very simple two-stage op-amp (without an output buffer). By pointing out the weaknesses with this two-stage topology, we'll set the stage for developing practical op-amps in the rest of the chapter.

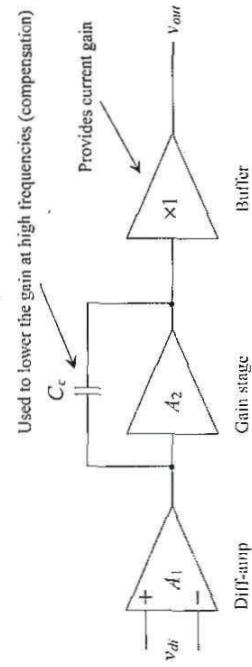


Figure 24.1 Block diagram of two-stage op-amp with output buffer.

24.1 The Two-Stage Op-Amp

Figure 24.2 shows the basic two stage op-amp made using an NMOS diff-amp and a PMOS common-source amplifier (M7). As seen in Fig. 22.8 M7 is biased to have the same current as M3 and M4 (10 μ A from Table 9.2). Note also the addition of the compensating network consisting of a compensation capacitor, C_c , (Miller compensation) and a zero-nulling resistor R_z (see Figs. 21.25 and 21.33 along with the associated discussion). Because the op-amp doesn't have an output buffer, it is limited to driving capacitive loads and very large resistances (comparable to the output resistance of a MOSFET, that is, megohms).

Low-Frequency, Open Loop Gain, A_{OLDC}

The low-frequency, open loop gain of the op-amp is calculated as the product of each stage gain, that is,

$$A_{OLDC} = A_1 \cdot A_2 = \underbrace{g_{m1} \cdot (r_{o1} \parallel r_{op})}_{A_1 = \text{diff-amp's gain}} \cdot \underbrace{g_{m7} \cdot r_{o7}}_{A_2, \text{ M7's gain}} \quad (24.1)$$

where the output resistance of the cascode current source load, M8, is assumed to be much larger than the M7 output resistance, r_{o7} . Using the values from Table 9.2, we get an A_{OLDC} of 832 V/V .

Input Common-Mode Range

The minimum input common-mode voltage is given by Eq. (22.11) or 450 mV. The maximum input common-mode voltage is given by Eq. (22.12) or 900 mV. This means, for proper operation of our two-stage op-amp, the input voltages (v_p and v_m) should fall within the range of 450 to 900 mV. If they go outside this range, the op-amp gain drops, and it is likely that the circuit employing the op-amp will not function properly. Figure 24.3 shows a SPICE DC sweep where the inverting input (v_m) is held at 500 mV and the noninverting input (v_p) is swept from 495 to 505 mV. The slope of this transfer curve is the DC open-loop gain of the op-amp, A_{OLDC} .

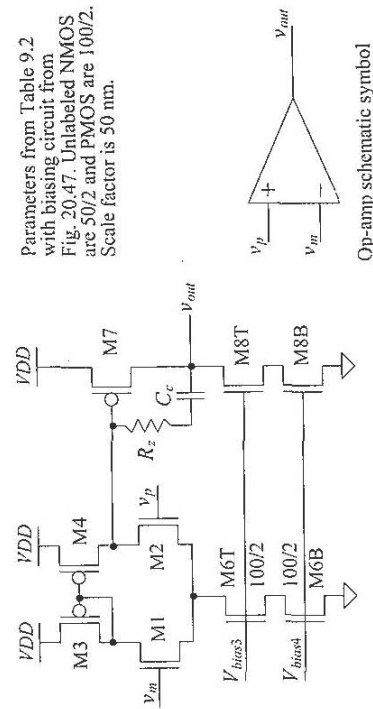


Figure 24.2 Basic two-stage op-amp.

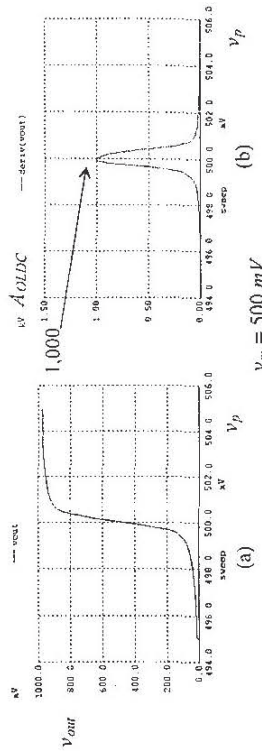


Figure 24.3 (a) DC transfer curves for the op-amp in Fig. 24.2 and (b) its gain (the derivation of (a)).

Power Dissipation

To determine the power dissipated by the op-amp, we sum the currents supplied by the constant current sources and multiply the result by V_{DD} . For the op-amp in Fig. 24.2, the current through M6 is 20 μ A and the current through M8 is 10 μ A. The total power dissipation is then 30 μ W ($V_{DD} = 1$ V).

Output Swing and Current Sourcing/Sinking Capability

The maximum output swing (for the op-amp in Fig. 24.2) is limited by M7 going into the triode region. If we must keep at least 100 mV across M7, then the maximum output voltage is 900 mV. When M8 goes into triode or roughly 100 mV (see Fig. 20.48), the minimum output voltage is set. As seen in Fig. 24.3a, the high-gain (or large slope) region falls between 900 and 490 mV. Note that the maximum amount of current that this op-amp can sink is limited by the constant current sink M8 or 10 μ A. The op-amp can source considerably more than 10 μ A by pulling the gate of M7 downwards. Because this topology can source a considerable amount of current, it is useful as a voltage regulator (because the op-amp is always only sourcing current in a voltage regulator application).

Offsets

We've talked in great length (earlier in the book) about random offsets and how to design and layout circuits to minimize their effects. Another type of offset (that is not random) is termed a *systematic offset*. When we sized the MOSFETs in Fig. 24.2, for example, we made sure that M7 was sized to source 10 μ A and M8 was sized to sink 10 μ A. What would happen if we sized M7 to source 100 μ A of current instead (changed its size from 100/2 to 1000/2)? Because M8 is a constant bias of 10 μ A, M7 would move into the triode region until it was sourcing the 10 μ A of current that M8 wants to sink. The output voltage would be very close to V_{DD} with M7 in the triode region. Effectively we would get a shift or offset in the transfer curves seen in Fig. 24.3a (see Fig. 24.4a). To model this output voltage shift, we can refer it back to the op-amp input as an input-referred offset voltage, Fig. 24.4b. Note that unlike a random offset, which may be positive or negative in value, a systematic offset will always be a known polarity. Finally, note that while we chose to model the offset in series with the noninverting input terminal, in Fig. 24.4, we could just as easily have placed it in series with the inverting op-amp terminal (with a change in polarity).

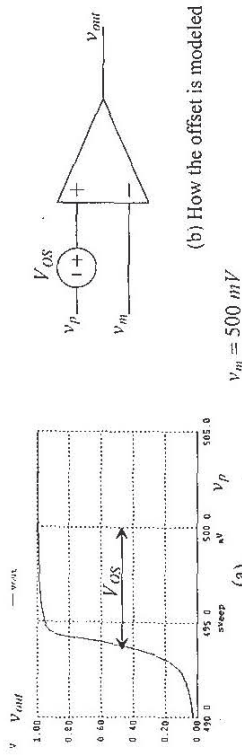


Figure 24.4 Showing how increasing M7's width to 1000 in Fig. 24.2 causes an input-referred (systematic) offset voltage.

Compensating the Op-Amp

An important step in op-amp design is the design of the compensation network. The op-amp takes the difference between the inverting and noninverting input terminal voltages and, ideally, multiplies the result by a very large number (the gain). A block diagram representation of an op-amp is seen in Fig. 24.5. The open-loop gain as a function of frequency is labeled $A_{OL}(f)$.

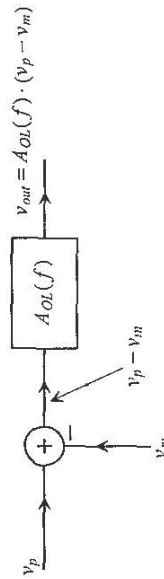


Figure 24.5 Block level diagram of an op-amp.

In all practical situations, the op-amp is used with feedback, Fig. 24.6. While our op-amp in Fig. 24.2 cannot drive a resistive load (unless it is megohms, as a resistor on the op-amp output will kill the gain of the second stage), we'll still use this figure (Fig. 24.6) to illustrate the concept of feedback and compensation. We can write

$$v_{out} = A_{OL}(f) \cdot (v_{in} - v_f) \quad (24.2)$$

and

$$v_f = v_{out} \cdot \frac{R_2}{R_1 + R_2} \quad (24.3)$$

The amount of the output that is fed back is often called the feedback factor β or

$$\beta = \frac{R_2}{R_1 + R_2} \quad (24.4)$$

Substituting Eqs. (24.3) and (24.4) into Eq. (24.2) and solving for the closed loop gain gives

$$A_{CL}(f) = \frac{v_{out}}{v_{in}} = \frac{A_{OL}(f)}{1 + \beta \cdot A_{OL}(f)} \quad (24.5)$$

If we take $A_{OL}(f) \rightarrow \infty$, then the closed loop gain becomes

$$A_{CL}(f) \rightarrow \frac{1}{\beta} = 1 + \frac{R_1}{R_2} \quad (24.6)$$

We have several important points that we need to discuss. To begin, notice that in Eq. (24.5) if

$$\beta \cdot A_{OL}(f) = -1 \quad (24.7)$$

or more precisely

$$|\beta \cdot A_{OL}(f)| = 1 \text{ and } \angle \beta \cdot A_{OL}(f) = \pm 180^\circ \quad (24.8)$$

the closed loop gain blows up (the feedback amplifier becomes unstable). The worst case situation (the largest value of β) occurs when all of the output is fed back to the op-amp input. The voltage follower, Fig. 24.7, is an example of this situation. To determine the stability of an op-amp, we'll look at the open loop gain when the feedback factor is one, that is,

$$|A_{OL}(f)| = 1 \text{ and } \angle A_{OL}(f) = 180^\circ \quad (24.9)$$

We'll discuss this in greater detail in a moment. Notice that the larger the closed loop gain, the smaller the value of β (the less output signal we feed back) and the more likely the op-amp circuit, with feedback, will be stable. This is important. While feedback helps to desensitize an amplifier's gain to variations in an op-amp's A_{OL} , the drawback is stability. In a high-performance op-amp that will never operate in a unity-follower configuration, we can get an enhancement in speed by reducing the amount of compensation (the amount of the reduction guided by Eq. (24.8) with the actual value of β used).

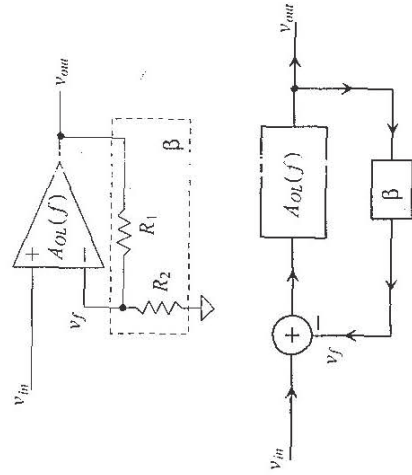


Figure 24.6 An example of feedback in an op-amp.

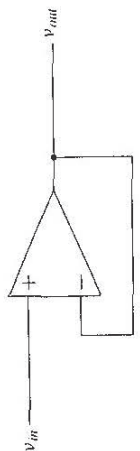


Figure 24.7 Voltage follower configuration, an example of a closed-loop amplifier with unity feedback factor.

To estimate the open-loop frequency response of the op-amp, let's use the generic model seen in Fig. 21.25. Figure 24.8 shows the location of nodes 1 and 2 on our two-stage op-amp. We've included a load capacitance in this figure. With the help of Table 9.2 we can write

$$\begin{aligned} R_1 &= r_{on} || r_{op} = 111 \text{ k}\Omega \\ R_2 &= r_{op} || R_{occur} \approx r_{op} = 333 \text{ k}\Omega \\ g_{m1} &= g_{mn} = 150 \text{ }\mu\text{A/V (diff-amp)} \\ g_{m2} &= g_{mp} = 150 \text{ }\mu\text{A/V (common-source)} \\ C_1 &= C_{dg4} + C_{gd2} + C_{gs7} = 13.6 \text{ fF} \\ C_2 &= C_L + C_{gd8} \approx C_L + 1.56 \text{ fF} \\ f_1 &\approx \frac{1}{2\pi g_{m2} R_1 R_2 C_c} = 287 \text{ kHz} \end{aligned}$$

Let's calculate the open-loop response with a load and compensation capacitance of 100 fF, that is, $C_L = C_c = 100 \text{ fF}$. The pole associated with node 1, from Eq. (21.65), is

$$f_1 \approx \frac{1}{2\pi g_{m2} R_1 R_2 C_c} = 287 \text{ kHz}$$

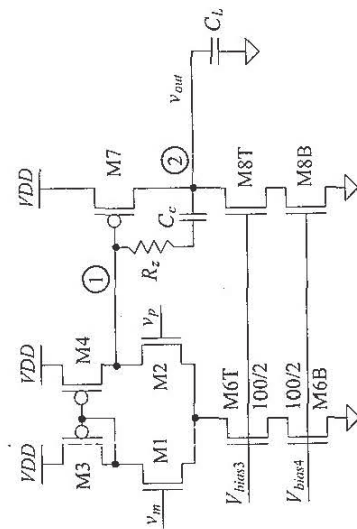


Figure 24.8 Calculating the frequency response of the op-amp.

The location of the pole associated with the output node (node 2) is, from Eq. (21.66),

$$f_2 = \frac{g_{m2} C_c}{2\pi(C_1 C_2 + C_1 C_c + C_2 C_c)} = 210 \text{ MHz}$$

The location of the zero, f_z in Eq. (21.63), is at 240 MHz (very near the second pole).

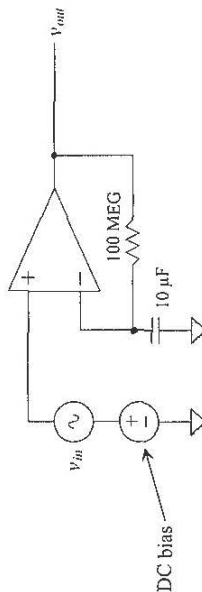


Figure 24.9 Circuit configuration used to simulate open-loop frequency response.

To simulate the open-loop response of the op-amp, we can use the configuration seen in Fig. 24.9. The feedback resistor and capacitor form a time constant so large that for all intents and purposes none of the AC output voltage is fed back to the inverting input. However, the DC bias level is fed back so that the op-amp biases up correctly (all MOSFETs are operating in the saturation region). With a DC bias voltage of 500 mV, Fig. 24.10 shows the open loop responses of the op-amp in Fig. 24.8 with 100 fF compensation capacitance and load capacitance. The simulated values are close to the

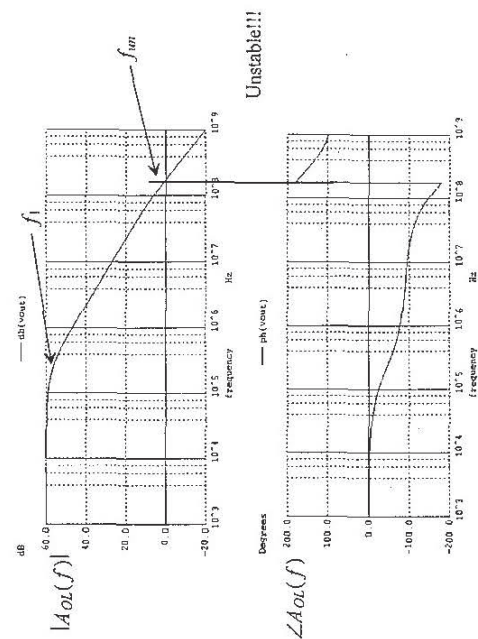


Figure 24.10 The open-loop frequency response of the op-amp in Fig. 24.8 with a 100 fF compensation capacitance and load capacitance.

hand-calculated values given above. However, from the criteria given in Eq. (24.9), the op-amp will clearly be unstable. *We want the open loop gain of the op-amp to be much less than one when the phase shift is 180°.* Looking at Fig. 24.10, we effectively want to shift the lower frequency pole (f_1) downwards in frequency. At the same time, we want to move the higher frequency pole, f_2 , higher in frequency (we want to *split the poles*). Remember this (pole-splitting) was the point of adding the compensation capacitor to an amplifier back in Ch. 21. Let's use Eq. (21.72) to select C_c . Looking at Fig. 24.10, we see that the phase shift is -100° at 10 MHz, so let's set the unity gain frequency to this value (in an attempt to make sure that the open loop gain is well under one when the phase shift is 180°).

$$f_{in} = \frac{g_{m1}}{2\pi C_c} = \frac{150 \mu A/V}{2\pi \cdot C_c} = 10 \text{ MHz} \rightarrow C_c = 2.4 \text{ pF} \quad (24.10)$$

The simulation results are seen Fig. 24.11. The unity-gain frequency, f_{in} , is close to 10 MHz. However, while the lower frequency moved downwards and the higher frequency pole moved upwards, the zero moved down to unity-gain frequency, see Eq. (21.63). This causes the open-loop gain to hover around unity instead of continuing to decrease (this is bad). The stability and step response of the op-amp will be degraded because of the zero. To illustrate this, consider the simulation results seen in Fig. 24.12. Notice that, in a transient simulation, we have to wait some time to let the bias circuit start up. Here, in this simulation, we've waited 500 ns before applying the input signal. Next, notice that our step input signal has a small amplitude change (5 mV). If we apply a larger step, the small-signal analysis used to derive pole-splitting is no longer valid (and we'll see the slew-rate limitations). Clearly the output of the op-amp doesn't behave well with the zero present. To eliminate the zero, we add the zero-nulling resistor, as seen in Fig. 21.33b. Figure 24.11 is regenerated in Fig. 24.13 with the addition of a zero-nulling resistor ($1/g_{m1} = 6.5k$). Figure 24.14 shows the well-behaved step response.

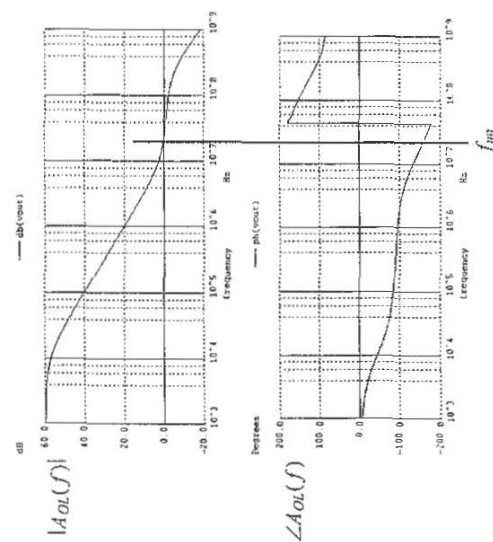


Figure 24.11 Increasing the compensation capacitor's value to 2.4 pF.

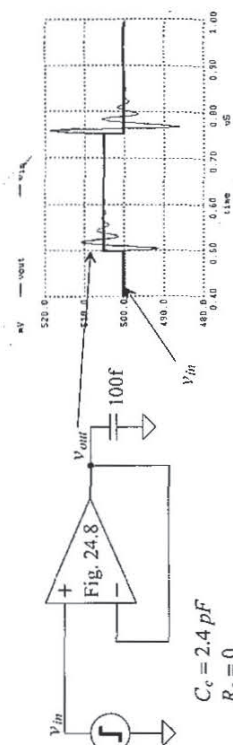


Figure 24.12 The poor step response of the op-amp with the zero present.

Gain and Phase Margins

In the previous discussions we assumed a load of 100 fF. If the load capacitance varies, the stability can (will) be affected. Further, with temperature, process, and power supply variations, the stability of the op-amp can change. In order to specify "how stable" the op-amp is at a given set of operating conditions, the parameters gain margin (GM) and phase margin (PM) are used. To determine an op-amp's PM, we look at the phase shift when the open-loop gain is unity. The amount of phase shift away from 180° is the PM of the op-amp. As seen in Fig. 24.13, the phase shift when the gain is unity is -90° . Taking the difference between this value and 180° gives a PM of 90° . To calculate the GM, we look at the difference between the open-loop gain and unity when the phase of the op-amp is $\pm 180^\circ$. For the op-amp response in Fig. 24.13, the GM is approximately 25 dB. Note that as seen in Fig. 24.14, it is nice to have a PM of 90° because the step response of the op-amp has a first-order response (like an RC circuit).

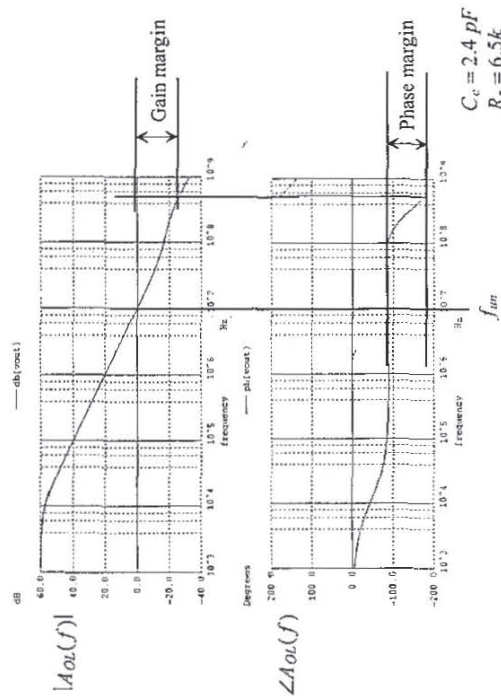


Figure 24.13 Adding a zero nulling resistor to the op-amp in Fig. 24.8.

$$C_c = 2.4 \text{ pF}$$

$$R_z = 6.5k$$

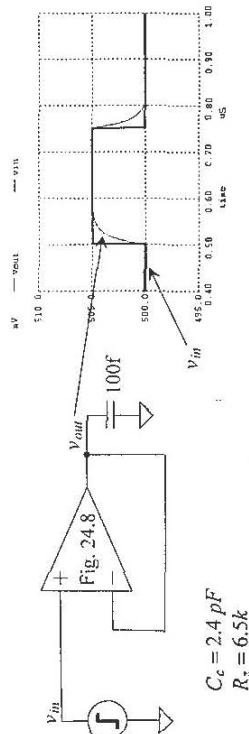


Figure 24.14 Good step response of the op-amp with the zero absent.

Removing the Zero

As the previous discussion illustrated, the RHP zero can raise issues concerning stability and settling time (this is important). As seen in Eq. (21.73) and the associated discussion, R_z can be added to eliminate ($R_z = 1/g_{m1}$) or move the zero into the LHP ($R_z > 1/g_{m1}$). When the zero is moved to the LHP, the phase response of the zero adds to the overall phase response, increasing the PM (this is called *lead compensation*). The practical problem with using R_z is that setting its value to a precise number (say $1/g_{m1}$) is challenging with shifts in process, temperature, or voltage. One solution to this problem is to replace the resistor with a MOSFET operating in the triode region, Fig. 24.15. Mz behaves like a resistor with a value of $1/g_{m1}$. Ideally, the source-gate voltage of M7 is the same as the V_{SG} of MP1. It then follows that the source-gate potential of MP2 equals the source-gate potential of Mz. The channel resistance of Mz is then, from Eq. (9.16), set to $1/g_{m1}$. The practical issues with this method are the wasted power dissipated by the additional circuitry and the fact that if the output swing becomes large (especially at higher frequencies where C_c has a small impedance), Mz can move out of the triode region, which can affect the large-signal behavior of the op-amp.

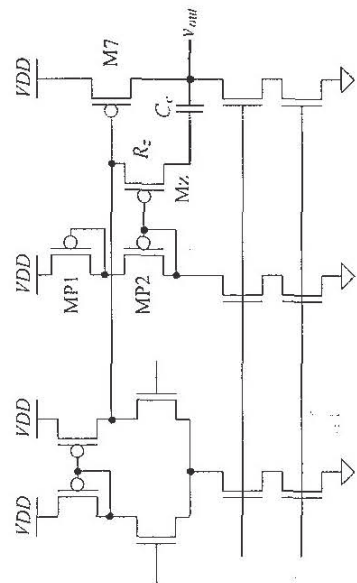


Figure 24.15 Making the zero-nulling resistor process independent.

The other method to remove the RHP zero seen in Fig. 21.33a is to add an amplifier with a gain of +1 in series with the compensation capacitor. Figure 24.16 shows the idea. A source follower allows the output signal to feed back through the compensation capacitor (so that the pole-splitting effect is still present). However, the root cause of the RHP zero, namely, C_c shorting the input of the second stage (the output of the diff-amp) to the output of the second stage (the output of the op-amp) at higher frequencies is removed. The concerns with this topology are, again, power dissipation and, perhaps more importantly, large signals. If the overall output voltage swings too low, it causes the source-follower to shut off.

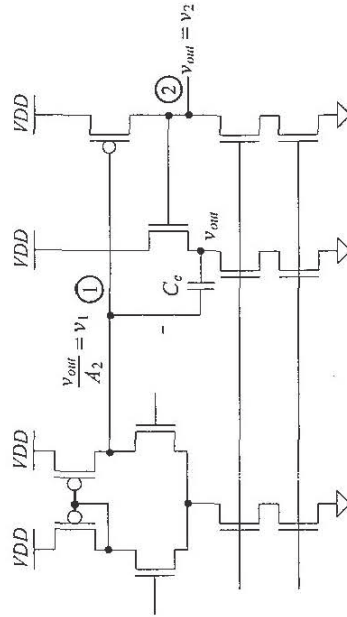


Figure 24.16 Using an amplifier to eliminate forward signal feedthrough via the compensation capacitor.

Compensation for High-Speed Operation

Notice, in Fig. 24.16 (or in any other of the topologies we've discussed up to this point), that the current fed back through C_c is

$$i_{C_c} = \frac{v_{out} - v_1}{1/j\omega C_c} \quad (24.11)$$

If the second-stage gain, A_2 ($g_{m2}R_{z2} = g_{m2}r_{o2}$), is reasonably large, then this equation can be approximated using

$$i_{C_c} \approx \frac{v_{out}}{1/j\omega C_c} \quad (24.12)$$

If we can feed back this current *indirectly* to the output of the diff-amp, we can still compensate the op-amp (and have pole-splitting). Further, if we do it correctly, we avoid connecting the compensation capacitor directly to the output of the diff-amp and thus avoid the RHP zero. Towards this goal, consider the modified op-amp schematic seen in Fig. 24.17. The added MOSFETs form a common-gate amplifier. (Note that here we are assuming $v_p \ll v_{out}$, so the source-follower action of MCG is negligible. MCG is connected to v_p to set its gate at the DC voltage of the input.) The current i_{C_c} is fed back through the common-gate MOSFET, MCG, to node 1 (the output of the diff-amp).