IN THE UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

POLARIS INNOVATIONS LIMITED., an Ireland limited company, Plaintiff, v. XILINX, INC., a Delaware corporation Defendant.	No. 1:22-cv-00174-RGA **FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

FIRST AMENDED COMPLAINT

Polaris Innovations Limited ("Polaris") files this First Amended Complaint against Xilinx, Inc. ("Xilinx"), for patent infringement as follows:

PARTIES

1. Plaintiff Polaris Innovations Limited is a corporation organized and existing under the law of Ireland, with its principal place of business at 77 Lower Camden Street, Dublin D02 XE80, Ireland.

2. Upon information and belief, Xilinx is a corporation organized and existing under the law of Delaware with its principal place of business at 2100 Logic Drive, San Jose, CA 95124.

JURISDICTION

3. This is an action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

4. This Court has personal jurisdiction over Xilinx. Xilinx is a Delaware corporation. Upon information and belief, Xilinx has committed and continues to commit acts of patent infringement, including making, selling, offering to sell, directly or through

intermediaries, subsidiaries and/or agents, infringing products within this district, including to customers in this district.

VENUE

5. Venue is proper in this Court pursuant to 28 U.S.C. § 1400 (b). Xilinx is subject to personal jurisdiction in this district, and a substantial part of the events giving rise to Polaris's claims occurred in this district.

THE ASSERTED PATENTS

6. On December 5, 2000, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,157,589 ("the '589 patent"), entitled "Dynamic semiconductor memory device and method for initializing a dynamic semiconductor memory device." A copy of the '589 patent is attached hereto as Exhibit 1.

7. The '589 patent has been assigned to Polaris. Polaris holds all right, title, and interest in the '589 Patent, including the right to collect and receive damages for past, present and future infringement of the '589 Patent.

8. On December 5, 2006, the United States Patent and Trademark office duly and legally issued United States Patent No. 7,145,369 (the "'369 patent"), which is entitled "Output Driver For An Integrated Circuit And Method For Driving An Output Driver." A true and correct copy of the '369 patent is attached hereto as Exhibit 2.

9. The '369 patent has been assigned to Polaris. Polaris holds all right, title, and interest in the '369 patent, including the right to collect and receive damages for past, present, and future infringement of the '369 patent.

10. On May 12, 2009, the United States Patent and Trademark Office duly and legally issued United States Patent No. 7,532,523 ("the '523 patent"), which is entitled "Memory Chip With Settable Termination Resistance Circuit." A true and correct copy of the '523 Patent is attached hereto as Exhibit 3.

11. The '523 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '523 Patent, including the right to collect and receive damages for past,

present and future infringement of the ’523 Patent.

12. On March 2, 2004, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,702,473, entitled “Electrical Circuit And Method For Testing A Circuit Component Of The Electrical Circuit.” A true and correct copy of the ’473 patent is attached hereto as Exhibit 4.

13. The ’473 patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the ’473 Patent, including the right to collect and receive damages for past, present and future infringement of the ’473 Patent.

XILINX’S INFRINGING PRODUCTS

14. Polaris incorporates and realleges paragraphs 1-13 above as though fully set forth herein.

15. Xilinx is the industry leader in field-programmable gate arrays (“FPGA”).

16. According to Xilinx, “Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.” https://www.xilinx.com/products/silicon-devices/fpga/what-is-an-fpga.html (Last accessed December 6, 2021).

17. Xilinx touts the wide applicability of its FPGAs, including aerospace & defense, ASIC prototyping, automotive, broadcast systems, consumer electronics, data center, high performance computing and data storage, industrial, medical, security, video and image processing, and wired and wireless communications applications.

18. Examples of Xilinx’s products include the Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, the 7-series product family, the 6-series product family, Virtex-6 and Virtex-5 product families, and the Spartan-6 product family.

19. Xilinx’s system on a chip (“SoC”) products, such as the Zynq Ultrascale+

MPSoC, Zynq-7000 SoC, and the UltraScale product family incorporate memory controllers as part of its memory interface solution, depicted below:

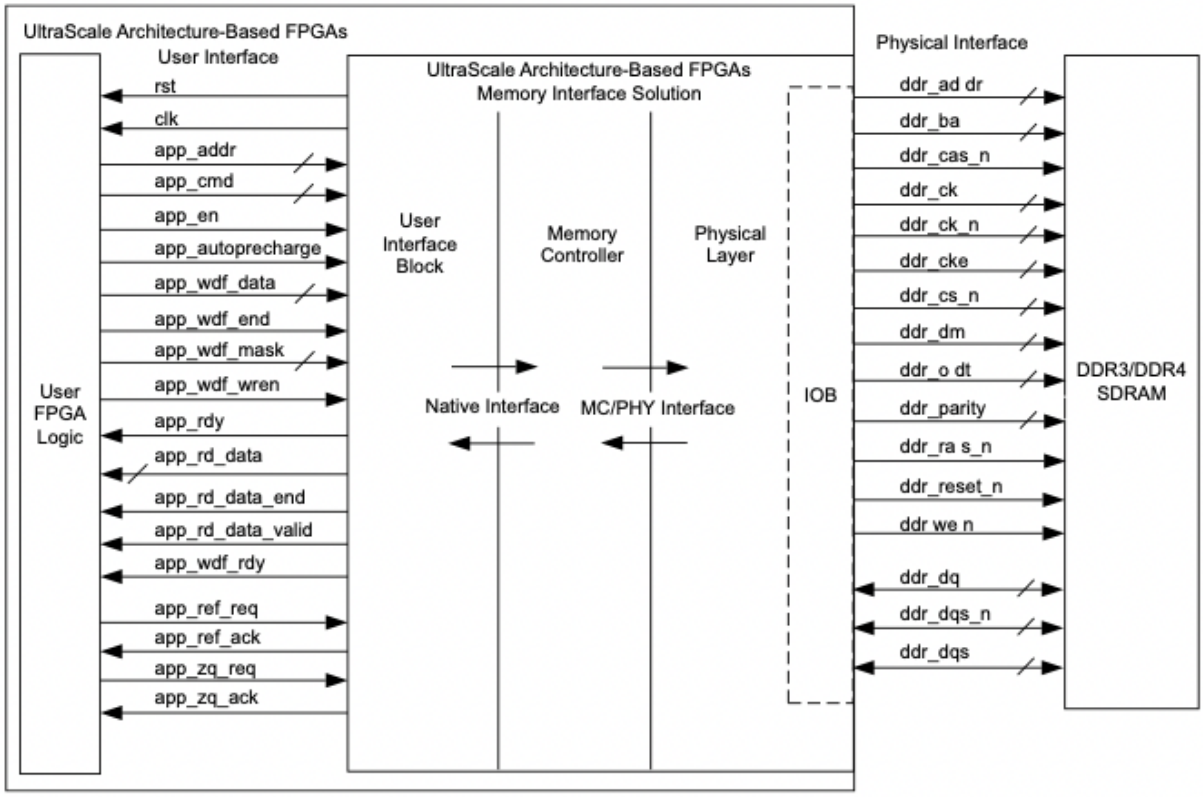
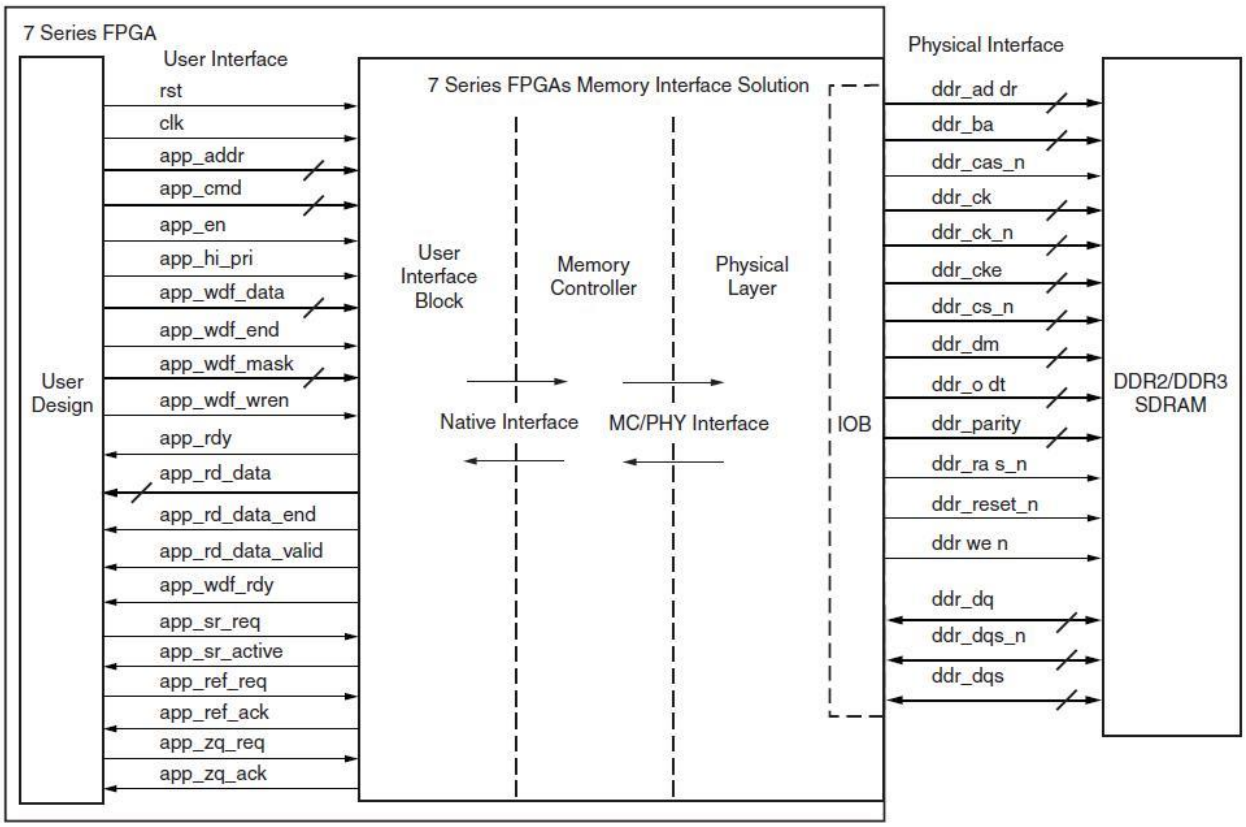


Figure 1-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution**

20. Users, including Xilinx and its customers, can program other products, such as the 7-series product family, the 6-series product family, Virtex-6 and Virtex-5 product families, and the Spartan-6 product family, to implement memory interface solutions between the FPGA and external DRAM, such as by using Xilinx's Memory Interface Generator tool, or other design tools provided by Xilinx.

21. In addition to its FPGA devices, Xilinx provides "advanced software" and "configurable, ready-to-use IP cores," that is, an off-the-shelf design for each such application of its FPGA devices. These tools allow the user to design, program, simulate, and test the desired configuration for the FPGA. As part of its design software, Xilinx provides a tool called the Memory Interface Generator that generates memory controllers compatible with DDR3, DDR3L, or DDR4 DRAM to be implemented in the FPGA. Xilinx also provides evaluation

boards and kits that allow potential customers and users to evaluate its FPGA products. The 7-series memory interface solution is depicted below:



COUNT I

(Infringement of U.S. Patent 6,157,589)

22. Polaris incorporates and realleges paragraphs 1-21 above as though fully set forth herein.

23. On information and belief, up until the expiration of the ’589 patent, Xilinx willfully infringed one or more claims of the ’589 patent, including, but not limited to, claims 11, 12, and 13 of the ’589 patent literally, or under the doctrine of equivalents, by using in the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L, and DDR4 memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family (collectively, “‘589 patent Infringing Products”). The ’589 patent Infringing Products perform the claimed methods for initializing a dynamic semiconductor memory device.

24. On information and belief, when Xilinx, its customers, and other third parties turn on the 589 Patent Infringing Products, their memory controllers supply, via an initialization circuit located in the physical layer of the memory controller, a supply voltage stable signal (for example, the ddr_reset_n or *RESET#* signal,) once a supply voltage has been stabilized (for example, at the time between Ta and the assertion of the RESET# signal) after the switching-on operation of the dynamic semiconductor memory device (for example, in the "Reset Procedure" state which follows the "Power ON" state, and *RESET#* must be HIGH during normal operation). The memory controller also supplies, via an enable circuit of the initialization circuit, located in the physical layer of the memory controller, an enable signal (for example, the Clock Enable signals ddr_cke, CKE, CKE0, or CKE1, which active internal clock signals, device input buffers, and output drivers when HIGH), the initialization circuit receiving the supply voltage stable signal (for example, the memory controller receives the *RESET#* signal) and further command signals (for example, the "MRS" signals) externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals (for example ZQ Calibration commands) the enable signal being generated and effecting an unlatching of a control circuit (for example, as indicated by the generation of the VALID signals generated on the CKE, COMMAND, CA, and ODT lines).

25. On information and belief, the controller provides at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals (for example, the MRS command, which acts both as a preparation command signal and as a loading configuration register command signal.)

26. On information and belief, the controller maintains a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit (for example, as seen in the state of the RTT line during the switching-on operation).

27. On information and belief, Xilinx induced infringement of one or more claims of the 589 Patent, including, but not limited to, Claims 11, 12, and 13, pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to perform the claimed method for initializing a dynamic semiconductor memory device. This performance of the claimed method for initializing a dynamic semiconductor memory device, constitutes infringement, literally or under the doctrine of equivalents, of one or more claims of the ’589 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the 589 Patent Infringing Products and intending its customers to use the 589 Patent Infringing Products with hardware, software, and other infrastructure, such as test boards, development kits, and design tools, that enable and/or make use of these products; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

28. Xilinx proceeded in this manner despite its actual knowledge of the ’589 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’589 patent at least as of October 25, 2016 when Polaris placed Xilinx on notice of infringement of the ’589 patent and identified Xilinx’s infringing products. At the very least, because Xilinx was on notice of the ’589 patent and the accused infringement, it was willfully blind regarding the infringement it induced.

29. On information and belief, Xilinx contributed to infringement of one or more claims of the ’589 patent, including, but not limited to, Claims 11, 12, and 13, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components of systems that perform the claimed methods for initializing a dynamic semiconductor memory device, including without limitation the 589 Patent Infringing Products. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. When, for example, these products are installed in an embedded system, such as Automotive Driver Assistant System applications used by Xilinx’s customers (including Mercedes-Benz, BMW, Nissan, VW, Honda, Ford, Chrysler, Toyota, Mazda, Acura, Subaru and Audi), and used, the claimed dynamic semiconductor

memory device is used, and/or the claimed methods performed, thereby infringing, literally or under the doctrine of equivalents, one or more claims of the '589 patent. Xilinx supplied these components, including without limitation the '589 patent Infringing Products, with the knowledge of the '589 patent and with the knowledge that these components constitute material parts of the claimed inventions of the '589 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the '589 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components, because the 589 Patent Infringing Products must perform the infringing reset and initialization sequence when powered on.

30. Polaris has suffered damages as a result of Xilinx's infringement of the '589 patent.

31. Up until the expiration of the '589 patent, Xilinx's infringement of the '589 patent was willful, deliberate, and in disregard of Polaris's patent rights. At least as of October 25, 2016, when Polaris placed Xilinx on notice of infringement of the '589 patent and identified Xilinx's infringing products, Xilinx had actual knowledge of infringement of the '589 patent and proceeded to infringe the '589 patent with full and complete knowledge of that patent and its applicability to Xilinx's products without taking a license under the '589 patent. Despite knowledge of the '589 patent, Xilinx acted despite an objectively high likelihood that its actions constituted patent infringement. This objective risk was known to Xilinx, and should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT II

(Infringement of U.S. Patent 7,145,369)

32. Polaris incorporates and realleges paragraphs 1-31 above as though fully set forth herein.

33. On information and belief, Xilinx has willfully infringed and continues to

willfully infringe one or more claims of the '369 patent, including, but not limited to, claim 2, literally, or under the doctrine of equivalents, by making, selling, using, offering for sale, and/or importing into the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family, and the Virtex-6 and Virtex-5 product families (collectively, "369 Patent Infringing Products"). Each 369 Patent Infringing Product meets each and every limitation of at least claim 2 of the '369 patent.

34. On information and belief, each 369 Patent Infringing Product is an integrated circuit that contains an output driver for driving an integrated circuit. The output driver of each 369 Patent Infringing Product includes a driver circuit, for example, the VRN and VRP circuits, as described in page 60 of the Xilinx Zynq-7000 All Programmable SoC Technical Reference Manual, that drive an input signal of the output driver onto an output line, for example, the outputs from VRN and VRP.

35. On information and belief, each 369 Patent Infringing Product contains a measuring circuit, for example, the VRN and VRP circuits, for measuring at least one of an output line current and an output line potential, for example, the potential of the outputs from the VRN and VRP circuits.

36. On information and belief, each 369 Patent Infringing Product contains a control unit, for example, the DCI state machine, providing a control signal, for example, through the DCI state machine's control of the drive strength of the 369 Patent Infringing Products' DDR Input Output Block ("IOB"), for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification- prescribed potential range and a specification-prescribed current range, for example, the power range and potential range as described in page 309 of the Xilinx Zynq-7000 All Programmable SoC Technical Reference Manual. The control unit includes a feedback control to affect the driver strength based on a measured value provided by the measuring circuit,

for example, by adjusting VRN relative to VREF based on the measuring value provided by the measuring circuit.

37. On information and belief, the desired power range of the output driver of the 369 Patent Infringing Products is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value, for example, VREF, and a specification prescribed lower potential limit value adjusted with the tolerance magnitude, for example, VRN adjusted relative to VREF.

38. On information and belief, Xilinx has induced and continues to induce infringement of one or more claims of the ’369 patent, including, but not limited to, claim 2 pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to install 369 Patent Infringing Products on their products in accordance with Xilinx’s specifications and instructions. This infringes, literally or under the doctrine of equivalents, of one or more claims of the ’369 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the 369 Patent Infringing Products and intending its customers to use the 369 Patent Infringing Products with hardware, software, and other infrastructure, such as test boards, development kits, and design tools, or Xilinx’s customers’ embedded systems, such as Automotive Driver Assistant System applications in Mercedes-Benz, BMW, Nissan, VW, Honda, Ford, Chrysler, Toyota, Mazda, Acura, Subaru and Audi automobiles, that enable and/or make use of these products; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

39. Xilinx proceeded in this manner despite its actual knowledge of the ’369 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’369 patent at least as of October 25, 2016 when Polaris placed Xilinx on notice of infringement of the ’369 patent and identified Xilinx’s infringing products. At the very least, because Xilinx has been and remains on notice of the ’369 patent and the accused infringement, it has been and remains willfully blind regarding the

infringement it has induced and continues to induce.

40. On information and belief, Xilinx has contributed to and continues to contribute to infringement of one or more claims of the ’369 patent, including, but not limited to, claim 2, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components of the claimed output driver for an integrated circuit, including without limitation the 369 Patent Infringing Products. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. When, for example, these products are installed in an embedded system with terminating resistors in accordance with Xilinx’s specification, the resulting system infringes, literally or under the doctrine of equivalents, one or more claims of the ’369 patent. Xilinx supplied and continues to supply these components, including without limitation the 369 Patent Infringing Products, with the knowledge of the ’369 patent and with the knowledge that these components constitute material parts of the claimed inventions of the ’369 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the ’369 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

41. Polaris has suffered damages as a result of Xilinx’s infringement of the ’369 patent.

42. Xilinx’s infringement of the ’369 patent has been and continues to be willful, deliberate, and in disregard of Polaris’s patent rights. At least as of October 25, 2016, when Polaris placed Xilinx on notice of infringement of the ’369 patent and identified Xilinx’s infringing products, Xilinx has had actual knowledge of infringement of the ’369 patent and has proceeded to infringe the ’369 patent with full and complete knowledge of that patent and its applicability to Xilinx’s products without taking a license under the ’369 patent. Despite knowledge of the ’369 patent, Xilinx has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Xilinx, and is also so obvious that it should have been known to Xilinx. Such willful and

deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT III

(Infringement of U.S. Patent 7,532,523)

43. Polaris incorporates and realleges paragraphs 1-42 above as though fully set forth herein.

44. On information and belief, Xilinx has willfully infringed and continues to willfully infringe one or more claims of the '523 patent, including, but not limited to, claims 5 and 6, literally, or under the doctrine of equivalents, by making, selling, using, offering for sale, and/or importing into the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family, and the Virtex-6 and Spartan-6 product families (collectively, "523 Patent Infringing Products"). Each 523 Patent Infringing Product, when installed on a board with DDR3 SDRAM, ("523 Patent Infringing System"), meets each and every limitation of at least claims 5 and 6 of the '523 patent. Examples of 523 Patent Infringing Systems include Xilinx's evaluation boards, and Xilinx's customer's embedded systems, such as the advanced driver assistance systems ("ADAS") used in Mercedes-Benz, BMW, Nissan, VW, Honda, Ford, Chrysler, Toyota, Mazda, Acura, Subaru and Audi automobiles.

45. On information and belief, each 523 Patent Infringing System contains a memory controller having a terminal, for example, the memory controllers of the 523 Patent Infringing Products.

46. On information and belief, each 523 Patent Infringing System contains a plurality of memory chips, for example, its DDR3 SDRAM.

47. On information and belief, each 523 Patent Infringing System contains a termination circuit, for example the RTT pullups and pulldowns of the on-die termination circuits, connectable with the terminal and configured to terminate the terminal according to a

settable resistance value, for example, RZQ/4, RZQ/2, or RZQ/6.

48. On information and belief, each 523 Patent Infringing System contains a control command port for receiving a control command signal for affecting accessibility of the memory chip, for example, the RAS#, CAS#, and WE# command inputs and Mode Register MR1 values.

49. On information and belief, each 523 Patent Infringing System contains a control circuit connected to the termination circuit, for example the "other circuitry like RCV, …" in Fig. 101 of the JEDEC DDR3 SDRAM standard, July 2012, and configured to set the resistance value as a function of the received control command signal, for example by setting the resistance value to "Rtt_Nom disabled, RZQ/4, RZQ/2, RZQ/6 in Mode Register 1.

50. On information and belief, each 523 Patent Infringing System contains a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller, for example, the memory bus between the 523 Patent Infringing Product and the DDR3 SDRAM as depicted in Figure 1-51 of the Xilinx "Zynq-7000 AP SoC and 7 Series Device Memory Interface Solutions v.3.0 User Guide" on page 89.

51. On information and belief, each 523 Patent Infringing System contains a termination port to receive a termination signal, for example ddr_odt, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value, e.g., RTT_NOM, in response to the termination signal.

52. On information and belief, the control circuit, as a function of the termination signal ODT, (1) selectively terminates the terminal with the set resistance value RTT_NOM after a first time delay, for example, ODTLon = CWL + AL - 2, or (2) does not terminate the terminal in accordance with a second time delay, for example, ODTLoff = CWL + AL -2. On information and belief, the first time delay is sufficient to set the resistance value, for example, as indicated by the assertion of RTT_NOM after the first time delay ODTLon.

53. On information and belief, the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second

predetermined switchover time. For example, as seen in the timing diagram below, the resistance value is set to a first resistance value (RTT_WR) after a first predetermined switchover time (ODTLon), and is set to a second resistance value (RTT_NOM) after a second predetermined switchover time (e.g., ODTLcwn4, ODTLcwn8).

54. On information and belief, Xilinx has induced and continues to induce infringement of one or more claims of the ’523 patent, including, but not limited to, claims 5 and 6 pursuant to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to install 523 Patent Infringing Products on their products, or to make, use, sell, offer for sale, or import 523 Patent Infringing Systems using 523 Patent Infringing Products in accordance with Xilinx’s specifications and instructions. This infringes, literally or under the doctrine of equivalents, of one or more claims of the ’523 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the 523 Patent Infringing Products and intending its customers to use the 523 Patent Infringing Products with hardware, software, and other infrastructure that enable and/or make use of these products; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

55. Xilinx proceeded in this manner despite its actual knowledge of the ’523 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’523 patent at least as of December 7, 2016 when Polaris placed Xilinx on notice of infringement of the ’523 patent and identified Xilinx’s infringing products. At the very least, because Xilinx has been and remains on notice of the ’523 patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

56. On information and belief, Xilinx has contributed to and continues to contribute to infringement of one or more claims of the ’523 patent, including, but not limited to, claims 5 and 6, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components of 523 Patent Infringing Systems,

including without limitation the 523 Patent Infringing Products. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. For example, as detailed above, the 523 Patent Infringing Systems infringe, literally or under the doctrine of equivalents, one or more claims of the '523 patent. Xilinx supplied and continues to supply these components, including without limitation the 523 Patent Infringing Products, with the knowledge of the '523 patent and with the knowledge that the 523 Patent Infringing Products constitute material parts of the claimed inventions of the '523 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the '523 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

57. Polaris has suffered damages as a result of Xilinx's infringement of the '523 patent.

58. Xilinx's infringement of the '523 patent has been and continues to be willful, deliberate, and in disregard of Polaris's patent rights. At least as of December 7, 2016, when Polaris placed Xilinx on notice of infringement of the '523 patent and identified Xilinx's infringing products, Xilinx has had actual knowledge of infringement of the '523 patent and has proceeded to infringe the '523 patent with full and complete knowledge of that patent and its applicability to Xilinx's products without taking a license under the '523 patent. Despite knowledge of the '523 patent, Xilinx has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Xilinx, and is also so obvious that it should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT IV

(Infringement of U.S. Patent No. 6,701,473)

59. Polaris incorporates and realleges paragraphs 1-58 as though fully set forth herein.

60. On information and belief, Xilinx has willfully infringed and continues to

willfully infringe one or more claims of the '473 patent, including, but not limited to, claims 20, 26, 27, and 28 of the '473 patent literally, or under the doctrine of equivalents, by using in the United States without authority, products containing a Dynamic Memory Interface compatible with DDR3, DDR3L, and DDR4 memory, including but not limited to Zynq Ultrascale+ MPSoC, Zynq-7000 SoC, the UltraScale product family, and the 7-series product family (collectively, "473 Patent Infringing Products"). The 473 Patent Infringing Products, when coupled with DDR3 SDRAM ("473 Patent Infringing Systems"), perform the claimed methods for testing a circuit component which is connected to other circuit components via a bus. Examples of 473 Patent Infringing Systems include Xilinx's evaluation boards, and Xilinx's customer's embedded systems, such as the advanced driver assistance systems ("ADAS") of Mercedes-Benz, BMW, Nissan, VW, Honda, Ford, Chrysler, Toyota, Mazda, Acura, Subaru and Audi.

61. On information and belief, when Xilinx, its customers, and other third parties turn on the 473 Patent Infringing Systems, they provide a plurality of circuit components that are connected to a bus, for example, the 473 Patent Infringing Products connected to the DDR3 SDRAM via the memory bus of the physical interface.

62. On information and belief, the 473 Patent Infringing Systems configure at least one of the plurality of circuit components, for example, one of the DDR3 SDRAM, such that it can be tested independently, for example, using the write leveling feature of DDR3 SDRAM, from all others of said plurality of circuit components, for example, the other DDR3 SDRAM of the 473 Patent Infringing System, the at least one of the plurality of circuit components defining a circuit component to be tested, for example, the DDR3 SDRAM that is to be undergoing the write leveling procedure.

63. On information and belief, while the 473 Patent Infringing Systems, while testing their DDR3 SDRAM, perform an operation, namely, write leveling, with the circuit component to be tested, the operation selected the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal

operation, for example, outputting data through the DQ feedback line as depicted in Fig. 1-63 of the Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide.

64. On information and belief, the 473 Patent Infringing Systems signal a bus control device which controls the bus that the circuit component to be tested is undergoing a test, for example, the write_calib_n signal indicating the start of the write leveling mode.

65. On information and belief, the 473 Patent Infringing Systems use the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated, for example, after ODT is asserted, by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components, for example, the other DDR3 SDRAMs of the 473 Patent Infringing Systems.

66. On information and belief, the 473 Patent Infringing Systems, during write leveling mode, output data to the bus that is other than the data which would be output to the bus during normal operation, and outputs infrequently changing data, for example, outputting infrequently changing data on the DQ Feedback line as depicted in Fig. 1-63 of the Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide.

67. On information and belief, Xilinx has induced and continues to induce infringement of one or more claims of the ’473 patent, including, but not limited to, claims 20, 26, 27, and 28 to 35 U.S.C. § 271(b), by encouraging its customers and other third parties to perform the claimed method for testing a circuit component which is connected to other circuit components via a bus. This infringes, literally or under the doctrine of equivalents, of one or more claims of the ’473 patent by such customers or third parties. Xilinx’s acts of inducement include: providing its customers with the 473 Patent Infringing Products and intending its customers to use the 473 Patent Infringing Products with hardware, software, and other infrastructure, such as test boards, development kits, and design tools, or Xilinx’s customers’ embedded systems, such as Automotive Driver Assistant System applications in Mercedes-Benz, BMW, Nissan, VW, Honda, Ford, Chrysler, Toyota, Mazda, Acura, Subaru and Audi

automobiles, that enable and/or make use of these products, such as the 473 Patent Infringing Systems; advertising these products through its own and third-party websites; and providing instructions on how to use these products.

68. Xilinx proceeded in this manner despite its actual knowledge of the ’473 patent and its knowledge that the specific actions it actively induced on the part of its customers and other third parties constitute infringement of the ’473 patent at least as of December 7, 2016 when Polaris placed Xilinx on notice of infringement of the ’473 patent and identified Xilinx’s infringing products. At the very least, because Xilinx has been and remains on notice of the ’473 patent and the accused infringement, it has been and remains willfully blind regarding the infringement it has induced and continues to induce.

69. On information and belief, Xilinx has contributed to and continues to contribute to infringement of one or more claims of the ’473 patent, including, but not limited to, claims 20, 26, 27, and 28, pursuant to 35 U.S.C. § 271(c) by, without authority, selling and/or offering to sell within the United States, importing, and/or supplying components, such as the 473 Patent Infringing Products, of systems, such as the 473 Patent Infringing Systems, that perform the claimed methods for testing a circuit component which is connected to other circuit components via bus. These components supplied by Xilinx are key components in automotive, defense, aerospace, and networking applications. For example, as detailed above, the 473 Patent Infringing Systems perform the claimed methods and infringe, literally or under the doctrine of equivalents, one or more claims of the ’473 patent. Xilinx supplied and continues to supply these components, including without limitation the 473 Patent Infringing Products, with the knowledge of the ’473 patent and with the knowledge that the 473 Patent Infringing Products constitute material parts of the claimed inventions of the ’473 patent. Xilinx knows that these components are especially made and/or especially adapted for use as claimed in the ’473 patent. Further, Xilinx knows that there is no substantial non-infringing use of these components.

70. Polaris has suffered damages as a result of Xilinx’s infringement of the ’473 patent.

71. Xilinx's infringement of the '473 patent has been and continues to be willful, deliberate, and in disregard of Polaris's patent rights. At least as of December 7, 2016, when Polaris placed Xilinx on notice of infringement of the '473 patent and identified Xilinx's infringing products, Xilinx has had actual knowledge of infringement of the '473 patent and has proceeded to infringe the '473 patent with full and complete knowledge of that patent and its applicability to Xilinx's products without taking a license under the '473 patent. Despite knowledge of the '473 patent, Xilinx has acted and is acting despite an objectively high likelihood that its actions constitute patent infringement. This objective risk was and is known to Xilinx, and is also so obvious that it should have been known to Xilinx. Such willful and deliberate conduct entitles Polaris to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

Polaris respectfully prays for relief as follows:

a. A judgment that Xilinx has infringed and continues to infringe one or more claims of the Asserted Patents;

b. A judgment that Xilinx has willfully infringed one or more claims of the Asserted Patents;

c. A judgment awarding Polaris all damages adequate to compensate for Xilinx's infringement, and in no event less than a reasonable royalty for its acts of infringement, including all pre-judgment and post-judgment interest at the maximum rate allowed by law;

d. A judgment awarding Polaris treble damages pursuant to 35 U.S.C. § 284 as a result of Xilinx's willful conduct;

e. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding Polaris its reasonable attorney's fees and costs; and

f. A judgment awarding Polaris such other relief as the Court may deem just and

equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Polaris demands a trial by jury on all issues so triable.

Dated: April 28, 2022

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Polaris Innovations Limited

EXHIBIT 1

US006157589A

United States Patent [19]

Krause

[11] **Patent Number: 6,157,589**

[45] **Date of Patent: Dec. 5, 2000**

[54] **DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE**

[75] Inventor: **Gunnar Krause**, Munich, Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Munich, Germany

[21] Appl. No.: **09/343,431**

[22] Filed: **Jun. 30, 1999**

[30] **Foreign Application Priority Data**

Jun. 30, 1998 [DE] Germany 198 29 287

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/226**; 365/228

[58] **Field of Search** 365/226, 227, 365/228

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Primary Examiner—Vu A. Le

Attorney, Agent, or Firm—Herbert L. Lerner; Laurence A. Greenber; Werner H. Stemer

[57] **ABSTRACT**

A dynamic semiconductor memory device of a random access type has an initialization circuit that controls the switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal once the supply voltage has been stabilized after the switching-on of the semiconductor memory device. The initialization circuit has an enable circuit that receives the supply voltage stable signal and further command signals externally applied to the semiconductor memory device. The enable circuit supplies an enable signal after a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is identified. The enable signal effects the unlatching of a control circuit provided for the proper operation of the semiconductor memory device.

13 Claims, 3 Drawing Sheets

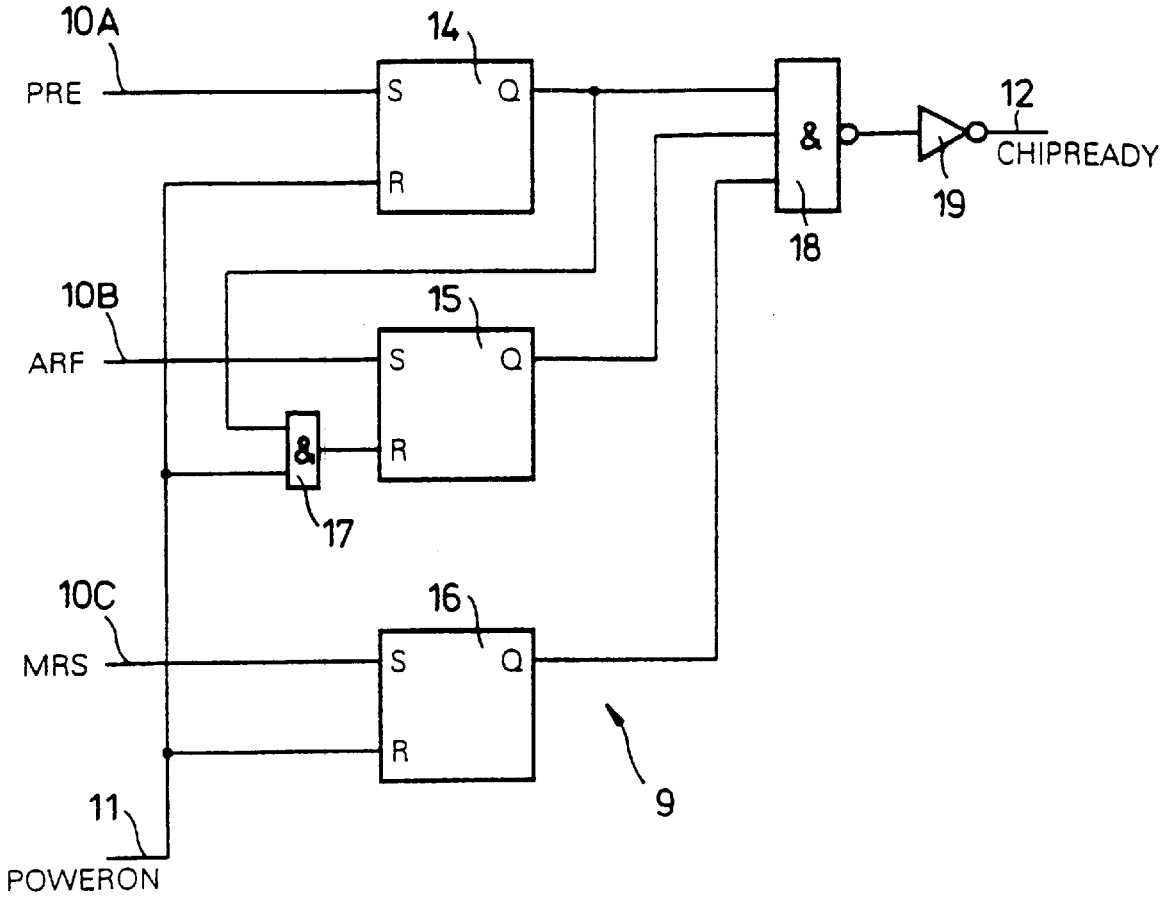
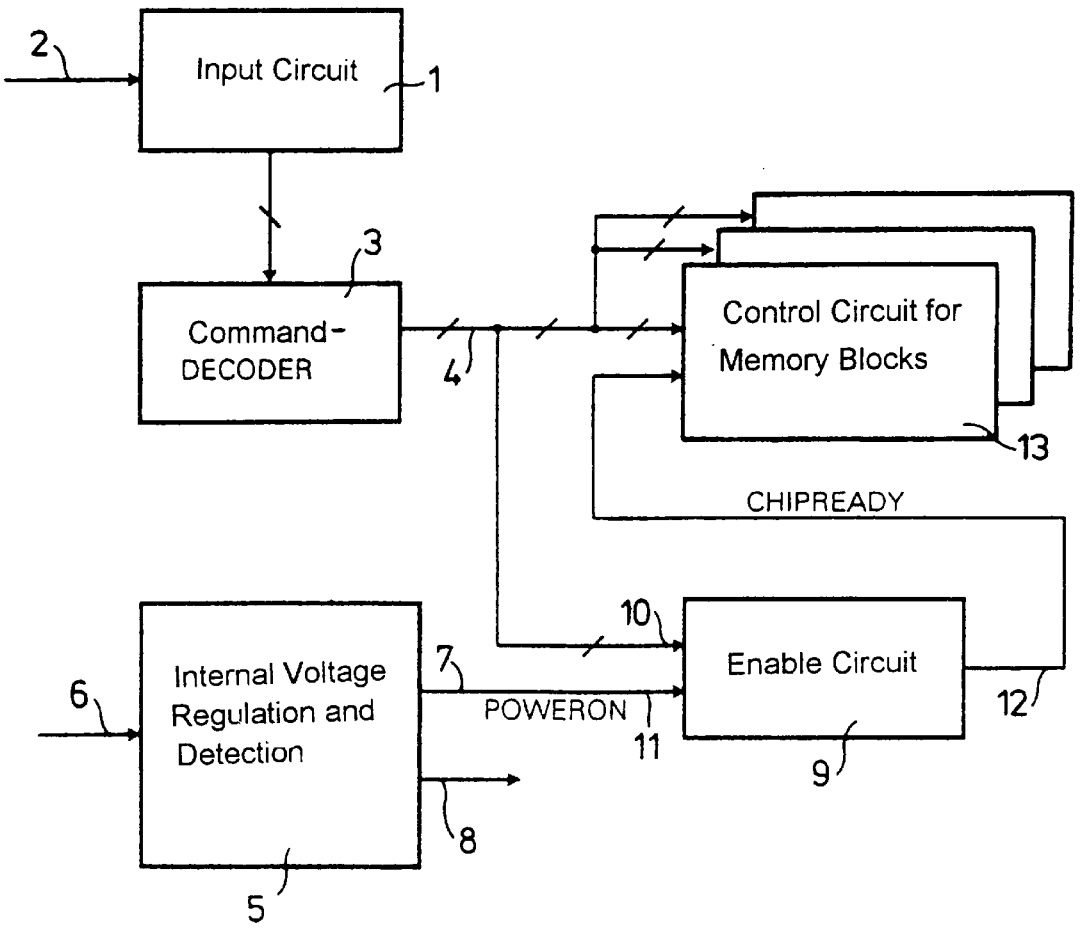


Fig 1


2
Input Circuit
1
3
Command-
DECODER
4
Control Circuit for
Memory Blocks
13
CHIPREADY
10
Enable Circuit
12
9
7
POWERON
11
6
Internal Voltage
Regulation and
Detection
8
5

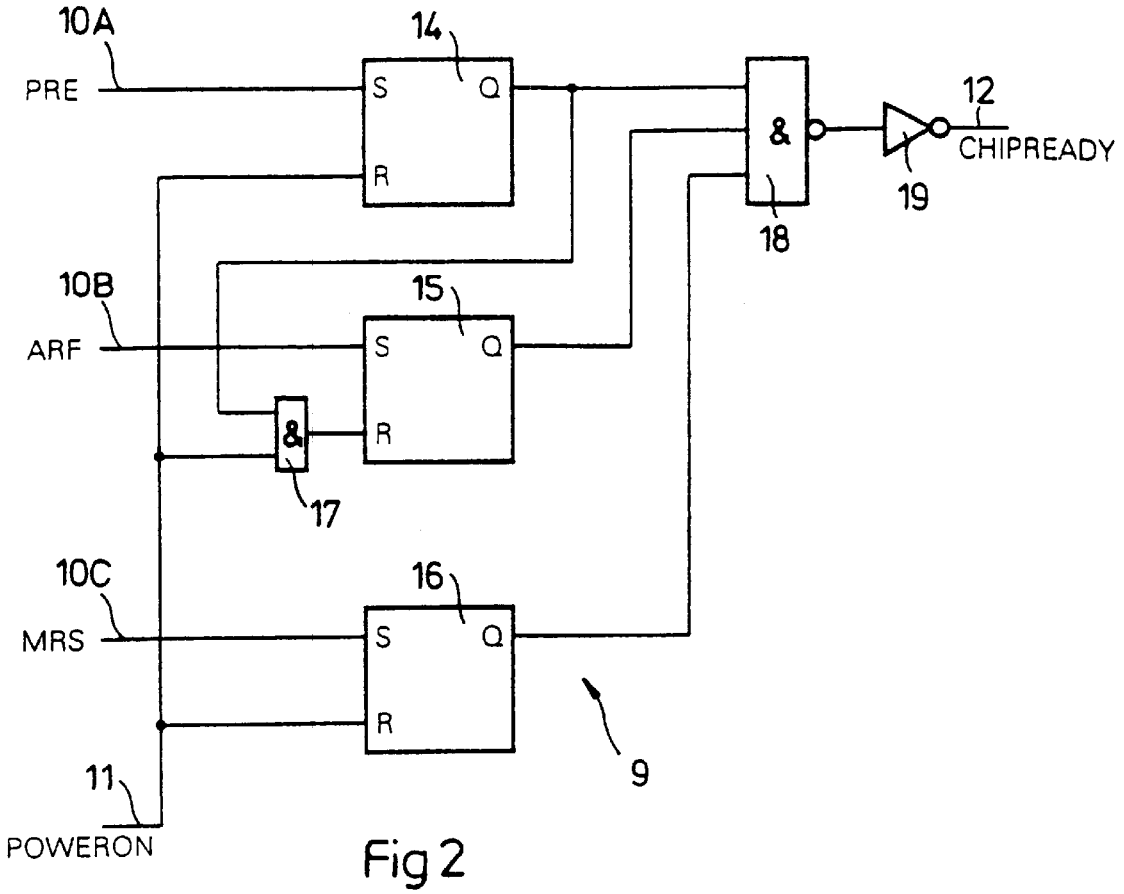

10A
PRE
14
S
Q
R
&
12
CHIPREADY
19
18
10B
ARF
15
S
Q
R
&
17
10C
MRS
16
S
Q
R
9
11
POWERON

Fig 2

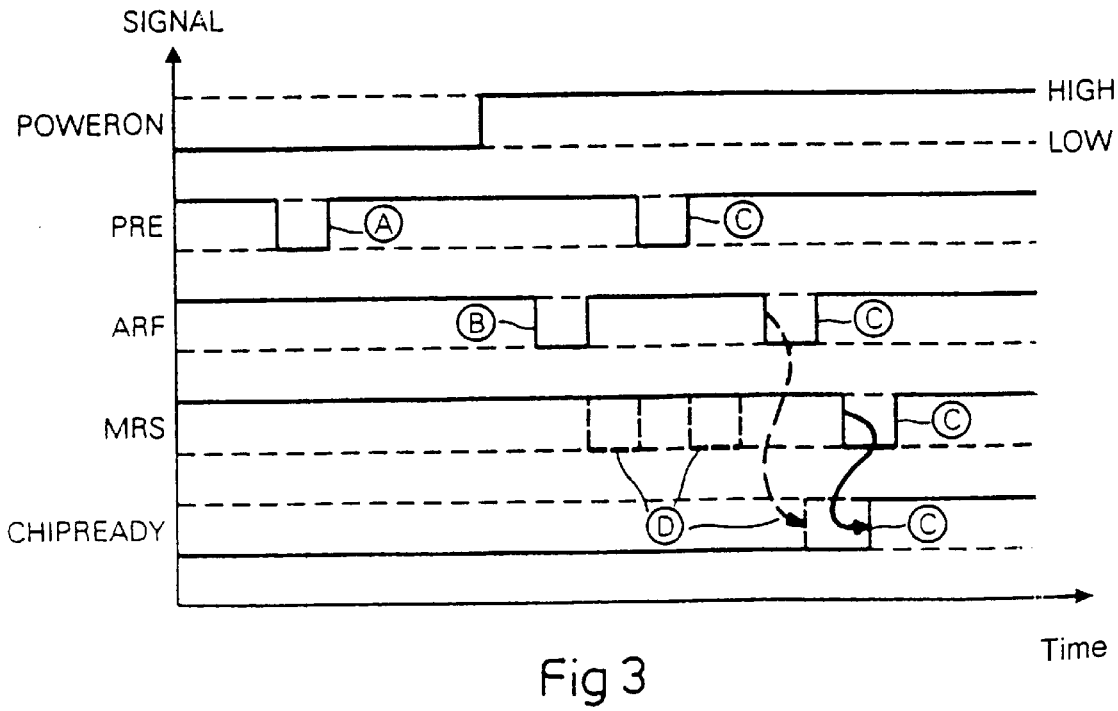

SIGNAL
POWERON
HIGH
LOW
PRE
A
C
ARF
B
C
MRS
C
CHIPREADY
D
C
Time

Fig 3

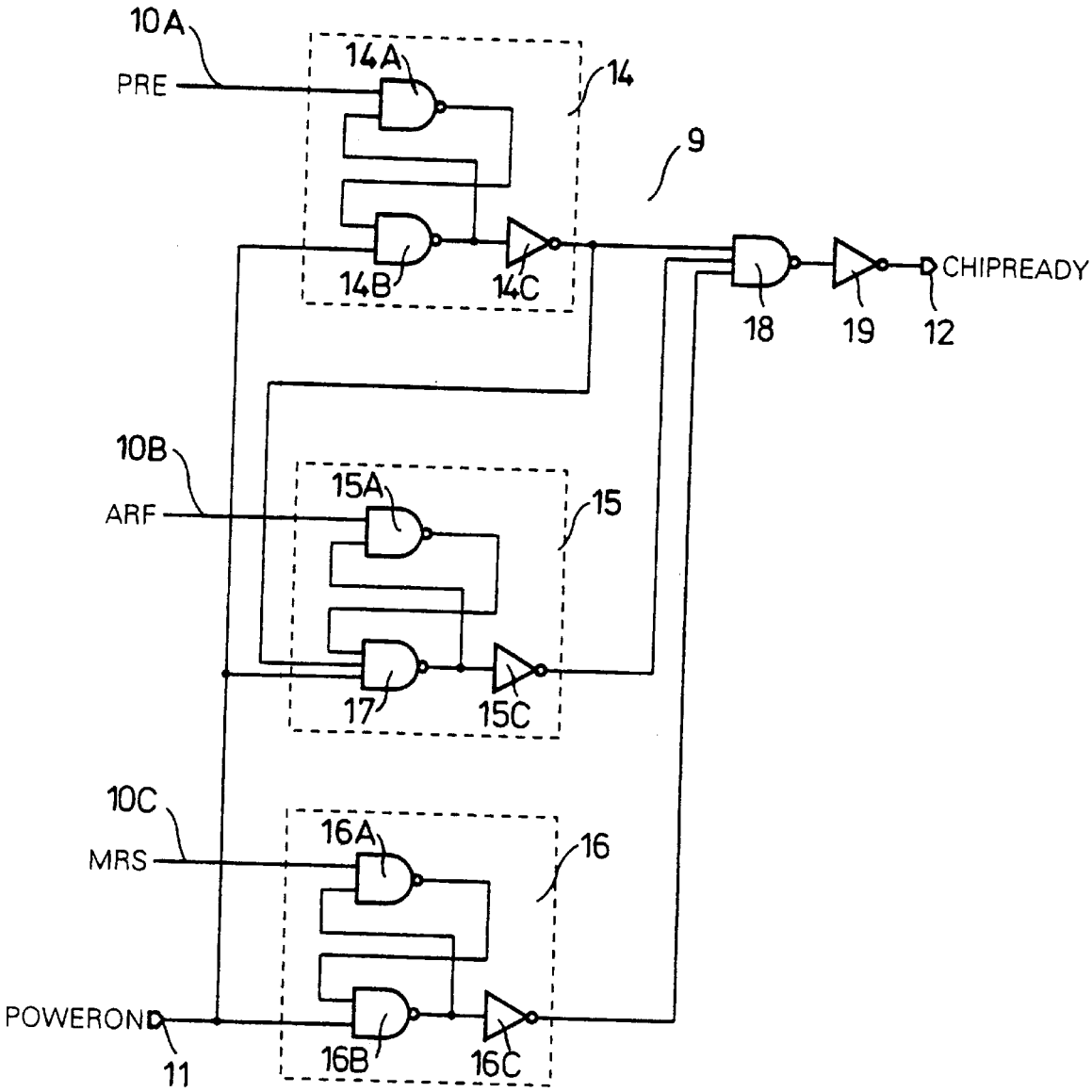

10A
PRE
14A
14
9
14B
14C
18
19
CHIPREADY
12
10B
ARF
15A
15
17
15C
10C
MRS
16A
16
POWERON
11
16B
16C

Fig 4

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on of the semiconductor memory device. The invention also relates to a method for initializing such a dynamic semiconductor memory device, and also to the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device.

In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data contention") or uncontrolled activation of internal current loads. The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory. According to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence. The sequence consists of predetermined commands that must be applied in a defined chronological order. However, a series of functions and commands which are allowed during proper operation of the component are desired or allowed chronologically only after the initialization sequence. According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called "POWERON-SEQUENCE") is provided as follows:

a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component;

b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us;

c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device;

4. the activation of eight or more refresh commands (AUTOREFRESH); and

5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.

After the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation. In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only

with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, which is as simple as possible in structural terms and which effectively prevents the risk of a short circuit of the data lines and/or of uncontrolled activation of internal current loads.

With the foregoing and other objects in view there is provided, in accordance with the invention, a dynamic semiconductor memory device of a random access type, containing an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. The initialization circuit has a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals. The enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals are identified and the enable signal effecting an unlatching of the control circuit.

The invention provides for the initialization circuit to have an enable circuit, which receives the supply voltage stable signal and the externally applied further command signals. The enable circuit generates the enable signal after the identification of the predetermined proper initialization sequence of the command signals is achieved. The enable signal effects the unlatching of the control circuit provided for the proper operation of the semiconductor memory device.

Following the principle of the invention, the enable signal (CHIPREADY) is generated and becomes active in dependence on further internal signals and the initialization sequence and then unlatches predetermined circuits. The predetermined circuits remain latched until the end of the predetermined initialization sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.

According to the preferred application in SDRAM memory devices according to the JEDEC standard, it is provided that the command signals, externally applied to the semiconductor memory device, of the initialization sequence are to be identified by the enable circuit. The command signals include a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).

According to an advantageous structural refinement of the initialization circuit according to the invention, it is provided that the enable circuit has at least one bistable multivibrator stage with a set input which receives the command signal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET). The bistable multivibrator also has a reset input to which the supply voltage stable signal (POWERON), a signal derived therefrom, or a linked signal is applied. The bistable multivibrator further has an output at which the enable signal (CHIPREADY) is outputted.

In particular, the enable circuit has a plurality of bistable multivibrator stages respectively receiving the command signals.

In an expedient refinement of the invention, it is provided that the output of at least one of the bistable multivibrator stages is passed to a reset input of a further multivibrator stage. In this case, it may furthermore be provided that, in one of the bistable multivibrator stages, the supply voltage stable signal (POWERON) and the signal output from the output of the further multivibrator stage are passed, after having been logically combined by a gate, to the reset input of the multivibrator stage.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic, block diagram of components of an initialization circuit which controls a switching-on operation of a semiconductor memory and its circuit components according to the invention;

FIG. **2** is circuit diagram of an enable circuit that supplies an enable signal (CHIPREADY);

FIG. **3** is a time sequence diagram for elucidating a method of operation of the circuit according to FIG. **2**; and

FIG. **4** is a circuit diagram of the enable circuit according to an exemplary embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to FIG. **1** thereof, there are shown circuit components, important for understanding the invention, of an SDRAM memory device operating according to the JEDEC standard. The circuit components include an initialization circuit controlling a switching-on operation of the SDRAM memory device and its circuit components. The initialization circuit has an input circuit **1**, to whose input **2** command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder **3** connected downstream of the input circuit **1** and at whose output **4**, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output. The initialization circuit further has a circuit **5** for internal voltage regulation and/or detection, at whose input **6** the external supply voltages that are externally applied to the semiconductor memory externally are fed in. The circuit **5** has a first output **7** outputting a POWERON signal and a second output **8** supplying stabilized internal supply voltages. The method of operation and the structure of the circuits **1**, **3** and **5** are sufficiently known to the person skilled in the art and therefore do not need to be explained in any more detail. What is important for understanding the invention is the fact that the circuit **5** supplies an active POWERON signal if, after the POWERUP phase of the SDRAM memory, the internal supply voltages present at the output **8** have reached the values necessary for proper operation of the component.

According to the invention, the initialization circuit furthermore has an enable circuit **9** connected downstream of the circuits **3** and **5**. The command signals PRE, ARF and MRS are applied to an input **10** of the enable circuit **9** and the POWERON signal is applied to an input **11** of the enable circuit **9**. An enable signal CHIPREADY is supplied at an output **12** of the enable circuit **9** after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits **13** provided for proper operation of the semiconductor memory device. The internal control circuits **13** serve inter alia for sequence control for one or more of the memory blocks of the SDRAM memory and are known as such.

FIG. **2** shows a preferred exemplary embodiment of the enable circuit **9** according to the invention. The enable circuit **9** contains three bistable multivibrator stages **14**, **15** and **16** each having a set input S, a reset input R, and also an output Q. An AND gate **17** connected upstream of the reset input R of the multivibrator stage **15** and an AND gate **18** connected downstream of all the outputs Q of the multivibrator stages **14**, **15**, **16** are further provided. The enable circuit further has an inverter **19** connected downstream of the AND gate **18**. The enable signal CHIPREADY being output at the output **12** of the inverter **19** and the enable signal CHIPREADY is active HIGH, that is to say activated when its voltage level is at logic HIGH. The command signals PRE, ARF, MRS applied to the respective set inputs S of the bistable multivibrator stages **14**, **15**, **16** are each active LOW, that is to say these signals are active when their voltage level is at logic LOW, while the POWERON signal is again active HIGH. The POWERON signal is applied directly to the reset inputs R in the case of the multivibrator stages **14** and **16** and is firstly applied to one input of the AND gate **17** in the case of the multivibrator stage **15**, the signal output from the output Q of the multivibrator stage **14** is applied to the other input of the AND gate **17**, the output of the AND gate **17** is connected to the reset input of the multivibrator stage **15**.

The method of operation of the enable circuit **9** illustrated in FIG. **2** is such that activation of the enable signal CHIPREADY at is the output **12** to logic HIGH is generated only when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected. Only then are the control circuits **13** unlatched on account of the activation of the enable signal CHIPREADY; the control circuits **13** remaining latched prior to this.

In the schematic time sequence diagram according to FIG. **3**, exemplary command sequences during the switching-on operation of the semiconductor memory device are illustrated in order to elucidate the method of operation of the enable circuit **9**. In the case situation A, the signal PRECHARGE is activated to active LOW too early relative to the activation of the POWERON signal, with the result that, the enable signal CHIPREADY is not yet activated to logic HIGH since the proper initialization sequence requires a

waiting time before the first command. The signal swing of the command PRECHARGE according to case situation A is thus correctly ignored. In case situation B, the chronological order of the activation of the signal AUTOREFRESH to logic LOW is incorrect since the proper initialization sequence prescribes a previous PRECHARGE command before the AUTOREFRESH command. The signal swing of the AUTOREFRESH signal to logic LOW according to case situation B is therefore likewise ignored, and the enable signal does not go to logic HIGH. In case situation C, a correct chronological order of the commands PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET is present conforming to the JEDEC standard, in a logically consistent manner, since the POWERON signal is also at logic HIGH, an enable signal CHIPREADY at logic HIGH is now supplied. Illustrated using dashed lines, another further conceivable initialization sequence that is allowed and therefore triggers an enable signal is represented by the symbol D; activation of the command MODE-REGISTER-SET to logic LOW is allowed at any time after the activation of the POWERON signal.

FIG. **4** shows further details of a preferred exemplary embodiment of the enable circuit **9** according to the invention. In this exemplary embodiment, each of the bistable multivibrators **14**, **15**, **16** is constructed from in each case two NAND gates **14**A, **14**B, **15**A, **17**, **16**A, **16**B and also an inverter **14**C, **15**C and **16**C, which are connected to one another in the manner illustrated. The NAND gate **17** is provided with three inputs in the bistable multivibrator **15**.

I claim:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

2. The semiconductor memory device according to claim **1**, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

3. The semiconductor memory device according to claim **1**, wherein said enable circuit has at least one bistable multivibrator stage having a set input receiving the externally applied further command signals, a reset input receiving one of the supply voltage stable signal, a signal derived from the supply voltage stable signal and a linked signal, and an output outputting said enable signal.

4. The semiconductor memory device according to claim **3**, wherein said at least one bistable multivibrator stage is a plurlity of bistable multivibrator stages respectively receiving one of the externally applied further command signals.

5. The semiconductor memory device according to claim **4**, wherein said output of one of said plurality of bistable multivibrator stages is passed to said reset input of another of said plurality of bistable multivibrator stages.

6. The semiconductor memory device according to claim **4**, including an AND gate receiving the supply voltage stable signal and a signal output from said output of one of said plurality of bistable multivibrator stages, said AND gate outputting an output signal received at said reset input of another of said plurality of bistable multivibrator stages.

7. The semiconductor memory device according to claim **4**, wherein said plurality of bistable multivibrator stages are each formed of an RS flip-flop constructed from one of at least two NOR and at least two NAND gates.

8. The semiconductor memory device according to claim **1**, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

9. The semiconductor memory device according to claim **1**, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

10. The semiconductor memory device according to claim **1**, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

a) firstly PRE, secondly ARF, thirdly MRS;

b) firstly PRE, secondly MRS, thirdly ARF; and

c) firstly MRS, secondly PRE, or thirdly ARF;

where,

PRE=the preparation command signal for word line activation,

ARF=the refresh command signal, and

MRS=the loading configuration register command signal.

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

12. The method according to claim **11**, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

13. The method according to claim **11**, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

* * * * *

EXHIBIT 2

US007145369B2

(12) **United States Patent**
Dickman

(10) **Patent No.: US 7,145,369 B2**
(45) **Date of Patent: Dec. 5, 2006**

(54) **OUTPUT DRIVER FOR AN INTEGRATED CIRCUIT AND METHOD FOR DRIVING AN OUTPUT DRIVER**

(75) Inventor: **Rory Dickman**, Regensburg (DE)

(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/887,949**

(22) Filed: **Jul. 9, 2004**

(65) **Prior Publication Data**

US 2005/0030068 A1 Feb. 10, 2005

(30) **Foreign Application Priority Data**

Jul. 12, 2003 (DE) 103 31 607

(51) **Int. Cl.**
H03K 3/00 (2006.01)

(52) **U.S. Cl.** **327/108**; 327/112

(58) **Field of Classification Search** 327/108, 327/112; 326/82–87
See application file for complete search history.

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(57) **ABSTRACT**

One embodiment of the invention provides an output driver for an integrated circuit. The output driver has a driver circuit for driving an input signal onto an output line. The driver circuit is dimensioned in such a way as to supply a current intensity dependent on the input signal to be driven and/or a potential dependent on the input signal to be driven on the output line. The current value and/or the potential value lie in a current intensity range and/or potential range defined by a predetermined specification. The driver strength of the driver circuit may be set in accordance with a control signal. A measuring circuit is provided to measure the current intensity of the current flowing on the output line and/or the potential of the output line. A control circuit serves for setting the driver strength of the driver circuit so that the potential on the output line is set to a potential value and/or the current intensity is set to a current value, wherein the set potential value and the set current value may lie in a lower power range of the current intensity range and/or potential range prescribed by the specification.

20 Claims, 2 Drawing Sheets

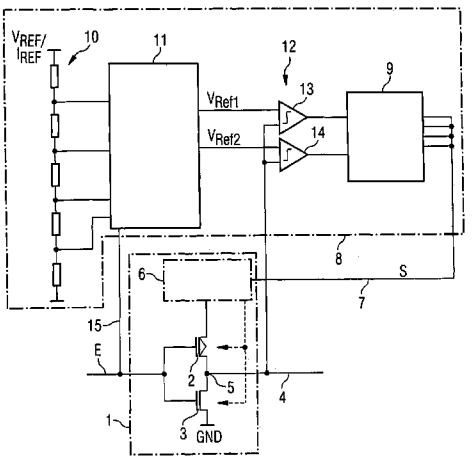

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FIG 1

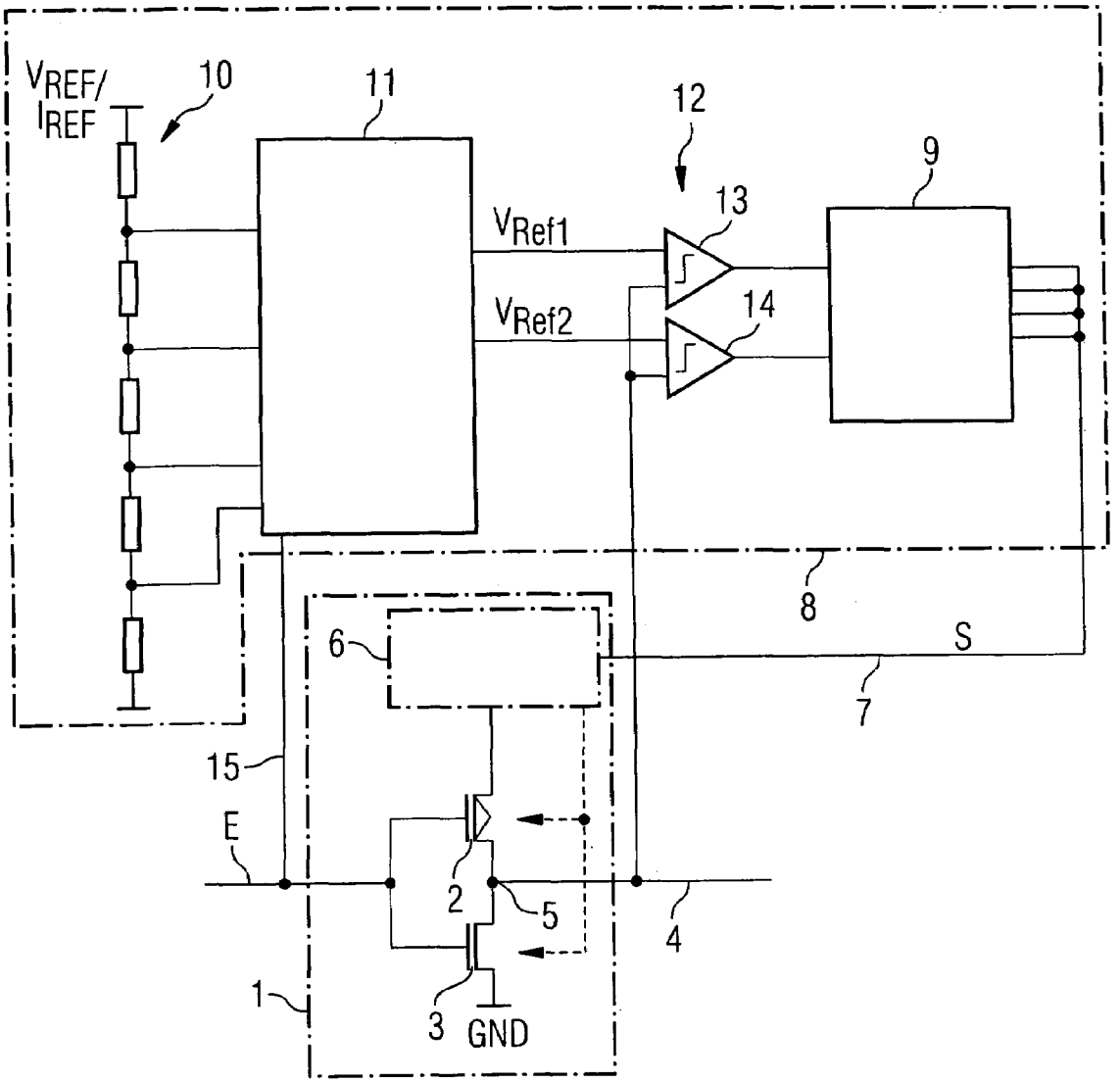

FIG 2A

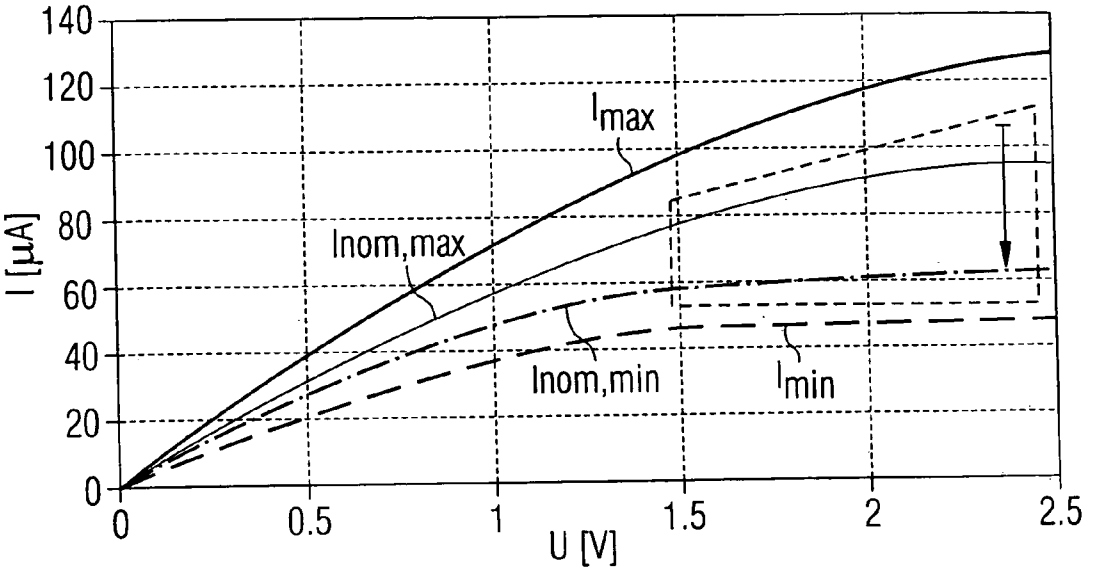
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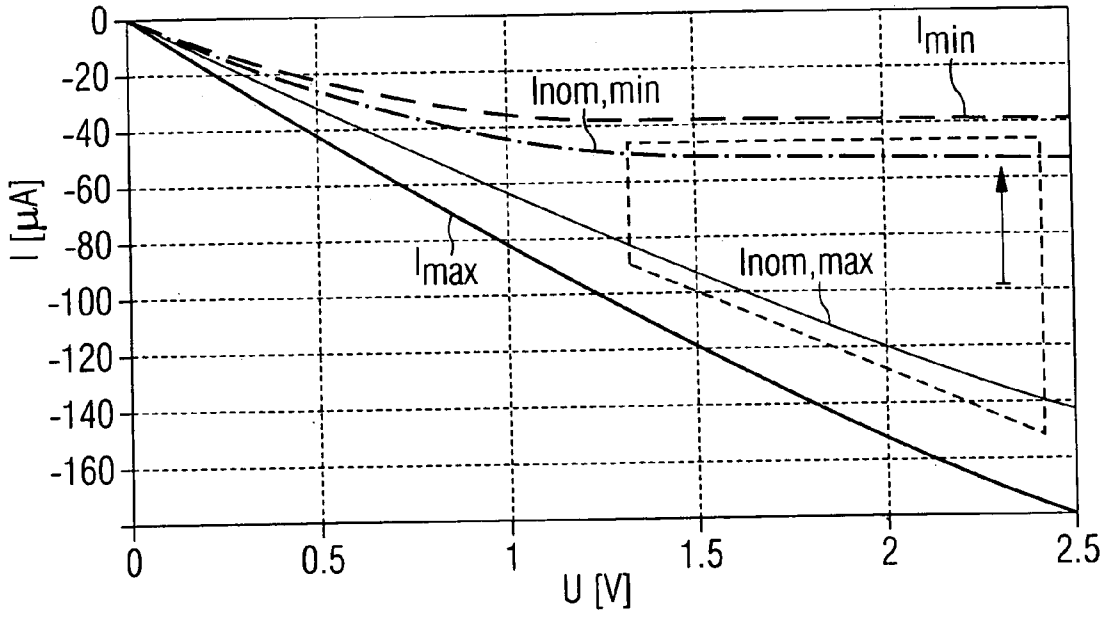
FIG 2B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OUTPUT DRIVER FOR AN INTEGRATED CIRCUIT AND METHOD FOR DRIVING AN OUTPUT DRIVER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number 103 31 607.8, filed Jul. 12, 2003. This related patent application is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to an output driver for an integrated circuit having a driver circuit for driving an input signal onto an output line. The invention furthermore relates to a method for driving an output driver for an integrated circuit.

2. Description of the Related Art

Integrated circuits usually have output drivers for driving signals which have been generated in circuits of the integrated circuit on external lines connected to the integrated circuit. To define the driver behavior of the output drivers, a specification is provided which, depending on the output driver, provides an upper and a lower current value or an upper and lower potential value depending on the signal state (high level or low level) of the output signal to be driven. In this case, the specification respectively specifies an upper and lower current-voltage characteristic curve for the activated pull-up path of the driver circuit and for the pull-down path of the driver circuit, which characteristic curve in each case defines a current intensity range within which the current intensity through the relevant path and thus through the output line must be. Depending on whether a high or low level is intended to be driven by the output driver, the specification prescribes different upper and lower current-voltage characteristic curves for the pull-up path and the pull-down path.

Usually, the specifications for integrated circuits, in particular for SDRAM and DDR memory circuits, provide a relatively large current intensity range or potential range for the output drivers, so that it is simpler to achieve the specification-conforming current intensity values or potential values for process cut-off values, temperatures and voltages (PVT). The specification-conforming current intensity ranges or voltage ranges of the pull-up paths and pull-down paths may signify great differences with regard to the power consumption depending on the position of the actual potential value or current value within the specification, since more power is required in an upper current intensity range and/or in an upper potential range than if the output signal is in a lower range of the permissible predetermined potential window and/or current intensity window.

However, the exact potential value or current value with which the signal is driven with the aid of the output driver cannot be established from the outset since it is necessary to take account of process deviations, temperature fluctuations and voltage fluctuations which might have the effect that the relevant value is outside the specification-conforming window. Moreover, different loads are possible at the outputs of the integrated circuit, so that this may result in different potential values or current values depending on the connected components or the switching states thereof.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an integrated circuit and a method for controlling an output driver which are able to reduce the power consumption of the integrated circuit and to ensure that the corresponding potential value or current value at the output of the output driver is within the specification.

A first aspect of the present invention provides an output driver for an integrated circuit. The output driver has a driver circuit for driving an input signal onto an output line. The driver circuit is dimensioned in such a way as to supply a current intensity dependent on the input signal to be driven and/or a potential dependent on the input signal to be driven on the output line. The current value and/or the potential value lie in a current intensity range and/or potential range defined by a predetermined specification. The driver strength of the driver circuit may be set in accordance with a control signal. A measuring circuit is provided to measure the current intensity of the current flowing on the output line and/or the potential of the output line. A control circuit serves for setting the driver strength of the driver circuit so that the potential on the output line is set to a potential value and/or the current intensity is set to a current value, wherein the set potential value and the set current value may lie in a lower power range of the current intensity range and/or potential range prescribed by the specification.

In this way, one aspect of the invention provides an output driver for an integrated circuit which makes it possible to set the current value and/or the potential value on the output line in a lower power range, i.e., to operate the integrated circuit at an operating point at which the power consumption of the output driver can be reduced, but without permitting a current value or potential value outside the specification-conforming limits. The current intensity ranges and/or potential ranges permissible in accordance with the specification are comparatively large on account of process fluctuations in the production of the integrated circuits, a high operating temperature range in which the integrated circuit can be operated reliably, and voltage fluctuations that may occur. It follows from this that the output driver has a different power consumption depending on the current intensity or potential within the permissible windows with which the output driver drives a signal onto the output line. Consequently, the range of possible power consumptions is likewise very large on account of the large range of values for the potential and the current intensity. In order not to reach an operating range outside the specification on account of temperature fluctuations, process fluctuations or the like, the driver strength of the output driver may be set by means of the production process such that the input signal to be driven is driven with a current intensity and a potential which essentially lies centrally within the current intensity range or potential range prescribed by the specification.

One aspect of the invention also provides a control circuit which influences the driver strength of the driver circuit. The driver strength of the driver circuit may be set by the control circuit in such a way that the current intensity and/or the potential on the output line, depending on the input signal to be driven, lies in a lower power range of the current intensity range and/or potential range prescribed by the specification, i.e., the power consumption of the output driver is reduced within the permissible range. As a result, it is possible to take into account the process fluctuations during the production of the integrated circuit, the respective operating temperature, the potential fluctuations, e.g., of the supply voltages, and the load connected to the output driver such that the driver circuit of the output driver supplies a potential value and a current intensity value lying within the specification-conforming range limits, albeit in a lower power range to reduce the power consumption of the output driver in comparison with the energy consumption of a noncontrolled driver circuit.

One aspect of the invention provides that the lower power range is determined by a lower current limit value prescribed by the specification and a lower current limit value increased by a tolerance magnitude and/or by a lower potential value prescribed by the specification and a lower potential value increased by a tolerance magnitude. In this way, a lower power range can be defined in the current or potential value prescribed by the specification.

The specification may specify a first maximum and minimum current-voltage characteristic curve for a pull-up path of the driver circuit and a second maximum and minimum current-voltage characteristic curve for a pull-down path of the driver circuit. Depending on the respectively driven pull-up path or pull-down path of the driver circuit, the lower power range is determined depending on the current intensity range which is prescribed by the specification and is specified by the first or second current-voltage characteristic curve.

The control circuit may comprise a comparator device for comparing the measured current value or the measured potential value with a reference current value or a reference potential value dependent on the specification. The reference current value or the reference potential value may be provided by a reference voltage source or a reference current source.

A further aspect of the present invention provides a method for driving an output driver for an integrated circuit having a driver circuit. The driver circuit serves for driving an output signal dependent on an input signal with a current intensity and/or a potential onto an output line. The current intensity of the current flowing on the output line and/or the potential on the output line are measured. The driver strength of the driver circuit is controlled in such a way as to set the current intensity and/or the potential in a current intensity range and/or potential range defined by a predetermined specification. Furthermore, the driver strength is set in such a way that the potential value and/or the current intensity lie in a lower power range of the current intensity range and potential range prescribed by the specification.

The method according to the invention affords the possibility of setting the driver power of an output driver in such a way that the current intensity and/or the potential on the output line are always set in such a way that the power consumption of the driver circuit lies in a lower power range of the current-voltage window prescribed by the specification. The power consumption of the output driver can thereby be reduced. Furthermore, the output driver can be controlled in this way such that it can also react to influences of the load applied to the output driver on the potential value of the output signal and always sets the current intensity or the potential on the output line such that it lies within the specification-conforming current-voltage window of the driver circuit.

The control of the driver strength of the driver circuit may be carried out continuously, periodically or in accordance with a setting signal.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention is explained in more detail with reference to the accompanying drawings, in which:

FIG. **1** shows a block diagram of an output driver according to one embodiment of the invention; and

FIGS. **2***a*, **2***b* show minimum and maximum current-voltage characteristic curves for illustrating the current-voltage windows for the pull-down path and the pull-up path of the driver circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** illustrates a block diagram of an output driver according to one embodiment of the invention. The output driver has a driver circuit **1** comprising a p-channel transistor **2** and an n-channel transistor **3**. An input signal E is applied to control inputs of the p-channel transistor **2** and of the n-channel transistor **3**, which input signal is driven in inverted fashion onto an output line **4** connected to an output **5** of the driver circuit **1**.

A first terminal of the p-channel transistor **2** is connected to a high supply potential. A second terminal of the p-channel transistor **2** is connected to a first terminal of the n-channel transistor **3**, and a second terminal of the n-channel transistor **3** is connected to a low supply potential, e.g., a ground potential GND.

The driver circuit **1** furthermore comprises a setting circuit **6**, by means of which the driver strength of the driver circuit **1** can be set in accordance with a control signal S on a control line **7**. The driver strength may be set, for example, by enlarging or decreasing the active area of the p-channel transistor **2** and of the n-channel transistor **3** in a manner dependent on the control signal S. Alternatively, a plurality of such circuits, each having a p-channel transistor and an n-channel transistor, may be connected in parallel to jointly drive an input signal present at the circuits' respective control inputs onto the output line **4**. Other possibilities are also conceivable for providing a setting circuit **6** such that the driver strength of an output stage connected thereto can be set in a manner dependent on a control signal.

The output line **4** of the driver circuit **1** is connected to a control unit **8**. The control unit **8** is configured to evaluate the potential value on the output line **4** in accordance with predetermined reference values and to generate the control signal S utilized to drive the driver circuit **1**. The control unit **8** is also configured to correspondingly adapt the driver strength of the driver circuit **1** if the potential of the respective output signal that is present on the output line lies above or below a range defined by reference potentials.

In the exemplary embodiment illustrated, the control unit **8** includes a comparator unit **12** comprising a first comparator **13** and a second comparator **14**. A first reference potential V_{Ref1} provided by a multiplexer **11** is applied to the first comparator **13** and a second reference potential V_{Ref2} is applied to the second comparator **14**. The first and second reference potentials V_{Ref1}, V_{Ref2} define a potential range within which the potential on the output line **4** is intended to lie. Outputs of the first comparator **13** and of the second comparator **14** are connected to an evaluation unit **9**, which generates the control signal S at an output and makes it available to the setting circuit **6** of the driver circuit **1**. If the potential on the output line **4** lies above the potential prescribed by the first reference potential value V_{Ref1}, then the evaluation unit **9** generates a control signal that specifies to the driver circuit **1** that the driver strength be reduced. If the potential value on the output line **4** is less than the second reference potential value V_{Ref2}, then the evaluation unit **9** generates a control signal that indicates to the driver circuit **1** that the driver strength be increased. In this way, the potential value on the output line **4** can be regulated to a driver strength which enables the potential value on the output line **4** to be put into a potential window defined by the first reference potential value V_{Ref1} and the second reference potential value V_{Ref2}.

Since the potential value on the output line **4** depends on the input signal E present, the input line connected to the

input of the driver circuit **1** is connected via a connecting line **15** to the control unit **8**, in particular to the multiplexer **11**. In this way, the multiplexer **11** may apply the first and second reference potential values V_{Ref1}, V_{Ref2} to the comparator unit **12** in such a way that corresponding selected reference potential values are specified depending on the signal level of the output signal to be output on the output line **4**. For this purpose, essentially four reference potentials may be prescribed for the multiplexer **11**, two respectively prescribing the desired potential value range for a high level and the respective other two reference potentials prescribing the potential value range for the low level of the output signal. The reference potentials may be provided by a voltage divider **10**, for example, to which a reference supply voltage V_{Ref} or a reference supply current I_{Ref} is applied. The reference potentials for defining the potential window for the high level of the output signal are chosen such that they lie within a lower range of the potential window permitted by the specification for the high level of the output signal on the output line **4**. The potential window for the low level of the output signal on the output line **4** is defined by the reference potentials such that it likewise lies within a lower range of the potential window prescribed by the specification for the low level of the output signal.

The evaluation unit **9** may be designed as a counter, for example, wherein the control signal is transmitted to the setting circuit **6** as a digital value of the counter reading or wherein the counter value is converted into an analog voltage signal which is provided to the setting circuit **6** as a control signal.

The first comparator **13** and the second comparator **14** are configured in such a way that, at the output of the first comparator **13**, a logic "1" is present if the potential on the output line **4** exceeds the first reference potential V_{Ref}, and a logic "0" is present if the potential on the output line **4** falls below the first reference potential V_{Ref1}. Equally, at the output of the second comparator **14**, a logic "1" is present if the potential on the output line **4** falls below the second reference potential V_{Ref2} and a logic "0" is present if the potential on the output line **4** exceeds the second reference potential V_{Ref2}.

The counter in the evaluation unit **9** is decremented if a logic "1" is present at the output of the first comparator **13**, and incremented if a logic "1" is present at the output of the second comparator **14**. If a logic "0" is present at both outputs of the comparators **13**, **14**, then the counter reading of the counter in the evaluation unit **9** is not altered.

The first and second reference voltages are prescribed such that the range formed by the first and second reference voltages V_{Ref1}, V_{Ref2} lies within a lower range of the permitted potential window prescribed by the specification. The reference voltages V_{Ref1}, V_{Ref2} are selected by the multiplexer **11** depending on whether a high level or a low level is intended to be output at the output **5** of the driver circuit **1**. For this purpose, by way of example, the input signal may be connected to the multiplexer **11**. Alternatively, the output signal on the output line **4** may be connected to the multiplexer **11**. By means of the voltage divider **10**, reference voltages are made available such that, in each case, two of the reference voltages may be selected by means of the multiplexer **11** to define a voltage range which determines a lower power range within the permissible current-voltage window for the output signal on the output line.

As an alternative, instead of the potential on the output line, a current may also be converted into a measurement voltage, e.g., with the aid of a measuring resistor or another current measuring method, and the measurement voltage may then be compared with the reference potentials made available. It is also possible for the two setting methods to be combined with one another in that both the potential and the current intensity on the output line **4** are measured and evaluated either by two separate comparator circuits or successively with the aid of the reference potentials made available.

FIGS. **2***a* and **2***b* show the switching behaviors of the n-channel transistor **3** in the pull-down path and of the p-channel transistor **2** of the driver circuit **1** in the pull-up path. The current-voltage characteristic curves define a range that is permissible in accordance with the specification. The permissible potential ranges for the high and low levels on the output line are thereby determined. The range is defined in accordance with the lower current-voltage characteristic curve, identified by I_{min}, and the upper current-voltage characteristic curve, identified by I_{max}. The current-voltage characteristic curves identified by $I_{nom,max}$ and $I_{nom,min}$ represent nominal values of the respective transistor **2**, **3**. The driver power is principally determined by the current driver capability of the n-channel and p-channel transistors.

In accordance with the specification, an output current may be provided in the current-voltage window defined by the lower and upper current-voltage characteristic curves. The less current flows on the output line, however, the lower the power consumption of the driver circuit **1**. A reduction of the power consumption through a reduction of the current intensity through the activated transistor is permissible as long as the current intensity is within the respective current-voltage window prescribed by the specification. It is thus possible, within the limits prescribed by the specification, to define a current intensity range which brings about minimal power consumption through the driver circuit **1**. This range is chosen to lie within the range prescribed by the current-voltage windows.

The range may be defined, for example, in that a tolerance magnitude is added to the minimum current intensity I_{min} prescribed for a state of the output signal in accordance with the lower current-voltage characteristic curve, and the corresponding lower power range is thereby defined. Equally, provision may be made for providing a certain distance between the lower power range and the minimum current intensity value, so that the lower current/voltage characteristic curve is not undershot during regulation.

The adaptation of the driver strength of the driver circuit **1** may take place continuously or at periodic time intervals. It is expedient for the setting of the driver strength not to be carried out continuously, since the control unit **8** also has a power consumption which might minimize or cancel the power saving. The driver strength may also be adapted in accordance with an adaptation signal at predetermined points in time.

What is claimed is:

1. An output driver for an integrated circuit, comprising:

a driver circuit for driving an input signal of the output driver onto an output line;

a measuring circuit for measuring at least one of an output line current and an output line potential; and

a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range, wherein the control unit includes

a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.

2. The output driver of claim **1**, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude.

3. The output driver of claim **1**, wherein the driver circuit includes a pull-up path defined by a first maximum and minimum current/potential (I/V) characteristic curve and a pull-down path defined by a second maximum and minimum I/V characteristic curve and wherein the desired power range is determined depending on respectively activated pull-up path and pull-down path of the driver circuit.

4. The output driver of claim **1**, wherein the desired power range corresponds to a lower portion of the specification-prescribed potential range and a lower portion of the specification-prescribed current range.

5. The output driver of claim **1**, wherein the driver circuit further comprises a setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit.

6. The output driver of claim **1**, wherein the control unit further comprises a comparator unit for comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value.

7. The output driver of claim **6**, wherein the control unit further comprises an evaluation unit connected to the comparator unit, the evaluation unit configured to change the control signal based upon a result from the comparator unit.

8. The output driver of claim **7**, wherein the evaluation unit comprises a counter.

9. The output driver of claim **6**, wherein the control unit further comprises a multiplexer connected to provide a first reference potential and a second reference potential to the comparator unit.

10. The output driver of claim **9**, wherein the multiplexer selects the first reference potential and the second reference potential supplied to the comparator unit based on the input signal.

11. The output driver of claim **10**, wherein the multiplexer includes an input connected to the input signal of the driver circuit, and wherein the input signal is utilized to determine whether a high level or a low level is to be output by the driver circuit.

12. The output driver of claim **9**, wherein the multiplexer selects the first reference voltage and the second reference voltage supplied to the comparator unit based on an output signal on the output line.

13. The output driver of claim **9**, wherein the control unit further comprises a voltage divider connected provide a plurality of reference potentials selectable by the multiplexer.

14. A method for driving an output driver for an integrated circuit having a driver circuit driving an input signal onto an output line, comprising:

measuring at least one of an output line current and an output line potential; and

controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range, respectively, wherein the driver strength is set such that the potential and the current intensity lie in a lower power range of the specification-prescribed current range and the specification-prescribed potential range, and wherein the driver strength is feedback-controlled based on a measured value provided by a measuring circuit.

15. The method of claim **14**, wherein the driver strength of the driver circuit is controlled in a manner selected from continuously, periodically and in accordance with a setting signal.

16. The method of claim **14**, further comprising:

comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value; and

changing a control signal for setting the driver strength supplied to the driver circuit based upon a result from the comparison.

17. The method of claim **16**, further comprising:

determining whether a high level or a low level is to be output by the driver circuit based on the input signal; and

selecting a first reference voltage and a second reference voltage from a plurality of voltage references to be compared against the measured output line potential, the first reference voltage and the second reference voltage selected based on the determination of high level or low level.

18. An output driver for an integrated circuit, comprising:

a driver means for driving an input signal of the output driver onto an output line; and

a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range of a specification-prescribed potential range and a specification-prescribed current range, the control means comprising:

a comparator means for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value; and

an evaluation means for changing the control signal based upon a comparison result from the comparator means.

19. The output driver of claim **18**, wherein the control means further comprises:

a multiplexing means connected to provide a first reference voltage and a second reference voltage to the comparator means for the output line potential to be compared; and

a voltage divider means for providing a plurality of reference voltages for selection by the multiplexing means.

20. The output driver of claim **19**, wherein the multiplexing means includes an input connected to the input signal of the driver circuit, wherein the input signal is utilized to determine whether a high level or a low level is to be output by the driver circuit and wherein the multiplexer selects the first reference voltage and the second reference voltage supplied to the comparator unit based on the input signal.

* * * * *

EXHIBIT 3

US007532523B2

(12) **United States Patent**
Braun et al.

(10) **Patent No.: US 7,532,523 B2**
(45) **Date of Patent: May 12, 2009**

(54) **MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT**

(75) Inventors: **Georg Braun**, Holzkirchen (DE); **Christian Weis**, Munich (DE); **Eckehard Plaettner**, Oberhaching (DE)

(73) Assignee: **Qimonda AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 263 days.

(21) Appl. No.: **11/461,380**

(22) Filed: **Jul. 31, 2006**

(65) **Prior Publication Data**

US 2007/0035326 A1 Feb. 15, 2007

(30) **Foreign Application Priority Data**

Jul. 29, 2005 (DE) 10 2005 035 780
Aug. 3, 2005 (DE) 10 2005 036 528

(51) **Int. Cl.**
G11C 7/00 (2006.01)

(52) **U.S. Cl.** **365/194**; 326/30; 365/198; 365/206

(58) **Field of Classification Search** 326/30; 365/51, 189.17, 191, 198, 206, 194
See application file for complete search history.

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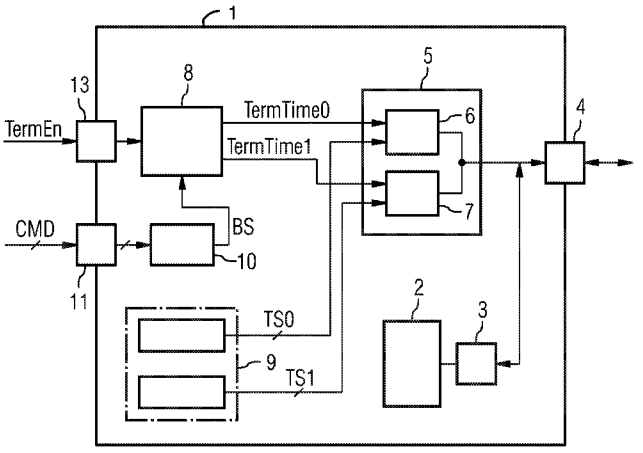
(74) *Attorney, Agent, or Firm*—Patterson & Sheridan, L.L.P.

(57) **ABSTRACT**

Methods and apparatus for setting various terminations of a memory chip. The memory chip includes a terminal, a termination circuit that can be connected to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination circuit in order to set a resistance value as a function of a received control command signal.

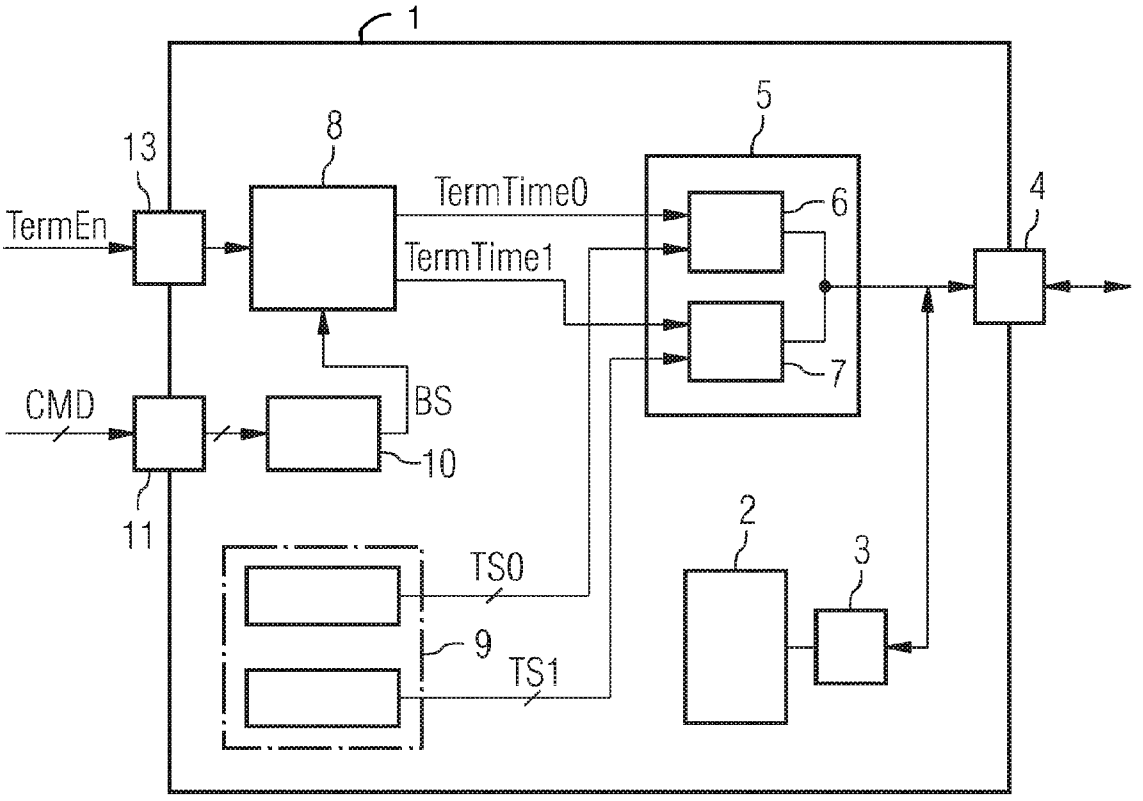
10 Claims, 5 Drawing Sheets



LEGEND:

1 - MEMORY CHIP
2 - MEMORY CELL ARRAY
3 - LOGIC CIRCUIT
4 - EXTERNAL TERMINAL
5 - TERMINATION CIRCUIT
6 - FIRST SETTABLE TERMINATING RESISTOR
7 - SECOND SETTABLE TERMINATING RESISTOR
8 - CONTROL UNIT
9 - CONFIGURATION UNIT
10 - COMMAND DECODER
11 - EXTERNAL CONTROL COMMAND PORTS
13 - EXTERNAL TERMINATION PORT

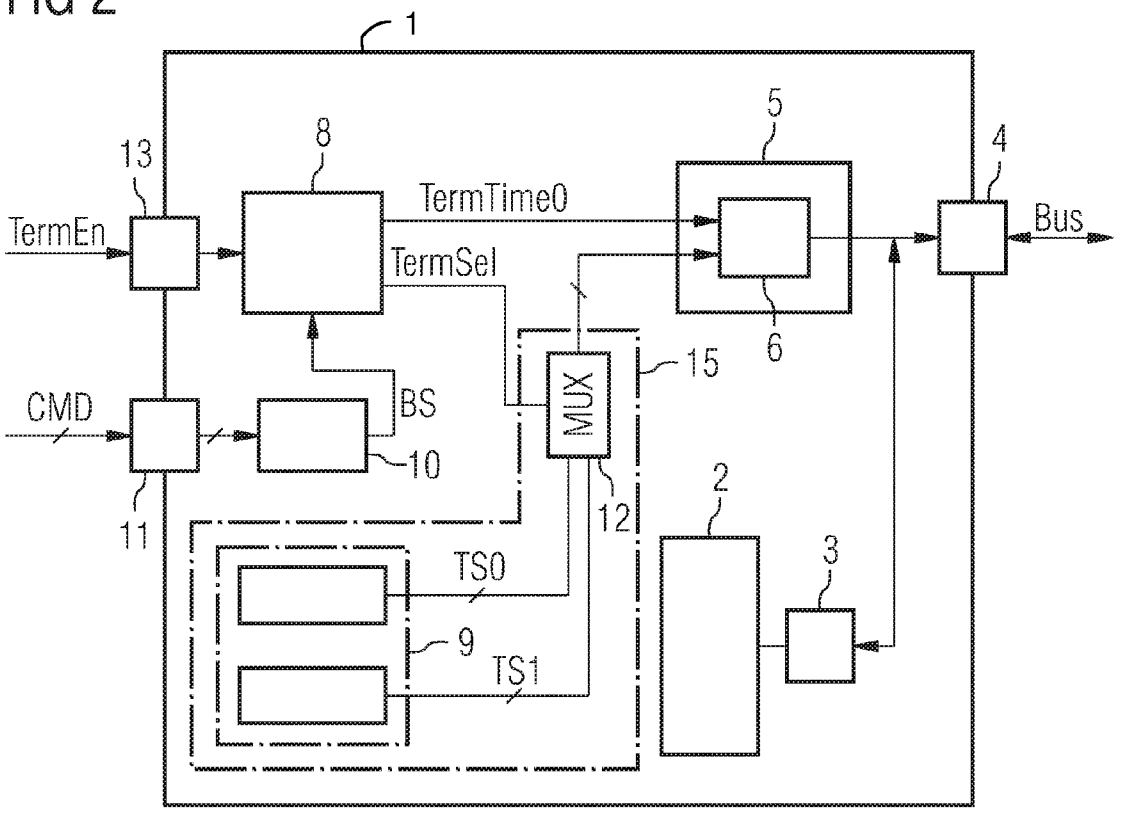
FIG 1



LEGEND:

1 - MEMORY CHIP
2 - MEMORY CELL ARRAY
3 - LOGIC CIRCUIT
4 - EXTERNAL TERMINAL
5 - TERMINATION CIRCUIT
6 - FIRST SETTABLE TERMINATING RESISTOR
7 - SECOND SETTABLE TERMINATING RESISTOR
8 - CONTROL UNIT
9 - CONFIGURATION UNIT
10 - COMMAND DECODER
11 - EXTERNAL CONTROL COMMAND PORTS
13 - EXTERNAL TERMINATION PORT

FIG 2



LEGEND:

1 - MEMORY CHIP
2 - MEMORY CELL ARRAY
3 - LOGIC CIRCUIT
4 - EXTERNAL TERMINAL
5 - TERMINATION CIRCUIT
6 - FIRST SETTABLE TERMINATING RESISTOR
8 - CONTROL UNIT
9 - CONFIGURATION UNIT
10 - COMMAND DECODER
11 - EXTERNAL CONTROL COMMAND PORTS
12 - MULTIPLEXER
13 - EXTERNAL TERMINATION PORT
15 - SETTING UNIT

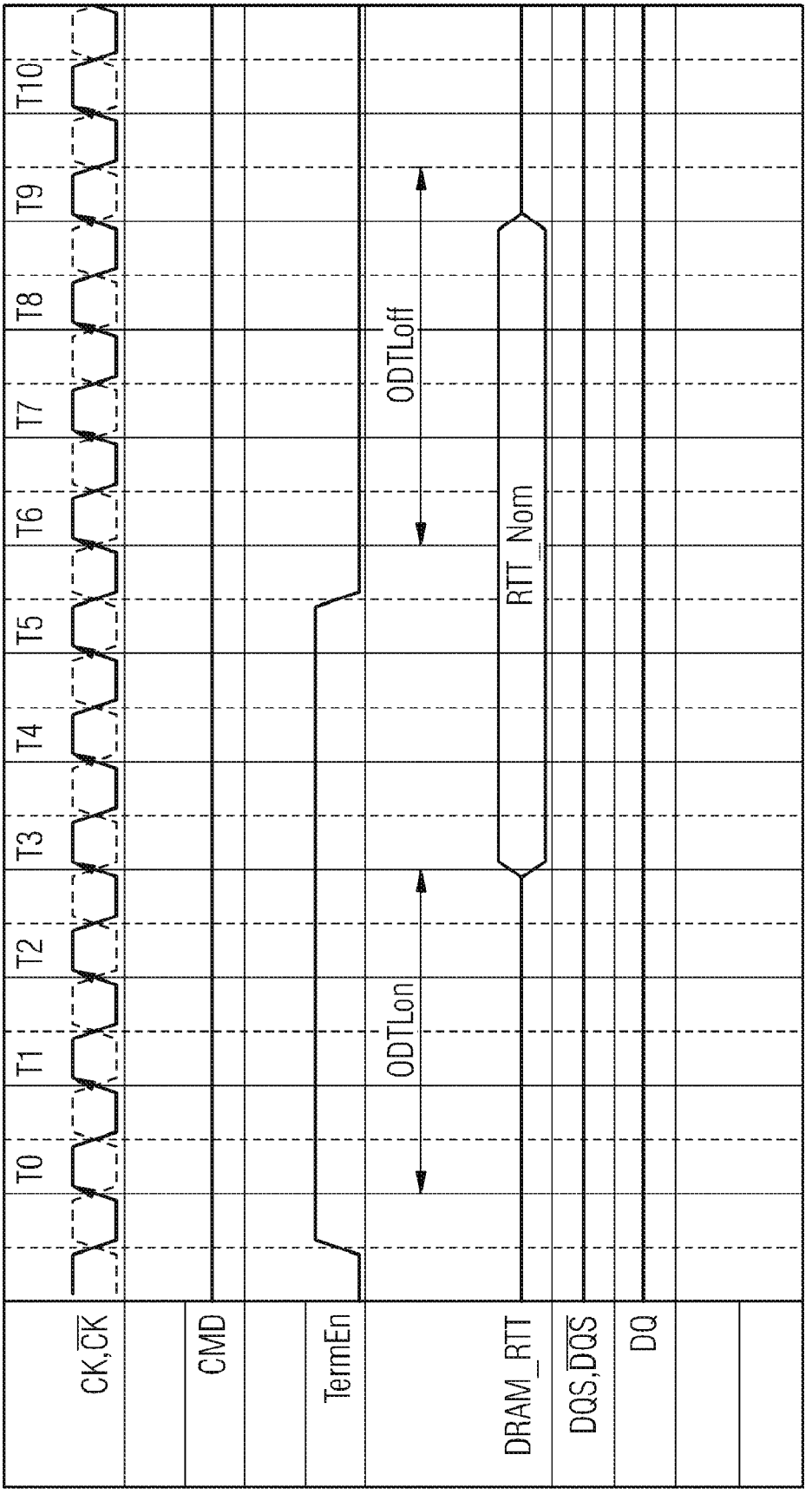

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK,$\overline{CK}$
CMD
TermEn
DRAM_RTT
DQS,$\overline{DQS}$
DQ
ODTLon
ODTLoff
RTT_Nom

FIG 3

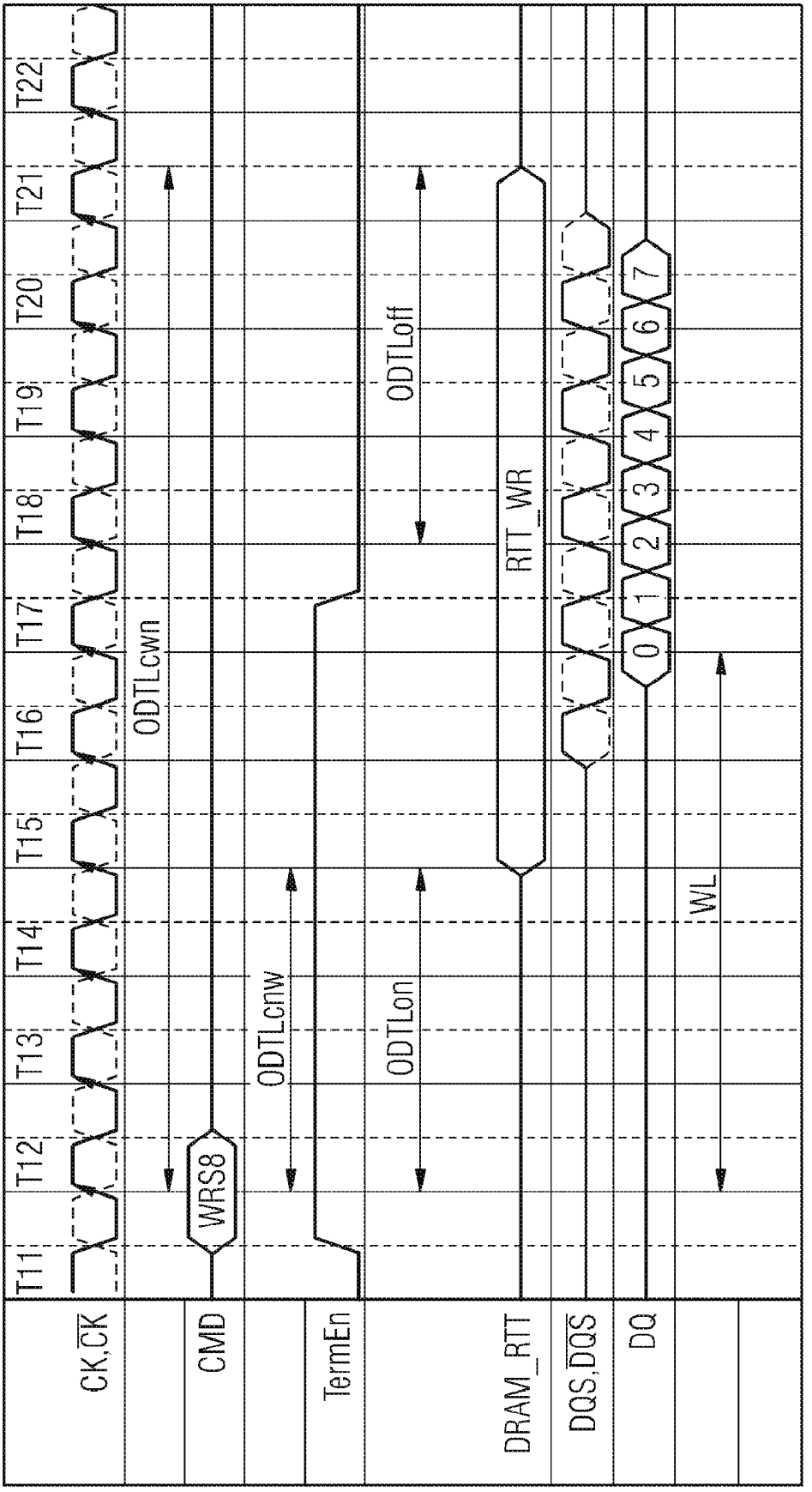

T11
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
CK,CK
CMD
TermEn
DRAM_RTT
DQS,DQS
DQ
WRS8
ODTLcwn
ODTLcnw
ODTLon
ODTLoff
RTT_WR
WL
0
1
2
3
4
5
6
7

FIG 4

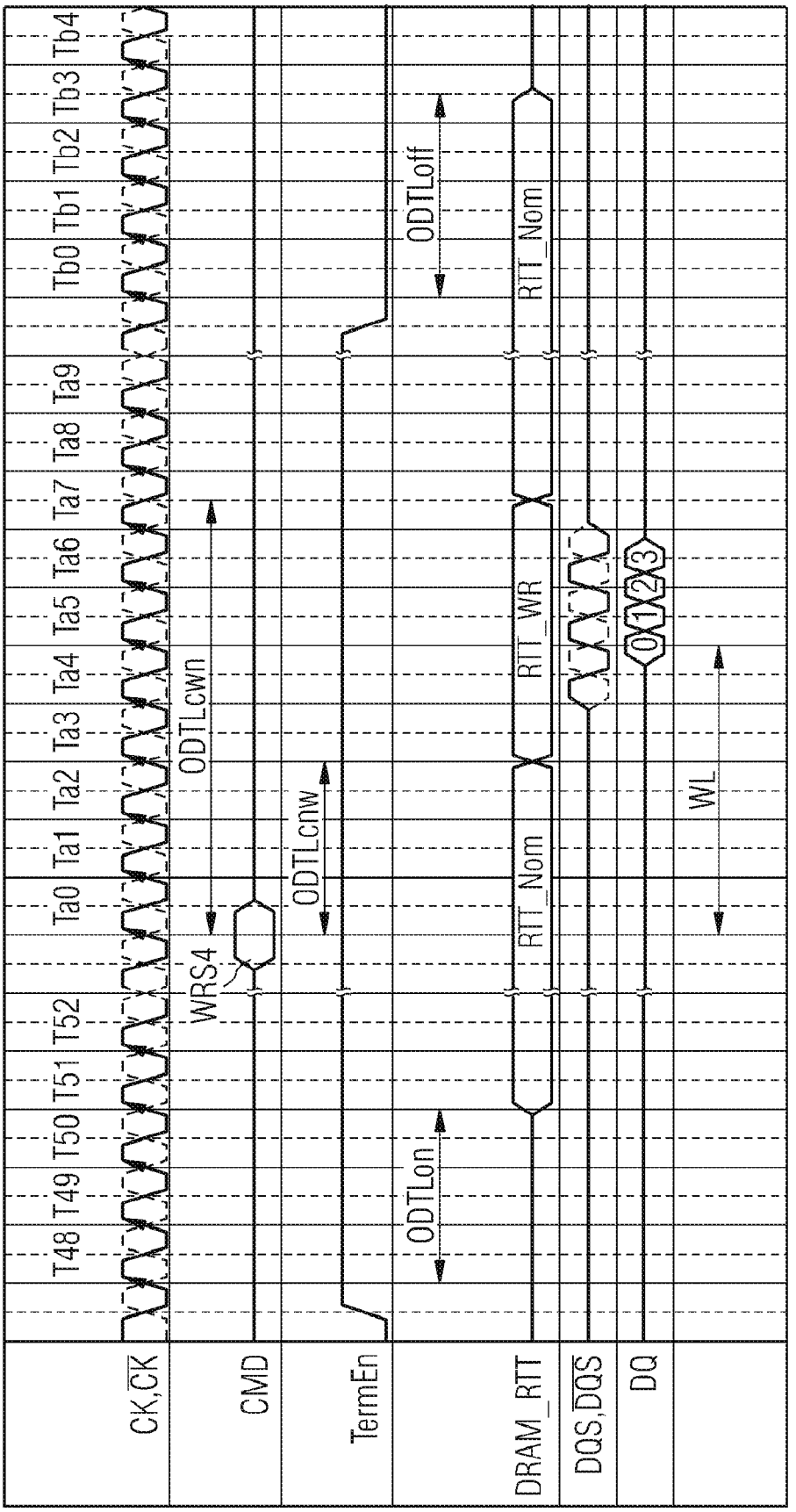

Tb4
Tb3
Tb2
Tb1
Tb0
Ta9
Ta8
Ta7
Ta6
Ta5
Ta4
Ta3
Ta2
Ta1
Ta0
T52
T51
T50
T49
T48
CK,CK
CMD
TermEn
DRAM_RTT
DQS,DQS
DQ
WRS4
ODTLcwn
ODTLcnw
ODTLon
ODTLoff
RTT_Nom
RTT_WR
RTT_Nom
0
1
2
3
WL

FIG 5

MEMORY CHIP WITH SETTABLE TERMINATION RESISTANCE CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number DE 10 2005 035 780.6, filed 29 Jul. 2005. This application also claims foreign priority benefits under 35 U.S.C. §119 to co-pending German patent application number DE 10 2005 036 528.0, filed 3 Aug. 2005. Each of these related patent applications is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The following description relates to a memory chip having a terminal for sending and/or receiving high-frequency signals. The description further relates to a method for operating a memory chip.

2. Description of the Related Art

In memory systems, use is normally made of a multiplicity of memory chips that are operated via a memory bus. Control command signals, clock signals, data signals and address signals are generally connected to the memory chips via the memory bus. The memory bus comprises signal lines that normally connect the memory chips to one another and to a memory controller. However, during transmission of high-frequency signals, signal reflections that disturb the data transmission on the memory bus and thereby limit the data transmission rates can occur at the terminals of the memory chips. It is necessary for this reason when transmitting data via the memory bus to provide suitable terminations at the terminals of the memory chips in order to reduce the signal reflections on the signal lines.

It has previously been provided in the case of memory chips to switch the termination on or off at a terminal of the memory chip as a function of a termination signal. That is to say, the memory controller makes a suitable termination signal available to each of the memory chips in order to support the following read, write or other operation onto the memory chips with an optimal termination at all the memory chips connected to the memory bus. The disadvantage of such a control of the memory chips consists in that switching the terminating resistors on and off is not sufficient as a rule to achieve an optimal termination in every operating state, and thus, also not sufficient to improve the data transmission via the memory bus.

Furthermore, it can be provided that the strength of the terminating resistors in the memory chips is fixed in accordance with a configuration value that is communicated to the memory chips by the memory controller in an initialization phase at the beginning of the operation of the memory system. Setting the configuration values in the memory chips before each write and read operation is time consuming. Consequently, the initial presetting of the terminating resistor by the configuration value is also not suitable for providing terminating resistors for applying to the memory bus that are suitable for every case of addressing the memory chips of the memory system, since the access time in the memory system would thereby be slowed down substantially.

SUMMARY OF THE INVENTION

According to a one aspect, a memory chip is provided for setting various terminations on a signal line of the data bus.

The memory chip comprises a terminal, a termination circuit which is connectable to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination circuit in order to set the resistance value as a function of a received control command signal and to make the resistance value available at the terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

FIG. **1** shows a block diagram of a memory chip in accordance with a first embodiment;

FIG. **2** shows a block diagram of a memory chip in accordance with a further embodiment;

FIG. **3** shows a signal-time diagram that illustrates the functionality of the embodiments of FIG. **1** and FIG. **2** given the presence of no operation affecting the memory chip;

FIG. **4** shows a signal-time diagram for illustrating the functionality of the embodiments of FIGS. **1** and **2** that illustrates the carrying out of a write operation; and

FIG. **5** shows a signal-time diagram for illustrating the functionality of the embodiments of FIGS. **1** and **2** that illustrates the carrying out of a write operation in conjunction with an activated termination signal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A memory chip **1** is illustrated in FIG. **1** as a block diagram. The memory chip **1** comprises a memory cell array **2**, such as, for example, a DRAM memory cell array, that can be written to and read from via a logic circuit **3**. The logic circuit **3** comprises driver circuits as well as input amplifiers and output drivers (not shown). The logic circuit **3** is connected to an external terminal **4** of the memory chip **1** via which, for example, address, clock and user data can be read in or driven out.

The external terminal **4** is connected to a termination circuit **5** that has a first settable terminating resistor **6** with a first resistance value, and a second settable terminating resistor **7** with a second resistance value. The termination circuit **5** is connected to a control unit **8** that makes available to the termination circuit **5** a first control signal TermTime**0**, and a second control signal TermTime**1**. Upon activation of the first control signal TermTime**0**, the first terminating resistor **6** is connected to the external terminal **4** such that the external terminal **4** is terminated with the first resistance value set accordingly in the first terminating resistor **6**. Upon activation of the second control signal TermTime**1**, the second terminating resistor **7** is correspondingly connected to the first terminal such that the external terminal **4** is terminated with the second resistance value. Furthermore, given simultaneous activation of the two control signals TermTime**0**, TermTime**1**, it is also possible to generate a further resistance value for termination that results from the parallel connection of the first and second resistance values.

Further provided is a configuration unit **9** that makes available a first configuration value TS**0** and a second configuration value TS**1**. The first configuration value TS**0** is connected to the first terminating resistor **6**, and the second configuration value is connected to the second terminating resistor **7** in order to set the respective resistance value of the corresponding terminating resistor **6**, **7**. The configuration values TS**0**, TS**1** can be made available in parallel via configuration signals. As a function of the respective control signal TermTime**0**, TermTime**1**, the corresponding terminating resistor **6**, **7**, whose resistance value is provided by the respective configuration value TS**0**, TS**1**, is then connected to the external terminal **4**.

A settable terminating resistor can be achieved, for example, by switchable, parallel-connected resistors. It is also possible to implement the resistors by means of transistors with the same or different channel width that are completely or partially switched through. The terminating resistors can be fashioned such that the respective control signal TermTime**0**, TermTime**1** is logically combined with each of the bits of the configuration value TS**0**, TS**1** made available by means of AND operation, and the respective logic results are connected to the inputs of transistors provided in the terminating resistor.

Via an external termination port **13**, the control unit **8** receives a termination enable signal TermEn that indicates whether or not a termination is to be provided at the external terminal **4**. That is to say, via the first and the second control signal TermTime**0**, TermTime**1**, the respective terminating resistor **6**, **7** is connected to the external terminal **4** only when the termination signal TermEn specifies that there is to be a termination. Otherwise, no termination of the external terminal **4** is undertaken.

Which of the two terminating resistors **6**, **7** is connected to the external terminal **4** is specified as a function of a command signal BS that is made available by a command decoder **10**, as a function of a received control command CMD. Via one or more external control command ports **11**, the command decoder **10** receives control command signals CMD for activating, addressing and/or driving the memory chip **1**.

The control command signals CMD can assume an active or inactive state. If the memory chip **1** is a DRAM memory chip, the control command signals can be, for example, the chip select signal CS for selecting the relevant memory chip for a specific operation, the write enable signal WE for enabling a write access to the memory chip, the RAS signal (row activation signal) for transmitting the word line address and for activating the word line, as well as the CAS signal (column activation signal) for transmitting the bit line address and for activating the bit line for reading data out and/or writing them into the memory cell field. Depending on whether the relevant memory chip in a memory system is or is not selected for an operation, or whether the aim is to carry out writing or reading on the relevant memory chip (write enable signal), only one of the two terminating resistors **6**, **7** or none of the two terminating resistors can be selected (under the control of the termination signal) in order to terminate the external terminal **4** in a suitable way.

FIG. **2** shows another embodiment of a memory chip **1**. Like functions or components relative to FIG. **1** are identified by like reference numbers or labels. The embodiment of FIG. **2** differs from the embodiment of FIG. **1** in that a setting unit **15** is provided that has the configuration unit **9** and a multiplexer **12**. A termination selection signal TermSel made available by the control unit **8** is connected to a control input of the multiplexer **12**. The termination selection signal TermSel is used to select which of the configuration values TS**0**, TS**1** made available by the configuration unit **9** is connected to the termination circuit **5**. In this embodiment, the termination circuit **5** comprises only one settable terminating resistor **6** whose resistance value is set as a function of the selected configuration value TS**0**, TS**1**. The sole terminating resistor **6** is now activated or deactivated, and thereby connected to the external terminal **4** or not as a function of the single control signal TermTime**0**, which is made available by the control unit **8**.

The magnitude of the resistance value of the terminating resistor **6** is determined by the termination selection signal TermSel with the aid of which one of the configuration values TS**0**, TS**1** is selected. By contrast with the embodiment of FIG. **1**, it is possible in the case of this embodiment to dispense with a second settable terminating resistor and instead of this to select the single settable terminating resistor in accordance with a configuration value that can be selected via the multiplexer **12**, doing so as a function of the current control command signals. A combination of various terminating resistors that are simultaneously connected to the external terminal **4**, as shown in FIG. **1**, is therefore not possible, but chip area can be saved since only one settable terminating resistor **6** is required.

FIG. **3** shows a signal-time diagram for explaining the signal profile for setting the termination in an inventive memory chip. Specified in the signal-time diagram of FIG. **3** is a case where the goal is to switch on a termination when the command control signal specifies that the relevant memory chip is not activated, that is to say no access to the memory chip is to be carried out (chip select signal deactivated). After a predetermined termination switch-on time ODTLon of, in this example, three clock periods, a desired first resistance value RTT_Nom (DRAM_RTT) is connected to the external terminal **4** in a fashion triggered by the activation of the termination signal TermEn by the memory controller and by a rising edge of a clock signal CK at an instant T**0**. After deactivation of the termination signal TermEn during the fifth clock period T**5**, the next rising edge of the clock signal T**6** starts a predetermined termination switch-off time ODTLoff that amounts in this exemplary embodiment to three and a half clock periods, and after the elapse thereof the terminating resistor is disconnected from the external terminal **4**. The time durations of the termination switch-on time ODTLon and of the termination switch-off time ODTLoff can be selected as desired, and should be selected such that they suffice to connect the terminating resistor reliably to the external terminal **4**, or to disconnect it therefrom. That is to say, they should at least have the time duration required for switching a terminating resistor on or off, or for connecting and disconnecting the terminating resistor from the external terminal **4**.

For example, given a deactivated chip select signal, that is to say when no operation is to be carried out in the memory chip, it is possible for the termination of the external terminal **4** to be undertaken or not, and this is controlled in a memory system by the memory controller issuing the termination signal TermEn. At the same time, it is established by the decoder **10** of the memory chip that the chip select signal CS is deactivated and as a function of the chip select signal CS an appropriate configuration value or control signal (according to the particular embodiment) is connected to the termination circuit **5** in order to connect the selected terminating resistor **6**, **7** (FIG. **1**) or **6** (FIG. **2**) to the external terminal **4**, doing so as a function of the termination signal TermEn.

FIG. **4** illustrates a further signal-time diagram for the embodiment of FIGS. **1** and **2**. The signal-time diagram of FIG. **4** exhibits a case in which the corresponding memory chip is activated by the chip select signal CS, and a write

command (WE-Signal) WRS**8** is sent to the memory chip by the memory controller. The memory controller may assert the termination signal TermEn and the write signal WRS**8** such that they can be accepted into the memory chip by a rising clock edge at an instant T**12**. The command decoder decodes the write signal WRS**8** and generates the command signal BS, which is applied to the control unit **8**. Depending on the command signal BS, it is established in the control unit **8** that it is now necessary to connect to the external terminal **4** a terminating resistor that is determined by the second configuration value. In the case of the embodiment of FIG. **1**, the control unit **8** therefore activates the second control signal TermTime**1** in order to activate the second terminating resistor **7**. In the embodiment of FIG. **2**, the control unit **8** switches the termination selection signal TermSel such that the multiplexer **12** connects the second configuration value to the termination circuit **5** in order to set there the resistance value of the terminating resistor **6** to the corresponding value, in this case to a second resistance value RTT_WR that corresponds to the terminating resistor that is to be connected to the activated memory chips in the event of a write access to the external terminal **4**.

Depending on the termination signal TermEn the terminating resistor is now connected to the external terminal **4** after the termination switch-on time ODTLon, the terminating resistor now being a different one, depending on the control command signal, as previously in the case of the deactivated memory chip (FIG. **3**). The write latency time duration WL, which amounts to 5 clock periods in the exemplary embodiments shown, begins to run at the same time as the reception of the write command WRS**8**. The data strobe signal DQS can be read into the memory chip at the same time as the data in terms of one clock period before the transmission of a data burst, that is to say transmission of 8 data bits. The termination switch-on time ODTLon may be selected to be equal to or less than the write latency time duration WL in order to ensure that the desired terminating resistor is connected to the external terminal **4** during transmission of data to the memory chip (during write access).

In general, the command signal BS is generated in the command decoder **10** such that it specifies to the control unit **8** which resistance value, RTT_Nom or RTT_WR, is to be set as terminating resistor for the terminal. In the case of a first group of control commands CMD that are present, the command decoder **10** outputs a command signal BS to the control unit **8** which specifies that a termination needs to be undertaken with the first resistance value RTT_Nom (with the termination signal TermEn activated), and in the case of a second group of control commands the command decoder **10** outputs a command signal BS to the control unit **8** which specifies that the terminal **4** is to be terminated with a second resistance value (with the termination signal TermEn activated). The first group of control commands can comprise control commands that, for example, indicate a deactivation of the integrated circuit, or a read access to the integrated memory circuit, while the second group of control commands can indicate write commands to the integrated memory circuit.

The time duration between the applying of a control command signal or between the making available of the command signal BS to the control unit **8** and changes, dependent thereon, to the resistance value in the termination circuit **5** may be established as first switchover time ODTLCNW that may be equal to or less than the termination switch-on time ODTLon.

In general, the control unit **8** may essentially switch on simultaneously the termination and the corresponding setting of the terminating resistor to the corresponding resistance value. Furthermore, it is likewise possible for the termination to be switched off and the resistance value to be changed simultaneously.

Furthermore, it can be provided, for example, when a control command of the second group of control commands is present that after the lapse of a second switchover time ODTLCWN the control unit **8** changes the termination of the second resistance value to the first resistance value irrespective of whether the termination signal TermEn provides a termination or not. The second switchover time ODTLCWN corresponds at least to a time duration that is determined by the ending of the write access or by the ending of an access to the memory chip that is triggered by a control command of the second group of control commands. In the case of a burst write access as described in conjunction with FIG. **4**, the second switchover time should be a function of the write latency time WL and of the time duration for the burst access. Alternatively, the second switchover time can also be set as a function of the end of a data transfer from and to the memory chip **1**. The second switchover time ODTLCBM may be the sum of the write latency WL, and the duration of the burst access (burst length/2*clock cycle length TCK) plus a safety period (½*TCK or a multiplier thereof). It is possible in this way for the second resistance value RTT_WR for terminating the terminal to be made available for terminating the terminal only for a specific time duration as a function of a control command CMD that is present, the terminal being terminated again after the elapse of this time duration with the first resistance value if the latter is specified by the termination signal TermEn.

Referring to FIG. **5**, an embodiment, is shown in which the termination signal TermEn permits the termination of the terminal **4** to be switched on before, during and after a write access WRS**4**, the termination being set before the write access to the first resistance value RTT_Nom. After the elapse of the first switchover time ODTLCNW the terminal **4** is terminated with the resistance value RTT_WR, and after the elapse of the second switchover time ODTLCWN, the termination is switched back again to the first resistance value RTT_Nom.

While in the exemplary embodiment shown in FIG. **1** only two different terminating resistors can be connected to the external terminal **4**, the number of different settable terminating resistors can, however, be as high as desired. Accordingly, different terminating resistors can be connected to the external terminals for different accesses in a memory system in which the memory chip is operated.

According to one aspect of the invention, during the operation of the memory chips in a memory system the terminating resistors can be specifically set for each of the memory chips as a function of the operation currently being carried out. Thus, it is possible to provide different terminating resistors that can individually, or else in combination, be connected to the external terminal. It can be possible, in addition, to apply a terminating resistor to the external terminal as a function of a termination signal TermEn.

In summary, a memory chip for setting various terminations is provided on a signal line of the data bus. The memory chip comprises a terminal, a termination circuit that can be connected to the terminal in order to terminate the terminal with a settable resistance value, a control command port for receiving a control command signal, and a control circuit that is connected to the termination circuit in order to set the resistance value as a function of a received control command signal and to make it available at the terminal.

The memory chip renders it possible to set a resistance value of the termination circuit as a function of a control command connected to the memory chip, and to terminate the terminal in an improved way such that the data transmission via the memory bus, which can be connected to the memory chip in a memory system, is supported in an optimal way. It is possible in this way to set the terminating resistor directly as a function of the operation of the memory system without the need to store a configuration value in the memory chip immediately before carrying out the operation by a corresponding setting operation controlled by the memory controller. It is advantageous that the setting of the respective termination need not be controlled by a memory controller of the memory system, but is prescribed by the control command signals in the memory system.

The termination circuit can further have a number of terminating resistors in order to provide a number of various resistance values, the control circuit being fashioned in order to select at least one of the terminating resistors and apply it to the terminal. By providing the number of the terminating resistors in the memory chip, the corresponding terminating resistors can be selected relatively quickly such that there is no, or no substantial time loss in carrying out the operation in the memory system.

In accordance with a further embodiment, a configuration unit is provided in order to set the resistance values of the number of terminating resistors. It is thereby possible to preselect the resistance values with which the terminal can be terminated.

In accordance with a further embodiment, the termination circuit can comprise a settable terminating resistor, a setting circuit being provided in order to make available as a function of a selection signal a setting value with the aid of which the resistance value of the terminating resistor is determined.

The memory chip further has a termination port in order to receive a termination signal, the control circuit being connected to the termination circuit in order, as a function of the termination signal either to terminate the terminal with the set resistance value, or not to terminate the terminal. It is possible in this way optionally also not to provide any termination at the terminal when this is prescribed by the memory controller and/or a control command.

The control circuit can further be connected to the termination circuit in order as a function of the termination signal to terminate the terminal with the set resistance with a first time delay in each case, or not to terminate it in accordance with a second time delay, the first time delay sufficing in order to set the resistance value. The first and the second time delays can be the same or different.

The control unit can further be fashioned such that the resistance value is set to a specific second resistance value as a function of the presence of a control command signal after a predetermined first switchover time and/or is set to a specific first resistance value after a predetermined second switchover time.

In accordance with a further embodiment, the control circuit sets the first switchover time as a function of the first time delay, and/or sets the second switchover time as a function of the second time delay.

In particular, the control unit can be fashioned such that the resistance value is set to the second resistance value in a fashion substantially simultaneous with the appliance of the termination at the terminal, and/or is set to the first resistance value in a fashion substantially simultaneous with the ending of the termination of the terminal.

In accordance with a further embodiment, a command decoder can be provided in order as a function of a control command signal that is present to communicate to the control unit whether a first or a second resistance value is to be set for termination.

In accordance with a further aspect, a memory system is provided having a memory controller, with a number of inventive memory chips and having a memory bus to which the memory controller and the memory chips are connected, the memory bus comprising a signal line that interconnects the terminals of the memory chips and a terminal of the memory controller.

In accordance with a further aspect, a method is provided for operating a memory chip in the case of which a control command signal is received, in which a terminal is terminated with a settable resistance value, and the resistance value is set as a function of the received control command signal, and the terminal is terminated with the set resistance value. It is possible in this way to set the terminating resistor, which is connected to a terminal of a memory chip, as a function of a control command such that it is possible during operation of the memory chip in a memory system to set the termination suitable for operations to be carried out at each of the memory chips in order to reduce signal reflections on the lines of the memory bus, and thus to increase the possible data transmission rate. It is also advantageous that the setting of the resistance value can be carried out without providing further signals to be connected from outside.

The resistance value can further be set by the selection of a setting value for a settable terminating resistor.

The method further includes setting the resistance value by selection from a number of terminating resistors that are connected to the terminal.

In accordance with a further embodiment, it is possible to receive a termination signal and, as a function of the termination signal, either the terminal with the set resistance value is terminated, or the terminal is not terminated.

In accordance with a further embodiment, it is possible as a function of a change in level of the termination signal either to switch on the termination with the set resistance value with a time delay, or to switch off the termination with the time delay, the time delay being selected such that the selected terminating resistor can be set.

While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A memory chip for variably setting terminations, comprising:

a terminal;

a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

a control command port for receiving a control command signal for affecting accessibility of the memory chip;

a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,

wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accor-

dance with a second time delay, the first time delay being sufficiently long to set the resistance value.

2. The memory chip of claim **1**, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

3. The memory chip of claim **2**, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

4. The memory chip of claim **3**, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal.

5. A system, comprising:

(a) a memory controller having a terminal;

(b) a plurality of memory chips, at least one of the memory chips comprising:

a terminal;

a termination circuit connectable with the terminal and configured to terminate the terminal according to a settable resistance value;

a control command port for receiving a control command signal for affecting accessibility of the memory chip; and

a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal;

(c) a memory bus comprising a signal line interconnecting the terminals of the memory chips and the terminal of the memory controller; and

(d) a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal of the respective memory chip with the set resistance value in response to the termination signal,

wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal of the respective memory chip with the set resistance value after a first time delay; and (ii) does not terminate the terminal of the respective memory chip in accordance with a second time delay, the first time delay being sufficient to set the resistance value.

6. The system of claim **5**, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.

7. The system of claim **6**, wherein the control circuit sets the first switchover time as a function of the first time delay, and sets the second switchover time as a function of the second time delay.

8. The system of claim **7**, wherein the control circuit sets the resistance value to the first resistance value as a function of the control command signal substantially simultaneously with the switching on of the termination of the terminal of the respective memory chip, and sets the resistance value to the second resistance value substantially simultaneously with the ending of the termination of the terminal of the respective memory chip.

9. A method for operating a memory chip, comprising:

receiving a control command signal for affecting accessibility of the memory chip;

setting a resistance value for a terminal as a function of the control command signal;

terminating the terminal with the resistance value, wherein terminating comprises at least one of: beginning the terminating after a first time delay relative to the termination enable signal and stopping the terminating after a second time delay relative to the termination enable signal, the first time delay being selected such that the selected terminating resistor can be set; and

receiving a termination enable signal, the presence of which is required for the terminating to occur.

10. The method of claim **9**, further comprising:

changing the resistance value after a predetermined first switchover time relative to receiving a predetermined command represented by the control command signal; and

terminating the terminal with the changed resistance value.

* * * * *

EXHIBIT 4

US006701473B2

(12) **United States Patent**
Nygren et al.

(10) **Patent No.: US 6,701,473 B2**
(45) **Date of Patent: Mar. 2, 2004**

(54) **ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT COMPONENT OF THE ELECTRICAL CIRCUIT**

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(52) **U.S. Cl.** **714/724**

(58) **Field of Search** 714/724

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(57) **ABSTRACT**

The electrical circuit includes a plurality of circuit components which are connected via a bus. At least one of the circuit components can be tested independently of the other circuit components. The circuit component which is to be tested and the method for testing the circuit component are distinguished in that steps are taken to ensure that, during testing, the circuit component which is tested, outputs no data to the bus, and/or instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus.

38 Claims, 2 Drawing Sheets

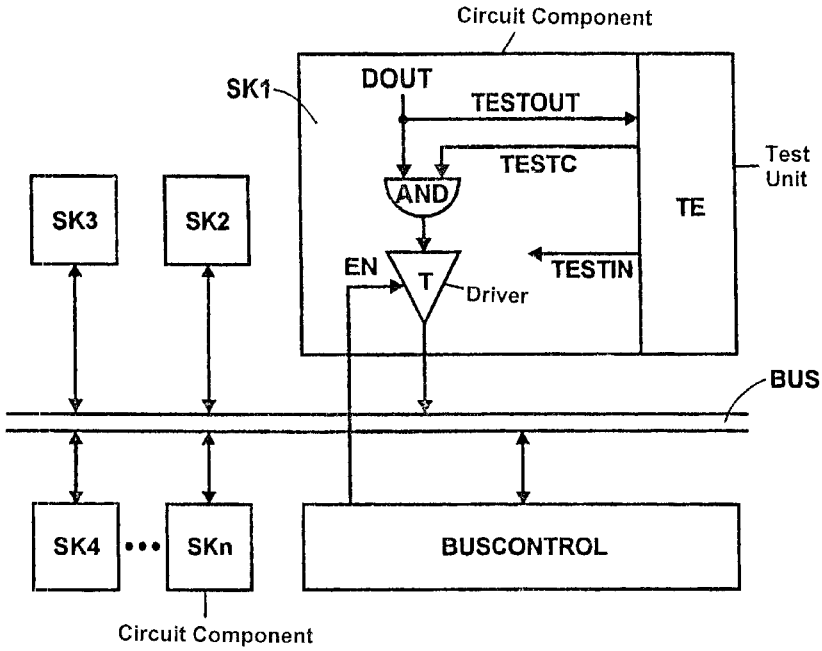


FIG 1

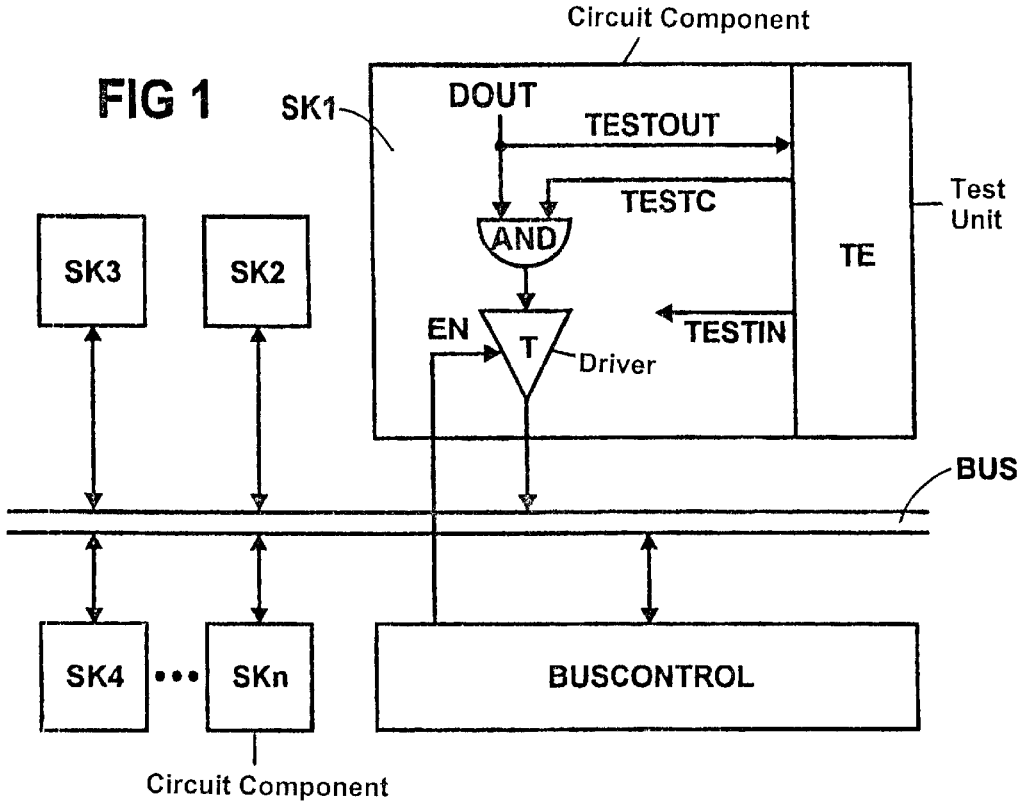
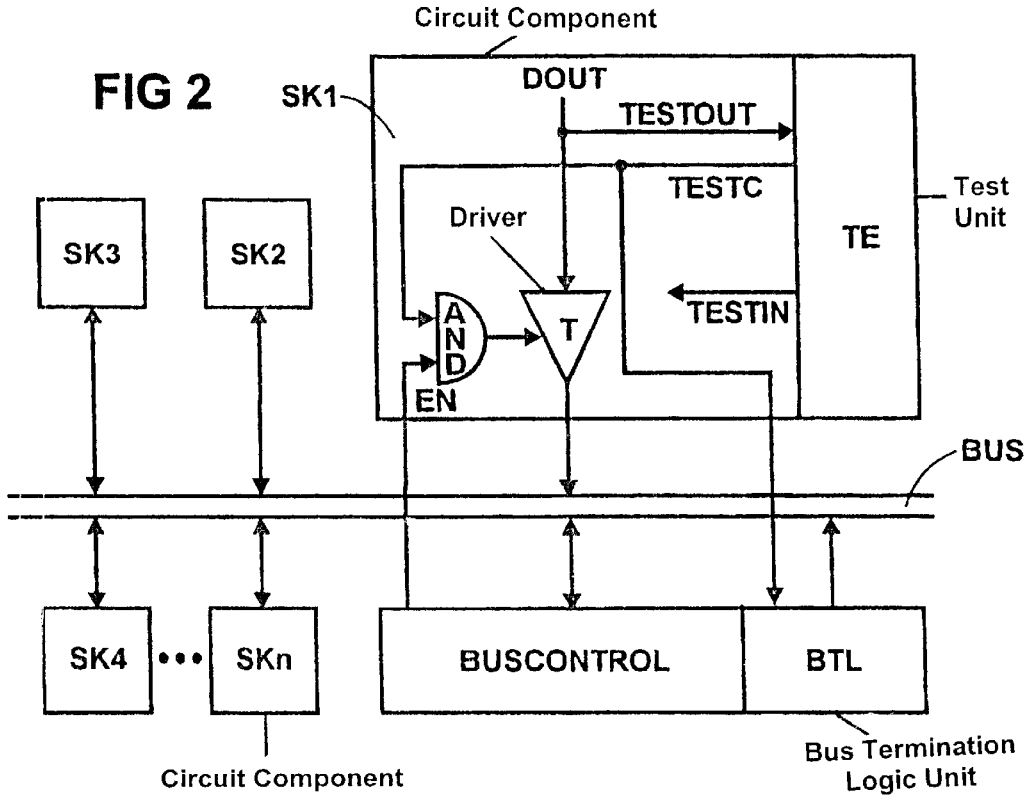

Circuit Component
SK1
DOUT
TESTOUT
TESTC
AND
TE
Test Unit
SK3
SK2
EN
T
Driver
TESTIN
BUS
SK4
SKn
BUSCONTROL
Circuit Component

FIG 2


Circuit Component
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EN
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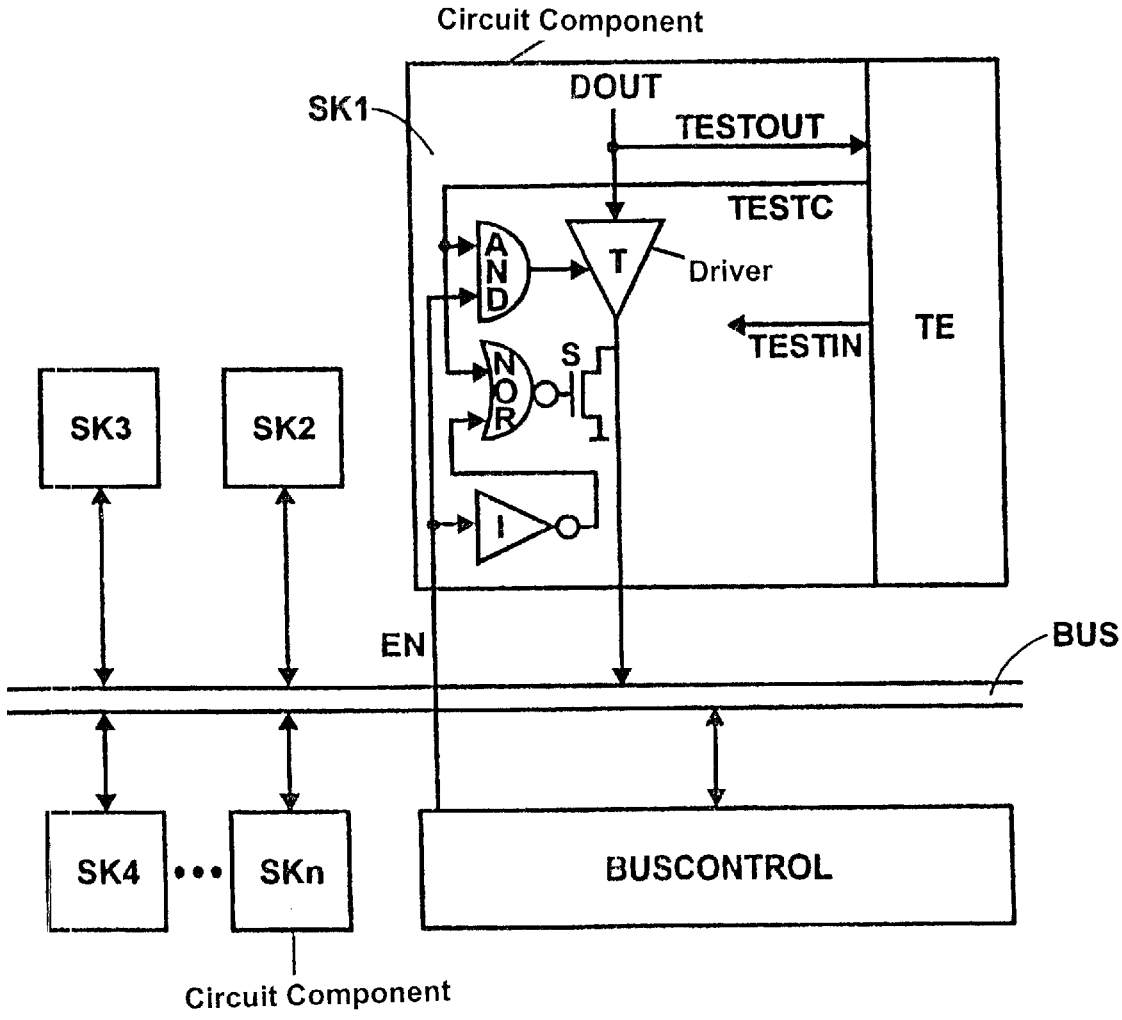
SK4
SKn
BUSCONTROL
BTL
Circuit Component
Bus Termination Logic Unit


Circuit Component
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I
EN
BUS
SK4
SKn
BUSCONTROL
Circuit Component

FIG 3

ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT COMPONENT OF THE ELECTRICAL CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an electrical circuit having circuit components that are connected through a bus where at least one of the circuit components can be tested independently of the other circuit components. Additionally, the present invention relates to a method for testing a circuit component that is connected to other circuit components through a bus, where the circuit component that is to be tested, can be tested independently of the other circuit components.

The circuit component that is to be tested is, by way of example, a so-called macro of an integrated circuit. When testing an integrated circuit, particular macros need or are intended to be tested individually, i.e. independently of the other circuit components of the integrated circuit.

Although only a relatively small part of the integrated circuit is tested during such tests, such tests are frequently relatively complex, particularly on account of the very high currents that can flow through the integrated circuit during testing, and on account of the associated extreme evolution of heat. For the aforementioned reasons, unreliable test results are sometimes also obtained.

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide an electrical circuit having circuit components that are connected through a bus and a method of testing at least one of the circuit components independently of the other circuit components which overcomes the above-mentioned disadvantageous of the prior art electrical circuits and methods of this general type, and in which the circuit components that are to be tested, can be reliably tested with a minimum amount of effort.

With the foregoing and other objects in view there is provided, in accordance with the invention an electrical circuit that includes a bus; and a plurality of circuit components which are connected via the bus. At least one of the plurality of circuit components defines a circuit component to be tested and is configured to be tested independently from all others of the plurality of circuit components. The circuit component to be tested is configured to perform an operation, during the testing thereof, that is selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

With the foregoing and other objects in view there is also provided, in accordance with the invention, a method for testing a circuit component which is connected to other circuit components via a bus. The method includes a step of providing a plurality of circuit components that are connected to a bus. At least one of the plurality of circuit components is configured such that it can be tested independently from all others of the plurality of circuit components, where the at least one of the plurality of circuit components defines a circuit component to be tested. While testing the circuit component to be tested, an operation is performed, with the circuit component to be tested. The operation is selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

Accordingly, the electrical circuit and the method are distinguished

in that, during testing, the at least one circuit component which can be tested independently of the other circuit components outputs no data to the bus and/or, instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus (characterizing part of patent claim **1**), and

in that steps are taken to ensure that, during testing, the circuit component which is to be tested outputs no data to the bus and/or, instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus (characterizing part of patent claim **2**).

By providing these features it is possible to ensure that the output drivers of the circuit component which is to be tested do not consume any power at all or only very little power. This is plausible for the case in which the circuit component which is to be tested outputs no data to the bus, but also applies to the case in which data are output to the bus. This is because the data which, if at all, are output to the bus by the circuit component which is tested, while it is being tested, are not the data which would be output to the bus by the tested circuit component during normal operation. The data can therefore be selected and output such that the power consumption of the output drivers is minimal.

The output drivers have a low power consumption when, amongst other things, the data which are to be output to the bus do not change or change only infrequently. The reason for this is that, in this case, the bus lines, which can have a considerable capacity and which may require relatively high currents for reloading them, particularly at high clock frequencies, need not be reloaded or need be reloaded only infrequently. Reloading of the bus lines, which is necessary infrequently or is not necessary at all, has the positive effect that the output drivers need never or need only infrequently deliver high currents. The effect achieved by this, in turn, is that, during testing, the relevant circuit component does not become nearly as hot as would be the case without the inventive measures regarding the absence of output data or the limitation on the output data.

A low power consumption by the output drivers and the associated advantages can also be achieved by providing, additionally or alternatively, for the data which need to be output to the bus to be able to be output so as to bypass the output drivers during testing. The output drivers can then be switched off or deactivated during testing.

The fact that, while it is being tested, the tested circuit component does not output data to the bus, and/or that it outputs data other than data which is output in the normal case, does not affect the test result. The circuit component which is to be tested is, of course, intended to be tested independently of the other circuit components, which means that it is not necessary for data interchange between the circuit components of the electrical circuit to take place via the bus.

The electrical circuit and the method therefore make it possible for circuit components, which are to be tested, to be reliably tested with a minimum amount of effort.

In accordance with an added feature of the invention, the circuit component to be tested includes output drivers for outputting data to the bus, the output drivers being deactivated during testing of the circuit component to be tested.

In accordance with an additional feature of the invention, the output drivers are deactivated by a test unit which is testing the circuit component to be tested.

In accordance with an another feature of the invention, a device is provided that is selected from the group consisting of a logic unit and a selection circuit. The device is for deactivating the output drivers. The device ensures: that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is supplied to the circuit component to be tested by a bus control device which controls the bus, and that during testing of the circuit component to be tested, the output drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested.

In accordance with a further feature of the invention, the device is the logic unit, and the logic unit provides an output signal resulting from a logical combination of the enable signal and a test control signal.

In accordance with a further added feature of the invention, the device is selected to be the selection circuit, the output drivers include control connections, and the selection circuit is formed by a multiplexer which selectively connects the enable signal or the test control signal to the control connections of the output driver.

In accordance with a further additional feature of the invention, a bus control device is provided for controlling the bus and for receiving a signal indicating testing of the circuit component to be tested.

In accordance with yet an added feature of the invention, during testing of the circuit component to be tested, the bus control device ensures that the bus is terminated by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components.

In accordance with yet an additional feature of the invention, the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation, and the data outputted to the bus is data selected from the group consisting of infrequently changing data and non-changing data.

In accordance with yet another feature of the invention, a device is provided that is selected from the group consisting of a logic unit and a selection circuit. The device ensures: that during normal operation of the circuit component to be tested, data that actually needs to be output to the bus are output to the bus, and that during testing of the circuit component to be tested, the data outputted to the bus is from a test unit carrying out the testing of the circuit component to be tested.

In accordance with yet a further feature of the invention, the device is selected to be the logic unit. The logic unit provides an output signal resulting from a logical combination of the data which would be output to the bus during normal operation and a test control signal. The test unit uses the test control signal to indicate that it is currently testing the circuit component to be tested.

In accordance with yet a further added feature of the invention, the device is selected to be the selection circuit. The circuit component to be tested includes output drivers for outputting data to the bus, and the selection circuit is formed by a multiplexer which selectively connects to the output drivers either the data which would be output to the bus during normal operation or the test control signal supplied by the test unit.

In accordance with yet a further additional feature of the invention, the circuit component to be tested includes output drivers for outputting data to the bus, and each one of the output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit.

In accordance with an added feature of the invention, each one of the output drivers receives an input signal that is an output signal of the respectively provided device.

In accordance with an additional feature of the invention, the circuit component to be tested includes output drivers with output connections; the operation performed by the circuit component to be tested, during testing thereof, is outputting data to the bus that is other than data which would be output to the bus during normal operation; and the outputted data are supplied to points situated between the output connections of the output drivers and the bus.

In accordance with another feature of the invention, a switching device is provided for supplying the outputted data to the points situated between the output connections of the output drivers and the bus.

In accordance with a further feature of the invention, a logic unit is provided for controlling the switching device.

In accordance with yet a further feature of the invention, the logic unit provides an output signal resulting from a logical combination of an enable signal and a test control signal.

In accordance with a concomitant feature of the invention, the switching device, when turned on, connects the points situated between the output connections of the output drivers and the bus to at least one point which has a predetermined potential.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in an electrical circuit and method for testing a circuit component of the electrical circuit, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a first illustrative embodiment of the inventive electrical circuit;

FIG. **2** shows a second illustrative embodiment of the electrical circuit; and

FIG. **3** shows a third illustrative embodiment of the electrical circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The electrical circuit described below is an integrated circuit. However, before continuing, it should be pointed out that there is no restriction to this. The electrical circuit may also be any other electrical circuit.

Referring now to the figures of the drawing in detail and first, particularly, to FIG. **1** thereof, there is shown a first illustrative embodiment of an inventive electrical circuit.

The electrical circuit shown in FIG. **1** includes circuit components (macros) SK**1**, SK**2**, . . . SKn, a bus "BUS" which connects the circuit components SK**1**, SK**2**, . . . SKn, and a bus control device BUSCONTROL which handles the control (in particular the arbitration) of the bus "BUS".

The circuit components SK**1**, SK**2**, . . . SKn include at least one circuit component which can be tested individually,

i.e. independently of the other circuit components of the electrical circuit.

In the example under consideration, this circuit component is the circuit component denoted by the reference symbol SK1.

In the example under consideration, the circuit component SK1 is a memory module, more precisely a DRAM macro. However, before continuing, it should be pointed out that there is no restriction to this. The testable circuit component as described below may also be any other circuit component.

For testing the circuit component SK1, a test unit TE is provided. In the example under consideration, this test unit is a component part of the circuit component SK1 which is to be tested. However, there is no restriction to this either. The test unit TE may also be provided outside the circuit component SK1 which is to be tested; in this context, it may be provided at random points within the electrical circuit, or else outside the electrical circuit.

The test unit TE

- inputs test data TESTIN into the circuit component SK1 which is to be tested,
- outputs test data TESTOUT from the circuit component SK1 which is to be tested,
- uses a test control signal TESTC to control the circuit component SK1 which is to be tested, and
- uses the test data TESTIN and TESTOUT to check whether the circuit component SK1 which is to be tested is operating correctly.

During normal operation of the circuit component SK1, that is to say when and so long as the circuit component SK1 is not being tested,

- data are supplied to the circuit component SK1 via the bus "BUS" and a data reception apparatus (not shown in FIG. 1), and
- the circuit component SK1 outputs data to the bus "BUS" via a multiplicity of output drivers, of which only a single output driver T is shown in FIG. 1.

In the example under consideration, the output drivers T are so-called tristate drivers and are activated and deactivated by the bus control device BUSCONTROL, more precisely by an enable signal EN output by the latter. When the output drivers T are activated, which may be the case when EN=1 in the example under consideration, they output the data supplied to them to the bus "BUS". When the output drivers T are deactivated, which may be the case when EN=0 in the example under consideration, they cannot output any data to the bus "BUS"; they are then in a high-impedance state.

During testing of the circuit component SK1,

- the test data TESTIN from the test unit TE are used by the circuit component SK1 instead of the data supplied to it via the bus "BUS",
- the data normally output to the bus "BUS" are used as test data TESTOUT for the test unit TE, and
- instead of the data normally output to the bus "BUS", other data are output to the bus.

In the example under consideration, the data which are output to the bus "BUS" while the circuit component SK1 is being tested are generated independently of the data which actually need to be output to the bus; they have the special feature that they do not change or change only very infrequently.

In the example under consideration, data which represent the level "0" are continuously output to the bus "BUS" while the circuit component SK1 is being tested.

In the example under consideration, when which data are output to the bus "BUS" is determined by a logic unit connected upstream of the output drivers T.

In the example under consideration, this logic unit includes an AND gate AND which receives as input signals the data DOUT which need to be output to the bus "BUS" during normal operation of the circuit component SK1 and the test control signal TESTC, and whose output signal is supplied to the output driver T as input signal.

During normal operation of the circuit component SK1, the test control signal TESTC has the value "1". The result of this is that the output signal from the AND gate is equivalent to the input signal DOUT of the AND gate. This means that, during normal operation of the circuit component SK1, the data DOUT which actually need to be output to the bus "BUS" are output to the bus.

During testing of the circuit component SK1, the test control signal has the value "0". The result of this is that the output signal from the AND gate has the value "0", irrespective of the value of the other input signal of the AND gate. This means that the value "0" is continuously output to the bus while the circuit component SK1 is being tested.

The fact that, while it is being tested, the circuit component SK1 outputs data which never change or change only infrequently to the bus "BUS" has the positive effect that the bus lines need never be reloaded or need be reloaded only infrequently. This is advantageous because

- the output drivers T consequently consume only relatively little power, and
- the output drivers T and hence also the circuit component SK1 do not heat up excessively.

The low power consumption of the electrical circuit during testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK1 which is to be tested can be reliably tested with a minimum of effort. In particular, it means that

- the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept small, and
- it is a comparatively simple matter to carry out low-temperature tests.

The fact that the data DOUT which actually need to be output to the bus "BUS" are not output to the bus while the circuit component SK1 is being tested, but instead other data are output to the bus, has no negative effect on the test result. The circuit component SK1 which is to be tested is, of course, intended to be tested independently of the other circuit components of the electrical circuit, so that it is unimportant whether, and possibly which, data are output to the bus by the circuit component SK1.

The fact that the circuit component SK1 outputs data to the bus "BUS" is nevertheless found to be advantageous. If the circuit component SK1 were to automatically deactivate its output drivers (put them into the high-impedance state) during testing, this could lead to problems. In general, this is because the components connected to the bus "BUS" are not intended to (must not) ever, or possibly only to briefly, have all of the output drivers put into the high-impedance state at the same time. The bus "BUS" is intended to (must) be continually terminated by precisely one of the components which are connected to it.

This problem does not arise in the present case, however. This means that the bus control device BUSCONTROL can continue to operate unchanged while the circuit component SK1 is being tested, and can retain exclusive control via the bus "BUS". This in turn makes it possible for a plurality of circuit components of the electrical circuit to be tested at the same time.

It ought to be clear that it is not imperative for data continuously representing the level "0" to be output to the bus "BUS" while the circuit component SK1 is being tested. Data continuously representing the level "1" can also be output to the bus "BUS". Furthermore, provision may be made for data which do not continuously have one predetermined level, but instead change, to be output to the bus "BUS" while the circuit component SK1 is being tested. In this case, the important factor is that the data which are output to the bus change only relatively infrequently, and thus it is essentially possible to attain the same advantageous effects as in the case when data which do not change are output to the bus.

It should likewise be clear that the logic unit used to generate the data which need to be output to the bus does not necessarily have to be an AND gate AND of the design and arrangement described. There are innumerable other options for this: by way of example, a NAND gate may be used instead of the AND gate AND. As another example, a multiplexer can be used to selectively connect, to the output driver T, the data DOUT which need to be output during normal operation or data which need to be output during testing.

The electrical circuit can alternatively be designed such that, while it is being tested, the circuit component which is to be tested outputs no data to the bus.

An illustrative embodiment of such an electrical circuit is shown in FIG. **2** and is described below with reference thereto.

The electrical circuit shown in FIG. **2** is largely consistent with the electrical circuit shown in FIG. **1**. Like the electrical circuit shown in FIG. **1**, it (the electrical circuit shown in FIG. **2**) includes circuit components (macros) SK1, SK2, . . . SKn, a bus "BUS" which connects the circuit components SK1, SK2, . . . SKn, and a bus control device BUSCONTROL which handles the control (in particular the arbitration) of the bus "BUS". Of the circuit components present SK1, SK2, . . . SKn, the intention is also again for the circuit component denoted by the reference symbol SK1 to be tested individually, i.e. independently of the other circuit components of the electrical circuit. The circuit component which is to be tested is tested by a test unit TE which, like the test unit TE provided in the electrical circuit shown in FIG. **1**, is contained in the circuit component which is to be tested, i.e. the circuit component SK1. To this extent, the electrical circuit shown in FIG. **2** is equivalent to the electrical circuit shown in FIG. **1**.

Unlike the circuit component SK1 shown in FIG. **1**, however, the circuit component SK2 shown in FIG. **2** outputs no data to the bus "BUS" while it is being tested.

In the example under consideration, this is achieved in that the (control) connections of the output drivers T (which are also present in the circuit component SK1 shown in FIG. **2**), which connections can be used to activate and deactivate the output drivers, no longer have the enable signal EN which is output by the bus control device BUSCONTROL applied to them, but instead have the output signal from a logic unit connected upstream of the control connection applied to them.

In the example under consideration, this logic unit includes an AND gate AND which receives as input signals, the enable signal EN and the test control signal TESTC which is also provided in the electrical circuit shown in FIG. **2**. The output signal of the AND gate AND is used to control the output drivers T.

During normal operation of the circuit component SK1, the test control signal TESTC has the value "1". The result of this is that, during normal operation of the circuit component SK1, the signal used to control the output drivers corresponds to the enable signal EN.

During testing of the circuit component SK1, the test control signal has the value "0". The result of this is that the signal used to control the output drivers T continuously has the value "0" while the circuit component SK1 is being tested, as a result of which the output drivers T are deactivated and cannot output data to the bus "BUS".

Unlike in the electrical circuit shown in FIG. **1**, in the electrical circuit shown in FIG. **2**, the test control signal TESTC is not supplied only to the circuit component SK1 which is to be tested, but also to a bus termination logic unit BTL, which is a component part of the bus control device BUSCONTROL in the example under consideration.

The bus termination logic unit BTL ensures that, during testing of the circuit component SK1 (when and so long as the test control signal TESTC is signaling that the circuit component SK1 is currently being tested), the bus "BUS" is terminated by one of the other components connected to the bus "BUS". In the example under consideration, the bus termination logic unit BTL terminates the bus "BUS" itself if required. Alternatively, provision could be made for the bus termination logic unit BTL to activate the output drivers of one of the other circuit components connected to the bus "BUS" while the circuit component SK1 is being tested, and for it then to have these circuit components terminate the bus.

It ought to be clear that the logic unit used to generate the control signal for controlling the output drivers T need not necessarily be an AND gate AND of the design and arrangement described. There are innumerable other options for this: by way of example, a NAND gate may be used instead of the AND gate AND, or else a multiplexer which is used to selectively connect the enable signal EN or the test control signal TESTC to the control connection of the output drivers T.

The fact that no data are output to the bus "BUS" while the circuit component SK1 is being tested has the positive effect that the output drivers T have no or only a negligibly low power consumption and consequently do not heat up at all, or heat up only to a very small extent.

The low power consumption of the electrical circuit during testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK1 which is to be tested can be reliably tested with a minimum of effort. In particular, this means that

- the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept small, and
- it is a comparatively simple matter to carry out low-temperature tests.

These advantages are even more pronounced in the electrical circuit shown in FIG. **2** than is the case in the electrical circuit shown in FIG. **1**.

The electrical circuit shown in FIG. **3** and described below with reference thereto permits the advantage of the electrical circuit shown in FIG. **1**, namely that, during testing of the circuit component which is to be tested, the bus is terminated, as may be necessary, by the actual circuit component which is to be tested, to be combined with the advantage of the electrical circuit shown in FIG. **2**, namely that the output drivers of the circuit component which is to be tested have no or only a negligibly low power consumption while the circuit component is being tested.

The electrical circuit shown in FIG. **3** is largely consistent with the electrical circuits shown in FIGS. **1** and **2**. Like the

electrical circuits shown in FIGS. **1** and **2**, it (the electrical circuit shown in FIG. **3**) includes circuit components (macros) SK**1**, SK**2**, . . . SKn, a bus "BUS" which connects the circuit components SK**1**, SK**2**, . . . SKn, and a bus control device BUSCONTROL which handles the control (in particular the arbitration) of the bus "BUS". Of the circuit components present SK**1**, SK**2**, . . . SKn, the intention is also again for the circuit component denoted by the reference symbol SK**1** to be tested individually, i.e. independently of the other circuit components of the electrical circuit. The circuit component which is to be tested is tested by a test unit TE which, like the test unit TE provided in the electrical circuits shown in FIGS. **1** and **2**, is contained in the circuit component which is to be tested, i.e. the circuit component SK**1**. To this extent, the electrical circuit shown in FIG. **3** is equivalent to the electrical circuits shown in FIGS. **1** and **2**.

Like the circuit component SK**1** shown in FIG. **1** and by contrast with the circuit component SK**1** shown in FIG. **2**, the circuit component SK**1** shown in FIG. **3** outputs data to the bus "BUS" as required (particularly when the circuit component SK**1** is determined by the bus control device BUSCONTROL as bus master) while the circuit component SK**1** is being tested.

In the example under consideration, however, this is done not by means of the output drivers T, which are also present for the circuit component SK**1** shown in FIG. **3**, but rather by applying a predetermined potential or potential profile to points situated between the output connections of the output drivers T and the bus "BUS".

In the example under consideration, the predetermined potential is ground potential. It may also be any other potential and also a potential which changes over time, however.

In the example under consideration, a predetermined potential or potential profile is applied to the points situated between the output connections of the output drivers T and the bus "BUS" by means of a switching device S, which in the present case is formed by a transistor. In this context, it is basically unimportant what type of transistor this is. Instead of the transistor, any other switching device may also be used, for example a so-called transmission gate.

The switching device S is controlled by a logic unit. In the example under consideration, this logic unit includes a NOR gate NOR and an inverter I, with the NOR gate NOR receiving a test control signal TESTC and an enable signal EN inverted by the inverter I as input signals, and the output signal from the NOR gate NOR being used to control the switching device S.

The test control signal TESTC and the enable signal EN are consistent with the signals of the same name in the electrical circuits shown in FIGS. **1** and **2**.

The output drivers T of the circuit component SK**1** which is to be tested are deactivated while the circuit component is being tested. In the example under consideration, this is achieved in that the (control) connections of the output drivers T, which connections can be used to activate and deactivate the output drivers, have the output signal from a logic unit which is connected upstream of the control connection applied to them, as in the case of the electrical circuit shown in FIG. **2**.

In the example under consideration, as in the case of the electrical circuit shown in FIG. **2**, this logic unit includes an AND gate AND which receives the test control signal TESTC and the enable signal EN as input signals, and whose output signal is used to control the output drivers T.

The switching device S, which controls the termination of the bus "BUS", and the output drivers T are controlled by the logic units AND and I/NOR such that the following conditions are established as a result:

TESTC	EN	Action
0	0	Test mode Output drivers deactivated Termination inactive
0	1	Test mode Output drivers deactivated Termination active
1	0	Normal operation Output drivers deactivated
1	1	Normal operation Output drivers activated

The electrical circuit shown in FIG. **3**

has the advantages, as compared with the electrical circuit shown in FIG. **1**,

that the path via which the data DOUT are output during normal operation contains no additional logic unit, which means that data can be output more quickly, and

that the output drivers are deactivated during testing of the circuit component which is to be tested, which means that they consume less power during testing and consequently also heat up to a lesser extent, and

has the advantage, as compared with the electrical circuit shown in FIG. **2**, that the circuit component which is to be tested terminates the bus itself, which means that it is possible to dispense with the bus termination logic unit BTL or similar devices.

Furthermore, this is achieved without having to accept significant disadvantages as compared with the electrical circuits shown in FIGS. **1** and **2**.

It ought to be clear that the logic units used to generate the control signals for controlling the output drivers T and the switching device S need not necessarily be designed and arranged as described. There are innumerable other options for this.

The fact that the output drivers T are deactivated while the circuit component SK**1** is being tested has the positive effect that they have no or only a negligibly low power consumption and consequently do not heat up at all or heat up only to a very small extent.

The low power consumption of the electrical circuit during testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK**1** which is to be tested can be reliably tested with a minimum of effort. In particular, it means that

the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept small, and

it is a comparatively simple matter to carry out low-temperature tests.

The precautions taken for testing the circuit component which is to be tested do not in any way impair it during normal operation. In particular, there is no need for concern about any kind of effects on the operating speed and the other essential properties of the circuit component which is to be tested.

A common feature of the electrical circuits described, independently of the details of the practical implementation, is that they provide an amazingly simple way of reliably testing circuit components which are to be tested with a minimum of effort.

We claim:

1. An electrical circuit comprising:

a bus; and

a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;

said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.

2. The electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested.

3. The electrical circuit according to claim 2, wherein said output drivers are deactivated by a test unit which is testing said circuit component to be tested.

4. The electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring:

that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus, and

that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested.

5. The electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal.

6. The electrical circuit according to claim 4, wherein said device is said selection circuit, said output drivers include control connections, and said selection circuit is formed by a multiplexer which selectively connects the enable signal or the test control signal to said control connections of said output driver.

7. The electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested.

8. The electrical circuit according to claim 7, wherein, during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by a device selected from the group consisting of said bus control device and one of said others of said plurality of circuit components.

9. The electrical circuit according to claim 1, wherein the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is data selected from the group consisting of infrequently changing data and non-changing data.

10. The electrical circuit according to claim 9, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device ensuring:

that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus, and

that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested.

11. The electrical circuit according to claim 10, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the data which would be output to said bus during normal operation and a test control signal, said test unit using said test control signal to indicate that it is currently testing said circuit component to be tested.

12. The electrical circuit according to claim 10, wherein said device is said selection circuit, said circuit component to be tested includes output drivers for outputting data to said bus, said selection circuit is formed by a multiplexer which selectively connects to said output drivers either the data which would be output to said bus during normal operation or said test control signal supplied by said test unit.

13. The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for outputting data to said bus, and each one of said output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit.

14. The electrical circuit according to claim 13, wherein each one of said output drivers receives an input signal that is an output signal of said respectively provided device.

15. The electrical circuit according to claim 1, wherein:

said circuit component to be tested includes output drivers with output connections;

the operation performed by said circuit component to be tested, during testing thereof, is outputting data to said bus that is other than data which would be output to said bus during normal operation; and

the outputted data are supplied to points situated between said output connections of said output drivers and said bus.

16. The electrical circuit according to claim 15, comprising a switching device for supplying the outputted data to said points situated between said output connections of said output drivers and said bus.

17. The electrical circuit according to claim 16, comprising a logic unit for controlling said switching device.

18. The electrical circuit according to claim 17, wherein said logic unit provides an output signal resulting from a logical combination of an enable signal and a test control signal.

19. The electrical circuit according to claim 16, wherein said switching device, when turned on, connects said points situated between said output connections of said output drivers and said bus to at least one point which has a predetermined potential.

20. A method for testing a circuit component which is connected to other circuit components via a bus, the method which comprises:

providing a plurality of circuit components that are connected to a bus;

configuring at least one of the plurality of circuit components such that it can be tested independently from all others of said plurality of circuit components, the at least one of the plurality of circuit components defining a circuit component to be tested; and

while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

21. The method according to claim 20, which comprises:

providing the circuit component to be tested with output drivers for outputting data to the bus; and

deactivating the output drivers during testing of the circuit component to be tested.

22. The method according to claim 21, which comprises deactivating the output drivers by a test unit which is testing the circuit component to be tested.

23. The method according to claim 22, which comprises:

providing a device for deactivating the output drivers;

selecting the device from the group consisting of a logic unit and a selection circuit;

using the device to ensure:

that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is supplied to the circuit component to be tested by a bus control device which controls the bus, and

that during testing of the circuit component to be tested, the output drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested.

24. The method according to claim 23, which comprises using the logic unit to provide an output signal resulting from a logical combination of the enable signal and a test control signal.

25. The method according to claim 23, which comprises providing the output drivers with control connections, and forming the selection circuit by a multiplexer which selectively connects the enable signal or the test control signal to the control connections of the output driver.

26. The method according to claim 20, which comprises signaling a bus control device which controls the bus that the circuit component to be tested is undergoing a test.

27. The method according to claim 26, which comprises using the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components.

28. The method according to claim 20, wherein the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation, and selecting the data output to the bus from the group consisting of infrequently changing data and non-changing data.

29. The method according to claim 28, which comprises:

selecting a device from the group consisting of a logic unit and a selection circuit;

using the device to ensure:

that during normal operation of the circuit component to be tested, data that actually needs to be output to the bus are output to the bus, and

that during testing of the circuit component to be tested, the data outputted to the bus is from a test unit carrying out the testing of the circuit component to be tested.

30. The method according to claim 29, which comprises:

selecting the device to be the logic unit;

constructing the logic unit to provide an output signal resulting from a logical combination of the data which would be output to the bus during normal operation and a test control signal; and

using the test control signal, by the test unit, to indicate that the test unit is currently testing the circuit component to be tested.

31. The method according to claim 29, which comprises:

selecting the device to be the selection circuit;

providing the circuit component to be tested with output drivers for outputting data to the bus;

forming the selection circuit by a multiplexer which selectively connects to the output drivers either the data which would be output to the bus during normal operation or the test control signal supplied by the test unit.

32. The method according to claim 29, which comprises:

providing the circuit component to be tested with output drivers for outputting data to the bus; and

providing each one of the output drivers with a device that is selected from the group consisting of a logic unit and a selection circuit.

33. The method according to claim 32, wherein each one of the output drivers receives an input signal that is an output signal of the respectively provided device.

34. The method according to claim 20, wherein:

the circuit component to be tested is provided with output drivers having output connections;

the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation; and

the outputted data are supplied to points situated between the output connections of the output drivers and the bus.

35. The method according to claim 34, which comprises providing a switching device for supplying the outputted data to the points situated between the output connections of the output drivers and the bus.

36. The method according to claim 35, which comprises controlling the switching device with a logic unit.

37. The method according to claim 36, wherein the logic unit provides an output signal resulting from a logical combination of an enable signal and a test control signal.

38. The method according to claim 36, wherein the switching device, when turned on, connects the points situated between the output connections of the output drivers and the bus to at least one point which has a predetermined potential.

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