UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,145,369

Case No. IPR2023-00514

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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1001	U.S. Patent No. 7,145,369 (the "'369 Patent")
1002	Prosecution history of the '369 Patent
1003	Declaration of Dr. R. Jacob Baker
1004	Curriculum Vitae of Dr. R. Jacob Baker
1005	U.S. Patent No. 6,549,036 to Lee ("Lee")
1006	U.S. Patent No. 6,330,194 to Thomann ("Thomann")
1007	JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79 ("JESD79")
1008	U.S. Patent No. 6,094,075 to Garrett ("Garrett")
1009	Declaration of Julie Carlson and Exhibits regarding JESD79
1010	U.S. Patent No. 5,254,883 to Horowitz ("Horowitz")
1011	U.S. Patent No. 4,665,326 to Domogalla ("Domogalla")
1012	Excerpts of CMOS: Circuit Design, Layout, and Simulation, 2nd Edition (IEEE Press) (2005)
1013	U.S. Patent Publication No. US2003/0052369 A1 to Kajimoto ("Kajimoto")
1014	U.S. Patent No. 6,985,037 to Veal ("Veal")
1015	First Amended Complaint, Polaris Innovations Limited v. Xilinx, Inc., 1:22-cv-00174-RGA, Docket No. 14 (April 28, 2022)
1016	UG585 (v1.11) Xilinx Zync-7000 All Programmable SoC Technical Reference Manual

Exhibit	Description
1017	Scheduling Order, Polaris Innovations Limited v. Xilinx, Inc., 1:22-cv-00174-RGA, Docket No. 20 (May 31, 2022)
1018	United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf
1019	Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.P]	An output driver for an integrated circuit, comprising:
[1.1]	a driver circuit for driving an input signal of the output driver onto an output line;
[1.2]	a measuring circuit for measuring at least one of an output line current and an output line potential; and
[1.3]	a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range,
[1.4]	wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.
Claim 2	
[2]	The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude.
Claim 3	
[3]	The output driver of claim 1, wherein the driver circuit includes a pull-up path defined by a first maximum and minimum current/potential (I/V) characteristic curve and a pull-down path defined by a second maximum and minimum I/V characteristic curve and wherein the desired power range is determined depending on respectively activated pull-up path and pull-down path of the driver circuit.

Claim 4	
[4]	The output driver of claim 1, wherein the desired power range corresponds to a lower portion of the specification-prescribed potential range and a lower portion of the specification-prescribed current range.
Claim 5	
[5]	The output driver of claim 1, wherein the driver circuit further comprises a setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit.
Claim 6	
[6]	The output driver of claim 1, wherein the control unit further comprises a comparator unit for comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value.
Claim 7	
[7]	The output driver of claim 6, wherein the control unit further comprises an evaluation unit connected to the comparator unit, the evaluation unit configured to change the control signal based upon a result from the comparator unit.
Claim 8	
[8]	The output driver of claim 7, wherein the evaluation unit comprises a counter.
Claim 14	
[14.P]	A method for driving an output driver for an integrated circuit having a driver circuit driving an input signal onto an output line, comprising:

[14.1]	measuring at least one of an output line current and an output line potential; and
[14.2]	controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range, respectively,
[14.3]	wherein the driver strength is set such that the potential and the current intensity lie in a lower power range of the specification-prescribed current range and the specification-prescribed potential range, and
[14.4]	wherein the driver strength is feedback-controlled based on a measured value provided by a measuring circuit.
Claim 15	
[15]	The method of claim 14, wherein the driver strength of the driver circuit is controlled in a manner selected from continuously, periodically and in accordance with a setting signal.
Claim 16	
[16.P]	The method of claim 14, further comprising:
[16.1]	comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value; and
[16.2]	changing a control signal for setting the driver strength supplied to the driver circuit based upon a result from the comparison.
Claim 18	

[18.P]	An output driver for an integrated circuit, comprising:
[18.1]	a driver means for driving an input signal of the output driver onto an output line; and
[18.2]	a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range of a specification-prescribed potential range and a specification-prescribed current range, the control means comprising:
[18.3]	a comparator means for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value; and
[18.4]	an evaluation means for changing the control signal based upon a comparison result from the comparator means.

I. INTRODUCTION

Xilinx, Inc. ("Xilinx" or "Petitioner") petitions for *Inter Partes* Review ("IPR") of claims 1-8, 14-16, and 18 of U.S. Patent 7,145,369 (the "'369 Patent"), assigned to Polaris Innovations Limited ("Polaris" or "Patent Owner").

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner Xilinx, Inc., Advanced Micro Devices, Inc. ("AMD"), and ATI Technologies ULC ("ATI") are the real parties-in-interest. AMD is the parent of Xilinx and ATI is an indirect, wholly owned subsidiary of AMD.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Polaris asserted the '369 Patent against Xilinx in *Polaris Innovations Ltd. v. Xilinx, Inc.*, CA 1:22-CV-00174-RGA (D. Del.), in a complaint, filed on February 8, 2022 and served on February 22, 2022, that asserts four patents, including the '369 Patent. In addition to this Petition for the '369 Patent, Xilinx is concurrently filing IPR petitions for the remaining three asserted patents: IPR2023-00513, and IPR2023-00516, IPR2023-00517.

C. Lead and Back-Up Counsel under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup Counsel
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D. Service Information

Please address all correspondence to the address above. Petitioner consents to electronic service by email at xilinxMWETeam@mwe.com.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103

Petitioner authorizes the Office to charge Deposit Account No. 50-0417 for the petition fee set in 37 C.F.R. §42.15(a) and for any other required fees.

IV. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’369 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR.

B. Challenge under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR of claims 1-8, 14-16, and 18 of the ’369 Patent on the grounds listed below. In support, this petition includes a declaration of Dr. Jacob R. Baker (EX1003).

Ground	Claims	Basis for Rejection
1	1, 2, 5-7	35 U.S.C. §103 over Lee
2	1-2, 5-7	35 U.S.C. §103 over Lee in combination with Thomann
3	1-7, 14-16	35 U.S.C. §103 over Lee in combination with JESD79
4	1-8, 14-16, 18	35 U.S.C. §103 over Lee and JESD79 in combination with Garrett

V. SUMMARY OF THE ’369 PATENT

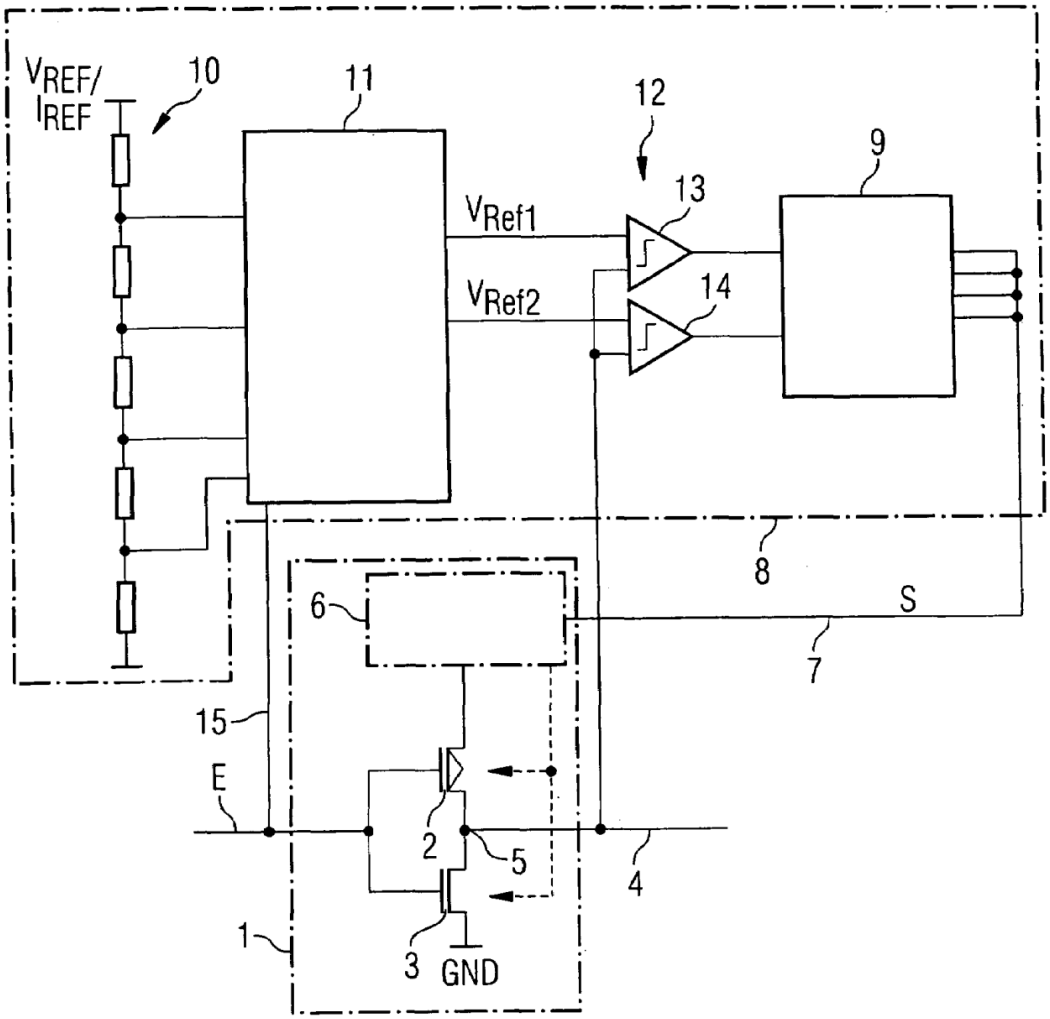
A. Brief Description

The ’369 Patent relates to an output driver for an integrated circuit. EX1001 at 1:1-2. The patent purports to reduce the power consumption of the integrated circuit. *Id.* at 1:66-2:2. This purported advancement is achieved by setting the strength of the driver using feedback control that sets a potential or current intensity at the output to a value in a desired power range of a specification-prescribed potential or current intensity range. *Id.* at 2:13-23, 7:1-3.

As shown below, the driver circuit 1 includes transistors (2, 3) to drive an input signal E to the output 5 and output line 4, which is fed back to a control unit 8 to compare the potential or voltage on the output line to reference potential(s) (at

13/14). *Id.* at 4:4-11, 4:32-40. The control unit 8, based on the comparison, generates a control signal S to setting circuit 6, which sets the driver strength based on control signal S. *Id.* at 4:18-31.

FIG 1



Further, a voltage divider 10 provides reference voltages to multiplexer 11 that correspond to a desired potential window for the output of the driver. *Id.* at 5:13-24. The multiplexer 11 selects two references, V_{Ref1} and V_{Ref2}, based on input

E, for comparison to the potential value on the output line, and an evaluation unit 9 counts based on the result of the comparison. *Id.* at 4:66-5:15, 5:25-30.

Figures 2a and 2b, below, show minimum (Imin), maximum (Imax), and nominal (Inom, max and Inom,min) current-voltage characteristic curves for the pull-down and pull-up paths of the driver. *Id.* at 3:64-67. The prescribed range, provided in a current-voltage window, spans between Imin and Imax. *Id.* at 6:15-18, 6:24-26. A lower range for reduced power consumption is defined within the permissible range. *Id.* at 6:27-37. For example, a tolerance magnitude is added to Imin, as shown by the Inom,min curves. *Id.* at 6:38-42; *see also* EX1003, ¶¶36-40.

FIG 2A

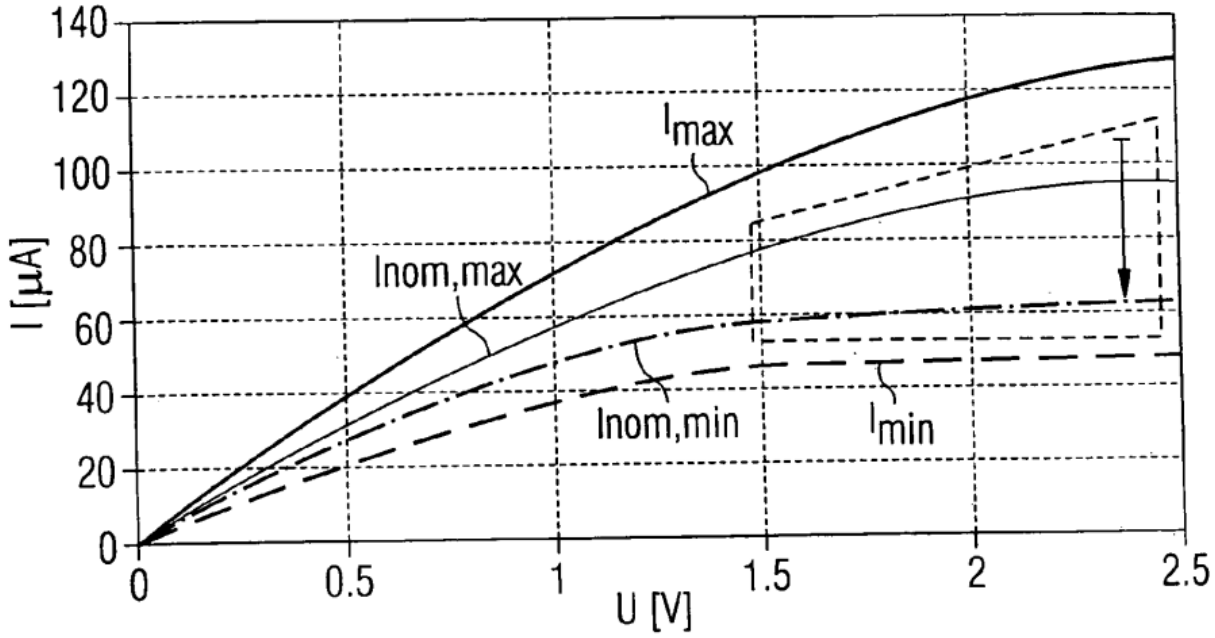
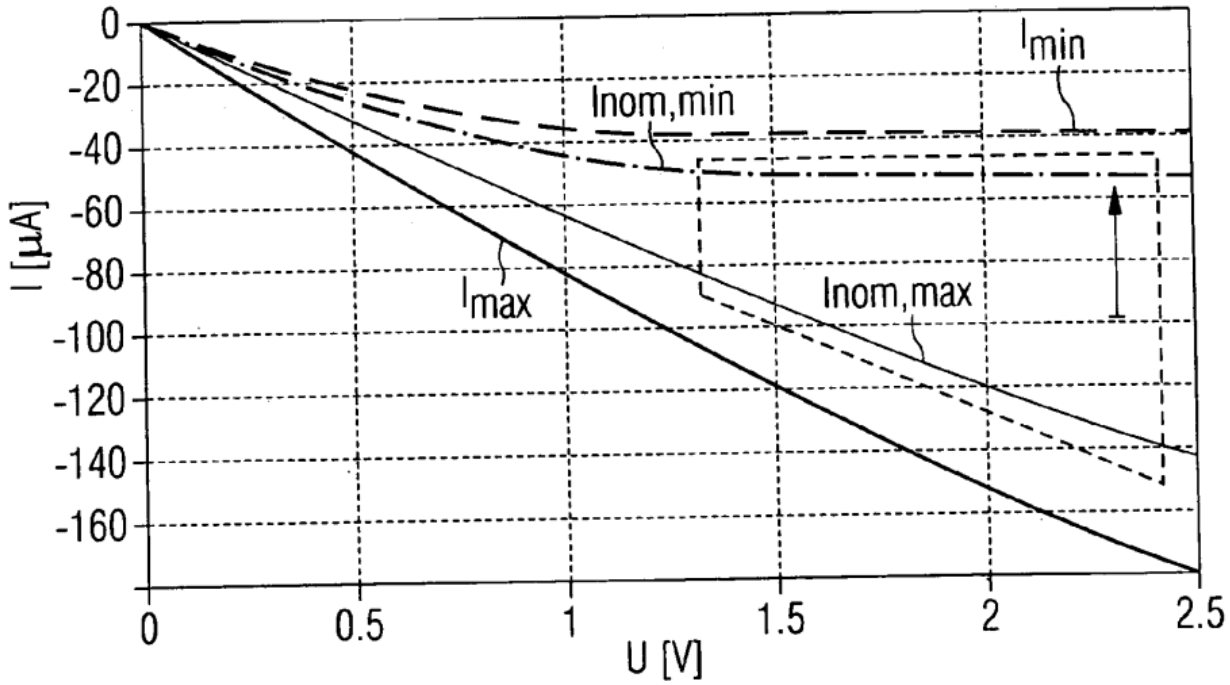

140
120
100
80
60
40
20
0
I [µA]
0
0.5
1
1.5
2
2.5
U [V]
Imax
Inom,max
Inom,min
Imin

FIG 2B


0
-20
-40
-60
-80
-100
-120
-140
-160
I [µA]
0
0.5
1
1.5
2
2.5
U [V]
Imin
Inom,min
Imax
Inom,max

B. Summary of the Prosecution

The ’369 Patent was filed as Application No. 10/887,949 (the “’949 Application”) on July 9, 2004 (“U.S. Filing Date”). The ’949 Application claims priority to DE10331607, filed July 12, 2003 (“Priority Date”), and listed 20 claims. EX1002, 3; EX1001, 1.

During prosecution, the applicant amended claim 6 to recite that “the control unit” comprises “a comparator unit,” and argued that the cited references did not disclose a “driver circuit,” “driver,” or “control signal for setting a driver strength.” EX1002, 148-52, 164, 167-70.

Thereafter, the examiner rejected claims 1-6 and 14-17 as anticipated by US Patent Application No. 2003/0052369 to Kajimoto. To obtain allowance, the applicant amended claims 1 and 14 to require feedback control and argued that Kajimoto discloses feed-forward control. *Id.*, 183, 187; *see* EX1013; *see also* EX1002, 198 (reasons for allowance); EX1003, ¶¶43-46.

VI. THE BOARD SHOULD NOT DISCRETIONARILY DENY INSTITUTION

A. Section 325(d)

Advanced Bionics and §325(d) do not support discretionary denial. The references and combinations cited by Petitioner, which disclose feedback control, were not presented to the Office, and no similar references were evaluated during

prosecution. Denial under §325(d) is thus unwarranted. *See Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18 at 8-9 (PTAB Aug. 12, 2021).

B. Fintiv (Section 314(a))

The *Fintiv* factors favor institution. This petition presents compelling evidence showing the unpatentability of the challenged claims, and thus institution should not be discretionarily denied under *Fintiv*. Although there is a case pending with Xilinx involving the ’369 Patent, it remains at an early stage. Initial discovery and contentions have been served, but the parties have not briefed or argued claim construction, and any final written decision will likely be issued before trial. The current trial date is November 18, 2024 and the median time-to-trial for the Delaware court suggests trial in February 2025. EX1017, 12; EX1018, 14. Further, Xilinx intends to request a stay pending IPR. EX1019 (showing the Delaware court grants majority of motions to stay).

VII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) would have had a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and two or three years of academic or industry experience in integrated circuit input/outputs and memory systems, or comparable experience. EX1003, ¶¶31-35. Additional work experience can substitute for educational or research experience,

and vice versa. A POSITA would have been familiar with the JEDEC industry standards and knowledgeable about the design and operation of standardized DRAM memory systems and with output driver designs including digital/analog circuitry. *Id.*

VIII. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3)

Petitioner submits that all claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100.

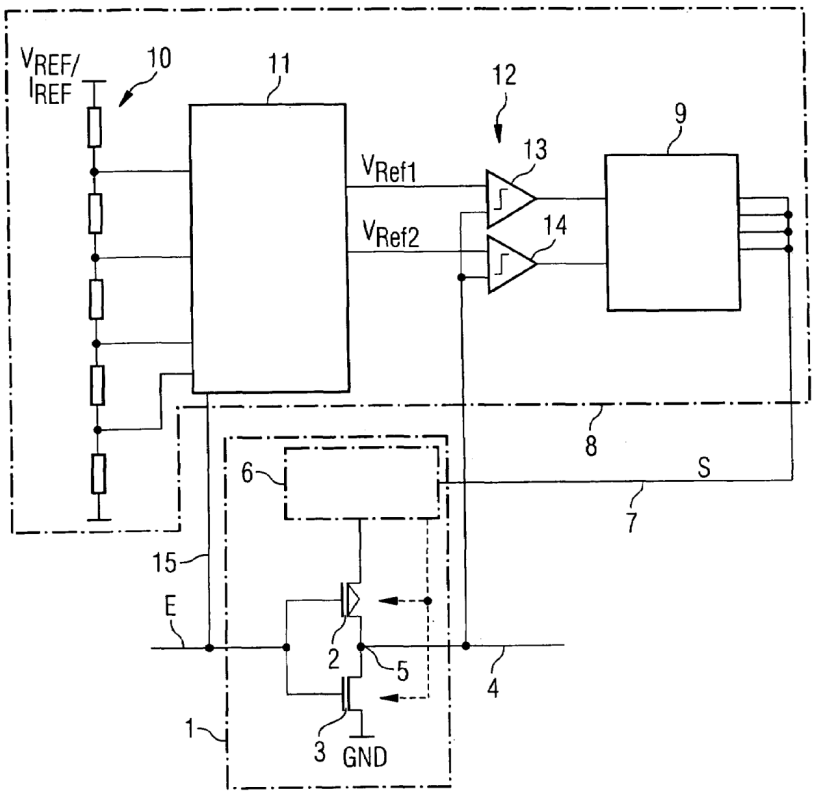
Several means-plus-function limitations in claim 18 should construed under 35 U.S.C. §112, paragraph 6. Although other claims recite similar terms ("control unit," "comparator unit," and "evaluation unit"), they do not recite the word "means," and thus are presumed not to invoke §112(6). *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc). However, if Patent Owner argues they do, the corresponding structure is the same as the similar means-plus-function limitation identified below (control, comparator, and evaluation means). *See* EX1003, ¶53.

Construction of other terms is unnecessary because it is not dispositive—the art teaches the claims under any construction. *Cf. Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

A. "driver means"

Claim [18.1] recites a driver means "*for driving an input signal of the output driver onto an output line*[1]." The corresponding structure for performing the claimed function is transistors 2 and 3 of driver circuit 1 that drive an input signal 'E,' which is coupled to the transistors' control inputs, to an output line 4:

FIG 1



EX1001 at FIG. 1, 4:4-17, 6:58-59; EX1003, ¶54.

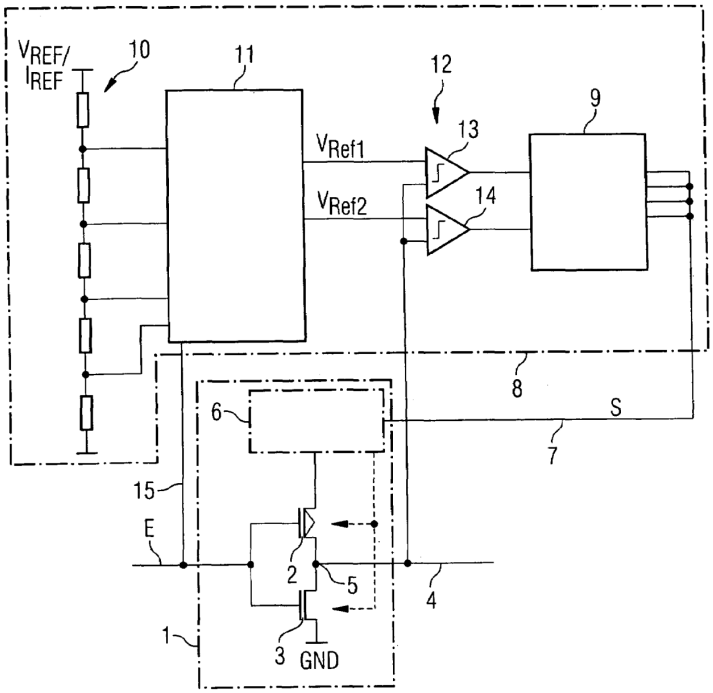
[1] The claimed function is indicated in italics unless otherwise specified.

B. "comparator means"

Claim [18.3] recites a comparator means "*for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value*." The corresponding structure is one or more comparators (13/14) of comparator unit 12 that compares the output line current and/or potential to one or more reference current and/or potential values[2]:

[2] Claim 18 does not require comparison to multiple reference values and thus only one of the two disclosed comparators corresponds to the claimed function. *Cf.* EX1001, 7:37-57, 8:21-30, 8:47-62 (claims 9-13, 17, 19-20) (reciting multiple reference potentials/voltages); EX1003, ¶55.

FIG 1

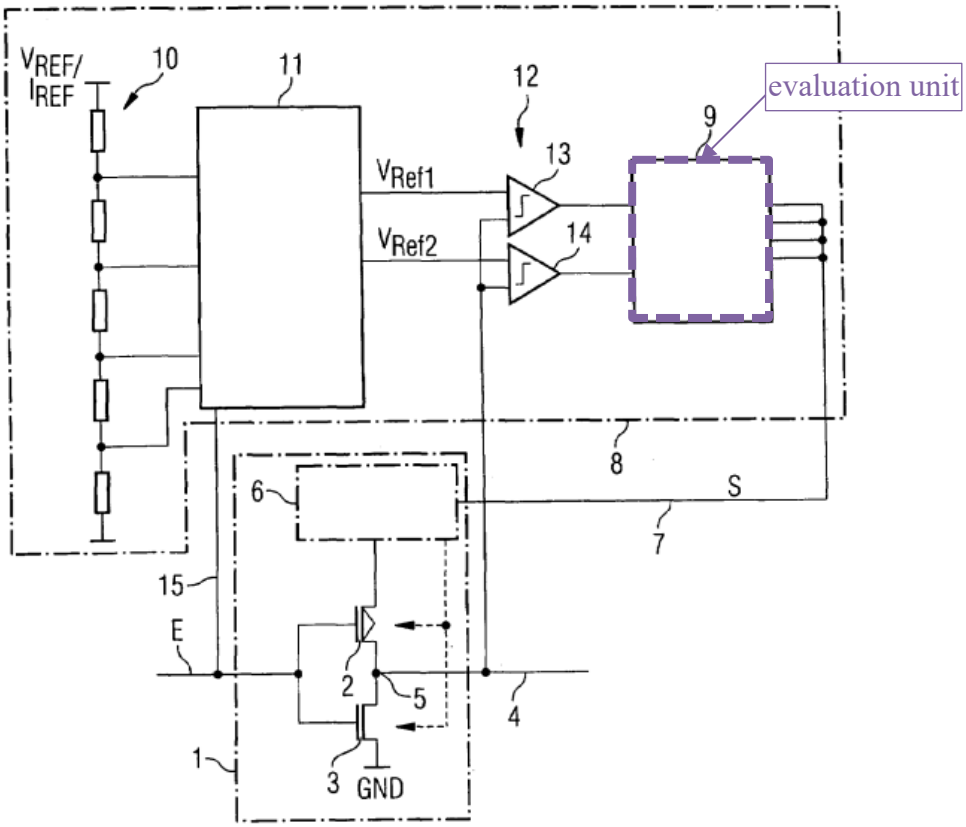


EX1001 at FIG. 1, 3:19-25, 4:41-65, 5:25-6:8; EX1003, ¶55.

C. "evaluation means"

Claim [18.4] recites an evaluation means "*for changing the control signal based upon a comparison result from the comparator means*." Shown below is an evaluation unit (9) that generally provides for the claimed function.

FIG 1



EX1001 at FIG. 1[3], 7:31-34 (claim 7); EX1003, ¶56. However, the illustrated black-box does not provide adequate support for performing the claimed function by itself. *See Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1383 (Fed. Cir. 2009) (A "black box" "is not a description of structure[.]"); EX1003, ¶56. The only other description of structure is that the black-box includes "a counter" that, based on the comparison, provides a changing control signal. *See* EX1001 at 5:25-30, 5:42-47, 7:31-36; EX1003, ¶56. Thus, a counter is the corresponding structure.

[3] The Petition adds the color annotations to figures unless otherwise stated.

D. "control means"

Claim [18.2] recites a control means "*for providing a control signal for setting a driver strength of the driver means*." The "*control means*" is comprised of the comparator and evaluation means, discussed above. *Supra* §§VIII.B-VIII.C; EX1001 at 8:34-46, FIG. 1; EX1003, ¶57. Accordingly, the corresponding structure is the combination of these two means: 1) one or more comparators that compares the output line current/potential to one or more reference current/potential values; and 2) a counter that provides a changing control signal based on the comparison result. *Id.*

IX. OVERVIEW OF THE PRIOR ART

Before the '369 Patent, techniques to adjust drive strength settings were well-known, as were solutions to adjust for output driver variations due to process, temperature, and voltage. *See* EX1003, ¶¶48-49. Indeed, many elements of the challenged claims are described in the background section of the '369 Patent. *See id.*, ¶¶41-42.

A. Lee (EX1005)

U.S. Patent No. 6,549,036 ("Lee") was filed as U.S. Application No. 09/583,884 on May 31, 2000 and issued and published on April 15, 2003. EX1005, 1. Lee is prior art under §§102(a) and 102(e) because it was filed and published

before the Priority Date and under §102(b) because it was published more than a year before the U.S. Filing Date. *See* EX1001, 1.

Lee discloses an output buffer driver with drive strength calibration for driving a bus. EX1005, 1, 2:11-19, 7:57-67, FIG. 5. As shown below, the output of the driver (11) is fed back to an input buffer (15).

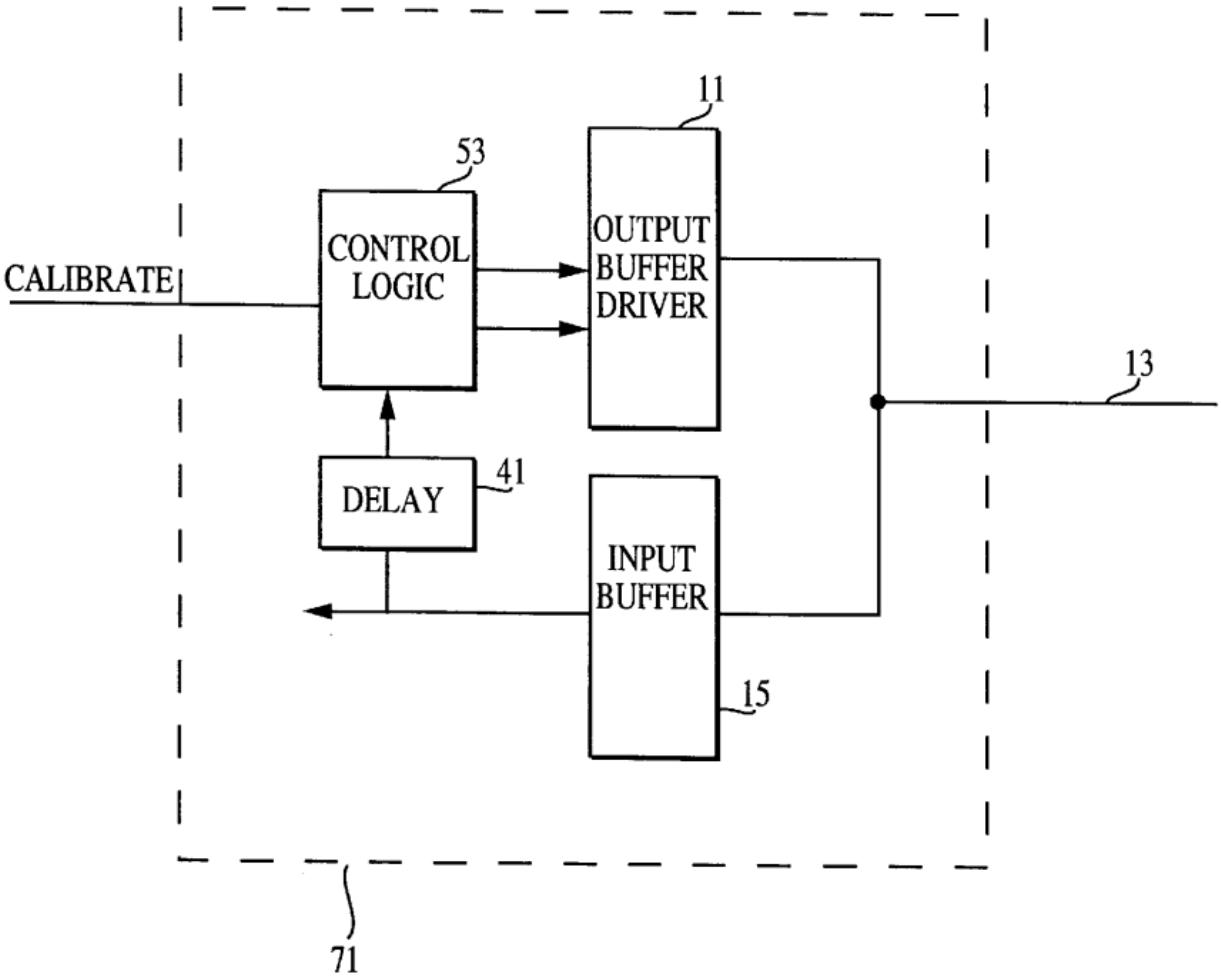


FIG. 5

The input buffer/receiver (15) compares the driver output to a reference voltage VREF.

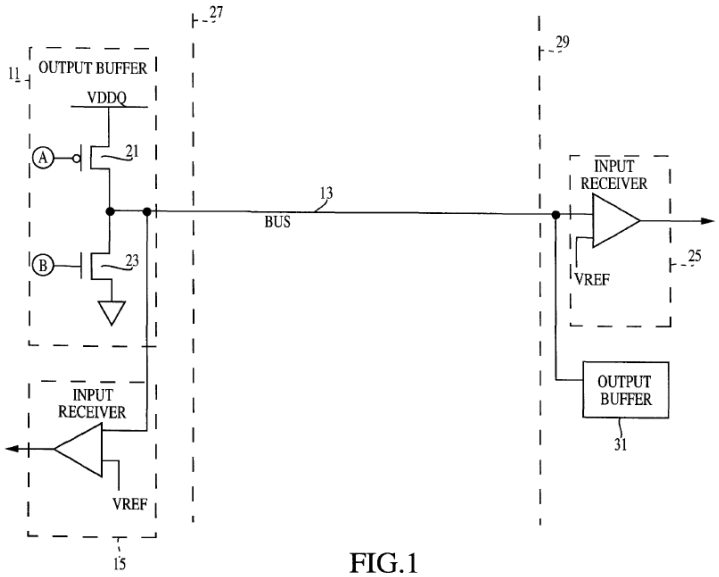


FIG.1

Id., FIG. 1. The result of the comparison is then used to adjust the drive strength setting such that the output voltage swings across a range between a high voltage VOH and low voltage VOL that are symmetric about a mid-voltage VREF. *Id.*, 3:7-24, 4:35-61, FIGS. 1-2; EX1003, ¶¶60-63.

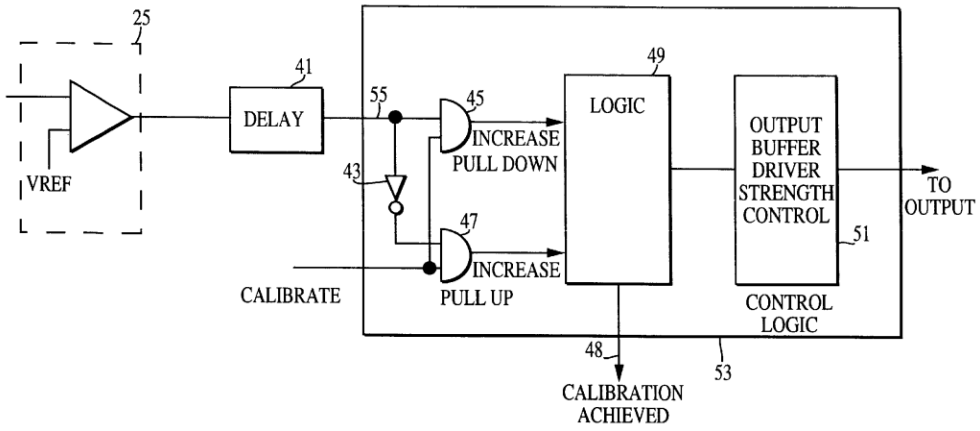


FIG. 2

Specifically, Lee increases or decreases the drive strength of the pull-up or pull-down paths of the driver by adjusting the effective width of the driver's transistors, the number of parallel transistors, or the gate fingers of the transistors. EX1005, 4:9-5:18.

B. Thomann (EX1006)

U.S. Patent No. 6,330,194 ("Thomann") was filed on June 26, 2000 and issued and published on December 11, 2001, and is prior art under §§102(a), 102(b), and 102(e). EX1006, 1; EX1001, 1.

Similar to Lee, Thomann discloses an output buffer circuit with drive strength calibration. EX1006, 1. The driver output is compared to a reference

signal VREF, and the result of the comparison is used to adjust the drive strength setting. *Id.*, 4:43-57, FIGS. 1-2; EX1003, ¶¶64-65.

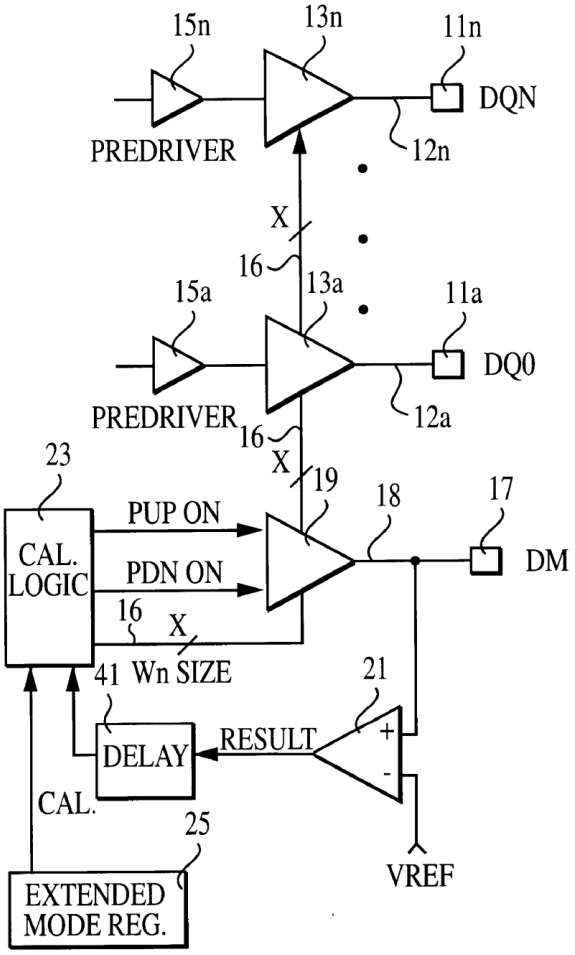


FIG. 1

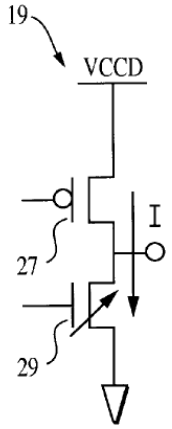


FIG. 2

Thomann also discloses that before calibration the driver may provide too much drive strength, despite the output voltage VOL DRIVER falling within the prescribed minimum and maximum potentials, VOL MIN. and VOL MAX. EX1006, 5:37-44, FIG. 3; EX1003, ¶¶66-67.

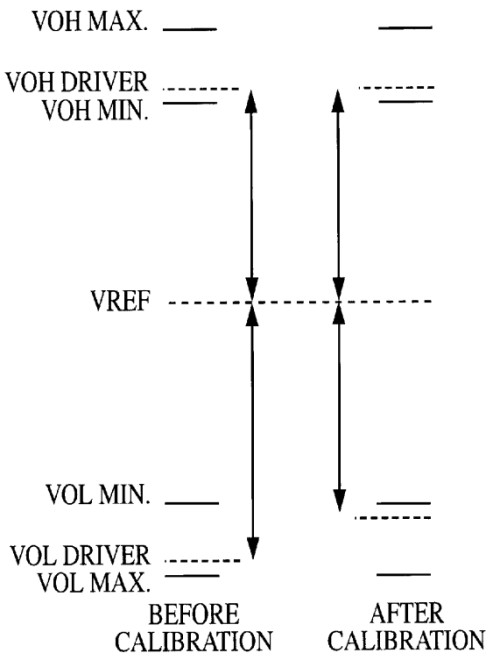


FIG. 3

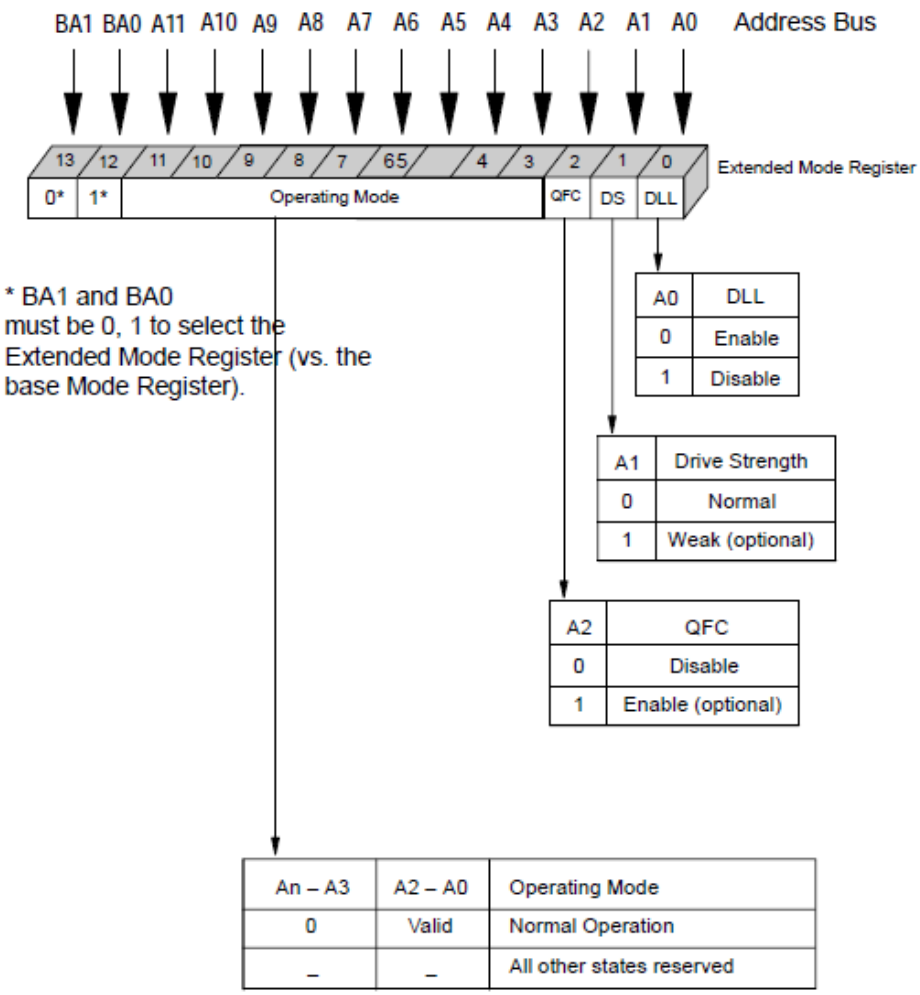
After calibration, the driver may achieve a balanced drive strength, centered around a reference voltage, VREF. EX1006, 6:18-31, FIG. 3. As shown above, the range or swing of the driver output voltage is lowered after calibration so that the VOL DRIVER value is closer to the VOH DRIVER and VOL MIN values. *Id.*

C. JESD79 (EX1007)

JEDEC's Double Data Rate (DDR) SDRAM Specification, JESD79, Release 1 ("JESD79") is prior art under §§102(a)-(b) because it is a printed publication that was publicly accessible before the Priority Date and more than a year before the U.S. Filing Date. JESD79 is a well-known standard published by the preeminent memory standards setting organization, JEDEC. EX1003, ¶68; *see SK hynix Inc. v. Netlist, Inc.*, IPR2017-00577, Paper 26 at 6 (PTAB July 5, 2018)

(JESD79 published in June 2000), *Samsung Elecs. Am., Inc. v. Goodman*, IPR2017-02021, Paper 19 at 18-19 (PTAB Oct. 29, 2019) (holding that another JEDEC standard was publicly available). In June 2000, JESD79 was "made publicly available via JEDEC's website" (EX1009, ¶14), "where they are cataloged and indexed by keyword and technological subject matter" for download for free or a fee (*id.*, ¶¶6-7). *See* EX1009; *see also* EX1009, ¶5 ("over 350 member companies"), 9-10, 187-214 (listing member companies). JESD79's cover page indicates it's the June 2000 date, and a capture of the JEDEC website indicates JESD79 was available at least on August 17, 2000. *Id.*, ¶17; *see* EX1007, 1.

JESD79 discloses a memory specification with a user-controlled drive strength settings (A1).



EX1007, 16[4].

The "normal" setting is defined by current-voltage characteristic curves that define the maximum, minimum, and nominal values.

[4] Citations follow the stamped page numbers unless otherwise stated.

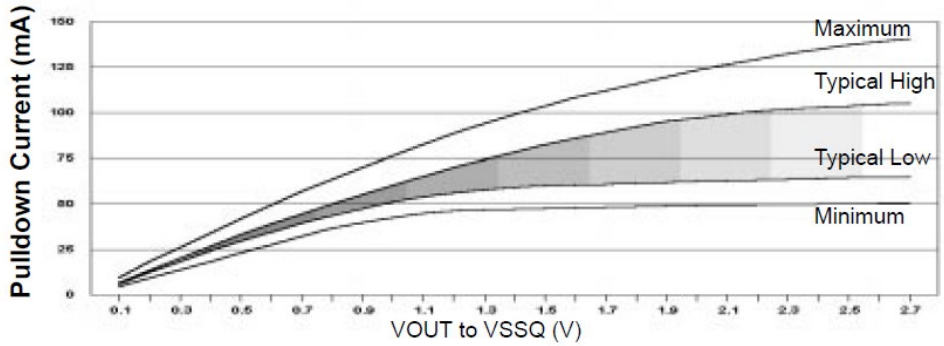
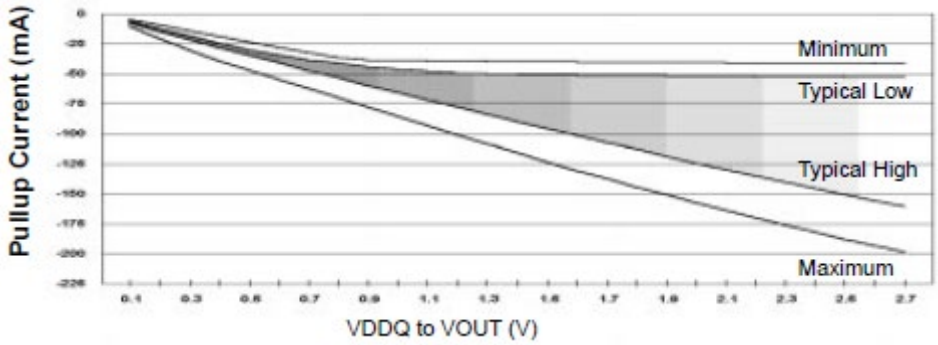


Figure a: Pulldown Characteristics



Id., 16, 59-60; EX1003, ¶¶69-70. Similarly, the "weak" setting is defined by current-voltage characteristic curves for lighter loads and/or point-to-point environments. *Id.* JESD79 also explains that the magnitude of the pullup and pulldown currents should match within a ten-percent tolerance. EX1007, 59; EX1003, ¶70.

D. Garrett (EX1008)

U.S. Patent No. 6,094,075 ("Garrett") was filed on August 27, 1998 and issued and published on July 25, 2000, and is prior art under §§102(a)-(b), 102(e) because it was filed and published before the Priority Date and because it was published more than a year before the U.S. Filing Date. EX1008, 1.

Garrett discloses an output driver with an adjustable drive current. *Id.*, 3:1-19. The output line (e.g., at BDA and BDB) is fed back and compared to a reference voltage (V_{ref}), sampled, and then input to a counter 115 that outputs a control signal (e.g., ictrl[n:0]) to adjust the width of the driver's transistors.

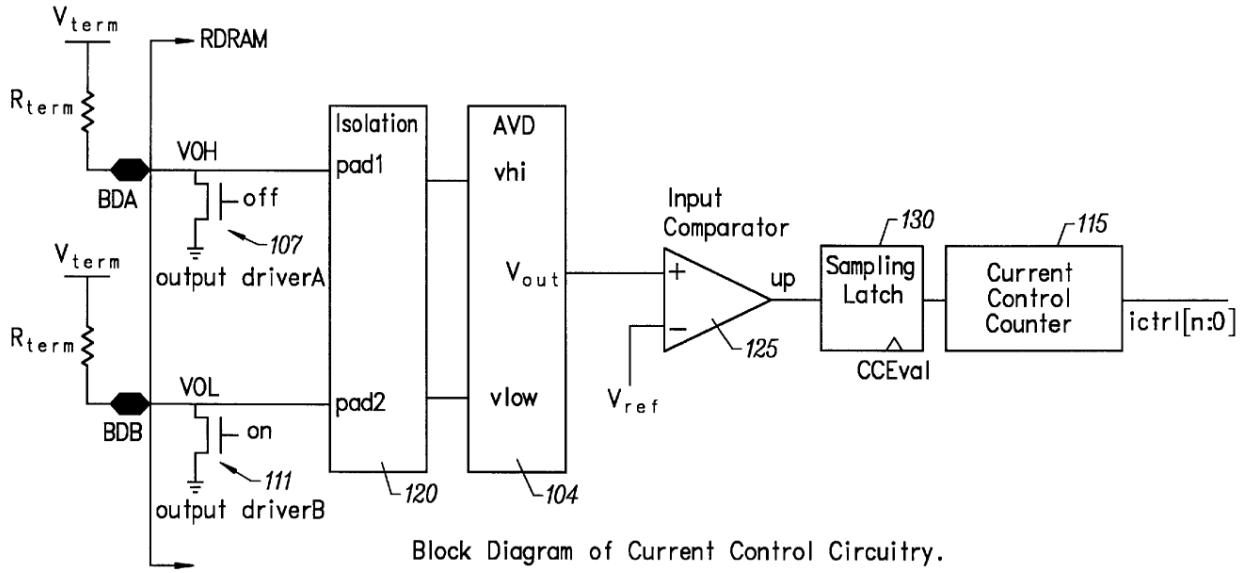


FIG. 2

Id., FIGS. 2-4, 11, 3:8-13, 5:26-6:24, 10:6-41; EX1003, ¶¶72-73. Garrett explains that the counter may be implemented as an up-down or a saturating binary search counter. EX1008, 3:38-40, 7:7-23, 8:67-9:9, 9:18-24; EX1003, ¶73.

X. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1-2 and 5-7 are obvious over Lee

1. Claim 1

a. "An output driver for an integrated circuit, comprising:" [1.P]

Lee teaches the preamble to the extent it is limiting. Lee discloses a system with an output location (27, annotated in purple below) that includes an output buffer driver circuit ("*an output driver*") for "*an integrated circuit*," such as memory or processor circuits (260, 280, 210 in FIG. 7, annotated in red), that drives its output onto a bus (13). EX1005, 3:13-32, 5:45-47, 7:33-35, 7:57-67, FIGS. 1, 5, 7 (each below); *see* EX1003, ¶¶75-76; EX1005, 1:39-44 (memory systems), FIGS. 4, 6 (output drivers).

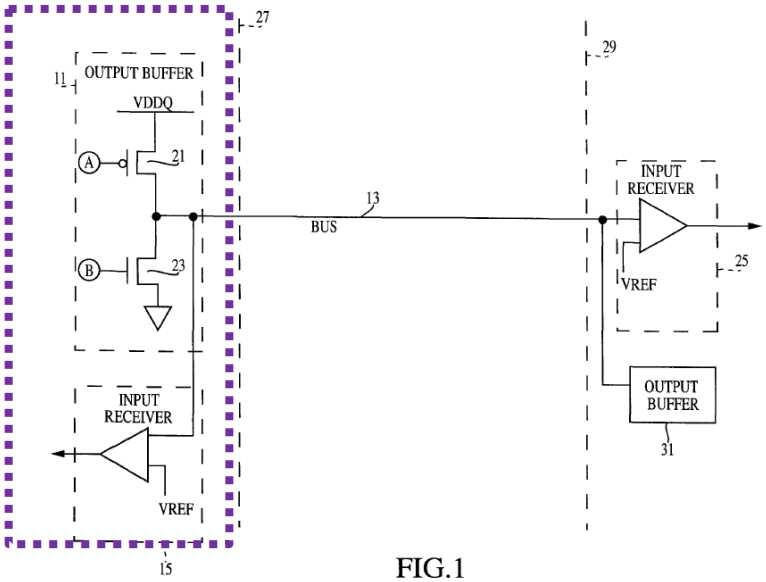


FIG.1

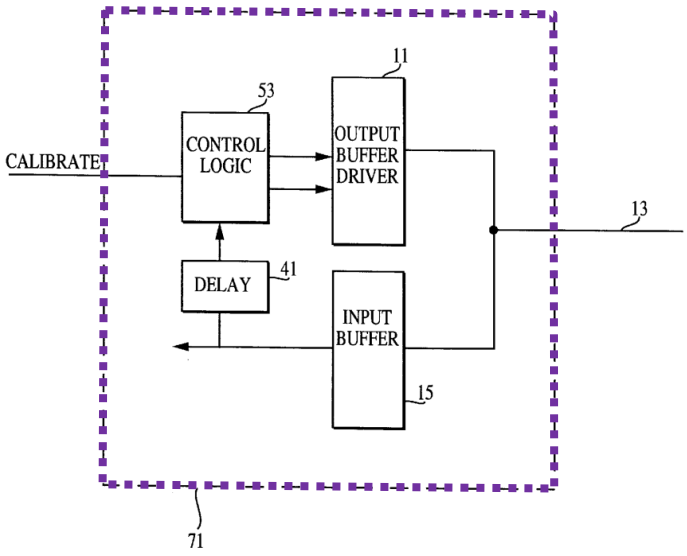


FIG. 5

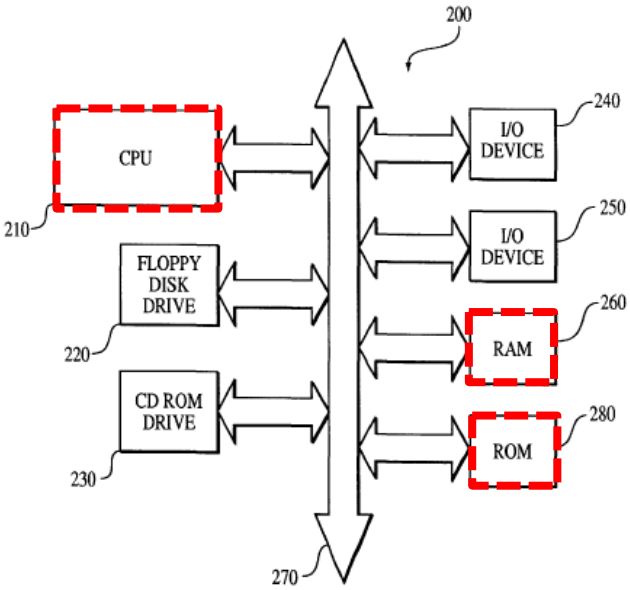


FIG.7

b. "a driver circuit for driving an input signal of the output driver onto an output line" [1.1]

Lee teaches this limitation. As shown below, Lee's "*driver circuit*" includes an output buffer driver (11/11') with two transistors (21 and 23) to drive an input

signal (received at nodes A and/or B) onto a bus (13) ("*for driving an input signal of the output driver onto an output line*").

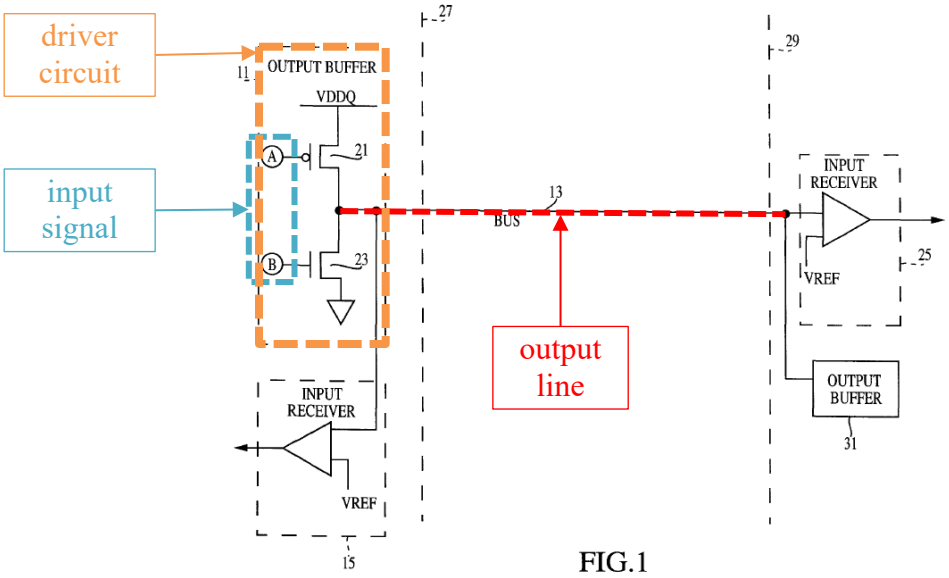


FIG.1

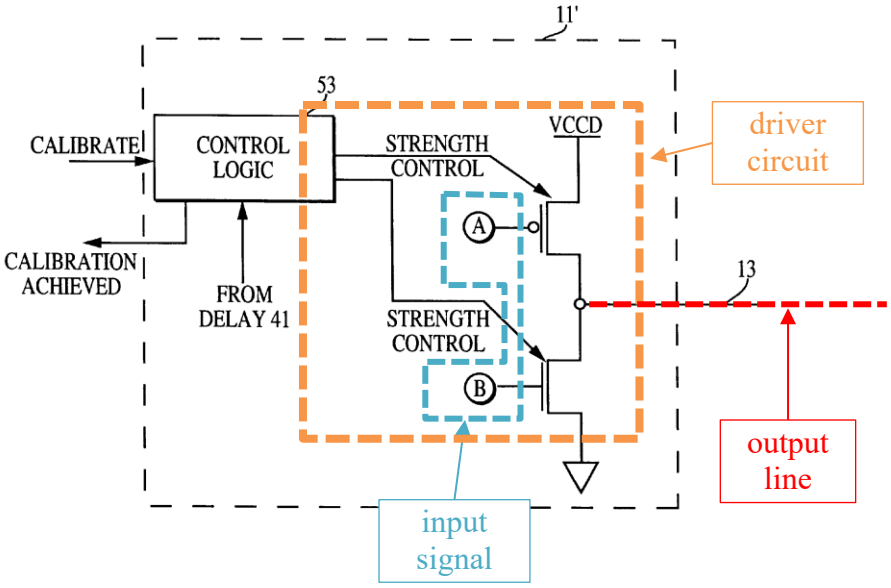


FIG. 4

EX1005, FIGS. 1, 4, 3:33-41; EX1003, ¶77. During normal operation, the driver circuit switches the bus voltage to a logic high or low level responsive to a logic

low or high level of the input signal (individually and collectively the signal received at nodes A and B). EX1005, 3:34-53. During calibration, node A is asserted low and node B is asserted high to turn on transistors 21 and 23 at the same time. *Id.*, 3:53-56. A POSITA would have thus understood the signal received at nodes A and/or B to be "*an input signal*." EX1003, ¶78.

In addition, Lee discloses to a POSITA that each node is configured to receive "*an input signal*" to be driven to the output by output buffer (11/11'). EX1005, FIGS. 1, 4, 6, 6:11-53; EX1003, ¶¶79-80. Further, it would have been obvious for a POSITA to implement Lee's output buffer in a system such that nodes A and B are coupled to one "*input signal*" for normal operation to enable the pull-up or pull-down path and control logic for calibration to enable both the pull-up and pull-down paths. EX1003, ¶80; EX1005, 3:34-56, FIG. 4; *see* EX1006, 4:45-52, FIGS. 2, 5.

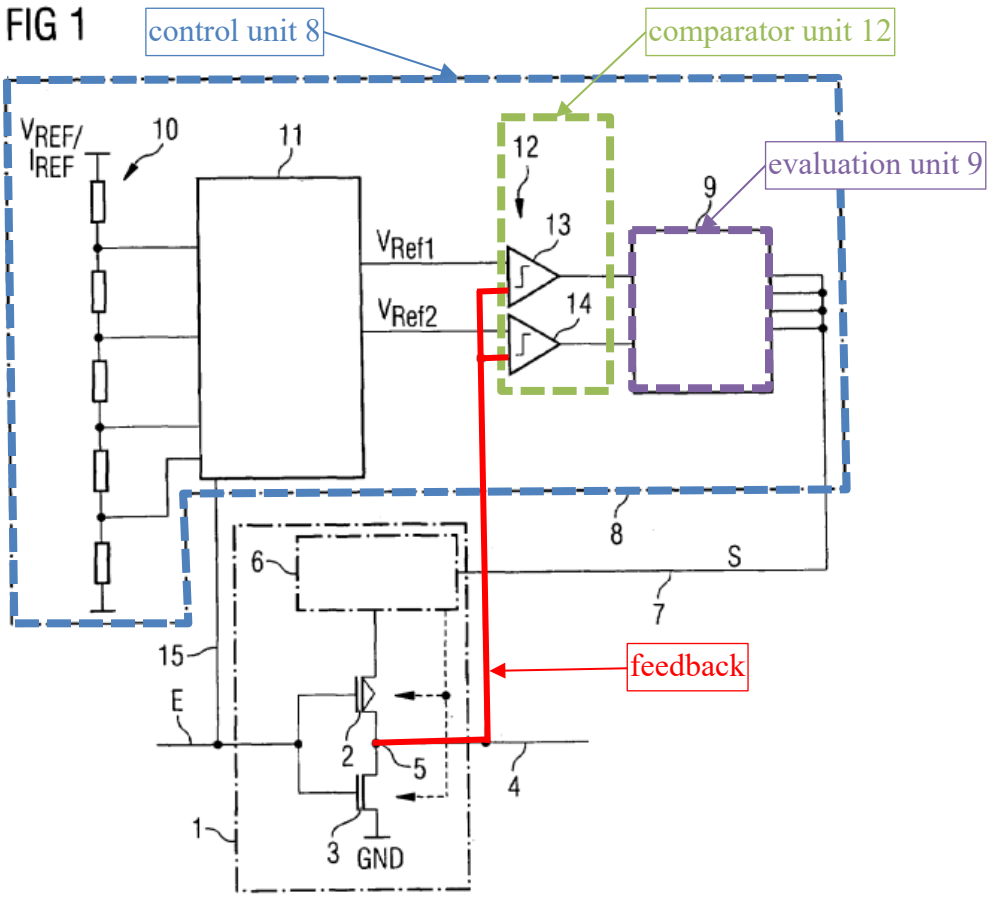
c. "a measuring circuit for measuring at least one of an output line current and an output line potential; and" [1.2]

Although it is unclear what structure is a "*measuring circuit*" "*for measuring . . . an output line potential*"[5] in the '369 Patent, Lee teaches this limitation because it contains a similar structure as the '369 Patent between the output line

[5] Potential is synonymous with voltage to a POSITA. EX1003, ¶81; *see* EX1001, 3:19-25, 4:15-17.

and circuitry for comparing the output line potential. EX1003, ¶¶81-93; *cf.* EX1001, 5:65-6:3.

As shown below, the ’369 Patent discloses a wire (annotated in red) that connects the output of driver circuit 1 and the input of a comparator unit 12 (in green).



EX1001, FIG. 1. The specification of the ’369 Patent (“’369 Specification”) explains that the control unit 8 (in blue above) comprises a comparator unit (in green) for comparing the *previously measured* potential value to a reference. *Id.*, 3:19-25, 4:32-36; EX1003, ¶83. The comparator unit 12 is connected to an

evaluation unit 9 (in purple) that outputs the control signal S to setting circuit 6 to set the driver strength. EX1001, 4:49-56.

Consistent with the ’369 Specification, claim 1 requires an “*output driver*” that comprises the “*measuring circuit*” and a separate “*control unit*” that “*includes a feedback control . . . based on a measured value provided by the measuring circuit*.” *Id.*, 6:57-7:3. Claim 6 requires that the “*control unit*” comprises “*a comparator unit for comparing . . . the measured output line potential . . . [to] a reference potential value*.” *Id.*, 7:26-30. Claim 7 further requires that the “*control unit*” comprises “*an evaluation unit connected to the comparator unit . . . [for changing] the control signal based upon a result from the comparator unit*.” *Id.*, 7:31-34. Accordingly, the “*measuring circuit*” measures the output line potential and provides the measurement as feedback to the “*control unit*,” including a “*comparator unit*,” to compare the measured potential to a reference and an “*evaluation unit*” for changing the control signal based on the comparison result. *Id.*, 6:57-7:34; EX1003, ¶84.

Similar to the feedback path (in red above) of the ’369 Patent, Lee discloses a wire (in red below) that feeds back the voltage of output buffer 11 to a comparator.

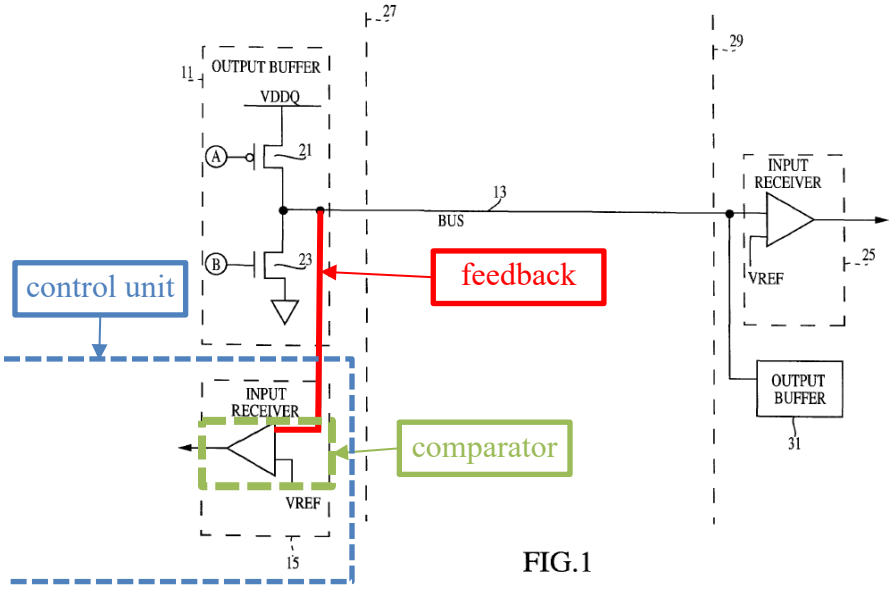


FIG.1

EX1005, FIG. 1, FIG. 5 (input buffer 15), FIGS. 3, 6 (comparator 61); EX1003, ¶85. And similar to the comparator of the '369 Specification that compares the feedback output value to a reference, Lee discloses an input receiver 15 for comparing the feedback output buffer value to a reference value VREF. EX1003, ¶85; EX1005, 3:43-46 (comparing with "a common source differential amplifier"), 4:46-49 (comparison result is a "'1' or '0' logic state … depending on whether the bus voltage is higher or lower than VREF."), 5:28-31 (alternatively using "a higher accuracy comparator 61"), FIGS. 1-3, 5-6. Thus, Lee teaches a "*measuring circuit*" that is similar to the one described in the '369 Specification, because the driver output of both is fed back via a wire (shown in red above) to the comparator (in green) that compares the driver output to a reference voltage. EX1001, FIG. 1; EX1005, at FIG. 1; EX1003, ¶85.

Further, Lee also teaches a "*measuring circuit*" for measuring the output potential that is part of its input receiver, which is part of the "control unit" identified below. *Infra* Section X.A.1.d. Lee discloses that the input receiver is "typically implemented as a common source differential amplifier." EX1005, 3:43-46. A POSITA would have understood that a common source differential amplifier compares two inputs by measuring them relative to a common source voltage. EX1003, ¶¶86-88; EX1011, FIG. 2a, 5:45-6:41. Thus, Lee's common source differential amplifier measures the voltages at its inputs, including the output voltage, relative to a common source and amplifies the difference between the voltages while rejecting the common source voltage. *Id.*

In addition to comparing the output voltage/potential to a reference voltage/potential, Lee teaches that calibration may also be performed by comparing the output drive *current* to a reference drive current value. EX1005, 7:22-26. Specifically, though Lee describes "a comparison of bus voltage" to "a reference voltage VREF, calibration may also be obtained by comparing the drive current on the bus 13 with a reference drive current." *Id.* It would have been obvious to a POSITA that to compare a drive current with a reference current value, such drive current output by the driver must be measured by a measuring circuit, such as a resistor. EX1003, ¶¶89-93; *see* EX1010, 10:8-11:18, FIGS. 4, 6; EX1014,

Abstract, FIG. 2, 3:24-30, 3:64-4:1; EX1012, 812-17. Thus, Lee also teaches "*a measuring circuit for measuring . . . an output line current*." EX1003, ¶¶89-93.

d. "a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range," [1.3]

Lee teaches this limitation. Figure 5 of Lee shows a calibration control logic circuit 53 connected via delay 41 to an input receiver/buffer 15:

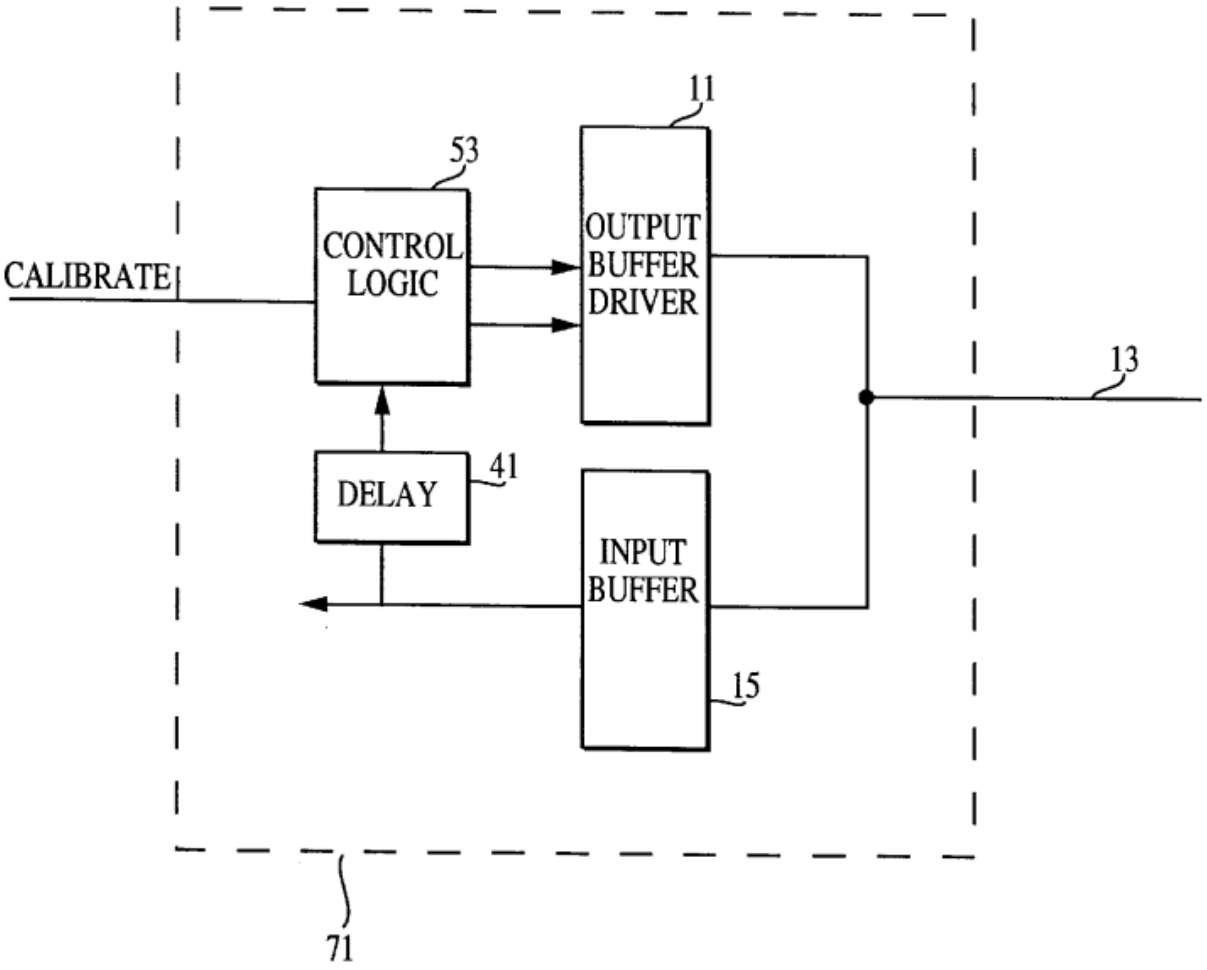
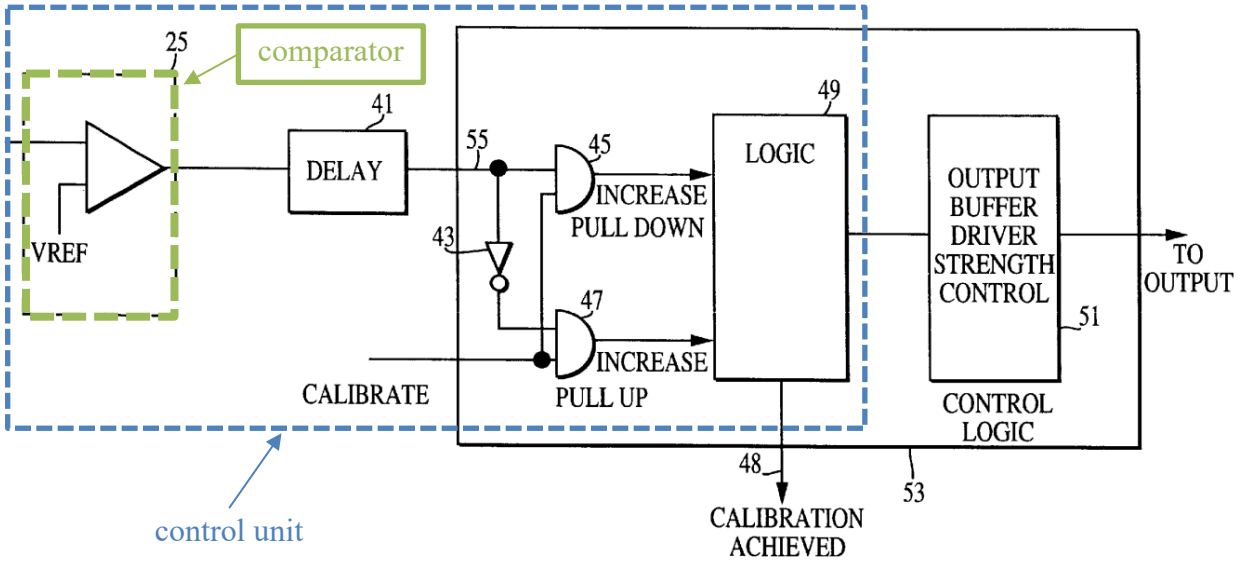


FIG. 5

EX1005, FIG. 5; EX1003, ¶94.

As shown below, Figure 2 of Lee illustrates the circuitry in more detail with the input receiver/buffer[6] including comparator and a logic circuit 49 to provide a signal for appropriate strength adjustments to an output buffer driver strength control circuit 51.



EX1005, FIG. 2, 4:31-34, 4:58-61; EX1003, ¶95. As explained in Section X.A.4 for claim 5, the circuit 51 is a "*setting circuit for receiving the control signal from the control unit and for setting the driver strength of the driver circuit*."

---

[6] Although Figure 2 illustrates input receiver 25, Lee explains that circuit 53 of Figure 2 can sample the output of the input receiver 25 or 15, the latter of which is co-located with the output buffer driver 11, as shown in Figures 1 and 5. EX1005, 4:31-34, FIGS. 1, 2, 5.

The comparator in Lee compares the output voltage to a voltage reference (VREF) and generates a resulting signal with "either a '1' or '0' logic state . . . depending on whether the bus voltage is higher or lower than VREF." EX1005, 4:46-48. The resulting signal is input to circuitry that provides a request to logic circuit 49 to change the drive strength. *Id.*, 4:46-55, FIG. 2 (delay 41, inverter 43, and AND-gates 45 and 47); *see also* EX1003, ¶¶96-97; EX1005, 2:39-44, 4:6-30, 4:62-5:27. Specifically, the logic circuit 49 outputs "an appropriate strength adjustment command" based on its inputs that adjusts the output driver strength of the pull-down transistor or the pull-up transistor. EX1005, 4:49-61. Thus, Lee teaches "*a control unit for providing a control signal for setting a driver strength of the driver circuit*." EX1003, ¶¶94-97.

Lee also teaches setting the driver strength "*to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*"[7] As an initial matter, though the '369 Patent generically references "specifications for integrated circuits . . . for SDRAM and DDR memory," it does not mention any particular specification available at the time, or provide a

[7] Xilinx reserves the right to challenge these claim limitations under 35 U.S.C. § 112 in other proceedings.

definition or example of a range that is prescribed by a specification or that is either included in, or excluded from, the meaning of a "*specification-prescribed*" range. *See* EX1001, 1:39-40; EX1003, ¶99. Also, the '369 Patent does not expressly define or otherwise explain how a "*power range*" is "*desired*" or by whom it is "*desired*." EX1003, ¶99. And, the term "desired" only appears once in the '369 Specification for a prescribed "potential value range." EX1001, 5:8-13. To the extent there is a sufficient disclosure in the '369 Patent for a "*specification-prescribed*" range and a "*desired*" power range, Lee discloses those ranges as explained below.

Lee teaches that the output range in normal operation is between VDDQ and ground (a "*specification-prescribed potential range*"). EX1003, ¶100. As shown below, transistor 21 is connected to VDDQ and transistor 23 is connected to ground.

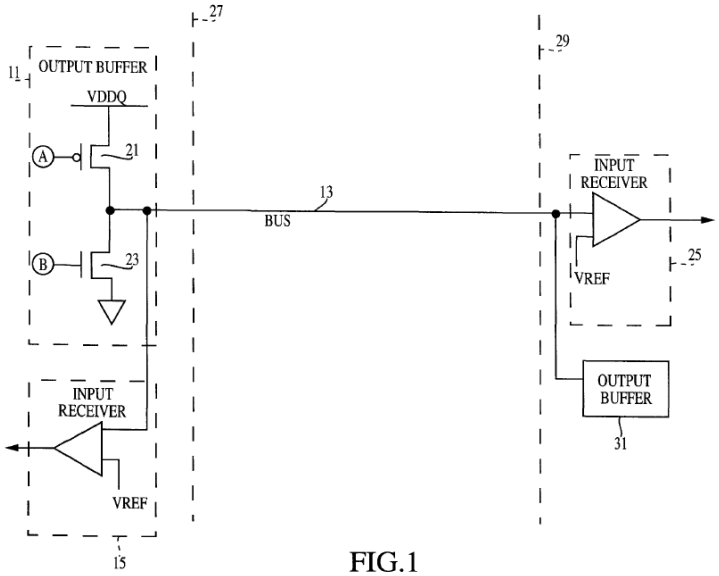


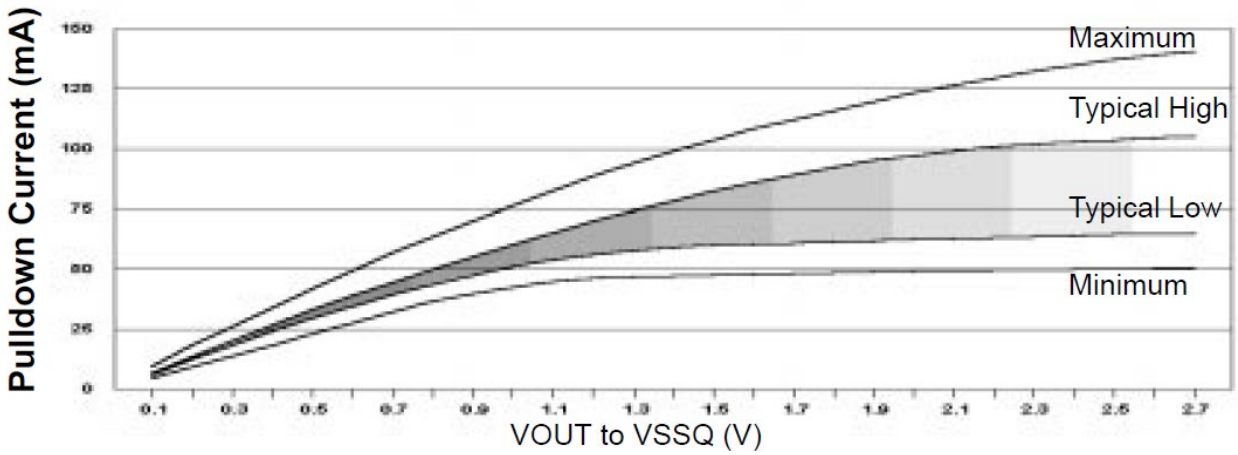
FIG.1

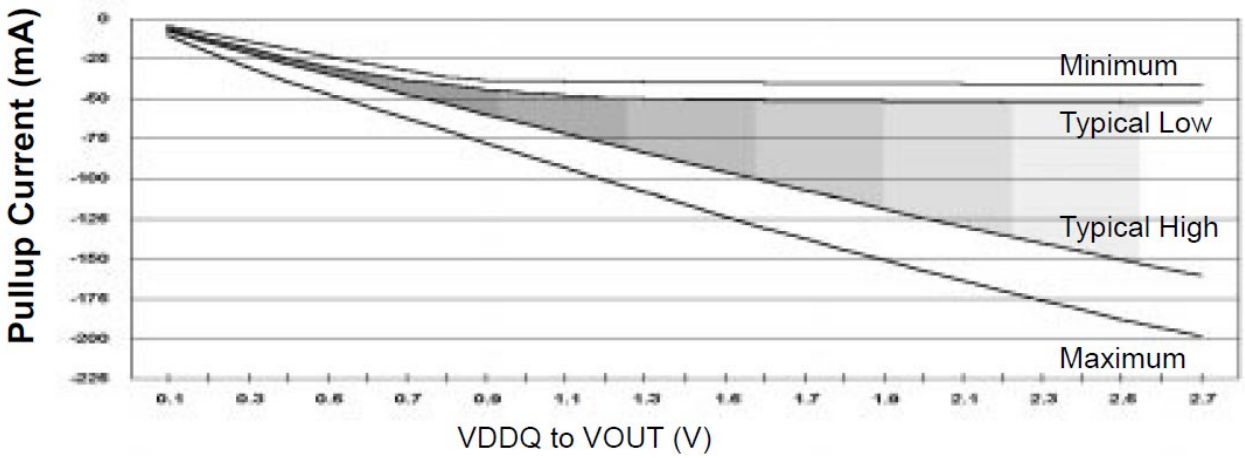
EX1005, FIG. 1, 3:33-41, 10:6-12, 12:37-46; EX1003, ¶100. Accordingly, a POSITA would have understood that the range of the output-line voltage during normal operation is between VDDQ and a ground potential. EX1003, ¶100. Further, the range between VDDQ and ground is expressly prescribed by Lee's specification[8] and thus teaches a "*specification-prescribed*" potential range to the extent the term is sufficiently disclosed by the '369 Patent. EX1003, ¶100.

Lee also teaches "*a specification-prescribed current range*." EX1003, ¶101. Lee discloses that current-versus-voltage curves for output buffer drivers are specified with minimum and maximum limits for the voltage and current levels. EX1005, 1:26-33. Specifically, Lee explains that some "benefits obtained by calibrated output buffer drivers can be achieved by [] specifying the driver characteristics for all transistors in an output buffer driver" including "specifying minimum and maximum output currents" and "specifying the current versus

[8] If Patent Owner argues "specification-prescribed" and the associated limitations should be interpreted to require ranges specified in a standard setting body's specification, that interpretation is inconsistent with Patent Owner's infringement allegations, which do not point to such a specification. *See* EX1015, ¶¶36-37. In any event, the limitations are still obvious over Lee in combination with the JEDEC JESD79 specification (Ground 3). *Supra* §X.C.2.d.

voltage curves with minimum and maximum limits." *Id.* A POSITA would have understood and found it obvious from this disclosure that for a given voltage on one axis of the curve, the corresponding current must be in a range between minimum and maximum limits specified on the other axis of the curve. EX1003, ¶101. A POSITA would also have understood that as the voltage increases, the minimum and maximum current limits specified by the curve also generally increase. *Id.* For example, as shown in the exemplary curves below, which are similar to the curves disclosed by the '369 Patent, as the voltage (labeled on the horizontal axis) increases, the magnitude of the pulldown and pullup currents (labeled on the vertical axis) also generally increases.





EX1007, 59-60; *see* EX1001, FIGS. 2a-2b.

As explained above, Lee teaches a voltage range during normal operation between VDDQ and ground. A POSITA would have understood and found it obvious that each of these two voltages (VDDQ and ground) has a corresponding current range (between minimum and maximum limits) that are individually and collectively "*a specification-prescribed current range*." EX1003, ¶101; *see, e.g.*, EX1005, 1:26-33; EX1007, 59-60.

Lee also teaches a "*desired power range*" that is the product of the prescribed potential and current ranges. EX1003, ¶102. As explained above, Lee teaches "*a specification-prescribed current range*" and "*a specification-prescribed potential range*" between the minimum and maximum currents associated with VDDQ and ground.

In addition, Lee teaches a desired potential range because its calibration scheme ensures that the output voltage swings across a range between a high

voltage VOH and a low voltage VOL, which are between VDDQ and ground, that are symmetric about a mid-voltage VREF after calibration. EX1005, 3:6-24, 4:35-61, FIGS. 2-3; EX1003, ¶102. During calibration, both transistors of the driver are turned on and the output bus voltage is compared to VREF:

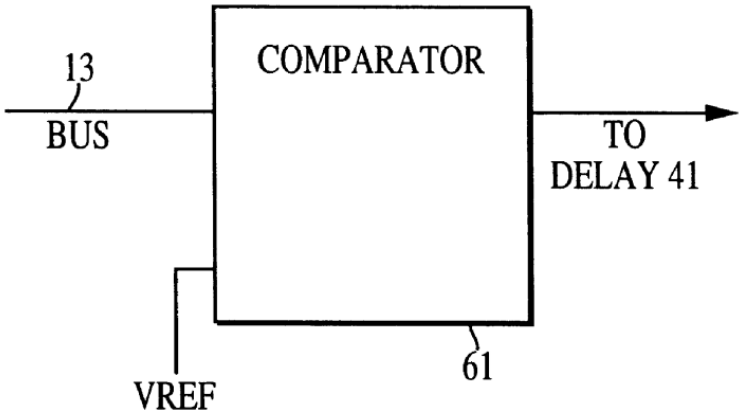


FIG. 3

EX1005, FIG. 3; EX1003, ¶102. A POSITA would have understood that the VOH and VOL levels, which Lee adjusts via calibration to be symmetric about VREF or VDDQ/2, would be used during normal operation to represent the high or low logic states of the output line. *See* EX1005, 3:47-53; EX1003, ¶102; *see also* EX1005, 3:6-9, 1:61-63, 3:56-58. A POSITA would have also understood that the VOH level for Lee's output buffer driver is no higher than VDDQ because the pull-up transistor 21 is supplied VDDQ and that the VOL level is no lower than a

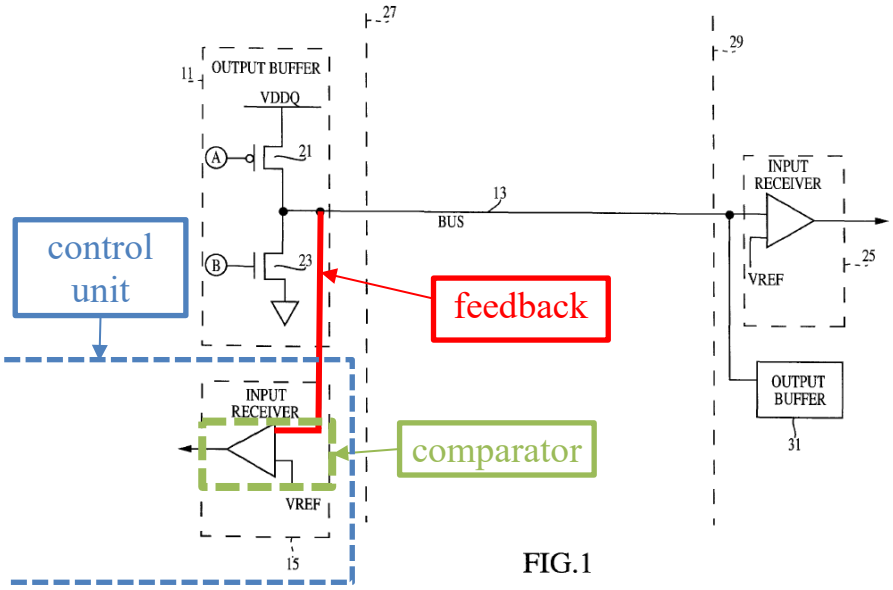
ground potential because the pull-down transistor 23 is supplied the ground potential. EX1003, ¶102; EX1005, 3:33-41, FIG. 1.

Further, a POSITA would have understood, based on Ohm's Law, that these potential and current ranges define an intended "*power range*" for the output buffer driver because power is equivalent to potential multiplied by current and because Lee teaches a voltage between VOH and VOL, between VDDQ and ground, and corresponding minimum/maximum current range(s). EX1003, ¶103; EX1005, 1:26-33, FIG. 1. Thus, Lee teaches and makes obvious drive strength adjustment "*to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range.*" EX1003, ¶¶98-103.

e. "wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit." [1.4]

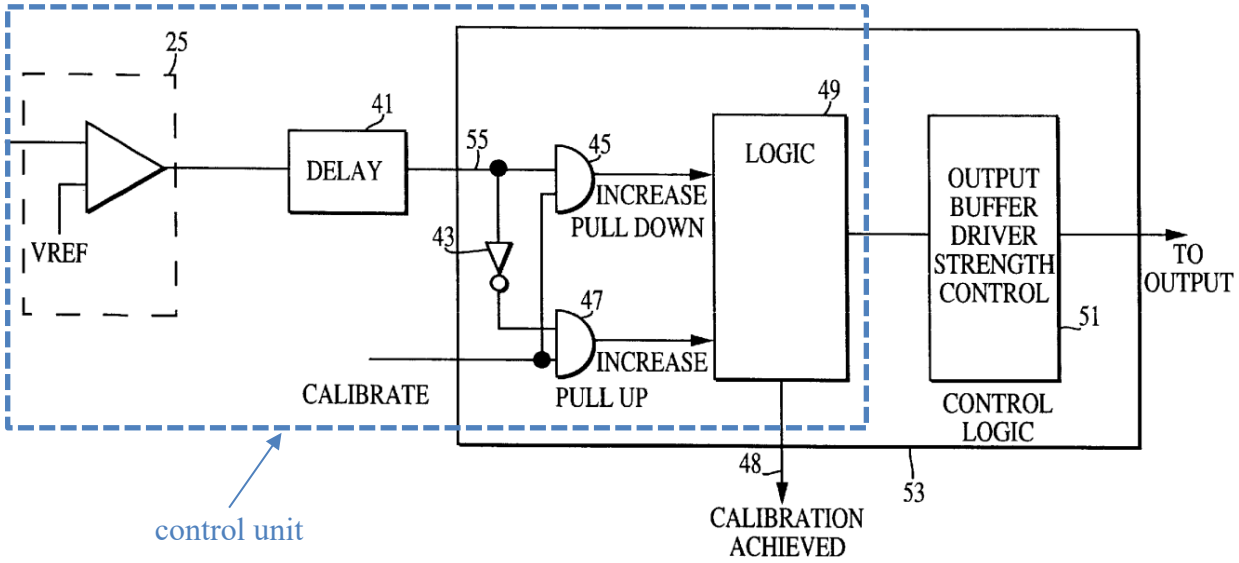
As discussed for claim [1.2], to the extent a "measuring circuit for measuring" an "output line potential" is supported by the '369 Specification, the limitation is taught by Lee. *Supra* §X.A.1.c. Similarly, to the extent the '369 Specification supports "a measured value provided by the measuring circuit," Lee teaches claim [1.4]. As shown below, Lee discloses that the driver's output is fed back ("*a measured value provided by the measuring circuit*") to a comparator via a

wire (similar to the wire disclosed in the ’369 Patent that feeds back the output to a comparator unit) to compare the output potential or current to a reference value.



EX1005, FIG. 1, FIGS. 3, 5-6, 7:26-32; *supra* §X.A.1.c; EX1003, ¶¶104-05.

The result of the comparison is provided to additional circuitry, including “*a control unit*,” that is used to determine the output buffer driver strength control (in 51):



EX1005, FIG. 2, 4:36-61, FIGS. 4-6. Specifically, the result is provided to delay circuit 41 and then provided to logic circuitry (including AND gates 45 and 47), which enables driver strength adjustments, such as increasing the pull-down or pull-up drive strength, when the CALIBRATE signal is asserted to indicate the start of calibration. *Id.*, FIG. 2, 5:39-41, 5:46-58. Thus, Lee teaches a control unit that includes a feedback control (feedback path from comparison circuit) to affect the setting of the driver strength (via circuit 51) based on a measured value provided by the measuring circuit that is input to the comparison circuit (input receiver 15). EX1003, ¶106.

2. Claim 2: "The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-

prescribed lower potential limit value adjusted with the tolerance magnitude."

As explained above, Lee teaches a desired power range during normal operation with a prescribed voltage range between VDDQ and ground and a desired voltage range between VOH and VOL within the prescribed range. *Supra* §X.A.1.d. A POSITA would have understood that Lee's desired power range is determined, in part, by the ground potential ("*a specification-prescribed lower potential limit value*") that is lower in potential than VDDQ. EX1003, ¶107; EX1005, 10:6-13 (claims 32-34), FIGS. 1-2. Lee also teaches adjusting the low voltage level, VOL, via drive strength settings during calibration such that the high voltage level, VOH, and VOL are symmetric about a reference voltage, VREF. *See* EX1005, 3:47-53; EX1003, ¶108. Accordingly, a POSITA would have understood that the power range intended by Lee's specification is also determined by VOL ("*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*"), which is adjusted relative to the ground potential to achieve symmetry with VOH about VREF. EX1003, ¶¶107-09; EX1005, 10:6-13 (claims 32-34), FIGS. 1-2.

Alternatively, Lee teaches this limitation under Patent Owner's interpretation of the claim where allegedly VREF (a reference voltage for inputs and outputs) is an example of "*a specification-prescribed lower potential limit value*" and VRN (the voltage of an impedance calibration output), adjusted relative

to VREF, is "*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*":

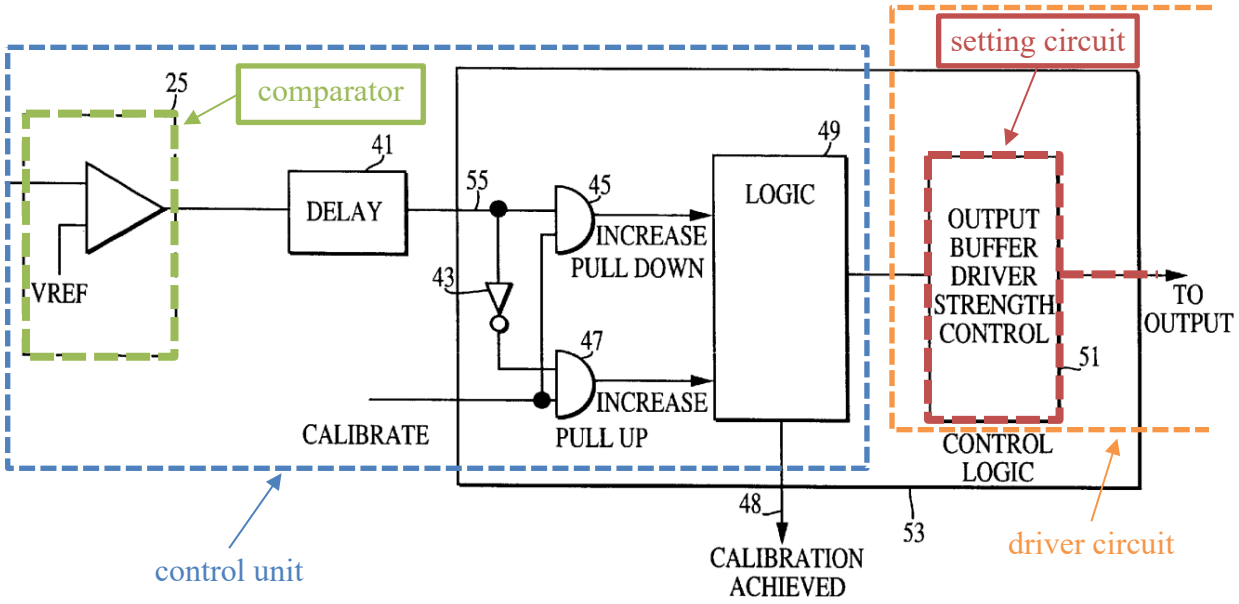
> 37. On information and belief, the desired power range of the output driver of the 369 Patent Infringing Products is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value, for example, VREF, and a specification prescribed lower potential limit value adjusted with the tolerance magnitude, for example, VRN adjusted relative to VREF.

EX1015, ¶37; *see* EX1016, 309. Under Patent Owner's interpretation, a POSITA would have understood that the power range intended by Lee's specification during calibration is also determined by VREF (a reference voltage for inputs and outputs in Lee and "*a specification-prescribed lower potential limit value,*" as alleged by Patent Owner) and the output to the bus 13, which is adjusted relative to VREF. EX1005, 3:8-10, 4:62-5:11, FIGS. 1, 2; EX1003, ¶110; *supra* §X.A.1.d. In particular, Lee's output voltage on the bus is compared to VREF to adjust the drive strength settings that, when applied, adjust the output voltage relative to VREF. *Id.* Thus, under Patent Owner's interpretation that the voltage VRN is "*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*" because it is adjusted relative to VREF, the output voltage to the bus in Lee also satisfies the same limitation. *Id.*

3. Claim 5: "The output driver of claim 1, wherein the driver circuit further comprises a setting circuit for receiving the control

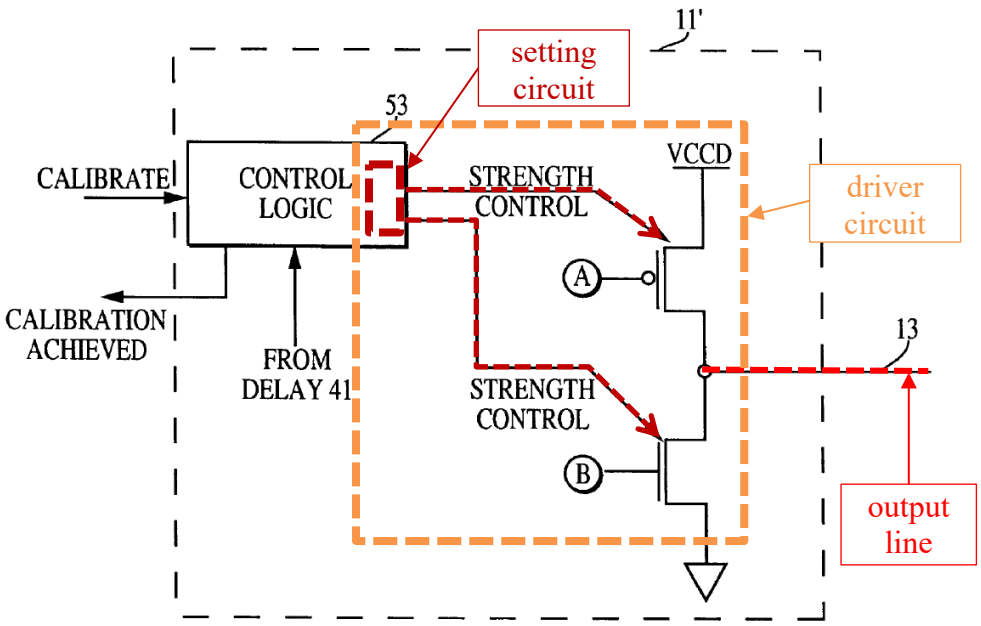
signal from the control unit and for setting the driver strength of the driver circuit."

As shown below, Lee discloses a driver circuit that includes an output buffer driver strength control circuit 51 ("*a setting circuit*") of control logic 53 that receives an appropriate strength adjustment command from logic circuit 49 ("*for receiving the control signal from the control unit*") and adjusts the output driver strength by providing an output from control logic 53.



EX1005, FIG. 2, 4:58-61; EX1003, ¶111.

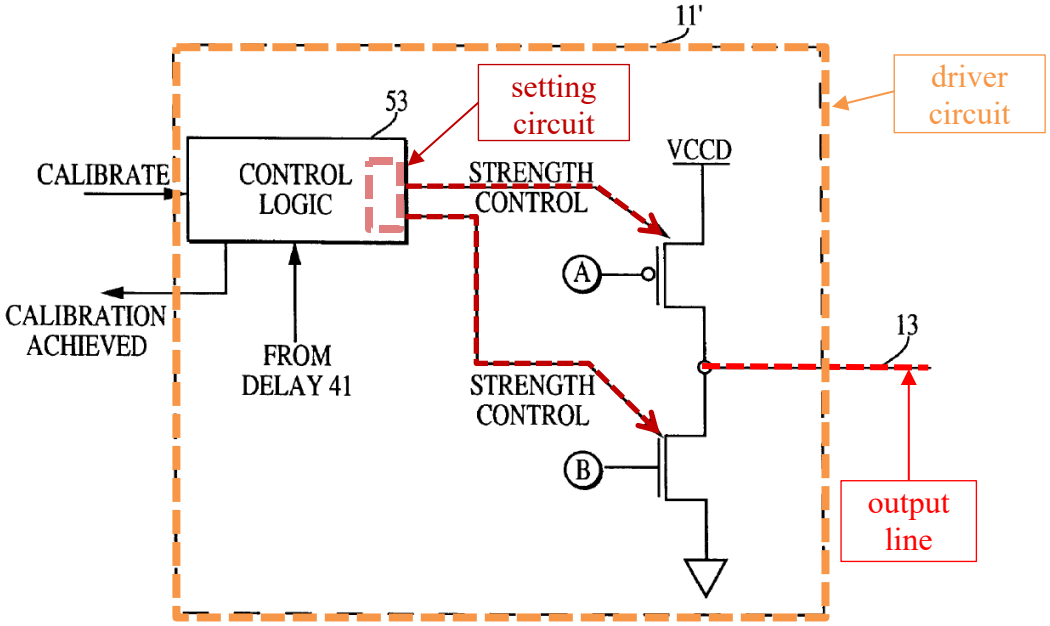
Figure 4 of Lee shows that the output from the circuit 51 in control logic 53[9] ("*setting circuit*") is a "STRENGTH CONTROL" signal for the pull-up and pull-down transistors of the driver circuit ("*for setting the driver strength of the driver circuit*"):



EX1005, FIG. 4, 5:42-67; *see also* EX1005, FIG. 6, 6:54-63.

Lee also discloses that the output buffer/driver (e.g., 11' in Figure 4 and/or 71 in Figure 5) can include the control logic 53, delay 41, and/or input buffer 15:

[9] Figure 4 shows the control logic 53, which includes both the logic unit 49 (in the "*control unit*") and the output buffer driver strength control circuit 51 ("*setting circuit*").



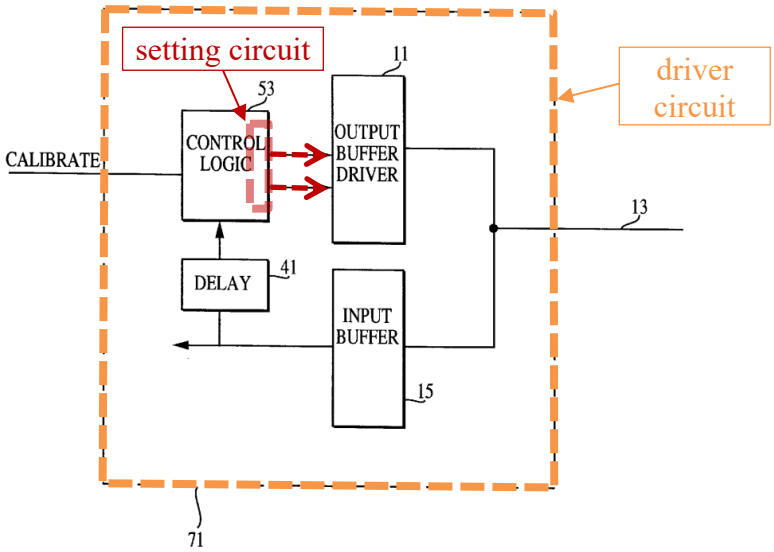


FIG. 5

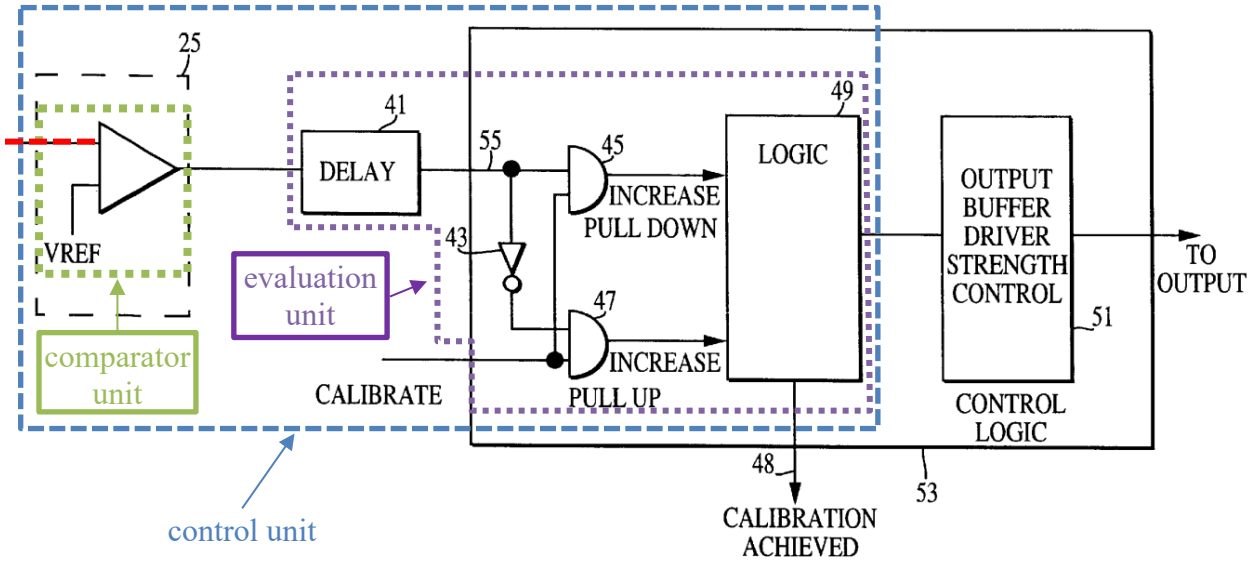
EX1005, FIGS. 4-5, 5:42-47; EX1003, ¶112. Thus, Lee teaches claim 5. EX1003, ¶¶111-12.

4. Claim 6: "The output driver of claim 1, wherein the control unit further comprises a comparator unit for comparing at least

one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value."

5. Claim 7: "The output driver of claim 6, wherein the control unit further comprises an evaluation unit connected to the comparator unit, the evaluation unit configured to change the control signal based upon a result from the comparator unit."

Lee teaches claims 6 and 7. As shown below, Lee discloses control logic and circuitry ("*control unit*") (in blue) that includes a "*comparator unit*" (in green) connected to an "evaluation unit" (in purple).



EX1005, FIG. 2, 4:31-34, FIG. 1; EX1003, ¶113; *see* EX1005, 5:29-34, FIGS. 3, 6. The comparator unit is implemented as "a common source differential amplifier" or "higher accuracy comparator" that compares the measured output line potential (in red) with a reference potential (VREF) ("*for comparing … the measured output line potential … with … a reference potential value*"). EX1005, 3:41-46, 3:58-63,

4:31-34, 4:46-49, 5:28-34, FIGS. 1-3, 6; EX1003, ¶114. Lee also teaches that the comparator unit can compare the measured output line current with a reference current ("*for comparing ... the measured output line current ... with ... a reference current value*"). EX1005, 7:22-32; EX1003, ¶114. Lee teaches that the output of the comparator is connected to the evaluation unit, which includes a delay 41 to ensure a precise comparison, AND-gates 45 and 47 to apply signals to logic 49 to instruct driver strength adjustments, such as increasing the pull-down or pull-up drive strength, when the CALIBRATE signal is logic high, and logic 49 to send an appropriate strength adjustment command to circuit 51. EX1005, FIG. 2, 4:31-5:5, 4:17-30 (drive strength adjustment techniques), 5:39-58; EX1003, ¶115. Accordingly, Lee also teaches that its evaluation unit changes the strength adjustment command based on the comparator output ("*change the control signal based upon a result from the comparator unit*"). EX1003, ¶115.

B. Ground 2: Claims 1-2 and 5-7 are obvious over Lee and Thomann

1. Motivation to Combine Lee and Thomann

Ground 2 combines Lee with Thomann. As explained below, Thomann teaches how to calibrate an output buffer driver, such as the one disclosed in Lee, to achieve a symmetric midpoint voltage, VREF.

A POSITA would have been motivated to combine Lee with Thomann, and had a reasonable expectation of success in doing so, because both references

disclose the same field of invention, relate to calibration of an output buffer driver, share common inventorship, and were originally assigned to the same entity. EX1005, 1, 1:6-8; EX1006, 1, 1:5-7; EX1003, ¶116-121. Lee discloses an output buffer driver that feeds back the driver output to a comparison circuit to adjust the drive strength. EX1005, FIG. 1, 3:13-32, 4:31-61; EX1003, ¶118; *supra* §IX.A. Similar to Lee, Thomann discloses an output buffer driver that feeds back the output to a comparison circuit to adjust the drive strength. EX1006, FIG. 1, 4:19-24, 4:47-57; EX1003, ¶118; *supra* §IX.B.

Lee recognizes that calibration adjusts the VOH and VOL levels at the output to be symmetric about a mid-point voltage, VREF, and that different algorithms may be used for drive strength adjustment, but it does not describe the range of VOH and VOL levels or how the output driver voltage swings between the VOH and VOL levels changes with calibration. EX1005, 3:7-9, 5:6-28; EX1003, ¶119. However, Thomann does provide these details, showing the ranges of VOH and VOL levels and the voltage swing of the driver between the VOH and VOL levels, both before and after calibration. *See, e.g.*, EX1006, 5:37-65, 6:17-31, FIGS. 1, 3; EX1003, ¶119.

As shown below, Thomann discloses that the range of the VOH level spans between VOH MIN and VOH MAX and that the range of the VOL level spans between VOL MIN and VOL MAX.

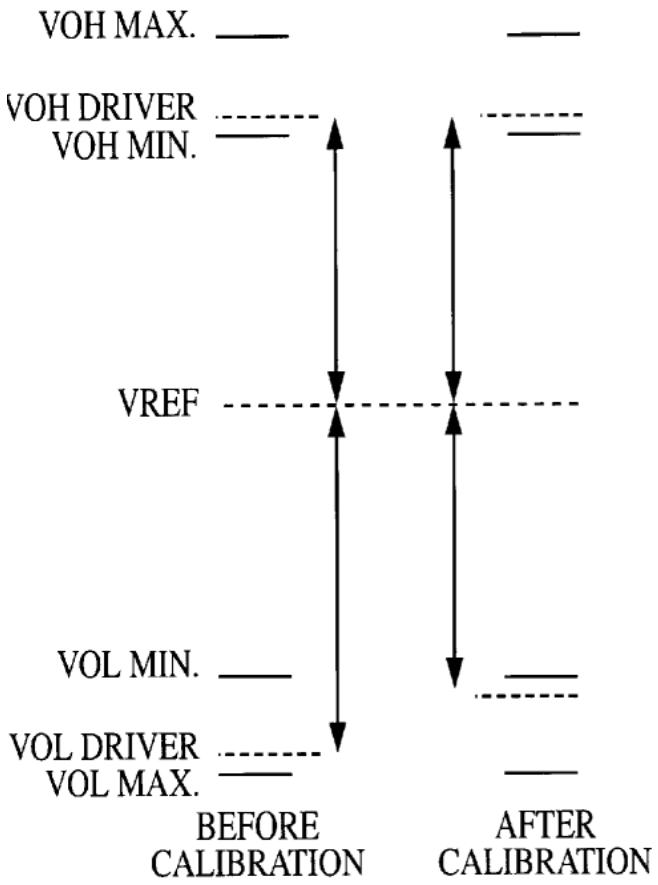


FIG. 3

EX1006, FIG. 3, 5:39-44; EX1003, ¶120. Before calibration (shown to the left above), the voltage swing of the driver output is unbalanced and the mid-point voltage deviates from the reference voltage VREF, because the VOL DRIVER level is further from VREF than the VOH DRIVER level. *Id.* By contrast, the voltage swing of the driver output after calibration of the drive strength setting is shown on the right above. Specifically, calibration enables the voltage swing to be balanced with a mid-point voltage VREF because the VOL DRIVER level and the VOH DRIVER level are symmetric about VREF. EX1006, FIG. 3, 5:58-65;

EX1003, ¶120. To achieve the balanced output voltage swing, Thomann explains that one of the transistors of the driver is first set to a drive strength, such as a minimum drive strength. EX1006, 6:23-31. Then similar to Lee, the drive strength is incrementally adjusted, such as being increased from the minimum setting. *Id.*; *see* EX1005, 4:3-5:19; EX1003, ¶120. Indeed, it was well-known that setting a minimum drive strength in which the voltage is above a minimum level, such as VOH MIN/VOL MIN, as disclosed in Thomann, minimizes the power dissipated during voltage swings. *See* EX1010, 8:13-32, FIGS. 4-5; EX1006, 6:23-31.

Thus, a POSITA would have been motivated to implement Lee's calibration logic with the teachings of Thomann's calibration routine to set an initial drive strength and adjust the voltage swing using drive strength adjustments to achieve a balanced driver. EX1003, ¶121. This straightforward modification of Lee's calibration logic in view of Thomann and the knowledge of a POSITA simply uses a known technique (e.g., Thomann's calibration technique to setting the initial drive strength and performing adjustments) to improve a similar device (e.g., Lee's output buffer driver with calibration) in the same way (e.g., adjusting the drive strength of the driver to obtain a reduced voltage swing balanced around a midpoint at a reference voltage VREF). EX1003, ¶121. Additionally, the modification simply applies a known technique (e.g., calibration by setting an initial drive strength and performing adjustments) to a known device (e.g., an

output buffer driver with calibration) that is ready for improvement to yield predictable results (e.g., a balanced driver with a reduced voltage swing having a midpoint at a reference voltage VREF). *Id.*

2. Claim 1

a. Claim limitations [1.P], [1.1], [1.2], and [1.4]

As explained above for Ground 1, Lee teaches limitations [1.P], [1.1], [1.2], and [1.4] to the extent each is limiting or supported by the '369 Specification. *Supra* §§ X.A.1.a-X.A.1.c, X.A.1.e; *see* EX1005, 3:13-56, 4:36-61, 5:28-58, 7:22-32, 7:57-67, FIGS. 1, 2, 4-7; *see also* EX1006, Abstract, FIG. 1, 4:7-47; EX1003, ¶122-24, 130.

b. "a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range," [1.3]

As explained above for Ground 1, Lee teaches limitation [1.3]. *Supra* §X.A.1.d; *see* EX1005, 1:26-33, 1:61-63, 3:6-9, 3:47-53, 4:6-30, 4:31-34, 4:46-5:27, FIGS. 1, 2.

Further, in the combination, Lee's comparator, delay, and calibration logic ("a control unit"), as modified by Thomann's teachings of its calibration routine, provides a control signal for driver strength settings to provide the output line potential "*in a desired power range of a specification-prescribed potential range*

and a specification-prescribed current range." *See* EX1003, ¶¶126-29. As explained for Ground 1, a POSITA would have understood that power is equivalent to potential multiplied by current. EX1003, ¶126.

Thomann specifies "*a specification-prescribed potential range*" for each of the VOH DRIVER output voltage level between VOH MAX and VOH MIN, and the VOL DRIVER output voltage level between VOL MAX and VOL MIN, as prescribed in the figure below.

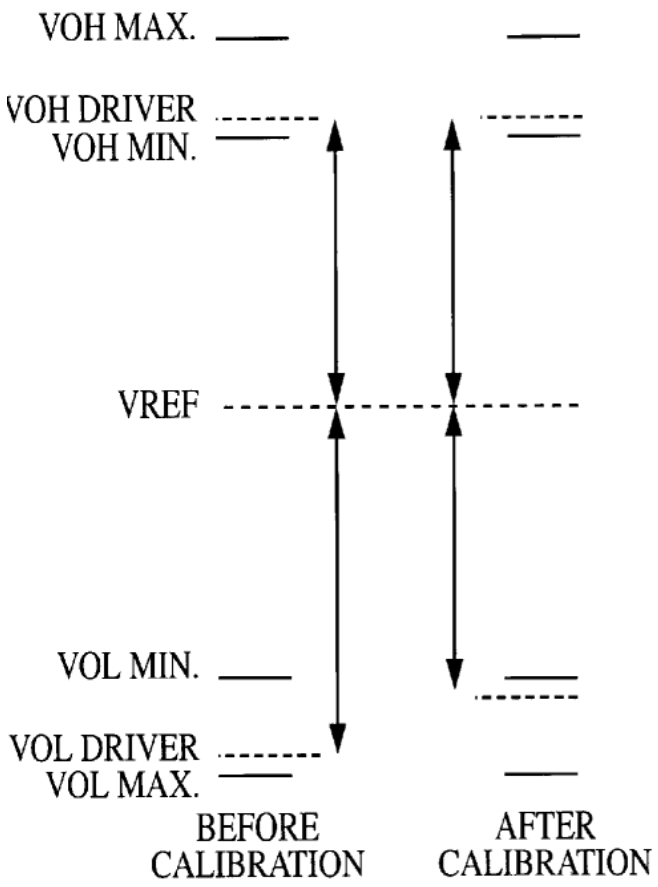


FIG. 3

EX1006, FIG. 3, 5:62-65, 6:23-26; EX1003, ¶127. Thomann explains that it desires for "the VOH and VOL levels to be symmetric about a midpoint voltage," VREF. EX1006, 3:33-36. Accordingly, a POSITA would have understood that the corresponding desired power range in Thomann corresponds to symmetric VOH and VOL levels symmetric about VREF and within the voltage ranges between VOH MAX and VOH MIN and between VOL MAX and VOL MIN. EX1003, ¶126-27, 103.

Thomann also teaches and discloses "*a specification-prescribed current range*." Like Lee, Thomann explains that specifications for output drivers prescribe current versus voltage curves with minimum and maximum limits. EX1005, 1:29-33; EX1006, 1:29-33; *see, e.g.*, EX1007, 59-60 (illustrating examples of curves). A POSITA would have understood that each of the VOH and VOL ranges, individually and collectively, have corresponding current ranges (between minimum and maximum current limits) that are individually and collectively "*a specification-prescribed current range*." EX1003, ¶128; *see, e.g.*, EX1007, 59-60.

Further, a POSITA would have understood that Thomann desires the power range to be the product of the prescribed voltage and current ranges and thus Thomann teaches the drive strength adjustment "*to provide at least one of the output line potential and the output line current in a desired power range of a*

specification-prescribed potential range and a specification-prescribed current range." EX1003, ¶¶129, 103. In the combination, the "desired power range" is the product of the voltage range(s), between VOL MAX and VOL MIN and/or between VOH MAX and VOH MIN, and the current range(s), corresponding minimum and maximum currents for each of the four voltages (VOL MAX, VOL MIN, VOH MAX, and VOH MIN). *Id.*

3. Claim 2: "The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude."

Claim 2 is obvious over Lee and Thomann. In the combination, Lee is modified by Thomann's teachings of its calibration routine and the combination teaches "*the desired power range is determined by . . . a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*." *Supra* §X.B.1. As explained above for limitation [1.3], a POSITA would have understood that the desired power range corresponds to a desired potential range because power is equivalent to potential multiplied by current. EX1003, ¶131; *supra* §§X.A.1.d, X.B.2.b. Thomann specifies a VOH DRIVER output voltage range between VOH MAX and VOH MIN, a VOL DRIVER output voltage range between VOL MAX and VOL MIN,

and teaches that the VOH and VOL levels should be symmetric about VREF. *Supra* §X.B.2.b. As shown below, the desired power range is determined by VOH MIN and VOL MIN (annotated in purple), which are individually and collectively, "*a specification-prescribed lower potential limit value*" as they are lower in magnitude from the mid-point voltage VREF than VOH MAX and VOL MAX (in red).

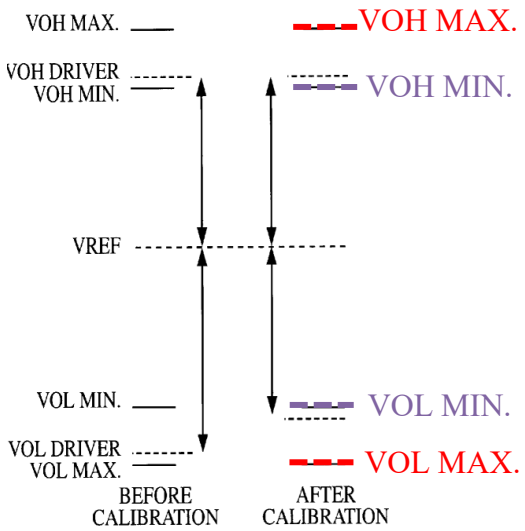


FIG. 3

EX1006, FIG. 3, 3:33-38, 6:23-31; EX1003, ¶131.

The desired power range is also determined by VOH DRIVER and VOL DRIVER, which are individually and collectively, "*a specification-prescribed*

lower potential limit value adjusted with the tolerance magnitude" [10] as VOH DRIVER is equivalent to VOH MIN ("*a specification-prescribed lower potential limit value*") increased by a tolerance magnitude (in blue) and VOL DRIVER is equivalent to VOL MIN ("*a specification-prescribed lower potential limit value*") decreased by the same tolerance magnitude (in blue), as shown by the annotations to Figure 3 of Thomann below.

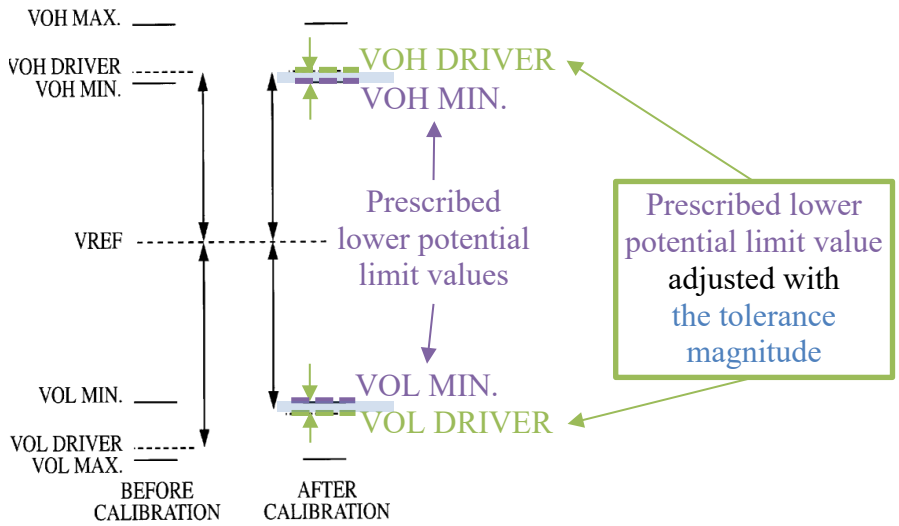


FIG. 3

[10] The '369 Patent does not define a particular amount of the tolerance magnitude, or specify whether it must be a fixed value or whether the adjustment with the tolerance magnitude is limited to, for example, adding the tolerance magnitude to the specification-prescribed lower potential limit value. *See* EX1001, 6:38-42; EX1003, ¶132.

EX1006, FIG. 3; EX1003, ¶133. Thomann discloses than the VOH and VOL levels of the driver should be symmetric about VREF. EX1006, 3:33-38, 6:23-31. A POSITA would have understood that the corresponding voltage range values, including the minimum values (VOH MIN. and VOL MIN.) and maximum values (VOH MAX. and VOL MAX.), are symmetric about VREF as well. EX1003, ¶133. Accordingly, a POSITA would have also understood that the tolerance magnitude between VOH DRIVER AND VOH MIN. and between VOL DRIVER and VOL MIN. are the same magnitude. EX1003, ¶133; *see* EX1006, 5:58-65, FIG. 3.

Although Thomann teaches that calibration adjusts the drive strengths of the pull-up or pull-down transistors, Thomann also teaches that, in a preferred embodiment, the drive strength of only one of the pull-up/pull-down transistors is adjusted. EX1006, 6:18-23; EX1003, ¶134. For example, as shown below, the VOL DRIVER can be calibrated by setting the pull-down transistors to a "minimum strength value … which can be adjusted up incrementally until it achieves a balanced driver with the pull-up transistor[s]." EX1006, 6:23-26.

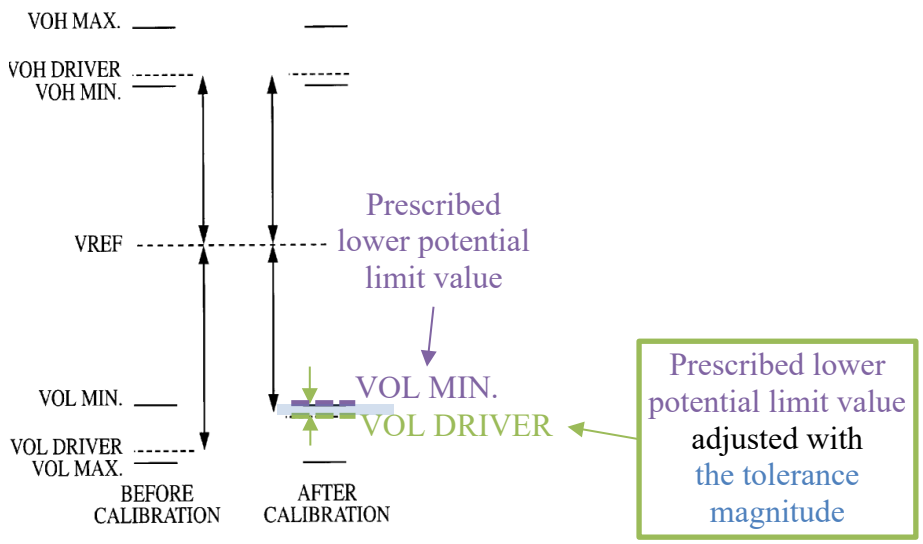


FIG. 3

EX1006, FIG. 3; EX1003, ¶134.

Thomann also explains that the VOH DRIVER can be calibrated by setting the pull-down transistors to a "maximum drive strength" and then "adjust[ing] the strength down until there is a balanced drive of the pull down transistor with the pull up transistor." EX1006, 6:26-31. This is shown below by the annotations to Figure 3 of Thomann in which VOH DRIVER is reduced to just above VOH MIN, adjusted with a tolerance magnitude (in blue).

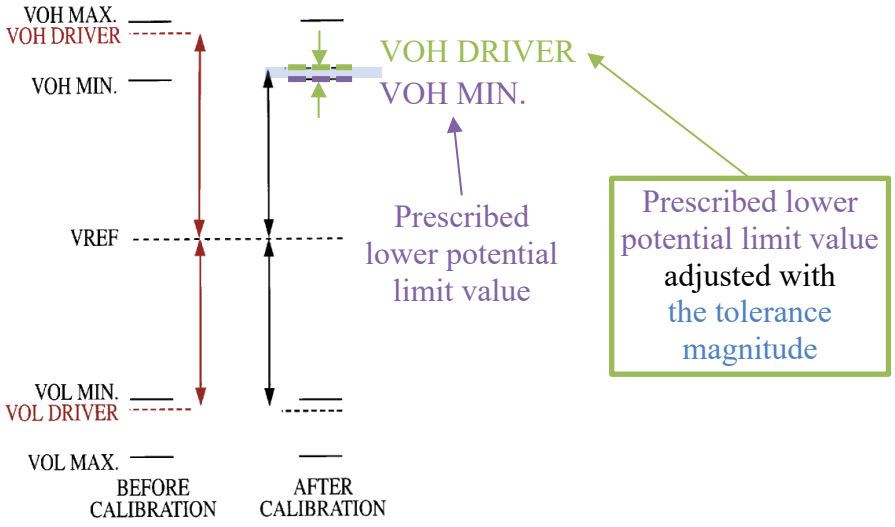


FIG. 3

EX1006, FIG. 3; EX1003, ¶135; *see* EX1006, 5:64-6:6, 6:26-31.

Thus, Thomann teaches that, in the combination, the output potential after calibration is in the desired power range determined by the current-voltage curves of the output driver transistors and the potential ranges for VOH and VOL, which include VOH MIN and VOL MIN ("*a specification-prescribed lower potential limit value*") and the output driver voltages VOH DRIVER and VOL DRIVER ("*a specification-prescribed lower potential limit value adjusted with the tolerance magnitude*"). EX1003, ¶131-36.

4. Claims 5-7

Claims 5-7 depend from claim 1, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Lee teaches the additional limitations of claims 5-7. *Supra* §§X.A.3-X.A.5; EX1003, ¶¶137-38.

C. Ground 3: Claims 1-7 and 14-16 are obvious over Lee and JESD79

1. Motivation to Combine Lee and JESD79

Ground 3 combines Lee with JESD79. As explained below, JESD79 is a memory specification that discloses prescribed potential and current ranges for pulldown and pullup paths of an output driver.

A POSITA would have been motivated to combine Lee with JESD79, and had a reasonable expectation of success in doing so, because both references relate to drive strengths of pull-up and pull-down devices for an output driver. EX1005, 1; EX1007, 59-60; EX1003, ¶¶139-48. Lee discloses an output buffer driver with drive strength adjustment. EX1005, FIG. 1, 3:13-32, 4:31-61; EX1003, ¶141; *supra* §IX.A. Lee expressly contemplates using its driver in memory circuits, including Dynamic Random Access Memory (DRAM), specifically. EX1005, 2:11-20, 7:38-47; EX1003, ¶141. JESD79 is a memory specification for DRAM, specifically Double Data Rate (DDR) Synchronous DRAM (SDRAM). EX1007, 1, 4-5; *supra* §IX.C.

Lee recognizes that output drivers have specified current versus voltage (I-V) curves with minimum and maximum limits and that the output buffer currents are well matched when the mid-voltage is at VREF, but it does not disclose examples of the I-V curves or specific currents for a well-matched driver. EX1005, 1:30-34; EX1003, ¶142. However, JESD79 does provide these details, providing I-

V curves for the output driver, including minimum, maximum, typical low, and typical high I-V curves for the pull-up and pull-down transistor(s) of the output driver. EX1007, 59-60; EX1003, ¶142. JESD79 also discloses a weak drive-strength curves for lighter loads and/or point-to-point environments. EX1007, 16; EX1003, ¶142.

As shown below, JESD79 discloses that for a normal drive strength the range of the pulldown I-V curve spans between maximum and minimum curves and it is recommended the range of the typical high and typical low curves fall within the lower portion between the maximum and minimum curves.

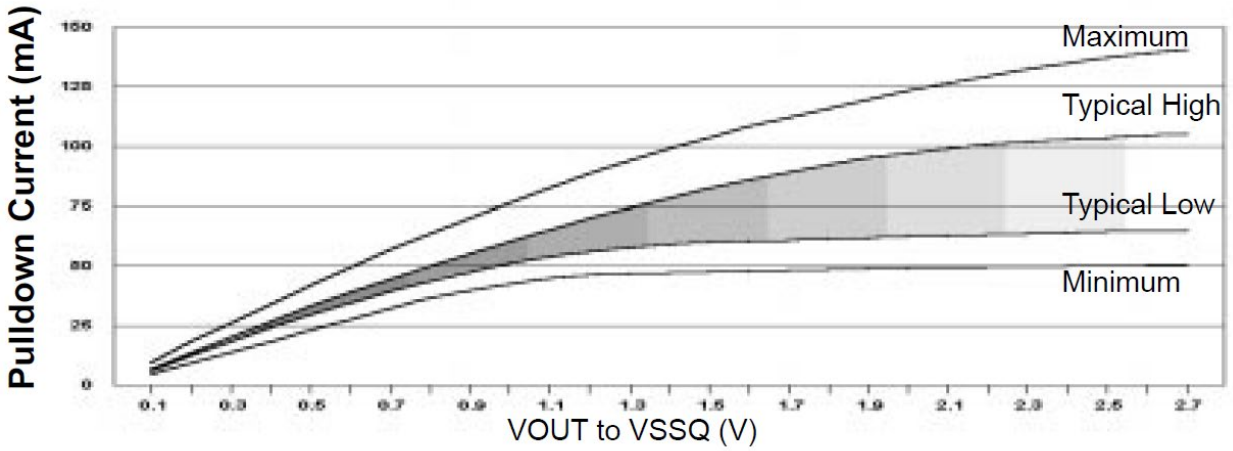


Figure a: Pulldown Characteristics

EX1007, 59-60; EX1003, ¶143. For example, at a voltage of 2.5 volts, the current ranges between a minimum of 50.2 milliamps and a maximum of 137.3 milliamps, within which the desired typical current ranges between 64.6 and 103.8 milliamps. *Id.*

Similarly, the range of the pullup I-V curve spans between maximum and minimum curves and is recommended to be in the range of the typical high and typical low curves.

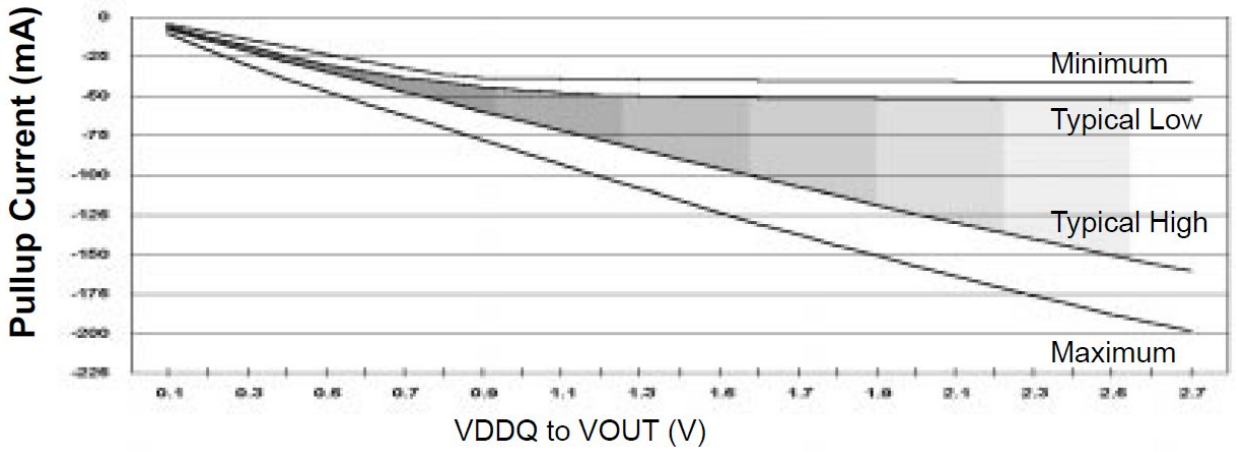


Figure b: Pull Up Characteristics

EX1007, 59-60; EX1003, ¶144. For example, at a voltage of 2.5 volts, the current ranges from a minimum magnitude of 41.0 milliamps and a maximum magnitude of 187.6 milliamps, within which the desired typical current ranges between a magnitude of 52.5 and 150.5 milliamps. *Id.*

JESD79 also teaches there are similar I-V curves for the weak drive strength setting, which represents a strength setting for lighter loads and/or point-to-point environments. EX1007, 16; EX1003, ¶144.

The curves specified by JESD79 also disclose an output voltage of the driver relative to VDDQ, a power supply potential for a DQ memory pin, and VSSQ, a ground potential for a DQ memory pin. EX1007, 11, 58. In the combination, a

POSITA would have understood that VDDQ is a power supply for Lee's output driver and VSSQ is a ground potential, as shown in the figure below:

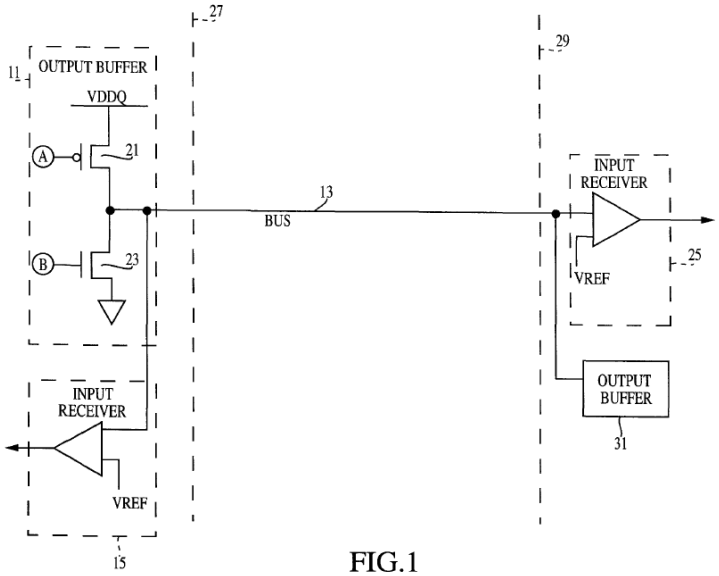


FIG.1

EX1005, FIG. 1; EX1003, ¶145.

Thus, a POSITA would have been motivated to implement Lee's feedback control logic in accordance with the teachings of JESD79 that specify the I-V curves for the pullup and pulldown transistors of Lee's buffer output driver for memory. EX1003, ¶146. This straightforward modification of Lee's control logic in view of the voltages and currents prescribed in JESD79 and the knowledge of a POSITA simply uses a known technique (e.g., setting the drive strength consistent with the I-V curves in JESD79) to improve a similar device (e.g., Lees' output buffer driver with feedback control logic) in the same way (e.g., setting the feedback control logic to adjust the drive strength consistent with the I-V curves in JESD79). EX1003, ¶146. Additionally, the modification simply applies a known

technique (e.g., setting the drive strength consistent with the I-V curves in JESD79) to a known device (e.g., an output buffer driver with calibration) that is ready for improvement to yield predictable results (e.g., a driver with drive strength settings such that the driver operates in a desired lower, typical range for the specified I-V curves). *Id.* Lee contemplates that his active calibration scheme can further improve upon fixed driver strengths settings based on specified curves, "by adjusting out the effects of process variance, voltage variation or temperature variation on output buffer drivers." EX1005, 1:34-38. In fact, it was well-known that a driver strength setting can be adjusted by, for example, adjusting the number of transistors enabled or the effective width of the transistors, to operate above a minimum voltage level, which minimizes power dissipation during voltage swings while allowing the current through the transistors of the driver to be largely independent of voltage. *See* EX1010, 7:28-8:32, FIGS. 4-5; EX1003, ¶147.

Further, a POSITA would have been motivated to implement Lee in accordance with well-known memory standards like JESD79. EX1003, ¶148. Using such standards for implementation ensures interoperability, proper operation, and compliance between the components in memory systems, such as a processor and memory devices. EX1003, ¶148; *see, e.g.*, EX1005, FIG. 7. Accordingly, a POSITA implementing Lee would have looked to JESD79, a well-

known memory standard to ensure interoperability, proper operation, and compliance of Lee's system. *Id.*

2. Claim 1

a. Claim limitations [1.P], [1.1], [1.2], and [1.4]

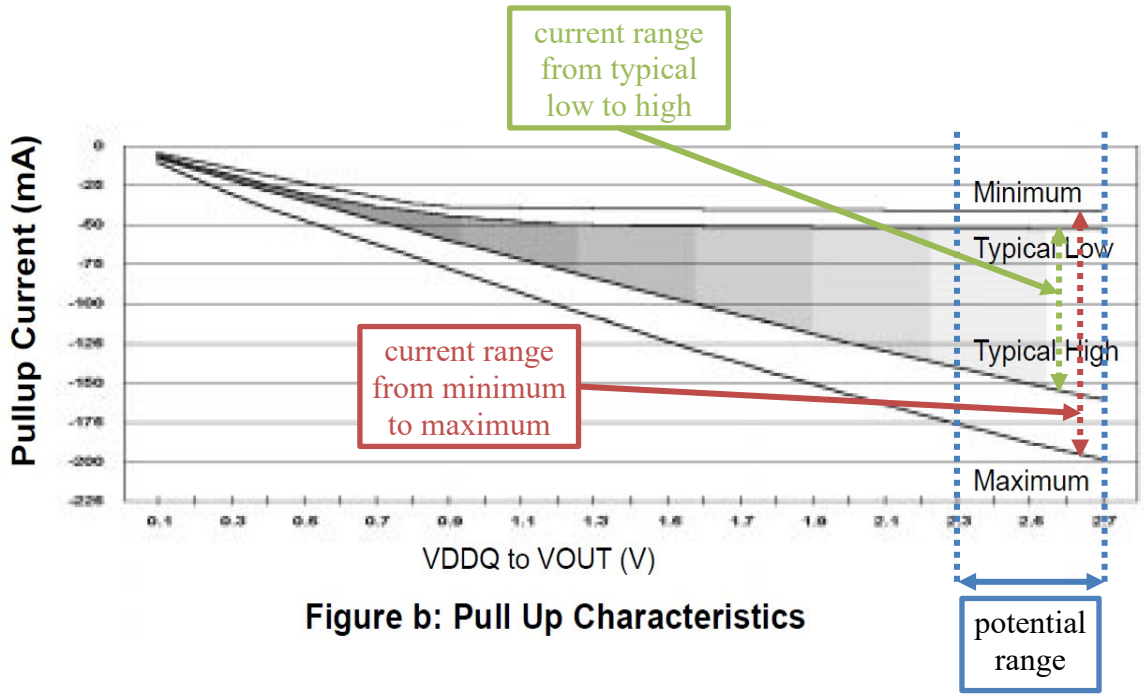
As explained above for Ground 1, Lee teaches limitations [1.P], [1.1], [1.2], and [1.4] to the extent each is limiting and supported by the '369 Specification. *Supra* §X.A.1.a-X.A.1.c, X.A.1.e; *see* EX1005, 3:13-56, 4:36-61, 5:28-58, 7:22-32, 7:57-67, FIGS. 1, 2, 4-7; *see also* EX1007, 16 (disclosing output drive strength options); 58-60 (disclosing input voltage levels, output currents and voltages, and "characteristic V-I data points"); EX1003, ¶149-51, 158.

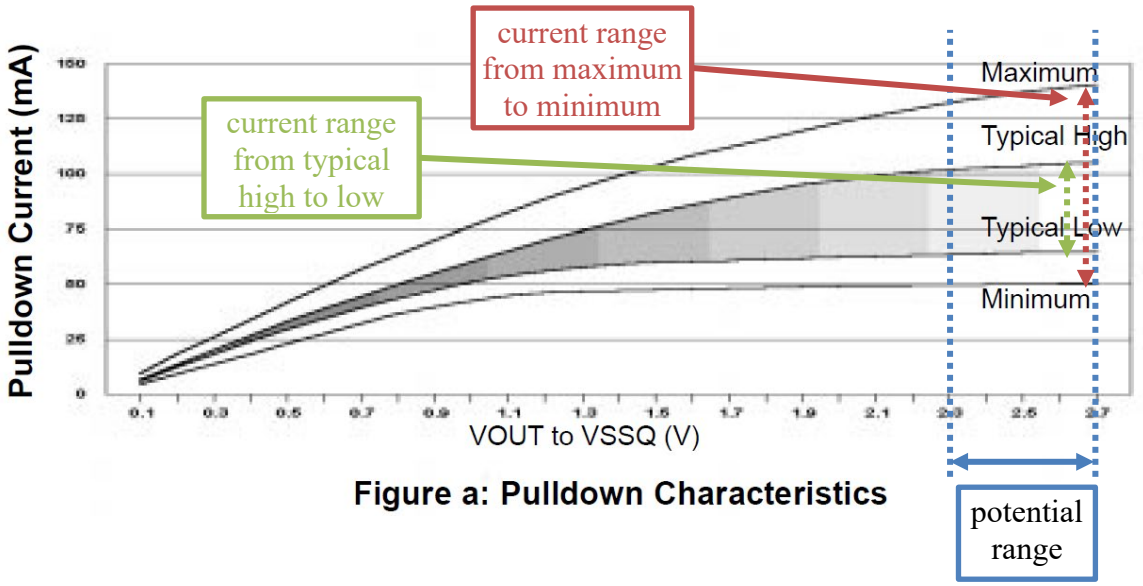
b. "a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range," [1.3]

As explained above for Ground 1, Lee teaches limitation [1.3]. *Supra* §X.A.1.d; *see* EX1005, 1:26-33, 1:61-63, 2:39-44, 3:6-24, 3:33-41, 3:47-53, 4:6-61, 4:62-5:27, 10:6-12, FIGS. 1, 2; EX1003, ¶152.

To the extent claim limitation [1.3] requires a prescribed potential range and prescribed current range that is in a memory standard specification, Lee's calibration logic (including "a control unit"), as modified by JESD79's teachings of setting a drive strength consistent with the desired, lower typical I-V curves,

provides a control signal for driver strength settings to provide the output line potential "*in a desired power range of a specification-prescribed potential range and a specification-prescribed current range*." EX1003, ¶¶153-57. JESD79 specifies "*a specification-prescribed current range*" between the maximum and minimum current to voltage (I-V) curves (annotated in red), as shown below for the pullup and pulldown transistors of the output driver.





EX1007, 59-60; EX1003, ¶154. For example, at a voltage of 2.5 volts, the pull-up current ranges from a minimum magnitude of 41.0 milliamps and a maximum magnitude of 187.6 milliamps and the pull-down current ranges from a minimum of 50.2 milliamps and a maximum of 137.3 milliamps. *Id.*

Further, the I-V curves also specify "*a specification-prescribed potential range*" between a minimum input/output (I/O) supply voltage, VDDQ, of 2.3 volts and a maximum I/O supply voltage of 2.7 volts, as annotated in blue above and in the table below. EX1007, 11, 58. A POSITA would have understood that the driver output in the combination would swing during normal operation between the prescribed range for VDDQ and a ground potential (e.g., VSSQ). *Id.*; EX1005, FIGS. 1, 4, 6; EX1003, ¶155. A POSITA would also have understood that in the combination the driver output would vary during calibration between 49 percent

and 51 percent of VDDQ, as specified by JESD79 for the I/O reference voltage VREF:

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6

EX1007, 58; *see also* EX1005, FIG. 1, 5:8-11, 5:29-32; EX1003, ¶156.

Further, a POSITA would have understood that the specified current range(s) and potential range(s) by the JESD79 collectively specify a "*desired power range*" in the combination because power is equivalent to current multiplied voltage and because, as shown in the figures below, the typical curves lie between the minimum and maximum curves.

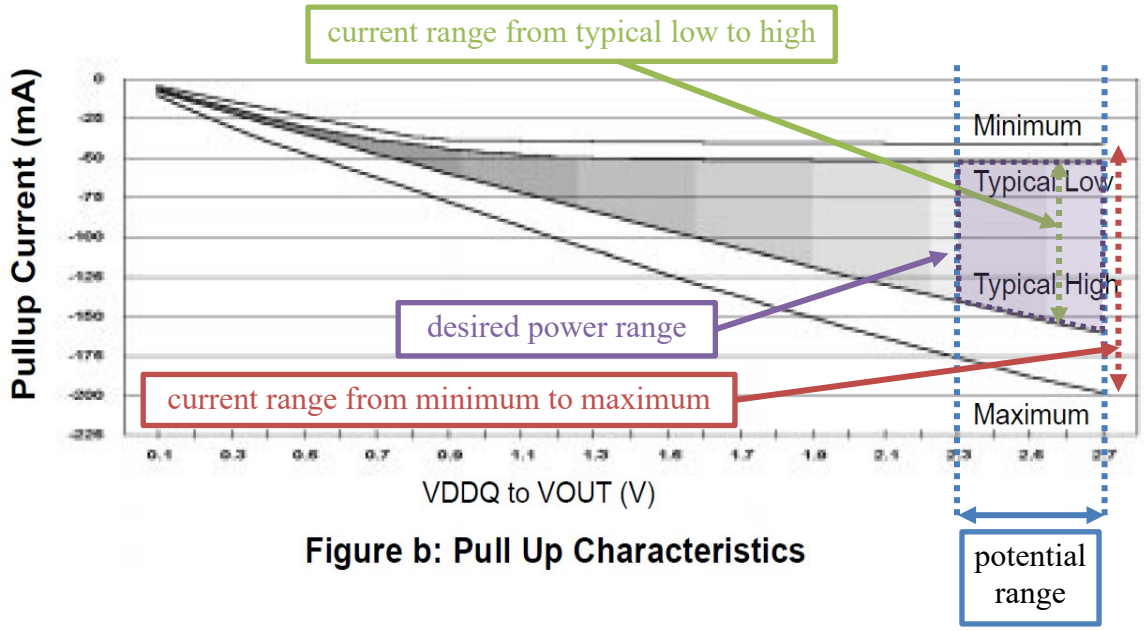


Figure b: Pull Up Characteristics

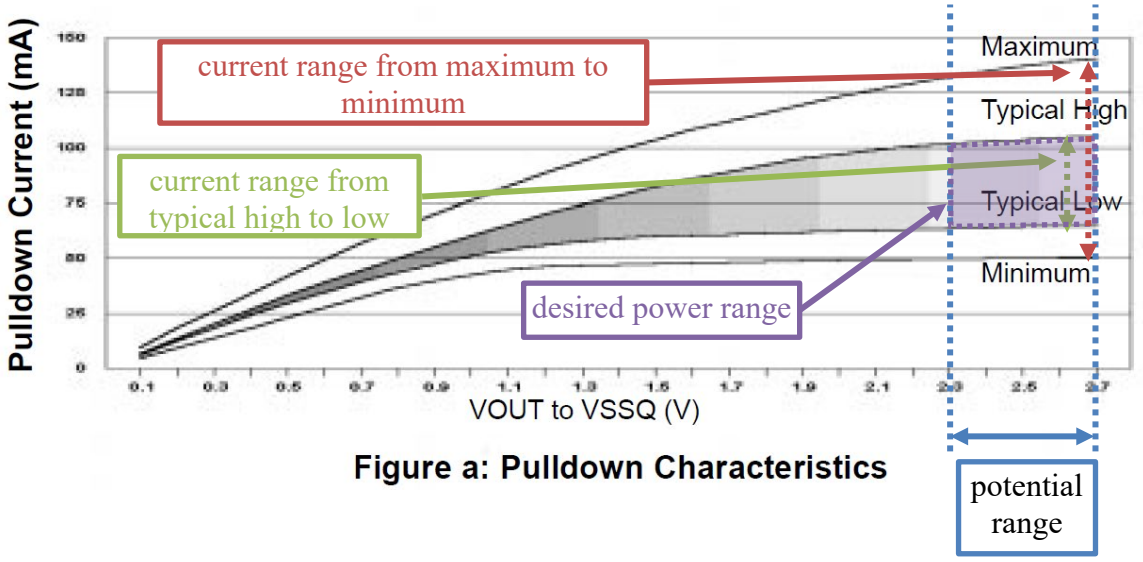


Figure a: Pulldown Characteristics

EX1007, 59-60; EX1003, ¶157. As shown in green, the current range(s) span between typical high to low, and the potential range(s) span between 2.3 and 2.7 volts. *See id.* A POSITA would thus have understood that in the combination, the desired power range (annotated in purple above) corresponds to the typical curves and the prescribed voltage range. EX1003, ¶157.

3. Claim 2: "The output driver of claim 1, wherein the desired power range is determined by one of a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude, a specification-prescribed lower potential limit value and a specification-prescribed lower potential limit value adjusted with the tolerance magnitude."

As explained above for Ground 1, Lee teaches claim 2 under Patent Owner's interpretation. *Supra* §X.A.2.

To the extent the scope of claim 2 is narrower than Patent Owner's interpretation that VREF is "*a specification-prescribed lower potential limit*

value," it would have been obvious over Lee and JESD79. In the combination, Lee is modified by JESD79's teachings regarding prescribed current and voltage range(s) such that "*the desired power range is determined by . . . a specification-prescribed lower current limit value, a specification-prescribed lower current limit value adjusted with a tolerance magnitude,* [and] *a specification-prescribed lower potential limit value . . . .*" As explained above for limitation [1.3], a POSITA would have understood that the desired power range can correspond to a potential range and a current range because power is equivalent to potential multiplied by current. EX1003, ¶160; *supra* §§X.A.1.d, X.B.2.b.

JESD79 species a desired potential range, such as a range for voltage VDDQ and a range for voltage VREF, as shown below.

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6

EX1007, 58; *supra* §X.C.2.b; *see also* EX1005, FIG. 1; EX1003, ¶161. JESD79 prescribes "*lower potential limit value*" of 2.3 volts for VDDQ and 0.49 percent of 2.3 volts or 1.15 volts for VREF. *Id.*

JESD79 also specifies a desired current range, such as between the typical high and typical low I-V curves, which are within the maximum and minimum I-V curves, as shown below.

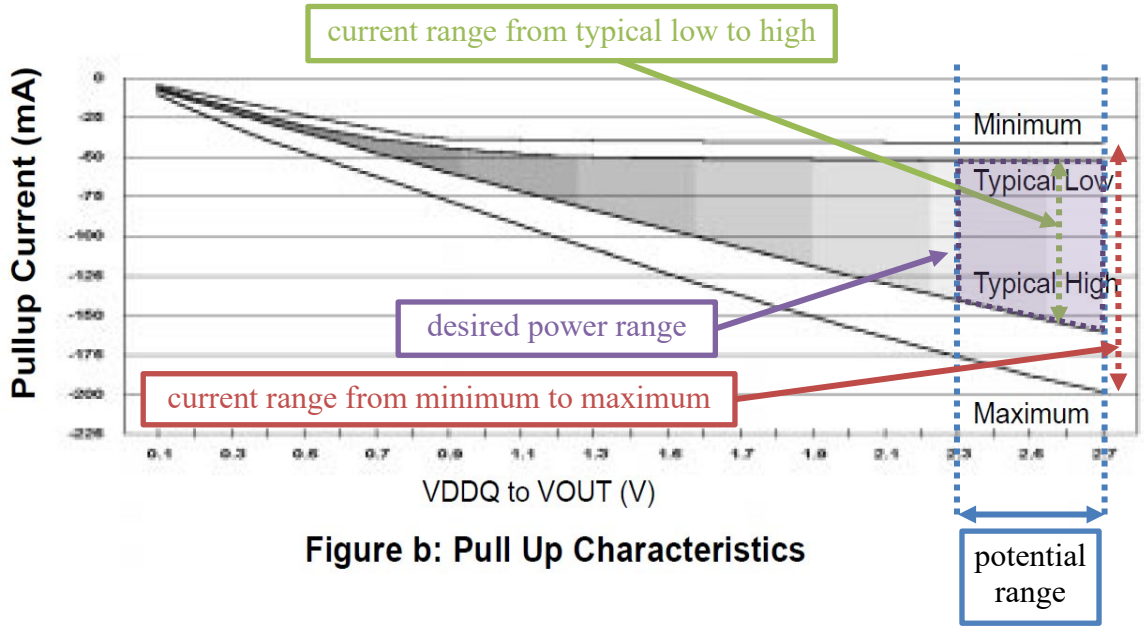


Figure b: Pull Up Characteristics

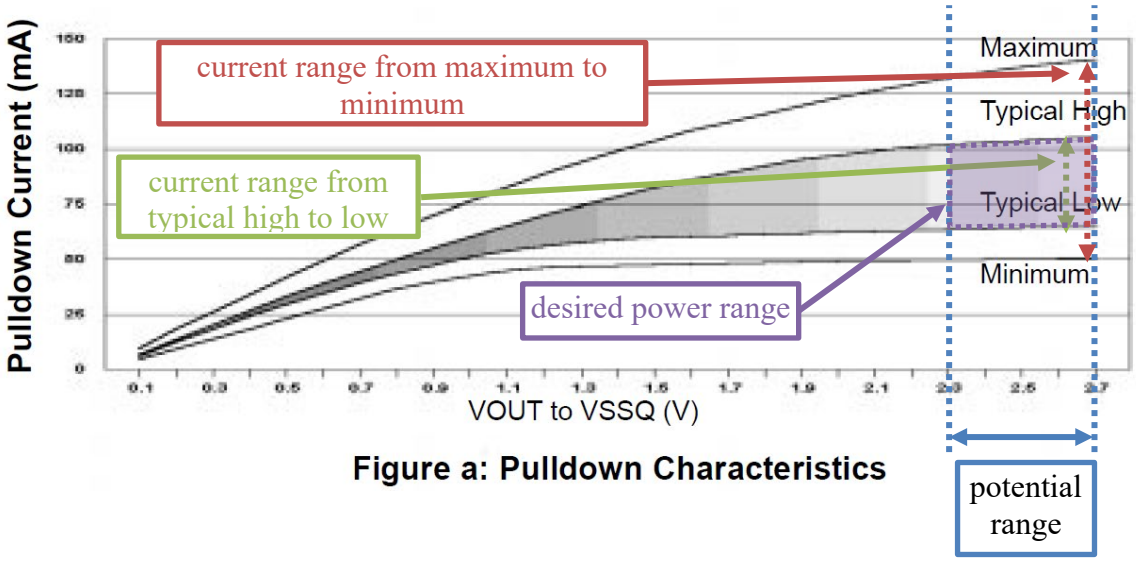


Figure a: Pulldown Characteristics

EX1007, 58-60; *supra* §X.C.2.b; *see also* EX1003, ¶162. As shown by the red annotations in the figures above, the minimum curve at the end of the current

range(s) corresponds to the "*specification-prescribed lower current limit value*" as the minimum curve is lower than the maximum curve. *Id.* Further, as shown by the green annotations, the typical low curve at the end of the narrower and lower current range(s) corresponds to the "*specification-prescribed lower current limit value adjusted with a tolerance magnitude*" as the typical low curve is adjusted relative to the minimum curve by a tolerance magnitude. *Id.*

For example, at 2.3 volts, the pull-down current range is between 49.9 and 132.4 milliamps with a desired typical range between 63.8 and 101.9 milliamps and the magnitude for the pull-up current range is between 40.8 and 176 milliamps with a desired typical range between 52.2 and 139.9 milliamps:

	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.9	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	–155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	–160.1	–41.2	–198.2

EX1007, 60. Accordingly, JESD79 prescribes for a voltage of 2.3 volts a "*specification-prescribed lower current limit value*" of 40.8 milliamps for the pull-up current and 49.9 milliamps for the pulldown current (as shown by the lower end of the current range in red in the figures above) and a "*specification-prescribed lower current limit value adjusted with a tolerance magnitude*" of 52.2 milliamps and 63.8 milliamps (shown by typical low curve in green in the figures above) in

which the adjusted tolerance magnitude is 11.4 and 13.8 milliamps relative to the "*specification-prescribed lower current limit value*." *Id.*; EX1003, ¶163. Further, JESD79 teaches that the ratio of typical pullup to pulldown current should be within a tolerance of 10 percent. EX1007, 59. Accordingly, a POSITA would have been motivated to also adjust the pull-up and pull-down current limits such that they were within a tolerance of 10 percent of each other. EX1003, ¶163.

Accordingly, in the combination, JESD79 teaches a desired power range determined by "*a specification-prescribed lower current limit value,*" "*a specification-prescribed lower current limit value adjusted with a tolerance magnitude,*" and "*a specification-prescribed lower potential limit value*." EX1003, ¶¶159-64.

4. Claim 3: "The output driver of claim 1, wherein the driver circuit includes a pull-up path defined by a first maximum and minimum current/potential (I/V) characteristic curve and a pull-down path defined by a second maximum and minimum I/V characteristic curve and wherein the desired power range is determined depending on respectively activated pull-up path and pull-down path of the driver circuit."

As explained above, Lee discloses a driver circuit with "a pull-up path" (via transistor 21) and "a pull-down path" (via transistor 23).

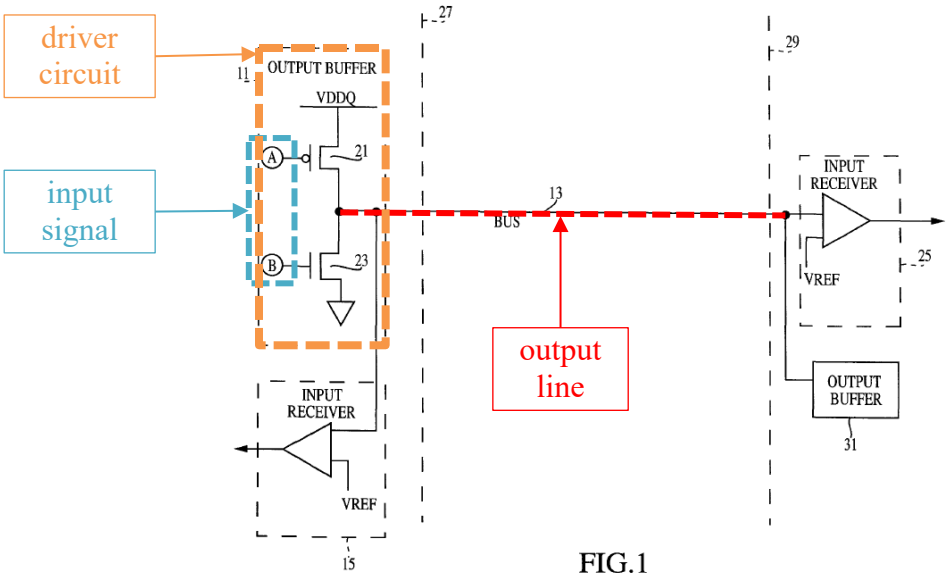


FIG.1

EX1005, FIGS. 1, 4; EX1003, ¶165. When the input is low, the driver activates the pull-up path to provide current to pull the bus (13) toward VDDQ and when the input is high, the driver activates the pull-down path to provide current to pull the bus toward ground. EX1005, 3:33-53; EX1003, ¶165.

As shown in JESD79's figures below, Lee in view of JESD79 teaches that the pull-up and pull-down paths each have a maximum and a minimum characteristic current/potential (I-V) curve.

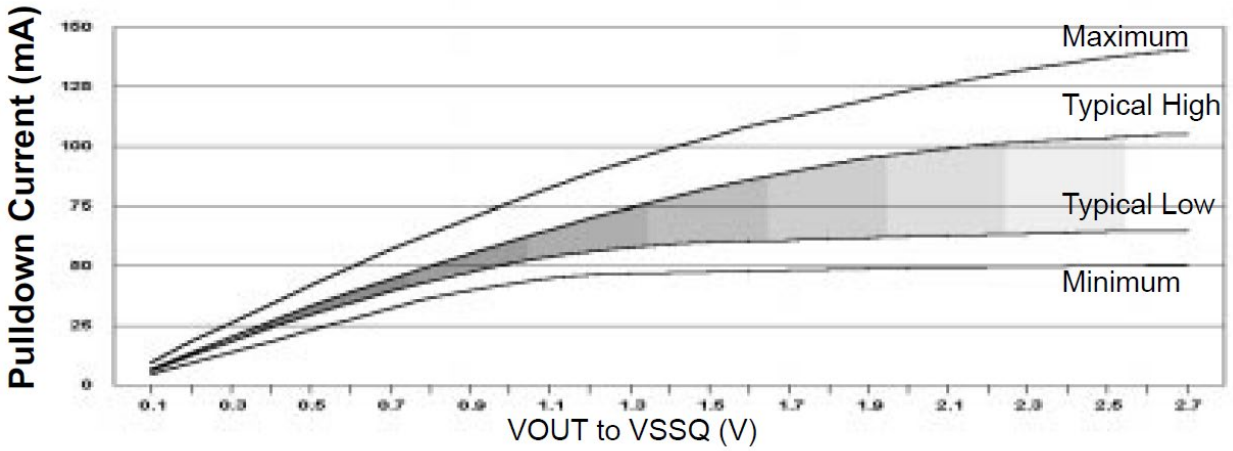


Figure a: Pulldown Characteristics

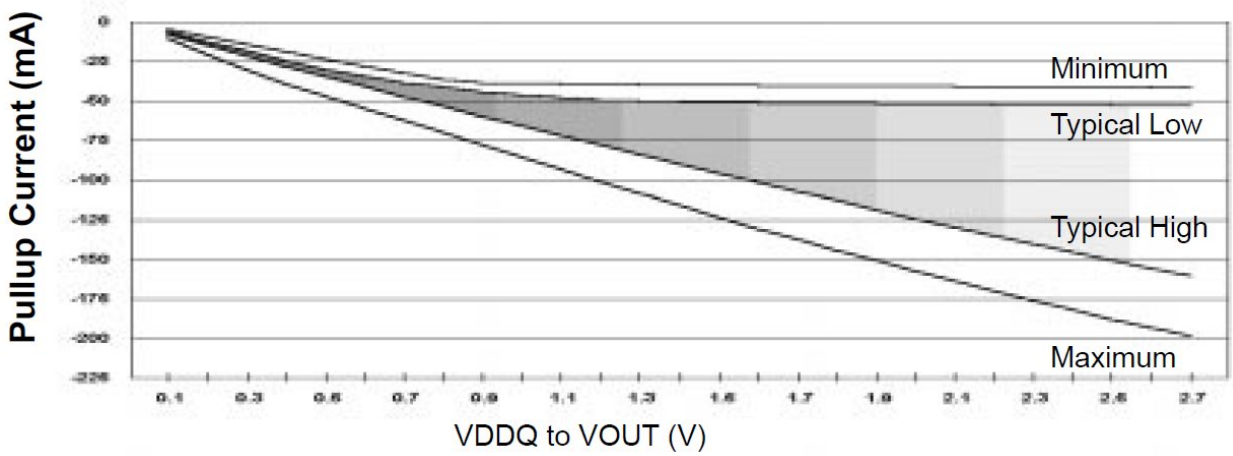


Figure b: Pull Up Characteristics

EX1007, 59-60; EX1003, ¶166.

Further, as explained above, the "*desired power range*" corresponds to these I/V curves and is determined based on the activation of the pull-up or pull-down path. *Supra* §X.C.2.b; EX1003, ¶167; *see, e.g.*, EX1007, 55.

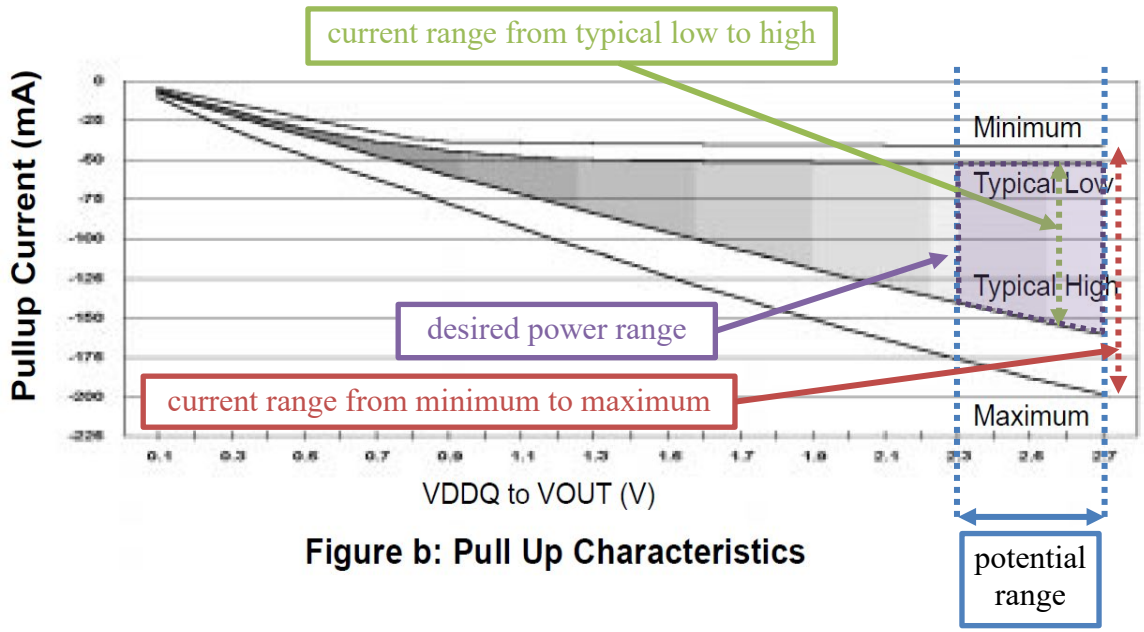


Figure b: Pull Up Characteristics

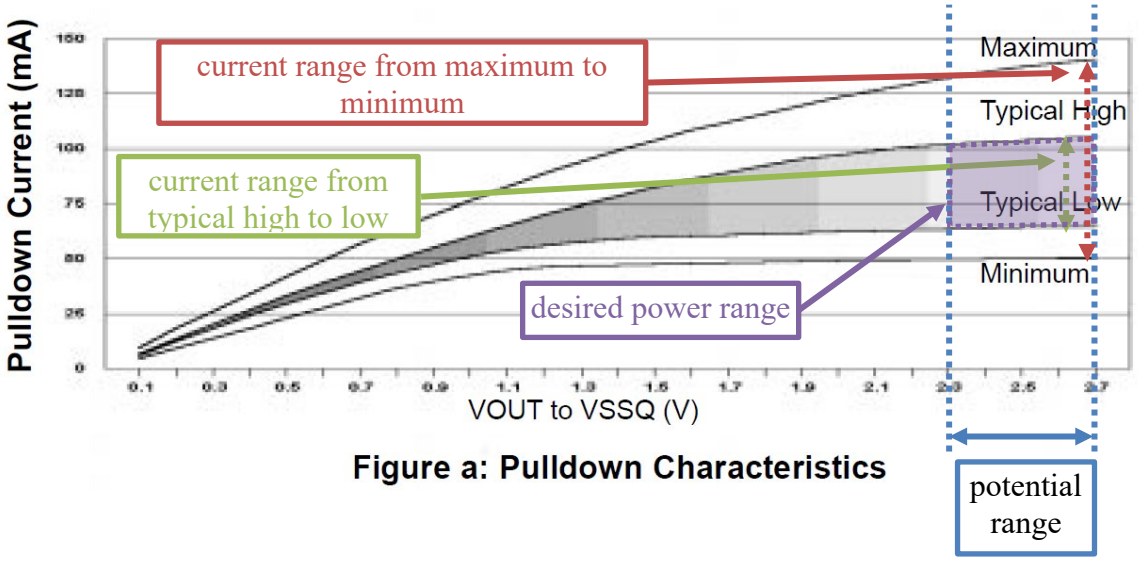


Figure a: Pulldown Characteristics

EX1007, 59-60; EX1003, ¶167; *supra* §X.C.2.d. Thus, Lee in view of JESD79 teaches claim 3. EX1003, ¶¶165-67.

5. Claim 4: "The output driver of claim 1, wherein the desired power range corresponds to a lower portion of the specification-

prescribed potential range and a lower portion of the specification-prescribed current range."

Lee in view of JESD79 teaches claim 4. EX1003, ¶¶168-69. As shown below, the combination teaches a "*desired power range*" for the pull-up and pull-down paths.

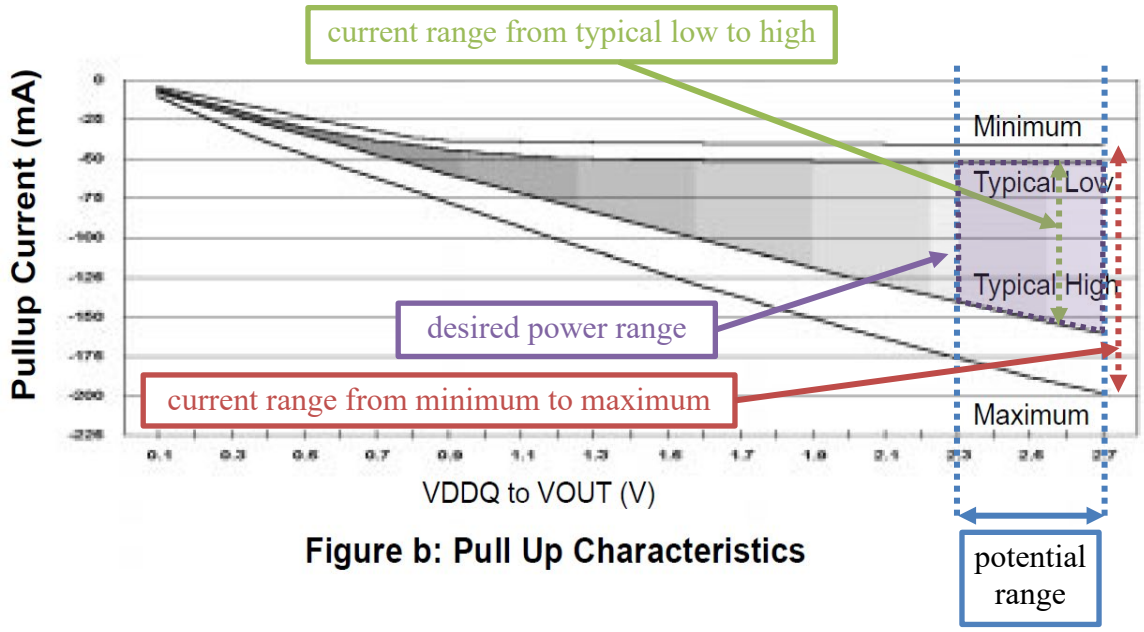


Figure b: Pull Up Characteristics

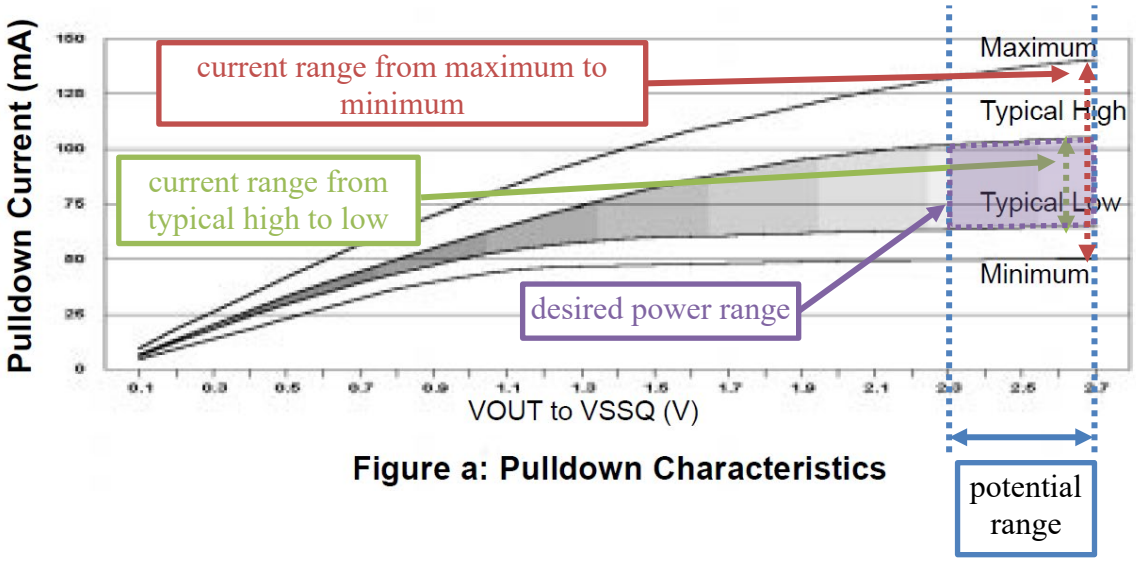


Figure a: Pulldown Characteristics

EX1007, 59-60; EX1003, ¶168; *supra* §X.C.2.b (claim [1.3]). As shown, the desired power range corresponds to a typical current range (annotated vertical range in green) that is between the typical high and low current curves, which are lower than the maximum current curves. *Id.* Accordingly, a POSITA would have understood that the "*desired power range*" in the combination corresponds to "*a lower portion of the specification-prescribed current range*" because the typical current range is lower than the maximum curve and because the typical current range (in green above) is narrower and in a lower portion of the specification-prescribed current range (annotated vertical range in red). EX1003, ¶168.

Further, JESD79 discloses that for a semiconductor process technology with slow NMOS and slow PMOS transistors, the voltage VDDQ is at 2.3V, and for a process technology with typical NMOS and PMOS transistors, the voltage VDDQ is around 2.5 volts. EX1007, 60. Indeed, a POSITA would have recognized that a range of operation between the voltages for slow and typical semiconductor process technologies would support minimizing the voltage and power of the driver during operation in which the output voltage swings between logical low (e.g., around 0 volts) and logical high (e.g., around VDDQ). EX1003, ¶169; *see, e.g.*, EX1010, 8:13-32, FIG. 5 (defining a range above a minimum level that minimizes voltage and power). A POSITA would have understood that the "*desired power range*" in the combination corresponds to "*a lower portion of the*

specification-prescribed potential range" because it corresponds more specifically to a voltage between 2.3 and 2.5 volts, which is lower than the maximum voltage of 2.7 volts for VDDQ and is narrower and in a lower portion of the specification-prescribed range (annotated horizontal range above in blue). EX1003, ¶169; EX1007, 58-60.

6. Claims 5-7

Claims 5-7 depend from claim 1, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Lee teaches the additional limitations of claims 5-7. *Supra* §§X.A.3-X.A.5; EX1003, ¶¶170-71.

7. Claim 14

a. "A method for driving an output driver for an integrated circuit having a driver circuit driving an input signal onto an output line, comprising:" [14.P]

For the reasons provided above for claim limitations [1.P] and [1.1], Lee teaches the preamble of claim 14 to the extent it is limiting. *Supra* §§X.A.1.a-X.A.1.b, X.C.2.a-X.C.2.b. Lee discloses driving an output driver (in purple below) for an integrated circuit, such as memory or processors, with a driver circuit (in orange) that drives an input signal (in blue) onto an output line (in red).

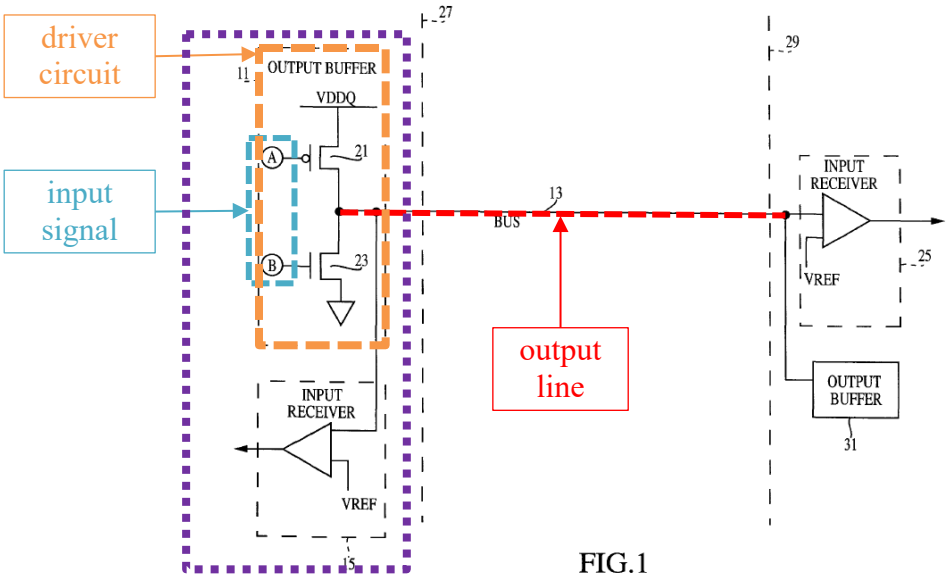

driver circuit
input signal
OUTPUT BUFFER
VDDQ
11
21
23
A
B
27
29
13
BUS
INPUT RECEIVER
VREF
25
output line
OUTPUT BUFFER
31
INPUT RECEIVER
VREF
15

FIG.1

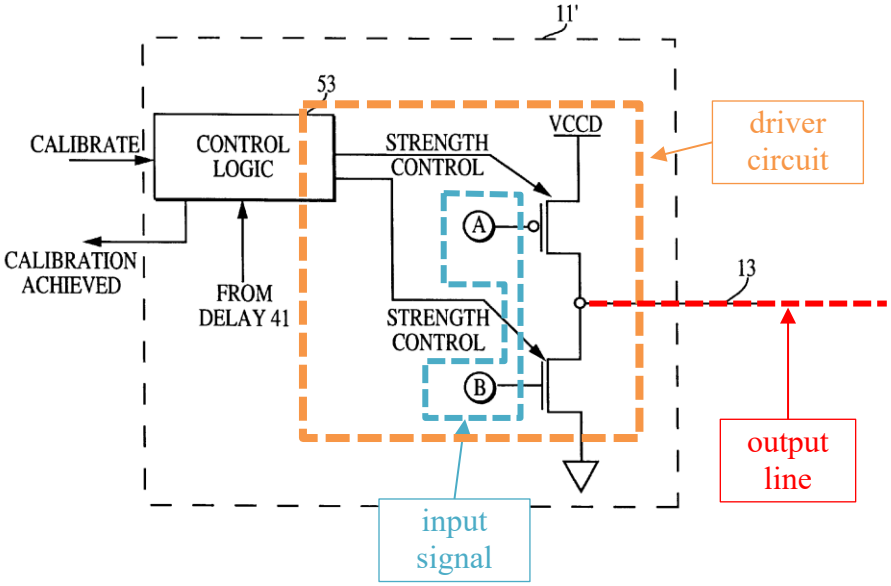

11'
53
CALIBRATE
CONTROL LOGIC
STRENGTH CONTROL
VCCD
driver circuit
CALIBRATION ACHIEVED
FROM DELAY 41
STRENGTH CONTROL
A
B
13
output line
input signal

FIG. 4

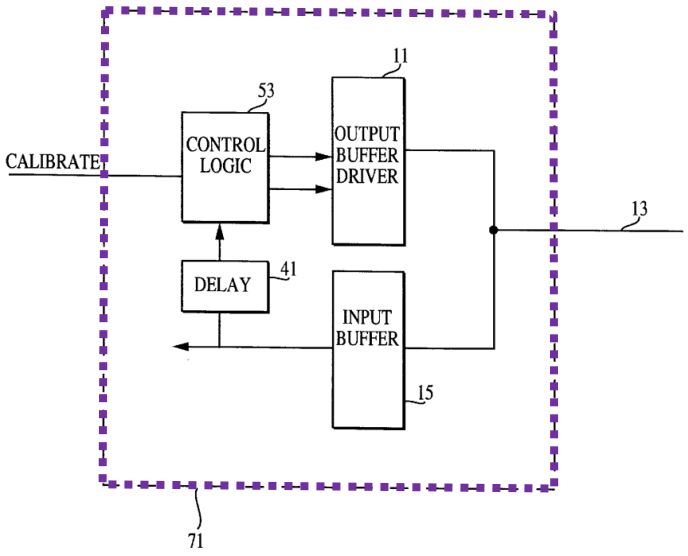


FIG. 5

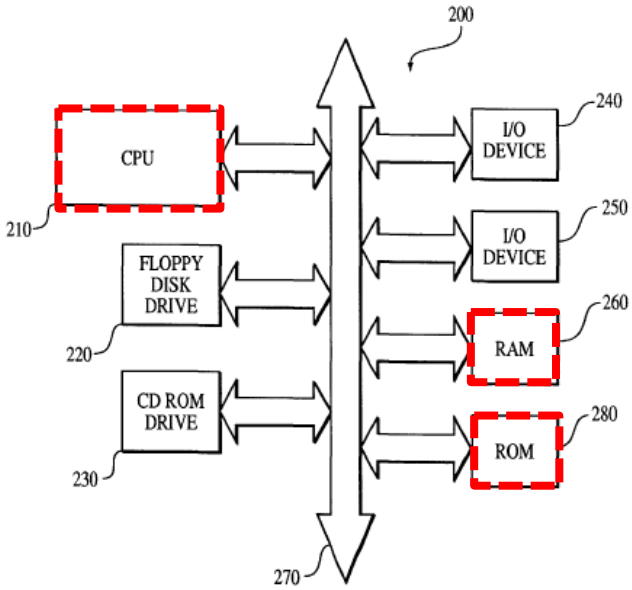


FIG.7

EX1005, 3:13-32, 7:57-67, FIGS. 1, 4, 5, 7; *see also* EX1003, ¶172; EX1005, 1:39-44, FIG. 6.

b. "measuring at least one of an output line current and an output line potential; and" [14.1]

As explained for limitation [1.2], Lee teaches "*a measuring circuit for measuring at least one of an output line current and an output line potential*" to the extent it is supported by the '369 Specification, and thus also teaches this limitation. *Supra* §§X.A.1.c, X.C.2.a; EX1005, FIG. 1, 3:43-46, 4:46-49, 5:28-31, 7:22-26; *see also* EX1003, ¶173.

c. "controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range, respectively," [14.2]

As explained for limitation [1.3], Lee in view of JESD79 teaches "*a control unit … for setting a driver strength … to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range*" and thus also teaches this limitation. *Supra* §X.C.2.b; *see* EX1005, 1:26-33, 1:61-63, 3:6-9, 3:47-53, 4:6-34, 4:46-5:27, FIGS. 1, 2; EX1007, 11, 59-60; EX1003, ¶174.

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1–5, 16) (0°C ≤ TA ≤ 70°C; VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6

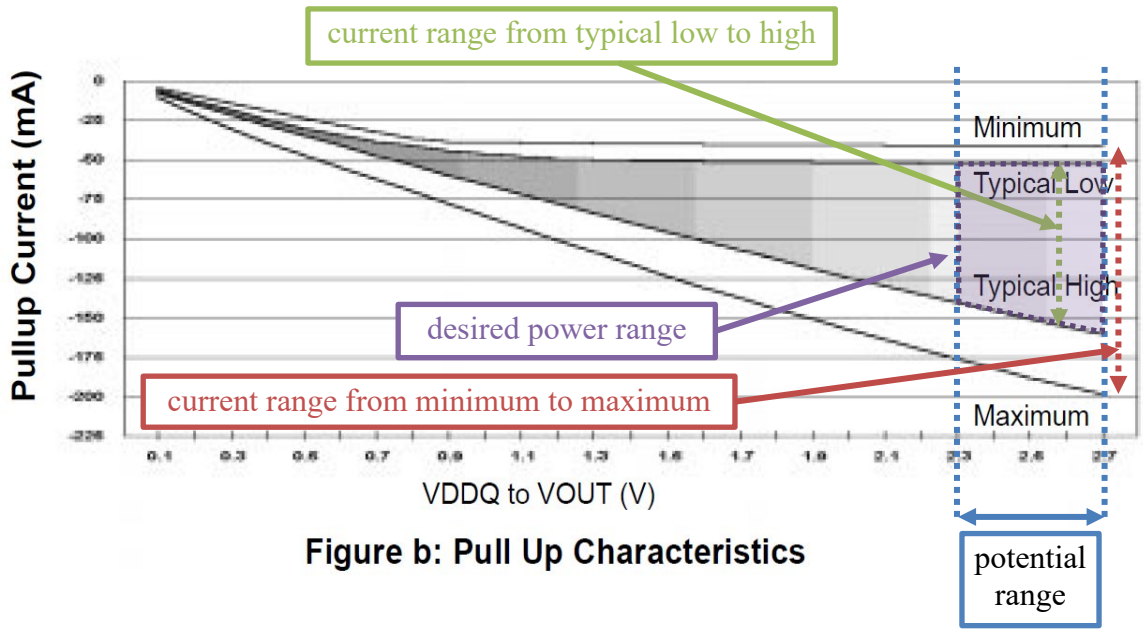


Figure b: Pull Up Characteristics

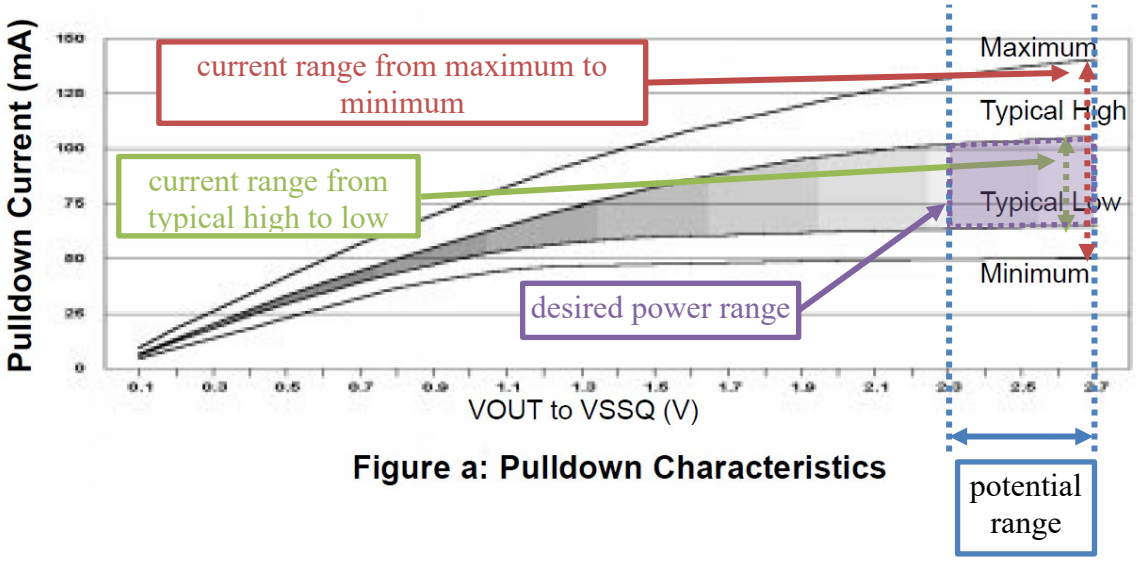
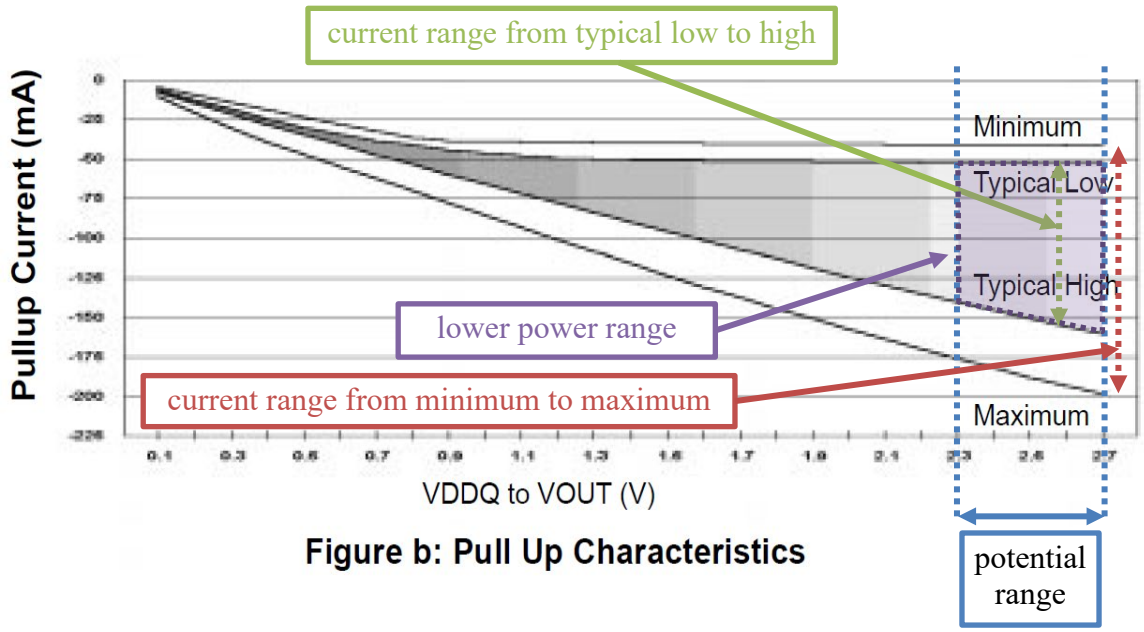


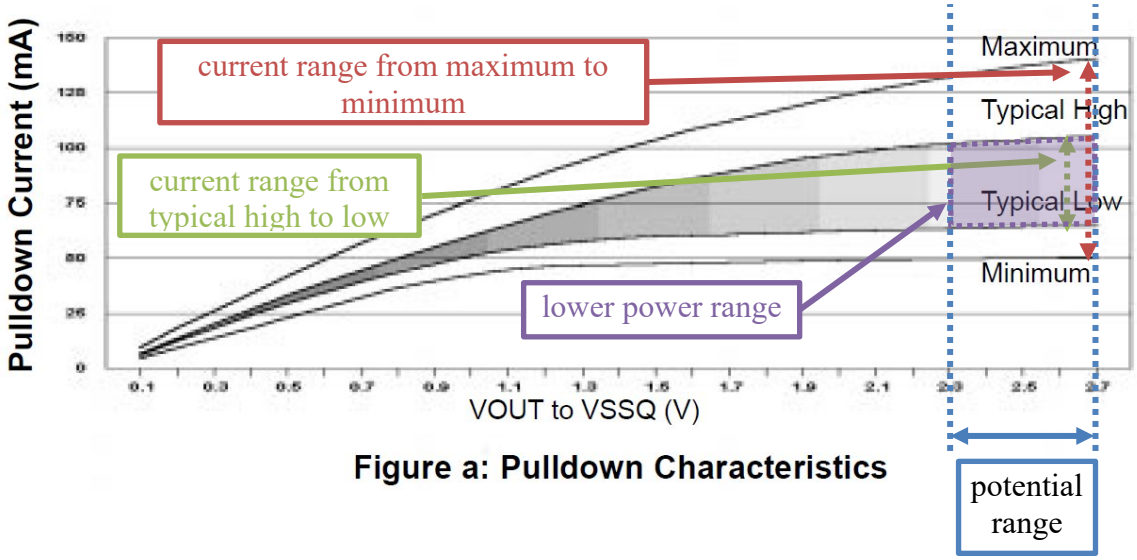
Figure a: Pulldown Characteristics

d. "wherein the driver strength is set such that the potential and the current intensity lie in a lower power range of the specification-prescribed current range and the specification-prescribed potential range, and" [14.3]

As explained for claim 4, Lee in view of JESD79 teaches a "*desired power range [that] corresponds to a lower portion of the specification-prescribed potential range and a lower portion of the specification-prescribed current range*"

Supra §§X.C.4 (claim 4), X.C.2.b (limitation [1.3]). For the reasons provided above, the combination teaches this limitation, including "*a lower power range*" that corresponds to the "*lower portion*" of the prescribed potential and current ranges.





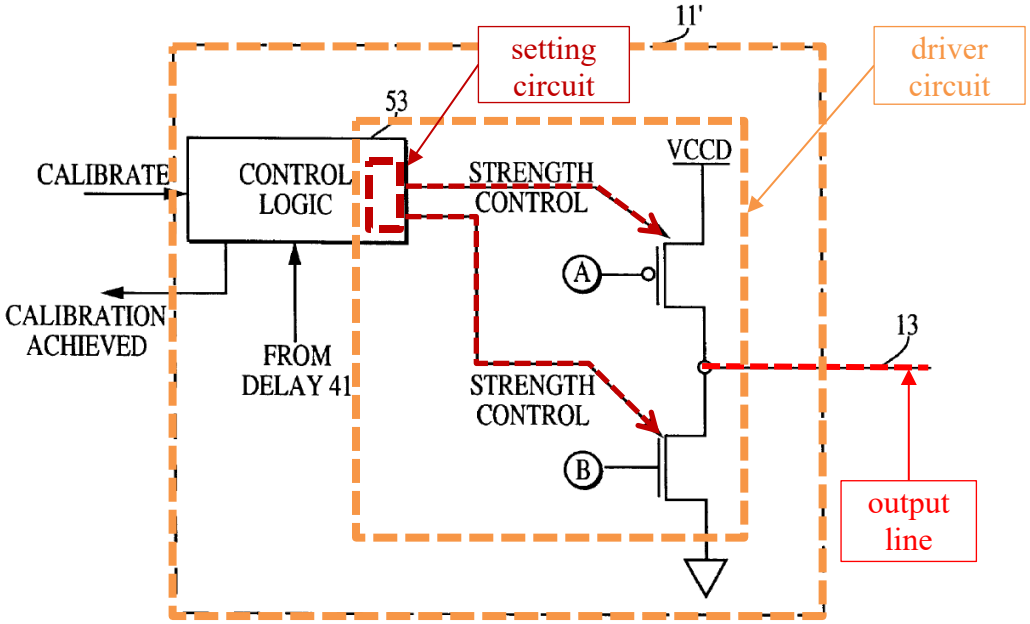
EX1007, 58-60; EX1003, ¶175; *supra* §X.C.2.b.

e. "wherein the driver strength is feedback-controlled based on a measured value provided by a measuring circuit." [14.4]

As explained for limitation [1.4], Lee teaches "*a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit*" to the extent the limitation is supported by the '369 Specification, and thus teaches this limitation for the same reasons. *Supra* §§X.A.1.e, X.C.2.a; *see* EX1005, 4:36-61, 5:39-58, 7:26-32, FIGS. 1, 2, 4-6; EX1003, ¶176.

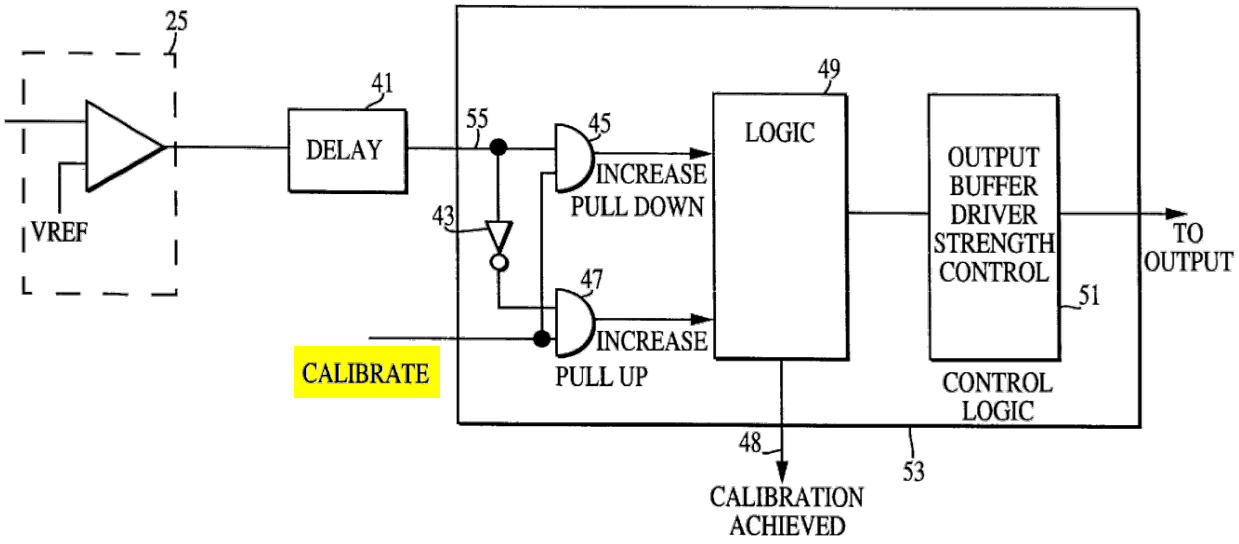
8. Claim 15: "The method of claim 14, wherein the driver strength of the driver circuit is controlled in a manner selected from continuously, periodically and in accordance with a setting signal."

As explained for claim 5, Lee teaches a "*setting circuit . . . for setting the driver strength of the driver circuit*." *Supra* §X.A.3. Specifically, Lee's circuit 51 ("*setting circuit*") outputs a strength control signal to the driver. *Id.*



EX1005, FIG. 4, 5:42-67; *see also* EX1005, FIGS. 5, 6, 6:54-63; EX1003, ¶177. The output of the setting circuit is "*a setting signal*," and thus Lee discloses controlling the driver strength of the driver circuit "*in accordance with a setting signal*." *See id.*

In addition, Lee teaches that the driver strength of the driver circuit is controlled in accordance with a CALIBRATE signal (an additional "*setting signal*"). EX1005, 4:39-41, 5:49-53; EX1003, ¶178. As shown below, the CALIBRATE signal is input to AND-gates 45 and 47.



EX1005, FIG. 2; EX1003, ¶178. If the CALIBRATE signal is de-asserted, the outputs of the gates are logic low, and if the CALIBRATE signal is asserted, the outputs of the gates can be logic low or high based on the comparator output via delay 41 and inverter 43. EX1005, 4:36-61, 5:48-54; EX1003, ¶178.

Further, a POSITA would have understood that Lee's CALIBRATE signal would have been periodically asserted "after an appropriate delay" to repeat the calibration process. EX1005, 4:66-67; EX1003, ¶179. Thus, the driver strength is also controlled "*periodically*." *Id.* Accordingly, Lee teaches and discloses this limitation alone or in combination with JESD79.

9. Claim 16: "The method of claim 14, further comprising: comparing at least one of the measured output line current and the measured output line potential respectively with at least one of a reference current value and a reference potential value; and

changing a control signal for setting the driver strength supplied to the driver circuit based upon a result from the comparison."

As explained for Ground 1, Lee teaches "*a comparator unit*" for comparing the measured output line current/potential with a reference current/potential value, "*a control unit*" for providing a control signal for setting a driver strength of the driver circuit, and "*an evaluation unit*" for changing the control signal based on the comparator unit's result. *Supra* §§X.A.1.d (limitation [1.3]), X.A.4-X.A.5 (claims 6-7); *see also supra* §§X.C.2.b, X.C.6 (Ground 3 for limitation [1.3] and claims 6-7). For the same reasons, Lee in combination with JESD79 teaches claim 16. EX1003, ¶180.

D. Ground 4: Claims 1-8, 14-16, and 18 are obvious over Lee, JESD79, and Garrett

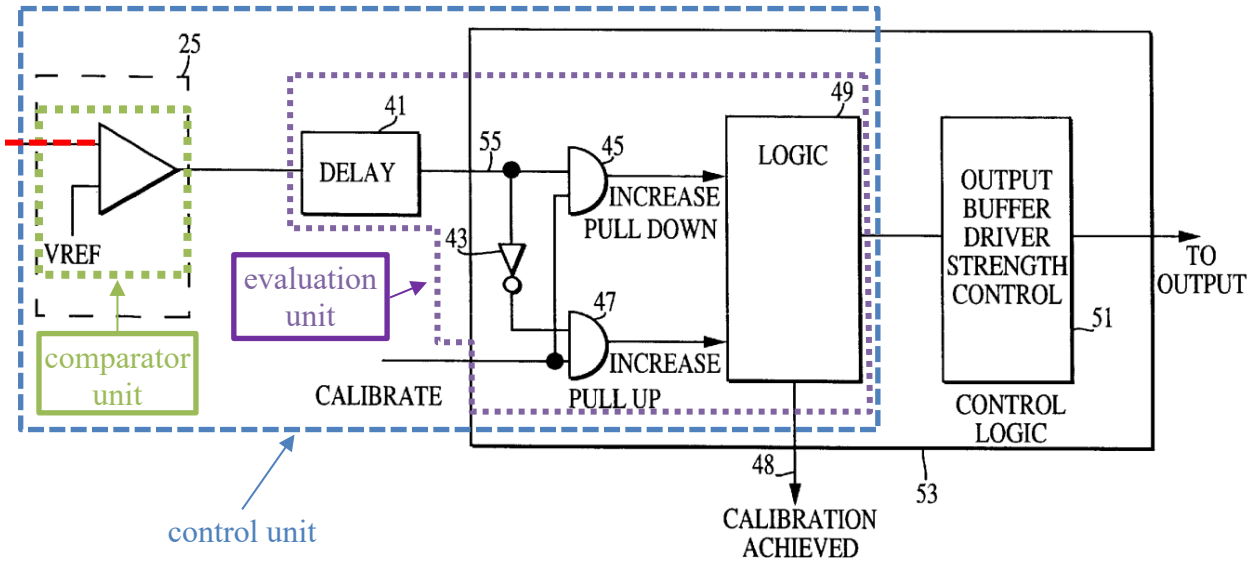
1. Motivation to Combine Lee and JESD79 with Garrett

Ground 4 combines Ground 3 (Lee and JESD79) with Garrett. As explained below, Garrett teaches logic for evaluating a comparison to a reference voltage by using a counter, and it would have been obvious to implement each of the pull-down and pull-up functionality in Lee's logic circuit 49 using the counter of Garrett. EX1003, ¶¶181-82.

A POSITA would have been motivated to combine Lee and JESD79 with Garrett, and had a reasonable expectation of success in doing so, because Lee and Garrett relate to drive current strength adjustment for a driver that uses feedback

control with a comparator. EX1003, ¶¶182-88; EX1005, FIG. 1, 3:13-32, 4:31-61; *supra* §IX.A; EX1008, Abstract, FIGS. 2, 11, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 10:6-41; *supra* §IX.D. Indeed, each of the references relate to DRAM. EX1005, 1:39-47, 2:11-20, 2:30-34, 7:38-47; EX1007, 1, 4-5; EX1008, 1, Abstract, 2:59-62, FIG. 2; EX1003, ¶183.

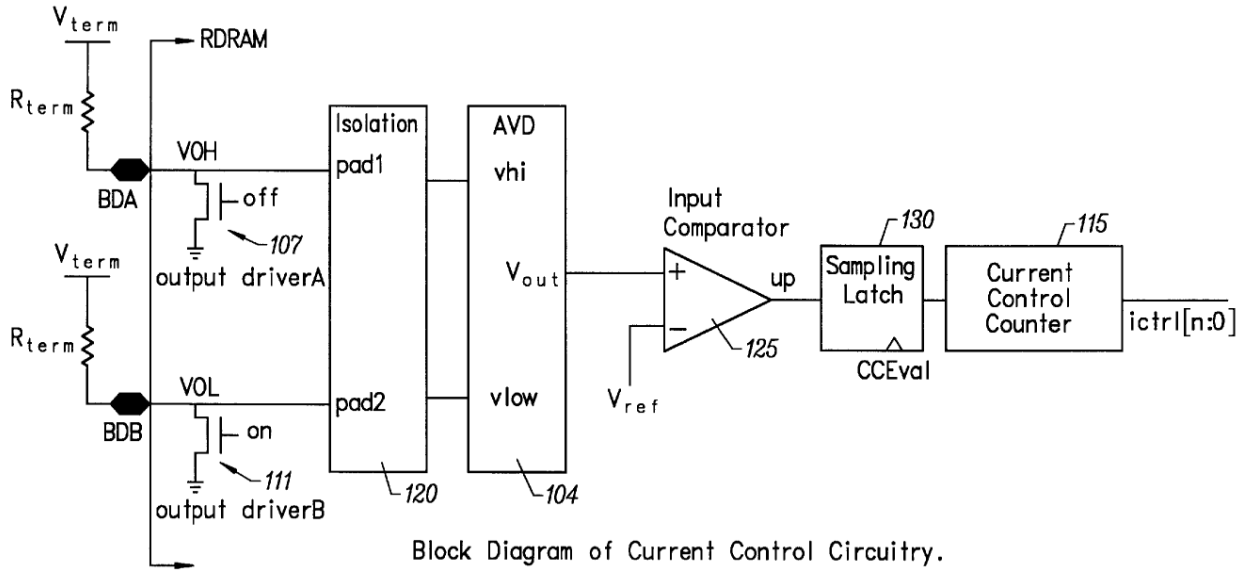
Lee discloses a control unit with a comparator unit that is connected to an evaluation unit in which the sampled output from the comparator is delayed and then input to AND-gates 45 and 47 that provide instructions to logic 49 for driver strength adjustments to the pull-up and pull-down paths.



EX1005, 4:67-5:5, 4:17-34, 5:29-58, FIGS. 1, 2 (shown above), 3, 6; EX1003, ¶184. Moreover, JESD79 provides I-V curves for calibration Lee's output driver. EX1007, 58-60; *supra* §X.C.1; EX1003, ¶184.

Although Lee describes algorithms for the logic block 49, it does not disclose a structure for performing the algorithms. *See* EX1005, 4:62-5:27. However, Garrett does disclose structure used to implement algorithms for driver strength feedback control, including a counter. EX1008, FIGS. 2, 11, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 10:6-41; EX1003, ¶185.

Similar to Lee's sampled comparator output, Garrett discloses a sampled comparator output from sampling latch 130, as shown below.



Block Diagram of Current Control Circuitry.

FIG. 2

EX1008, FIGS. 2, 10, 11, 3:14-29, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 9:29-10:5, 10:6-41; EX1003, ¶186; *supra* §IX.D. Garrett discloses that the sampling latch output (130) is input to a counter (115), which may be implemented as an up-down counter or a saturating binary search counter, to provide a control signal (ictrl[n:0]) for setting the drive strength. *Id.*

Thus, a POSITA would have been motivated to implement Lee's calibration logic 49 with counters to implement the algorithms disclosed in Lee for the pull-up and pull-down paths. EX1003, ¶187; EX1005, 4:62-5:27, FIG. 2. Specifically, Lee discloses iteratively adjusting the drive strength by increasing or decreasing the strengths of the pull-up or pull-down transistors. *See* EX1005, 4:9-10 (adjusting effective width of transistors), 4:11-20 (adjusting parallel transistors), 4:20-24 (adjusting gate fingers of transistors); 4:43-61 (example of increasing drive strength of weaker transistor), 4:62-5:18 (repeating calibration using newly set driver strength settings until calibration is achieved), FIG. 2; EX1003, ¶187. Lee also discloses that a binary search algorithm with coarse and fine adjustments can be used to perform calibration. EX1005, 5:20-27 (disclosing a binary search algorithm), 9:63-10:5 (claims 30-31) (coarse and fine adjustment), 12:28-36 (claims 68-69) (same); EX1003, ¶187. Similarly, Garrett teaches using a counter for simple up and down adjustments for drive strengths and more complex binary search algorithms. EX1008, 3:38-40, 7:7-23, 8:67-9:9, 9:18-24; EX1003, ¶187.

This is simple implementation of Lee's calibration logic in view of Garrett and the knowledge of a POSITA simply combines prior art elements (e.g., Lee's output buffer driver with feedback to adjust the drive strength in accordance with JESD79's I-V curves based on a sampled comparison with a reference and Garrett's counters coupled to a sampled comparison with a reference) according to

known methods (e.g., implementing logic to adjust the drive strength settings for the pull-up and pull-down paths using counters) to yield predictable results (e.g., a logic block with counters to perform the algorithms disclosed in Lee for the pull-up and pull-down paths). EX1003, ¶188. Additionally, the implementation applies a known technique (e.g., implementing logic for drive strength adjustment with counters) to a known device (e.g., Lee's logic block in combination with JESD79) that is ready for improvement to yield predictable results (e.g., structure for Lee's logic block that includes counters to perform the algorithms disclosed by Lee for the pull-up and pull-down paths). *Id.*

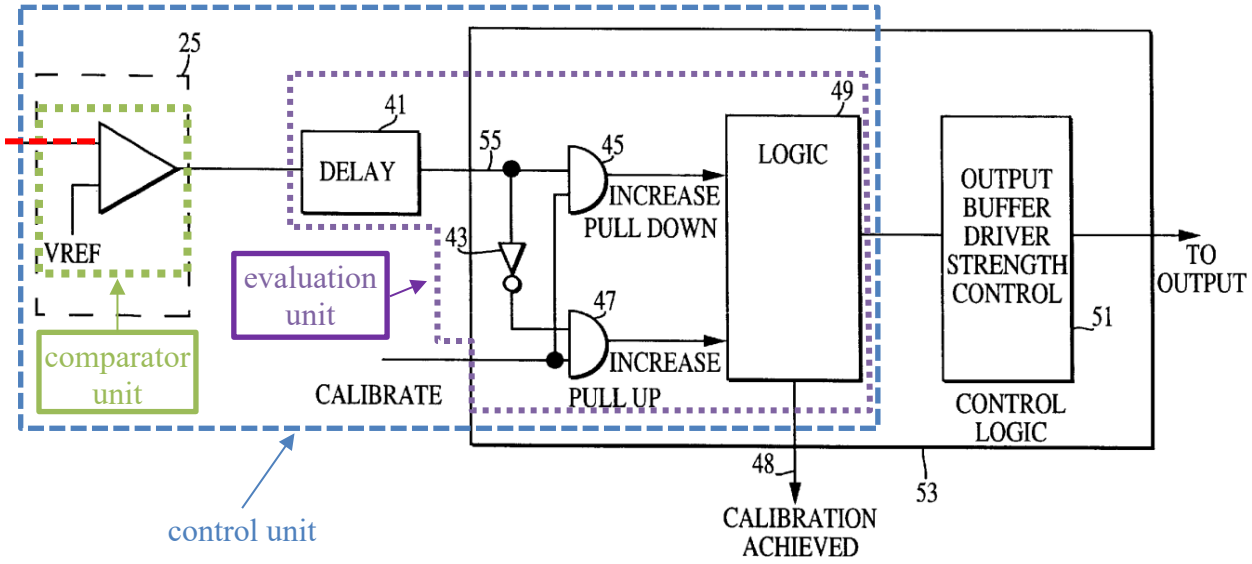
2. Claims 1-7 and 14-16

As explained above for Ground 3, Lee and JESD79 teach the limitations of claims 1-7 and 14-16 to the extent each is limiting and supported by the '369 Specification. *Supra* §§X.C.2-X.C.9 (Ground 3), X.A.1-X.A.5 (Ground 1); EX1003, ¶189.

Should any terms (e.g., "control unit" in claim 1, "comparator unit" in claim 6, "evaluation unit" in claim 7) be construed as means-plus-function limitations, the combination of Lee, JESD79, and Garrett teaches the corresponding structures and claimed functions as discussed below for claim 18. *Supra* §§X.D.4.c ("control means"), X.D.4.d ("comparator means"), X.D.4.e ("evaluation means").

3. Claim 8: "The output driver of claim 7, wherein the evaluation unit comprises a counter."

Lee and JESD79 in view of Garrett teaches claim 8. EX1003, ¶¶191-92. As discussed above for claim 7, Lee discloses an evaluation unit (annotated below in purple) in which the sampled output from the comparator is delayed, input to AND-gates 45 and 47 that provide instructions to logic 49 for driver strength adjustments.



EX1005, 4:67-5:5, 4:17-34, 5:29-58, FIGS. 1, 2 (shown above), 3, 6; EX1003, ¶191; *supra* §X.A.6.

In combination with Garrett, a POSITA would have been motivated to implement Lee's logic 49 using a counter, as disclosed in Garrett. Specifically, Garrett discloses a counter 115 coupled to a sampled comparator output from sampling latch 130, as shown below.

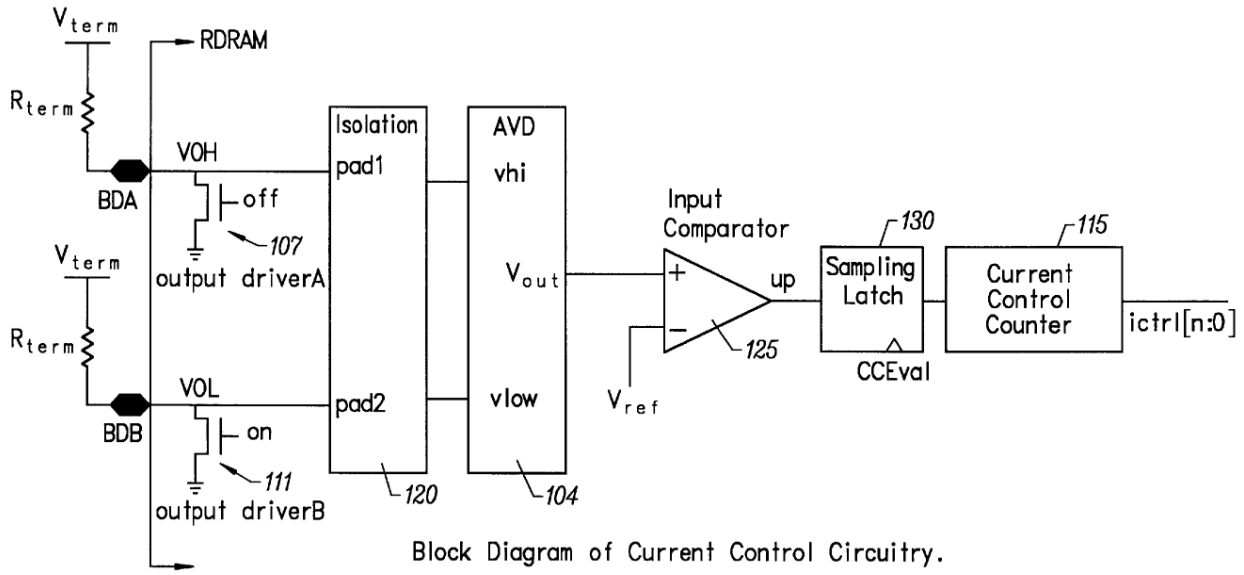


FIG. 2

EX1008, FIGS. 2, 11, 3:38-40, 5:26-6:24, 7:7-23, 8:67-9:9, 9:18-24, 10:6-41; EX1003, ¶192; *supra* §IX.D. Garrett discloses that the counter may be implemented as an up-down counter or a saturating binary search counter. *Id.* A POSITA would have understood that the counter in Garrett would have been used to implement the calibration algorithm in Lee for each of the pull-up and pull-down paths, in which the algorithm can be a simple iterative increase or decrease in drive strength (similar to simple up-down control) or a more complex binary search algorithm. EX1005, 4:9-24, 4:43-5:18, 5:20-27; EX1003, ¶192. Accordingly, Lee's logic 49 (in the "*evaluation unit*") would have been implemented in the combination with Garrett with "*a counter*." EX1003, ¶192.

4. Claim 18

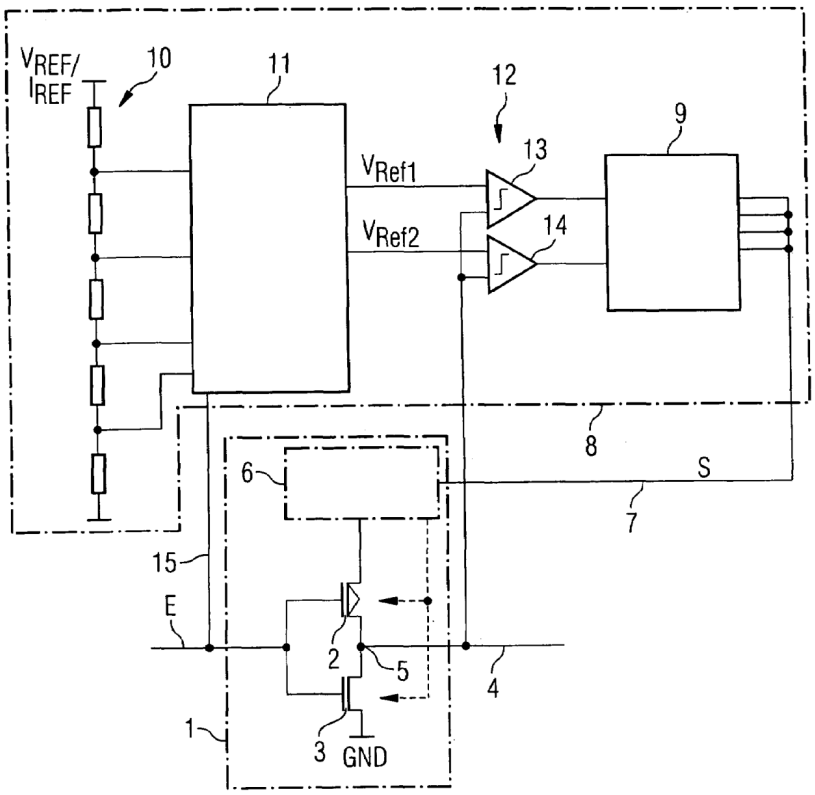
a. "An output driver for an integrated circuit, comprising:" [18.P]

For the reasons provided above for claim [1.P], Lee alone or in combination with JESD79 and with JESD79 and Garrett discloses this limitation. *Supra* §§X.A.1.a, X.C.2.a; EX1003, ¶193.

b. "a driver means for driving an input signal of the output driver onto an output line; and" [18.1]

As discussed above, "a driver means" is properly construed as transistors 2 and 3 in Figure 1 of the '369 Patent that correspond to the claimed function. *Supra* §VIII.A; EX1001, FIG. 1 (below).

FIG 1



As discussed for claim limitations [1.1] and [14.P] that recite the same claimed function, Lee teaches two transistors to drive an input signal onto a bus (13) and thus the combination teaches both the claimed function and corresponding structure. *Supra* §§X.A.1.b, X.C.2.a, X.C.7.a, X.D.2; *see, e.g.*, EX1005, FIGS. 1, 4 (below); EX1003, ¶¶194-95.

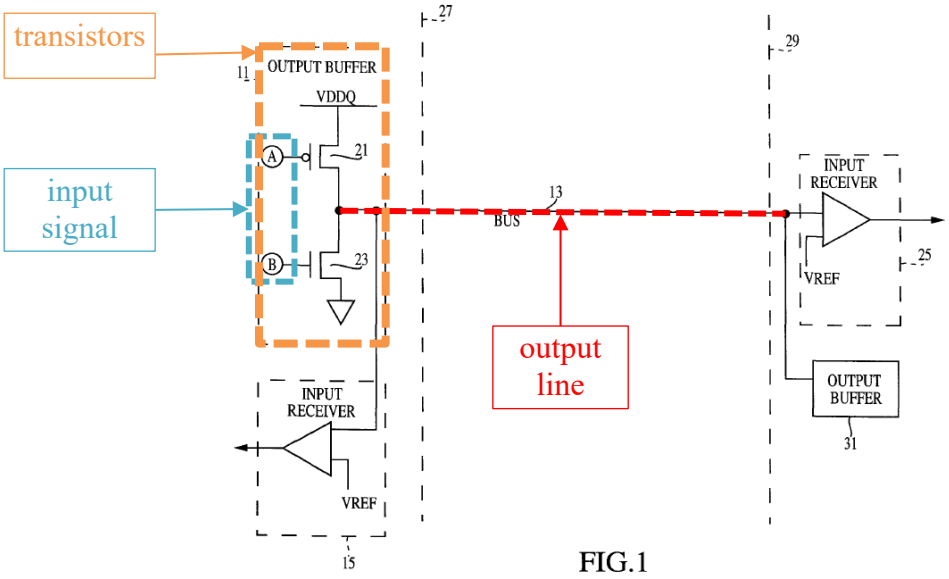


FIG.1

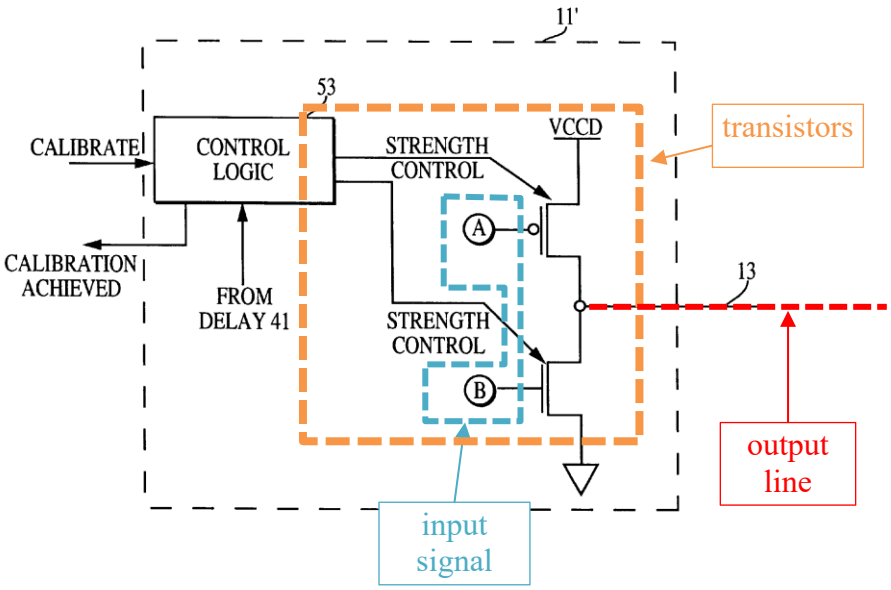
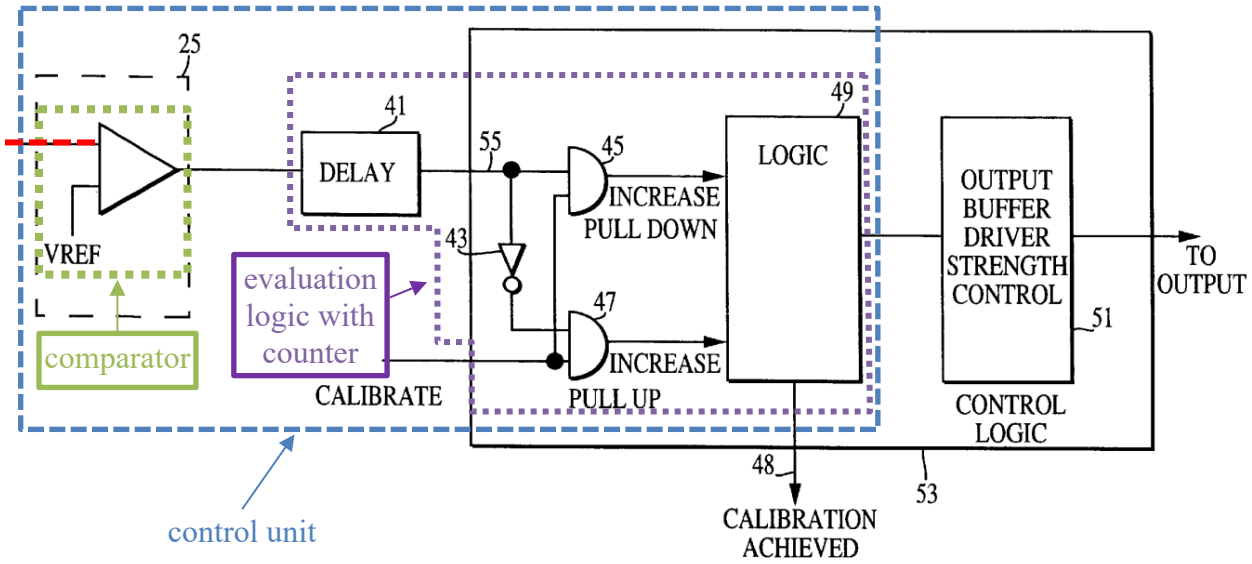


FIG. 4

c. "a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range of a specification-prescribed potential range and a specification-prescribed current range, the control means comprising:" [18.2]

As discussed above, "a control means" is properly construed as comprising the combined structure of the comparator means (a comparator) and evaluation means (a counter), which are discussed below for claim limitations [18.3] and [18.4]. *Supra* §VIII.D. As discussed for claim limitation [1.3] and claim 8, Lee and Garrett teach a "control unit," with a comparator and a counter, for nearly the same claimed function ("*for providing a control signal for setting a driver strength of*

the driver") to provide a similar intended result ("*... a desired power range ...*")[11]. *Supra* §§X.A.1.d, X.C.2.b, X.D.2, X.D.3 (counter of claim 8); EX1003, ¶¶196-97; *see, e.g.*, EX1005, FIG. 2 (below).



Further, the same intended result ("*... a lower power range ...*") is very similar to that in claim limitation [14.3] ("*... a lower power range ...*"), which is taught by Lee in view of JESD79 and Garrett. *Supra* §§X.C.7.d, X.D.2; EX1003, ¶198. Thus, the combination teaches both the claimed function and corresponding structure. EX1003, ¶198.

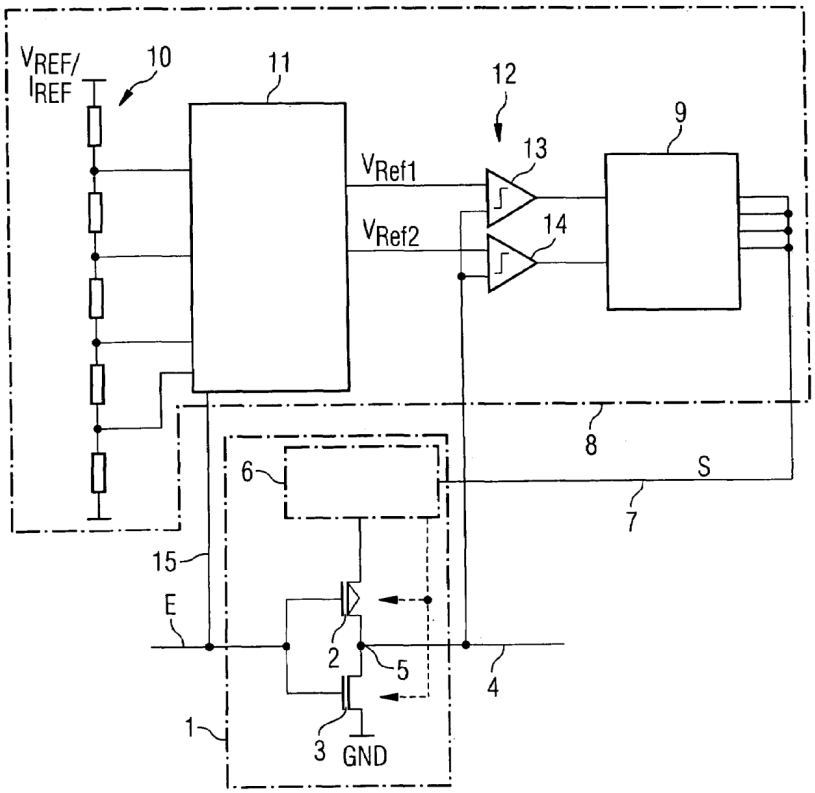
d. "a comparator means for comparing at least one of the output line current and the output line potential

[11] For these reasons, the combination also teaches the "*control unit*" of claim 1 if it is construed as a means-plus-function limitation. EX1003, ¶197.

respectively with at least one of a reference current value and a reference potential value; and" [18.3]

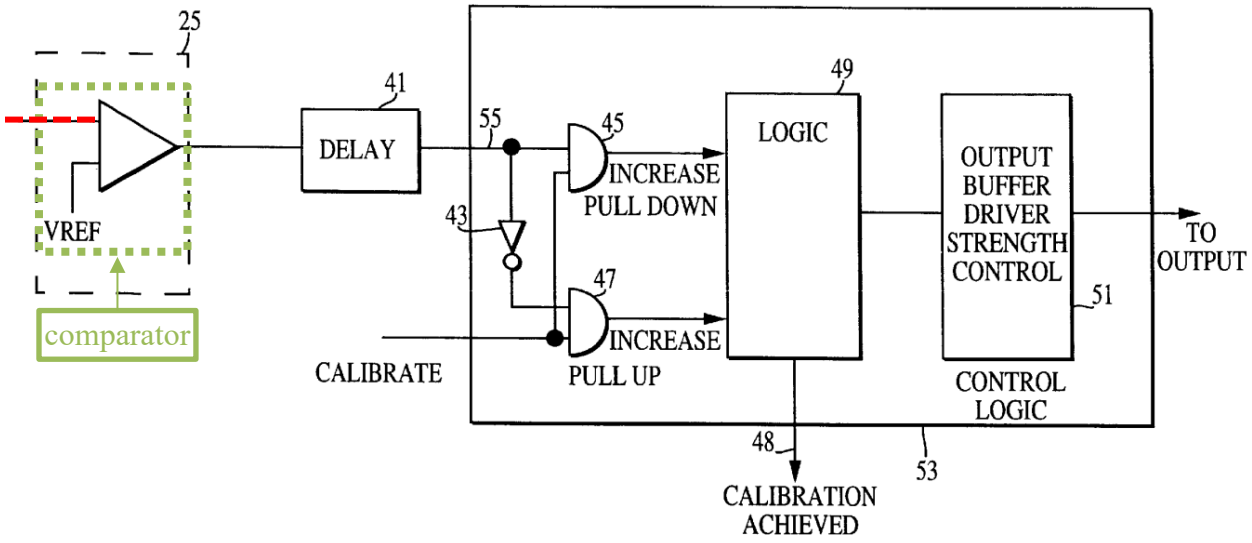
As discussed above, "a comparator means" is properly construed as one or more comparators (e.g., 13 or 14 in Figure 1 of the '369 Patent) that corresponds to the claimed function. *Supra* §VIII.B; EX1001, FIG. 1 (below).

FIG 1



As discussed for claim 6, which recites a "comparator unit" and the same claimed function, Lee teaches a comparator that compares the measured output line potential/current to a reference potential/current, and thus the combination teaches

both the claimed function and corresponding structure[12]. *Supra* §X.A.4; EX1003, ¶¶199-200; *see, e.g.*, EX1005, FIG. 2 (below).



e. "an evaluation means for changing the control signal based upon a comparison result from the comparator means." [18.4]

As discussed above, "an evaluation means" is properly construed as a counter that corresponds to the claimed function. *Supra* §VIII.C; EX1001 at 5:25-30, 5:42-47, 7:35-36.

As discussed for claim 7, which recites the same claimed function, Lee teaches an evaluation unit that includes Lee's calibration logic 49. *Supra* §X.A.5; EX1003, ¶¶202-03; *see, e.g.*, EX1005, FIG. 2. Further, as discussed for claim 8,

[12] For this reason, the combination also teaches the "comparator unit" of claim 6 if it is construed as a means-plus-function limitation. EX1003, ¶201.

which recites "*a counter*" in the evaluation unit, a POSITA would have understood that the counter disclosed in Garrett would have been used in implementing Lee's calibration logic 49 for each of the pull-up and pull-down paths. *Supra* §X.D.3; EX1003, ¶203; *see, e.g.*, EX1008, FIG. 2. Thus, the combination teaches the claimed function and the corresponding structure.[13] EX1003, ¶203.

XI. CONCLUSION

Accordingly, Petitioner requests *inter partes* review of claims 1-8, 14-16, and 18 pursuant to Grounds 1-4 set forth above.

[13] For this reason, the combination also teaches the "evaluation unit" of claim 7 if it is construed as a means-plus-function limitation. EX1003, ¶204.

Date: February 6, 2023

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,907 words, which is less than the 14,000 allowed under 37 C.F.R. § 42.24(a)(1)(i).

/Brian W. Oaks/
Brian W. Oaks

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(a), the undersigned certifies that on February 6, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, cost prepaid, to the Patent Owner by serving the correspondence address of record and another address known to Petitioner as likely to effect service, as follows:

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Additionally, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were served via e-mail on:

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Petitioner knows this to be an additional address likely to effect service.

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Lead Counsel for Petitioner