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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

Case IPR2023-00514

U.S. Patent 7,145,369

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Polaris Innovations Limited (“Patent Owner”) submits this Preliminary Response to Xilinx, Inc.’s (“Petitioner”) Petition for *Inter Partes* Review (“Petition,” Paper 2), challenging Claims 1-8, 14-16, and 18 of U.S. Patent 7,145,369 (the “’369 Patent”) (Ex. 1001).

The ’369 Patent is directed to an output driver for an integrated circuit. The claimed inventions address the problem of setting the output voltage in a particular power range in light of process deviations, temperature and voltage fluctuations, and different loads. The independent claims solve this problem by using feedback control to set the output potential or current of the driver, specifically requiring:

Claim 1:

. . . a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range . . .

Claim 14:

. . . controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range . . .

Claim 18:

. . . a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range . . .

See EX1001, Cls. 1, 14, and 18. These claim limitations, in combination with the other requirements of the independent claims, allow a driver circuit to set its output in a particular range.

The Petition's primary reference Lee is directed to a different problem. Lee is concerned with mismatch between the drive strength of the transistors of a driver circuit that can cause timing problems when its transistors switch to different logic states. To solve this problem, Lee discloses a calibration circuit and method that adjusts the drive strength of the transistors so that the output for logic high and the output for logic low are symmetric about a midpoint by simultaneously turning on the pull-up and pull-down transistors of the driver circuit during the adjustment. Lee does not, however, disclose any circuitry or method for setting the output voltage or current of the drive circuit in a particular range. None of the other references cited in the Petition cure these deficiencies in the primary reference Lee.

Because the Petition fails to show at least one element of each of the challenged independent claim in the asserted references or combinations, the Petitioner cannot show that any of the challenged claims are reasonably likely to be found unpatentable. The Board should not institute *inter partes* review of the '369 Patent for at least this reason as described more fully herein.

II. THE '369 PATENT AND THE CHALLENGED CLAIMS

A. Overview of the '369 Patent

The '369 patent “invention relates to an output driver for an integrated circuit having a driver circuit for driving an input signal onto an output line.” Ex. 1001 at 1:14-19. “Usually, the specifications for integrated circuits, in particular for SDRAM and DDR memory circuits, provide a relatively large current intensity range or potential range for the output drivers.” *Id.* at 1:39-42. “However, the exact potential value or current value with which the signal is driven with the aid of the output driver cannot be established from the outset since it is necessary to take account of process deviations, temperature fluctuations and voltage fluctuations.” *Id.* at 1:52-55. “Moreover, different loads are possible at the outputs of the integrated circuit, so that this may result in different potential values or current values depending on the connected components or the switching states thereof.” *Id.* at 1:59-62.

In light of these issues, the '369 Patent invention seeks “to provide an integrated circuit and a method for controlling an output driver which are able to reduce the power consumption of the integrated circuit and to ensure that the corresponding potential value or current value at the output of the output driver is within the specification.” *Id.* at 1:66-2:4. “[O]ne aspect of the invention provides an output driver for an integrated circuit which makes it possible to set the current value

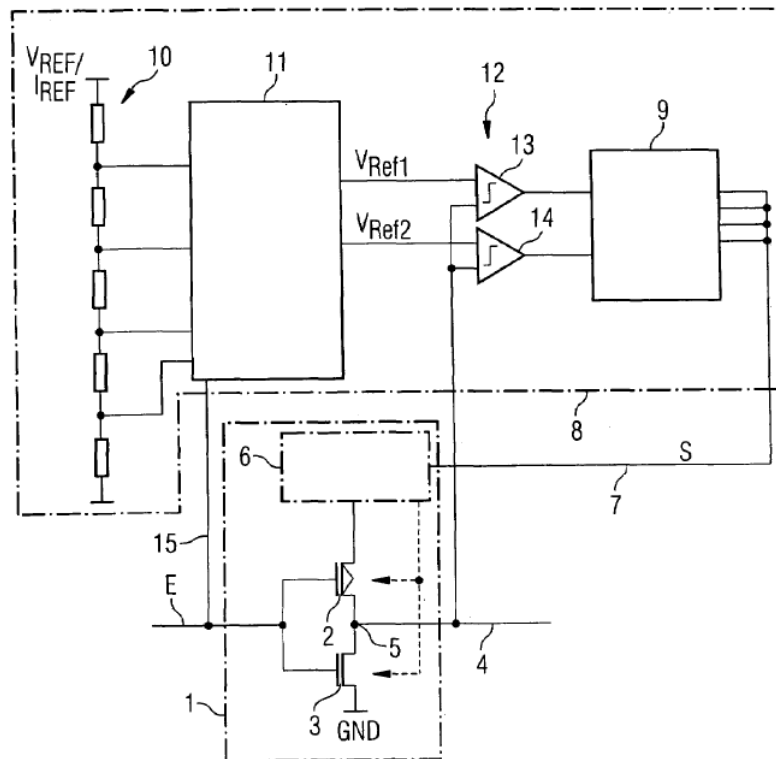
and/or the potential value on the output line in a lower power range, i.e., to operate the integrated circuit at an operating point at which the power consumption of the output driver can be reduced, but without permitting a current value or potential value outside the specification-conforming limits.” *Id.* at 2:24-31.

The ’369 Patent teaches “a control circuit which influences the driver strength of the driver circuit” and “[t]he driver strength of the driver circuit may be set by the control circuit in such a way that the current intensity and/or the potential on the output line, . . . lies in a lower power range of the current intensity range and/or potential range prescribed by the specification, i.e., the power consumption of the output driver is reduced within the permissible range.” *Id.* at 2:50-58. The control circuit sets the strength of the driver circuit in a particular current intensity and/or potential range “to take into account the process fluctuations during the production of the integrated circuit, the respective operating temperature, the potential fluctuations, e.g., of the supply voltages, and the load connected to the output driver.” *Id.* at 2:58-62.

The ’369 Patent describes an embodiment of the invention in Figure 1, including how it uses feedback control to set the potential and/or current range of the driver output. *See id.* at 4:4-65. As shown in Figure 1, the exemplary output driver includes a driver circuit 1 with p-channel transistor 2 and an n-channel

transistor 3 which drive the input signal E (in inverted fashion) to the output 5 onto output line 4. *Id.* at 4:4-11.

FIG 1



EX1001, Figure 1.

The output line 4 connects to a control unit 8 that compares the output (i.e., output potential or current intensity) to reference values. *Id.* at 4:32-40; *see also id.* at 5:65-6:8. This comparison is used to generate a control signal S that is provided to the setting circuit 6 that sets the driver strength of the transistors 2 and 3. *Id.* at 4:18-31. The setting circuit 6 sets the driver strength of the transistors so that “the potential value on the output line 4 can be regulated to a driver strength which enables the

potential value on the output line 4 to be put into a potential window defined by” the reference values. *Id.* at 4:60-65.

As illustrated through the exemplary embodiment of Figure 1, the ’369 Patent teaches an output driver that sets its output potential and/or current based on a comparison of the output to reference values. The ’369 Patent also teaches additional details, e.g. regarding selection of the reference values and generation of the control signal, in order to allow the output drive to set its output potential and/or current to reduce power consumption. *Id.* at 4:66-6:54.

B. Challenged Claims

The Petition challenges claims 1-8, 14-16, and 18 of the ’369 Patent. Claims 1, 14, and 18 are independent claims. Claims 2-8 depend from claim 1, and claims 15 and 16 depend from claim 14. The Petition provides a listing of all the challenged claims at pages v-viii.

The independent claims are reproduced below with emphasis on the particular limitations that are at issue in this Preliminary Response:

Claim 1 recites:

1. An output driver for an integrated circuit, comprising:
 - a driver circuit for driving an input signal of the output driver onto an output line;
 - a measuring circuit for measuring at least one of an output line current and an output line potential; and

a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range, wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.

Claim 14 recites:

14. A method for driving an output driver for an integrated circuit having a driver circuit driving an input signal onto an output line, comprising:

measuring at least one of an output line current and an output line potential; and

controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range, respectively, wherein the driver strength is set such that the potential and the current intensity lie in a lower power range of the specification-prescribed current range and the specification-prescribed potential range, and wherein the driver strength is feedback-controlled based on a measured value provided by a measuring circuit.

Claim 18 recites:

18. An output driver for an integrated circuit, comprising:

a driver means for driving an input signal of the output driver onto an output line; and

a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range of a specification-prescribed potential range and a specification-prescribed current range, the control means comprising:

a comparator means for comparing at least one of the output line current and the output line potential respectively with at least one of a reference current value and a reference potential value; and

an evaluation means for changing the control signal based upon a comparison result from the comparator means.

The emphasized limitations in each independent claim require that the claimed inventions, in accordance with the other requirements of each claim, provide a control signal that sets the driver to provide output line potential or current in a particular range or, for the method claim, sets the driver to a potential or current in a particular range. As addressed further herein, none of the Petitioner's references disclose these limitations nor does the Petition articulate a motivation to modify any of the references to meet these limitations. Because the remaining challenged claims all depend from these independent claims, should the Board accept Patent Owner's arguments that trial should not be instituted on these claims, it necessarily follows that trial should not be instituted on the dependent claims.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art, but it reserves the right to do so in the event that trial is instituted.

IV. CLAIM CONSTRUCTION

Patent Owner submits that the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012) (“The Board ... may institute a trial where the petitioner establishes that the standards for instituting the requested trial are met”).

A. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established; the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

Additionally, it is improper to use the challenged claim as a roadmap to piece together disparate disclosure using hindsight bias. *See InTouch Techs., Inc. v. VGo Comm'ns., Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (reversing obviousness where “[i]t appears that [the expert] relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”).

2. A petition must address the Graham factors.

Obviousness is resolved on a number of factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” *See Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there

must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

VI. SUMMARY OF THE PRIOR ART REFERENCES

A. Overview of Primary Reference: Lee

Petitioner’s rely on U.S. Patent No. 6,549,036 to Lee as the primary reference in each of the four grounds it asserts. *See, e.g.*, Petition at 3. Lee “relates to an output buffer driver calibration circuit and calibration method for reducing timing uncertainty in high speed signaling systems.” EX1005 at 1:6-8.

In the Background of the Invention, Lee explains that “[a] mismatch of the pull-up transistor characteristic with the pull-down transistor characteristic [in an output buffer driver] will create a different timing relationship with signals

transitioning to a logic one state versus signals transitioning to a logic zero state.”

Id. at 2:4-8. “This results in a timing uncertainty in the system, which will limit the maximum system operational data rate,” which is the problem Lee seeks to address.

Id. at 2:8-10.

Lee discloses “a simple output driver calibration circuit and calibration method which reduces timing uncertainty.” *Id.* at 2:30-33. “The calibration circuit and associated calibration method simultaneously turns on the pull-up and pull-down transistor in an output buffer driver” and “[t]he resulting output voltage is compared to a reference voltage that is set for the appropriate ratio of pull-up to pull-down drive strength.” *Id.* at 2:34-39. The drive strength of the pull-up or pull-down transistor are then adjusted to match this ratio of pull-up to pull-down drive strength. *Id.* at 2:39-44.

Specifically, Lee discloses in Figure 1 an output driver 11 and input receiver 15:

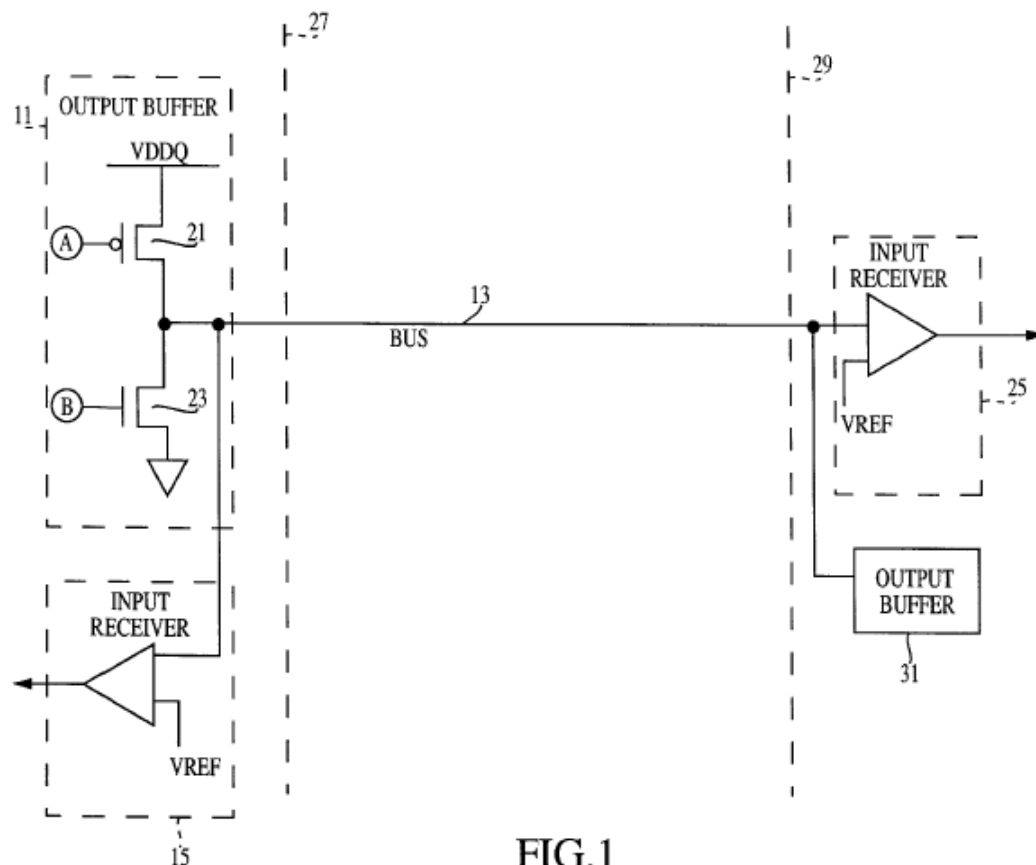


FIG.1

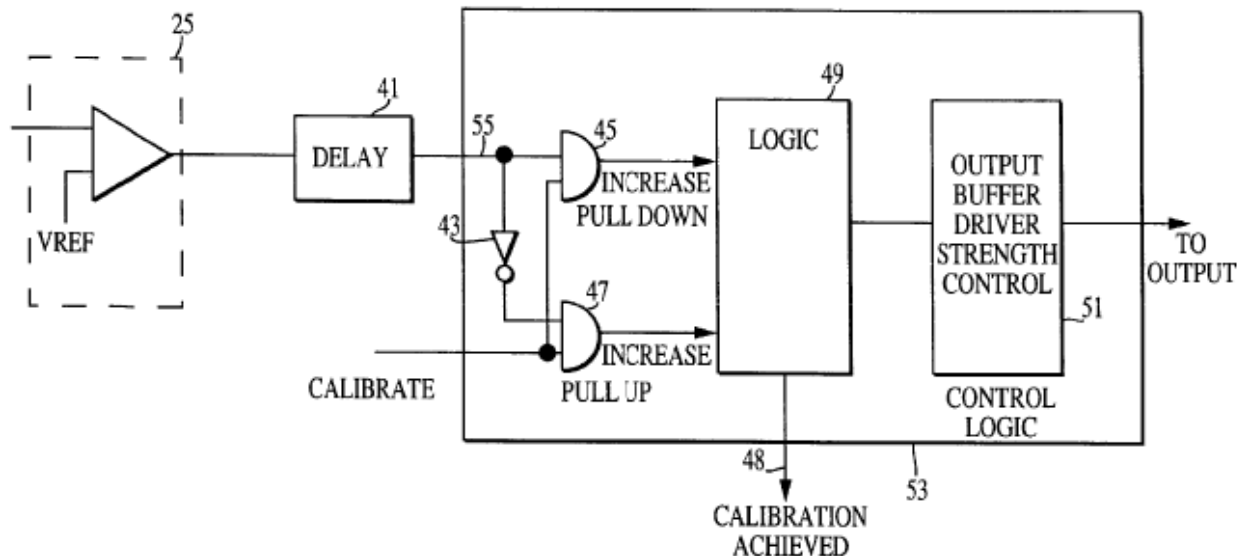
EX1005, Figure 1

Id. at 3:13-32. The output buffer driver 11 includes transistors 21 and 23. *Id.* at 3:33-45. Transistor 21 provides the current to pull the bus 13 voltage high and is referred to as a pull-up transistor. *Id.* at 3:33-35. Transistor 23 provides the current to pull the bus 13 voltage low and is referred to as a pull-down transistor. *Id.* at 3:38-39.

During normal operation, the inputs A and B to the transistors 21 and 23 are both asserted low to switch the bus to logic 1, and both inputs are asserted high for a logic 0. *Id.* at 3:47-53. During the calibration process described in Lee, however, input A is asserted low while input B is asserted high so that both transistors are on

at the same time. *Id.* 3:53-56. The purpose of switching both transistors on during calibration is to determine whether or not these transistors are well-matched. *Id.* at 3:56-60. If the output voltage on the bus 13 with both transistors 21 and 23 in the on state is equal to $VDDQ/2$, then they are well-matched, and Lee refers to this voltage as $VREF$. *Id.* at 3:56-58.

Lee describes the calibration process in more detail with respect to Figure 2. *Id.* at 4:6-61.



EX1005, Figure 2

The input receiver (reference 25 in Figure 2 or reference 15 from Figure 1) compares the output from bus 13 to $VREF$ “to determine which transistor 21, 23 has the greater drive strength.” *Id.* at 4:6-9; *see also id.* at 4:46-55. Lee explains that the transistor with the greater drive strength can be reduced or the transistor

with the weaker drive strength can be increased. *Id.* at 4:9-10; 4:26-30; 4:49-55.

Lee also discloses that the drive strength of either transistor may first be set to a fixed value and then calibration is performed on the other transistor. *Id.* at 6:1-7.

Regardless of which method is followed, “the calibration process is complete” when “the relative drive strengths of the pull-up and pull-down transistors are matched,” and “normal bus operations can begin.” *Id.* at 5:8-12.

The calibration scheme of Lee adjusts the drive strengths of the pull-up and pull-down transistors such that “VOH [logic output high voltage] and VOL [logic output low voltage] levels [are] symmetric about a midpoint voltage, VREF.” *Id.* at 3:8-10. Notably, for purposes of this Preliminary Response, Lee does not disclose setting the drive strength of these transistors to provide the output potential or current within any particular range, during calibration or normal operation. Lee only describes a calibration circuit and method to match the strength of the pull-up and pull-down transistors to address the timing uncertainty issues to which it is directed.

B. Overview of Secondary References:

Petitioner relies on four additional prior art references in addition to its primary reference Lee. A brief description of each follows.

1. Thomann

U.S. Patent No. 6,330,194 to Thomann was assigned to the same company as the Lee reference and includes Mr. Lee as a co-inventor. The Field of the Invention and Background of the Invention sections in Thomann are identical to the same sections in Lee (correcting a couple of typographical errors). *Compare* EX1006 at 1:4-2:25 *with* EX1005 at 1:5-2:27. Accordingly, Thomann likewise “relates to an output buffer driver calibration circuit and calibration method for reducing timing uncertainty in high speed signaling systems” and describes the problems it is addressing as reducing timing uncertainty caused by mismatched pull-up and pull-down transistors. *See* EX1006 at 1:5-7; 1:10-24.

Like the calibration circuit and method in Lee, Thomann discloses turning on both pull-up and pull-down transistors in a buffer driver circuit, comparing the drive signal to a reference voltage, and increasing or decreasing the drive strength of either transistor until the output of the buffer driver approaches the reference voltage. *Id.* at 4:27-63; Figs. 1-2. Like Lee, the disclosed process uses the comparison to match the strength of the transistors such that V_{OH} (logic output high) and V_{OL} (logic output low) are equidistant from V_{REF}, as shown graphically in Figure 3:

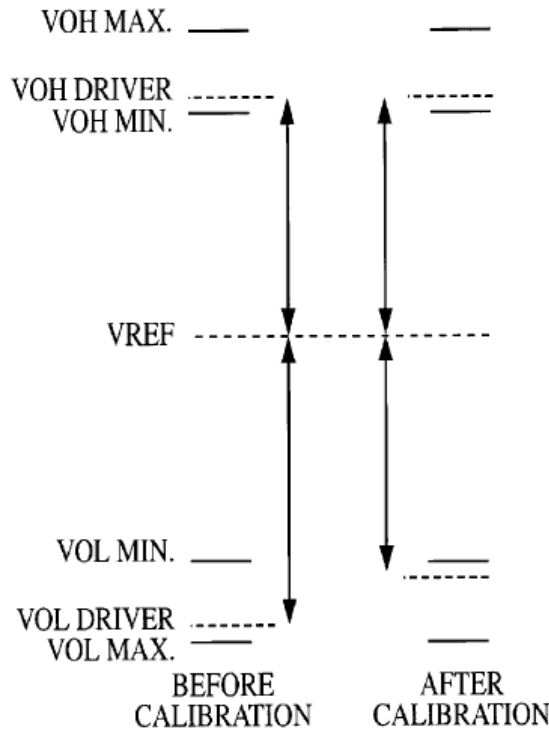


FIG. 3

EX1006, Figure 3

Id. at 5:37-65. Like Lee, Thomann does not disclose setting the drive strength of these transistors provide the output potential (or current) in any particular range in response to this calibration circuitry or otherwise. Thomann simply discloses a circuit and method that, whatever output range is set, matches the relative drive strength of the pull-up and pull-down transistors.

2. JESD79

Petitioner relies on JEDEC's Double Data Rate (DDR) SDRAM Specification, JESD79, Release 1 for providing "user-controlled drive strength settings" and providing Voltage-Current curves for "Pulldown" and "Pull Up"

Characteristics. Petition at 21-23; EX1007 at 16, 59-60. JESD79 does not disclose any circuit or method for achieving these characteristics, nor does Petitioner allege that it does.

3. Garrett

Petitioner relies on U.S. Patent No. 6,094,075 to Garrett for allegedly “disclos[ing] structure used to implement algorithms for driver strength feedback control, including a counter” to address terms that might be construed as means-plus-function limitations. Petition at 95 and 97. Garrett does not address the deficiencies of Lee presented in this Preliminary Response, nor does Petitioner allege that it does.

VII. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS

To justify the institution of an *inter partes* review, a petitioner must establish that there is a “reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Petitioner has not met its burden of establishing a reasonable likelihood of success at least because the Petition fails to show that each limitation of the challenged claims is disclosed or taught by the asserted prior art references of each ground. Consequently, the Board should deny the Petition and decline to institute the *inter partes* review.

A. The Primary Reference Lee Does Not Teach or Suggest At Least One Limitation of Each Independent Claim, And None of the Asserted Combinations Resolve This Flaw.

The '369 Patent claims an output driver and method for driving the same that uses feedback control to set the output potential or current in a particular range. This is reflected as a requirement of each independent claim, specifically:

Claim 1 requires:

. . . a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range . . .

Claim 14 requires:

. . . controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range . . .

Claim 18 requires:

. . . a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range . . .

See EX1001, Cls. 1, 14, and 18. The independent claims including these limitations address the problem identified by the '369 Patent that the exact potential value or current value of a driver circuit cannot be set at the outset because of process deviations, temperature and voltage fluctuations, and different loads. EX1001 at 1:52-55; 1:59-62. The solution of the independent claims is to provide a feedback control mechanism whereby the driver circuit can set its output in a particular range.

The Petition's primary reference Lee is directed to a different problem. Lee is concerned with mismatch between the drive strength of the transistors of a driver circuit that can cause timing problems when the transistors switch to different logic states. EX1005 at 1:6-8; 2:4-10. To solve this problem, Lee discloses a calibration circuit and method that adjusts the drive strength of the transistors so that the output for logic high and the output for logic low are symmetric about a midpoint voltage. *Id.* at 3:8-10.

Lee does not disclose any circuitry or method for setting the output voltage or current of the drive circuit in a particular range. Lee instead discloses a calibration process that, however the drive circuit output is set, can be used to equalize the drive strength of the pull-up and pull-down transistors such that they are matched in order to address the timing issues with which it is concerned. To be sure, Lee discloses that one or the other of the transistors may "first be set to a fixed value and then calibration performed on the other transistor," but however it is initially set is not described. *Id.* at 6:1-4. There is no teaching or suggestion in Lee, and Petitioner does not allege, that this initial fixed value is established through any of the circuitry or processes that Petitioner relies on for the other requirements of the claim. That is, nowhere in Lee does the reference teach or suggest measuring the output and using the claimed feedback control circuitry or steps in order to set the output voltage or current in a particular range.

The Petition’s failure to demonstrate that Lee teaches or suggests at least these limitations of each independent claim undermines its obviousness claims for all of the challenged claims. The secondary references cited in the Petition fail to cure the deficiencies of Lee for these limitations. Petitioner’s arguments on these limitations are discussed in more detail for each Ground below.

1. Ground 1: The Petition Fails to Demonstrate Obviousness Over Lee for Claim 1 or its dependents.

The Petition fails to demonstrate that Lee teaches or suggests:

. . . a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range . . .

Ex. 1001, Cl. 1. Other than conclusory assertions that the limitation is met (e.g., Petition at 36 and 42), the Petition never actually asserts that driver strength is set “to provide” an output line potential or current in a desired range. *See* Petition at 33-42.

Instead, the Petition bootstraps its interpretation of Lee to conclude that whatever potential is supplied defines the desired power range. The Petition argues that “Lee teaches a desired potential range because its calibration scheme ensures that the output voltage swings across a range between a high voltage V_{OH} and a low voltage V_{OL} . . . that are symmetric about a mid-voltage V_{REF} after calibration.” *Id.* at 40-41. But, this disclosure, and the circuitry in Lee that produces this result, does not set the strength of the driver circuit “to provide” any particular output

potential or range. Rather, Lee discloses that the power range is set to be symmetric around a mid-voltage VREF without regard to whether the potential is within any particular power range.

Lee fails to disclose setting the potential in a particular power range because that is not the problem with which it is concerned. Lee's calibration circuit only addresses the issue identified in Lee that the pull-up and pull-down transistors need to be matched to reduce timing uncertainty. *Id.* at 1:6-8; 2:4-10. The Petition does not identify any reasoning or explanation for how or why one of ordinary skill would adapt or modify the circuitry in Lee to set the output potential (or current) in a particular power range. The Petition's conclusory assertions to the contrary lack supported reasoning and merely use the '369 Patent as a roadmap for interpreting Lee as providing a different solution than what it actually describes.

2. Ground 2: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Thomann for Claim 1.

Similar to the arguments for Ground 1, the Petition fails to demonstrate that Lee and Thomann teach or suggest:

. . . a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range . . .

Ex. 1001, Cl. 1. As noted supra in Section VI.B.1, Thomann includes Inventor Lee as co-inventor and was assigned to the same company. Moreover, Thomann includes the same Background and thus describes the same problem to be solved as Lee, i.e.

the matching of transistor strength to address timing issues. EX1006 at 1:5-7; 1:10-24.

The Petition relies on Thomann for its addition of Figure 3 showing graphically the result of Lee/Thomann's calibration scheme which match the transistor strength in order to render "the VOH and VOL levels to be symmetric about a midpoint voltage, VREF." Petition at 57 (citing EX1006, 3:33-36).

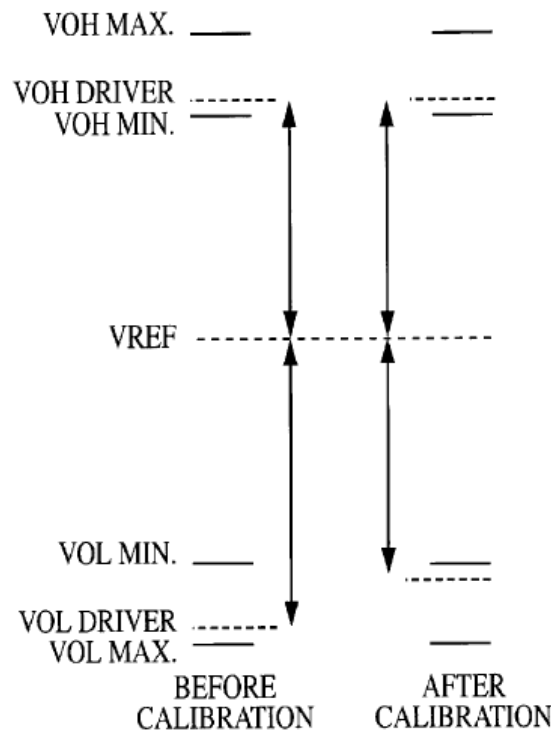


FIG. 3

EX1006, Figure 3

The Petition's arguments are otherwise the same as for Lee and rely on the same hindsight/bootstrapped argument that the calibrated voltages symmetric about

a midpoint are thereby “set” by Thomann in a desired power range. Petition at 57. But, neither Thomann nor Lee, disclose a circuit or method that sets the strength of the driver circuit to provide a potential or current in a desired power range. For example, with reference to Figure 3, the calibration process in Thomann ensures only that the two arrows indicating the VOH DRIVER and VOL DRIVER are the same magnitude, but fails to disclose anything about how or where to set the absolute value of VOH DRIVER or VOL DRIVER or whether or not that value is in a particular power range.

As explained above, all the circuits in Thomann and Lee do is ensure that whatever the power range happens to be, the high and low voltages are symmetric about a midpoint. This addresses the mismatch between transistor driver strength identified in Thomann and Lee but fails to teach or disclose the claimed “control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range.”

3. Ground 3: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with JESD79 for Claim 1 or 14.

The Petition fails to demonstrate that Lee and JESD79 teach or suggest the limitations of:

Claim 1:

. . . a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range . . .

Or,

Claim 14:

. . . controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range . . .

Ex. 1001, Cls. 1 and 14. The Petition references the arguments it makes for Lee as to Claim 1 in Section X.A.1.d of the Petition and adds little, if any, substance. Petition at 69. Section X.A.1.d on Lee alone includes the Voltage-Current curves from JESD79 (Petition at 39-40) although they are reproduced with annotations in this combination (Petition at 70-71). The Petition cross-references these same arguments for the method step in claim 14 with no additional substance. *Id.* at 88.

The identification of an alleged “desired power range” from the requirements of the JESD79 specification fails to address the flaws in Lee as discussed in the previous sections. JESD79’s definition of a desired power range says nothing about how to achieve it with the circuitry of Lee or otherwise. The Petition fails to explain how any of the circuitry in Lee would be used or modified to produce an output voltage in these specified ranges. As explained above, the Lee circuitry only ensures that the transistors are matched and the output high and low are symmetric about a midpoint. There is no disclosure, and the Petition does not allege any, for how to use

the identified circuitry in Lee to set the output high or low levels such that, following calibration or not, these voltages would fall within a desired power range as specified by JESD79 or otherwise.

4. Ground 4: The Petition Fails to Demonstrate Obviousness Over Lee And JESD79 in Combination with Garrett for Claim 1, 14 or 18.

The Petition fails to demonstrate that Lee and JESD79 in combination with Garrett teach or suggest the limitations of:

Claim 1:

. . . a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range . . .

Or,

Claim 14:

. . . controlling a driver strength of the driver circuit to set at least one of the current and the potential in at least one of a specification-prescribed current range and a specification-prescribed potential range . . .

Or,

Claim 18:

. . . a control means for providing a control signal for setting a driver strength of the driver means to provide at least one of an output line potential and an output line current in a lower power range . . .

Ex. 1001, Cls. 1, 14, 18. The Petition adds Garrett to the combination discussed in the previous section in order to allegedly “disclose[] structure used to implement

algorithms for driver strength feedback control, including a counter” to address terms that might be construed as means-plus-function limitations. Petition at 95, 97, 102 and 107. The Petition provides no additional analysis for the limitations above beyond that already addressed for Ground 3. *See* Petition at 97 and 102-103. Accordingly, the Petition fails to demonstrate that this combination in Ground 4 teaches or suggests any circuitry or method for setting the output voltage or current of the drive circuit in a particular range as required by the cited claim limitations.

VIII. PATENT OWNER’S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute *inter partes* review of the ’369 patent.

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 5,932 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Dated: May 15, 2023

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on May 15, 2023, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

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