

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2023-00514
Patent 7,145,369 B2

Before JEAN R. HOMERE, GREGG I. ANDERSON,
and NORMAN H. BEAMER, *Administrative Patent Judges*.

BEAMER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

On February 6, 2023, Xilinx, Inc. (“Petitioner”) filed a Petition (“Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–8, 14–16, and 18 of U.S. Patent No. 7,145,369 B2 (“the ’369 patent”). Paper 2 (“Pet”), 1. On May 15, 2023, Polaris Innovations Limited (“Patent Owner”) filed a Preliminary Response (“Prelim. Resp.”). Paper 9.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and any preliminary response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” *See* 37 C.F.R. § 42.108.

For the reasons expressed below, we determine that, on this record, Petitioner has not established a reasonable likelihood that it would prevail with respect to at least one of the challenged claims of the ’369 patent. Accordingly, we do not institute an *inter partes* review as to the challenged claims on the grounds of unpatentability presented.

II. BACKGROUND

A. The ’369 Patent

The ’369 patent, titled “Output Driver For An Integrated Circuit And Method For Driving An Output Driver,” was filed on July 9, 2004 and issued on December 5, 2006. Ex. 1001, codes (54), (22), (45). The ’369 patent is directed to an output driver for an integrated circuit dimensioned to supply a current intensity and/or a potential set to values within a lower power range of the current intensity and potential ranges defined by the

integrated circuit specification. *Id.* at code (57). Figure 1 is reproduced below.

FIG 1

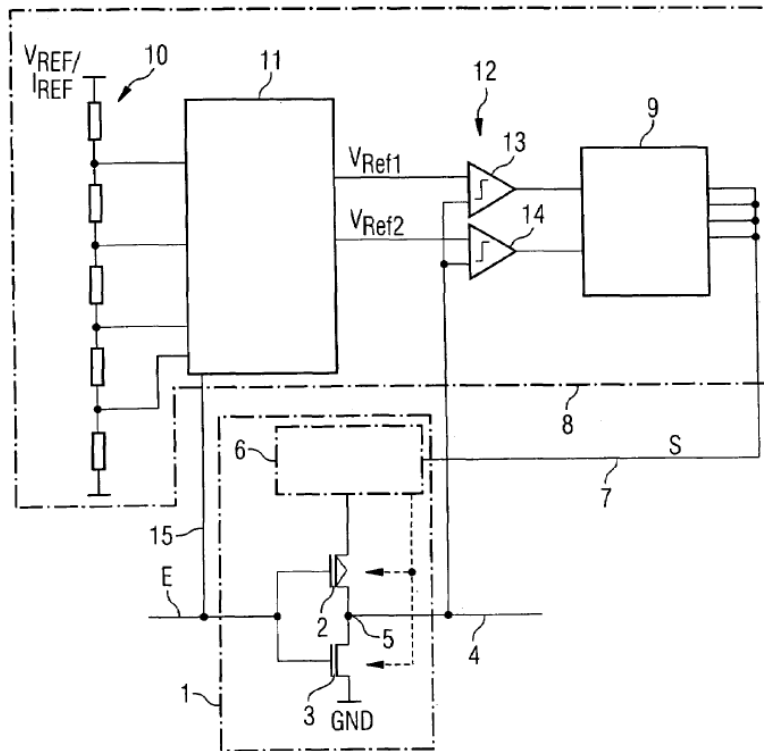


Figure 1 is a block diagram of an output driver, with driver circuit 1 including p-channel transistor 2 and n-channel transistor 3, which generates output 4 (high level, logic one, or low level, logic zero) in response to input E. Ex. 1001, 1:27, 3:62–63, 4:5–11, 5:33–36. Setting circuit 6 sets the driver strength of driver circuit 1 in response to control signal S, generated by control unit 8. *Id.* at 4:18–21, 4:33–36. The driver strength may be set, for example, by enlarging or decreasing the active area of the p-channel transistor 2 and of the n-channel transistor 3 in a manner dependent on the control signal S. *Id.* at 4:21–24.

Control unit 8 includes comparator unit 12, which compares output 4 to first and second reference potentials V_{Ref1} and V_{Ref2} , provided by voltage

divider 10 via multiplexer 11 (which selects the applicable pair of reference voltages in response to input E), and which reference potentials define a potential range within which the potential on output 4 is intended to lie. *Id.* at 4:41–49, 4:66–5:15. The result of the comparison is provided to evaluation unit 9, which generates control signal S. *Id.* at 4:49–53.

The first and second reference voltages are prescribed such that the range formed by V_{Ref1} and V_{Ref2} lies within a lower range of the permitted potential window prescribed by the integrated circuit specification.¹

Ex. 1001, 5:48–51. For example, the V_{Ref2} lower limit of a desired potential range can be set to the lower limit of the specification range (or some “distance” above the specification lower limit), and the V_{Ref1} upper limit can be a “tolerance magnitude” added to V_{Ref2} . Ex. 1001, 6:38–46, claim 2. This reduces power consumption of the integrated circuit by operating in a lower power range while ensuring that the corresponding potential and current values at the output driver are within the integrated circuit specifications.² *Id.* at 1:66–2:4, 2:17–31, 2:57–67, 5:58–66.

B. Illustrative Claim

Independent claim 1 is reproduced below.

1. An output driver for an integrated circuit, comprising:

¹ The '369 patent explains that integrated circuits have specifications which provide an upper and a lower current value or an upper and lower potential value depending on the signal state (high level or low level) of the output signal to be driven. Ex. 1001, 1:21–29.

² Power consumption is the product of the potential and current values. Baker Decl. ¶ 103.

- a driver circuit for driving an input signal of the output driver onto an output line;
- a measuring circuit for measuring at least one of an output line current and an output line potential; and
- a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range, wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit.

Ex. 1001, 6:57–7:3.

C. References

Petitioner relies on the following references (Pet. iii, 3):

- Lee, US 6,549,036 B1, filed May 31, 2000, issued April 15, 2003. Ex. 1005 (“Lee”).
- Thomann et al., US 6,330,194 B1, filed June 26, 2000, issued December 11, 2001. Ex. 1006 (“Thomann”).
- JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79 (June, 2000). Ex. 1007 (“JESD79”).
- Garrett et al., 6,094,075, filed August 27, 1998, issued July 25, 2000. Ex. 1008 (“Garrett”).

Petitioner also filed the Declaration of Dr. R. Jacob Baker in support of the Petition. Ex. 1003 (“Baker Decl.”).

D. Asserted Challenges to Patentability

Petitioner challenges the patentability of claims 1–8, 14–16, and 18 of the '369 patent on the following bases (Pet. 3):

Claims Challenged	35 U.S.C. §³	References
1–2, 5–7	103	Lee
1–2, 5–7	103	Lee, Thomann
1–7, 14–16	103	Lee, JESD79
1–8, 14–16, 18	103	Lee, JESD79, Garrett

E. Real Parties in Interest

Petitioner identifies Xilinx, Inc., Advanced Micro Devices, Inc., and ATI Technologies ULC as real parties in interest. Pet. 1. Patent Owner identifies itself as a real party in interest, and states that it is a subsidiary of Wi-LAN Inc., whose parent company is Quarterhill Inc. Paper 7, 2.

F. Related Proceedings

The parties identify *Polaris Innovations Limited v. Xilinx, Inc.*, Case No. 1:22-cv-00174-RGA (D. Del.) as a related proceeding. Pet. 1; Paper 7, 2.

³ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), included amendments to 35 U.S.C. §§ 102 and 103 that became effective after the filing of the application for the '369 patent. Therefore, we apply the pre-AIA versions of these sections.

III. ANALYSIS OF PETITIONER’S CHALLENGE

A. *Legal Standards*

To prevail in its challenge, Petitioner must show a reasonable likelihood that at least one claim is unpatentable. 35 U.S.C. § 314(a). Under § 314 the Board is required to make a binary choice to institute review or not. *SAS Institute Inc. v. Iancu*, 138 S.Ct. 1348, 1355 (2018). “In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (2012) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective indicia of non-obviousness (also called secondary considerations), such as

commercial success, long-felt but unsolved needs, and failure of others.⁴ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze grounds based on obviousness in accordance with the above-stated principles.

B. Level of Skill in the Art

In determining whether an invention would have been obvious at the time it was made, 35 U.S.C. § 103(a) requires us to resolve the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors that may be considered in determining the level of ordinary skill in the art include, but are not limited to, the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *Id.* In a given case, one or more factors may predominate. *Id.*

Petitioner asserts that a person of ordinary skill in the art at the time of the alleged invention of the '369 patent:

[W]ould have had a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and two or three years of academic or industry experience in integrated circuit input/outputs and memory systems, or comparable experience. . . . Additional work experience can substitute for educational or research experience, and vice versa. A POSITA would have been familiar with the JEDEC industry standards and knowledgeable about the design and operation of standardized DRAM memory systems and with output driver designs including digital/analog circuitry.

⁴ The record does not include evidence or argument regarding objective indicia of nonobviousness.

Pet. 8–9 (citing Baker Decl. ¶¶ 31–35). Patent Owner does not contest Petitioner’s proposal at this stage of the proceeding. Prelim. Resp. 9.

Petitioner’s proposal is consistent with the level of ordinary skill in the art reflected by the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *GPAC*, 57 F.3d at 1579. On this record, the level of ordinary skill is neither in dispute nor dispositive of any challenge. For purposes of this Decision, we apply Petitioner’s articulation.

C. Claim Construction

The Petition was accorded a filing date of February 6, 2023. Paper 3. In an *inter partes* review for a petition filed on or after November 13, 2018, a claim “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). We apply the claim construction standard from *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (*en banc*).

Claim terms need only be construed to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner provides constructions of several means-plus-function limitations in claim 18 pursuant to 35 U.S.C. §112, paragraph 6. Pet. 9–14. It is not necessary at this stage of the proceeding to resolve Petitioner’s proposals regarding these means-plus-function limitations. Patent Owner submits that the Board need not construe any claim term. Prelim. Resp. 9.

In our discussion below we nevertheless consider the proper scope of the independent claim requirements of a “control unit” (claim 1), of “controlling a driver strength” (claim 14), and of a “control means”

(claim 18). In particular, as discussed in Section III.D.2.c) below, the scope of the term “desired power range” is at issue.

D. Alleged Obviousness of Claims 1–2 and 5–7 over Lee

Petitioner challenges claims 1–2 and 5–7 as obvious over Lee.
Pet. 25–51.

1. Lee

Lee, titled “Simple Output Buffer Drive Strength Calibration,” issued April 15, 2003 from an application filed May 31, 2000. Ex. 1005, codes (54), (45), (22). Lee discloses an output buffer driver calibration circuit which includes pull-up and pull-down transistors which are adjusted so that they have the same drive strengths. *Id.* at code (57). According to Lee, this “reduces timing uncertainty in high speed signaling systems.” *Id.* at 2:31–32. As further explained:

A mismatch of the pull-up transistor characteristic with the pull-down transistor characteristic will create a different timing relationship with signals transitioning to a logic one state versus signals transitioning to a logic zero state. This results in a timing uncertainty in the system, which will limit the maximum system operational data rate.

Ex. 1005, 2:4–10. Figure 4 is reproduced below.

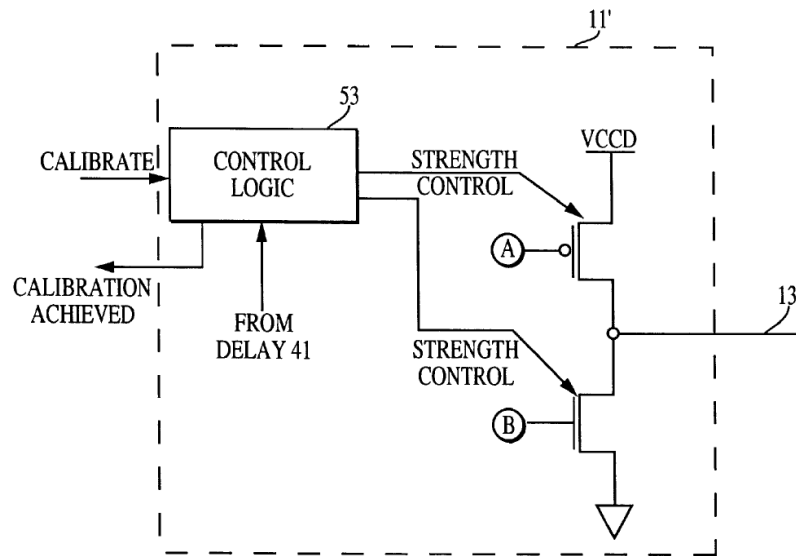


FIG. 4

Figure 4 illustrates output buffer 11' with calibration control logic 53 which outputs “strength control” signals to control the upper, pull-up transistor output and the lower, pull-down transistor output, so that the transistors have the same drive strengths. Ex. 1005, 2:58–60, 5:43–45, 5:53–58. During normal operation, the gate of the pull-up transistor at node A is asserted low while the gate of the pull-down transistor at node B is asserted low to switch the bus voltage to a high voltage VOH (the logic “1” level), and node A is asserted high, while node B is asserted high for low voltage VOL (the logic “0” state). *Id.* at 1:61–63, 3:7–9. 3:47–53. For fastest switching, nodes A and B should be transitioned simultaneously, which requires them to have the same drive strengths. *Id.* at 1:17–23, 2:30–32, 3:50–51.

To ensure this, during a calibration stage, node A is asserted low while node B is asserted high, so both transistors are turned on at the same time, and the resulting output is compared to a midpoint reference voltage VREF, which is set to VDDQ/2 (*i.e.*, halfway between the VDDQ supply

voltage and ground). Ex. 1005, Fig. 1, 3:53–60. If the transistor strengths are well matched in this condition, the output voltage from the output buffer will equal VREF, indicating that the transistors are calibrated. *Id.* at 3:56–58. Otherwise, the control logic will change the drive strengths of one of the transistors, such as by reducing its effective device width, so that the transistors match. *Id.* at 3:63–66, 4:6–10, 4:46–61.

Lee explains that this “active calibration” is needed to account for “the effects of process variance, voltage variation or temperature variation on output buffer drivers.” Ex. 1005, 1:34–37.

2. Independent Claim 1

a) Petitioner’s Challenge

For the “output driver for an integrated circuit” preamble of independent claim 1, Petitioner generally relies on the disclosures in Lee of its output driver circuit embodiments. Pet. 25–26 (citing Ex. 1005, Figs. 1, 5, 7, 3:13–32, 5:45–47, 7:33–35, 7:57–67; Baker Decl. ¶¶ 75–76).⁵

For the claim 1 requirement of “a driver circuit for driving an input signal of the output driver onto an output line,” Petitioner relies the above-described output buffer including the pull-up and pull-down transistors. Pet. 26–28 (citing Ex. 1005, Figs. 1, 4, 3:33–56, 6:11–53; Baker Decl. ¶¶ 77–80).

For the claim 1 requirement of “a measuring circuit for measuring at least one of an output line current and an output line potential,” Petitioner relies on input buffer circuitry, to which the output from the output buffer is

⁵ Based on the present record, we make no determination whether or not the preamble of claim 1 is limiting.

applied, and which is implemented as “a common source differential amplifier,” or alternatively relies on “a higher accuracy comparator,” either of which perform, during calibration, the above described comparison of the buffer output to reference voltage VREF. Pet. 30–32 (citing Ex. 1003, Figs. 1, 3, 5, 6, 3:43–46, 4:46–49, 5:28–31, 5:45–6:41; Baker Decl. ¶¶ 85–88).

For the claim 1 requirement of

a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a desired power range of a specification-prescribed potential range and a specification-prescribed current range,

Petitioner relies on the above-described control logic, which, in response to the comparison of the output buffer voltage to VREF, provides signals for controlling the drive strengths of the output buffer transistors. Pet. 33–42 (citing Ex. 1005, Figs. 1, 2, 3, 5, 1:26–33, 1:61–63, 2:39–44, 3:6–24, 3:33–41, 3:47–53, 3:56–58, 4:6–5:27, 10:6–12, 12:37–46; Baker Decl. ¶¶ 94–103).

In regard to the required “specification-prescribed potential range,” Petitioner relies on the fact that the output driver of Figure 1 has its transistors connected between the supply voltage VDDQ and ground, which therefore “expressly describe[s]” the range of the output-line voltage during normal operation. *Id.* at 37–38 (citing Ex. 1005, Fig. 1, 3:33–41, 10:6–12, 12:37–46; Baker Decl. ¶ 100). For the required “specification-prescribed current range,” Petitioner relies on the disclosure in Lee that “current-versus-voltage curves for output buffer drivers are specified with minimum and maximum limits for the voltage and current levels,” and argues that one of ordinary skill would have appreciated that specifying a voltage range

necessarily also specifies a current range. *Id.* at 38–40 (citing Ex. 1005, 1:26–33; Baker Decl. ¶ 101).

In regard to the requirement that the output be provided in a “desired power range,” Petitioner first argues that the ’369 patent does not “expressly define or otherwise explain how a ‘power range’ is ‘desired’ or by whom it is ‘desired.’” *Id.* at 37 (citing Baker Decl. ¶ 99). Notwithstanding that observation, Petitioner relies on the fact that, per Ohm’s Law, power consumption is the product of the potential and current values, and from that argues that the specified voltage and current ranges necessarily specify a power range. *Id.* at 40, 42 (citing Baker Decl. ¶¶ 102–103). Petitioner also argues that the above-described calibration scheme of Lee teaches a desired potential range because it ensures that the output voltage swings across a range between a high voltage V_{OH} and a low voltage V_{OL} , which are between V_{DDQ} and ground, and which are symmetric about a mid-voltage V_{REF} after calibration. *Id.* at 40–42 (citing Ex. 1005, Figs. 2, 3, 1:61–63, 3:6–9, 3:47–58, 4:35–61; Baker Decl. ¶¶ 102–103).

For the claim 1 requirement of “wherein the control unit includes a feedback control to affect the setting of the driver strength based on a measured value provided by the measuring circuit,” Petitioner relies on the fact that the output of the output buffer is fed back to the input buffer circuitry, or alternatively fed back to “a higher accuracy comparator.” Pet. 42–44 (citing Ex. 1005, Figs. 1–6, 4:36–61, 5:39–41, 5:46–58, 7:26–32; Baker Decl. ¶¶ 104–106).

b) Patent Owner’s Response

Patent Owner argues that Lee does not teach the claim 1 requirement of “a control unit for providing a control signal for setting a driver strength

of the driver circuit to provide at least one of the output line potential and the output line current *in a desired power range*.” Prelim. Resp. 22–23 (emphasis supplied). Patent Owner explains that the ’369 patent is directed to the problem of setting the output voltage in a particular power range in light of process deviations, temperature and voltage fluctuations, and different loads, by using feedback control to set the output potential or current of the driver. *Id.* at 1. In contrast, argues Patent Owner:

Lee is directed to a different problem. Lee is concerned with mismatch between the drive strength of the transistors of a driver circuit that can cause timing problems when its transistors switch to different logic states. To solve this problem, Lee discloses a calibration circuit and method that adjusts the drive strength of the transistors so that the output for logic high and the output for logic low are symmetric about a midpoint by simultaneously turning on the pull-up and pull-down transistors of the driver circuit during the adjustment.

Prelim. Resp. 2. Patent Owner further argues that “Lee does not . . . disclose any circuitry or method for setting the output voltage or current of the drive circuit in a particular range.” *Id.*, *see also* Prelim. Resp. 20–23.

Patent Owner notes that Petitioner argues that “Lee teaches a desired potential range because its calibration scheme ensures that the output voltage swings across a range between a high voltage V_{OH} and a low voltage V_{OL} . . . that are symmetric about a mid-voltage V_{REF} after calibration.” *Id.* at 22 (citing Pet. 40–41). But, argues Patent Owner, in Lee, “the power range is set to be symmetric around a mid-voltage V_{REF} without regard to whether the potential is within any particular power range.” *Id.* at 23. Patent Owner attributes the absence of any teaching in Lee of providing potential or current output in a desired range to the fact that “Lee’s calibration circuit only addresses the issue identified in Lee that the pull-up

and pull-down transistors need to be matched to reduce timing uncertainty. *Id.* (citing. Ex. 1005, 1:6–8, 2:4–10). Patent Owner argues that “Petitioner does not identify any reasoning or explanation for how or why one of ordinary skill would adapt or modify the circuitry in Lee to set the output potential (or current) in a particular power range.” *Id.*

c) Analysis

At issue is whether Lee teaches or suggests the claim 1 requirement, “a control unit for providing a control signal for setting a driver strength of the driver circuit to provide at least one of the output line potential and the output line current in a *desired power range* of a specification-prescribed potential range and a specification-prescribed current range.” Ex.1001, 6:63–66 (emphasis supplied). We do not agree with Petitioner’s assertion that the ’369 patent does not “expressly define or otherwise explain how a ‘power range’ is ‘desired’ or by whom it is ‘desired.’” Pet. 37 (citing Baker Decl. ¶ 99). As a threshold matter, as Petitioner has explained, one of ordinary skill would have understood, in the context of the ’369 patent, that for a given potential range, there is a corresponding current range, because integrated circuit devices have specifications which establish the relationship between potential and current. *Id.* at 38–30 (citing Ex. 1001, Figs. 2A, 2b, 6:12–14; Baker Decl. ¶ 101). Moreover, as Petitioner has also explained, one of ordinary skill would have understood that a “power range” is defined by a corresponding potential range and current range, given the Ohm’s Law relationship of power as the product of voltage and current. Pet. 42 (citing Baker Decl. ¶ 103). Thus, given a particular potential value range, there is both a corresponding current range and power range.

Accordingly, in answer to Petitioner’s question as to how a power range is desired, as discussed above in Section II.A, the ’369 patent provides techniques for setting “desired potential value range[s]” for each of the high level (digital one) and low level (digital zero) of the output signal:

[E]ssentially four reference potentials may be prescribed . . . two respectively prescribing the *desired potential value range* for a high level and the respective other two reference potentials prescribing the *potential value range* for the low level of the output signal.

Ex. 1001, 5:8–13 (emphasis supplied). Thus, given that the ’369 patent describes setting desired potential value ranges, it also would be understood to set corresponding desired power ranges for the high and low output levels. As to the criteria for selecting the potential ranges (and thus the power ranges), the ’369 patent explains that the potential value ranges are selected to “lie within a lower range of the permitted potential window prescribed by the specification.” *Id.* at 5:16–18. In particular, the ’369 patent explains that “specifications for integrated circuits . . . provide a relatively large current intensity range or potential range for the output drivers,” which “may signify great differences with regard to the power consumption depending on the position of the actual potential value or current value within the specification.” *Id.* at 1:39–49. Therefore, the ’369 patent control circuitry reduces the power consumption of the integrated circuit by confining the potential and current intensity values to a lower power range lying within the specification conforming range limits. *Id.* at 2:1, 2:17–31, 2:50–67, 3:35–51. *I.e.:*

The first and second reference voltages are prescribed such that the range formed by the first and second reference Voltages V_{Ref1} , V_{Ref2} lies within a lower range of the

permitted potential window prescribed by the specification
[T]he reference voltages may be selected . . . to define a voltage range which determines a lower power range within the permissible current-voltage window for the output signal on the output line.

Ex. 1001, 5:48–64. Also:

A reduction of the power consumption through a reduction of the current intensity through the activated transistor is permissible as long as the current intensity is within the respective current voltage window prescribed by the specification. It is thus possible, within the limits prescribed by the specification, to define a current intensity range which brings about minimal power consumption through the driver circuit This range is chosen to lie within the range prescribed by the current-voltage windows.

Ex. 1001, 6:27–37. For example, as discussed above in Section II.A, the V_{Ref2} lower limit of a desired potential range can be set to the lower limit of the specification range (or some “distance” above the specification lower limit), and the V_{Ref1} upper limit can be a “tolerance magnitude” added to V_{Ref2} . *Id.* at 3:1–8, 6:38–46, claim 2. Also, as is apparent from the above, the answer to Petitioner’s other question — who “desires” the power range — is that it is the designer of the device in question, who determines the values of V_{Ref1} and V_{Ref2} (or whatever equivalent means for controlling the outputs is used).

Turning to the claim 1 requirement of providing an “output line potential [or current] *in a desired power range* of a specification-prescribed potential range and a specification-prescribed current range,” as discussed above, given that any voltage range necessarily has a corresponding current range, and given the Ohm’s Law relationship that power is voltage times

current, this claim requirement may be restated as providing an “output line *power* in a desired power range of a *specification-prescribed power range*.” The desired power range is not the specification-prescribed power range, but rather a *controlled* range *in* that range. As stated in the ’369 patent, “[t]his [desired] range is chosen to lie *within* the range prescribed by the current-voltage windows.” *Id.* at 6:35–37 (emphasis supplied). Although the embodiment disclosed in the ’369 patent sets the desired range to a “lower power range within the permissible current-voltage window” (5:50–51), as does claim 4, which depends from claim 1 (“wherein the desired power range corresponds to a lower portion of the specification prescribed potential range and a lower portion of the specification-prescribed current range”), independent claim 1 does not specify where within the specification-prescribed power range the desired range must be. Nonetheless, claim 1 requires the “desired power range” to be a range that a “control unit . . . provide[s].” *Id.* at 6:62–67.

Petitioner alleges that this requirement is satisfied by the fact that, in Lee, the output line potential ranges between a high voltage V_{OH} and a low voltage V_{OL}, which are between V_{DDQ} and ground. Pet. 40–41. Thus, argues Petitioner, the “desired power range” is satisfied given the Ohm’s Law relationship between voltage and power. *Id.* at 42. “V_{OH}” in this context refers to the output voltage when the pull-up transistor of the output buffer is turned on, representing a “logical high” value (*i.e.*, a digital value of “one”), and “V_{OL}” represents when the pull-down transistor of is turned on, for a “logical low” value (*i.e.*, a “zero”). Ex. 1005, 3:7–9, 3:33–39, 3:47–53; Baker Decl. ¶ 48.

However, we agree with Patent Owner that Lee does not teach or suggest the claim 1 requirement of “provid[ing] at least one of the output line potential and the output line current in a desired power range,” because Lee merely sets the VOH and VOL levels so that pull-up and pull-down transistors have the same drive strengths, without any provision for controlling those levels to lie within a desired range. As Patent Owner points out, neither Petitioner nor its declarant provides any reasoning or explanation for how or why one of ordinary skill would adapt or modify the circuitry in Lee to set the output potential (or current) for VOH or VOL in a particular power range. Prelim. Resp. 23.

There is an additional error in Petitioner’s assertion (at Pet. 40–41) that Lee satisfies the control unit requirement of claim 1 because the output line potential ranges between a high voltage VOH and a low voltage VOL, which are between VDDQ and ground. Petitioner errs because the “desired power range” referred to in claim 1 is not referring to the range between high and low logical states. Rather, the desired range of values is for a particular logic state — *i.e.*, a desired range for the pull-up path, generating VOH, within the specification-prescribed range for that value, and/or the desired range for the pull-down path, generating VOL, within its specification-prescribed range. As stated in the ’369 patent, “[d]epending on whether a high or low level is intended to be driven by the output driver, the specification prescribes different upper and lower current-voltage characteristic curves for the pull-up path and the pull-down path.” Ex. 1001, 1:34–38 (emphasis supplied). Likewise, the control circuit of the invention insures that “the current intensity and/or the potential on the output line, *depending on the input signal to be driven*, lies in a lower power range of the

current intensity range and/or potential range prescribed by the specification.” *Id.* at 2:53–56 (emphasis supplied). To maintain separate power ranges for the VOH and VOL signals, as discussed in Section II.A above, the ’369 patent uses two different pairs of V_{Ref1} and V_{Ref2} potentials, selected by multiplexer 11 in response to logical input E. *Id.* at 5:3–13. As the ’369 patent further explains these two different desired ranges, one for high output, and one for low output:

The reference potentials for defining the potential window for the *high* level of the output signal are chosen such that they lie within a lower range of the potential window permitted by the specification for the *high* level of the output signal on the output line 4. The potential window for the *low* level of the output signal on the output line 4 is defined by the reference potentials such that it likewise lies within a lower range of the potential window prescribed by the specification for the *low* level of the output signal.

Ex. 1001, 5:15–24 (emphasis supplied).

Thus, when Petitioner argues that “Lee teaches a desired potential range because it ensures that the output voltage swings across a range between a high voltage VOH and a low voltage VOL, which are between VDDQ and ground” (Pet. 40–41), Petitioner is incorrectly focusing on the range between VOH and VOL, when the claimed range refers to the range of pull-up, VOH values and/or the range of pull-down, VOL values.

Accordingly, for the reasons set forth above, we determine that the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail in establishing that claim 1 is unpatentable under 35 U.S.C. § 103(a) over Lee.

3. Dependent Claims 2 and 5–7

For the same reasons as discussed above for claim 1, we determine that the information presented in the Petition does not demonstrate a reasonable likelihood that Petitioner will prevail in establishing that claims 2 and 5–7, which depend from claim 1, are unpatentable under 35 U.S.C. § 103 over Lee.

E. Alleged Obviousness of Claims 1–2 and 5–7 over Lee and Thomann

Petitioner challenges claims 1–2 and 5–7 as obvious over the combination of Lee and Thomann. Pet. 51–63.

1. Thomann

Thomann, titled “High Speed I/O Calibration Using An Input Path And Simplified Logic,” issued December 11, 2001 from an application filed June 7, 2000. Ex. 1006, codes (54), (45), (22). For all purposes here, Thomann is very similar to Lee, and like Lee discloses an output buffer driver calibration circuit which includes pull-up and pull-down transistors which are adjusted so that they have the same drive strengths to “reduce[] timing uncertainty in high speed signaling systems.” *Id.* at 1:16–22, 2:28–30, 2:53–57, 4:58–63. Figure 3 is reproduced below.

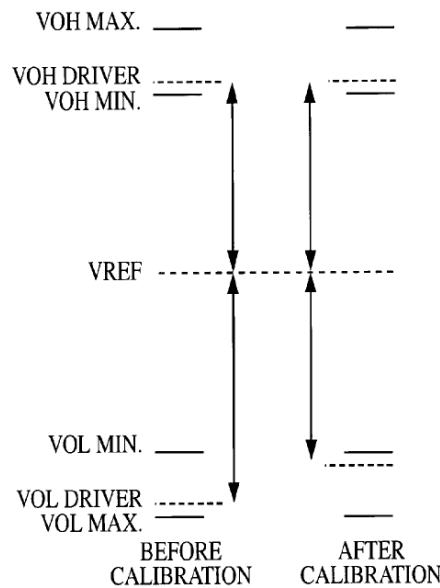


FIG. 3

Figure 3 illustrates a graph of the calibration operations performed in accordance with the disclosed embodiment. Ex. 1006, 3:8–9. The left portion of the figure depicts a mismatch between VOH Driver (*i.e.*, the voltage for logic high, or “one”) and VOL Driver (the voltage for logic low, or “zero”) before calibration, and the right side depicts that relationship after calibration, where the voltages are equally balanced between VREF. *Id.* at 1:60–62, 5:37–44, 5:58–65. Also shown are ranges for the two levels: “VOH MAX.” to “VOH MIN.” for the logic high level, and “VOL MAX.” to “VOL MIN.” for the logic low level. Ex. 1006, Fig. 3; Baker Decl. ¶ 66. Although Thomann does not explain what these ranges pertain to, the prior art background section of Thomann includes a reference to “specifying the driver characteristics for all transistors in an output buffer driver [s]uch as specifying minimum and maximum output currents [and] specifying the current versus voltage curves with minimum and maximum limits” Ex. 1006, 1:26–31. Also, Petitioner’s declarant characterizes these ranges as

“specification-prescribed” ranges. Baker Decl. ¶ 127. We therefore treat them as such — there is no indication in Thomann that VOH or VOL are controlled to lie within these ranges.

2. *The Combination of Lee and Thomann*

Petitioner argues that one of ordinary skill would have been motivated to combine Lee and Thomann because both address calibration of an output buffer driver using similar techniques, share common inventorship, and were originally assigned to the same entity. Pet. 51–52 (citing Ex. 1005, codes (73) (75), Fig. 1, 1:6–8, 3:13–32, 4:31–61; Ex. 1006, codes (73) (75), Fig. 1, 1:5–7, 4:19–24, 4:47–57; Baker Decl. ¶¶ 116–121). Petitioner argues that Thomann would have provided one of ordinary skill with additional details about the range of VOH and VOL levels and how the output driver voltage between the VOH and VOL levels changes with calibration. *Id.* at 52 (citing Ex. 1006, Figs. 1, 3, 5:37–65, 6:17–31; Baker Decl. ¶ 119).

Patent Owner does not specifically challenge the motivation for combining Thomann with Lee. *See generally* Prelim. Resp. For purposes of this Decision, we determine that Petitioner has provided sufficiently articulated reasoning with rational underpinnings for the proffered combined teachings of Lee and Thomann.

3. *Claim 1*

Petitioner relies on its above analysis of Lee alone for all of the requirements of claim 1 other than the “control unit” requirement. Pet. 55.

For the control limit requirement, Petitioner supplements its arguments based on Lee by invoking the above-discussed Figure 3 of Thomann, which discloses “specification-prescribed” ranges of “VOH

MAX.” to “VOH MIN.” for the logic high level VOH Drive, and “VOL MAX.” to “VOL MIN.” for the logic low level VOL Drive. Pet. 55–58.

Petitioner, relying on its declarant Dr. Baker’s testimony, asserts:

In the combination, the “desired power range” corresponds to the product of the voltage range(s), between VOL MAX and VOL MIN and/or between VOH MAX and VOH MIN, and the current range(s), corresponding minimum and maximum currents for each of the four voltages (VOL MAX, VOL MIN, VOH MAX, and VOH MIN).

Pet. 57–58 (citing Baker Decl. ¶ 129).

Patent Owner argues that the Lee/Thomann combination does not teach or suggest the “control unit” requirement of claim 1, for the same reasons as consideration of Lee alone fails. Prelim. Resp. 23–25. Like Lee, argues Patent Owner, Thomann is directed to matching transistor strengths to address timing issues, rather than controlling the power ranges of the transistor outputs. *Id.* at 23–24. Patent Owner argues that, notwithstanding the addition of Figure 3 of Thomann (reproduced above), “neither Thomann nor Lee, disclose a circuit or method that sets the strength of the driver circuit to provide a potential or current in a desired power range.” *Id.* at 25. Patent Owner points out that Figure 3 only depicts the Lee/Thomann calibration technique by which VOH DRIVER and VOL DRIVER are set to the same magnitude, but fails to disclose anything about how or where to set the absolute value of VOH DRIVER or VOL DRIVER or whether or not that value is in a particular power range. *Id.*

We agree with Patent Owner for the same reasons as discussed above in Section III.D.2.c). Although Thomann adds to Lee an illustration of specification-prescribed voltage ranges for VOH and VOL, it provides no teaching or suggestion of providing an “output line potential [or current] *in a*

desired power range of a specification-prescribed potential range and a specification-prescribed current range,” as required by the claim.

Accordingly, for the reasons set forth above, we determine that the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail in establishing that claim 1 is unpatentable under 35 U.S.C. § 103(a) over the combination of Lee and Thomann.

4. Dependent Claims 2 and 5–7

For the same reasons as discussed above for claim 1, we determine that the information presented in the Petition does not demonstrate a reasonable likelihood that Petitioner will prevail in establishing that claims 2 and 5–7, which depend from claim 1, are unpatentable under 35 U.S.C. § 103 over the combination of Lee and Thomann.

F. Alleged Obviousness of Claims 1–7 and 14–16 over Lee and JESD79

Petitioner challenges claims 1–7 and 14–16 as obvious over the combination of Lee and JESD79. Pet. 64–93.

1. JESD79

JESD79 is a June 2000 standard specification for a “Double Data Rate (DDR) SDRAM Specification.” Ex. 1007. Petitioner provides evidence, not disputed by Patent Owner, that JESD79 was available at least on August 17, 2000. Pet. 20–21; *see generally* Prelim. Resp. JESD79 includes recommended current-voltage characteristic curves and tables that define the maximum, minimum, and “typical” values for “Pulldown” and “Pullup” characteristics. *Id.* at 59–60. The “typical” values are the recommended specifications for implementation in a memory device being designed using the “IBIS” simulation tool. *Id.* at 59, 64. JESD79 also specifies a supply

voltage range between 2.3 and 2.7 volts. *Id.* at 58. The JESD79 specification provides for a user to set a control bit to indicate the use of current-voltage characteristic curves for “Normal” or “Weak” drive strength (although that actual curves for the “Weak” setting were not available for the May 2000 edition of the standard). *Id.* at 16.

2. The Combination of Lee and JESD79

Petitioner argues that one of ordinary skill would have been motivated to use the JESD79 current-voltage specification values in Lee, because both references relate to drive strengths of pull-up and pull-down devices for an output driver, Lee specifically contemplates use for Dynamic Random Access Memory (DRAM), Lee refers to the fact that output drivers are characterized by specification-prescribed current-voltage characteristic curves, and JESD79 was an established standard suitable to be implemented in a device in accord with Lee. Pet. 64–69 (citing Ex. 1005, code (57), Fig. 1, 1:30–34, 2:11–20, 3:13–32, 4:31–61, 7:38–47; Ex. 1007, 4–5, 59–60; Baker Decl. ¶¶ 139–148).

Patent Owner does not specifically challenge the motivation for combining JESD79 with Lee. *See generally* Prelim. Resp. For purposes of this Decision, we determine that Petitioner has provided sufficiently articulated reasoning with rational underpinnings for the proffered combined teachings of Lee and JESD79.

3. Independent Claims 1 and 14

Petitioner relies on its above analysis of Lee alone, discussed in Section III.D.2.a) above, for all of the requirements of claim 1 other than the “control unit” requirement. Pet. 69.

For the control limit requirement of claim 1, Petitioner supplements its arguments based on Lee by relying on the current-voltage characteristic curves and tables disclosed in JESD79, and the JESD79-specified supply voltage range, as satisfying the requirements for a “specification-prescribed potential range and a specification-prescribed current range.” Pet. 69–72 (citing Ex. 1005, Figs. 1, 4, 6; Ex. 1007, 11, 58–60; Baker Decl. ¶¶ 153–156). For the “desired power range” requirement, Petitioner relies on the portion of the JESD79 current-voltage characteristic curves labeled as “Typical High” and “Typical Low,” and which lie within the curves labeled “Minimum” and “Maximum,” and argues that this teaches a desired power range given the Ohm’s Law relationship of power as the product of voltage and current. *Id.* at 72–73 (citing Ex. 1007, 59–60; Baker Decl. ¶ 157).

For the most part, the requirements of independent claim 14, and Petitioner’s analysis of those requirements, essentially track those of claim 1. Pet. 84–90. An additional requirement of claim 14 is that “the driver strength is set such that the potential and the current intensity lie in a lower power range of the specification-prescribed current range and the specification-prescribed potential range.”⁶ Ex. 1001, 8:3–6. For this requirement, Petitioner relies on the fact that the JESD79 current-voltage characteristic curves labeled as “Typical High” and “Typical Low” lie within the curves labeled “Minimum” and “Maximum,” and are thus in a lower power range. Pet. 82–83, 88–89 (citing Ex. 1007, 59–60; Baker Decl. ¶¶ 168, 175). Petitioner also relies on the provision in JESD79 for a lower voltage range (2.3-2.5 volts) for slow transistors compared to the

⁶ Dependent claim 4 adds this requirement to claim 1. Ex. 1001, 7:18–21.

typical 2.3-2.7 volt range. Pet. 83–84 (citing Ex. 1007, 56–60; Baker Decl. ¶ 169).

Patent Owner argues that the Lee/ JESD79 combination does not teach or suggest the “control unit” requirement of claim 1 or of “controlling the driver strength” of claim 14 for the same reasons as consideration of Lee alone fails. Prelim. Resp. 25–27. Patent Owner argues that, notwithstanding introducing the JESD79 current-voltage characteristic curves into the combination, there is no teaching or suggestion in the combination of achieving any desired power range, or lower power range — rather, argues Patent Owner, it is still the case that Lee only ensures that the pull-up and pull-down transistors are matched and the output high and low are symmetric about a midpoint. *Id.* at 26–27.

We agree with Patent Owner for the same reasons as discussed above in Section III.D.2.c). Although JESD79 adds to Lee examples of specification-prescribed current-voltage characteristic curves and voltage ranges, it provides no teaching or suggestion of providing an “output line potential [or current] *in a desired power range* of a specification-prescribed potential range and a specification-prescribed current range,” as required by claim 1, or a “lower power range” as required by claim 14. Petitioner does not demonstrate any likelihood that the Lee/ JESD79 combination teaches these claim requirements. Petitioner relies on the fact that the JESD79 current-voltage characteristic curves for the pull-up and pull-down paths include curves labelled “Typical High” and “Typical Low” that are within curves labelled “Maximum” and “Minimum.” Pet. 70–71. But Petitioner mischaracterizes these curves: the “Typical” curves are not suggested ranges for use within the Maximum and Minimum curves, but rather are suggested

for use as a *specification* for a memory device being designed using a simulation tool. Ex. 1007, 59, 64. There is no teaching or suggestion that the “Typical” curves are to be implemented as an operational range in a memory device where the specification-prescribed ranges are defined by the “Maximum” and “Minimum” curves. And, in any event, as Patent Owner argues, there is no teaching or suggestion in the combination of achieving any desired power range, or lower power range, within specification-provided ranges.

Accordingly, for the reasons set forth above, we determine that the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail in establishing that claims 1 and 14 are unpatentable under 35 U.S.C. § 103(a) over the combination of Lee and JESD79.

4. Dependent Claims 2–7 and 15–16

For the same reasons as discussed above for independent claims 1 and 14, we determine that the information presented in the Petition does not demonstrate a reasonable likelihood that Petitioner will prevail in establishing that claims 2–7 and 15–16, which depend from claim 1 or claim 14, are unpatentable under 35 U.S.C. § 103 over the combination of Lee and JESD79.

G. Alleged Obviousness of Claims 1–8, 14–16, and 18 over Lee, JESD79, and Garrett

Petitioner challenges claims 1–8, 14–16, and 18 as obvious over the combination of Lee, JESD79, and Garrett. Pet. 93–106. Petitioner relies on Garrett for the requirement in dependent claim 8 for a “counter,” and the commensurate requirement in independent claim 18 by virtue of the fact that

a counter is part of the structure disclosed in the '369 specification that corresponds to the mean-plus function claim requirement, “evaluation means.” Pet. 97–99, 105–106. Petitioner does not rely on Garrett for any of the above-discussed requirements of a desired power range or lower power range of independent claims 1, 14, and 18. *See generally*, Pet. 93–106. Therefore, for the reasons discussed above, we determine that the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail in establishing that claims 1 and 14 are unpatentable under 35 U.S.C. § 103(a) over the combination of Lee, JESD79, and Garrett. Likewise, we determine that the information presented in the Petition does not demonstrate a reasonable likelihood that Petitioner will prevail in establishing that claims 2–8 and 15–16, which depend from claim 1 or claim 14, are unpatentable under 35 U.S.C. § 103 over the combination of Lee, JESD79, and Garrett.

IV. CONCLUSION

After considering the evidence and arguments presented in the Petition and the Preliminary Response, Petitioner has not established a reasonable likelihood of prevailing on its assertion that at least one claim of the '369 patent is unpatentable. Accordingly, we do not institute an *inter partes* review.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied and no *inter partes* review is instituted.

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Patent 7,145,369 B2

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