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Patent claims

1. A dynamic semiconductor memory device of a random-access
5 type (DRAM/SDRAM) having an initialization circuit which
controls the switching-on operation of the semiconductor
memory device and of its circuit components and which supplies
a supply voltage stable signal (POWERON) once the supply
voltage has been stabilized after the switching-on of the
10 semiconductor memory device,
wherein the initialization circuit has an enable circuit (9)
that receives the supply voltage stable signal (POWERON) and
further command signals (PRE, ARF, MRS) externally applied to
the semiconductor memory device, which enable circuit supplies
15 an enable signal (CHIPREADY) after the recognition of a
predetermined proper initialization sequence of the command
signals (PRE, ARF, MRS) applied to the semiconductor memory
device, which enable signal causes the unlatching of a control
circuit (13) provided for the proper operation of the
20 semiconductor memory device,
c h a r a c t e r i z e d i n t h a t
the command signals (PRE, ARF, MRS) externally applied to the
semiconductor memory device in the initialization sequence
recognized by the enable circuit (9) comprise the preparation
25 command for word line activation (PRE-CHARGE), and/or the
refresh command (AUTOREFRESH), and/or the load configuration
register command (MODE-REGISTER-SET).

30 2. A semiconductor memory device according to Claim 1,
c h a r a c t e r i z e d i n t h a t
the enable circuit (9) has at least one bistable multivibrator
stage (14, 15, 16) with a set input (S) to which a command
35 signal (PRECHARGE, AUTOREFRESH, MODE-

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REGISTER-SET) is applied, a reset input (R) to which the supply
voltage stable signal (POWERON) or a signal derived therefrom
or a linked signal is applied, and with an output (Q) at which
5 the enable signal (CHIPREADY) (9) is derived.

3. A semiconductor memory device according to Claim 2,
c h a r a c t e r i z e d in that
the enable circuit (9) has a number of bistable multivibrator
10 stages (14, 15, 16) each associated to a command signal (PRE,
ARF, MRS).

4. A semiconductor memory device according to Claim 2 or 3,
c h a r a c t e r i z e d in that
the output (Q) of at least one of the bistable multivibrator
15 stages (14) is fed to a reset input of a further multivibrator
stage (15).

5. A semiconductor memory device according to Claim 3 or 4, c
20 h a r a c t e r i z e d in that,
in one of the bistable multivibrator stages (15), the supply
voltage stable signal (POWERON) and the signal output from the
output (Q) of the further multivibrator stage (14) are fed to
the reset input (R) of the multivibrator stage (15) after
25 having been logically combined by a gate (17).

6. A semiconductor memory device according to any one of Claims
3 to 5,
30 c h a r a c t e r i z e d in that
the bistable multivibrator stage (14, 15, 16) is formed in
each case by an RS multivibrator constructed of at least two
NOR or NAND gates (14A, 14B, 15A, 17, 16A, 16B).

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7. A semiconductor memory device according to any one of Claims 1 to 6,

c h a r a c t e r i z e d in that

the initialization sequence recognized as a proper
5 initialization sequence by the enable circuit (9) and the
initialization sequence triggering of the enable signal
(CHIPREADY) is a command sequence conforming to the JEDEC
standard.

10 8. A semiconductor memory device according to any one of Claims 1 to 7,

c h a r a c t e r i z e d in that

the output drivers of the semiconductor memory device remain
15 latched during the switching-on operation until the enable
signal (CHIPREADY) generated by the enable circuit (9) is
issued.

9. A semiconductor memory device according to any one of Claims
20 1 to 8,

c h a r a c t e r i z e d in that

the proper initialization sequence, which causes the
triggering of an enable signal (CHIPREADY), includes the
following chronologically successive command sequences:

25 (a) first PRE, second ARF, third MRS; or

(b) first PRE, second MRS, third ARF; or

(c) first MRS, second PRE, or third ARF,

wherein the abbreviations denote the following commands:

PRE = the preparation command for word line activation

30 (PRECHARGE),

ARF = the refresh command (AUTOREFRESH), and

MRS = load configuration register command (MODE-REGISTER-
SET).

10. A method for initializing a dynamic semiconductor memory
device of a random-access type (DRAM/

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SDRAM) by means of an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components which initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device,

wherein the initialization circuit supplies an enable signal (CHIP-READY) by means of an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device after identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device, which enable signal causes the unlatching of the control circuit (13) provided for the proper operation of the semiconductor memory device,

c h a r a c t e r i z e d i n t h a t

the command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRECHARGE), and/or the refresh command (AUTOREFRESH), and/or the load configuration register command (MODE-REGISTER-SET).

11. A method according to Claim 10,

c h a r a c t e r i z e d i n t h a t

the output drivers of the semiconductor memory device remain latched during the switching-on operation until the enable signal (CHIPREADY) generated by the enable circuit (9) is issued.



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[Stamp:]

EPO - Munich
42
30 Jan. 2006

European Patent Office

80298 Munich, Germany

Your Reference

Our reference:
1998P1989 EP N

Munich,
January 30, 2006
(CL/HA)

EP Patent Claim No. 99113048.5-2210

Applicant: Infineon Technologies AG

Communication dated September 28, 2005

In response to the above communication, replacement pages 1, 1a, 3, 4 and 9 to 12 have been filed instead of the original pages 1, 3, 4 and 9 to 13 of the application. Also attached is a working copy in which the changes made are underlined.

The feature of the original Claim 2 was included in Claim 1, which, according to the communication, the Office considers to be grantable. Accordingly, the feature of original Claim 12, which corresponds to original Claim 2, was included in subsidiary Claim 11 (10 in the new numbering). The original Claim 14 was deleted.

The description has been adapted accordingly. The relevant prior art is cited on page 1, line 25.

In the communication, reference was made to Claims 15 to 20 in Section 6. However, the application filed contained only Patent Claims 1 to 14. Thus, apart from the set of claims now presented with 11 patent claims, there are no further patent claims in the proceedings.

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It should now be possible to issue the communication according to R. 51 (4)

EPPING HERMANN FISCHER
Patentanwaltsgesellschaft mbH

[Signature]
Volker Fischer
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Attachments
Exchange pages 1, 1a, 3,
4, 9-12
Working copy



The examination is based on the **following application documents**:

Description, pages

1-8 original version

Claims, nos.

1-14 original version

Drawings, sheets

1/3-3/3 original version

1. The following documents D1-D2 cited in the search report are cited in this communication; the numbering will be maintained in the subsequent proceedings:

D1: JP 09 106668 A (SAMSUNG ELECTRON CO LTD) 22 Apr. 97 (1997-04-22).

D2: EP-A-0 797 207 (FUJITSU LTD) Sep 24, 1997 (1997-09-24).

Document D1 discloses (references in parentheses are to this document): a dynamic semiconductor memory device of a random access type (DRAM/SDRAM) having an initialization circuit which controls the switching-on operation of the semiconductor memory device (Fig. 3) and of its circuit components (Fig. 3 references 12, 14, 16, 46 and 56), and which supplies a supply voltage stable signal (VCCH) once the supply voltage (VCC) has been stabilized after the switching-on of the semiconductor memory device, characterized in that the initialization circuit has an enable circuit (46) which is assigned to the supply voltage stable signal (VCCH) and to further command signals (DSF, RASB, CASB) externally applied to the semiconductor memory device, which, after the recognition of a predetermined proper initialization sequence (column 3 lines 19-22 "SET in response to a sequence of reset control signals DSF, RASB, and CASB," and column 2 line 28) of the command signals (DSF, RASB, and CAB) applied to the semiconductor memory device provide an enable signal (output RST) which causes the unlatching (column 2 line 26-28 "initialization signal being activated") of the control circuit provided for the proper operation of the semiconductor memory device (Connected to output RST, column 3 line 21 "circuit within the memory device").



The subject-matter of Claim 1 is therefore not new (Articles 54(1) and 54(2) EPC).

2. Concerning Claim 3, the characterizing features of the use of a bistable multivibrator stage are also disclosed in D1 (Figure 3: bistable multivibrator stage 20-22 and 34-36; applied command signals phi.DSF phi.R, phi.C; supply voltage stable signal phi.SVSS connected to 20; a signal phi.INIT derived therefrom; enable signal phi.RST).
3. The invention according to Claims 2 and 10 appears to be new and inventive, thereby fulfilling the provisions of Article 52(1) EPC.
4. The features of dependent Claims 4-7 are either known from D1 or are obvious.
5. From D2 (column 3, lines 25-40), the feature that the output drivers remain latched until the enable signal provided by the enable circuit is issued to prevent unwanted activation of output transistors is known. A skilled person would use such an enable circuit in the device known from D1 to achieve the same advantage. Consequently, this Claim 9 does not satisfy the requirements of Articles 52(1) and 56 EPC and is accordingly not allowable.
6. Claims 16-20 essentially define the features of Claims 1-15 in method terms, therefore the same objections apply to Claims 16-20 as to Claims 1-15 (see the points above).
7. If the applicant intends to pursue this application accordingly, the following points should also be noted in addition to those mentioned above:
 - a. In revising the application, particularly the introductory part and the description of the object or advantages of the invention, care should be taken to ensure that the subject matter does not go beyond the content of the application as originally filed (cf. Article (123(2) EPC). To facilitate examination of amended application documents in view of Article 123(2) EPC, the applicant is requested to indicate clearly the amendments made,

**Communication/Minutes (Annex)**Date
09/28/2005**Communication/Minutes (Annex)**Sheet
3**Communication/Minutes (Annex)**Application No.:
99 113 048.5

- whether by addition, substitution or deletion, and to indicate the passages in the application as originally filed on which these amendments are based.
- b. To meet the requirements of Rule 27(1)(b) EPC, document D1 must be cited in the description and its relevant contents should be briefly outlined.
 - c. The description must be made consistent with the new claims to be filed, cf. Rule 27(1)(c) EPC.



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(Formalities and other matters)

[Bar Code]

Application No. 99 113 048.5 - 2210	Reference GR 98P1989E	Date 09/28/2005
Applicant Infineon Technologies AG		

Communication under Article 96(2) EPC

Examination of the above application has revealed that it does not meet the requirements of the European Patent Convention for the reasons given in the enclosed documents. If the above deficiencies are not remedied, the application may be refused under Article 97(1) EPC.

You are requested to submit your comments within a period

of 4 months

from the date of notification of this communication and to remedy the deficiencies indicated, insofar as they can be remedied. The time limit is calculated according to the provisions of Rules 78(2), 83(2) and (4) EPC.

Amendments to the description, claims and drawings, if any, shall be filed in **one copy** on separate sheets (Rule 36(1) EPC) within the above-mentioned time limit.

Failure to reply to this invitation in due time will result in the European application being deemed withdrawn (Article 96(3) EPC).

[Seal:]



European Patent Office

Operti, A
Examinations Officer
for the Examining Division

Enclosures: 3 page/s Reasons (Form 2906)



RELEVANT DOCUMENTS			
Category	Identification of the document with indication, if necessary, of the relevant parts	Regarding Claim	CLASSIFICATION OF APPLICATION (Int.Cl.7)
X	JP 09 106668 A (SAMSUNG ELECTRON CO LTD) April 22, 1997 (1997-04-22)	1,3,4, 12,13	G11C7/00
Y	& US 5 774 402 A (LEE CHEOL-HA) June 30, 1998 (1998-06-30) * The entire document *	9	
Y	EP 0 797 207 A (FUJITSU LTD) September 24, 1997 (1997-09-24) * Column 3, lines 25-39; Figures 1-4 *	9	
			RESEARCHED AREAS (Int.Cl.7)
			G11C
This search report was drawn up for all patent claims			
Search location THE HAGUE		Date of completion of search October 28, 1999	Examiner Czarik, D
CATEGORY OF DOCUMENTS CITED X: Of particular importance considered alone Y: Of particular importance in conjunction with another publication of the same category A: Technological background O: Non-written disclosure P: Intermediate literature		T: Theories or principles underlying the invention E: Earlier patent document, but published on or after the application date D: Document cited in the application L: Document cited for other reasons &: Member of the same patent family, corresponding document	

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EPO FORM 1503 03.82 (P04C03)

Patent claims

1. A dynamic semiconductor memory device of a random-access type (DRAM/SDRAM) having an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components and which supplies a supply voltage stable signal (POWERON) once the supply voltage has been stabilized after the switching-on of the semiconductor memory device,

characterized in that

the initialization circuit has an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device which enable circuit supplies an enable signal (CHIPREADY) after the recognition of a predetermined proper initialization sequence of the command signals (PRE, ARF, MRS) applied to the semiconductor memory device which enable signal causes the unlatching of a control circuit (13) provided for the proper operation of the semiconductor memory device.

2. A semiconductor memory device according to Claim 1,

characterized in that

the command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRE-CHARGE), and/or the refresh command (AUTOREFRESH), and/or the load configuration register command (MODE-REGISTER-SET).

10

3. A semiconductor memory device according to Claim 1 or 2, characterized in that

the enable circuit (9) has at least one bistable multivibrator stage (14, 15, 16) with a set input (S) to which a command signal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET) is applied, a reset input (R) to which the supply voltage stable signal (POWERON) or a signal derived therefrom or a linked signal is applied and with an output (Q) at which the enable signal (CHIPREADY) (9) is derived.

10

4. A semiconductor memory device according to Claim 3,

characterized in that

the enable circuit (9) has a number of bistable multivibrator stages (14, 15, 16) each associated to a command signal (PRE,

15 ARF, MRS).

5. A semiconductor memory device according to Claims 3 or 4,

characterized in that

the output (Q) of at least one of the bistable multivibrator stages (14) is fed to a reset input of a further multivibrator stage (15).

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6. A semiconductor memory device according any one of Claims 3 to 5,

characterized in that,

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in one of the bistable multivibrator stages (15), the supply voltage stable signal (POWERON) and the signal output from the output (Q) of the further multivibrator stage (14) are fed to the reset input (R) of the multivibrator stage (15) after having been logically combined by a gate (17).

30

7. A semiconductor memory device according to any one of Claims 3 to 6,

c h a r a c t e r i z e d in that

the bistable multivibrator stage (14, 15, 16) is formed in each case by an RS multivibrator constructed of at least two NOR or NAND gates (14A, 14B, 15A, 17, 16A, 16B).

8. A semiconductor memory device according to any one of Claims 2 to 7,

c h a r a c t e r i z e d in that

the initialization sequence recognized as a proper initialization sequence by the enable circuit (9) and the initialization sequence triggering of the enable signal (CHIPREADY) is a command sequence conforming to the JEDEC standard.

9. A semiconductor memory device according to any one of Claims 1 to 8,

c h a r a c t e r i z e d in that

the output drivers of the semiconductor memory device remain latched during the switching-on operation until the enable signal (CHIPREADY) generated by the enable circuit (9) is issued.

10. A semiconductor memory device according to any one of Claims 1 to 9,

c h a r a c t e r i z e d in that

the proper initialization sequence, which causes the triggering of an enable signal (CHIPREADY), includes the following chronologically successive command sequences:

(a) first PRE, second ARF, third MRS; or

(b) first PRE, second MRS, third ARF; or

(c) first MRS, second PRE, or third ARF,

wherein the abbreviations denote the following commands:

PRE = the preparation command for word line activation

(PRECHARGE),

ARF = the refresh command (AUTOREFRESH), and

MRS = load configuration register command (MODE-REGISTER-SET).

5

11. A method for initializing a dynamic semiconductor memory device of a random-access type (DRAM/ SDRAM) by means of an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components and supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device,

10

c h a r a c t e r i z e d in that

15

the initialization circuit supplies an enable signal (CHIP-READY) by means of an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device after identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device, which causes the unlatching of the control circuit (13) provided for the proper operation of the semiconductor memory device.

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12. A method according to Claim 11,

c h a r a c t e r i z e d in that

the command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRECHARGE), and/or the refresh command (AUTOREFRESH), and/or the load configuration register command (MODE-REGISTER-SET).

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13. A method according to Claim 11 or 12,

c h a r a c t e r i z e d in that

the output drivers of the semiconductor memory device remain

latched during the switching-on operation until the enable

5 signal (CHIPREADY) generated by the enable circuit (9) is
issued.

14. The use of an enable circuit (9) providing an enable signal

10 (CHIPREADY) for controlling the switching-on operation of a

dynamic semiconductor memory device of a selective access type

(DRAM/SDRAM) according to any one of Claims 1 to 10.

Request for the granting of a European patent

User's reference: GR 98P1989E
System ID no: 111111 36284,3315701968
Application No:

6	Designation of Contracting States				
6-1	All Contracting States of the EPC which are members of the EPC at the date of filing of this application are designated herein.	✓			
6-2	It is requested that notifications under Rule 85a(1) and Rule 69(1) be waived for the Contracting States not marked under 6.4.	✓			
6-3	If an automatic debit order has been issued (Box 14), it is requested that designation fees be debited only for the Contracting States marked under 6.4 when the basic period under Article 79(2) EPC expires.	✓			
6-4	The applicant currently intends to pay designation fees for the following states:	DE FR GB IE IT			
7	Extension of the European patent				
7-1	This application is deemed to be a request to extend the European patent application and the European patent granted thereupon to all non-contracting states to the EPC with which "extension agreements" exist on the date of filing. However, the extension will only become effective if the prescribed extension fee is paid.	✓			
7-2	The applicant currently intends to pay extension fees for the following states:				
8	Declaration of priority	State	Application date	Type	Application number
8-1	Priority 01 [handwritten:] DE	DE	June 30, 1998	ap	19829287.2
9	Deposit of biological material The invention relates to or uses biological material deposited under Rule 28 EPC.				
10	Nucleotide and amino acid sequences				
11	Forms	Details:	Electronic file:		
11-1	Application	Printed	as EPF1001.RTF		
11-2	Fee payment				
11-3	EASY match	Printed	as EPCLIST.RTF		
11-4	Verification protocol				
11-5	Submission Protocol		as EPL-SUB.RTF		
12	Technical documentation	Details:	Electronic file:		
12-1	Description	Attached, 8 p.	98p1989b.rtf		
12-2	Patent claim	Attached, 5 p.; 14 claims	98p1989a.rtf		
12-3	Drawings	Attached, 3 p.; 4 Fig.			
12-4	Abstract	Attached, 1 p.; Fig. 1	98p1989z.rtf		
13	Additional documentation	Details:	Electronic file:		
13-1	1. priority	attached; DE 19829287.2			

User's reference: **GR 98P1989E**
 System ID no: **111111 36284,3315701968**
 Application No:

14	Payment			
14-1	Payment method	Separate (collective) debit order ✓		
14-2	The fees and expenses indicated under the heading "Fees" are paid within one month after the application date by a separate (collective) debit order from the current account at the EPO. Currency: DEM Deutsche Mark Current account no.: 28000003 Account holder: Siemens AG Refund/Repayment Any refunds to current account at the EPO 28000003			
15	Fees	Factor applied	Fee schedule	Amount to be paid
15-1	001 Application fee	1	248.39	248,39
15-2	002 Search fee	1	1,699.62	1,699.62
15-3	015 Claims fee	4	78.23	312.92
	Total amount:		DEM	2,260.93
16	Notes			
17-1	Signature: Signed by: Margraf, Roland in the capacity of: Siemens Aktiengesellschaft (Employee)	[Stamp:] For Payment [handwritten:] <i>on behalf of [Signature]</i>		

Receipt for documents

(Checklist of enclosed documents)

6

Receipt of the documents indicated below is hereby acknowledged.

If this receipt is issued by the European Patent Office and the European patent claim was filed with a national authority it serves as a communication under Rule 24(4) (see Section RENA). **Once the communication under Rule 24(4) has been received, all further documents relating to the application must be sent directly to the European Patent Office.**

[handwritten:]

Siemens AG

001120.5

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Application No.		99113048.5		
Date of receipt (Rule 24(2))	DREC	06 / 30 99		
Applicant's/ Representative's ref	AREF	GR 98 P 1989 E		
Only after filing of the application with a national authority.				
Date of receipt at EPO (Rule 24(4))	RENA			
A. Application documents and priority documents	47	Number of copies	Number of sheets in each copy	Total number of figures
1 Description		1	8	
2 Claim(s)		1	5	
3 Drawing(s) DRAW 1 #		3	3	
4 Abstract		1	1	
5 Translation of the application documents				
6 Priority documents		1		
7 Translation of priority documents				
8 The application as filed is accompanied by the items below:	48			
1 Specific authorization				
2 General authorization				
3 Designation of inventor				
4 Earlier search report				
5 Voucher for the settlement of fees (EPO form 1010)				
6 Check (not when filing with national authorities)				
7 Data carrier for sequence listing SEQL (4)				
8 Additional sheet				
9 Other (please specify here)				
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* [Illegible text]

EASY Declaration of Conformity

User's reference: GR 98P1989E
System ID no: 111111 36284,3315701968
Application No: 99113048 . 5

It is hereby declared that the data stored on the data carrier (application diskette) corresponds to the printed and submitted application documents.

Date: 30 JUN 1999

[handwritten:]
on behalf of [Signature]

Signed **Margraf, Roland**
by:
in the capacity of: **Siemens Aktiengesellschaft**
(Employee)



January 23, 2023

Certification

Welocalize Translations

TRANSLATOR'S DECLARATION:

I, James E. LaRue, am fluent in both the German and English languages. I have translated the file titled "'589 EPO PH Excerpts" from German to English. I hereby certify that the translation is accurate and complete to the best of my judgment and ability. I understand that willful false statements and the like are punishable by fine or imprisonment, or both, pursuant to 18 U.S.C. § 1001.

I certify under penalty of perjury under the laws of the United States that the foregoing is true and correct.

A handwritten signature in black ink that reads "JE LaRue".

James E. LaRue

Project Number: BBLLP_2205_P0008

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