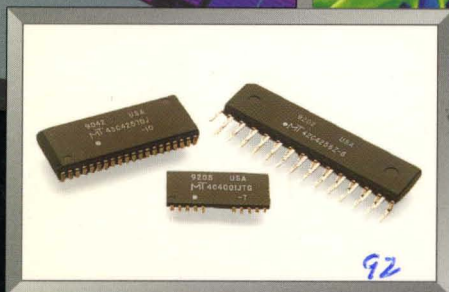
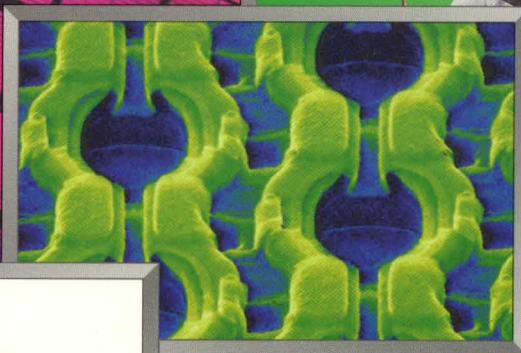
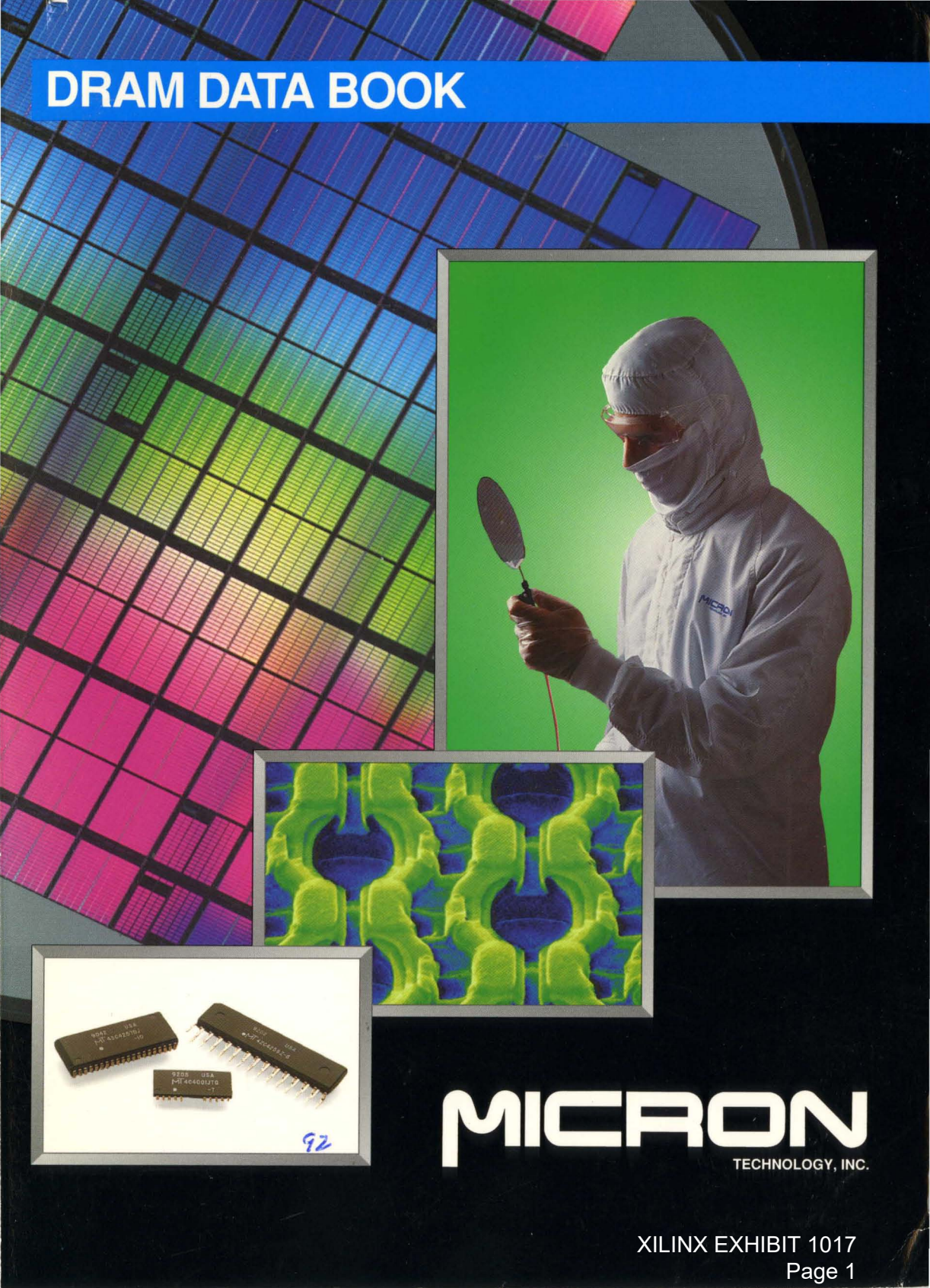


# DRAM DATA BOOK



**MICRON**  
TECHNOLOGY, INC.

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# DRAM DATA BOOK

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### **ABOUT THE COVER:**

Front — Clockwise from left, 1) Micron's 16 Meg DRAM wafer; 2) More than 4,000 Micron team members give painstaking attention to every step of the production process; 3) Scanning electron microscope (SEM) photograph of Micron's DRAM mini-stack process; and 4) Micron's Triple Port, Dual Port and 4 Meg DRAMs in SOJ, ZIP and TSOP packages.

Back — Micron's Boise, Idaho, corporate headquarters including three fabrication facilities.

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Dear Customer:

Micron Technology, Inc., is dedicated to the design, manufacture and marketing of high quality, highly reliable memory components. Our corporate mission is

*"To be a world class team  
developing advantages for our customers"*

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX™, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And, when you have a design or application question, you can get the answers you need from the source through one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

## ADVANTAGES

Micron Technology brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on your expectations, including JIT programs, made possible by ever-increasing product reliability.

## COMPONENT INTEGRATED CIRCUITS

Micron Technology entered the memory market 14 years ago first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and Triple Port DRAM), and a variety of other memory products.

As we bring progressive memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. In 1990, Micron's Triple Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

## SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Triple Port's tradition. From FIFOs to processors, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin IC DRAM Card. Ideal for laptop, notebook and other portable systems, Micron's IC DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.\*

## MILITARY CERTIFIED PRODUCTS

As one of the few manufacturers of military-grade memory in North America, Micron is proud to provide a documented source inspection from wafer start to finished product. We've earned recognition from U.S. and European space agencies as well as Joint Army/Naval

certification for both our NMOS and CMOS process technologies.

## DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare die products are available both in 6" wafers and wafflepacks.

## CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers added-value services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

## QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with every Micron shipment. That's because we believe that quality must be internalized consistently at every level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX™ intelligent burn-in and test system\*\* gives Micron a unique edge in product reliability.

\*See NOTE, page v.

\*\*For more information on Micron's AMBYX™, see Section 7.

## ABOUT THIS BOOK

### CONTENT

The 1992 *DRAM Data Book* from Micron Technology provides complete specifications on all standard DRAMs and DRAM modules as well as specialty and derivative products based on our DRAM production process.

The *DRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *SRAM Data Book* and *Military Data Book*.

### SECTION ORGANIZATION

Micron's 1992 *DRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The Data Book is organized into nine sections:

- **Sections 1–5:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 6:** Application/technical notes.
- **Section 7:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX™ intelligent burn-in and test system.\*
- **Section 8:** Packaging information.
- **Section 9:** Product ordering information, including a list of sales representatives and distributors worldwide.

## DATA SHEET DESIGNATIONS

| DATA SHEET MARKING | DEFINITION                                                                                                                                                                                                                                                                                  |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| "Advance"          | This data sheet contains initial descriptions of products still under development.                                                                                                                                                                                                          |
| "Preliminary"      | This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.                                                                                                                                                       |
| No Marking (Final) | This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur. |
| "New"              | This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the Data Book.                                                                                                                                                                                     |

**NOTE:** Micron's DRAM Data Book uses acronyms to refer to certain industry-standard-setting bodies. These are defined below for your reference:

EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council.

JEIDA—Japanese Electronics Industry Development Association.

PCMCIA—Personal Computer Memory Card International Association.

\*Micron's *Quality/Reliability Handbook* is available by calling (208) 368-3900.

### DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the DRAM section begins with the 1 Meg x 1 followed by 4 Meg x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

### DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either **Advance**, **Preliminary** or **Final**. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of the front page.

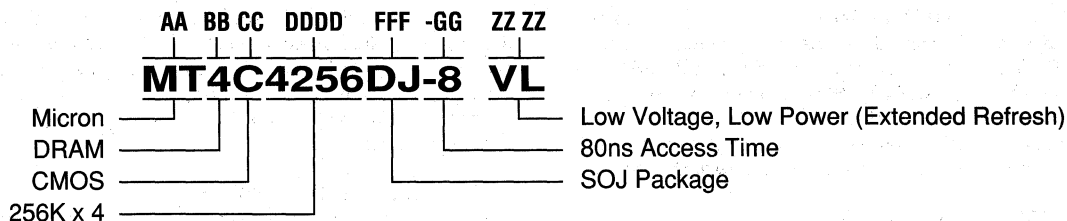
### SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact

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01-208-368-3410 (Intl.)

**EXPANDED COMPONENT NUMBERING SYSTEM**



**AA – PRODUCT LINE IDENTIFIER**

Component Product ..... MT

**BB – PRODUCT FAMILY**

DRAM ..... 4  
 DPDRAM ..... 42  
 TPDram ..... 43  
 SRAM ..... 5  
 FIFO ..... 52  
 Cache Data SRAM ..... 56  
 Synchronous SRAM ..... 58

**CC – PROCESS TECHNOLOGY**

CMOS ..... C  
 Low Voltage CMOS ..... LC

**DDDD – DEVICE NUMBER**

(Can be modified to indicate variations)

DRAM ..... Width, Density  
 DPDRAM ..... Width, Density  
 TPDram ..... Width, Density  
 SRAM ..... Total Bits, Width  
 CACHE ..... Density, Width  
 Latched SRAM ..... Total Bits, Width  
 FIFO ..... Width, Total Bits  
 Synchronous SRAM ..... Density, Width

**E – DEVICE VERSIONS**

(Alphabetic characters only; located between D and F when required)

JEDEC Test Mode (4 Meg DRAM) ..... J  
 Errata on Base Part ..... Q

**FFF – PACKAGE CODES**

PLASTIC  
 DIP ..... Blank  
 DIP (Wide Body) ..... W  
 ZIP ..... Z  
 LCC ..... EJ  
 SOP/SOIC ..... SG

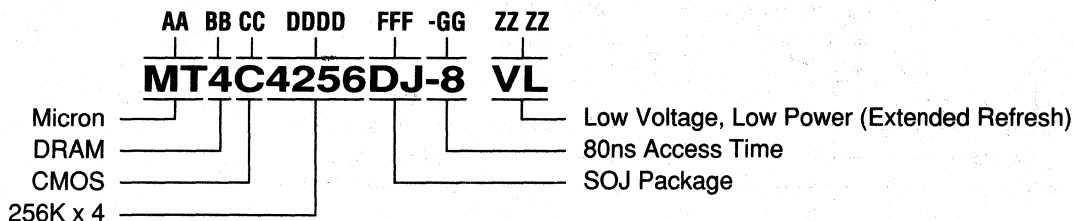
**FFF – PACKAGE CODES (continued)**

QFP ..... LG  
 TSOP (Type II) ..... TG  
 TSOP (Reversed) ..... RG  
 TSOP (Longer) ..... TL  
 SOJ ..... DJ  
 SOJ (Reversed) ..... DR  
 SOJ (Longer) ..... DL  
 DIE  
 Die ..... XDC  
 Wafer ..... XWC  
 Military Die ..... XD  
 Military Wafer ..... XW  
 Ceramic  
 DIP ..... C  
 DIP (Narrow Body) ..... CN  
 DIP (Wide Body) ..... CW  
 LCC ..... EC  
 LCC (Narrow Body) ..... ECN  
 LCC (Wide Body) ..... ECW  
 SOP/SOIC ..... CG  
 SOJ ..... DCJ  
 PGA ..... CA  
 FLAT PACK ..... F

**GG – ACCESS TIME**

-5 ..... 5ns or 50ns  
 -6 ..... 6ns or 60ns  
 -7 ..... 7ns or 70ns  
 -8 ..... 8ns or 80ns  
 -10 ..... 10ns or 100ns  
 -12 ..... 12ns or 120ns  
 -15 ..... 15ns or 150ns  
 -17 ..... 17ns  
 -20 ..... 20ns  
 -25 ..... 25ns  
 -35 ..... 35ns  
 -45 ..... 45ns  
 -50 (SRAM only) ..... 50ns  
 -53 ..... 53ns

**EXPANDED COMPONENT NUMBERING SYSTEM (continued)**



**GG – ACCESS TIME (continued)**

|                       |      |
|-----------------------|------|
| -55 .....             | 55ns |
| -70 (SRAM only) ..... | 70ns |

**ZZ ZZ – PROCESSING CODES**

(Multiple processing codes are separated by a space and are listed in hierarchical order).

**Example:**

A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:  
**V L IT**

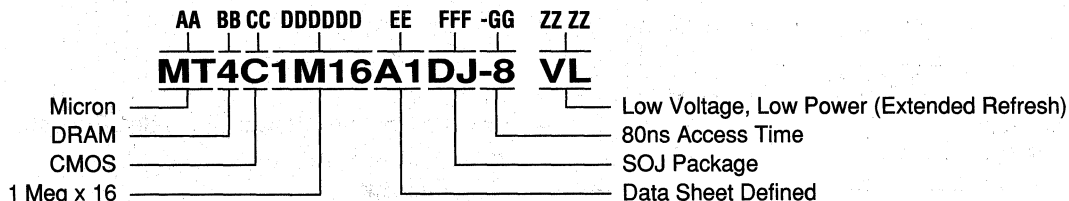
|                                                 |    |
|-------------------------------------------------|----|
| Interim .....                                   | I  |
| Low Voltage .....                               | V  |
| DRAMS                                           |    |
| Low Power (Extended Refresh) .....              | L  |
| Low Voltage, Low Power (Extended Refresh) ..... | VL |
| Low Power (Self Refresh) .....                  | S  |
| Low Voltage, Low Power (Self Refresh) .....     | VS |
| SRAMS                                           |    |
| Low Volt Data Retention .....                   | L  |
| Low Power .....                                 | P  |
| Low Power, Low Volt Data Retention .....        | LP |
| Low Voltage, Low Power .....                    | VP |

**ZZ ZZ – PROCESSING CODES (continued)**

|                                                       |       |
|-------------------------------------------------------|-------|
| Low Voltage, Low Volt Data Retention .....            | VL    |
| Low Voltage, Low Volt Data Retention, Low Power ..... | VB    |
| EPI Wafer .....                                       | E     |
| Commercial Testing                                    |       |
| 0°C to +70°C .....                                    | Blank |
| -40°C to +85°C .....                                  | IT    |
| -40°C to +125°C .....                                 | AT    |
| -55°C to +125°C .....                                 | XT    |
| MIL-STD-883C Testing                                  |       |
| -55°C to +125°C .....                                 | 883C  |
| -55°C to +110°C (DRAMs) .....                         | 883C  |
| 0°C to +70°C .....                                    | M070  |
| Special Processing                                    |       |
| Engineering Sample .....                              | ES    |
| Mechanical Sample .....                               | MS    |
| Sample Kit* .....                                     | SK    |
| Tape and Reel* .....                                  | TR    |
| Bar Code* .....                                       | BC    |

\* Used in device order codes; this code is not marked on device.

**NEW COMPONENT NUMBERING SYSTEM**



**AA – PRODUCT LINE IDENTIFIER**

Component Product ..... MT

**BB – PRODUCT FAMILY**

DRAM ..... 4  
 DPDRAM ..... 42  
 TPD RAM ..... 43  
 Synchronous DRAM ..... 48  
 SRAM ..... 5  
 FIFO ..... 52  
 Latched SRAM ..... 56  
 Synchronous SRAM ..... 58

**CC – PROCESS TECHNOLOGY**

CMOS ..... C  
 Low Voltage CMOS ..... LC

**DDDDDD – DEVICE NUMBER**

Depth, Width

**Example:**

**1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory**

No Letter ..... Bits  
 K ..... Kilobits  
 M ..... Megabits  
 G ..... Gigabits

**EE – DEVICE VERSIONS**

(The first character is an alphabetic character only; the second character is a numeric character only.)  
 Specified by individual data sheet

**FFF – PACKAGE CODES**

Plastic  
 DIP ..... Blank  
 DIP (Wide Body) ..... W  
 ZIP ..... Z  
 LCC ..... EJ  
 SOP/SOIC ..... SG

**FFF – PACKAGE CODES (continued)**

QFP ..... LG  
 TSOP (Type II) ..... TG  
 TSOP (Reversed) ..... RG  
 TSOP (Longer) ..... TL  
 SOJ ..... DJ  
 SOJ (Reversed) ..... DR  
 SOJ (Longer) ..... DL

**DIE**

Die ..... XDC  
 Wafer ..... XWC  
 Military Die ..... XD  
 Military Wafer ..... XW

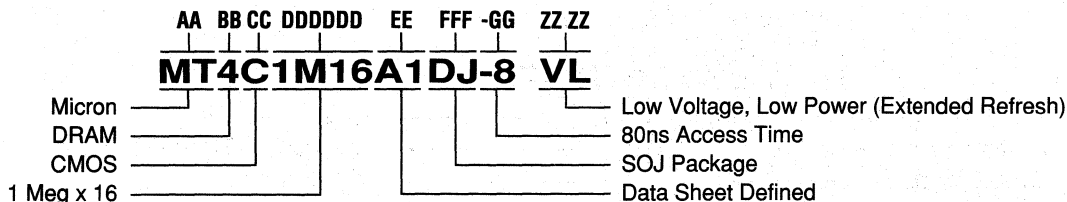
**CERAMIC**

DIP ..... C  
 DIP (Narrow Body) ..... CN  
 DIP (Wide Body) ..... CW  
 LCC (Narrow Body) ..... ECN  
 LCC ..... EC  
 LCC (Wide Body) ..... ECW  
 SOP/SOIC ..... CG  
 SOJ ..... DCJ  
 PGA ..... CA  
 FLAT PACK ..... F

**GG – ACCESS TIME**

-5 ..... 5ns or 50ns  
 -6 ..... 6ns or 60ns  
 -7 ..... 7ns or 70ns  
 -8 ..... 8ns or 80ns  
 -10 ..... 10ns or 100ns  
 -12 ..... 12ns or 120ns  
 -15 ..... 15ns or 150ns  
 -17 ..... 17ns  
 -20 ..... 20ns  
 -25 ..... 25ns  
 -35 ..... 35ns  
 -45 ..... 45ns  
 -50 (SRAM only) ..... 50ns

**NEW COMPONENT NUMBERING SYSTEM (continued)**



**GG – ACCESS TIME (continued)**

|                       |      |
|-----------------------|------|
| -53 .....             | 53ns |
| -55 .....             | 55ns |
| -70 (SRAM only) ..... | 70ns |

**ZZ ZZ – PROCESSING CODES**

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

**Example:**

**A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as:**  
**V L IT**

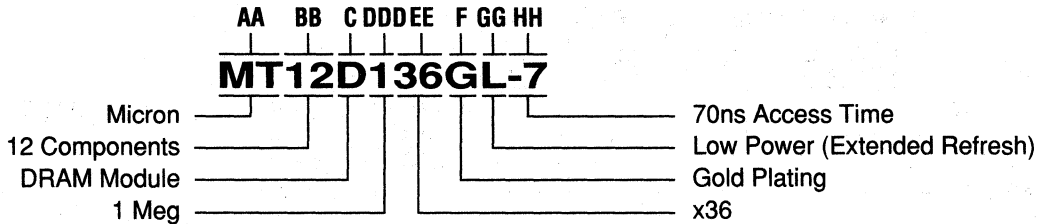
|                                                 |    |
|-------------------------------------------------|----|
| Interim .....                                   | I  |
| Low Voltage .....                               | V  |
| DRAMs                                           |    |
| Low Power (Extended Refresh) .....              | L  |
| Low Voltage, Low Power (Extended Refresh) ..... | VL |
| Low Power (Self Refresh) .....                  | S  |
| Low Voltage, Low Power (Self Refresh) .....     | VS |
| SRAMs                                           |    |
| Low Volt Data Retention .....                   | L  |
| Low Power .....                                 | P  |
| Low Power, Low Volt Data Retention .....        | LP |
| Low Voltage, Low Power .....                    | VP |

**ZZ ZZ – PROCESSING CODES (continued)**

|                                            |       |
|--------------------------------------------|-------|
| Low Voltage, Low Volt Data Retention ..... | VL    |
| Low Voltage, Low Volt Data Retention,      |       |
| Low Power .....                            | VB    |
| EPI Wafer .....                            | E     |
| Commercial Testing                         |       |
| 0°C to +70°C .....                         | Blank |
| -40°C to +85°C .....                       | IT    |
| -40°C to +125°C .....                      | AT    |
| -55°C to +125°C .....                      | XT    |
| MIL-STD-883C Testing                       |       |
| -55°C to +125°C .....                      | 883C  |
| -55°C to +110°C (DRAMs) .....              | 883C  |
| 0°C to +70°C .....                         | M070  |
| Special Processing                         |       |
| Engineering Sample .....                   | ES    |
| Mechanical Sample .....                    | MS    |
| Sample Kit* .....                          | SK    |
| Tape and Reel* .....                       | TR    |
| Bar Code* .....                            | BC    |

\* Used in device order codes; this code is not marked on device.

**MODULE NUMBERING SYSTEM**



**AA – PRODUCT LINE IDENTIFIER**

Micron Technology Component Product ..... MT

**BB – NUMBER OF MEMORY COMPONENTS**

**C – RAM FAMILY**

SRAM ..... S  
DRAM ..... D

**DDD – DEPTH**

**EE – WIDTH**

**F – PACKAGE CODE**

DIP ..... D  
Gold Plate ..... G  
ZIP ..... Z  
SIP ..... N  
SIMM ..... M

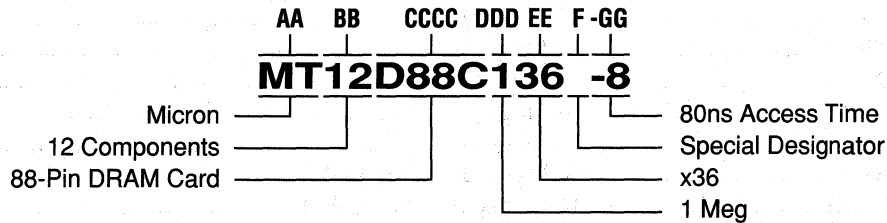
**GG – SPECIAL DESIGNATOR**

Low Power ..... L

**HH – ACCESS TIME**

-10 ..... 10ns or 100ns  
-15 ..... 15ns  
-20 ..... 20ns  
-25 ..... 25ns  
-30 ..... 30ns  
-35 ..... 35ns  
-45 ..... 45ns  
-6 ..... 60ns  
-7 ..... 70ns  
-8 ..... 80ns

**IC DRAM CARD NUMBERING SYSTEM**



**AA – PRODUCT LINE IDENTIFIER**

Micron Technology Component Product ..... MT

**BB – NUMBER OF MEMORY COMPONENTS**

**CCCC – DRAM CARD DESIGNATOR AND PIN COUNT**

88-Pin DRAM Card ..... D88C  
60-Pin DRAM Card ..... D60C

**DDD – DEPTH**

**EE – WIDTH**

**F – SPECIAL DESIGNATOR**

3.3 Volts ..... V

**G – ACCESS TIME**

-5 ..... 50ns  
-6 ..... 60ns  
-7 ..... 70ns  
-8 ..... 80ns

**DYNAMIC RAMS**
**PAGE**

|                   |            |                   |       |
|-------------------|------------|-------------------|-------|
| MT4C1024 .....    | 1 Meg x 1  | FP .....          | 1-1   |
| MT4C1024 L .....  | 1 Meg x 1  | FP, LP .....      | 1-13  |
| MT4C1026 .....    | 1 Meg x 1  | SC .....          | 1-25  |
| MT4C1004J .....   | 4 Meg x 1  | FP .....          | 1-37  |
| MT4C1004J L ..... | 4 Meg x 1  | FP, LP .....      | 1-49  |
| MT4C1006J .....   | 4 Meg x 1  | SC .....          | 1-61  |
| MT4C16M1A1 .....  | 16 Meg x 1 | FP, 4KR .....     | 1-73  |
| MT4LC16M1A1 ..... | 16 Meg x 1 | FP, 4KR, LV ..... | 1-73  |
| MT4C16M1D1 .....  | 16 Meg x 1 | SC, 4KR .....     | 1-85  |
| MT4C4256 .....    | 256K x 4   | FP .....          | 1-87  |
| MT4C4256 L .....  | 256K x 4   | FP, LP .....      | 1-97  |
| MT4C4256 VL ..... | 256K x 4   | FP, LP, LV .....  | 1-109 |
| MT4C4258 .....    | 256K x 4   | SC .....          | 1-121 |
| MT4C4001J .....   | 1 Meg x 4  | FP .....          | 1-133 |
| MT4C4001J L ..... | 1 Meg x 4  | FP, LP .....      | 1-145 |
| MT4C4003J .....   | 1 Meg x 4  | SC .....          | 1-157 |
| MT4C4004J .....   | 1 Meg x 4  | FP, QCP .....     | 1-169 |
| MT4C4M4A1 .....   | 4 Meg x 4  | FP, 4KR .....     | 1-183 |
| MT4C4M4B1 .....   | 4 Meg x 4  | FP, 2KR .....     | 1-183 |
| MT4LC4M4A1 .....  | 4 Meg x 4  | FP, 4KR, LV ..... | 1-195 |
| MT4LC4M4B1 .....  | 4 Meg x 4  | FP, 2KR, LV ..... | 1-195 |
| MT4C4M4D1 .....   | 4 Meg x 4  | SC, 4KR .....     | 1-207 |

FP ..... FAST PAGE MODE  
 SC ..... STATIC COLUMN MODE  
 LP ..... Low Power, Extended Refresh  
 QCP ..... Quad CAS Parity

LV ..... Low Voltage  
 2KR ..... 2,048 Row Refresh  
 4KR ..... 4,096 Row Refresh

**WIDE DRAMS**
**PAGE**

|                      |           |                           |      |
|----------------------|-----------|---------------------------|------|
| MT4C8512 .....       | 512K x 8  | FP .....                  | 2-1  |
| MT4C8513 .....       | 512K x 8  | FP, WPB .....             | 2-1  |
| MT4C8512 L .....     | 512K x 8  | FP, LP .....              | 2-15 |
| MT4C8513 L .....     | 512K x 8  | FP, WPB, LP .....         | 2-15 |
| MT4(L)C2M8A1 .....   | 2 Meg x 8 | FP, 4KR .....             | 2-31 |
| MT4(L)C2M8A2 .....   | 2 Meg x 8 | FP, 4KR, WPB .....        | 2-31 |
| MT4(L)C2M8B1 .....   | 2 Meg x 8 | FP, 2KR .....             | 2-47 |
| MT4(L)C2M8B2 .....   | 2 Meg x 8 | FP, 2KR, WPB .....        | 2-47 |
| MT4(L)C2M8A1 S ..... | 2 Meg x 8 | FP, 4KR, S, LP .....      | 2-63 |
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FP ..... FAST PAGE MODE  
 LP ..... Low Power, Extended Refresh  
 DW ..... Dual WE  
 2KR ..... 2,048 Refresh  
 S ..... Self Refresh

SC ..... STATIC COLUMN  
 WPB ..... WRITE PER BIT  
 DC ..... Dual CAS  
 4KR ..... 4,096 Refresh  
 ASY ..... Asymmetrical Addressing

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LP ..... Low Power  
**NOTE:** All modules include FAST PAGE MODE cycle.

LV ..... Low Voltage  
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FP ..... FAST PAGE MODE  
 LP ..... Low Power, Extended Refresh

BW ..... BLOCK WRITE

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**DRAM PRODUCT SELECTION GUIDE**

| Memory Configuration | Optional Access Cycle | Part Number | Access Time (ns) | Typical Power Dissipation |        | Package and Number of Pins |     |     |      | Page  |
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|                      |                       |             |                  | Standby                   | Active | PDIP                       | ZIP | SOJ | TSOP |       |
| 1 Meg x 1            | FP                    | MT4C1024    | 60, 70, 80       | 3mW                       | 175mW  | 18                         | 20  | 20  | 20   | 1-1   |
| 1 Meg x 1            | FP, LP                | MT4C1024 L  | 70, 80, 100      | 0.3mW                     | 150mW  | 18                         | 20  | 20  | 20   | 1-13  |
| 1 Meg x 1            | SC                    | MT4C1026    | 70, 80           | 3mW                       | 175mW  | 18                         | 20  | 20  | -    | 1-25  |
| 4 Meg x 1            | FP                    | MT4C1004J   | 60, 70, 80       | 3mW                       | 225mW  | -                          | 20  | 20  | 20   | 1-37  |
| 4 Meg x 1            | FP, LP                | MT4C1004J L | 60, 70, 80       | 1mW                       | 225mW  | -                          | 20  | 20  | 20   | 1-49  |
| 4 Meg x 1            | SC                    | MT4C1006J   | 70, 80           | 3mW                       | 225mW  | -                          | 20  | 20  | -    | 1-61  |
| 16 Meg x 1           | FP, 4KR               | MT4C16M1A1  | 60, 70, 80       | 3mW                       | 325mW  | -                          | -   | 24  | 24   | 1-73  |
| 16 Meg x 1           | FP, 4KR, LV           | MT4LC16M1A1 | 60, 70, 80       | 1mW                       | 125mW  | -                          | -   | 24  | 24   | 1-73  |
| 16 Meg x 1           | SC, 4KR               | MT4C16M1D1  | 60, 70, 80       | 3mW                       | 330mW  | -                          | -   | 24  | -    | 1-85  |
| 256K x 4             | FP                    | MT4C4256    | 60, 70, 80       | 3mW                       | 175mW  | 20                         | 20  | 20  | 20   | 1-87  |
| 256K x 4             | FP, LP                | MT4C4256 L  | 70, 80, 100      | 0.3mW                     | 150mW  | 20                         | 20  | 20  | 20   | 1-97  |
| 256K x 4             | FP, LP, LV            | MT4C4256 VL | 100, 120         | 0.1mW                     | 100mW  | -                          | 20  | 20  | 20   | 1-109 |
| 256K x 4             | SC                    | MT4C4258    | 70, 80, 100      | 3mW                       | 175mW  | 20                         | 20  | 20  | -    | 1-121 |
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| 4 Meg x 4            | FP, 4KR               | MT4C4M4A1   | 60, 70, 80       | 3mW                       | 325mW  | -                          | -   | 24  | 24   | 1-183 |
| 4 Meg x 4            | FP, 2KR               | MT4C4M4B1   | 60, 70, 80       | 3mW                       | 400mW  | -                          | -   | 24  | 24   | 1-183 |
| 4 Meg x 4            | FP, 4KR, LV           | MT4LC4M4A1  | 60, 70, 80       | 1mW                       | 125mW  | -                          | -   | 24  | 24   | 1-195 |
| 4 Meg x 4            | FP, 2KR, LV           | MT4LC4M4B1  | 60, 70, 80       | 1mW                       | 175mW  | -                          | -   | 24  | 24   | 1-195 |
| 4 Meg x 4            | SC, 4KR               | MT4C4M4D1   | 60, 70, 80       | 3mW                       | 325mW  | -                          | -   | 24  | -    | 1-207 |

FP = Fast Page Mode, SC = Static Column Mode, LP = Low Power, Extended Refresh; QCP = Quad CAS Parity,  
 LV = Low Voltage, 2KR = 2,048 Row Refresh, 4KR = 4,096 Row Refresh

**WIDE DRAM PRODUCT SELECTION GUIDE**

| Memory Configuration | Optional Access Cycle | Part Number*    | Access Time (ns) | Typical Power Dissipation |        | Package/Number of Pins |        |        | Page  |
|----------------------|-----------------------|-----------------|------------------|---------------------------|--------|------------------------|--------|--------|-------|
|                      |                       |                 |                  | Standby                   | Active | ZIP                    | SOJ    | TSOP   |       |
| 512K x 8             | FP                    | MT4C8512        | 70, 80, 100      | 3mW                       | 350mW  | 28                     | 28     | 28     | 2-1   |
| 512K x 8             | FP, WPB               | MT4C8513        | 70, 80, 100      | 3mW                       | 350mW  | 28                     | 28     | 28     | 2-1   |
| 512K x 8             | FP, LP                | MT4C8512 L      | 70, 80, 100      | 1mW                       | 350mW  | 28                     | 28     | 28     | 2-15  |
| 512K x 8             | FP, WPB, LP           | MT4C8513 L      | 70, 80, 100      | 1mW                       | 350mW  | 28                     | 28     | 28     | 2-15  |
| 2 Meg x 8            | FP, 4KR               | MT4(L)C2M8A1    | 60, 70, 80       | 5mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-31  |
| 2 Meg x 8            | FP, 4KR, WPB          | MT4(L)C2M8A2    | 60, 70, 80       | 5mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-31  |
| 2 Meg x 8            | FP, 2KR               | MT4(L)C2M8B1    | 60, 70, 80       | 5mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-47  |
| 2 Meg x 8            | FP, 2KR, WPB          | MT4(L)C2M8B2    | 60, 70, 80       | 5mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-47  |
| 2 Meg x 8            | FP, 4KR, S, LP        | MT4(L)C2M8A1 S  | 60, 70, 80       | 2mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-63  |
| 2 Meg x 8            | FP, 4KR, WPB, S, LP   | MT4(L)C2M8A2 S  | 60, 70, 80       | 2mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-63  |
| 2 Meg x 8            | FP, 2KR, S, LP        | MT4(L)C2M8B1 S  | 60, 70, 80       | 2mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-81  |
| 2 Meg x 8            | FP, 2KR, WPB, S, LP   | MT4(L)C2M8B2 S  | 60, 70, 80       | 2mW                       | 400mW  | -                      | 28, 32 | 28, 32 | 2-81  |
| 64K x 16             | FP, DW                | MT4C1664        | 70, 80, 100      | 3mW                       | 225mW  | 40                     | 40     | 40     | 2-99  |
| 64K x 16             | FP, WPB               | MT4C1665        | 70, 80, 100      | 3mW                       | 225mW  | 40                     | 40     | 40     | 2-99  |
| 64K x 16             | FP, DW, LP            | MT4C1664 L      | 70, 80, 100      | 1mW                       | 225mW  | 40                     | 40     | 40     | 2-115 |
| 64K x 16             | FP, WPB, LP           | MT4C1665 L      | 70, 80, 100      | 1mW                       | 225mW  | 40                     | 40     | 40     | 2-115 |
| 64K x 16             | SC, DW                | MT4C1670        | 70, 80, 100      | 3mW                       | 225mW  | 40                     | 40     | 40     | 2-133 |
| 64K x 16             | SC, WPB               | MT4C1671        | 70, 80, 100      | 3mW                       | 225mW  | 40                     | 40     | 40     | 2-133 |
| 64K x 16             | SC, DW, LP            | MT4C1670 L      | 70, 80, 100      | 1mW                       | 225mW  | 40                     | 40     | 40     | 2-151 |
| 64K x 16             | SC, WPB, LP           | MT4C1671 L      | 70, 80, 100      | 1mW                       | 225mW  | 40                     | 40     | 40     | 2-151 |
| 256K x 16            | FP, DW                | MT4C16256       | 70, 80, 100      | 3mW                       | 500mW  | 40                     | 40     | 40     | 2-169 |
| 256K x 16            | FP, DC                | MT4C16257       | 70, 80, 100      | 3mW                       | 500mW  | 40                     | 40     | 40     | 2-169 |
| 256K x 16            | FP, DW, WPB           | MT4C16258       | 70, 80, 100      | 3mW                       | 500mW  | 40                     | 40     | 40     | 2-169 |
| 256K x 16            | FP, DC, WPB           | MT4C16259       | 70, 80, 100      | 3mW                       | 500mW  | 40                     | 40     | 40     | 2-169 |
| 256K x 16            | FP, DW, LP            | MT4C16256 L     | 70, 80, 100      | 1mW                       | 500mW  | 40                     | 40     | 40     | 2-191 |
| 256K x 16            | FP, DC, LP            | MT4C16257 L     | 70, 80, 100      | 1mW                       | 500mW  | 40                     | 40     | 40     | 2-191 |
| 256K x 16            | FP, DW, WPB, LP       | MT4C16258 L     | 70, 80, 100      | 1mW                       | 500mW  | 40                     | 40     | 40     | 2-191 |
| 256K x 16            | FP, DC, WPB, LP       | MT4C16259 L     | 70, 80, 100      | 1mW                       | 500mW  | 40                     | 40     | 40     | 2-191 |
| 256K x 16            | FP, ASY, DW           | MT4C16260       | 70, 80, 100      | 1mW                       | 500mW  | 40                     | 40     | 40     | 2-213 |
| 256K x 16            | FP, WPB, ASY          | MT4C16261       | 70, 80, 100      | 1mW                       | 500mW  | 40                     | 40     | 40     | 2-213 |
| 1 Meg x 16           | FP, DC                | MT4(L)C1M16C3   | 60, 70, 80       | 5mW                       | 500mW  | -                      | 42     | 44     | 2-229 |
| 1 Meg x 16           | FP, DW                | MT4(L)C1M16C5   | 60, 70, 80       | 5mW                       | 500mW  | -                      | 42     | 44     | 2-229 |
| 1 Meg x 16           | FP, DC, WPB           | MT4(L)C1M16C6   | 60, 70, 80       | 5mW                       | 500mW  | -                      | 42     | 44     | 2-229 |
| 1 Meg x 16           | FP, DW, WPB           | MT4(L)C1M16C7   | 60, 70, 80       | 5mW                       | 500mW  | -                      | 42     | 44     | 2-229 |
| 1 Meg x 16           | FP, DC, S, LP         | MT4(L)C1M16C3 S | 60, 70, 80       | 2mW                       | 500mW  | -                      | 42     | 44     | 2-251 |
| 1 Meg x 16           | FP, DW, S, LP         | MT4(L)C1M16C5 S | 60, 70, 80       | 2mW                       | 500mW  | -                      | 42     | 44     | 2-251 |
| 1 Meg x 16           | FP, DC, WPB, S, LP    | MT4(L)C1M16C6 S | 60, 70, 80       | 2mW                       | 500mW  | -                      | 42     | 44     | 2-251 |
| 1 Meg x 16           | FP, DW, WPB, S, LP    | MT4(L)C1M16C7 S | 60, 70, 80       | 2mW                       | 500mW  | -                      | 42     | 44     | 2-251 |

FP = Fast Page Mode, SC = Static Column, LP = Low Power, Extended Refresh; WPB = Write Per Bit, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing

\*(L)C means device is available in both 5V Vcc (MT4CXXXXX) and 3/3.3V Vcc (MT4LCXXXXX) versions

**DRAM MODULE PRODUCT SELECTION GUIDE**

| Memory Configuration | Part Number | Optional Access Cycle | Access Time (ns) | Power Dissipation |         | Package |     | Page  |
|----------------------|-------------|-----------------------|------------------|-------------------|---------|---------|-----|-------|
|                      |             |                       |                  | Standby           | Active  | SIMM    | SIP |       |
| 256K x 8             | MT2D2568    | LP, LV*               | 60, 70, 80       | 6mW               | 350mW   | 30      | 30  | 3-1   |
| 1 Meg x 8            | MT2D18      | LP, LV*               | 60, 70, 80       | 6mW               | 450mW   | 30      | 30  | 3-11  |
| 1 Meg x 8            | MT8D18      | LP                    | 60, 70, 80       | 24mW              | 1,400mW | 30      | 30  | 3-21  |
| 4 Meg x 8            | MT2D48      |                       | 60, 70, 80       | 10mW              | 550mW   | 30      | 30  | 3-31  |
| 4 Meg x 8            | MT8D48      | LP                    | 60, 70, 80       | 24mW              | 1,800mW | 30      | 30  | 3-41  |
| 16 Meg x 8           | MT8D168     |                       | 60, 70, 80       | 24mW              | 2,200mW | 30      | 30  | 3-51  |
| 256K x 9             | MT3D2569    | LP                    | 60, 70, 80       | 9mW               | 625mW   | 30      | 30  | 3-61  |
| 1 Meg x 9            | MT3D19      | LP                    | 60, 70, 80       | 9mW               | 625mW   | 30      | 30  | 3-71  |
| 1 Meg x 9            | MT9D19      | LP                    | 60, 70, 80       | 27mW              | 1,575mW | 30      | 30  | 3-81  |
| 4 Meg x 9            | MT3D49      |                       | 60, 70, 80       | 12mW              | 775mW   | 30      | 30  | 3-91  |
| 4 Meg x 9            | MT9D49      | LP                    | 60, 70, 80       | 27mW              | 2,025mW | 30      | 30  | 3-101 |
| 16 Meg x 9           | MT9D169     |                       | 60, 70, 80       | 27mW              | 2,475mW | 30      | 30  | 3-111 |
| 512K x 16            | MT8D25632   | LP, LV*               | 60, 70, 80       | 24mW              | 1,400mW | 72      | -   | 3-121 |
| 1 Meg x 16           | MT16D51232  | LP, LV*               | 60, 70, 80       | 48mW              | 2,800mW | 72      | -   | 3-133 |
| 2 Meg x 16           | MT8D132     | LP, LV*               | 60, 70, 80       | 24mW              | 1,800mW | 72      | -   | 3-145 |
| 4 Meg x 16           | MT16D232    | LP, LV*               | 60, 70, 80       | 48mW              | 1,824mW | 72      | -   | 3-157 |
| 8 Meg x 16           | MT8D432     |                       | 60, 70, 80       | 40mW              | 2,200mW | 72      | -   | 3-169 |
| 16 Meg x 16          | MT16D832    |                       | 60, 70, 80       | 80mW              | 2,240mW | 72      | -   | 3-179 |
| 512K x 18            | MT10D25636  |                       | 60, 70, 80       | 30mW              | 1,750mW | 72      | -   | 3-199 |
| 1 Meg x 18           | MT6D118     |                       | 60, 70, 80       | 18mW              | 1,250mW | 72      | -   | 3-209 |
| 1 Meg x 18           | MT20D51236  |                       | 60, 70, 80       | 60mW              | 1,780mW | 72      | -   | 3-229 |
| 2 Meg x 18           | MT12D136    | LP                    | 60, 70, 80       | 36mW              | 2,500mW | 72      | -   | 3-249 |
| 4 Meg x 18           | MT24D236    | LP                    | 60, 70, 80       | 72mW              | 2,536mW | 72      | -   | 3-271 |
| 8 Meg x 18           | MT12D436    |                       | 60, 70, 80       | 52mW              | 3,100mW | 72      | -   | 3-283 |
| 16 Meg x 18          | MT24D836    |                       | 60, 70, 80       | 104mW             | 3,152mW | 72      | -   | 3-293 |
| 256K x 32            | MT8D25632   | LP, LV*               | 60, 70, 80       | 24mW              | 1,400mW | 72      | -   | 3-121 |
| 512K x 32            | MT16D51232  | LP, LV*               | 60, 70, 80       | 48mW              | 1,424mW | 72      | -   | 3-133 |
| 1 Meg x 32           | MT8D132     | LP, LV*               | 60, 70, 80       | 24mW              | 1,800mW | 72      | -   | 3-145 |
| 2 Meg x 32           | MT16D232    | LP, LV*               | 60, 70, 80       | 48mW              | 1,824mW | 72      | -   | 3-157 |
| 4 Meg x 32           | MT8D432     |                       | 60, 70, 80       | 40mW              | 2,200mW | 72      | -   | 3-169 |
| 8 Meg x 32           | MT16D832    |                       | 60, 70, 80       | 80mW              | 2,240mW | 72      | -   | 3-179 |
| 256K x 36            | MT9D25636   |                       | 60, 70, 80       | 27mW              | 1,575mW | 72      | -   | 3-189 |
| 256K x 36            | MT10D25636  |                       | 60, 70, 80       | 30mW              | 1,750mW | 72      | -   | 3-199 |
| 512K x 36            | MT18D51236  |                       | 60, 70, 80       | 54mW              | 1,600mW | 72      | -   | 3-219 |
| 512K x 36            | MT20D51236  |                       | 60, 70, 80       | 60mW              | 1,780mW | 72      | -   | 3-229 |
| 1 Meg x 36           | MT9D136     |                       | 60, 70, 80       | 27mW              | 2,175mW | 72      | -   | 3-239 |
| 1 Meg x 36           | MT12D136    | LP                    | 60, 70, 80       | 36mW              | 2,500mW | 72      | -   | 3-249 |
| 2 Meg x 36           | MT18D236    |                       | 60, 70, 80       | 54mW              | 2,052mW | 72      | -   | 3-261 |
| 2 Meg x 36           | MT24D236    | LP                    | 60, 70, 80       | 72mW              | 2,536mW | 72      | -   | 3-271 |
| 4 Meg x 36           | MT12D436    |                       | 60, 70, 80       | 52mW              | 3,100mW | 72      | -   | 3-283 |
| 8 Meg x 36           | MT24D836    |                       | 60, 70, 80       | 104mW             | 3,152mW | 72      | -   | 3-293 |
| 256K x 40            | MT10D25640  | LP, LV*               | 60, 70, 80       | 30mW              | 1,750mW | 72      | -   | 3-303 |
| 512K x 40            | MT20D51240  | LP, LV*               | 60, 70, 80       | 60mW              | 1,780mW | 72      | -   | 3-315 |
| 1 Meg x 40           | MT10D140    | LP, LV*               | 60, 70, 80       | 30mW              | 2,250mW | 72      | -   | 3-327 |
| 2 Meg x 40           | MT20D240    | LP, LV*               | 60, 70, 80       | 60mW              | 2,280mW | 72      | -   | 3-339 |

LP = Low Power, Extended Refresh; LV = Low Voltage  
**NOTE:** All modules include FAST PAGE MODE cycle.

\*Contact factory regarding availability of low voltage versions.

**IC DRAM CARD SELECTION GUIDE**

| Memory Configuration |             | Part Number   | Access Time (ns) | Number of Pins | Page  |
|----------------------|-------------|---------------|------------------|----------------|-------|
|                      |             |               |                  | Card           |       |
| 512K x 16            | 1 Megabyte  | MT8D88C25632  | 60, 70, 80       | 88             | 4-1   |
| 1 Meg x 16           | 2 Megabytes | MT16D88C51232 | 60, 70, 80       | 88             | 4-17  |
| 2 Meg x 16           | 4 Megabytes | MT8D88C132    | 60, 70, 80       | 88             | 4-33  |
| 4 Meg x 16           | 8 Megabytes | MT16D88C232   | 60, 70, 80       | 88             | 4-49  |
| 512K x 18            | 1 Megabyte  | MT12D88C25636 | 60, 70, 80       | 88             | 4-65  |
| 1 Meg x 18           | 2 Megabytes | MT24D88C51236 | 60, 70, 80       | 88             | 4-79  |
| 2 Meg x 18           | 4 Megabytes | MT12D88C136   | 60, 70, 80       | 88             | 4-93  |
| 4 Meg x 18           | 8 Megabytes | MT24D88C236   | 60, 70, 80       | 88             | 4-107 |
| 512K x 20            | 1 Megabyte  | MT12D88C25640 | 60, 70, 80       | 88             | 4-121 |
| 1 Meg x 20           | 2 Megabytes | MT24D88C51240 | 60, 70, 80       | 88             | 4-137 |
| 2 Meg x 20           | 4 Megabytes | MT12D88C140   | 60, 70, 80       | 88             | 4-153 |
| 4 Meg x 20           | 8 Megabytes | MT24D88C240   | 60, 70, 80       | 88             | 4-169 |
| 256K x 32            | 1 Megabyte  | MT8D88C25632  | 60, 70, 80       | 88             | 4-1   |
| 512K x 32            | 2 Megabytes | MT16D88C51232 | 60, 70, 80       | 88             | 4-17  |
| 1 Meg x 32           | 4 Megabytes | MT8D88C132    | 60, 70, 80       | 88             | 4-33  |
| 2 Meg x 32           | 8 Megabytes | MT16D88C232   | 60, 70, 80       | 88             | 4-49  |
| 256K x 36            | 1 Megabyte  | MT12D88C25636 | 60, 70, 80       | 88             | 4-65  |
| 512K x 36            | 2 Megabytes | MT24D88C51236 | 60, 70, 80       | 88             | 4-79  |
| 1 Meg x 36           | 4 Megabytes | MT12D88C136   | 60, 70, 80       | 88             | 4-93  |
| 2 Meg x 36           | 8 Megabytes | MT24D88C236   | 60, 70, 80       | 88             | 4-107 |
| 256K x 40            | 1 Megabyte  | MT12D88C25640 | 60, 70, 80       | 88             | 4-121 |
| 512K x 40            | 2 Megabytes | MT24D88C51240 | 60, 70, 80       | 88             | 4-137 |
| 1 Meg x 40           | 4 Megabytes | MT12D88C140   | 60, 70, 80       | 88             | 4-153 |
| 2 Meg x 40           | 8 Megabytes | MT24D88C240   | 60, 70, 80       | 88             | 4-169 |

**DUAL PORT DRAM (VRAM) PRODUCT SELECTION GUIDE**

| Memory Configuration | Access Cycle | Part Number   | Access Time (ns) | Power Dissipation |        | Package and Number of Pins |     |       |     | Page  |
|----------------------|--------------|---------------|------------------|-------------------|--------|----------------------------|-----|-------|-----|-------|
|                      |              |               |                  | Standby           | Active | SOJ                        | SOG | TSOP  | ZIP |       |
| 256K x 4             | FP           | MT42C4255     | 80, 100          | 15mW              | 275mW  | 28                         | -   | -     | 28  | 5-1   |
| 256K x 4             | FP, BW, LP   | MT42C4256     | 70, 80, 100      | 15mW              | 275mW  | 28                         | -   | -     | 28  | 5-3   |
| 128K x 8             | FP           | MT42C8127     | 80, 100          | 15mW              | 275mW  | 40                         | -   | -     | -   | 5-39  |
| 128K x 8             | FP, BW, LP   | MT42C8128     | 70, 80, 100      | 15mW              | 275mW  | 40                         | -   | 40/44 | -   | 5-41  |
| 256K x 8             | FP, BW       | MT42C8255     | 70, 80           | 10mW              | 300mW  | 40                         | -   | 40/44 | -   | 5-79  |
| 256K x 8             | FP, BW       | MT42C8256     | 70, 80           | 10mW              | 300mW  | 40                         | -   | 40/44 | -   | 5-111 |
| 256K x 16            | FP, BW       | MT42C256K16A1 | 60, 70, 80       | 10mW              | 350mW  | -                          | 64  | -     | -   | 5-153 |

FP = Fast Page Mode, BW = Block Write, LP = Low Power, Extended Refresh

**TRIPLE PORT DRAM PRODUCT SELECTION GUIDE**

| Memory Configuration | Access Cycle    | Part Number  | Access Time (ns) | Power Dissipation |        | Package/Number of Pins |     |       |      | Page  |
|----------------------|-----------------|--------------|------------------|-------------------|--------|------------------------|-----|-------|------|-------|
|                      |                 |              |                  | Standby           | Active | SOJ                    | SOG | TSOP  | PLCC |       |
| 256K x 4             | FP, BW, QSF pin | MT43C4257    | 80, 100          | 15mW              | 500mW  | 40                     | -   | 40/44 | -    | 5-155 |
| 256K x 4             | FP, BW, SSF pin | MT43C4258    | 80, 100          | 15mW              | 500mW  | 40                     | -   | 40/44 | -    | 5-155 |
| 128K x 8             | FP, BW, QSF pin | MT43C8128    | 80, 100          | 15mW              | 550mW  | -                      | -   | -     | 52   | 5-201 |
| 128K x 8             | FP, BW, SSF pin | MT43C8129    | 80, 100          | 15mW              | 550mW  | -                      | -   | -     | 52   | 5-201 |
| 256K x 8             | FP, BW          | MT43C256K8A1 | 60, 70, 80       | 15mW              | 400mW  | -                      | 64  | -     | -    | 5-247 |

FP = Fast Page Mode, BW = Block Write

**APPLICATION/TECHNICAL NOTE SELECTION GUIDE**

| Technical Note | Title                                                                        | Page |
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| TN-04-04       | MT4C1664: 256 Kilobyte Memory System with Four $\overline{\text{CAS}}$ Lines | 6-15 |
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## DRAM PRODUCT SELECTION GUIDE

| Memory Configuration | Optional Access Cycle | Part Number | Access Time (ns) | Typical Power Dissipation |        | Package and Number of Pins |     |     |      | Page  |
|----------------------|-----------------------|-------------|------------------|---------------------------|--------|----------------------------|-----|-----|------|-------|
|                      |                       |             |                  | Standby                   | Active | PDIP                       | ZIP | SOJ | TSOP |       |
| 1 Meg x 1            | FP                    | MT4C1024    | 60, 70, 80       | 3mW                       | 175mW  | 18                         | 20  | 20  | 20   | 1-1   |
| 1 Meg x 1            | FP, LP                | MT4C1024 L  | 70, 80, 100      | 0.3mW                     | 150mW  | 18                         | 20  | 20  | 20   | 1-13  |
| 1 Meg x 1            | SC                    | MT4C1026    | 70, 80           | 3mW                       | 175mW  | 18                         | 20  | 20  | -    | 1-25  |
| 4 Meg x 1            | FP                    | MT4C1004J   | 60, 70, 80       | 3mW                       | 225mW  | -                          | 20  | 20  | 20   | 1-37  |
| 4 Meg x 1            | FP, LP                | MT4C1004J L | 60, 70, 80       | 1mW                       | 225mW  | -                          | 20  | 20  | 20   | 1-49  |
| 4 Meg x 1            | SC                    | MT4C1006J   | 70, 80           | 3mW                       | 225mW  | -                          | 20  | 20  | -    | 1-61  |
| 16 Meg x 1           | FP, 4KR               | MT4C16M1A1  | 60, 70, 80       | 3mW                       | 325mW  | -                          | -   | 24  | 24   | 1-73  |
| 16 Meg x 1           | FP, 4KR, LV           | MT4LC16M1A1 | 60, 70, 80       | 1mW                       | 125mW  | -                          | -   | 24  | 24   | 1-73  |
| 16 Meg x 1           | SC, 4KR               | MT4C16M1D1  | 60, 70, 80       | 3mW                       | 330mW  | -                          | -   | 24  | -    | 1-85  |
| 256K x 4             | FP                    | MT4C4256    | 60, 70, 80       | 3mW                       | 175mW  | 20                         | 20  | 20  | 20   | 1-87  |
| 256K x 4             | FP, LP                | MT4C4256 L  | 70, 80, 100      | 0.3mW                     | 150mW  | 20                         | 20  | 20  | 20   | 1-97  |
| 256K x 4             | FP, LP, LV            | MT4C4256 VL | 100, 120         | 0.1mW                     | 100mW  | -                          | 20  | 20  | 20   | 1-109 |
| 256K x 4             | SC                    | MT4C4258    | 70, 80, 100      | 3mW                       | 175mW  | 20                         | 20  | 20  | -    | 1-121 |
| 1 Meg x 4            | FP                    | MT4C4001J   | 60, 70, 80       | 3mW                       | 225mW  | -                          | 20  | 20  | 20   | 1-133 |
| 1 Meg x 4            | FP, LP                | MT4C4001J L | 60, 70, 80       | 1mW                       | 225mW  | -                          | 20  | 20  | 20   | 1-145 |
| 1 Meg x 4            | SC                    | MT4C4003J   | 70, 80           | 3mW                       | 225mW  | -                          | 20  | 20  | -    | 1-157 |
| 1 Meg x 4            | FP, QCP               | MT4C4004J   | 70, 80, 100      | 3mW                       | 225mW  | -                          | -   | 24  | -    | 1-169 |
| 4 Meg x 4            | FP, 4KR               | MT4C4M4A1   | 60, 70, 80       | 3mW                       | 325mW  | -                          | -   | 24  | 24   | 1-183 |
| 4 Meg x 4            | FP, 2KR               | MT4C4M4B1   | 60, 70, 80       | 3mW                       | 400mW  | -                          | -   | 24  | 24   | 1-183 |
| 4 Meg x 4            | FP, 4KR, LV           | MT4LC4M4A1  | 60, 70, 80       | 1mW                       | 125mW  | -                          | -   | 24  | 24   | 1-195 |
| 4 Meg x 4            | FP, 2KR, LV           | MT4LC4M4B1  | 60, 70, 80       | 1mW                       | 175mW  | -                          | -   | 24  | 24   | 1-195 |
| 4 Meg x 4            | SC, 4KR               | MT4C4M4D1   | 60, 70, 80       | 3mW                       | 325mW  | -                          | -   | 24  | -    | 1-207 |

FP = Fast Page Mode, SC = Static Column Mode, LP = Low Power, Extended Refresh; QCP = Quad CAS Parity,  
 LV = Low Voltage, 2KR = 2,048 Row Refresh, 4KR = 4,096 Row Refresh

# DRAM

# 16 MEG x 1 DRAM

## FAST PAGE MODE

### FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V  $\pm 10\%$  only or +3.3V  $\pm 10\%$  only
- Low power, 3mW standby; 325mW active, typical (5V)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

### OPTIONS

- Timing
  - 60ns access
  - 70ns access
  - 80ns access

### MARKING

-6  
-7  
-8

- Packages

Plastic SOJ (400 mil)  
Plastic TSOP (400 mil)

DJ  
TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Operating Temperature,  $T_A$   
Commercial (0°C to +70°C)

None

- Power Supply

+5V  $\pm 10\%$   
+3.3V  $\pm 10\%$

MT4C16M1A1  
MT4LC16M1A1

### GENERAL DESCRIPTION

The MT4(L)C16M1A1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. The MT4C16M1A1 and MT4LC16M1A1 are the same DRAM versions except that the MT4LC16M1A1 is a low voltage version of the MT4C16M1A1. The MT4LC16M1A1 is designed to operate in a 3.3+/-10% memory system. All further references made for the MT4C16M1A1 also apply to the MT4LC16M1A1 unless specifically stated otherwise. During READ and WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time.  $\overline{\text{RAS}}$  is used to latch the first 12 bits and  $\overline{\text{CAS}}$  the latter 12 bits. READ and WRITE cycles are selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE

### PIN ASSIGNMENT (Top View)

#### 24-Pin SOJ (Q-3)

|     |    |    |     |
|-----|----|----|-----|
| Vcc | 1  | 28 | Vss |
| D   | 2  | 27 | Q   |
| NC  | 3  | 26 | NC  |
| WE  | 4  | 25 | CAS |
| RAS | 5  | 24 | NC  |
| A11 | 6  | 23 | A9  |
|     |    |    |     |
| A10 | 9  | 20 | A8  |
| A0  | 10 | 19 | A7  |
| A1  | 11 | 18 | A6  |
| A2  | 12 | 17 | A5  |
| A3  | 13 | 16 | A4  |
| Vcc | 14 | 15 | Vss |

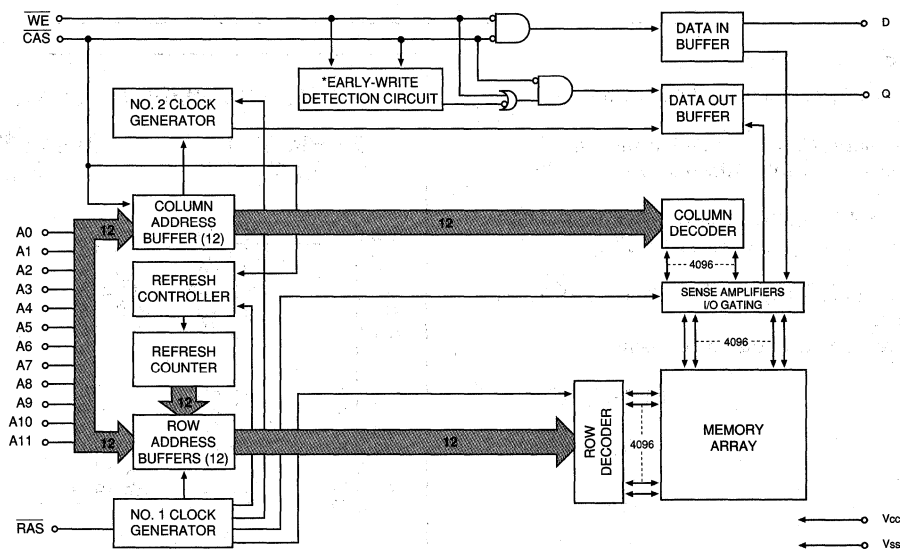
#### 24-Pin TSOP (R-2)

|     |    |    |     |
|-----|----|----|-----|
| Vcc | 1  | 28 | Vss |
| D   | 2  | 27 | Q   |
| NC  | 3  | 26 | NC  |
| WE  | 4  | 25 | CAS |
| RAS | 5  | 24 | NC  |
| A11 | 6  | 23 | A9  |
|     |    |    |     |
| A10 | 9  | 20 | A8  |
| A0  | 10 | 19 | A7  |
| A1  | 11 | 18 | A6  |
| A2  | 12 | 17 | A5  |
| A3  | 13 | 16 | A4  |
| Vcc | 14 | 15 | Vss |

cycle, data in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pin remains open (High-Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains LOW (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by  $\overline{\text{RAS}}$  followed by a column address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning  $\overline{\text{RAS}}$  HIGH terminates the FAST PAGE MODE operation.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR), or HIDDEN refresh) so that all 4,096 combinations of  $\overline{\text{RAS}}$  addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic  $\overline{\text{RAS}}$  addressing.

FUNCTIONAL BLOCK DIAGRAM  
FAST PAGE MODE

\*NOTE:  $\overline{WE}$  LOW prior to  $\overline{CAS}$  LOW, EW detection circuit output is a HIGH (EARLY-WRITE)  
 $\overline{CAS}$  LOW prior to  $\overline{WE}$  LOW, EW detection circuit output is a LOW (LATE-WRITE)

## TRUTH TABLE

| FUNCTION                      |           | RAS   | CAS | WE  | ADDRESSES      |                | DATA        |              |
|-------------------------------|-----------|-------|-----|-----|----------------|----------------|-------------|--------------|
|                               |           |       |     |     | $\overline{R}$ | $\overline{C}$ | D (Data In) | Q (Data Out) |
| Standby                       |           | H     | H→X | X   | X              | X              | Don't Care  | High-Z       |
| READ                          |           | L     | L   | H   | ROW            | COL            | Don't Care  | Data Out     |
| EARLY-WRITE                   |           | L     | L   | L   | ROW            | COL            | Data In     | High-Z       |
| READ-WRITE                    |           | L     | L   | H→L | ROW            | COL            | Data In     | Data Out     |
| FAST-PAGE-MODE<br>READ        | 1st Cycle | L     | H→L | H   | ROW            | COL            | Don't Care  | Data Out     |
|                               | 2nd Cycle | L     | H→L | H   | n/a            | COL            | Don't Care  | Data Out     |
| FAST-PAGE-MODE<br>EARLY-WRITE | 1st Cycle | L     | H→L | L   | ROW            | COL            | Data In     | High-Z       |
|                               | 2nd Cycle | L     | H→L | L   | n/a            | COL            | Data In     | High-Z       |
| FAST-PAGE-MODE<br>READ-WRITE  | 1st Cycle | L     | H→L | H→L | ROW            | COL            | Data In     | Data Out     |
|                               | 2nd Cycle | L     | H→L | H→L | n/a            | COL            | Data In     | Data Out     |
| RAS-ONLY REFRESH              |           | L     | H   | X   | ROW            | n/a            | Don't Care  | High-Z       |
| HIDDEN<br>REFRESH             | READ      | L→H→L | L   | H   | ROW            | COL            | Don't Care  | Data Out     |
|                               | WRITE     | L→H→L | L   | L   | ROW            | COL            | Data In     | High-Z       |
| CAS-BEFORE-RAS REFRESH        |           | H→L   | L   | H   | X              | X              | Don't Care  | High-Z       |

**ABSOLUTE MAXIMUM RATINGS\***

|                                                           |                 |
|-----------------------------------------------------------|-----------------|
| Voltage on Any Pin Relative to V <sub>SS</sub> (3.3V) ... | -1V to +4.5V    |
| Voltage on Any Pin Relative to V <sub>SS</sub> (5V) ..... | -1V to +7V      |
| Operating Temperature, T <sub>A</sub> (Ambient) .....     | 0°C to +70°C    |
| Storage Temperature (Plastic) .....                       | -55°C to +150°C |
| Power Dissipation .....                                   | 1W              |
| Short Circuit Output Current .....                        | 50mA            |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 3, 4, 6, 7) (V<sub>CC</sub> = 5V ±10%)

| PARAMETER/CONDITION                                                                                    | SYMBOL          | MIN  | MAX                | UNITS | NOTES |
|--------------------------------------------------------------------------------------------------------|-----------------|------|--------------------|-------|-------|
| Supply Voltage                                                                                         | V <sub>CC</sub> | 4.5  | 5.5                | V     | 1     |
| Input High (Logic 1) Voltage, All Inputs                                                               | V <sub>IH</sub> | 2.4  | V <sub>CC</sub> +1 | V     | 1     |
| Input Low (Logic 0) Voltage, All Inputs                                                                | V <sub>IL</sub> | -1.0 | 0.8                | V     | 1     |
| INPUT LEAKAGE CURRENT<br>Any Input 0V ≤ V <sub>IN</sub> ≤ 6.5V<br>(All other pins not under test = 0V) | I <sub>I</sub>  | -2   | 2                  | μA    |       |
| OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V <sub>OUT</sub> ≤ 5.5V)                                   | I <sub>OZ</sub> | -10  | 10                 | μA    |       |
| OUTPUT LEVELS<br>Output High Voltage (I <sub>OUT</sub> = -5mA)                                         | V <sub>OH</sub> | 2.4  |                    | V     |       |
| Output Low Voltage (I <sub>OUT</sub> = 4.2mA)                                                          | V <sub>OL</sub> |      | 0.4                | V     |       |

(Notes: 1, 3, 4, 6, 7) (V<sub>CC</sub> = 3.3V ±10%)

| PARAMETER/CONDITION                                                                                    | SYMBOL          | MIN  | MAX                | UNITS | NOTES |
|--------------------------------------------------------------------------------------------------------|-----------------|------|--------------------|-------|-------|
| Supply Voltage                                                                                         | V <sub>CC</sub> | 3.0  | 3.6                | V     | 1     |
| Input High (Logic 1) Voltage, All Inputs                                                               | V <sub>IH</sub> | 2.0  | V <sub>CC</sub> +1 | V     | 1     |
| Input Low (Logic 0) Voltage, All Inputs                                                                | V <sub>IL</sub> | -1.0 | 0.8                | V     | 1     |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ V <sub>IN</sub> ≤ 3.6V<br>(All other pins not under test = 0V) | I <sub>I</sub>  | -2   | 2                  | μA    |       |
| OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V <sub>OUT</sub> ≤ 3.6V)                                   | I <sub>OZ</sub> | -10  | 10                 | μA    |       |
| OUTPUT LEVELS<br>Output High Voltage (I <sub>OUT</sub> = -2mA)                                         | V <sub>OH</sub> | 2.4  |                    | V     |       |
| Output Low Voltage (I <sub>OUT</sub> = 2mA)                                                            | V <sub>OL</sub> |      | 0.4                | V     |       |

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

 (Notes: 1, 3, 4, 6, 7) ( $V_{CC} = 5V \pm 10\%$ )

| PARAMETER/CONDITION                                                                                                                                                          | SYMBOL | MAX |    |    | UNITS | NOTES |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|----|----|-------|-------|
|                                                                                                                                                                              |        | -6  | -7 | -8 |       |       |
| STANDBY CURRENT: (TTL)<br>( $\overline{RAS} = \overline{CAS} = V_{IH}$ )                                                                                                     | lcc1   | 2   | 2  | 2  | mA    |       |
| STANDBY CURRENT: (CMOS)<br>( $\overline{RAS} = \overline{CAS} = \text{Other Inputs} = V_{CC} - 0.2V$ )                                                                       | lcc2   | 1   | 1  | 1  | mA    |       |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t'RC = t'RC$ (MIN))                        | lcc3   | 90  | 80 | 70 | mA    | 3, 4  |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t'PC = t'PC$ (MIN))                  | lcc4   | 70  | 60 | 50 | mA    | 3, 4  |
| REFRESH CURRENT: $\overline{RAS}$ -ONLY<br>Average power supply current<br>( $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ : $t'RC = t'RC$ (MIN))                      | lcc5   | 90  | 80 | 70 | mA    | 3     |
| REFRESH CURRENT: $\overline{CAS}$ -BEFORE- $\overline{RAS}$<br>Average power supply current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t'RC = t'RC$ (MIN)) | lcc6   | 90  | 80 | 70 | mA    | 3, 5  |

 (Notes: 1, 3, 4, 6, 7) ( $V_{CC} = 3.3V \pm 10\%$ )

| PARAMETER/CONDITION                                                                                                                                                          | SYMBOL | MAX |     |     | UNITS   | NOTES |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|-----|---------|-------|
|                                                                                                                                                                              |        | -6  | -7  | -8  |         |       |
| STANDBY CURRENT: (TTL)<br>( $\overline{RAS} = \overline{CAS} = V_{IH}$ )                                                                                                     | lcc1   | 2   | 2   | 2   | mA      |       |
| STANDBY CURRENT: (CMOS)<br>( $\overline{RAS} = \overline{CAS} = \text{Other Inputs} = V_{CC} - 0.2V$ )                                                                       | lcc2   | 400 | 400 | 400 | $\mu A$ |       |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t'RC = t'RC$ (MIN))                        | lcc3   | 60  | 55  | 50  | mA      | 3, 4  |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t'PC = t'PC$ (MIN))                  | lcc4   | 40  | 35  | 30  | mA      | 3, 4  |
| REFRESH CURRENT: $\overline{RAS}$ -ONLY<br>Average power supply current<br>( $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ : $t'RC = t'RC$ (MIN))                      | lcc5   | 60  | 55  | 50  | mA      | 3     |
| REFRESH CURRENT: $\overline{CAS}$ -BEFORE- $\overline{RAS}$<br>Average power supply current<br>( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t'RC = t'RC$ (MIN)) | lcc6   | 60  | 55  | 50  | mA      | 3, 5  |

## CAPACITANCE

| PARAMETER                       | SYMBOL          | MIN | MAX | UNITS | NOTES |
|---------------------------------|-----------------|-----|-----|-------|-------|
| Input Capacitance: A0-A11, D    | C <sub>I1</sub> |     | 5   | pF    | 2     |
| Input Capacitance: RAS, CAS, WE | C <sub>I2</sub> |     | 7   | pF    | 2     |
| Output Capacitance: Q           | C <sub>O</sub>  |     | 7   | pF    | 2     |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13)

| AC CHARACTERISTICS                              |                   | -6  |         | -7  |         | -8  |         | UNITS | NOTES |
|-------------------------------------------------|-------------------|-----|---------|-----|---------|-----|---------|-------|-------|
| PARAMETER                                       | SYM               | MIN | MAX     | MIN | MAX     | MIN | MAX     |       |       |
| Random READ or WRITE cycle time                 | <sup>1</sup> RC   | 110 |         | 130 |         | 150 |         | ns    |       |
| READ-WRITE cycle time                           | <sup>1</sup> RWC  | 130 |         | 155 |         | 175 |         | ns    |       |
| FAST-PAGE-MODE<br>READ or WRITE cycle time      | <sup>1</sup> PC   | 40  |         | 45  |         | 50  |         | ns    |       |
| FAST-PAGE-MODE<br>READ-WRITE cycle time         | <sup>1</sup> PRWC | 60  |         | 70  |         | 75  |         | ns    |       |
| Access time from RAS                            | <sup>1</sup> RAC  |     | 60      |     | 70      |     | 80      | ns    | 14    |
| Access time from CAS                            | <sup>1</sup> CAC  |     | 15      |     | 20      |     | 20      | ns    | 15    |
| Access time from column address                 | <sup>1</sup> AA   |     | 30      |     | 35      |     | 40      | ns    |       |
| Access time from CAS precharge                  | <sup>1</sup> CPA  |     | 35      |     | 40      |     | 45      | ns    |       |
| RAS pulse width                                 | <sup>1</sup> RAS  | 60  | 100,000 | 70  | 100,000 | 80  | 100,000 | ns    |       |
| RAS pulse width (FAST PAGE MODE)                | <sup>1</sup> RASP | 60  | 100,000 | 70  | 100,000 | 80  | 100,000 | ns    |       |
| RAS hold time                                   | <sup>1</sup> RSH  | 15  |         | 20  |         | 20  |         | ns    |       |
| RAS precharge time                              | <sup>1</sup> RP   | 40  |         | 50  |         | 60  |         | ns    |       |
| CAS pulse width                                 | <sup>1</sup> CAS  | 15  | 100,000 | 20  | 100,000 | 20  | 100,000 | ns    |       |
| CAS hold time                                   | <sup>1</sup> CSH  | 60  |         | 70  |         | 80  |         | ns    |       |
| CAS precharge time                              | <sup>1</sup> CPN  | 10  |         | 10  |         | 10  |         | ns    | 16    |
| CAS precharge time (FAST PAGE MODE)             | <sup>1</sup> CP   | 10  |         | 10  |         | 10  |         | ns    |       |
| RAS to CAS delay time                           | <sup>1</sup> RCD  | 20  | 45      | 20  | 50      | 20  | 60      | ns    | 17    |
| CAS to RAS precharge time                       | <sup>1</sup> CRP  | 5   |         | 5   |         | 5   |         | ns    |       |
| Row address setup time                          | <sup>1</sup> ASR  | 0   |         | 0   |         | 0   |         | ns    |       |
| Row address hold time                           | <sup>1</sup> RAH  | 10  |         | 10  |         | 10  |         | ns    |       |
| RAS to column<br>address delay time             | <sup>1</sup> RAD  | 15  | 30      | 15  | 35      | 15  | 40      | ns    | 18    |
| Column address setup time                       | <sup>1</sup> ASC  | 0   |         | 0   |         | 0   |         | ns    |       |
| Column address hold time                        | <sup>1</sup> CAH  | 10  |         | 15  |         | 15  |         | ns    |       |
| Column address hold time<br>(referenced to RAS) | <sup>1</sup> AR   | 50  |         | 55  |         | 60  |         | ns    |       |
| Column address to<br>RAS lead time              | <sup>1</sup> RAL  | 30  |         | 35  |         | 40  |         | ns    |       |
| Read command setup time                         | <sup>1</sup> RCS  | 0   |         | 0   |         | 0   |         | ns    |       |
| Read command hold time<br>(referenced to CAS)   | <sup>1</sup> RCH  | 0   |         | 0   |         | 0   |         | ns    | 19    |
| Read command hold time<br>(referenced to RAS)   | <sup>1</sup> RRH  | 0   |         | 0   |         | 0   |         | ns    | 19    |
| CAS to output in Low-Z                          | <sup>1</sup> CLZ  | 0   |         | 0   |         | 0   |         | ns    |       |
| Output buffer turn-off delay                    | <sup>1</sup> OFF  | 0   | 15      | 0   | 20      | 0   | 20      | ns    | 20    |
| WE command setup time                           | <sup>1</sup> WCS  | 0   |         | 0   |         | 0   |         | ns    | 21    |

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

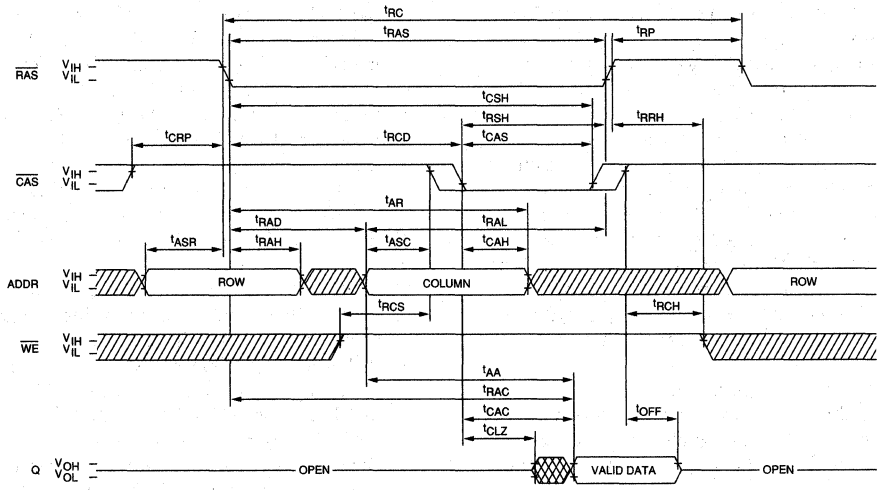
 (Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $V_{CC} = 5V \pm 10\%$ )

| AC CHARACTERISTICS                             |           | -6  |     | -7  |     | -8  |     | UNITS | NOTES |
|------------------------------------------------|-----------|-----|-----|-----|-----|-----|-----|-------|-------|
| PARAMETER                                      | SYM       | MIN | MAX | MIN | MAX | MIN | MAX |       |       |
| Write command hold time                        | $t_{WCH}$ | 10  |     | 15  |     | 15  |     | ns    |       |
| Write command hold time<br>(referenced to RAS) | $t_{WCR}$ | 45  |     | 55  |     | 60  |     | ns    |       |
| Write command pulse width                      | $t_{WP}$  | 10  |     | 15  |     | 15  |     | ns    |       |
| Write command to RAS lead time                 | $t_{RWL}$ | 15  |     | 20  |     | 20  |     | ns    |       |
| Write command to CAS lead time                 | $t_{CWL}$ | 15  |     | 20  |     | 20  |     | ns    |       |
| Data-in setup time                             | $t_{DS}$  | 0   |     | 0   |     | 0   |     | ns    | 22    |
| Data-in hold time                              | $t_{DH}$  | 10  |     | 15  |     | 15  |     | ns    | 22    |
| Data-in hold time<br>(referenced to RAS)       | $t_{DHR}$ | 45  |     | 55  |     | 60  |     | ns    |       |
| RAS to WE delay time                           | $t_{RWD}$ | 60  |     | 70  |     | 80  |     | ns    | 21    |
| Column address<br>to WE delay time             | $t_{AWD}$ | 30  |     | 35  |     | 40  |     | ns    | 21    |
| CAS to WE delay time                           | $t_{CWD}$ | 15  |     | 20  |     | 20  |     | ns    | 21    |
| Transition time (rise or fall)                 | $t_T$     | 3   | 50  | 3   | 50  | 3   | 50  | ns    | 9, 10 |
| Refresh period (1,024 cycles)                  | $t_{REF}$ |     | 64  |     | 64  |     | 64  | ms    |       |
| RAS to CAS precharge time                      | $t_{RPC}$ | 0   |     | 0   |     | 0   |     | ns    |       |
| CAS setup time<br>(CAS-BEFORE-RAS refresh)     | $t_{CSR}$ | 5   |     | 5   |     | 5   |     | ns    | 5     |
| CAS hold time<br>(CAS-BEFORE-RAS refresh)      | $t_{CHR}$ | 15  |     | 15  |     | 15  |     | ns    | 5     |
| WE hold time<br>(CAS-BEFORE-RAS refresh)       | $t_{WRH}$ | 10  |     | 10  |     | 10  |     | ns    | 24    |
| WE setup time<br>(CAS-BEFORE-RAS refresh)      | $t_{WRP}$ | 10  |     | 10  |     | 10  |     | ns    | 24    |
| WE hold time<br>(WCBR test cycle)              | $t_{WTH}$ | 10  |     | 10  |     | 10  |     | ns    | 24    |
| WE setup time<br>(WCBR test cycle)             | $t_{WTS}$ | 10  |     | 10  |     | 10  |     | ns    | 24    |

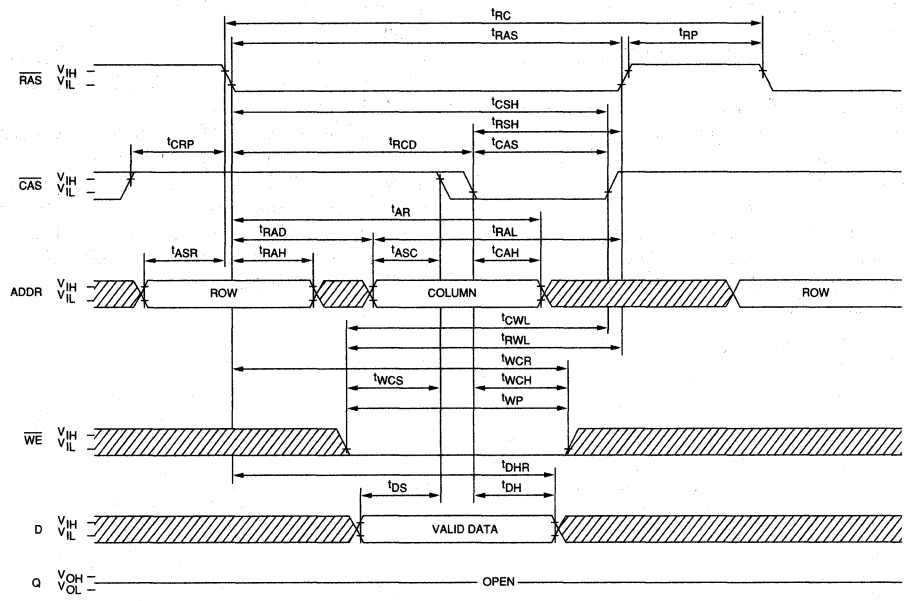
## NOTES

1. All voltages referenced to V<sub>SS</sub>.
2. This parameter is sampled. V<sub>CC</sub> = 5V ±10%, f = 1 MHz.
3. I<sub>CC</sub> is dependent on cycle rates.
4. I<sub>CC</sub> is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
7. An initial pause of 100μs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
8. AC characteristics assume T = 5ns.
9. V<sub>IH</sub> (MIN) and V<sub>IL</sub> (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>).
10. In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
11. If  $\overline{\text{CAS}} = V_{IH}$ , data output is High-Z.
12. If  $\overline{\text{CAS}} = V_{IL}$ , data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
15. Assumes that tRCD ≥ tRCD (MAX).
16. If  $\overline{\text{CAS}}$  is LOW at the falling edge of  $\overline{\text{RAS}}$ , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer,  $\overline{\text{CAS}}$  must be pulsed HIGH for tCPN.
17. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
18. Operation within the tRAD (MAX) limit ensures that tRAC (MIN) and tCAC (MIN) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, then access time is controlled exclusively by tAA.
19. Either tRCH or tRRH must be satisfied for a READ cycle.
20. tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until  $\overline{\text{CAS}}$  goes back to V<sub>IH</sub>).
22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early WRITE cycles and  $\overline{\text{WE}}$  leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{\text{WE}} = \text{LOW}$ .
24. tWTS and tWTH are set up and hold specifications for the  $\overline{\text{WE}}$  pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverses of tWRP and tWRH in the CBR refresh cycle.

**READ CYCLE**

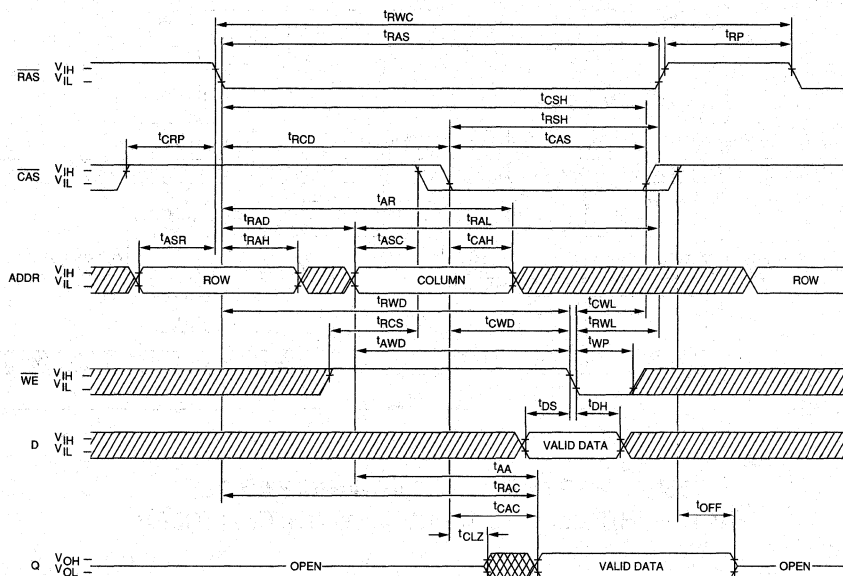


**EARLY-WRITE CYCLE**

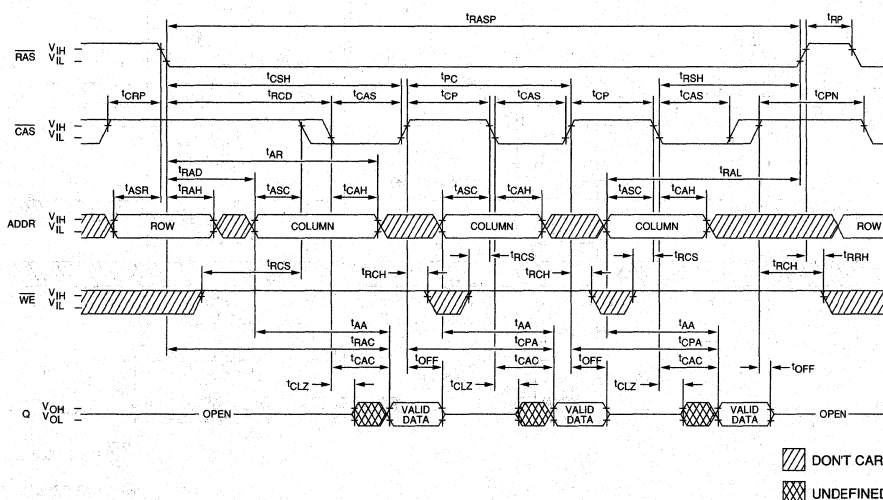


DON'T CARE  
 UNDEFINED

# **READ-WRITE CYCLE** **(LATE-WRITE and READ-MODIFY-WRITE CYCLES)**



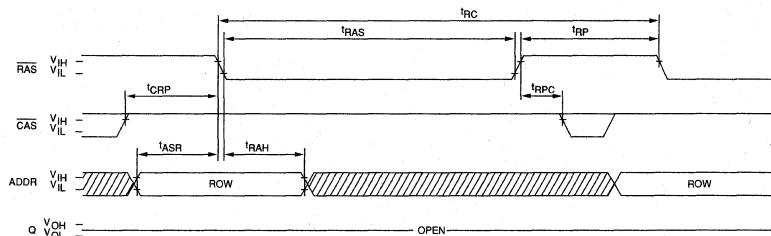
## **FAST-PAGE-MODE READ CYCLE**



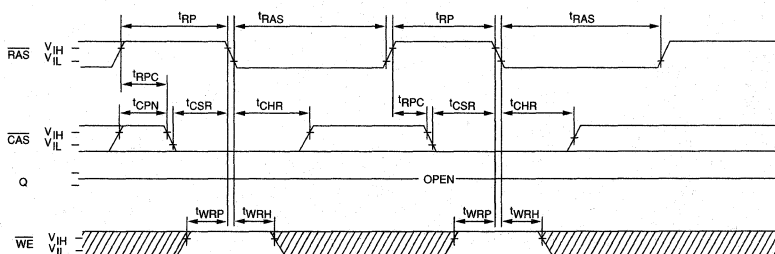
[illegible]

The diagram illustrates the timing relationships for the 64K1602S2-1000 memory device. It shows the signals RAS, CAS, ADDR, WE, D, and Q, along with their respective timing parameters. The signals are shown as waveforms, and the timing parameters are indicated by arrows and labels. The diagram is divided into several sections, each representing a different memory access operation. The signals are labeled with their high and low levels (V<sub>OH</sub>, V<sub>OL</sub> for Q; V<sub>IH</sub>, V<sub>IL</sub> for others). The timing parameters are labeled with 't' followed by a subscript. The diagram also includes a legend for 'DON'T CARE' (hatched area) and 'UNDEFINED' (cross-hatched area).

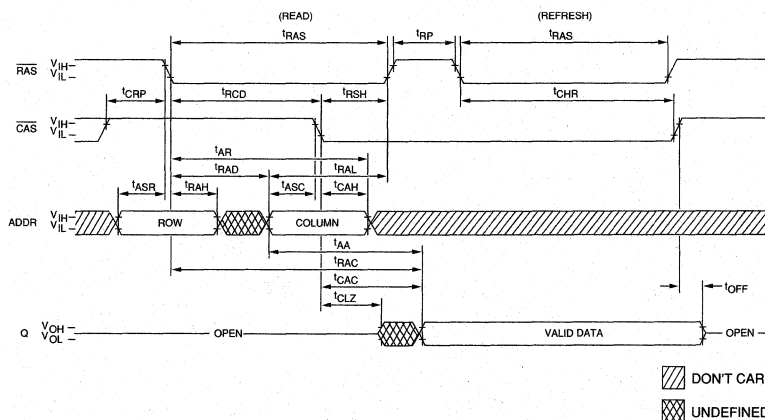
**RAS-ONLY REFRESH CYCLE**  
(ADDR = A0-A10; A11 and  $\overline{WE}$  = DON'T CARE)



**CAS-BEFORE-RAS REFRESH CYCLE**  
(A0-A11 = DON'T CARE)



**HIDDEN REFRESH CYCLE <sup>23</sup>**  
( $\overline{WE}$  = HIGH)





# DRAM

# 16 MEG x 1 DRAM

## STATIC COLUMN

### FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V  $\pm 10\%$
- Low power, 3mW standby; 330mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

### OPTIONS

- Timing
- 60ns access
- 70ns access
- 80ns access

### MARKING

-6  
-7  
-8

- Packages

Plastic SOJ (400 mil)

DJ

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Operating Temperature,  $T_A$

Commercial (0°C to +70°C)

None

- Part Number Example: MT4C16M1D1DJ-6

### GENERAL DESCRIPTION

The MT4C16M1D1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time.  $\overline{\text{RAS}}$  is used to latch the first 12 bits and  $\overline{\text{CAS}}$  the latter 12 bits. READ and WRITE cycles are selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pin remains open (High-Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$

### PIN ASSIGNMENT (Top View)

#### 24-Pin SOJ (Q-3)

|                         |    |    |                         |
|-------------------------|----|----|-------------------------|
| Vcc                     | 1  | 28 | Vss                     |
| D                       | 2  | 27 | Q                       |
| NC                      | 3  | 26 | NC                      |
| $\overline{\text{WE}}$  | 4  | 25 | $\overline{\text{CAS}}$ |
| $\overline{\text{RAS}}$ | 5  | 24 | NC                      |
| A11                     | 6  | 23 | A9                      |
| A10                     | 9  | 20 | A8                      |
| A0                      | 10 | 19 | A7                      |
| A1                      | 11 | 18 | A6                      |
| A2                      | 12 | 17 | A5                      |
| A3                      | 13 | 16 | A4                      |
| Vcc                     | 14 | 15 | Vss                     |

remains LOW (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the PAGE-MODE part, which requires  $\overline{\text{CAS}}$  to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows  $\overline{\text{CAS}}$  to be left LOW for successive STATIC COLUMN accesses. Returning  $\overline{\text{RAS}}$  HIGH terminates the STATIC COLUMN operation.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  or HIDDEN refresh) so that all 4,096 combinations of  $\overline{\text{RAS}}$  addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic  $\overline{\text{RAS}}$  addressing.



# DRAM

# 256K x 4 DRAM

## FAST PAGE MODE

DRAM

### FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V  $\pm 10\%$  power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle

### OPTIONS

- Timing
- 60ns access
- 70ns access
- 80ns access

- Packages

Plastic DIP (300 mil)  
 Plastic SOJ (300 mil)  
 Plastic TSOP (300 mil)\*  
 Plastic ZIP (350 mil)

### MARKING

- 6  
 - 7  
 - 8

None  
 DJ  
 TG  
 Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Operating Temperature,  $T_A$   
 Commercial (0°C to +70°C)  
 Industrial (-40°C to +85°C)

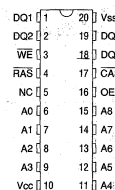
None  
 IT

### GENERAL DESCRIPTION

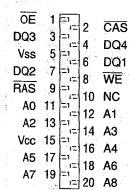
The MT4C4256 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time.  $\overline{\text{RAS}}$  is used to latch the first 9 bits and  $\overline{\text{CAS}}$  the latter 9 bits. READ and WRITE cycles are selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If  $\overline{\text{WE}}$  goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains LOW regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ . This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle. The four data inputs and four data

### PIN ASSIGNMENT (Top View)

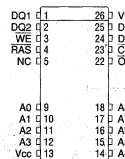
#### 20-Pin DIP (N-2)



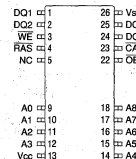
#### 20-Pin ZIP (O-1)



#### 20-Pin SOJ (Q-1)



#### 20-Pin TSOP (R-1)



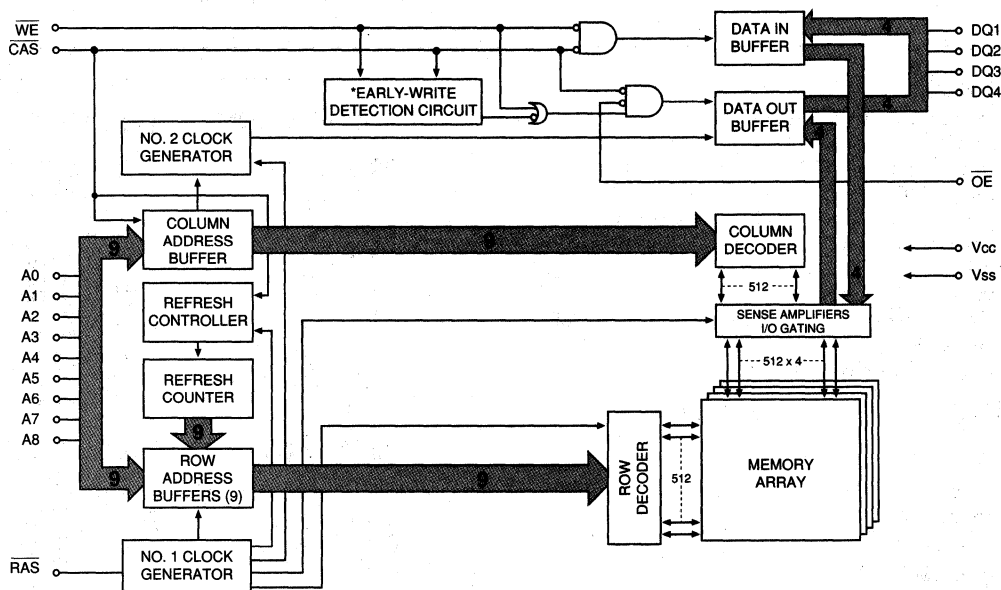
\*Consult factory on availability of reverse pinout TSOP packages

outputs are routed through four pins using common I/O, and pin direction is controlled by  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$ .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by  $\overline{\text{RAS}}$  followed by a column address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing-in different column addresses; thus executing faster memory cycles. Returning  $\overline{\text{RAS}}$  HIGH terminates the FAST PAGE MODE cycle.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR) or HIDDEN refresh) so that all 512 combinations of  $\overline{\text{RAS}}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic  $\overline{\text{RAS}}$  addressing.

# **FUNCTIONAL BLOCK DIAGRAM** **FAST PAGE MODE**



\*NOTE:  $\overline{WE}$  LOW prior to  $\overline{CAS}$  LOW, EW detection circuit output is a HIGH (EARLY-WRITE)  
 $\overline{CAS}$  LOW prior to  $\overline{WE}$  LOW, EW detection circuit output is a LOW (LATE-WRITE)

## **TRUTH TABLE**

| FUNCTION                      |           | RAS   | CAS | WE  | OE  | ADDRESSES |     | DATA IN/OUT       |
|-------------------------------|-----------|-------|-----|-----|-----|-----------|-----|-------------------|
|                               |           |       |     |     |     | r         | c   | DQ1-DQ4           |
| Standby                       |           | H     | H→X | X   | X   | X         | X   | High-Z            |
| READ                          |           | L     | L   | H   | L   | ROW       | COL | Data Out          |
| EARLY-WRITE                   |           | L     | L   | L   | X   | ROW       | COL | Data In           |
| READ-WRITE                    |           | L     | L   | H→L | L→H | ROW       | COL | Data Out, Data In |
| FAST-PAGE-MODE<br>READ        | 1st Cycle | L     | H→L | H   | L   | ROW       | COL | Data Out          |
|                               | 2nd Cycle | L     | H→L | H   | L   | n/a       | COL | Data Out          |
| FAST-PAGE-MODE<br>EARLY-WRITE | 1st Cycle | L     | H→L | L   | X   | ROW       | COL | Data In           |
|                               | 2nd Cycle | L     | H→L | L   | X   | n/a       | COL | Data In           |
| FAST-PAGE-MODE<br>READ-WRITE  | 1st Cycle | L     | H→L | H→L | L→H | ROW       | COL | Data Out, Data In |
|                               | 2nd Cycle | L     | H→L | H→L | L→H | n/a       | COL | Data Out, Data In |
| RAS-ONLY REFRESH              |           | L     | H   | X   | X   | ROW       | n/a | High-Z            |
| HIDDEN<br>REFRESH             | READ      | L→H→L | L   | H   | L   | ROW       | COL | Data Out          |
|                               | WRITE     | L→H→L | L   | L   | X   | ROW       | COL | Data In           |
| CAS-BEFORE-RAS REFRESH        |           | H→L   | L   | X   | X   | X         | X   | High-Z            |

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to V<sub>SS</sub> ..... -1V to +7V  
 Operating Temperature, T<sub>A</sub> (Ambient) ..... 0°C to +70°C  
 Storage Temperature (Plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 3, 4, 6, 7) (V<sub>CC</sub> = 5V ±10%)

| PARAMETER/CONDITION                                                                                    | SYMBOL          | MIN  | MAX                | UNITS | NOTES |
|--------------------------------------------------------------------------------------------------------|-----------------|------|--------------------|-------|-------|
| Supply Voltage                                                                                         | V <sub>CC</sub> | 4.5  | 5.5                | V     | 1     |
| Input High (Logic 1) Voltage, All Inputs                                                               | V <sub>IH</sub> | 2.4  | V <sub>CC</sub> +1 | V     | 1     |
| Input Low (Logic 0) Voltage, All Inputs                                                                | V <sub>IL</sub> | -1.0 | 0.8                | V     | 1     |
| INPUT LEAKAGE CURRENT<br>Any Input 0V ≤ V <sub>IN</sub> ≤ 6.5V<br>(All other pins not under test = 0V) | I <sub>I</sub>  | -2   | 2                  | μA    |       |
| OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ 5.5V)                                  | I <sub>OZ</sub> | -10  | 10                 | μA    |       |
| OUTPUT LEVELS                                                                                          | V <sub>OH</sub> | 2.4  |                    | V     |       |
| Output High Voltage (I <sub>OUT</sub> = -5mA)                                                          | V <sub>OL</sub> |      | 0.4                | V     |       |
| Output Low Voltage (I <sub>OUT</sub> = 4.2mA)                                                          |                 |      |                    |       |       |

| PARAMETER/CONDITION                                                                                                                                                                                        | SYMBOL           | MAX |    |    | UNITS | NOTES |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|----|----|-------|-------|
|                                                                                                                                                                                                            |                  | -6  | -7 | -8 |       |       |
| STANDBY CURRENT: (TTL)<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )                                                                                                                     | I <sub>CC1</sub> | 2   | 2  | 2  | mA    |       |
| STANDBY CURRENT: (CMOS)<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2V$ )                                                                                                             | I <sub>CC2</sub> | 1   | 1  | 1  | mA    |       |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t^1RC = t^1RC$ (MIN))                                      | I <sub>CC3</sub> | 90  | 80 | 70 | mA    | 3, 4  |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t^1PC = t^1PC$ (MIN))                                | I <sub>CC4</sub> | 70  | 60 | 50 | mA    | 3, 4  |
| REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY<br>Average power supply current<br>( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$ : $t^1RC = t^1RC$ (MIN))                             | I <sub>CC5</sub> | 90  | 80 | 70 | mA    | 3     |
| REFRESH CURRENT: $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$<br>Average power supply current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t^1RC = t^1RC$ (MIN)) | I <sub>CC6</sub> | 90  | 80 | 70 | mA    | 3, 5  |

## CAPACITANCE

| PARAMETER                           | SYMBOL          | MIN | MAX | UNITS | NOTES |
|-------------------------------------|-----------------|-----|-----|-------|-------|
| Input Capacitance: A0-A8            | C <sub>I1</sub> |     | 5   | pF    | 2     |
| Input Capacitance: RAS, CAS, WE, OE | C <sub>I2</sub> |     | 7   | pF    | 2     |
| Input/Output Capacitance: DQ        | C <sub>IO</sub> |     | 7   | pF    | 2     |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V<sub>CC</sub> = 5V ±10%)

| AC CHARACTERISTICS                           |                   | -6  |         | -7  |         | -8  |         | UNITS | NOTES |
|----------------------------------------------|-------------------|-----|---------|-----|---------|-----|---------|-------|-------|
| PARAMETER                                    | SYM               | MIN | MAX     | MIN | MAX     | MIN | MAX     |       |       |
| Random READ or WRITE cycle time              | <sup>t</sup> RC   | 110 |         | 130 |         | 150 |         | ns    |       |
| READ-WRITE cycle time                        | <sup>t</sup> RWC  | 165 |         | 185 |         | 205 |         | ns    |       |
| FAST-PAGE-MODE READ or WRITE cycle time      | <sup>t</sup> PC   | 40  |         | 40  |         | 45  |         | ns    |       |
| FAST-PAGE-MODE READ-WRITE cycle time         | <sup>t</sup> PRWC | 90  |         | 95  |         | 100 |         | ns    |       |
| Access time from RAS                         | <sup>t</sup> RAC  |     | 60      |     | 70      |     | 80      | ns    | 14    |
| Access time from CAS                         | <sup>t</sup> CAC  |     | 20      |     | 20      |     | 20      | ns    | 15    |
| Output Enable                                | <sup>t</sup> OE   |     | 20      |     | 20      |     | 20      | ns    |       |
| Access time from column address              | <sup>t</sup> AA   |     | 30      |     | 35      |     | 40      | ns    |       |
| Access time from CAS precharge               | <sup>t</sup> CPA  |     | 35      |     | 40      |     | 45      | ns    |       |
| RAS pulse width                              | <sup>t</sup> RAS  | 60  | 100,000 | 70  | 100,000 | 80  | 100,000 | ns    |       |
| RAS pulse width (FAST PAGE MODE)             | <sup>t</sup> RASP | 60  | 100,000 | 70  | 100,000 | 80  | 100,000 | ns    |       |
| RAS hold time                                | <sup>t</sup> RSH  | 20  |         | 20  |         | 20  |         | ns    |       |
| RAS precharge time                           | <sup>t</sup> RP   | 40  |         | 50  |         | 60  |         | ns    |       |
| CAS pulse width                              | <sup>t</sup> CAS  | 20  | 100,000 | 20  | 100,000 | 20  | 100,000 | ns    |       |
| CAS hold time                                | <sup>t</sup> CSH  | 60  |         | 70  |         | 80  |         | ns    |       |
| CAS precharge time                           | <sup>t</sup> CPN  | 10  |         | 10  |         | 10  |         | ns    | 16    |
| CAS precharge time (FAST PAGE MODE)          | <sup>t</sup> CP   | 10  |         | 10  |         | 10  |         | ns    |       |
| RAS to CAS delay time                        | <sup>t</sup> RCD  | 20  | 40      | 20  | 50      | 20  | 60      | ns    | 17    |
| CAS to RAS precharge time                    | <sup>t</sup> CRP  | 5   |         | 5   |         | 5   |         | ns    |       |
| Row address setup time                       | <sup>t</sup> ASR  | 0   |         | 0   |         | 0   |         | ns    |       |
| Row address hold time                        | <sup>t</sup> RAH  | 10  |         | 10  |         | 10  |         | ns    |       |
| RAS to column address delay time             | <sup>t</sup> RAD  | 15  | 30      | 15  | 35      | 15  | 40      | ns    | 18    |
| Column address setup time                    | <sup>t</sup> ASC  | 0   |         | 0   |         | 0   |         | ns    |       |
| Column address hold time                     | <sup>t</sup> CAH  | 15  |         | 15  |         | 15  |         | ns    |       |
| Column address hold time (referenced to RAS) | <sup>t</sup> AR   | 45  |         | 55  |         | 60  |         | ns    |       |
| Column address to RAS lead time              | <sup>t</sup> RAL  | 30  |         | 35  |         | 40  |         | ns    |       |
| Read command setup time                      | <sup>t</sup> RCS  | 0   |         | 0   |         | 0   |         | ns    |       |
| Read command hold time (referenced to CAS)   | <sup>t</sup> RCH  | 0   |         | 0   |         | 0   |         | ns    | 19    |
| Read command hold time (referenced to RAS)   | <sup>t</sup> RRH  | 0   |         | 0   |         | 0   |         | ns    | 19    |
| CAS to output in Low-Z                       | <sup>t</sup> CLZ  | 0   |         | 0   |         | 0   |         | ns    |       |

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ( $V_{CC} = 5V \pm 10\%$ )

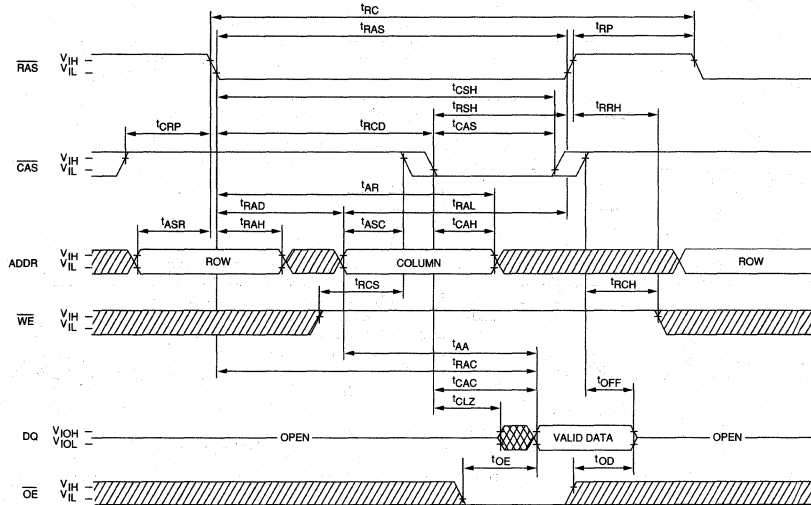
| AC CHARACTERISTICS                                                                   |           | -6  |     | -7  |     | -8  |     | UNITS | NOTES  |
|--------------------------------------------------------------------------------------|-----------|-----|-----|-----|-----|-----|-----|-------|--------|
| PARAMETER                                                                            | SYM       | MIN | MAX | MIN | MAX | MIN | MAX |       |        |
| Output buffer turn-off delay                                                         | $t_{OFF}$ | 0   | 20  | 0   | 20  | 0   | 20  | ns    | 20, 26 |
| Output disable                                                                       | $t_{OD}$  |     | 15  |     | 20  |     | 20  | ns    | 26     |
| WE command setup time                                                                | $t_{WCS}$ | 0   |     | 0   |     | 0   |     | ns    | 21     |
| Write command hold time                                                              | $t_{WCH}$ | 10  |     | 15  |     | 15  |     | ns    |        |
| Write command hold time<br>(referenced to $\overline{RAS}$ )                         | $t_{WCR}$ | 45  |     | 55  |     | 60  |     | ns    |        |
| Write command pulse width                                                            | $t_{WP}$  | 10  |     | 15  |     | 15  |     | ns    |        |
| Write command to $\overline{RAS}$ lead time                                          | $t_{RWL}$ | 20  |     | 20  |     | 20  |     | ns    |        |
| Write command to $\overline{CAS}$ lead time                                          | $t_{CWL}$ | 20  |     | 20  |     | 20  |     | ns    |        |
| Data-in setup time                                                                   | $t_{DS}$  | 0   |     | 0   |     | 0   |     | ns    | 22     |
| Data-in hold time                                                                    | $t_{DH}$  | 15  |     | 15  |     | 15  |     | ns    | 22     |
| Data-in hold time<br>(referenced to $\overline{RAS}$ )                               | $t_{DHR}$ | 45  |     | 55  |     | 60  |     | ns    |        |
| $\overline{RAS}$ to WE delay time                                                    | $t_{RWD}$ | 85  |     | 100 |     | 110 |     | ns    | 21     |
| Column address<br>to WE delay time                                                   | $t_{AWD}$ | 60  |     | 65  |     | 70  |     | ns    | 21     |
| $\overline{CAS}$ to WE delay time                                                    | $t_{CWD}$ | 40  |     | 50  |     | 55  |     | ns    | 21     |
| Transition time (rise or fall)                                                       | $t_T$     | 3   | 50  | 3   | 50  | 3   | 50  | ns    | 9, 10  |
| Refresh period (512 cycles)                                                          | $t_{REF}$ |     | 8   |     | 8   |     | 8   | ms    |        |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time                                  | $t_{RPC}$ | 0   |     | 0   |     | 0   |     | ns    |        |
| $\overline{CAS}$ setup time<br>( $\overline{CAS}$ -BEFORE- $\overline{RAS}$ refresh) | $t_{CSR}$ | 10  |     | 10  |     | 10  |     | ns    | 5      |
| $\overline{CAS}$ hold time<br>( $\overline{CAS}$ -BEFORE- $\overline{RAS}$ refresh)  | $t_{CHR}$ | 10  |     | 15  |     | 15  |     | ns    | 5      |
| $\overline{OE}$ hold time from WE during<br>READ-MODIFY-WRITE cycle                  | $t_{OEH}$ | 15  |     | 20  |     | 20  |     | ns    | 25     |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during<br>HIDDEN REFRESH cycle       | $t_{ORD}$ | 0   |     | 0   |     | 0   |     | ns    | 24     |

**DRAM**

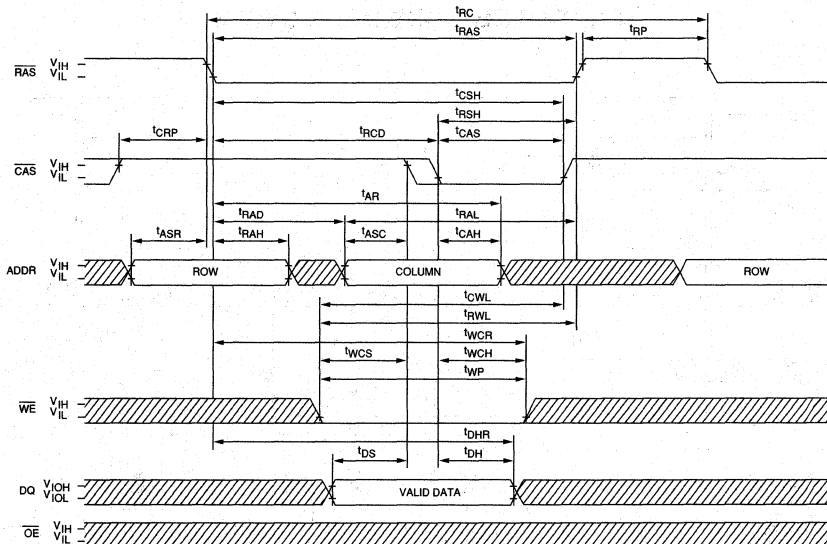
## NOTES

1. All voltages referenced to  $V_{SS}$ .
2. This parameter is sampled.  $V_{CC} = 5V \pm 10\%$ ,  $f = 1\text{ MHz}$ .
3.  $I_{CC}$  is dependent on cycle rates.
4.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of  $100\mu s$  is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 'REF refresh requirement is exceeded.
8. AC characteristics assume  $t_T = 5ns$ .
9.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
10. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
11. If  $\overline{CAS} = V_{IH}$ , data output is High-Z.
12. If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and  $100pF$ .
14. Assumes that  $t_{RCD} < t_{RCD}(\text{MAX})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
15. Assumes that  $t_{RCD} \geq t_{RCD}(\text{MAX})$ .
16. If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer,  $\overline{CAS}$  must be pulsed HIGH for  $t_{CPN}$ .
17. Operation within the  $t_{RCD}(\text{MAX})$  limit ensures that  $t_{RAC}(\text{MAX})$  can be met.  $t_{RCD}(\text{MAX})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{MAX})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
18. Operation within the  $t_{RAD}(\text{MAX})$  limit ensures that  $t_{RAC}(\text{MIN})$  and  $t_{CAC}(\text{MIN})$  can be met.  $t_{RAD}(\text{MAX})$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{MAX})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
19. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
20.  $t_{OFF}(\text{MAX})$  defines the time at which the output achieves the open circuit condition, and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
21.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.  $t_{WCS}$  applies to EARLY-WRITE cycles.  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  apply to READ-MODIFY-WRITE cycles. If  $t_{WCS} \geq t_{WCS}(\text{MIN})$ , the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{MIN})$ ,  $t_{AWD} \geq t_{AWD}(\text{MIN})$  and  $t_{CWD} \geq t_{CWD}(\text{MIN})$ , the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate.  $\overline{OE}$  held HIGH and  $\overline{WE}$  taken LOW after  $\overline{CAS}$  goes LOW results in a LATE-WRITE ( $\overline{OE}$  controlled) cycle.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to  $\overline{CAS}$  leading edge in EARLY-WRITE cycles and  $\overline{WE}$  leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If  $\overline{OE}$  is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{WE} = \text{LOW}$  and  $\overline{OE} = \text{HIGH}$ .
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OD}$  and  $t_{OE}$  met ( $\overline{OE}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if  $\overline{CAS}$  remains LOW and  $\overline{OE}$  is taken back LOW after  $t_{OE}$  is met. If  $\overline{CAS}$  goes HIGH prior to  $\overline{OE}$  going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once  $t_{OD}$  or  $t_{OFF}$  occur. If  $\overline{CAS}$  goes HIGH first,  $\overline{OE}$  becomes a "don't care." If  $\overline{OE}$  goes HIGH and  $\overline{CAS}$  stays LOW,  $\overline{OE}$  is not a "don't care;" and the DQs will provide the previously read data if  $\overline{OE}$  is taken back LOW (while  $\overline{CAS}$  remains LOW).

# **READ CYCLE**

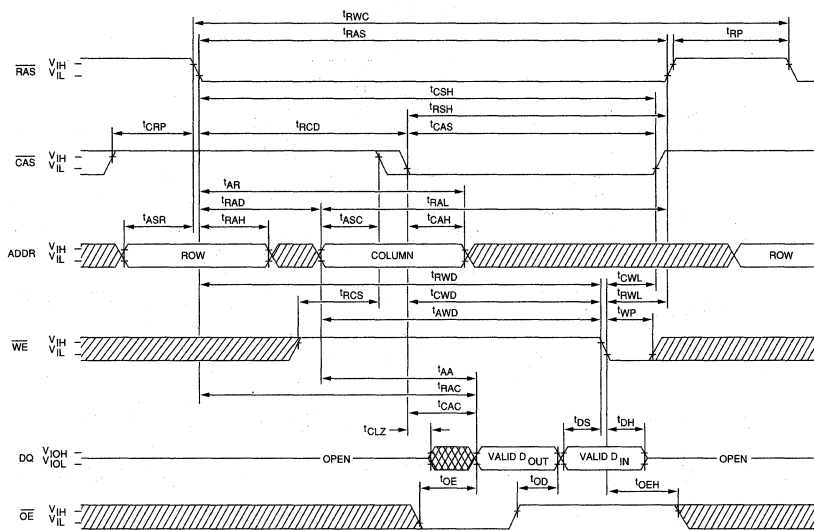


# **EARLY-WRITE CYCLE**

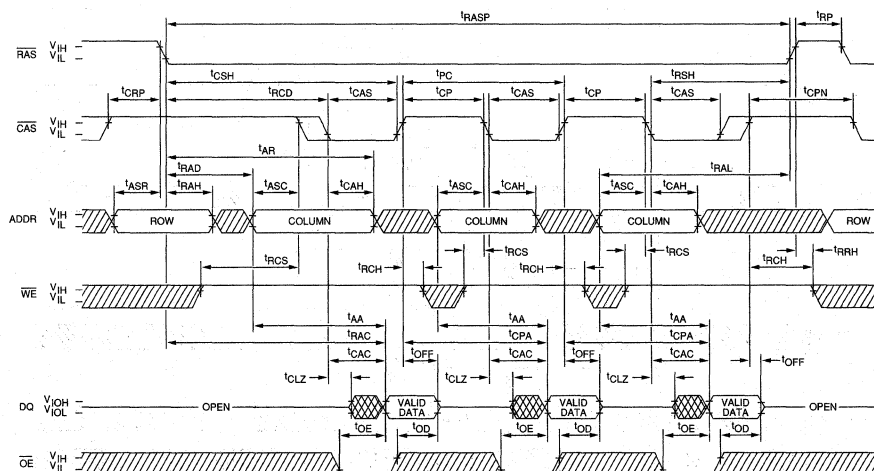


DON'T CARE  
 UNDEFINED

# **READ-WRITE CYCLE** (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

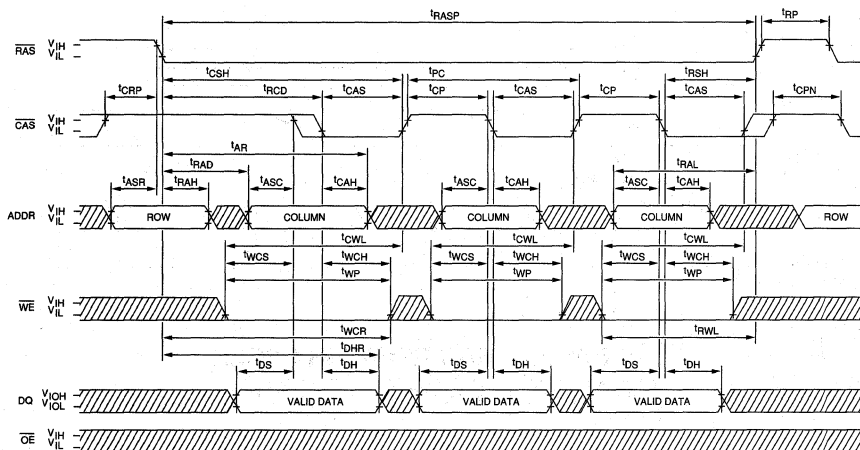


# **FAST-PAGE-MODE READ CYCLE**

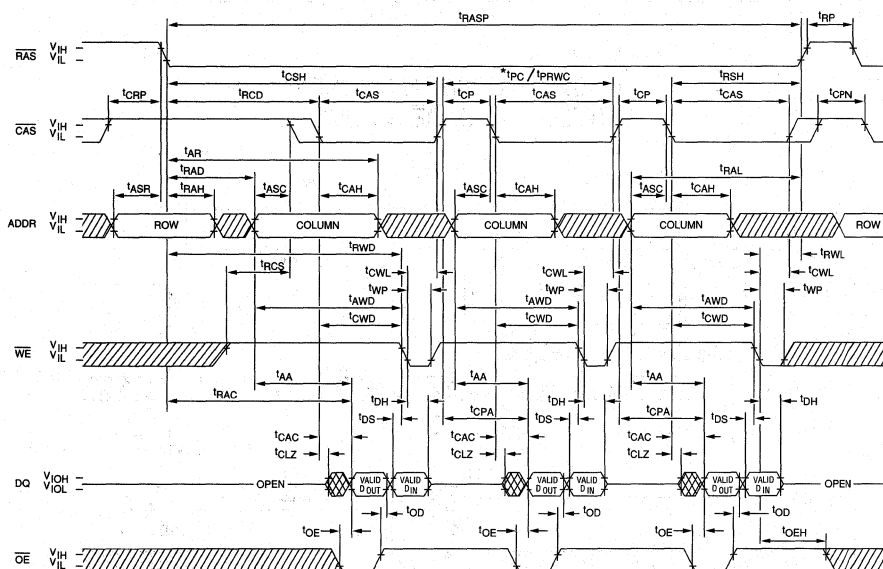


DON'T CARE  
 UNDEFINED

## FAST-PAGE-MODE EARLY-WRITE CYCLE



### FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

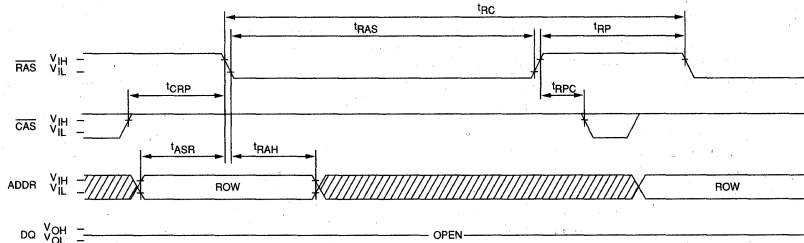


\*tPC is for LATE-WRITE only.

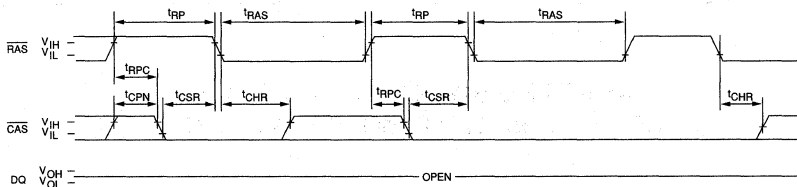
 DON'T CARE

 UNDEFINED

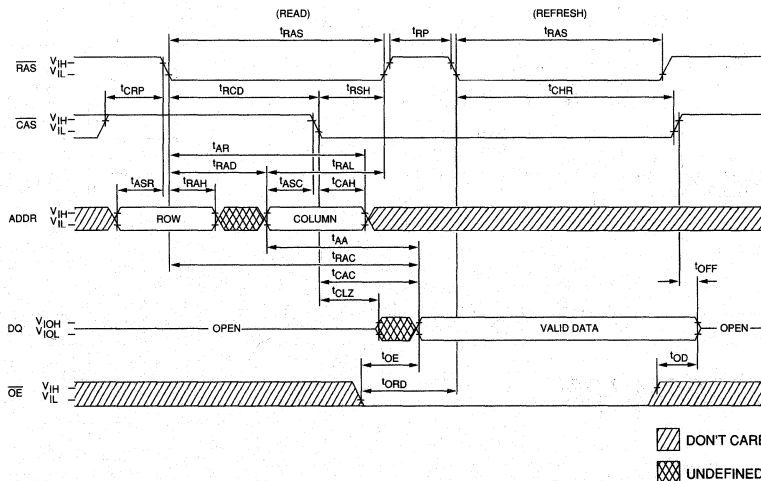
**RAS-ONLY REFRESH CYCLE**  
(ADDR = A0-A8;  $\overline{WE}$  = DON'T CARE)



**$\overline{CAS}$ -BEFORE- $\overline{RAS}$  REFRESH CYCLE**  
(A0-A8,  $\overline{WE}$  and  $\overline{OE}$  = DON'T CARE)



**HIDDEN REFRESH CYCLE <sup>24</sup>**  
( $\overline{WE}$  = HIGH;  $\overline{OE}$  = LOW)



DON'T CARE  
 UNDEFINED