

SAMSUNG

DRAM DATA BOOK

1996



LORI STEINTHAL

I² INCORPORATED

MANUFACTURERS REPRESENTATIVES

3255 Scott Boulevard
Suite 1-102
Santa Clara, CA 95054-3013

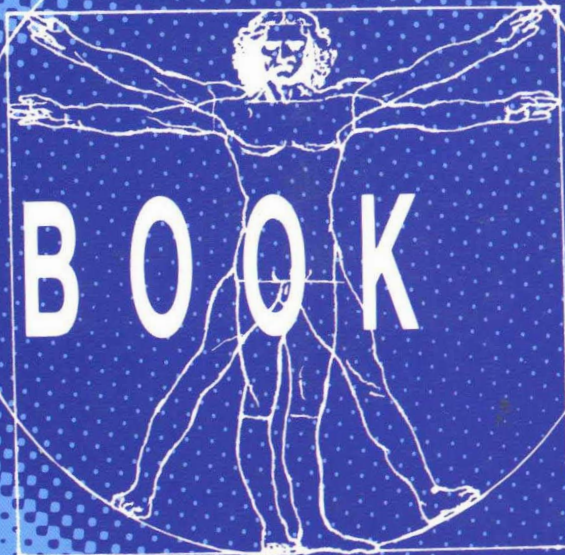
Tel: (408) 988-3400

Fax: (408) 988-2079

1110-5121
Dec. 1995

1996

DATA BOOK



DRAM

SAMSUNG

PRINTED IN KOREA

Circuit diagrams utilizing SAMSUNG products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of SAMSUNG or others. SAMSUNG reserves the right to change device specifications.

Certified ISO 9001



Certificate No FM 24651

TABLE OF CONTENTS

I. General Information

1. Introduction	13
2. Product Guide	21
3. Ordering Information	25

II. Data sheets

1M DRAM

- KM41C1000D	1Mx1, 5V, F/P	31
- KM44C256D	256KX4, 5V, F/P	38
- KM48C128	128KX8, 5V, F/P	45
- KM48C124	128KX8, 5V, EDO	52
- KM416C60	64KX16, 5V, F/P	59
- KM416C64	64KX16, 5V, EDO	66

4M DRAM

- KM41C4000C, KM41V4000C	4Mx1, 5V/3.3V, F/P	75
- KM44C1000C, KM44V1000C	1Mx4, 5V/3.3V, F/P	83
- KM44C1003C	1Mx4, 5V, Quad $\overline{\text{CAS}}$, F/P	91
- KM44C1004C, KM44V1004C	1Mx4, 5V/3.3V, EDO	99
- KM44C1005C	1Mx4, 5V, Quad $\overline{\text{CAS}}$, EDO	107
- KM48C512B, KM48V512B	512Kx8, 5V/3.3V, F/P	115
- KM48C514B, KM48V514B	512KX8, 5V/3.3V, EDO	122
- KM416C256B, KM416V256B	256Kx16, 5V/3.3V, F/P	129
- KM416C254B, KM416V254B	256Kx16, 5V/3.3V, EDO	137
- KM48C512D, KM48V512D	* 512Kx8, 5V/3.3V, F/P	145
- KM48C514D, KM48V514D	* 512KX8, 5V/3.3V, EDO	152
- KM416C256D, KM416V256D	* 256Kx16, 5V/3.3V, F/P	159
- KM416C254D, KM416V254D	* 256Kx16, 5V/3.3V, EDO	167

* The D-version is under development and will take the place of B-version from March 1996.

TABLE OF CONTENTS(Continued)

16M DRAM

- KM41C16000B	-----16Mx1, 5V, F/P	----- 177
KM41V16000B	16Mx1, 3.3V, F/P	
- KM44C4000B, KM44C4100B	----- 4Mx4, 5V, F/P	----- 185
KM44V4000B, KM44V4100B	4Mx4, 3.3V, F/P	
- KM44C4003B, KM44C4103B	----- 4Mx4, 5V, Quad $\overline{\text{CAS}}$, F/P	----- 193
- KM44C4004B, KM44C4104B	----- 4Mx4, 5V, EDO	----- 201
KM44V4004B, KM44V4104B	4Mx4, 3.3V, EDO	
- KM44C4005B, KM44C4105B	----- 4Mx4, 5V, Quad $\overline{\text{CAS}}$, EDO	----- 209
- KM48C2000B, KM48C2100B	----- 2Mx8, 5V, F/P	----- 217
KM48V2000B, KM48V2100B	2Mx8, 3.3V, F/P	
- KM48C2004B, KM48C2104B	----- 2Mx8, 5V, EDO	----- 225
KM48V2004B, KM48V2104B	2Mx8, 3.3V, EDO	
- KM416C1000A, KM416C1200A	-----1Mx16, 5V, F/P(2nd gen.)	----- 233
KM416V1000A, KM416V1200A	1Mx16, 3.3V, F/P(2nd gen.)	
- KM416C1004A, KM416C1204A	-----1Mx16, 5V, EDO (2nd gen.)	----- 241
KM416V1004A, KM416V1204A	1Mx16, 3.3V, EDO (2nd gen.)	
- KM416C1000B, KM416C1200B	-----*1Mx16, 5V, F/P(3rd gen.)	----- 249
KM416V1000B, KM416V1200B	1Mx16, 3.3V, F/P(3rd gen.)	
- KM416C1004B, KM416C1204B	-----*1Mx16, 5V, EDO (3rd gen.)	----- 257
KM416V1004B, KM416V1204B	1Mx16, 3.3V, EDO (3rd gen.)	

* The B-version is under development and will take the place of A-version from May 1996.

64M DRAM

- KM44V16000A, KM44V16100A	----- 16Mx4, 3.3V, F/P	----- 267
- KM44V16004A, KM44V16104A	----- 16Mx4, 3.3V, EDO	----- 275
- KM44C16000A, KM44C16100A	----- 16Mx4, 5V, F/P	----- 283
- KM44C16004A, KM44C16104A	----- 16Mx4, 5V, EDO	----- 291
- KM48V8000A, KM48V8100A	----- 8Mx8, 3.3V, F/P	----- 299
- KM48V8004A, KM48V8104A	----- 8Mx8, 3.3V, EDO	----- 307
- KM48C8000A, KM48C8100A	----- 8Mx8, 5V, F/P	----- 315
- KM48C8004A, KM48C8104A	----- 8Mx8, 5V, EDO	----- 323
- KM416V4000A, KM416V4100A	----- 4MX16, 3.3V, F/P	----- 331
- KM416V4004A, KM416V4104A	----- 4Mx16, 3.3V, EDO	----- 340

TABLE OF CONTENTS (Continued)

III. Timing Chart

- F/P Mode, x1 Device	351
- F/P Mode, x4 and x8 Device	365
- F/P Mode, x16($2\overline{CAS}$) Device	379
- F/P Mode, x16($2\overline{WE}$) Device	407
- F/P Mode, Quad $\overline{CAS}$ Device	431
- EDO Mode, x4 and x8 Device	445
- EDO Mode, x16($2\overline{CAS}$) Device	461
- EDO Mode, x16($2\overline{WE}$) Device	491
- EDO Mode, Quad $\overline{CAS}$ Device	515

IV. Package Dimension 529

V. Sales Offices and Manufacturer's Representatives 543

Changed Point in '96 DRAM Databook (Compared with '95 databook)

	Changed Point in '96 DRAM databook			Remarks
General	- Remove TSOP II(reverse) package - Remove 80ns version in 5V product - Remove SC Mode, WPB Mode product - Remove 512Kx9 and 256Kx18 product			
Generation Change	Device	in '95	in '96	
	- 128Kx8, 64Kx16 - 4Mx1, 1Mx4 - 512Kx8, 256Kx16 - 16Mx1, 4Mx4, 2Mx8 - 1Mx16 - 16Mx4, 8Mx8 - 4Mx16	- None - C-version - B-version - A-version - A-version - 1st gen. - None	- 1st gen. - C-Version - D-Version - B-Version - A-Version & B-version - A-version (2nd gen.) - A-version	- Add EDO Quad $\overline{\text{CAS}}$ product - Remove x9 & x18 product - Add EDO Quad $\overline{\text{CAS}}$ product - B-ver. will be available from 3Q '96 - Add 5V 64M DRAM : x4(4K) and x8(K)
1M	- Add 128Kx8(FP/EDO), 64Kx16(2WE, FP/EDO)			
4M C-ver	- Add EDO Quad $\overline{\text{CAS}}$ product - Remove DIP and ZIP package - Remove SC, WPB Mode product			
4M B/W	- Remove 512Kx9 and 256Kx18 product			
16M (x1,x4,x8)	- Remove SC Mode WPB Mode product - Add EDO Quad $\overline{\text{CAS}}$ product - Change the CMOS Standby current(ICC5) of Normal-power version from 1mA to 0.5mA			- Changed package size from 400mil to 300mil
16M (1Mx16)	- 50ns version will be available in B-version(3rd gen.) from May 1996. - Change the CMOS Standby current(ICC5) of Normal-power version from 1mA to 0.5mA			
64M (x4,x8,x16)	- Add 4Mx16 product - Add 5V product - Change the Refresh cycle of Low -power version from 256ms to 128ms			

In "Remove ~", "~" means that "~" is not supported anymore.

In "Add ~", "~" means that "~" is new product and is available from '96.

2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 2,097,152 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 2Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

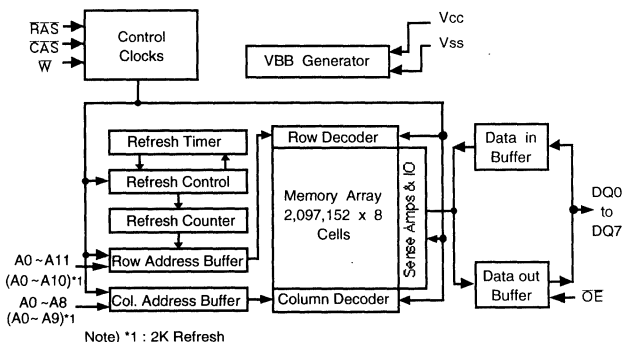
- Part Identification
 - KM48C2000B/B-L (5V, 4K Ref.)
 - KM48C2100B/B-L (5V, 2K Ref.)
 - KM48V2000B/B-L (3.3V, 4K Ref.)
 - KM48V2100B/B-L (3.3V, 2K Ref.)
- Active Power Dissipation Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	-	-
- Refresh cycles

Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C2000B	5V	4K	64ms	128ms
V2000B	3.3V			
C2100B	5V	2K	32ms	
V2100B	3.3V			
- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	3.3V
- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V $\pm$ 10% power supply (5V product)
- Single +3.3V $\pm$ 0.3V power supply (3.3V product)

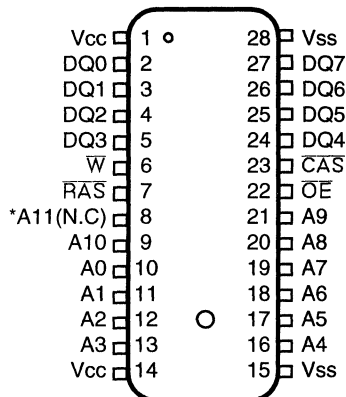
FUNCTIONAL BLOCK DIAGRAM



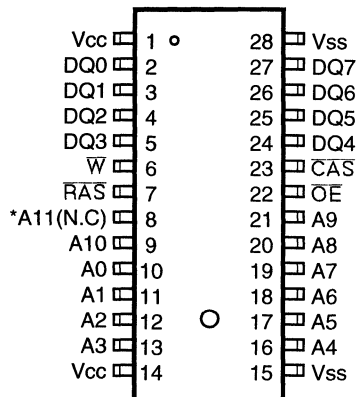
SAMSUNG ELECTRONIC CO., LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• KM48C/V20(1)00BK



• KM48C/V20(1)00BS



* A11 is N.C for KM48C/V2100B (5V/3.3V, 2K Ref. product)

K : 300mil 28 SOJ

S : 300mil 28 TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K product)
A0 ~ A10	Address Inputs (2K product)
DQ0 ~ 7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	2.4	-	V _{CC} +1 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}.

*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.3V, all other pins not under test=0 volt.)	I _{I(L)}	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	- 5	5	μA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.5V, all other pins not under test=0 volt.)	I _{I(L)}	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	- 5	5	μA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM48V2000 B	KM48V2100B	KM48C2000B	KM48C2100B	
Icc1	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
Icc2	Normal L	Don't care	1	1	2	2	mA
			1	1	1	1	mA
Icc3	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
Icc4	Don't care	-5	-	-	80	90	mA
		-6	70	80	70	80	mA
		-7	60	70	60	70	mA
		-8	50	60	-	-	mA
Icc5	Normal L	Don't care	0.5	0.5	1	1	mA
			0.3	0.3	0.3	0.3	mA
Icc6	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	-	-	mA
Icc7	L	Don't care	450	400	450	400	μA
Icc8	L	Don't care	250	250	300	300	μA

Icc1* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

Icc2 : Standby Current ($\overline{RAS}=\overline{CAS}=W=V_{IH}$)

Icc3* : $\overline{RAS}$ -only Refresh Current ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ cycling @tRC=min.)

Icc4* : Fast Page Mode Current ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address cycling @tPC=min.)

Icc5 : Standby Current ($\overline{RAS}=\overline{CAS}=W=V_{CC}-0.2V$)

Icc6* : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})= $0.2V$, $\overline{CAS}=0.2V$

Din = Don't care, tRC = 31.25μs(4K/L-ver), 62.5μs(2K/L-ver),

tRAS=tRASmin~300ns

Icc8 : Self Refresh Current

$\overline{RAS}=\overline{CAS}=0.2V$, $W=\overline{OE}=A0 \sim A11 = V_{CC}-0.2V$ or $0.2V$, $DQ0 \sim DQ7 = V_{CC}-0.2V$, $0.2V$ or Open

* NOTE : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3, and Icc6, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In Icc4, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, See note 1,2)Test condition (5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.4/0.4\text{V}$ Test condition (3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.0/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{\text{CAS}}$	tCAC		13		15		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	5
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, See note 1,2)Test condition (5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.4/0.4\text{V}$ Test condition (3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.0/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8
Data hold time	tDH	10		10		15		15		ns	8
Refresh period (2K, Normal)	tREF		32		32		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
CAS to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	6
RAS to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	6
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	6
CAS precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	6
CAS set-up time (CAS-before-RAS refresh)	tCSR	5		5		5		5		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (CBR counter test cycle)	tCPT	20		20		30		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
CAS precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
RAS pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	
OE to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from OE	tOEZ	0	13	0	15	0	20	0	20	ns	5
OE command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	10
$\overline{W}$ to RAS precharge time ($\overline{C}$ -B-R refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to RAS hold time ($\overline{C}$ -B-R refresh)	tWRH	10		10		10		10		ns	
RAS pulse width ($\overline{C}$ -B-R self refresh)	tRASS	100		100		100		100		us	12
RAS precharge time ($\overline{C}$ -B-R self refresh)	tRPS	90		110		130		150		ns	12
CAS hold time ($\overline{C}$ -B-R self refresh)	tCHS	-50		-50		-50		-50		ns	12

Note) *1 : 5V only, *2 : 3.3V only

TEST MODE CYCLE

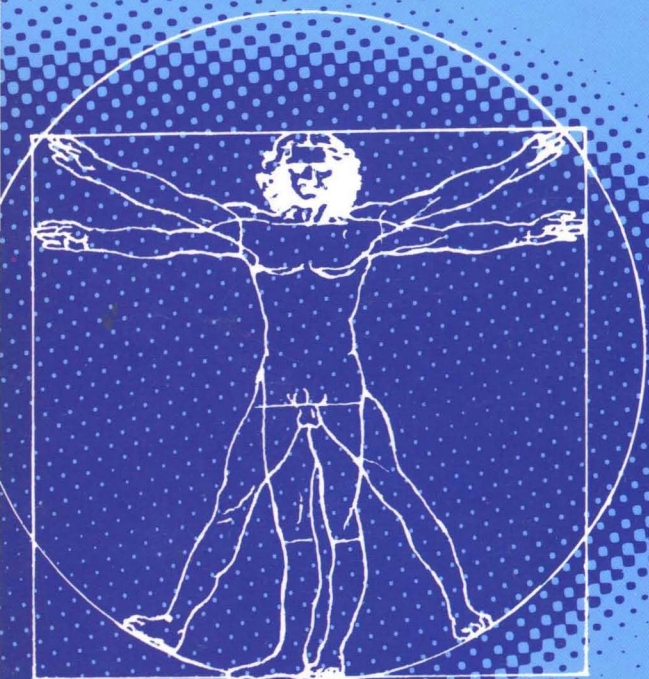
(Note. 10, 11)

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8 ^{*2}		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	tRAC		55		65		75		85	ns	3,4,9
Access time from $\overline{\text{CAS}}$	tCAC		18		20		25		25	ns	3,4
Access time from column address	tAA		30		35		40		45	ns	3,9
$\overline{\text{RAS}}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{\text{CAS}}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		45		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	41		45		55		55		ns	6
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	78		90		105		115		ns	6
Column address to $\overline{\text{W}}$ delay time	tAWD	53		60		70		75		ns	6
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	58		65		75		80		ns	6
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{\text{CAS}}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only, *2 : 3.3V only

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
6. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPWD} \geq t_{CPWD}(\min)$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of t_{RAC} , t_{AA} and t_{CAC} are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$ -Before- ~~$\overline{RAS}$~~ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.



HEAD OFFICE

8/11FL., SAMSUNG MAIN BLDG.
250, 2-KA, TAEYUNG-RO,
CHUNG-KU, SEOUL-KOREA
C.P.O. BOX 8780
TELEX: KORSST K27970
TEL: 82(2)776-0114
FAX: 82(2)753-0967

SEMICONDUCTOR BUSINESS SALES & MARKETING DIVISION

16TH FL., SEVERANCE BLDG., 84-11,
5-KA, NAMDAEMOON-RO, CHUNG-KU
SEOUL, KOREA
TEL: 82(2)776-0114
FAX: 82(2)751-6061

GUMI BRANCH

5TH FL., SAMSUNG INSURANCE BLDG.,
71, SONGJEONG-DONG, GUMI
KYUNGSANGBUK-DO, KOREA
TEL: 82(546)457-2525
FAX: 82(546)457-2460

SAMSUNG SEMICONDUCTOR INC.

3655 NORTH FIRST STREET
SAN JOSE, CA 95134, USA
TEL: 1(408)954-7000
FAX: 1(408)954-7286

SAMSUNG SEMICONDUCTOR EUROPE GMBH

AM UNISYSPARK 1,
65843 SULZBACH/TS, GERMANY
TEL: 49(6196)58206
FAX: 49(6196)750345

SAMSUNG ELECTRONICS JAPAN CO., LTD.

HAMACHO CENTER BLDG.,
31-1, NIHONBASHI-HAMACHO 2-CHOME,
CHUO-KU, TOKYO 103, JAPAN
TEL: 81(3)5641-9850
FAX: 81(3)5641-9851

SAMSUNG ELECTRONICS HONGKONG CO., LTD.

65TH FL., CENTRAL PLAZA,
18 HARBOUR ROAD,
WANCHAI, HONG KONG
TELEX: 80303 SSTC HX
TEL: 852-2862-6900
FAX: 852-2866-1343

SAMSUNG ELECTRONICS TAIPEI OFFICE

TWTC INT'L TRADE BLDG., RM2508
25F, NO.333, KEELUNG RD., SEC.1,
TAIPEI, TAIWAN, R.O.C.
TEL: 886(2)757-7040
FAX: 886(2)757-7286

SAMSUNG ELECTRONICS SINGAPORE PTE LTD.

80, ROBINSON ROAD, #20-00,
SINGAPORE 0106
TEL: 65-535-2808
FAX: 65-227-2792

SAMSUNG ELECTRONICS CO., LTD. SHANGHAI OFFICE

SUITE 4034,
SHERATON HUATING HOTEL,
1200 CAOXIBEILU, SHANGHAI
200030, CHINA
TEL: 86(21)439-0707
FAX: 86(21)439-3798

