

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

DECLARATION OF STEPHEN W. MELVIN

Case No. IPR2023-00516

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 6,157,589 (the “’589 Patent”)
1002	U.S. Prosecution History of the ’589 Patent
1003	Declaration of Stephen W. Melvin
1004	U.S. Patent No. 5,559,753 to Kocis entitled “Apparatus and Method for Preventing Bus Contention During Power-Up in a Computer System With Two or More DRAM Banks” (“Kocis”)
1005	U.S. Patent No. 5,774,402 to Lee entitled “Initialization Circuit for a Semiconductor Memory Device” (“Lee”)
1006	JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Compilation of Releases 1 through 7, dated January 1997 (“JESD 21-C”)
1007	U.S. Patent No. 5,703,510 to Iketani et al. entitled “Power On Reset Circuit For Generating Reset Signal at Power On” (“Iketani”)
1008	Prosecution History of EPO Patent Application No. 99 113 048.5 (Original)
1009	Excerpt of Prosecution History of EPO Patent Application No. 99 113 048.5 (Original)
1010	Excerpt of Prosecution History of EPO Patent Application No. 99 113 048.5 (English Translation)
1011	Japanese Patent Publication No. JP 09 106668 A to Samsung Electronics Co. Ltd. dated April 22, 1997 (“Tetsuka”)
1012	Declaration of Julie Carson
1013	JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Release 7, dated January 1997
1014	Scheduling Order, <i>Polaris Innovations Limited v. Xilinx, Inc.</i> , 1:22-cv-00174-RGA, Docket No. 20 (May 31, 2022)
1015	United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf
1016	Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)
1017	Excerpt of Micron Technology, Inc., “DRAM Data Book” (1992)

Exhibit No.	Description
1018	Excerpt of Samsung Electronics Co., Ltd., “Data Book: DRAM” (Dec. 1995)
1019	Samsung Electronics, “4M x 8Bit x 4 Banks Synchronous DRAM” Doc. No. KM48S16030, Rev. 2 (March 1998)

I. Introduction

1. I have prepared this Declaration in connection with Xilinx, Inc.'s Petition for *Inter Partes* Review of U.S. Patent No. 6,157,589 (the "'589 Patent") (Ex. 1001), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the '589 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have been retained by Xilinx, Inc. ("Xilinx" or "Petitioner") as an expert in the fields of computer engineering, computer memory systems and related technologies. My employer is being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in Xilinx, the '589 Patent or the owner of the '589 Patent.

II. Background and Qualifications

4. I received a Ph.D. in Computer Science from the University of California at Berkeley in 1991 and a B.S. in Electrical Engineering and Computer Science from the University of California at Berkeley in 1982. I have more than 40 years of experience in computer science and computer engineering. I am an inventor on over 45 patents, and I am a registered patent agent before the USPTO.

5. My Ph.D. research areas included high-performance computer architecture and microarchitecture and microcode-based system performance analysis tools. From September 2001 through April 2002, I was a Visiting Scholar at the University of Texas, Austin, where I directed graduate students in research in the area of high-performance computer architecture.

6. In May 2001, I co-founded and was the Chief Architect of Flowstorm, Inc., a start-up company based in Silicon Valley, where I defined and guided the overall chip architecture for a multithreaded packet processor. From March 2000 through May 2001, I worked as the Senior CPU Architect at Clearwater Networks, where I was involved in defining the architecture and microarchitecture of Clearwater's CNP810S multithreaded network processor. Both of those professional experiences required a deep understanding of memory devices and memory interfacing techniques, including DRAM devices conforming to JEDEC standards.

7. From 1983 to 2020, I was the President of Zytek Communications Corporation ("Zytek"). Zytek was an engineering, consulting, and small-scale manufacturing company that provided intellectual property consulting services as well as services related to the design, implementation, and testing of embedded systems. Zytek's general areas of activity included industrial control and measurement, Internet-related services, hard disk analysis and file recovery, and

computer engineering research services. Through my work at Zytex, I have designed numerous microprocessor-based embedded systems, including analog and digital circuit design, firmware development for embedded microcontrollers, and software development for host interfacing, product development, and debugging. My designs for embedded systems have all involved an understanding of memory devices and interfacing between microprocessors and memory devices.

8. I am currently employed as a Principal with Exponent, Inc., which is an international multidisciplinary engineering and scientific consulting firm.

9. I am a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Association for Computing Machinery (ACM).

10. I served as General Chair of the 45th Annual International Symposium on Microarchitecture (Micro-45), held in Vancouver in December of 2012. I also served as co-chair of the 29th Annual International Symposium on Microarchitecture (Micro-29), held in Paris in December of 1996.

11. Additional details regarding my employment and academic history are included in my curriculum vitae, attached hereto as Appendix A.

III. Documents and Materials Considered

12. In forming my opinions, in addition to my knowledge, education, training, and experience, I have considered the materials cited in this Declaration

and the documents and things that I have obtained, or that have been provided to me, as listed above in the Table of Exhibits.

13. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me. My consideration of materials in relation to this Declaration is ongoing and I will continue to review any new materials as it is provided. This Declaration represents only those opinions I have formed to date and I may supplement or amend this Declaration if additional facts or information that affects my opinions becomes available.

IV. Relevant Legal Principles

14. I am not an attorney. I offer no opinions on the law. But counsel has informed me of legal standards that apply to the issue of patent validity. I have applied these standards in arriving at my conclusions.

15. I understand that in an *inter partes* review the petitioner has the burden of proving a proposition of unpatentability by a preponderance of the evidence. I understand this standard is different from the standard that applies in a district court, where I understand a challenger bears the burden of proving invalidity by clear and convincing evidence.

16. I understand that a patent claim is invalid based on anticipation if a single prior art reference discloses all of the features of that claim, and does so in a way that enables one of ordinary skill in the art to make and use the invention. Each of the claim features may be expressly or inherently present in the prior art reference. I understand that if the prior art necessarily functions in accordance with, or includes a claim's feature, then that prior art inherently discloses that feature. I have relied on this understanding in expressing the opinions set forth below.

17. I understand that a prior art reference describes the claimed invention if it either expressly or inherently describes each and every feature set forth in the claim; *i.e.*, in determining whether a single item of prior art anticipates a patent claim, one should take into consideration not only what is expressly disclosed in that item, but also what is inherently present as a natural result of the practice of the system or method disclosed in that item.

18. I understand that to establish inherency, the evidence must make clear that the missing descriptive matter is necessarily present in the item of prior art and that it would be so recognized by persons of ordinary skill in the art. I also understand that prior art use of the claimed patented invention that was accidental, unrecognized, or unappreciated at the time of filing can still be an invalidating anticipation.

19. I understand that although multiple prior art references may not be combined to show anticipation, additional references may be used to interpret the allegedly anticipating reference and shed light on what it would have meant to those skilled in the art at the time of the invention. These additional references must make it clear that the missing descriptive matter in the patent claim is necessarily present in the allegedly anticipating reference, and that it would be so recognized by persons of ordinary skill in the art.

20. I understand that a patent may not be valid even though the invention is not identically disclosed or described in the prior art if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art in the relevant subject matter at the time the invention was made.

21. To determine if a claim is obvious, the following factors should be considered: (1) the level of ordinary skill in the art at the time the invention was made; (2) the scope and content of the prior art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations, including evidence of commercial success, long-felt but unsolved need, unsuccessful attempts by others, copying of the claimed invention, unexpected and superior results, acceptance and praise by others, independent invention by others, and the like.

22. For example, I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim because a court can take account of the inferences and/or creative steps that a person of ordinary skill in the art would employ.

23. I understand that the following rationales may be used to determine whether a piece of prior art can be combined with other prior art or with other information within the knowledge of one of ordinary skill in the art:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known techniques to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- “Obvious to try” - choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; or

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

24. I understand that when a work is available in one field of endeavor, design incentives and/or other market forces, for example, can prompt variations of it, either in the same field or a different one. Moreover, if a person of ordinary skill can implement a predictable variation, I understand that that likely bars its patentability.

25. I understand that obviousness must be tested as of the time the invention was made. I understand that the test for obviousness is what the combined teachings of the prior art references would have suggested, disclosed, or taught to one of ordinary skill in the art. In particular, it is my understanding that a patent claim is invalid based upon obviousness if it does nothing more than combine familiar elements from one or more prior art references or products according to known methods to yield predictable results. For example, I understand that where a technique has been used to improve one device, and a person of ordinary skill in the art would have recognized that it would improve similar devices in the same way, using that technique is obvious. I understand that obviousness can be proved by showing that a combination of elements was obvious to try, *i.e.*: that it does no more than yield predictable results; implements a predictable variation; is no more than the predictable use of prior art elements according to their established functions; or

when there is design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions. I have been further informed that when a patent claim simply arranges old elements with each element performing the same function it had been known to perform and yields results no more than one would expect from such an arrangement, the combination is obvious.

26. I understand that another factor to be considered is common sense. For example, I understand that common sense teaches that familiar items may have obvious uses beyond their primary purposes, and, in many cases, a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.

27. I understand that the Supreme Court articulated additional guidance for obviousness in its *KSR* decision. My understanding is that the Supreme Court said that technical people of ordinary skill look for guidance in other solutions to problems of a similar nature, and that the obviousness inquiry must track reality, and not legal fictions. I have relied on these understandings in expressing the opinions set forth below.

28. I understand that a new use of an old product or material cannot be claimed as a new product; the apparatus or system itself is old and cannot be patented. I further understand that, in general, merely discovering and claiming a new benefit to an old process cannot render the process newly patentable.

29. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a person of ordinary skill in the art (“POSITA”). I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

30. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have been asked to use the priority date of June 30, 1998. However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the mid to late 1990s.

V. Person of Ordinary Skill in the Art

31. In order to determine the characteristics of a POSITA of the '589 Patent, I have used June 30, 1998 as the relevant time frame. My understanding is that this is the priority date of the application that resulted in the '589 Patent. For purposes of this Declaration, any reference to the priority date of the '589 Patent is intended to refer to this June 30, 1998 date.

32. In determining the characteristics of a person of ordinary skill for the '589 Patent, I have considered the state of the art of semiconductor memory devices at that time, the types of problems encountered with power-on and initialization of such devices, and the solutions that then existed. I have also considered the then-existing technology for semiconductor memory devices and computer memory systems, including the sophistication of the technology involved. I have also considered the education and experience of those working in the field at that time. I have also considered my personal knowledge and experience in the field at that time, including those I worked and interacted with regarding semiconductor memory devices and computer memory systems. I have also considered the knowledge, education, and experience of those in academia and industry at that time that were working, innovating, or performing research in the field of semiconductor memory devices and computer memory systems.

33. It is my opinion that a POSITA for the '589 Patent at the time of this filing date would have had a Bachelor's degree in Electrical Engineering or Computer Science and two years of experience working in the field of system design using semiconductor memories, or a person with equivalent education, work, or experience in this field. More education could substitute for experience, and vice versa.

34. Based on my background and qualifications, I was as of the priority date of the '589 Patent someone who had more than the level of experience of a POSITA in the subject matter of the '589 Patent. When developing the opinions set forth in this declaration, I assumed the perspective of a POSITA.

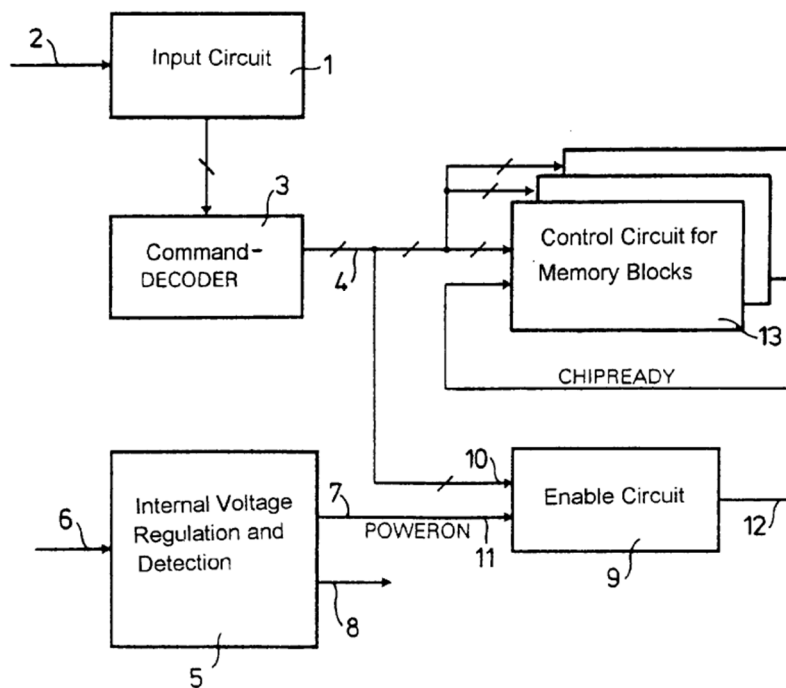
VI. '589 Patent

A. Overview

35. The '589 Patent is directed to a Dynamic Semiconductor Random Access Memory ("DRAM") device and a method for initializing a DRAM device. EX1001 at 2:7-14. The device and method purportedly solve a problem in the prior art by providing a way for circuits to be "reliably held in a desired defined state" while the device is powering on. *Id.* at 1:22-35. This purported advancement is achieved by detecting a particular initialization sequence. *Id.* To detect the initialization sequence, the device contains an initialization circuit having a control circuit and an enable circuit. *Id.* at 2:15-36.

36. As seen in FIG. 1 of the '589 Patent (reproduced below for reference), once the initialization circuit performs a switching-on operation and the internal voltage regulation and detection circuit 5 detects that the supply voltage at input 6 is stabilized, detection circuit 5 supplies a supply voltage stable signal (POWERON) to the enable circuit 9. *Id.* at 3:42-4:23.

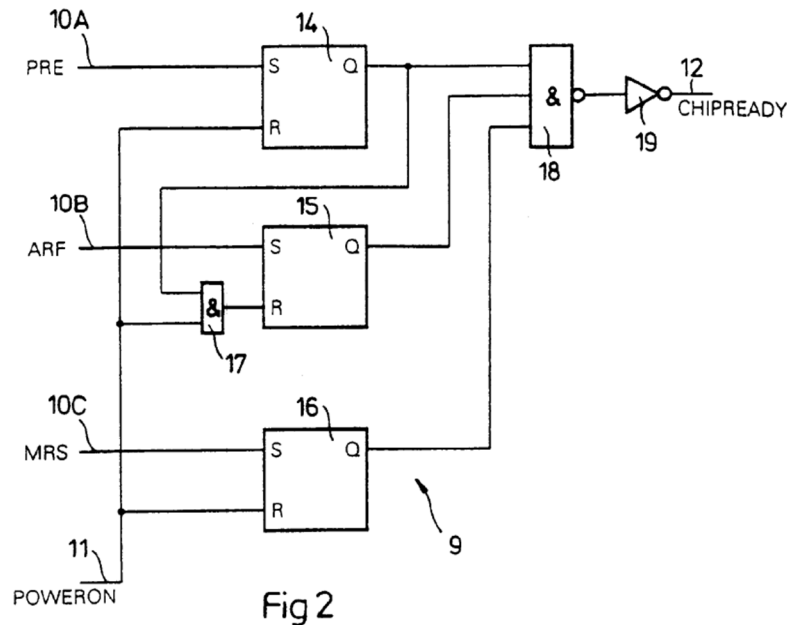
Fig 1



EX1001 ('589 Patent) at FIG. 1

The enable circuit 9 receives the supply voltage stable signal (POWERON) at input 11 and various command signals at input 10. *Id.* Once the enable circuit receives the supply voltage stable (POWERON) signal and the various command signals in a specific sequence, it outputs an enable signal (CHIPREADY) at output 12 which then unlatches the control circuit 13. *Id.*

37. FIG. 2 of the '589 Patent (reproduced below for reference), illustrates an example of enable circuit 9 in more detail.



EX1001 ('589 Patent) at FIG. 2

It contains “three bistable multivibrator stages 14, 15 and 16 each having a set input S, a reset input R, and also an output Q.” *Id.* at 4:24-58. The supply voltage stable signal (POWERON), described above, is applied to the enable circuit at input 11. *Id.* Additionally, the command signals described above at input 10 are shown in more detail. *Id.* Input 10A receives a preparation command for word line activation, called PRE or PRECHARGE. *Id.* Input 10B receives a refresh command, called ARF or AUTOREFRESH. *Id.* Input 10C receives a loading configuration register command, called MRS or MODE-REGISTER-SET. *Id.* The enable signal (CHIPREADY) is output at output 12 after “a predetermined chronological initialization sequence of

the command signals PRE, ARF and MRS and activation of the [supply voltage steady] POWERON signal.” *Id.*

B. Background / Applicant Admitted Prior Art

38. I have reviewed the '589 Patent, including the section of the Specification titled “BACKGROUND OF THE INVENTION.” I understand this section of the '589 Patent to disclose technologies that were already known in the art as of the priority date of the '589 Patent. In particular, I note that many of the elements that are recited in the '589 Patent claims are described and/or rendered obvious in this Background section. For example:

Claim	Claim Language	Background
[1.P]	A dynamic semiconductor memory device of a random access type <i>See also, claim [11.P]</i>	“In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation (“POWERUP”) that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state” EX1001 at 1:22-27. “In the case of the SDRAM semiconductor memory modules that have been disclosed to date...” EX1001 at 1:65-66.
[1.1]	an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has	“In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal

Claim	Claim Language	Background
	been stabilized after the switching-on operation <i>See also</i>, claim [11.1]	POWERON is active if the internal Supply Voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.” EX1001 at 1:65-2:5.
[1.2]	said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals <i>See also</i>, claim [11.2]	“According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called “POWERON-SEQUENCE”) is provided as follows: a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component; b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us; c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device; 4. the activation of eight or more refresh commands (AUTOREFRESH); and 5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.” EX1001 at 1:43-61. “In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal.” EX1001 at 1:65-2:1.

Claim	Claim Language	Background
[1.3]	said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit <i>See also, claim [11.3]</i>	“According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called “POWERON-SEQUENCE”) is provided as follows: a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component; b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us; c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device; 4. the activation of eight or more refresh commands (AUTOREFRESH); and 5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.” EX1001 at 1:43-61. “In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.” EX1001 at 1:65-2:5.

Claim	Claim Language	Background
[2]	The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal. <i>See also, claim [12]</i>	“[A] recommended initialization sequence (so-called “POWERON-SEQUENCE”) is provided as follows: ...c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device; 4. the activation of eight or more refresh commands (AUTOREFRESH); and 5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.” EX1001 at 1:44-61.
[8]	The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.	“In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation (“POWERUP”) that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state.” EX1001 at 1:22-27. “According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called “POWERON-SEQUENCE”) is provided.” EX1001 at 1:43-46.
[9]	The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.	“In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the

Claim	Claim Language	Background
	<i>See also</i> , claim [13]	necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.” EX1001 at 1:65-2:5.
[10]	The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal.	“According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called “POWERON-SEQUENCE”) is provided as follows: a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component; b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us; c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device; 4. the activation of eight or more refresh commands (AUTOREFRESH); and 5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.” EX1001 at 1:43-61.

These same AAPA concepts are also found in the prior art references that I discuss in the grounds of unpatentability below.

C. Prosecution History

1. EPO

39. I understand that U.S. Patent Application No. 09/343,431, which issued as the '589 Patent, claims priority to a German Patent publication filed on June 30, 1998. *See* EX1001 at [30]. Accordingly, I have reviewed the prosecution history of EPO Patent Application No. 99 113 048.5 (*i.e.*, the German Patent publication). Original EPO claim 1 has nearly identical scope and subject matter to granted US claim 1:

Original EPO Claim 1	Granted US Claim 1
A dynamic semiconductor memory device of a random-access type (DRAM/SDRAM) having an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components and which supplies a supply voltage stable signal (POWERON) once the supply voltage has been stabilized after the switching-on of the semiconductor memory device, characterized in that the initialization circuit has an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device which enable circuit supplies an enable signal (CHIPREADY) after the recognition of a predetermined proper initialization sequence of the	A dynamic semiconductor memory device of a random access type, comprising: an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

Original EPO Claim 1	Granted US Claim 1
command signals (PRE, ARF, MRS) applied to the semiconductor memory device which enable signal causes the unlatching of a control circuit (13) provided for the proper operation of the semiconductor memory device.	

EX1010 at 12; EX1001 at claim 1.

40. In a communication from the EPO Examining Division dated September 28, 2005, the EPO rejected independent claim 1 based on Japanese Patent Publication No. JP 09 106668 A to Samsung Electronics Co. Ltd. dated April 22, 1997 (“Tetsuka,” attached as EX1011). EX1010 at 7-9. Tetsuka is the Japanese counterpart to U.S. Patent No. 5,774,402 to Lee entitled “Initialization Circuit for a Semiconductor Memory Device” (“Lee”), which forms the basis for the invalidity grounds discussed herein. Compare EX1011 at Cover, (31) with EX1005 at Cover, [30] (each claiming priority to Korean Patent Publication 26181/1995); *see also* EX1008 at 67 (indicating that Lee is a “Member of the Patent Family” of Tetsuka). In response to this rejection, the applicant amended claim 1 to incorporate the subject matter of dependent claim 2, which ultimately led to allowance. EX1010 at 1, 5. Original EPO claim 2 has nearly identical scope and subject matter to granted US claim 2:

Original EPO Claim 2	Granted US Claim 2
A semiconductor memory device according to Claim 1, characterized in that the command signals (PRE, ARF, MRS) externally	The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined

Original EPO Claim 2	Granted US Claim 2
applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRE-CHARGE), and/or the refresh command (AUTOREFRESH), and/or the load configuration register command (MODE-REGISTER-SET).	proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

EX1010 at 12; EX1001 at claim 2.

41. I further understand that in submitting the claim amendments identified above, the applicant did not argue that the Examiner's rejections based on Tetsuka were in any way improper or incorrect. *See* EX1010 at 5-6. I also understand that JESD 21-C, which is discussed in more detail below, does not appear in the EPO prosecution history.

2. USPTO

42. U.S. Patent Application No. 09/343,431, which issued as the '589 Patent, was filed on June 30, 1999 (EX1002 at 5) and a claim of priority to German patent application dated June 30, 1998 (EX1002 at 31).

43. As discussed above, during EPO prosecution, the applicant amended original EPO claim 1 to incorporate the subject matter of original EPO claim 2 in order to gain allowance. The claims filed in front of the USPTO had the same subject matter as the original EPO claims (*i.e.*, original US claim 1 had the same subject matter as original EPO claim 1, without the additional limitations of original EPO

claim 2 that has to eventually be added into the EPO claim 1 to obtain allowance).
See EX1002 at 20. *Compare* EX1002 at 20 *with* EX1010 at 12. Despite knowledge that Lee was an English language family member of Tetsuka, as reported in the European Search Report (EX1008 at 67), the applicant cited only Tetsuka, without a separate English translation, to the USPTO. The applicant did not disclose the European Search Report or the Lee reference to the USPTO. Subsequently, the US Examiner allowed the claims without any rejections and without any amendment being made to claim 1, as the applicant later made to obtain allowance in the EPO. EX1002 at 100-01.

44. I understand that another party, Kingston Technology Company, Inc. (“Kingston”), previously petitioned for *inter partes* review of claims 11 and 12 of the ’589 Patent on November 10, 2016 and that the Patent Trial and Appeal Board (“Board”) denied Kingston’s petition. *Kingston Tech. Co., Inc. v. Polaris Innovations Ltd.*, IPR2017-00238, Paper 9 (PTAB May 2, 2017). I understand that Kingston based its petition on different grounds than those I describe below. In particular, Kingston’s grounds were based on U.S. Patent Nos. 6,243,797 to Meritt and 5,448,528 to Nagai.

D. Priority Date

45. U.S. Patent Application No. 09/343,431, which issued as the ’589 Patent, was filed on June 30, 1999 and claims priority to a German patent application

dated June 30, 1998. EX1001. For the purposes of this Declaration, I have been asked to assume that the earliest priority date of the '589 Patent is June 30, 1998.

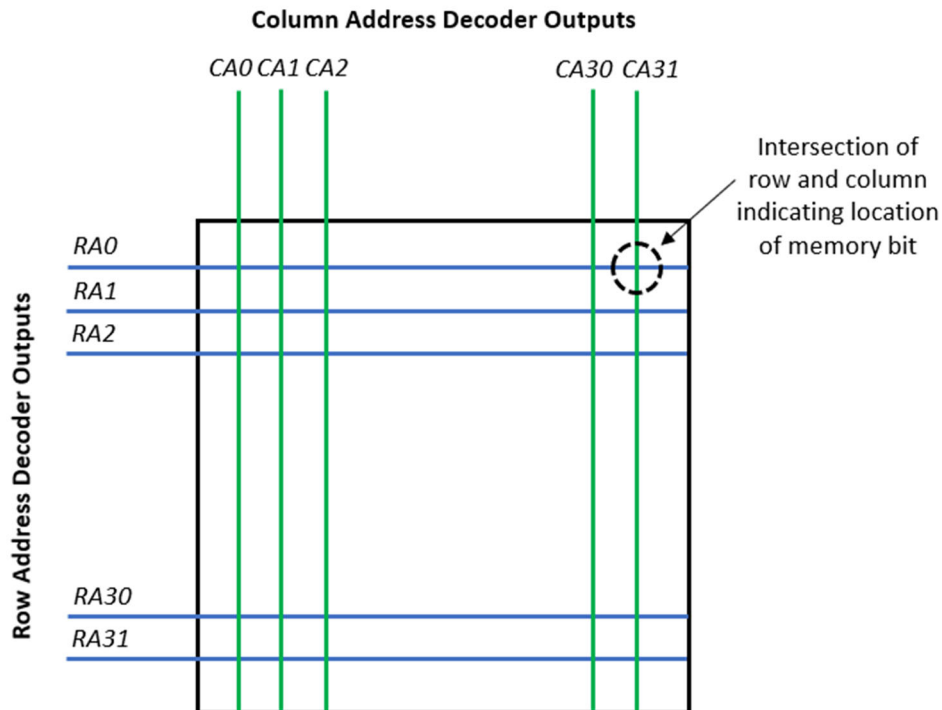
E. Related Proceedings

46. I understand that Patent Owner, Polaris Innovations, Ltd. ("Patent Owner" or "Polaris"), filed a complaint on February 8, 2022 in the United States District Court for the District of Delaware (CA 1:22-CV-00174-RGA) against Petitioner, asserting 4 patents, including the '589 Patent.

VII. Technology Background

47. The technology of the '589 Patent generally relates to semiconductor memory devices, also referred to as random access memory ("RAM"). As of the filing date of the '589 Patent, there were multiple types of RAM available. Such variants include Dynamic RAM ("DRAM") and Synchronous Dynamic RAM ("SDRAM").

48. DRAM chips contain one or more memory arrays, which are rectangular grids of storage cells where each cell holds one bit of data. Because the arrays are rectangular grids, memory arrays are organized into rows and columns. A depiction of a DRAM chip's memory array with the rows and columns indicated is reproduced below.



49. By identifying the intersection of a row and a column, a computer's central processing unit ("CPU") can access an individual storage cell inside a DRAM chip so as to read or write the data held there. This is accomplished by sending both a row address and a column address to the DRAM. In practice, a CPU accesses a DRAM by addressing a group of bits together as a unit, such that a single read or write operation takes place on multiple individual memory cells at the same time.

50. DRAM is characterized as "dynamic" because the values held in the memory array's storage cells are represented by electric charges that slowly leak out of the circuit over time. In this sense, DRAM memory cells are similar to capacitors, in contrast to static memory cells, where the electric charge in a memory cell will be maintained indefinitely as long as power is applied. In order to maintain the data

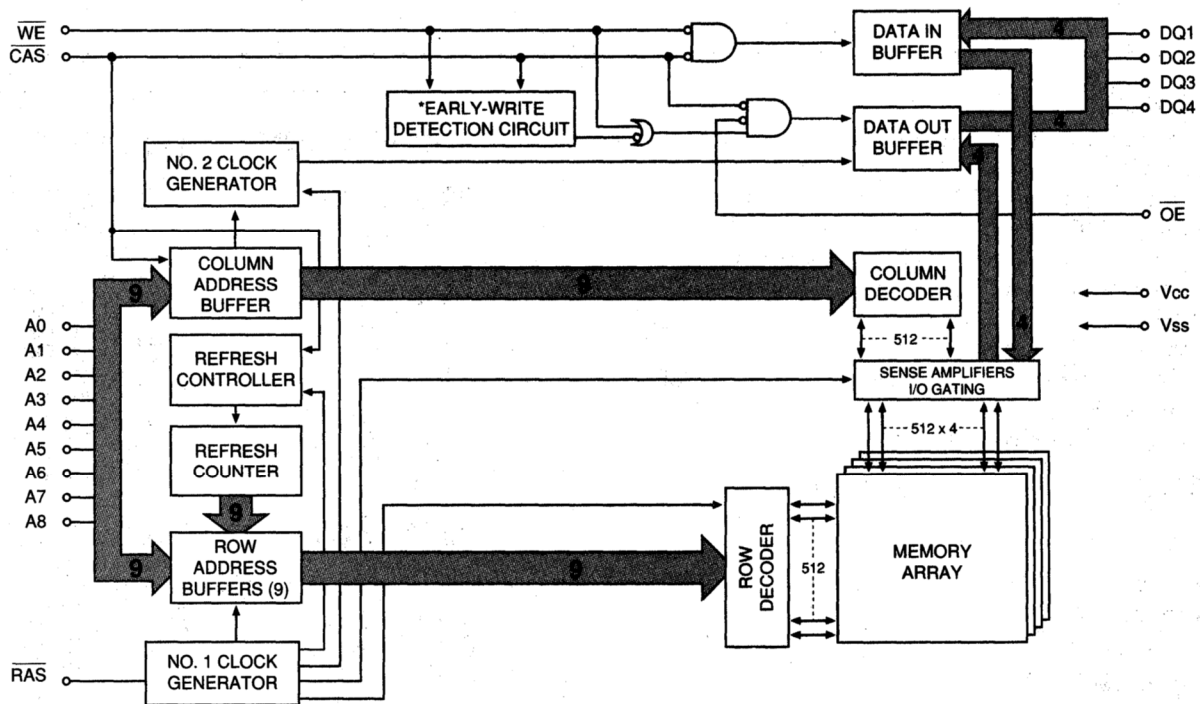
stored in dynamic memory cells, they must be periodically “refreshed” by reading the current value of a memory cell and restoring its charge. Another aspect of dynamic memory cells is that before a read operation can be performed, a “precharge” operation is necessary to prepare the internal circuitry to be able detect the current state of a memory cell. This affects the timing of how reads and writes are processed in a dynamic memory device.

51. DRAM devices are equipped with address and data pins which connect the DRAM to address and data buses. A bus is a group of one or more wires that carry electrical signals between components. Address buses convey address information to the DRAM device and data buses communicate data for memory reads and writes. DRAM devices also include control pins and may include one or more clock input pins. Example of control pins are CAS and RAS input strobes, write-enable and chip-select. A “strobe” is a signal that indicates to the recipient that another signal is valid.

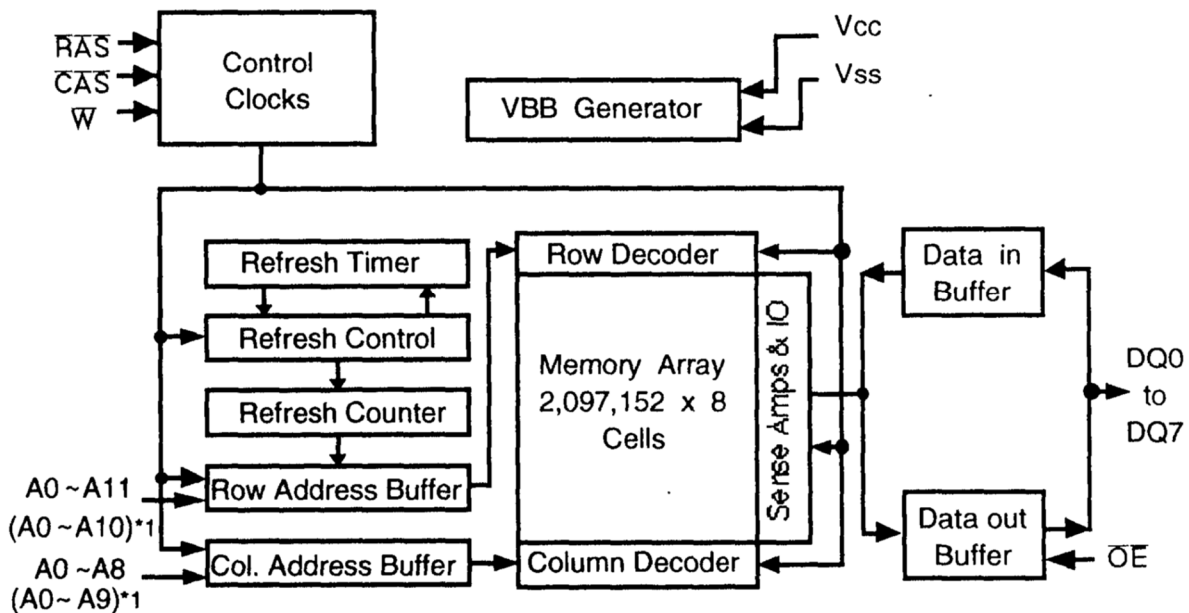
52. In typical systems involving DRAM devices, there is a dedicated address bus that carries row and column addresses to the DRAMs and has a width that grows with the physical storage on a DRAM device. There is also a dedicated data bus that communicates read and write data between the CPU and the DRAMs. Finally the control signals comprise the row and column strobes, output enables, clocks, clock enables, chip enables and other related signals. These signals are

typically controlled by a memory controller, that is either integrated with or separate from the CPU, and connect to every DRAM in the system.

53. Input signals labeled “CAS” and “RAS” (or sometimes “CASB” and “RASB,” in which the “B” refers to “bar” which means that the signals are low active) are specific to DRAM type devices. Column Address Strobe (CAS) and Row Address Strobe (RAS) signals have to do with the multiplexing of column and row lines on the same address pins. Additional control signals include, for example, Chip Select (CS), which enables the memory chip’s command decoder and Write Enable (WE), which determines whether an operation is a read or a write. Additionally, DRAM may have special function signals, such as DSF, which enables certain special operational functions when active. These various input signals are used to perform specific commands by way of a command decoder within the DRAM device, which accepts the various signals and interprets the sequence as a particular command. Depending on the combination of these input signals sent from the memory controller to the DRAM device, a different command is identified and performed. For reference, a functional block diagram of a 1992 Micron DRAM device is provided below (EX1017 at 1-88).

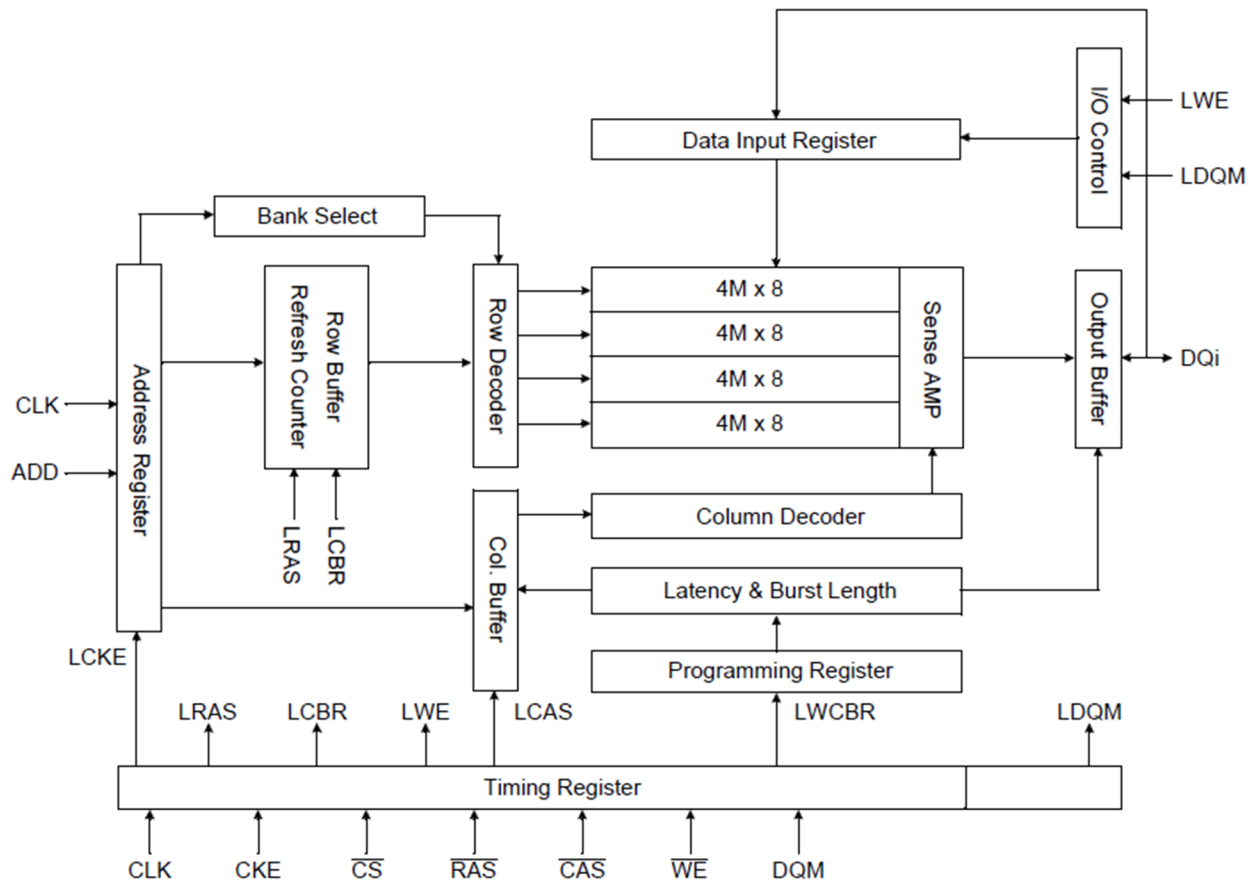


Similarly, a functional block diagram of a 1996 Samsung DRAM device is provided below (EX1018 at 217).



Similar to the prior art used in the grounds below, both of these DRAM devices required a power-on sequence that utilized a initialization sequence of control signals. *See* EX1017 at 1-79; EX1018 at 224 n.1.

54. The original DRAM devices were asynchronous, meaning that they did not rely on an external clock signal. Subsequently, synchronous DRAM devices (SDRAMs) were introduced in which an external clock signal is supplied by the memory controller and signals are sampled based on the clock signal. The primary benefit of SDRAM is that it allows faster operation due to increased predictability of event timing. Despite some changes to control signal nomenclature and other functionality specific to the use of external clock signals, the underlying architecture of SDRAM is essentially the same as asynchronous DRAM. For example, both asynchronous DRAMs and SDRAMs have row and column strobe signals. Sometimes these signals are referred to as CAS and RAS and sometimes they are referred to as Column Enable (CE) and Row Enable (RE). *See, e.g.*, EX1006 at page 2-2 (equating CAS with the Column Enable (CE) input); *id.* at page 2-4 (equating RAS with the Row Enable (RE) input). For reference, a functional block diagram of a 1998 Samsung SDRAM device is provided below (EX1019 at 1).



VIII. Claim Construction

55. I have interpreted the terms of the '589 Patent according to their plain meaning. In interpreting the terms, I have carefully considered and applied the claim construction standard referred to in Section IV above.

IX. Summary of Opinions

56. In my opinion, U.S. Patent No. 5,559,753 to Kocis entitled "Apparatus and Method for Preventing Bus Contention During Power-Up in a Computer System With Two or More DRAM Banks" ("Kocis") anticipates claims 1, 9, 11, and 13 of the '589 Patent (*see infra* at Section X).

57. In my opinion, Kocis in combination with JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Release 7, dated January 1997 (“JESD 21-C”) renders obvious claims 2, 8, 10, and 12 of the ’589 Patent (*see infra* at Section XI).

58. In my opinion, U.S. Patent No. 5,774,402 to Lee entitled “Initialization Circuit for a Semiconductor Memory Device” (“Lee”) anticipates or, in the alternative, renders obvious claims 1 and 11 of the ’589 Patent (*see infra* at Section XII).

59. In addition, in my opinion, Lee in combination with U.S. Patent No. 5,703,510 to Iketani *et al.* entitled “Power On Reset Circuit For Generating Reset Signal at Power On” (“Iketani”) renders obvious claims 1 and 11 of the ’589 Patent (*see infra* at Section XIII).

60. In my opinion, Lee in combination with JESD 21-C renders obvious claims 2, 8, 10, and 12 of the ’589 Patent (*see infra* at Section XIV).

61. In addition, in my opinion, Lee in combination with Iketani and JESD 21-C renders obvious claims 2, 8, 10, and 12 of the ’589 Patent (*see infra* at Section XV).

62. In my opinion, Lee in combination with Kocis renders obvious claims 9 and 13 of the ’589 Patent (*see infra* at Section XVI).

63. In addition, in my opinion, Lee in combination with Iketani and Kocis renders obvious claims 9 and 13 of the '589 Patent (*see infra* at Section XVII).

64. A table of the grounds is provided below for ease of reference:

	Grounds	Claims
1	§102: Kocis	1, 9, 11, 13
2	§103: Kocis in combination with JESD 21-C	2, 8, 10, 12
3	§102/§103: Lee	1, 11
4	§103: Lee in combination with Iketani	1, 11
5	§103: Lee in combination with JESD 21-C	2, 8, 10, 12
6	§103: Lee in combination with Iketani and JESD 21-C	2, 8, 10, 12
7	§103: Lee in combination with Kocis	9, 13
8	§103: Lee in combination with Iketani and Kocis	9, 13

X. Claims 1, 9, 11, and 13 are Anticipated by Kocis

65. In my opinion, Kocis anticipates claims 1, 9, 11, and 13 of the '589 Patent.

A. Overview of Kocis

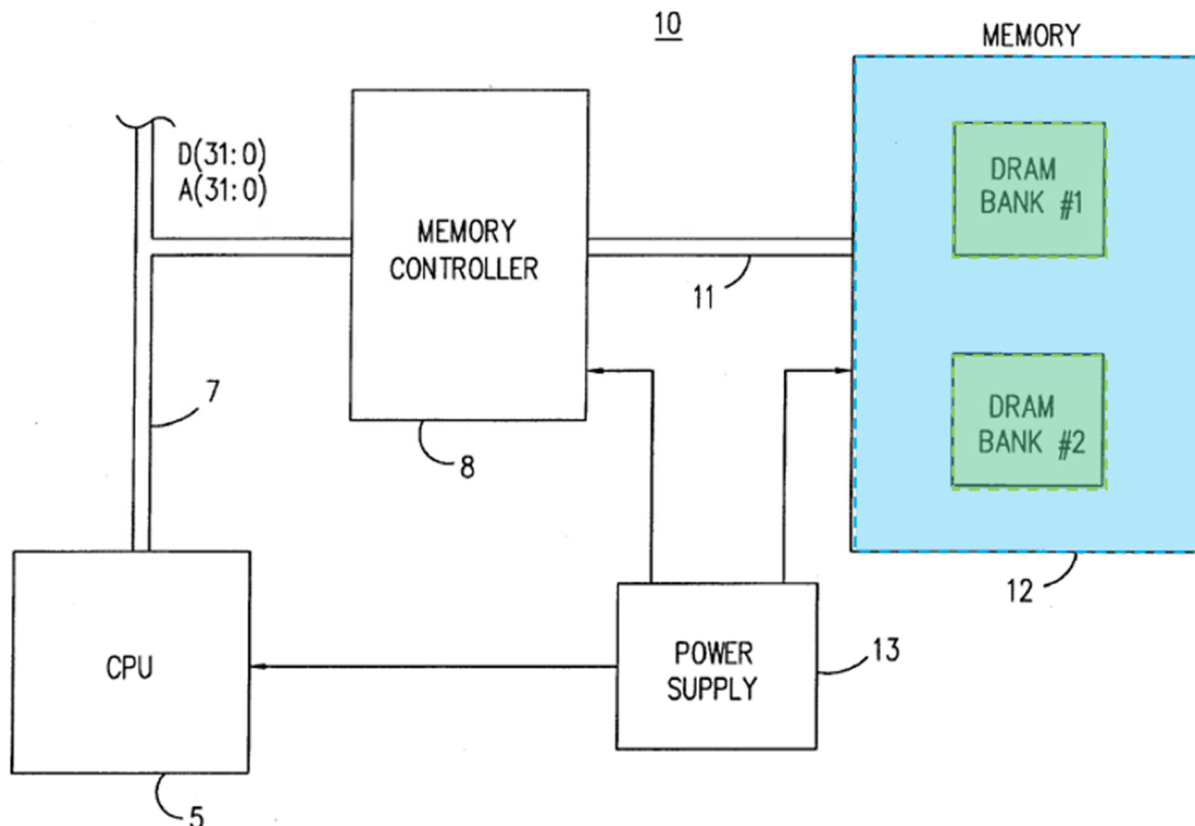
66. Kocis was filed on January 25, 1995 and discloses a DRAM circuit with circuitry for disabling data output drivers to prevent bus contention during system power-up. EX1004 at [22], Abst. The circuitry disclosed in Kocis includes a counter for counting RAS signals and a circuit for detecting that a supply voltage has achieved a proper voltage threshold. EX1004 at Abst. The circuitry in Kocis disables output drivers and an associated control circuit until a certain number of RAS signals are received and the supply voltage has met the necessary threshold. EX1004 at Abst.

B. Claim 1

1. Claim Element [1.P]: A dynamic semiconductor memory device of a random access type

67. I understand that the preamble of claim 1 is not limiting. Nevertheless, to the extent the preamble is found to be limiting, the devices described in Kocis disclose “a dynamic semiconductor memory device of a random access type.” In particular, Kocis is directed to “a computer system with two or more banks of dynamic random access memory (DRAM) chips, [and in particular,] to a system for preventing contention on the memory bus between conflicting data signals from two or more DRAM banks.” EX1004 at 1:8-15.

68. Furthermore, Kocis Figure 1 (annotated below) shows a block diagram of a typical system configuration.



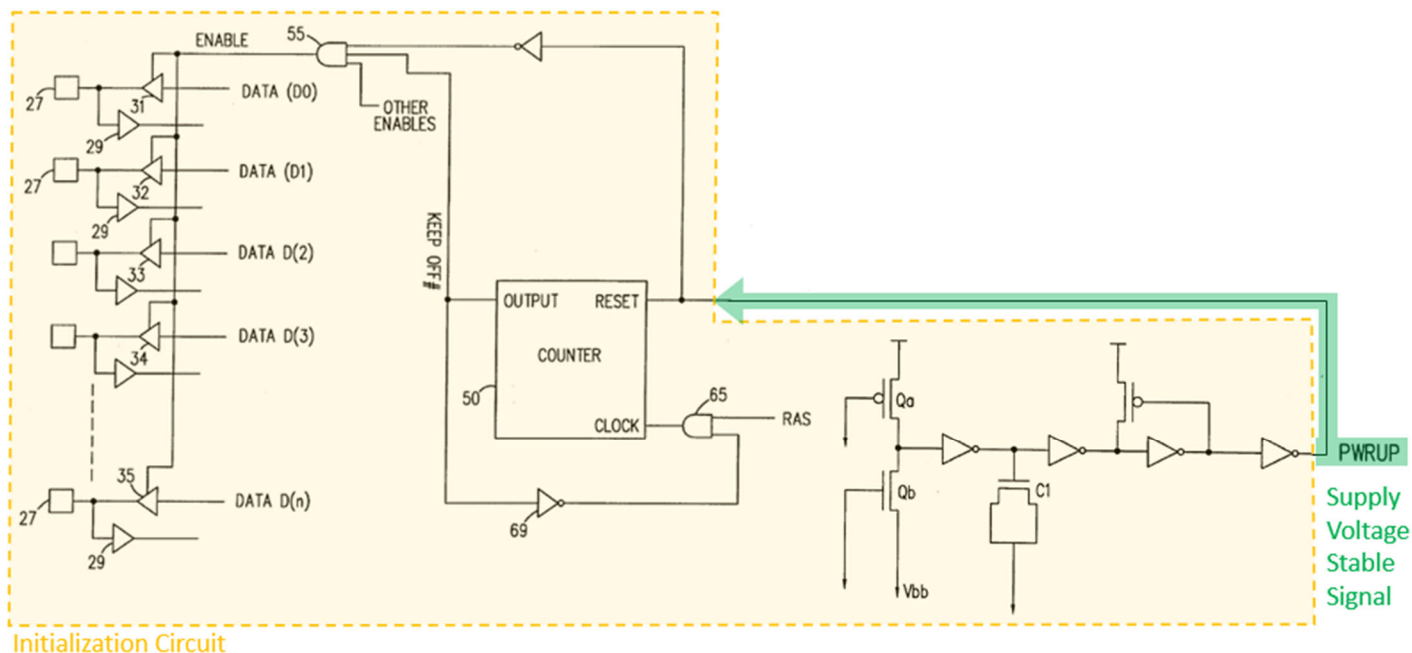
EX1004 (Kocis) at Figure 1 (annotated)

69. The system configuration includes system memory 12 (blue) which “typically includes banks of dynamic random access memory (DRAM) devices. Two DRAM banks are shown in FIG. 1 [green] for purposes of illustration.” EX1004 at 1:45-48; *see also id.* at FIG. 1. Accordingly, a POSITA would have understood that Kocis discloses a dynamic semiconductor memory device of a random access type.

2. Claim Element [1.1]: an initialization circuit controlling a switching-on operation and supplying a supply voltage stable

signal once a supply voltage has been stabilized after the switching-on operation

70. Kocis discloses an initialization circuit that is part of the DRAM memory and that (1) controls a switching-on operation and (2) supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. EX1004 at Abstract, 1:8-15, 3:5-9, 4:40-44. In order to better demonstrate the initialization circuit, I have included an annotated version of Kocis Figures 4A and 5 below, which shows components of Kocis that disclose the claimed initialization circuit, outlined in yellow. I note that even though Figure 4A is labeled as “PRIOR ART”, the specification clarifies that this circuit is also used in the preferred embodiment: “The Pwrap input signal preferably comprises the output signal of FIG. 4A, which already is available on certain prior art DRAM chips.” EX1004 at 5:18-20.



EX1004 (Kocis) at Figures 4A and 5 (annotated)

71. The initialization circuit shown above in yellow controls a switching-on operation (*i.e.*, the process for powering on the memory chip). For example, Kocis explains that “The Pwrup signal is an active low signal, which indicates that the power supply has ramped to a certain absolute threshold voltage value.” EX1004 at 5:20-22. A POSITA would have understood that the power supply ramping up to a certain absolute threshold voltage value discloses the claimed switching-on operation.

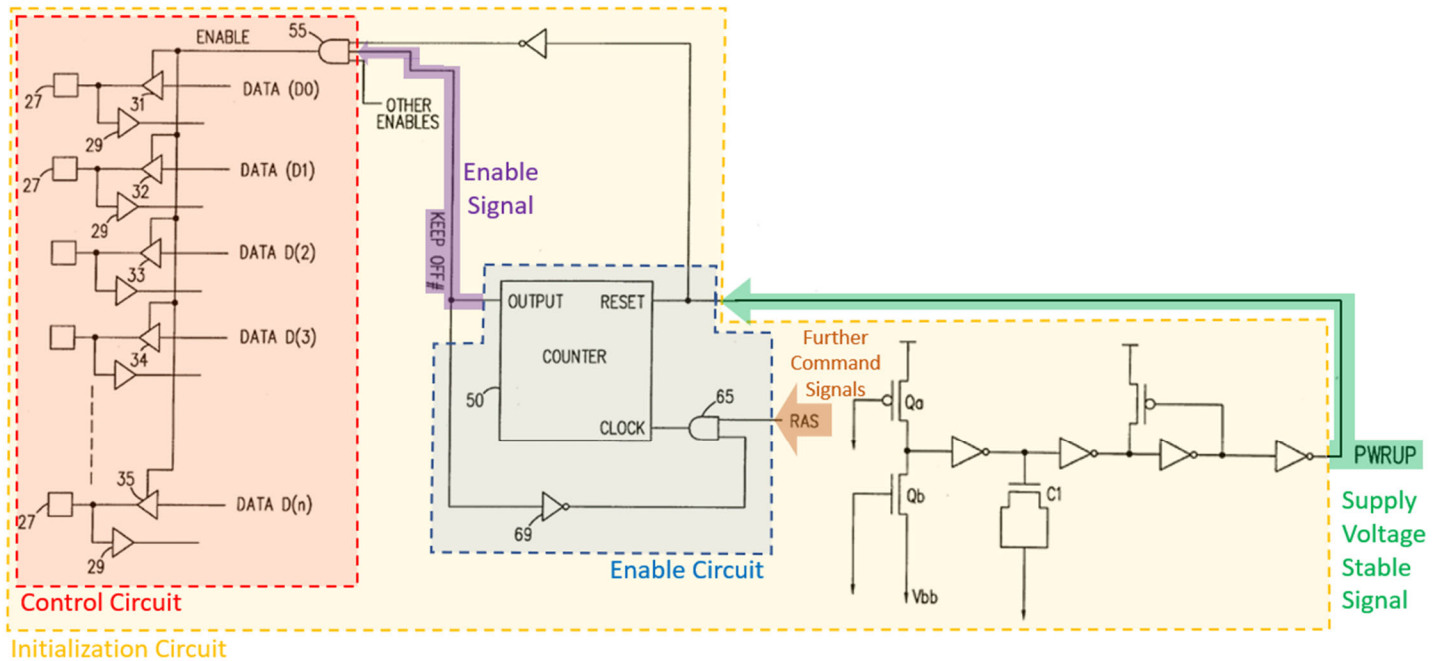
72. The initialization circuit supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. One of skill in the art would understand that the PWRUP signal (outlined in green in the annotated figure above) discloses the claimed supply voltage stable signal. The '589 Patent

indicates that the supply voltage stable signal (*i.e.*, the “POWERON” signal) is active if the internal supply voltages have reached the values necessary for the proper operation of the memory device. EX1001 at 1:13-16, 2:1-4. Similarly, the PWRUP signal “indicates that the power supply has ramped to a certain absolute threshold voltage value.” EX1004 at 5:20-22.

73. Accordingly, a POSITA would have understood that Kocis discloses an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation.

3. Claim Element [1.2]: said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals

74. Kocis discloses an initialization circuit having (i) an enable circuit for receiving the supply voltage stable signal and externally applied further command signals and (ii) a control circuit for controlling operations. In order to better illustrate this disclosure, I have provided annotated Figures 4A and 5 of Kocis with the claimed control circuit (red), enable circuit (blue), and further command signals (brown), below.



EX1004 (Kocis) at Figures 4A and 5 (annotated)

75. Kocis discloses the claimed enable circuit. Specifically, the counter 50, AND gate 65, and inverter 69 in Kocis disclose the claimed enable circuit (shown in blue above). As recited in claim 1, the enable circuit receives both the supply voltage stable signal (the PWRUP signal, shown in green above) and externally applied further command signals (shown in brown above). As discussed in element [1.1], Kocis' PWRUP signal discloses the claimed supply voltage stable signal. This signal is received by the counter 50 in Kocis, as shown in Kocis Figure 5. EX1004 at FIG. 5; *see also id.* at 6:15-17.

76. Kocis discloses that the enable circuit receives the externally applied further command signals. Kocis describes the RAS signals as a “control signal” which is used to transfer data by identifying a specific row associated with a memory

location. EX1004 at 2:63, 2:22-28. RAS stands for row address strobe signal. RAS (and CAS) signals have to do with multiplexing of row and column lines on the same address pins. RAS (and CAS) signals are primarily used to instruct the memory chip to activate or open a row and then to read a column within the activated row. First a column address is provided, then the CAS strobe occurs, then a row address is provided, then the RAS strobe occurs. *See* EX1004 at 2:22-36. Kocis explains that the RAS signal is regularly used for more than just addressing. For example, “[w]hen seven RAS signals have been detected after a threshold voltage is achieved, the DRAM data output lines are enabled. The receipt of eight RAS signals are typically required by DRAM manufacturers to wake-up the DRAM.” EX1004 at 3:45-48. A POSITA would recognize that this signal is a command signal, as it provides specific commands to the memory chip.

77. Kocis additionally discloses a control circuit for controlling operations (shown in red above), which includes AND gate 55 and the tri-state buffers 31, 32, 33, 34, and 35. In particular, Kocis discloses that the AND gate 55 and tri-state buffers control when data signals are output to the memory bus. *See, e.g.*, EX1004 at 5:3-12 (“The AND gate 55 receives the following input signals in the preferred embodiment: (1) an inverted Pwrap signal from the output of the voltage detection circuit of FIG. 4A [and] (2) an output signal (Keep Off) from counter 50 The output of the AND gate 55 . . . is driven high if all input signals are high. Thus, tri-

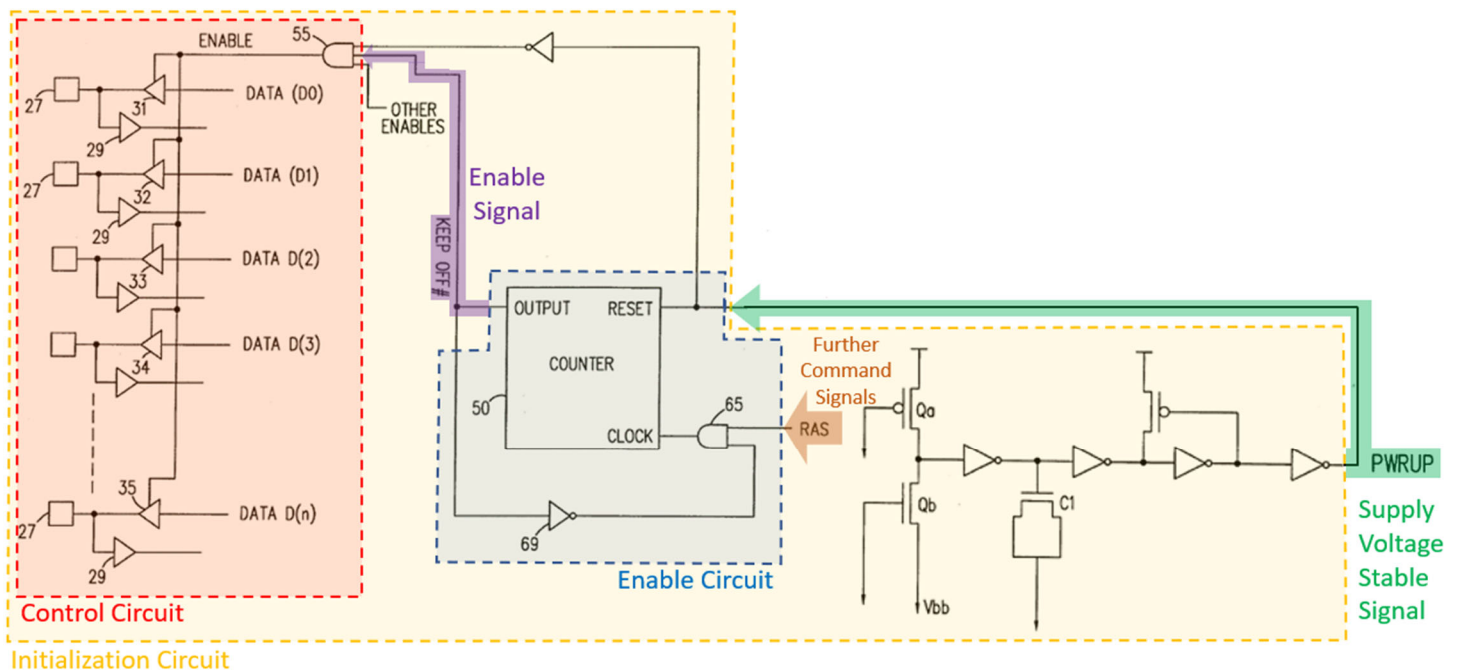
state buffers 31, 32, 33, 34, 35 only are enabled if all [the] input signals are high”); *id.* at 1:54-66 (“Because several DRAM banks connect to the memory bus 11 in a typical computer system, precautionary steps must be taken to prevent multiple devices from simultaneously driving signals on the memory bus 11. . . . To prevent the problem with bus contention, each DRAM bank typically includes a tri-state buffer 13 for each of its various data output lines.”).

78. Thus, proper control of the output drivers is essential for controlling operations of the memory device. Specifically, during a write operation, the output drivers must be turned off to allow external data into the chip, and during a read operation the output drivers must be turned on at the right time to output data to the external pins. Furthermore, it’s clear that the ‘589 Patent considered output drivers as part of the claimed control circuit: “The predetermined circuits remain latched until the end of the predetermined initialization Sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.” EX1001 at 2:41-45; *see also id.* at cl. 9, 13. Based on this disclosure, a POSITA would have understood that Kocis discloses the claimed control circuit. Accordingly, Kocis discloses an initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals.

4. Claim Element [1.3]: said enable circuit outputting an enable signal after a predetermined proper initialization sequence

of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit

79. Kocis discloses that (1) the enable circuit outputs an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and (2) the enable signal unlatches the control circuit. With reference again to the annotated alternate disclosure (reproduced below), Kocis' enable signal (shown in purple) which is output from counter 50 (*i.e.*, the Keep Off signal) discloses the enable signal output from the enable circuit.



EX1004 (Kocis) at Figures 4A and 5 (annotated)

80. As explained in Kocis, the enable signal (*i.e.*, Kocis' Keep Off signal) is only output after a predetermined proper initialization sequence of the externally applied further command signals (*i.e.*, Kocis RAS signal). Specifically, “[i]n the preferred embodiment of the present invention, the counter 50 counts the number of

RAS signals received from the memory controller 8 (of FIG. 1). After the counter 50 counts eight RAS signals, an output signal (Keep Off) is generated by the counter.” EX1004 at 5:39-43.

81. Once the enable signal is driven to a high logic level, it unlatches the control circuit. In other words, unless PWRUP (green) and RAS (brown) signals are input in the correct initialization sequence, the enable circuit (blue) will not output the enable signal (purple). *See, e.g.*, EX1004 at 5:3-12 (“The AND gate 55 receives the following input signals in the preferred embodiment: (1) an inverted Pwrup signal from the output of the voltage detection circuit of FIG. 4A [and] (2) an output signal (Keep Off) from counter 50 The output of the AND gate 55 . . . is driven high if all input signals are high. Thus, tri-state buffers 31, 32, 33, 34, 35 only are enabled if all [the] input signals are high”); *id.* at 4:56-61 (“all data signals transmitted onto the memory bus 11 by DRAM 100 are driven by tri-state buffers . . . the tri-state buffers transmit the associated data signal only when enabled by the [output of AND gate 55].”); *id.* at 5:22-28 (“Until the voltage supply has reached the threshold value (which will vary from circuit to circuit depending upon the proper operating voltage and other considerations), the AND gate 55 keeps the ENABLE line low, disabling the tri-state buffers 31, 32, 33, 34, 35, thus preventing possible buss contention during start-up or reset.”); *id.* at 2:3-8 (“When the buffer 13 is not enabled, the tri-state buffer 13 functions to ‘disconnect’ the data output line from the

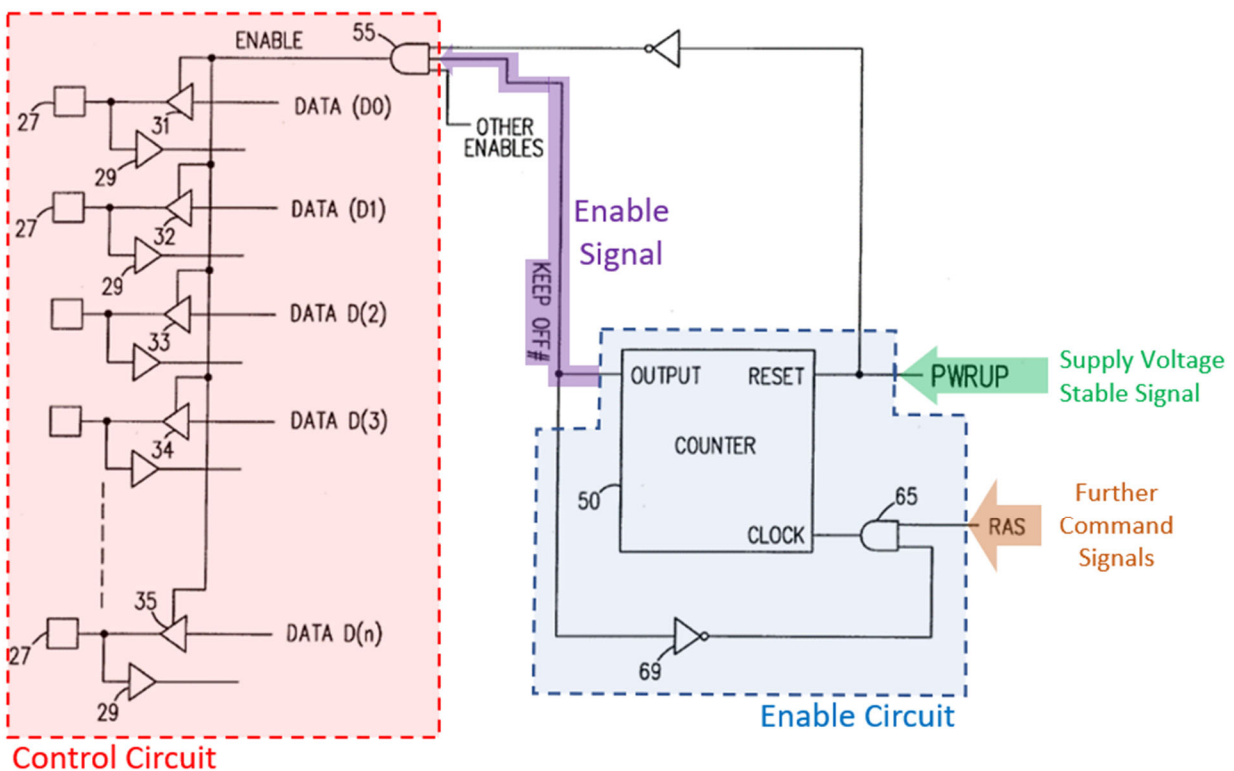
memory bus 11, so that neither a low or high signal is driven on the bus, and instead, the buffer presents a high impedance state thereby allowing other circuitry to determine the state of the bus.”). A POSITA would have understood that driving a high input to the AND gate 55 which ultimately enables the tri-state buffers, as is disclosed in Kocis, teaches unlatching the control circuit because it causes the start of normal operation of the buffers.

82. Although Kocis labels another signal as an “ENABLE” signal (the output of AND gate 55), a POSITA would have understood that the Keep Off signal is also enable signal as claimed. This is supported by both how the Keep Off signal is used in Kocis’ circuit, as discussed above, as well as the fact that Kocis refers to the other inputs to AND gate 55 along with the Keep Off signal input as “Other Enables,” implying that the Keep Off signal is also an enable signal. In addition, although the discussion above maps Kocis’ AND gate 55 and output buffers as the claimed “control circuit” and the Keep Off signal as the claimed “enable signal,” Kocis alternatively discloses the claimed “control circuit” as only its output buffers and with the “Enable” as the claimed “enable signal.”

83. Accordingly, a POSITA would have understood that Kocis discloses the enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

C. **Claim [9]: The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit**

84. Kocis discloses a control circuit having output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit. Kocis explains that Figure 5 shows a circuit “for disabling DRAM data output drivers until power supply voltages are satisfactory and all enable conditions are met.” EX1004 at 4:23-26.



EX1004 (Kocis) at Figure 5 (annotated)

85. As shown in annotated Figure 5 (above), a POSITA would have understood that disabling the output drivers until the enable conditions are met (*i.e.*,

the proper initialization sequence has been performed) teaches latching the output drivers until the enable signal is generated by the enable circuit. As discussed with respect to claim 1, unless PWRUP (green) and RAS (brown) signals are input in the correct initialization sequence, the enable circuit (blue) will not output the enable signal (purple). *See* EX1004 at 5:8-12 (“The output of the AND gate 55 (which comprises the ENABLE signal), only is driven high if all input signals are high. Thus, tri-state buffers 31, 32, 33, 34, 35 are only enabled if all three input signals are high.”); *id.* at 5:22-28 (“Until the voltage supply has reached the threshold value (which will vary from circuit to circuit depending upon the proper operating voltage and other considerations), the AND gate 55 keeps the ENABLE line low, disabling the tri-state buffers 31, 32, 33, 34, 35, thus preventing possible buss contention during start-up or reset.”); *id.* at 2:3-8 (“When the buffer 13 is not enabled, the tri-state buffer 13 functions to ‘disconnect’ the data output line from the memory bus 11, so that neither a low or high signal is driven on the bus, and instead, the buffer presents a high impedance state thereby allowing other circuitry to determine the state of the bus.”). Accordingly, Kocis discloses a control circuit having output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

D. Claim 11

- 1. Claim Element [11.P]: An improved method for initializing a dynamic semiconductor memory device of a random access**

type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components

86. For the same reasons discussed in Sections X.B.1 and X.B.2 with respect to claim elements [1.P] and [1.1], Kocis discloses an improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components.

2. Claim Element [11.1]: supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device

87. For the same reasons discussed in Section X.B.2 with respect to claim element [1.1], Kocis discloses supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device.

3. Claim Element [11.2]: supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device

88. For the same reasons discussed in Section X.B.3 with respect to claim element [1.2], Kocis discloses the initialization circuit receiving the supply voltage

stable signal and further command signals externally applied to the dynamic semiconductor memory device. Furthermore, for the same reasons discussed in Section X.B.4 with respect to claim element [1.3], Kocis discloses supplying, via an enable circuit of the initialization circuit, an enable signal ... after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

E. Claim [13]: The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit

89. For the same reasons discussed in Section X.C with respect to claim element [9], Kocis discloses maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

XI. Claims 2, 8, 10, and 12 are Obvious Over Kocis in Combination with JESD 21-C

90. In my opinion, Kocis in combination with JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Kocis disclosing the limitations of independent Claims 1 and 11 from which they depend (*see* Sections X.B and X.D, *supra*).

A. Overview of JESD 21-C

91. JESD 21-C is a “Memory Device Standard” for “establish[ing] pin assignments, power supply potentials, and package configurations and dimensions for a series of memory devices.” EX1006 at page 3-1. Furthermore, “In some cases, special timing diagrams are included, where they are essential to the implementation and use of the standards.” *Id.*

92. The JESD 21-C Standard is an industry standard compiled and published by the Electronic Industries Association (EIA) and JEDEC. JESD 21-C, was and remains a well-known memory standard published by a prominent memory standards setting organization, JEDEC. The standard “contain[s] material that has been prepared, progressively reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.” EX1006 at Copyright Notice. The purpose of the standard is to “serve the public interest through eliminating misunderstandings between manufacturers and purchase[r]s, facilitating interchangeability and improvement of products, and assisting the purchaser [in] selecting and obtaining with minimum delay the proper product for his particular need.” *Id.*

93. A POSITA would have been familiar with JEDEC memory standards like JESD 21-C, as these standards are widely relied upon by manufacturers to create memory products with a high level of interoperability and interchangeability. In

fact, many manufacturers' product datasheets closely mirror JEDEC's standards and specifications. JEDEC's specifications are easily accessible on its website, and a POSITA would have understood how to access the standards and use them to design a conforming memory device.

B. Combination of Kocis and JESD 21-C

94. JESD 21-C provides various standardized signals, timing diagrams, and other specifications for solid state memory in order to promote interoperability between products. This information includes a power-up sequence to initialize memory to an IDLE state for normal operation in an attempt to eliminate bus contention. EX1006 at page 3.11.5-9. As described above, Kocis discloses the circuitry for detection of an initialization sequence of dynamic random access memory, and also has the same stated goal of JESD 21-C (*i.e.*, to initialize memory to an IDLE state for normal operation in an attempt to eliminate bus contention). *See* EX1004 at 1:12-15; *id.* at 3:41-52. The stated intention of Kocis is to detect an initialization sequence performed by external logic that is required by DRAM vendors: "The present invention takes advantage of these preliminary cycles already required as part of the DRAM start-up protocol in designing a scheme to disable the output data drivers of the DRAM 100, thereby preventing bus contention." EX1004 at 5:34-38.

95. A POSITA would have been motivated to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Kocis in order to ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by the POSITA. In particular, the series of RAS command signals disclosed in Kocis as causing the counter 50 to output the Keep Off signal to effect initialization of the memory circuitry would be replaced in the combination by the series of command signals disclosed in JESD 21-C to be used for initializing memory. This improvement constitutes the use of a known technique (*i.e.*, the initialization signals and timing for memory devices, including DRAM and SDRAM disclosed in JESD 21-C) to improve similar devices (*i.e.*, the initialization circuitry for the memory devices, including DRAM, disclosed in Kocis) in the same way (*i.e.*, by applying the same initialization signals and timing disclosed in JESD 21-C).

96. This improvement is also a simple substitution of the signals and timing of Kocis with the signals and timing specified in JESD 21-C. A POSITA would have understood that substituting the signals and timing element of JESD 21-C for those of Kocis would yield predictable results. Specifically, incorporating JESD 21-C's signals and timing would ensure interoperability and compatibility with other products in the solid state memory field.

C. Claim [2]: The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming

the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal

97. The Combination of Kocis and JESD 21-C discloses that the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit including at least one of (i) a preparation command signal for word line activation, (ii) a refresh command signal, and (iii) a loading configuration register command signal.

98. JESD 21-C discloses each of the claimed further command signals and the predetermined proper initialization sequence of such signals. JESD 21-C teaches the following sequence for initialization of SDRAM:

“The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge* commands for all banks of the device.
4. Issue 8 or more *autorefresh* commands.
5. Issue a *mode register set* command to initialize the mode register.

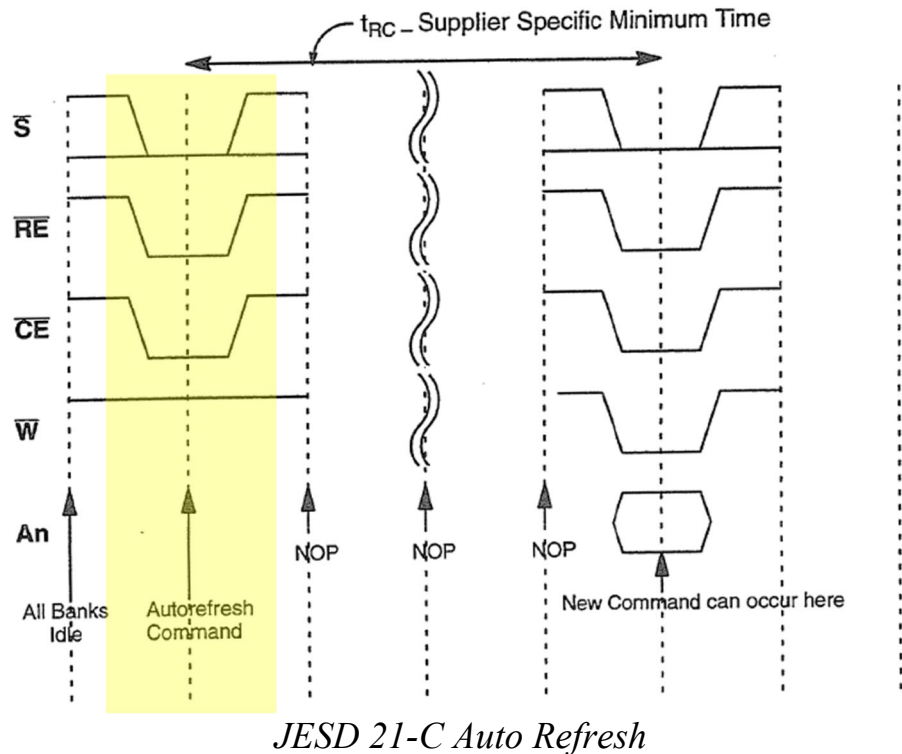
The device is now in the IDLE state and is ready for normal operation.”

EX1006 at page 3.11.5-9 (emphasis added).

99. JESD 21-C additionally discloses details of each of these command signals. The Background of the '589 Patent describes the prior art preparation command signal for word line activation as a "PRE" or "PRECHARGE" event for all memory banks of the device. EX1001 at 1:53-55. A POSITA would have understood that this signal is intended to ensure that all memory cells are at an initial baseline charge prior to operation. JESD 21-C discloses the PRECHARGE signal. JESD 21-C discloses two different Precharge signals: Auto Precharge and Precharge All Banks. EX1006 at page 3.11.5-9. In Auto Precharge, "[t]he user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle." *Id.* To precharge all banks, "[t]he user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks."

100. The Background of the '589 Patent describes the prior art refresh command signal as an "ARF" or "AUTOREFRESH" signal. EX1001 at 2:2:52-53. A POSITA would have understood that the AUTOREFRESH signal is also associated with restoring charge on the memory cells. JESD 21-C discloses the AUTOREFRESH signal. JESD 21-C explains that "AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address being supplied

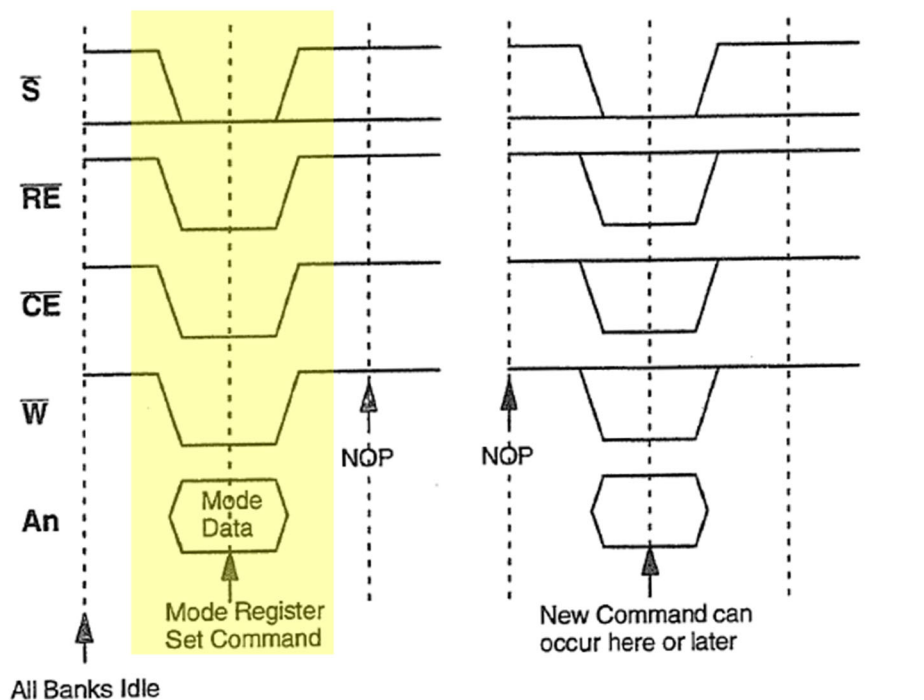
by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE).”



EX1006 at page 3.11.5-11.

101. The Background of the '589 Patent describes the prior art loading configuration register command signal as an “MRS” or “MODE-REGISTER-SET” signal. EX1001 at 2:2:53-54. JESD 21-C discloses the MODE-REGISTER-SET signal. JESD 21-C provides the timing diagram necessary to initiate a Mode-Register-Set Command in Section 3.11.5.7. “The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set

cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.”



JESD 21-C Mode Register Write Timing

EX1006 at page 3.11.5-10.

102. A POSITA would have understood that Kocis can accept the three further command signals listed above. In particular, a POSITA would have understood that the CASB and RASB (CAS and RAS with low activation) inputs identified in Lee are standard DRAM inputs. Thus, a POSITA would have understood that the proper sequencing of inputs on the CASB and RASB signals, along with other control signals, could be used to generate each of the Precharge, AutoRefresh, and Mode-Register-Set commands, as described in the JESD 21-C standard.

103. Accordingly, the combination of Kocis and JESD 21-C discloses that the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit including at least one of (i) a preparation command signal for word line activation, (ii) a refresh command signal, and (iii) a loading configuration register command signal.

D. Claim [8]: The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard

104. The combination of Kocis and JESD 21-C discloses the initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard. Although neither claim 8 nor the '589 Patent specification identify any particular JEDEC standard that this claim was intended to cover, the background of the '589 Patent does disclose that one predetermined proper initialization sequence that conforms to an unnamed JEDEC standard constitutes the commands PRECHARGE, AUTO REFRESH, and MODE-REGISTER-SET in the following chronological order: (1) PRECHARGE, (2) AUTOREFRESH, and (3) MODE-REGISTER-SET. *See* EX1001 at 1:43-61; *id.* at FIG. 3, 5:10-16, 4:59-5:21, claim 10. The background section of the '589 Patent admits that this sequence is known and incorporated in a JEDEC standard for

SDRAM that was available as of the filing of the '589 Patent. EX1001 at 1:43-61.

Indeed, JESD 21-C does in fact teach this exact sequence for initialization of SDRAM:

“The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge* commands for all banks of the device.
4. Issue 8 or more *autorefresh* commands.
5. Issue a *mode register set* command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.”

EX1006 at page 3.11.5-9 (emphasis added).

105. As previously discussed, JESD 21-C is a JEDEC standard. *See, e.g.*, EX1006 at Copyright Notice; *id.* at 1-1 (“This standard is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council through September, 1989.”). Accordingly, the combination of Kocis and JESD 21-C teaches identification of an initialization sequence that is identified as a predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

- E. Claim [10]: The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal**

106. As described in my analysis of claims [2] and [8] in Sections XI.C and XI.D, the combination of Lee and JESD 21-C teaches each of a preparation command signal for word line activation (precharge / PRE), refresh command signal (autorefresh / ARF), and loading configuration register command signal (mode register set / MRS). JESD 21-C further discloses the claimed predetermined proper initialization sequence.

107. Claim 10 recites that the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

Claimed Order 1	PRE	ARF	MRS
Claimed Order 2	PRE	MRS	ARF
Claimed Order 3	MRS	PRE	ARF

108. JESD 21-C discloses the first claimed order: “The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs

2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge commands* for all banks of the device.
4. Issue 8 or more *autorefresh commands*.
5. Issue a *mode register set command* to initialize the mode register.”

EX1006 at page 3.11.5-9 (emphasis added).

109. Accordingly, the combination of Kocis and JESD 21-C disclose all of the elements of claim [10].

F. Claim [12]: The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals

110. For the same reasons discussed in Section XI.C with respect to claim [2], Kocis in combination with JESD 21-C discloses the method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

XII. Claims 1 and 11 are Anticipated by or Obvious Over Lee

111. In my opinion, Lee anticipates or renders obvious claims 1 and 11 of the '589 Patent.

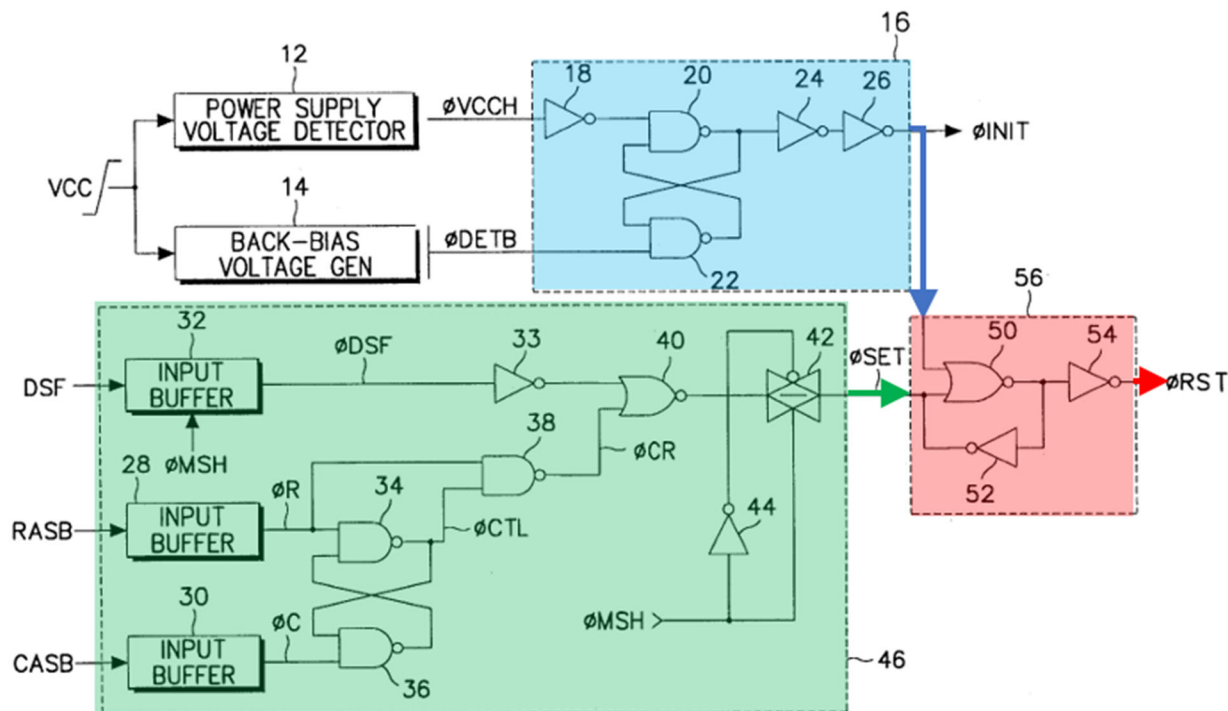
A. Overview of Lee

112. Lee (attached as EX1005) was filed on August 23, 1996 and claims priority to Korean Document No. 26181/1995 dated August 23, 1995. EX1005. Lee explains that as semiconductor memory devices become more complicated, they require initialization circuits for resetting the various functional circuits within the chip. EX1005 at 1:18-27. Traditionally, power-on reset circuits were provided to ensure stable power sources. *Id.* Lee takes this one step further and seeks to additionally provide an initialization circuit for semiconductor memory that is based on external logic signals. EX1005 at 2:21-23.

113. Lee describes an initialization circuit for a semiconductor memory device which includes an initialization signal generator that generates an initialization signal in response to a specific sequence of reset control signals. EX1005 at Abst. The initialization signal is activated when three reset control signals are activated in the proper sequence and is deactivated when one of the control signals is deactivated. *Id.*

114. Lee contains both a first and second initialization signal generator. The first initialization circuit generator 46 is triggered based on the correct sequence of control signals DSF, RASB, and CASB. EX1005 at 3:9-22. The second initialization circuit generator 16 is triggered based on proper powerup of the power source. *Id.* Both of these initialization circuit generators are displayed in Lee Figure

3, which I have annotated below with the first initialization circuit generator in green and second initialization circuit generator in blue.



EX1005 (Lee) at Figure 3 (annotated)

115. The resulting initialization signals are then sent to Lee's transfer unit 56 (shown in red), which, based on the initialization signals, generates a reset signal ϕRST sent "to a circuit to be initialized within the chip." EX1005 at 4:14-24, 4:59-5:4.

B. Claim 1

1. Claim Element [1.P]: A dynamic semiconductor memory device of a random access type

116. I understand that the preamble of claim 1 is not limiting. Nevertheless, to the extent the preamble is found to be limiting, the devices described in Lee

disclose “a dynamic semiconductor memory device of a random access type.” In particular, Lee is directed to an “initialization circuit for a *semiconductor memory device*.” EX1005 at Abst. (emphasis added). The stated objects of the Lee disclosure include: (1) “to reliably initialize a *semiconductor memory device* when a power-up reset circuit malfunctions” and (2) “to initialize a *semiconductor memory device* in response to external logic signals.” EX1005 at 2:18-23 (emphasis added).

117. A POSITA would have understood that the semiconductor memory device of Lee is a dynamic device of a random access type. In particular, a POSITA would have understood that the input signals CASB and RASB are specific to Dynamic Random Access Memory (DRAM) type devices. Column Address Strobe (CAS) and Row Address Strobe (RAS) signals have to do with multiplexing of column and row lines on the same address pins and are used almost exclusively on DRAMs. First a column address is provided, then the CAS strobe occurs, then a row address is provided, then the RAS strobe occurs. This procedure requires half as many address pins as the same pins are used for both column and row addressing. A POSITA would have understood that the “B” in CASB and RASB refers to “bar” which means that the signals are low active.

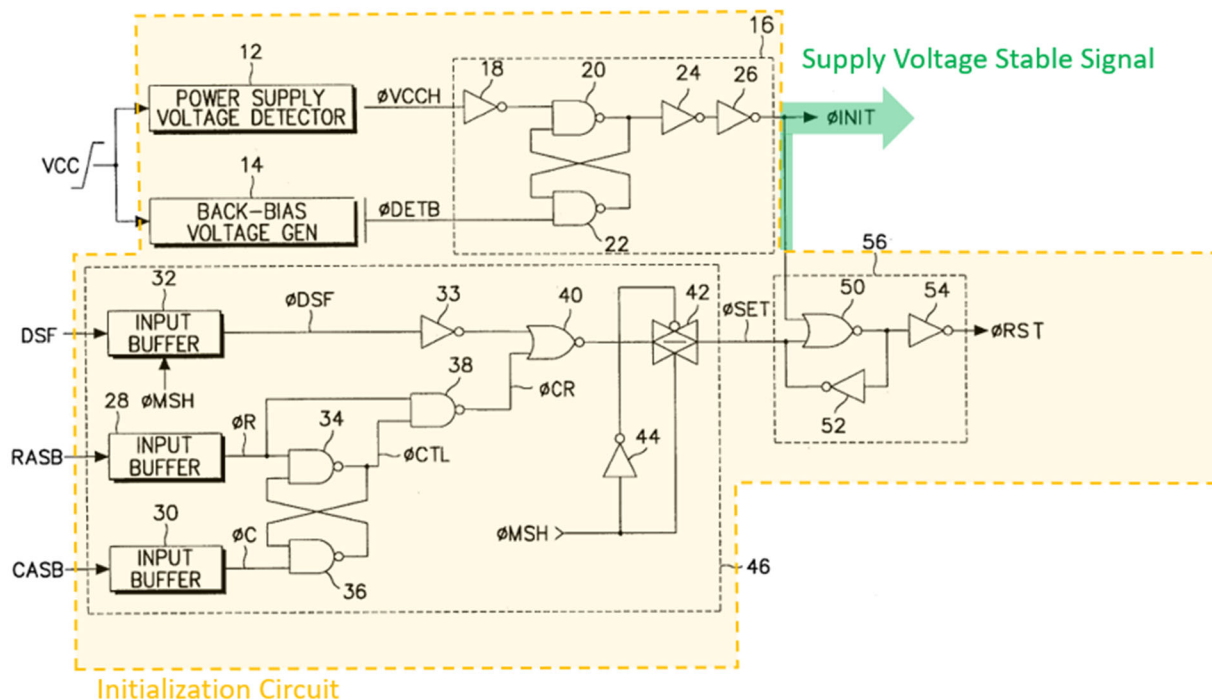
118. As further support that a POSITA would recognize this functionality, Release 7 of JEDEC Standard No. 21-C, entitled Configurations for Solid State Memories, and which is dated January 1997 indicates that that CAS signal is “an

enable signal that on some *dynamic RAMs* actuates only the column oriented internal circuits and the data input/output circuits. Most Devices normally require the RAS\ signal to be present for the CAS\ signal to be effective.” EX1006 at page 2-2. The RAS signal is defined similarly, as “a chip enable signal that, on certain *dynamic RAMs*, actuates only row address oriented internal circuitry.” EX1006 at page 2-4.

119. Accordingly, Lee discloses claim element [1.P].

2. Claim Element [1.1]: an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation

120. Lee discloses an initialization circuit that (1) controls a switching-on operation and (2) supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. In order to better demonstrate the initialization circuit, I have included an annotated version of Lee Figure 3 below, which shows components of Lee (namely elements 12, 14, 16, 46, and 56) that disclose the claimed initialization circuit, outlined in yellow.



EX1005 (Lee) at Figure 3 (annotated)

121. The initialization circuit shown above in yellow controls a switching-on operation (*i.e.*, the process for powering on the memory chip). For example, Lee explains that these types of “initialization circuits are typically referred to as power on reset circuits and generate a reset signal in response to a power supply voltage VCC being applied to the [DRAM] chip. The typical power on reset circuit operates by sensing the level of the power supply voltage VCC and generating an initialization signal for a predetermined length of time when the power supply voltage reaches a predetermined level.” EX1005 at 1:18-29.

122. The initialization circuit supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. Lee indicates that the circuit “includes a first initialization signal generator 46, a second

initialization signal generator 16 and a transfer unit 56. The first initialization signal generator generates a first initialization signal ϕ SET in response to a sequence of reset control signals DSF, RASB, and CASB. The second initialization signal generator 16 . . . generates a second initialization signal ϕ INIT in response to the power-up of a power supply VCC. The transfer unit 56 generates a reset signal ϕ RST for resetting a circuit within the memory device responsive to the first and second initialization signals.” *Id.* at 3:9-23.

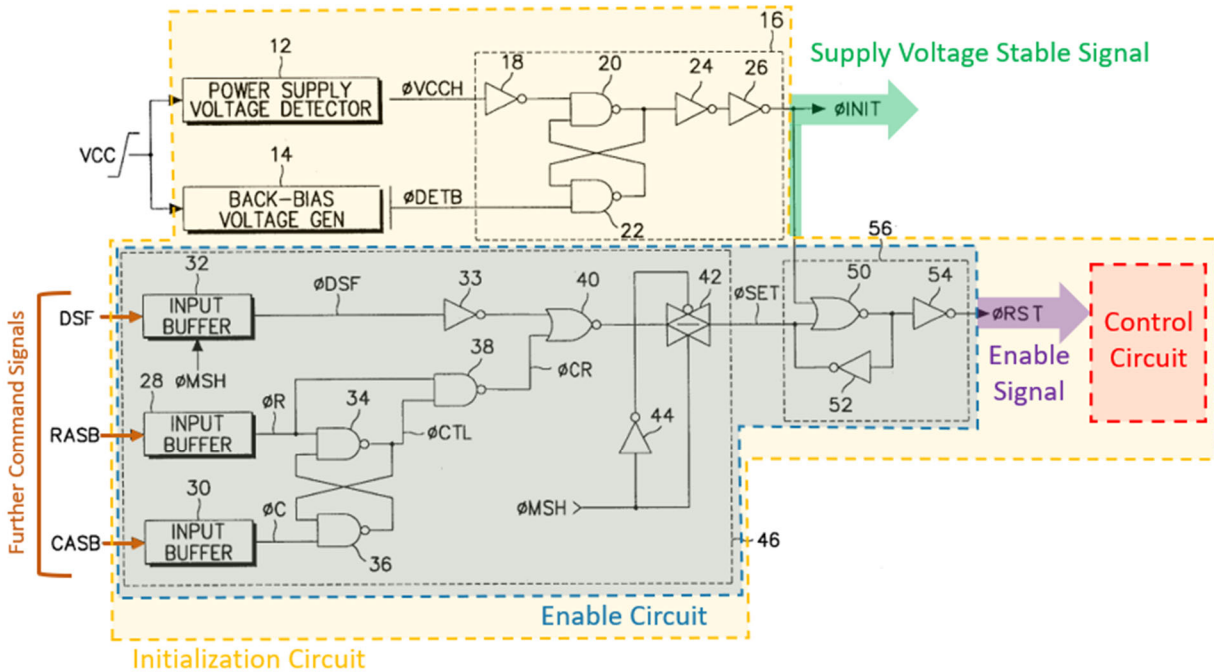
123. One of skill in the art would understand that the ϕ INIT signal (outlined in green in the annotated figure above) discloses the claimed supply voltage stable signal. The '589 Patent indicates that the supply voltage stable signal (*i.e.*, the “POWERON” signal) is active if the internal supply voltages have reached the values necessary for the proper operation of the memory device. EX1001 at 1:13-16, 2:1-4. Similarly, the ϕ INIT signal goes to a logic high level immediately in response to the power supply detection signal ϕ VCCH, which monitors the voltage level of the power supply voltage (VCC), and subsequently goes low upon detection of the proper device operating voltages, which is triggered by a low voltage on the ϕ DETB signal. EX1005 at 1:31-34, 1:47-54. Furthermore, Lee explains that the ϕ INIT signal is generated “in response to the power-up of a power supply VCC” (*id.* at 3:9-23) meaning it is supplied once a supply voltage has been stabilized after the switching-on operation. The low voltage on the ϕ RST signal, triggered by the

ϕ DETB signal going low, is the indication that the supply voltage VCC has stabilized. EX1005 at FIG. 2, 1:34-40.

124. Accordingly, a POSITA would have understood that Lee discloses an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation.

3. Claim Element [1.2]: said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals

125. Lee discloses an initialization circuit (i) an enable circuit for receiving the supply voltage stable signal and externally applied further command signals and (ii) a control circuit for controlling operations. In order to better illustrate the combination, I have again annotated Figure 3 of Lee with the claimed control circuit (red), enable circuit (blue), and further command signals (brown), below.



EX1005 (Lee) at Figure 3 (annotated)

126. Lee discloses the claimed enable circuit. Specifically, Lee’s first initialization signal generator 46 and transfer unit 56 disclose the claimed enable circuit (shown in blue above). As recited in claim 1, the enable circuit receives both the supply voltage stable signal (shown in green above) and externally applied further command signals (shown in brown above). As discussed in element [1.1], Lee’s ϕINIT signal discloses the claimed supply voltage stable signal. This signal is received by the transfer unit 56 of Lee, as shown in Lee Figure 3. EX1005 at FIG. 3; *see also id.* at 4:33-35, 4:59-62.

127. Lee also discloses that the enable circuit receives the externally applied further command signals. The ’589 Patent identifies the command signals as “a preparation command signal for word line activation (PRECHARGE), and/or a

refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).” EX1001 at 2:50-54. A POSITA would have understood that Lee discloses similar command signals in the CASB, RASB, and DSF signals shown in Lee’s Figure 3. *See supra*, at Section VII. Lee describes the CASB, RASB, and DSF signals as a first control signal, second control signal, and mode selection signal, respectively, each of which are inputs to the first initialization signal generator 46. EX1005 at 3:37-49. CASB is a column address strobe signal and RASB is a row address strobe signal. CAS and RAS signals have to do with multiplexing of column and row lines on the same address pins. CAS and RAS signals are primarily used to instruct the memory chip to activate or open a row and then to read a column within the activated row. First a column address is provided, then the CAS strobe occurs, then a row address is provided, then the RAS strobe occurs. A POSITA would have understood that the “B” in CASB and RASB refers to “bar,” which indicates that the signals are low active. DSF is a special function enable input that, when true, can actual certain special functions on the memory chip. Lee refers to these three signals collectively as “reset control signals.” EX1005 at 3:14-16. A POSITA would recognize that these signals are command signals as they provide specific commands to the memory chip.

128. Additionally, the CASB and RASB signals are further command signals because a POSITA would have understood that they can be used to generate

the PRECHARGE, AUTOREFRESH, and MODE-REGISTER-SET commands disclosed in the '589 Patent. CAS and RAS are fundamental DRAM signals. Additional DRAM signals include Chip Select (CS), which enables the memory chip's command decoder and Write Enable (WE), which enables writing to memory registers. A POSITA would have understood that applying certain inputs to these signals in a certain sequence will initiate certain commands on the memory chip. These commands are performed by way of a command decoder, which accepts the RAS, CAS, CS, and WE signals and interprets the sequence as a particular command. Depending on the combination of these signals, a different command is requested and performed on the memory chip. For example, a POSITA would have understood that the PRECHARGE command is performed by activating CS, RAS, and WE and leaving CAS inactive. *See, e.g.*, EX1019 at 10.

129. Lee additionally teaches to a POSITA or, in the alternative, renders obvious a control circuit for controlling operations (shown in red above). *See, e.g.*, EX1005 at 4:20-24 (“An inverter 54 has an input terminal connected to the output terminal of NOR gate 50 and an output terminal which forms the output terminal of the transfer unit 56 for sending the reset signal ϕ RST to a circuit to be initialized within the chip.”); *id.* at 4:59-62 (“The transfer unit 56 combines the first initialization signal ϕ SET and the second initialization signal ϕ INIT and activates the reset signal ϕ RST by driving it to a high logic level, thereby initializing the

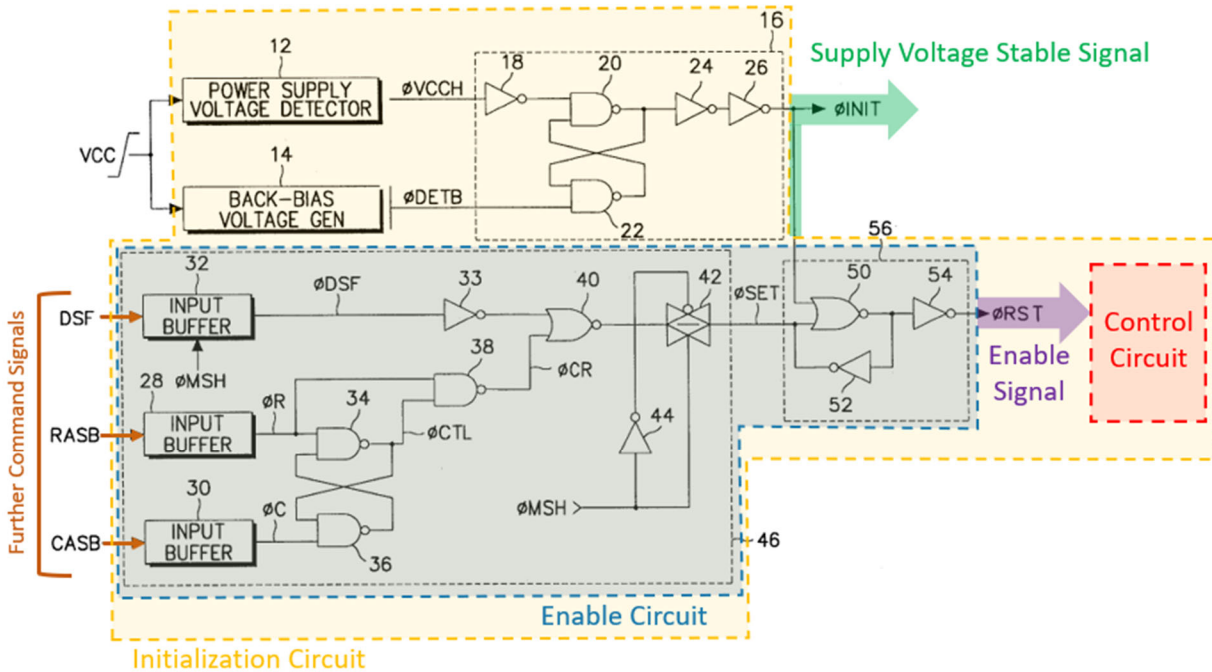
circuits within the chip.”); *id.* at 5:11-13 (“In the embodiment of FIG. 3, the first and second initialization signals are supplied to individual circuits via one transfer unit.”); *id.* at 3:19-22 (“The transfer unit 56 generates a reset signal ϕ RST for resetting a circuit within the memory device responsive to the first and second initialization signals.”); *id.* at 4:35-37 (“Thus, all circuits within the chip which are connected to the output terminal of transfer unit 56 is held in the initialized state.”); *id.* at 1:20-21 (“Such devices require initialization circuits for resetting the various functional circuits within the chip.”).

130. Based on this disclosure, a POSITA would have understood that Lee discloses the claimed control circuit. In particular, a POSITA would have understood that all memory devices have control circuits for controlling operations. These circuits are necessary because sequences of commands are sent to the memory device in order to perform reads and writes to memory cells and to perform configuration operations. A POSITA would have understood that there would be a control circuit that receives these external commands and controls the internal operation of the memory device so as to properly respond to the commands. A POSITA would also understand that every control circuit needs to be initialized in order for it to operate reliably. In fact, as a basic part of undergraduate courses in logic design, electrical engineers are taught that every sequential circuit (a circuit that maintains state), such as a control circuit, needs a reset mechanism to ensure

that it powers up in a known state. Powering up sequential logic without initialization could lead to an unknown state and unpredictable operation. Thus, it follows that a memory device requires an initialization sequence that resets the control circuit and this initialization sequence must be complete before operation of the memory device can take place. Accordingly, Lee discloses, or at the very least renders obvious, an initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals.

4. **Claim Element [1.3]: said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit**

131. Lee discloses that (1) the enable circuit outputs an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and (2) the enable signal unlatches the control circuit. With reference again to the annotated combination (reproduced below), Lee's ϕ RST signal (shown in purple) which is output from transfer unit 56 discloses the enable signal output from the enable circuit.



EX1005 (Lee) at Figure 3 (annotated)

132. As explained in Lee, the ϕRST signal is set to a high voltage immediately after power is applied, triggered by the $\phi INIT$ signal going high, and only goes to a low voltage after a predetermined proper initialization sequence of the externally applied further command signals (*i.e.*, Lee signals CASB, RASB, and DSF). “[I]f the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence, the first initialization signal generator activates the first initialization signal ϕSET . For this to occur, the reset control signals DSF, RASB, and CASB must be activated in the CBR (CAS before RAS) mode. The mode selection clock signal ϕDSF is first activated, *i.e.*, driven to a high-logic level. . . . If the first control signal CASB is then activated by being driven to a low logic state, . . . [t]hen, if the second control signal RASB is driven to the active low logic level, .

. . the first initialization signal ϕSET [is activated] at the output terminal of NOR gate 40. . . . The transfer unit 56 combines the first initialization signal ϕSET and the second initialization signal ϕINIT and activates the reset signal ϕRST by driving it to a high logic level.” EX1005 at 4:38-61.

133. After the initialization sequence is complete, the ϕRST signal goes to a low logic level. Thus, once the reset signal ϕRST is driven to a low logic level, it unlatches the control circuit. *See, e.g.*, EX1005 at 4:59-5:4 (“The transfer unit 56 combines the first initialization signal ϕSET and the second initialization signal ϕINIT and activates the reset signal ϕRST by driving it to a high logic level, thereby initializing the circuits within the chip.”); *id.* at 4:13-24 (“The transfer unit 56 includes . . . an output terminal which forms the output terminal of the transfer unit 56 for sending the reset signal ϕRST to a circuit to be initialized within the chip.”). A POSITA would have understood that initializing the circuit within the chip, followed by deactivating the reset signal, as is disclosed in Lee, teaches unlatching the control circuit because it causes the start of normal operation of the buffers.

134. Accordingly, a POSITA would have understood that Lee discloses the enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

C. Claim 11

1. **Claim Element [11.P]: An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components**

135. For the same reasons discussed in Sections XII.B.1 and XII.B.2 with respect to claim elements [1.P] and [1.1], Lee discloses an improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components.

2. **Claim Element [11.1]: supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device**

136. For the same reasons discussed in Section XII.B.2 with respect to claim element [1.1], Lee discloses supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device.

3. **Claim Element [11.2]: supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a**

proper operation of the dynamic semiconductor memory device

137. For the same reasons discussed in Section XII.B.3 with respect to claim element [1.2], Lee discloses the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device. Furthermore, for the same reasons discussed in Section XII.B.4 with respect to claim element [1.3], Lee discloses supplying, via an enable circuit of the initialization circuit, an enable signal ... after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

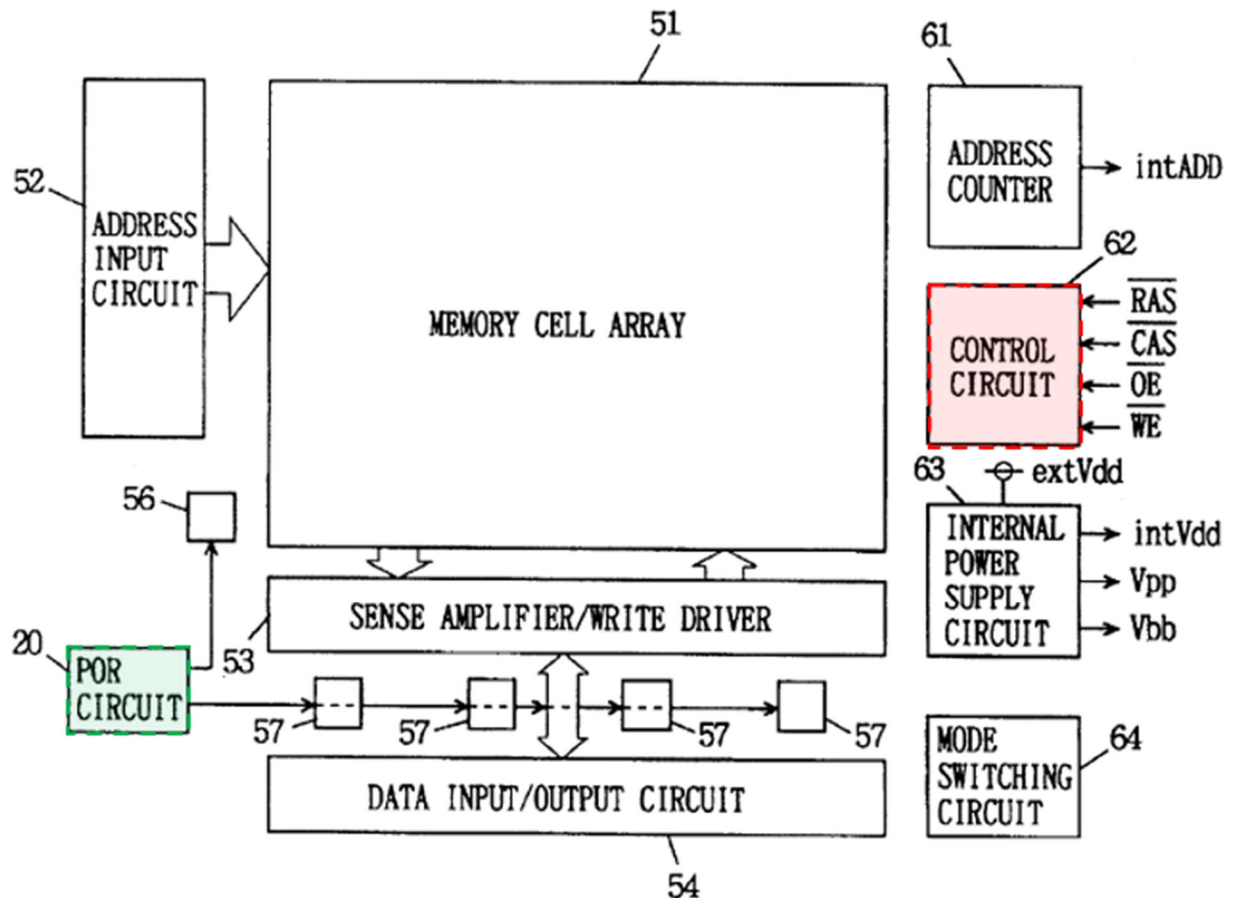
XIII. Claims 1 and 11 are Obvious Over Lee in Combination with Iketani

138. In my opinion, Lee in combination with Iketani renders obvious claims 1 and 11 of the '589 Patent.

A. Overview of Iketani

139. Iketani was filed on February 28, 1996. EX1007 at [22]. Iketani describes a power on reset circuit for use in a DRAM memory device for initializing the internal circuitry thereof when the power is turned on. EX1007 at 1:5-13. In particular, Iketani recognizes that if the power supply voltage for a memory device chip fluctuates significantly, traditional power on reset circuits may activate, causing inadvertent initialization of the chip. EX1007 at 1:59-62. As such, Iketani seeks to

provide an improved power on reset circuit that does not erroneously generate such a signal upon power fluctuation. EX1007 at 2:1-4. As shown in Figure 6 of Iketani (reproduced below), in certain embodiments, Iketani discloses this improved power on reset circuit (shown in green) which generates a power on reset signal that it sends to various components, including a control circuit 62 (shown in red). These circuits are initialized in response to the power on reset signal. *See* EX1007 at 5:20-26 (“The power on reset signal generated by power on reset circuit 20 is supplied to address counter 61, control circuit 62, internal power supply circuit 63, mode switching circuit 64, redundant row program circuit 56, redundant column program circuit 57 and so on. Therefore, these circuits 61 to 64, 56, 57 are initialized in response to the power on reset signal.”).

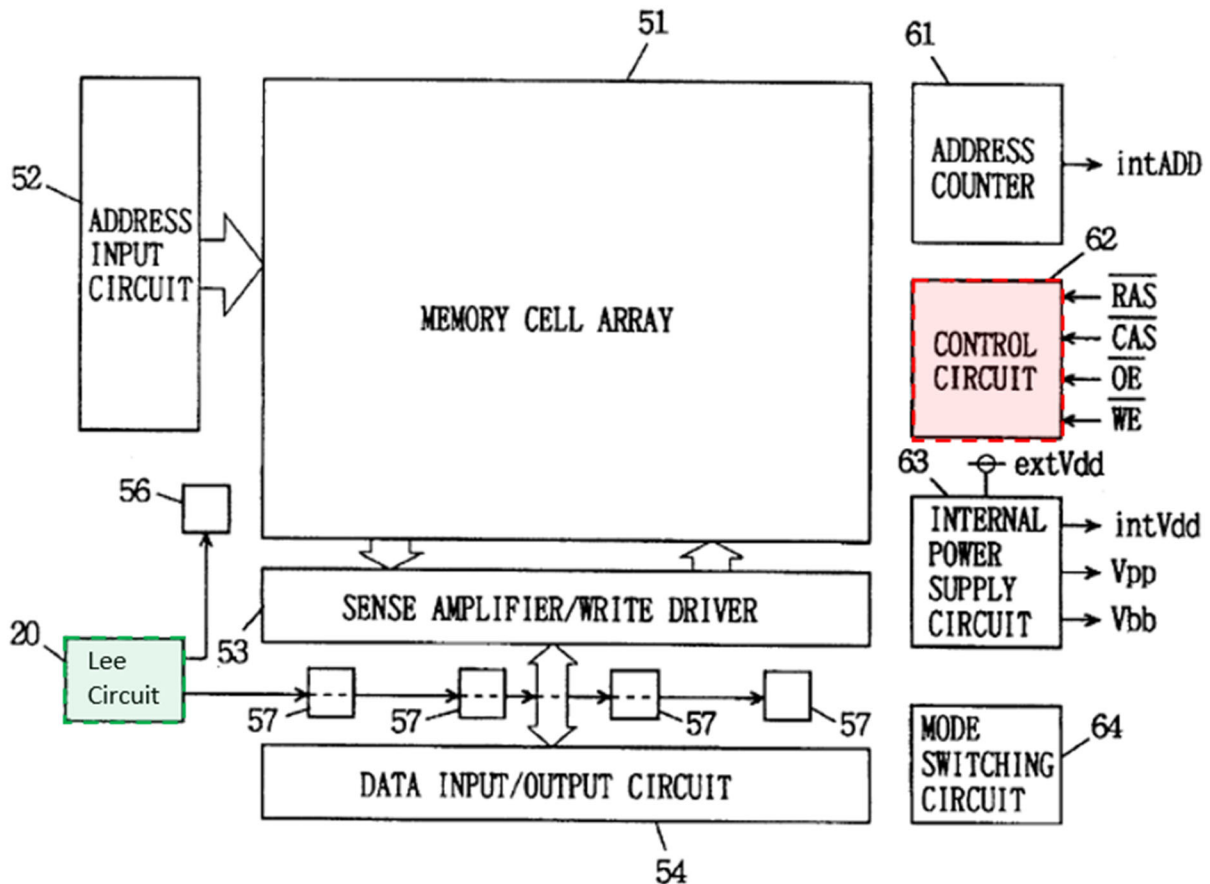


EX1007 (Iketani) at Figure 6 (annotated)

B. Combination of Lee and Iketani

140. The disclosed circuit configurations of Lee and Iketani can and would have been combined to arrive at the claimed memory device of the '589 patent. In particular, a POSITA could and would have recognized that the initialization circuit of Lee is compatible with the controller of Iketani and would have combined the disclosure of Lee with that of Iketani. While Lee does expressly illustrate the “circuitry” that is initialized by the reset signal ϕRST output from its initialization circuit, Iketani illustrates and describes in detail the various circuits, including the control circuit, that receive and are initialized by such an initialization signal.

141. In particular, the initialization circuit disclosed in Lee has the same functionality as the power on reset circuit 20 of Iketani. Both the power on reset circuit of Iketani and the initialization circuit of Lee perform similar functions and are used for the same purpose. *Compare* EX1005 at 2:4-6, 18-20 (“A problem with [a conventional initialization circuit] is that it may malfunction if the power supply voltage VCC is unstable input. . . . It is therefore an object of the invention to reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions.”) *with* EX1007 at 2:1-4 (“[a]nother object of the present invention is to provide a power on reset circuit which does not erroneously generate a reset signal even when the power supply voltage fluctuates significantly.”). As shown in Iketani Figure 6, annotated below, Lee’s initialization circuit (shown in green) can be substituted for Iketani’s power on reset circuit.



EX1007 (Iketani) at Figure 6 (annotated)

142. Furthermore, both Lee's initialization circuit and Iketani's power on reset circuit output similar signals. Compare EX1005 at 4:59-62 ("The transfer unit 56 combines the first initialization signal ϕ SET and the second initialization signal ϕ INIT and activates the reset signal ϕ RST by driving it to a high logic level, thereby initializing the circuits within the chip.") with EX1007 at 1:36-38 ("In response to the power on reset signal POR at the L level, internal circuitry of the SRAM, DRAM or the like is initialized."). As Iketani's power on reset circuit outputs signals that are accepted by the control circuit, a POSITA would have understood that Lee's

initialization circuit is additionally compatible with Iketani's control circuit. *See* EX1007 at 5:20-26 ("The power on reset signal generated by power on reset circuit 20 is supplied to address counter 61, control circuit 62, internal power supply circuit 63, mode switching circuit 64, redundant row program circuit 56, redundant column program circuit 57 and so on. Therefore, these circuits 61 to 64, 56, 57 are initialized in response to the power on reset signal.").

143. This amounts to a simple substitution of one component (*i.e.*, Lee's initialization circuit) for another (*i.e.*, Iketani's power on reset circuit), and a POSITA would have understood that this substitution would yield predicable results.

C. Claim 1

1. Claim Element [1.P]: A dynamic semiconductor memory device of a random access type

144. For the same reasons discussed in Section XII.B.1 with respect to claim element [1.P], Lee disclosed the preamble. Furthermore, Lee in combination with Iketani discloses a dynamic semiconductor memory device of a random access type through Iketani's express disclosure of a DRAM. *See* EX1007 at FIG. 6 and 5:4-26.

2. Claim Element [1.1]: an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation

145. For the same reasons discussed in Section XII.B.2 with respect to claim element [1.1], Lee in combination with Iketani discloses an initialization circuit

controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation.

3. Claim Element [1.2]: said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals

146. For the same reasons discussed in Section XII.B.3 with respect to claim element [1.2], Lee discloses initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals.

147. The combination of Lee and Iketani further discloses the claimed control circuit for controlling operations. Iketani's control circuit 62 is for "controlling internal circuitry" of the memory device and initializes the memory device in response to the power on reset signal. *See* EX1007 at 5:12-26 ("The power on reset signal generated by power on reset circuit 20 is supplied to address counter 61, *control circuit* 62, internal power supply circuit 63, mode switching circuit 64, redundant row program circuit 56, redundant column program circuit 57 and so on. Therefore, these circuits 61 to 64, 56, 57 are initialized in response to the power on reset signal.") (emphasis added); *see also* EX1007 at FIG. 6 (identifying control circuit 62). A POSITA would have understood that this disclosure teaches the claimed control circuit for controlling operations.

4. **Claim Element [1.3]: said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit**

148. For the same reasons discussed in Section XII.B.4 with respect to claim element [1.3], Lee in combination with Iketani discloses an enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit. The combination of Lee and Iketani further discloses that the control circuit is unlatched by an enable signal through Iketani's disclosure that the control circuit is initialized by the reset signal. *See* EX1007 at 5:12-26.

D. Claim 11

1. **Claim Element [11.P]: An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components**

149. For the same reasons discussed in Sections XIII.C.1 and XIII.C.2 with respect to claim elements [1.P] and [1.1], Lee in combination with Iketani discloses an improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components.

2. **Claim Element [11.1]: supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device**

150. For the same reasons discussed in Section XIII.C.2 with respect to claim element [1.1], Lee in combination with Iketani discloses supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device.

3. **Claim Element [11.2]: supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device**

151. For the same reasons discussed in Section XIII.C.3 with respect to claim element [1.2], Lee in combination with Iketani discloses the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device. Furthermore, for the same reasons discussed in Section XIII.C.4 with respect to claim element [1.3], Lee in combination with Iketani discloses supplying, via an enable circuit of the initialization circuit, an enable signal ... after an identification of a predetermined

proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

XIV. Claims 2, 8, 10, and 12 are Obvious Over Lee in Combination with JESD 21-C

152. In my opinion, Lee in combination with JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Lee disclosing or rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Sections XII.B and XII.C, *supra*).

A. Combination of Lee and JESD 21-C

153. JESD 21-C provides various standardized signals, timing diagrams, and other specifications for solid state memory in order to promote interoperability between products. This information includes a power-up sequence to initialize memory to an IDLE state for normal operation in an attempt to eliminate errors during power-up. EX1006 at page 3.11.5-9. As described above, Lee discloses the necessary circuitry for proper initialization and power-up of dynamic random access memory, and also has the same stated goal of JESD 21-C (*i.e.*, to initialize memory to an IDLE state for normal operation in an attempt to eliminate errors during power-up). *See* EX1005 at 2:4-7; *id.* at 2:18-20.

154. A POSITA would have been motivated to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Lee in order to

ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by the POSITA. This improvement constitutes the use of a known technique (*i.e.*, the initialization signals and timing for memory devices, including DRAM and SDRAM disclosed in JESD 21-C) to improve similar devices (*i.e.*, the memory devices, including DRAM disclosed in Lee) in the same way (*i.e.*, by applying the same initialization signals and timing disclosed in JESD 21-C).

155. This improvement is also a simple substitution of the signals and timing of Lee with the signals and timing specified in JESD 21-C. A POSITA would have understood that substituting the signals and timing element of JESD 21-C for those of Lee would yield predictable results. Specifically, incorporating JESD 21-C's signals and timing would ensure interoperability and compatibility with other products in the solid state memory field. For example, if using the initialization circuit of Lee with SDRAM instead of DRAM, a POSITA would have been motivated to use the SDRAM initialization sequence disclosed and standardized in JESD 21-C.

B. Claim [2]: The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation

command signal for word line activation, a refresh command signal, and a loading configuration register command signal

156. The Combination of Lee and JESD 21-C discloses that the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit including at least one of (i) a preparation command signal for word line activation, (ii) a refresh command signal, and (iii) a loading configuration register command signal.

157. JESD 21-C discloses each of the claimed further command signals and the predetermined proper initialization sequence of such signals. JESD 21-C teaches the following sequence for initialization of SDRAM:

“The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge* commands for all banks of the device.
4. Issue 8 or more *autorefresh* commands.
5. Issue a *mode register set* command to initialize the mode register.

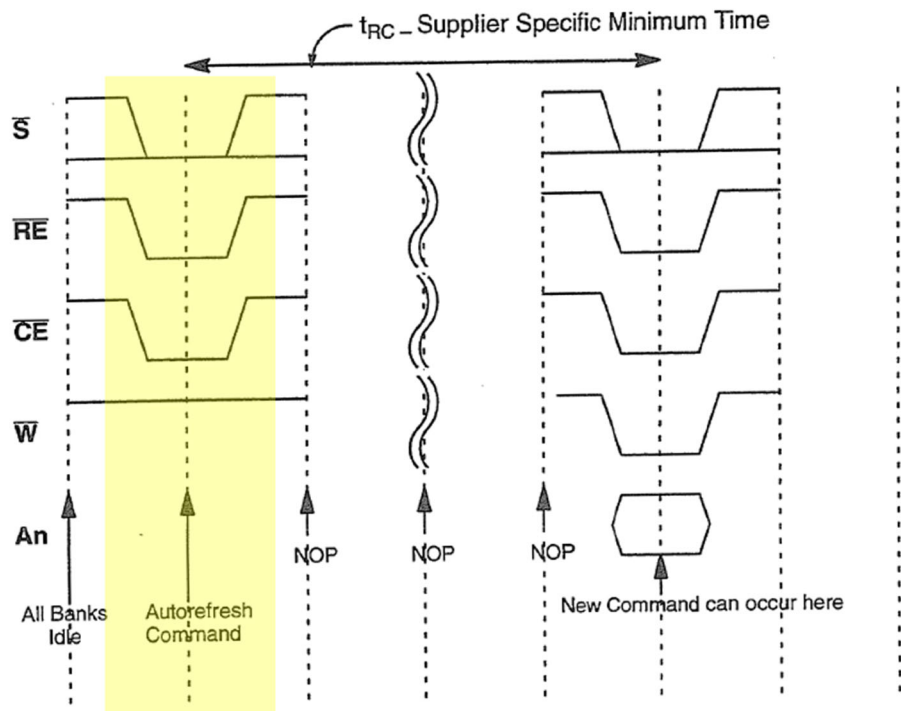
The device is now in the IDLE state and is ready for normal operation.”

EX1006 at page 3.11.5-9 (emphasis added).

158. JESD 21-C additionally discloses details of each of these command signals. The Background of the '589 Patent describes the prior art preparation

command signal for word line activation as a “PRE” or “PRECHARGE” event for all memory banks of the device. EX1001 at 1:53-55. A POSITA would have understood that this signal is intended to ensure that all memory cells are at an initial baseline charge prior to operation. JESD 21-C discloses the PRECHARGE signal. JESD 21-C discloses two different Precharge signals: Auto Precharge and Precharge All Banks. EX1006 at page 3.11.5-9. In Auto Precharge, “[t]he user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle.” *Id.* To precharge all banks, “[t]he user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks.”

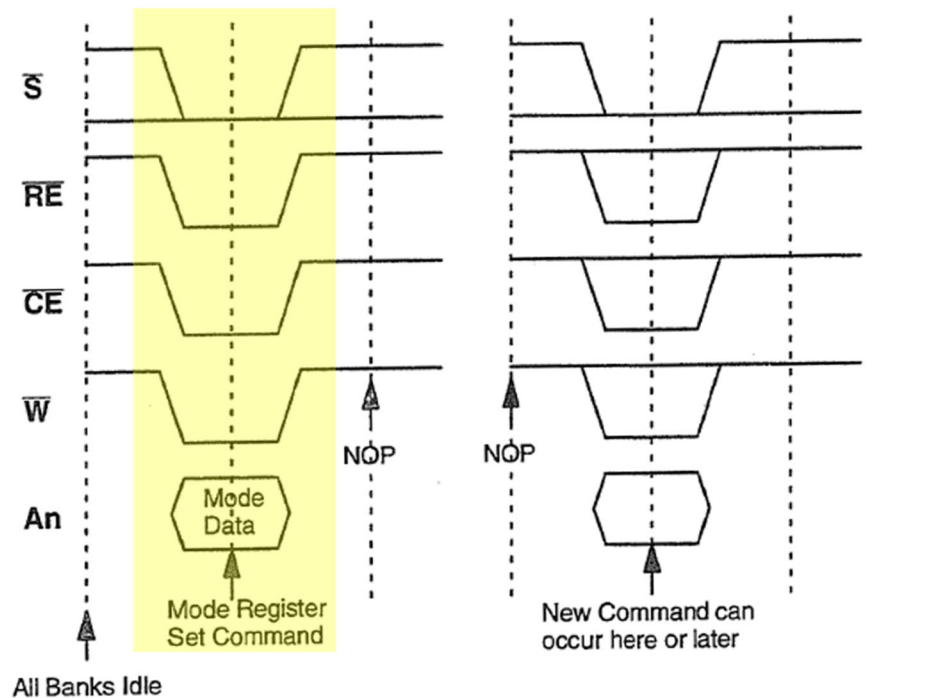
159. The Background of the ’589 Patent describes the prior art refresh command signal as an “ARF” or “AUTOREFRESH” signal. EX1001 at 2:2:52-53. A POSITA would have understood that the AUTOREFRESH signal is also associated with restoring charge on the memory cells. JESD 21-C discloses the AUTOREFRESH signal. JESD 21-C explains that “AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address being supplied by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE).”



JESD 21-C Auto Refresh

EX1006 at page 3.11.5-11.

160. The Background of the '589 Patent describes the prior art loading configuration register command signal as an “MRS” or “MODE-REGISTER-SET” signal. EX1001 at 2:2:53-54. JESD 21-C discloses the MODE-REGISTER-SET signal. JESD 21-C provides the timing diagram necessary to initiate a Mode-Register-Set Command in Section 3.11.5.7. “The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.”



JESD 21-C Mode Register Write Timing

EX1006 at page 3.11.5-10.

161. A POSITA would have understood that Lee can accept the three further command signals listed above. In particular, a POSITA would have understood that the CASB and RASB (CAS and RAS with low activation) inputs identified in Lee are standard DRAM inputs. Thus, a POSITA would have understood that the proper sequencing of inputs on the CASB and RASB signals, along with other control signals, could be used to generate each of the Precharge, AutoRefresh, and Mode-Register-Set commands, as described in the JESD 21-C standard.

162. Accordingly, the combination of Lee and JESD 21-C discloses that the externally applied further command signals forming the predetermined proper

initialization sequence to be identified by said enable circuit including at least one of (i) a preparation command signal for word line activation, (ii) a refresh command signal, and (iii) a loading configuration register command signal.

C. Claim [8]: The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard

163. The Combination of Lee and JESD 21-C discloses the initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard. Although neither claim 8 nor the '589 Patent specification identify any particular JEDEC standard that this claim was intended to cover, the '589 Patent does disclose that one predetermined proper initialization sequence that conforms to an unnamed JEDEC standard constitutes the commands PRECHARGE, AUTO REFRESH, and MODE-REGISTER-SET in the following chronological order: (1) PRECHARGE, (2) AUTOREFRESH, and (3) MODE-REGISTER-SET. *See* EX1001 at 1:43-61; *id.* at FIG. 3, 5:10-16, 4:59-5:21, claim 10. The background section of the '589 Patent admits that this sequence is known and incorporated in a JEDEC standard for SDRAM that was available as of the filing of the '589 Patent. EX1001 at 1:43-61. JESD 21-C teaches this exact sequence for initialization of SDRAM:

“The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge* commands for all banks of the device.
4. Issue 8 or more *autorefresh* commands.
5. Issue a *mode register set* command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.”

EX1006 at page 3.11.5-9 (emphasis added).

164. As previously discussed, JESD 21-C is a JEDEC standard. *See, e.g.*, EX1006 at Copyright Notice; *id.* at 1-1 (“This standard is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council through September, 1989.”). Accordingly, the combination of Lee and JESD 21-C teaches identification of an initialization sequence that is identified as a predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

D. Claim [10]: The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command

signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal

165. As described in my analysis of claims [2] and [8] in Sections XIV.B and XIV.C, the combination of Lee and JESD 21-C teaches each of a preparation command signal for word line activation (PRE), refresh command signal (ARF), and loading configuration register command signal (MRS). JESD 21-C further discloses the claimed predetermined proper initialization sequence.

166. Claim 10 recites that the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

Claimed Order 1	PRE	ARF	MRS
Claimed Order 2	PRE	MRS	ARF
Claimed Order 3	MRS	PRE	ARF

167. JESD 21-C discloses the first claimed order: “The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge commands* for all banks of the device.
4. Issue 8 or more *autorefresh commands*.
5. Issue a *mode register set command* to initialize the mode register.”

EX1006 at page 3.11.5-9 (emphasis added).

168. Accordingly, the combination of Lee and JESD 21-C disclose all of the elements of claim [10].

E. Claim [12]: The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals

169. For the same reasons discussed in Sections XIV.B with respect to claim [2], Lee in combination with JESD 21-C discloses the method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

XV. Claims 2, 8, 10, and 12 are Obvious over Lee in Combination with Iketani and JESD 21-C

170. In my opinion, Lee in combination with Iketani and JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Lee and Iketani rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Sections XIII.C and XIII.D, *supra*).

A. Combination of Lee, Iketani, and JESD 21-C

171. For the reasons discussed in Sections XIII.B and XIV.A, a POSITA would have been motivated to combine the teachings of Lee, Iketani, and JESD 21-C.

- B. Claim [2]: The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal**

172. For the same reasons discussed in Section XIV.B with respect to claim [2], Lee in combination with Iketani and JESD 21-C discloses the semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

- C. Claim [8]: The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard**

173. For the same reasons discussed in Section XIV.C with respect to claim [8], Lee in combination with Iketani and JESD 21-C discloses the semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

- D. Claim [10]: The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal**

174. For the same reasons discussed in Section XIV.D with respect to claim [10], Lee in combination with Iketani and JESD 21-C discloses the semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal.

- E. Claim [12]: The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals**

175. For the same reasons discussed in Section XIV.E with respect to claim [12], Lee in combination with Iketani and JESD 21-C discloses The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

XVI. Claims 9 and 13 are Obvious Over Lee in Combination with Kocis

176. In my opinion, Lee in combination with Kocis renders obvious claims 9 and 13 of the '589 Patent, with Lee disclosing or rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Sections XII.B and XII.C, *supra*).

A. Combination of Lee and Kocis

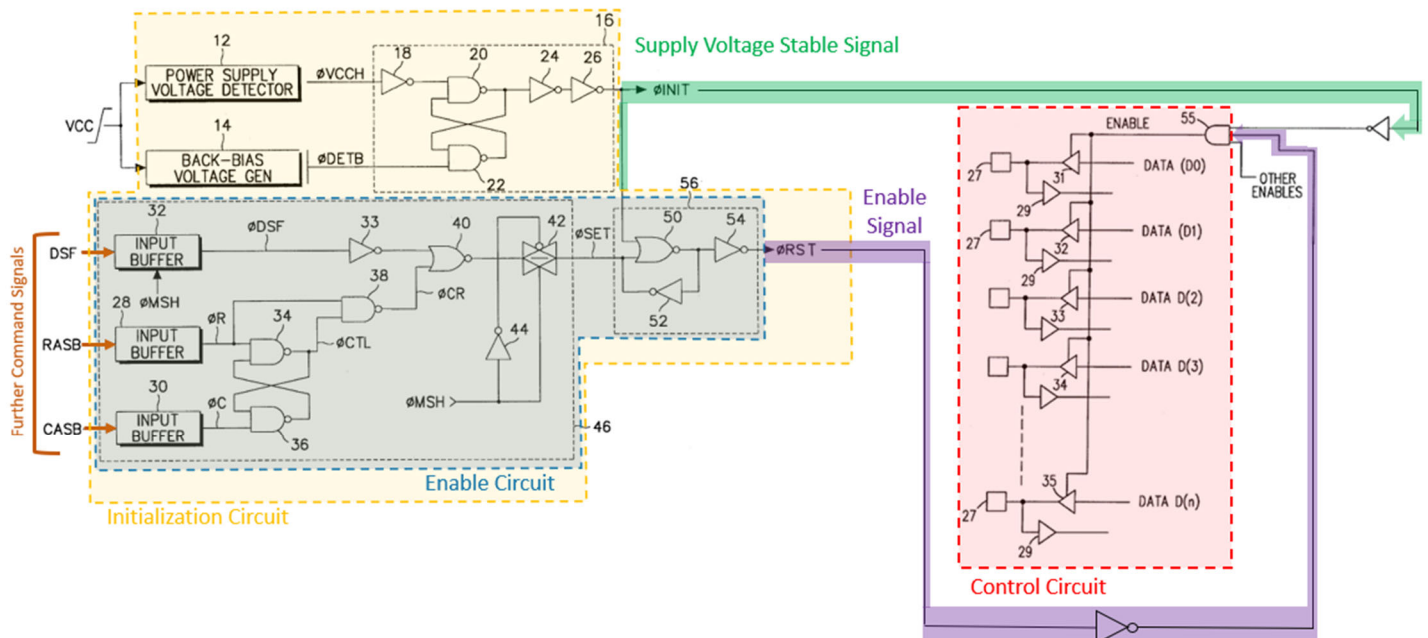
177. As previously described, Kocis provides output drivers that remain latched during the initialization and switching-on operation of the memory device and that are then unlatched upon the stabilization of power and the receipt of a proper initialization sequence of command signals. *See*, Section X.C, *supra*. Similarly, as described above, Lee also discloses that circuitry of a memory device remains latched until the stabilization of power and the receipt of a proper initialization sequence of command signals. *See*, Section XII.B.4, *supra*. However, Lee does not expressly disclose that the output buffers/drivers of the memory device are part of this circuitry that is unlatched upon initialization. A POSITA would have been motivated to use the reset signal output by the initialization circuit of Lee to unlatch the memory device's output buffers/drivers, as disclosed in Kocis, as one of the various circuitry that are disclosed in Lee as being unlatched in order to ensure the ability to "reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions," which is the stated goal of Lee (EX1005 at 2:18-20), and to

address “problems which may arise on a memory bus during system power-up” such as “preventing contention on the memory bus between conflicting data signals from two or more DRAM banks, which is the stated goal of Kocis (EX1004 at 1:11-15). This improvement constitutes the use of a known technique (*i.e.*, the output driver disabling feature of Kocis) to improve similar devices (*i.e.*, the memory devices, including DRAM disclosed in Lee) in the same way (*i.e.*, by applying the same initialization procedure disclosed in Lee to unlatch output drivers as in Kocis). Because of the similarities between the initialization procedures in both Lee and Kocis, a POSITA would have a reasonable expectation of success in combining the two references.

178. Furthermore, one of skill in the art would be motivated to combine the teachings of Lee with the teachings of Kocis at least because the two references are directed to solving the same problem (*i.e.*, ensuring proper initialization and power-up of a memory device in order to avoid malfunction). *See, e.g.*, EX1005 at 1:19-29, 2:4-23; EX1007 at 2:36-48, 2:60-64.

B. Claim [9]: The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit

179. Lee in combination with Kocis discloses a semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is



Kocis and Lee Combination

180. As shown in the annotated figure (above), a POSITA would have understood that disabling the output drivers until the enable conditions are met (*i.e.*, the proper initialization sequence has been performed) teaches latching the output drivers until the enable signal is generated by the enable circuit. The ϕ RST signal is driven low after a predetermined proper initialization sequence of the externally

applied further command signals (*i.e.*, Lee signals CASB, RASB, and DSF). “[I]f the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence, the first initialization signal generator activates the first initialization signal ϕ SET. For this to occur, the reset control signals DSF, RASB, and CASB must be activated in the CBR (CAS before RAS) mode. The mode selection clock signal ϕ DSF is first activated, *i.e.*, driven to a high-logic level. . . . If the first control signal CASB is then activated by being driven to a low logic state, . . . [t]hen, if the second control signal RASB is driven to the active low logic level, . . . the first initialization signal ϕ SET [is activated] at the output terminal of NOR gate 40. . . . The transfer unit 56 combines the first initialization signal ϕ SET and the second initialization signal ϕ INIT and activates the reset signal ϕ RST by driving it to a high logic level.” EX1005 at 4:38-61.

181. Once the reset signal ϕ RST is driven to a low logic level, it unlatches the control circuit. *See* EX1004 at 5:8-12 (“The output of the AND gate 55 (which comprises the ENABLE signal), only is driven high if all input signals are high. Thus, tri-state buffers 31, 32, 33, 34, 35 are only enabled if all three input signals are high.”); *id.* at 5:22-28 (“Until the voltage supply has reached the threshold value (which will vary from circuit to circuit depending upon the proper operating voltage and other considerations), the AND gate 55 keeps the ENABLE line low, disabling the tri-state buffers 31, 32, 33, 34, 35, thus preventing possible bus contention during

start-up or reset.”); *id.* at 2:3-8 (“When the buffer 13 is not enabled, the tri-state buffer 13 functions to ‘disconnect’ the data output line from the memory bus 11, so that neither a low or high signal is driven on the bus, and instead, the buffer presents a high impedance state thereby allowing other circuitry to determine the state of the bus.”).

182. Accordingly, Lee in combination with Kocis discloses a control circuit having output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

C. Claim [13]: The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit

183. For the same reasons discussed in Section XVI.B with respect to claim [9], Lee in combination with Kocis discloses the method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

XVII. Claims 9 and 13 are Obvious Over Lee in Combination with Iketani and Kocis

184. In my opinion, Lee in combination with Iketani and Kocis renders obvious claims 9 and 13 of the ’589 Patent, with Lee and Iketani rendering obvious

the limitations of independent Claims 1 and 11 from which they depend (*see* Sections XIII.C and XIII.D, *supra*).

A. Combination of Lee, Iketani, and Kocis

185. For the reasons discussed in Sections XIII.B and XVI.A, a POSITA would have been motivated to combine the teachings of Lee, Iketani, and Kocis.

B. Claim [9]: The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit

186. For the same reasons discussed in Section XVI.B with respect to claim [9], Lee in combination with Iketani and Kocis discloses the semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

C. Claim [13]: The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit

187. For the same reasons discussed in Section XVII.B with respect to claim [9], Lee in combination with Iketani and Kocis discloses the method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

I, Stephen W. Melvin, Ph.D., declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Dated: January 30, 2023



Stephen W. Melvin, Ph.D.

EDUCATION

Ph.D., Computer Science, University of California, Berkeley, May 1991.

Research Areas: High-performance computer architecture and microarchitecture (exploiting fine-grained parallelism in general purpose programs through a combination of hardware and software techniques); Microcode-based system performance analysis tools.

Minor Areas: Statistics, Computer Theory

B.S. (with high honors), Electrical Engineering and Computer Science, University of California, Berkeley, May 1982.

GENERAL WORK EXPERIENCE

April 2020 – Present, **Principal, Exponent, Inc.**

Advising industrial and legal clients on issues relating to intellectual property, including patent, copyright and trade secret litigation.

August 1983 – March 2020, **President, Zytek Communications Corporation**

Founded Zytek as an engineering, consulting and small-scale manufacturing company. Zytek provided consulting services related to intellectual property litigation and licensing, patent prosecution as well as services related to the design, implementation and testing of embedded systems. General areas of activity have also included source code analysis and comparison, forensic hard disk analysis and file recovery, industrial control and measurement, Internet related services and computer engineering research services.

January 2014 - December 2015, **President, Stage Innovations, Inc.**

Formed Stage Innovations to hold and develop patents in the area of Internet based voice messaging and fax and email notification. Prosecuted multiple patent applications to issuance and successfully negotiated a sale of the entire portfolio.

August 2002 – October 2005, **Patent Agent and Technical Advisor, O'Melveny & Myers LLP**

Assistance with a broad range of intellectual property cases, including patent, copyright and trade secret litigation, patent licensing and due diligence. Prior art research, patent validity and infringement analysis, source code comparison, forensic hard disk analysis. Preparation and prosecution of patents in different areas of technology.

May 2001 – August 2002, **Founder and Chief Architect, FlowStorm, Inc. (later ConSentry Networks)**

Defined and guided the overall chip architecture for a new packet processor. Managed a group of RTL designers to develop working RTL code for the processing core, packet management and interconnect blocks. Developed verification strategy and worked with performance analysis and software groups.

March 2000 - May 2001, **Senior Architect, Clearwater Networks (formerly XStream Logic, Inc.)**

Helped define the architecture and microarchitecture of the XStream network processor. Worked with a team of design engineers to evaluate tradeoffs in microarchitecture, directed design choices to balance tradeoffs in performance and cost. Documented the architecture and worked with software engineers to analyze performance and develop software.

July 1999 – July 2002, **Consulting Engineer, Adroit Engineering, Inc.**

Development of hardware and firmware for optical headlight alignment system for Ford Motor Company. Analog and digital circuit design, firmware engineering, calibration and testing.

September 1998 - December 1998, 1991-1995 **Consulting Engineer, HaL Computer Systems, Inc.**

Analysis and testing of cycle by cycle simulator of new SPARC based microprocessor. Validation of results and comparison with microarchitecture definition. Assisted in advanced microarchitecture research on a new implementation of the SPARC architecture, including performance modeling and simulation. Maintenance and enhancement of microarchitecture level and architecture level simulation tools.

June 1986 - December 1987, **Consulting Engineer, Digital Equipment Corporation**

Consulting for the High-Performance Advanced Development Group in Marlboro on VAX 8600 microcode and the application of out-of-order execution concepts to the VAX architecture. Development of special purpose VAX 8600 microcode and porting and improvement of an HPS/VAX microarchitectural simulator.

June 1984 - September 1984, **Engineer, Denelcor Corporation**

Investigation of the design of architecture to follow the HEP-1 and HEP-2 under the supervision of Dr. Burton Smith. Development of a new architecture, Vulture, allowing higher function unit utilization and incorporating a new method of scheduling register reads and writes in a multiprogrammed pipelined system.

INTELLECTUAL PROPERTY CONSULTING EXPERIENCE

September 2018 – September 2019, **Testifying Expert, F. Tabaian and A. Ashrafzadeh v. Intel Corp. (OR)**

Analysis of patents, analysis of source code related to voltage regulation technology.

August 2017 – October 2017, **Testifying Expert, Tripwire, Inc. v. UpGuard, Inc. (OR)**

Analysis of patents, analysis of source code related to security software.

December 2017 – January 2018, **Testifying Expert, NFL Enterprises LLC v. OpenTV, Inc. (USPTO)**

Analysis of patents and prior art related to media streaming and content distribution, declaration for IPR.

November 2015 – May 2016, **Testifying Expert, OpenTV, Inc., NagraVision SA and Nagra France S.A.S. v. Apple, Inc. (NDCAL, USPTO)**

Analysis of patents and prior art related to media streaming and content distribution, declaration for IPR.

December 2014 – January 2015, **Testifying Expert, Amazon, Inc. v. c4cast.com, Inc. (USPTO)**

Analysis of patents and prior art related to content distribution, declaration for IPR.

February 2012 – December 2017, **Testifying Expert / Consulting Expert, Mentor Graphics Corporation v. EVE-USA, Inc., Emulation and Verification Engineering, S.A., Synopsys, Inc. (OR, CAND, Japan)**

Analysis of patents, prior art and software and firmware technology related to electronic design automation. Declarations for Japan litigation.

August 2010 – March 2014, **Testifying Expert, The Quantum World Corporation v. Dell Inc. et al. (TXWD)**

Analysis of patents and prior art relating to true random number generators. Statistical analysis of random data sets.

February 2011 – April 2012, **Testifying Expert, Pact XPP Technologies, AG v. Xilinx, Inc. (TXED)**

Analysis of patents, prior art and technology related to programmable logic devices.

April 2011 – May 2011, **Testifying Expert, Microsoft Corporation v. Phoenix Solutions, Inc. (CACD)**

Analysis of technology related to speech processing and voice recognition.

January 2010 – June 2010, **Testifying Expert, Optimum Processing Solutions, v. AMD et al. (GAND)**

Analysis of patent relating to optically interconnected processing elements. Testimony regarding claim construction.

May 2009 – October 2009, **Testifying Expert, Saxon Innovations v. Samsung Electronics (ITC)**

Analysis of patents and prior art relating to interprocessor communication and interrupt masking. Review of source code for cellphones. Testimony at ITC hearing.

January 2008 – March 2009, **Testifying Expert, Quantum World Corporation v. Atmel Corp., et al. (TXED)**

Analysis of patents and prior art relating to true random number generators. Statistical analysis of random data sets.

March 2007 – August 2008, **Testifying Expert, Silicon Image Inc. v. Analogix Semiconductor, Inc. (CAND)**

Analysis of data sheets, product specifications and firmware related to HDMI digital television interface and devices for receiving and processing digital video data.

July 2001 – October 2001, **Testifying Expert, Intel v. Via Technologies**

Analysis of patents, AGP specifications, and other documents related to CPU/memory systems and architectures.

October 1999 - May 2000, **Testifying Expert, Accton v. Micro Linear Corporation**

July 1999 - September 1999, **Testifying Expert, Allied Telesyn v. Micro Linear Corporation**

Analysis of on-chip circuitry, testing procedures and data sheets for Ethernet controller ICs. Analysis of the application of Ethernet controller ICs in hubs and switches, design and testing. Compliance with data sheet and other published specifications.

August 1998 - December 1998, **Court Appointed Expert, Cadence v. Avant!**

Assisting Northern California Federal District Court Judge Ronald Whyte in understanding issues and technology relating to CAD design software and its alleged copyright infringement and trade secret misappropriation; source code analysis and comparison.

June 1998 - December 1998, **Testifying Expert, Canter, et. al. v. West Publishing**

Analysis of source code, proposals, internal documentation and other materials relating to natural language processing of database queries in connection with patent and trade secret misappropriation case.

June 1998 – December 1998, **Testifying Expert, Xircom v. General Patent**

Analysis of patents and other references relating to modem and packaging technology.

May 1998 – August 1999, **Testifying Expert, Hilgraeve v. Symantec**

December 1997 - February 1998, **Consulting Expert, Trend v. Symantec**

Analysis of source code, patents and other references relating to virus checking software. Analysis and operation of virus checking software and development operational tests.

May 1995 - May 1997, **Testifying Expert, DSC v. DGI**

Analysis and comparison of firm ware for a microprocessor-based telecommunications board relating to copyright issues. Testimony regarding source code analysis and concepts and practices in reverse engineering.

March 1996 - November 1996, **Testifying Expert, AMD v. Hyundai**

Analysis of flash EEPROM integrated circuits including analysis of internal circuitry, analysis of product development data and comparison of testing procedures in a trade secret case.

October 1996 - November 1996, **Testifying Expert, Texas Instruments v. Samsung**

Analysis of firm ware (ladder logic) for programmable controllers used in assembly lines in a patent infringement case.

December 1992 - July 1993, **Testifying Expert, Conner v. Western Digital**

August 1994 to December 1995, **Testifying Expert, IBM v. Conner**

Analysis of the architecture of hard disk drives, including microcontroller firm ware analysis, digital and analog circuit analysis, and dynamic testing. Analysis of patents and other references.

TEACHING AND ACADEMIC EXPERIENCE

December 2011 - December 2012, **General Chair, 45th Annual Symposium in Microarchitecture (MICRO-45)**

Set up and managed academic conference held in Vancouver, British Columbia in December 2012.

September 2001 – April 2002, **Visiting Scholar, University of Texas, Austin**

Monthly visit to lead discussions and direct graduate students in research into high performance computer architecture.

December 1995 - December 1996, **Co-Chair, 29th Annual Symposium in Microarchitecture (MICRO-29)**

Set up and managed academic conference held in Paris, France in December 1996.

PUBLICATIONS

Patt, Y., Hwu, W., Melvin, S., and Shebanow, M., "HPS Papers: A Retrospective," IEEE Micro July/August 2016, vol. 36, no. 4, pp. 76-79.

Melvin, S., "Endpoint Identification Using System Logs", Workshop on the Analysis of System Logs (WASL) 2009, held in conjunction with the 22nd ACM Symposium on Operating System Principles (SOSP), Big Sky, Montana, October 2009.

Melvin, S., Nemirovsky, M., Musoll, E., Huynh, J., Milito, R., Urdaneta, H., and Saraf, K., "A Massively Multithreaded Packet Processor," *NP2: Workshop on Network Processors, held in conjunction with The 9th International Symposium on High-Performance Computer Architecture (HPCA-9)*, Anaheim, California, February 8-9, 2003.

Melvin, S. and Patt, Y., "Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors," *Proceedings, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems*, October 8 – 11, 2002.

Melvin, S., and Patt, Y., "Enhancing Instruction Scheduling with a Block-Structured ISA," *International Journal of Parallel Processing*, 23(3):221-243, 1995.

Melvin, S., and Patt, Y., "Exploiting Fine-grained Parallelism Through a Combination of Hardware and Software Techniques," *Proceedings, 18th International Symposium on Computer Architecture*, Toronto, Canada, May 1991.

Melvin, S., and Patt, Y., "Performance Benefits of Large Execution Atomic Units in Dynamically Scheduled Machines," *Proceedings, 1989 Supercomputer Conference*, Crete, Greece, June 1989.

Melvin, S., Shebanow, M., and Patt, Y., "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines," *Proceedings, 21st Annual Workshop on Microprogramming and Microarchitecture*, San Diego, California, November 1988.

Melvin, S., and Patt, Y., "The Use of Microcode Instrumentation for Development, Debugging and Tuning of Operating System Kernels," *Proceedings, 1988 ACM SIGMETRICS*, Santa Fe, New Mexico, May 1988.

Melvin, S., and Patt, Y., "A Clarification of the Dynamic/Static Interface," *Proceedings, 20th Hawaii International Conference on System Sciences*, Kailua-Kona, Hawaii, January 1987.

Gee, J., Melvin, S., and Patt, Y., "Advantages of Implementing Prolog by Microprogramming a General Purpose Host Computer," *Proceedings, Fourth International Conference on Logic Programming*, Melbourne, Australia, May 1987.

Melvin, S., and Patt, Y., "SPAM: A Microcode Based Tool for Tracing Operating System Events," *Proceedings, 20th Annual Workshop on Microprogramming*, Colorado Springs, Colorado, December 1987.

Melvin, S., Wilson, J., Shebanow, M., Hwu, W. and Patt, Y., "On Tuning the Microarchitecture of an HPS Implementation of the VAX," *Proceedings, 20th Annual Workshop on Microprogramming*, Colorado Springs, Colorado, December 1987.

Melvin, S., and Patt, Y., "A Microcode-Based Environment for Non-invasive Performance Analysis," *Proceedings, 19th Annual International Workshop on Microprogramming*, New York, October 1986.

Gee, J., Melvin, S., and Patt, Y., "The Implementation of Prolog via VAX 8600 Microcode," *Proceedings, 19th Annual Workshop on Microprogramming*, New York, October 1986.

Patt, Y., Melvin, S., Hwu, W., Shebanow, M., Chien, C., and Wei, J., "Run-Time Generation of HPS Microinstructions from a VAX Instruction Stream," *Proceedings, 19th Annual Workshop on Microprogramming*, New York, October 1986.

Patt, Y., Hwu, W., Melvin, S., Shebanow, M., Chien, C., and Wei, J., "An HPS Implementation of VAX: Initial Design and Analysis," *Proceedings, 19th Hawaii International Conference on System Sciences*, Honolulu, Hawaii, January 1986.

Patt, Y., Shebanow, M., Hwu, W., and Melvin, S., "A C Compiler for HPS I, A Highly Parallel Execution Engine," *Proceedings, 19th Hawaii International Conference on System Sciences*, Honolulu, Hawaii, January 1986.

Patt, Y., Melvin, S., Hwu, W., and Shebanow, M., "Critical Issues Regarding HPS, A High Performance Microarchitecture," *Proceedings, 18th Annual Workshop on Microprogramming*, Asilomar, California, December 1985.

OTHER

USPTO Registered Patent Agent

Named Inventor on 49 U.S. Patents

Professional Association Memberships:

The Institute of Electrical and Electronics Engineers (IEEE)

The Association for Computing Machinery (ACM)