

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,157,589

Case No. IPR2023-00516

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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Alexandria, VA 22313-1450

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent No. 6,157,589 (the “’589 Patent”)
1002	U.S. Prosecution History of the ’589 Patent
1003	Declaration of Stephen W. Melvin
1004	U.S. Patent No. 5,559,753 to Kocis entitled “Apparatus and Method for Preventing Bus Contention During Power-Up in a Computer System With Two or More DRAM Banks” (“Kocis”)
1005	U.S. Patent No. 5,774,402 to Lee entitled “Initialization Circuit for a Semiconductor Memory Device” (“Lee”)
1006	JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Compilation of Releases 1 through 7, dated January 1997 (“JESD 21-C”)
1007	U.S. Patent No. 5,703,510 to Iketani et al. entitled “Power On Reset Circuit For Generating Reset Signal at Power On” (“Iketani”)
1008	Prosecution History of EPO Patent Application No. 99 113 048.5 (Original)
1009	Excerpt of Prosecution History of EPO Patent Application No. 99 113 048.5 (Original)
1010	Excerpt of Prosecution History of EPO Patent Application No. 99 113 048.5 (English Translation)
1011	Japanese Patent Publication No. JP 09 106668 A to Samsung Electronics Co. Ltd. dated April 22, 1997 (“Tetsuka”)
1012	Declaration of Julie Carson
1013	JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Release 7, dated January 1997

Exhibit	Description
1014	Scheduling Order, <i>Polaris Innovations Limited v. Xilinx, Inc.</i> , 1:22-cv-00174-RGA, Docket No. 20 (May 31, 2022)
1015	United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf
1016	Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)
1017	Excerpt of Micron Technology, Inc., “DRAM Data Book” (1992)
1018	Excerpt of Samsung Electronics Co., Ltd., “Data Book: DRAM” (Dec. 1995)
1019	Samsung Electronics, “4M x 8Bit x 4 Banks Synchronous DRAM” Doc. No. KM48S16030, Rev. 2 (March 1998)

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.P]	A dynamic semiconductor memory device of a random access type, comprising:
[1.1]	an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation,
[1.2]	said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals,
[1.3]	said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.
Claim 2	
[2]	The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.
Claim 8	
[8]	The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

Claim 9	
[9]	The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.
Claim 10	
[10]	The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal.
Claim 11	
[11.P]	An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:
[11.1]	supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

[11.2]	supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.
Claim 12	
[12]	The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.
Claim 13	
[13]	The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

I. INTRODUCTION

Xilinx, Inc. petitions for *Inter Partes* Review (“IPR”) of claims 1, 2, and 8-13 of U.S. Patent 6,157,589 (the “’589 Patent”).

II. MANDATORY NOTICES (37 C.F.R. §42.8)

A. Real Parties-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Xilinx, Inc. (“Xilinx” or “Petitioner”), Advanced Micro Devices, Inc. (“AMD”), and ATI Technologies ULC (“ATI”) are the real parties-in-interest. AMD is the parent of Xilinx and ATI is an indirect, wholly owned subsidiary of AMD.

B. Related Matters (37 C.F.R. §42.8(b)(2))

Polaris asserted four patents, including the ’589 Patent, against Xilinx in *Polaris Innovations Ltd. v. Xilinx, Inc.*, CA 1:22-CV-00174-RGA (D. Del.), in a complaint filed on February 8, 2022 and served on February 22, 2022. Xilinx is concurrently filing this Petition and IPR petitions for the other three asserted patents: IPR2023-00513, IPR2023-00514, and IPR2023-00517.

Kingston Technology Company, Inc. (“Kingston”), previously petitioned for *inter partes* review of claims 11 and 12 of the ’589 Patent on November 10, 2016, and the Patent Trial and Appeal Board (“Board”) denied Kingston’s petition. *Kingston Tech. Co., Inc. v. Polaris Innovations Ltd.*, IPR2017-00238, Paper 9

(PTAB May 2, 2017). Kingston based its petition on different grounds and prior art than those described herein.

C. Lead and Back-Up Counsel (37 C.F.R. §42.8(b)(3))

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence to the address above. Petitioner consents to electronic service by email at xilinxMWETeam@mwe.com.

III. PAYMENT OF FEES (37 C.F.R. §42.103)

Petitioner authorizes the Office to charge Deposit Account No. 50-0417 for the petition fee set in 37 C.F.R. §42.15(a) and for any other required fees.

IV. REQUIREMENTS FOR IPR (37 C.F.R. §42.104)

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the '589 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR.

B. Challenge Under 37 C.F.R. §42.104(b) and Relief Requested

Petitioner requests IPR of claims 1, 2, and 8-13 of the '589 Patent on the grounds listed below. In support, this petition includes a declaration of Dr. Stephen Melvin (EX1003).

Ground	Claims	Basis for Rejection
1	1, 9, 11, 13	§102: Kocis
2	2, 8, 10, 12	§103: Kocis in combination with JESD 21-C
3A/3B	1, 11	§102/§103: Lee
4	1, 11	§103: Lee in combination with Iketani
5	2, 8, 10, 12	§103: Lee in combination with JESD 21-C
6	2, 8, 10, 12	§103: Lee in combination with Iketani and JESD 21-C
7	9, 13	§103: Lee in combination with Kocis
8	9, 13	§103: Lee in combination with Iketani and Kocis

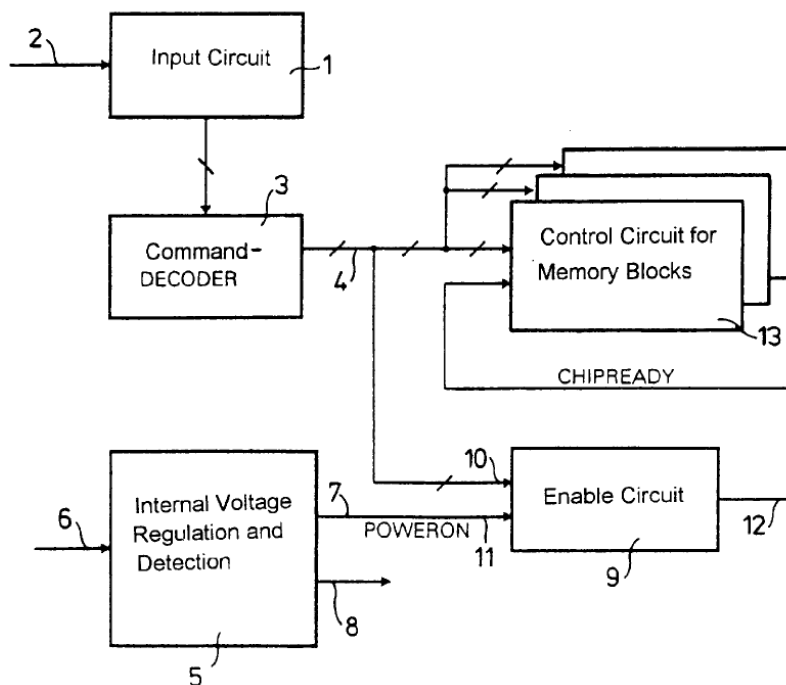
V. SUMMARY OF THE '589 PATENT

A. Brief Description

The '589 Patent is directed to a Dynamic Semiconductor Random Access Memory ("DRAM") device and a method for initializing a DRAM device. EX1001 at 2:7-14. The device and method purportedly solve a problem in the prior art by providing a way for circuits to be "reliably held in a desired defined state" while the device is powering on. *Id.* at 1:22-35. This purported advancement is achieved by detecting a particular initialization sequence. *Id.* To detect the initialization sequence, the device contains an initialization circuit having a control circuit and an enable circuit. *Id.* at 2:15-36.

As seen in FIG. 1 of the '589 Patent (reproduced below), once the initialization circuit performs a switching-on operation and the internal voltage regulation and detection circuit 5 detects that the supply voltage at input 6 is stabilized, detection circuit 5 supplies a supply voltage stable signal (POWERON) to the enable circuit 9. *Id.* at 3:42-4:23.

Fig 1



EX1001 ('589 Patent) at FIG. 1

The enable circuit 9 receives the supply voltage stable signal (POWERON) at input 11 and various command signals at input 10. *Id.* Once the enable circuit receives the supply voltage stable (POWERON) signal and the various command signals in a specific sequence, it outputs an enable signal (CHIPREADY) at output 12 which then unlatches the control circuit 13. *Id.*

FIG. 2 of the '589 Patent (reproduced below for reference), illustrates an example of enable circuit 9 in more detail.

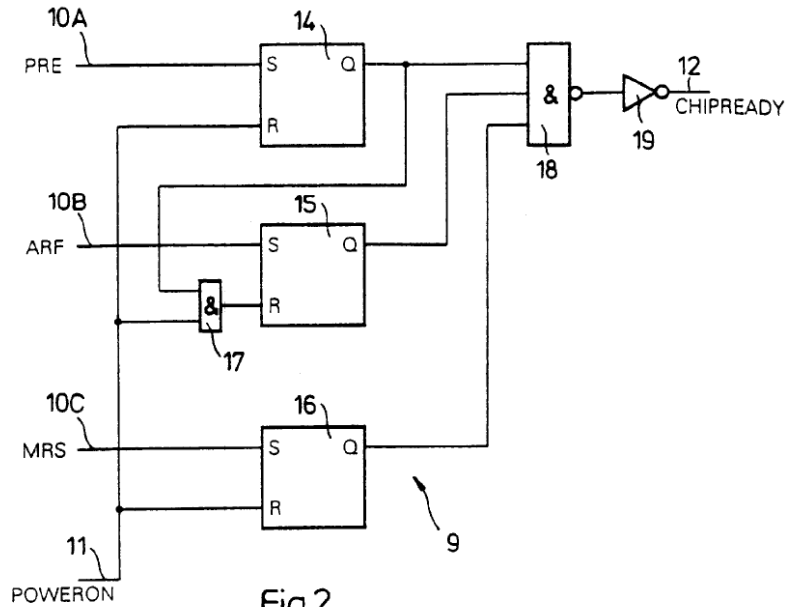


Fig 2
EX1001 ('589 Patent) at FIG. 2

It contains “three bistable multivibrator stages 14, 15 and 16 each having a set input S, a reset input R, and also an output Q.” *Id.* at 4:24-58. The supply voltage stable signal (POWERON), described above, is applied to the enable circuit at input 11. *Id.* Additionally, the command signals described above at input 10 are shown in more detail. *Id.* Input 10A receives a preparation command for word line activation, called PRE or PRECHARGE. *Id.* Input 10B receives a refresh command, called ARF or AUTOREFRESH. *Id.* Input 10C receives a loading configuration register command, called MRS or MODE-REGISTER-SET. *Id.* The enable signal (CHIPREADY) is output at output 12 after “a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the [supply voltage steady] POWERON signal.” *Id.*

B. Summary of the Prosecution

1. EPO

U.S. Patent Application No. 09/343,431, which issued as the '589 Patent, claims priority to a German Patent publication filed on June 30, 1998. *See* EX1001 at [30]. Original EPO claim 1 has nearly identical scope and subject matter to granted US claim 1:

Original EPO Claim 1	Granted US Claim 1
A dynamic semiconductor memory device of a random-access type (DRAM/SDRAM) having an initialization circuit which controls the switching-on operation of the semiconductor memory device and of its circuit components and which supplies a supply voltage stable signal (POWERON) once the supply voltage has been stabilized after the switching-on of the semiconductor memory device, characterized in that the initialization circuit has an enable circuit (9) that receives the supply voltage stable signal (POWERON) and further command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device which enable circuit supplies an enable signal (CHIPREADY) after the recognition of a predetermined proper initialization sequence of the command signals (PRE, ARF, MRS) applied to the semiconductor memory device which enable signal causes the unlatching of a control circuit (13)	A dynamic semiconductor memory device of a random access type, comprising: an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

Original EPO Claim 1	Granted US Claim 1
provided for the proper operation of the semiconductor memory device.	

EX1010 at 12; EX1001 at claim 1.

During prosecution, the EPO rejected claim 1 based on Japanese Patent Publication No. JP09106668A dated April 22, 1997 (“Tetsuka,” attached as EX1011). EX1010 at 7-9. Tetsuka is the Japanese counterpart to U.S. Patent No. 5,774,402 to Lee (“Lee”), which forms the basis for the invalidity Grounds 3-8 discussed herein. *Compare* EX1011 at Cover, (31) *with* EX1005 at Cover, [30] (each claiming priority to Korean Patent Publication 26181/1995); *see also* EX1008 at 67 (indicating that Lee is a “Member of the Patent Family” of Tetsuka). In response to this rejection, the applicant amended claim 1 to incorporate the subject matter of dependent claim 2, which ultimately led to allowance. EX1010 at 1, 5. Original EPO claim 2, the subject matter of which was required to obtain allowance, has nearly identical scope and subject matter to granted US claim 2:

Original EPO Claim 2	Granted US Claim 2
A semiconductor memory device according to Claim 1, characterized in that the command signals (PRE, ARF, MRS) externally applied to the semiconductor memory device in the initialization sequence recognized by the enable circuit (9) comprise the preparation command for word line activation (PRE-CHARGE), and/or the refresh command (AUTOREFRESH), and/or the load	The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

Original EPO Claim 2	Granted US Claim 2
configuration register command (MODE-REGISTER-SET).	

EX1010 at 12; EX1001 at claim 2.

In submitting the claim amendments identified above, the applicant did not argue that the Examiner's rejections based on Tetsuka were improper or incorrect.

See EX1010 at 12.

2. USPTO

U.S. Patent Application No. 09/343,431, which issued as the '589 Patent, was filed on June 30, 1999 with a claim of priority to the German patent application dated June 30, 1998 referenced above (EX1002 at 31).

As discussed above, during EPO prosecution, the applicant amended original EPO claim 1 to incorporate the subject matter of original EPO claim 2 in order to gain allowance. The claims filed in front of the USPTO had the same subject matter as the original EPO claims (*i.e.*, original US claim 1 had the same subject matter as original EPO claim 1, without the additional limitations of original EPO claim 2 that was eventually added into the EPO claim 1 to obtain allowance).

Compare EX1002 at 20 *with* EX1010 at 12. Despite knowledge that Lee was an English language family member of Tetsuka, as reported in the European Search Report (EX1008 at 67), the applicant cited only Tetsuka, without a separate English translation, to the USPTO. The applicant did not disclose the European Search Report or the Lee reference to the USPTO. Subsequently, the U.S.

Examiner allowed the claims without any rejections and without any amendment to claim 1, contrary to the amendment made to obtain allowance in the EPO. EX1002 at 100-01.

As is detailed below in the grounds of unpatentability, the EPO examiner was correct to not allow claim 1 of the EPO patent, and the US examiner should also not have allowed the similar US claim 1. The EPO examiner correctly determined that Tetsuka anticipated EPO claim 1, and the same is true of the anticipation of US claim 1 by Lee, which has the same content as Tetsuka. The Grounds below include Lee, and an additional reference, Kocis, that was not before either examiner.

C. Applicant Admitted Prior Art in the Background of the '589 Patent

The admitted prior art in the background section of the '589 Patent further confirms that the subject matter of the challenged claims, including the dependent claims, is not patentable. EX1003, ¶38. For example, the background explains:

In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal Supply Voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

EX1001 at 1:65-2:5. The Kocis, Lee and Iketani references used in the Grounds of this Petition confirm that this concept of initializing the memory circuits only after there is a stable voltage was in the prior art.

Furthermore, the background of the '589 Patent goes on to describe all the details of the initialization sequence recited in the challenged independent and dependent claims:

According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called "POWERON-SEQUENCE") is provided as follows:

- a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component;
- b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us;
- c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device;
4. the activation of eight or more refresh commands (AUTOREFRESH); and
5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.

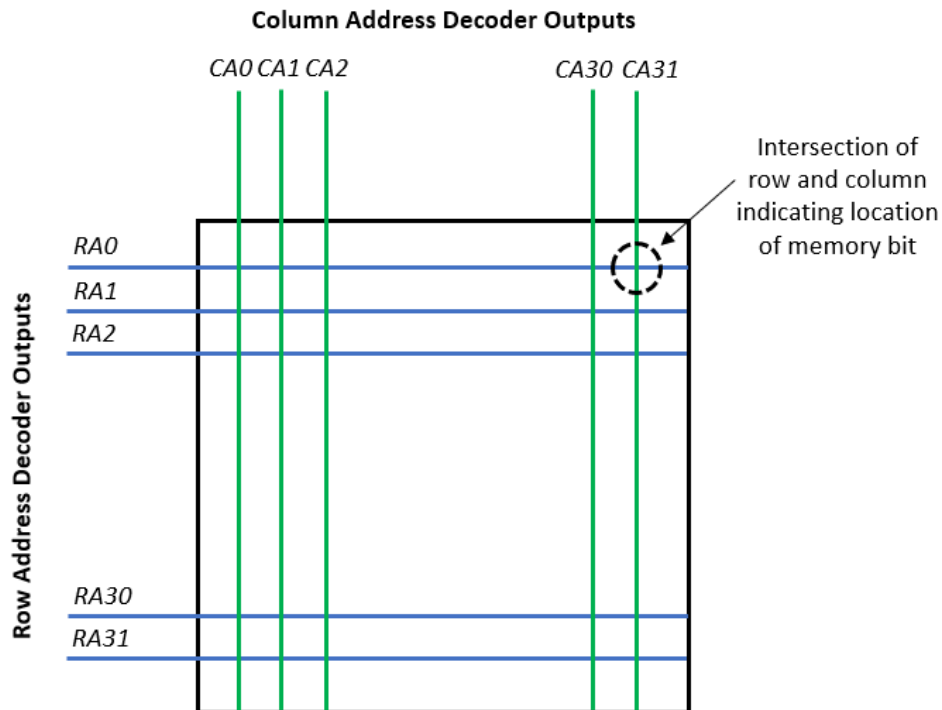
EX1001 at 1:43-61. The Kocis, Lee and JESD 21-C references used in the Grounds of this Petition confirm that this concept of not initializing the memory circuits until there is a predetermined initialization sequence of command signals was in the prior art—the exact same sequence of commands disclosed in the '589 Patent

background and recited in the challenged dependent claims was disclosed in JESD 21-C.

VI. TECHNOLOGY OVERVIEW

The technology of the '589 Patent generally relates to semiconductor memory devices, also referred to as random access memory ("RAM"). As of the filing date of the '589 Patent, there were multiple types of RAM available. Such variants include Dynamic RAM ("DRAM") and Synchronous Dynamic RAM ("SDRAM"). EX1003, ¶47.

DRAM chips contain one or more memory arrays, which are rectangular grids of storage cells, organized into rows and columns, each cell holding one bit of data. A depiction of a DRAM chip's memory array with the rows and columns is reproduced below. EX1003, ¶¶48-49.

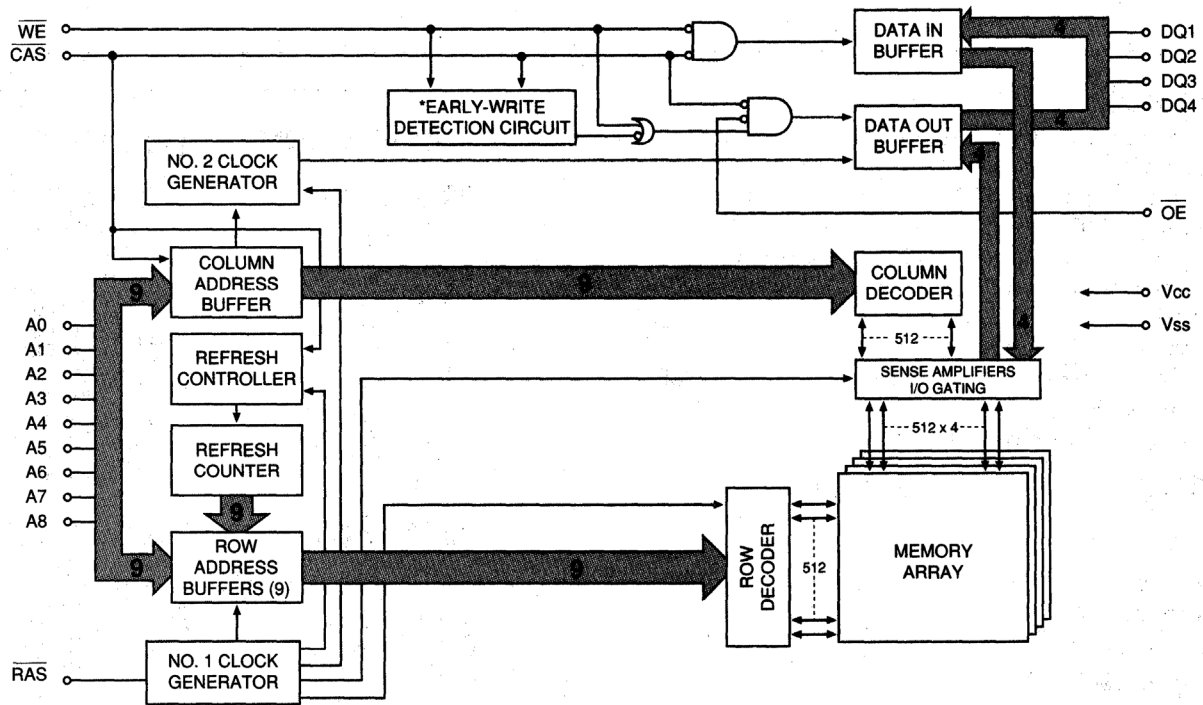


DRAM is characterized as “dynamic” because the values held in the memory array’s storage cells are represented by electric charges that slowly leak out of the circuit over time. In order to maintain the data stored in dynamic memory cells, they must be periodically “refreshed” by reading the cell’s value and restoring its charge. Another aspect of dynamic memory is that before a read operation can be performed, a “precharge” operation is necessary. This affects the timing of how reads and writes are processed in a dynamic memory device. EX1003, ¶¶50-51.

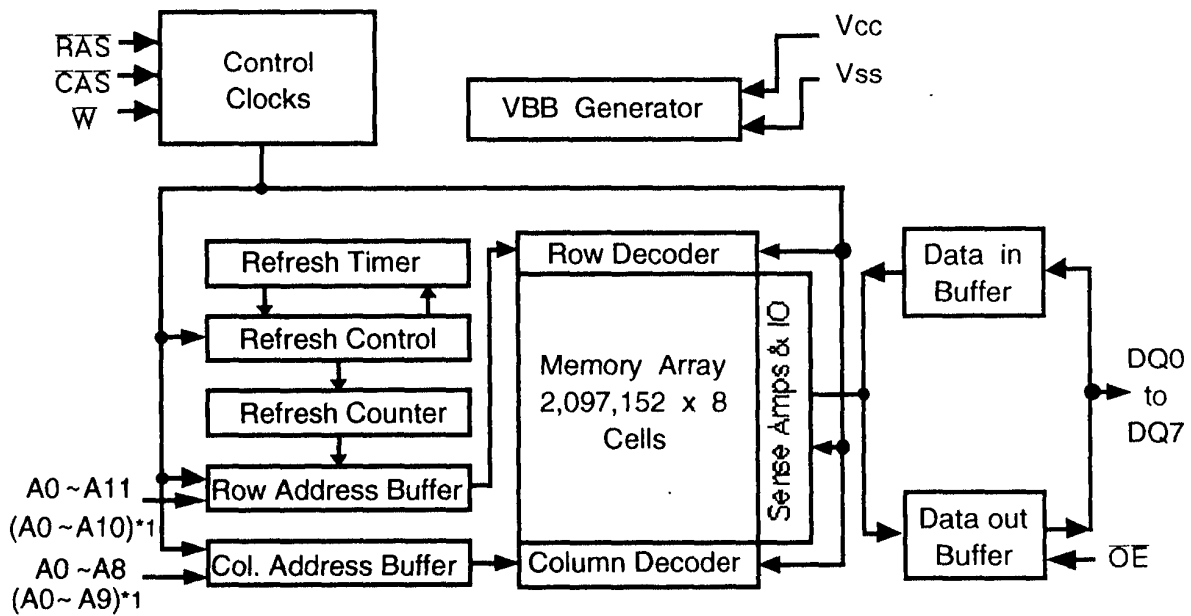
In typical systems involving DRAM devices, there is a dedicated address bus that carries row and column addresses to the DRAMs and a dedicated data bus that communicates read and write data between the CPU and the DRAMs. Control

signals comprise the row and column strobes, output enables, clocks, clock enables, chip enables and other related signals. These signals are typically controlled by a memory controller, that is either integrated with or separate from the CPU, and connect to every DRAM in the system. EX1003, ¶52.

Input signals labeled “CAS” and “RAS” (or sometimes “CASB” and “RASB,” in which the “B” refers to “bar” which means that the signals are low active) are specific to DRAM type devices. Column Address Strobe (CAS) and Row Address Strobe (RAS) signals have to do with the multiplexing of column and row lines on the same address pins. Additional control signals include, for example, Chip Select (CS), which enables the memory chip’s command decoder, and Write Enable (WE), which determines whether an operation is a read or a write. Additionally, DRAM may have special function signals, such as DSF, which enables certain special operational functions when active. These various input signals are used to perform specific commands by way of a command decoder within the DRAM device, which accepts the various signals and interprets the sequence as a particular command. Depending on the combination of these input signals sent from the memory controller to the DRAM device, a different command is identified and performed. For reference, a functional block diagram of a 1992 Micron DRAM device is provided below (EX1017 at 1-88). EX1003, ¶53.



Similarly, a functional block diagram of a 1996 Samsung DRAM device is provided below (EX1018 at 217).



Similar to the prior art used in the grounds below, both of these DRAM devices required a power-on sequence that utilized a initialization sequence of control signals. *See* EX1017 at 1-79; EX1018 at 224 n.1.

The original DRAM devices were asynchronous, meaning that they did not rely on an external clock signal. Subsequently, synchronous DRAM devices (SDRAMs) were introduced in which an external clock signal is supplied by the memory controller and signals are sampled based on the clock signal. The primary benefit of SDRAM is that it allows faster operation due to increased predictability of event timing. Despite some changes to control signal nomenclature and other functionality specific to the use of external clock signals, the underlying architecture of SDRAM is essentially the same as asynchronous DRAM. EX1003, ¶54.

VII. OVERVIEW OF THE PRIOR ART USED IN THE GROUNDS

A. Kocis (EX1004)

Kocis was filed on January 25, 1995 and was issued on September 24, 1996. EX1004 at [22], [45]. Kocis discloses a DRAM circuit with circuitry for disabling data output drivers to prevent bus contention during system power-up. EX1004 at Abst. The circuitry disclosed in Kocis includes a counter for counting a initialization sequence of RAS signals and a circuit for detecting that a supply voltage has achieved a proper voltage threshold. EX1004 at Abst. The circuitry in

Kocis disables output drivers and an associated control circuit until a certain number of RAS signals are received and the supply voltage has met the necessary threshold. EX1004 at Abst.

Kocis qualifies as prior art under at least §§102(a), (b), and (e) because it was filed, published, and issued before the earliest possible priority date (June 30 1998, hereinafter the “Priority Date”) of the ’589 patent.

B. Lee (EX1005)

Lee was filed on August 23, 1996 and claims priority to Korean Document No. 26181/1995 dated August 23, 1995. EX1005 at [22], [30]. Lee explains that as semiconductor memory devices become more complicated, they require initialization circuits for resetting the various functional circuits within the chip. EX1005 at 1:18-27. Traditionally, power-on reset circuits were provided to ensure stable power sources. *Id.* As with Kocis, Lee takes this one step further and seeks to additionally provide an initialization circuit for semiconductor memory that is based on external logic signals. EX1005 at 2:21-23.

In particular, Lee describes an initialization circuit for a semiconductor memory device which includes an initialization signal generator that generates an initialization signal in response to a specific sequence of reset control signals. EX1005 at Abst. The initialization signal is activated when three reset control

signals are activated in the proper sequence and is deactivated when one of the control signals is deactivated. *Id.*

Lee contains both a first and second initialization signal generator. The first initialization circuit generator is triggered based on the correct sequence of control signals DSF, RASB, and CASB. EX1005 at 3:9-22. The second initialization circuit generator is triggered based on proper powerup of the power source. *Id.* The resulting initialization signals are then sent to Lee's transfer unit which, based on the initialization signals, generates a reset signal ϕ RST sent "to a circuit to be initialized within the chip." EX1005 at 4:14-24, 4:59-5:4.

Lee qualifies as prior art under at least §102(e) because it was filed before the Priority Date of the '589 Patent (and then subsequently was issued as a granted patent).

C. JESD 21-C (EX1006)

JESD 21-C is a "Memory Device Standard" for "establish[ing] pin assignments, power supply potentials, and package configurations and dimensions for a series of memory devices." EX1006 at page 3-1. Furthermore, "In some cases, special timing diagrams are included, where they are essential to the implementation and use of the standards." *Id.* In particular, JESD 21-C discloses the exact initialization sequence of control signals for power-up that is recited in the claims.

The JESD 21-C Standard is and was a well-known industry standard compiled and published by the Joint Electron Device Engineering Council (“JEDEC”). EX1003, ¶¶91-93 (explaining that a POSITA would have been well-aware of JEDEC memory standards like JESD 21-C and would have been aware of how to access those standards, what they disclose, and how to design a memory device according to the standards); *see also, e.g., Samsung Elecs. Am., Inc. v. Goodman*, IPR2017-02021, Paper 19 at 18-19 (PTAB Oct. 29, 2019) (finding that JEDEC’s JESD 21-C is a printed publication available in January 1997, which is listed on the face of the standard); *SK hynix Inc. v. Netlist, Inc.*, IPR2017-00577, Paper 26 at 6 (PTAB July 5, 2018) (holding that another JEDEC standard was publicly available). The standard “contain[s] material that has been prepared, progressively reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.” EX1006 at Copyright Notice. The purpose of the standard is to “serve the public interest through eliminating misunderstandings between manufacturers and purchase[r]s, facilitating interchangeability and improvement of products, and assisting the purchaser [in] selecting and obtaining with minimum delay the proper product for his particular need.” *Id.*

As already held in IPR2017-02021, cited above, JESD 21-C Release 7 was published in January 1997. *See also* EX1006 at Title. As further support of this

public availability, Petitioner relies upon the Declaration of Julie Carson of JEDEC. *See* EX1012. Ms. Carson states that JEDEC specification JESD 21-C “was made publicly available in January 1997.” EX1012, ¶14. In particular, Ms. Carson testifies that in January 1997 copies of JESD 21-C would have been available for purchase by anyone in the public and that pages comprising the specifically updated modules would have been sent to those who subscribed to the annual updating service for JESD 21-C. *Id.* ¶¶10-15. JESD 21-C qualifies as prior art under at least §102(a) and (b) because it was published before the Priority Date and over a year before the U.S. filing date of the ’589 Patent.

D. Iketani (EX1007)

Iketani was filed on February 28, 1996 and issued in December 30, 1997. EX1007 at [22], [45]. Iketani describes a power on reset circuit for use in a DRAM memory device for initializing the internal circuitry thereof when the power is turned on. EX1007 at 1:5-13. In particular, Iketani recognizes that if the power supply voltage for a memory device chip fluctuates significantly, traditional power on reset circuits may activate, causing inadvertent initialization of the chip. EX1007 at 1:59-62. As such, Iketani seeks to provide an improved power on reset circuit that does not erroneously generate such a signal upon power fluctuation. EX1007 at 2:1-4. As shown in Figure 6 of Iketani, Iketani discloses this improved power on reset circuit which generates a power on reset signal that it sends to

various components, including a control circuit. These components, including the control circuit, are then initialized in response to the power on reset signal. *See* EX1007 at 5:20-26.

Iketani qualifies as prior art under at least §102(a), (b) and/or (e) because it was filed, published, and issued before the Priority Date of the '589 patent.

VIII. CLAIM CONSTRUCTION (37 C.F.R. §42.104(B)(3))

Petitioner submits that all claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. In its institution decision for a prior IPR petition against the '589 Patent, the Board found that it “need not interpret explicitly any claim term for purposes of this decision.” *Kingston Tech. Co., Inc. v. Polaris Innovations Ltd.*, IPR2017-00238, Paper 9 at 6 (P.T.A.B. May 2, 2017). Likewise here, construction of terms is unnecessary because it is not dispositive to this case—the art teaches the limitations under any construction under the *Phillips* standard.

IX. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) would have had a Bachelor's degree in Electrical Engineering or Computer Science and two years of experience working in the field of system design using semiconductor memories, or a person with equivalent education, work, or experience in this field. More education could substitute for experience, and vice versa. EX1003, ¶¶31-34.

X. THERE IS A REASONABLE LIKELIHOOD THAT AT LEAST ONE CLAIM OF THE '589 PATENT IS UNPATENTABLE

A. Ground 1: Claims 1, 9, 11, and 13 are Anticipated by Kocis

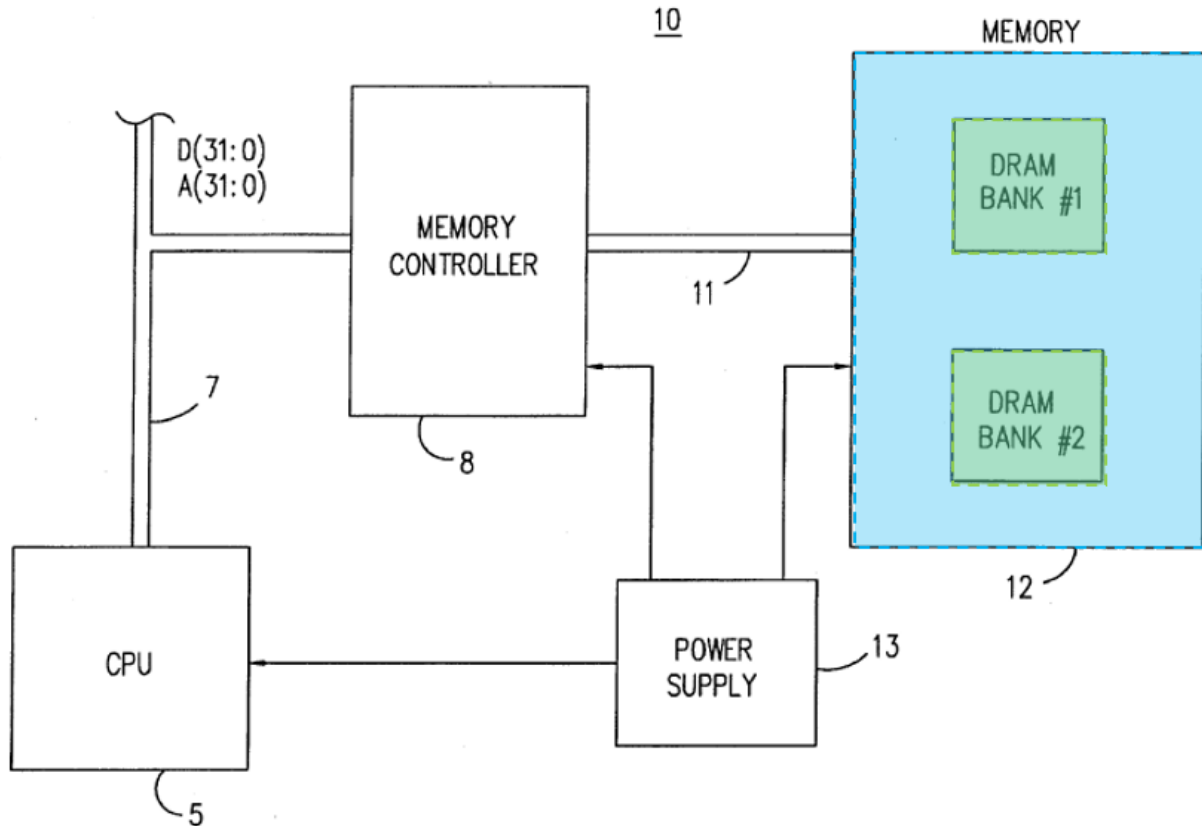
Kocis anticipates claims 1, 9, 11, and 13.

1. Claim [1]

a) Element [1.P]: A dynamic semiconductor memory device of a random access type

The preamble of claim 1 is not limiting because the body of the claim describes a structurally complete invention. *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328-29 (Fed. Cir. 2019). However, to the extent the preamble is found to be limiting, the devices described in Kocis disclose “a dynamic semiconductor memory device of a random access type.” Kocis is directed to “a computer system with two or more banks of dynamic random access memory (DRAM) chips, [and in particular,] to a system for preventing contention on the memory bus between conflicting data signals from two or more DRAM banks.” EX1004 at 1:8-15.

Furthermore, Kocis Figure 1 (annotated below) shows a block diagram of a typical system configuration.



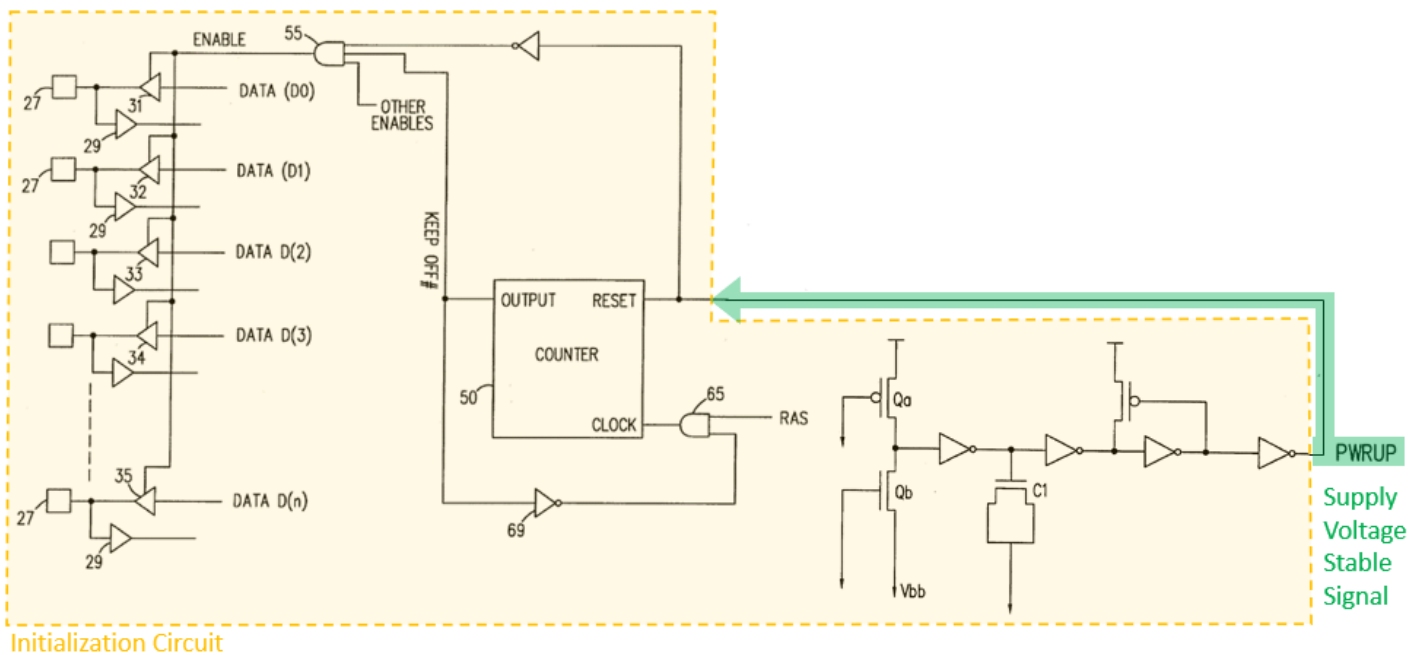
EX1004 (Kocis) at Figure 1 (annotated)

The system configuration includes system memory 12 (blue) which “typically includes banks of dynamic random access memory (DRAM) [devices]. Two DRAM banks are shown in FIG. 1 [green] for purposes of illustration.” EX1004 at 1:45-48; *see also id.* at FIG. 1. Accordingly, a POSITA would have understood that Kocis discloses a dynamic semiconductor memory device of a random access type. EX1003, ¶¶67-69.

- b) Element [1.1]: an initialization circuit controlling a switching-on operation and supplying a supply**

voltage stable signal once a supply voltage has been stabilized after the switching-on operation

Kocis discloses an initialization circuit that is part of the DRAM memory and that (1) controls a switching-on operation and (2) supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. EX1014 at Abstract, 1:8-15, 3:5-9, 4:40-44; EX1003, ¶70. In order to better illustrate the initialization circuit, Petitioner includes annotated version of Kocis Figures 4A and 5 below. EX1003, ¶70. This figure shows components of Kocis that disclose the claimed initialization circuit, outlined in yellow.



EX1004 (Kocis) at Figures 4A and 5 (annotated)

The initialization circuit shown above in yellow controls a switching-on operation (*i.e.*, the process for powering on the memory chip). For example, Kocis explains that “The Pwrup signal is an active low signal, which indicates that the

power supply has ramped to a certain absolute threshold voltage value.” EX1004 at 5:20-22. A POSITA would have understood that the power supply ramping up to a certain absolute threshold voltage value discloses the claimed switching-on operation. EX1003, ¶71.

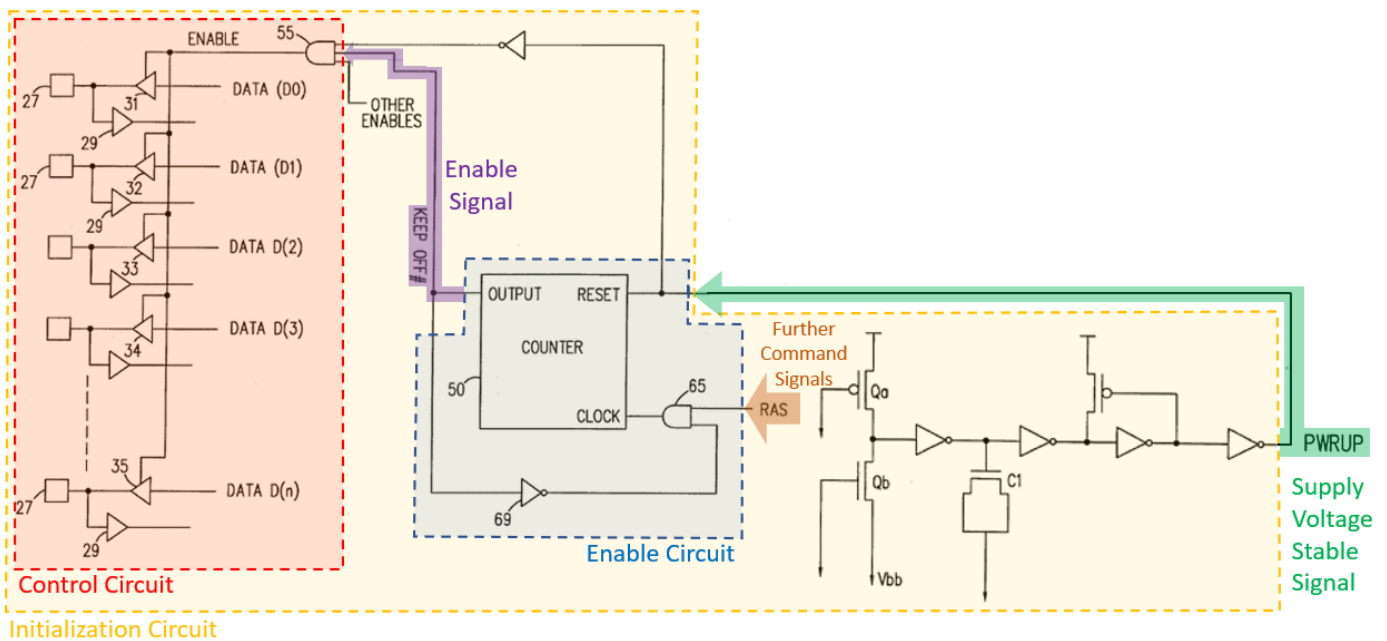
The initialization circuit supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. A POSITA would have understood that the PWRUP signal (outlined in green in the annotated figure above) discloses the claimed supply voltage stable signal. The ’589 Patent indicates that the supply voltage stable signal (*i.e.*, the “POWERON” signal) is active if the internal supply voltages have reached the values necessary for the proper operation of the memory device. EX1001 at 1:13-16, 2:1-4. Similarly, the PWRUP signal “indicates that the power supply has ramped to a certain absolute threshold voltage value.” EX1004 at 5:20-22.

Accordingly, a POSITA would have understood that Kocis discloses an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. EX1003, ¶¶70-73.

- c) **Element [1.2]: said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable**

signal and externally applied further command signals

Kocis discloses an initialization circuit having (i) an enable circuit for receiving the supply voltage stable signal and externally applied further command signals and (ii) a control circuit for controlling operations. In order to better illustrate this disclosure, Figures 4A and 5 of Kocis are annotated below, showing the claimed control circuit (red), enable circuit (blue), and further command signals (brown). EX1003, ¶74.



EX1004 (Kocis) at Figures 4A and 5 (annotated)

Kocis discloses the claimed enable circuit. Specifically, the counter 50, AND gate 65, and inverter 69 in Kocis disclose the claimed enable circuit (shown in blue above). As recited in claim 1, the enable circuit receives both the supply voltage stable signal (the PWRUP signal, shown in green above) and externally

applied further command signals (shown in brown above). As discussed in element [1.1], Kocis' PWRUP signal discloses the claimed supply voltage stable signal. This signal is received by the counter 50 in Kocis, as shown in Kocis Figure 5. EX1004 at FIG. 5; *see also id.* at 6:15-17; EX1003, ¶75.

Kocis discloses that the enable circuit receives the externally applied further command signals. Kocis describes the RAS signals as a "control signal" which is used to transfer data by identifying a specific row associated with a memory location. EX1004 at 2:63, 2:22-28. RAS stands for row address strobe signal. EX1003, ¶76. RAS (and CAS) signals have to do with multiplexing of row and column lines on the same address pins. EX1003, ¶76. RAS (and CAS) signals are primarily used to instruct the memory chip to activate or open a row and then to read a column within the activated row. EX1003, ¶76. First a column address is provided, then the CAS strobe occurs, then a row address is provided, then the RAS strobe occurs. EX1003, ¶76; *see* EX1004 at 2:22-36. Kocis explains that the RAS signal is regularly used for more than just addressing. For example, "[w]hen seven RAS signals have been detected after a threshold voltage is achieved, the DRAM data output lines are enabled. The receipt of eight RAS signals are typically required by DRAM manufacturers to wake-up the DRAM." EX1004 at 3:45-48. A POSITA would recognize that this signal is a command signal, as it provides specific commands to the memory chip. EX1003, ¶76.

Kocis additionally discloses a control circuit for controlling operations (shown in red above), which includes AND gate 55 and the tri-state buffers 31, 32, 33, 34, and 35. EX1003, ¶77. In particular, Kocis discloses that the AND gate 55 and tri-state buffers control when data signals are output to the memory bus. *See, e.g.,* EX1004 at 5:3-12 (“The AND gate 55 receives the following input signals in the preferred embodiment: (1) an inverted Pwrap signal from the output of the voltage detection circuit of FIG. 4A [and] (2) an output signal (Keep Off) from counter 50 The output of the AND gate 55 . . . is driven high if all input signals are high. Thus, tri-state buffers 31, 32, 33, 34, 35 only are enabled if all [the] input signals are high”); *id.* at 1:54-66 (“Because several DRAM banks connect to the memory bus 11 in a typical computer system, precautionary steps must be taken to prevent multiple devices from simultaneously driving signals on the memory bus 11. . . . To prevent the problem with bus contention, each DRAM bank typically includes a tri-state buffer 13 for each of its various data output lines.”).

Thus, proper control of the output drivers is essential for controlling operations of the memory device. Specifically, during a write operation, the output drivers must be turned off to allow external data into the chip, and during a read operation the output drivers must be turned on at the right time to output data to the external pins. EX1003, ¶78. Furthermore, it’s clear the ’589 Patent considered

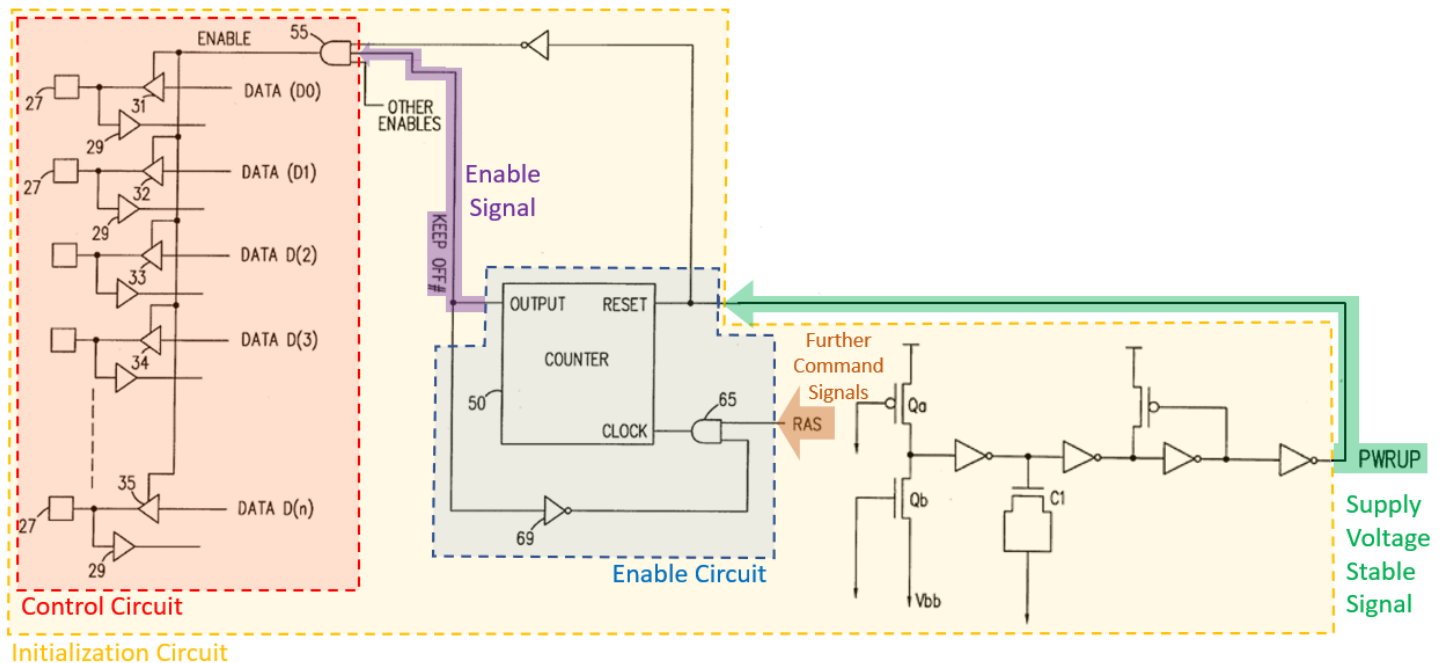
output drivers as part of the claimed control circuit: “The predetermined circuits remain latched until the end of the predetermined initialization sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.” EX1001 at 2:41-45; *see also id.* at cl. 9, 13. Based on this disclosure, a POSITA would have understood that Kocis discloses the claimed control circuit. EX1003, ¶78. Accordingly, Kocis discloses an initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals.

- d) **Element [1.3]: said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit**

Kocis discloses that (1) the enable circuit outputs an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and (2) the enable signal unlatches the control circuit. With reference again to the annotated alternate disclosure (reproduced below), Kocis’ enable signal (shown in purple) which is output from counter 50

(i.e., the Keep Off signal) discloses the enable signal output from the enable circuit.¹ EX1003, ¶79-80.

¹ Although Kocis labels another signal as an “ENABLE” signal (the output of AND gate 55), a POSITA would have understood that the Keep Off signal is also enable signal as claimed. This is supported by both how the Keep Off signal is used in Kocis’ circuit, as discussed in this section, and the fact that Kocis refers to the other inputs to AND gate 55 along with the Keep Off signal input as “Other Enables,” implying that the Keep Off signal is also an enable signal. In addition, although the discussion in this section maps Kocis’ AND gate 55 and output buffers as the claimed “control circuit” and the Keep Off signal as the claimed “enable signal,” Kocis alternatively discloses the claimed “control circuit” as only output buffers and with the “Enable” as the claimed “enable signal.” EX1003, ¶82.



EX1004 (Kocis) at Figures 4A and 5 (annotated)

As explained in Kocis, the enable signal (*i.e.*, Kocis' Keep Off signal) is only output after a predetermined proper initialization sequence of the externally applied further command signals (*i.e.*, Kocis RAS signal). Specifically, “[i]n the preferred embodiment of the present invention, the counter 50 counts the number of RAS signals received from the memory controller 8 (of FIG. 1). After the counter 50 counts eight RAS signals, an output signal (Keep Off) is generated by the counter.” EX1004 at 5:39-43.

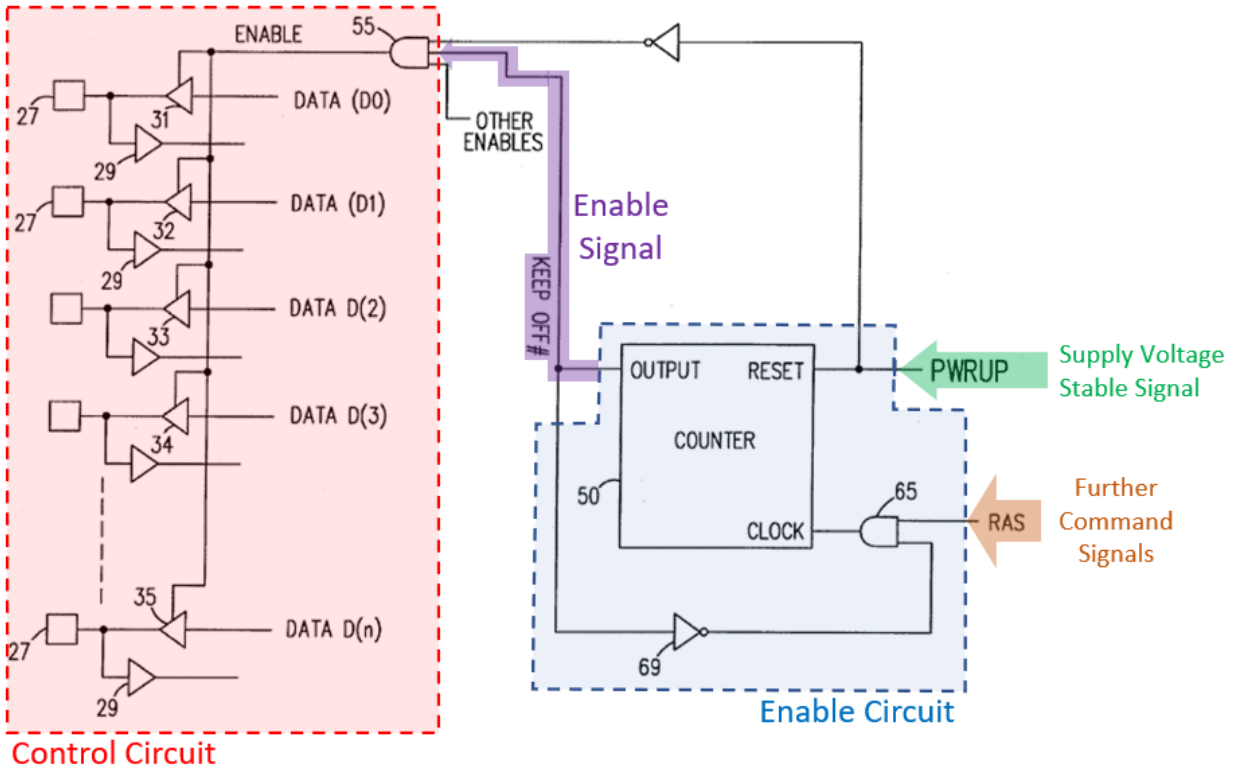
Once the enable signal is driven to a high logic level, it unlatches the control circuit. In other words, unless PWRUP (green) and RAS (brown) signals are input in the correct initialization sequence, the enable circuit (blue) will not output the enable signal (purple). *See, e.g.*, EX1004 at 5:3-12 (“The AND gate 55 receives the

following input signals in the preferred embodiment: (1) an inverted Pwrap signal from the output of the voltage detection circuit of FIG. 4A [and] (2) an output signal (Keep Off) from counter 50 The output of the AND gate 55 . . . is driven high if all input signals are high. Thus, tri-state buffers 31, 32, 33, 34, 35 only are enabled if all [the] input signals are high”); *id.* at 4:56-61 (“all data signals transmitted onto the memory bus 11 by DRAM 100 are driven by tri-state buffers . . . the tri-state buffers transmit the associated data signal only when enabled by the [output of AND gate 55].”); *id.* at 5:22-28 (“Until the voltage supply has reached the threshold value (which will vary from circuit to circuit depending upon the proper operating voltage and other considerations), the AND gate 55 keeps the ENABLE line low, disabling the tri-state buffers 31, 32, 33, 34, 35, thus preventing possible bus contention during start-up or reset.”); *id.* at 2:3-8 (“When the buffer 13 is not enabled, the tri-state buffer 13 functions to ‘disconnect’ the data output line from the memory bus 11, so that neither a low or high signal is driven on the bus, and instead, the buffer presents a high impedance state thereby allowing other circuitry to determine the state of the bus.”). A POSITA would have understood that driving a high input to the AND gate 55 which ultimately enables the tri-state buffers, as is disclosed in Kocis, teaches unlatching the control circuit because it causes the start of normal operation of the buffers. EX1003, ¶81.

Accordingly, a POSITA would have understood that Kocis discloses the enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit. EX1003, ¶¶79-83.

2. Claim [9]: The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit

Kocis discloses a control circuit having output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit. Kocis explains that Figure 5 shows a circuit “for disabling DRAM data output drivers until power supply voltages are satisfactory and all enable conditions are met.” EX1004 at 4:23-26.



EX1004 (Kocis) at Figure 5 (annotated)

As shown in annotated Figure 5 (above), a POSITA would have understood that disabling the output drivers until the enable conditions are met (*i.e.*, the proper initialization sequence has been performed) results in latching the output drivers until the enable signal is generated by the enable circuit. *See* EX1003, ¶85. As discussed with respect to claim 1 (*see* Section X.A.1.d), *supra*), unless PWRUP (green) and RAS (brown) signals are input in the correct initialization sequence, the enable circuit (blue) will not output the enable signal (purple). *See* EX1004 at 5:8-12; *id.* at 5:22-28; *id.* at 2:3-8. Accordingly, Kocis discloses a control circuit having output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit. EX1003, ¶¶84-85.

3. Claim [11]

For the same reasons as those disclosed above in claim 1, Kocis discloses all the limitations of claim 11. EX1003, ¶¶86-88.

- a) **Element [11.P]: An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components**

For the same reasons discussed in Sections X.A.1.a) and X.A.1.b) with respect to claim elements [1.P] and [1.1]. Kocis discloses claim element [11.P].

- b) **Element [11.1]: supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device**

For the same reasons discussed in Section X.A.1.b) with respect to claim element [1.1], Kocis discloses claim element [11.1].

- c) **Element [11.2]: supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit**

provided for a proper operation of the dynamic semiconductor memory device

Furthermore, for the same reasons discussed in Section X.A.1.c) with respect to claim element [1.2], Kocis discloses the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device. Furthermore, for the same reasons discussed in Section X.A.1.d) with respect to claim element [1.3], Kocis discloses supplying, via an enable circuit of the initialization circuit, an enable signal ... after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

- 4. Claim [13]: The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit**

For the same reasons discussed in Section X.A.2 with respect to claim element [9], Kocis discloses claim [13]. EX1003, ¶89.

B. Ground 2: Claims 2, 8, 10, and 12 are Obvious Over Kocis in Combination with JESD 21-C

Kocis in combination with JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Kocis disclosing the limitations of independent Claims 1 and 11 from which they depend (*see* Sections X.A.1 and X.A.3, *supra*).

1. Combination of Kocis and JESD 21-C

JESD 21-C provides various standardized signals, timing diagrams, and other specifications for solid state memory in order to promote interoperability between products. This information includes a power-up sequence to initialize memory to an IDLE state for normal operation in an attempt to eliminate bus contention. EX1006 at page 3.11.5-9. Kocis discloses the circuitry for detection of an initialization sequence of dynamic random access memory, and also has the same stated goal of JESD 21-C (*i.e.*, to initialize memory to an IDLE state for normal operation in an attempt to eliminate bus contention). *See* EX1004 at 1:12-15; *id.* at 3:41-52. The stated intention of Kocis is to detect an initialization sequence performed by external logic that is required by DRAM vendors: “The present invention takes advantage of these preliminary cycles already required as part of the DRAM start-up protocol in designing a scheme to disable the output data drivers of the DRAM 100, thereby preventing bus contention.” EX1004 at 5:34-38.

A POSITA would have been motivated to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Kocis in order to ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by the POSITA. EX1003, ¶¶94-95. In particular, the series of RAS command signals disclosed in Kocis as causing the counter 50 to output the Keep Off signal to effect initialization of the memory circuitry would be replaced in the combination by the series of command signals disclosed in JESD 21-C to be used for initializing memory. EX1003, ¶95. This improvement constitutes the use of a known technique (*i.e.*, the initialization signals and timing for memory devices, including DRAM and SDRAM disclosed in JESD 21-C) to improve similar devices (*i.e.*, the initialization circuitry for the memory devices, including DRAM, disclosed in Kocis) in the same way (*i.e.*, by applying the same initialization signals and timing disclosed in JESD 21-C).

This improvement is also a simple substitution of the signals and timing of Kocis with the signals and timing specified in JESD 21-C. A POSITA would have understood that substituting the signals and timing element of JESD 21-C for those of Kocis would yield predictable results. Specifically, incorporating JESD 21-C's signals and timing would ensure interoperability and compatibility with other products in the solid state memory field. EX1003, ¶96.

2. **Claim [2]: The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal**

The Combination of Kocis and JESD 21-C discloses that the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit including at least one of (i) a preparation command signal for word line activation, (ii) a refresh command signal, and (iii) a loading configuration register command signal.

JESD 21-C discloses each of the claimed further command signals and the predetermined proper initialization sequence of such signals. JESD 21-C teaches the following sequence for initialization of SDRAM:

“The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge* commands for all banks of the device.
4. Issue 8 or more *autorefresh* commands.
5. Issue a *mode register set* command to initialize the mode register.

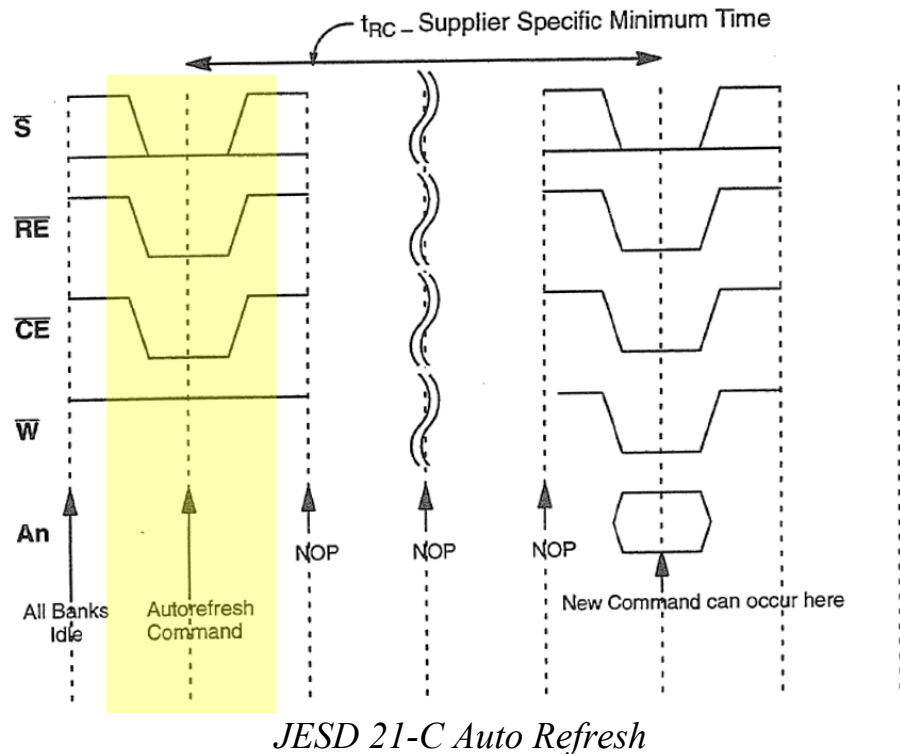
The device is now in the IDLE state and is ready for normal operation.”

EX1006 at page 3.11.5-9 (emphasis added).

JESD 21-C additionally discloses details of each of these command signals. The Background of the '589 Patent describes the prior art preparation command signal for word line activation as a "PRE" or "PRECHARGE" event for all memory banks of the device. EX1001 at 1:53-55. A POSITA would have understood that this signal is intended to ensure that all memory cells are at an initial baseline charge prior to operation. EX1003, ¶99. JESD 21-C discloses the PRECHARGE signal. JESD 21-C discloses two different Precharge signals: Auto Precharge and Precharge All Banks. EX1006 at page 3.11.5-9. In Auto Precharge, "[t]he user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle." *Id.* To precharge all banks, "[t]he user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks."

The Background of the '589 Patent describes the prior art refresh command signal as an "ARF" or "AUTOREFRESH" signal. EX1001 at 2:2:52-53. A POSITA would have understood that the AUTOREFRESH signal is also associated with restoring charge on the memory cells. EX1003, ¶100. JESD 21-C discloses the AUTOREFRESH signal. JESD 21-C explains that "AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address

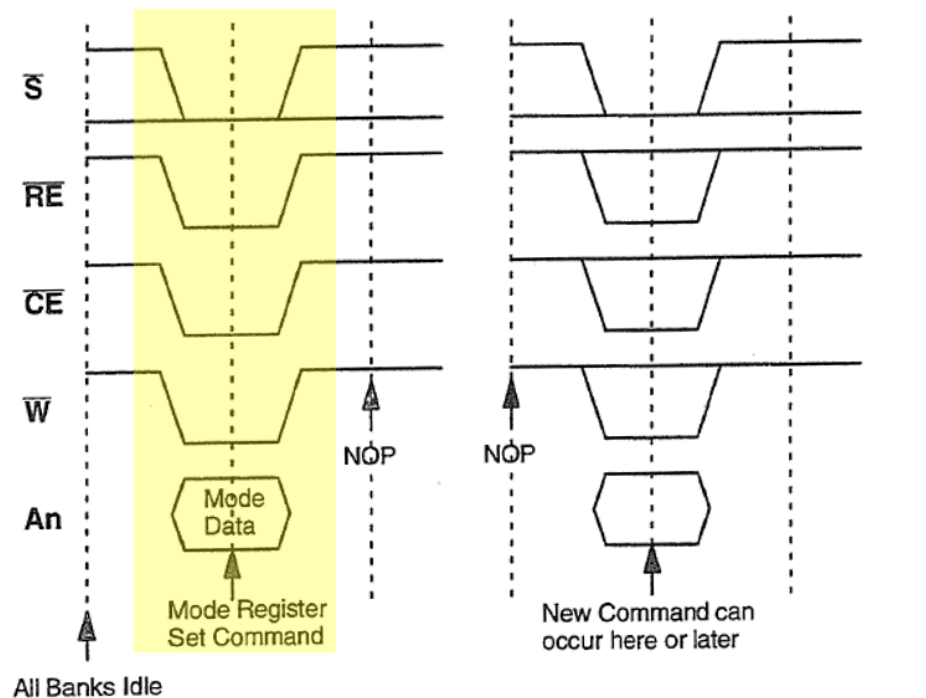
being supplied by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE).”



EX1006 at page 3.11.5-11.

The Background of the '589 Patent describes the prior art loading configuration register command signal as an “MRS” or “MODE-REGISTER-SET” signal. EX1001 at 2:2:53-54. JESD 21-C discloses the MODE-REGISTER-SET signal. JESD 21-C provides the timing diagram necessary to initiate a Mode-Register-Set Command in Section 3.11.5.7. “The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set

cycle can be followed by a new command in [as little as] 3 clock cycles as illustrated in the diagram below.”



JESD 21-C Mode Register Write Timing

EX1006 at page 3.11.5-10.

A POSITA would have understood that Kocis can accept the three further command signals listed above. EX1003, ¶102. In particular, a POSITA would have understood that the CASB and RASB (CAS and RAS with low activation) inputs identified in Lee are standard DRAM inputs. EX1003, ¶102. Thus, a POSITA would have understood that the proper sequencing of inputs on the CASB and RASB signals, along with other control signals, could be used to generate each of the Precharge, AutoRefresh, and Mode-Register-Set commands, as described in the JESD 21-C standard. EX1003, ¶102.

Accordingly, the combination of Kocis and JESD 21-C discloses that the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit including at least one of (i) a preparation command signal for word line activation, (ii) a refresh command signal, and (iii) a loading configuration register command signal.

EX1003, ¶¶97-103.

3. **Claim [8]: The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard**

The combination of Kocis and JESD 21-C discloses the initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard. Although neither claim 8 nor the '589 Patent specification identify any particular JEDEC standard that this claim was intended to cover, the background of the '589 Patent does disclose that one predetermined proper initialization sequence that conforms to an unnamed JEDEC standard constitutes the commands PRECHARGE, AUTO REFRESH, and MODE-REGISTER-SET in the following chronological order: (1) PRECHARGE, (2) AUTOREFRESH, and (3) MODE-REGISTER-SET. *See* EX1001 at 1:43-61; *id.* at FIG. 3, 5:10-16, 4:59-5:21, claim 10. The background section of the '589 Patent

admits that this sequence is known and incorporated in a JEDEC standard for SDRAM that was available as of the filing of the '589 Patent. EX1001 at 1:43-61. Indeed, JESD 21-C does in fact teach this exact sequence for initialization of SDRAM:

“The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge* commands for all banks of the device.
4. Issue 8 or more *autorefresh* commands.
5. Issue a *mode register set* command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.”

EX1006 at page 3.11.5-9 (emphasis added).

JESD 21-C is a JEDEC standard. *See, e.g.,* EX1006 at Copyright Notice; *id.* at 1-1 (“This standard is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council through September, 1989.”). Accordingly, the combination of Kocis and JESD 21-C teaches identification of an initialization sequence that is identified as a predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard. EX1003, ¶¶104-05.

4. **Claim [10]: The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal**

As described in the analysis of claims [2] and [8] in Sections X.B.2 and X.B.3, the combination of Lee and JESD 21-C teaches each of a preparation command signal for word line activation (precharge / PRE), refresh command signal (autorefresh / ARF), and loading configuration register command signal (mode register set / MRS). JESD 21-C further discloses the claimed predetermined proper initialization sequence. EX1003, ¶106.

Claim 10 recites that the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

Claimed Order 1	PRE	ARF	MRS
Claimed Order 2	PRE	MRS	ARF
Claimed Order 3	MRS	PRE	ARF

JESD 21-C discloses the first claimed order: “The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs

2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue *precharge commands* [PRE] for all banks of the device.
4. Issue 8 or more *autorefresh commands* [ARF].
5. Issue a *mode register set command* [MRS] to initialize the mode register.”

EX1006 at page 3.11.5-9 (emphasis added).

Accordingly, the combination of Kocis and JESD 21-C disclose all of the elements of claim [10]. EX1003, ¶106-09.

5. **Claim [12]: The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals**

For the same reasons discussed in Section X.B.2 with respect to claim [2], Kocis in combination with JESD 21-C discloses claim [12].

C. Grounds 3A & 3B: Claims 1 and 11 are Anticipated by or Obvious Over Lee

Lee anticipates or renders obvious claims 1 and 11 of the '589 Patent.

1. **Claim [1]**
 - a) **Element [1.P]**

As discussed above in Ground 1, the preamble of claim 1 is not limiting. Nevertheless, to the extent the preamble is found to be limiting, the devices described in Lee disclose “a dynamic semiconductor memory device of a random

access type.” In particular, Lee is directed to an “initialization circuit for a *semiconductor memory device*.” EX1005 at Abst. (emphasis added). The stated objects of the Lee disclosure include: (1) “to reliably initialize a *semiconductor memory device* when a power-up reset circuit malfunctions” and (2) “to initialize a *semiconductor memory device* in response to external logic signals.” EX1005 at 2:18-23 (emphasis added).

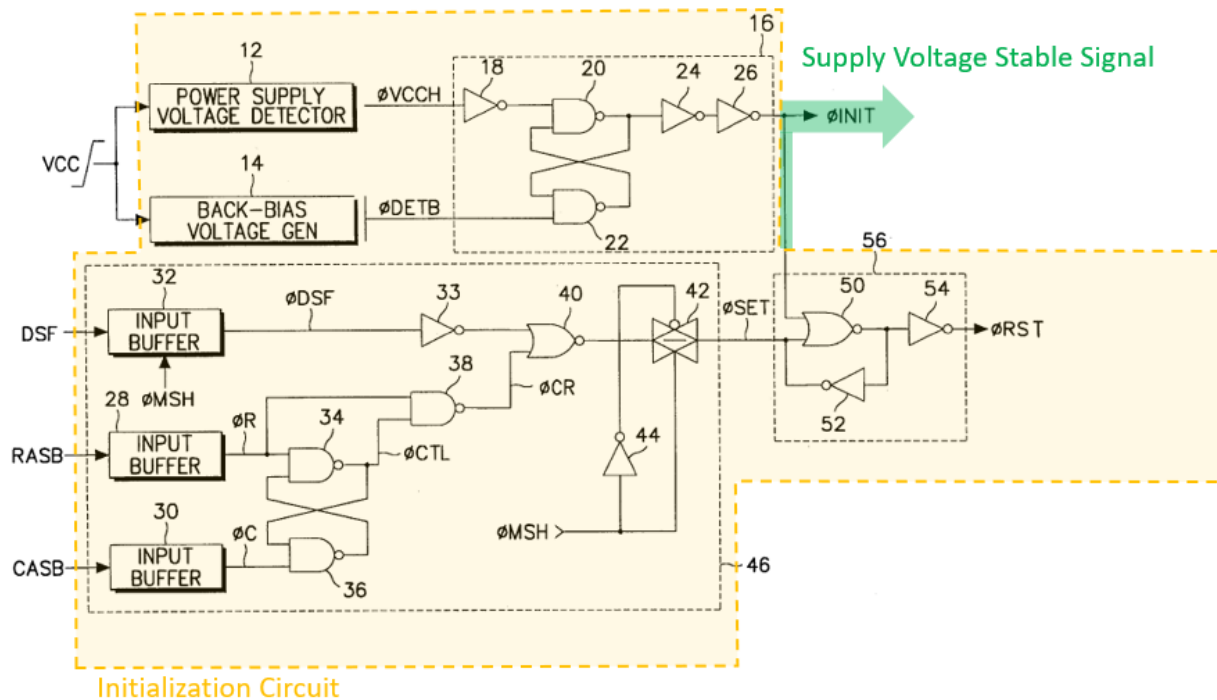
A POSITA would have understood that the semiconductor memory device of Lee is a dynamic device of a random access type. EX1003, ¶117. In particular, a POSITA would have understood that the input signals CASB and RASB are specific to Dynamic Random Access Memory (DRAM) type devices. Column Address Strobe (CAS) and Row Address Strobe (RAS) signals have to do with multiplexing of column and row lines on the same address pins and are used almost exclusively on DRAMs. EX1003, ¶117.

As further support that a POSITA would recognize this functionality, JESD 21-C indicates that that CAS signal is “an enable signal that on some *dynamic RAMs* actuates only the column oriented internal circuits and the data input/output circuits. Most Devices normally require the RAS\ signal to be present for the CAS\ signal to be effective.” EX1006 at page 2-2. The RAS signal is defined similarly, as “a chip enable signal that, on certain *dynamic RAMs*, actuates only row address oriented internal circuitry.” EX1006 at page 2-4.

Accordingly, Lee discloses claim element [1.P]. EX1003, ¶116-19.

b) Element [1.1]

Lee discloses an initialization circuit that (1) controls a switching-on operation and (2) supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. In order to better demonstrate the initialization circuit, annotated version of Lee Figure 3 is provided below, which shows components of Lee (namely elements 12, 14, 16, 46, and 56) that disclose the claimed initialization circuit, outlined in yellow. EX1003, ¶120.



EX1005 (Lee) at Figure 3 (annotated)

The initialization circuit shown above in yellow controls a switching-on operation (*i.e.*, the process for powering on the memory chip). For example, Lee explains that these types of “initialization circuits are typically referred to as power

on reset circuits and generate a reset signal in response to a power supply voltage VCC being applied to the [DRAM] chip. The typical power on reset circuit operates by sensing the level of the power supply voltage VCC and generating an initialization signal for a predetermined length of time when the power supply voltage reaches a predetermined level.” EX1005 at 1:18-29.

The initialization circuit supplies a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. Lee indicates that the circuit “includes a first initialization signal generator 46, a second initialization signal generator 16 and a transfer unit 56. The first initialization signal generator generates a first initialization signal ϕ SET in response to a sequence of reset control signals DSF, RASB, and CASB. The second initialization signal generator 16 . . . generates a second initialization signal ϕ INIT in response to the power-up of a power supply VCC. The transfer unit 56 generates a reset signal ϕ RST for resetting a circuit within the memory device responsive to the first and second initialization signals.” *Id.* at 3:9-23.

One of skill in the art would have understood that the ϕ INIT signal (outlined in green in the annotated figure above) discloses the claimed supply voltage stable signal. EX1003, ¶123. The ’589 Patent indicates that the supply voltage stable signal (*i.e.*, the “POWERON” signal) is active if the internal supply voltages have reached the values necessary for the proper operation of the memory device.

EX1001 at 1:13-16, 2:1-4. Similarly, the ϕ INIT signal goes to a logic high level immediately in response to the power supply detection signal ϕ VCCH, which monitors the voltage level of the power supply voltage (VCC), and subsequently goes low upon detection of the proper device operating voltages, which is triggered by a low voltage on the ϕ DETB signal. EX1005 at 1:31-34, 1:47-54. Furthermore, Lee explains that the ϕ INIT signal is generated “in response to the power-up of a power supply VCC” (*id.* at 3:9-23) meaning it is supplied once a supply voltage has been stabilized after the switching-on operation. The low voltage on the ϕ RST signal, triggered by the ϕ DETB signal going low, is the indication that the supply voltage VCC has stabilized. EX1005 at FIG. 2, 1:34-40; EX1003, ¶123.

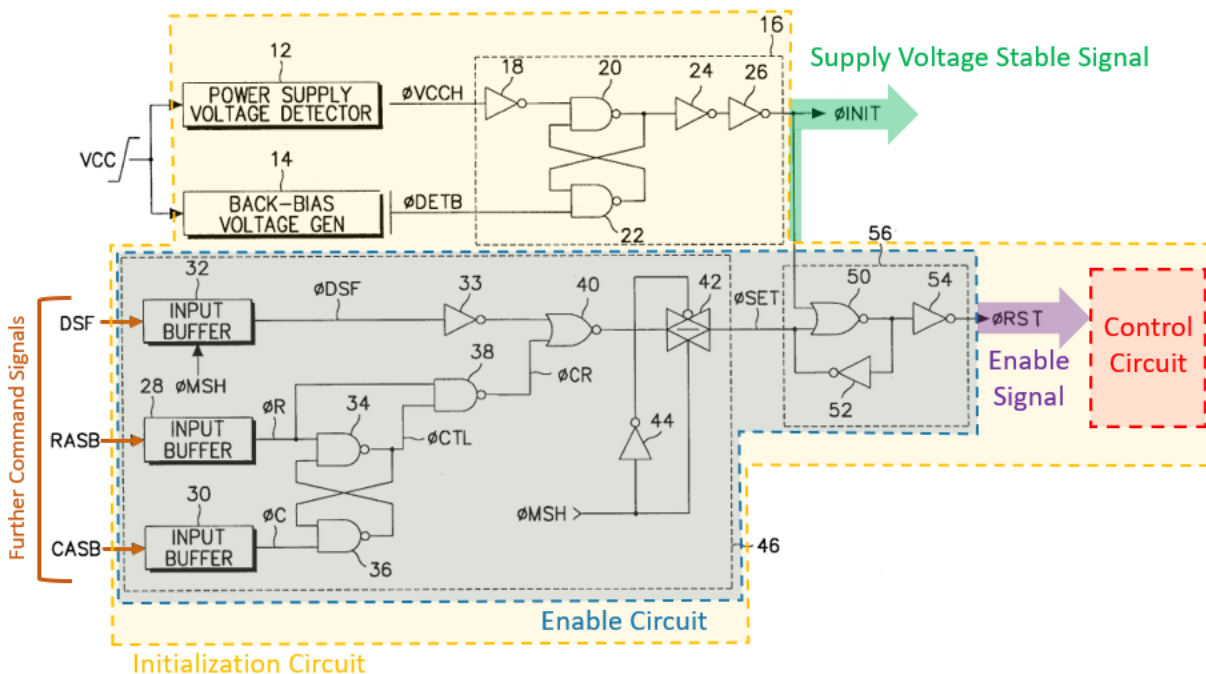
Accordingly, a POSITA would have understood that Lee discloses an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. EX1003, ¶¶120-24.

c) Element [1.2]

Lee discloses an initialization circuit (i) an enable circuit for receiving the supply voltage stable signal and externally applied further command signals and (ii) a control circuit for controlling operations. In order to better illustrate the combination, annotated Figure 3 of Lee with the claimed control circuit (red),

enable circuit (blue), and further command signals (brown), is provided below.

EX1003, ¶125.



EX1005 (Lee) at Figure 3 (annotated)

Lee discloses the claimed enable circuit. Specifically, Lee's first initialization signal generator 46 and transfer unit 56 disclose the claimed enable circuit (shown in blue above). As recited in claim 1, the enable circuit receives both the supply voltage stable signal (shown in green above) and externally applied further command signals (shown in brown above). As discussed in element [1.1], Lee's ϕ INIT signal discloses the claimed supply voltage stable signal. This signal is received by the transfer unit 56 of Lee, as shown in Lee Figure 3. EX1005 at FIG. 3; *see also id.* at 4:33-35, 4:59-62.

Lee also discloses that the enable circuit receives the externally applied further command signals. The '589 Patent identifies the command signals as “a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).” EX1001 at 2:50-54. A POSITA would have understood that Lee discloses similar command signals in the CASB, RASB, and DSF signals shown in Lee’s Figure 3. EX1003, ¶127. Lee describes the CASB, RASB, and DSF signals as a first control signal, second control signal, and mode selection signal, respectively, each of which are inputs to the first initialization signal generator 46. EX1005 at 3:37-49. CAS and RAS signals have to do with multiplexing of column and row lines on the same address pins. CAS and RAS signals are primarily used to instruct the memory chip to activate or open a row and then to read a column within the activated row. DSF is a special function enable input that, when true, can enable certain special functions on the memory chip. Lee refers to these three signals collectively as “reset control signals.” EX1005 at 3:14-16. A POSITA would recognize that these signals are command signals as they provide specific commands to the memory chip. EX1003, ¶127.

Additionally, the CASB and RASB signals are further command signals because a POSITA would have understood that they can be used to generate the

PRECHARGE, AUTOREFRESH, and MODE-REGISTER-SET commands disclosed in the '589 Patent. EX1003, ¶128. CAS and RAS are fundamental DRAM signals. EX1003, ¶128. Additional DRAM signals include Chip Select (CS), which enables the memory chip's command decoder and Write Enable (WE), which enables writing to memory registers. EX1003, ¶128. A POSITA would have understood that applying certain inputs to these signals in a certain sequence will initiate certain commands on the memory chip. EX1003, ¶128. These commands are performed by way of a command decoder, which accepts the RAS, CAS, CS, and WE signals and interprets the sequence as a particular command. EX1003, ¶128. Depending on the combination of these signals, a different command is requested and performed on the memory chip. EX1003, ¶128. For example, a POSITA would have understood that the PRECHARGE command is performed by activating CS, RAS, and WE and leaving CAS inactive. *See, e.g.*, EX1019 at 10; EX1003, ¶128.

Lee additionally teaches to a POSITA or, in the alternative, renders obvious a control circuit for controlling operations (shown in red above). *See, e.g.*, EX1005 at 4:20-24 (“An inverter 54 has an input terminal connected to the output terminal of NOR gate 50 and an output terminal which forms the output terminal of the transfer unit 56 for sending the reset signal ϕ RST to a circuit to be initialized within the chip.”); *id.* at 4:59-62 (“The transfer unit 56 combines the first

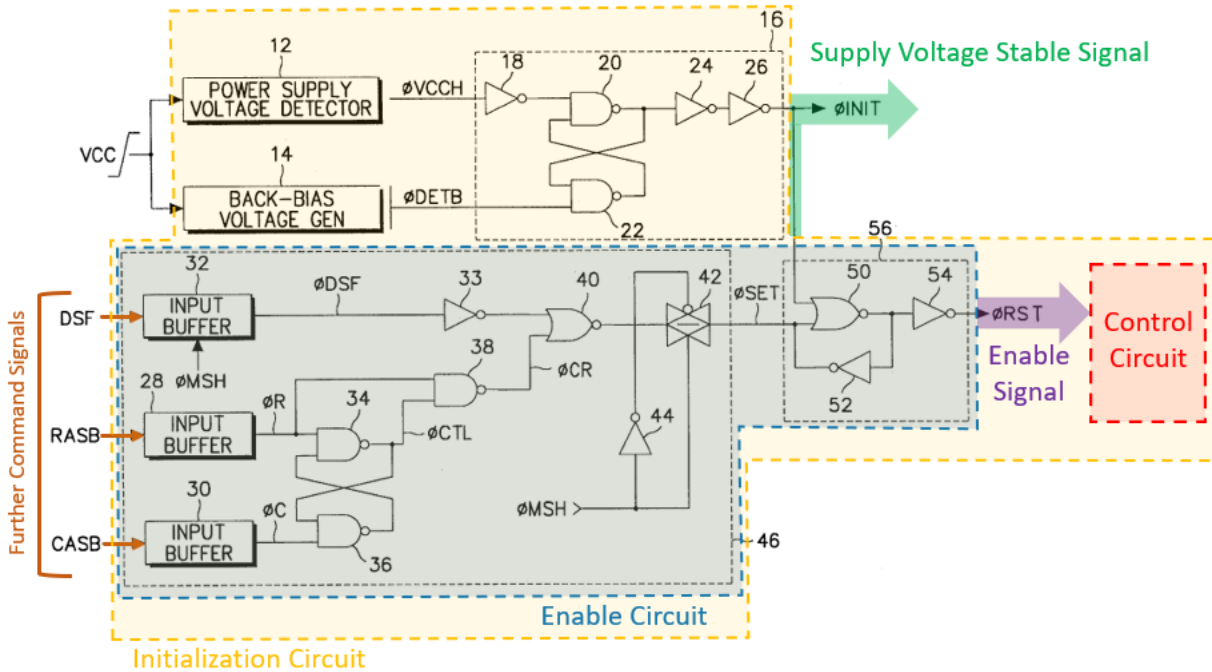
initialization signal ϕSET and the second initialization signal ϕINIT and activates the reset signal ϕRST by driving it to a high logic level, thereby initializing the circuits within the chip.”); *id.* at 5:11-13 (“In the embodiment of FIG. 3, the first and second initialization signals are supplied to individual circuits via one transfer unit.”); *id.* at 3:19-22 (“The transfer unit 56 generates a reset signal ϕRST for resetting a circuit within the memory device responsive to the first and second initialization signals.”); *id.* at 4:35-37 (“Thus, all circuits within the chip which are connected to the output terminal of transfer unit 56 is held in the initialized state.”); *id.* at 1:20-21 (“Such devices require initialization circuits for resetting the various functional circuits within the chip.”).

Based on this disclosure, a POSITA would have understood that Lee discloses the claimed control circuit. EX1003, ¶130. In particular, a POSITA would have understood that all memory devices have control circuits for controlling operations. EX1003, ¶130. These circuits are necessary because sequences of commands are sent to the memory device in order to perform reads and writes to memory cells and to perform configuration operations. EX1003, ¶130. A POSITA would have understood that there would be a control circuit that receives these external commands and controls the internal operation of the memory device so as to properly respond to the commands. EX1003, ¶130. A POSITA would also understand that every control circuit needs to be initialized in

order for it to operate reliably. EX1003, ¶130. A basic part of logic design indicates that every sequential circuit (a circuit that maintains state), such as a control circuit, needs a reset mechanism to ensure that it powers up in a known state. EX1003, ¶130. Powering up sequential logic without initialization could lead to an unknown state and unpredictable operation. EX1003, ¶130. Thus, it follows that a memory device requires an initialization sequence that resets the control circuit and this initialization sequence must be complete before operation of the memory device can take place. EX1003, ¶130. Accordingly, Lee discloses, or at the very least renders obvious, an initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals. EX1003, ¶¶125-30.

d) Element [1.3]

Lee discloses that (1) the enable circuit outputs an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and (2) the enable signal unlatches the control circuit. With reference again to the annotated combination (reproduced below), Lee's ϕ RST signal (shown in purple) which is output from transfer unit 56 discloses the enable signal output from the enable circuit. EX1003, ¶131.



EX1005 (Lee) at Figure 3 (annotated)

As explained in Lee, the ϕRST signal is set to a high voltage immediately after power is applied, triggered by the $\phi INIT$ signal going high, and only goes to a low voltage after a predetermined proper initialization sequence of the externally applied further command signals (*i.e.*, Lee signals CASB, RASB, and DSF). “[I]f the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence, the first initialization signal generator activates the first initialization signal ϕSET . For this to occur, the reset control signals DSF, RASB, and CASB must be activated in the CBR (CAS before RAS) mode. The mode selection clock signal ϕDSF is first activated, *i.e.*, driven to a high-logic level. . . . If the first control signal CASB is then activated by being driven to a low logic state, . . . [t]hen, if the second control signal RASB is driven to the active low logic

level, . . . the first initialization signal ϕSET [is activated] at the output terminal of NOR gate 40. . . . The transfer unit 56 combines the first initialization signal ϕSET and the second initialization signal ϕINIT and activates the reset signal ϕRST by driving it to a high logic level.” EX1005 at 4:38-61.

After the initialization sequence is complete, the ϕRST signal goes to a low logic level. Thus, once the reset signal ϕRST is driven to a low logic level, it unlatches the control circuit. *See, e.g.*, EX1005 at 4:59-5:4 (“The transfer unit 56 combines the first initialization signal ϕSET and the second initialization signal ϕINIT and activates the reset signal ϕRST by driving it to a high logic level, thereby initializing the circuits within the chip.”); *id.* at 4:13-24 (“The transfer unit 56 includes . . . an output terminal which forms the output terminal of the transfer unit 56 for sending the reset signal ϕRST to a circuit to be initialized within the chip.”). A POSITA would have understood that initializing the circuit within the chip, followed by deactivating the reset signal, as is disclosed in Lee, teaches unlatching the control circuit because it causes the start of normal operation of the buffers. EX1003, ¶133.

Accordingly, a POSITA would have understood that Lee discloses the enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being

identified and the enable signal effecting an unlatching of said control circuit.

EX1003, ¶¶131-34.

2. Claim [11]

For the same reasons as those disclosed above in claim 1, Lee discloses all the limitations of claim 11. EX1003, ¶¶135-37.

For the same reasons discussed in Sections X.C.1.a) and X.C.1.b) with respect to claim elements [1.P] and [1.1]. Lee discloses claim element [11.P].

For the same reasons discussed in Section X.C.1.b) with respect to claim element [1.1], Lee discloses claim element [11.1].

Furthermore, for the same reasons discussed above for claim elements [1.2] and [1.3], Lee discloses claim element [11.3]. In particular, for the same reasons discussed in Section X.C.1.c) with respect to claim element [1.2], Lee discloses the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device. Furthermore, for the same reasons discussed in Section X.C.1.d) with respect to claim element [1.3], Lee discloses supplying, via an enable circuit of the initialization circuit, an enable signal ... after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

D. Ground 4: Claims 1 and 11 are Obvious Over Lee in Combination with Iketani

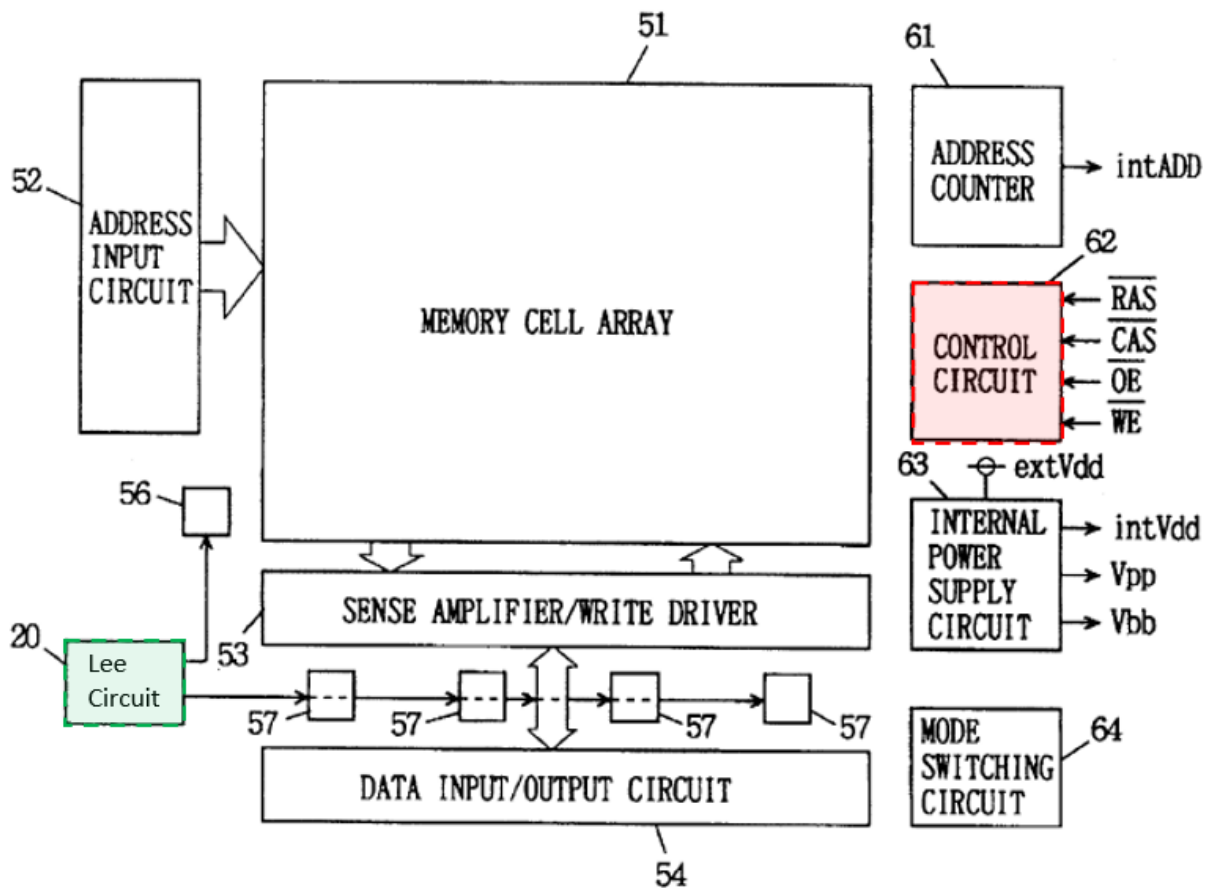
Lee in combination with Iketani renders obvious claims 1 and 11 of the '589 Patent.

1. Combination of Lee and Iketani

The disclosed circuit configurations of Lee and Iketani can and would have been combined to arrive at the claimed memory device of the '589 patent. In particular, a POSITA could and would have recognized that the initialization circuit of Lee is compatible with the controller of Iketani and would have combined the disclosure of Lee with that of Iketani. EX1003, ¶140. While Lee does expressly illustrate the “circuitry” that is initialized by the reset signal ϕRST output from its initialization circuit, Iketani illustrates and describes in detail the various circuits, including the control circuit, that receive and are initialized by such an initialization signal.

In particular, the initialization circuit disclosed in Lee has the same functionality as the power on reset circuit 20 of Iketani. Both the power on reset circuit of Iketani and the initialization circuit of Lee perform similar functions and are used for the same purpose. *Compare* EX1005 at 2:4-6, 18-20 (“A problem with [a conventional initialization circuit] is that it may malfunction if the power supply voltage VCC is unstable input. . . . It is therefore an object of the invention to reliably initialize a semiconductor memory device when a power-up reset circuit

malfunctions.”) *with* EX1007 at 2:1-4 (“[a]nother object of the present invention is to provide a power on reset circuit which does not erroneously generate a reset signal even when the power supply voltage fluctuates significantly.”). As shown in Iketani Figure 6 (annotated below) Lee’s initialization circuit (shown in green) can be substituted for Iketani’s power on reset circuit.



EX1007 (Iketani) at Figure 6 (annotated)

Both Lee’s initialization circuit and Iketani’s power on reset circuit output similar signals. *Compare* EX1005 at 4:59-62 (“The transfer unit 56 combines the first initialization signal ϕ_{SET} and the second initialization signal ϕ_{INIT} and

activates the reset signal ϕ RST by driving it to a high logic level, thereby initializing the circuits within the chip.”) *with* EX1007 at 1:36-38 (“In response to the power on reset signal POR at the L level, internal circuitry of the SRAM, DRAM or the like is initialized.”). As Iketani’s power on reset circuit outputs signals that are accepted by the control circuit, a POSITA would have understood that Lee’s initialization circuit is additionally compatible with Iketani’s control circuit. EX1003, ¶142; *see* EX1007 at 5:20-26 (“The power on reset signal generated by power on reset circuit 20 is supplied to address counter 61, control circuit 62, internal power supply circuit 63, mode switching circuit 64, redundant row program circuit 56, redundant column program circuit 57 and so on. Therefore, these circuits 61 to 64, 56, 57 are initialized in response to the power on reset signal.”).

This amounts to a simple substitution of one component (*i.e.*, Lee’s initialization circuit) for another (*i.e.*, Iketani’s power on reset circuit), and a POSITA would have understood that this substitution would yield predictable results. EX1003, ¶143.

2. Claims [1] and [11]

The combination of Lee and Iketani disclose the claim elements of claims [1] and [11] for the same reasons as those disclosed in Grounds 3A and 3B (*see* Section X.C, *supra*). EX1003, ¶¶144-51. However, to the extent the Patent Owner

argues incorrectly that Lee does not disclose or render obvious the claimed control circuit, this ground shows the combination of Lee and Iketani also discloses the claimed control circuit for controlling operations. *Id.*

First, as recited in claim preambles [1.P] and [11.P], Iketani discloses a dynamic semiconductor memory device of a random access type through Iketani's express disclosure of a DRAM. *See* EX1007 at FIG. 6 and 5:4-26.

Second, in the combination, Lee discloses the initialization circuit supplying a supply voltage stable signal, as recited in claim elements [1.1] and [11.1].

Third, in the combination, Iketani discloses the claimed control circuit for controlling operations, as recited in claim elements [1.2] and [11.2] (with Lee disclosing the other portions of these elements) . In particular, Iketani's control circuit 62 is for "controlling internal circuitry" of the memory device and initializes the memory device in response to the power on reset signal. *See* EX1007 at 5:12-26 ("The power on reset signal generated by power on reset circuit 20 is supplied to address counter 61, *control circuit 62*, internal power supply circuit 63, mode switching circuit 64, redundant row program circuit 56, redundant column program circuit 57 and so on. Therefore, these circuits 61 to 64, 56, 57 are initialized in response to the power on reset signal.") (emphasis added); *see also* EX1007 at FIG. 6 (identifying control circuit 62). A POSITA would have

understood that this disclosure teaches the claimed control circuit for controlling operations. EX1003, ¶147, 151.

Finally, in addition to Lee's disclosure of an enable signal unlatching the memory circuits, including the control circuit, as recited in claim elements [1.3] and [11.2], the combination of Lee and Iketani further discloses that the control circuit is unlatched by an enable signal through Iketani's disclosure that the control circuit is initialized by the reset signal. *See* EX1007 at 5:12-26; EX1003, ¶148, 151.

E. Ground 5: Claims 2, 8, 10, and 12 are Obvious Over Lee in Combination with JESD 21-C

Lee in combination with JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Lee disclosing or rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Sections X.C.1 and X.C.2, *supra*).

1. Combination of Lee and JESD 21-C

JESD 21-C provides various standardized signals, timing diagrams, and other specifications for solid state memory in order to promote interoperability between products. This information includes a power-up sequence to initialize memory to an IDLE state for normal operation in an attempt to eliminate errors during power-up. EX1006 at page 3.11.5-9. Lee discloses the necessary circuitry for proper initialization and power-up of dynamic random access memory, and also

has the same stated goal of JESD 21-C (*i.e.*, to initialize memory to an IDLE state for normal operation in an attempt to eliminate errors during power-up). *See* EX1005 at 2:4-7; *id.* at 2:18-20.

A POSITA would have been motivated to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Lee in order to ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by the POSITA. EX1003, ¶154. This improvement constitutes the use of a known technique (*i.e.*, the initialization signals and timing for memory devices, including DRAM and SDRAM disclosed in JESD 21-C) to improve similar devices (*i.e.*, the memory devices, including DRAM disclosed in Lee) in the same way (*i.e.*, by applying the same initialization signals and timing disclosed in JESD 21-C).

This improvement is also a simple substitution of the signals and timing of Lee with the signals and timing specified in JESD 21-C. A POSITA would have understood that substituting the signals and timing element of JESD 21-C for those of Lee would yield predictable results. EX1003, ¶155. Specifically, incorporating JESD 21-C's signals and timing would ensure interoperability and compatibility with other products in the solid state memory field. For example, if using the initialization circuit of Lee with SDRAM instead of DRAM, a POSITA would

have been motivated to use the SDRAM initialization sequence disclosed and standardized in JESD 21-C. EX1003, ¶155.

2. Claims [2], [8], [10], and [12]

The combination of Lee and JESD 21-C disclose the claim elements of claims [2], [8], [10], and [12] for the same reasons as those disclosed in Ground 2 (*see* Section X.B, *supra*). EX1003, ¶¶156-69. These claims recite characteristics of the claimed predetermined proper initialization sequence, and the disclosure of JESD 21-C of such characteristics applies equally whether combined with Kocis or Lee.

F. Ground 6: Claims 2, 8, 10, and 12 are Obvious over Lee in Combination with Iketani and JESD 21-C

Lee in combination with Iketani and JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Lee and Iketani rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Section X.D.2, *supra*). EX1003, ¶¶170-75.

1. Combination of Lee, Iketani, and JESD 21-C

For the reasons discussed in Section X.D.1, a POSITA would have been motivated to combine the teachings of Lee and Iketani, and for the reasons discussed in Section X.E.1, a POSITA would have been further motivated to combine the teachings of JESD 21-C into that Lee-Iketani combination. EX1003, ¶171.

2. Claims [2], [8], [10], [12]

As discussed in Ground 4, to the extent the Patent Owner argues incorrectly that Lee does not disclose or render obvious the claimed control circuit, this ground shows that the combination of Lee and Iketani also discloses the claimed control circuit for controlling operations. *See* Section X.D.2 , *supra*. Otherwise, the combination of Lee, Iketani, and JESD 21-C discloses the claim elements of claims [2], [8], [10], and [12] for the same reasons as those disclosed in Ground 5. *See* Section X.E, *supra*. EX1003, ¶¶172-75.

G. Ground 7: Claims 9 and 13 are Obvious Over Lee in Combination with Kocis

Lee in combination with Kocis renders obvious claims 9 and 13 of the '589 Patent, with Lee disclosing or rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Sections X.C.1 and X.C.2, *supra*).

1. Combination of Lee and Kocis

As previously described, Kocis provides output drivers that remain latched during the initialization and switching-on operation of the memory device and that are then unlatched upon the stabilization of power and the receipt of a proper initialization sequence of command signals. *See*, Section X.A.2, *supra*. Similarly, as described above, Lee also discloses that circuitry of a memory device remains latched until the stabilization of power and the receipt of a proper initialization sequence of command signals. *See*, Section X.C.1.d), *supra*. However, Lee does

not expressly disclose that the output buffers/drivers of the memory device are part of this circuitry that is unlatched upon initialization. A POSITA would have been motivated to use the reset signal output by the initialization circuit of Lee to unlatch the memory device's output buffers/drivers, as disclosed in Kocis, as one of the various circuitry that are disclosed in Lee as being unlatched in order to ensure the ability to "reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions," which is the stated goal of Lee (EX1005 at 2:18-20), and to address "problems which may arise on a memory bus during system power-up" such as "preventing contention on the memory bus between conflicting data signals from two or more DRAM banks, which is the stated goal of Kocis (EX1004 at 1:11-15). EX1003, ¶177. This improvement constitutes the use of a known technique (*i.e.*, the output driver disabling feature of Kocis) to improve similar devices (*i.e.*, the memory devices, including DRAM disclosed in Lee) in the same way (*i.e.*, by applying the same initialization procedure disclosed in Lee to unlatch output drivers as in Kocis). Because of the similarities between the initialization procedures in both Lee and Kocis, a POSITA would have a reasonable expectation of success in combining the two references. EX1003, ¶177.

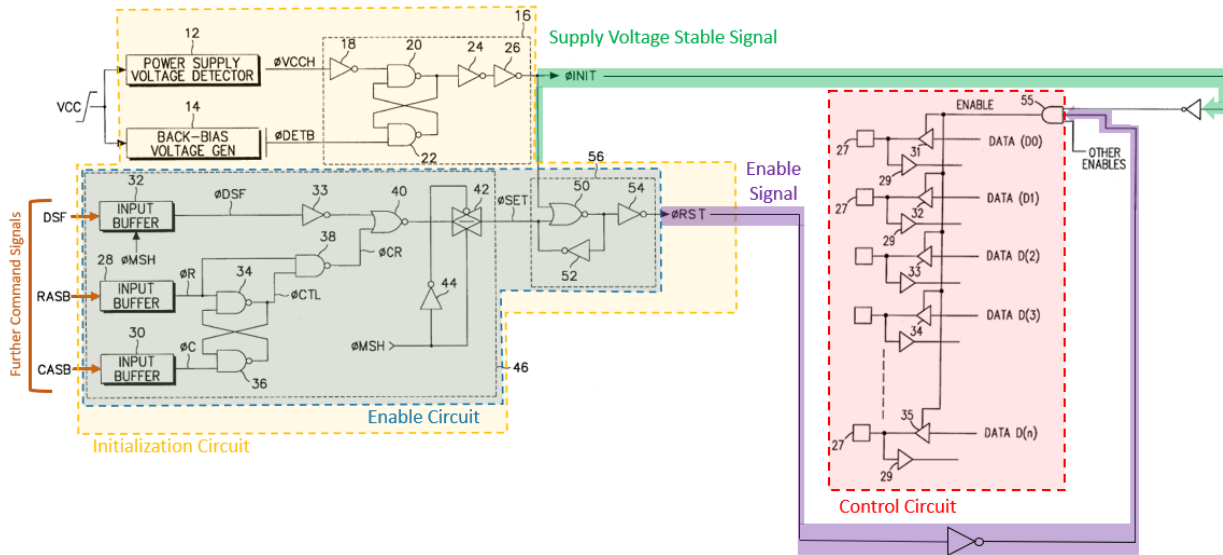
Furthermore, one of skill in the art would have been motivated to combine the teachings of Lee with the teachings of Kocis at least because the two references are directed to solving the same problem (*i.e.*, ensuring proper initialization and

power-up of a memory device in order to avoid malfunction). *See, e.g.*, EX1005 at 1:19-29, 2:4-23; EX1007 at 2:36-48, 2:60-64; EX1003, ¶178.

2. Claim [9]

Lee in combination with Kocis discloses a semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit. In particular, a POSITA would have understood to combine the output drivers of Kocis with the initialization circuitry of Lee. EX1003, ¶179. For reference, annotated combinations of Lee and Kocis under Interpretations 1 and 2 are provided below (*see* EX1005 at FIG. 3 and EX1004 at FIG 5)².

² In the combination there is an inverter between the ϕ RST signal and the middle pin of gate 55 since the ϕ RST signal is low to enable normal operation and the KEEP OFF# signal of Kocis is high to enable normal operation. EX1003, ¶179.



Kocis and Lee Combination

As shown in the annotated figure (above), a POSITA would have understood that disabling the output drivers until the enable conditions are met (*i.e.*, the proper initialization sequence has been performed) teaches latching the output drivers until the enable signal is generated by the enable circuit. EX1003, ¶180. The ϕRST signal is driven low after a predetermined proper initialization sequence of the externally applied further command signals (*i.e.*, Lee signals CASB, RASB, and DSF). “[I]f the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence, the first initialization signal generator activates the first initialization signal ϕSET . For this to occur, the reset control signals DSF, RASB, and CASB must be activated in the CBR (CAS before RAS) mode. The mode selection clock signal ϕDSF is first activated, *i.e.*, driven to a high-logic level. . . . If the first control signal CASB is then activated by being driven to a low

logic state, . . . [t]hen, if the second control signal RASB is driven to the active low logic level, . . . the first initialization signal ϕ SET [is activated] at the output terminal of NOR gate 40. . . . The transfer unit 56 combines the first initialization signal ϕ SET and the second initialization signal ϕ INIT and activates the reset signal ϕ RST by driving it to a high logic level.” EX1005 at 4:38-61.

Once the reset signal ϕ RST is driven to a low logic level, it unlatches the control circuit. *See* EX1004 at 5:8-12 (“The output of the AND gate 55 (which comprises the ENABLE signal), only is driven high if all input signals are high. Thus, tri-state buffers 31, 32, 33, 34, 35 are only enabled if all three input signals are high.”); *id.* at 5:22-28 (“Until the voltage supply has reached the threshold value (which will vary from circuit to circuit depending upon the proper operating voltage and other considerations), the AND gate 55 keeps the ENABLE line low, disabling the tri-state buffers 31, 32, 33, 34, 35, thus preventing possible buss contention during start-up or reset.”); *id.* at 2:3-8 (“When the buffer 13 is not enabled, the tri-state buffer 13 functions to ‘disconnect’ the data output line from the memory bus 11, so that neither a low or high signal is driven on the bus, and instead, the buffer presents a high impedance state thereby allowing other circuitry to determine the state of the bus.”).

Accordingly, Lee in combination with Kocis discloses a control circuit having output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit. EX1003, ¶¶179-82.

3. Claim [13]

For the same reasons discussed in Section X.G.2 with respect to claim element [9], Lee in combination with Kocis discloses claim [13].

H. Ground 8: Claims 9 and 13 are Obvious Over Lee in Combination with Iketani and Kocis

Lee in combination with Iketani and Kocis renders obvious claims 9 and 13 of the '589 Patent, with Lee and Iketani rendering obvious the limitations of independent Claims 1 and 11 from which they depend (*see* Section X.D.2, *supra*).

1. Combination of Lee, Iketani, and Kocis

For the reasons discussed in Section X.D.1 , a POSITA would have been motivated to combine the teachings of Lee and Iketani, and for the reasons discussed in Section X.G.1, a POSITA would have been further motivated to combine the teachings of Kocis into that Lee-Iketani combination.

2. Claims [9] and [13]

As discussed in Ground 4, to the extent the Patent Owner argues incorrectly that Lee does not disclose or render obvious the claimed control circuit, the combination of Lee and Iketani also discloses the claimed control circuit for controlling operations. *See* Section X.D.2 , *supra*. Otherwise, the combination of

Lee, Iketani, and Kocis discloses the claim elements of claims [9] and [13] for the same reasons as those disclosed in Ground 7. *See* Section X.G, *supra*.

XI. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION

A. *Fintiv* (Section 314(a))

The *Fintiv* factors favor institution. This petition presents compelling evidence showing the unpatentability of the challenged claims, and thus institution should not be discretionarily denied under *Fintiv*. Although there is a case pending with Xilinx involving the '589 Patent, it remains at an early stage. Initial discovery and contentions have been served, but the parties have not briefed or argued claim construction, and any final written decision will likely be issued before trial. The current trial date is November 18, 2024 and the median time-to-trial for the Delaware court suggests trial in February 2025. EX1014 at 12; EX1015 at 14. Further, Xilinx intends to request a stay in the case pending IPR. EX1016 (showing the Delaware court grants majority of motions to stay).

B. Section 325(d)

The Board should not exercise its discretion to deny institution under §325(d) because none of the references or arguments relied upon in this Petition were substantively considered by the Examiner. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-9 (2020)

(precedential) (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (2017) (precedential)). This Petition relies on new references—Kocis, JESD 21-C³, and Iketani, which were never before the Examiner. Furthermore, neither the Lee reference, nor an English translation of the Japanese priority document, was before the Examiner.

1. *Advanced Bionics*: Part 1

Petitioner acknowledges that Tetsuka, the Japanese counterpart to Lee which is relied upon herein, is cited on the face of the '589 Patent. EX1001 at [56]; EX1011. However, the Examiner (1) did not apply this reference (or its Lee counterpart) in any rejection, (2) did not evaluate the particular combinations of references with the Lee counterpart set forth in Grounds 4-8, and (3) was not provided with an English language translation of Tetsuka during prosecution. *See* generally EX1002. The references and arguments presented herein therefore do not overlap with references and arguments considered during prosecution. Accordingly, Petitioner submits that the first part of the *Advanced Bionics* framework is not satisfied.

³ The Background section of the '589 patent describes a “JEDEC standard” the applicant failed to disclose to the Office during prosecution. *See* EX1001 at 1:22-23, 1:43-46.

2. *Advanced Bionics*: Part 2

To the extent the Board determines an analysis under part 2 of *Advanced Bionics* is warranted, Petitioner submits that the asserted grounds demonstrate that the Examiner erred in the unlikely event he made any evaluation of the Japanese-language Tetsuka reference. Accordingly, Petitioner submits that the evidence and facts presented in the Petition warrant reconsideration of the prior art, and respectfully requests the Board decline to exercise its discretion to deny institution under §325(d).

XII. CONCLUSION

Accordingly, Petitioner requests *inter partes* review of claims 1, 2, and 8-13 pursuant to Grounds 1-8 set forth above.

Date: February 6, 2023

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Under the provisions of 37 C.F.R. §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,975 words, which is less than the 14,000 allowed under 37 C.F.R. §42.24(a)(1)(i).

/Brian W. Oaks/

Brian W. Oaks

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(a), the undersigned certifies that on February 6, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, cost prepaid, to the Patent Owner by serving the correspondence address of record and another address known to Petitioner as likely to effect service, as follows:

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Additionally, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were served via e-mail on:

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