

Filed on behalf of: Polaris Innovations Limited

By: David T. DeZern
Registration No. 60,117
NELSON BUMGARDNER CONROY P.C.
2727 N. Harwood Street, Suite 250
Dallas, TX 75201
Telephone: (214) 446-4950
Email: david@nelbum.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

Case IPR2023-00516

U.S. Patent 6,157,589

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	THE '589 PATENT AND THE CHALLENGED CLAIMS	3
	A. Overview of the '589 Patent.....	3
	B. Challenged Claims	9
III.	LEVEL OF ORDINARY SKILL	11
IV.	CLAIM CONSTRUCTION	11
V.	APPLICABLE LEGAL STANDARDS.....	12
	A. Anticipation	12
	B. Obviousness.....	13
	1. Claims cannot be found obvious if an element is absent.	14
	2. A petition must address the Graham factors.	15
	3. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.	15
VI.	SUMMARY OF THE PRIOR ART REFERENCES.....	16
	A. Overview of Primary Reference: Kocis	16
	B. Overview of Primary Reference: Lee	18
	C. Overview of Secondary References:	21
	1. JESD 21-C.....	21
	2. Iketani.....	23
VII.	THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS	24
	A. Ground 1: Kocis Does Not Disclose At Least One Limitation of Each Independent Claim.	24
	B. Ground 2: The Petition Fails to Demonstrate Obviousness Over Kocis in Combination with JESD 21-C for Claims 2, 8, 10, and 12.....	30
	C. Ground 3A/3B: Lee Does Not Disclose At Least One Limitation of Each Independent Claim.	32

D.	Ground 4: The Combination of Lee with Iketani Does Not Cure the Deficiencies of Lee.....	36
E.	Ground 5: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with JESD 21-C for Claims 2, 8, 10, and 12.....	37
F.	Ground 6: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Iketani and JESD 21-C for Claims 2, 8, 10, and 12.	38
G.	Ground 7: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Kocis for Claims 9 and 13.....	39
H.	Ground 8: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Iketani and Kocis for Claims 9 and 13.....	39
VIII.	PATENT OWNER’S FINAL COMMENTS	39
IX.	CONCLUSION.....	40

TABLE OF AUTHORITIES

Cases

<i>CFMT, Inc. v. YieldUp Int’l Corp.</i> , 349 F.3d 1333 (Fed. Cir. 2003)	14
<i>Continental Can Co. USA, Inc. v. Monsanto Co.</i> , 948 F.2d 1264 (Fed. Cir. 1991)	13
<i>Cook Inc. v. Medtronic Vascular, Inc.</i> , Case No. IPR2018-01570 (P.T.A.B. March 4, 2019).....	32, 35
<i>Eizo Corp. v. Barco N.V.</i> , Case No. IPR2014-00358 (P.T.A.B. 2014)	15
<i>EMC Corporation v. Intellectual Ventures I LLC</i> , Case No. IPR2017-00429 (P.T.A.B. 2017)	2
<i>Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC</i> , Case No. IPR2012-00001 (P.T.A.B. 2013)	14
<i>Graham v. John Deere Co.</i> , 383 U.S. 1 (1966).....	14, 15
<i>Hansgird v. Kemmer</i> , 102 F.2d 212 (CCPA 1939)	13
<i>In re Arkley</i> , 455 F.2d 586 (CCPA 1972)	12
<i>In re Kahn</i> , 441 F.3d 977 (Fed. Cir. 2006)	15
<i>In re Magnum Oil Tools Int’l Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016)	32, 35
<i>In re Oelrich</i> , 666 F.2d 578 (CCPA 1981)	13

<i>In re Rijckaert</i> , 9 F.3d 1531 (Fed. Cir. 1993)	14
<i>In re Royka</i> , 490 F.2d 981 (C.C.P.A. 1974)	14
<i>InTouch Techs., Inc. v. VGo Comm'ns., Inc.</i> , 751 F.3d 1327 (Fed. Cir. 2014)	14
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	14, 15
<i>LG Elecs., Inc. v. Cellular Commc'ns Equip. LLC</i> , Case No. IPR2016-00197 (P.T.A.B. 2016)	16
<i>N.V. v. Abbott Labs.</i> , 512 F.3d 1363 (Fed. Cir. 2008)	15
<i>Net MoneyIN, Inc. v. VeriSign, Inc.</i> , 545 F.3d 1359 (Fed. Cir. 2008)	13
<i>Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.</i> , 200 F.3d 795 (Fed. Cir. 1999)	12
<i>Wellman, Inc. v. Eastman Chem. Co.</i> , 642 F.3d 1355 (Fed. Cir. 2011)	11
<i>Xerox Corp. v. Bytemark, Inc.</i> , Case No. IPR2022-00624 (P.T.A.B. 2022).....	31

Statutes, Rules and Regulations

35 U.S.C. § 103	14
35 U.S.C. § 103(a)	13
35 U.S.C. § 313	1
37 C.F.R. § 42.107	1

37 C.F.R. § 42.108(c).....	12
----------------------------	----

Other Authorities

Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012)	12
---	----

I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Polaris Innovations Limited (“Patent Owner”) submits this Preliminary Response to Xilinx, Inc.’s (“Petitioner”) Petition for *Inter Partes* Review (“Petition,” Paper 2), challenging Claims 1, 2, and 8-13 of U.S. Patent 6,157,589 (the “’589 Patent”) (Ex. 1001).

The ’589 Patent concerns methods and circuitry for powering on dynamic random access memories (“DRAM”). The patent describes and claims particular circuitry and methods of operating such circuitry in order to initialize and unlatch a DRAM for operation.

Petitioner alleges invalidity on eight or nine different grounds (numbered one through eight including both 3A and 3B). The grounds are based on four different references in various combinations. Each of the primary references, Kocis and Lee¹, fail to disclose or teach at least one limitation of the independent claims. The other references fail to cure these deficiencies. Petitioner’s approach including the number of grounds, alternative readings of the same circuitry, assertion that both primary references are anticipating but also in need of numerous combinations to support

¹ The Japanese counterpart of Lee was considered by the Examiner during examination of the ’589 Patent. *See infra* Section VI.B.

obviousness, and the sheer number of words² expended indicate the weakness of Petitioner’s invalidity case. Petitioner picks and chooses circuits and signals from prior art related to DRAM and attempts to knit them together using the asserted claims as a roadmap. This is of course improper.

The two primary references fail to disclose key limitations of the independent claims. Kocis does not disclose any sequential logic like that described in the ’589 Patent’s specification and fails to disclose the independent claim’s requirements to generate an enable signal based on a predetermined sequence of command signals. Lee fails to disclose an enable signal that unlatches the control circuit for operation in a DRAM as required by the independent claims and instead describes a reset signal provided as a back up for initializing a circuit when prior art power signals malfunction. Petitioner’s attempts to overcome these flaws with conclusory assertions repeated by its expert are insufficient to meet its burden to show anticipation or obviousness, and the Board should not institute IPR.

² Petitioner’s certification under 37 C.F.R. § 42.24(d) asserts that the petition contains 13,975 words—25 less than the limit—while removing the space in exhibit cites (e.g., EX1001 of which there are 227), a practice to circumvent word limits that has been found to violate the Board’s rules. *See EMC Corporation v. Intellectual Ventures I LLC*, IPR2017-00429, Paper 11 at 27–29 (PTAB July 5, 2017) (“Petitioner’s use of atypical citations amounts to formatting tricks designed to avoid the word count limit for petitions set forth in our rules.”).

II. THE '589 PATENT AND THE CHALLENGED CLAIMS

A. Overview of the '589 Patent

The '589 Patent “relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device.” Ex. 1001 at 1:9-13. “The invention [] relates to a method for initializing such a dynamic semiconductor memory device, and [] the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device.” *Id.* at 1:16-21.

The '589 Patent explains that “during the switch-on operation (‘POWERUP’)” for “SDRAM semiconductor memories according to the JEDEC standard” “the internal control circuits” must be “held in a defined desired state, in order to prevent undesirable activation” “or uncontrolled activation.” *Id.* at 1:22-30. “The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory.” *Id.* at 1:30-35.

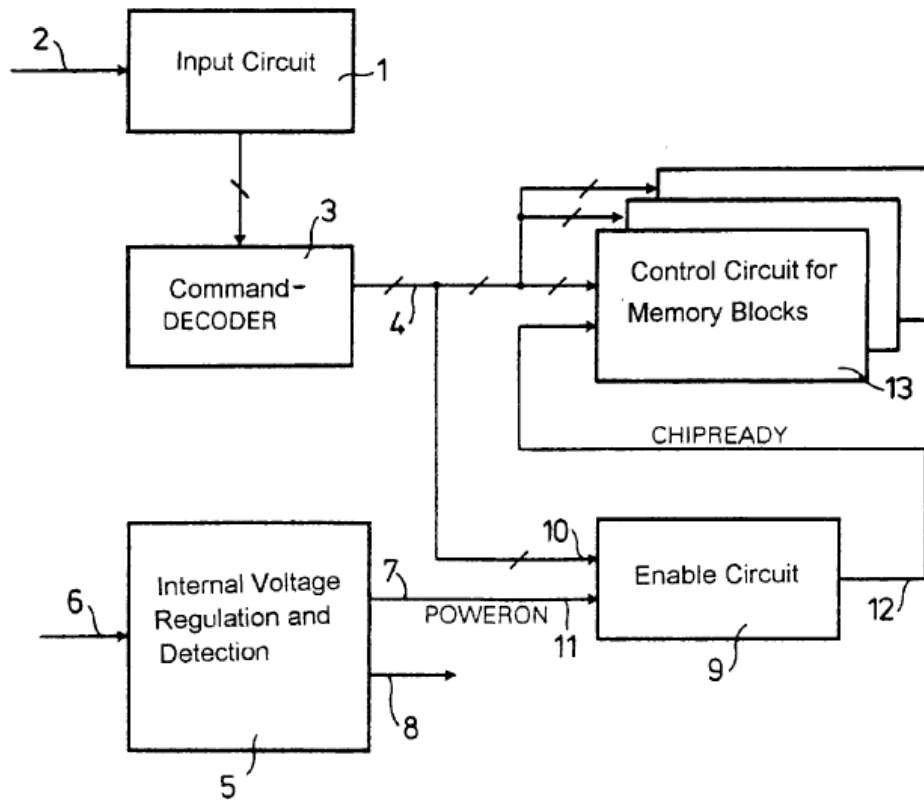
The '589 patent explains that “[a]ccording to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence.” *Id.* at Col. 1:35-38. “The

sequence consists of predetermined commands that must be applied in a defined chronological order.” *Id.* at Col. 1:38-40. The ’589 Patent provides an example of “a recommended initialization sequence” from the JEDEC standard. *Id.* at 1:43-61. The ’589 Patent explains that “[a]fter the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation.” *Id.* at Col. 1:62-65. “In the case of SDRAM semiconductor memory modules that have been disclosed to date,” all the control circuits of the component have been *unlatched* only with the POWERON signal.” *Id.* at Col. 1:65-2:1 (emphasis added). “The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component.” *Id.* at Col. 2:1-4.

The ’589 Patent addresses these issues by providing “an initialization circuit controlling a switching-on operation.” *Id.* at Col. 2:15-21. The initialization circuit includes an “enable circuit outputting an enable signal after a predetermined proper initialization sequence . . . and the enable signal effecting an unlatching of the control circuit.” *Id.* at Col. 2:20-28.

The ’589 Patent provides a block diagram of an initialization circuit according to the invention in Figure 1:

Fig 1



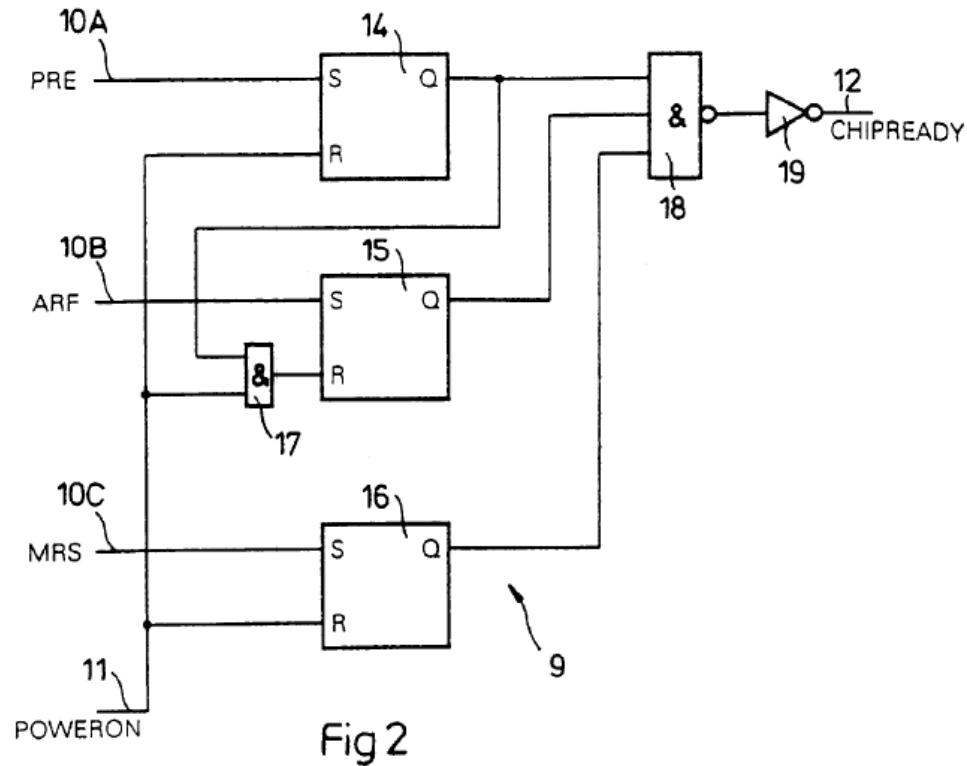
Ex. 1001, Fig. 1.

“The initialization circuit has an input circuit 1, to whose input 2 command and clock signals [] are externally applied.” *Id.* at 3:51-53. “The command and clock signals are amplified and conditioned before being received by a command decoder 3 . . . at whose output 4, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output.” *Id.* at 3:54-61. “The initialization circuit further has a

circuit 5 for internal voltage regulation and/or detection” which “has a first output 7 outputting a POWERON signal and a second output 8 supplying stabilized internal supply voltages.” *Id.* at 3:61-65.

The initialization circuit also has an enable circuit 9 that receives the command signals from command decoder 3 and the POWERON signal from the voltage regulation/detection circuit 5. *Id.* at 4:9-14. The enable circuit provides “[a]n enable signal CHIPREADY” “after the identification of a predetermined proper initialization sequence of the command signals.” *Id.* at Col. 4:14-18. “The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device.” *Id.* at Col. 4:18-20.

Figure 2 shows an exemplary embodiment of an enable circuit according to the invention:

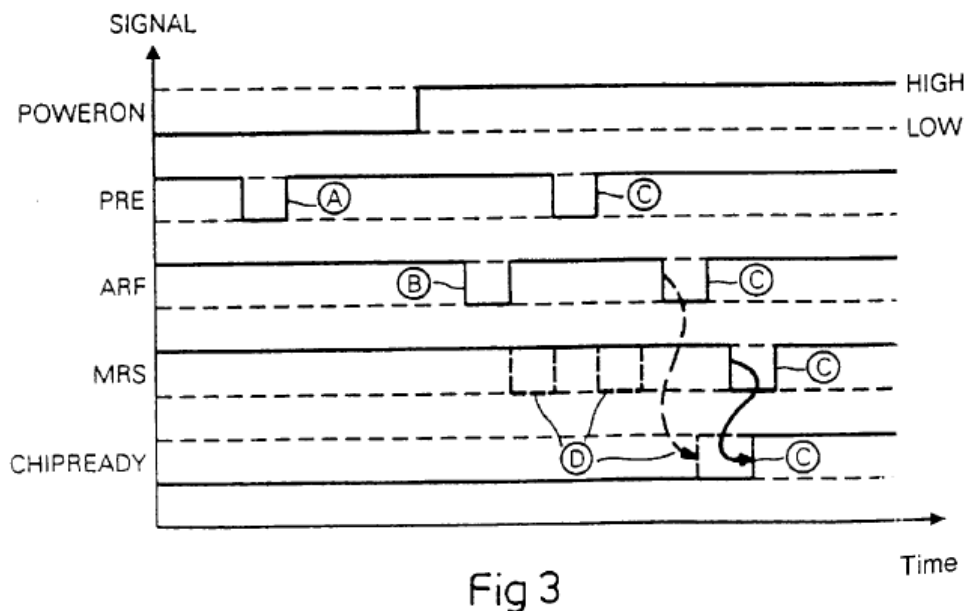


Ex. 1001, Fig. 2.

The enable circuit in Figure 2 contains three bistable multivibrator stages each with set and reset inputs. *Id.* at Col. 4:24-28. “The command signals PRE, ARF, MRS applied to the respective set inputs S” and “[t]he POWERON signal is applied directly to the reset inputs R.” *Id.* at Col. 4:37-48. With these connections and the additional logic described in Figure 2, “activation of the enable signal CHIPREADY at [] the output 12 . . . is generated *only* when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected.” *Id.* at Col. 4:49-55

(emphasis added). “Only then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY.” *Id.* at Col. 4:55-58.

The '589 Patent further illustrates the operation of the enable circuit in the schematic time sequence diagram of Figure 3. *Id.* at Col. 4:59-63.



Ex. 1001, Fig. 3.

The '589 Patent describes four potential sequences A through D and their results. *Id.* at 4:63-5:21. For example in case A, PRE activates before the POWERON and because “the proper initialization sequence requires a waiting time before the first command,” CHIPREADY does not activate. *Id.* at 4:63-5:1. In case B, “the chronological order of the activation of the signal AUTOREFRESH [ARF] . . . is incorrect since the proper initialization sequence prescribes a previous PRECHARGE [PRE] command.” *Id.* at 5:3-10. In case C, “a correct chronological

order of the commands PRECHARGE [PRE], AUTOREFRESH [ARF], MODE-REGISTER-SET [MRS] is present,” and therefore “an enable signal CHIPREADY at logic HIGH is now supplied.” *Id.* at Col. 5:10-16. Case D provides another conceivable sequence that is allowed in this example. *Id.* at Col. 5:15-21.

Based on these disclosed inventions, the ’589 Patent claims, inter alia, an apparatus and method for switching on, or unlatching the control circuits of (*see, e.g., id.* at Col. 4:18-20), a DRAM based on identification of an acceptable initialization sequence. The next section provides more detail regarding the specific claims at issue.

B. Challenged Claims

The Petition challenges claims 1, 2, and 8-13 of the ’589 Patent. *See* Petition at 3. Claims 1 and 11 are independent claims. Claims 2 and 8-10 depend from claim 1, and claims 12 and 13 depend from claim 1.

The independent claims are reproduced below with emphasis on the particular limitations that are at issue in this Preliminary Response:

Claim 1 recites:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation,

said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals,

said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

Claim 11 recites:

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

The emphasized limitations in each independent claim require that the claimed inventions, in accordance with the other requirements of each claim, output an enable signal after identifying a “proper initialization sequence” of “further command signals” and that enable signal “effecting an unlatching” of the control circuit. As addressed further herein, none of the Petitioner’s references disclose these limitations nor does the Petition articulate a motivation to modify any of the references to meet these limitations. Because the remaining challenged claims all depend from these independent claims, should the Board accept Patent Owner’s arguments that trial should not be instituted on these claims, it necessarily follows that trial should not be instituted on the dependent claims.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so in the event that trial is instituted.

IV. CLAIM CONSTRUCTION

Patent Owner submits that the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“need only be construed ‘to the extent necessary to resolve the controversy’”

(quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012) (“The Board ... may institute a trial where the petitioner establishes that the standards for instituting the requested trial are met”).

A. Anticipation

“[R]ejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in ‘the prior art. . . .’ The [prior art] reference must clearly and unequivocally disclose the claimed [invention] or direct those skilled in the art to the [invention] without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference.” *In re Arkley*, 455 F.2d 586, 587 (CCPA 1972). Thus, “unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same

way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

“To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.” *Continental Can Co. USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (citing *In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981)). “Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *Id.* at 1268–69 (quoting *Hansgirk v. Kemmer*, 102 F.2d 212, 214 (CCPA 1939)).

B. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established;

the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

Additionally, it is improper to use the challenged claim as a roadmap to piece together disparate disclosure using hindsight bias. *See InTouch Techs., Inc. v. VGo Comm’ns., Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (reversing obviousness where “[i]t appears that [the expert] relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of

the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”).

2. A petition must address the Graham factors.

Obviousness is resolved on a number of factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” *See Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying

one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

VI. SUMMARY OF THE PRIOR ART REFERENCES

Petitioner requests relief on eight or nine grounds. Petition at 3 (grounds 1 through 8 with 3A and 3B). The Kocis or Lee reference serves as the primary reference in each of these grounds, and the two references are used together for dependent claims in one ground (#7). *Id.* These two primary references and the other secondary references are summarized below.

A. Overview of Primary Reference: Kocis

Petitioner relies on U.S. Patent No. 5,559,753 to Kocis as the primary reference in Grounds 1 and 2, and the Petition combines Kocis with Lee in Ground 7. *See, e.g.*, Petition at 3. Kocis “relates to a system for preventing contention on the memory bus between conflicting data signals from two or more DRAM banks.” Ex. 1004 at Col. 1:12-15.

Kocis describes “a circuit for disabling DRAM data output signals, which counts the number of RAS (and/or CAS) signals received by the DRAM circuit.” *Id.*

at Col. 3:42-44. “When seven RAS signals have been detected after a threshold voltage is achieved, the DRAM data output lines are enabled.” *Id.* at 3:44-47.

Petitioner relies on Figure 5 which Kocis describes as “a circuit. . . for disabling DRAM data output drivers until power supply voltages are satisfactory and all enable conditions are met.” *Id.* at Col. 4:23-26.

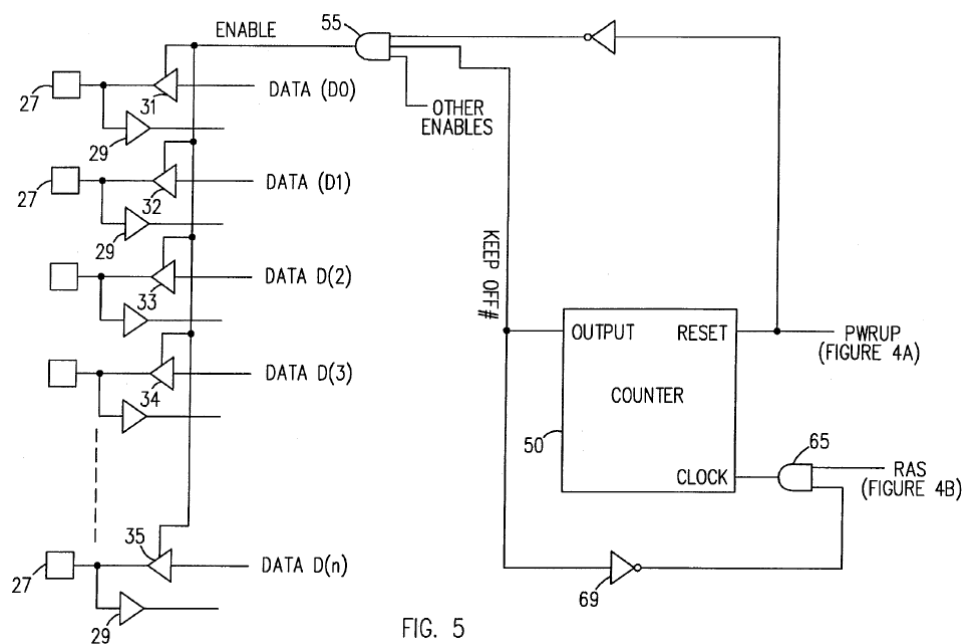


FIG. 5

Ex. 1004, Fig. 5.

Figure 5 includes “a plurality of tri-state output drivers 31, 32, 33, 34, 35 for driving data lines D0-Dn of a DRAM circuit 100, a counter 50, and an AND gate 55.” *Id.* at 4:33-38. “[T]he tri-state buffers transmit the associated data signal only when enabled by the ENABLE line” emanating from AND gate 55. *Id.* at 4:60-61. “The AND gate 55 receives the following input signals in the preferred embodiment: (1) an inverted Pwrup signal from the output of the voltage detection circuit of FIG. 4A;

(2) an output signal (Keep Off) from counter 50; and (3) other enable signals.” *Id.* at 5:3-7.

In Kocis’s preferred embodiment, “the counter 50 counts the number of RAS signals received from the memory controller 8 (of FIG. 1).” *Id.* at Col. 5:40-42. The counter generates “an output signal (Keep Off)” after counting a number of RAS and/or CAS signals. *Id.* at Col. 5:42-49. The “Keep Off” signal is supplied to AND gate 55 which also receives “an inverted Pwrap signal” and “other enable signals.” *Id.* at Col. 5:1-8. The tri-state buffers 31-35 are disabled while “AND gate 55 keeps the ENABLE line low.” *Id.* at Col. 5:22-28. Notably, for purposes of this Preliminary Response, neither the ENABLE signal nor the “Keep Off” signal is dependent on the sequence in which any other signals are received. The “Keep Off” signal counts the number of a particular signal, but not the sequence, and the sequence in which the AND gate 55 providing the ENABLE line (or any AND gate) receives its inputs does not have any effect on its output.

B. Overview of Primary Reference: Lee

Petitioner relies on U.S. Patent No. 5,774,402 to Lee as the primary reference in six or seven of the grounds it asserts (#3A/3B through 8). *See, e.g.*, Petition at 3. The Japanese counterpart to Lee (JP 9-106668 to Tetsuka) is cited on the face of the ’589 Patent and was marked as considered by the Examiner. *See* Petition at 73; Ex. 1002 at 75; 93-98.

Lee “relates generally to initialization circuits for semiconductor memory devices and more particularly to initialization circuits which operate in response to an external control signal, thereby *providing reliable initialization when conventional power supply reset circuits malfunction.*” Ex. 1005 at 1:11-16 (emphasis added).

Lee describes how “[t]he typical power on reset circuit operates by sensing the level of the power supply voltage VCC and generating an initialization signal for a predetermined length of time when the power supply voltage reaches a predetermined level.” *Id.* at 1:25-29; *see also id.* at 1:30-2:3. Lee identifies “[a] problem with” such a typical/prior art initialization circuit in “that it may malfunction if the power supply voltage VCC is unstable input.” *Id.* at Col. 2:4-6. In such an instance, the initialization circuit may “fail[] to initialize the circuits within the chip.” *Id.* at 2:12-14. To address this problem, Lee discloses “an object of the invention [is] to reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions.” *Id.* at 2:18-20. “A further object of the invention is to initialize a semiconductor memory device in response to external logic signals.” *Id.* at 2:21-23.

Lee discloses an initialization circuit in Figure 3 that includes both first (46) and second (16) initialization signal generators that generate signals ϕ SET and ϕ INIT, respectively. *Id.* at Col. 3:9-20.

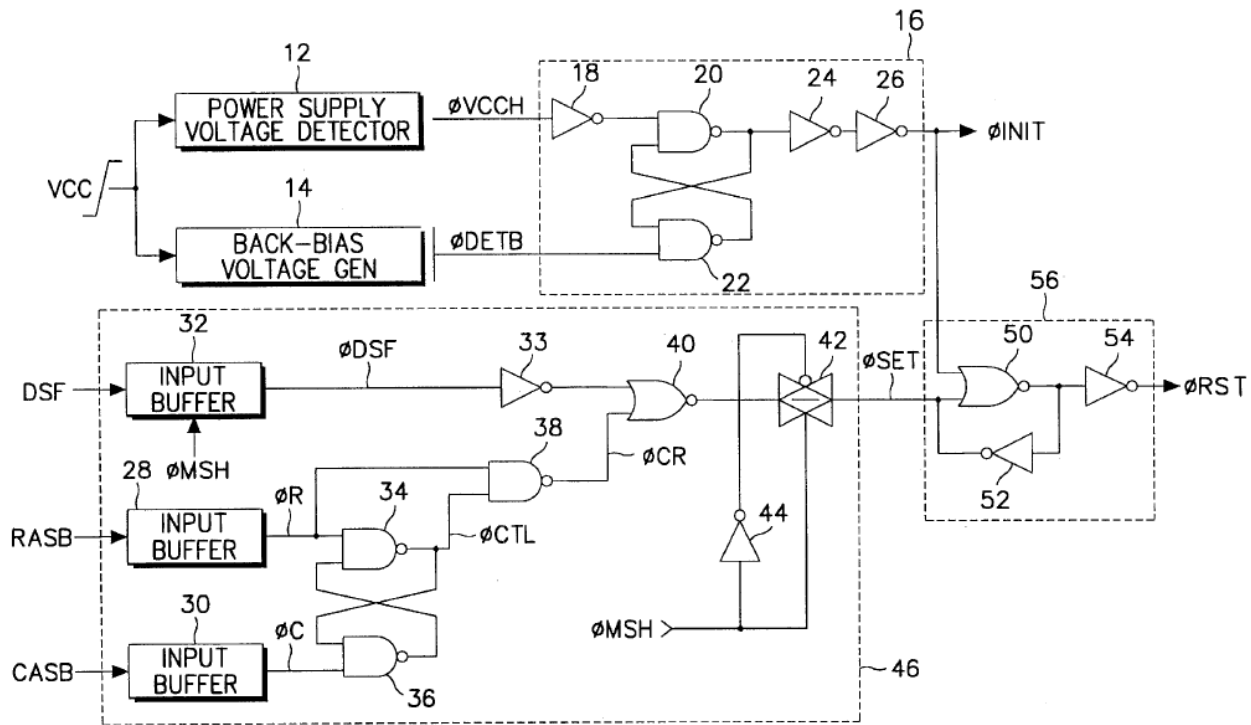


Fig. 3

Ex. 1005, Fig. 3.

“[T]he second initialization signal generator 16 activates the second initialization signal ϕINIT ” “[w]hen the power supply VCC is first powered-up” as in a typical power on reset circuit described in the background. *Id.* at Col. 4:25-31. “[T]he first initialization signal generator activates the first initialization signal ϕSET ” “if the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence.” *Id.* at Col. 4:38-41.

The outputs of the two initialization signal generators (16 and 46) are connected to transfer unit 56. *Id.* at Col. 4:14-20. “[T]he transfer unit 56 activates the reset signal ϕRST in response to the activation of either the first or second

initialization signals ϕ SET or ϕ INIT.” *Id.* at Col. 3:24-26; *see also id.* at Col. 3:31-33 (“the reset signal ϕ RST is activated in response to either the power supply power-up or the reset information.”). The “reset signal ϕ RST [is] for resetting a circuit within the memory device.” *Id.* at Col. 3:20-21. “Therefore, if the power-up reset circuit [providing the second initialization signal ϕ INIT] malfunctions, the circuitry will still be properly initialized by the first initialization signal ϕ SET.” *Id.* at Col. 3:33-35.

In this way, Lee discloses an initialization circuit that addresses the problem it identifies in the prior art—the need for reliable initialization when a conventional power supply reset circuit malfunctions. *See, e.g., id.* at 1:11-16; 2:4-14. As described above, the circuit in Lee generates a reset signal ϕ RST to initialize the circuit either based on activation of a conventional power-up circuit or in response to external logic signals. Notably, for purposes of this Preliminary Response, Lee does not disclose an enable signal that effects the unlatching of any control circuit.

C. Overview of Secondary References:

Petitioner relies on two additional prior art references in addition to its primary references. A brief description of each follows.

1. JESD 21-C

Petitioner relies on JEDEC’s Configurations for Solid State Memories, Standard No. 21-C, Release 7 (JESD 21-C) for its “recommended power on

sequence.” Ex. 1006 at 3.11.5-9 (p.483 of PDF). JESD 21-C explains that “both system and device designers *should strive* toward ensuring a High-Z output state during the initial power up sequence” and offers a “recommended power on sequence” to achieve that end. *Id.* (emphasis added).

JESD 21-C does not disclose any circuit or method for achieving this recommended power up sequence, nor does Petitioner allege that it does. The ’589 Patent describes a JEDEC recommended sequence (*see* Ex. 1001 at Col. 1:43-61) in the same paragraph that explains that achieving JEDEC’s goals for switch-on operation “turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory.” *Id.* at Col. 1:22-35.

JESD 21-C also includes in its “recommended power on sequence” that “[t]he device is now in the IDLE state and is ready for normal operation.” Ex. 1006 at 3.11.5-9 (p.483 of PDF). This mirrors the acknowledgement in the ’589 Patent that “[a]fter the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and *prepared for proper operation.*” Ex. 1001 at Col. 1:62-65 (emphasis added). The ’589 Patent notes further, however, that in SDRAM modules “disclosed to date all the control circuits of the component have been *unlatched* only with the

POWERON signal.” *Id.* at 1:65-2:1 (emphasis added). The JESD 21-C reference includes no recommendation for unlatching the control circuits after placing them in the IDLE state, and the Petitioner identifies none. This distinction will be elucidated further below with regard to the ’589 Patent’s claimed enable signal and other reset or initialization signals identified by Petitioner.

2. Iketani

Petitioner relies on U.S. Patent No. 5,703,510 to Iketani et al. as allegedly “illustrat[ing] and describe[ing] in detail the various circuits, including the control circuit, that receive and are initialized by [] an initialization signal.” *See, e.g.*, Petition at 59. Iketani “relates to a power on reset circuit.” Ex. 1007 at Col. 1:7.

Iketani is concerned with the problem caused “if the power supply voltage Vdd fluctuates significantly, it may possibly activate the power on reset signal /POR to the L level again even after initialization.” *Id.* at 1:59-62. To that end, Iketani describes various structures for generating a power on reset signal. *Id. generally.*

Iketani mentions “a control circuit 62 for controlling internal circuitry in response to a row address strobe signal RAS, a column address strobe signal CAS, an output enable signal OE, a write enable signal WE or the like” which can be “initialized in response to the power on reset signal.” *Id.* at Col. 5:12-15, 5:20-25. But, notably for purposes of this Preliminary Response, Iketani does not disclose

that the power on reset signal unlatches this control circuit for operation. Rather, it explicitly mentions other signals identified as an output or write “enable signal” provided to this control circuit from elsewhere.

VII. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS

To justify the institution of an *inter partes* review, a petitioner must establish that there is a “reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Petitioner has not met its burden of establishing a reasonable likelihood of success at least because the Petition fails to show that each limitation of the challenged claims is disclosed or taught by the asserted prior art references of each ground. Consequently, the Board should deny the Petition and decline to institute the *inter partes* review.

A. Ground 1: Kocis Does Not Disclose At Least One Limitation of Each Independent Claim.

Kocis at least fails to disclose the requirements of independent claims 1 and 11 that an enable signal is output after a predetermined proper initialization *sequence* of *further command signals*. Petitioner’s anticipation argument in Ground 1, therefore, fails.

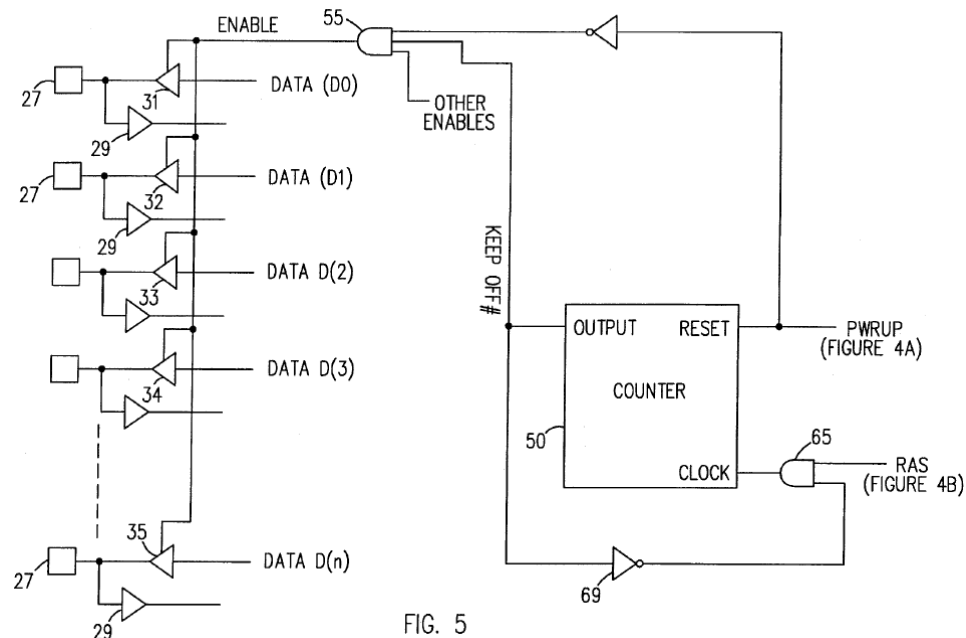
Claim 1 requires:

. . . enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified

Claim 11 requires:

... supplying, via an enable circuit ... , an enable signal, ... after an identification of a predetermined proper initialization sequence of the further command signals

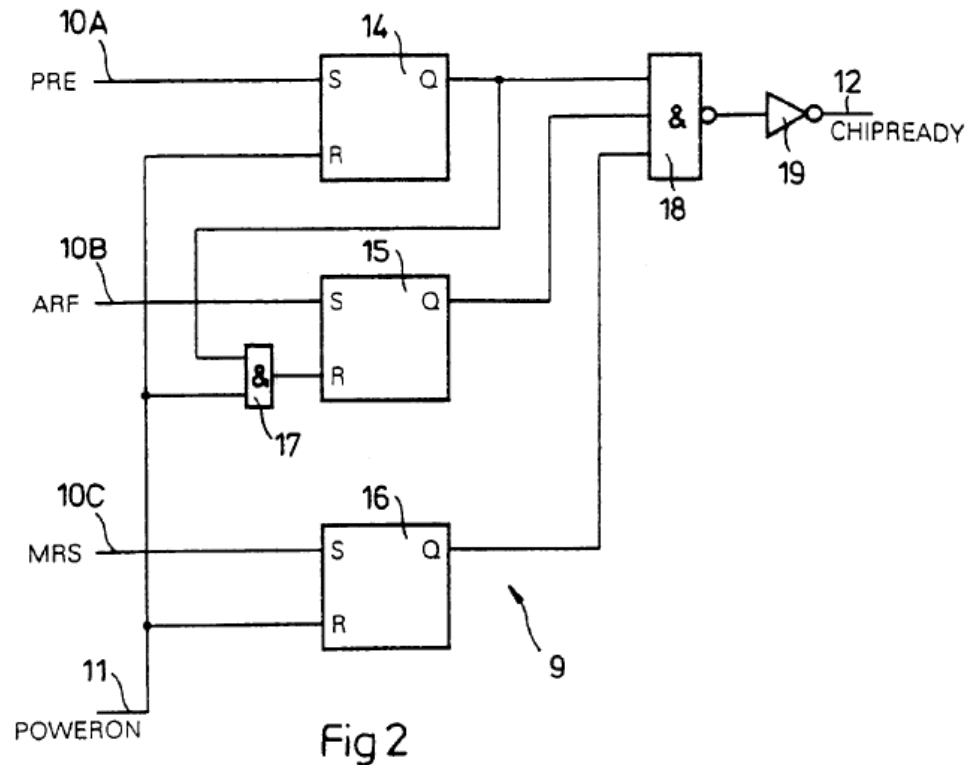
Petitioner identifies either the ENABLE signal or the “Keep Off” signal in Figure 5 of Kocis as the claimed enable signal. Petition at 30 n.1.



Ex. 1004, Fig. 5.

For the “Keep Off” signal, Petitioner asserts that it is “only output after a predetermined proper initialization sequence of the externally applied further command signals (i.e., Kocis RAS signal),” but then acknowledges that the counter 50 in Kocis in fact counts the number of RAS signals received and not any sequence of this one signal. Petition at 31.

As explained in the '589 patent with respect to the exemplary embodiment, the enable circuit in Figure 2 includes three bistable multivibrator stages that receive the command signals PRE, ARF, and MRS, respectively. Ex. 1001 at Col. 4:24-28; 4:37-48.



Ex. 1001, Fig. 2.

The '589 Patent explains that “activation of the enable signal CHIPREADY at [] the output 12 . . . is generated *only* when a predetermined *chronological* initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected.” *Id.* at Col. 4:49-55 (emphasis added). The '589 Patent further illustrates the operation of the enable

circuit in the time sequence diagram of Figure 3 where it provides example case B in which “the chronological order of the activation of the signal AUTOREFRESH [ARF] . . . is incorrect since the proper initialization sequence prescribes a previous PRECHARGE [PRE] command.” *Id.* at 5:3-10.

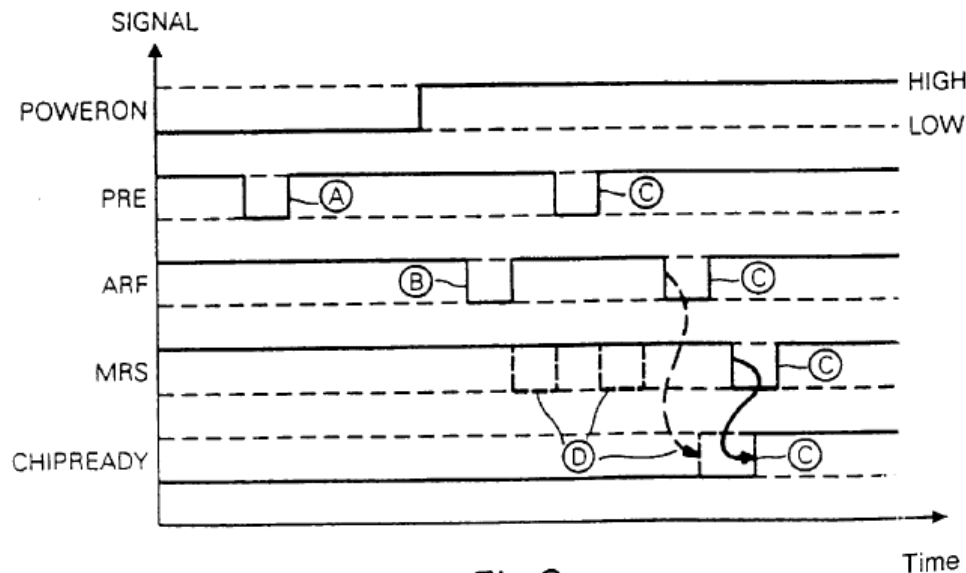


Fig 3

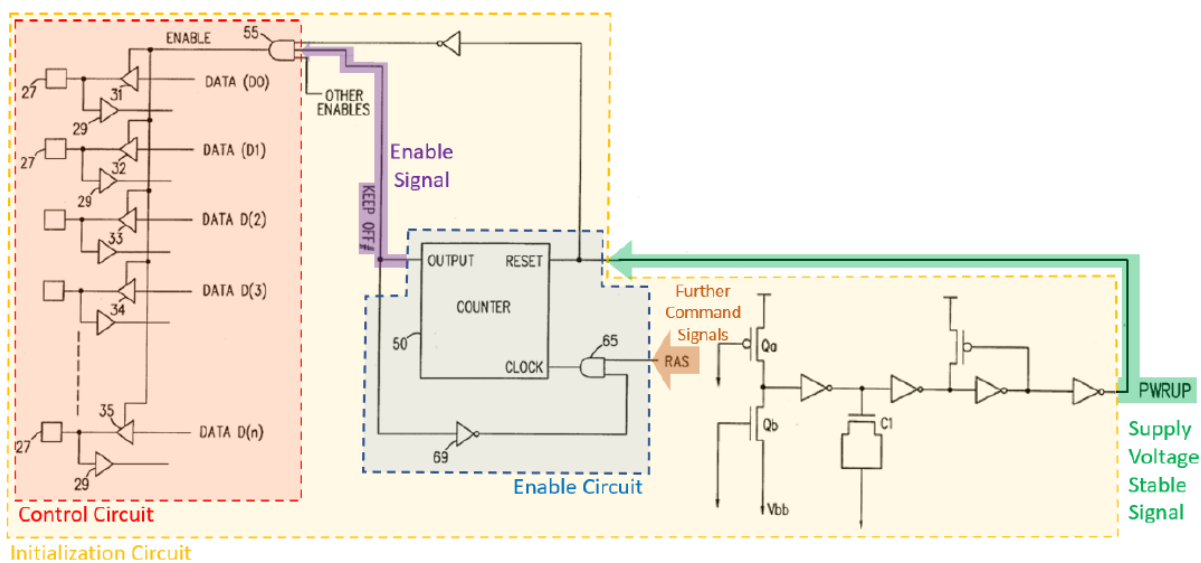
Ex. 1001, Fig. 3.

Thus, as shown in Figure 3, “[t]he signal swing of the AUTOREFRESH signal to logic LOW according to case situation B is therefore [] ignored, and the enable signal does not go to logic HIGH. *Id.* at Col. 5:7-10.

Kocis’ “Keep Off” signal does not disclose the claimed “enable signal” of the ’589 Patent because it is not output based on identification of any “predetermined proper initialization sequence of the [externally applied] further command signals.” *See supra* Section.II.B (Cls. 1 and 11 (bracketed material in Cl.

1 only)). It instead counts the number of RAS signal rather than identify a sequence of multiple command signals.

Including the PWRUP signal in Kocis does not solve Petitioner's inability to identify a sequence of further command signals. Although Petitioner clearly states that the further command signals are "i.e., Kocis RAS signal" as quoted above, in the next paragraph Petitioner asserts that "unless PWRUP (green) and RAS (brown) signals are input in the correct initialization sequence, the enable circuit (blue) will not output the enable signal (purple)." Petition at 31 (referencing annotated figure provided below).



EX1004 (Kocis) at Figures 4A and 5 (annotated)

Petition at 31.

Petitioner identifies the "PWRUP" signal in Kocis as the claimed "supply voltage stable signal" of the asserted claims. See Petition at 25; see also Petitioner's

annotated figure above. Claims 1 and 11 of the '589 Patent, however, distinguish between the “supply voltage stable signal” and “further command signals,” with the latter being the basis for the “proper initialization sequence.” Specifically:

Claim 1 requires:

. . . said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the *supply voltage stable signal* and externally applied *further command signals*, . . .

. . . enable circuit outputting an enable signal after a predetermined proper initialization sequence of *the* externally applied *further command signals* being identified

Claim 11 requires:

. . . the initialization circuit receiving the *supply voltage stable signal* and *further command signals*. . .

. . . supplying, via an enable circuit . . . , an enable signal, . . . after an identification of a predetermined proper initialization sequence of *the further command signals*

Whichever reading of Kocis Petitioner is arguing (Petition at 31), Kocis does not disclose the “Keep Off” signal being generated based on any sequence of further command signals.

The ENABLE signal emanating from AND gate 55 in Figure 5 of Kocis also does not disclose the claimed “enable signal” of the '589 Patent. *See* Petition at 30 n.1 (asserting alternative argument). None of the inputs to AND gate 55 are

generated based on a predetermined proper initialization sequence of further command signals for the same reasons explained above. Moreover, the output of an AND gate does not depend on the sequence in which its inputs are received—when all the inputs are high, its output is high, otherwise not. Petitioner’s expert provides no more explanation than its conclusory footnote alleging this alternate theory. *See* Ex. 1003 at ¶82. Petitioner’s alternative reading of Kocis likewise does not disclose these limitations.

Because Petitioner fails to show that Kocis discloses all of the limitations of the independent claims, Kocis cannot anticipate claim 1 or 11 of the ’589 Patent or the claims that depend from them.

B. Ground 2: The Petition Fails to Demonstrate Obviousness Over Kocis in Combination with JESD 21-C for Claims 2, 8, 10, and 12.

Petitioner’s proposed combination of Kocis with JESD-21C fails to address any of the deficiencies in Kocis identified in the previous section for Ground 1. Because each of these dependent claims depends from independent claim 1 or 11, Petitioner’s asserted combination fails to render these claims obvious for the same reasons addressed above for Ground 1.

Petitioner’s conclusory obviousness assertions in Ground 2 highlight the deficiencies of Kocis. Petitioner asserts that “JESD 21-C provides various standardized signals, timing diagrams, and other specifications for solid state memory” including “a power-up sequence.” Petition at 37. Petitioner does not

assert that JESD 21-C discloses any circuitry or method for achieving any power-up sequence. Instead, Petitioner asserts that “the series of RAS command signals disclosed in Kocis as causing the counter 50 to output the Keep Off signal to effect initialization of the memory circuitry would be replaced in the combination by the series of command signals disclosed in JESD 21-C to be used for initializing memory.” Petition at 38. Petitioner describes this as a “a simple substitution of the signals and timing of Kocis with the signals and timing specified in JESD 21-C.” *Id.*

Petitioner does not explain how the counter of Kocis, which counts the number of times that one signal is received as discussed above, could be modified to identify a sequence of multiple signals and account for their timing. Petitioner’s expert declaration is equally conclusory and asserts the same arguments as the petition. *See* Ex. 1003 at ¶¶94-96. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-16 (P.T.A.B. Aug. 24, 2022) (precedential) (rejecting expert testimony when “the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.”).

Petitioner cannot rely on conclusory assertions to modify the single counter disclosed in Kocis into circuitry like that described in the ’589 Patent directed to the detection of sequential input of multiple signals. *See, e.g., Cook Inc. v.*

Medtronic Vascular, Inc., IPR2018-01570, Paper 7 at 17 (P.T.A.B. March 4, 2019) (denying institution because Petitioner’s reasoning is premised on an unsupportable assertion never mentioned in the actual reference itself); *In re Magnum Oil Tools Int’l Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements” and “must instead articulate specific reasoning, based on evidence of record . . .”).

Because Petitioner fails to show that Kocis in combination with JESD 21-C discloses all of the limitations of these claims (including the claims from which they depend), this combination fails to render these claims obvious.

C. Ground 3A/3B: Lee Does Not Disclose At Least One Limitation of Each Independent Claim.

Lee at least fails to disclose the requirements of independent claims 1 and 11 that require output of an enable signal that effects an unlatching of a control circuit. Lee, therefore, cannot anticipate or render obvious these claims, and Grounds 3A and 3B must fail.

Claim 1 requires:

. . . said enable circuit outputting an enable signal . . . and the enable signal effecting an unlatching of said control circuit.

Claim 11 requires:

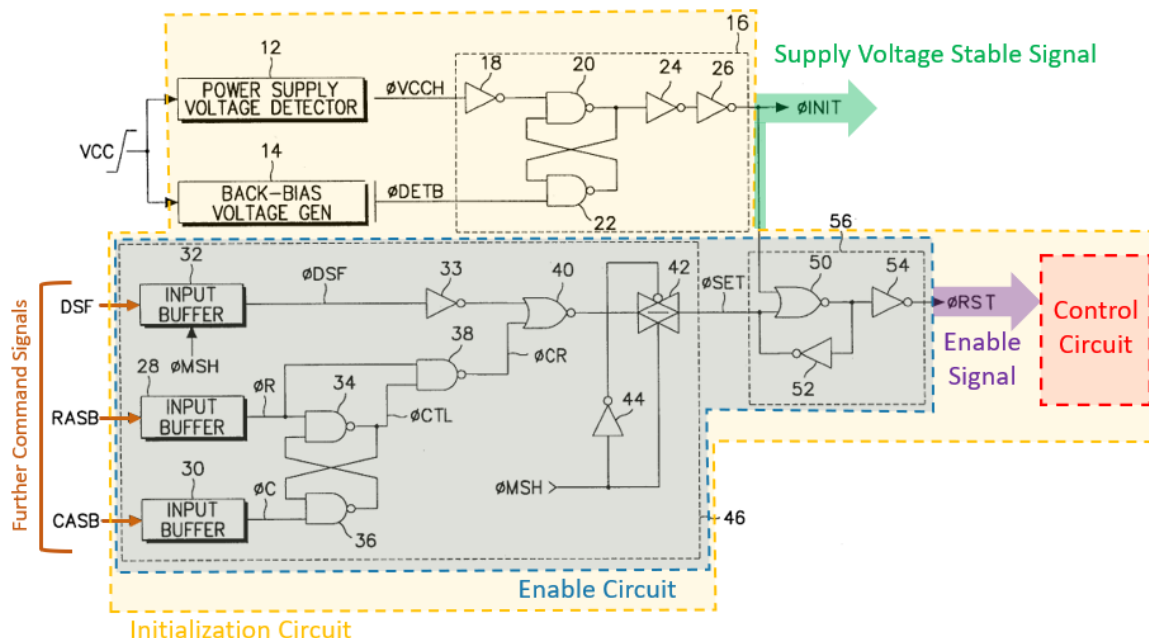
. . . supplying, via an enable circuit of the initialization circuit, an enable signal, . . . and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

Lee discloses no control circuit as claimed (which the Petition seems to admit), and more particularly provides no disclosure of any signal for “unlatching” any control circuit for controlling operation. Lee instead discloses a circuit for *initializing* circuits “*thereby providing reliable initialization when conventional power supply reset circuits malfunction.*” Ex. 1005 at 1:11-16 (emphasis added).

Lee identifies the problem it seeks to address as power on reset circuits “failing to initialize the circuits within the chip.” *Id.* at Col. 1:25-29, 2:12-14. Lee accordingly describes the object of its invention being “to reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions” and to do so “in response to external logic signals” rather than relying only on the power supply signal. *Id.* at Col. 2:18-23. To that end, Lee discloses circuitry for generating “a reset signal ϕ RST for resetting a circuit within the memory device” as summarized above in Section.VI.B. *Id.* at Col. 3:20-21. Lee, however, contains no disclosure that this reset signal, when it is activated or deactivated, unlatches any control circuit for normal operation.

Petitioner appears to acknowledge the absence of any control circuit unlatched for operation when Petitioner adds this component to the reference.

Throughout the Petition, Petitioner includes the annotated figure below where Petitioner purports to add the claimed “control circuit” to the disclosure of Lee:



EX1005 (Lee) at Figure 3 (annotated)

Petition at 51.

Petitioner has to not only add a “control circuit” to the Lee reference, but Petitioner also ascribes functionality based on Lee’s reset signal ϕRST that finds no support in the reference. For example, Petitioner quotes numerous passages from Lee in support of its contention that “Lee additionally teaches to a POSITA or, in the alternative, renders obvious a control circuit for controlling operations.” Petition at 53. But, every quoted reference refers only to the reset signal ϕRST causing “a circuit to be initialized,” “initializing the circuits,” “resetting a circuit,” “held in the initialized state,” or “resetting the various functional circuits.” *Id.*

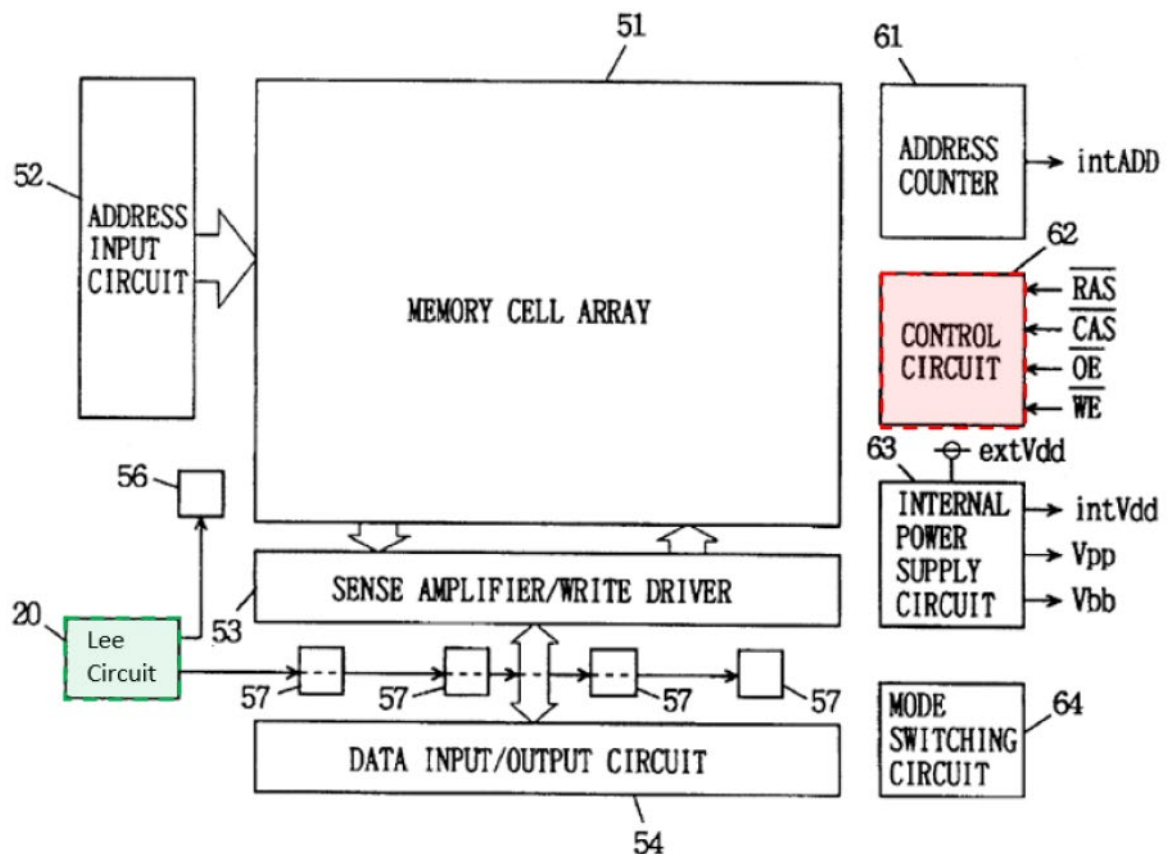
Initializing a circuit does not disclose unlatching the control circuit for normal operation. Petitioner asserts that “[a] POSITA would have understood that initializing the circuit within the chip, followed by deactivating the reset signal, as is disclosed in Lee, teaches unlatching the control circuit because it causes the start of normal operation of the buffers.” Petition at 57. Petitioner’s support for this contention is its expert’s verbatim assertion of the same. *See* Ex. 1003 at ¶133. Lee describes no such use or functionality of the reset signal.

Petitioner and its expert’s conclusory assertions are insufficient to fill in Lee’s disclosure of the functionality and use of its reset signal. *See Cook Inc. v. Medtronic Vascular, Inc.*, IPR2018-01570, Paper 7 at 17 (P.T.A.B. March 4, 2019) (denying institution because Petitioner’s reasoning is premised on an unsupportable assertion never mentioned in the actual reference itself); *In re Magnum Oil Tools Int’l Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements” and “must instead articulate specific reasoning, based on evidence of record . . .”). The reset signal in Lee does not disclose an “enable signal effecting an unlatching of [said/a] control circuit” as required by the independent claims. *See* Ex. 1001, Cls. 1 and 11. Thus, Lee cannot anticipate the claims of the ’589 Patent, and Petitioner has failed to demonstrate that it would render them obvious.

D. Ground 4: The Combination of Lee with Iketani Does Not Cure the Deficiencies of Lee.

Petitioner proposes combining Lee with Iketani to address the issues discussed in the preceding section—that Lee fails to disclose unlatching a control circuit for operation in response to an enable signal. But, even Petitioner’s proposed substitution of these references fails to cure this deficiency.

Petitioner proposes substituting the circuits disclosed in Lee for the power on reset circuit in Iketani as shown below:



EX1007 (Iketani) at Figure 6 (annotated)

Petition at 60.

Iketani discloses that the control circuit 62 in Figure 6 is “*initialized* in response to the power on reset signal” that Petitioner seeks to replace with Lee’s reset signal. Ex. 1007 at Col. 5:20-25 (emphasis added). Like Lee, the initialization of the control circuit as described in Iketani fails to disclose that the control circuit is unlatched for operation. Moreover, Iketani specifically refers to other enable signals, not provided by the power on reset circuit to be replaced by Lee, to which the control circuit responds. *See* Ex. 1007 at Col. 5:12-15 (referencing output enable signal $\overline{\text{OE}}$ and write enable signal $\overline{\text{WE}}$, shown in Figure 6 of Iketani as being supplied to the control circuit from elsewhere).

Like Lee by itself, the combination of Lee and Iketani does not disclose an “enable signal effecting an unlatching of [said/a] control circuit” as required by the independent claims. *See* Ex. 1001, Cls. 1 and 11. Because Iketani fails to disclose these limitations of the asserted claims lacking in Lee, Petitioner’s proposed combination fails to demonstrate that either of the independent claims is obvious.

E. Ground 5: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with JESD 21-C for Claims 2, 8, 10, and 12.

Petitioner’s proposed combination of Lee with JESD-21C fails to address any of the deficiencies in Lee for the independent claims identified for Grounds 3A and 3B above. Because each of these dependent claims depends from independent

claim 1 or 11, Petitioner's asserted combination fails to render these claims obvious for the same reasons addressed above.

Specifically, as noted in Grounds 3A and 3B, Lee's reset signal fails to disclose an "enable signal effecting an unlatching of [said/a] control circuit" as required by the independent claims. *See* Ex. 1001, Cls. 1 and 11. Likewise, the recommended power on sequence in JESD 21-C concludes with a recommendation that "the device is now in the IDLE state and is ready for normal operation." Ex. 1006 at 3.11.5-9 (p.483 of PDF). The '589 Patent distinguishes between such an initialized state and unlatching of a control circuit for proper operation. *Compare* Ex. 1001 at Col. 1:62-65 *with* 1:65-2:1. Thus, the addition of JESD 21-C fails to cure the deficiency of Lee, and Petitioner's proposed combination fails to demonstrate that these claims are obvious.

F. Ground 6: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Iketani and JESD 21-C for Claims 2, 8, 10, and 12.

Petitioner's proposed combination of Lee with Iketani and JESD-21C fails to address any of the deficiencies in Lee identified for Grounds 3A and 3B, or in the combination of Lee and Iketani identified for Ground 4. Because each of these dependent claims depends from independent claim 1 or 11, Petitioner's asserted combination fails to render these claims obvious for the same reasons addressed above.

G. Ground 7: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Kocis for Claims 9 and 13.

Petitioner's proposed combination of Lee with Kocis fails to address any of the deficiencies in Lee identified for Grounds 3A and 3B. Ground 7 relies entirely on Lee and cross-references its argument for the independent claims. Petition at 66. Because each of these dependent claims depends from independent claim 1 or 11, Petitioner's asserted combination fails to render these claims obvious for the same reasons addressed above.

H. Ground 8: The Petition Fails to Demonstrate Obviousness Over Lee in Combination with Iketani and Kocis for Claims 9 and 13.

Petitioner's proposed combination of Lee with Iketani and Kocis fails to address any of the deficiencies in Lee identified for Grounds 3A and 3B, or in the combination of Lee and Iketani identified for Ground 4. Ground 7 relies entirely on the combination of Lee Iketani, and cross-references its argument for the independent claims. Petition at 71. Because each of these dependent claims depends from independent claim 1 or 11, Petitioner's asserted combination fails to render these claims obvious for the same reasons addressed above.

VIII. PATENT OWNER'S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the

Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute *inter partes* review of the '589 patent.

Dated: June 21, 2023

By: /s/David T. DeZern
David T. DeZern
Registration No. 60,117
NELSON BUMGARDNER
CONROY P.C.
2727 N. Harwood Street, Suite 250
Dallas, TX 75201
Telephone: (214) 446-4950
Email: david@nelbum.com

Attorney for Patent Owner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 7,656 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Dated: June 21, 2023

By: /s/David T. DeZern
David T. DeZern
Registration No. 60,117
NELSON BUMGARDNER
CONROY P.C.
2727 N. Harwood Street, Suite 250
Dallas, TX 75201
Telephone: (214) 446-4950
Email: david@nelbum.com
Attorney for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on June 21, 2023, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

Email: xilinxMWETeam@mwe.com

Dated: June 21, 2023

By: /s/David T. DeZern
David T. DeZern
Registration No. 60,117
NELSON BUMGARDNER
CONROY P.C.
2727 N. Harwood Street, Suite 250
Dallas, TX 75201
Telephone: (214) 446-4950
Email: david@nelbum.com

Attorney for Patent Owner