

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2023-00516
Patent 6,157,589

Before JEAN R. HOMERE, BARBARA A. PARVIS, and MINN CHUNG,
Administrative Patent Judges.

CHUNG, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Xilinx, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1, 2, and 8–13 (the “challenged claims”) of U.S. Patent No. 6,157,589 (Ex. 1001, “the ’589 patent”). Polaris Innovations Limited (“Patent Owner”) timely filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), institution of an *inter partes* review is authorized when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Taking into account the arguments and evidence presented in Patent Owner’s Preliminary Response, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one challenged claim. Accordingly, we institute an *inter partes* review of all challenged claims of the ’589 patent, based on all grounds raised in the Petition.

II. BACKGROUND

A. Related Matters

According to the parties, the ’589 patent is involved in the following proceeding: *Polaris Innovations Ltd. v. Xilinx, Inc.*, No. 1:22-cv-00174-RGA (D. Del.). Pet. 1; Paper 3, 2. Patent Owner further states that the ’589 patent is also the subject of *Polaris Innovations Limited v. Broadcom, Inc.*, No. 2:22-cv-00347 (E.D. Tex.). Paper 10, 2–3.

B. Real Parties-in-Interest

Petitioner identifies itself, Advanced Micro Devices, Inc., and ATI Technologies ULC as the real parties-in-interest. Pet. 1. Patent Owner identifies itself, Wi-LAN Inc., Owlpoint IP Opportunities JVF LP, and Quarterhill Inc. as the real parties-in-interest. Paper 10, 2.

C. The '589 Patent

The '589 patent issued December 5, 2000 from U.S. Patent Application No. 09/343,431, filed June 30, 1999. Ex. 1001, codes (21), (22), (45).

The '589 patent describes an initialization circuit for a dynamic semiconductor memory device ("DRAM"). *Id.* at 1:10–13, Abstract. As background, the '589 patent describes that for proper operation of a semiconductor memory device,

it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits . . . are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data contention") or uncontrolled activation of internal current loads.

Id. at 1:23–30. According to the '589 patent, "[t]he solution to the problem turns out to be difficult" due to "a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory." *Id.* at 1:30–35. The '589 patent describes that, to address this problem, the JEDEC standard for dynamic semiconductor memories specified that a predetermined initialization sequence of commands—e.g., a sequence comprising PRECHARGE, AUTOREFRESH, and

MODE-REGISTER-SET commands—must be applied in a defined chronological order before proper operation of the control circuits is allowed. *Id.* at 1:35–61. According to the '589 patent, “[a]fter the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state . . . and prepared for proper operation”—i.e., “all the control circuits of the component have been unlatched.” *Id.* at 1:62–67.

Against this backdrop, the '589 patent describes embodiments of a DRAM initialization circuit that contains a control circuit for controlling operations and an enable circuit that outputs an enable signal after identifying a predetermined proper initialization sequence of externally applied further command signals, the enable signal effecting an unlatching of the control circuit for proper operation of the semiconductor memory device. *Id.* at 2:15–37.

Figure 1 of the '589 patent is reproduced below.

Fig 1

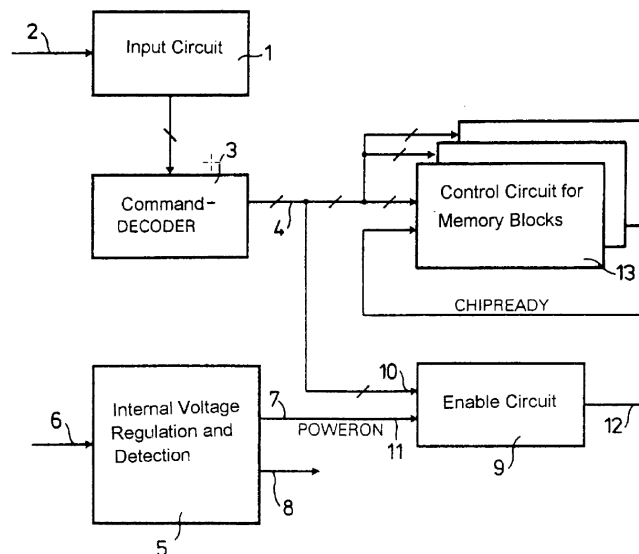


Figure 1 is a block diagram of components of the '589 patent's initialization circuit which controls a switching-on operation of a semiconductor memory operating according to the JEDEC standard. *Id.* at 3:28–31, 3:44–48.

With reference to Figure 1, the '589 patent describes:

The initialization circuit has an input circuit 1, to whose input 2 command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder 3 connected downstream of the input circuit 1 and at whose output 4, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output.

Id. at 3:51–61. The initialization circuit further includes circuit 5 for internal voltage regulation and/or detection, which supplies an active POWERON signal if, after the POWERUP phase of the memory device, the internal supply voltages present at output 8 have reached the values necessary for proper operation of the component. *Id.* at 3:61–4:8.

According to the '589 patent,

the initialization circuit furthermore has an enable circuit 9 connected downstream of the circuits 3 and 5. The command signals PRE, ARF and MRS are applied to an input 10 of the enable circuit 9 and the POWERON signal is applied to an input 11 of the enable circuit 9. An enable signal CHIPREADY is supplied at an output 12 of the enable circuit 9 after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device.

Id. at 4:9–20.

Figure 2 of the '589 patent is reproduced below.

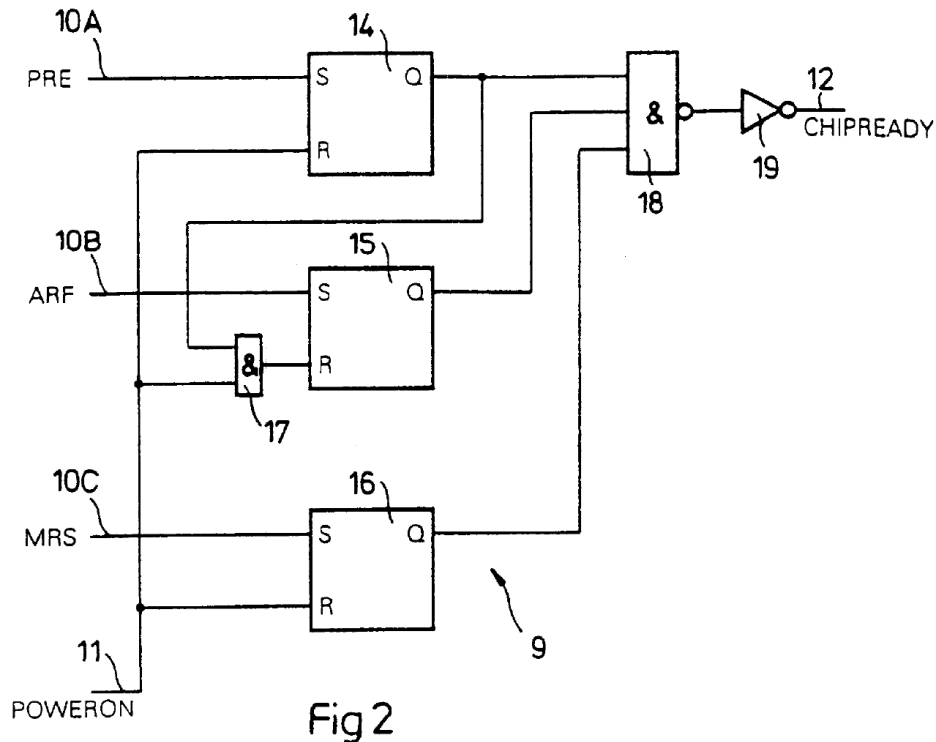


Figure 2 shows an exemplary enable circuit that supplies an enable signal (CHIPREADY). *Id.* at 3:32–33, 4:24–25.

As shown in Figure 2, enable circuit 9 contains three bistable multivibrator stages 14, 15 and 16, each having a set input S, a reset input R, and also an output Q. *Id.* at 4:25–28. The command signals PRE, ARF, MRS are applied to the respective set inputs S of the bistable multivibrator stages 14, 15, 16, whereas the POWERON signal is applied to the reset inputs R. *Id.* at 4:36–38, 4:41–45.

According to the '589 patent,

activation of the enable signal CHIPREADY at is the output 12 to logic HIGH is generated only when a predetermined chronological initialization sequence of the command signals

PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected. Only then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY.

Id. at 4:50–57.

Figure 3 of the '589 patent is reproduced below.

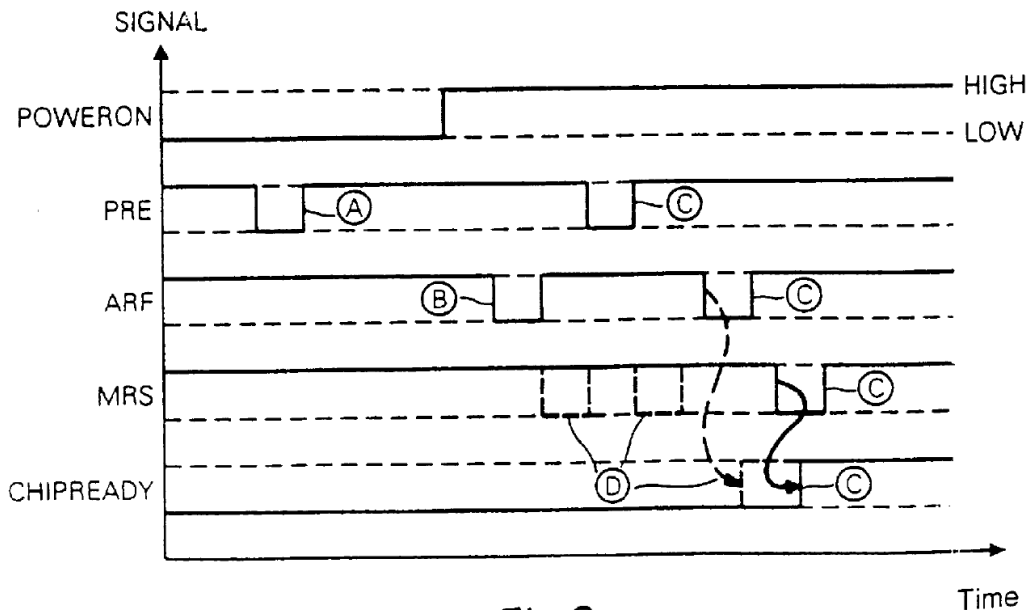


Fig 3

Figure 3 is a schematic time sequence diagram illustrating exemplary command sequences detected by enable circuit 9 of Figure 2. *Id.* at 3:34–35, 4:59–63.

According to the '589 patent,

In case situation C, a correct chronological order of the commands PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET is present conforming to the JEDEC standard, in a logically consistent manner, since the POWERON signal is also at logic HIGH, an enable signal CHIPREADY at logic HIGH is now supplied. Illustrated using dashed lines, another further conceivable initialization sequence that is allowed and therefore triggers an enable signal is represented by the symbol

D; activation of the command MODE-REGISTER-SET to logic LOW is allowed at any time after the activation of the POWERON signal.

Id. at 5:10–21.

D. Illustrative Claim

Of the challenged claims, claims 1 and 11 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below with line breaks and indenting added to improve readability.

1. A dynamic semiconductor memory device of a random access type, comprising:
 - an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation,
 - said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals,
 - said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

Ex. 1001, 5:31–44.

E. Prior Art and Declaration Evidence

Petitioner cites the following references in its challenge to patentability:

U.S. Patent No. 5,559,753, issued Sept. 24, 1996 (Ex. 1004, “Kocis”);

U.S. Patent No. 5,703,510, issued Dec. 30, 1997 (Ex. 1007, “Iketani”);

U.S. Patent No. 5,774,402, issued June 30, 1998 (Ex. 1005, “Lee”);
and

JEDEC Standard No. 21-C, Jan. 1997 (Ex. 1006, “JESD 21-C”).

Petitioner supports its challenge with a declaration from Stephen W. Melvin (Ex. 1003, “Melvin Declaration”). Patent Owner’s Preliminary Response does not rely on the testimony of any declarant.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 3).

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)
1, 9, 11, 13	102	Kocis
2, 8, 10, 12	103	Kocis, JESD 21-C
1, 11	102	Lee
1, 11	103	Lee
1, 11	103	Lee, Iketani
2, 8, 10, 12	103	Lee, JESD 21-C
2, 8, 10, 12	103	Lee, Iketani, JESD 21-C

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’589 patent has a filing date prior to the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of §§ 102 and 103.

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)
9, 13	103	Lee, Kocis
9, 13	103	Lee, Iketani, Kocis

III. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the relevant time is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To assess the level of ordinary skill, we construct a hypothetical “person of ordinary skill in the art,” from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct “presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Citing testimony from Dr. Melvin, Petitioner asserts a person of ordinary skill in the art (“POSITA”) at the relevant time would have had “a Bachelor’s degree in Electrical Engineering or Computer Science and two years of experience” or “equivalent education, work, or experience in this field.” Pet. 21 (citing Ex. 1003 ¶¶ 31–34). According to Dr. Melvin, “[m]ore education could substitute for experience, and vice versa.” Ex. 1003 ¶ 33.

Patent Owner states that “[f]or the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so in the event that trial is instituted.” Prelim. Resp. 11.

For purposes of this Decision, based on our review of the ’589 patent, the types of problems and solutions described in the ’589 patent, and cited prior art, we adopt and apply Petitioner’s unopposed definition of a person of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2022). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the effective filing date of the patent application and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner asserts that “construction of terms is unnecessary because it is not dispositive to this case—the art teaches the limitations under any construction under the *Phillips* standard.” Pet. 21. Patent Owner states that

we need not construe any claim term for purposes of this Decision. *See* Prelim. Resp. 11.

Based on the record presented, we need not construe any claim term for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Asserted Grounds of Unpatentability Based on Lee or the Combination of Lee and Iketani

Petitioner contends that independent claims 1 and 11 are unpatentable under 35 U.S.C. § 103(a) over Lee. Pet. 46–58. In addition, Petitioner asserts that the subject matter of claims 1 and 11 would have been obvious over the combination of Lee and Iketani. *Id.* at 59–63. Petitioner also contends that claims 1 and 11 are unpatentable as anticipated by Lee. *Id.* at 46–58. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 32–37.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 102 only if a single prior art reference expressly or inherently describes each and every limitation set forth in the claim. *See Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005); *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Further, a reference cannot anticipate “unless [it] discloses within the four corners of the document not only all of the limitations claimed[,] but also all of the limitations arranged or combined in

the same way as recited in the claim.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)); accord *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that “some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two

or more references or modifying one to achieve the patented [invention]”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

We analyze the asserted grounds of unpatentability with the principles identified above in mind.

2. Overview of Lee (Ex. 1005)

Lee describes an initialization circuit for a semiconductor memory device, which includes an initialization signal generator that generates an initialization signal in response to a specific sequence of reset control signals. Ex. 1005, Abstract.

As background, Lee describes that semiconductor memory devices require initialization circuits for resetting the various functional circuits within the chip. *Id.* at 1:18–21. According to Lee, conventional initialization circuits, called “power on reset circuits,” generate a reset signal in response to a power supply voltage being applied to the chip. *Id.* at 1:22–24. Figure 1 of Lee (not reproduced herein) describes one such conventional initialization circuit. *Id.* at 1:30–45, Fig. 1. Lee describes that conventional power on reset circuits may malfunction and fail to initialize the circuits within the chip if input power supply voltage is unstable. *Id.* at 2:4–14. Against this backdrop, Lee purports to disclose improved initialization circuits that reliably initialize a semiconductor memory device in response to external logic signals. *Id.* at 2:18–23.

Figure 3 of Lee is reproduced below.

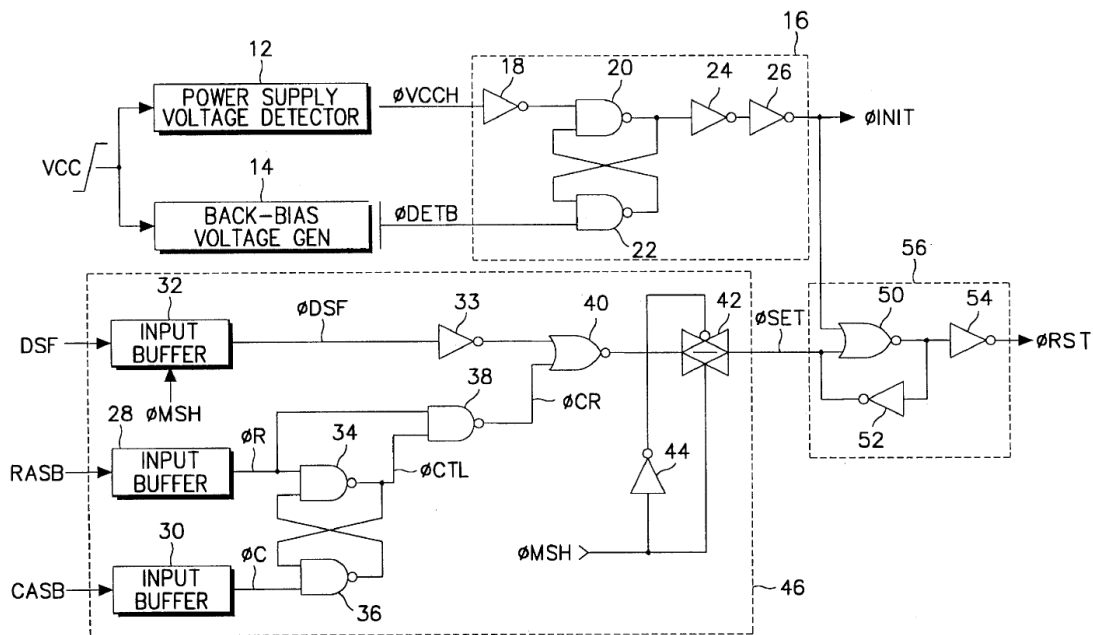


Fig. 3

Figure 3 is a schematic diagram of an embodiment of Lee's initialization circuit. *Id.* at 3:1–3.

As shown in Figure 3, Lee's exemplary initialization circuit comprises first initialization signal generator 46, second initialization signal generator 16, and transfer unit 56. *Id.* at 3:10–14. According to Lee, second initialization signal generator 16, which is “essentially the same” as the conventional power on reset circuit of Figure 1, generates a second initialization signal φINIT in response to the power up of a power supply VCC. *Id.* at 3:17–20. First initialization signal generator 46 generates a first initialization signal φSET in response to a sequence of reset control signals DSF, RASB, and CASB. *Id.* at 3:14–16. Transfer unit 56 combines the first initialization signal φSET and the second initialization signal φINIT to

generate a reset Signal ϕ RST for resetting the circuits within the memory device. *Id.* at 3:20–23, 4:59–62.

3. Overview of Iketani (Ex. 1007)

Iketani describes a DRAM device with a power on reset circuit that initializes the internal circuitry of the DRAM when the power is turned on. Ex. 1007, 1:7–12.

Figure 6 of Iketani is reproduced below.

FIG. 6

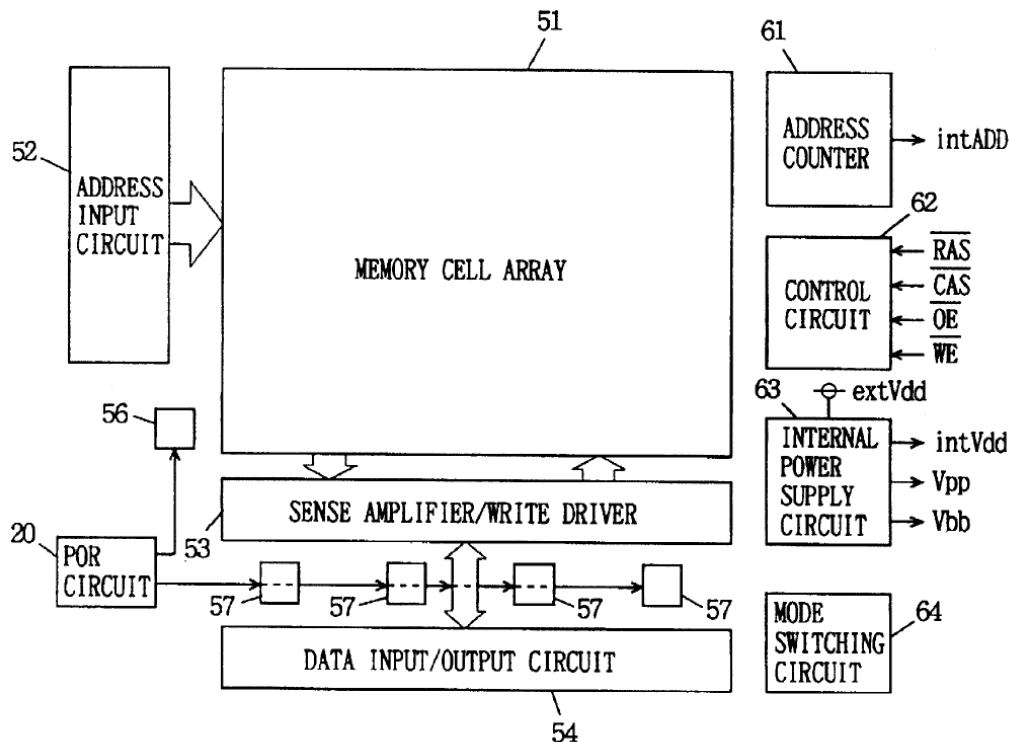


Figure 6 is a block diagram showing an example of Iketani's DRAM for which a power on reset circuit is used. *Id.* at 2:40–41.

Iketani describes that the DRAM shown in Figure 6 includes memory cell array 51, control circuit 62 for controlling internal circuitry, and power on reset circuit 20. *Id.* at 5:4–20. Iketani further describes that power on

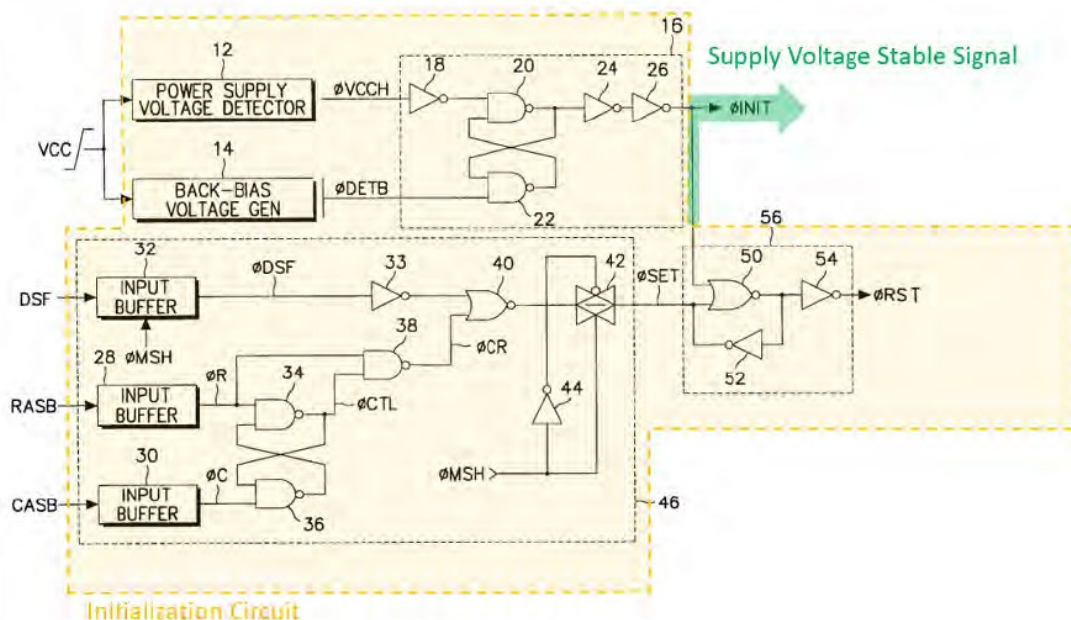
reset circuit 20 generates a power on reset signal that initializes the DRAM circuits, including control circuit 62. *Id.* at 5:20–26.

4. Independent Claims 1 and 11

Petitioner presents essentially the same analysis regarding independent claims 1 and 11, asserting that the independent claims recite similar limitations. *See* Pet. 58, 61–63. Patent Owner contests Petitioner’s showing, addressing claims 1 and 11 together. Prelim. Resp. 32–37. At this stage of the proceeding, Patent Owner’s dispute mostly focuses on the limitation “the enable signal effecting an unlatching of said control circuit” recited in claim 1. *See id.*

Because the parties do not dispute, and we agree, that claims 1 and 11 recite substantially similar limitations, our discussion below focuses on claim 1. Unless otherwise noted, our analysis below applies equally to both independent claims 1 and 11.

Figure 3 of Lee as annotated by Petitioner is reproduced below.



Pet. 48. Annotated Figure 3 of Lee reproduced above illustrates Petitioner's alleged identification in Lee of certain elements of claim 1. *Id.* at 48–50.

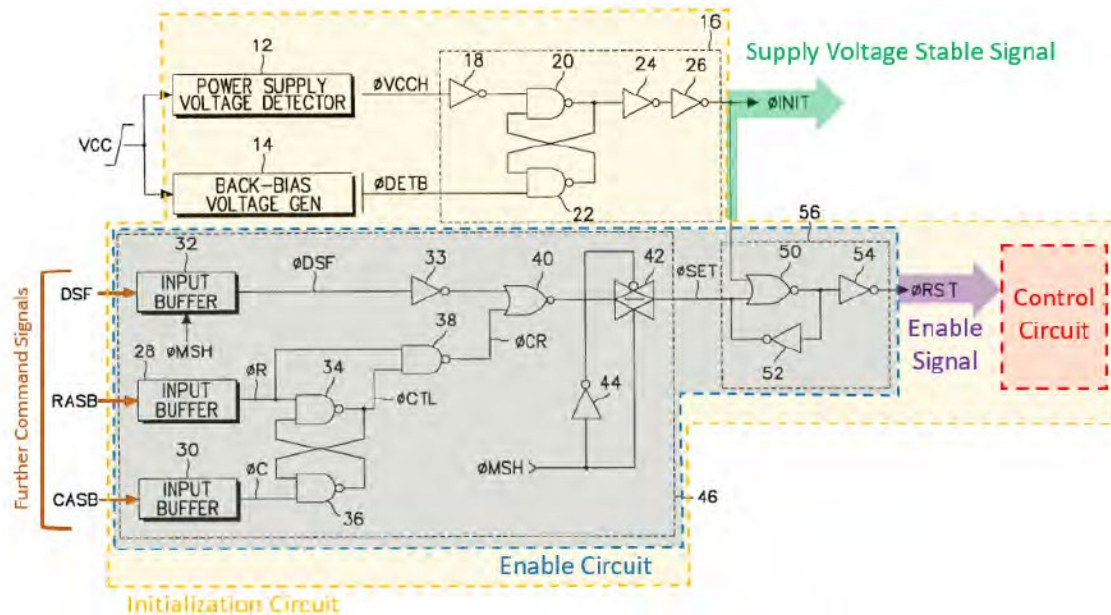
Referencing annotated Figure 3 of Lee reproduced above, Petitioner asserts that Lee discloses the recited “initialization circuit” (Lee’s circuit components 12, 14, 16, 46, and 56, annotated in yellow) for “controlling a switching-on operation and supplying a supply voltage stable signal.”

Pet. 48 (citing Ex. 1003 ¶ 120). Petitioner contends that Lee’s initialization circuit controls a switching-on operation (i.e., the process for powering on the memory chip) because

Lee explains that these types of “initialization circuits are typically referred to as power on reset circuits and generate a reset signal in response to a power supply voltage VCC being applied to the [DRAM] chip. The typical power on reset circuit operates by sensing the level of the power supply voltage VCC and generating an initialization signal for a predetermined length of time when the power supply voltage reaches a predetermined level.”

Id. at 48–49 (quoting Ex. 1005, 1:18–29). Petitioner further asserts that the ϕ INIT signal in Figure 3 of Lee (annotated in green in annotated Figure 3 of Lee reproduced above) teaches the recited “supply voltage stable signal” because Lee’s ϕ INIT signal is generated in response to the power-up of a power supply VCC. *Id.* at 49–50 (citing Ex. 1005, 1:31–34, 1:47–54, 3:9–23; Ex. 1003 ¶ 123).

Figure 3 of Lee as annotated and modified by Petitioner is reproduced below.



Pet. 51 (citing Ex. 1003 ¶ 125). Petitioner-modified Figure 3 of Lee reproduced above illustrates Petitioner’s contentions regarding Lee’s alleged teachings of certain elements of claim 1, including the recited “enable circuit,” “enable signal,” and “control circuit.” *Id.* at 48–58.

Referencing modified Figure 3 of Lee reproduced above, Petitioner asserts that Lee’s first initialization signal generator 46 and transfer unit 56 (annotated in blue above) disclose “an enable circuit receiving the supply voltage stable signal and externally applied further command signals,” as recited in claim 1, because Lee’s enable circuit “receives both the supply voltage stable signal (shown in green above) and externally applied further command signals (shown in brown above).” Pet. 51. Petitioner explains that, as shown in Figure 3 of Lee, transfer unit 56 of Lee’s enable circuit

receives the ϕ INIT signal (the claimed “supply voltage stable signal”). *Id.* (citing Ex. 1005, 4:33–35, 4:59–62, Fig. 3).

Petitioner further contends that the CASB, RASB, and DSF signals (annotated in brown in modified Figure 3 of Lee reproduced above), which are received by first initialization signal generator 46 of Lee’s enable circuit, teach the recited “externally applied further command signals” because a person of ordinary skill in the art would have understood that Lee’s CASB, RASB, and DSF signals are similar to and related to the PRECHARGE, AUTOREFRESH, and MODE-REGISTER-SET commands described in the ’589 patent as examples of the claimed “externally applied further command signals.” Pet. 52–53 (citing Ex. 1001, 2:50–54; Ex. 1005, 3:14–16, 3:37–49; Ex. 1003 ¶¶ 127, 128; Ex. 1019, 10). In particular, Petitioner relies on the testimony of Dr. Melvin that “the CASB and RASB signals are further command signals because a POSITA would have understood that they can be used to generate the PRECHARGE, AUTOREFRESH, and MODE-REGISTER-SET commands disclosed in the ’589 Patent.” Ex. 1003 ¶ 128. In support of his testimony, Dr. Melvin cites to a “TRUTH TABLE” in a DRAM specification that describes how the Precharge, Auto Refresh, and Mode Register Set commands are related to the CAS and RAS signals. *Id.* (citing Ex. 1019, 10).

Further, Petitioner asserts that Lee’s reset signal ϕ RST (annotated in purple above in modified Figure 3 of Lee reproduced above, the claimed “enable signal”) output by Lee’s enable circuit teaches “said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being

identified,” as recited in claim 1, because Lee describes that the reset signal ϕ RST is activated only after the CASB, RASB, and DSF signals produce “a predetermined bit pattern in the proper sequence.” Pet. 55–56 (citing Ex. 1005, 4:38–61).

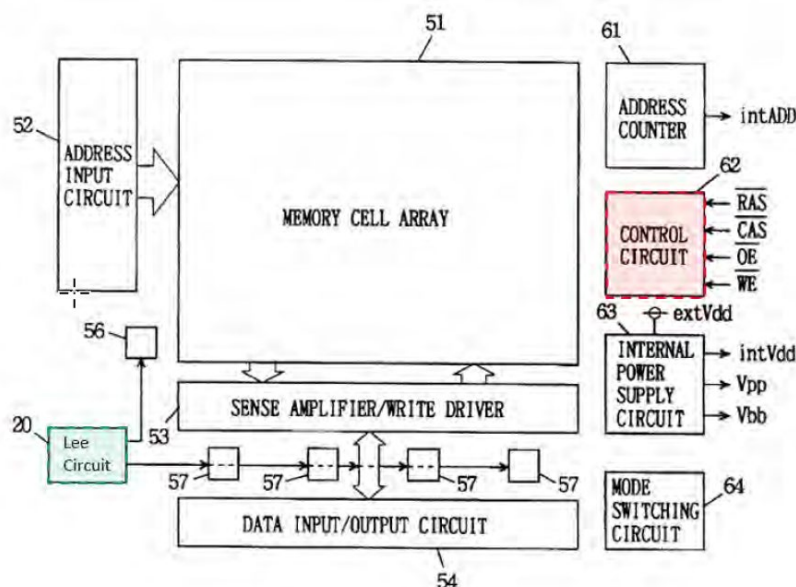
Next, Petitioner asserts that a person of ordinary skill in the art would have understood that Lee teaches or renders obvious “a control circuit for controlling operations” recited in claim 1 because a person of ordinary skill in the art would have understood that Lee includes “a control circuit that receives external commands and controls the internal operation of the memory device so as to properly respond to the commands.” Pet. 54 (citing Ex. 1003 ¶ 130). As discussed above, Petitioner contends that Lee’s external commands include the CASB and RASB commands, which are described in Lee as a “first control signal” and a “second control signal” used to control the read operation of the memory device. *Id.* at 52 (citing Ex. 1005, 3:37–49; Ex. 1003 ¶ 127). In the cited paragraph of his Declaration, Dr. Melvin states that “CASB is a column address strobe signal and RASB is a row address strobe signal,” which are “primarily used to instruct the memory chip to activate or open a row and then to read a column within the activated row.” Ex. 1003 ¶ 127. Dr. Melvin provides a similar explanation in the “Technology Background” section of his Declaration, citing a DRAM specification as support. *Id.* ¶ 53 (citing Exs. 1017, 1018).

Petitioner further contends that a person of ordinary skill in the art would have understood that Lee’s reset signal ϕ RST initializes the control circuit because Lee discloses that the reset signal initializes “circuit[s] within the memory device” or “circuit[s] within the chip.” Pet. 53–55 (citing

Ex. 1005, 1:20–21 (“[Semiconductor memory] devices require initialization circuits for resetting the various functional circuits within the chip.”), 3:19–22 (“The transfer unit 56 generates a reset signal ϕ RST for resetting a circuit within the memory device responsive to the first and second initialization signals.”), 4:20–24 (“transfer unit 56 for sending the reset signal ϕ RST to a circuit to be initialized within the chip”), 4:35–37 (“all circuits within the chip which are connected to the output terminal of transfer unit 56 [are] held in the initialized state”), 4:59–62 (“The transfer unit 56 . . . activates the reset signal ϕ RST . . . thereby initializing the circuits within the chip.”), 5:11–13). Petitioner’s contention is illustrated by Petitioner’s modification of Figure 3 of Lee (reproduced above) to add a Control Circuit (in red color) that receives the reset signal ϕ RST. *Id.* at 51, 53.

In the alternative, Petitioner asserts that the combination of Lee and Iketani teaches the recited “control circuit.” Pet. 59–63.

Annotated and modified Figure 6 of Iketani illustrating Petitioner’s proposed combination of Lee and Iketani is reproduced below.



Pet. 60. The figure reproduced above shows Petitioner's illustration of the proposed combination of Lee and Iketani. *Id.* at 59–61.

As illustrated in the Petitioner-modified Figure 6 of Iketani reproduced above, in the proposed combination of Lee and Iketani, Lee's initialization circuit replaces Iketani's power on reset circuit 20, with Lee's reset signal ϕ RST providing the initialization signal for Iketani's control circuit. Pet. 59–60. Petitioner contends that a person of ordinary skill in the art would have recognized that the initialization circuit of Lee is compatible with the controller of Iketani because “[b]oth the power on reset circuit of Iketani and the initialization circuit of Lee perform similar functions and are used for the same purpose.” *Id.* (citing Ex. 1005, 2:4–6, 2:18–20; Ex. 1007, 2:1–4; Ex. 1003 ¶ 140). Citing Iketani's disclosure that the power on reset signal generated by Iketani's power on reset circuit 20 is supplied to control circuit 62 of Iketani, Petitioner asserts that “a POSITA would have understood that Lee's initialization circuit is . . . compatible with Iketani's control circuit.” *Id.* at 61 (citing Ex. 1007, 5:20–26; Ex. 1003 ¶ 142).

Petitioner argues that Lee and Iketani expressly provide the motivation to combine the references because “[w]hile Lee does expressly illustrate the ‘circuitry’ that is initialized by the reset signal ϕ RST output from its initialization circuit, Iketani illustrates and describes in detail the various circuits, including *the control circuit*, that receive and are initialized by such an initialization signal.” Pet. 59 (emphasis added) (citing Ex. 1003 ¶ 140). Petitioner further asserts that the proposed combination “amounts to a simple substitution of one component (i.e., Lee's initialization circuit) for another (i.e., Iketani's power on reset circuit), and a POSITA would have

understood that this substitution would yield predictable results.” *Id.* at 61 (citing Ex. 1003 ¶ 143).

Lastly, Petitioner contends that Lee’s reset signal ϕ RST (the claimed “enable signal”) teaches “the enable signal effecting an unlatching of said control circuit,” as recited in claim 1, because a person of ordinary skill in the art would have understood that initialization of the control circuit “causes the start of normal operation” of the control circuit. Pet. 57 (citing Ex. 1005, 4:13–24, 4:59–5:4; Ex. 1003 ¶ 133). In the combination of Lee and Iketani, Petitioner further argues that “the control circuit is unlatched by an enable signal through Iketani’s disclosure that the control circuit is initialized by the reset signal.” *Id.* at 63 (citing Ex. 1007, 5:12–26; Ex. 1003 ¶¶ 148, 151).

In the Preliminary Response, Patent Owner asserts that Lee “contains no disclosure that this [reset signal ϕ RST] . . . unlatches any control circuit for normal operation.” Prelim. Resp. 33. Similarly, Patent Owner argues that “[l]ike Lee, the initialization of the control circuit as described in Iketani fails to disclose that the control circuit is unlatched for operation.” *Id.* at 37.

Although we agree with Patent Owner that Lee and Iketani do not use the word “unlatch” in describing the reset or initialization of the memory circuit, identity of terminology is not required to disclose a claim limitation. *See In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009). Rather, “[w]hether prior art invalidates a patent claim as obvious is determined from the perspective of one of ordinary skill in the art.” *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1374 (Fed. Cir. 2011). Under 35 U.S.C. § 103, the obviousness inquiry turns not only on the prior art, but

whether “the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious . . . to a person having ordinary skill in the art to which the claimed invention pertains.” *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020) (quoting 35 U.S.C. § 103). And “the inquiry into whether any ‘differences’ between the invention and the prior art would have rendered the invention obvious to a skilled artisan *necessarily depends on such artisan’s knowledge.*” *Id.* (emphasis added); *see also Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015) (“Art can legitimately serve to document the knowledge that skilled artisans would bring to bear *in reading the prior art identified as producing obviousness.*” (emphasis added)); *Hyosung TNS Inc. v. Int’l Trade Comm’n*, 926 F.3d 1353, 1360 (Fed. Cir. 2019) (citing *Ariosa* and concluding that the patent challenger permissibly relied on a reference, “not as a separate piece of prior art to be combined with” the two references in the asserted combination, “but rather as evidence of the knowledge of a person of ordinary skill in the art that” one of the asserted references teaches a claim limitation); *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1336 (Fed. Cir. 2008) (“[T]he meaning of a prior art reference requires analysis of the understanding of an artisan of ordinary skill.”).

In an IPR, a patentee’s admissions regarding the scope and content of the prior art may be used to demonstrate the knowledge of the ordinarily-skilled artisan at the time of the invention for purposes of assessing a claim’s patentability under § 103. *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022); *see also* June 9, 2022 Updated Guidance on the Treatment

of Statements of the Applicant in the Challenged Patent in *Inter Partes* Reviews under § 311 (“Updated Guidance”), 4 (“A patentee’s admissions regarding the scope and content of the prior art under § 103 can be used, for example, to . . . demonstrate the knowledge of the ordinarily-skilled artisan at the time of the invention . . .”).² The statements in a challenged patent regarding prior art or what was known to a person of ordinary skill in the art are generally referred to as “applicant-admitted-prior-art” or “AAPA.” Updated Guidance, 1.

In the Petition, Petitioner relies on Patent Owner’s statements in the Background of the Invention section of the ’589 patent as evidence of the knowledge the ordinarily-skilled artisan would bring to bear in reading Lee or Iketani as teaching the limitation reciting “the enable signal effecting an unlatching of said control circuit.” For instance, under the heading “Applicant Admitted Prior Art in the Background of the ’589 Patent,” Petitioner argues that the background section of the ’589 patent states as follows:

In the case of the SDRAM semiconductor memory modules that have been *disclosed to date*, all the control circuits of the component have been *unlatched* only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for *the proper operation of the component*. The module is then in a position to recognize and execute instructions.

Pet. 10–11 (emphases added) (quoting Ex. 1001, 1:65–2:5). In other words, Petitioner asserts that Patent Owner admitted in the ’589 patent that it was

² Available at <https://www.uspto.gov/sites/default/files/documents/2022060912updatedAAPAmemo.pdf>.

known at the time of the filing that a power on reset signal *unlatches* the control circuit for proper operation of the circuit.

Similarly, in the Melvin Declaration, under the heading “Background / Applicant Admitted Prior Art,” Dr. Melvin discusses the background portion of the ’589 patent quoted above, in connection with the alleged obviousness of the “enable signal effecting an unlatching of said control circuit” limitation of claim 1. Ex. 1003 ¶ 38.

As discussed above, Petitioner asserts that a person of ordinary skill in the art would have understood Lee’s disclosures regarding initialization of the control circuit by a reset signal—initialization that “causes the start of normal operation” of the control circuit—teaches “unlatching” of the control circuit. Pet. 57. Similarly, Petitioner argues that Iketani’s initialization of the control circuit by a reset signal teaches that “the control circuit is unlatched by an enable signal.” *Id.* at 63.

Based on the record presented, in view of the cited statements by Patent Owner in the ’589 patent, we are persuaded Petitioner has shown sufficiently for purposes of institution that Lee’s reset signal ϕ RST or Iketani’s power on reset signal that initializes the control circuit for proper operation teaches or suggests “the enable signal effecting an unlatching of said control circuit,” as recited in claim 1.³

³ Under the factual circumstances presented, the fact that Applicant Admitted Prior Art is not included in the asserted grounds in the Petition does not bar Petitioner’s use in this proceeding of Patent Owner’s admissions in the patent to demonstrate the knowledge of the ordinarily-skilled artisan at the time of the invention for purposes of arguing the unpatentability of the challenged claims under § 103. *See Qualcomm*, 24 F.4th at 1376; Updated Guidance, 4; *see also Lone Star Silicon*

At this stage of the proceeding, Patent Owner does not dispute that Lee or the combination of Lee and Iketani teaches any other limitations of claim 1. *See* Prelim. Resp. 32–37. Based on the current record, for the reasons explained by Petitioner in the Petition, as summarized above, we determine that Petitioner has shown sufficiently for purposes of institution that Lee or the combination of Lee and Iketani teaches or suggests all elements of claim 1. We also find, for purposes of this Decision, Petitioner has provided sufficient explanation and evidence to show that a person of ordinary skill in the art would have been motivated to combine Lee and Iketani, as proposed by Petitioner, with a reasonable expectation of success.

Based on the record presented and for the foregoing reasons, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to independent claims 1 and 11 under 35 U.S.C. § 103 as obvious over Lee or the combination of Lee and Iketani.⁴

Innovations LLC v. Iancu, 809 F. App'x 773, 777 (Fed. Cir. 2020) (affirming the Board's finding of obviousness based on Watatani and Tanaka, as well as additional references that were relied on exclusively for their teachings about what was well-known in the art, although the additional references were not listed in the ground presented in the petition) (nonprecedential).

⁴ Because, among other reasons, Petitioner relies on a modified Figure 3 of Lee, we do not determine Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 1 and 11 under 35 U.S.C. § 102 as anticipated by Lee. *See Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008) (“[D]ifferences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.”).

*D. Asserted Obviousness over Lee and JESD 21-C or
Lee, Iketani, and JESD 21-C*

Petitioner contends that dependent claims 2, 8, 10, and 12 would have been obvious over the combination of Lee and JESD 21-C or Lee, Iketani, and JESD 21-C. Pet. 63–66.

Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 2, 8, 10, and 12 are taught in JESD 21-C, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 39–46, 65, 66. Petitioner also explains persuasively that a person of ordinary skill in the art would have been motivated to combine Lee with JESD 21-C or Lee and Iketani with JESD 21-C “to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Lee in order to ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by the POSITA.” *Id.* at 64 (citing Ex. 1003 ¶ 154).

Patent Owner does not respond specifically to Petitioner’s challenge to these dependent claims beyond Patent Owner’s arguments advanced with respect to independent claims 1 and 11 discussed above. *See* Prelim. Resp. 37–38.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 2, 8, 10, and 12 as unpatentable under § 103 over Lee and JESD 21-C or Lee, Iketani, and JESD 21-C.

E. Asserted Anticipation by Kocis

Petitioner asserts that claims 1, 9, 11, and 13 are unpatentable as anticipated by Kocis. Pet. 22–36. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 24–30.

1. Overview of Kocis (Ex. 1004)

Kocis describes a DRAM circuit with circuitry for disabling data output drivers to prevent bus contention during system power-up. Ex. 1004, Abstract.

According to Kocis, the conventional approach of using a time delay circuit to wait for the power supply to stabilize before operating a DRAM may be problematic because “the stabilization period for the power supply may vary considerably from one system to another.” *Id.* at 3:26–28. Kocis purports to “solve[] the shortcomings and deficiencies of the prior art” by constructing a circuit that disables DRAM data output signals until seven or eight RAS and/or CAS signals are received by the DRAM circuit. *Id.* at 3:41–48.

Figure 5 of Kocis is reproduced below.

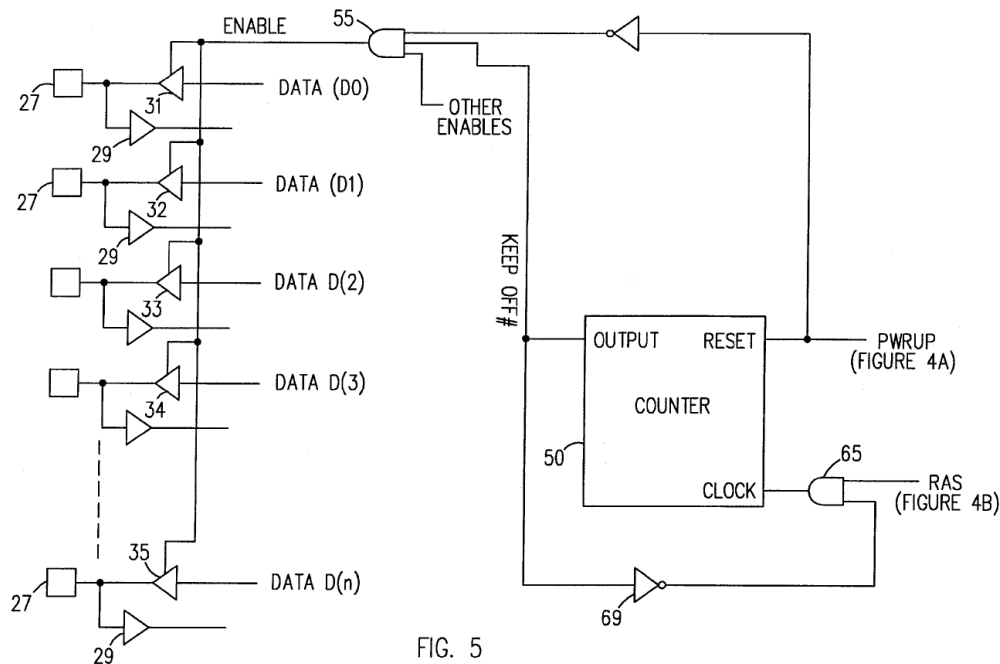


Figure 5 of Kocis is a functional drawing of an exemplary circuit for disabling DRAM data output until power supply voltages are satisfactory and all enable conditions are met. *Id.* at 4:23–26.

According to Kocis, tri-state buffers 31, 32, 33, 34, 35 shown in Figure 5 transmit the associated data signal only when enabled by the ENABLE line—i.e., when the ENABLE line is high. *Id.* at 4:60–64. As shown in Figure 5, the ENABLE signal comprises an output signal from AND gate 55. *Id.* at 5:1–3.

In the preferred embodiment of Figure 5, the AND gate 55 receives three input signals—(1) an inverted Pwrup signal from the output of the voltage detection circuit of Figure 4A; (2) an output signal (Keep Off) from counter 50; and (3) other enable signals. *Id.* at 5:3–7. Kocis further discloses that “[t]he output of the AND gate 55 (which comprises the

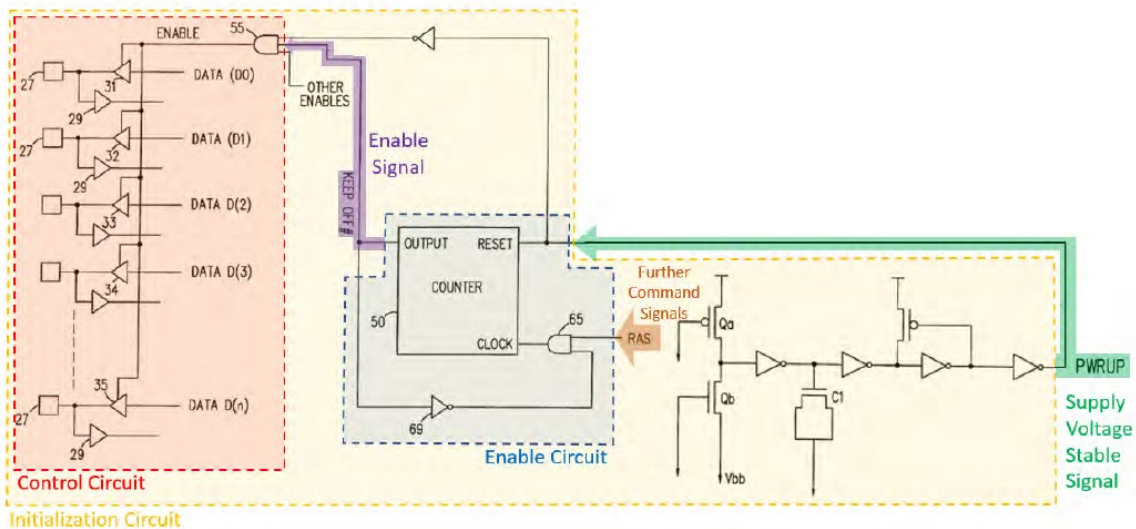
ENABLE signal), only is driven high if all input signals are high” and consequently, “tri-state buffers 31, 32,33,34, 35 only are enabled if all three input signals are high.” *Id.* at 5:8–12.

As for the output signal (Keep Off) from counter 50, Kocis describes that counter 50 counts the number of RAS signals received from memory controller 8 and that after the counter 50 counts eight RAS signals, an output signal (Keep Off) is generated by the counter. *Id.* at 5:40–44.

2. Independent Claims 1 and 11

Petitioner contends that Kocis discloses all elements of independent claims 1 and 11. Pet. 22–33, 35–36.

Petitioner annotated Figures 4A and 5 of Kocis are reproduced below.



Pet. 26, 31. Annotated Figures 4A and 5 of Kocis reproduced above illustrate Petitioner’s alleged identification in Kocis of an “enable signal” recited in claim 1. *Id.* at 29–31.

Referencing the annotated Figures 4A and 5 of Kocis reproduced above, Petitioner contends that the Keep Off signal of Kocis (annotated in

purple), i.e., the output signal of counter 50, discloses an “enable signal” recited in claim 1 because the Keep Off is an input to AND gate 55 and “[a] POSITA would have understood that driving a high input to the AND gate 55 which *ultimately* enables the tri-state buffers.” Pet. 32 (emphasis added) (citing Ex. 1003 ¶ 81).

Based on the record presented, we are not persuaded by Petitioner’s argument because it is contrary to express disclosure in Kocis. As Petitioner acknowledges, the Keep Off signal of Kocis is only *one of three input signals* to AND gate 55—(1) an inverted Pwrap signal from the output of the voltage detection circuit of Figure 4A; (2) an output signal (Keep Off) from counter 50; and (3) other enable signals. Pet. 28 (quoting Ex. 1004, 5:3–12). Petitioner further concedes that Kocis discloses that “[t]he output of the AND gate 55 . . . is driven high *if all input signals are high*. Thus, tri-state buffers 31, 32, 33, 34, 35 *only are enabled if all [the] input signals are high*.” *Id.* (emphases added) (quoting Ex. 1004, 5:3–12).

Thus, Kocis discloses that the tri-state buffers are enabled by the output signal of AND gate 55, *not* the Keep Off signal. Ex. 1004, 5:3–12; *see also id.* at 4:60–64 (“the tri-state buffers transmit the associated data signal only when enabled by the ENABLE line. The tri-state buffers 31, 32, 33, 34, 35 . . . only drive the data signals when the ENABLE line is high.”). As Petitioner concedes, the Keep Off signal is only one of the three input signals to AND gate 55, *all of which* must be activated to activate the output signal of the AND gate 55 and enable the buffer. Pet. 28 (quoting Ex. 1004, 5:3–12).

To the extent Petitioner argues that the Keep Off signal “enables” the AND gate 55, Petitioner’s argument is also contrary to express disclosure in Kocis that *all three input signals* to AND gate 55 must be activated to activate the AND gate 55.⁵ *See* Ex. 1004, 5:3–12.

In the cited paragraph of his Declaration, Dr. Melvin essentially repeats Petitioner’s argument and does not explain why the Keep Off signal of Kocis discloses an “enable signal” despite the express disclosures in Kocis that contradict Petitioner’s contention. *See* Ex. 1003 ¶ 81. Thus, based on the record presented, Petitioner does not establish sufficiently that Kocis discloses the recited “enable signal” for purposes of showing anticipation by Kocis. *See Net MoneyIN*, 545 F.3d at 1371 (“[D]ifferences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.”).

In a footnote, Petitioner argues alternatively that Kocis discloses the “Enable” signal as the claimed “enable signal.” Pet. 30 n.1. Petitioner’s alternative argument, however, is not sufficiently developed to address all elements of claim 1. For example, Petitioner does not explain how counter 50 of Kocis, the “enable circuit” relied on by Petitioner (*id.* at 26), generates the “Enable” signal, as required by claim 1. *See id.* at 30 n.1.

Petitioner presents essentially the same argument with respect to anticipation of claim 11 by Kocis. Pet. 35–36. Thus, based on the record

⁵ To the extent Petitioner argues that any input signal “enables” the AND gate 55, Petitioner appears to propose modifying AND gate 55 to an OR gate, which would be activated by any active input signal.

presented, Petitioner does not demonstrate a reasonable likelihood of proving that Kocis anticipates independent claims 1 and 11.

3. Dependent Claims 9 and 13

Petitioner's discussion of dependent claims 9 and 13, which depend from claims 1 and 11, respectively, does not cure the deficiencies in Petitioner's arguments and evidence regarding independent claims 1 and 11 discussed above. *See* Pet. 33–34, 36. Thus, based on the record presented, Petitioner does not demonstrate a reasonable likelihood of proving that Kocis anticipates dependent claims 9 and 13.

F. Asserted Obviousness over Lee and Kocis or Lee, Iketani, and Kocis

Petitioner contends that dependent claims 9 and 13 would have been obvious over the combination of Lee and Kocis or Lee, Iketani, and Kocis. Pet. 66–71. In these asserted grounds of obviousness, Petitioner relies on its arguments and evidence presented in the context of Petitioner's contention that Kocis anticipates dependent claims 9 and 13. For example, Petitioner asserts that “[a]s previously described, Kocis provides output drivers that remain latched during the initialization and switching-on operation of the memory device and that are then unlatched upon the stabilization of power and the receipt of a proper initialization sequence of command signals.” *Id.* at 66 (citing Pet. § X.A.2 (arguing purported anticipation of claim 9 by Kocis)). Petitioner relies on this alleged disclosure in Kocis as teaching the additional limitations of dependent claims 9 and 13 in the proposed combination of Lee and Kocis because Lee does not disclose that the output

buffers/drivers of the memory device are part of the circuitry that is unlatched upon initialization. *Id.* at 66–67.

Petitioner’s contention that Kocis anticipates dependent claims 9 and 13 rely on Petitioner’s argument and evidence that Kocis anticipates independent claims 1 and 11. *See id.* at 33–34, 36. Because, for the reasons discussed above in Sections III.E.2 and III.E.3, we determine Petitioner does not demonstrate a reasonable likelihood of proving that Kocis anticipates independent claims 1 and 11 and dependent claims 9 and 13, we are unable to determine, based on the current record, that the information presented shows a reasonable likelihood that Petitioner would prevail in showing that claims 9 and 13 would have been obvious over the combination of Lee and Kocis or Lee, Iketani, and Kocis.

IV. CONCLUSION

For the foregoing reasons, taking into account the arguments and evidence presented in Patent Owner’s Preliminary Response, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in proving that at least one challenged claim of the ’589 patent is unpatentable. Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

At this stage of the proceeding, we have not made a final determination as to the patentability of any of the challenged claims. Our final determination will be based on the record as fully developed during trial.

V. ORDER

In consideration of the foregoing, it is
ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review is
hereby instituted as to claims 1, 2, and 8–13 of the '589 patent on all
grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and
37 C.F.R. § 42.4, notice is hereby given of the institution of a trial,
commencing on the entry date of this Decision.

IPR2023-00516
Patent 6,157,589

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