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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

Case IPR2023-00516

U.S. Patent 6,157,589

PATENT OWNER'S RESPONSE

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<i>Net MoneyIN, Inc. v. VeriSign, Inc.</i> , 545 F.3d 1359 (Fed. Cir. 2008)	18
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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Timothy D. Dorney, Ph.D. Pursuant to 37 C.F.R. § 1.68
2002	Transcript of the Deposition Stephen W. Melvin, Ph.D.

LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.P]	A dynamic semiconductor memory device of a random access type, comprising:
[1.1]	an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation,
[1.2]	said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals,
[1.3]	said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.
Claim 2	
[2]	The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.
Claim 8	
[8]	The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

Claim 9	
[9]	The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.
Claim 10	
[10]	The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal.
Claim 11	
[11.P]	An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:
[11.1]	supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and
[11.2]	supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

Claim 12	
[12]	The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.
Claim 13	
[13]	The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

I. INTRODUCTION

Polaris Innovations Limited (“Patent Owner”) submits this Response to Xilinx, Inc.’s (“Petitioner”) Petition for *Inter Partes* Review (“Petition,” Paper 2), challenging Claims 1, 2, and 8-13 of U.S. Patent 6,157,589 (the “’589 Patent”) (Ex. 1001).

The ’589 Patent concerns methods and circuitry for powering on dynamic random-access memories (“DRAM”). The claims require circuitry to identify a sequence of command signals and then unlatch the DRAM for normal operation. Petitioner raises nine grounds to challenge these claims combining four different references in various configurations in an attempt to reconstruct the claimed invention. The overall approach and an examination of the individual references and assertions demonstrates that these arguments are nothing more than the application of hindsight bias to cobble together prior art circuitry to achieve the ends and requirements of the claimed inventions.

The Board previously found that five of the grounds asserted in the petition were not likely to be successful. The other four, obviousness combinations based on the primary Lee reference, fail to render the challenged claims obvious at least because they do not disclose identifying a sequence of command signals or unlatching a DRAM as explained in more detail below. The remaining grounds that

the Board previously found lacking should fail for the same reasons previously identified and additional ones provided herein.

The Board should reject each of Petitioner's proposed grounds for invalidity and confirm that Petitioner has failed to show unpatentability for the challenged claims.

II. THE '589 PATENT AND THE CHALLENGED CLAIMS

A. Overview of the '589 Patent

The '589 Patent "relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device." Ex. 1001 at 1:9-13. "The invention [] relates to a method for initializing such a dynamic semiconductor memory device, and [] the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device." *Id.* at 1:16-21.

The '589 Patent explains that "during the switch-on operation ('POWERUP')" for "SDRAM semiconductor memories according to the JEDEC standard" "the internal control circuits" must be "held in a defined desired state, in order to prevent undesirable activation" "or uncontrolled activation." *Id.* at 1:22-30. "The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage

level or levels at the external control inputs during the switch-on operation of the semiconductor memory.” *Id.* at 1:30-35.

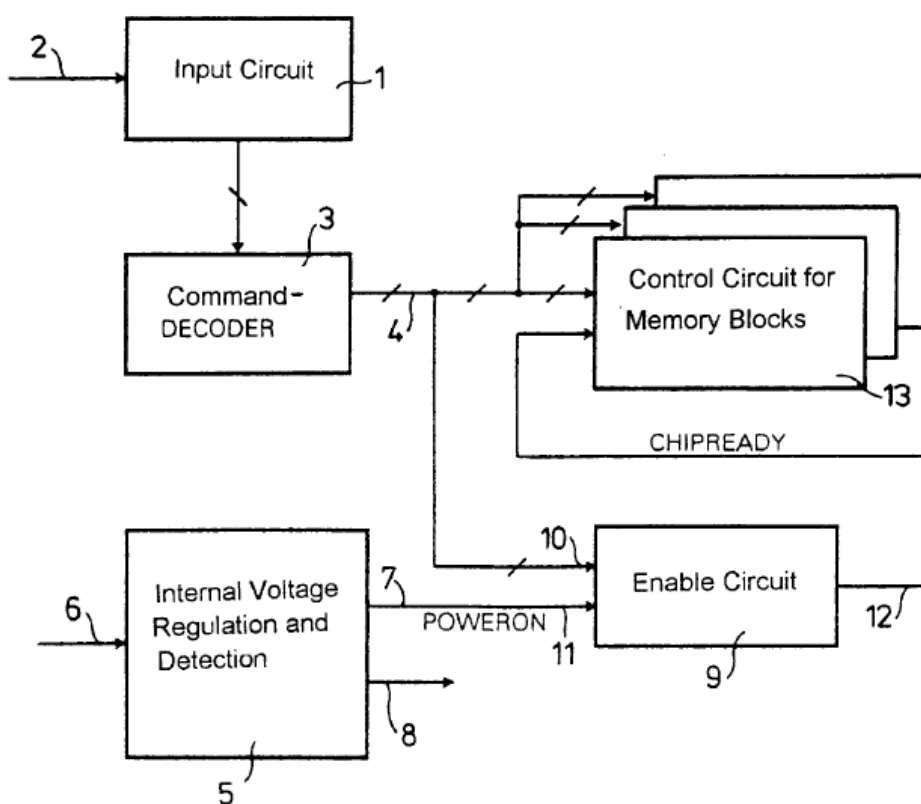
The ’589 patent explains that “[a]ccording to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence.” *Id.* at Col. 1:35-38. “The sequence consists of predetermined commands that must be applied in a defined chronological order.” *Id.* at Col. 1:38-40. The ’589 Patent provides an example of “a recommended initialization sequence” from the JEDEC standard. *Id.* at 1:43-61. The ’589 Patent explains that “[a]fter the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation.” *Id.* at Col. 1:62-65. “In the case of SDRAM semiconductor memory modules that have been disclosed to date,” all the control circuits of the component have been unlatched only with the POWERON signal.” *Id.* at Col. 1:65-2:1. “The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component.” *Id.* at Col. 2:1-4.

The ’589 Patent addresses these issues by providing “an initialization circuit controlling a switching-on operation.” *Id.* at Col. 2:15-21. The initialization circuit includes an “enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals are

identified and the enable signal effecting an unlatching of the control circuit.” *Id.* at Col. 2:20-28.

The ’589 Patent provides a block diagram of an initialization circuit according to the invention in Figure 1:

Fig 1



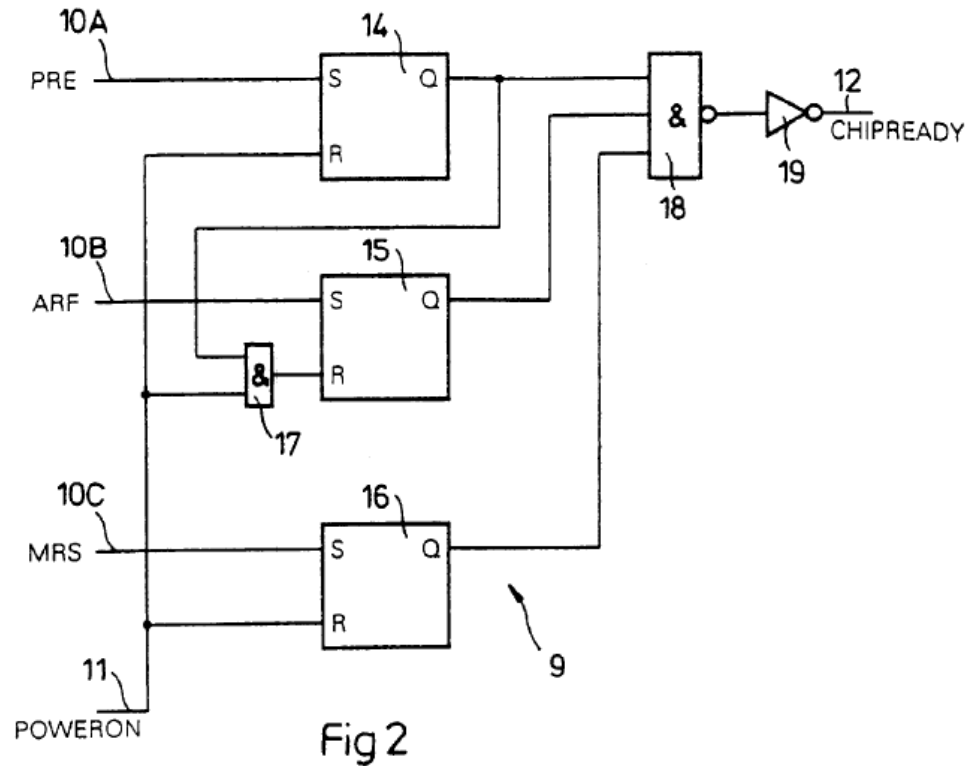
Ex. 1001, Fig. 1.

“The initialization circuit has an input circuit 1, to whose input 2 command and clock signals [] are externally applied.” *Id.* at 3:51-53. “The command and clock signals are amplified and conditioned before being received by a command decoder

3 . . . at whose output 4, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output.” *Id.* at 3:54-61. “The initialization circuit further has a circuit 5 for internal voltage regulation and/or detection” which “has a first output 7 outputting a POWERON signal and a second output 8 supplying stabilized internal supply voltages.” *Id.* at 3:61-65.

The initialization circuit also has an enable circuit 9 that receives the command signals from command decoder 3 and the POWERON signal from the voltage regulation/detection circuit 5. *Id.* at 4:9-14. The enable circuit provides “[a]n enable signal CHIPREADY” “after the identification of a predetermined proper initialization sequence of the command signals.” *Id.* at Col. 4:14-18. “The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device.” *Id.* at Col. 4:18-20.

Figure 2 shows an exemplary embodiment of an enable circuit according to the invention:

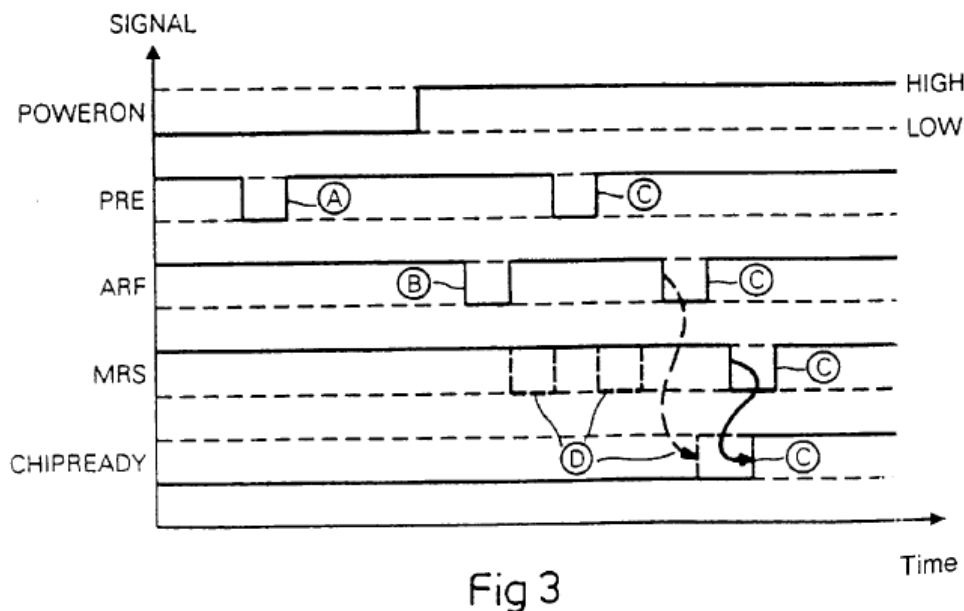


Ex. 1001, Fig. 2.

The enable circuit in Figure 2 contains three bistable multivibrator stages each with set and reset inputs. *Id.* at Col. 4:24-28. “The command signals PRE, ARF, MRS applied to the respective set inputs S” and “[t]he POWERON signal is applied directly to the reset inputs R.” *Id.* at Col. 4:37-48. With these connections and the additional logic described in Figure 2, “activation of the enable signal CHIPREADY at [] the output 12 . . . is generated *only* when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected.” *Id.* at Col. 4:49-55

(emphasis added). “Only then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY.” *Id.* at Col. 4:55-58.

The '589 Patent further illustrates the operation of the enable circuit in the schematic time sequence diagram of Figure 3. *Id.* at Col. 4:59-63.



Ex. 1001, Fig. 3.

The '589 Patent describes four potential sequences A through D and their results. *Id.* at 4:63-5:21. For example in case A, PRE activates before the POWERON and because “the proper initialization sequence requires a waiting time before the first command,” CHIPREADY does not activate. *Id.* at 4:63-5:1. In case B, “the chronological order of the activation of the signal AUTOREFRESH [ARF] . . . is incorrect since the proper initialization sequence prescribes a previous PRECHARGE [PRE] command.” *Id.* at 5:3-10. In case C, “a correct chronological

order of the commands PRECHARGE [PRE], AUTOREFRESH [ARF], MODE-REGISTER-SET [MRS] is present,” and therefore “an enable signal CHIPREADY at logic HIGH is now supplied.” *Id.* at Col. 5:10-16. Case D provides another conceivable sequence that is allowed in this example. *Id.* at Col. 5:15-21.

Based on these disclosed inventions, the '589 Patent claims, inter alia, an apparatus and method for switching on, or unlatching the control circuits of (*see, e.g., id.* at Col. 4:18-20), a DRAM based on identification of an acceptable initialization sequence. The next section provides more detail regarding the specific claims at issue.

B. Challenged Claims

The Petition challenges claims 1, 2, and 8-13 of the '589 Patent. *See* Petition at 3. Claims 1 and 11 are independent claims. Claims 2 and 8-10 depend from claim 1, and claims 12 and 13 depend from claim 11. The full text of these claims is provided in the Listing of Challenged Claims preceding this response with the same indices as the Petition for ease of reference. *See* Pet. at v-vii.

The independent claims are reproduced below with emphasis on the particular limitations that will be addressed in particular in this Response:

Claim 1 recites:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation,

said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals,

said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

Claim 11 recites:

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching

of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

The emphasized limitations in each independent claim require that the claimed inventions, in accordance with the other requirements of each claim, output an enable signal after identifying a “proper initialization sequence” of “further command signals” and that enable signal “effecting an unlatching” of the control circuit. As addressed further herein, none of the Petitioner’s references disclose these limitations nor does the Petition articulate a motivation to modify any of the references to meet these limitations. Because the remaining challenged claims all depend from these independent claims, it necessarily follows that the challenged dependent claims are likewise not disclosed or rendered obvious by the asserted references.

III. LEVEL OF ORDINARY SKILL

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the time of the ’589 patent would have had a “Bachelor’s degree in Electrical Engineering or Computer Science and two years of experience working in the field of system design using semiconductor memories, or a person with equivalent education, work, or experience in this field. More education could substitute for experience, and vice versa.” See Pet. at 21. Patent Owner’s expert believes that a POSITA would have (1) a bachelor’s degree in computer engineering or electrical

engineering with two to three years of circuit design experience, or (2) a master's degree in computer engineering or electrical engineering with one year of circuit design experience at the time of filing of the '589 Patent. *See* Ex. 2001 at ¶104. For the purposes of this trial, Patent Owner contends that both Petitioner's and its own expert's description of the POSITA are consistent.

IV. CLAIM CONSTRUCTION

Claim terms subject to inter partes review are to be “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b).

A. “Externally Applied Further Command Signals” (Cl. 1) / “Further Command Signals Externally Applied” (Cl. 11)

Patent Owner asserts that the term “externally applied further command signals” (claim 1) or “further command signals externally applied” (claim 11) requires construction in order to properly evaluate the scope of the claims and the asserted art raised by Petitioner. Following applicable claim construction standards, we analyze the language of the claims, the specification, and the prosecution history from the perspective of a POSITA. There were no statements in the prosecution history that would affect the construction of “command signals,” (Ex. 2001 at ¶48),

and we must look to how a POSITA would have understood this term in the claims and specification.

Looking first to the claims (set forth in full above in Section II.B), the independent claims provide:

Claim 1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit . . .

said initialization circuit having a control circuit . . . and an enable circuit receiving . . . *externally applied further command signals*,

said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified

Claim 11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit . . . which comprises:

. . .

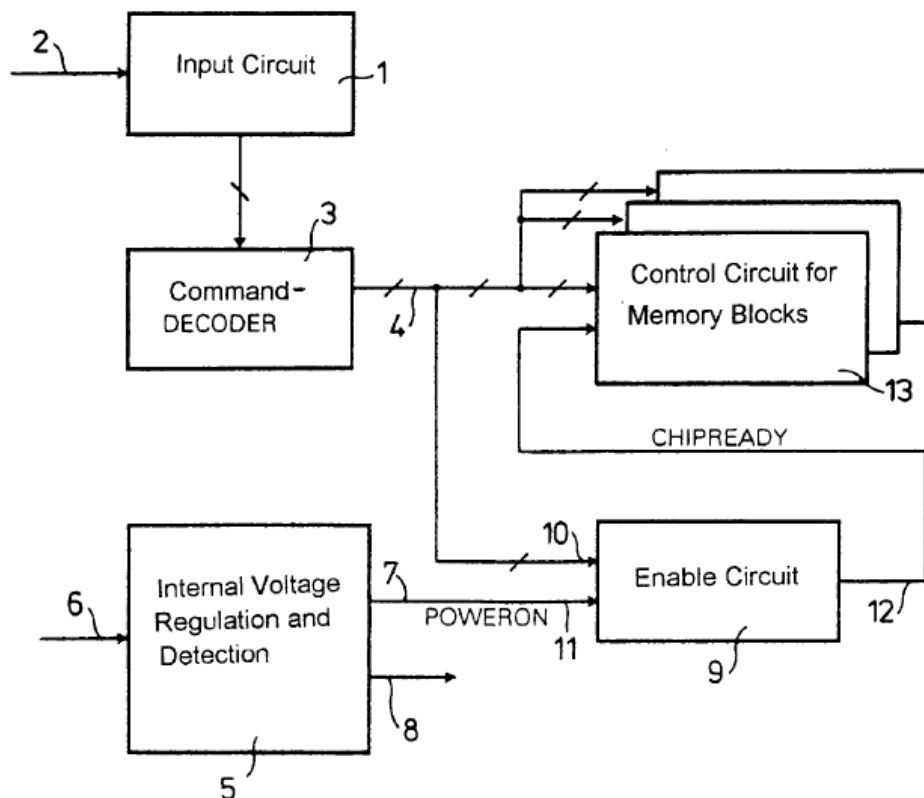
supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving . . . *further command signals externally applied* to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the *further command signals* the enable signal being generated

Ex.. 1001, Cls. 1 and 11 (emphasis added). Thus, as it relates to this term, the claims require that the claimed initialization circuit (or method for operating the same)

receives *externally applied further command signals* and then outputs an enable signal after identifying a proper initialization sequence of such *further command signals*.

To further understand what is meant by these “further command signals” in the claims, we next look to the specification and its description of the embodiments of the invention. The '589 Patent describes command signals, e.g., with reference to Figure 1:

Fig 1



Ex. 1001, Fig. 1.

Specifically, the '589 Patent states:

The initialization circuit has an input circuit 1, to whose input 2 *command* and clock *signals that are externally applied* in reference to the semiconductor memory are provided. The *command* and clock *signals* are amplified and conditioned before being received by a command decoder 3 connected downstream of the input circuit 1 and at whose output 4, inter alia, *the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command)* are output.

Ex. 1001 at Col. 3:51-61 (emphasis added). That is, the '589 Patent teaches that “command signals” are applied externally to the input of the initialization circuit, and those command signals (after amplification, conditioning and decoding) are used within the initialization circuit as “command signals” such as PRECHARGE (PRE), AUTOREFRESH (ARF), and MODE-REGISTER-SET (MRS). *See also* Ex. 2001 at ¶¶108-10.

The “command signals” PRE, ARF, and MRS would have been well known to a POSITA at the time of the invention, and indeed the '589 Patent specifically references them as commands that were described in the JEDEC standard, an industry standard for SDRAM semiconductor memories. *See, e.g.,* Ex. 1001 at Col. 1:22-61. Petitioner’s expert agrees that “[a] POSITA would have been familiar with JEDEC memory standards like JESD 21-C.” Ex. 1003 at ¶93. In the JEDEC

standards, such as JESD 21-C, these command signals are specified as particular patterns of individual signals. For example, the excerpt below from JESD 21-C describes the patterns for each of the commands PRE, ARF, and MRS:

SDRAM FUNCTION TRUTH TABLE

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	A_n	ACTION
IDLE	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL ²
	L	H	L	X	BA, CA	ILLEGAL ²
	L	L	H	H	BA, BA	Row (& Bank) active; Latch Row Address
	L	L	H	L	BA, A10	NOP ⁴
	L	L	L	H	X	Auto-Refresh ⁵
	L	L	L	L	Op-code	Mode Register Access ⁵

4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).

Ex. 1006 at 479-80 (annotated).

The JESD 21-C truth table above identifies the “Action” that occurs from the “Current State” (here, Idle) based on the pattern of individual signals applied to an SDRAM. The individual signals are $\overline{S}$, $\overline{RE}$, $\overline{CE}$, $\overline{W}$, and A_n . $\overline{S}$ is what is typically called Chip Select or Chip Enable, $\overline{RE}$ is row enable or RAS, and $\overline{CE}$ is Column Enable sometimes called CAS. *See* Ex. 1006 at 27, 29 (defining CAS/ $\overline{CE}$ (2.1.12), RAS/ $\overline{RE}$ (2.1.49), $\overline{S}$ /Chip Select (2.1.54); *see also* Ex. 2001 at ¶110; Ex. 2002 at 36:5-10 (Petitioner’s expert agreeing). $\overline{W}$ is write enable, and A_n refers to the address inputs. *See* Ex. 1006 at 27 and 30 ($\overline{W}$ (2.1.61) and $A(n)$ (2.1.2)).

Depending on the patterns of these various signals, different “Actions” are to occur according to the standard, which the ’589 Patent refers to as “command signals.” For example, the Actions highlighted within the red rectangles above correspond to the specific commands discussed in the ’589 patent. That is, “NOP⁴” corresponds to PRE or PRECHARGE according to footnote 4, Auto-refresh corresponds to ARF or AUTOREFRESH, and Mode Register Access corresponds to MRS or MODE-REGISTER-SET. Ex. 2001 at ¶110; *see also* Ex. 2002 at 37:12-38:15, 39:8-40:3 (Petitioner’s expert discussing the actions corresponding to ARF and MRS).

Accordingly, a POSITA would have understood that the command signals described in the ’589 Patent (with PRE, ARF, and MRS given as examples) are not the individual signals that comprise the pattern for those commands. Rather, one of ordinary skill in the art would understand that “externally applied further command signal” are “a pattern of individual external signals that as a group represent a command.” Ex. 2001 at ¶111. And, thus, “externally applied further command signals” or “further command signals externally applied” are “a plurality of command signals.” Ex. 2001 at ¶112.

This distinction is important for evaluating the challenged claims and the prior art as discussed in more detail below because identifying the appropriate sequence of command signals presents different issues than a sequence of the constituent

individual signals. In particular, different command signals have different patterns of the individual signals but they include those same individual signals. For example, as shown in the table above, all of the different commands depend on the values of S/chip select, RE/RAS, CE/CAS, and W/Write at a particular point in time. As Petitioner's expert has acknowledged:

14 Q. Okay. Yeah. The -- whichever command you
15 have, it's going to be based on a -- a pattern of
16 signals, right?

17 A. Yes.

18 Q. And both of those commands, Auto-Refresh
19 and Mode Register, they require -- as part of the
20 pattern of signals, it includes a RAS and CAS
21 signal, right?

22 A. Yes. They -- they require -- they -- in
23 this case they require those to both be low.

Ex. 2002 at 40:14-23. As Petitioner's expert further explained:

21 . . . I think what
22 you're asking is, would you expect AUTOREFRESH and
23 MODE-REGISTER-SET to be asserted simultaneously.
24 And you -- one wouldn't. One would expect the
25 decoder would say, okay, this is AUTOREFRESH action
1 that's occurring; and different pattern would cause
2 MODE-REGISTER-SET action.

Ex. 2002 at 41:21-42:2. Accordingly, the claimed invention's identification of a sequence of "command signals" is different from and would require different circuitry than an identification of a sequence of the constituent individual signals (i.e., control signals) that form a command signal.

V. APPLICABLE LEGAL STANDARDS

A. Anticipation

"[R]ejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in 'the prior art. . . .' The [prior art] reference must clearly and unequivocally disclose the claimed [invention] or direct those skilled in the art to the [invention] without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference." *In re Arkley*, 455 F.2d 586, 587 (CCPA 1972). Thus, "unless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102." *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

"To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive

matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.” *Continental Can Co. USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (citing *In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981)). “Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *Id.* at 1268–69 (quoting *Hansgird v. Kemmer*, 102 F.2d 212, 214 (CCPA 1939)).

B. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established; the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342

(Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

Additionally, it is improper to use the challenged claim as a roadmap to piece together disparate disclosure using hindsight bias. See *InTouch Techs., Inc. v. VGo Comm’ns., Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (reversing obviousness where “[i]t appears that [the expert] relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”).

2. A petition must address the Graham factors.

Obviousness is resolved on a number of factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” See *Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham

factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

VI. SUMMARY OF THE REFERENCES

Petitioner requests relief on eight or nine grounds. Petition at 3 (Grounds 1 through 8 with 3A and 3B). The Kocis or Lee reference serves as the primary reference in each of these grounds, and the two references are used together for dependent claims in one ground (#7). *Id.* These two primary references and the other secondary references are summarized below.

A. Overview of Primary Reference: Kocis

Petitioner relies on U.S. Patent No. 5,559,753 to Kocis as the primary reference in Grounds 1 and 2, and the Petition combines Kocis with Lee in Grounds 7 and 8. *See, e.g.*, Petition at 3. Kocis “relates to a system for preventing contention on the memory bus between conflicting data signals from two or more DRAM banks.” Ex. 1004 at Col. 1:12-15; *see also* Ex. 2001 at ¶¶50-62.

Kocis describes “a circuit for disabling DRAM data output signals, which counts the number of RAS (and/or CAS) signals received by the DRAM circuit.” *Id.* at Col. 3:42-44. “When seven RAS signals have been detected after a threshold voltage is achieved, the DRAM data output lines are enabled.” *Id.* at 3:44-47.

Petitioner relies on Figure 5 which Kocis describes as “a circuit. . . for disabling DRAM data output drivers until power supply voltages are satisfactory and all enable conditions are met.” *Id.* at Col. 4:23-26.

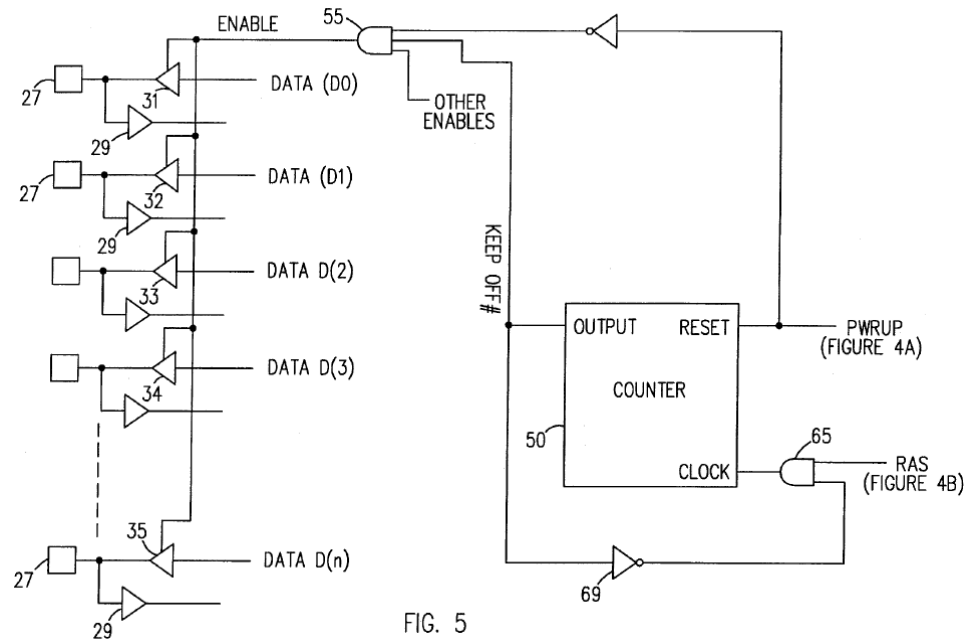


FIG. 5

Ex. 1004, Fig. 5.

Figure 5 includes “a plurality of tri-state output drivers 31, 32, 33, 34, 35 for driving data lines D0-Dn of a DRAM circuit 100, a counter 50, and an AND gate 55.” *Id.* at 4:33-38. “[T]he tri-state buffers transmit the associated data signal only when enabled by the ENABLE line” emanating from AND gate 55. *Id.* at 4:60-61. “The AND gate 55 receives the following input signals in the preferred embodiment: (1) an inverted Pwrup signal from the output of the voltage detection circuit of FIG. 4A; (2) an output signal (Keep Off) from counter 50; and (3) other enable signals.” *Id.* at 5:3-7.

In Kocis’s preferred embodiment, “the counter 50 counts the number of RAS signals received from the memory controller 8 (of FIG. 1).” *Id.* at Col. 5:40-42. The counter generates “an output signal (Keep Off)” after counting a number of RAS

and/or CAS signals. *Id.* at Col. 5:42-49. The “Keep Off” signal is supplied to AND gate 55 which also receives “an inverted Pwrap signal” and “other enable signals.” *Id.* at Col. 5:1-8. The tri-state buffers 31-35 are disabled while “AND gate 55 keeps the ENABLE line low.” *Id.* at Col. 5:22-28. Notably, neither the ENABLE signal nor the “Keep Off” signal is dependent on the sequence in which any other signals are received. The “Keep Off” signal counts the number of a particular signal, but not the sequence, and the sequence in which the AND gate 55 providing the ENABLE line (or any AND gate) receives its inputs does not have any effect on its output. *See* Ex. 2001 at ¶61.

B. Overview of Primary Reference: Lee

Petitioner relies on U.S. Patent No. 5,774,402 to Lee as the primary reference in seven of the grounds it asserts (#3A/3B through 8). *See, e.g.*, Petition at 3. The Japanese counterpart to Lee (JP 9-106668 to Tetsuka) is cited on the face of the ’589 Patent and was marked as considered by the Examiner. *See* Petition at 73; Ex. 1002 at 75; 93-98.

Lee “relates generally to initialization circuits for semiconductor memory devices and more particularly to initialization circuits which operate in response to an external control signal, thereby *providing reliable initialization when conventional power supply reset circuits malfunction.*” Ex. 1005 at 1:11-16 (emphasis added); *see also* Ex. 2001 at ¶¶63-73.

Lee describes how “[t]he typical power on reset circuit operates by sensing the level of the power supply voltage VCC and generating an initialization signal for a predetermined length of time when the power supply voltage reaches a predetermined level.” *Id.* at 1:25-29; *see also id.* at 1:30-2:3. Lee identifies “[a] problem with” such a typical/prior art initialization circuit in “that it may malfunction if the power supply voltage VCC is unstable input.” *Id.* at Col. 2:4-6. In such an instance, the initialization circuit may “fail[] to initialize the circuits within the chip.” *Id.* at 2:12-14. To address this problem, Lee discloses “an object of the invention [is] to reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions.” *Id.* at 2:18-20. “A further object of the invention is to initialize a semiconductor memory device in response to external logic signals.” *Id.* at 2:21-23.

Lee discloses an initialization circuit in Figure 3 that includes both first (46) and second (16) initialization signal generators that generate signals ϕ SET and ϕ INIT, respectively. *Id.* at Col. 3:9-20.

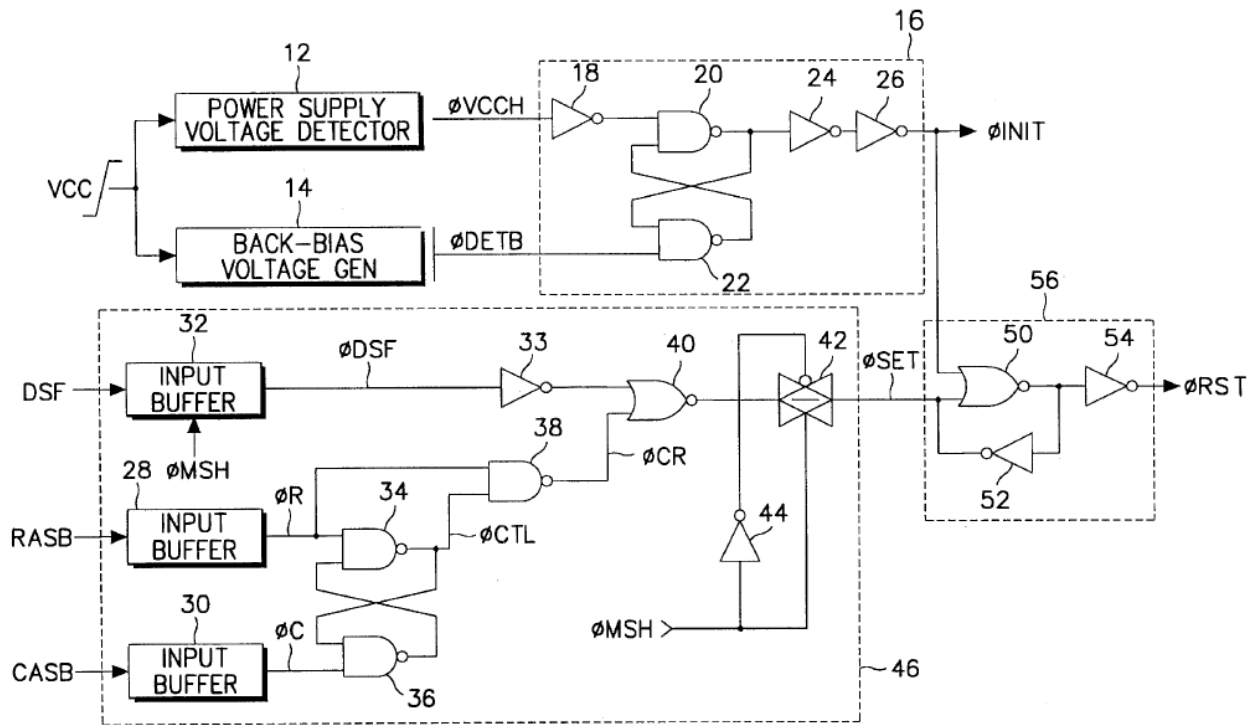


Fig. 3

Ex. 1005, Fig. 3.

“[T]he second initialization signal generator 16 activates the second initialization signal ϕINIT ” “[w]hen the power supply VCC is first powered-up” as in a typical power on reset circuit described in the background. *Id.* at Col. 4:25-31. “[T]he first initialization signal generator activates the first initialization signal ϕSET ” “if the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence.” *Id.* at Col. 4:38-41.

The outputs of the two initialization signal generators (16 and 46) are connected to transfer unit 56. *Id.* at Col. 4:14-20. “[T]he transfer unit 56 activates the reset signal ϕRST in response to the activation of either the first or second

initialization signals ϕSET or ϕINIT .” *Id.* at Col. 3:24-26; *see also id.* at Col. 3:31-33 (“the reset signal ϕRST is activated in response to either the power supply power-up or the reset information.”). The “reset signal ϕRST [is] for resetting a circuit within the memory device.” *Id.* at Col. 3:20-21. “Therefore, if the power-up reset circuit [providing the second initialization signal ϕINIT] malfunctions, the circuitry will still be properly initialized by the first initialization signal ϕSET .” *Id.* at Col. 3:33-35.

Lee goes on to disclose that initialization of circuits within the chip occurs when ϕRST is at a high-logic level. “When the power supply VCC is first powered-up, the second initialization signal generator 16 activates the second initialization signal ϕINIT as shown in FIG. 2, thus driving the second input terminal of NOR gate 50 to a high-logic level. ... The transfer unit 56 activates the reset signal ϕRST in response to the second initialization signal ϕINIT and latches the second initialization signal. Thus, all circuits within the chip which are connected to the output terminal of transfer unit 56 is held in the initialized state.” *Id.* at Col. 4:27-37.

In this way, Lee discloses an initialization circuit that addresses the problem it identifies in the prior art—the need for reliable initialization when a conventional power supply reset circuit malfunctions. *See, e.g., id.* at 1:11-16; 2:4-14. As described above, the circuit in Lee generates a reset signal ϕRST pulse to initialize

the circuit either based on activation of a conventional power-up circuit or in response to external logic signals. Notably, Lee does not disclose an enable signal that effects the unlatching of any control circuit.

C. Overview of Secondary References

Petitioner relies on two additional prior art references in addition to its primary references. A brief description of each follows.

1. JESD 21-C

Petitioner relies on JEDEC's Configurations for Solid State Memories, Standard No. 21-C, Release 7 (JESD 21-C) for its "recommended power on sequence." Ex. 1006 at 3.11.5-9 (p.483 of PDF). JESD 21-C explains that "both system and device designers *should strive* toward ensuring a High-Z output state during the initial power up sequence" and offers a "recommended power on sequence" to achieve that end. *Id.* (emphasis added); *see also* Ex. 2001 at ¶¶87-93.

JESD 21-C does not disclose any circuit or method for achieving this recommended power up sequence, nor does Petitioner allege that it does. The '589 Patent describes a JEDEC recommended sequence (*see* Ex. 1001 at Col. 1:43-61) in the same paragraph that explains that achieving JEDEC's goals for switch-on operation "turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the

external control inputs during the switch-on operation of the semiconductor memory.” *Id.* at Col. 1:22-35.

JESD 21-C also includes in its “recommended power on sequence” that “[t]he device is now in the IDLE state and is ready for normal operation.” Ex. 1006 at 3.11.5-9 (p.483 of PDF). This mirrors the acknowledgement in the ’589 Patent that “[a]fter the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and *prepared for proper operation.*” Ex. 1001 at Col. 1:62-65 (emphasis added). The ’589 Patent notes further, however, that in SDRAM modules “disclosed to date all the control circuits of the component have been *unlatched* only with the POWERON signal.” *Id.* at 1:65-2:1 (emphasis added). The JESD 21-C reference includes no recommendation for unlatching the control circuits after placing them in the IDLE state, and the Petitioner identifies none.

2. Iketani

Petitioner relies on U.S. Patent No. 5,703,510 to Iketani et al. as allegedly “illustrat[ing] and describe[ing] in detail the various circuits, including the control circuit, that receive and are initialized by [] an initialization signal.” *See, e.g.*, Petition at 59. Iketani “relates to a power on reset circuit.” Ex. 1007 at Col. 1:7; *see also* Ex. 2001 at ¶¶94-101.

Iketani is concerned with the problem caused “if the power supply voltage Vdd fluctuates significantly, it may possibly activate the power on reset signal /POR to the L level again even after initialization.” *Id.* at 1:59-62. To that end, Iketani describes various structures for generating a power on reset signal. *Id. generally.*

Iketani mentions “a control circuit 62 for controlling internal circuitry in response to a row address strobe signal RAS, a column address strobe signal CAS, an output enable signal OE, a write enable signal WE or the like” which can be “initialized in response to the power on reset signal.” *Id.* at Col. 5:12-15, 5:20-25. But, notably for purposes of this Response, Iketani does not disclose that the power on reset signal unlatches this control circuit for operation. Ex. 2001 at ¶101.

VII. THE CHALLENGED CLAIMS ARE PATENTABLE OVER THE ASSERTED GROUNDS

The Petition challenges claims 1, 2, and 8-13 of the '589 Patent on nine different grounds (numbered 1 through 8, with 3A and 3B). *See* Pet. at 3.

Ground from Petition	Claim(s) Challenged	35 U.S.C. §¹	Reference(s)
1	1, 9, 11, 13	102	Kocis
2	2, 8, 10, 12	103	Kocis, JESD 21-C
3A	1, 11	102	Lee
3B	1, 11	103	Lee

Ground from Petition	Claim(s) Challenged	35 U.S.C. §¹	Reference(s)
4	1, 11	103	Lee, Iketani
5	2, 8, 10, 12	103	Lee, JESD 21-C
6	2, 8, 10, 12	103	Lee, Iketani, JESD 21-C
7	9, 13	103	Lee, Kocis
8	9, 13	103	Lee, Iketani, Kocis

The Board's Institution Decision (Paper 12) was based on its determination that Grounds 3B, 4, 5, and 6 asserting obviousness with Lee as the primary reference had a reasonable likelihood of prevailing. Paper 12 at 28-29. The Board determined that the Petition did not demonstrate a reasonable likelihood of prevailing on Ground 3A asserting anticipation based on Lee (Paper 12 at 28 n.4), or any of the remaining Grounds 1, 2, 7, and 8 including Kocis (Paper 12 at 35-36). Accordingly, this response first addresses Grounds 3B, 4, 5, and 6 asserting obviousness over Lee, and

then the remaining Grounds which fail to demonstrate anticipation or obviousness at least for the reasons identified in the Institution Decision.¹

A. Grounds 3B, 4, 5, and 6: Lee and the Asserted Combinations Fail to Render the Challenged Claims Obvious.

Lee at least fails to disclose or render obvious the requirements of independent claims 1 and 11 that require receiving and identifying a sequence of “command signals” and outputting an enable signal “effecting an unlatching” of a control circuit. Neither Iketani nor JESD 21-C cure these deficiencies in Lee, and therefore the Grounds 3B, 4, 5, and 6 fail.

1. Lee Alone or in Combination with Iketani and/or JESD 21-C Fails to Render Obvious Receiving Or Identifying a Sequence of “Further Command Signals.” (Claim elements 1.2, 1.3, 11.2)

Lee discloses that its circuitry operates on “control signals.” Ex. 1005 at 2:27. Specifically, Lee discloses that these are “reset control signals DSF, RASB, and CASB.” Ex. 1005 at 3:15-16. Lee’s first initialization signal generator 46 responds directly to the logic states of these external control signals. These signals are control

¹ Patent Owner’s expert, Dr. Dorney, provides his opinions with respect to each asserted ground in order from Ground 1 through 8. *See* Ex. 2002 at Section X.C-J.

signals, and not command signals as properly construed in the '589 Patent. *See also* Ex. 2001 at ¶¶171-178, 193, 205.

As noted above, an “externally applied further command signal,” as claimed, is “a pattern of individual external signals that as a group represent a command.” *See* Section IV.A *supra*. Lee only discloses control signals. Lee is silent as to a command signal or command signals.

Petitioner’s expert takes the position that “[a] POSITA would recognize that these signals are command signals as they provide specific commands to the memory chip.” Ex. 1003 at ¶ 127.) The control signals DSF, RASB, and CASB disclosed in Lee are individual, external signals that control the internal operations of the memory device; however, the '589 Patent neither teaches nor claims *control signals*. Instead, the '589 Patent teaches and claims “command signals,” which are different than “control signals.” Ex. 2001 at ¶173. A “command signal” is “a pattern of individual external signals that as a group represent a command.” *See* Section IV.A *supra*.

Petitioner’s expert argues that “the CASB and RASB signals are further command signals because a POSITA would have understood that they *can be used to generate* the PRECHARGE, AUTOREFRESH, and MODE-REGISTER-SET commands disclosed in the '589 Patent.” Ex. 1003, ¶ 128 (emphasis added). Thus, Petitioner’s expert acknowledges that these signals are not, in and of themselves,

“command signals.” RASB and CASB, by themselves cannot generate the PRECHARGE, AUTOREFRESH, or MODE-REGISTER-SET commands. Ex. 1003 at ¶128. The command signals used in the ’589 Patent require control signals in addition to RASB and CASB. Ex. 2001 at ¶174. These commands also require chip select (S_ or CS_), write (W_ or WE_), a clock signal, a clock enable (CKE) signal, and row address and/or bank address for the PRECHARGE command. *Id.* Petitioner’s Expert acknowledged this fact in his declaration and at his deposition. Ex. 1003 at ¶128; Ex. 2002 at 37:12-40:17.

This distinction between Lee and the claims of the ’589 Patent cannot be dismissed as easily as swapping one type of signal for another. Petitioner’s expert has agreed that “command signals” are a pattern of signals, such that RAS and CAS signals discussed in Lee combined and evaluated with other signals to form a command as disclosed in the JESD 21-C standard. *See* Ex. 2002 at 37:14-17; Ex. 1006 at 479. And, these control signals are included in the patterns of signals that represent the different command signals. *See* Ex. 1006 at 479-80. That is, only one command signal can be asserted at a time given that each command is dependent on the same constituent signals (though different patterns thereof). Ex. 2002 at 41:21-42:2. As such, Petitioner’s assertion regarding Lee would require additional circuitry to obtain and keep track of the “command signals” supplied by the various combinations of control signals, and then be able to identify the appropriate

predetermined sequence as required by the independent claims of the '589 Patent. There is no such disclosure, suggestion, or even identification of such a problem in Lee, nor has Petitioner's expert provided any basis to so modify Lee.

In other words, independent claims 1 and 11 require "a predetermined proper initialization sequence of the [externally applied] further command signals." Command signals, when properly construed, requires "a pattern of individual external signals that as a group represent a command." To have a sequence of commands, each command must be recognized to be able to determine if "a predetermined proper initialization sequence" of those commands has occurred. Lee completely fails to show or suggest "command signals." Lee only discloses control signals. Furthermore, Lee contemporaneously uses the control signals during a single CAS-before-RAS cycle to elicit a response with his logic (Lee, Figs. 3-4), but completely fails to recognize a pattern (i.e., command signal) such that a sequence of patterns can be evaluated to determine if the command signals are in a proper sequence as required by the claims.

Neither Iketani nor JESD 21-C cure this issue in Lee or provide any basis to modify Lee to adapt its circuit operating on control signals to identify a sequence of

“further command signals” as claimed in the ’589 Patent. Accordingly, Grounds 3B, 4, 5, and 6 must fail for at least this reason.

2. Lee Alone or in Combination with Iketani Fails to Render Obvious An Enable Signal “Effecting An Unlatching of [a/said] Control Circuit.” (Claim elements 1.3 and 11.2)

The ’589 Patent independent claims require “the enable signal [...] effecting an unlatching of [said/a] control circuit.” Ex. 1001, Cls. 1 and 11 (brackets indicating minor differences between the two claims). The ’589 Patent teaches a CHIPREADY signal that starts at a low logic level upon application of a supply voltage, and the CHIPREADY signal transitions to a logic high-level after identifying “a predetermined proper initialization sequence of the externally applied further command signals” as claimed. *See, e.g.*, Ex. 1001 at 4:49-58 (the enable circuit of the preferred embodiment generates the enable signal CHIPREADY when a predetermined sequence of command signals is detected and “[o]nly then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY”); Fig. 3. Figure 3 in the ’589 Patent shows how the CHIPREADY

signal transitions from low to high following the identification of the proper sequence of command signals:

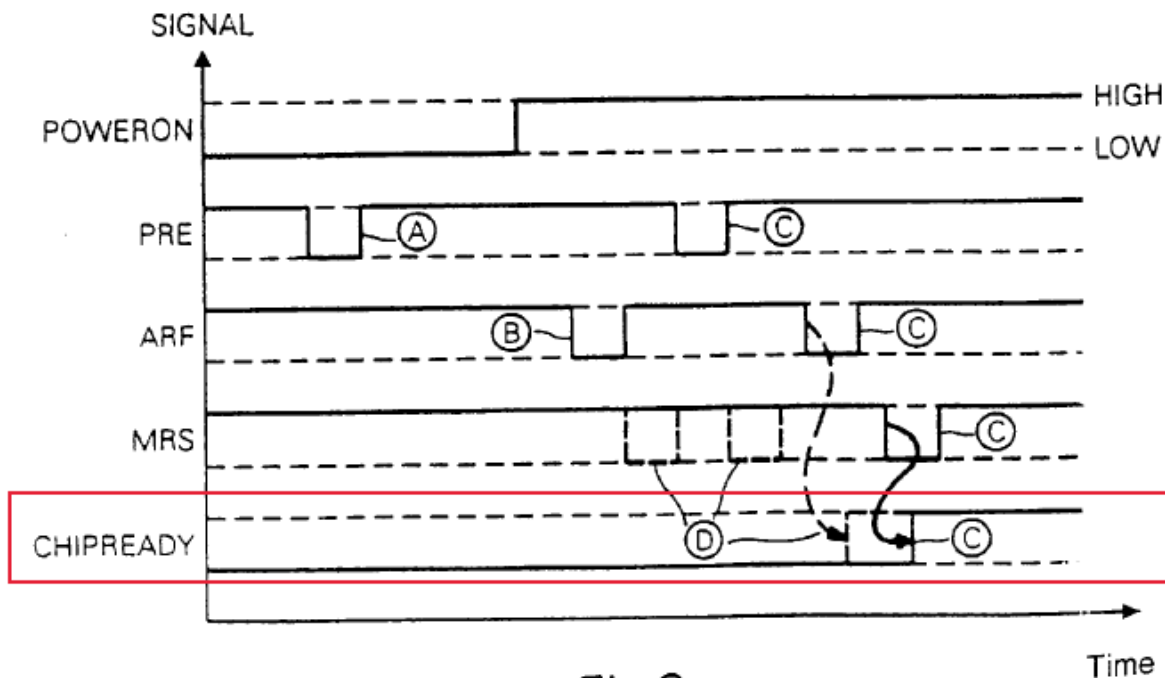


Fig 3

Ex. 1001, Fig. 3 (annotated). The requirement of the claims can be understood in the context of the '589 Patent's embodiments that this signal transitioning from one state to another effects an "unlatching." Ex. 2001 at ¶179. Lee, in contrast, discloses a pulse which, setting aside its operation depending on control signals as opposed to command signals, transitions a ϕ RST signal from low-to-high-to-low "thereby

initializing the circuits within the chip. *See* Ex. 1005 at Col. 4:59-5:4. This pulse for ϕ RST is shown below in Lee's Figure 4:

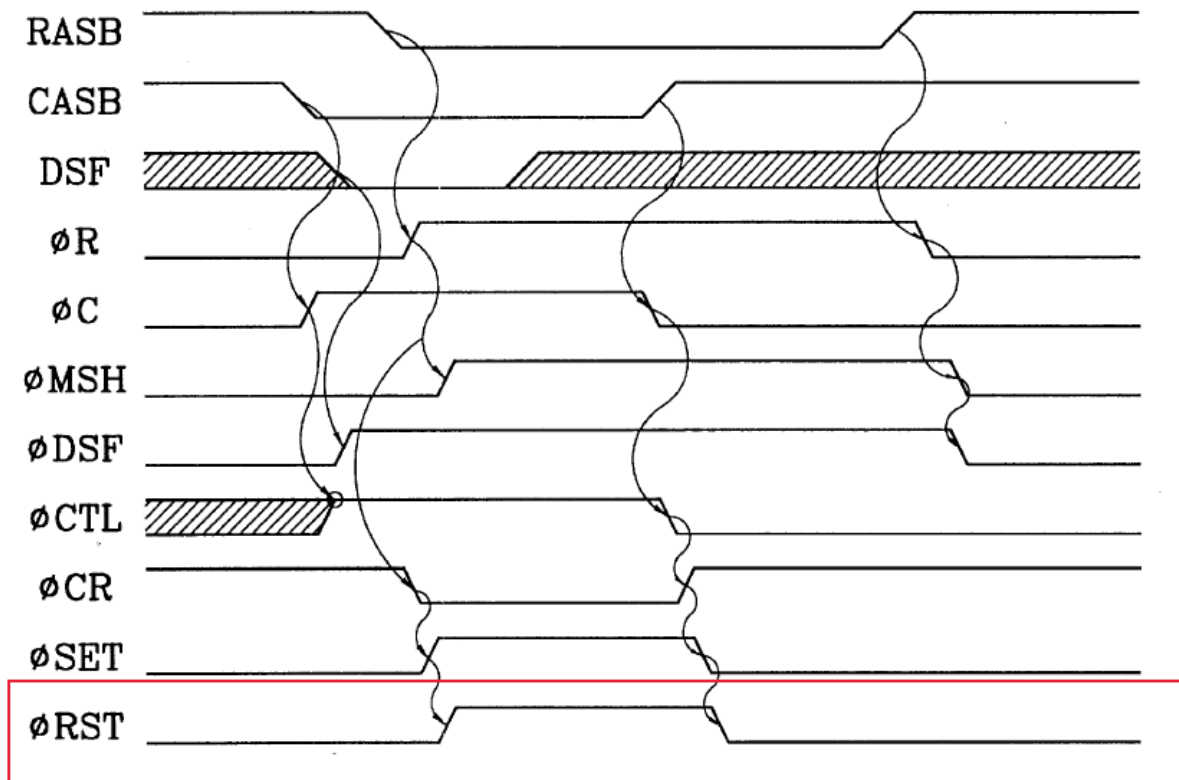


Fig. 4

Ex. 1005, Fig. 4 (annotated). Lee neither describes this as “unlatching” any circuits for operation (as opposed to “initializing”) nor that the circuits were latched prior to activation of this pulse. Ex. 2001 at ¶180. And, even if one were to assume the circuits were latched, then a pulse signal would imply that upon the signal’s return to its original state, latching would be reenabled, which would disable normal operation. Ex. 2001 at ¶181. For example, Lee openly states that initialization occurs

when ϕ RST is at a high-logic level. Ex. 1005, 4:27-37. Petitioner argues that initializing is the same as unlatching. By extension, Petitioner's argument would mean latching is reenabled when ϕ RST is at a low-logic level, which would disable normal operation. Ex. 2001 at ¶184.

Lee discloses initializing a circuit with ϕ RST, but is silent as to unlatching (or even latching). "Initializing" and "unlatching" are not the same. Ex. 2001 at ¶183. Even Petitioner's expert seems to acknowledge this, arguing a POSITA would understand "that every sequential circuit (a circuit that maintains state), such as a control circuit, needs a reset mechanism to ensure that it powers up in a known state. Powering up sequential logic without *initialization* could lead to an unknown state and unpredictable operation." Ex. 1003, ¶130, emphasis added.) Petitioner's expert is silent as to how initializing a sequential circuit is equivalent to the claimed "unlatching." Ex. 2001 at ¶183. At best, Petitioner equates "unlatching" to "initializing" by (1) conclusory statement, and (2) quoting Lee's statements about initializing. Ex. 2001 at ¶183. Nowhere is the two-state condition (latched and unlatched) taught by the '589 Patent addressed with respect to the low-high-low logic level ϕ RST signal pulse in Lee. Ex 2001 at ¶183.

Furthermore, Lee may generate a ϕ RST signal pulse multiple times during power up and during normal operation. Ex. 2001 at ¶184. Petitioner's expert acknowledged that any time the circuit in Lee received those control signals, it would

pulse ϕ RST and obtain the attendant initialization. *See* Ex. 2002 at 27:6-28:6. This is in contrast to the '589 Patent's claimed unlatching, exemplified by the preferred embodiment's CHIPREADY signal which transitions and remains at a high state following the proper initialization sequence. *See* Ex. 1001, Fig. 4. In fact, Lee's Fig. 3 has been analyzed to understand its operation when RASB, CASB, and DSF transition differently than the single example provided by Lee in Fig. 4. RASB, CASB, and DSF are control signals that regularly transition during normal (i.e., after power-up) operation. *See* Ex. 2001 at ¶¶80-83. Depending on race conditions, Lee's circuit in Fig. 3 may cause the ϕ RST signal to pulse during normal operation. If Petitioner is to be believed, then Petitioner is also stating that latching during normal operation could occur, which would disrupt I/O operations on the memory device. Ex. 2001 at ¶184.

This distinction between Lee's ϕ RST signal and the '589 Patent's claimed enable signal demonstrates that Lee does not disclose a signal capable of performing the function of the claimed enable signal and effecting an "unlatching." Nor does combining Lee's pulsed signal with any other "power-on reset" art (such as Iketani) address how to modify Lee's signal in order achieve the '589 Patent's requirements regarding unlatching.

Petitioner's expert contends that his reading of Lee and its combination with other art like Iketani disclose the claimed "unlatching" because of what he contends

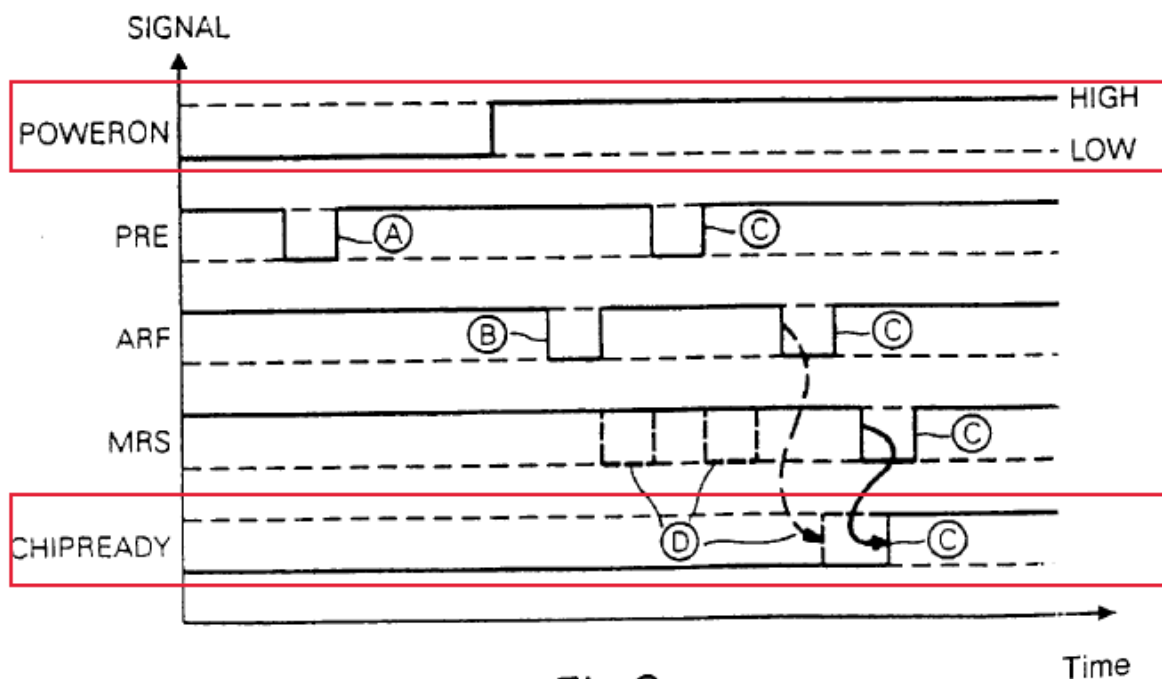
is understood by a “power-on reset.” *See* Ex. 2002 at 59:10-12. As Petitioner’s expert explains:

3 . . . Power-on reset
4 circuits are well known. And what they do is they
5 initialize circuits, and they also have a delay
6 associated with power -- with power supply reaching
7 a voltage. And so they -- they hold circuits in a
8 reset state until it's safe to release them, and
9 then they do. So it's -- it accomplishes a reset
10 and a release when power's applied.

Ex. 2002 at 60:3-10. But, Petitioner’s expert acknowledges that such circuits should not interfere with operation after power-up and “typically . . . it’s only used on power-up.” Ex. 2002 at 60:11-22 (also agreeing that “you wouldn’t want it [power-on reset] to interfere with operation”). Petitioner and its expert have also relied on the ’589 Patent’s general statement that:

In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

Ex. 1001, 1:65-2:5. But, they ignore that the power-on reset as described in the '589 Patent is based on a transition, i.e. not a pulse, just like the '589 Patent's CHIPREADY or enable signal as shown in Figure 3:



Ex. 1001, Fig. 3 (annotated). The point being that a power-on reset, as Petitioner's expert acknowledges, must change the state of the circuit to "unlatch" it and maintain that state for normal operation. Lee's pulse is not designed to perform that function, could not without additional modification, and Petitioner's attempts to assert that the circuit in Lee can simply be plugged into any power-on reset fails to demonstrate that the claimed "unlatching" would occur. Petitioner's conclusory assertions that it would is based on hindsight bias viewing the art through the lens of the '589 Patent invention.

There is nothing in Iketani that suggests that providing the pulse from Lee would effect an “unlatching” as claimed. Iketani merely states that its “power on reset signal” is supplied to “control circuit 62” and other circuits which are “initialized in response to the power on reset signal.” Ex. 1007 at 5:20-26. There is nothing in Iketani to disclose or suggest that supplying Iketani’s control circuit with the pulse from Lee instead of Iketani would effect an unlatching. *See* Ex. 2001 at ¶¶198-99. In fact, Iketani’s Figs. 2, 7, or 8 appear to be a replacement for Lee’s Fig. 1 used in Fig. 3. At best, Lee and/or Iketani disclose *initialization* during power-on reset, but are completely silent as to the claimed “unlatching.”

Thus, neither Iketani nor JESD 21-C cure this issue in Lee or provide any basis to modify Lee to adapt its pulsed ϕ RST signal to effect an “unlatching” of a control circuit as claimed in the ’589 Patent. Accordingly, Grounds 3B, 4, 5, and 6 must fail for at least this additional reason.

B. Ground 3A: Lee Does Not Anticipate Either of the Independent Claims.

The Board’s Institution Decision correctly noted that the Petitioner failed to demonstrate a reasonable likelihood of prevailing on its anticipation Ground 3A based on Lee at least because the Petition relied on a modification of Lee. *See* Paper 12 at 288 n.4. Additionally, because Lee fails to disclose (or even suggest) the

limitations discussed above in Section VII.A, Lee cannot anticipate at least independent claims 1 and 11 of the '589 Patent. *See also* Ex. 2001 at ¶¶170-90.

C. Grounds 1 and 2: Kocis Fails to Anticipate or Render Obvious the Challenged Claims.

1. Kocis Does Not Anticipate Either of the Independent Claims.

The Board previously found that Petitioner's asserted Grounds based on Kocis did not demonstrate a reasonable likelihood of proving that Kocis anticipates challenged claims. Paper 12 at 35. As explained therein, neither of Petitioner's purported "enable signals" disclose an enable signal as claimed in the independent claims of the '589 Patent. Additionally, Kocis fails to disclose the use of "externally applied further command signals" as properly construed herein for the same reasons explained with respect to Lee. *See also* Ex. 2001 at ¶¶114-17; 119-20. Kocis further does not detect any sequence of signals—it instead counts the number of times one control signal is received. Ex. 2001 at ¶121. Kocis also fails to disclose the claimed unlatching. Ex. 2001 at ¶¶122-28. For any one of these reasons, Kocis cannot anticipate the independent claims or claims 9 and 13 that depend from them, and asserted Ground 1 must fail.

2. JESD 21-C Does Not Cure Any of the Issues Identified in the Independent Claims.

JESD 21-C does not cure any of the issues identified in Kocis or provide any basis to modify Kocis to address these issues. Ex. 2001 at ¶¶145-50. Nor does

Petitioner so allege. Accordingly, Ground 2 addressed to the additional dependent claims must likewise fail.

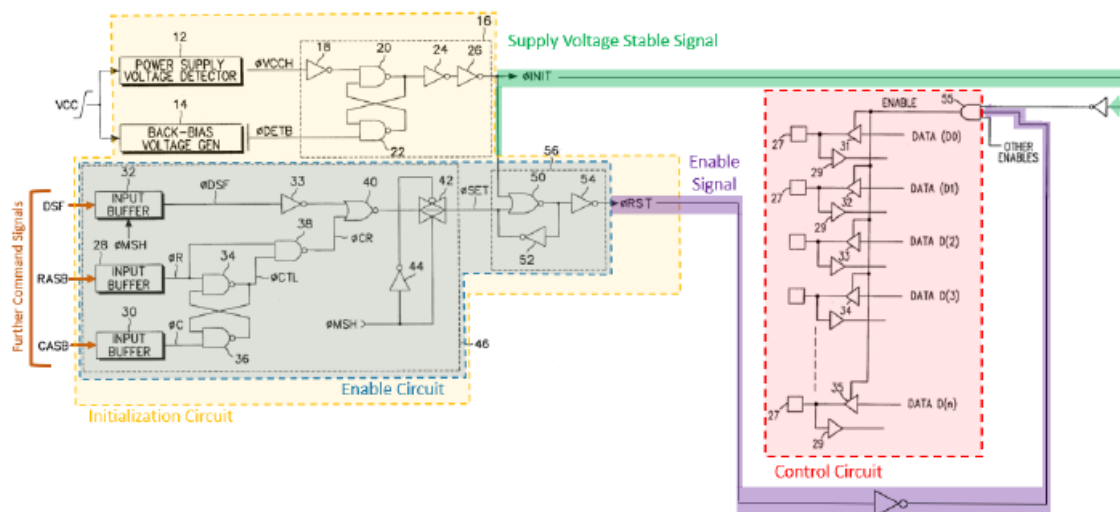
D. Grounds 7 and 8: The Addition of Kocis to Lee or Lee in Combination with Iketani Fails to Render Obvious Dependent Claims 9 and 13.

The Board previously found that Petitioner's asserted Grounds adding Kocis to Lee or Lee and Iketani did not demonstrate a reasonable likelihood of proving that dependent claims 9 or 13 were obvious. Paper 12 at 36. Moreover, Kocis does not, and is not alleged to, cure the deficiencies identified above in Section VII.A regarding the application of Lee or Lee and Iketani to the independent claims. For at least these reasons, dependent claims 9 and 13 cannot be rendered obvious through the addition of Kocis.

First, Petitioner advocated simply combining Lee and Kocis. Pet. at 67. Lee discloses a low-high-low logic level ϕ RST pulse as an output. Kocis discloses a low-to-high logic level KEEP OFF# signal as an output of the enable circuit as identified by the Petitioner. These two signals act differently. Lee's ϕ RST pulse (as designed) may pulse several times due to power-on reset and normal operation. According to Petitioner, a POSITA would use Lee's low-high-low logic level ϕ RST pulse to drive the three-input AND gate 55 of Kocis. Accordingly, as soon as the ϕ RST signal returns low, the tristate buffers of Kocis will be disabled (go to tristate) during *normal operation* after power up. Ex. 2001 at ¶256. This would obviously

not be the desired function and would fail to render obvious these dependent claims including because it would not satisfy the independent claims’ “unlatching” limitations discussed above.

Second, the Petitioner has constructed a circuit by cobbling together these references as reproduced below:



Kocis and Lee Combination

Pet. at 69 (annotations in original). In Petitioner’s circuit (above) both the potentially malfunctioning ϕ INIT signal (according to Lee) and the ϕ RST signal are inverted to solve the problem of non-functionality detailed immediately above. However, in doing so, Petitioner has created a circuit that enables the tristate buffers at power up, which has no ability to prevent bus contentions. Ex. 2001 at ¶257. Preventing bus contentions was the entire problem attempted to be solved by Kocis. Again, this would obviously not be the desired function and would fail to render obvious these

dependent claims because it would not satisfy the independent claims’ “unlatching” limitations discussed above.

For at least these reasons, Petitioner’s proposed combination of Lee and Kocis under Ground 7 cannot render claims 9 or 13 obvious.

The addition of Iketani to the above combination does nothing to address these issues noted for the Lee and Kocis combination. Petitioner relies entirely on cross-references to arguments for the independent claims. Pet. at 71-72. Accordingly, Ground 8 must also fail. *See also* Ex. 2001 at ¶¶272-92.

VIII. CONCLUSION

For the reasons above, Petitioner failed to demonstrate by a preponderance of the evidence that any of Grounds 1 through 8 render any of the independent challenged claims anticipated or obvious. Because each of the dependent claims depend from valid independent claims, Petitioner has failed to demonstrate that Grounds 1, 2, 5, 6, 7, or 8 render any of the challenged dependent claims anticipated or obvious as well. The Board should find in favor of Patent Owner and uphold the validity the of the challenged claims.

Dated: December 11, 2023

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 9,071 words, excluding the parts of this Patent Owner's Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Response.

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Response was served on December 11, 2023, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

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