

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner

Case No.: IPR2023-00516
Patent No.: 6,157,589
For: Dynamic Semiconductor Memory Device and Method for Initializing a
Dynamic Semiconductor Memory Device

DECLARATION OF TIMOTHY D. DORNEY, PH.D.

PURSUANT TO 37 C.F.R. § 1.68

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LISTING OF CHALLENGED CLAIMS

Claim 1	
[1.P]	A dynamic semiconductor memory device of a random access type, comprising:
[1.1]	an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation,
[1.2]	said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals,
[1.3]	said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.
Claim 2	
[2]	The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.
Claim 8	
[8]	The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

Claim 9	
[9]	The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.
Claim 10	
[10]	The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal.
Claim 11	
[11.P]	An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:
[11.1]	supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and
[11.2]	supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

Claim 12	
[12]	The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.
Claim 13	
[13]	The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

I, Timothy D. Dorney, Ph.D., do hereby declare:

I. INTRODUCTION

1. I am making this declaration (“Declaration”) at the request of Patent Owner Polaris Innovations Limited (“Polaris”) in the matter of the *Inter Partes* Review No. IPR2023-00516 of U.S. Patent No. 6,157,589 (“the ’589 Patent”).

2. I have been asked to consider whether or not a person of ordinary skill in the art (“POSITA”) would have found the invention in the ’589 Patent as set forth by the issued claims 1, 2, 8, 9, 10, 11, 12, and 13 are anticipated and/or obvious in light of the material made available to me in this case.

3. In this declaration, I set forth my opinions concerning the general subject matter of the issued claims in the ’589 Patent, including the state of the art in DRAM memory design in the 1990s. My opinions are based on my knowledge, education, experience, and a review of the material provided to me in this case.

4. I understand that the PTAB has instituted an *Inter Partes* Review of claims 1, 2, 8, 9, 10, 11, 12, and 13 of the ’589 Patent based on the arguments presented in the Petition (IPR2023-00516, Document 2) as supported by the Declaration of Dr. Stephen W. Melvin (IPR2023-00513, Ex. 1003) (“the Melvin Declaration”). Claims 1 and 11 are independent claims.

5. I understand that nine grounds for challenging the patentability of the claims were presented (numbered 1 through 8 with 3A and 3B). The first ground

challenged claims 1, 9, 11, and 13 as anticipated over U.S. Patent No. 5,559,753 to Kocis (“Kocis”). The second ground challenged claims 2, 8, 10, and 12 as obvious over Kocis in view of the JEDEC STANDARD, Configuration for Solid State Memories, Compilation of Releases 1 through 7, dated January 1997 (“JESD 21-C”). The third ground (including 3A and 3B) challenged claims 1 and 11 as anticipated or obvious over U.S. Patent No. 5,774,402 to Lee (“Lee”). The fourth ground challenged claims 1 and 11 as obvious over Lee in view of U.S. Patent No. 5,703,510 to Iketani et al. (“Iketani”). The fifth ground challenged claims 2, 8, 10, and 12 as obvious over Lee in view of JESD 21-C. The sixth ground challenged claims 2, 8, 10, and 12 as obvious over Lee in view of Iketani and JESD 21-C. The seventh ground challenged claims 9 and 13 as obvious over Lee in view of Kocis. The eighth ground challenged claims 9 and 13 as obvious over Lee in view of Iketani and Kocis.

6. I reserve the right to supplement or amend this Declaration based on any additional information that becomes known that affects my opinions.

7. I am being compensated for my work in this matter at an hourly rate of \$400 for consulting services. My compensation for this matter is neither determined by nor contingent on the outcome of this case.

II. PROFESSIONAL BACKGROUND

8. I earned a Bachelor of Science degree in Electrical Engineering from Texas A&M University in College Station, Texas, in 1990.

9. I earned a Master of Science degree in Electrical Engineering and Applied Physics from Case Western Reserve University in Cleveland, Ohio, in 1992.

10. I earned a Doctor of Philosophy degree in Electrical and Computer Engineering from Rice University in Houston, Texas in 2002.

11. I have extensive experience with semiconductor dynamic random access memory design and architecture. I was employed by Texas Instruments Incorporated in the Memory Products Group from 1988 to 1998. During that time, I was an engineer in the Circuits Center of Expertise, an integrated circuit design engineer, and a product development engineer.

12. The goal of the Circuits Center of Expertise was to investigate issues and provide solutions for future circuit designs that would be common across multiple devices.

13. As an integrated circuit design engineer, I worked on application specific memory designs for numerous devices including Video Random Access Memory (VRAM) and Synchronous Random Access Memory (SDRAM). As a DRAM memory designer, I was responsible for circuit design, circuit layout, and

pre- and post-silicon verification. Design areas included row and row redundancy, column and column redundancy, design-for-test, I/O buffers, internal refresh, and data I/O. I performed full-chip schematic verification, design rule verification, and probe versus simulation comparison. I supported the lead frame design, ESD implementation, parasitic back annotation, laser repair, and device layout and routing.

14. I supported the identification and solution for design issues encountered by video card/graphics processor design companies. As a product development engineer, I also used memory device testing systems to investigate memory device parameter characterization and failure mechanisms.

15. While employed at Texas Instruments Incorporated (TI), I traveled to Japan (KTI) and Singapore (TECH) to provide DRAM design support and training. I also traveled to TI-Singapore for DRAM T3/batch testing support. The training educated engineers about the new design functionality and test capabilities of forthcoming devices. Also, I was tasked with leading a team to create internal training materials on the basics of DRAM operation and to provide on-site training to TI's worldwide locations.

16. In 1998, I left Texas Instruments Incorporated to pursue my Doctor of Philosophy degree full-time. During my time at Rice University, I investigated processor design and researched the effects of modifying DRAM parameters on the

processing system; I investigated improvements to wavelet-based image compression; and I investigated computed tomography and methodologies to improve imaging.

17. My thesis research involved material parameter estimation and imaging using terahertz frequency waves. The terahertz frequency band is above the microwave frequency band and below the infrared frequency band. This research, using a fiber optic coupled, terahertz time-domain spectroscopy system, often centered on providing computer calculated graphical and synthetic image representations resulting from solutions of inverse problems.

18. Upon completion of the Ph.D. degree requirements, I was employed by Rosenthal & Osha L.L.P., to draft and prosecute patent applications. Major clients included Sun Microsystems, which was a processor and computer manufacturer, and NASA's Johnson Space Center. In 2003, I started working in patent licensing, first at Texas Instruments Incorporated and then at Personalized Media Communications, LLC, which has involved investigating patents and products from technical fields including DRAM and nonvolatile memory, analog circuits, image sensors, digital displays, processors, digital systems, video streaming, and Internet communications.

19. Beginning during my Bachelor of Science degree, I have experimented and designed multiple systems using embedded microcontrollers,

including Motorola's 68HC11 (BUFFALO development system), Texas Instruments MSP430, Microchip's PIC, and ARM's RP2040.

20. In 2005, I formed a company to focus on an optical delay system that would be relevant to the terahertz systems involved in my Doctor of Philosophy research. In 2009, the name of the company was changed to Uviri, LLC, as my interests expanded to basic research, development of consumer products, photography, and consulting. Many of the consumer products designs require an embedded microcontroller to support the desired operation. During my work at Uviri, LLC, I have also been involved in 2D image editing including layering and masks using Photoshop, and 3D photo-realistic rendering using Keyshot.

21. I am a member of the Institute of Electrical and Electronics Engineers (IEEE). I am a member of the IEEE honor society Eta Kappa Nu, the engineering honor society Tau Beta Pi, and the Phi Kappa Phi honor society. I passed the Texas Board of Professional Engineers and Land Surveyors: Fundamentals of Engineering exam while pursuing a Bachelor of Science degree in Electrical Engineering from Texas A&M University. In 2002, I became a registered patent agent. I am listed as an inventor on at least ten domestic or foreign patents. The subject matter of the majority of these inventions includes improvements to the performance and/or capabilities of dynamic random access memory.

22. A more complete summary of my background, qualifications, and professional experience and affiliations is set forth in my *curriculum vitae*, which is attached hereto as Appendix A, and includes a list of my patents and publications. Also included in my *curriculum vitae* is a complete list of the cases in which I have testified as an expert or have been deposed.

III. MATERIALS REVIEWED AND RELIED UPON

23. In the course of preparing this Declaration, I reviewed the following documents:

- Petition for *Inter Partes* Review of U.S. Patent No. 6,157,589 (“Petition”)
- Ex. 1001 U.S. Patent No. 6,157,589 (“the ’589 Patent”)
- Ex. 1002 Prosecution history of the ’589 Patent (“Application”)
- Ex. 1003 Declaration of Dr. Stephen W. Melvin (“the Melvin Declaration”)
- Ex. 1004 U.S. Patent No. 5,559,753 to Kocis (“Kocis”)
- Ex. 1005 U.S. Patent No. 5,774,402 to Lee (“Lee”)
- Ex. 1006 JEDEC STANDARD, Configurations for Solid State Memories, Compilation of Releases 1 through 7, dated January 1997 (“JESD 21-C”)
- Ex. 1007 U.S. Patent No. 5,703,510 to Iketani et al. (“Iketani”)
- Patent Owner’s Preliminary Response for IPR2023-00516
- Decision Granting Institution of *Inter Partes* Review for IPR2023-00516 (“Institution Decision”)

- Ex. 2002 Deposition of Stephen W. Melvin, Ph.D. (Nov. 21, 2023)

IV. LEGAL STANDARDS

24. I am not an attorney. I have been advised of the following general principles of patent law to be considered in formulating my opinions as to whether the claims of the '589 Patent would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the invention in view of the prior art.

A. Anticipation

25. I understand that a prior art reference anticipates a claim if every limitation of the claimed invention is found in a single prior art reference, either expressly or inherently, arranged as in the claim. I understand that a claim element is inherent in a prior art reference if it is "necessarily present" in the disclosed apparatus, system or method, not merely probably or possibly present. I understand that a patent claim cannot be anticipated by a prior art reference if the allegedly anticipatory disclosures in the reference are not enabled. I understand that merely naming or description of the subject matter is insufficient if it cannot be produced without undue experimentation.

B. Obviousness

26. I understand that a prior art reference can render a patent claim obvious to one of ordinary skill in the art if the differences between the subject matter set forth in the patent claim and the prior art are such that the subject matter

of the claim would have been obvious at the time the claimed invention was made. In analyzing obviousness, I understand that it is important to consider the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any secondary considerations.

27. I understand that when the claimed subject matter involves combining preexisting elements to yield no more than one would expect from such an arrangement, the combination is obvious. I also understand that in assessing whether a claim is obvious, one must consider whether the claimed improvement is more than the predictable use of prior art elements according to their established functions. I understand that there need not be a precise teaching in the prior art directed to the specific subject matter of a claim because one can take account of the inferences and creative steps that a person of ordinary skill in the art would employ. I further understand that a person of ordinary skill is a person of ordinary creativity, not an automaton. However, I understand that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art. I also understand that a combination is not obvious if it requires extensive additional problem-solving steps that are not taught in the references and that are not simple matters for a person of ordinary skill in the art. That is, a

combination is not obvious if it requires the development of an additional complex infrastructure.

28. I understand that, when there is a reason to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. I further understand that, if this leads to the anticipated success, it is likely the product, not of innovation, but of ordinary skill and common sense, which bears on whether the claim would have been obvious.

C. Claim Construction Standard

29. It is my understanding that in determining whether a patent claim is anticipated or obvious in view of the prior art, the PTAB must construe the claim using the federal court claim construction standard that is used to construe a claim in a civil action under 35 U.S.C. § 282(b). This is the same claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) (“*Phillips*”), and its progeny.

30. The *Phillips* standard requires the claims be given their ordinary and customary meaning to a person of ordinary skill in the art at the time of the invention, by considering the claims, specification, and prosecution history, as well as evidence extrinsic to the patent, when construing patent claims.

31. For the purposes of this Declaration, unless otherwise stated, I have construed each claim term in accordance with the *Phillips* standard.

V. THE '589 PATENT

32. The '589 Patent was filed as U.S. Application No. 09/343,431 on June 30, 1999, and was issued as U.S. Patent No. 6,157,589 to Gunnar Krause on December 5, 2000. The '589 Patent claims a foreign application priority to German Application DE 198 29 287 A1 filed June 30, 1998. The '589 Patent is entitled "Dynamic Semiconductor Memory Device and Method for Initializing a Dynamic Semiconductor Memory Device."

A. Overview of the '589 Patent Background

33. As explained in the Background of the '589 Patent, the invention is generally concerned with "a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit components." (Ex. 1001, 1:9-13.) The "switching-on operation" is necessary so that "the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called 'bus contention' or 'data contention') or uncontrolled activation of internal current loads." (Ex. 1001, 1:24-30.) To

properly perform the “switching-on operation,” the JEDEC standard recommends a specific initialization sequence. The ’589 Patent Background states that “[i]n the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.” (Ex. 1001, 1:65-2:5.)

34. In other words, the ’589 Patent discloses that the POWERON signal keeps internal circuits latched when external power is first applied to a memory device. When “the internal supply voltages have reached the necessary values,” the POWERON signal is made active and the internal control circuits are unlatched.

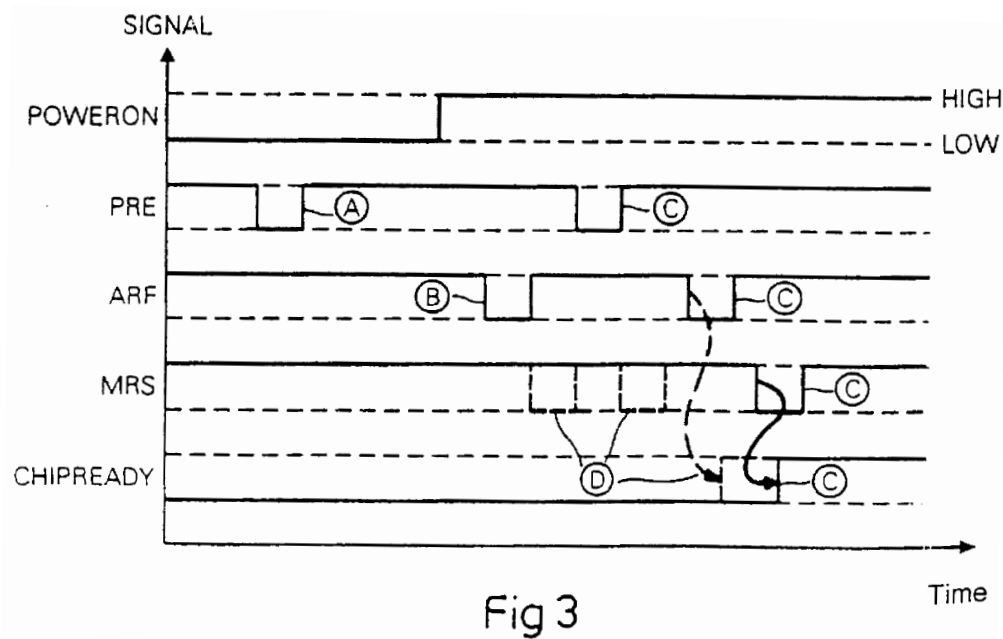
35. Accordingly, the memory device may not function properly if the POWERON circuit does not operate as intended because internal control circuits may remain latched. The ’589 Patent teaches an improved circuit to guarantee proper “switching-on operation,” which is dependent on more than just the POWERON signal.

B. The '589 Patent Invention

- 1. The '589 Patent teaches “said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified”.**

36. Claim element 1.3 of the '589 Patent requires, “said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.” Breaking claim element 1.3 down, claim element 1.3 requires (1) the enable circuit outputs an enable signal, after (2) the enable circuit identifies a predetermined proper initialization sequence of the externally applied further command signals, and (3) the enable signal effects an unlatching of the control circuits.

37. The '589 Patent teaches that the enable circuit identifies whether externally applied command signals occur in a predetermined proper initialization sequence. To that end, the '589 Patent provides an example timing diagram in Fig. 3 (reproduced below).



38. Externally applied command signals cause internally generated signals that indicate which command has been entered externally. “The command signals include a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).” (Ex. 1001, 2:50-54.) The signal PRE represents PRECHARGE; the signal ARF represents AUTOREFRESH; and the signal MRS represents MODE-REGISTER-SET.

39. As shown in Fig. 3 (above), CHIPREADY transitions from a low logic level to a high logic level when PRE, ARF, and MRS occur in a predetermined proper initialization sequence. As shown in this embodiment, command signal PRE occurs before command signal ARF. Command signal MRS

may occur before or after PRE and/or ARF. When the command signals have occurred in the proper sequence, CHIPREADY transitions from a low logic level to a high logic level.

40. Accordingly, the PRE and ARF signals must transition in the proper sequence (along with the occurrence of the MRS signal transition), while POWERON is at a high logic level, for the enable circuit to transition its CHIPREADY signal.

2. The '589 Patent teaches “the enable signal effecting an unlatching of said control circuit.”

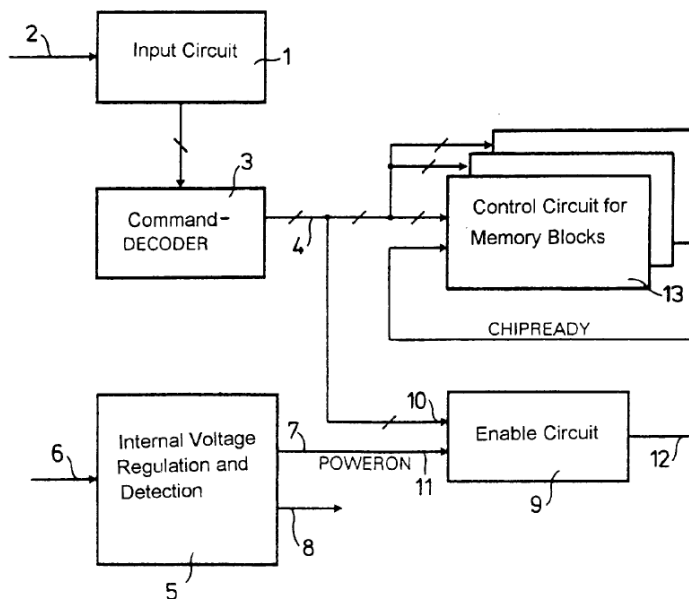
41. Claim element 1.3 of the '589 Patent requires, “said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.” Breaking claim element 1.3 down, claim element 1.3 requires (1) the enable circuit outputs an enable signal, after (2) the enable circuit identifies a predetermined proper initialization sequence of the externally applied further command signals, and (3) the enable signal effects an unlatching of the control circuits.

42. The '589 Patent specification states in the Background, “In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages

have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.” (Ex. 1001, 1:65-2:5.) Accordingly, the ’589 Patent discloses that the internal control circuits of the memory may include latches, and if so, the unlatching occurs due to the POWERON signal. This passage **does not** admit that all control circuits are either latched or unlatched. A careful reading of the passage clearly states that prior art SDRAMs were unlatched using the **POWERON signal**, not that all control circuits contained latches.

43. The ’589 Patent teaches that instead of the POWERON signal performing the latching and unlatching operation, the CHIPREADY signal is used for this purpose. In Fig. 1 (reproduced below) of the ’589 Patent, the POWERON signal is applied to an input 11 of an enable circuit 9, along with the command signals PRE, ARF, and MRS at an input 10 of the enable circuit 9. The command signals PRE, ARF, and MRS are internal signals generated by command decoder 3 in response to externally applied command signals.

Fig 1



44. As well-known through the JEDEC standard (e.g., Ex. 1006, pp. 479-480, IDLE), combinations of external signals form commands. Those commands are indicated internally by command signals. In Fig. 1 (above), the command signals PRE, ARF, and MRS are provided on output 4 of the command decoder 3, and applied to input 10 of enable circuit 9. (Ex. 1001, 3:54-61; 4:11-12.)

45. Enable circuit 9 outputs an enable signal CHIPREADY on output 12. “An enable signal CHIPREADY is supplied at an output 12 of the enable circuit 9 after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device. The internal control circuits 13 serve inter

alia for sequence control for one or more of the memory blocks of the SDRAM memory and are known as such.” (Ex. 1001, 4:14-23.)

46. For both the POWERON signal disclosed in the Background of the ’589 Patent and in the CHIPREADY signal taught by the ’589 Patent, the control circuits are latched when the POWERON / CHIPREADY signal is at a low logic level and unlatched when the POWERON / CHIPREADY signal is at a high logic level.

47. Accordingly, the ’589 Patent teaches the claim element 1.3 that requires “the enable signal effecting an unlatching of said control circuit.”

C. Prosecution History

48. The USPTO Patent Center web site shows that the ’589 Patent was issued on its first office action. As such, no prior art or issues were discussed between the Examiner and Applicant. This can also be confirmed from the prosecution history attached to the Petition at Ex. 1002.

49. In the Petition, the Petitioner notes that the EPO allowed a claim equivalent to claim 2 of the ’589 Patent, and the Applicant did not make any arguments over Tetsuka (Ex. 1011), a family member of Lee, during the EPO prosecution. (Petition, pp. 7-9.) Accordingly, no discussion between the Examiner and Applicant occurred that addressed the failings in Tetsuka (Ex. 1011), which would bear on the current arguments concerning Lee.

VI. KOCIS (EXHIBIT 1004)

50. Kocis was filed as U.S. Application No. 08/378,164 on January 25, 1995, and was issued as U.S. Patent No. 5,559,753 to Thomas Kocis on September 24, 1996. Kocis is entitled “Apparatus and Method for Preventing Bus Contention During Power-Up in a Computer System with Two or More DRAM Banks.”

A. Overview of Kocis’ Background

51. As explained in the Background of Kocis, his invention is generally concerned with “problems which may arise on a memory bus during system power-up. Still more particularly, the present invention relates to a system for preventing contention on the memory bus between conflicting data signals from two or more DRAM banks.” (Ex. 1004, 1:11-15.)

52. Kocis provides prior art circuitry in Figs. 1, 2, 3, 4A, and 4B, which illustrate the issue with bus contentions on power-up. In the Background, Kocis states that the DRAMs may experience latch-up due to bus contentions, which may shorten the life of the DRAMs. (Ex. 1004, 2:53-59.) Kocis states that the reason for the bus contentions may be traced back to the use of a prior art approach that “relies primarily on an analog time delay circuit to disable the receipt of a RAS (and/or CAS) control signal giving the power supply a minimum time period to reach a nominal operating level.” (Ex. 1004, 3:1-4.)

B. Kocis' Disclosure

53. In an effort to get away from time-based delay circuits in the prior art (including Lee Fig. 1, and Iketani), Kocis discloses a counter that is added to the prior art delay circuits. The counter will not change its output until seven (7) cycles of RAS (or CAS) have occurred. Only then are the conditions met to enable the output buffers.

54. Kocis Fig. 4A (reproduced below) shows a time delay circuit based on the rising voltage of VCC (also known as Vdd). The PWRUP signal will be a low-high-low logic level pulse under proper operation.

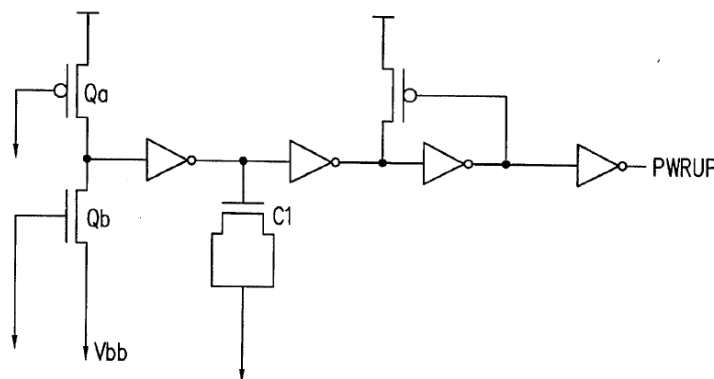
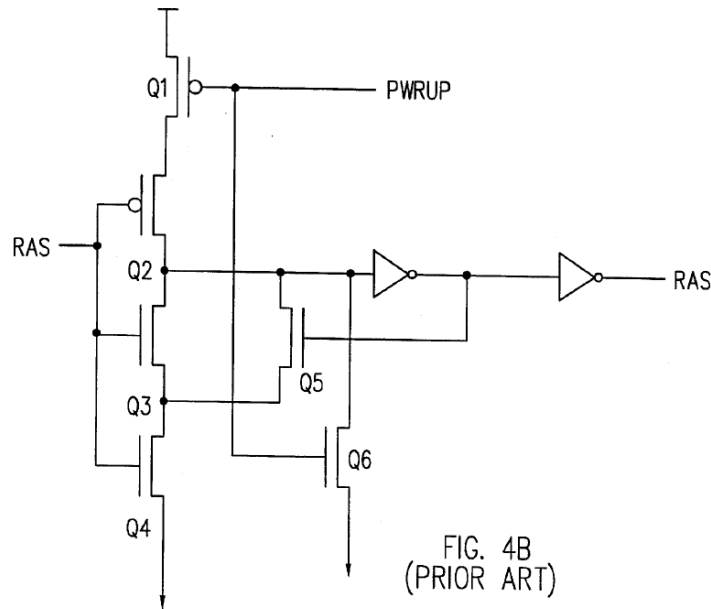


FIG. 4A
(PRIOR ART)

55. Kocis Fig. 4B (reproduced below) shows a lockout and initialization circuit for the RAS buffer circuit. The circuit (1) prevents RAS from being transmitted internally until PWRUP (from Fig. 4A above) has established that the external positive power supply VCC has reached a threshold voltage, and (2) initializes RAS internally to a low logic level.



56. Kocis Fig. 5 (reproduced below) shows a disable circuit wherein PWRUP from Fig. 4A (above) and RAS output from Fig. 4B (above) are inputs to counter 50. The enable signal output from AND 55 will not go active (to a high logic level) unless both the PWRUP signal is at a low logic level and the counter 50 has counted seven (7) RAS cycles. When seven (7) RAS cycles have been counted, KEEP OFF# goes to a high logic level, otherwise counter 50 outputs a low logic level on KEEP OFF#.

condition until the enable signal goes to a high logic level. The enable signal is dependent on both the PWRUP signal indicating that VCC has reached a predetermine threshold and the external host has clocked seven (7) RAS cycles, which indicates the external host has been properly powered up.

C. Limitations of the Kocis' Disclosure

59. While Kocis addresses an issue with bus contention, Kocis is completely silent as to the failings involved with his time delay circuit of Fig. 4A. He presents the time delay circuit in both prior art Fig. 4A and as part of his invention in Figs. 5-6. Lee in Figs. 1-2 explain why Kocis' Fig. 4A may malfunction. Likewise, Iketani also explains possible malfunction mechanisms related to power on reset circuits. Kocis fails to address this issue.

60. Kocis is silent as to the use of “externally applied further *command* signals” as claimed. Kocis clearly discloses the use of “the *control* signals (such as RAS or CAS)”. (Ex. 1004, 2:63, emphasis added.)

61. Kocis does not and cannot identify a proper initialization sequence of command signals because only one signal is used. The RAS or CAS control signal is counted. There is no plurality of signals to sequence, for which the enable circuit could identify.

62. Kocis discloses the use of tri-state buffers 31, 32, 33, 34, 35 in Fig. 5. Tri-state buffers are disabled to cause a high-Z output, or are enabled to output a

low logic level or high logic level dependent on the logic level of the tri-state buffer's input. Kocis is completely silent as to any latching or unlatching of his tri-state buffers. In fact, Kocis must presume that the inputs to tri-state buffers 31, 32, 33, 34, 35 in Fig. 5 are at a known state because when the enable signal in Fig. 5 goes to a high logic level, the tri-state buffers 31, 32, 33, 34, 35 in Fig. 5 will drive their outputs corresponding to their inputs. A bus contention can still occur if the devices on the common bus drive different logic levels.

VII. LEE (EXHIBIT 1005)

63. Lee was filed as U.S. Application No. 08/697,356 on August 23, 1996, and was issued as U.S. Patent No. 5,774,402 to Cheol-Ha Lee on June 30, 1998. Lee claims a foreign application priority to Korean Application KR 26181/1995 filed August 23, 1995. Lee is entitled "Initialization Circuit for a Semiconductor Memory Device."

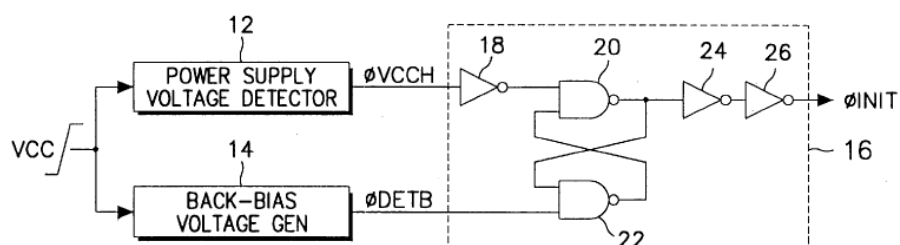
A. Overview of Lee's Background

64. As explained in the Background of Lee, the invention is generally concerned with "initialization circuits which operate in response to an external control signal, thereby providing reliable initialization when conventional power supply reset circuits malfunction." (Ex. 1005, 1:13-16.)

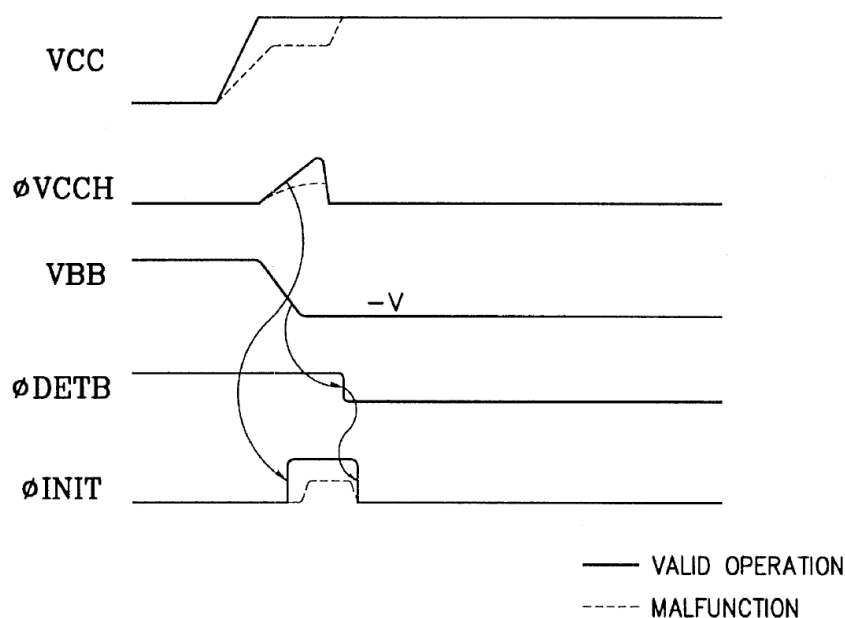
65. To that end, Lee provides Figs. 1 and 2 (reproduced below). Fig. 1 discloses a prior art circuit for generating an initialization signal based on both an

external power supply (VCC) and an internally pumped back bias voltage VBB.

Fig. 2 shows the ideal waveforms in solid lines, and a potential malfunction caused by VCC not following the expected rising transition pattern. The output ϕINIT fails both to rise to a proper maximum voltage and to have a proper duration when a malfunction occurs.



(PRIOR ART)
Fig. 1



(PRIOR ART)
Fig. 2

66. Lee addresses the potential malfunction of the initialization circuit in Fig. 1 by adding a new circuit in parallel to the initialization circuit in Fig. 1, and combining the outputs of those two circuits into a single output to be used in place of output ϕINIT .

B. Lee's Disclosure

67. In Fig. 3, Lee discloses his modified Fig. 1 circuit to address the malfunction of Fig. 1. Lee uses the same Fig. 1 circuit (second initialization signal generator 16), and appends an additional circuit in parallel (first initialization circuit 46), and combines the outputs of the two circuits with transfer unit 56. Fig. 3 is reproduced below:

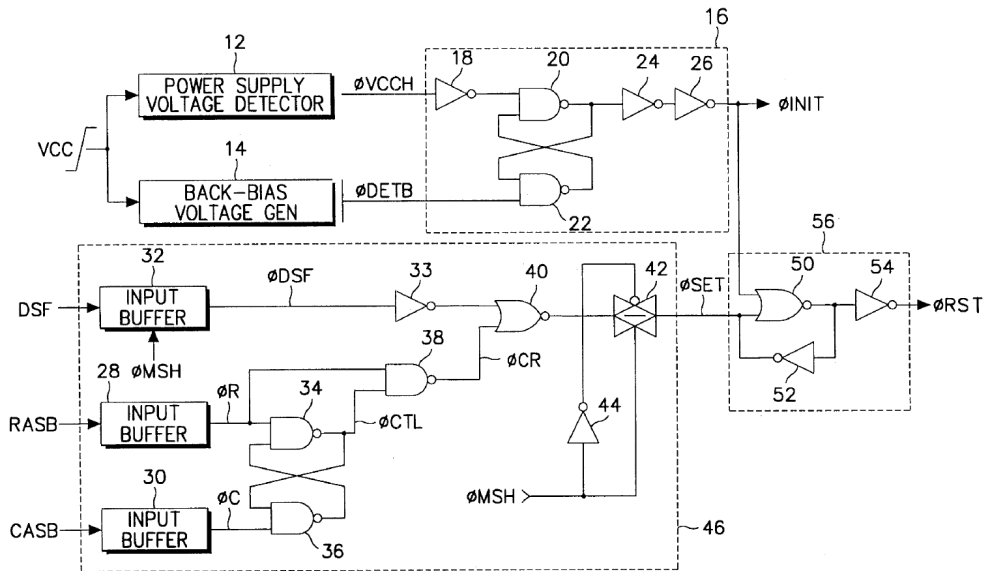


Fig. 3

68. To support an understanding of how the circuit in Fig. 3 operates, Lee discloses that the external control signals RASB, CASB, and DSF are used to generate a reset signal ϕ RST. (Ex. 1005, 3:9-22.) Lee explains that buffer 30 generates a column address clock signal ϕ C in response to CASB, buffer 28 generates a row address clock signal ϕ R in response to RASB, and buffer 32 generates a mode selection clock signal ϕ DSF in response to DSF. (Ex. 1005, 3:36-49.)

69. A POSITA would know that RASB, CASB, and DSF are external signals used to control a DRAM, typical of the mid-1990s.

70. Lee provides a timing diagram in Fig. 4 (reproduced below) to help explain the circuit's operation in Fig. 3.

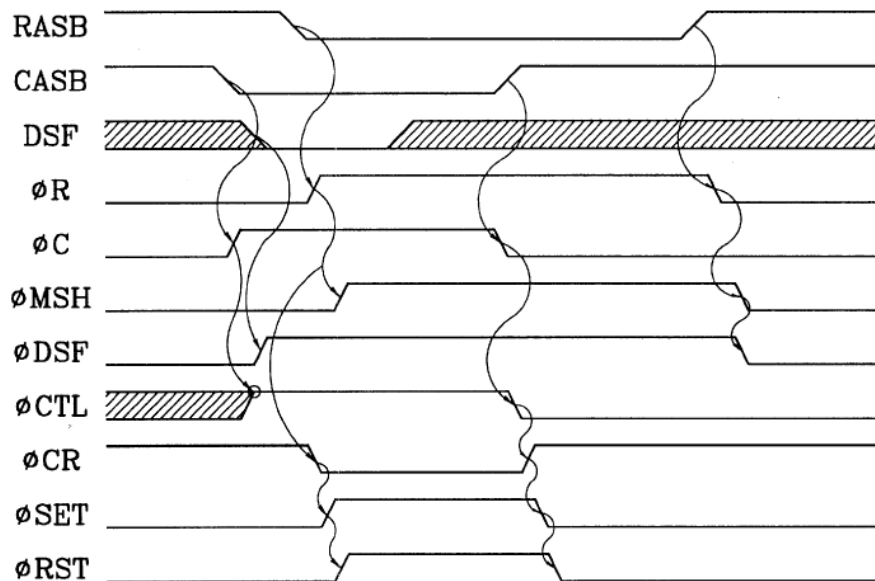


Fig. 4

71. Lee explains Fig. 4 by noting that ϕMSH is a delayed version of ϕR . Furthermore, JESD 21-C discloses that DSF is latched at RAS_ falling. (Ex. 1006, pg. 388.) Lee discloses that “[a] third input buffer 32 is connected to a third input terminal and receives a mode selection signal DSF for generating a mode selection clock signal ϕDSF . Input buffer 32 is also connected to a delay clock signal ϕMSH which is generated by delaying the row address clock signal ϕR . The delay clock signal ϕMSH is used to latch the mode selection clock signal [ϕR] ϕDSF .” (Ex. 1005, 3:47-53, errors corrected.) Lee also discloses that “[t]he mode selection clock signal ϕDSF is latched (sic) in the high state by the delay clock signal ϕMSH which is generated by delaying the the (sic) row address clock signal ϕR .” (Ex. 1005, 4:45-48.)

72. Lee discloses that “if the reset signals DSF, RASB and CASB generate a predetermined bit pattern in the proper sequence, the first initialization signal generator activates the first initialization signal ϕSET . For this to occur, the reset control signals DSF, RASB, and CASB must be activated in the CBR (CAS before RAS) mode.” (Ex. 1005, 3:38-43.) Lee explains the combination of the signals from the first and second initialization signal generator circuits as follows:

The transfer unit 56 combines the first initialization signal ϕSET and the second initialization signal ϕINIT and activates the reset signal ϕRST by driving it to a high logic level, thereby initializing the circuits within the chip. The

reset signal ϕ RST remains at the logic high-level until the first control signal CASB is deactivated and driven to the logic high-level. When the signal CASB switches to the high level, the column address clock ϕ C switches to a logic low-level, thereby driving the control clock ϕ CTL to the low-logic level. Therefore, if signal CASB Switches to the high logic level while the second control signal RASB is in the active low state, the first initialization signal ϕ SET is deactivated, which in turn, deactivates the reset signal ϕ RST. (Ex. 1005, 4:59-5:4.)

73. Lee discloses that his “initialization circuit according to the present invention generates a reset signal in response to either a power supply power-up or a sequence of reset signals. Thus, the present invention can properly reset circuits in the chip even when the power-up reset circuit malfunctions.” (Ex. 1005, 5:5-10.)

C. Limitations of the Lee’s Disclosure

74. There is a myriad of issues with Lee’s circuit and his statements surrounding them.

75. First, Lee discloses that the ϕ RST signal starts at a low voltage level directly after power is applied to the device. While this is true for the second initialization signal generator 16, as shown in Fig. 2, this is **not** guaranteed by the

circuit in Fig. 3. Fig. 3 is reproduced again (below) with a boxed region to indicate from where the next figure was copied:

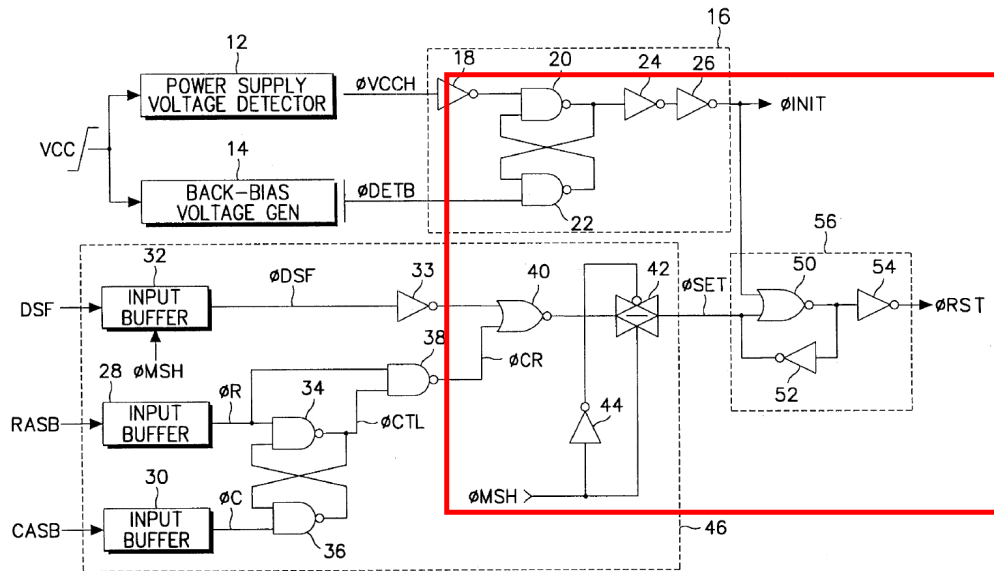
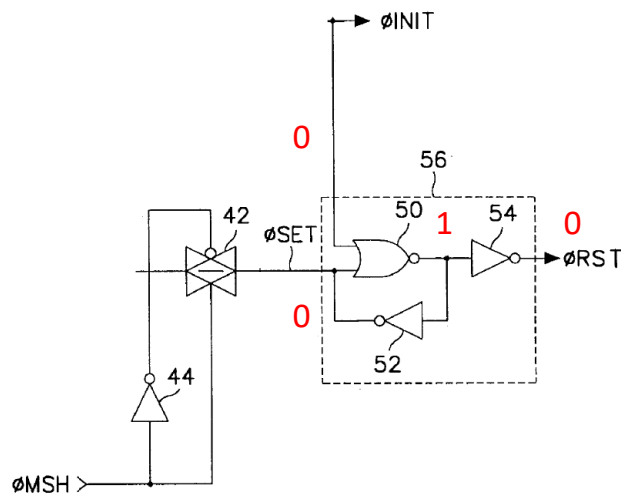


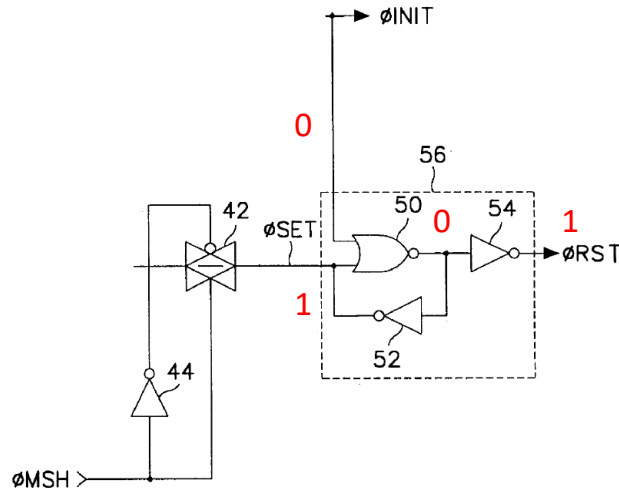
Fig. 3

76. The figures below are copies of the boxed region above with certain irrelevant circuit elements removed to focus the discussion. When power is applied to the device, ϕINIT is at a low logic level as shown in Fig. 2, and could be derived from analysis of the second initialization signal generator 16 shown in Fig. 1. As such, NOR gate 50 is solely dependent on the other input, ϕSET , to determine its output. However, the transmission gate 42 is off (as shown in Fig. 4); therefore, ϕSET is floating. Accordingly, NOR gate 50 may output a low logic level or a high logic level signal dependent on probability. Whichever logic level is output by NOR gate 50, the logic level is latched due to inverter 52 feeding back to the ϕSET signal.



77. If NOR gate 50 outputs a high logic level (above), the ϕSET signal will become a low logic level and remain at a low logic level unless the first initialization signal generator 46 or the second initialization signal generator 16

changes its value. At this point, ϕRST is a low logic level, and the circuit acts according to the timing diagram in Fig. 4.



78. However, if NOR gate 50 outputs a low logic level (above), the ϕSET signal will become a high logic level and remain at a high logic level unless the first initialization signal generator 46 changes its value. At this point, ϕRST is a high logic level and the input $\phi INIT$ is a don't care. The result of a power up **and** the CAS before RAS reset in Lee will simply be a single ϕRST falling edge from a high logic level to a low logic level.

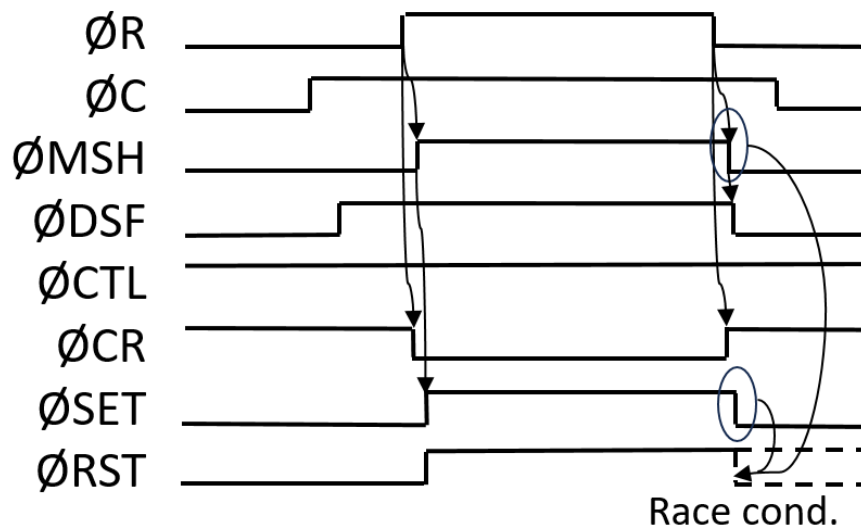
79. Lee is silent as to how the circuitry connected to ϕRST will respond if a single high logic level to low logic level transition occurs instead of the expected ϕRST pulse from a low logic level to a high logic level to a low logic level.

80. Second, Lee discloses the first initialization signal generator 46 activates if the reset signals DSF, RASB, and CASB generate a predetermined bit

pattern in the proper sequence. (Ex 1005, 4:38-40.) Lee is silent as to what happens if the prescribed sequence is not followed.

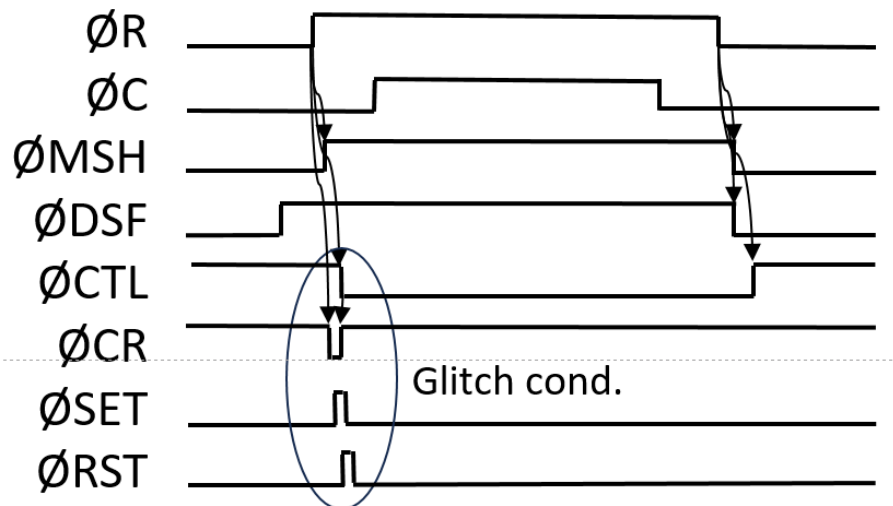
81. For example, Lee discloses a desired sequence (created by an external host) where CAS before RAS occurs (Ex. 1005, 4:41-43.), which is drawn in Fig.

4. However, Lee is silent as to the conclusion of the cycle. The timing diagram below shows the effect of a CAS before RAS with RAS resetting before CAS at the end of the cycle. The result is a race condition, which may leave ϕ RST permanently at a high logic level. Lee is silent as to how the circuitry connected to ϕ RST will respond if ϕ RST permanently remains at a high logic level after power-up.

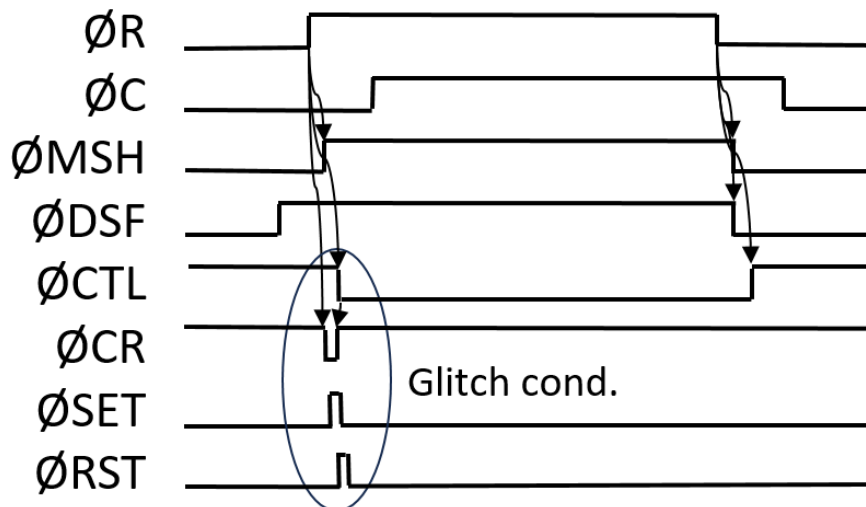


82. Because Lee does not lockout erroneous bit patterns, various bit patterns may be entered. The timing diagram below shows the effect of a RAS before CAS with CAS resetting before RAS at the end of the cycle. The result is a

glitch condition, which produces a runt pulse on ϕRST . This is exactly the condition Lee was trying to solve with regards to the malfunction of the second initialization signal generator 16. Lee is silent as to how the circuitry connected to ϕRST will respond if a runt pulse occurs on ϕRST ; however, given that Lee was attempting to prevent a runt pulse, the effects are undesirable.



83. Because Lee does not lockout erroneous bit patterns, various bit patterns may be entered. The timing diagram below shows the effect of a RAS before CAS with RAS resetting before CAS at the end of the cycle. The result is a glitch condition, which produces a runt pulse on ϕRST . This is exactly the condition Lee was trying to solve with regards to the malfunction of the second initialization signal generator 16. Lee is silent as to how the circuitry connected to ϕRST will respond if a runt pulse occurs on ϕRST ; however, given that Lee was attempting to prevent a runt pulse, the effects are undesirable.



84. Third, Lee discloses that external *control* signals DSF, RASB, and CASB are used to directly control the first initialization signal generator 46. Lee is silent as to the claimed “externally applied further command signal,” nor can he. Lee discloses the use of *control* signals, and not “command signals” as claimed.

85. Fourth, Lee’s circuit will generate a low-high-low logic level pulse on ϕ RST every time the predetermined sequence occurs. For example, a “CBR REFRESH (1)” is allowed during normal operation (after initialization), which exactly aligns with the input pattern for RASB, CASB, and DSF according to Lee’s Fig. 4, and will cause a pulse on ϕ RST. (Ex. 1006, pg. 388.) Lee fails to address what would happen if a ϕ RST pulse occurs during normal operation beyond initialization.

86. Individual external signals are evaluated as a group to form a command. Lee uses the individual external *control* signals directly, without forming a command, and Lee is silent as to any other arrangement.

VIII. JESD 21-C (EXHIBIT 1006)

87. JESD 21-C is a Joint Electron Device Engineering Council (JEDEC) Standard that governs various types and configurations of memory devices. JESD 21-C Release 7 was made available in January 1997. The JEDEC Standard No. 21-C is currently on Release 29, which was made available in January 2020.

A. Overview of JESD 21-C

88. JESD 21-C is almost 800 pages long and covers various memory devices including ROM, PROM, EPROM, EEPROM, SRAM, DRAM, SDRAM, VRAM (listed as MPDRAM), and so on. The JESD 21-C Standard's stated goal is "to serve the public interest through eliminating misunderstandings between manufacturers and purchases (sic), facilitating interchangeability and improvement of products, and assisting the purchaser is (sic) selecting and obtaining with minimum delay the proper product for his particular need." (Ex. 1006, pg. 2.) However, JESD 21-C goes on to state, "Existence of such standards shall not in any respect preclude any member or nonmember of JEDEC from manufacturing or selling products not conforming to such standards, nor shall the existence of such

standards preclude their voluntary use by those other than EIA members, whether the standard is to be used either domestically or internationally.” (Ex. 1006, pg. 2.)

89. Through the previously listed JESD 21-C Notice, two key considerations come to light. First, JESD 21-C provides a suggested standard to follow, and second, manufacturers have the right to design their devices according to own internal practices.

90. Petitioner has focused solely on the half page description at Section 3.11.5.4 on page 3.11.5-9. (Ex. 1006, pg. 483.) Section 3.11.5.4 is reproduced below.

3.11.5.4-Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High-Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High-Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μ S.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

91. JESD 21-C Section 3.11.5.4 (above) provides a recommended power on sequence; however, there are many limitations from this section that Petitioner fails to address.

B. Limitations of the JESD 21-C Disclosure

92. First, and foremost, as stated in JESD 21-C, the standard is meant to be a guide to help interoperability and compatibility between device manufacturers and purchasers. JESD 21-C is completely devoid of any information about how

the circuitry for a memory should be designed. So long as the circuitry supports the JESD 21-C guidelines, interoperability and compatibility should be met.

However, the various circuit designs that could meet the JESD 21-C guidelines are as numerous as there are manufacturers, plus some. No inference as to a particular circuit design can be gleaned from JESD 21-C. For all intents and purposes, JESD 21-C provides a guideline for the signals interacting with a memory, but the memory is a black box. What specifically happens inside the memory, let alone the circuitry that causes the memory to operate, is unknown. And, on top of not knowing the circuitry internal to the memory, the timing involved with the activation and deactivation of that circuitry, adds another layer of complexity.

93. Second, JESD 21-C provides a recommended power on sequence with the understanding that the memory will receive the sequence to (1) “strive toward ensuring a High-Z output state during the initial power up sequence,” and (2) place the memory into an IDLE state. In fact, a memory may be designed to use any of the prior art reset circuits (i.e., Iketani, Lee Fig. 1) that rely solely on a rising external power supply to generate a “power on reset” signal internal to the memory device. In this case, the JESD 21-C recommended power on sequence would simply initialize registers and circuits within the row path, auto refresh counter, and mode register.

IX. IKETANI (EXHIBIT 1007)

94. Iketani was filed as U.S. Application No. 08/608,075 on February 28, 1996, and was issued as U.S. Patent No. 5,703,510 to Masayuki Iketani on December 30, 1997. Iketani is entitled “Power On Reset Circuit for Generating Reset Signal at Power On.”

A. Overview of Iketani’s Background

95. As explained in the Background of Iketani, the invention is generally concerned with “a power on reset circuit” used in a SRAM or DRAM “for initializing internal circuitry thereof when the power is turned on.” (Ex. 1007, 1:7-12.)

96. Iketani provides a prior art circuit in Fig. 1, then notes “if the power supply voltage Vdd fluctuates significantly, it may possibly activate the power on reset signal/POR to the L level again even after initialization.” (Ex. 1007, 1:59-62.) Iketani’s invention is to improve the functionality of the prior art power on reset circuit.

B. Iketani’s Disclosure

97. To improve the prior art power on reset circuit presented in Iketani, the inventor discloses Figs. 2 (emphasis added in the figure below) and 4, both reproduced below. Figure 2 discloses several additional circuit elements, which are indicated by red boxes, to the prior art circuit. Corresponding timing diagrams

are shown in Fig. 4 to provide an understanding of how the circuit in Fig. 2 will react to Vdd rising during power up. As shown in Iketani's Fig. 4, the output POR_ will be a high going pulse, albeit without a stable high-level voltage.

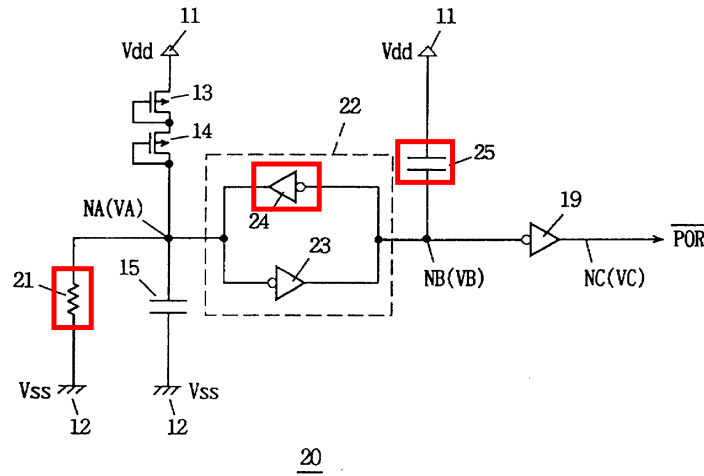
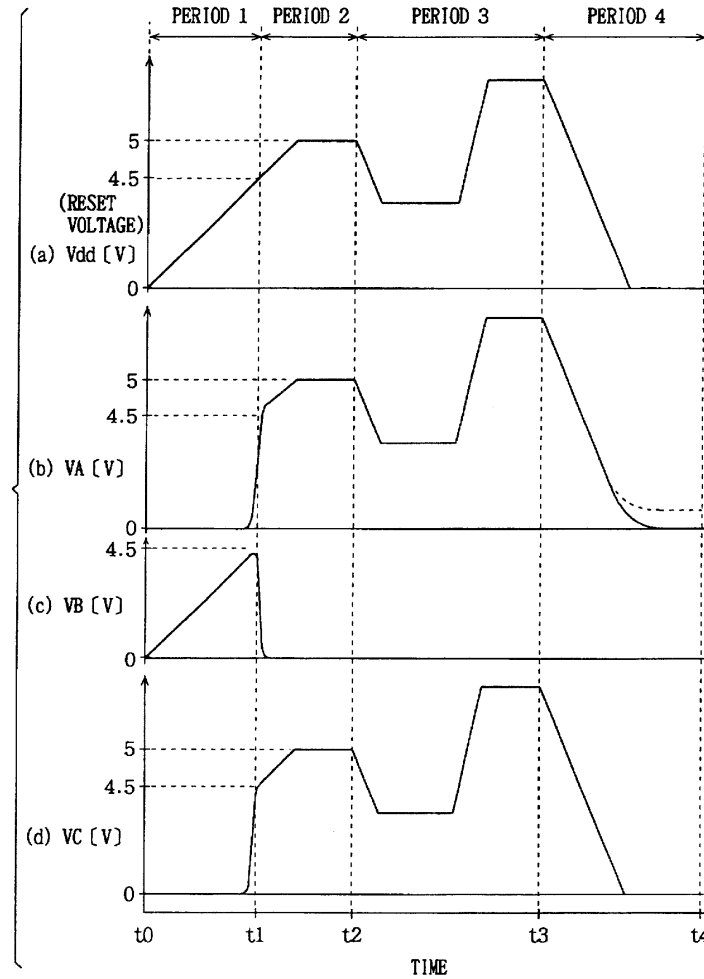


FIG. 4



98. Iketani goes on to explain that the power on reset circuit 20 in Fig. 2, with the timing diagram shown in Fig.4, may be used to provide a power on reset signal for a SRAM in Fig. 5 and a DRAM in Fig. 6. Iketani discloses two more embodiments with modifications to the power on reset circuit 20 shown in Fig. 2. These additional embodiments flow from the same ideas presented with regards to the power on reset circuit 20 shown in Fig. 2.

99. Bottom line, Iketani discloses a power on reset circuit that responds exclusively to an external Vdd power supply signal to generate a power on reset.

C. Limitations of the Iketani's Disclosure

100. While Iketani discloses a power on reset, his circuit is completely based on reacting to the rise of Vdd. Iketani is silent as to any command signals, or even control signals, being used in his power on reset circuit.

101. Further, Iketani is silent as to unlatching any circuit. Iketani only discloses initializing internal circuitry in response to the power on reset signal.
(Ex. 1007, 5:2-3, 5:24-26.)

X. OPINIONS

102. I have formed the following opinions based principally upon (1) my experience summarized above, and (2) my review of the materials cited above in “Section III. Materials Reviewed and Relied Upon,” with regards to what a POSITA would understand at the time of the effective filing date of the '589 Patent on June 30, 1999.

A. Standard for a POSITA

103. My assessment of the claim terms addressed herein assumes that they are being interpreted by a POSITA. In that regard, I have been asked to provide my opinion as to the educational level and professional experience of such a POSITA.

104. Based on the relevant time frame, my review of the '589 Patent and its file history, and my experience in the field of the art applicable to the patent, I believe that a POSITA would have (1) a bachelor's degree in computer engineering or electrical engineering with two to three years of circuit design experience, or (2) a master's degree in computer engineering or electrical engineering with one year of circuit design experience at the time of filing of the '589 Patent.

105. I note that I would have met or exceeded the qualifications of a POSITA. My opinions provided herein are from the perspective of such a person.

106. From the vantage point of such a POSITA, at the time of effective filing of the '589 Patent, issued claims 1, 2, 8, 9, 10, 11, 12, and 13 of the '589 Patent would not have been anticipated under Kocis (Ground 1), would not have been obvious under Kocis in view of JESD 21-C (Ground 2), would neither have been anticipated nor obvious under Lee (Ground 3), would not have been obvious under Lee in view of Iketani (Ground 4), would not have been obvious under Lee in view of JESD 21-C (Ground 5), would not have been obvious under Lee in view of Iketani and JESD 21-C (Ground 6), would not have been obvious under Lee in view of Kocis (Ground 7), and would not have been obvious under Lee in view of Iketani and Kocis (Ground 8).

107. A detailed explanation of the reasoning that led to these opinions is provided below.

B. Claim Construction For “Externally Applied Further Command Signals”

108. The claims require “externally applied further command signals” (claim 1) or “further command signals externally applied” (claim 11). In the ’589 Patent, Figs. 2-4 reference command signals PRE, ARF, and MRS. Fig. 1 teaches that these command signals are externally applied to an input circuit, amplified and conditioned before being provided to a command decoder 3 with output 4, and supplied to input 10 of the enable circuit 9. (Ex. 1001, 3:50-61; 4:11-12.)

109. The ’589 Patent teaches the following:

The initialization circuit has a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and *externally applied further command signals*. The enable circuit outputting an enable signal after a predetermined proper initialization sequence of the *externally applied further command signals* are identified and the enable signal effecting an unlatching of the control circuit.” (Ex. 1001, 2:21-28, emphasis added.)

According to the preferred application in SDRAM memory devices according to the JEDEC standard, it is provided that *the command signals, externally applied* to the semiconductor memory device, of the initialization sequence are to be identified by the enable circuit. *The command signals* include a preparation command signal

for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET). (Ex. 1001, 2:46-54, emphasis added.)

The initialization circuit has an input circuit 1, to whose input 2 *command* and clock *signals that are externally applied* in reference to the semiconductor memory are provided. The *command* and clock *signals* are amplified and conditioned before being received by a command decoder 3 connected downstream of the input circuit 1 and at whose output 4, inter alia, *the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command)* are output. (Ex. 1001, 3:51-61, emphasis added.)

110. In other words, the claimed “externally applied further command signals” are a group of signals that together form a command. In the ’589 Patent, the command decoder 3 takes in a particular pattern of individual external signals representing a command. For example, JESD 21-C page 3.11.5-5 (Ex. 1006, pp. 479-480) IDLE shows the patterns of external signals (e.g., S_ (chip select), RE_ (row enable), CE_ (column enable), W_ (write), An (address) on the rising edge of clock) necessary to cause internal command signals PRE (i.e., NOP⁴ where note 4

reads: “NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).”), ARF (i.e., Auto-Refresh), and MRS (i.e., Mode Register Access, also known as Mode Register Set). Equally, JESD 21-C shows example timing diagrams for MRS on page 3.11.5.7-10 (Ex. 1006, pg. 484), and ARF on page 3.11.5.7-11 (Ex. 1006, pg. 485).

111. A “command signal” is **not** the individual external signals. A “command signal” is a pattern of individual external signals, that represent a particular command. A different pattern of the same signals would represent a different command (or an error, if that pattern happened to be unspecified).

112. Accordingly, “externally applied further command signal” is construed in this Declaration as “a pattern of individual external signals that as a group represent a command.” Furthermore, “externally applied further command signals” or “further command signals externally applied” is construed in this Declaration as “a plurality of command signals.”

C. Claims 1, 9, 11, and 13 are Not Invalid under Ground 1

113. The discussion about Kocis in Section VI (above) is incorporated by reference into this Section X.C.

1. **Claim Element 1.2, “said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and *externally applied further command signals*” is not disclosed in Kocis**

114. Kocis discloses use of “a RAS (and/or CAS) *control signal*”. (Ex. 1004, 3:2-3, emphasis added.) Specifically, Kocis uses a prior art time delay circuit (Fig. 4A) based on the rising voltage of VCC, and a prior art lockout and initialization circuit for the RAS buffer circuit (Fig. 4B). Kocis discloses a counter that is added to the prior art delay circuit and RAS buffer in at least Fig. 5. The counter will not change its output until seven (7) cycles of RAS (or CAS) have occurred. Only then are the conditions met to enable the output buffers. Accordingly, Kocis only discloses use of *control signals*, and **not command signals** as construed in this Declaration.

115. An “externally applied further command signal,” as claimed, is “a pattern of individual external signals that as a group represent a command.” Kocis only discloses use of a ***control signal***. Kocis is silent as to a command signal or command signals. Accordingly, Kocis does not anticipate at least claim element 1.2 of the ’589 Patent.

116. The Melvin Declaration refers to the control signal in Kocis as a command signal (Ex. 1003, ¶¶ 74-76, 78.), even though Kocis himself refers to

RAS and CAS as control signals. (Ex. 1004, 2:63, 2:66, 3:2-3, claims.) Kocis is completely silent as to command signals. The Melvin Declaration calling RAS and/or CAS a command signal fails to appreciate the distinction between the two types of signals. The Melvin Declaration fails to address this deficiency in Kocis.

117. Given Kocis, a POSITA would not be motivated to make a change to use command signals because Kocis fails to show or suggest use of a command signal(s).

118. Accordingly, Kocis with or without explanation by the Melvin Declaration does not anticipate at least claim element 1.2 of the '589 Patent.

2. Claim Element 1.3, “said enable circuit outputting an enable signal after *a predetermined proper initialization sequence of the externally applied further command signals* being identified and *the enable signal effecting an unlatching of said control circuit*” is not disclosed in Kocis

119. Kocis discloses use of “a RAS (and/or CAS) *control signal*”. (Ex. 1004, 3:2-3, emphasis added.) Specifically, Kocis uses a prior art time delay circuit (Fig. 4A) based on the rising voltage of VCC, and a prior art lockout and initialization circuit for the RAS buffer circuit (Fig. 4B). Kocis discloses a counter that is added to the prior art delay circuit and RAS buffer in at least Fig. 5. The counter will not change its output until seven (7) cycles of RAS (or CAS) have occurred. Only then are the conditions met to enable the output buffers.

Accordingly, Kocis only discloses use of *control signals*, and **not command signals** as construed in this Declaration.

120. An “externally applied further command signal,” as claimed, is “a pattern of individual external signals that as a group represent a command.” Kocis only discloses use of a ***control signal***. Kocis is silent as to a command signal or command signals. Accordingly, Kocis does not anticipate at least claim element 1.3 of the ’589 Patent.

121. Furthermore, Kocis’ invention operates because an external host generates a control signal (RAS or CAS) a particular number of times. Kocis simply counts cycles of a control signal, and is completely silent as to a sequence of signals. Kocis fails to show or suggest a plurality of signals, such that those signals could be “a predetermined proper initialization sequence” as claimed. Kocis has no sequence of signals to identify.

122. Also, Kocis discloses enabling a plurality of tri-state buffers using the ENABLE signal. (Ex. 1004, 4:56-61.) Kocis is completely silent as to latching or unlatching of Kocis’ tri-state buffers (i.e., Fig. 5, elements 31, 32, 33, 34, 35). In fact, Kocis is completely silent as to initializing the tri-state buffers using the ENABLE signal. This silence is in keeping with the typical design of tri-state buffers, which do **not** hold state. Tri-state buffers, depending on their enable

signal's input logic level, either create an output based on their input or disconnect the output (i.e., create a high-Z output).

123. Curiously, the Melvin Declaration states, “A POSITA would have understood that driving a high input to the AND gate 55 which ultimately enables the tri-state buffers, as is disclosed in Kocis, teaches *unlatching* the control circuit because it causes the start of normal operation of the buffers” (Ex. 1003, ¶82, emphasis added) without evidence or analysis. The Melvin Declaration, however, does not disclose that a tri-state buffer includes a latch (that would hold state) anywhere in his section on Kocis claim element 1.3. (Ex. 1003, ¶¶79-83.) Also, the Melvin Declaration states as fact that “a basic part of undergraduate courses in logic design, electrical engineers are taught that every sequential circuit (a circuit that maintains state) ... needs a reset mechanism.” (Ex. 1004, ¶130.) Again, tri-state buffers are not argued as holding state, requiring initialization, or are “unlatched” by Kocis, Dr. Melvin, or myself. The Melvin Declaration simply slips in conclusory statements such as “the enable signal unlatches the control circuit” (Ex. 1004, ¶ 79), “[o]nce the enable signal is driven to a high logic level, it unlatches the control circuit” (Ex. 1004, ¶ 81), and “Kocis discloses ... unlatching of said control circuit” (Ex. 1004, ¶ 83) without analysis.

124. Conclusory statements in an Expert Declaration should not substitute for what a reference actually discloses.

125. Petitioner makes an additional argument by citing to Applicant's Background Section in the '589 Patent. (See Petition, pg. 10-12.) At issue is the following sentence:

In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions. (Ex. 1001, 1:65-2:5.)

126. The '589 Patent discloses that the internal control circuits of the memory may include latches, and if so, the unlatching occurs due to the POWERON signal. This passage **does not** admit that all control circuits are either latched or unlatched. A careful reading of the passage clearly states that prior art SDRAMs were unlatched using the **POWERON signal**, not that all control circuits contained latches. The '589 Patent teaches that instead of the POWERON signal performing the latching and unlatching operation, the CHIPREADY signal is used for this purpose.

127. Petitioner has misread this sentence and puts forward that the '589 Patent admits that all prior art SDRAMs latched and unlatched their control circuits. Curiously, Petitioner only references *initialization* of circuits by Kocis,

Lee, and Iketani, and fails to address “unlatching,” (or latching) as claimed.

Because Petitioner has mistakenly used the ’589 Patent’s Background Section as support for the claimed “unlatching,” and Kocis is silent as to unlatching (Kocis only discloses an ENABLE signal for tri-state buffers), Petitioner has failed to invalidate at least claim element 1.3.

128. Additionally, the PTAB has recognized (Institution Decision, pg. 32-34) that an input to AND 55 in Kocis, as identified by Petitioner, cannot be the claimed “enable signal.” “Thus, tri-state buffers 31, 32, 33, 34, 35 *only* are *enabled if all [the] input signals are high.*” *Id.* (emphases added) (quoting Ex. 1004, 5:3–12).” (Institution Decision, pg. 33, emphasis in original.)

129. Accordingly, Kocis (with or without explanation by the Melvin Declaration) does not anticipate at least claim element 1.3 of the ’589 Patent.

3. Claim 9, “said control circuit has *output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit*” is not disclosed in Kocis

130. Petitioner argues by citing the Melvin Declaration that “a POSITA would have understood that disabling the output drivers until the enable conditions are met (*i.e.*, the proper initialization sequence has been performed) results in latching the output drivers until the enable signal is generated by the enable circuit. *See* EX1003, ¶85.” (Petition, pg. 34.) However, Kocis simply discloses

enabling/disabling a plurality of tri-state buffers using the ENABLE signal. (Ex. 1004, 4:56-61.) In Kocis, a low logic level for ENABLE places the tri-state buffers into a high-Z output condition, while a high logic level for ENABLE causes the tri-state buffers to output a signal that is responsive to their input signal, which is DATA.

131. Kocis is completely silent as to latching or unlatching of Kocis' tri-state buffers (i.e., Fig. 5, elements 31, 32, 33, 34, 35). In fact, Kocis is completely silent as to initializing the tri-state buffers using the ENABLE signal. This silence is in keeping with the typical design of tri-state buffers, which do **not** hold state. Tri-state buffers, depending on their enable signal's input value, either create an output based on their input or disconnect the output (i.e., create a high-Z output).

132. Furthermore, claim 9 requires the "output buffers remaining latched", not a signal to keep the output buffers in tri-state. Again, Kocis is silent as to his tri-state buffers containing a latch or holding state. The Melvin Declaration uses conclusory statements to attempt to match Kocis' circuitry with the language of the '589 Patent claims. This language is repeated in the Petition.

133. The Melvin Declaration has failed to provide any analysis as to why a tri-state buffer would hold state, in general, and more specifically through the disclosure of Kocis.

134. The Melvin Declaration states as fact that “a basic part of undergraduate courses in logic design, electrical engineers are taught that every sequential circuit (a circuit that maintains state) ... needs a reset mechanism.” (Ex. 1004, ¶130.) Again, tri-state buffers are not argued as holding state, requiring initialization, or are “latched” by Kocis, Dr. Melvin, or myself. The Melvin Declaration simply slips in conclusory statements such as “a POSITA would have understood that disabling the output drivers until the enable conditions are met ... teaches latching the output drivers until the enable signal is generated by the enable circuit” (Ex. 1003, ¶ 85; Petition , pg. 34), without analysis.

135. Conclusory statements in an Expert Declaration should not substitute for what a reference actually discloses.

136. Furthermore, claim 9 is dependent on independent claim 1, which has not been shown to be anticipated by Kocis.

137. Accordingly, Kocis (with or without explanation by the Melvin Declaration) does not anticipate at least claim 9 of the '589 Patent.

4. **Claim Element 11.2, “supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and *further command signals externally applied* to the dynamic semiconductor memory device, after an identification of *a predetermined proper initialization sequence of the further command signals* the enable signal being generated and *effecting an unlatching of a control circuit* provided for a proper operation of the dynamic semiconductor memory device” is not disclosed in Kocis**

138. Petitioner argues, “Furthermore, for the same reasons discussed in Section X.A.1.c) with respect to claim element [1.2], Kocis discloses the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device. Furthermore, for the same reasons discussed in Section X.A.1.d) with respect to claim element [1.3], Kocis discloses supplying, via an enable circuit of the initialization circuit, an enable signal ... after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.” (Petition, pp. 35-36.)

139. Correspondingly, support for claim element 11.2 has already been provided above, will not be repeated here, and is incorporated in this section. Specifically, the support for claim element 11.2 is found above in Section X.C.1 and Section X.C.2 for claim element 1.3.

140. Claim element 11.2 has at least some of the requirements addressed above with respect to claim elements 1.2 and 1.3. For at least these reasons, Kocis does not anticipate at least claim element 11.2 of the '589 Patent. The Melvin declaration does not add what is missing in Kocis; therefore, Kocis (with or without the Melvin Declaration) does not anticipate at least claim element 11.2 of the '589 Patent.

5. Claim 13, “*maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit*” is not disclosed in Kocis

141. Petitioner argues, “For the same reasons discussed in Section X.A.2 with respect to claim element [9], Kocis discloses claim [13]. EX1003, ¶89.” (Petition, pg. 36.)

142. Correspondingly, support for claim 13 has already been provided above, will not be repeated here, and is incorporated in this section. Specifically, the support for claim 9 is found above in Section X.C.3.

143. Claim 13 has at least some of the requirements addressed above with respect to claim 9. For at least these reasons, Kocis does not anticipate at least claim 13 of the '589 Patent. Furthermore, claim 13 is dependent on independent claim 11, which has not been shown to be invalid. The Melvin declaration does not add what is missing in Kocis; therefore, Kocis (with or without the Melvin Declaration) does not anticipate at least claim 13 of the '589 Patent.

D. Claims 2, 8, 10, and 12 are Not Invalid under Ground 2

144. The discussion about Kocis in Section VI (above) and the discussion about JESD 21-C in Section VIII (above) are incorporated by reference into this Section X.D. Furthermore, the discussion about Kocis (with or without the Melvin Declaration) in Section X.C (above) is incorporated by reference into this Section X.D.

145. Petitioner argues for Ground 2, “Kocis in combination with JESD 21-C renders obvious claims 2, 8, 10, and 12 of the '589 Patent, with Kocis disclosing the limitations of independent Claims 1 and 11 from which they depend (*see* Sections X.A.1 and X.A.3, *supra*).” (Petition, pg. 37.) Petitioner goes on to broadly state, “A POSITA would have been motivated to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Kocis in order to ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by

the POSITA. EX1003, ¶¶94-95.” (Petition, pg. 38.) Further, Petitioner broadly states, “This improvement is also a simple substitution of the signals and timing of Kocis with the signals and timing specified in JESD 21-C.” (Petition, pg. 38.)

146. First, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry.

147. Second, JESD 21-C provides a section entitled, “Power On Sequence (Recommended)”. (Ex. 1006, pg. 483.) This JESD 21-C section requires an external host to generate the sequence and the memory to receive the sequence. As explained, (1) the purpose of the MODE-REGISTER-SET is to initialize the register holding the mode information, and (2) an optional AUTO REFRESH command may be used. Each command in the initialization is listed as only performing the command requested.

148. To this point, the Petition makes the same argument. The Petition spends considerable page space describing what a precharge, autorefresh, and mode register set commands do according to JESD 21-C. (Petition, pg. 39-42.) By explaining the functionality of each command, the Petition reinforces that a POSITA would understand what these commands do (regardless of a power on initialization or during normal operation), but fails to motivate identifying them as a “predetermined proper initialization sequence” by an enable circuit on the memory device. Each of these commands in JESD 21-C causes an internal

initialization to occur within the memory device, but knowing this recommended sequence fails to show or suggest identifying a predetermined sequence by an enable circuit, let alone latching or unlatching a control circuit.

149. Third, the JESD 21-C section entitled, “Power On Sequence (Recommended)” (Ex. 1006, pg. 483) recommends a process; however, it is only a recommendation, not a requirement. As such, a system designer has the option to skip the recommended JESD 21-C Power On Sequence if proper operation of the system can be accomplished through different means.

150. JESD 21-C fails to make up for what is missing in Kocis.

1. **Claim 2, “*externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal*” is not disclosed in Kocis in view of JESD 21-C**

151. Kocis is silent as to command signals, let alone a sequence of command signals. Kocis discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration. Kocis simply counts cycles of a control signal, and is completely silent as to a sequence of signals.

152. Adding JESD 21-C as a reference does not show or suggest that a POSITA would understand that Kocis’ control signals should or could be (1)

substituted by command signals, and (2) the predetermined proper initialization sequence of command signals are identified by an enable circuit, which Kocis does not show or suggest. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 2.

153. Petitioner argues, “A POSITA would have been motivated to incorporate the signals and timing specifications disclosed in JESD 21-C with the circuitry of Kocis in order to ensure interoperability and compatibility with other products in the solid state memory field, thus promoting wider adoption of any products developed by the POSITA. EX1003, ¶¶94-95.” (Petition, pg. 38.) *Arguendo*, even if this were true, JESD 21-C is silent as to “the predetermined proper initialization sequence to be identified by said enable circuit” as claimed, which is missing in Kocis.

154. Furthermore, claim 2 is dependent on independent claim 1, which has not been shown to be invalid.

155. Accordingly, Kocis in combination with JESD 21-C does not obviate at least claim 2 of the '589 Patent.

2. **Claim 8, “the identification of an initialization sequence that is identified as *the predetermined proper initialization sequence* by said enable circuit and generates the enable signal constitutes *a command sequence* conforming to a JEDEC standard” is not disclosed in Kocis in view of JESD 21-C**

156. Kocis is silent as to the identification of a “predetermined proper initialization sequence” because Kocis only counts a control signal. Simply adding JESD 21-C as a reference does not show or suggest what is missing from Kocis. A POSITA would not understand that Kocis’ control signals should or could be substituted by command signals, let alone “a command sequence,” which Kocis does not show or suggest.

157. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 8.

158. Furthermore, claim 8 is dependent on independent claim 1, which has not been shown to be invalid.

159. Accordingly, Kocis in combination with JESD 21-C does not obviate at least claim 8 of the ’589 Patent.

3. **Claim 10, “the predetermined proper initialization sequence includes one of the following chronologically successive *command sequences*: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal” is not disclosed in Kocis in view of JESD 21-C**

160. Kocis is silent as to command signals, let alone “command sequences”, as claimed. Kocis discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

161. Simply adding JESD 21-C as a reference does not show or suggest that a POSITA would understand that Kocis’ control signals should or could be substituted by command signals. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry.

162. Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 10.

163. Furthermore, claim 10 is dependent on independent claim 1, which has not been shown to be invalid.

164. Accordingly, Kocis in combination with JESD 21-C does not obviate at least claim 10 of the ’589 Patent.

4. **Claim 12, “providing at least one of a preparation *command signal* for word line activation, a refresh *command signal*, and a loading configuration register *command signal* as the further command signals” is not disclosed in Kocis in view of JESD 21-C**

165. Kocis is silent as to command signals, as claimed. Kocis discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

166. Simply adding JESD 21-C as a reference does not show or suggest that a POSITA would understand that Kocis’ control signals should or could be substituted by command signals. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry.

167. Petitioner relies on hindsight to construct the functionality, let alone the actual circuitry, as claimed to render claim 12 obvious.

168. Furthermore, claim 12 is dependent on independent claim 11, which has not been shown to be invalid over Kocis.

169. Accordingly, Kocis in combination with JESD 21-C does not render obvious at least claim 12 of the ’589 Patent.

E. Claims 1 and 11 are Not Invalid under Ground 3A/3B

170. The discussion about Lee in Section VII (above) is incorporated by reference into this Section X.E.

1. **Claim Element 1.2, “said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and *externally applied further command signals*” is not disclosed in Lee**

171. Lee discloses use of “a plurality of *control signals*.” (Ex. 1005, 2:27, emphasis added.) Specifically, Lee discloses the use of “reset control signals DSF, RASB, and CASB.” (Ex. 1005, 3:15-16.) Furthermore, Lee discloses that these signals are “external logic signals.” (Ex. 1005, 2:22-23.) Lee’s first initialization signal generator 46 responds directly to the logic states of these external control signals. These signals are *control signals*, and **not command signals** as construed in this Declaration.

172. An “externally applied further command signal,” as claimed, is “a pattern of individual external signals that as a group represent a command.” Lee only discloses ***control signals***. Lee is silent as to a command signal or command signals. Accordingly, Lee does not anticipate at least claim element 1.2 of the ’589 Patent.

173. The Melvin Declaration takes the position that “[a] POSITA would recognize that these signals are command signals as they provide specific commands to the memory chip.” (Ex. 1003, ¶ 127.) The control signals DSF, RASB, and CASB disclosed in Lee are individual, external signals that control the

internal operations of the memory device; however, the '589 Patent neither teaches nor claims *control signals*. Instead, the '589 Patent teaches and claims “command signals,” which are different than “control signals.” A “command signal” is construed in this Declaration as “a pattern of individual external signals that as a group represent a command.”

174. The Melvin Declaration goes on to advocate for the position that RASB and CASB are command signals by arguing “the CASB and RASB signals are further command signals because a POSITA would have understood that they can be used to generate the PRECHARGE, AUTOREFRESH, and MODE-REGISTER-SET commands disclosed in the '589 Patent.” (Ex. 1003, ¶ 128.) RASB and CASB, by themselves **cannot** generate the PRECHARGE, AUTOREFRESH, or MODE-REGISTER-SET commands. These commands used in the '589 Patent require control signals beyond just RASB and CASB. These commands also require chip select (S_ or CS_), write (W_ or WE_), a clock signal, a clock enable (CKE) signal, and row address and/or bank address for the PRECHARGE command (e.g., Ex. 1006, pp. 479-480).

175. The Melvin Declaration goes on to explain, that in practice, RASB and CASB requires additional signals (i.e., CS and WE) to be interpreted by a command decoder. (Ex. 1003, ¶ 128.) By offering this explanation, the Melvin

Declaration concedes that RASB and CASB are insufficient to form a command given the JEDEC standard

176. More to the point, Lee completely fails to show or suggest “command signals.” Lee only discloses control signals. Lee states that RASB, CASB, and DSF are control signals. (Ex. 1005, 3:15-16.) As construed, a “command signal” is “a pattern of individual external signals that as a group represent a command.” Lee’s circuitry only receives control signals, which act upon Lee’s circuitry as individual signals during a single cycle (i.e., CAS-before-RAS mode). (Ex. 1005, 4:41-43.) According to the claims, command signals must be received, which necessarily must require a plurality of cycles. Each cycle allows a new command signal to be entered. In the ’589 Patent, the command signals (e.g., precharge (PRE), autorefresh (ARF), and mode-register-set (MRS)), not the individual control signals, must operate the circuitry. (Ex. 1001, 1:53-61, Fig. 4.)

177. Accordingly, Lee in combination with the Melvin Declaration does not render obvious at least claim element 1.2 of the ’589 Patent.

2. Claim Element 1.3, “said enable circuit outputting an enable signal after *a predetermined proper initialization sequence of the externally applied further command signals* being identified and *the enable signal effecting an unlatching of said control circuit*” is not disclosed in Lee

178. As discussed above with respect to Lee (Section VII.C), Lee fails to show or suggest *command signals*. Lee only discloses control signals. As such, Lee cannot reasonably show or suggest the claimed *predetermined proper initialization sequence of the externally applied further command signals*.

179. Also, the '589 Patent requires “the enable signal effecting an unlatching of said control circuit.” The '589 Patent teaches a CHIPREADY signal that starts at a low logic level upon application of a supply voltage, and the CHIPREADY signal transitions to a logic high-level after identifying “a predetermined proper initialization sequence of the externally applied further command signals” as claimed. *See, e.g.*, Ex. 1001 at 4:49-58; Fig. 3. As such, claim element 1.3 requires the enable circuit to output an enable signal effecting “an unlatching of said control circuit.” The requirement of the claims can be understood in the context of the '589 Patent’s embodiments that this signal transitioning from one state to another effects an “unlatching.”

180. Lee only provides for a low-high-low logic level *pulse*. Lee neither describes this as “unlatching” any circuits for operation (as opposed to “initializing”) nor that the circuits were latched prior to activation of this pulse.

181. And, even if one were to assume the circuits were latched, then a pulse signal would imply that upon the signal’s return to its original state, latching would be reenabled, which would disable normal operation.

182. Specifically, Lee discloses “[t]he transfer unit 56 combines the first initialization signal ϕ SET and the second initialization signal ϕ INIT and **activates the reset signal ϕ RST by driving it to a high logic level, thereby initializing the circuits within the chip.** The reset signal ϕ RST remains at the logic high-level until the first control signal CASB is deactivated and driven to the logic high-level. When the signal CASB switches to the high level, the column address clock ϕ C switches to a low logic level, thereby driving the control clock ϕ CTL to the low-logic level. Therefore, if signal CASB switches to the high logic level while the second control signal RASB is in the active low state, the first initialization signal ϕ SET is deactivated, which in turn, deactivates the reset signal ϕ RST.” (Ex. 1005, 4:59-5:4, emphasis added.) In other words, ϕ RST has a low-high-low logic level *pulse* in which ϕ RST goes from a low logic level, to a high logic level, to a low logic level. Furthermore, Lee states that when ϕ RST is driven to a high logic level, the circuits within the chip are initialized.

183. Bottom line, Lee discloses initializing a circuit with ϕ RST, but is silent as to unlatching (or even latching). “Initializing” and “unlatching” are not the same. Even the Melvin Declaration seems to acknowledge this, arguing a POSITA would understand “that every sequential circuit (a circuit that maintains state), such as a control circuit, needs a reset mechanism to ensure that it powers up in a known state. Powering up sequential logic without *initialization* could lead to an unknown state and unpredictable operation.” (Ex. 1003, ¶130, emphasis added.) Petitioner’s expert is silent as to how initializing a sequential circuit is equivalent to the claimed “unlatching.” Petitioner equates “unlatching” to “initializing” by (1) conclusory statement, and (2) quoting Lee’s statements about initializing. Nowhere is the two-state condition (latched and unlatched) taught by the ’589 Patent addressed with respect to the low-high-low logic level ϕ RST signal pulse in Lee.

184. Furthermore, Lee may generate a ϕ RST signal pulse multiple times during power up and during normal operation. If Petitioner is to be believed, then Petitioner is also stating that latching during normal operation could occur, which would disrupt I/O operations on the memory device.

185. Petitioner makes an additional argument by citing to Applicant’s Background Section in the ’589 Patent. (See Petition, pg. 10-12.) At issue is the following sentence:

In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions. (Ex. 1001, 1:65-2:5.)

186. The '589 Patent discloses that the internal control circuits of the memory may include latches, and if so, the unlatching occurs due to the POWERON signal. This passage **does not** admit that all control circuits are either latched or unlatched. A careful reading of the passage clearly states that prior art SDRAMs were unlatched using the **POWERON signal**, not that all control circuits contained latches. The '589 Patent teaches that instead of the POWERON signal performing the latching and unlatching operation, the CHIPREADY signal is used for this purpose.

187. Petitioner has misread this sentence and puts forward that the '589 Patent admits that all prior art SDRAMs latched and unlatched their control circuits. Curiously, Petitioner only references *initialization* of circuits by Kocis, Lee, and Iketani, and fails to address “unlatching,” (or latching) as claimed. Because Petitioner has mistakenly used the '589 Patent's Background Section as support for the claimed “unlatching,” and Lee is silent as to unlatching (Lee only

discloses *initialization*), Petitioner has failed to invalidate at least claim element 1.3.

188. Accordingly, Lee does not anticipate at least claim element 1.3 of the '589 Patent. The Melvin declaration does not add what is missing in Lee with regards to “unlatching,” as claimed; therefore, Lee in combination with the Melvin Declaration does not render obvious at least claim element 1.3 of the '589 Patent.

3. Claim Element 11.2, “supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and *further command signals externally applied* to the dynamic semiconductor memory device, after an identification of a *predetermined proper initialization sequence of the further command signals* the enable signal being generated and *effecting an unlatching of a control circuit* provided for a proper operation of the dynamic semiconductor memory device” is not disclosed in Lee

189. Support for claim element 11.2 has already been provided above, will not be repeated here, and is incorporated in this section. Specifically, the support for claim element 11.2 is found above in Section X.E.1 for claim element 1.2 and Section X.E.2 for claim element 1.3.

190. Claim element 11.2 has at least some of the requirements addressed above with respect to claim elements 1.2 and 1.3. For at least these reasons, Lee

does not anticipate at least claim element 11.2 of the '589 Patent. The Melvin declaration does not add what is missing in Lee; therefore, Lee in combination with the Melvin Declaration does not obviate at least claim element 11.2 of the '589 Patent.

F. Claims 1 and 11 are Not Invalid under Ground 4

191. The discussion about Lee in Section VII (above) and the discussion about Iketani in Section IX (above) are incorporated by reference into this Section X.F. Furthermore, the discussion about Lee (with or without the Melvin Declaration) in Section X.E (above) is incorporated by reference into this Section X.F.

1. Claim Element 1.2, “said initialization circuit having a control circuit for controlling operations and an enable circuit *receiving* the supply voltage stable signal and *externally applied further command signals*” is not disclosed in Lee in view of Iketani

192. Iketani discloses a power on reset (POR) circuit that responds solely to the power supply Vdd (Ex. 1007, Figs. 2, 3, 7, 8), and generates a POR_ signal that pulses with a low-high-low logic level (Ex. 1007, Fig. 4). A POSITA would understand Iketani's power on reset (POR) circuit as an improvement over Lee's second initialization signal generator 16. As such, a POSITA would understand that Iketani's power on reset (POR) circuit could be used in place of Lee's second

initialization signal generator 16. However, this substitution does not address the failings in Lee.

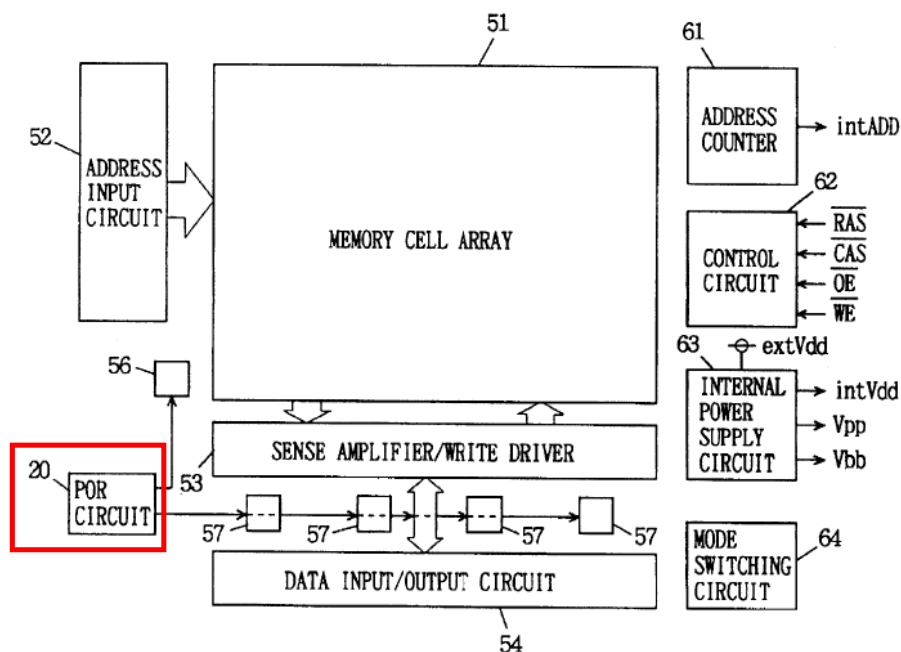
193. Iketani is completely silent as to the claimed “externally applied further command signals”, as is Lee. Iketani discloses a power on reset (POR) circuit that responds solely to the power supply Vdd. Accordingly, Iketani cannot make up for Lee’s lack of disclosure with regards to the claimed “receiving ... externally applied further command signals”.

194. Accordingly, Lee in combination with Iketani does not render obvious at least claim element 1.2 of the ’589 Patent.

2. Claim Element 1.3, “said enable circuit outputting an enable signal after *a predetermined proper initialization sequence of the externally applied further command signals* being identified and *the enable signal effecting an unlatching of said control circuit*” is not disclosed in Lee in view of Iketani

195. The Petition combines Lee and Iketani by substituting Iketani’s power on reset (POR) circuit in Iketani’s Fig. 6 with Lee’s initialization circuit (Ex. 1005, Fig. 3). (Petition, pg. 60.) Iketani’s Fig. 6 is reproduced below with the substitution location argued by Petitioner boxed in red.

FIG. 6



196. This combination fails to make up for what is missing in Lee.

197. As already explained, Lee fails to show or suggest use of *command* signals. At best, Lee uses *control* signals. Iketani is silent as to command signals, a sequence of command signals, let alone identifying command signals. Iketani fails to make up for what is missing in Lee.

198. Petitioner argues that Lee's initialization circuit could initialize the circuitry in Iketani. (Petition, pp. 59-61, citing Ex. 1003 ¶ 140.) Initializing a circuit is not the same as the claimed "unlatching." Initializing simply places a circuit into a known condition. Latching holds a state. Circuits that do not hold a state can be initialized, as well as latched circuits can be initialized to a known state. Initialization does not imply that the circuit being initialized holds a state or

not. Furthermore, only circuits that hold a state can be unlatched, or in other words, able to change their state.

199. Iketani is completely silent as to unlatching. Petitioner has failed to explain how a two-state condition taught in the '589 Patent for latched and unlatched can be obviated by Iketani's POR_ pulse (low-high-low logic level) that transitions back to its original state, which would be "latched" according to the '589 Patent. Lee suffers from the same failings.

200. Accordingly, Lee in combination with Iketani does not render obvious at least claim element 1.3 of the '589 Patent.

3. **Claim Element 11.2, "supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and *further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals* the enable signal being generated and *effecting an unlatching of a control circuit* provided for a proper operation of the dynamic semiconductor memory device" is not disclosed in Lee in view of Iketani**

201. Support for claim element 11.2 has already been provided above, will not be repeated here, and is incorporated in this section. Specifically, the support

for claim element 11.2 is found above in Section X.F.1 for claim element 1.2 and Section X.F.2 for claim element 1.3.

202. Claim element 11.2 has at least some of the requirements addressed above with respect to claim elements 1.2 and 1.3. For at least these reasons, Lee in combination with Iketani does not obviate at least claim element 11.2 of the '589 Patent.

G. Claims 2, 8, 10, and 12 are Not Invalid under Ground 5

203. The discussion about Lee in Section VII (above) and the discussion about JESD 21-C in Section VIII (above) are incorporated by reference into this Section X.G. Furthermore, the discussion about Lee (with or without the Melvin Declaration) in Section X.E (above) is incorporated by reference into this Section X.G.

204. Petitioner argues for Ground 5, “The combination of Lee and JESD 21-C disclose the claim elements of claims [2], [8], [10], and [12] for the same reasons as those disclosed in Ground 2 (*see* Section X.B, *supra*). EX1003, ¶¶156-69. These claims recite characteristics of the claimed predetermined proper initialization sequence, and the disclosure of JESD 21-C of such characteristics applies equally whether combined with Kocis or Lee.” (Petition, pg. 65.) Accordingly, the discussion about JESD 21-C in Section X.D (above) is

incorporated by reference into this Section X.G whether combined with Kocis or Lee.

1. **Claim 2, “*externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal*” is not disclosed in Lee in view of JESD 21-C**

205. Lee is silent as to command signals, let alone a sequence of command signals. Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

206. Simply adding JESD 21-C as a reference does not show or suggest that a POSITA would understand that Lee’s control signals should or could be (1) substituted by command signals, and (2) the predetermined proper initialization sequence of command signals are identified by an enable circuit, which Lee does not show or suggest. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to render obvious claim 2.

207. Furthermore, claim 2 is dependent on independent claim 1, which has not been shown to be invalid.

208. Accordingly, Lee in combination with JESD 21-C does not obviate at least claim 2 of the '589 Patent.

2. Claim 8, “the identification of an initialization sequence that is identified as *the predetermined proper initialization sequence* by said enable circuit and generates the enable signal constitutes *a command sequence* conforming to a JEDEC standard” is not disclosed in Lee in view of JESD 21-C

209. Lee is silent as to command signals, let alone “a command sequence.” Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

210. Simply adding JESD 21-C as a reference does not show or suggest what is missing from Lee. A POSITA would not understand that Lee’s control signals should or could be substituted by command signals, let alone “a command sequence.” JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 8.

211. Furthermore, claim 8 is dependent on independent claim 1, which has not been shown to be invalid.

212. Accordingly, Lee in combination with JESD 21-C does not obviate at least claim 8 of the '589 Patent.

3. **Claim 10, “the predetermined proper initialization sequence includes one of the following chronologically successive *command sequences*: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal” is not disclosed in Lee in view of JESD 21-C**

213. Lee is silent as to command signals, let alone “command sequences”, as claimed. Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

214. Simply adding JESD 21-C as a reference does not show or suggest that a POSITA would understand that Lee’s control signals should or could be substituted by command signals. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry.

215. Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 10.

216. Furthermore, claim 10 is dependent on independent claim 1, which has not been shown to be invalid.

217. Accordingly, Lee in combination with JESD 21-C does not obviate at least claim 10 of the '589 Patent.

4. Claim 12, “providing at least one of a preparation *command signal* for word line activation, a refresh *command signal*, and a loading configuration register *command signal* as the further command signals” is not disclosed in Lee in view of JESD 21-C

218. Lee is silent as to command signals, as claimed. Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

219. Simply adding JESD 21-C as a reference does not show or suggest that a POSITA would understand that Lee’s control signals should or could be substituted by command signals. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry.

220. Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 12.

221. Furthermore, claim 12 is dependent on independent claim 11, which has not been shown to be invalid.

222. Accordingly, Lee in combination with JESD 21-C does not obviate at least claim 12 of the '589 Patent.

H. Claims 2, 8, 10, and 12 are Not Invalid under Ground 6

223. The discussion about Lee in Section VII (above), the discussion about JESD 21-C in Section VIII (above), and the discussion about Iketani in Section IX (above) are incorporated by reference into this Section X.H. Furthermore, the discussion about Lee (with or without the Melvin Declaration) in Section X.E (above) is incorporated by reference into this Section X.H.

224. Petitioner argues for Ground 6, “As discussed in Ground 4, to the extent the Patent Owner argues incorrectly that Lee does not disclose or render obvious the claimed control circuit, this ground shows that the combination of Lee and Iketani also discloses the claimed control circuit for controlling operations. *See* Section X.D.2 , *supra*. Otherwise, the combination of Lee, Iketani, and JESD 21-C discloses the claim elements of claims [2], [8], [10], and [12] for the same reasons as those disclosed in Ground 5. *See* Section X.E, *supra*. EX1003, ¶¶172-75.” (Petition, pg. 66.) Accordingly, the discussion for Ground 4 (above) in Section X.F, and the discussion above for Ground 5 (above) in Section X.G are incorporated by reference into this Section X.H.

1. **Claim 2, “*externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal*” is not disclosed in Lee in view of Iketani and JESD 21-C**

225. Lee is silent as to command signals, let alone a sequence of command signals. Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

226. Adding Iketani and JESD 21-C as references does not show or suggest that a POSITA would understand that Lee’s control signals should or could be substituted by command signals, let alone a sequence of commands.

227. Iketani discloses a power on reset (POR) circuit that responds solely to the power supply Vdd (Ex. 1007, Figs. 2, 3, 7, 8), and generates a POR_ signal that pulses with a low-high-low logic level (Ex. 1007, Fig. 4). A POSITA would understand Iketani’s power on reset (POR) circuit as an improvement over Lee’s second initialization signal generator 16. As such, a POSITA would understand that Iketani’s power on reset (POR) circuit could be used in place of Lee’s second initialization signal generator 16. However, Iketani is silent as to identifying “the predetermined proper initialization sequence ... by said enable circuit”.

228. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 2.

229. Iketani in combination with JESD 21-C fail to make up for what is missing in Lee.

230. Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 2.

231. Furthermore, claim 2 is dependent on independent claim 1, which has not been shown to be invalid.

232. Accordingly, Lee in combination with Iketani and JESD 21-C does not obviate at least claim 2 of the '589 Patent.

2. Claim 8, “the identification of an initialization sequence that is identified as *the predetermined proper initialization sequence* by said enable circuit and generates the enable signal constitutes *a command sequence* conforming to a JEDEC standard” is not disclosed in Lee in view of Iketani and JESD 21-C

233. Lee is silent as to command signals, let alone “a command sequence.” Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

234. Adding Iketani and JESD 21-C as references does not show or suggest what is missing from Lee. A POSITA would not understand that Lee's control signals should or could be substituted by command signals, let alone a "command sequence."

235. Iketani discloses a power on reset (POR) circuit that responds solely to the power supply Vdd (Ex. 1007, Figs. 2, 3, 7, 8), and generates a POR_ signal that pulses with a low-high-low logic level (Ex. 1007, Fig. 4). A POSITA would understand Iketani's power on reset (POR) circuit as an improvement over Lee's second initialization signal generator 16. As such, a POSITA would understand that Iketani's power on reset (POR) circuit could be used in place of Lee's second initialization signal generator 16. However, Iketani is silent as to "the predetermined proper initialization sequence."

236. JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry.

237. Iketani in combination with JESD 21-C fail to make up for what is missing in Lee.

238. Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 8.

239. Furthermore, claim 8 is dependent on independent claim 1, which has not been shown to be invalid.

240. Accordingly, Lee in combination with Iketani and JESD 21-C does not obviate at least claim 8 of the '589 Patent.

3. **Claim 10, “the predetermined proper initialization sequence includes one of the following chronologically successive *command sequences*: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal” is not disclosed in Lee in view of Iketani and JESD 21-C**

241. Lee is silent as to command signals, let alone “command sequences”, as claimed. Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

242. Simply adding Iketani and JESD 21-C as references does not show or suggest that a POSITA would understand that Lee’s control signals should or could be substituted by command signals.

243. Iketani discloses a power on reset (POR) circuit that responds solely to the power supply Vdd (Ex. 1007, Figs. 2, 3, 7, 8), and generates a POR_ signal that pulses with a low-high-low logic level (Ex. 1007, Fig. 4). A POSITA would understand Iketani’s power on reset (POR) circuit as an improvement over Lee’s second initialization signal generator 16. As such, a POSITA would understand

that Iketani's power on reset (POR) circuit could be used in place of Lee's second initialization signal generator 16. However, this substitution does not address the failings in Lee.

244. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 10.

245. Iketani in combination with JESD 21-C fail to make up for what is missing in Lee.

246. Furthermore, claim 10 is dependent on independent claim 1, which has not been shown to be invalid.

247. Accordingly, Lee in combination with Iketani and JESD 21-C does not obviate at least claim 10 of the '589 Patent.

4. Claim 12, “providing at least one of a preparation *command signal* for word line activation, a refresh *command signal*, and a loading configuration register *command signal* as the further command signals” is not disclosed in Lee in view of Iketani and JESD 21-C

248. Lee is silent as to command signals, as claimed. Lee discloses the use of *control* signals, which are not the same as *command* signals as construed in this Declaration.

249. Simply adding Iketani and JESD 21-C as references does not show or suggest that a POSITA would understand that Lee's control signals should or could be substituted by command signals.

250. Iketani discloses a power on reset (POR) circuit that responds solely to the power supply Vdd (Ex. 1007, Figs. 2, 3, 7, 8), and generates a POR_ signal that pulses with a low-high-low logic level (Ex. 1007, Fig. 4). A POSITA would understand Iketani's power on reset (POR) circuit as an improvement over Lee's second initialization signal generator 16. As such, a POSITA would understand that Iketani's power on reset (POR) circuit could be used in place of Lee's second initialization signal generator 16. However, this substitution does not address the failings in Lee.

251. Furthermore, JESD 21-C is a standard for interoperability. JESD 21-C is silent as to any particular circuitry. Accordingly, Petitioner relies on hindsight to actively construct the functionality, let alone the actual circuitry, as claimed to obviate claim 12.

252. Furthermore, claim 12 is dependent on independent claim 11, which has not been shown to be invalid.

253. Accordingly, Lee in combination with Iketani and JESD 21-C does not obviate at least claim 12 of the '589 Patent.

I. Claims 9 and 13 are Not Invalid under Ground 7

254. The discussion about Lee in Section VII (above) and the discussion about Kocis in Section VI (above) are incorporated by reference into this Section X.I. Furthermore, the discussion about Lee (with or without the Melvin Declaration) in Section X.E (above) and the discussion about Kocis (with or without the Melvin Declaration) in Section X.C (above) are incorporated by reference into this Section X.I.

255. Petitioner argues for Ground 7, “A POSITA would have been motivated to use the reset signal output by the initialization circuit of Lee to unlatch the memory device’s output buffers/drivers, as disclosed in Kocis, as one of the various circuitry that are disclosed in Lee as being unlatched in order to ensure the ability to ‘reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions,’ which is the stated goal of Lee (EX1005 at 2:18-20), and to address ‘problems which may arise on a memory bus during system power-up’ such as ‘preventing contention on the memory bus between conflicting data signals from two or more DRAM banks, which is the stated goal of Kocis (EX1004 at 1:11-15). EX1003, ¶177.” (Petition, pg. 67, emphasis added.)

256. First, Lee discloses a low-high-low logic level ϕ RST pulse as an output of the enable circuit as identified by the Petitioner. Kocis discloses a low-to-high logic level KEEP OFF# signal as an output of the enable circuit as

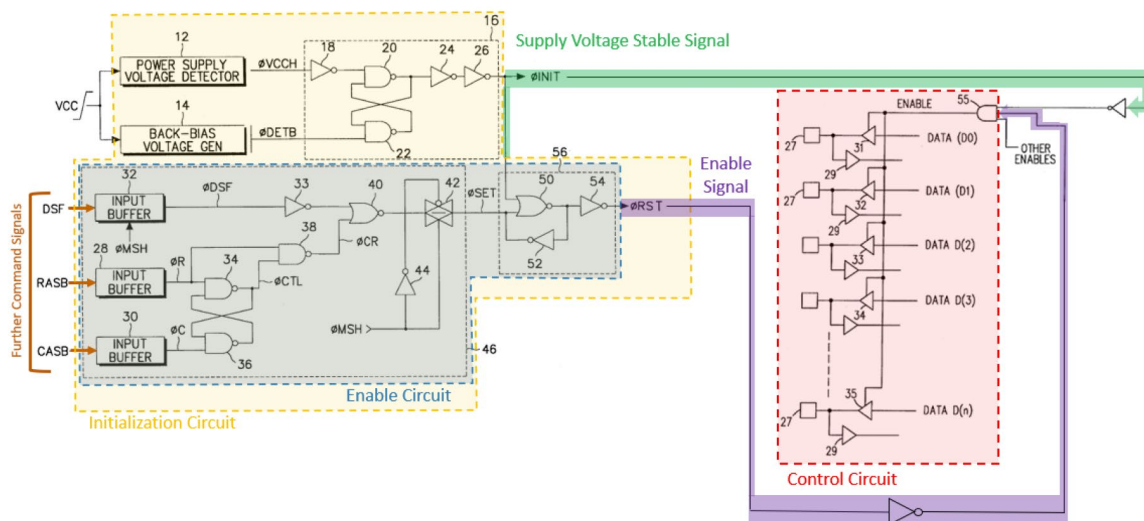
identified by the Petitioner. These two signals act differently. Lee's ϕ RST pulse (as designed) may pulse several times due to power-on reset and normal operation. According to Petitioner, a POSITA would use Lee's low-high-low logic level ϕ RST pulse to drive the three-input AND gate 55 of Kocis. (Petition, pg. 67.) Accordingly, as soon as the ϕ RST signal returns low, the tristate buffers of Kocis will be disabled (go to tristate) during *normal operation* after power up. This is functionally bizarre and results in a non-operable memory device.

257. However, Petitioner went one step further by constructing their own circuit (Petition, pg. 69), in which both the potentially malfunctioning ϕ INIT signal (according to Lee) and the ϕ RST signal are inverted to solve the problem of non-functionality detailed immediately above. However, in doing so, Petitioner has created a circuit that enables the tristate buffers at power up, which has no ability to prevent bus contentions. Preventing bus contentions was the entire problem attempted to be solved by Kocis, and repeated by Petitioner at Petition, pg. 67 (reproduced above). Petitioner's argument that a POSITA would have understood how to create a circuit given Lee and Kocis falls flat, when the Petitioner's Expert creates a circuit that encourages bus contention, which is the opposite of the stated goal by inventor Kocis. For at least this reason, a POSITA would not be motivated to combine Lee and Kocis as claimed by Petitioner.

258. Second, neither Lee nor Kocis shows or suggests latched or unlatched output drivers. Lee is silent as to output drivers. Kocis has tristate output buffers; however, Kocis is silent as to these tristate output buffers having any latch or state maintained by them. Having a signal (ENABLE in Kocis) for the tristate buffers to maintain a value is not equivalent to the output buffers in the control circuit remaining latched. The output drivers themselves need to be latched.

1. **Claim 9, “said control circuit has *output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit*” is not disclosed in Lee in view of Kocis**

259. First, Petitioner crafts a new circuit (reproduced below) by combining Lee and Kocis as an example of what a POSITA might create. (Petition, pg. 69.)



Kocis and Lee Combination

260. Lee discloses a ϕ INIT signal (that when working properly) provides a low-high-low logic level pulse. Lee discloses a ϕ RST signal (that when working properly) provides a low-high-low logic level pulse. Petitioner inverts these signals to provide two high-low-high logic level pulses. These two high-low-high logic level pulses are provided as inputs to AND gate 55 to generate an ENABLE signal that controls a plurality of tristate buffers (31-35). When the ENABLE signal is high, the tristate buffer are enabled to output their respective DATA values. Petitioner has provided input signals to AND gate 55 that are initially at a high logic level. As such, the circuit Petitioner has crafted will immediately have the potential to create bus contentions on power up (if “OTHER ENABLES” are also at a high logic level). The entire point of Kocis’ disclosure was to prevent bus contentions using an enable circuit. The circuit created by Petitioner is incongruous to the stated goal of Kocis.

261. Second, besides simply making the statement, Petitioner has not provided any evidence that Kocis’ output buffers have a latch or can maintain state. Kocis is silent as to his tristate buffers latching or unlatching.

262. Third, the PTAB has recognized (Institution Decision, pg. 32-34) that an input to AND 55 cannot be the claimed “enable signal.” “Thus, tri-state buffers 31, 32, 33, 34, 35 *only are enabled if all [the] input signals are high.*” *Id.* (emphases added) (quoting Ex. 1004, 5:3–12).” (Institution Decision, pg. 33,

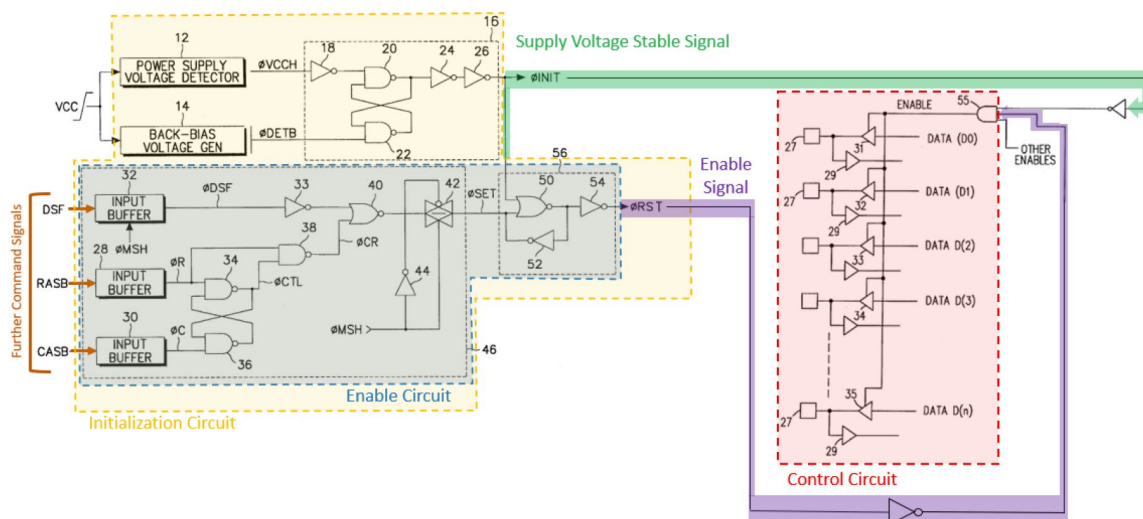
emphasis in original.) Accordingly, Petitioner, with their combination of circuitry from Lee and Kocis, have not demonstrated claim 9 would be obvious over Lee in view of Kocis.

263. Furthermore, claim 9 is dependent on independent claim 1, which has not been shown to be invalid.

264. Accordingly, Lee in combination with Kocis does not obviate at least claim 9 of the '589 Patent.

2. Claim 13, “maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit” is not disclosed in Lee in view of Kocis

265. First, Petitioner crafts a new circuit (reproduced below) by combining Lee and Kocis as an example of what a POSITA might create. (Petition, pg. 69.)



266. *Kocis and Lee Combination*

267. Petitioner references this circuit in their arguments for claim 13. (Petition, pg. 71.) Lee discloses a ϕ INIT signal (that when working properly) provides a low-high-low logic level pulse. Lee discloses a ϕ RST signal (that when working properly) provides a low-high-low logic level pulse. Petitioner inverts these signals to provide two high-low-high logic level pulses. These two high-low-high logic level pulses are provided as inputs to AND gate 55 to generate an ENABLE signal that controls a plurality of tristate buffers (31-35). When the ENABLE signal is high, the tristate buffer are enabled to output their respective DATA values. Petitioner has provided input signals to AND gate 55 that are initially at a high logic level. As such, the circuit Petitioner has crafted will immediately have the potential to create bus contentions on power up (if “OTHER ENABLES” are also at a high logic level). The entire point of Kocis’ disclosure was to prevent bus contentions using an enable circuit. The circuit created by Petitioner is incongruous to the stated goal of Kocis.

268. Second, besides simply making the statement, Petitioner has not provided any evidence that Kocis’ output buffers have a latch or can maintain state. Kocis is silent as to his tristate buffers latching or unlatching.

269. Third, the PTAB has recognized (Institution Decision, pg. 32-34) that an input to AND 55 cannot be the claimed “enable signal.” “Thus, tri-state buffers 31, 32, 33, 34, 35 *only are enabled if all [the] input signals are high.*” *Id.*

(emphases added) (quoting Ex. 1004, 5:3–12).” (Institution Decision, pg. 33, emphasis in original.) Accordingly, Petitioner, with their combination of circuitry from Lee and Kocis, have not demonstrated claim 13 would be obvious over Lee in view of Kocis.

270. Furthermore, claim 13 is dependent on independent claim 11, which has not been shown to be invalid.

271. Accordingly, Lee in combination with Kocis does not obviate at least claim 13 of the ’589 Patent.

J. Claims 9 and 13 are Not Invalid under Ground 8

272. The discussion about Lee in Section VII (above), the discussion about Iketani in Section IX (above), and the discussion about Kocis in Section VI (above) are incorporated by reference into this Section X.J. Furthermore, the discussion about Lee (with or without the Melvin Declaration) in Section X.E (above) and the discussion about Kocis (with or without the Melvin Declaration) in Section X.C (above) are incorporated by reference into this Section X.J.

273. For Ground 8, Petitioner references their support for Ground 7. (Petition, pg. 71.)

274. Accordingly, Petitioner argues for Ground 8, “A POSITA would have been motivated to use the reset signal output by the initialization circuit of Lee to unlatch the memory device’s output buffers/drivers, as disclosed in Kocis, as one

of the various circuitry that are disclosed in Lee as being unlatched in order to ensure the ability to ‘reliably initialize a semiconductor memory device when a power-up reset circuit malfunctions,’ which is the stated goal of Lee (EX1005 at 2:18-20), and to address ‘problems which may arise on a memory bus during system power-up’ such as ‘**preventing contention on the memory bus** between conflicting data signals from two or more DRAM banks, which is the stated goal of Kocis (EX1004 at 1:11-15). EX1003, ¶177.” (Petition, pg. 67, emphasis added.)

275. First, Lee discloses a low-high-low logic level ϕ RST pulse as an output of the enable circuit as identified by the Petitioner. Kocis discloses a low-to-high logic level KEEP OFF# signal as an output of the enable circuit as identified by the Petitioner. These two signals act differently. Lee’s ϕ RST pulse (as designed) may pulse several times due to power-on reset and normal operation. According to Petitioner, a POSITA would use Lee’s low-high-low logic level ϕ RST pulse to drive the three-input AND gate 55 of Kocis. (Petition, pg. 67.) Accordingly, as soon as the ϕ RST signal returns low, the tristate buffers of Kocis will be disabled (go to tristate) during normal operation after power up. This is functionally incongruous and results in a non-operable memory device.

276. However, Petitioner went one step further by constructing their own circuit (Petition, pg. 69), in which both the potentially malfunctioning ϕ INIT signal (according to Lee) and the ϕ RST signal are inverted to solve the problem of non-

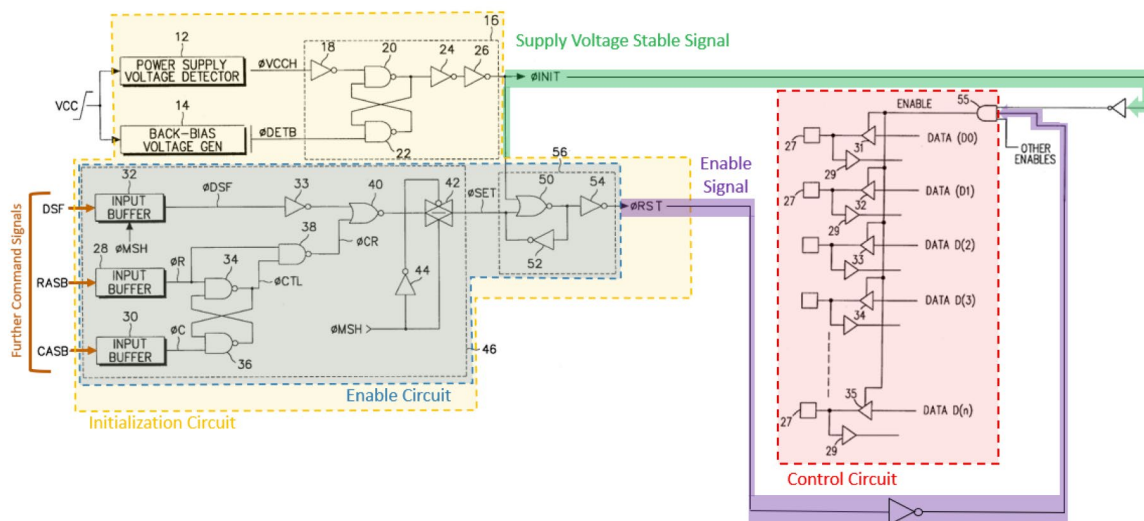
functionality detailed immediately above. However, in doing so, Petitioner has created a circuit that enables the tristate buffers at power up, which has no ability to prevent bus contentions. Preventing bus contentions was the entire problem attempted to be solved by Kocis, and repeated by Petitioner at Petition, pg. 67 (reproduced above). Petitioner's argument that a POSITA would have understood how to create a circuit given Lee, Iketani, and Kocis falls flat, when the Petitioner's Expert creates a circuit that encourages bus contention, which is the opposite of the stated goal by inventor Kocis. For at least this reason, a POSITA would not be motivated to combine Lee and Kocis (with or without Iketani) as claimed by Petitioner.

277. Second, neither Lee, Iketani, nor Kocis shows or suggests latched or unlatched output drivers. Lee is silent as to output drivers. Iketani makes a passing reference to the existence of a data input/output circuit 54, which is not subject to initialization. (Iketani, 5:24-26.) Kocis has tristate output buffers; however, Kocis is silent as to these tristate output buffers having any latch or state maintained by them. Having a signal (ENABLE in Kocis) for the tristate buffers to maintain a value is not equivalent to the output buffers in the control circuit remaining latched. The output drivers themselves need to be latched.

278. Petitioner arguments for Ground 8 are based on Ground 4. (Petition, pg. 71.) Accordingly, the Ground 4 Section X.F (above) is incorporated by reference into this Section X.J.

1. **Claim 9, “said control circuit has *output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit*” is not disclosed in Lee in view of Iketani and Kocis**

279. First, Petitioner crafts a new circuit (reproduced below) by combining Lee and Kocis as an example of what a POSITA might create. (Petition, pg. 69.)



Kocis and Lee Combination

280. Lee discloses a ϕ INIT signal (that when working properly) provides a low-high-low logic level pulse. Lee discloses a ϕ RST signal (that when working properly) provides a low-high-low logic level pulse. Petitioner inverts these signals to provide two high-low-high logic level pulses. These two high-low-high

logic level pulses are provided as inputs to an AND gate 55 to generate an ENABLE signal that controls a plurality of tristate buffers (31-35). When the ENABLE signal is high, the tristate buffer are enabled to output their respective DATA values. Petitioner has provided input signals to AND gate 55 that are initially at a high logic level. As such, the circuit Petitioner has crafted will immediately have the potential to create bus contentions on power up (if “OTHER ENABLES” are also at a high logic level). The entire point of Kocis’ disclosure was to prevent bus contentions using an enable circuit. The circuit created by Petitioner is incongruous to the stated goal of Kocis.

281. Second, besides simply making the statement, Petitioner has not provided any evidence that Kocis’ output buffers have a latch or can maintain state. Kocis is silent as to his tristate buffers latching or unlatching.

282. Third, Iketani’s circuit (Figs. 2, 3, 7, 8) with a low-high-low logic level pulse (Iketani, Fig. 4) is a reasonable replacement for Lee’s second initialization signal generator 16. Otherwise, Iketani does not make up for what is missing in Lee and Kocis.

283. Fourth, the PTAB has recognized (Institution Decision, pg. 32-34) that an input to AND 55 cannot be the claimed “enable signal.” “Thus, tri-state buffers 31, 32, 33, 34, 35 *only are enabled if all [the] input signals are high.*” *Id.* (emphases added) (quoting Ex. 1004, 5:3–12).” (Institution Decision, pg. 33,

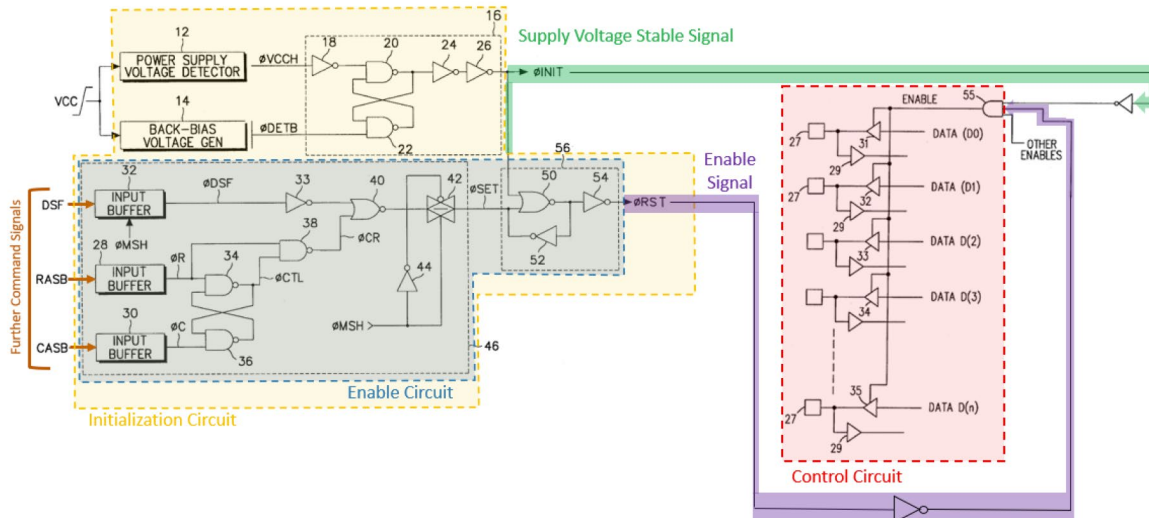
emphasis in original.) Accordingly, Petitioner, with their combination of circuitry from Lee, Kocis, and Iketani, have not demonstrated claim 9 would be obvious over Lee in view of Iketani and Kocis.

284. Furthermore, claim 9 is dependent on independent claim 1, which has not been shown to be invalid.

285. Accordingly, Lee in combination with Iketani and Kocis does not obviate at least claim 9 of the '589 Patent.

2. Claim 13, “*maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit*” is not disclosed in Lee in view of Iketani and Kocis

286. First, Petitioner crafts a new circuit (reproduced below) by combining Lee and Kocis as an example of what a POSITA might create. (Petition, pg. 69.)



Kocis and Lee Combination

287. Petitioner references this circuit in their arguments for claim 13. (Petition, pg. 71.) Lee discloses a ϕ INIT signal (that when working properly) provides a low-high-low logic level pulse. Lee discloses a ϕ RST signal (that when working properly) provides a low-high-low logic level pulse. Petitioner inverts these signals to provide two high-low-high logic level pulses. These two high-low-high logic level pulses are provided as inputs to AND gate 55 to generate an ENABLE signal that controls a plurality of tristate buffers (31-35). When the ENABLE signal is high, the tristate buffer are enabled to output their respective DATA values. Petitioner has provided input signals to AND gate 55 that are initially at a high logic level. As such, the circuit Petitioner has crafted will immediately have the potential to create bus contentions on power up (if “OTHER ENABLES” are also at a high logic level). The entire point of Kocis’ disclosure

was to prevent bus contentions. The circuit created by Petitioner is incongruous to the stated goal of Kocis.

288. Second, besides simply making the statement, Petitioner has not provided any evidence that Kocis' output buffers have a latch or can maintain state. Kocis is silent as to his tristate buffers latching or unlatching.

289. Third, Iketani's circuit (Figs. 2, 3, 7, 8) with a low-high-low logic level pulse (Iketani, Fig. 4) is a reasonable replacement for Lee's second initialization signal generator 16. Otherwise, Iketani does not make up for what is missing in Lee and Kocis.

290. Fourth, the PTAB has recognized (Institution Decision, pg. 32-34) that an input to AND 55 cannot be the claimed "enable signal." "Thus, tri-state buffers 31, 32, 33, 34, 35 *only are enabled if all [the] input signals are high.*" *Id.* (emphases added) (quoting Ex. 1004, 5:3–12)." (Institution Decision, pg. 33, emphasis in original.) Accordingly, Petitioner, with their combination of circuitry from Lee, Kocis, and Iketani, have not demonstrated claim 13 would be obvious over Lee in view of Iketani and Kocis.

291. Furthermore, claim 13 is dependent on independent claim 11, which has not been shown to be invalid.

292. Accordingly, Lee in combination with Iketani and Kocis does not obviate at least claim 13 of the '589 Patent.

XI. CONCLUSIONS

293. As set forth above, it is my opinion that none of the art referenced by the Petitioner in the Petition and discussed by the Melvin Declaration (Ex. 1003) invalidates any of the claims 1, 2, 8, 9, 10, 11, 12, and 13 of the '589 Patent. Furthermore, the Board did not address claim 13 in its Institution Decision.

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signed in Plano, Texas, on December 10, 2023

/s/ Timothy D. Dorney

Timothy D. Dorney, Ph.D.

Appendix A

Timothy D. Dorney, Ph.D.

3501 Pennsylvania Lane
Plano, TX 75075-7810
tdorney@ieee.org

Mobile: 214-364-9511
Direct: 469-467-6560
Citizenship: U.S.A.

EDUCATION

- **Rice University**
Doctor of Philosophy in Electrical and Computer Engineering, January 2002
Thesis Title: *Material Parameter Estimation and Imaging with Terahertz Time-Domain Spectroscopy*
Thesis Advisor: Dr. Daniel Mittleman
- **Case Western Reserve University**
Master of Science in Electrical Engineering and Applied Physics, May 1992
Thesis Title: *Learned Adaptive Environment Control using Artificial Neural Networks and Fuzzy Logic*
Thesis Advisor: Dr. Yoh-Han Pao
- **Texas A&M University**
Bachelor of Science in Electrical Engineering (Cum Laude, University Honors), May 1990

REGISTRATIONS / MEMBERSHIPS

- United States Patent and Trademark Office, Patent Agent, Registration Number 51,623
- Institute of Electrical and Electronics Engineers, Member

DEPOSITIONS

- *Personalized Media Communications, LLC v. Google LLC*
EDTX Case No. 2:19-cv-00090-JRG
- *Personalized Media Communications, LLC v. Netflix, Inc.*
EDTX Case No. 2:19-cv-00091-JRG
Firm: Susman Godfrey LLP
Deposed as a Rule 30(b)(1) witness, March 2020
- *Apple Incorporated v. Personalized Media Communications, LLC*
USPTO Inter Partes Review, IPR2016-00754 and IPR2016-00755
Firm: Goodwin Proctor LLP
Deposed as an Expert in support of claim amendments, February 2017
- *Personalized Media Communications, LLC v. Samsung Electronics America, Inc.*
EDTX Case No. 2:15-cv-01754-JRG-RSP
Firm: Susman Godfrey LLP
Deposed as a Rule 30(b)(1) witness, November 2016

EXPERT WITNESS

- *Xueshan Technologies, Inc. v. Renesas Electronics Corporation*
EDTX Case No. 2:22-cv-00157-JRG-RSP
Firm: Nelson Bumgardner Conroy PC representing Xueshan Technologies, Inc.
Case Disposition: Settled
- *Polaris Innovations Limited v. Broadcom, Inc.*
EDTX Case No. 2:22-cv-00347-JRG
Firm: Nelson Bumgardner Conroy PC representing Polaris Innovations Limited
Case Disposition: Settled

EMPLOYMENT

- **Personalized Media Communications, LLC, Sugar Land, TX** **2014 - Present**
Vice President – Intellectual Property
Responsibilities include working on both patent licensing and patent litigation activities for approximately 100 assets originated by the same inventors. Responsible for the identification of potential patent infringement, design and execution of tests to show infringement, claim chart creation, presentation of those findings to accused infringers, and negotiation of settlement agreements. Have also been heavily involved in approximately 20 Inter Partes Reviews. Responsible for ex parte reexamination and reissue patent filings.
- **Uviri, LLC, Plano, TX** **2009 - Present**
President
The company is involved with many different types of research projects and business activities, including the following:
 - Consulting services related to the review of patents and the enforcement of patent rights.
 - Preparation and prosecution of U.S. patent applications.
 - Research and design of a new type of fractional horsepower electric motor.
 - Basic research and development into an alternative to Fourier decomposition.
 - Product and electrical design of A-series and T-series LED lighting systems.
 - Product and electrical design of small wattage AC/DC converters.
 - Research and design of a rotating optical oscillator for use in terahertz time-domain spectroscopy systems.
 - Provide photography and photographic services.
- **Texas Instruments Incorporated, Dallas, TX** **2003 - 2014**
Patent Licensing Associate
Responsible for the assertion and defense of patents in technical fields including DRAM and nonvolatile memory, analog circuits, image sensors, digital displays, processors, and digital systems. Identified patents of interest from a pool of over 14,000 assets. Created

claim charts to demonstrate infringement and presented those findings to accused infringers. Managed multiple teams working to identify patent infringement, to ascertain the scope of reverse engineering, and to create uniform claim charts across all teams. Worked with licensees in Japan, Asia Pacific Region, North America, and Europe. Licensing revenue generated during this employment exceeded U.S. \$3 billion. Also maintained a small docket of patents submitted for ex parte reexamination with the USPTO.

- **Rosenthal & Osha L.L.P., Houston, TX** **2001 - 2003**
Patent Agent
Prepared over 50 utility patent applications per year by applying a broad background of experience. Technical fields for the applications included analog and digital circuits, microprocessor architecture, computer system design, and digital signal processing (DSP). Responded to both national and international Office Actions, and filed RCEs in response to Advisory Actions. Managed a five-person team focused on protecting microprocessor core IP. Mentored patent engineers and reviewed draft applications.

- **Rice University, Houston, TX** **1994 - 2001**
Research Associate - Department of Electrical and Computer Engineering
Applied a wide variety of DSP techniques to investigate terahertz (THz) time-domain spectroscopy signals. Solved inverse problems, improved resolution, and facilitated imaging and classification for real-time THz systems. Authored numerous journal articles and conference papers, and presented findings at numerous conferences (listed below). Other areas of investigation included wavelets, speech processing, biomedical imaging, and computer architecture.

- **Texas Instruments Incorporated, Houston, TX** **1988 - 1998**
1997 - 1998 Circuits Center of Expertise Engineer - Memory Products Design
Originated comparisons of internal and competitor DRAM designs through simulation, characterization, deprocessing, and internal probe. Identified and evaluated key aspects of DRAM designs by interacting with design teams, product engineering, and external resources to gather and disseminate information. Built web pages to report the analysis to a broad audience. Integrated information and made sound conclusions from which future designs could draw.

Personal accomplishments included the following:
 - Promoted and helped implement the formation of the Circuits COE that resulted in being the only individual contributor chosen from the Houston design center.
 - Achieved an 8% speed improvement in access time through a redesign of the critical path and output buffers.
 - Identified and correlated device processing characteristics which degraded signal transmission and device performance.

- Simulated and summarized the work on competing access versus hold time specifications which demonstrated that additional regulation circuitry was not needed.
- Texas Instruments representative during SynchLink DRAM (MOSAID) engagement.

1990 - 1997 IC Design Engineer - Application Specific DRAM Design

Demonstrated engineering breadth and depth through the design, simulation, probe, debug, and test support of various major sections on at least five DRAM devices, two of which had 95M units shipped with \$525M in sales. These included row and row redundancy, column and column redundancy, design-for-test, I/O buffers, internal refresh, and data I/O. Performed full-chip schematic verification, design rule verification, and probe versus simulation comparison. Supported the lead frame design, ESD implementation, parasitic back annotation, laser repair, and layout.

Personal accomplishments included the following:

- Originated numerous patents (listed below) that focused on reduced silicon usage and improved DRAM performance.
- Traveled to Japan (KTI) and Singapore (TECH) to provide DRAM design support and training.
- Traveled to TI-Singapore for DRAM T3/batch testing support.
- Investigated and audited TI's first commercial 64 megabit Synchronous DRAM column, internal refresh, voltage regulators, and power-up circuitry.
- Selected point person by V.P. to assemble a team, create, and help instruct "DRAM Design for Non-DRAM Designers". Implemented the course both in Europe and Asia Pacific Region.
- Provided weekly training of DRAM design basics to Houston PDE/CQE engineers.
- Mentored and supervised engineers and layout support to achieve on-time schematic verification.
- Spearheaded new hire activities and on-campus recruiting which resulted in at least ten new employees.

1988 - 1990 Product Development Engineer - Video RAM Development

Programmed a PWS Colt IIIA device tester for gross functional tests and test time reduction. Drafted specification sheets. Created and updated device comparison tables. Resolved customer issues including returned device evaluation and device specification comparison.

PUBLICATIONS

Book Chapters

- "Multistatic Reflection Imaging with Terahertz Pulses," T. Dorney, W. W. Symes, and D. Mittleman, in Terahertz Sensing Technology, Vol. 1. Electronic Devices and Advanced Systems Technology, Ed. D. Woolard, W. Loerop, and M. Shur, World Scientific Publishing, Singapore (2003), pp. 327-349.

Refereed Journal Articles

- Timothy D. Dorney, William W. Symes, Daniel M. Mittleman, “Multistatic Reflection Imaging with Terahertz Pulses”, *International Journal of High Speed Electronics and Systems*, Vol. 13, Issue 02, pp. 677-699, June, 2003.
- Timothy D. Dorney, Molly Rossow, William W. Symes, Daniel M. Mittleman, “Single-cycle Terahertz Electromagnetic Pulses: A New Test Bed for Physical Seismic Modeling”, *Geophysics*, Vol. 68, No. 1, pp. 308-313, January, 2003.
- Timothy D. Dorney, William W. Symes, Richard G. Baraniuk, Daniel M. Mittleman, “Terahertz Multistatic Reflection Imaging”, *Journal of the Optical Society of America A*, Vol. 19, Issue 7, pp. 1432-1442, 2002.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, “Enhanced Depth Resolution Using Phase-Shift Interferometry”, *Optics and Photonics News*, Vol. 12, December, 2001.
- Timothy D. Dorney, Jon L. Johnson, James Van Rudd, Richard G. Baraniuk, William Symes, Daniel M. Mittleman, “Terahertz Reflection Imaging using Kirchhoff Migration”, *Optics Letters*, Vol. 26, No. 19, pp. 1513-1515, October, 2001.
- Timothy D. Dorney, Richard G. Baraniuk, Daniel M. Mittleman, “Material Parameter Estimation with Terahertz Time-Domain Spectroscopy”, *Journal of the Optical Society of America A*, Vol. 18, Issue 7, pp. 1562-1571, August, 2001.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, “Interferometric Imaging with Terahertz Pulses”, *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 7, Issue 4, pp. 592-599, July-Sept., 2001.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, “Enhanced Depth Resolution in Terahertz Imaging using Phase-Shift Interferometry”, *Applied Physics Letters*, Vol. 78, pp. 835-837, February, 2001.
- Timothy D. Dorney, “An Introduction to Fuzzy Logic Control”, *Texas Instruments Technical Journal*, Vol. 10, No. 4, July/August, 1993, pp. 84-89.
- Timothy D. Dorney, “An Improved Architecture and Training Technique for Artificial Neural Networks”, *Texas Instruments Technical Journal*, Vol. 10, No. 3, May/June, 1993, pp. 10-17.

Other Articles

- Jon L. Johnson, Tim Dorney, and Daniel Mittleman, “Enhanced depth resolution using phase-shift interferometry,” *Optics and Photonics News, Special Issue: Optics in 2001*, 12, 21, December 2001.

Conference Proceedings

- Timothy D. Dorney, Jon Johnson, Daniel M. Mittleman, Richard G. Baraniuk, “Imaging with Terahertz Pulses”, *Proceedings of SPIE - The International Society for Optical Engineering*, SPIE 4115, Applications of Digital Image Processing XXIII, December, 2000.
- J. L. Johnson, T. D. Dorney, J. V. Rudd, and D. M. Mittleman, “Terahertz Reflectometry: A Model System for the Inverse Problem,” *ITW 2000 – International Terahertz Workshop*, p. 39, Sandbjerg, Denmark, December 2000.
- J. L. Johnson, T. D. Dorney, J. V. Rudd, and D. M. Mittleman, “Terahertz Reflectometry: A Model System for the Inverse Problem,” *IEEE/LEOS Annual Meeting Conference Proceedings*, Vol. 1, p. 242, Rio Grande, Puerto Rico, November 2000.
- Timothy D. Dorney, Srikrishna Bhashyam, Andrew Doran, Hyeokho Choi, Patrick Flandrin, Richard G. Baraniuk, “Edge Localized Image Sharpening via Reassignment with Application to Computed Tomography”, *Proceedings of SPIE - The International Society for Optical Engineering*, SPIE 4121, Mathematical Modeling, Estimation, and Imaging, October, 2000.
- Jon L. Johnson, Timothy D. Dorney, Daniel M. Mittleman, “Background-free THz Imaging using Interferometric Tomography”, *Ultrafast Phenomena XII*, Springer Series in Chemical Physics, Vol. 66, pp. 262-264, Springer, Charleston, SC, July 2000.
- Timothy D. Dorney, Jon Johnson, Daniel M. Mittleman, Richard G. Baraniuk, “Imaging with THz Pulses”, *International Conference on Image Processing* 1:764-767, Vol. 1, February, 2000.
- J.L. Johnson, Timothy D. Dorney, James V Rudd, Daniel M. Mittleman, “Terahertz Reflectometry: A Model System for the Inverse Problem”, *Conference Proceedings - Lasers and Electro-Optics Society Annual Meeting-LEOS* 1:242 Vol.1, February, 2000.
- Timothy D. Dorney, Richard G. Baraniuk, Daniel M. Mittleman, “Spectroscopic Imaging using Terahertz Time-Domain Signals”, *4th IEEE Southwest Symposium on Image Analysis and Interpretation*, Austin, TX, USA, 2000. *Proceedings. 4th IEEE Southwest Symposium*, April 2-4, 2000.
- J. L. Johnson, T. Dorney and D. Mittleman, “Background-free THz imaging using interferometric tomography”, *Conference on Lasers and Electro-Optics (CLEO 2000). Technical Digest. Postconference Edition. TOPS Vol.39* (IEEE Cat. No.00CH37088), San Francisco, CA, USA, 2000, pp. 526-527.

Presentations

- “Terahertz Reflectometry: A Model System for the Inverse Problem”, presented at the IEEE/LEOS Annual Meeting Conference, Rio Grande, Puerto Rico, November, 2000.

- “Edge localized image sharpening via reassignment with application to computed tomography”, presented at the SPIE Mathematical Modeling, Estimation, and Imaging Conference, San Diego, CA, July 31, 2000.
- “Identification and Classification of Materials Using Terahertz Time-Domain Spectroscopy”, presented at the Rice Quantum Institute Summer Research Colloquium, August 20, 1999.

PATENTS

- U.S. Patent Number 7,046,412, “Scanning optical delay line using a reflective element arranged to rotate”, Timothy D. Dorney, May 16, 2006.
- Korean Patent Number KR100336951B1, “Method and apparatus for testing memory circuits using parallel block write operations”, Timothy Dominic Dorney, Anthony Michael Balistreri, September 9, 2002.
- U.S. Patent Number 6,091,665, “Synchronous random access memory having column factor counter for both serial and interleave counting”, Timothy D. Dorney, July 18, 2000.
- U.S. Patent Number 6,088,274, “Method and device for testing a semiconductor serial access memory device through a main memory”, Timothy D. Dorney, Steven C. Eplett, Rishad S. Omer, John E. Riley, July 11, 2000.
- U.S. Patent Number 6,084,811, “Phased sense amplifiers”, Timothy D. Dorney, July 4, 2000.
- U.S. Patent Number 5,920,573, “Method and apparatus for reducing area and pin count required in design for test of wide data path memories”, Timothy D. Dorney, July 6, 1999.
- German Patent Number DE69505806T2, “Method and device for a design for testing a memory with parallel block-write operation”, Timothy Dominic Dorney, Anthony Michael Balistreri, May 12, 1999.
- European Patent Number EP0757837B1, “A method and apparatus for testing a memory circuit with parallel block write operation”, Timothy Dominic Dorney, Anthony Michael Balistreri, November 4, 1998.
- U.S. Patent Number 5,740,179, “Method and apparatus for a design for test, parallel block write operation”, Timothy Dominic Dorney, Anthony Michael Balistreri, April 14, 1998.
- U.S. Patent Number 5,732,030, “Method and system for reduced column redundancy using a dual column select”, Timothy D. Dorney, March 24, 1998.

SKILLS & ADVANCED COURSES

Languages: C, Windows C, FORTRAN, Pascal, Assembly, BASIC, PWS tslang

Programs: TISpice, Cadence Analog Artist, Mentor Graphics Design Architect and IC Station, ADCAP, ICE, LSIM, Siganal, MATLAB, HTML, Windows, UNIX, AWK, Texas Instruments and Microchip Technology Integrated Development Environment, Interleaf, Microsoft Office, Adobe Photoshop, Nikon Capture, Imagenomic Portraiture, Alibre, KeyShot

Hardware: PC, Macintosh, DEC, HP, Apollo, Sun, PWS Colt IIIA device testers, Texas Instruments and Microchip Technology development boards

- Six Sigma Design for Manufacturability
- Advanced DSP
- Digital Image Processing
- VLSI Design and Layout
- Filter Theory
- Image Feature Extraction
- Spectral Estimation
- Computer Architecture
- Communication Theory
- Digital System Design
- Wavelets
- Random Processes
- Digital Control
- Artificial Neural Networks
- Fuzzy Logic
- Speech Processing
- Leading Effective Meetings
- Presentation Skills
- PC Board Design, Manufacture, and Test
- Laboratory Bench Testing
- Photography
- Photo editing tools