

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

V.

POLARIS INNOVATIONS LIMITED,

Patent Owner

IPR2023-00516

Patent No. 6,157,589

Deposition of
STEPHEN W. MELVIN, Ph.D.
Tuesday, November 21, 2023

REPORTED BY: JOHN WISSENBACH, RDR, CRR, CSR 6862

Page 2	Page 4
1 INDEX OF EXAMINATIONS 2 Page 3 WITNESS: 4 STEPHEN W. MELVIN, Ph.D. 5 Examination by Mr. DeZern 4 6 7 * * * * 8 9 EXHIBITS REFERENCED 10 Exhibit 1003 (Deposition Exhibit 1) 11 Exhibit 1005 (Deposition Exhibit 2) 12 Exhibit 1006 (Deposition Exhibit 3) 13 14 * * * * 15 16 17 18 19 20 21 22 23 24 25	1 THE VIDEOGRAPHER: We are now on the record 2 for the video deposition of Dr. Stephen Melvin -- 3 the time is 8:33 a.m. November 21st, 2023 -- in the 4 matter of Xilinx, Incorporated vs. Polaris 5 Innovations Limited, IPR Number 2023-00516, being 6 held in the United States Patent and Trademark 7 Office before the Patent Trial and Appeal Board. 8 The court reporter is John Wissenbach, the 9 videographer is Gus Phillips, and both are 10 representatives of GregoryEdwards LLC. 11 Will counsel please state their appearances 12 for the record, beginning with the petitioner. 13 MR. KAPADIA: Yes. Aashish Kapadia, for 14 petitioner, Xilinx, Incorporated. 15 MR. DeZERN: And David DeZern, of Nelson 16 Bumgardner Conroy, for the respondent, Polaris. 17 THE VIDEOGRAPHER: Will the court reporter 18 please administer the oath. 19 STEPHEN W. MELVIN, Ph.D., 20 having been first duly sworn, testified as follows: 21 EXAMINATION BY MR. DeZERN 22 Q. All right. Good morning. 23 A. Good morning. 24 Q. Could you please state your name. 25 A. Yes. Stephen Melvin.
Page 3	Page 5
1 BE IT REMEMBERED that, pursuant to the laws 2 governing the taking and use of depositions, on 3 Tuesday, November 21, 2023, commencing at 8:33 a.m., 4 before me, JOHN WISSENBACH, CSR 6862, of San 5 Francisco, California, appeared through 6 videoconference STEPHEN W. MELVIN, Ph.D., at Delta, 7 British Columbia, Canada, called as a witness by the 8 Patent Owner, who, being by me first duly sworn, was 9 thereupon examined as a witness in said action. 10 APPEARANCES OF COUNSEL VIA VIDEOCONFERENCE 11 For the Petitioner: 12 McDERMOTT WILL & EMERY LLP 13 BY: AASHISH KAPADIA, Attorney at Law 14 BRIAN W. OAKS, Attorney at Law 15 300 Colorado Street, Suite 2200 16 Austin, Texas 78701 17 (512) 298-6488 akapadia@mwe.com 18 (512) 726-2574 boaks@mwe.com 19 For the Patent Owner: 20 NELSON BUMGARDNER CONROY PC 21 BY: DAVID T. DeZERN, Attorney at Law 22 2727 N. Harwood Street, Suite 250 23 Dallas, Texas 75201 24 (214) 446-4958 david@nelbum.com 25 ALSO PRESENT: GUS PHILLIPS, Videographer 26 27 * * * * 28 29 30 31	1 Q. And Dr. Melvin, because this is a remote 2 deposition and we aren't in the same room, do you 3 have any materials, written or electronic, with you 4 today? 5 A. I don't. 6 Q. Do you intend to open any materials during 7 the course of this deposition? 8 A. Only the PDFs that -- that you put in the 9 chat box. 10 Q. Okay. Well, I'd just ask you, if there's 11 any materials you might want to open that you have 12 accessible, please let me know, so that we can mark 13 them and keep a clean record of this deposition. Is 14 that okay? 15 A. Okay. That's fine, yes. 16 Q. And do you have access to any chat or 17 messaging applications other than through this Zoom 18 platform that we are using? 19 A. Not at the moment, no. 20 Q. Okay. Will you let me know if you receive 21 any messages during this deposition? 22 A. Yes. 23 Q. And is there anyone else in the room with 24 you? 25 A. No.

Page 6 1 Q. And will you please advise if anyone does 2 enter? 3 A. Yes, I will. 4 Q. Okay. Dr. Melvin, you've been deposed 5 before, right? 6 A. Yes. 7 Q. Approximately how many times? 8 A. 20 -- 20 to 30 times, maybe. 9 Q. Okay. So you know the drill. I'll ask 10 questions. You're under oath to answer. Your 11 counsel may object, but you still have to answer. 12 Is that okay? 13 A. Yes. 14 Q. And if you need a break, please just let me 15 know. We can do that. But I'd ask that you finish 16 responding to any pending questions. 17 A. Okay. 18 Q. Any reason you can't testify truthfully to 19 the best of your ability today? 20 A. No. 21 (Deposition Exhibit 1 was marked for 22 identification.) 23 BY MR. DeZERN: 24 Q. All right. Now, I'm going to mark as 25 Exhibit 1 -- which, as we discussed, I'm submitting	Page 8 1 A. Yes. 2 Q. Did anyone else contribute to the work or 3 analysis for your opinions in this declaration? 4 A. I don't recall any. 5 Q. Okay. And in your declaration, you 6 provided your opinions regarding the validity of the 7 '589 patent based on several different references, 8 right? 9 A. That's correct. 10 Q. So I just have to -- I just want to ask a 11 few questions about some of -- some of those 12 opinions. And let's start with -- well, actually, 13 we can -- if you still have the second page of your 14 declaration pulled up, some of the opinions you 15 provided were based on a reference which is listed 16 here as 1005, U.S. Patent Number 5,774,402, to Lee, 17 correct? 18 A. That's correct. 19 Q. And can we just refer to that as the Lee 20 reference this morning? 21 A. Yeah, sure. 22 Q. Okay. So if you will flip in your 23 declaration to page 70, I believe. Please let me 24 know when you're there. 25 A. Okay. That's page 70 on the bottom or --
Page 7 1 through the chat. And it will upload. And I'll 2 give you a second. Please let me know when you've 3 got that. 4 A. Okay. I have it. Shall I open it? 5 Q. Please. 6 A. Okay. I see it. 7 Q. And is this Exhibit 1 your declaration? 8 A. Yes, it is. 9 Q. And specifically, just looking at the top 10 of it, this is a declaration you submitted in this 11 IPR, which relates to -- actually, the patent 12 number's not on the top, is it? -- the -- if you go 13 to the second page, this is about your opinions 14 regarding U.S. Patent Number 6,157,589, correct? 15 A. That's correct. 16 Q. And could we just refer to that as the '589 17 patent this morning? 18 A. Sure. 19 Q. Dr. Melvin, was anyone else involved in 20 creating this declaration? 21 A. Well, I worked with the attorneys on it. 22 Q. Your counsel defending you today? 23 A. Yes. 24 Q. And potentially other lawyers at his law 25 firm, I presume?	Page 9 1 Q. It is. And it should also be page 70 in 2 the PDF. 3 A. Okay. There's different numbers. The 4 exhibit page number is four off from the PDF. So 5 which page? I think you want me to turn to page 66 6 of the -- the -- 7 Q. Oh, I'm sorry. I forgot there are two page 8 numbers. I was looking in the bottom right corner. 9 So, yes, 66 in the middle; page 70 in the bottom 10 right. 11 A. Yeah. Okay. I got it. 12 Q. Okay. And this is an annotated figure of 13 Lee of one of -- of figure 3 from Lee that you 14 provide in your declaration, correct? 15 A. That is correct. 16 Q. So I just want to kind of use this to 17 orient -- orient us to -- to what we're talking 18 about here. So just at a high level, can you kind 19 of describe what is presented here and -- and 20 generally what -- what this annotated figure is 21 showing? 22 A. Yeah. In -- what I'm doing here with this 23 figure is mapping the -- the circuitry that's 24 disclosed in Lee onto the claim limitations. And 25 this signal INIT is what I'm saying is -- I'm

Page 10 1 mapping that to the supply voltage stable signal. 2 And the signal RST, R-S-T, is the enable signal. 3 And what's shown in gray is the enable circuit. And 4 what's shown in yellow is the initialization 5 circuit. 6 Q. Okay. And you've got -- I believe you put 7 some orange -- an orange bracket around the inputs 8 to what you've labeled as the "Enable Circuit." 9 There's three different signals there, right? 10 A. On the left you mean, yeah, the command 11 signals. 12 Q. And those signals are, in Lee, DSF, RASB, 13 and CASB, right? 14 A. That is correct. Yeah. 15 Q. So I wanted to ask you some questions about 16 what those signals are precisely. And feel free to 17 reference your declaration or point me to anywhere 18 where you've discussed it if that would be helpful. 19 But let's just start at the top. Well, actually, 20 let's start at the bottom. 21 So what -- what is CASB? And is that how 22 you would refer to it, or call it "CASB," or what 23 would be easiest this morning? 24 A. I would refer to it as CAS. It's -- 25 Q. CAS?	Page 12 1 A. Yeah. So DRAMs have other signals, 2 typically Output Enable, Write Enable, Chip Enable. 3 They sometimes have different names. But those are 4 commonly used in -- in memory -- memory devices as 5 additional control signals. 6 Q. Okay. And, actually, if I could direct you 7 to paragraph 53 of your declaration, which is on 8 page 31 in the bottom right corner, which is 31 of 9 the PDF -- 10 A. Okay. 11 Q. -- or page 27 in the -- in the middle. 12 A. Yes, I see that. 13 Q. Okay. So I'm just looking at this 14 statement. The -- well, let me back up. 15 So at the start of paragraph 53, brief 16 explanation of CAS and RAS and those other 17 additional control signals, such as Chip Select and 18 Write Enable, right? 19 A. Yes, I see that. 20 Q. And then you explain, let's see, "These 21 various input signals are used to perform specific 22 commands by way of a command decoder," et cetera, 23 right? Do you see that? 24 A. Yes. 25 Q. And then "Depending on the combination of
Page 11 1 A. The B is -- stands for "bar," meaning it's 2 low true. But RAS and CAS are commonly used signals 3 in DRAMs. Frequently they're low. They're low 4 active. They're drawn with a bar over them. So 5 what Lee has done is -- which is fairly common, is 6 just labeled it, you know, "CASB," which is -- which 7 is the same as "CAS" with a bar over it, meaning 8 it's low -- it's low active. So I think we could 9 just refer to those as RAS and CAS if you want. 10 Q. Okay. That works. 11 And what is the DSF signal? 12 A. That's a special mode pin that is used on 13 certain DRAMs to enable the activation of certain 14 modes, special modes. 15 Q. And so I believe in your declaration, you 16 refer to these -- these are examples of control 17 signals that are typically provided to a DRAM, 18 right? 19 A. That's correct. 20 Q. And I think you had identified some other 21 ones. There are additional control signals, such as 22 Chip Select, Write Enable. Does that sound right? 23 A. Did I identify those with respect to Lee or 24 in general? I mean -- 25 Q. Just in general for DRAM devices.	Page 13 1 these input signals sent from the memory controller 2 to the DRAM device, a different command is 3 identified and performed," correct? 4 A. Yes. 5 Q. Okay. So -- so signals such as RAS and CAS 6 and -- or DSF, those would be individual signals 7 provided to a DRAM normally, right? 8 A. Yeah. In general those are signals coming 9 in externally to the DRAM. 10 Q. Okay. Those are -- those are examples of 11 signals that come in externally to the DRAM. Got 12 it. 13 And can you kind of walk me through -- 14 again, looking back at your annotated figure of Lee, 15 what does the -- what you have put a box around 16 calling it "Enable Circuit," what does it do with 17 these signals that are provided to the DRAM? 18 A. So there's a circuit -- there's a -- a 19 circuit there. You see the three inputs coming into 20 input buffers. And then there's a circuit that 21 requires a certain sequence, or a certain pattern, 22 if you will, of those signals. And when it gets 23 that pattern, then it -- then SET goes out. Then 24 the output SET is activated and then deactivated. 25 And I think -- there's a timing diagram in

Page 14 1 figure 4. I don't know if it's here. We'd have to 2 pull up Lee. But it illustrates the -- the sequence 3 of -- or the pattern of -- of -- of inputs that 4 causes that to happen. So the purpose of the gray 5 box is to -- or at least the -- box 46 is to detect 6 that sequence on the input signals. 7 Q. Okay. And let me -- since you mentioned 8 Lee and the timing diagram, let me just go ahead and 9 mark Lee for us. If you'll give me a second. 10 (Deposition Exhibit 2 was marked for 11 identification.) 12 BY MR. DeZERN: 13 Q. I've put in the chat what I've marked as 14 Exhibit 2. Let me know when you've got it pulled 15 up, please. 16 A. Okay. I have it. 17 Q. Okay. And if you could flip to figure 4, 18 which I believe is the timing diagram you were just 19 referring to. And let me know when you've got that. 20 A. Yeah, I have that. 21 I've got it. 22 Q. Okay. Thank you. Sorry. I just wanted to 23 make sure I've got it, too. 24 Okay. So with figure 4 pulled up, if you 25 could just kind of explain at a high level what --	Page 16 1 illustrates what Lee calls -- calls the failure 2 mode, or the error, or the case when the supply 3 voltage stable signal doesn't trigger properly. But 4 in the normal operation, that RST signal would be 5 shown as high coming in from the left. And it's 6 the -- it's the -- the ultimate goal of this whole 7 sequence is for the RST signal to go low, which 8 causes the -- releases the circuits out of 9 initialization. 10 So -- so that very last little arrow going 11 down to RST is not actually -- doesn't actually 12 exist in the normal operation, but in the case 13 that -- what Lee calls the -- the failure of the 14 power-up signal to enable properly, then that would 15 cause RST to go high before it goes low. 16 Q. Okay. So let me follow up on -- on some of 17 that to make sure I understand. 18 So if we're looking at figure 4 of Lee -- 19 and correct me if I'm wrong, but if -- if operating 20 normally, then the RST signal, R-S-T -- again, we'll 21 just -- we'll ignore the Greek symbol in front of 22 it. But the RST signal, you're saying, should be 23 high. It should already have been high regardless 24 of the operation of -- of this -- the rest of this 25 timing diagram that we're looking at?
Page 15 1 what's going on in your annotated figure 3 using 2 these RAS, CAS, and DSF signals and reference -- 3 referencing the -- figure 4 of Lee as needed to help 4 me understand what's going on. 5 A. Yeah. So this is showing RAS -- showing 6 CAS going low, and then there's a little arrow that 7 is drawn down to the signal C. I'm just going to 8 call it C. There's a little Greek symbol before it 9 indicating that's a clock signal, PHY symbol. But 10 let's just call it C. 11 So CAS goes down to C. And so this shows 12 the causality here, where CAS goes low, causes C to 13 go high, and that causes this -- the signal called 14 CTL to go high. And then you have RAS going low, 15 which causes R to go high, which then causes the 16 signal MSH to go high; and similarly with DSF. 17 So the top three lines in this figure are 18 the external pins, and everything else are the 19 internal signals. And this is illustrating how this 20 sequence of CAS low, RAS low, with DSF low causes 21 ultimately SET to go high. And the SET signal going 22 high is what will basically hold the RST signal 23 high. 24 Now, one thing to understand about figure 4 25 is that the very last line on this figure is --	Page 17 1 A. Yeah, that's right. And that can be seen 2 by looking at figure 3, because in -- when -- when 3 the INIT -- the INIT signal triggers RST to go high. 4 And everything in figure 4 is what happens after 5 power-on, after the voltage supply signal. 6 So in the normal mode, the INIT signal -- 7 and you can see the INIT signal goes down to this 8 gate 50 if you look at figure 3. And that's a 9 little latch, because there's feedback. So -- so 10 when INIT goes high, then the output goes low, which 11 causes 52 to go high, which then will hold that NOR 12 gate in -- in a high state -- or I mean in a low 13 state, which will cause RST to go high. 14 So in the normal mode of operation, when, 15 you know, the -- the power-up circuit works 16 correctly, then you would see the RST signal high 17 coming in from the left, because -- because you only 18 need the circuit -- you only need 46 to -- to 19 trigger it to go low in the normal mode. But the -- 20 Lee has drawn it this way, I think, to illustrate 21 one of the ideas, which was that even in the case 22 that you have failed -- that the power-up supply 23 circuit has failed, you can still -- 24 (Discussion off the record.) 25 THE WITNESS: I'm sorry.

Page 18 1 -- the power-up circuit has failed, you can 2 still recover -- you can still initialize the 3 device. 4 BY MR. DeZERN: 5 Q. Okay. And let me just clarify one thing. 6 So the -- when the INIT signal from the -- 7 the circuit on top -- which I believe is labeled 16 8 in figure 3 of Lee, right? 9 A. Yes. 10 Q. And I believe you said that's provided to, 11 I think you were talking about the NOR gate 50, 12 correct? 13 A. Correct. 14 Q. And you said that -- that latches the value 15 or -- or that is a latch? I may have missed that. 16 A. This -- this -- the combination of 50 and 17 52 is a latch, a type of latch, because -- because 18 of the feedback. And you can see that because when 19 one side of the NOR gate is high, then the output 20 will go low, and then 50 will cause the other side 21 of the NOR gate to go high, which now means it will 22 be held high, regardless of what the first input 23 does. So what that means is a pulse on INIT, which 24 is what happens if you look at figure 2 -- just a 25 high-going pulse on INIT will cause this thing to	Page 20 1 A. Yes. So -- 2 Q. Yeah. Go ahead. 3 A. Yeah. So, I mean, the -- on the right half 4 of figure 4, you see the sequence that leads to SET 5 going low. And so basically once CAS and RAS are 6 both low, with DSF low, then at some point later CAS 7 will go high. And that's shown with that little 8 arrow. That will cause the internal signal C to go 9 low, which will cause the internal signal CTL to go 10 low, which will cause CR to go high, and then that 11 causes SET to go low, which then causes RST to go 12 low. So that whole sequence of events there will 13 then result in the RST signal going low. 14 Q. Okay. And then -- then what's your 15 understanding of -- what happens when that RST 16 signal goes low? 17 A. Well, that basically releases the -- the 18 circuits from -- the control circuits in the chip 19 from being held in RST. So they're no longer being 20 held, and so they can then operate normally, is 21 essentially what happens. 22 Q. Well, can you point me to where in Lee -- 23 well, first of all, actually, let me back up. 24 So looking at your annotated figure on, 25 again, in the bottom right corner, page 70 of your
Page 19 1 latch high and stay high -- 2 Q. Okay. 3 A. -- because of the feedback. 4 Q. Okay. And so that latch should maintain 5 the value that's provided it from INIT? 6 A. Yeah, until something happens on SET. 7 Q. Okay. And so let's go back, then, to -- 8 well, let's talk about the SET signal, then. So if 9 we're looking at figure 4 of Lee, you first walked 10 through, a moment ago, how the -- the external 11 control signals RAS, CAS, and DSF results in sending 12 SET high, right? 13 A. Right. 14 Q. And that -- that I believe you described as 15 a -- a fail-safe to deal with in case -- in case -- 16 in case RST is not already high from the -- from the 17 INIT operation that we just discussed, right? 18 A. Yeah, that's right. The -- in the normal 19 mode, SET going high doesn't trigger anything, 20 because RST is already high. 21 Q. Okay. And then what I wanted to ask you 22 about -- okay. So then what does -- what does the 23 circuit 46 in figure 3 of Lee -- what does it then 24 do to change that? Can you -- can you walk through 25 the operation of --	Page 21 1 declaration, you've drawn in a control circuit to 2 the right here, correct? 3 A. Yes. 4 Q. Because Lee doesn't explicitly describe any 5 control circuit, correct? 6 A. Well, I think there is explicit disclosure 7 in Lee, in the spec, that describes circuits that I 8 would consider to be control circuits. And that's 9 why I consider Lee to be an anticipatory reference, 10 even outside, you know, the obviousness question or 11 the combination with Iketani. I've drawn it in here 12 because it's not in a figure. But somewhere in 13 here -- I don't know the paragraph -- I quote from 14 the spec where Lee talks about control circuits and 15 functional circuitry, and I think that that would be 16 understood -- especially in the context of power-on 17 reset and what that means, someone of skill in the 18 art would understand that that is control circuitry 19 is -- as that is in the '589, in my opinion. 20 Q. Okay. Can you point me to the places in 21 Lee that you're describing that -- that suggest this 22 control circuitry? 23 A. Yeah. Let me just look at the declaration. 24 MR. KAPADIA: Objection; misstates -- 25 objection; misstates witness testimony.

Page 22 1 THE WITNESS: Okay. In paragraph 129, I 2 have some citations to Lee, and -- so, I mean, we 3 could go back and look at Lee, but, I mean, I think 4 that I've kind of summarized them in paragraph 129, 5 the portions of Lee, at least the most significant 6 ones, that I think disclose a control circuit. 7 BY MR. DeZERN: 8 Q. Okay. So let's start with the first one. 9 I'm looking at paragraph 129. And you've quoted 10 from Lee. Again, in your declaration Exhibit 1005 11 is Lee, correct? 12 A. That's right. 13 Q. And you've quoted: "'An inverter 54'" -- 14 and I won't read the whole thing, but it goes on, 15 "...for sending the reset signal RST to a circuit 16 to be initialized within the chip,'" right? 17 A. That's right. 18 Q. So that's one. Let me look at the next 19 one. 20 And, again, I won't read the whole quote. 21 You're quoting again from column 4, 59 to 62, and at 22 the end of that quote, you know, "thereby 23 initializing the circuits within the chip,'" right? 24 A. Yes. 25 Q. So what's your understanding of what it	Page 24 1 a flip-flop or a latch powers up in an undetermined 2 state. You don't know whether it's a 0 or a 1, for 3 example. So they need to be reset. And the way 4 that works in a power-on environment is that there's 5 a signal that holds them in an uninitialized state 6 until the reset is deasserted, in which case they 7 have been initialized. And once they -- once the 8 initialization signal is deasserted, then they 9 operate the way they're intended. They operate 10 normally. 11 Q. Okay. So when -- when the RST signal in 12 Lee is asserted, that -- that holds these circuits 13 in a particular state? 14 A. Correct. 15 Q. Okay. And now let me ask you, and so in 16 paragraph, when we're talking about the circuitry 17 in figure 3 of Lee, when it operates as you've 18 described and asserts that RST, that initializes 19 the -- that initializes some circuit and holds them 20 in a particular state, right? 21 A. That's right. I think it's -- that would 22 be understood by one of skill in the art as what RST 23 does -- 24 Q. Okay. 25 A. -- given the disclosure of Lee.
Page 23 1 means to -- when Lee says "initializing the 2 circuits" in "the chip"? 3 A. Well, you know, in the context of Lee, 4 which is a semiconductor memory, and what's 5 understood as a power-on reset, what -- I think it's 6 pretty clear to someone of skill that that means 7 circuitry in the chip, for example, sequential 8 circuitry or other circuitry, that needs to be 9 initialized in order to -- for it to operate 10 properly. 11 It's -- I mention in here in the background 12 section it's well known that circuitry with state 13 needs to be initialized. And so I think it's pretty 14 clear that when Lee talks about circuits to be 15 initialized, they mean that there are circuits, and 16 the RST signal will hold them in RST until it goes 17 low, and then they're allowed to operate. And those 18 circuits are circuits in a RAM -- a DRAM or a memory 19 device that control the operation. 20 Q. Okay. Let me unpack that a little bit. 21 So circuits to be -- if I understood 22 correctly, are you saying that for -- for circuits 23 that have state, initializing is to put them in a 24 particular state? 25 A. It's to -- yeah. It -- generally speaking,	Page 25 1 (Discussion off the record.) 2 THE WITNESS: Given the disclosure of Lee. 3 BY MR. DeZERN: 4 Q. Okay. And then looking at figure 3 again, 5 so this RST signal is asserted based on the 6 occurrence of DSF, RAS, and CAS signals, which are 7 externally provided to the DRAM, right? 8 A. No. It's asserted when the power is -- is 9 provided. Right? So in the normal mode, as soon as 10 the power is applied, RST goes high. So it starts 11 out high, essentially, before anything is applied to 12 the chip, in the normal mode. 13 Q. Okay. Yeah. You're -- thank you. So -- 14 so assuming the -- the top circuit and the -- the 15 INIT signal operates as -- as expected or hoped, 16 then RST would already be asserted high, correct? 17 A. Correct. 18 Q. And then in Lee, Lee, in order to provide a 19 solution in case there's a malfunction, it provides 20 this other circuitry which will assert it high -- if 21 it's -- if it's not already, it will assert the RST 22 high based on the external signals, RAS, CAS, and 23 DSF, right? 24 A. That's not exactly correct. The RAS, CAS, 25 and DSF are needed to enable the circuit, period,

Page 26 1 regardless of whether you're in the normal mode or 2 not, because they're needed in order to deassert 3 RST. So -- so when -- in the normal mode, RST 4 starts out high, and then after a sequence of 5 signals on RAS, CAS, and DSF, then it gets 6 deasserted. 7 Q. Okay. 8 A. So it's not just to deal with this failure 9 mode. It's in normal mode as well. You need the 10 external sequence in order to deassert RST. 11 Q. So what do you mean by "normal mode" in 12 this context? 13 A. I'm using the word "normal mode" to mean 14 when the circuit 16 -- or 12, 14, and 16 operate, 15 you know, without an error, you know -- 16 Q. Okay. 17 A. -- sort like figure 2, which is prior art, 18 but it shows these solid lines and these little 19 dotted lines. And the dotted lines indicate a -- 20 what they -- what Lee calls a malfunction, and the 21 solid line is valid operation. So I guess even 22 though this is prior art, that applies to the top 23 half of figure 3. So when I say the normal mode, 24 I'm talking about what he calls "Valid Operation." 25 Q. Okay. And so -- so, then, it needs the --	Page 28 1 RST would go high and then go low, right? 2 A. Yeah. I think what you're asking is, 3 theoretically if a memory controller were applied 4 this initialization sequence at some subsequent 5 time, which in theory it could happen, then, yeah, 6 RST would go high and would -- low -- low again. 7 Q. Okay. 8 A. So -- 9 Q. And you experience it -- oh, I'm sorry. I 10 didn't mean to cut you off. 11 A. No, so, I mean, that would be -- you know, 12 that would be the case if -- if you were to assert 13 the same pattern of signals in the circuit of Lee. 14 Q. And these -- these external signals like 15 RAS and CAS are used in DRAMs for a number of 16 purposes, right? 17 A. Well, yeah. RAS and CAS are used for 18 normal reads and writes to strobe -- I mean, it's a 19 Row Address Strobe and Column Address Strobe, is 20 what the acronym stands for. So it's used to -- to 21 indicate to the DRAM that there's address -- that 22 the address signals are valid. 23 Q. Okay. Yeah, and I think you described 24 generally in your declaration, if I can remind 25 myself -- again, I think this is in column -- I'm
Page 27 1 the application of the external signals, DSF, RAS, 2 and CAS, to -- I forget how you said it -- deassert 3 RST or to drop RST low? 4 A. Yeah, "deassert" is okay; drop it low. 5 Same thing. Yeah. To deassert it. 6 Q. Okay. So thereafter, if -- if the circuit 7 in Lee received those external signals -- again, 8 DSF, RAS, and CAS -- would the same operation play 9 out again; i.e., it would -- it would cause RST to 10 rise and then bring it down again? 11 A. Yeah, theoretically one could do that. I 12 don't think that Lee's concerned with that idea. 13 It's the -- it's just when you're powering up. But 14 in theory one could apply that pattern subsequent 15 to -- I mean, multiple times. But the teaching of 16 Lee is that, you know, this is done at power-up. 17 Q. Okay. So -- well, what would happen in 18 a -- I mean, because we talked at the beginning, the 19 DSF, RAS, and CAS, these are -- are or were 20 common -- common external signals provided to a 21 DRAM, right? 22 A. Yes. 23 Q. So if a DRAM included the circuit described 24 in Lee and it received those signals, RAS, CAS, and 25 DSF, you would expect the behavior to continue where	Page 29 1 sorry, paragraph 53 of your declaration -- what 2 Column Address Strobe -- well, actually, could you 3 kind of elaborate on what -- what precisely CAS, 4 what it should cause a DRAM to do? "DRAM." 5 A. Well, it's used in a number of different 6 ways. So it -- so different patterns on RAS and CAS 7 can cause special, you know, functions: precharge, 8 refresh, and so forth. And so DRAM can look at the 9 pattern of signals and -- and, you know, decode some 10 kind of command. 11 But at a high level, you know, sort of -- 12 just sort of historically, RAS and CAS were used to 13 strobe in the addresses, and hence the name. So 14 DRAMs typically have multiplex addresses so that 15 each pin serves as both a row and a column, so -- to 16 save pins. So you would -- the memory controller 17 would present valid data on the address bus and then 18 assert RAS, and then it would present different data 19 on the same bus and then assert CAS. And then the 20 memory controller would know -- I mean, the DRAM 21 would know what memory cell was being read or 22 written. 23 So they have a function for just regular 24 reads and writes, but they also have other 25 functions. And that's shown in Lee, is that, you

Page 30 1 know, there's this special pattern on RAS and CAS 2 that's used to trigger, you know, the deassertion 3 and RST. So they're used for this additional 4 purpose besides just regular addressing. 5 Q. Okay. So -- if I'm understanding 6 correctly, so CAS and RAS, and -- and potentially 7 other -- other external signals, can be used in 8 different combinations, can be decoded for 9 particular functions; like if you get certain 10 numbers of them, or -- or not numbers, but if you 11 get -- if you get those external signals asserted in 12 a certain way -- HIGH LOW, LOW HIGH, LOW LOW; 13 whatever -- it could instruct the DRAM to perform a 14 different function. Is that the idea? 15 A. Generally, yes, that's -- 16 Q. Okay. 17 A. -- true. 18 Q. And one other thing just in terms of 19 terminology, and I think you provided this in your 20 declaration at paragraph 54, but -- talking about 21 DRAMs and synchronous DRAMs, that CAS can sometimes 22 be referred to as Column Enable, or CE, right? 23 A. Yeah, that's sometimes -- some people refer 24 to it that way. 25 Q. And that's just a naming thing. Those are	Page 32 1 have truth tables, typically, that say what pattern 2 of signals causes various functions to occur. 3 Q. Right. And you provided some examples of 4 those in your declaration, right? We can pull them 5 up if you need to, but just -- if you have a DRAM 6 data sheet, it will have a truth table and say: 7 These external signals in this combination will 8 cause this command. Right? 9 A. That's correct. Basically, yeah. 10 Q. And -- well, we can come back to that in a 11 second. 12 But, yeah, in talking about the '589 13 patent, so the '589 patent specifically talks about 14 these commands, specifically PRECHARGE, AUTOREFRESH, 15 and MODE-REGISTER-SET, right? 16 A. That's right. 17 Q. And so those -- those -- those commands 18 are, like we discussed, based on a particular 19 combination of subsidiary external signals, right? 20 A. Well, I would call them decoded. So 21 there's -- there's signals that come into the chip, 22 which could be considered command signals, and then 23 there's a decoder, and then based on a certain 24 pattern there's decoded command signals. So -- so, 25 for example, AUTOREFRESH is disclosed as being an
Page 31 1 the -- we're talking about the same -- from a 2 functional standpoint, we're talking about the same 3 signal, right? 4 A. Yeah. I mean, there's different standards, 5 different chips. At a high level it's the same 6 thing, basic idea. 7 Q. Okay. Same basic idea. And it's -- again, 8 it's -- it's an -- it's an individual external 9 signal that is provided to the DRAM? 10 A. That's right. 11 Q. And, likewise, RAS might be referred to as 12 Row Enable, or RE? 13 A. Correct. 14 Q. Okay. And I think we just kind of talked 15 about this, but -- but basically the idea is that 16 these external signals like RAS, CAS, or the other 17 ones we mentioned -- I think Chip Select was one -- 18 depending on the combination of signals provided, 19 they could be interpreted as different commands, 20 right? 21 A. Yeah, that's right. So if you look at -- 22 for example, the '589 patent illustrates a command 23 decoder where they illustrate the signals going in, 24 and then there's, if you will, decoded command 25 signals coming out, based on a pattern. And DRAMs	Page 33 1 internal signal, which is based on a pattern, 2 typically of CAS and RAS, that -- that's coming in 3 externally. So there's external signals and there's 4 internal signals. And it has to do with whether 5 they've been decoded, which is essentially the 6 function or the -- described in the truth table. 7 Q. Well, so let's take an example of one of 8 these -- one of the command signals from the '589 9 patent, PRECHARGE. And I think -- oh, I -- I 10 apologize. Let me look at your declaration. I 11 think you may have told us what the subsidiary 12 signals are for that one, if I remember correctly. 13 Or if you recall sitting here -- do you -- 14 A. Yeah, I'd -- 15 Q. -- recall -- 16 A. I'd have to look back at the data sheet. I 17 mean, I think CAS -- hang on. 18 (Deposition Exhibit 3 was marked for 19 identification.) 20 BY MR. DeZERN: 21 Q. Okay. Well, actually, I've got an idea. 22 So hold on one second, and I'm going to mark another 23 exhibit. And this should be Exhibit 3, that I'm 24 about to drop into the chat. Please let me know 25 when you've got it pulled up.

Page 34 1 A. Okay. 2 Q. And it's a big one, so it will take a 3 second. 4 A. Don't see it yet, but -- okay, there it is. 5 Q. Okay. Do you recognize this document that 6 says "JEDEC Standard" at the top? 7 A. One second. I'm still downloading. 8 Okay. I have it. Yes. 9 Q. Okay. And so do you see at the top, this 10 is a -- a JEDEC standard that was also referenced in 11 your declaration. Right? 12 A. That's correct. 13 Q. And it -- specifically it's JEDEC standard 14 number 21-C, Release 7. 15 A. Correct. 16 Q. Okay. So if you can flip to -- it's page 17 479 in the PDF, which is also what it says in the 18 bottom right corner. 19 A. Okay. I'm there. 20 Q. Okay. So this is an SDRAM function truth 21 table, right? 22 A. Yes. 23 Q. And let's just look at the -- to orient 24 ourselves here, looking in the top -- well, let's 25 just look at the top row, the header rows. Right?	Page 36 1 that's what the "S Bar" -- 2 (Discussion off the record.) 3 THE WITNESS: I'm sorry. I apologize for 4 mumbling. 5 I'm looking at the table on page 479. And 6 there's a column labeled "S Bar," as well as "RE" 7 and "CE" and "W Bar." They all have bars over them. 8 So I believe that the "RE" is RAS, the "CE" is CAS, 9 and the "S" is what we sometimes call Chip Select or 10 Chip Enable. 11 BY MR. DeZERN: 12 Q. Okay. Perfect. 13 And then underneath those headings, we have 14 this truth table, which -- well, can you just kind 15 of explain what it shows? 16 A. Yeah. It's -- it's illustrating in -- 17 for -- for each state what happens when the pattern 18 of those signals occurs. So in this case, let's 19 just look at the first line, IDLE. If you're in 20 IDLE and if Chip Select is high, if S Bar is high, 21 then all the other inputs are "don't cares." That's 22 what "X" means. And you stay in the IDLE state. 23 It's -- the action is no-op, meaning nothing 24 happens. So what it's saying is that if you're in 25 the IDLE state and the Chip Select's high, you stay
Page 35 1 So the far left, this is the "CURRENT 2 STATE," right, which I understand to be, whatever 3 state you're currently in, this is what happens when 4 you get the -- the -- the signals that we'll -- in 5 the truth table. Is that -- 6 A. Yeah. 7 Q. -- fair? 8 A. So this is basically sort of like a state 9 diagram. It -- it -- it tells you, from each state, 10 if there's a pattern of signals then there's some 11 action that occurs based on that. And maybe you go 12 to -- to a different state. 13 So it's a -- sort of a combination of a -- 14 I mean, it's really a textual illustration of a 15 state -- a state diagram, what we could call a state 16 diagram. But it illustrates the functions and the 17 patterns that occur with those. 18 Q. Okay. And so in the next column over, 19 there's an S -- I think it's an S bar. I can barely 20 read it, but -- that's like the Chip Select signal 21 we were talking about, right? 22 A. I'd have to look. There's a -- there's a 23 Chip Enable here. Oh, no. Oh. Yeah. So CAS and 24 then RAS -- yeah, that's probably Chip Enable. 25 That's probably -- and writing it. Yeah. I think	Page 37 1 in the IDLE state. Nothing happens. There's no 2 action. 3 And so for each of these lines, it's 4 telling you what the actions are depending on the 5 state you're in and depending on the pattern of 6 signals at the inputs. 7 Q. Okay. So if you look at the -- yeah. And 8 you've got different -- and depending on different 9 LOW HIGH or in some cases "don't care" for those 10 different inputs, you get different actions, right? 11 A. Right. 12 Q. And so those would -- those would be the -- 13 the -- the -- those would be the -- the commands, 14 like PRECHARGE and AUTOREFRESH, that are discussed 15 in the '589 patent, right? 16 A. Yeah. Well, it's a little different. 17 The -- the command -- so it's a pattern of 18 signals -- yeah, I suppose you could call them the 19 commands. Like if you see -- from the IDLE state, 20 you see the line that says "Auto-Refresh," which is 21 LOW LOW LOW HIGH and "don't care." So that's saying 22 that if RAS and CAS are low and Chip Enable's low, 23 then that's what it recognizes as "Auto-Refresh." 24 Now -- let me just look at footnote 5. 25 Okay. So there's some conditions on. But,

Page 38 1 yeah, that's -- that's essentially the illustration 2 of the mapping between the signals -- the input 3 signals and the command, or what they call the 4 action here. 5 Q. Okay. But yeah. So there's -- you pointed 6 to one example, where, again, in the -- in the -- 7 where the current state is IDLE, if we're looking at 8 the -- well, I'll do it. The second -- the second 9 row from the bottom gives us the truth table for 10 Auto-Refresh, right? 11 A. Correct. 12 Q. And that's one -- that's one of the 13 commands that's discussed specifically in the '589 14 patent, right? 15 A. Yes. 16 Q. And it is based on receiving this 17 particular specified combination of external 18 signals, which I think you read off for us, but in 19 order as shown here, it's -- for Chip Select, RAS, 20 CAS, and Write Enable, it's LOW LOW LOW HIGH. And 21 then there's a "don't care." 22 What's the -- what's the "An"? I actually 23 don't know what that is. 24 A. That's the address lines. 25 Q. Address. Ah. Thank you.	Page 40 1 Register -- what they call the Mode Register Access 2 action, it's a -- it's a -- yeah, a pattern on RAS, 3 CAS, SET, and WRITE. 4 Q. Right. So each of these commands requires 5 a specific combination of the external signals, 6 right? 7 A. Of those two, yeah. I mean, you know, this 8 is complicated, and it depends on this -- the timing 9 and also the state you're in. But in that simple 10 example, whether you're in IDLE and you're going to 11 do either Auto-Refresh or Mode Register Access, we 12 see that there's a pattern of signals which will 13 cause those actions. 14 Q. Okay. Yeah. The -- whichever command you 15 have, it's going to be based on a -- a pattern of 16 signals, right? 17 A. Yes. 18 Q. And both of those commands, Auto-Refresh 19 and Mode Register, they require -- as part of the 20 pattern of signals, it includes a RAS and CAS 21 signal, right? 22 A. Yes. They -- they require -- they -- in 23 this case they require those to both be low. 24 Q. Okay. And so the -- the RAS and CAS -- 25 well, let me ask you this: When RAS and CAS are
Page 39 1 A. It's "n" because there's multiple. There's 2 multiple wires. But it's the address lines. 3 Q. Got it. 4 And then the very bottom row -- sorry, 5 bottom row, again, sticking with the IDLE -- that's 6 for the command mode register, right? 7 A. Yes. 8 Q. And it's, similarly, based on a combination 9 of those signals, but it's a -- it's a slightly 10 different combination, right? 11 A. Yeah. It's a slightly different 12 combination, and there's additional information 13 that's provided on the address lines. 14 Q. Okay. So -- 15 A. (Audio dropout) "Op-code." 16 (Discussion off the record.) 17 THE WITNESS: It's referenced as "Op-code." 18 BY MR. DeZERN: 19 Q. Okay. So for Mode Register Access, yeah, 20 it includes additional information from the address 21 line, the opcode, right? 22 A. Yes. 23 Q. But it likewise requires a specific signal 24 for RAS and CAS, right? 25 A. Yeah. In order to activate the Mode	Page 41 1 provided to the DRAM, those can only be evaluated -- 2 only -- well, let me back up. Let me look at it 3 this way. 4 Since -- since -- each command requires a 5 pattern of the external signals, right? 6 A. Okay. 7 Q. So you can only evaluate one command at a 8 time, right? 9 A. I'm not sure what you mean. I mean, 10 there's a -- there's a decoder, typically. And 11 Auto-Refresh and Mode Register Access are -- are 12 distinct actions. So you're doing one or the other, 13 if that's what you mean. But the decoder is looking 14 at all the signals all the time. Right? 15 Q. Right. I -- yes. I think that answers 16 my -- my question. So -- right. The decoder can 17 only decode one -- one command signal at a time, 18 right? 19 A. I'm not sure -- your question is confusing. 20 The decoder is just some logic that is 21 working simultaneously on all signals. I think what 22 you're asking is, would you expect AUTOREFRESH and 23 MODE-REGISTER-SET to be asserted simultaneously. 24 And you -- one wouldn't. One would expect the 25 decoder would say, okay, this is AUTOREFRESH action

Page 42 1 that's occurring; and different pattern would cause 2 MODE-REGISTER-SET action. 3 Q. Yes. I think that -- I think that's right. 4 Yeah. Thank you for clarifying that. 5 And -- and both of those commands require a 6 particular value for RAS and CAS, right? 7 A. Correct. 8 Q. So you couldn't -- you'd -- I guess you'd 9 have to evaluate -- you'd have to evaluate the 10 command -- let me state it this way. And I think 11 this is basically what you just said, but -- you 12 couldn't evaluate a Mode Register Access at the same 13 time while you're evaluating an Auto-Refresh, right? 14 A. Well, I don't understand what you mean by 15 "evaluate." You evaluate everything all the time. 16 It's just that you wouldn't expect to assert -- I 17 mean, this depends on the operation of the decoder, 18 which is internal. But a decoder, which looks at 19 the external signals and asserts an internal signal 20 which says "I'm in AUTOREFRESH" and asserts a 21 different external signal which says "I'm doing a 22 MODE-REGISTER-SET," I wouldn't expect those two 23 signals to be asserted at the same time, because 24 they're distinct actions. But I wouldn't say that 25 they're not evaluating them at the same time. It's	Page 44 1 Q. Okay. And -- and both of those, 2 AUTOREFRESH or MODE-REGISTER-SET, are -- are based 3 on, among other things, how the RAS or CAS is 4 being -- is being provided to the DRAM, right? 5 A. Correct. 6 Q. And there -- well, and let me just make 7 this clear. 8 There's only one -- typically you would 9 expect there's only one RAS/CAS control signal 10 being -- well, let me back up. 11 There's only one of each, RAS or CAS, 12 signal being provided to a DRAM, right? 13 A. That's typically true. 14 Q. And, again, looking at page 479 of what 15 we've marked as Exhibit 3, this JEDEC standard, 16 that -- if you go four rows up in the IDLE state, 17 the "Row (&Bank) active; Latch Row Address," do you 18 see that? 19 A. Yes. 20 Q. Is it your understanding -- is that the 21 same as -- as a Precharge command? 22 A. It's maybe the -- it's maybe related to 23 precharges. The way it's described here is 24 essentially it's the beginning of a -- a read or a 25 write, because you've -- you're capturing the row
Page 43 1 evaluating them all the time, of whether or not 2 you're in AUTOREFRESH, yes or no. 3 Q. Okay. So they would -- well, let me try to 4 say that right. 5 So you wouldn't -- the different commands, 6 you would not expect -- they would not be asserted 7 at the same time, right? You would assert one 8 command and then assert another command, right? 9 A. Typically, yes. But, you know, like I 10 said, it depends on the -- the operation of the 11 decoder. And, you know, this is a spec on what 12 happens external to the chip, and so there's not any 13 detailed, you know, diagram of -- of a decoder and 14 what -- and there's no requirement that there be 15 internal signals. But I guess what I'm saying is, 16 if you had a decoder and the decoder is telling you 17 what action is being taken -- for example, 18 AUTOREFRESH, MODE-REGISTER-SET, or PRECHARGE -- then 19 I would expect those to be distinct, not -- not 20 asserted at the same time. 21 Now, you know, someone could build a 22 decoder that has some weird pattern. But normally 23 one would expect those are distinct phases or 24 distinct periods of time where the internal -- the 25 decoder would assert those signals.	Page 45 1 address. So -- it's not exactly Precharge, 2 because -- it's -- it's what's called Row Active. 3 Now, you would then -- you know, it would -- it 4 would typically subsequently cause a precharge, 5 but -- so I would say it's related to Precharge. 6 Q. Okay. What do you mean, you would 7 subsequently cause a precharge? 8 A. Well, if you look at Row Active in this 9 chart, you see that there's a "Precharge" line 10 there. So I think the way they -- 11 Q. I see. 12 A. -- have described this state diagram is you 13 go from IDLE to Row Active as a state, and then you 14 would precharge before you went to begin READ or 15 begin WRITE. So -- 16 Q. Okay. I see that. 17 But either way, on -- so for that -- that 18 row from the IDLE state, the Row Active that we were 19 looking at, or if you were in the Row Active state 20 if we're looking to precharge, again, that's just 21 another command that's based on a different pattern 22 of external signals, right? 23 A. Correct. 24 Q. And those -- among those external signals 25 are the RAS and CAS signals, right?

Page 46 1 A. Correct. 2 Q. So if we go back to your declaration, page 3 70, your annotated figure 3 from Lee. Do you still 4 have that pulled up? 5 A. Yeah. Yeah, I've got it. 6 Q. Okay. So the -- the external signals that 7 are provided to Lee on this bottom circuit, DSF, 8 RAS, and CAS, that we were discussing, right, 9 those -- as we were just looking and discussing with 10 respect to the JEDEC standard, those are component 11 parts of a command signal, right? They aren't 12 necessarily in and of themselves a command signal? 13 A. Well, no, I think that the -- I'm using the 14 term "command signal" here with respect to the '589. 15 And I think that the way the '589 uses that phrase, 16 it's broad enough to cover both or either, the -- 17 the signals externally or the decoded signals. So I 18 think they're both command signals. The pins are 19 command signals. The internal decoded signals after 20 the decoder are also command signals. 21 Q. Okay. So it's your position that even 22 these individual -- the pin signals, as you're 23 calling them, that those themselves are command 24 signals, right? 25 A. As that term is used in the '589, yes.	Page 48 1 Q. Including RAS and CAS, right? 2 A. Correct. 3 Q. Right. And depending on which -- what the 4 exact combination of those are, you get a different 5 command, right? 6 A. Basically, yes. 7 Q. Okay. Oh, one other question about the -- 8 figure 3 in Lee, in -- we've talked about some of 9 the circuitry, and no need to walk all the way 10 through it, but you see that -- well, let me get 11 the -- in -- it's marked with reference numeral 42, 12 and I believe it's called -- or perhaps you can tell 13 me. But I've written it down, I thought. 14 Oh, yeah. It's a transmission gate, 15 according to Lee. What's your understanding of what 16 that structure is? 17 A. Yeah, that's a special kind of structure 18 that's -- normally a transition -- a transmission 19 gate is a gate that allows for it to flow in both 20 directions. It doesn't have an input/output. It 21 can be -- you know, inputs can occur on both sides. 22 The reason you need a special structure 23 there is just that you have gate -- inverter 52 24 holding SET high, and so you need to overpower it so 25 that it will then reset the NOR gate. So you
Page 47 1 Q. Well, what about -- what's your general 2 understanding? I mean, what's -- what's your 3 opinion on how one of skill in the art would -- 4 would describe these -- these signals such as RAS, 5 CAS, DSF? 6 A. Well, it wouldn't be unusual to describe 7 them as command signals. They're signals that are 8 used to determine what commands to perform. And 9 whether or not they're decoded or not I think is -- 10 you know, they're still signals. And I don't read 11 the '589 claim 1 and 11 to require a decoder. I 12 think that it's broad enough to include the input 13 signals that are used, you know, predecoding or the 14 output of the -- the decoder. 15 Q. Okay. And so predecoding there's multiple 16 signals, that are provided to the pins of the DRAM, 17 right? 18 A. Yeah. And there's multiple signals coming 19 out of the decoder. 20 Q. Right. So -- but so the -- a controller 21 for a DRAM, if it wanted to institute a particular 22 command, it sends several signals to the DRAM, 23 right? 24 A. Well, there's multiple signals, as we've 25 been discussing, yes.	Page 49 1 basically have, you know, two things driving the 2 same wire, so you need to temporarily hold that pin 3 low, so you're fighting against 52, until the output 4 goes high, and then it will -- and then it will stay 5 low. 6 So there's this brief period of time where 7 you need to fight against 52, and then it will -- it 8 will -- the feedback will cause it to be low, and 9 then you're okay. So it basically has to do with 10 electrical properties and needing to have this 11 special kind of override mechanism. 12 Q. Okay. So if we look at the -- the timing 13 diagram of Lee figure 4 again -- if you'll give me a 14 second. 15 Yeah, there it is. 16 Okay. So -- and we -- try not to recover 17 the ground we already covered this morning, but -- 18 in the -- in the scenario shown in figure 4, if -- 19 well, perhaps not exactly. 20 But what we discussed this morning, if 21 the -- if the top power supply voltage sets a INIT 22 signal, gets latched into 56 to hold the RST signal 23 high -- right? If we're in that scenario. 24 A. Correct. Okay. Fine. 25 Q. Okay. So that -- we're in that scenario.

Page 50 1 But the circuit 46 is not yet -- has not yet 2 asserted the SET signal. Okay? 3 A. Okay. 4 Q. Okay. So then what's -- what's the 5 transmission gate 42 doing at that point about? 6 I -- you may have explained, but I just want to 7 understand. In that scenario, what's the -- what's 8 the output at the -- at SET? 9 A. Well, it would depend on the state of this 10 internal MSH signal as to whether the transmission 11 gate is -- is activated or not. So -- so there's 12 other dependencies here. Right? 13 Q. Okay. 14 A. But suffice it to say that -- that inverter 15 52 is going to hold the second input to NOR gate 50 16 in -- high until it gets overridden by circuit 46. 17 And -- and that, you can see in figure 4, is 18 triggered by the CR signal going high. CR going 19 high, and this is with MSH being high, will cause 20 SET to go low, which then causes -- because the 21 other side of NOR gate 50 is also low, that causes 22 it to go high, which causes RST to go low. 23 Q. Okay. 24 A. So the details of that transmission gate 25 relate to -- it's -- it has to do with the fact that	Page 52 1 the claims of the '589 patent based on the position 2 that RAS and CAS are command signals in the sense of 3 the '589 patent? 4 A. Yes. That's -- I think that's accurate. 5 The -- I've mapped the RAS, CAS, and DSF onto the 6 command signals in the claims. And -- 7 Q. Okay. 8 Sorry. I didn't mean to cut you off. Is 9 that -- that it? 10 A. Yeah. 11 Q. Okay. So if -- if those were -- so if 12 those aren't command signals in the sense of the 13 '589 patent, then when -- this -- the operation of 14 this circuit is neither here nor there, right? 15 A. Well, they are command signals. If -- 16 in -- 17 Q. Okay. But if they're not, then -- then you 18 wouldn't say it's -- it's anticipating or rendering 19 obvious the -- the claims, right? 20 A. Well, I probably would say it was obvious. 21 But I haven't looked at that. I mean, in my opinion 22 they are command signals. They're clearly within 23 the scope of the claim. 24 Q. Okay. 25 A. I don't think that having a decoder and
Page 51 1 you've got two -- two outputs being connected 2 together, and in order to make that work 3 electrically with that, essentially. 4 Q. Okay. So -- and correct me if I'm wrong. 5 So in order to make that work, it relies on this MSH 6 signal to -- to properly control the transmission 7 gate; is that fair? 8 A. Yeah. MSH is part of the sequence. It's 9 an internal signal which is part of recognizing the 10 sequence that will then trigger -- trigger SET. 11 Q. Okay. And what is MSH based on in Lee? 12 Like what controls whether it goes high or low, or 13 vice versa? 14 A. Yeah. I have to go back to Lee. It's 15 shown in figure 4 as being based on R going high, 16 but -- but I don't know offhand -- 17 Q. Okay. 18 A. -- where the connection is there. 19 Oh. Yeah. Yeah, it's also shown as going 20 into 32. Yeah, I'd need to -- I need to go back to 21 Lee to -- 22 Q. Okay. No, that's fine. 23 So just to kind of finalize my 24 understanding of your opinions on Lee in this 25 annotated figure here, is your assertion of Lee for	Page 53 1 using decoded inputs would change at least the -- an 2 obviousness analysis, because the -- the claims -- 3 you know, the '589 relates to detecting a sequence 4 on some external pins, and that's exactly what Lee's 5 doing. It's detecting a sequence on external pins. 6 And -- so it would certainly be obvious. But I 7 haven't done an analysis here, because in my view it 8 reads directly on the claims. 9 Q. Okay. Understood. 10 And then, like you described, in your 11 opinion if -- this is identifying a sequence of -- 12 of what you contend are command signals, the result 13 of which being that the Lee circuit will drop this 14 RST signal, right? 15 A. That's right. 16 Q. I mean, that's the -- that's the end goal 17 of the circuit, right, or the end -- the 18 functionality you're trying to get to, right? 19 A. Yeah, the deassertion of the RST signal is 20 what I'm -- what I consider to be the -- the 21 unlatching of the control circuit. 22 Q. Okay. Perfect. So the -- right. So 23 that's your position on latching. And we looked at 24 what Lee -- what Lee actually says about the RST 25 signal, which it describes as initializing those

Page 54 1 circuits, right? 2 A. Well, at least in a couple of instances 3 in -- I -- I cite to in paragraph 129, the -- I 4 think Lee also talks about resetting and holding in 5 initialized state. So I think in the -- it's not 6 just -- Lee discusses it in multiple ways, and so -- 7 not just using the word "initialization." 8 Q. Okay. But -- but the way -- the way Lee -- 9 Lee's description of resetting, holding in 10 initialized state, initializing, that is what you 11 contend meets the unlatching required by the '589 12 patent? 13 A. Well, yes. But there's three levels here 14 in my declaration. There's Lee by itself as an 15 anticipatory reference. And in my view, what you 16 just said is true. The resetting, the -- the 17 initialization, the holding into a reset state is 18 sufficient to one of skill of art to -- to 19 understand that as being unlatching. But I also 20 apply one of three analysis on Lee, and then also 21 combining with Iketani. So to the extent, you know, 22 Iketani adds power-on reset, and also just even 23 without the explicit disclosure in Lee, I think 24 there's also -- it's -- it would be obvious to use 25 the RST signal as a signal which basically releases	Page 56 1 BY MR. DeZERN: 2 Q. All right. Welcome back, Dr. Melvin. Did 3 you speak to anybody during the break? 4 A. No. 5 Q. Okay. So before we broke, we were just 6 talking about your opinions on Lee and the '589's 7 requirement regarding unlatching a control circuit. 8 And just to summarize, I think I understand your 9 position that you think it's in Lee; if it's -- if 10 it's not explicitly then it would be obvious; and 11 then also, as a third position, combined with 12 Iketani, right? 13 A. Yeah. That's -- that's basically what's 14 outlined in my declaration. 15 Q. Yeah. And so I've got your report and -- 16 or, I'm sorry, your declaration and opinion on that. 17 So I get it. And the idea is basically just that 18 you would use the RST signal from Lee as the 19 power-on reset applied to Iketani for whatever it 20 discloses for doing with a power-on reset? 21 A. Well, yes, but it's not just a simple 22 substitution. It's also just the teaching -- 23 combining the teachings. And Iketani is -- is very 24 specific about this power-on reset and what it does. 25 It -- you know, resetting circuitry allows, you
Page 55 1 or allows proper operation, you know, as -- as 2 "unlatching" is used in the -- in the '589. 3 Q. Okay. So I think I understand. I 4 understand that's your position, that it's there in 5 Lee, but if not, then your -- your position is to 6 use that same signal to pause the unlatching for 7 normal operation that's described in the '589 8 patent, right? 9 A. Yes, so as an obviousness analysis or in -- 10 alternatively in combination with Iketani. 11 Q. Okay. And Iketani -- I don't need to 12 belabor that in -- well, give me a second. 13 Actually, I tell you what. We've been 14 going about an hour. Would you -- would now be a 15 good time to take a break? 16 A. Sure. Yeah, that would be great. 17 MR. DeZERN: Yeah. Let's come back in -- 18 let's see. It's 11:52. Let's come back -- 19 THE VIDEOGRAPHER: Let me take us off real 20 quick, Counsel. 21 We are off the record. The time is 9:52 22 a.m. 23 (Recess taken.) 24 THE VIDEOGRAPHER: We are back on the 25 record. The time is 10:07 a.m.	Page 57 1 know, enabling them, you know, to operate properly 2 after power-on. And so I think the combination 3 of -- of Lee and Iketani would be even -- you know, 4 be further clarity that that's what RST could be 5 used for. 6 Q. Well, with regard to that -- and we can 7 reference your -- excuse me -- your declaration as 8 needed. 9 What do you mean about the -- the further 10 details from Iketani about what to do with a 11 power-on reset? 12 A. Well, I think Iketani describes its 13 power-on reset circuit, which is described as, you 14 know, going to these other control circuits, various 15 control circuits within the device. And I think 16 it's clear from Iketani that that's equivalent to or 17 analogous to what the '589 talks about as 18 unlatching. So I think the combination of the 19 teaching of Iketani and Lee, you know, is another 20 basis for understanding that the RST signal in Lee 21 can be used for unlatching. 22 Q. Okay. Well, so if you -- if you jump to 23 paragraph -- let me find it -- 139 in your 24 declaration, that's your "Overview of Iketani." 25 A. Uh-huh.

Page 58 1 Q. And I see, for example, the last sentence 2 of that paragraph, which is actually on the next 3 page: "these circuits...are initialized in response 4 to." You see that, right? 5 A. Yes. 6 Q. And there's a quote from Iketani, which 7 I'll try not to repeat the whole thing, but at 8 column 5, 20 to 26. And I see it explains that in 9 Iketani the power-on reset -- I'm sorry, the reset 10 signal is supplied to, among other things, control 11 circuit, and it says, last sentence of your quote 12 there: "Therefore, these circuits 61 to 64, 56, 57 13 are initialized in response to the power on reset 14 signal," right? 15 A. That's what it says, yes. 16 Q. And I believe that same passage is cited in 17 other places. I mean, you're free to review your 18 declaration as needed, but -- so, again, your 19 position is that -- that this discussion of 20 initialization in Iketani likewise in Lee discloses 21 the claimed unlatching from the '589 patent, right? 22 A. Well, it describes the function of 23 unlatching. And it's not just, you know, that 24 sentence; it's also the fact that it's a power-on 25 reset. And -- and it's understood -- it's well	Page 60 1 power-on reset? 2 A. Well, that's close. I mean, basically 3 it's -- it's -- it's well known. Power-on reset 4 circuits are well known. And what they do is they 5 initialize circuits, and they also have a delay 6 associated with power -- with power supply reaching 7 a voltage. And so they -- they hold circuits in a 8 reset state until it's safe to release them, and 9 then they do. So it's -- it accomplishes a reset 10 and a release when power's applied. 11 Q. Reset and release when power's applied. 12 Okay. And then I suppose it's -- it's important 13 that once they've reset the circuit and released it, 14 then that's it; they -- they won't interfere with 15 operation anymore, right? 16 A. In, you know, typical -- typically 17 speaking, that -- it's only used on power-up. 18 Q. Okay. But -- yeah, but the idea being that 19 after that, you wouldn't want it to interfere with 20 normal operation, right? 21 A. Normally that would be the typical use of 22 the power-on reset. 23 Q. Okay. All right. Dr. Melvin, just a 24 couple other questions about your declaration and 25 its creation.
Page 59 1 understood by those of skill in the art what 2 power-on reset means. It's the circuit that 3 maintains a level on a signal until voltage supply 4 reaches a point, and then it's deasserted. And 5 that's what's described in -- in the background 6 section of -- of the '589, is that there's a 7 power-on signal that, once it's deasserted, is -- or 8 asserted, as the case may be, then it allows 9 circuits to then operate properly. 10 So it's a combination of what's understood 11 by "power-on reset," what's taught by Iketani, and 12 in comparison to what's described in the '589. 13 Q. Okay. So -- so your position is partially 14 based on what -- what your position is that one of 15 skill in the art would understand a power-on reset 16 circuit to do, right? 17 A. Yeah. I think -- it's partially based on, 18 yeah, that description in Iketani, and describing 19 that as power-on reset, in addition to, you know, 20 what it says it does. 21 Q. Okay. And I believe you just said -- so 22 the idea of a power-on reset circuit is that it will 23 maintain a signal until -- for a certain point until 24 it's deasserted, and then it's ready for normal 25 operation. Is that your basic understanding of the	Page 61 1 I believe you state that you created this 2 declaration at your normal hourly rate. What is 3 your normal hourly rate for -- for work -- for -- 4 well, for this work in particular? 5 A. Well, my -- my current hourly rate through 6 my current consulting company is \$600 an hour. 7 Q. Okay. 8 A. But I prepared -- just to clarify, I -- I 9 prepared this report when I was employed at Exponent 10 Inc., and so some of the work on this project was 11 done through Exponent and some was done through my 12 current company. And I believe that the rate at 13 Exponent was 650. So some is at 650; some is at 14 600. 15 Q. Okay. Understood. And do you know 16 approximately how much you billed Xilinx just to 17 create this declaration? 18 A. Well, I worked on two IPRs, and I didn't -- 19 I don't think I segregated the time. It was 20 probably like 50 to a hundred hours, I'm 21 approximating, for both, for both the -- 22 Q. 50 -- oh, 50 to a hundred for two IPR 23 declarations? 24 A. Yeah, I believe so. I think it's in that 25 ballpark.

Page 62 1 Q. Well, I think I can look it up. But I 2 presume that's -- you're referring to one of the 3 other IPRs for Xilinx on a different Polaris patent, 4 right? 5 A. That's correct. '473. 6 Q. Ah. Okay. Yes. '473. 7 Are you working on any other matters for 8 Xilinx other than this IPR? I guess the other IPR's 9 done. But anything else? 10 A. Not for Xilinx, no. 11 MR. DeZERN: All right. Well, I don't have 12 any further questions, so I'll pass the witness, 13 Aashish. 14 MR. KAPADIA: Can we take a quick break? 15 MR. DeZERN: Sure. 16 THE VIDEOGRAPHER: We are off the record. 17 The time is 10:17 p.m. 18 (Recess taken.) 19 THE VIDEOGRAPHER: We are back on the 20 record. The time is 10:30 a.m. 21 MR. KAPADIA: Thank you. 22 I do not think we have any further 23 questions, so that will be it. 24 MR. DeZERN: All right. 25 THE VIDEOGRAPHER: Off record, Counsel?	Page 64 1 CERTIFICATE OF REPORTER 2 3 I, JOHN WISSENBACH, hereby certify that the 4 witness in the foregoing deposition was by me duly 5 sworn to testify the truth, the whole truth, and 6 nothing but the truth in the within-entitled cause; 7 that said deposition was taken at the time and place 8 therein stated; that the testimony of said witness 9 was reported by me, a Certified Shorthand Reporter 10 and disinterested person, and was thereafter 11 transcribed into typewriting, that the pertinent 12 provisions of the applicable code or rules of civil 13 procedure relating to the notification of the 14 witness and counsel for the parties hereto of the 15 availability of the original transcript of the 16 deposition for reading, correcting, and signing have 17 been met, and that the transcript is a true record 18 of the testimony given. 19 And I further certify that I am not of 20 counsel or attorney for either or any of the parties 21 to said deposition, nor in any way interested in the 22 outcome of the cause named in said caption. 23 DATED: November 27, 2023 24 25  JOHN WISSENBACH, CSR No. 6862
Page 63 1 MR. DeZERN: Yes. 2 THE VIDEOGRAPHER: We are off the record. 3 The time is 2:30 a.m. 4 (Whereupon, the deposition session ended at 5 10:30 a.m.) 6 ---o0o--- 7 8 9 10 I declare under penalty of perjury that the 11 foregoing is true and correct. Subscribed at 12 _____, California, this ____ day of 13 _____, 2023. 14 15 _____ 16 Signature of the witness 17 18 19 20 21 22 23 24 25	